NEMS by Sidewall Transfer Lithography

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Abstract - A batch fabrication process for nano-electro-mechanical systems (NEMS) based on sidewall transfer lithography (STL) is demonstrated. STL is used to form nanoscale flexible silicon suspensions entirely by conventional photolithography. A two-step process for combining microscale and nanoscale features is used to fabricate double-ended and single-ended electrothermal actuators with a minimum feature width of 100 nm and an aspect ratio of 40 : 1. All devices are fabricated by deep reactive ion etching in 4.5 μm thick silicon using bonded silicon-on-insulator material. The process could allow low cost fabrication of nanoscale sensors and actuators.

***Index Terms*—Nanoelectromechanical systems, NEMS, sidewall transfer lithography, STL**

I. Introduction

Nanoelectromechanical systems (NEMS) have a variety of applications. In sensing, these include ultra-sensitive detection of inertial mass [1], electric force [2] and chemical and biochemical species [3, 4], and probe microscopy [5, 6]. Accompanying miniaturization is a reduction in the mass, stiffness, thermal capacity and thermal conductance of flexible elements. For example, scaling the thickness of a beam from 1 μm to 100 nm will result in a thousand-fold reduction in stiffness. Other scaling laws may be calculated similarly. Expected benefits include an increase in sensitivity to mass and a reduction in sensitivity to shock in sensors, an increase in resonant frequency in signal processing devices [7], and reduction in drive power in actuators [8-10]. For example, attogram mass sensitivity has been demonstrated using NEMS cantilevers, limited mainly by noise in the displacement transducer [1]. Similarly, quality factors of 2 x10^4 have been measured under high vacuum, using built-in NEMS beams operating at 70 MHz [7].

Out-of-plane NEMS may of course be fabricated using thin deposited layers, patterned using optical lithography. However, reduced pattern dimensions are required in NEMS designed for in-plane motion. Conventionally, fabrication requires a nanoscale patterning method such as electron beam lithography [8]. Replication methods such as nanoimprint or soft lithography still typically require a nanostructured master. However, considerable advantages would follow from the development of low-cost, parallel alternatives that can yield nanoscale features directly over a large area.

One possibility is sidewall transfer lithography (STL), also known as size reduction lithography, and spacer- or edge-defined lithography. STL is based on the transformation of thin layers deposited on mesas into nanoscale ribs [11-17], slots [18-21] and vertically stacked multilayers [22-24]. It was originally developed for CMOS applications [25], and processes for FinFET fabrication have received increasing attention in recent years with the drive towards strongly sub-micron channels [26-32]. STL has also been applied to nanowire arrays in various materials including silicon, diamond, platinum, platinum silicide and nickel silicide, with applications ranging from sensing to catalytic surfaces [33-38]. Further applications include field emission electrodes [39, 40] and quantum dots [41-43]. Silicon stamps for nanoimprint lithography have also been extensively explored [44-51].

STL has received limited attention in more general 3D micromachining. The only applications we are aware of are nanoscale needles [52] and channels [53]. However, STL may have considerable potential as a low-cost method of defining nanoscale mechanisms. We have already used STL to construct elementary suspended structures in bulk Si [54]. Here we demonstrate in-plane electrothermal actuators in bonded silicon-on-insulator (BSOI), using a combination of STL, deep silicon etching and vapor undercut. The process is outlined in Section II, actuator designs are introduced in Section III, experimental results and a theoretical model are presented in sections IV and V, process issues and geometric constraints are discussed in Sections VI and VII, and conclusions are drawn in Section VIII.

II. STL NEMS Process

The sidewall transfer NEMS process presented here uses optical lithography to combine microscale parts with a limited subset of nanoscale features. Particularly, STL is used to form thin, flexible beams that may (for example) allow a reduction in suspension stiffness. Sidewall materials are used as surface masks, reducing the in-plane width of silicon features formed by deep reactive ion etching (DRIE) well below the resolution of the optical patterning system. The main requirements of the mask materials are a) low intrinsic stress, b) good adhesion, and c) ease of removal. Here, we have used sputtered metals. We have also investigated thermal oxide; this has good adhesion but high intrinsic stress. However, low-stress methods of silica deposition such as plasma enhanced chemical vapor deposition would be suitable. Similarly, the main requirements in deep etching are low lateral erosion and high sidewall verticality. Here we have used the Bosch DRIE process, but cryogenic etching could also be used.

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Fig.1 shows a STL process for BSOI NEMS. Conventional lithography is first used to pattern the device layer, using an optical resist and a mask that defines the nanoscale features (1). DRIE is then used to transfer the pattern into the silicon as a set of shallow mesas (2), and the resist is stripped (3). RF sputtering is then used to coat the mesas with a conformal layer of metal (4). Directional etching is then used to remove the horizontal metal surfaces, leaving the vertical surfaces in place (5). The remaining vertical features have a width defined by the original coating thickness rather than by optical lithography, but are spaced by the mesa width. A second lithography step is then used to pattern the structure once more, using a mask that defines all the microscale features (6). DRIE is then used to transfer the pattern into the silicon device layer (7), and the resist is stripped (8). HF vapor undercut (9) is then used to remove the oxide interlayer, releasing nanoscale parts of the type labeled A (which can then act as flexible suspensions) while larger parts B remain as anchors. Finally, aluminium metallization of the entire structure (10) is used to improve electrical contact.

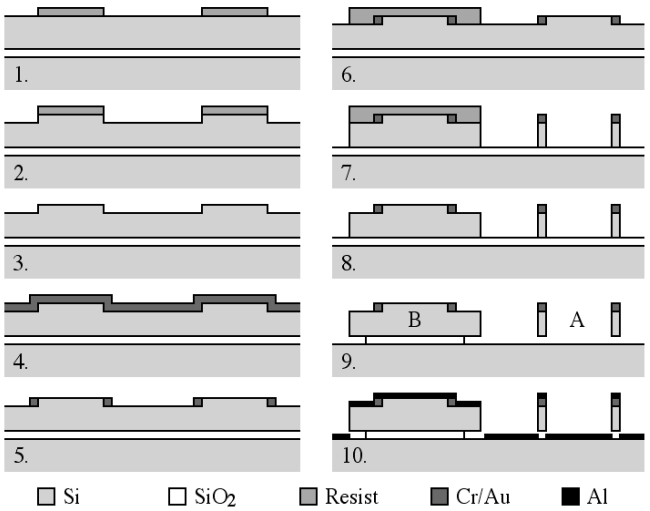

Fig.1. Process flow for BSOI NEMS: 1) coat resist, and pattern with Mask 1, 2) DRIE to form mesas, 3) strip resist, 4) sputter coat Cr/Au, 5) sputter-etch Cr/Au, 6) spin coat resist and pattern with Mask 2, 7) strip resist, 8) DRIE to oxide interlayer, 9) HF vapour undercut, 10) metallize.

As shown in Fig. 2, patterning can be divided into two steps. In the first, the perimeters of a set of patterns on Mask 1 are used to outline all the nanoscale features. In the second, the actual patterns on Mask 2 are used to define all microscale features. However, neither set exists as mechanical parts until they are transferred into the silicon by the final DRIE step.

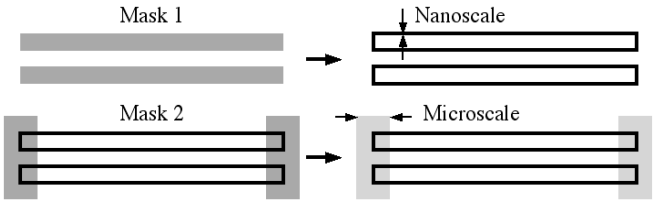

Fig.2. Sidewall NEMS patterning steps.

The ends of the polygons defining the nanoscale features are buried in the microscale ones, and hence are eliminated from the overall pattern. Other deposition and lithography steps may be inserted into the process, e.g. to define regions of doped silicon or provide separate metal contact pads.

III. NEMS Actuator Designs

To demonstrate the process, two well-known electrothermal microactuator designs were adapted as NEMS as shown in Fig. 3. The geometries were chosen to highlight different aspects of processing, particularly the effects of stress.

Fig. 3a shows a double-ended buckling or V-beam actuator [55, 56]. Here Mask 1 defines the suspension, now fabricated as a set of parallel nanoscale beams, while Mask 2 defines anchors at either end, and a central crossbeam to tie the nanoscale beams together. Differential thermal expansion with a pre-buckled beam causes in-plane motion when a heater current is passed between the anchors. The beams (which here all act as hot arms) have chevron shapes, so that quasi-linear motion arises in the direction shown. The crossbeam forces collective deflection of the entire array and minimizes the occurrence of higher-order buckling modes.

Fig. 3b shows a single-ended or folded V-beam actuator [57, 58]. Here, the beam array is divided into sets of cold and hot arms tied by a crossbeam at the free end, and the anchors are subdivided so that a current may be passed only through the hot arms, leaving the cold arms as tethers that constrain longitudinal expansion. In-plane motion is again forced by differential thermal expansion, in the direction shown.

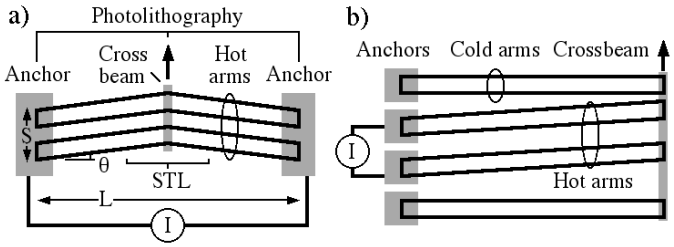

Fig.3 a) Double- and b) single-ended electrothermal NEMS actuators.

Designs were based on previous experience with electrothermal microactuators [57]. A total beam length L = 1 mm was used for both devices, with a range of suspension separations (30, 20, 10, 5 and 2 μm). Use of a large span S = 640 μm allowed hot arms to be used in much larger numbers than shown in Fig. 3 (22 for 30 μm separations, 58 for 10 μm and 282 for 2 μm). However, cold arms were arranged in pairs as shown. In each case the hot arm slope angle was θ = 0.01 rad, and crossbeam widths were 2 μm. Devices were designed for fabrication as 100 nm wide beams in 4 μm thick layers, so that the ratio of out-of-plane to in-plane stiffness of a single beam was 64,000 : 1. Devices were arranged in blocks of die variants, with 2420 dies in a 100 mm diameter wafer.

IV. Experimental Results

Demonstrator devices were fabricated in 100 mm diameter bonded silicon-on-insulator wafers, obtained commercially from Icemos Technology, Belfast, with a 2 μm thick buried oxide layer and a 4.5 μm thick device layer.

The initial photoresist pattern defining the suspension was

formed using mid-UV contact optical lithography, based on 0.45 μm thickness of Shipley S18105 resist. The wafer was then etched to form 0.5 μm high Si mesas using a Surface Technology Systems inductively coupled Single-chamber Multiplex DRIE system operating a cyclic process based on etching with SF_6 and O_2 and passivation with C_4F_8. This depth was chosen so that the height of the sidewall mask was significantly (8x) less than the thickness of the resulting Si suspension (4 μm), to minimize deformation due to residual stress. The resist was then stripped.

Sputter-deposition with a Nordiko RF sputtering system was used for deposition of sidewall materials, since this is a low-temperature process that can be used for conformal deposition of many metals and dielectrics with low intrinsic stress. After considering various alternatives, gold was chosen as the lowest-stress material available, deposited as a 100 nm thick layer. However, Au typically requires an additional chrome adhesion layer, which has higher stress. A very thin (10 nm) Cr layer was used, leading to a bilayer sidewall mask with an overall thickness of 110 nm. Horizontal surfaces of this layer were etched using RF sputtering in Ar plasma, at 100 W RF power and 1.5 x 10^{-2} mbar pressure. Residual Cr specks were cleared by wet etching, leaving the vertical sidewall masks attached to the silicon mesas.

The second pattern defining the anchors and crossbeams was then formed using optical lithography. This time, a thicker resist (1.5 μm thickness of Shipley S1813) was used, to planarize the 0.5 μm high steps at mesas. The combined pattern was then transferred down to the buried oxide layer by DRIE, and the resist was stripped in oxygen plasma.

The Bosch process is well understood. Despite this, care is required to form high-aspect ratio nanostructures, since there is little margin for lateral error. DRIE parameters were chosen to avoid grass formation and to ensure that the scallops inherent in cyclic etching did not erode the nanoscale features (which will occur when their depth rises above 50 nm). For example, Fig. 4 shows the variation of scallop depth with the duration of the etch step, for two different RF powers (350 W and 600 W). These data were extracted from scanning electron microscope (SEM) photographs, assuming a semicircular scallop profile (in practice, an overestimate).

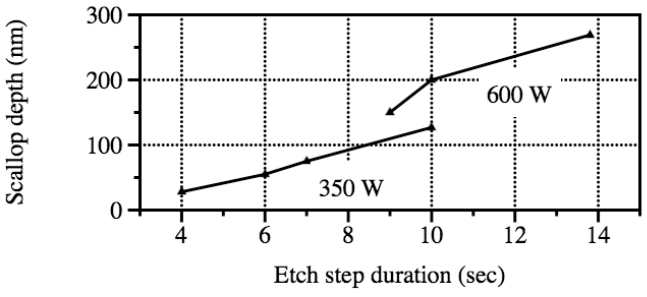

Fig. 4 Variation of scallop depth with etch step duration, at different RF powers.

In each case, the duration of the passivation step was equal to that of the etch step. Gas flow rates were 50 sccm (SF_6), 5 sccm (O_2) and 70 sccm (C_4F_8) at 350 W power, and 130 sccm (SF_6), 13 sccm (O_2) and 110 sccm (C_4F_8) at 600 W. Pressures were 7.4 mTorr (etch), 7.6 mTorr (passivation) at 350 W power, and 20 mTorr (etch), 15 mTorr (passivation) at 600 W. Scallop depths clearly reduce with RF power and etch step duration, and only the lowest values yield depths compatible with nanoscale structuring.

The DRIE schedule was then adjusted to achieve the correct depth. For example, Fig. 5a shows the variation of the etch depth with the number of etch cycles, for 4-second cycles at 350 W RF power. Etching is clearly linear, and 4 μm depth is achieved after 52 cycles. However, over-etching is required to remove the 0.5 μm of additional silicon in the mesa regions, and to compensate for variations in device layer thickness; 60 cycles were therefore used in the final recipe. Because of the RF low power, it was not necessary to use low-frequency plasma to stop on the oxide interlayer.

The schedule was then adjusted further to control the beam profile. Trace A in Fig. 5b shows the variation of beam width with depth, for a schedule with excessive passivation. The beam width clearly increases significantly with depth (to almost 300 nm) starting from an initial value (150 nm) that is also too large due to excessive scalloping of the mesa. Trace B shows the variation that can be achieved with an optimized schedule; here the beam width is close to 100 nm throughout.

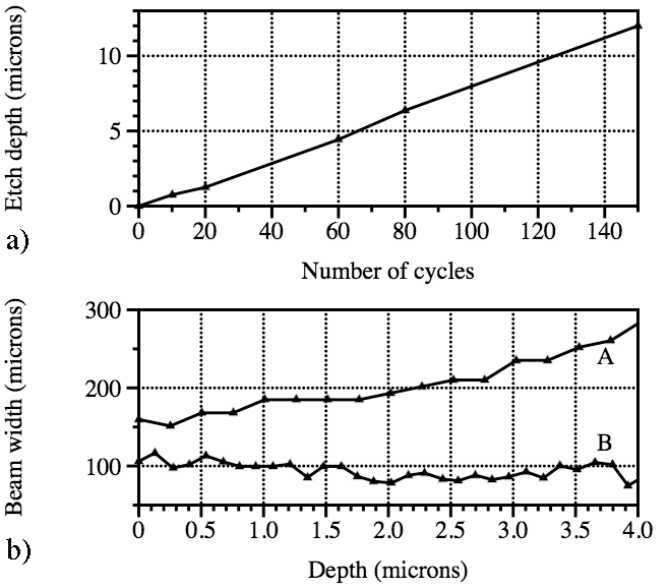

Fig. 5 Variation of a) etch depth with number of etching cycles, and b) beam width with depth, for different process schedules.

The Cr/Au sidewall mask can in principle be removed, by wet chemical etching first in potassium iodide and then in ceric ammonium nitrate. However, for reasons that will become clear, the sidewall mask was left in place. Suspended parts were released using HF vapor phase etching in an Idonus VPE system, for a time sufficient to remove the 2 μm thick buried oxide layer. Finally, the structure was metallized by evaporation of 40 nm Al metal.

Fig. 6 shows structures at different steps through processing. Fig. 6a shows a SEM photograph obtained by cleaving across a mesa after sputter coating and etching horizontal metal surfaces (Step 5 in Fig. 2). The combination of conformal coating and ion bombardment during sputter

etching is responsible for the rounded mesa corner. These effects in turn form a chisel-shaped apex in the sidewall mask, which is unimportant in the final pattern transfer.

Fig. 6b shows a similar SEM view obtained before completion of deep silicon etching (between Steps 6 and 7) of a device with 5 μm suspension separation. The location of the original mesa structures may be identified as the higher of the two horizontal Si surfaces, which are enclosed on either side by vertical Si sheets that form the nanoscale suspension.

Fig. 6c shows a similar structure obtained by cleaving across the suspension of a fully etched but unreleased device (Step 8). The sidewall mask (enlarged in the inset) is still in place, and the Si etching has followed the width at its base. The etch has now bottomed on the oxide interlayer, and a nanoscale beam with a high (40 : 1) aspect ratio has been formed with only minor variations in thickness. There are however significant vertical striations; these are typical of the results obtained using mid-UV contact lithography.

The adhesion of the metal is excellent, and some effort is required to detach it. Fig. 6d shows a similar specimen, where cleaving has resulted in a section of the nanoscale Si beam becoming detached without breaking the sidewall mask or separating it from the silicon. This figure shows the rear of the mask; it is highly vertical, and details such as the original scalloping of the mesa may be seen.

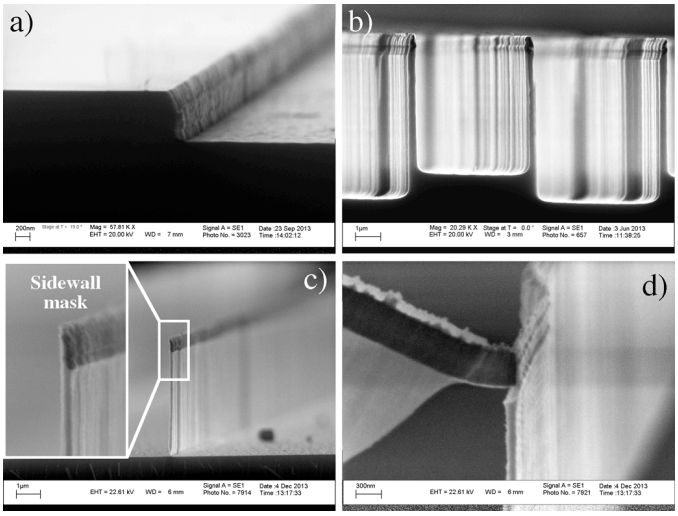

Fig. 6 SEM views of a) mesa with sidewall mask in place; b) and c) partly and fully etched suspension beams, and d) broken suspension beam.

Fig. 7 shows SEM views of completed devices. Fig. 7a shows a double-ended electrothermal actuator with 10 μm beam separation, which contains 58 unbroken nanoscale beams. Fig. 7b shows a close-up of the central crossbeam. The nanoscale and microscale beams have clearly been released from the sacrificial oxide interlayer and are suspended above the Si substrate. The suspension beams have near-vertical walls, with little sign of twisting or lateral deflection caused by residual stress in the sidewall mask.

Of course, devices with suspensions that are built in at both ends might be expected to show limited stress distortion. For comparison, Figs. 7c and 7d show close-up views of a single-ended electrothermal actuator near the anchors and crossbeam, respectively. These structures have similar high quality. Robust mechanical joints are formed between the nano- and micro-scale features, and the anchors are undercut to eliminate a tracking path to the substrate for metallisation. The structure has been entirely released without noticeable deformation.

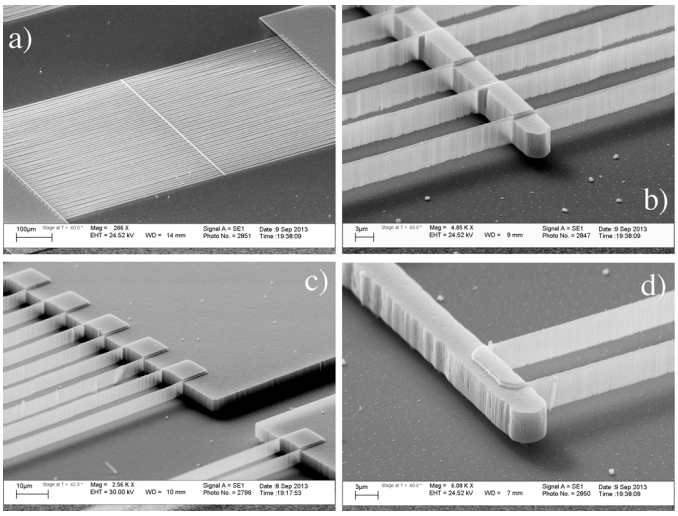

Fig. 7 SEM views of a), b) double-ended actuator, overall and near the crossbeam; c), d) single-ended actuator, near the anchors and crossbeam.

Fig. 8 shows surface profiles of a double-ended actuator with 10 μm beam separation after HF vapor phase undercut, measured using a Veeco NT 3300 white light interferometric profilometer. The suspension dimensions are clearly below the resolution of the imaging system, but there is sufficient reflection to delineate the complete structure.

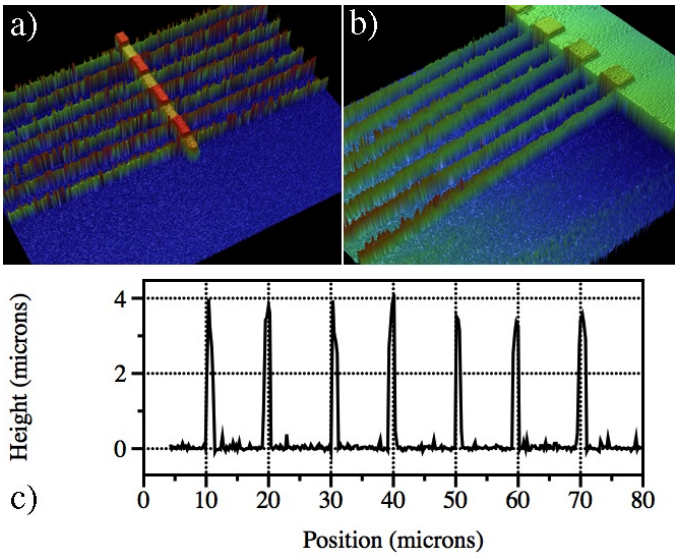

Fig. 8 Optical surface profiles of double-ended actuators showing a) crossbeams, b) anchors and c) beam spacing.

Fig. 8a shows a 3D reconstruction near the central crossbeam, which is formed together with the anchors and suspension in the final DRIE step. The stepped surface of the crossbeam follows from the mesas used to define the sidewall. This effect could be eliminated, by using a separate sacrificial layer such as silica to form the mesas. Fig. 8b shows a view of the anchors, which have a similar terracing. Fig. 8c shows a line profile extracted from Fig. 8a; although the width of the

nanoscale beams is clearly incorrect, their spacing is regular.

Electromechanical performance was difficult to quantify, because of the very small feature size, the transparency of the nanoscale beams and the small displacement. Electrical contact was made using probe tips attached to 3-axis micromanipulators and a DC current was passed between the anchors. Static performance was characterized with the optical profilometer, using image analysis software to extract the difference between the thermally relaxed and distorted states of multiple suspension beams. The points in Fig. 9a show the variation of deflection with drive power for two different double-ended devices with 58 beams 10 μm apart, which follows the quasi-linear characteristic of a chevron actuator [56]. Very low powers (calculated from the drive voltage and the device resistance) are needed to achieve useful displacements. For example, a displacement of ~ 5 μm is achieved at a power of 25 mW, corresponding to 0.43 mW per beam. By comparison, single-beam MEMS actuators in [56] required around 180 mW to achieve a similar displacement.

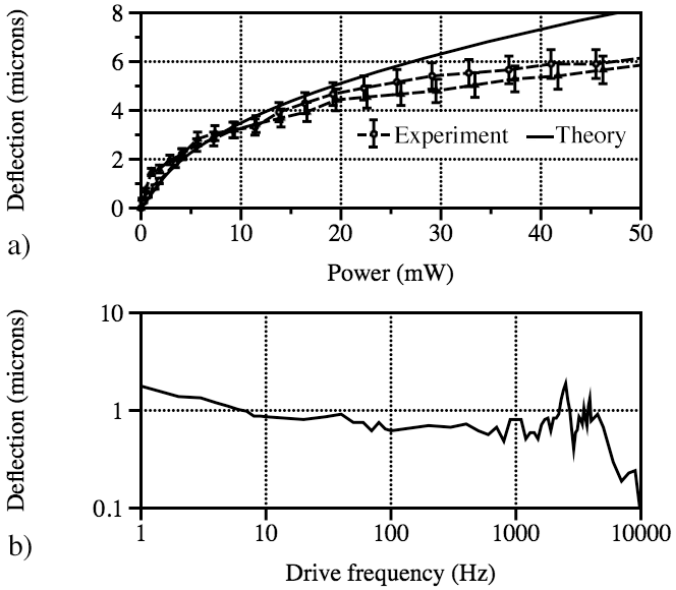

Fig. 9. Variation of deflection with a) power and b) frequency, for double-ended actuators.

Dynamic performance was established using a sinusoidal drive; as with all electrothermal actuators, the mechanical response was at twice the driving frequency. Several methods were used to measure the frequency response, including conventional and confocal microscopy and measurement of the scattering from a moving device. Similar results were obtained in each case. Fig. 9b shows the frequency variation of deflection. There is some evidence of resonance at ~ 3 kHz; however, it was difficult to establish whether this followed from collective resonance or uncorrelated vibration of individual beams. Roll-off of the electrothermal transducer then appears to occur at almost the same frequency. Motion was clearly visible using dark field microscopy (Fig. 10); however further work is required to improve metrology.

Single-ended actuators could also be driven, but their behaviour was generally much less predictable due to the effects of stress-induced distortion, which acts to alter the pre-buckled state. For example, some devices moved in the opposite direction to that shown in Fig. 3b.

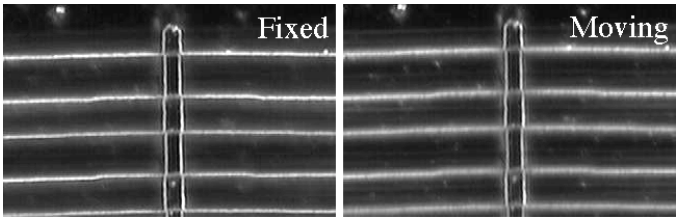

Fig. 10. Dark-field microscope views of fixed and moving actuators.

V. Theoretical Model

Problems with meshing make it difficult to model long, thin beams accurately with finite-element analysis. Here we use the simple analytic model for an electrothermal actuator in [56]. Solving the Euler equation for a single chevron beam with width W, depth D, slope angle θ and length L loaded by a compressive force F yields the midpoint deflection d as:

$$d = (2/k)\tan(\theta)\,(G - kL/4) \tag{1}$$

Here $kL = \sqrt{(F/EI)}$, E is Young's modulus, $I = DW^3/12$ is the second moment of area and $G = \tan(kL/4)$. From the deflected beam shape, the fractional extension $\Delta L/L$ can be found as:

$$\Delta L/L = \tan^2(\theta)\,\{(1 - G^2)\,(S - kL) + 2G(1 - C)\}/4kL \tag{2}$$

Here $S = \sin(kL)$ and $C = \cos(kL)$. The force F_{y1} exerted by the actuator can be estimated from the transverse force needed to eliminate the deflection, which for small d yields:

$$F_{y1} = d\,K_{y1} \text{ where } K_{y1} \approx 4EWD\sin^2(\theta)/\mathrm{L} \tag{3}$$

Since F arises from constrained thermal expansion, the average temperature rise ΔT_{avg} can be estimated from the compatibility condition:

$$\Delta T_{avg} = (F/EWD + \Delta L/L + \sigma_{int}/E)/\alpha \tag{4}$$

Here α is the expansion coefficient, and we have added an additional term σ_{int} representing intrinsic stress. For cooling by solid conduction, ΔT_{avg} can be related to the drive power P_1 by solving the heat conduction equation to get:

$$P_1 = \Delta T_{avg}(12k_{th}WD/L) \tag{5}$$

Here k_{th} is the thermal conductivity of the beam material. Assuming additional convection cooling, the result increases by a factor β that must typically be estimated. The drive power and force of an N-beam actuator are then $P_N = \beta N P_1$ and $F_{yN} = NF_{y1}$. Eqns. 1-4 may be evaluated as a function of F, allowing d and F_y to be related to ΔT_{avg}; Eqn. 5 then allows d and F_{yN} to be related to P_N. The formulae are valid even when $F < 0$, although care must be used since k becomes imaginary.

To compare with experiments, we have assumed $N = 58$, $W = 100$ μm, $D = 4$ μm, $L = 1$ mm, $\theta = 0.01$ rad and $E = 170 \times 10^9$ N m^{-2}, $\alpha = 2.6 \times 10^{-6}$ K^{-1} and $k_{th} = 130$ W m^{-1} K^{-1} (for Si). Setting σ_{int} to zero and β to 1, poor agreement is obtained with the data in Fig. 9a. Much better agreement is obtained when these parameters are adjusted, and the full line shows results

for σ_{int} = 8 x 10^6 N/m^2 and β = 22. The need for large fitting parameters implies that intrinsic stress and convection cooling dominate performance. Neither is unexpected; the presence of residual sidewall material is responsible for the former, while the increase in the ratio between the area $2(W + D)L$ available for convection cooling to the area WD available for conduction cooling is responsible for the latter.

Stress and size scaling affect other aspects of performance. Because the beam is so thin, the resonant frequency is dominated by stress to the extent that predictions become inaccurate in the absence of independent knowledge of σ_{int}. Residual stress and increased convection cooling also affect the force F_{y1}, since they reduce the deflection d at a given power. However, assuming similar beam angles θ, similar beam lengths and depths L and D and similar (μm-scale) displacements as a MEMS actuator, Eqn. 3 implies that F_{y1} is proportional to W. A reduction in W of at least a factor of 10 (as here) will then reduce the force per beam by a similar factor. NEMS actuators will therefore be low-force devices.

VI. Processing Issues

The main difficulty with the sidewall mask is to avoid intrinsic stress. The existence and nature of such stress can be revealed using alternative processing that effectively forms gauges for the sidewall stress, as we now show. For example, Fig. 11a shows the mask for a double-ended actuator, which has been deliberately undercut by isotropic etching in SF_6 to remove the Si beneath and leave the mask as a freestanding metal structure. Suspended metal beams from either side of the same mesa have clearly bunched together, indicating differential stress between the Cr and Au in the vertical parts of the bilayer metal sidewall.

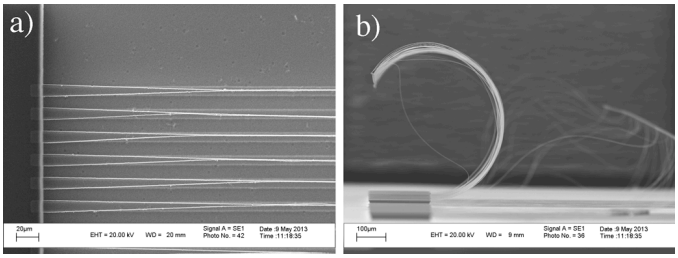

Fig. 11 SEM views of suspended metal sidewall structures, corresponding to a) double-ended and b) single-ended actuators.

Fig. 11b shows the similarly released mask for a single-ended actuator, which has curled out-of-plane by more than 180^o, indicating additional differential stress between horizontal metal layers. This effect is attributed to a vestigial layer of Cr beneath the foot of the sidewall mask. Both effects could be eliminated using a single sidewall material.

Sidewall mask stresses may be sufficient to distort released structures. For example, Fig. 12a shows a single-ended actuator fabricated in BSOI with a much thinner (2 μm) device layer, using a deeper (1 μm) sidewall mask and hence a very shallow (1 μm) Si suspension. Residual stress in the mask has clearly overcome the suspension after HF vapor release. However, the obvious solution – to remove the mask before sacrificial undercut using wet chemical etching – can cause a variant of surface tension collapse in which the fragile suspension is twisted down onto the substrate during the drying step (Fig. 12b). The approach used here – to leave the mask in place over a deep Si structure – does allow fabrication of operating devices. However, a better solution would be to use a SiO_2 mask, since this can be removed together with the oxide interlayer during HF vapor undercut.

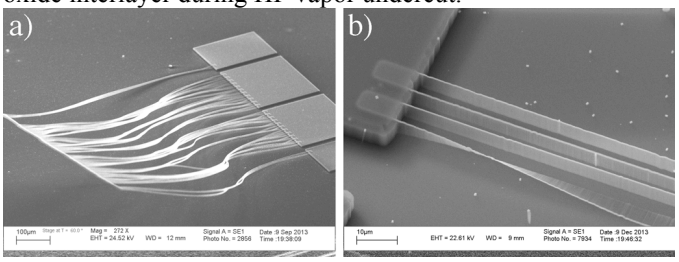

Fig. 12 SEM views of single-ended actuators, showing distortion of suspended Si parts caused by a) sidewall stress and b) surface tension.

The main difficulty in deep silicon etching is to control scalloping and passivation. We have already mentioned some aspects. Scalloping may make it difficult to preserve nanoscale feature widths in structures narrower than 100 nm. However, modern cyclic DRIE equipment allows extremely rapid gas switching, and minimizes scallop formation. Consequently it is likely that the 40 : 1 aspect ratio achieved here will be exceeded. However, in addition, excessive passivation may lead to 'grass' formation, as shown in Fig. 13a. Alternatively, lack of passivation may lead to the erosion of nanoscale features, particularly near corners in the device where the plasma is concentrated during etching, as shown in Fig. 13b.

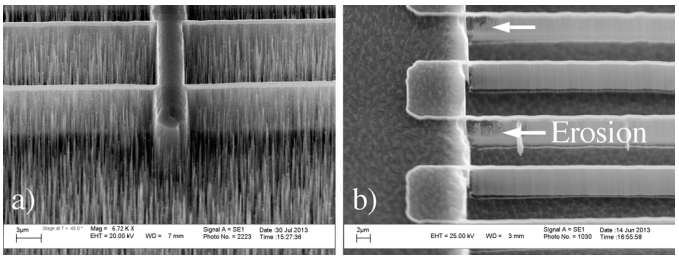

Fig. 13 SEM views of unreleased Si structures showing a) grass, b) erosion.

VII. Geometric Constraints

Geometric constraints are more fundamental. For example, all nanoscale features must follow the perimeters of closed polygons. This makes STL well suited to the formation of multiple built-in beams (as here) but will present a limitation for other designs. For example, it is not possible to form single cantilevers using the process of Fig. 2. However, it is simple to envisage additional patterning steps that interrupt polygons to allow cantilevers, or overlay polygons to generate more complex designs such as intersecting suspensions.

Similarly, all nanoscale features must have constant width. However, it would be possible to employ additional sidewall layers, which are removed over part of the perimeter by patterning and differential etching, to yield nanoscale features with variable width. This approach might be used (for example) to construct shape bimorphs, but clearly requires additional deposition, lithography and etching steps.

Finally, it is not simple to introduce nanoscale separations;

typically, STL yields nanoscale features or slots, but not both together. The use of multilayer sidewalls based on alternating materials should at least allow the formation of parallel beams with nanoscale gaps. Other post-processes such thermal, surface tension or electrostatic actuation might be used to adjust released structures. However, it is hard to see how some common MEMS components (for example, electrostatic combs) could be formed with both nanoscale parts and nanoscale gaps. Thus, the method has significant constraints.

VIII. CONCLUSIONS

We have developed a fabrication process for BSOI NEMS that uses sidewall transfer lithography and deep reactive ion etching to combine 100 nm wide suspension elements with microscale anchors and crossbeams. Silicon was used as a structural material and as a sacrificial mesa material and Cr/Au as a sidewall mask material. However, a wide range of alternative materials and processes exist. We have demonstrated suspended nanostructures and operating electrothermal devices, together with diagnostic techniques that that can reveal the effects of intrinsic stress. Further work is required to improve metrology, but these preliminary results demonstrate that relatively sophisticated NEMS can indeed be fabricated using simple equipment.

The process suffers from several limitations, particularly a requirement for well-chosen sidewall material and careful control of deep silicon etching. There are also inherent geometric constraints that preclude the fabrication of many layouts. However, there may well be applications where these are offset by the low capital cost of the equipment and the possibility of mass parallel fabrication.

Example applications for low force actuators include variable optical attenuators [59] and iris mechanisms [60]. In addition, STL may be adapted to form many other fixed or suspended NEMS in metals, dielectrics and multilayers. Potential applications include ultrasensitive sensors, needle electrodes for intracellular measurement, silicon-cored waveguides and plasmonic resonators. The initial pattern definition and the minimum separation between features can be improved using deep UV or excimer laser lithography. Oxidation machining may also be used to reduce feature sizes in Si. Subsequent fabrication can take advantage of many existing plasma-based etching and deposition processes.

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REFERENCES

[1] K.L. Ekinci, X.M.H. Huang and M.L. Roukes, "Ultrasensitive nanoelectromechanical mass detection" *Appl. Phys. Lett.* vol. 84, pp. 4469-4471, May 2004.

[2] A.N. Cleland and M.L. Roukes, "Nanometre-scale mechanical electrometer" Nature vol. 421, pp. 160-162, March 2003.

[3] X.M.H. Huang, S.C. Jun, M. Manolidis and J. Hone, "Nanomechanical hydrogen sensing" Appl. Phys. Lett. vol. 86, pp. 143104, Mar. 2005.

[4] B. Ilic, Y.Yang., H.G. Craighead, "Virus detection using nanoelectromechanical devices" Appl. Phys. Lett. vol. 85, pp. 2604-2606, Sept. 2004.

[5] M. Li, X. Tang, M.L. Roukes, "Ultrasensitive NEMS-based cantilevers for sensing, scanned probe and very high frequency applications" Nature Nanotechnology vol. 2, pp. 114-120 Feb. 2007.

[6] C. Leung, A. Bestembayeva A., R. Thorogate et al., "Atomic force microscopy with nanoscale cantilevers resolves different structural conformations of the DNA double helix" Nano Letts. vol. 12, pp. 3846-3850, June 2012.

[7] A.N. Cleland and M.L. Roukes "Fabrication of high frequency nanometre scale mechanical resonators from bulk Si crystals" Appl. Phys. Lett. vol. 69, 2653-2655, Oct. 1996.

[8] H.G. Craighead, "Nanoelectromechanical systems" *Science* vol. 390, pp. 1532-1535, Nov. 2002.

[9] I. Bargatin, I. Kozinsky and M.L. Roukes, "Efficient electrothermal actuation of multiple modes of high frequency nanoelectromechanical resonators" Appl. Phys. Lett. vol. 90, 093116, Feb. 2007.

[10] N. Sinha, G.E. Wabiszewski, R. Mohammeed et al., "Piezoelectric aluminium nitride nanoelectromechanical actuators" Appl. Phys. Lett. vol. 95, 053106, Aug. 2009.

[11] E.P. Harris and R.W. Keyes, "Method for fabricating ultranarrow metallic lines" US patent 4,093,503, June 1978.

[12] W.R. Hunter, A.F. Tasch and T.C. Holloway, "Formation of submicron substrate element" US patent 4,354,896, Oct. 1982.

[13] H.S. Fu, "Submicron patterning without using submicron lithographic technique" US patent 4,358,340, Nov. 1982.

[14] P. Vettiger, P. Buchmann K. Dätwyler, G. Sasso and B.J. Van Zeghbroeck, "Nanometer sidewall lithography by resist silylation" *J. Vac. Sci. Tech. B* vol. 7, pp. 1756-1759, Nov./Dec. 1989.

[15] D.S.Y. Hsu, N.H. Turner, K.W. Pierson and V.A. Shamamian, "20 nm linewidth platinum pattern fabrication using conformal effusive-source molecular precursor deposition and sidewall lithography" *J. Vac. Sci. Tech. B* vol. 10, pp. 2251-2258, Sept./Oct. 1992.

[16] U. Hilleringmann, T. Vierigge and J.T. Horstmann, "A structure definition technique for 25 nm lines of silicon and related material" *Microelectr. Engng.* vol. 53, pp. 569-572, June 2000.

[17] K.H. Chung, S.K. Sung, D.H. Kim, W.Y. Choi, C.A. Lee, J.D. Lee and B.G. Park, "Nanoscale multi-line patterning using sidewall structure" *Jpn. J. Appl. Phys.* vol. 41, pp. 4410-4414, June 2002.

[18] I.T. Ho and J. Riseman, "Method for forming a narrow dimensioned mask opening on a silicon body utilizing reactive ion etching" US patent 4,209, 349, June 1980.

[19] R.R.A. Syms, "Sub-micron structuring at mesa edges" *Microelectr. Engng.* vol. 73-74, pp. 295-300, Mar. 2004.

[20] A. Carlson and T.-J.K. Liu, "Negative and iterated spacer lithography process for low variability and ultra-dense integration" SPIE Proc. vol. 6924, pp. 69240B-1-69240B-9, Feb. 2008.

[21] J. Sakimoto, H. Kawata, M. Yasuda and H. Yoshiko, "25 nm wide silicon trench fabrication by edge lithography" *Jpn. J. Appl. Phys.* vol. 50, pp. 08KC03-1-08KC03-05, Aug. 2011.

[22] K.-H. Chung, W.Y. Choi, S.-K. Sung, et al. "Pattern multiplication method and the uniformity of nanoscale multiple lines" *J. Vac. Sci. Tech. B* vol. 21, pp. 1491-1495, July/Aug. 2003.

[23] G.F. Cerofolini, G. Arena, C.M. Camalleri, C. Galati, S. Reina, L. Renna and D. Mascalo "A hybrid approach to nanoelectronics" *Nanotechnology* vol. 16, pp. 1040-1047, May 2005.

[24] S.R. Sonkusale, C.J. Amsinck, D.P. Nackashi, et al. "Fabrication of wafer scale, aligned sub-25 nm nanowire and nanowire templates using planar edge defined alternate layer process" *Physica E* vol. 28, pp. 107-114, May 2005.

[25] W.R. Hunter, T.C. Holloway, P.K. Chatterjee and A.F. Tasch, "A new edge-defined approach for submicrometer MOSFET fabrication" *IEEE Electron. Dev. Letts.* vol. 2, pp. 4-6, Jan. 1981.

[26] D.H. Kim, S.-K. Sung, J.S. Sim, K.R. Kim, J.D. Lee, B.G. Park, B.H. Choi, S.W. Hwang and D. Ahn, "Single-electron transistor based on a silicon-on-insulator quantum wire fabricated by a side-wall patterning method" *Appl. Phys. Lett.* vol. 79, pp. 3812-3814, Dec. 2001.

[27] Y.-K. Choi, T.-J. King and C. Hu, "A spacer patterning technology for nanoscale CMOS" *IEEE Trans. Electron Devices* vol. 49, pp. 436-441, Mar. 2002.

[28] J.T. Horstmann and K.F. Goser, "New fabrication technique for nano-MOS transistors with W = 25 nm and L = 75 nm using only conventional optical lithography" *Microelectr. Engng.* vol. 61-62, pp. 601-605, July 2002.

[29] L. Sun, X.Y. Liu, D.Q. Hou and R.Q. Han, "SOI Schottky barrier tunnelling transistors fabricated with spacer technology" *Elect. Lett.* vol. 40, pp. 511-513, Dec. 2003.

[30] H.C. Lin, M.-H. Lee, C.-J. Su, et al., "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel*" IEEE Electron Dev. Letts.* vol. 26, pp. 643-645, Sept. 2005.

[31] J. Hållstedt, P.-E. Hellström, Z. Zhang, et al. "A robust spacer gate process for deca-nanometer high-frequency MOSFETs" *Microelectr. Engng.* vol. 83, pp. 434-439, Dec. 2006.

[32] B. Degroote, R. Rooyackers, T. Vandeweyer, et al. "Spacer defined FinFET: Active area patterning of sub-20 nm fins with high density*" Microelectr. Engng.* vol. 84, pp. 609-618, Dec. 2007.

[33] R. Otterbach, U. Hilleringmann, J.T. Horstmann and K. Goser, "Structures with a minimum feature size of less than 100 nm in CVD diamond for sensor applications" *Diamond and Related Materials* vol. 10, pp. 511-514, March-July 2001.

[34] Y.-K. Choi, J. Zhu,, J. Grunes, J. Bokor and G.A. Somorjai, "Fabrication of sub-10-nm silicon nanowire arrays by size reduction lithography" *J. Phys. Chem.* vol. 107, pp. 3340-3343, March 2003.

[35] X.M. Yan, S. Kwon, A.M. Contreras, et al. "Fabrication of dense arrays of platinum nanowires on silica, alumina, zirconia and ceria surfaces as 2-D model catalysis" *Catalysis Letts.* vol. 105, pp. 127-132, Dec. 2005.

[36] A.M. Contreras, X.-M. Yan, S. Kwon, J. Bokor and G.A. Somorjai, "Catalytic CO oxidation reaction studies on lithographically fabricated platinum nanowire arrays with different oxide supports" *Catalysis Letts.* vol. 111, pp. 5-13, Oct. 2006.

[37] Z. Zhang, J. Lu, P.-E. Hellström, M. Östling and S.-L. Zhang, "Ni_2Si nanowires of extraordinarily low resistivity" *Appl. Phys. Lett.* vol. 88, 213103, May 2006.

[38] Z. Zhang, P.-E. Hellström, J. Lu, M. Östling and S.-L. Zhang, "A novel self-aligned process for platinum silicide nanowires" *Microelectr. Eng.* vol. 83, pp. 2107-2111, Oct. 2006.

[39] D.S.Y. Hsu and H.F. Gray, "Vertical thin-film-edge field emitters: fabrication by chemical beam deposition, imaging of cathodoluminescence and characterisation of emission" *Thin Solid Films* vol. 286, pp. 92-97, Sept. 1996.

[40] D.S.Y. Hsu and Gray H.F. "A low-voltage, low-capacitance, vertical ruthenium-lithium-ruthenium sandwich layer thin-film edge dispenser field emitter electron source*" Appl. Phys. Lett.* vol. 75, pp. 2497-2499, Oct. 1999.

[41] J.C. Yi, "Miniband properties of superlattice quantum dot arrays fabricated by the edge-defined nanowires" *Microelectronics J.* vol. 39, pp. 369-374, Aug. 2008.

[42] J.C. Yi, "Anisotropic transport properties of quantum dot arrays fabricated by the edge-defined nanowires" *Microelectronics J.* vol. 40, pp. 473-475, Mar. 2009.

[43] F.M. Gomez-Campos, S. Rodriguez-Bolivar, A. Luque-Rodriguez and J.A. Lopez-Villanueva, "Intraband photon absorption in edge-defined nanowire superlattices for optoelectronic applications" *J. Appl. Phys.* vol. 108, pp. 12307-12307-6, Dec. 2010.

[44] P.B. Grabiec, M. Zaborowski, K. Domanski, et al. "Nano-width lines using lateral pattern definition technique for nanoimprint template fabrication" *Microelectr. Engng.* vol. 73-74, pp. 599-603, Mar. 2004.

[45] X.M. Yan, S. Kwon, et al., "Fabrication of large number density platinum nanowire arrays by size reduction lithography and nanoimprint lithography" *Nano Letts.* vol. 5, pp. 745-748, April 2005.

[46] J. Haneveld, E. Berenschot, P. Maury, H. Jansen "Nano-ridge fabrication by local oxidation of silicon edges with silicon nitride as a mask" *J. Micromech. Microeng.* vol. 16, pp. S24-S28, May 2006.

[47] L.Q. Chen, M.B. Chan-Park, Y.H. Yan, et al. "High aspect ratio silicon nanomoulds for UV embossing fabricated by directional thermal oxidation using an oxidation mask" *Nanotechnology* vol. 18, 355307, Aug. 2007.

[48] S.R. Sonkusale, N.H. Di Spigna and P.D. Franzen, "Uniformity analysis of wafer-scale sub-25 nm wide nanowire array nanoimprint mold fabricated by PEDAL process" *Microelectr. Eng.* vol. 84, pp. 1532-1527, Feb. 2007.

[49] Y. Zhao, E. Berenschot, M. de Boer, H. Jansen, N. Tas, J. Huskens and M. Elewenspoek "Fabrication of a silicon oxide stamp by edge lithography reinforced with silicon nitride for nanoimprint lithography" *J. Micromech. Microeng.* vol. 18, 064013, May 2008.

[50] K.S. Park, K.H. Baik, D.P. Kim, et al., "Sub 30 nm gate template fabrication for nanoimprint lithography using spacer patterning technology" *J. Nanosci. Nanotech.* vol. 11, pp. 1625-1625, Feb. 2011.

[51] J. Rao, H. Zou, R.R.A. Syms, E. Cheng and C. Liu, "Fabrication of 2D silicon nano-mold based on sidewall transfer" *Micro and Nano Letts.* vol. 6, pp. 29-33, Jan. 2011.

[52] X. Han, H. Luo, W.G. Wu, et al., "Stacked SiO_2/Si nanonail array fabricated by spacer technology for biomedical applications" *Proc. Transducers 2007*, Lyon, France, pp 1609-1612, Jun. 10-14, 2007.

[53] Q. Xie, Q. Zhou, F. Xie, et al. "Wafer-scale fabrication of high-aspect ratio nanochannels based on edge-lithography technique" *Biomicrofluidics* vol. 6, 016502-016502-08, Mar. 2012.

[54] D. Liu and R. R. A. Syms, "NEMS actuators by sidewall transfer lithography" *Proc. 39th Int. Conf. on Micro and Nano Eng.*, London, pp. 34, Sept. 2013.

[55] M.J. Sinclair, "A high force low area MEMS thermal actuator*" Proc. 7th Intersociety Conf. on Thermal phenomena*, pp. 127-132 , May 2000.

[56] L. Que, J.-S. Park and Y.B. Gianchandani, "Bent-beam electrothermal actuators - Part I: single-beam and cascaded devices" *J. Microelectromech. Syst.* vol. 10, pp. 247-254, June 2001.

[57] R.R.A. Syms, H. Zou, J. Yao, D. Uttamchandani and J. Stagg, "Scalable electrothermal MEMS actuator for optical fibre alignment" *J. Micromech. Microeng.* vol. 14, pp. 1633-1639, Aug. 2004.

[58] W.P. Sassen, V.A. Henneken, M. Tichem, P.M. Sarro, "An improved in-plane thermal folded V-beam actuator for optical fibre alignment" *J. Micromech. Microeng.* vol. 18, 075033, June 2008.

[59] R. Wood, V. Dhuler and E. Hill, "A MEMS variable attenuator" Proc. IEEE/LEOS Int. Conf. on Optical MEMS, Kauai, Hawaii, pp. 121-2, 21-24 Aug. 2004.

[60] R.R.A. Syms, H. Zou, J. Stagg and H. Veladi, "Sliding-blade MEMS iris and variable optical attenuator" J. Micromech. Microeng. vol. 14, pp. 1700-1710, Sept. 2004.

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