Radio Frequency Co-Planar ZnO Schottky Nano-Diodes Processed from Solution on Plastic Substrates

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Main Text

Radio Frequency Identification (RFID) is a rapidly growing technology used for wireless communication and the identification of objects in close proximity through radio waves.[1] Although already a billion dollar industry[2], RFID technology promises substantial further growth by adopting fully printable processing routes. However, there remain several bottlenecks to be overcome before this opportunity can be realised, particularly pertaining to the high frequency performance of printable electronics.

RFID tags are generally composed of a coupling element, or antenna, a direct current (DC) rectifier and integrated circuitry (IC). The rectifying element is by far the most important component in terms of high-frequency (HF) operation, as the logic may take place at much

lower frequencies than the RF base carrier frequency. Different frequency bands exist for different applications, though the current target for printable RFID is the widely employed 13.56 MHz band.[1] Conventionally, complementary metal-oxide-semiconductor (CMOS) technology favours the use of diode-connected metal-oxide-semiconductor field-effect transistors (MOSFETs) for rectification within this element. However, Schottky diodes, with their inherently lower voltage operation, lower series resistance and exponential current-voltage relationship offer a superior choice for rectifiers.[4]

There has been extensive work carried out in recent years to develop high frequency organic Schottky diodes following the pioneering work of Steudel *et al.* who demonstrated pentacene-based Schottky diode rectifiers operating at 50 MHz.[5] More recently C_{60}-based Schottky diodes with a cut-off frequency (f_{CO}) up to 0.7 GHz have also been reported.[6] Diodes based on metal oxide materials (particularly In-Ga-Zn-O) have recently emerged as a promising material, demonstrating device performance up to and above 1 GHz. [7-9] Despite such promising results, manufacturing of these conventional staggered diodes relies on vacuum processing, which renders them incompatible with cost-effective large-volume product integration. To address this important bottleneck, recent work has been devoted to solution-processable organic diodes with adequate performance.[10-12] Si nanoparticles have recently been demonstrated as a potential route to solution processed diodes with cut-off frequencies as high as 1.6 GHz.[13] However, demonstrating high yield manufacturing of solution-processed diodes with cut-off frequency ≥50 MHz still remains a significant challenge.

The operational frequency of Schottky diodes is inversely proportional to the product of the series resistance (R_S) and junction capacitance (C_j). A common approach to boosting the device cut-off frequency is by reducing R_S through the use of a high charge carrier mobility

semiconductor. Unfortunately, the carrier mobility of the vast majority of solution processable organic semiconductors is relatively low as compared to their vacuum-processed counterparts. An alternative approach is to minimize the thickness of the semiconductor layer and/or use more advanced device architectures. **Figure 1a** shows the schematic cross-section of a sandwich-type Schottky diode. Here, reduction of the semiconductor thickness (d) provides one route towards minimizing R_S. In practice, d can be reduced down to the depletion region width (W_d), even when the diode is in forward bias. This so-called Mott operating regime has been used to fabricate monolithic silicon Schottky diodes operating in the THz range.[14] However, there are inherent problems with implementing this concept using solution-processable semiconductors. Firstly, depositing semiconducting layers with thickness on the order of tens of nanometres with reliable uniformity is technically very challenging. Secondly, such thin layers tend to exhibit a large density of pinhole defects that scales with diode area, causing devices to short. Finally, since the active area of solution-processed diodes is often required to be large in order to boost the current output, reducing the active layer thickness to the nanoscale while maintaining a large enough active area, leads to a large increase in C_j, with adverse effects on the operating frequency of the diode. Therefore, development of advanced device concepts and/or new material systems with improved charge transport characteristics are required if solution-processable RF electronics are to become a reality.

Here, we report the development of co-planar Schottky-diodes manufactured by adhesion-lithography (a-Lith) on inexpensive substrate materials including glass and plastic. Unlike conventional sandwich-type diodes, in co-planar devices the inter-electrode distance defines the thickness d of the active semiconductor channel (**Figure 1b**). By reducing d to <20 nm we can significantly reduce the transit time (t_T) of charge carriers through the device and increase its f_{CO}. Furthermore, any detrimental effects on device capacitance due to reduced d

are more than compensated for by the reduction in the active area of the diode by several orders of magnitude. To this end, vertical diodes are routinely fabricated with relatively large active area in the range 0.001-1 cm^2, which leads to large C_j values. In contrast, in the co-planar diodes shown in **Figure 1b**, the active area is defined by the thickness of the asymmetric electrodes employed times the nano-gap length (W), although the extrinsic capacitance due to the 3D coupling of the electrodes through the substrate/air, must also be considered[15] (see **Figure S1**). However, even when taking this paracitic contribution into account, and even for devices with extremely large W/d ratio (>10,000), this geometrical alteration translates to a dramatic drop in C_j, potentially enabling sub-pF device capacitances and a corresponding increase in f_{CO}.

Despite such tremendous potential, the co-planar device architecture has not been investigated for Schottky diode applications. The reason for this is that it has, up until now, been an impractical architecture to implement due to the complex, and hence expensive, processing steps required. To this end, growth of nanogap electrodes is complex, requiring techniques such as electron beam lithography, oblique angle shadow mask evaporation, scanning probe lithography or mechanical break junctions.[16] Fabrication of asymmetric nano-gap electrodes, as would be required to form an Ohmic and a Schottky contact with the semiconductor, requires even more specialist techniques such as solid-state silicidation[17] or electron-beam overlay techniques.[18] The combination of such highly complex, unreliable and poorly scalable methods, with the ease of printable electronics has thus not been a practical choice. Recently we reported the simple yet highly effective nanofabrication technique a-Lith, for the production of asymmetric metal nanogap electrodes (≤15 nm) with aspect ratios up to 1,000,000 on various substrates.[19] Since originally reporting on this technique we have optimised to process so that peel direction has no influence on gap size. As a result we can now

realise uniform sub-10 nm gaps that appear to be independent of the processing conditions i.e. peel direction (see **Figure S2**). Using this early work as our starting point we attempted to develop co-planar Schottky diodes using different solution-processable semiconducting materials.

The details on the fabrication procedures used to pattern the nano-gap electrodes via a-Lith have been reported previously.[20] **Figure 1c** and **1d** show the scanning electron microscope (SEM) and transmission electron microscope (TEM) images respectively of a representative Au/Al electrode nanogap patterned on a glass substrate by a-Lith. Typical inter-electrode separation is ≤20 nm although accurate estimation of the latter is difficult due to the sensitivity of the gap to high energy electrons.

The first family of semiconductors that was investigated in combination with co-planar nano-gap Al-Au electrodes was that of C_{60} fullerene and several of its methano-fullerene derivatives. Although electron-transporting methano-fullerenes are particularly attractive due to their solubility[20], un-substituted C_{60} offers significantly higher electron mobility[21,22] and a significant cost advantage.[23] Unfortunately, solution deposition of pure C_{60} layers is troublesome due to the hydrophobicity of C_{60}.[21,24] To circumvent this problem we blended C_{60} (20 mg/mL) with high molecular weight polystyrene (5 wt.%) acting as the binder. Using this formulation we were able to grow uniform C_{60}:polystyrene blend films up to 700 nm in thickness. The electron mobility in these films was evaluated using field-effect measurements yielding values up to 2 cm^2/Vs.[21,24] The latter value is amongst the highest reported to date for any solution-processed molecular semiconductor, hence making C_{60} highly attractive for application in high-performance RF diodes.

Figure 2a shows the current-voltage (I-V) characteristics for a representative C_{60}:polystyrene-based co-planar diode with 0.9 mm channel width (w) measured at room temperature in nitrogen atmosphere. The energy level offset (~1 eV) between the Au's work function (-4.8 eV) and C_{60}'s lowest unoccupied molecular orbital (LUMO = -3.8 eV) give rise to a significant barrier for electron injection under reverse bias resulting in an off-current of <0.2 nA (lower measurement limit of our apparatus). Under forward bias, the Al electrode (work function of -4.1 eV) facilitates efficient injection of electrons to the LUMO of C_{60} resulting to an on-current of ~0.2 μA. The combined effect is the realisation of co-planar diodes with rectification ratio of the order of 10^3 at ±2.5 V (**Figure 2a**). Worth noting is that no surface modification of the Au/Al electrodes or injection layers are employed here while the unintentional oxidation of the aluminium electrode (i.e. formation of native Al_2O_3) during processing in air seems to cause no significant hindrance to device operation.

The dynamic response of the diodes was investigated using the rectifier circuit shown in **Figure 2b** together with a photograph of the experimental setup. Here, an alternating current (AC) input voltage (V_{IN}) of constant amplitude is applied at increasing frequencies (f) and the resultant DC voltage (V_{OUT}) is monitored at the output. The cut-off frequency of the diode is defined as the half power point, where V_{OUT} drops to -3dB. **Figure 2c** displays both the AC V_{IN} and DC V_{OUT} signals as a function of time for a fixed frequency of 13.56 MHz while **Figure 2d** shows the DC voltage output (in dB) as a function of frequency up to 20 MHz. While there is a noticeable drop in DC output of approximately -1.2 dB for signal frequency of 20 MHz, the ultimate cut-off frequency for these C_{60}:polystyrene diodes lies well beyond the measurement range. Extrapolations of the experimental data (dashed line in **Figure 2d**) suggest an ultimate f_{CO} on the order of ~400 MHz.

These simple to implement co-planar C_{60}:polystyrene diodes demonstrate the feasibility of realising organic RF devices from solution at low temperatures. However, the choice of C_{60}:polystyrene as the active layer has several drawbacks. For instance, despite the low weight fraction of polystyrene present, small-molecule/polymer blends are known to phase separate during film drying.[25] The formation of a polymer layer at the electrode interface would adversely affect charge injection in this device structure. The presence of the polymer binder also causes the starting solution to be highly viscous making processing of thin layers of C_{60} challenging. When considering the extremely low dimensionality of these nanogap structures, capillary forces become significant reducing the chances of gap filling. Finally, electron transport in C_{60}, and its derivatives, is known to be highly susceptible to atmospheric oxidants such as water and oxygen.[26] The result is that semiconductor deposition and testing has to be performed under inert atmosphere. For these reasons we have consider alternative n-type semiconductors that can be processed from solution at low temperatures and can still yield functional Schottky diodes.

Zinc oxide (ZnO) has garnered much attention in recent years as a transparent n-type semiconductor in applications ranging from thin-film transistors (TFTs) for large area electronics[27], to ultraviolet (UV) and optical photodetectors with high transparency[28,29], to piezoelectric nanogenerators and strain sensors[30,31]. While work has been carried out on high-speed applications in the form of TFTs[32,33], little or no effort has been placed on utilising ZnO in Schottky diodes. To this end, numerous groups have reported the difficulty in forming Schottky contacts between various metals and ZnO.[34-36] One highlighted solution to this problem is the creation of an oxygen rich surface at the metal/ZnO interface[35]. The latter has been shown to be effective in removing residual surface contaminants such as H, C and OH. Furthermore, as oxygen vacancies are considered to be donor-like in ZnO, oxygen abundance

effectively reduces the electron concentration at the interface. Thus the tunnelling probability is reduced and current rectification is enabled due to the formation of a barrier for electron injection from the metal to the conduction band (CB) of ZnO. Importantly, it has been shown that high quality ZnO can be grown from solution-phase using various techniques at relatively low temperature.[37,38]

Due to these attractive attributes we have decided to explore the potential of ZnO as the semiconductor in our co-planar diode architectures (**Figure 1b**). ZnO deposition was performed at low-temperatures (180 ℃) using the previously reported amine-hydroxo zinc complex route.[39-42] Using this chemical route, low-dimensional (i.e. ultra-thin) polycrystalline thin films can easily be grown at low temperatures in air without any special precautions.[43] **Figure 3a** shows low and higher magnification TEM images (top to bottom) of the device cross-section together with a HR-TEM image of a region of the ZnO layer located between the Au-Al electrodes. From these images an inter-electrode distance of ~20 nm can be extracted with the ZnO filling the nanogap entirely. The higher magnification HR-TEM image (bottom image) also shows that the semiconductor is nano-crystalline since the atomic planes of ZnO are clearly visible.

Next, the electrical properties of the diodes where studied at room temperature in nitrogen atmosphere. **Figure 3b** displays representative I-V characteristics for 38 coplanar ZnO diodes (channel width = 0.9 mm) fabricated simultaneously on a single substrate. The devices exhibit uniform I-V characteristics with high on-currents (~0.1 mA), negligible operating hysteresis and low off-currents (~1 nA) that lead to high current rectification ratios of $\geq 10^5$ at ±2.5V. Most importantly the rectification ratio of the diodes may be enhanced further by increasing the channel width. In the latter case, the forward current is found to increase linearly

with increasing *w*, while the reverse bias current remains constant for all devices studied. These results compare favourably to state-of-the-art sandwich-type ZnO Schottky diodes reported to date.[44,45] Furthermore, we note that treatment of the gold electrode with 1 min exposure to UV/ozone before depositing the ZnO layer is unnecessary for the formation of Schottky diodes as the formed Au/ZnO contacts appears to be highly rectifying even when the Au electrodes are evaporated directly onto the ZnO layers.

The dynamic response of discrete ZnO diodes and DC rectifier circuits was also studied. **Figure 3c** shows the V_{IN} and V_{OUT} signals as a function of time ($f = 13.76$ MHz) for a co-planar ZnO diode, while **Figure 3d** displays the DC voltage output of a ZnO diode-based rectifier circuit (in dB) versus input signal frequency. Remarkably the DC voltage output of the rectifier circuit remains constant for signal frequencies up to 20 MHz - i.e. our measurement limit. Due to the enhanced diode quality, as compared to C_{60}:polystyrene-based devices (**Figure 2c**), the V_{OUT} remains high (~1.3 V) even for a low V_{IN} signal amplitude of ±4 V.

To assess the operating stability of these co-planar ZnO RF diodes, continuous operation stress experiments at 13.56 MHz have been carried out for prolonged periods of time. Obtained results reveal only a small drop in the output DC voltage even after 16h continuous operation corresponding roughly to 10^{12} cycles (**Figure S4**). Although the origin of this voltage drop is unknown, it may not be a generic/representative characteristic and further work would be required. Finally, because of the lack of signal attenuation within the frequency range investigated, we were unable to estimate the ultimate cut-off frequency of the circuit at -3bB. On the basis of this observation, as well as the significantly lower value of R_S extracted from I-V characteristics of the ZnO device as compared to the C_{60} device (1.8 kΩ versus 2 MΩ), coupled with the similarity in C_j between devices (see **Figure S1**), we expect the cutoff frequency of the ZnO device to exceed that of the C_{60};polystyrene diodes and potentially

approaching the GHz regime. However, further work using appropriate experimental setup would be required to prove or refute this experimentally.

An important advantage of the a-Lith method is the low process temperature requirement and its compatibility with inexpensive, temperature-sensitive substrate materials such as plastic. To explore this possibility, we fabricate co-planar ZnO Schottky diodes on 150 μm-thick polyethylene terephthalate (PET) foils. **Figure 4a** shows a photograph of diode arrays fabricated on a PET substrate. A statistical analysis of the operating frequency range of 60 ZnO-based Schottky diodes is shown in **Figure 4b**. As can be seen, only two out of 60 devices tested were electrically shorted while the rest function as diodes, corresponding to a yield of ~97% of working devices. Of those working devices, a total of 50 diodes (~83%) exhibited a cut-off frequency at -3 dB (f_{3dB}) of >1 MHz for a $V_{IN} = \pm 4$ V. Among those, 36 devices operated above our measurement limit of 20 MHz corresponding to a yield of 60% of diodes with f_{3dB} >> 20 MHz. Undoubtedly, further process optimisation is expected to lead to higher yield and improved device performance.

Finally, several representative RF ZnO diodes were mechanically stressed through 100 manual bending cycles to radii down to 4 mm. The current-voltage characteristics of a representative diode measured before and after bending are shown in **Figure S5.** As can be seen no significant effect on the operating frequency can be observed with only a minimal drop in diode's forward current. The nature of the mechanical stress (compressive or tensile) appears not to influence the operating characteristics of the diodes following bending. Although preliminary, these results provide solid evidence of the potential of the technology not only for low-temperature processing but also use in large-area flexible electronics of the future.

In conclusion, we have developed co-planar Schottky diodes based on asymmetric metal nanogap electrodes patterned via adhesion-lithography. The proposed device architecture was evaluated using two solution-processable n-type semiconductors namely C_{60} and ZnO. Both materials were found to yield functional Schottky diodes with excellent operating characteristics. Due to the co-planar nature of the nanogap electrodes, as-fabricated diodes exhibited reduced RC constants and low voltage operation. Analysis of the dynamic response of discrete diodes reveals that cut-off frequencies $\gg$20 MHz are easily achievable. In the case of C_{60} diodes, experimental results indicate a maximum cut-off frequency at -3 dB of the output DC voltage, of around 400 MHz, while for ZnO diodes this value was found to be significantly higher and beyond our measurement range. These proof-of-principle co-planar diodes highlight the potential of a-Lith method for the manufacturing of RF electronics on arbitrary substrate materials including plastic. Expanding the range of electrode and semiconductor materials used and exploring more advanced device architectures for higher frequency ranges will be of much interest to probe the limits of this family of devices, and its importance to the development of future all-printed RFID technology.

Experimental Section

Nanogap electrode fabrication: Thermally evaporated aluminium films [i.e. metal 1 (M1) in **Figure 1b**] were patterned using conventional photolithography and wet chemical etching. Samples were immersed in a 2 mM solution of octadecylphosphonic acid (ODPA) in 2-propanol (IPA) for 20 h to allow the formation of a self-assembled monolayer (SAM) on M1 and then rinsed in a stream of IPA for 30 sec in order to remove residual ODPA. The hydrophobic nature of the methyl end-group in ODPA resulted in the surface of M1 electrode becoming significantly more hydrophobic as compared to the substrate's surface. Samples were then dried in nitrogen gas followed by thermal annealing in air at 70° C for 3 min. Next a 35 nm-thick gold film [metal 2 (M2)] with a 5 nm-thick aluminium acting as the substrate

adhesion interlayer was evaporated on top of the entire substrate. M2 was then selectively removed by applying a commercially available adhesive (First Contact) to the sample's surface, followed by a peel-off step. During this step, regions of M2 that overlap with M1 were removed due to weaker adhesion with the M1-ODPA surface, while regions of M2 in contact with the substrate remained in place due to the strong adhesion forces. During this mechanical lift-off step, fracture of the M2 electrode occurred at the interface with M1. The result was the creation of a metal nanogap formed between M2-M1 electrodes. The ODPA layer was removed by exposing the samples to UV/ozone for 1 min.

C_{60} device fabrication: Solutions of C_{60} and polysterene were prepared individually in dichlorobenzene in a nitrogen environment, by stirring at 80˚C for 1 hour. The solutions were blended to create a 20 mg/mL blend of C_{60} containing 5% polystyrene by weight. The solution was spin coated onto the prefabricated nanogap substrates at room temperature. Samples were then thermally annealed at 80˚ C for 10 minutes in nitrogen before being electrically characterized.

ZnO device fabrication: Precursor solutions (0.25 M concentration) were prepared by dissolving zinc oxide hydrate in ammonium hydroxide (50% aqueous). Nanogap substrates were treated with 30 minutes UV/ozone to completely remove the ODPA monolayer. The solution was then spin coated directly onto the substrates followed by a 20 min thermal annealing at 180 ˚C in air.

High-Resolution Transmission Electron Microscopy (HR-TEM): A transmission electron microscope operating at an accelerating voltage of 300 kV (Titan 80–300 Super Twin, FEI Company) was used to acquire cross-section micrographs. A charged couple device (CCD) camera (Model: US4000, Gatan Inc.) was used to record HR-TEM images. Samples were prepared on a focused ion beam (FIB; Helios 400s, FEI) equipped with a nanomanipulator (Omniprobe, AutoProbe300) with lift-out method. Electron beam assisted carbon and platinum

deposition was performed on the sample surface to protect the thin film surface against the ion beam bombardment during ion beam milling. Ga ion beam (30 kV, 9 nA) was first used to cut the sample from the bulk (30 kV, 9 nA), after which it was attached to a Cu grid using a lift-out method. The sample was subsequently thinned down to ≈50 nm thickness (30 kV, 93 pA) and cleaned (2 kV, 28 pA) to get rid of areas of the sample damaged during the thinning process.

Electrical characterization: DC electrical characterization was carried out in a nitrogen atmosphere at room temperature using an Agilent B2902A semiconductor parameter analyzer. High frequency measurements were performed by applying an alternating current signal to the circuit shown in figure 2 (b) using an Agilent 33220A function generator. This was done by mounting a 1 nF capacitor directly onto the measurement micromanipulator, as well as a 50 Ω terminator resistor. The output and input signals were monitored using an Agilent DSO6014A oscilloscope. The setup was controlled using a LabView program.

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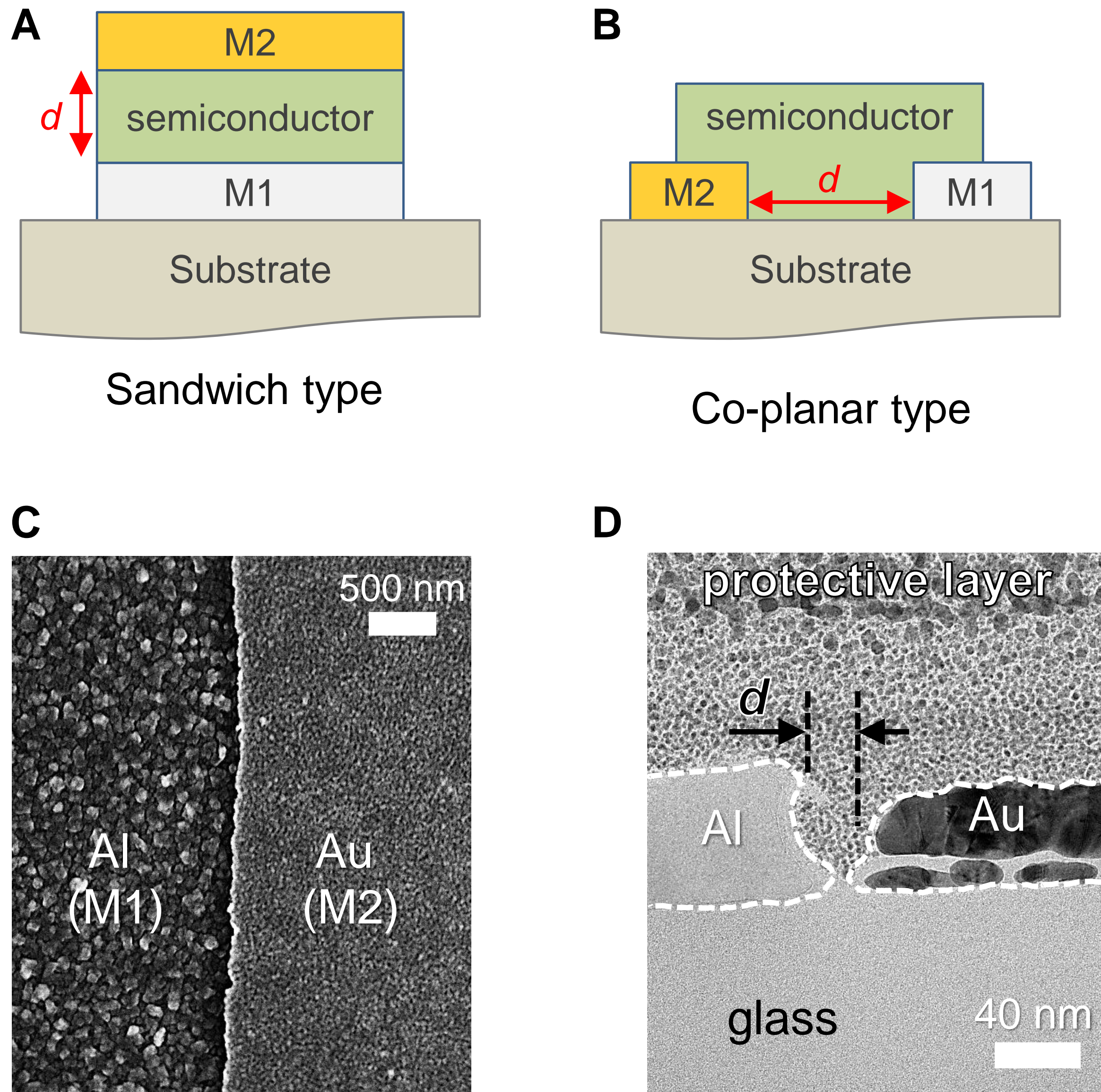

Figure 1. (a) Schematic cross section of a conventional sandwich type Schottky diode. In this case, d is determined by the semiconductor thickness. (b) Proposed new nano-Schottky diode utilising prefabricated asymmetric nanogap electrodes. Here, d is defined by the nanogap size while the device's width by the electrodes' length. (c) SEM and (d) HR-TEM images of a representative pair of Au-Al nanogap electrodes fabricated via a-Lith.

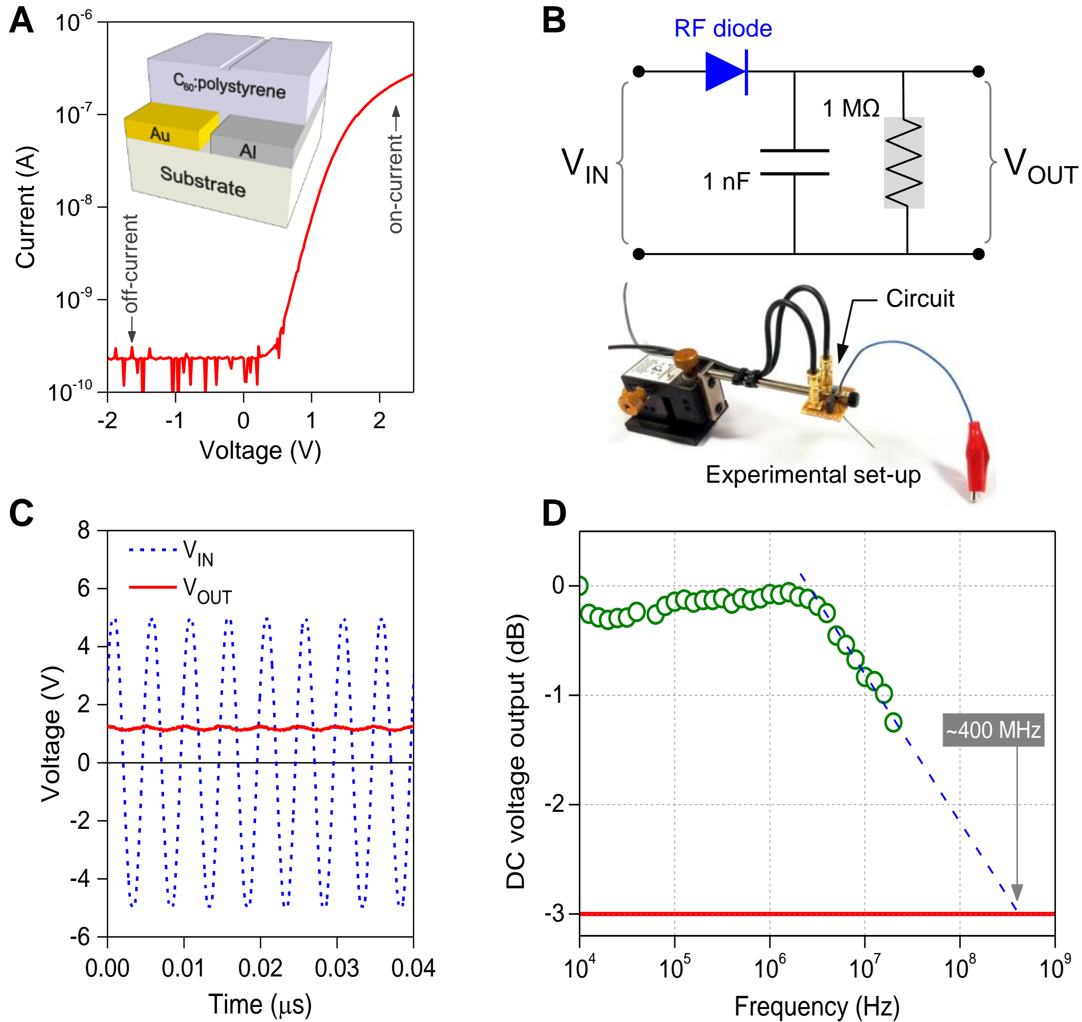

Figure 2. (a) I-V characteristics of a representative C60 Schottky diode. The inset shows a schematic of the device structure. (b) Circuitry of the DC rectifier circuit and a photo of the experimental setup employed. External circuit elements such as the capacitor (1 nF) and the resistor (1 M□) were mounted directly onto a micromanipulator and with the aid of a micro-probe were connected to the co-planar ZnO diode under test. (c) Typical DC waveform (red) measured for a device operating at 13.56 MHz. The AC input signal of 10 Volts peak-to-peak (VPP) is also shown in blue. (d) Bode plot of output DC signal vs input signal frequency. The -3dB line is highlighted in red, while the dashed blue line represents the extrapolation of experimental data.

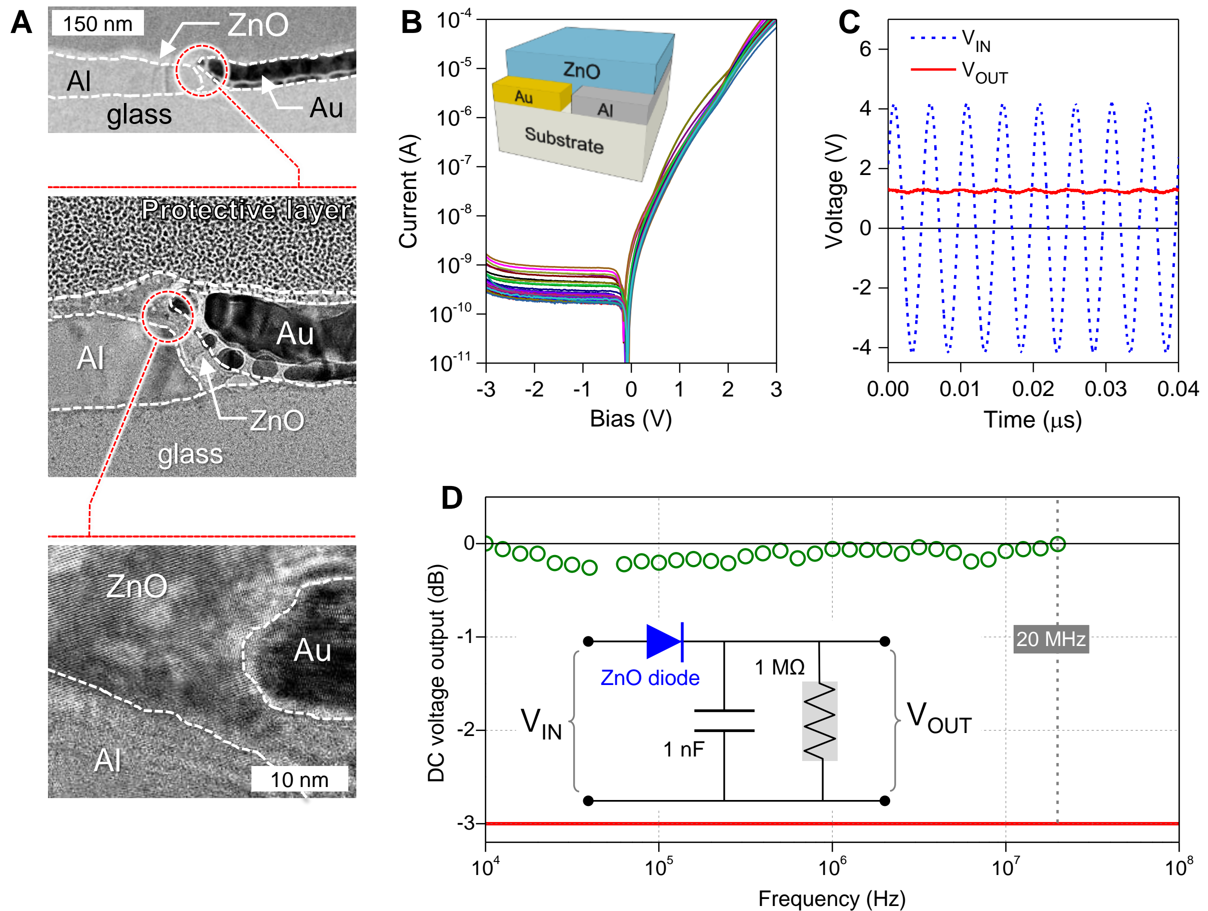

Figure 3. (a) HR-TEM images of the cross-section of a representative ZnO coplanar nano-Schottky diode. Dashed lines indicating the different materials/layers are added for clarity. The high magnification TEM image of the ZnO region located between the metal electrodes reveals the nanocrystalline nature of the ZnO layer. Analysis of the image yields nanocrystalline domains up to 5 nm in diameter. (b) Quasi-static I-V characteristics of 38 ZnO coplanar nano-Schottky diodes fabricated on the same substrate. (c) AC input and DC output signals of a ZnO diode-based rectifier circuit operating at 13.56 MHz. (d) Bode plot of the DC output signal vs AC input signal frequency up to 20 MHz (our measurement limit). Inset in D shows the circuitry of the DC rectifier circuit used.

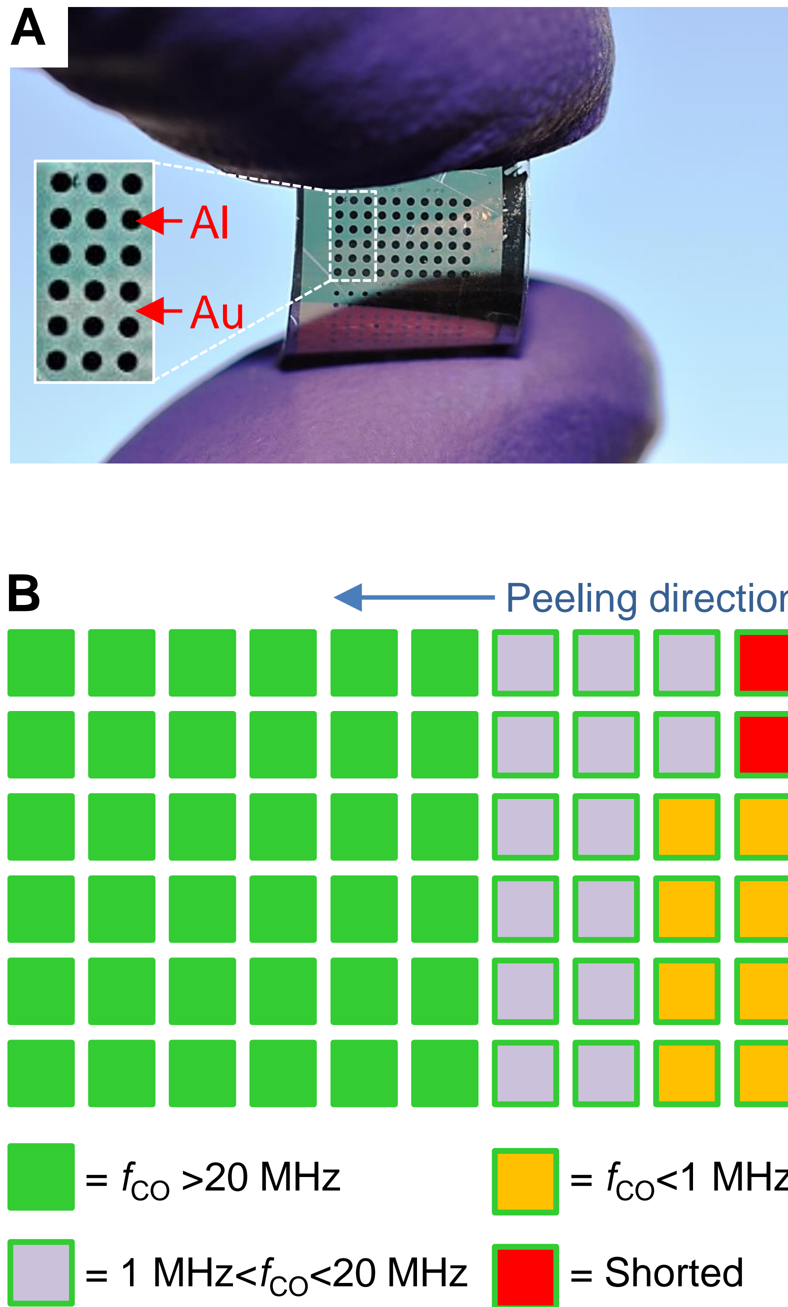

Figure 4. (a) Image of ZnO nanogap Schottky diodes arrays fabricated on a flexible polyethylene terephthalate (PET) substrate. (b) Statistical analysis of the operating frequency range for 60 devices fabricated on the same PET substrate.

The Table of Contents Entry

Co-planar radio frequency (RF) Schottky diodes based on solution-processed C_{60} and ZnO semiconductors are fabricated via adhesion-lithography. The development of a unique asymmetric nanogap electrode architecture results in devices with a high current rectification ratio (10^3-10^6), low operating voltage (<3 V) and cut-off frequencies >400 MHz. Device fabrication is scalable and can be performed at low-temperatures even on plastic substrates with very high yield (**Figure**).

Keyword: Schottky diode, radio frequency diodes, RFID, nanogap electrode, 13.56 MHz

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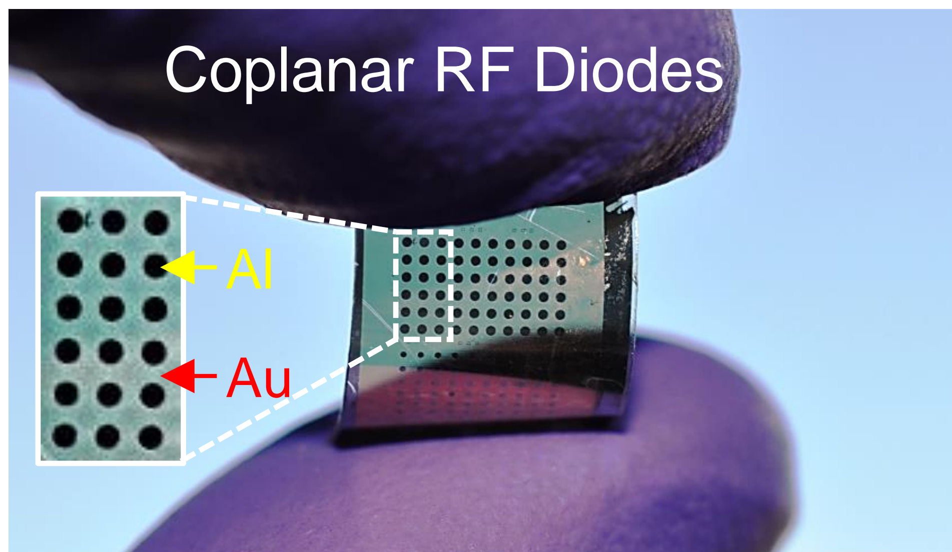
Title: Radio Frequency Co-Planar ZnO Schottky Nano-Diodes Processed from Solution on Plastic Substrates

ToC Figure



Supporting Information

Radio Frequency Co-Planar ZnO Schottky Nano-Diodes Processed from Solution on Plastic Substrates

*James Semple, Stephan Rossbauer, Claire H. Burgess, Dr. Kui Zhao, Dr. Lethy Krishnan Jagadamma, Prof. Aram Amassian, Dr. Martyn A. McLachlan, Prof. Thomas D. Anthopoulos**

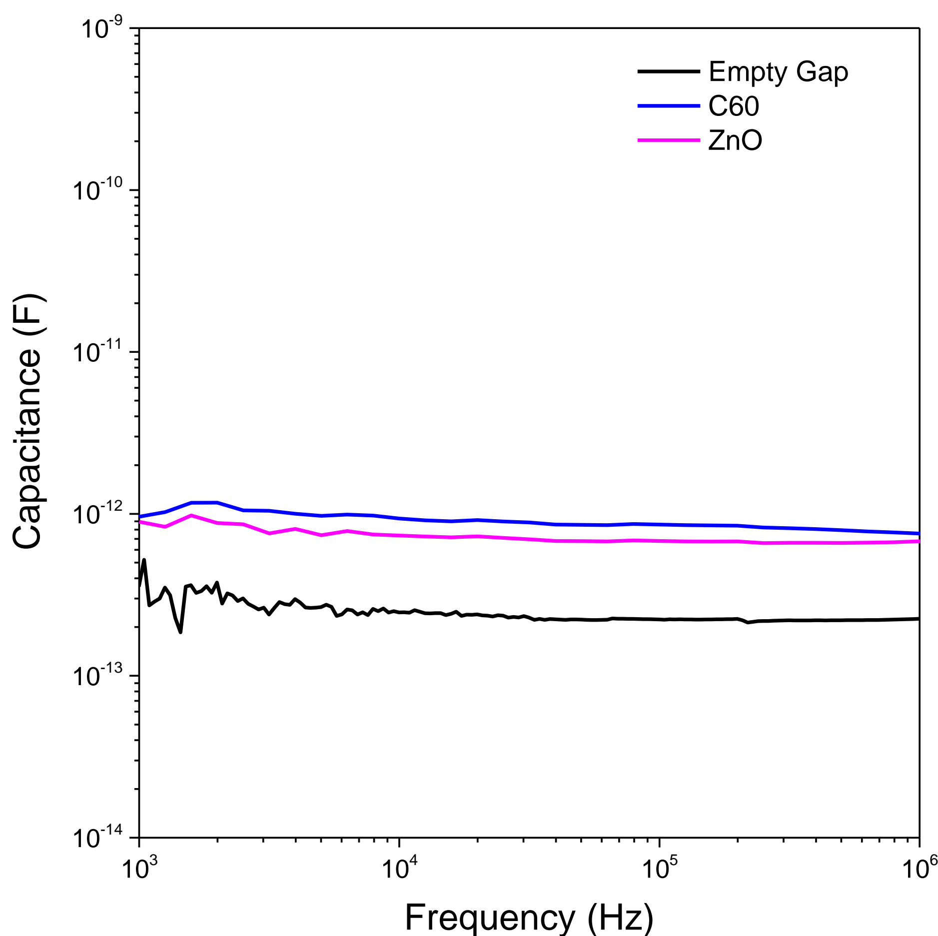


Figure S1. Capacitance as a function of frequency for the empty Al-Au nanogap, C_{60} diode and ZnO diode. While a simplistic calculation for the intrinsic junction capacitance yields a value on the order of 10^{-14} F, measured capacitances are significantly higher (~10^{-12} F). This is attributed to additional intrinsic and extrinsic capacitances due to the 3D coupling of the electrodes.

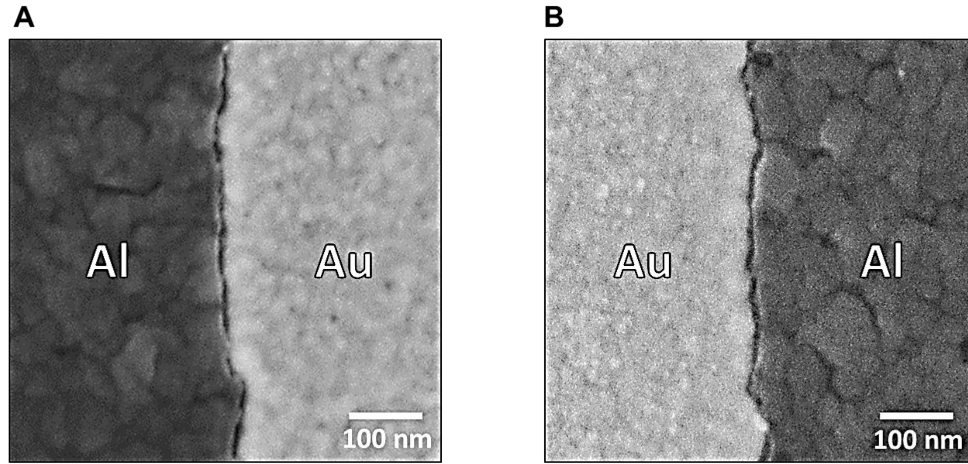


Figure S2. SEM images of the nanogap interface for both the (a) leading edge and (b) trailing edge of the peel direction. Due to process optimisation we see no dependence of the nano-gap size on peel direction and are now capable of realising uniform sub-10 nm gaps regardless of peel direction.

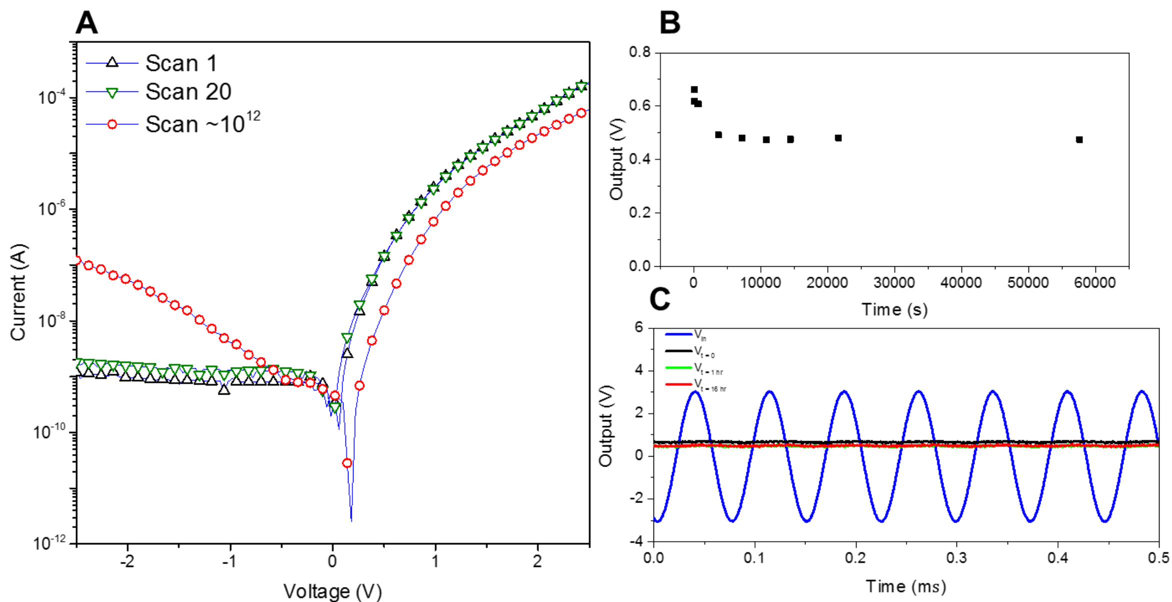


Figure S3. (a) Current-voltage characteristics of the ZnO diode before stressing (upward facing triangles), after 20 cycles measured at DC (downward facing triangles) and after 16 h of continuous operation stressing using a 6 V_{pp} input signal at 13.56 MHz, corresponding to roughly 10^{12} cycles (circles). While there is no detectable shift over the first few scans, there is a marked change over the course of 16 hours as the forward bias current drops and the reverse bias leakage current increases by up to two orders of magnitude at -2.5 V. (b) Over the course of the 16 h measurement, the output DC voltage from the diode in the rectifier setup was monitored. The drop in the output of the diode, (corresponding to the drop in the diode forward current) occurs over roughly the first hour, but after that the output SIGNAL stabilises. (c) Characteristic output waveforms of the dc output from the diode at the beginning of the stressing experiment, after 1 hour and after 16 h continuous operation.

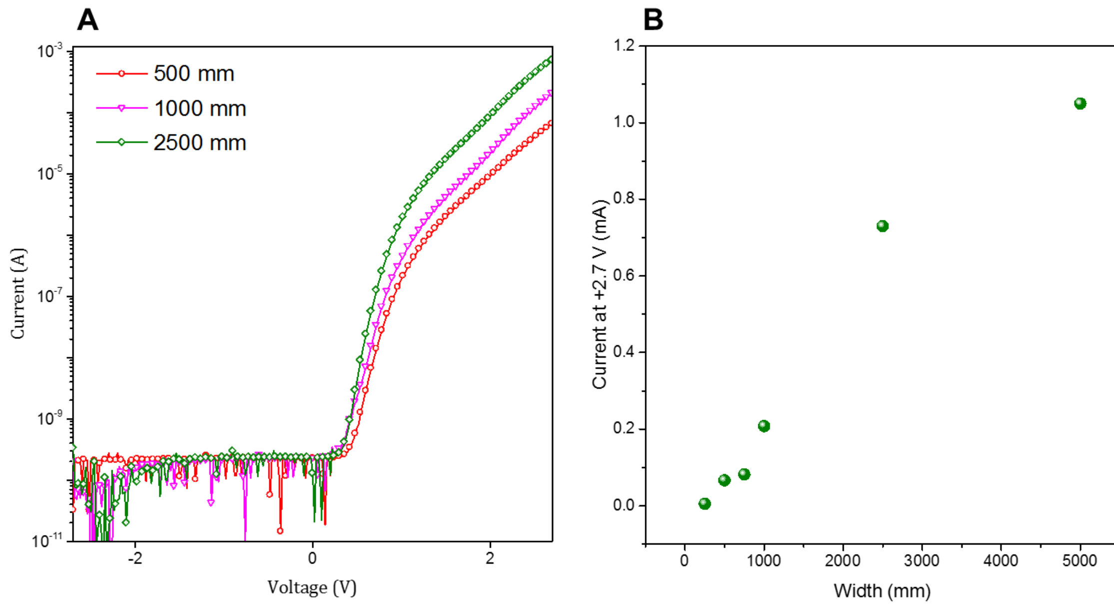


Figure S4. Effect of increasing ZnO diode width. The forward bias current scales linearly with width as would be expected. The lack of change in the observed reverse bias current leads to the conclusion that the reverse bias current remains below the measurement limit of the setup.

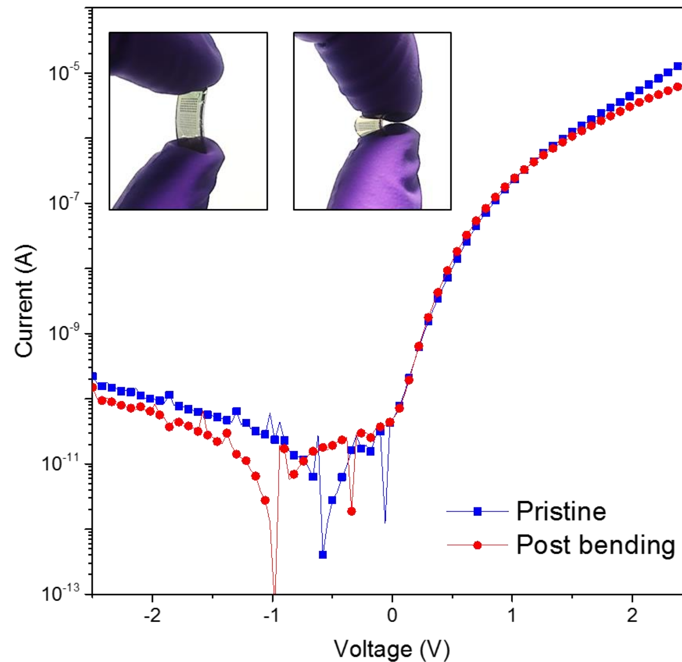


Figure S5. Current-voltage characteristics measured for a representative ZnO diode fabricated on plastic substrate before and after 100 bending cycles. Inset shows a photograph of the actual diode arrays studied.