High Electron Mobility Thin-Film Transistors Based on Solution-Processed Semiconducting Metal Oxide Heterojunctions and Quasi-Superlattices

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Abstract:

High mobility thin-film transistor technologies that can be implemented using simple and inexpensive fabrication methods are in great demand owing to their applicability in a wide range of emerging optoelectronics. Here we report a novel concept of thin-film transistors that exploit the enhanced electron transport properties of low-dimensional polycrystalline quasi-superlattices (QSLs) consisting of alternating layers of In_2O_3, Ga_2O_3 and ZnO grown by sequential spin casting of different precursors in air at low temperatures (180-200 °C). Our prototype QSL transistors exhibit band-like transport with electron mobilities approximately a tenfold greater (25-45 cm^2/Vs) than single oxide devices (typically 2-5 cm^2/Vs). Based on temperature dependent electron transport and capacitance-voltage measurements we argue that the enhanced performance arises from the presence of quasi two-dimensional electron gas-like systems formed at the carefully engineered oxide heterointerfaces within the QSLs. The QSL transistor architecture concept proposed here could in principle extend to a range of other oxide material systems and fabrication methods (sputtering, atomic layer deposition, spray pyrolysis, roll-to-roll, etc.) and can be seen as a promising technology for application in next-generation large area opto/electronics such as ultra-high definition displays and large-area microelectronics where high performance is a key requirement.

Main text:

Thin-film transistors (TFTs) based on transparent metal oxide semiconductors represent an emerging technology that promises to revolutionise large-area electronics due to the high carrier mobility,[1] optical transparency,[2] mechanical flexibility[3] and the potential for low-temperature processing.[4] Like many other transistor technologies the performance level of oxide TFTs ultimately depends on the intrinsic properties of the semiconducting material employed.[5] As a result the maximum electron mobility that can be achieved in conventional devices is limited by the intrinsic mobility of the semiconductor used. In the case of a handful of inorganic transistor technologies (*e.g.* GaN,[6] GaAs[7]), this intrinsic mobility limitation has been overcome through the use of epitaxially grown low-dimensional heterostructures composed of an un-doped (intrinsic) and an extrinsically doped semiconducting layers.[8-9] In such heterostructures the majority carriers minimize their energy by diffusing out of the doped semiconductor layer and into the lower potential undoped semiconductor where they form a two-dimensional electron gas (2DEG) in close proximity to the hetero-interface.[10-11] A key aspect of the 2DEG systems is that the confined carriers become spatially separated from the donor/acceptor sites leading to a reduction in ionised impurity scattering and to high charge carrier mobilities which in many cases exceed the bulk mobility of the individual semiconductors used.[8-11]

Recently, there has been a mounting interest in 2DEG systems formed at epitaxially grown insulating metal oxide heterointerfaces[12] due to the very high charge carrier mobilities[13] and their potential for high-performance electronics[14-15] as well as the rich new physics.[16] Building on the early work on insulating oxides, Tampo *et al.* demonstrated the formation of 2DEGs in semiconducting ZnO/MgZnO heterointerfaces[17] for which electron mobilities exceeding 700,000 cm^2/Vs, albeit at cryogenic temperatures, have recently been reported.[18]

A more technologically relevant development was the recent implementation of the ZnO/MgZnO heterointerface as the active channel in high mobility TFTs.[19] The latter work can be seen as the steppingstone towards practical application of the oxide 2DEG technology in large-area thin-film electronics.[20-22] A summary of the field-effect electron mobility values reported in recent years for different metal oxide hetero-interface systems grown by different methods [e.g. sputtering, molecular beam epitaxy (MBE), metalorganic chemical vapour deposition (MOCVD) and atomic layer deposition (ALD) techniques] is given in Table S1. Despite these very promising early results and the tremendous potential of the 2DEG transistor technology, however, its widespread adoption in practical electronic applications is currently hampered by the rather complex[23] and high temperature (600-900 °C, see Table S1) manufacturing processes often required in order to ensure the formation of the all-important high quality heterointerface.[19, 24-25] Because of the latter requirement it is not a trivial question whether high-quality oxide hetero-interfaces can be realized using simpler, cost-efficient and high-throughput fabrication methods that are compatible with existing semiconductor fabrication processes (e.g. solution-based) and even perhaps temperature-sensitive substrate materials such as plastic. Thus, the development of easy to implement metal oxide hetero/multi-layer structures could help overcoming important bottlenecks associated with the level of performance and manufacturing of incumbent TFT technologies, and enable the emergence of a host of large-area, flexible opto/electronics.[4,26-30]

Here we report the development of low-dimensional quasi-superlattices (QSLs) grown by sequential deposition of different metal oxides by spin casting and thermal annealing at temperatures in the range of 180–200 °C. Structural characterisation of the QSLs revealed the existence of discrete binary oxide layers and the presence of high quality hetero-interfaces.

Remarkably, we found that when the QSLs are incorporated as the active channels in TFTs, the electron mobility is enhanced by approximately one order of magnitude and the charge transport becomes temperature independent resembling band-like conduction. The incorporation of solution processed QSLs as active channels in TFTs not only substantially improves the electrical performance of the devices but also brings a new perspective on the design principles that can be used to develop the next generation metal oxide semiconductors, devices and circuits.

We have recently demonstrated the ability to grow ultra-thin layers of ZnO by spin casting a suitable precursor solution.[31] Using the same aqueous precursor route we have grown polycrystalline ZnO layers with thicknesses in the range 3–10 nm (**Figure 1**a) at 180 °C (see *Experimental Section*). As-grown ZnO layers are found to be continuous and conformal with root mean square (rms) surface roughness of ~0.43 nm as determined by atomic force microscopy (AFM) (Figure 1b). The polycrystalline nature of the ZnO films was also confirmed by grazing incident diffraction (GID) measurements (Figure 1c). The results suggest that ZnO layers exhibit powder-like diffraction peaks (i.e. no preferred orientation) in agreement with the TEM data in Figure 1a. It is worth noting that the high-resolution GID results reported here is the first to reveal the polycrystalline nature of these ultra-thin ZnO layers as compared to early work[32] where only the (002) peak was detected. Using previously reported methods[33] we have also grown ultra-thin layers (5-10 nm) of In_2O_3 (Figure 1d) by spin casting an aqueous solution of indium nitrate [$In(NO_3)_3$] at room temperature followed by thermal annealing at ~200 °C in air. In_2O_3 films are found to be continuous and conformal (Figures 1d and 1e), ultra-smooth (rms ~0.2 nm, Figure 1e) and highly polycrystalline (evidence of which are presented in Figures 1d and 1f) in good agreement with previously reported data.[34] Similarly, ultra-thin (2–5 nm) films of stoichiometric Ga_2O_3 were also grown using the same processing steps (Figure S1).[35]

Unlike ZnO and In_2O_3, however, Ga_2O_3 layers appear to be largely amorphous with no signs of crystallinity as no diffraction peaks could be detected.

Reducing the semiconductor thickness to such extreme dimensions is also expected to impact the physical properties of the resulting oxide layers due to energy quantisation phenomena.[36-37] The latter is expected to lead to widening of the energy bandgap of the semiconductor as compared to its bulk value with reducing layer thickness (L). To investigate this effect we performed absorption measurements in several solution-processed ZnO and In_2O_3 layers of variable thickness and calculated the optical bandgap using Tauc analysis[38-39] (see *Experimental Section*). If we define the dimension perpendicular to the substrate surface as (z), then the energy of conduction band and valence band states available to electrons and holes respectively, confined to an infinite quantum well (QW) can be described by[36]:

$$E_{n,e} = E_{xy} + \frac{n^2 h^2}{8 m_e^* L^2} \quad (1)$$

$$E_{n,h} = E_{xy} - \frac{n^2 h^2}{8 m_h^* L^2} \quad (2)$$

Here, E_{xy} is the energy associated with the carrier in the (unconfined) x,y-plane, n is a positive integer, h is the Planck Constant, m_e^* and m_h^* are the effective masses of the electron and hole in the semiconductor, respectively, and L is the thickness of the quantum well in the z-direction (**Figure 2**a). As L is reduced the energy of the first electron state (n = 1), and hence the conduction band minimum (CBM), increases. Similarly the energy of the first hole state (n = 1), and hence the valence band maximum (VBM), decreases. As a result the energy of the first allowed transition from the VBM to the CBM in the confined direction increases resulting in a blue-shift in the onset of the optical absorption. The energy increase (ΔE_G) as a result of L can then be written as[40]:

$$\Delta E_G = \frac{h^2}{8L^2}\left(\frac{1}{m_e{}^*} + \frac{1}{m_h{}^*}\right) \quad (3)$$

Since the band gap of the quartz substrates used is extremely large (~8.9 eV) the single layers of ZnO and In_2O_3 were modeled as infinite QW. Finite QW energies were also calculated using known techniques,[41] but the results were found to be negligibly different from those evaluated using the infinite QW approximation (**Equation 3**). The values for the effective mass of holes ($m_h{}^*$) and electrons ($m_e{}^*$) in In_2O_3 employed were $m_e{}^* = 0.3m_e$ and $m_h{}^* = 0.6m_e$;[42] where m_e is the rest-mass of an electron in a vacuum. Values of effective mass for ZnO were $m_e{}^* = 0.29m_e$ and $m_h{}^* = 1.2m_e$.[43-44]

Figure 2b–c display the measured change in the energy band gap (ΔE_G) as a function of *L* extracted using the Tauc analysis (see *Experimental Section*). The solid lines in each plot represent the theoretical values for ΔE_G calculated using Equation 3. Good agreement between the experimental determined and the theoretically predicted ΔE_G is observed for both material systems. In the case of ZnO layers, reducing *L* leads to E_G values close to ~150 meV, while in the case of In_2O_3 this energy difference is much larger and approaches values close to ~450 meV. Interestingly, for In_2O_3 layers the extracted ΔE_G is in good agreement, within experimental error, to values calculated assuming a direct or an indirect bandgap (see *Experimental Section*). The noticeable differences in the measured ΔE_G values for ZnO and In_2O_3 layers (Figure 2b-c) are attributed to various effects the most important of which include; (i) the difference in the effective hole masses, (ii) the differences in the conduction band energies and (iii) the different degrees of crystallinity characterising each system. On the basis of this data we conclude that reducing the thickness of the ZnO and In_2O_3 layers results in a characteristic widening of the optical band gap in good agreement with theoretical predictions for energy quantization.

The elemental compositions of the discrete metal oxide films were verified by X-ray photoelectron spectroscopy (XPS) (Figure S1–S3) while their valence band structure was studied using ultraviolet photoelectron spectroscopy (UPS) (Figure S4). The Fermi energies (E_F) were estimated from Kelvin probe (KP) measurements performed in nitrogen (Figure S5), yielding E_F ~4.32 eV, E_F ~4.65 eV and E_F ~4.90 eV for ZnO, In_2O_3 and Ga_2O_3 respectively. The optical bandgap (E_G) for each discrete metal oxide layers were obtained via Tauc analysis of the absorption spectra (Figure S6).

Exploring whether the sequential spin coating method can be applied to fabricate high quality oxide heterointerfaces, we grew multilayer oxide stacks based on combinations of ZnO, In_2O_3 and Ga_2O_3. **Figure 3**a displays schematics of the different layered structures grown including heterojunctions (In_2O_3/ZnO) and multilayer QSLs consisting of In_2O_3/ZnO/In_2O_3 (QSL-I), In_2O_3/Ga_2O_3/ZnO (QSL-II) and In_2O_3/Ga_2O_3/ZnO/Ga_2O_3/In_2O_3 (QSL-III). Unlike conventional a-IGZO TFTs,[45-46] here we use binary metal oxides for each layer in the stacked structures. This strategy helps to avoid complex and in some cases unwanted chemical interactions between different precursor molecules that are generally known to degrade the electrical performance of solution-processed oxide TFTs.[4, 30, 47]

The interfacial nature of these solution grown metal oxide systems was investigated using X-ray reflectometry (XRR) (Figure 3b and S7). Obtained results show clear interference fringes in good agreement with theoretical simulations (Figure 3b) and in support of the existence of well-defined binary layers with abrupt interfaces (Figure S7). Table S2 summarises the parameters used to fit (dash lines) the experimental data (solid lines) in Figure 3b and S7. Surprisingly, the XRR data shows less oscillating fringes for monolayer than multilayer

samples. This finding suggests that the interface roughness (i.e. substrate roughness) is significantly higher than the film's surface roughness. However, since the surface roughness of SiO_2 is expected to be ≤5 Å, the data most likely suggests that the extracted roughness does not originate from the substrate but from the SiO_2/In_2O_3 interface. The fitting parameters in Table S2 also suggest that incorporation of the Ga_2O_3 interlayer in-between In_2O_3 and ZnO (i.e. QSL-I) leads to a significant reduction in the interfacial roughness. This observation is in qualitative agreement with the AFM data in Figure 3c. As the AFM measurements show, the In_2O_3/ZnO heterojunction structure exhibits the highest rms surface roughness (~21 Å) followed by QSL-II (~12 Å). In contrast, QSL-I and QSL-III stacks show ultra-smooth surfaces with rms values of ~2.2 Å and ~4 Å, respectively. From these results we conclude that incorporation of Ga_2O_3 and In_2O_3 helps to planarize both the buried heterointerfaces and surfaces of the QSLs.

Elemental composition profiles as a function of depth collected with ToF-SIMS provide further direct evidence for the existence of sharp interfaces between the different oxide layers in QSL-III. Figure 3d shows the Poisson corrected ion signals as a function of nominal thickness (air interface at x = 0 nm). Both the leading and trailing edges of the ion signal are indicative of the presence of sharp chemical interfaces between the In_2O_3, Ga_2O_3 and ZnO. The gradual increase in Zn^+ signal within the Ga_2O_3 layer and concurrent loss of Ga^+ dynamic range is a classic example of interfacial broadening due to interfacial roughness - a feature also seen in the cross-sectional TEM images of the individual layers shown in Figure 1a. Therefore, on the basis of the XRR (Figure 3b and S7) and ToF-SIMS (Figure 3d) data we conclude that the solution-grown oxide multilayers are indeed composed of ultra-thin alternating layers separated by well-defined interfaces. Furthermore, the existence of different ions at well-defined depths seen in the ToF-SIMS data (Figure 3d) indicates relatively limited intermixing.

Figure 4a displays the measured energy levels of the individual oxide layers used to form the heterojunction and QSL-I, before contact. In contrast to previously published studies in which bi-layered metal oxide structures and transistor channels were formed using similar chemical elements,[48-49] in the present systems the large difference in the Fermi energies (ΔE_F) between the ZnO and In_2O_3 layers (~300 meV) is expected to lead to electron transfer from ZnO to In_2O_3 upon physical contact (Figure 4b). Since the available energy levels at the conduction band minimum (CBM) in the ultra-thin In_2O_3 are quantised (Figure 2c), the transferred electrons may well be confined in a two-dimensional potential well. On the basis of this discussion, it is not unreasonable to assume that the confined electrons will resemble the 2DEG system formed in the MgZnO/ZnO heterointerface.[19] However, due to the polycrystalline nature of the In_2O_3 layer (Figure 1f), the confined electrons are not expected to behave like classic 2DEGs since macroscopic conduction in the QSL-I is expected to be hindered by the presence of grain boundaries that are clearly visible in the HRTEM images in Figure 1.

In the case of QSL-II and QSL-III, insertion of the deeper Fermi energy Ga_2O_3 interlayer (Figure 4c) may enhance electron migration from In_2O_3 and ZnO and at the same time improve electron confinement due to higher interface planarity (Table S2). This process is better illustrated in the energy band diagram of QSL-III after contact shown in Figure 4d. Additionally, Ga is known to passivated interface electron trap states owing to the presence of oxygen and/or hydroxyl groups during Ga_2O_3 formation.[50-52] Therefore, the combination of these beneficial attributes may yield heterointerfaces with improved electron transporting properties as compared to simple In_2O_3/ZnO heterointerfaces (Figure 4b). In view of these experimental findings we argue that in In_2O_3/ZnO and QSL-I structures, a confined electron system is expected to form at the vicinity of each In_2O_3/ZnO heterointerface due to the mismatch between the conduction and Fermi energies of the semiconductors. Similarly, in

QSL-II and QSL-III systems the presence of the deeper Fermi energy Ga_2O_3 layer is expected to planarize the heterointerface(s) as well as improve the electron confinement due to its favourable energetics and trap passivation properties.

To study the nature of charge transport in these complex oxides structures, we fabricated bottom gate, top contact field effect transistors using ZnO, In_2O_3, Ga_2O_3, ZnO/In_2O_3, QSL-I, QSL-II and QSL-III as the channel layers (**Figure 5**a). With the exception of Ga_2O_3, all samples showed n-channel transistor behaviour (Figure 5b), negligible operating hysteresis and high on/off channel current ratios (>10^5). Representative sets of the transfer characteristics (that show both the forward and reverse sweeps) for each device are displayed in **Figure S8**. The room temperature electron mobilities calculated in the saturation regime (μ_{SAT}) for ZnO and In_2O_3 transistors were similar and in the range 2–4 cm^2/Vs. Transistors based on In_2O_3/ZnO heterojunction channels exhibit slightly improved electron transport with maximum mobility values in the range 3–5 cm^2/Vs. Remarkably, we found μ_{SAT} to increase with increasing channel complexity, reaching values between 10–12 cm^2/Vs for QSL-I and QSL-II devices, and up to 25–30 cm^2/Vs for QSL-III based transistors. Insertion of the Ga_2O_3 interlayers between In_2O_3 and ZnO to form QSL-II is found to significantly improve the electron mobility of the devices while in the case of QSL-III transistors the impact of the Ga_2O_3 interlayer is even greater when compared to QSL-I. To this end the μ_{SAT} (Figure 5c) and the linear electron mobility (μ_{LIN}) (Figure S9) measured for optimised QSL-III devices are amongst the highest reported to date for solution deposited metal oxide transistor channels processed at ≤200 °C.

For QSL-I and QSL-III transistors the μ_{SAT} enhancement was accompanied by a threshold voltage (V_T) shift to more negative gate bias, as compared to ZnO and In_2O_3 devices, most likely indicating the presence of a higher density of free/mobile electrons within the transistor

channel (Table S3).[53] Taking into account the low-dimensional nature of QSL and the non-uniform field distribution across it, we argue that these additional free electrons are confined at the critical heterointerfaces (see Figure 4b and d) rather than been distributed uniformly across the QSL. The increase in the off-current in QSL-III transistors (Figure 5b) supports this assumption since the formation of parallel channel(s) further away from the conventional dielectric/semiconductor interface will be manifested as an increase in the channel off current. Despite this, however, the devices continue to function as field-effect transistors exhibiting excellent operating characteristics including high carrier mobility and current on/off ratios. To this end, we note that the ability to manipulate the concentration of free electrons within the confinement region by an external electric field is not unusual but on the contrary a key feature of conventional 2DEG systems.[54-56]

To examine whether the enhanced electron mobility in QSLs transistors is the result of low-dimensional electron transport phenomena taking place at the critical In_2O_3/ZnO and In_2O_3/Ga_2O_3/ZnO interfaces, rather than at the conventional bottom SiO_2/In_2O_3 channel interface, we carried out temperature-dependent charge transport measurements (Figure 5c). As can be seen in single layer ZnO and In_2O_3 devices both the μ_{SAT} (Figure 5c) and μ_{LIN} (Figure S9) decrease with reducing temperature down to 77 K. ZnO transistors showed consistently higher activation energies (E_A) with values in the range 28–37 meV as compared to In_2O_3 devices for which E_A is found to vary between 14–27 meV (Figure S10–S11 and Table S4). Transistors based on In_2O_3/ZnO heterojunctions show similar thermally-activated transport behaviour but with a higher electron mobility value maintained for temperatures in the range 77–250 K (Figure 5c, S9 and S12), most likely suggesting parallel electron conduction in the upper In_2O_3/ZnO interface. On the contrary, electron transport in QSLs-based devices appear to remain significantly enhanced across the entire temperature range investigated (77–300 K)

with QSL-I and QSL-III transistors exhibiting a characteristic temperature-independent electron mobility trend (Figure 5c, S9, S13 and S15). QSL-II devices are also found to exhibit consistently improved performance as compared to In_2O_3/ZnO heterojunction transistors (Figure 5c, S9 and S14). The latter is attributed to the improved structural and electronic quality of the critical oxide heterointerface due to the presence of the Ga_2O_3 interlayer. Small but negative E_A values are calculated for the μ_{LIN} in QSL-I and under certain biasing conditions for QSL-III devices too (Table S4). This temperature independent electron behaviour is unique to devices based on QSL-I and QSL-III and is completely absent from transistors based in any other layer configurations, including QSL-II. These findings support the idea that the nature of electron conduction in QSLs-based devices is radically different from that in single metal oxides based transistors and that this difference most likely originates from the presence of free electrons confined in the vicinity of the low-dimensional ZnO/In_2O_3 and In_2O_3/Ga_2O_3/ZnO interface(s) that act as parallel channels to the conventional bottom SiO_2/In_2O_3 transistor channel. To this end we emphasize that the formation of additional "conventional" parallel channels alone cannot be held solely responsible for the enhanced electron transport observed in QSL-III transistors since such assumption will imply the somewhat unrealistic co-existence of 5–10 parallel channels in order to account for the dramatically enhanced electron mobility measured. Co-existence of several parallel conventional channels is also not expected to alter the temperature dependence of the electron transport which should remain temperature activated and similar to that of single oxide transistors. It may further be argued that even if such multiple channels were to exist it would have been difficult to manipulate the free electron concentration with the gate field due to significant field attenuation occurring across each channel. Therefore, on the basis of this discussion and experimental findings we argued that the nature of electron transport in QSLs-based transistors is fundamentally different to the transport processes in conventional single oxide devices.

To better understand the charge transport characteristics of the different oxide layers, we have analysed the interplay between two key conduction mechanisms, namely trap-limited conduction (TLC) and percolation conduction (PC). Indeed, analysis of the gate-field dependence of μ_{LIN} shown in Figure S9 reveals that electron transport in single metal oxide based transistors is dominated by a characteristic TLC mechanism (Figure S16–S17) whilst transport in QSL-I/III transistors is dominated by PC - two significantly different transport processes. This difference is most likely attributed to the different electronic properties of the two active channels and particularly their Fermi energies. Specifically, in metal oxides the high mobility states may become more accessible in systems where E_F is closer to the mobility edge.[57-58] Since the E_F in oxide QSLs is higher than that of In_2O_3 (Figure S5), i.e. the layer in which electron transport is believed to take place, access to those highly delocalised states becomes easier hence leading to higher electron mobility. These findings further support the idea that electron conduction within the QSLs-based devices is significantly different from that in single layer ZnO and In_2O_3 based devices, and that it is most likely determined by the nature of the low-dimensional oxide heterointerface(s).

In our effort to either prove or disprove the existence of confined electrons within the QSLs, we have attempted to determine the concentration and depth-profile of electrons within the different oxide channels using the capacitance-voltage (C-V) profiling technique.[11, 59-61] C-V measurements were performed using the metal-insulator-semiconductor (MIS) device structure shown in **Figure 6**a. The hybrid AlO_X/ZrO_2 dielectric was chosen since QSL-based transistors made with this system were found to yield optimum performance while its thickness is comparable to that of the semiconducting channels. In the case of semiconducting heterostructures with quantum confinement, the C-V technique enables the determination of the

apparent free carrier concentration ($N_{C\text{-}V}$) as well as the presence and location of the confined electrons within the heterostructure.[11, 59-61] In Figure 6b the measured C-V characteristics are presented for devices based on ZnO, In_2O_3, QSL-I and QSL-III. MIS devices based on ZnO and In_2O_3 exhibit typical C-V behaviour with the accumulation ($V_G \geq 2$ V) and depletion regimes ($V_G \leq 0.5$ V) clearly visible. QSL-I and QSL-III based devices on the other hand exhibit significant differences with most notable ones the dramatic shift of the C-V curves to more negative V_G and the appearance of differently shaped depletion regimes. To investigate the possible existence and spatial location of the confined electrons within the QSLs, we calculated the $N_{C\text{-}V}$ using:[59-60]

$$N_{C-V} = -\frac{2}{\varepsilon\varepsilon_0 q A^2 d(C^{-2})/dV} \quad (4)$$

as a function of depth (x):

$$x(\mathrm{V}) = \mathrm{A}\varepsilon\varepsilon_0\left(\frac{1}{\mathrm{C(V)}} - \frac{1}{\mathrm{C_{oxide}}}\right) \quad (5)$$

Here, ε is the permittivity of the semiconductor, ε_0 the dielectric constant of vacuum and A is the active area of the device.

Figure 6c presents the $N_{C\text{-}V}$ profiles as a function of depth *i.e.* the distance from the top electrode. Unlike ZnO and In_2O_3 devices where $N_{C\text{-}V}$ remains relatively low and uniform across the semiconductor layer, the apparent electron density within QSL-I and QSL-III appears consistently higher and non-uniform. For QSL-I devices $N_{C\text{-}V}$ exhibits a clear maximum at a depth of ~10 nm from the top electrode which suggests the presence of confined electrons. For QSL-III based devices, the electron confinement is better defined and appears at a slightly increased depth of ~15 nm. The calculated depths for the confined electrons in both QSLs coincide with the expected position of the critical heterointerfaces as these are depicted in Figure 4b and 4d. Similar signatures of electron confinement are also present in C-V measurements taken at room temperature. The lack of two $N_{C\text{-}V}$ maxima for QSL-I/III devices,

which would indicate the existence of a confined electron system at each critical heterointerface, is attributed to the relatively rough - compared to its thickness of ~5 nm - nature of the central ZnO layer (Figure 1a) and the inability to resolve with high enough accuracy the two discrete electron confinement layers as these are depicted in Figure 4d. As a result, the $N_{C\text{-}V}$ peak appears broader. On the basis of these findings we conclude that a significant concentration of free electrons appears to be confined at the critical oxide heterointerfaces in accordance with the energy band diagrams of Figure 4b and 4d. To be noted that similar confinement signatures were observed in QSL-III based MIS devices measured at room temperature as well as in MIS structures made on 100 nm-thick SiO_2 dielectrics.

The ability to grow ultra-thin layers of oxide dielectrics (*e.g.* ZrO_2) and semiconducting QSLs at low temperatures enables the creation of transistors with state-of-the-art electron mobility values and low voltage operation on arbitrary substrates. To further demonstrate the opportunities the QSL transistor technology has to offer, we fabricated bottom-gate, top-contact transistors on glass and plastic substrates employing the AlO_X/ZrO_2 as the gate dielectric (see *Experimental Section*). The bottom-gate staggered device geometry used was similar to that used for transistors made on Si/SiO_2 with only exceptions the gate electrode and gate dielectric materials employed. Because of the thin (~25 nm) and high-*k* (~9) nature of the bilayer AlO_X/ZrO_2 gate dielectric (C_i ~235 nF/cm^2),[31] as-prepared QSL-I/III transistors operate at significantly reduced voltages (**Figure 7**a). QSL-I transistors are found to exhibit consistently slightly lower mobility than QSL-III devices with a mean value ($\mu_{SAT(mean)}$) of ~37 cm^2/Vs as compared to the record value of ~40 cm^2/Vs for QSL-III devices (Figure 7b). We note that both mobility values are higher than those obtained for SiO_2-based transistors (Figure 5c). This difference is most likely attributed to improved microstructure of the semiconducting layers due to the epitaxial-like growth on top of the polycrystalline dielectric.[31, 47, 62-64] The low

operating voltage transistors also exhibit respectable on/off current ratios (~10^4) and mean subthreshold swings (SS = $dV_G/d[\log(I_D)]$) of ~275 mV/dec and ~160 mV/dec for QSL-I and QSL-III devices (Figure S18), respectively.

Finally, low operating voltage oxide QSL transistors were also fabricated on flexible polyethylene naphthalate (PEN) plastic substrates. As-prepared devices showed reduced performance with $\mu_{SAT(mean)}$ of ~8.5 cm^2/Vs and ~11 cm^2/Vs for QSL-I and QSL-III transistors, respectively (Figure S19 and S20). The reduced mobility values are attributed to the lower annealing temperature (<175 °C) used in order to avoid damaging the PEN substrate during the sequential spin cast-annealing steps used to grow the QSLs (see *Experimental Section*). Despite the mobility reduction, however, low-voltage QSL-based transistors are found to consistently outperform, in terms of electron mobility, low operating voltage transistors based on single layer ZnO and In_2O_3 channels fabricated on either glass (μ_{SAT} ~ 3–5 cm^2/Vs) or PEN (μ_{SAT} ~ 1–3 cm^2/Vs) substrates (Figure S21 and S22), respectively, clearly demonstrating the advantage of the proposed oxide QSL technology over conventional single oxide layer transistors.

In summary, we have demonstrated a new concept of solution-processed metal oxide quasi-superlattice transistors. In contrast to conventional single metal oxide devices, the performance level of our transistors is not limited by the carrier mobility of the individual semiconductor(s), and the associated structural layer defects, involved but instead is determined by the physical properties of the oxide heterointerfaces buried within the quasi-superlattice. Already, our proof of concept devices show dramatically enhanced electron mobility (>40 cm^2/Vs) that far exceed values reported for oxide transistors fabricated via solution at ≤200 °C[22, 26-28] while they compare favourably with oxide heterojunction-based transistors manufactured by different vacuum-based techniques (Table S1). On the basis of these results we argue that further

engineering of the band structure of the oxide quasi-superlattices – e.g. through appropriate material combinations and/or suitable chemical doping – could lead to even higher device performance and enable the design and fabrication of devices, circuits and systems on arbitrary substrate materials via spin-casting or other large-area compatible deposition methods such as spray pyrolysis, printing as well as numerous vacuum-based techniques. The unique combination of low-cost, low-temperature processing with the exceptionally high electron mobility achieved can potentially fulfil the ever increasing demand for high performance thin-film transistor technologies across a wide range of applications spanning from next-generation ultra-high-definition displays to future generations high-volume transparent electronics.

Experimental Section:

Oxide precursor preparation and processing

Zn ammine complex solutions were prepared by dissolving ZnO hydrate ($ZnO{\cdot}xH_2O$, 97% Sigma-Aldrich) in ammonium hydroxide (Alfa Aesar, 50% V/V) at 10 mg/mL. As-prepared solutions were then stirred rigorously at room temperature for 2 h. This process yielded a clear transparent Zn ammine complex based solution. For the growth of In_2O_3 layers, the precursor solution was prepared by dissolving anhydrous indium nitrate ($In(NO_3)_3$, 99.99% Indium Corporation) in deionized (DI) water at a concentration of 30 mg/mL. The solution was subjected to rigorous stirring at room temperature for 60 min before use. For solution-processable gallium oxide (Ga_2O_3), the precursor solution was prepared by dissolving gallium nitrate hydrate ($Ga(NO_3)_3{\cdot}xH_2O$, 99% Sigma-Aldrich) in DI water at a concentration of 10 mg/mL. The solution was also stirred at room temperature for 1 h before use. For ZrO_2 deposition the precursor solution was synthesised by dissolving Zr(IV) acetylacetonate ($Zr(C_5H_7O_2)_4$) (98% Sigma–Aldrich) in N,N-dimethylformamide (DMF, C_3H_7NO) (Sigma–Aldrich) at a concentration of 0.15 M in inert gas atmosphere with the addition of an equal

molar concentration of ethanolamine (MEA, C_2H_7NO) (≥99% Sigma–Aldrich). The solution was then subjected to rigorous stirring at 70–80 °C for 1 h before use.

Substrate preparation

Heavily-doped silicon (Si^{++}) wafers acting as the common gate electrode and a thermally grown SiO_2 layers (400 nm) as the gate dielectric were used as the transistors substrates. Prior to spin casting the semiconductor layer, the substrates were cleaned by sonication in a solvent bath lasting for ~10 min. The four steps were: (1) sonication in DI water with 2 mL Decon 90, (2) sonication in DI water, (3) sonication in acetone, (4) followed by sonication in isopropanol. The residual solvent was then dried by blowing dry nitrogen over the surface of the substrates. Finally, the substrates were exposed to UV ozone for 10 min to remove residual hydrocarbons from the SiO_2 surface. All other types of device and sample substrates used in this work were cleaned using the same process protocol, except for plastic films (i.e. polyethylene naphthalate, PEN, Teijin Dupont Films) for which the sonication bath step was performed using purified DI water in order to remove dust particles and other impurities.

Metal oxide layers deposition and transistor fabrication

For the In_2O_3 and ZnO TFTs, the semiconductor thin-film deposition was carried out by spin-casting the precursor solutions onto the Si^{++}/SiO_2 substrates at 4000 rpm for 30 sec in ambient air, followed by a post-deposition thermal-annealing process for 30 min at 180–200 ℃ in ambient air. The overall layer thickness was controlled by the number of deposition steps performed. For single layer ZnO and In_2O_3 transistors, semiconductors were grown using a two deposition step process in order to increase the overall thickness of the channel layer. Fabrication of the In_2O_3 and ZnO transistors was completed with the thermal evaporation of 40 nm-thickness Au and Al top source and drain (S-D) electrodes through a shadow mask in high

vacuum (~10^{-6} mbar), respectively. Fabrication of heterojunction and QSL-based transistors was performed using identical spin-casting and thermal-annealing conditions to those used for the fabrication of single layer ZnO and In_2O_3 transistors with the exception that each layer growth was performed using a single-step deposition in order to maintain a similar channel layer thickness with that of single oxide devices. Similarly, deposition of Ga_2O_3 layers was carried out using a single deposition step. Top S-D electrodes in QSLs transistors were formed by thermal evaporation of 40 nm-thick Au through a shadow mask in high vacuum. For transistors prepared on Si/SiO_2 wafers, the channel width (W_{ch}) and length (L_{ch}) were 1000 μm and 50 μm, respectively, while for the low operating voltage transistors the channel dimensions of W_{ch} = 1000 μm and L_{ch} = 30 μm, were employed. For each transistor configuration the semiconducting layer(s) was patterned by wiping the as-deposited wet precursor film prior to thermal annealing/conversion. The latter process step together with the use of large W_{ch}/L_{ch} ratios (≥20) ensured minimum contribution of fringing currents and elimination of associated errors in electron mobility calculations.

Absorption spectroscopy of metal oxide films

Several ZnO and In_2O_3 films were spin-cast onto quartz substrates from the precursor solutions in air. As-spun layers were then annealed at 200 °C for 30 minutes in air. Ultraviolet-visible (UV-Vis) absorption measurements were carried out with a Shimadzu UV-2600 ultraviolet-visible spectrophotometer. Transmittance and reflectance measurements were carried out for each sample. The transmittance corrected for reflectance was derived from the raw transmittance + raw reflectance.

Tauc analysis[38-39] was used to approximate the band gap of each film. The technique entails plotting $(\alpha h\nu)^X$ against the incident photon energy ($h\nu$), then extrapolating the linear part of

the plot to $(\alpha h\nu)^X = 0$. Here, α is the optical absorbance of the material and X is an exponent that depends on the nature of the semiconductor band-gap i.e. direct or indirect. For direct band-gap semiconductors $X = 2$ is used, whilst for indirect band-gap semiconductors $X = 1/2$ is used. Since the nature of the band gap in In_2O_3 is still under debate,[65-67] we have here used both approaches. ZnO is known to be a direct band gap semiconductor[68] thus the value of $X = 2$ was employed. By assuming that the optical properties of layers with thickness >20 nm are representative of the bulk semiconductors, the increase in band-gap (ΔE_G) relative to the bulk was evaluated for each semiconducting layer.

Processing of high-k dielectrics for metal-insulator-semiconductor capacitors and low-operating voltage transistors

The metal-insulator-semiconductor (MIS) capacitors and low-voltage transistors were fabricated using a combination of metal oxides as the dielectric layers. Devices were fabricated on glass as well as plastic substrates. Following substrate cleaning, 40 nm thick Al gate electrodes were deposited by thermal evaporation through a shadow mask. The native aluminium oxide was grown on the surface of the Al gate electrodes using a low-pressure mercury UV lamp, which emits at wavelengths of 253.7 nm (97% of overall power) and of 184.9 nm (3% of overall power) at total output power of approximately 5 mW/cm^2 (at a distance of 1 cm). The entire UV illumination was taken in ambient air for 10–12 h. Following, the ZrO_2 film was grown by spin-coating the precursor solution at 3000 rpm for 60 s in nitrogen followed by curing the samples using a metal halide lamp of 250 mW/cm^2, equipped with a UVA spectrum filter, for 90 min in ambient air.

Grazing incident diffraction (GID) and X-ray reflectivity (XRR) measurements

Grazing incident diffraction and X-ray reflectivity were carried out on beamline G2 in Cornell High Energy Synchrotron Source (CHESS) at Cornell University (USA). The samples were aligned on a Kappa diffractometer with the X-ray energy of 13.65 keV ($\lambda = 0.0908$ nm) through a Be single-crystal monochromator. The data was collected using a 640-element 1D diode-array detector, with a set of 0.1° Soller slits mounted on the detector arm to provide an in-plane resolution of 0.16°. The grazing incident angle was fixed at 0.1° in grazing incident diffraction. The XRR results were simulated by Parratt32 software program developed at HMI in Berlin (Germany).

Transistor characterisation

Device electrical characterisation was carried out under high vacuum (~10^{-5} mbar) at temperature ranging from 77 K to 305 K using a cryogenic probe station (Janis ST-500). Electrical measurements were carried out with a Keithley 4200 semiconductor parameter analyser. Electron mobility was extracted from the transfer curves in the linear/saturation regime using the gradual channel approximation:

$$\mu_{LIN} = \frac{L_{ch}}{C_i W_{ch}} \cdot \frac{\partial I_D}{\partial V_G} \cdot \frac{1}{V_D}, \quad (6)$$

$$\mu_{SAT} = \frac{L_{ch}}{C_i W_{ch}} \cdot \frac{\partial^2 I_D}{\partial V_G^2}, \quad (7)$$

where, C_i is the geometrical capacitance of the SiO_2 dielectric layer, and L_{ch} and W_{ch} are the length and width of the transistor channel, respectively.

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Figure Legends

Figure 1. Structural analysis of low-dimensional solution-processed ZnO and In_2O_3 layers. (**a**) High-resolution transmission electron microscope (HRTEM) cross-section images of the SiO_2/ZnO interface. Left: low-magnification TEM image confirms an ultra-thin and continuous ZnO film. Right: higher-magnification TEM image reveals the presence of polycrystalline ZnO regions with clearly visible lattice fringes. (**b**) AFM phase images of ZnO film with individual grains clearly visible, the calculated rms ZnO surface roughness was ~0.43 nm. (**c**) GID measurement (X-ray wavelength λ= 0.0908 nm) shows powder-like crystallization, *i.e.* different crystalline orientations, coexisting in the ZnO film. (**d**) HRTEM cross-section images of the SiO_2/In_2O_3 interfaces reveal the presence of an ultra-thin and smooth In_2O_3 film with highly oriented crystalline domains. (**e**) AFM image indicates the surface roughness of the In_2O_3 film is ~0.20 nm. (**f**) GID analysis (X-ray wavelength λ= 0.0908 nm) shows similar powder-like crystallization characterising the In_2O_3 layers.

Figure 2. Energy quantisation in solution processed ZnO and In_2O_3 layers. (**a**) Schematic illustration of the sample configuration used for the optical absorption measurements where *L* represents the layer thickness of the spin coated oxide semiconductor. (**b**) Plot of the change in optical band gap (ΔE_G) calculated via Tauc analysis versus film thickness (*L*) for several ZnO layers with respect to that of bulk ZnO (L > 20 nm). (**c**) Plot of ΔE_G calculated via Tauc analysis assuming a direct (squares) and an indirect (circles) band gap, versus film thickness for several In_2O_3 layers with respect to that of bulk In_2O_3 (L > 20 nm). In both plots the solid red lines illustrate the calculated ΔE_G for an infinite quantum well using Equation 3.

Figure 3. Structural analysis of metal oxide quasi-superlattices (QSLs). (**a**) Schematics of the different layered structures grown including heterojunctions (In_2O_3/ZnO, In_2O_3/Ga_2O_3,

ZnO/Ga_2O_3) and multilayer QSLs consisting of $In_2O_3/ZnO/In_2O_3$ (QSL-I), $In_2O_3/Ga_2O_3/ZnO$ (QSL-II) and $In_2O_3/Ga_2O_3/ZnO/Ga_2O_3/In_2O_3$ (QSL-III). (**b**) Measured (blue lines) and calculated (red-dashed lines) XRR spectra of the In_2O_3/ZnO and QSL-II layered structures. (**c**) AFM surface phase images of the different structures namely; heterojunction, QSL-I, QSL-II and QSL-III. (**d**) TOF-SIMS analysis for a QSL-III grown on Si^{++}/SiO_2 substrate. Here a thicker top layer of In_2O_3 (~25 nm) was employed in order to stabilize the ion beam during measurement.

Figure 4. Energy levels of the metal oxide semiconductors. (**a**) Measured energy levels of the individual oxides used in QSL-I before contact. (**b**) Schematic energy band diagram of QSL-I after contact. (**c**) Energy levels of the individual oxides used in QSL-III before contact. (**d**) Schematic energy band diagram of QSL-III after contact. The energy bandgaps, Fermi energy levels and valence band maximum (VBM) energy for each oxide material were determined using UV-Vis absorption, KP and UPS measurements, respectively (see Supporting Information Figures S4–S6).

Figure 5. Electrical characterisation of thin-film transistor. (**a**) Schematics of the heterojunction (HJ) and QSLs based metal oxide transistors developed using Si^{++} and SiO_2 (400 nm) as the gate and the gate dielectric, respectively. (**b**) Transfer characteristics measured from transistors with different oxide-based channel layers including single layer ZnO and In_2O_3. (**c**) Arrhenius plots of the temperature dependence of saturation mobility (μ_{SAT}) for ZnO, In_2O_3, In_2O_3/ZnO heterojunction, QSL-I, QSL-II and QSL-III based transistors measured at $V_G = 80$ V and $V_D = 100$ V.

Figure 6. **Analysis of electron confinement in metal oxide quasi-superlattices.** (**a**) Schematic of the MIS structures used for the C-V profile analysis. (**b**) Capacitance-voltage (C-V) measurements obtained at 77 K for ZnO, In_2O_3, QSL-I and QSL-III based MIS devices. (**c**) Apparent free electron ($N_{C\text{-}V}$) profiles as a function of depth for MIS devices based on the different semiconducting layers calculated from the C-V data in (**b**).

Figure 7. **Low operating voltage transistors based on metal oxide quasi-superlattices.** (**a**) Representative sets of transfer characteristics measured from transistors based on QSL-I and QSL-III channels. (**b**) Histogram plots of the saturation mobility (μ_{SAT}) calculated for a number of low-voltage QSL-I and QSL-III based transistors fabricated on the same substrates. The Gaussian fitting curves are guides to the eye.

List of Figures

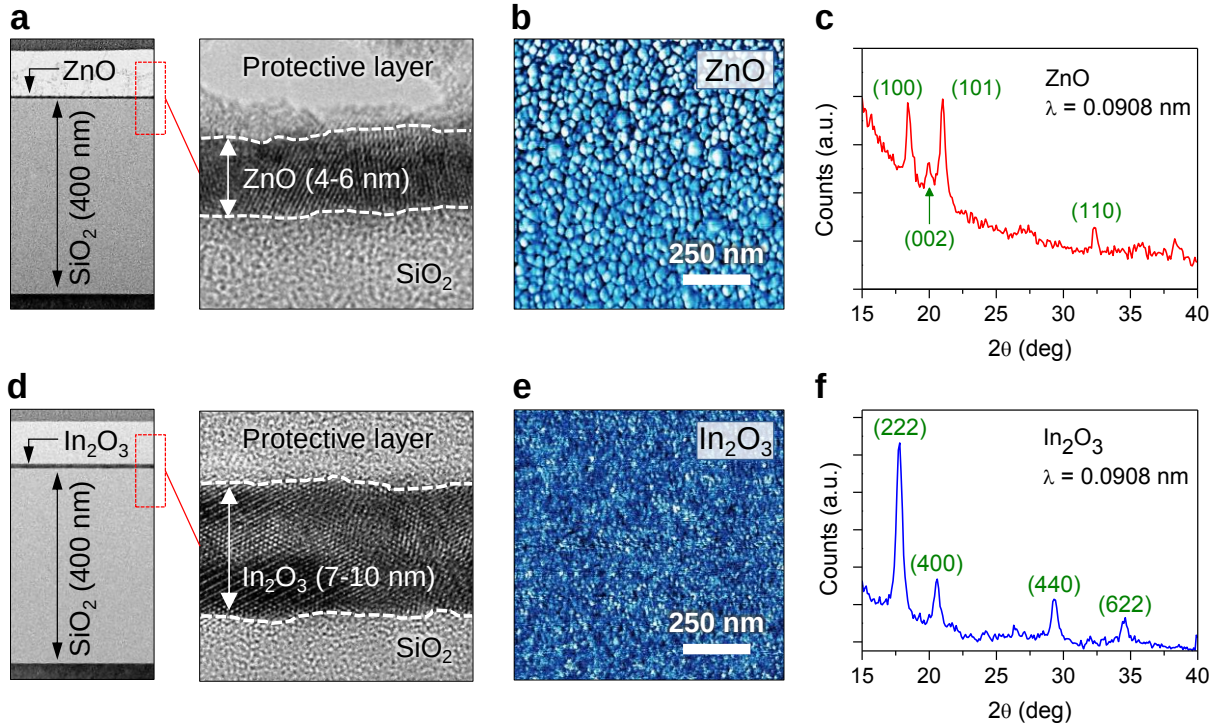
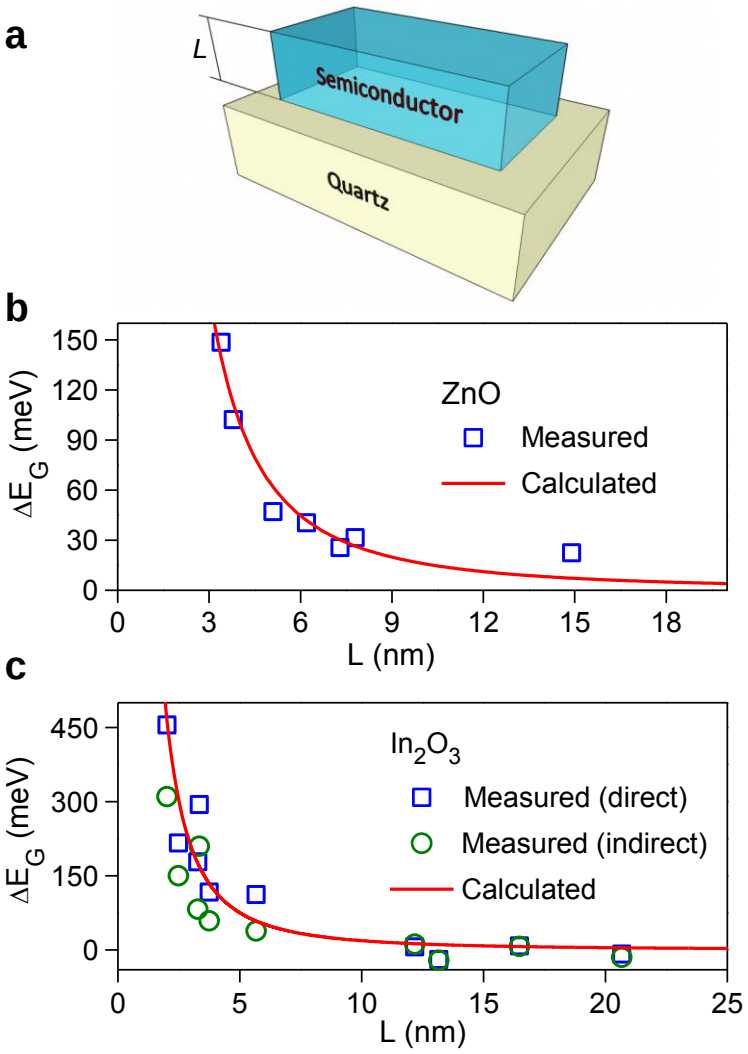


Figure 1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Semiconductor
Quartz
b
ZnO
Measured
Calculated
ΔE_G (meV)
L (nm)
c
In2O3
Measured (direct)
Measured (indirect)
Calculated
ΔE_G (meV)
L (nm)

Figure 2

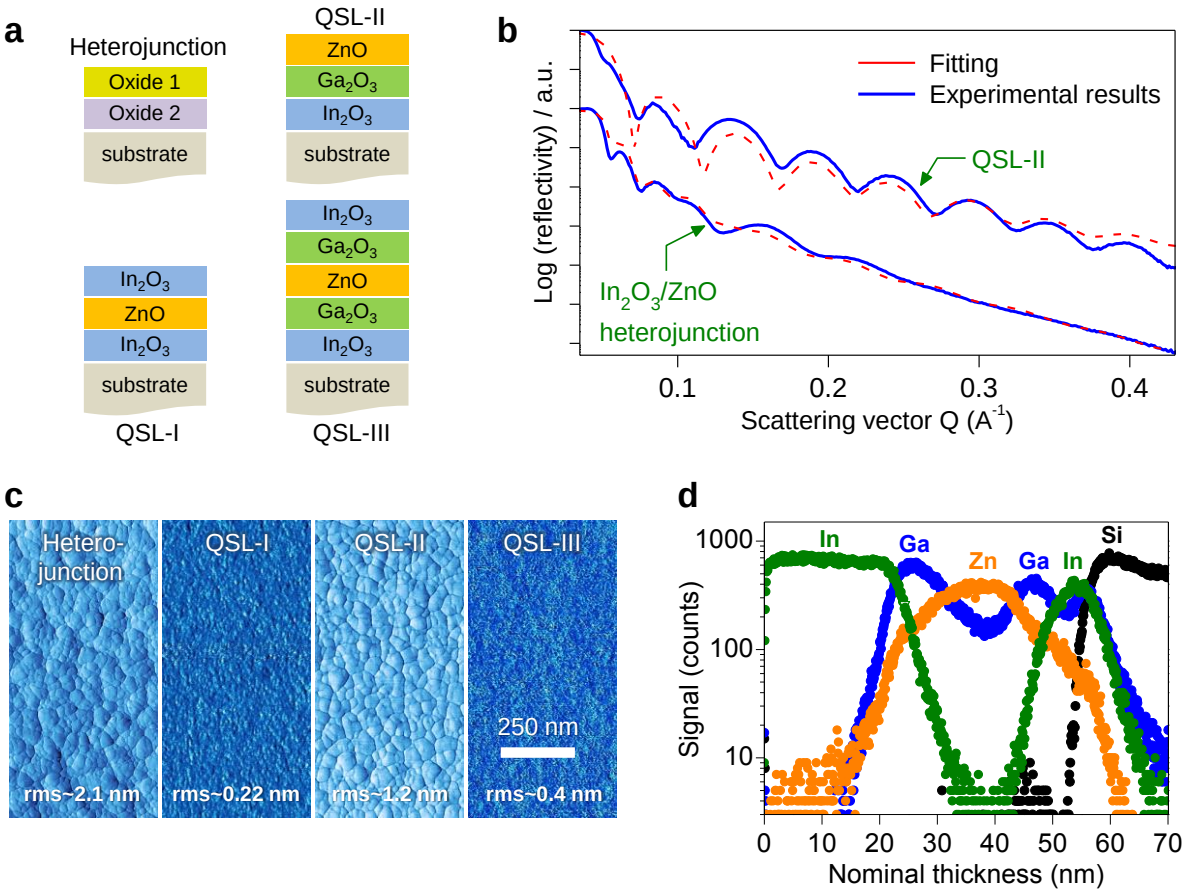
a
Heterojunction
Oxide 1
Oxide 2
substrate
QSL-I
QSL-II
ZnO
Ga_2O_3
In_2O_3
substrate
QSL-III
b
Fitting
Experimental results
QSL-II
In_2O_3/ZnO
heterojunction
Log (reflectivity) / a.u.
Scattering vector Q (A^{-1})
c
Hetero-junction
QSL-I
QSL-II
QSL-III
250 nm
rms~2.1 nm
rms~0.22 nm
rms~1.2 nm
rms~0.4 nm
d
In
Ga
Zn
Ga
In
Si
Signal (counts)
Nominal thickness (nm)

Figure 3

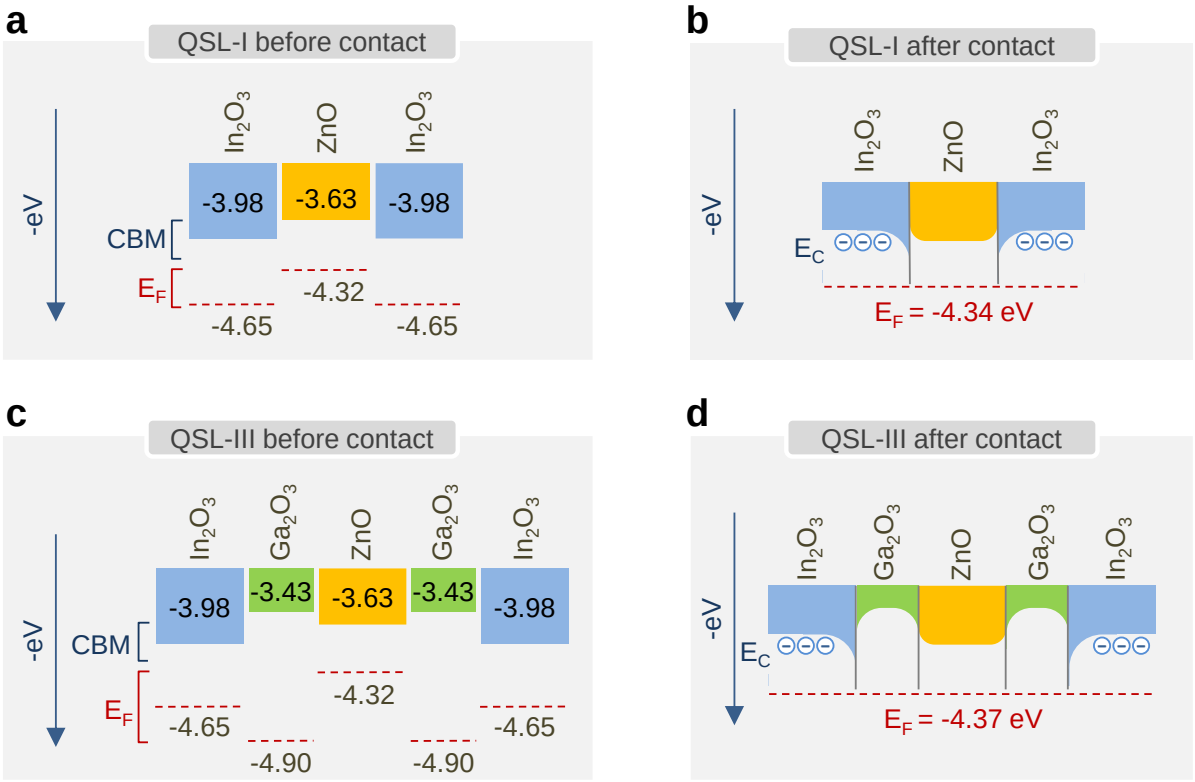
a
QSL-I before contact
In2O3
ZnO
In2O3
-eV
-3.98
-3.63
-3.98
CBM
EF
-4.32
-4.65
-4.65
b
QSL-I after contact
In2O3
ZnO
In2O3
-eV
EC
EF = -4.34 eV
c
QSL-III before contact
In2O3
Ga2O3
ZnO
Ga2O3
In2O3
-eV
-3.98
-3.43
-3.63
-3.43
-3.98
CBM
EF
-4.65
-4.32
-4.65
-4.90
-4.90
d
QSL-III after contact
In2O3
Ga2O3
ZnO
Ga2O3
In2O3
-eV
EC
EF = -4.37 eV

Figure 4

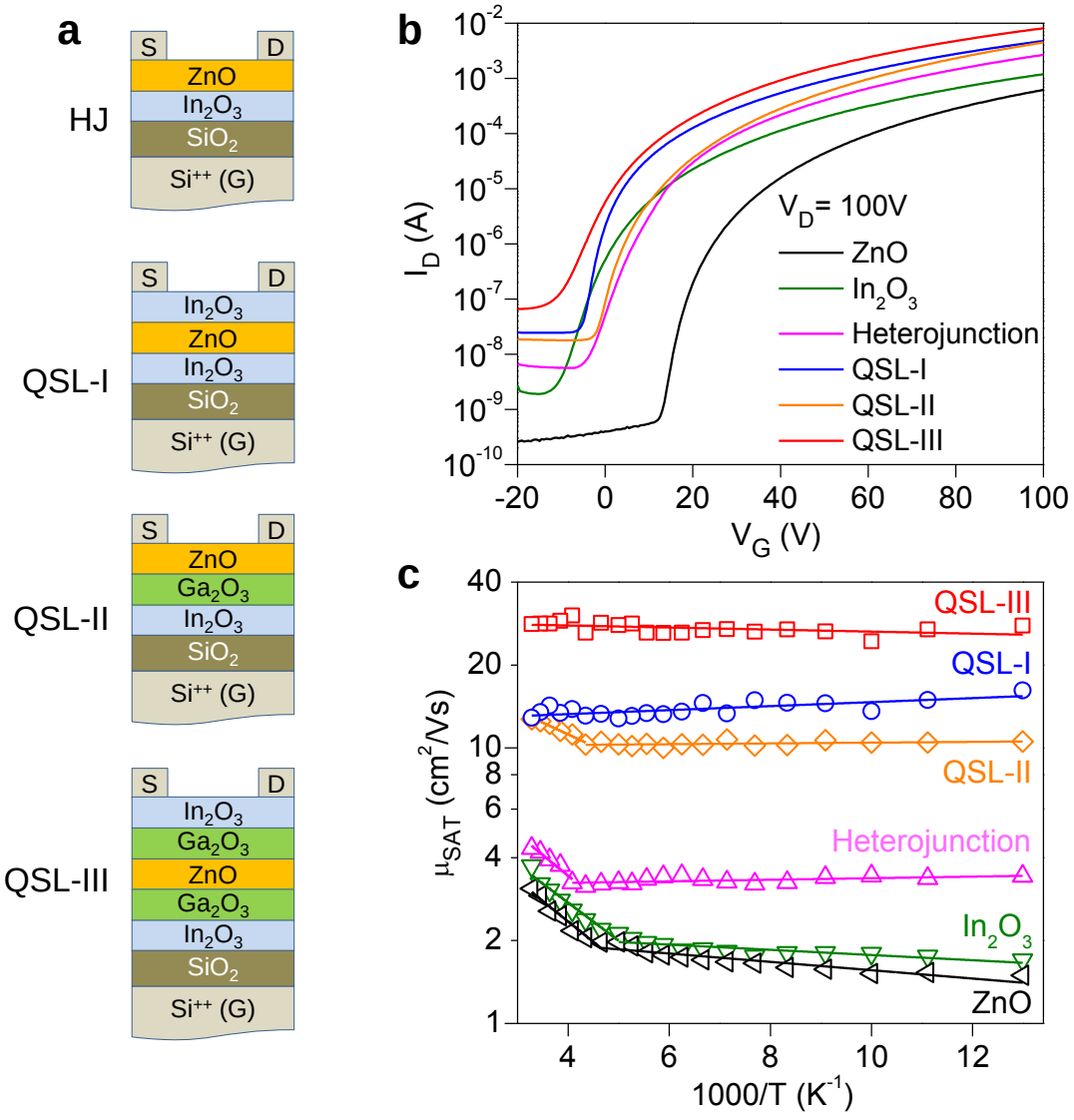
a
HJ
QSL-I
QSL-II
QSL-III
S
D
ZnO
In2O3
Ga2O3
SiO2
Si++ (G)
b
ID (A)
VG (V)
VD= 100V
ZnO
In2O3
Heterojunction
QSL-I
QSL-II
QSL-III
c
μSAT (cm2/Vs)
1000/T (K-1)
QSL-III
QSL-I
QSL-II
Heterojunction
In2O3
ZnO

Figure 5

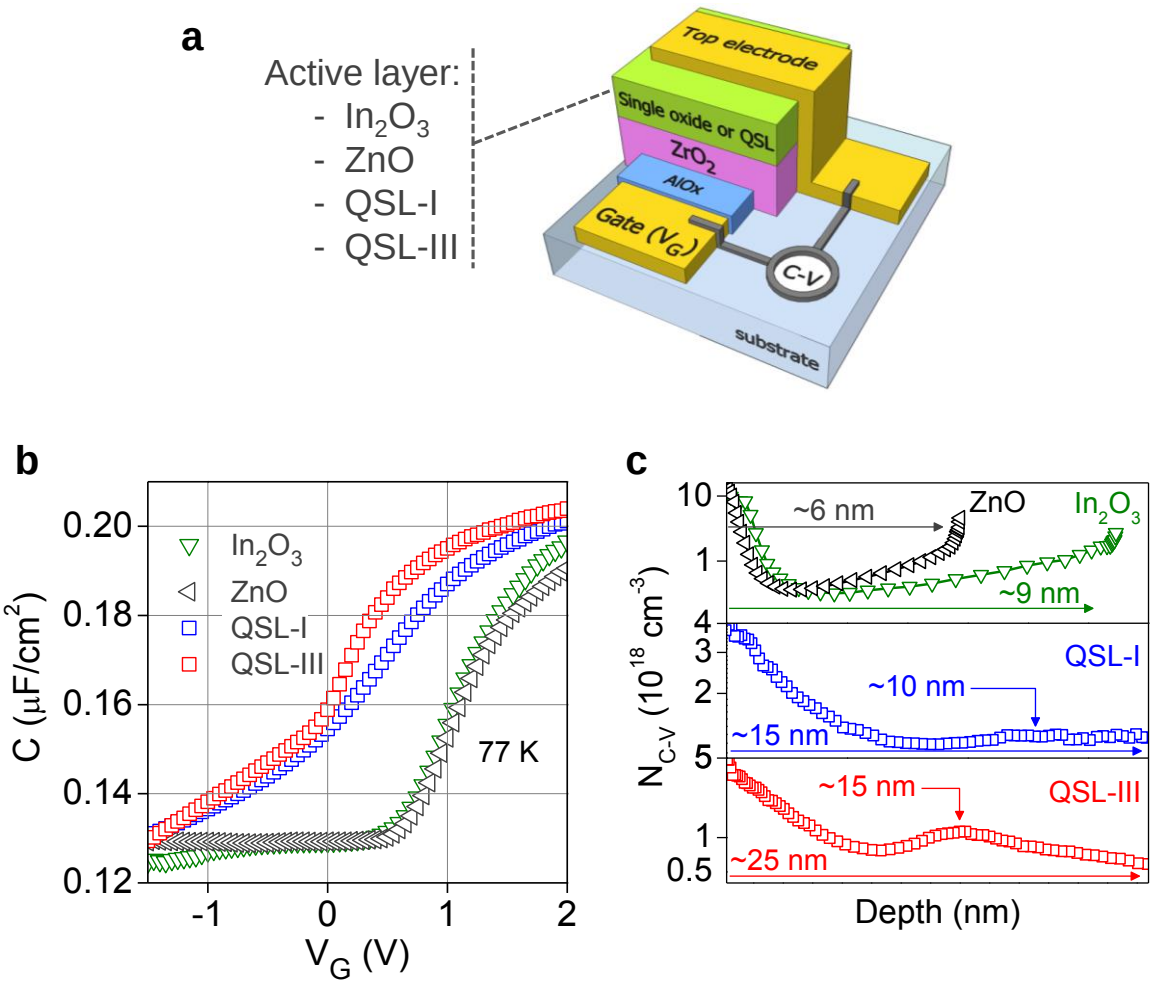
a
Active layer:
- In_2O_3
- ZnO
- QSL-I
- QSL-III
Top electrode
Single oxide or QSL
ZrO_2
AlOx
Gate (V_G)
C-V
substrate
b
C ($\mu F/cm^2$)
In_2O_3
ZnO
QSL-I
QSL-III
77 K
V_G (V)
c
N_{C-V} (10^{18} cm^{-3})
~6 nm
ZnO
In_2O_3
~9 nm
QSL-I
~10 nm
~15 nm
~15 nm
QSL-III
~25 nm
Depth (nm)

Figure 6

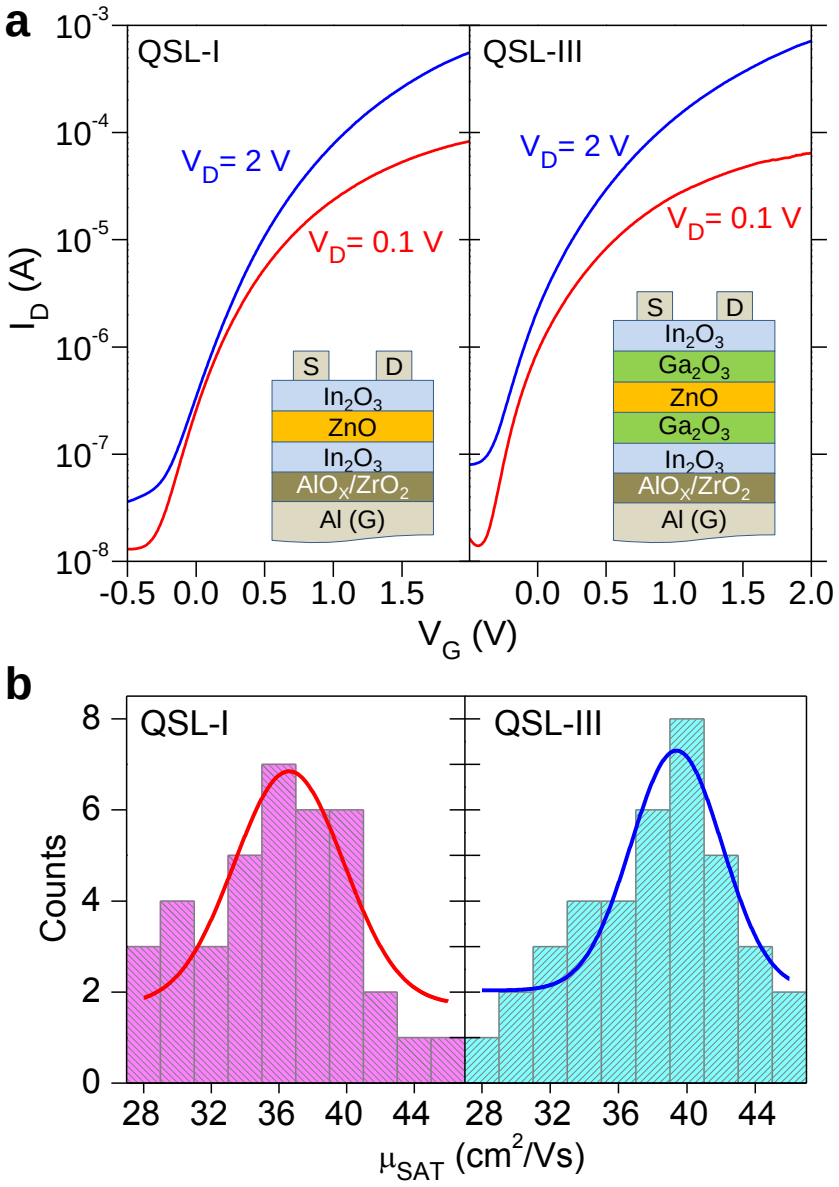
a
QSL-I
QSL-III
V_D= 2 V
V_D= 0.1 V
I_D (A)
V_G (V)
S
D
In_2O_3
ZnO
In_2O_3
AlO_X/ZrO_2
Al (G)
In_2O_3
Ga_2O_3
ZnO
Ga_2O_3
In_2O_3
AlO_X/ZrO_2
Al (G)
b
QSL-I
QSL-III
Counts
μ_{SAT} (cm^2/Vs)

Figure 7

The table of contents entry:

A new concept of solution-processed low-dimensional metal oxide quasi-superlattice (QSL)-based transistors is demonstrated. In contrast to conventional single oxide semiconductor-based devices, the performance level of the QSL transistors is determined by the physical properties of the oxide heterointerfaces buried within the superlattice rather than the electronic properties of the individual materials employed. As a result, QSL transistors show dramatically enhanced electron mobilities (>40 cm^2/Vs) that exceed values reported for conventional metal oxide transistors processed from solution at ≤200 °C.

TOC: