# Assessment of HVDC Technologies for an Offshore MTDC Grid

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# Abstract

This thesis examines various HVDC converter technologies that could be used in offshore Multi-Terminal DC (MTDC) grids. MTDC grids rely on AC/DC converters to interface with AC systems and also for control services. Two AC/DC topologies were compared, the half-bridge Modular Multi-level Converter (MMC) and the Alternate Arm Converter (AAC). As new DC system voltages emerge the DC/DC converter could be an enabling technology for interconnection and future MTDC networks. As yet there is no consensus on DC/DC converter topology and a critical comparison of several potential designs was conducted. An MMC based DC/DC converter had distinct advantages compared with other designs. Several average value converter models of the converters were developed to allow efficient simulation of MTDC networks, while maintaining a high level of accuracy of the converter characteristics. These models were verified with full switching models for steady state and fault conditions. Two offshore MTDC networks were studied; a four-terminal network, and a MTDC network. The four-terminal network used a normally open point to connect two existing point-to-point links, allowing reconfiguration in the event of a DC fault. The MTDC network uses a DC/DC converter to interconnect a bipole HVDC link with the previously studied four-terminal network. Several simulation studies show how new converters can improve the operation of a MTDC and provide additional capabilities such as DC fault blocking.

# Declaration of Originality

I, hereby declare that this thesis is the result of my own work, and that any ideas or quotations from the work of others, published or otherwise, are appropriately referenced. This work presented in this thesis was carried out from January 2012 to October 2015 under the supervision of Prof. Tim C. Green at Imperial College London.

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# Nomenclature

| | |
|---|---|
| AAC | Alternate Arm Converter |
| ADM | Alternate Discontinuous Mode |
| AVM | Average Value Model |
| BM | Blocking Module |
| CCM | Continuous Conduction Mode |
| CSC | Current Source Converter |
| CTLC | Cascases Two-Level Converter |
| DCM | Discontinuous Conduction Mode |
| EENS | Expected Energy Not Supplied |
| EES | Expected Energy Supplied |
| ENTSO-E | European Network of Transmission System Operators for Electricity |
| FB | Full-Bridge |
| FSM | Full Switching Model |
| HB | Half-Bridge |

| | |
|---|---|
| HVAC | High Voltage Alternating Current |
| HVDC | High Voltage Direct Current |
| IGBT | Insulated Gate Bipolat Transistor |
| LCoE | Levelised Cost of Energy |
| MAVM | Modified Average Value Model |
| MMC | Modular Multilevel Converter |
| MTBF | Mean Time Between Failure |
| MTDC | Multi-Terminal DC |
| MTTR | Mean Time To Repair |
| MWh | Megawatt Hour |
| NOP | Normally Open Point |
| PI | Proportional Integral |
| PWM | Pulse Width Modulation |
| RES | Renewable Energy Source |
| rms | Root Mean Square |
| SHE | Selective Harmonic Elimination |
| THD | Total Harmonic Distortion |
| VSC | Voltage Source Converter |
| XLPE | Cross-Linked Polyethylene |

# 1. Introduction

This thesis will describe work on particular aspects of offshore transmission networks aimed at increasing renewable energy penetration as part of a response to climate change. It is widely accepted that the increase in greenhouse gases since the pre-industrial era (1861-1890) has contributed significantly to global climate change [1]. Climate change has had direct impact on humans and natural systems across the world. Therefore, it is essential to mitigate against further dangerous increases in the temperature of the climate system caused by greenhouse gas emissions [2]. It is believed that limiting the global mean temperature rise to 2°C above pre-industrial times could avoid many irreversible climate system changes [3]. The Kyoto Protocol calls for the reduction in six greenhouse gases including the main contributor $CO_2$ [4, 1].

A significant producer of $CO_2$ is the use of fossil fuels to power homes and industry [1]. Thus a key step in preventing further climate change is to decarbonise the energy sector. This decarbonisation can be achieved by using carbon neutral fuel sources, such as Renewable Energy Sources (RES), and by safeguarding forests [1, 5]. The leading RES is bioenergy, followed by hydropower and wind generation [5]. At present 5.3% of global power generation comes from RES [6].

The European Commission has put regulatory framework in place to reduce carbon emissions and increase the use of RES for its member states. The targets for 2020 and 2030 are given in Table 1.1.

| Measure | EU 2020 | EU 2030 |
|---|---|---|
| Reduce greenhouse gases compared to 1990 levels | 20% | 40% |
| Increase share of renewable energy sources | 20% | 27% |
| Increase energy efficiency[1] | 20% | 27% |

**Table 1.1.:** European carbon reduction targetsThe European Commission [7, 8]

The 2020 targets were launched in 2010 to create conditions for sustainable economic growth and Figure 1.1 shows the increase of RES into the EU energy system since 2004.

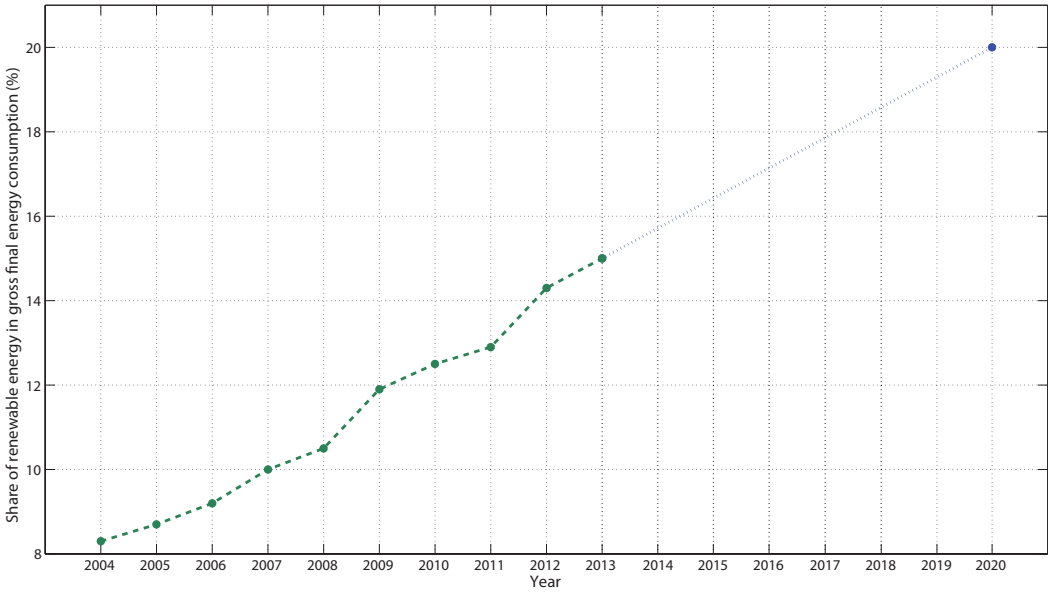



**Figure 1.1.:** Share of renewable energy in gross final energy consumption [9]

These European targets have specific implications for the UK energy system, namely a target of 15 % of all energy used is to come from RES by 2020, this includes electricity, heat and transport [10]. This target translates to 30% of electricity generation to come from RES [11]. Toward the end of 2014 the penetration of renewable generation in to the UK electricity system was 17.8% [11]. Offshore wind generation is likely to be a large contributor to meeting the renewable targets for

the UK, with more than 33 GW of potential capacity identified in UK waters [12]. Offshore wind has the advantages of a higher energy output and less constraints from public planning issues when compared to onshore wind generation [13]. However, building wind generation offshore has a high capital requirement, and in 2012 the Round 3 developments had a levelised cost of energy (LCoE) of £134 per megawatt hour (MWh) which was 1.6 times greater than the cost of gas generation [14]. The estimated LCoE at the end of 2014 was 121 £/MWh, and the cost is mainly being driven down by the use of larger wind turbines [15].

## 1.1. Offshore Transmission Networks

### 1.1.1. AC versus DC Transmission

Traditionally High Voltage AC (HVAC) has been used to transmit large amount of electrical energy. This is due to the key elements required for AC transmission being available from the beginning of the 20th century [16]. The transformer enables easy conversion to higher voltages which enables efficient transport of energy over long distances, and the AC circuit breaker can interrupt AC faults effectively [17].

In recent years High Voltage DC (HVDC) has become increasingly popular for bulk power transmission over great distances. This is due to advancement in semiconductor devices and to several advantages that HVDC has over traditional HVAC transmission. The first being that HVDC is not limited in the distance it can transfer power, Figure 1.2 shows the cost each transmission technology as the distance is increased for cable technology.

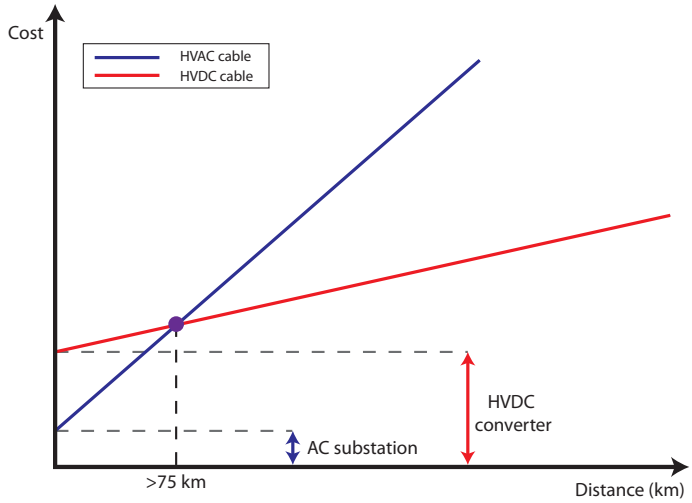



**Figure 1.2.:** Distance versus cost for HVAC and HVDC cables

There is an initial setup cost associated with HVDC due the necessity of an AC/DC converter, at each end of the link, and for short cable distances HVAC is the more economic solution. For longer cables, HVAC has a limited power transfer due to the high capacitance of the cable. As the cable is a closed conductor, this causes increased capacitance and thus an increased capacitive charging current [18]. For cable lengths greater than approximately 75 km, additional reactive power compensation is necessary to charge the cable which makes the option uneconomical [18]. Alternatively HVDC transmission can be used as the cables only require charging once and it does not suffer reactive losses [19]. For overhead lines HVAC is the economic choice up to approximately 500 km [20].

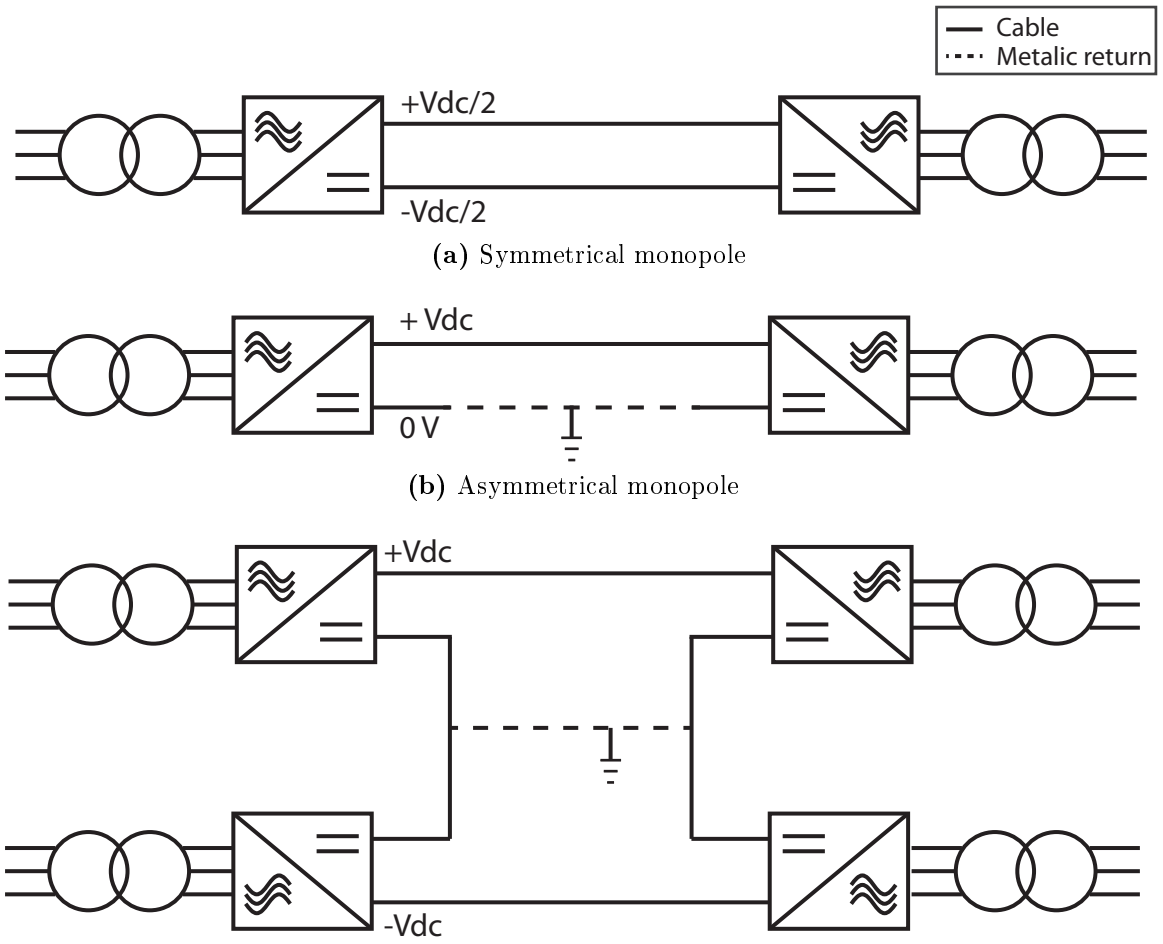
HVDC can also carry more power for a given conductor and insulator size than an equivalent HVAC conductor [21]. A single DC circuit requires a minimum of two conductors, compared to traditional AC transmission which requires three. This results in HVDC transmission requiring a smaller right of way when compared with HVAC [22].

Another advantage of HVDC is that can be used to connect asynchronous AC systems [21]. This can be done using back-to-back links, where two AC/DC converters are placed in the same station. Each AC/DC converter can adapt to the voltage and frequency of the AC system it is connected to [23]. This also means that the HVDC link can act as a firewall between the two connected AC systems, meaning that a disturbance on one AC grid is not seen on the other [24].

Given the great distance many of the Round 3 wind generation developments are from the UK shore, it is likely that many developments will be connected using HVDC transmission. Additionally any interconnectors with Europe may require HVDC as the asynchronous AC systems cannot be directly connected easily using HVAC, and many of the connections would be made using submarine cables.

HVDC link configurations can vary depending on the application. Some of the different configurations are shown in Figure 1.3. The symmetric monopole has no ground current and thus the converter transformers are not exposed to DC stresses. This arrangement requires two cables rated for half the DC voltage each [25]. The asymmetrical monopole requires one cable rated for the full DC voltage and can use a metallic return which requires less insulation, making it less expensive than the symmetric monopole scheme as only one fully rated cable is required. However the converter transformers must be designed to cope with DC stresses, as there is a DC voltage offset due to the asymmetric configuration of the converter. This configuration also enables expansion to a bipole system allowing an increase of power transfer capability at a later date. The monopole solutions are the least expensive option as they require only one converter per terminal [26]. The bipole system has two converters, at half the power rating, at each terminal and the system has the advantage of being able to operate at 50% power in the event of a fault on one of the cables or one of the converters. This arrangement also requires that the transformers

be able to handle DC voltage stress [25].




**(a)** Symmetrical monopole

**(b)** Asymmetrical monopole

**(c)** Bipole configuration

**Figure 1.3.:** HVDC link configurations

## 1.2. Multi-Terminal DC Grids

As more point-to-point HVDC links are completed, either between the UK and offshore generation or between the UK and other countries, it may become desirable to connect adjacent links to create a Multi-Terminal DC (MTDC) grid. A MTDC network is one that has three or more terminals. An offshore MTDC network in the North Sea could act as a precursor to a European Super Grid [27]. A pan-European grid could bring several advantages [28, 29]:

- Improved security of supply through international interconnection
- Balancing intermittent renewable energy sources over a wider area
- Decarbonisation of the electricity network through increased renewable energy penetration
- Increased energy trading within Europe
- Reduce congestion in existing AC transmission systems
- Reduced dependency on imports of fossil fuels

Despite these advantages there are a number of challenges to realising this grid. The main challenges are regulatory, economic, and technical. At present there are no grid codes in place for MTDC networks. A grid code would specify standards for voltage and power rating, and would detail regulation for interconnecting adjacent HVDC systems [28]. Such a grid code would complement the agreement made between the European countries which signed the North Sea Countries' Offshore Grid Initiative Memorandum of Understanding [30]. This memorandum outlines that the signatory countries are to cooperate to find common solutions to the development of an offshore grid in the North Sea [30]. The European Network of Transmission

System Operators for Electricity (ENTSO-E) has developed a draft network code for HVDC connections and DC connected generation, the document does not explicitly outline any regulation for MTDC networks [31]. The ENTSO-E draft does outline framework for HVDC links between different TSOs but it does not provide recommendations for standard DC voltages or maximum DC power ratings. Cigré working group B4.56 are currently working on guidelines for grid codes for MTDC grids, which includes guidelines for technical specifications such as DC voltage range and functional requirements for future extensions [32].

A significant amount of capital investment is necessary to create a pan European grid and it is likely to come from several investors and governments, rather than a single investor. The investment required for power transmission infrastructure is estimated to be in the range of €114-184 billion up to 2030 [33]. By coordinating and creating an offshore grid, rather than using solely point-to-point links, significant investment savings could be made [29].

### 1.2.1. Technical Challenges for MTDC

There are also technical barriers to a MTDC grid including difficulties in protection of DC networks and voltage conversion. A DC grid has low impedance through absence of impedance, which results in low losses, but in the event of a short circuit the low impedance of the network means that the fault current rises quickly and spreads rapidly through the network [34]. To break this fault current it must be forced to zero, as there is no natural zero crossing as in the AC system. Thus a DC circuit breaker must force the fault current to zero, dissipate the energy from the system, and do so quickly [34]. The speed at which a DC breaker opens is dependent on its topology. Electromechanical DC breakers, which use high speed mechanical switches, can operate at high voltages but take some time to open, in the region

of 100 ms [35]. Solid-state DC circuit breakers, using semiconductor devices, can achieve fast opening times, in the order of microseconds. The cost of such a DC circuit breaker is high, and it has higher operational losses than a electromechanical breaker. At present there are no DC circuit breakers commercially available but manufacturers are developing prototypes. The most promising design prototypes are hybrid breakers which use a combination of a high speed mechanical switch, to maintain low power losses, and fast power electronic switches to achieve fast opening times. The ABB hybrid DC circuit breaker is shown in Figure 1.4 [36].

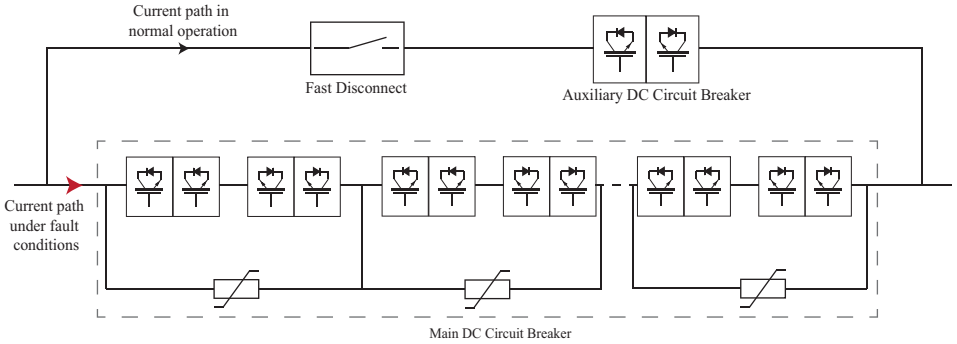


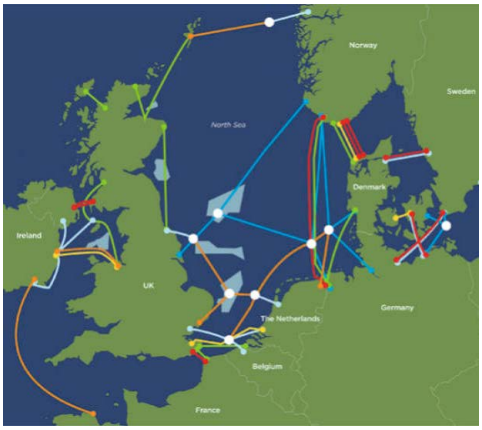

**Figure 1.4.:** ABB hybrid DC circuit breaker

The largest prototype to date is the State Grid Research Institute DC circuit breaker which operates at 200 kV and is capable of interrupting fault current of 15 kA within 3 ms [37].

As of yet there are no standardised DC voltage levels and as cable ratings increase it is likely that newly commissioned projects will use the latest technology, meaning adjacent HVDC projects may not operate at the same voltage level [38]. Connecting projects operating at different voltages requires a voltage conversion stage. This is achieved using a DC/DC converter which are described further in Chapter 3.

How a European Supergrid might look, both technically and geographically, is still unclear. There are many proposals about how this supergrid might look, and some are shown in Figure 1.5.

**(a)** Friends of the Supergrid [39]




**(b)** European Wind Energy Association


**(c)** DNV GL vision [40]

**Figure 1.5.:** European supergrid proposals

Many of the proposals have the same traits, they show significant interconnection between European countries, and that the UK offshore developments play a big

role in developing a MTDC network. An additional common feature is that several HVDC links connect at a single point, or node. This node could be a single platform or it could spread across a large geographical area. It is not yet known for certain how these nodes will be built.

There are two broad approaches that can be made to create this node, the use of either AC or DC technology. An AC node would make use of readily available and well known equipment, however the distance that AC submarine cables can travel is limited. An AC hub could be used within a wind farm development to allow a common connection point for several adjacent wind farms [41]. The clustering of nearby wind farms into AC hubs could also save a large amount of investment [42].

The alternative is to use DC technology to create this node. The Belgian transmission system operator, Elia, proposes an international HVDC platform in the North Sea that could enable energy trading between countries connected to that platform [43]. A benefit of using DC to create these offshore nodes that DC/DC converter could potentially be more compact than AC transformers, as medium frequency transformers can be used within the DC/DC converter, reducing platform size [44]. Additionally DC cables are more economical for cable applications and have lower losses than equivalent AC cables [45].

## 1.3. HVDC Converters

In order to convert from AC to DC, a power electronic converter is required at each terminal. There are two HVDC converter types, Current Source Converters (CSC) and Voltage Source Converters (VSC).

### 1.3.1. Current Source Converter

The first commercial CSC was the Gotland 1 project by ABB, built in Sweden in 1954 and was operated at 200 kV and 20 MW [46]. The converters in this project used mercury arc valves, however this technology suffers from several problems, including limited voltage ratings, a limit on the rate of change of load, and high maintenance costs [47]. Modern CSCs use thyristor valves, and the first thyristor based converter was the Eel River Scheme in Canada in 1972 [46]. Voltages of up to 1,100 kV are now available with power transfer capability of up to 10 GW [48]. Today the largest CSC project commissioned is the Jinping - Sunan project in China, which is rated for 7.2 GW at ± 800 kV [49]. A simplified circuit diagram of the thyristor valve based CSC is shown in Figure 1.6.

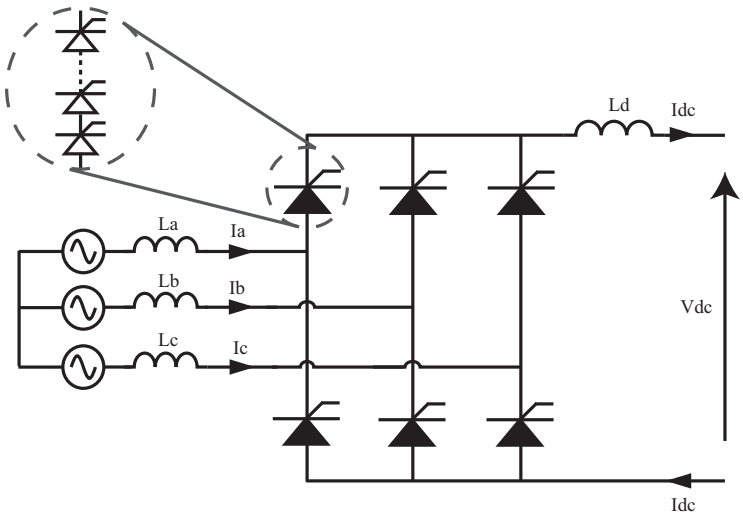



**Figure 1.6.:** Six pulse CSC with thyristors

The circuit is laid out as a three-bridge rectifier, and each thyristor in Figure 1.6 represents a valve of series connected devices. The firing angle of the thyristors determines whether the converter is inverting or rectifying [50]. The power flow control is achieved by varying the current and maintaining a constant voltage magnitude. In order to change the direction of the power flow the DC voltage polarity

is reversed and the current is unidirectional [46]. The number of series thyristor devices required is proportional to the value of the DC bus voltage. The advantage of using thyristors is that they are very robust and have high voltage and current ratings, which enable bulk power transfer. Typical phase control thyristors, which are used for HVDC applications, are available with ratings up to 8.5 kV and 3.6 kA [51]. The converter has low power losses in the region of 0.7 % [52]. The power losses of the converter are an important factor and are optimised to be low in order to reduce the cost of losses over the lifetime of the converter [50].

The CSC has a significant reactive power load, this is due to the converter operating with a delay due to the firing angle of the thyristor which results in the current lagging the voltage [50]. This requires reactive power compensation, which comes mainly from AC harmonic filters [26]. In order to ensure that operates correctly it is necessary to connect both terminals to strong AC networks [21]. The filtering requirement is a major factor in the footprint of the converter, and can be as much as 75 % of the total footprint of the converter station [26].

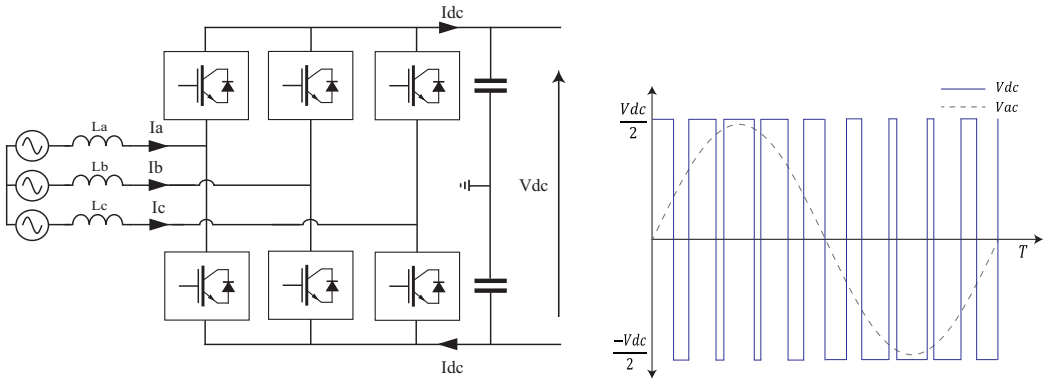
### CSC for MTDC Grids

The use of CSC in MTDC is limited as it is difficult to change the direction of power flow in a CSC based MTDC network. This is due to the power flow reversal being achieved by changing the voltage polarity. Thus special DC side switching arrangements must be put in place to allow the direction of power to change at one terminal while the same power direction is maintained on the other terminals [26]. Despite this difficulty the first MTDC schemes were developed using CSCs. The first MTDC scheme is the world was the SACOI project, which is still used to exchange energy with the Italian mainland with the islands of Sardinia and Corsica. The original scheme consisted of two terminals and was upgraded to three terminals in 1988 to add the connection to Corsica [53]. Another existing CSC MTDC scheme

is the Québec - New England project commissioned in the early 1990's, and it was used to connect remote hydro generation in Québec to load centres in Montreal and Boston [54].

### 1.3.2. Voltage Source Converter

The VSC is becoming increasingly popular for HVDC applications. The first HVDC VSCs were introduced in 1997 by ABB and the first converters were installed in Sweden in a demonstrator project [55]. The demonstrator was a 3 MW, ± 10 kV converter with 10 km of overhead DC lines. Today the largest VSC commissioned is the INELFE bipole link connecting the French and Spanish transmission systems, which enables the transfer of 2000 MW at ± 320 kV between the two systems [56]. The semiconductor device used for HVDC VSCs is the Insulated Gate Bipolar Transistor (IGBT). The IGBTs can be controlled to turn off as well as on which means the VSC can provide flexible and independent control of real and reactive power [26]. This ability allows the VSC to connect to small or weak AC systems, making it the preferred technology for connecting intermittent remote generation such as wind generation [25]. The IGBT is limited in current and voltage ratings and more devices are required in the circuit when compared with the thyristor based CSC devices. However ratings are starting to become comparable to thyristors with the latest generation of IGBTs rated for 4.5 kV and 2 kA [57]. The first generation of VSC, the two-level converter is shown in Figure 1.7a.




**(a)** Circuit diagram **(b)** Sample AC waveform

**Figure 1.7.:** Two-level VSC

The converter works by holding a constant DC voltage and the power flow is controlled by changing the value of the DC current. The power flow is reversed by changing the polarity of the current. A DC bus capacitor is required on the DC terminals of the converter to stabilise the DC voltage and to absorb the harmonic switching content [58]. In the two-level VSC the AC waveform is generated by switching between the positive and negative DC voltage. Pulse Width Modulation (PWM) is used to improve the shape of the AC waveform, as shown in Figure 1.7b. PWM uses high switching frequencies which increases the switching losses of the converter and filtering is needed to remove the switching content from the AC waveforms [59]. Filtering increases the losses and the volume of the converter, however the filtering requirement is lower than the CSC as VSCs do not require reactive power compensation [60]. The power loss figure for the first generation of two-level VSCs was approximately 3 % [25].

In order to reach the high voltages required for HVDC the two-level converter can have hundreds of IGBTs connected in series to block the DC voltage. It is a challenge to switch all of the series connected devices simultaneously. If one devices turns off prior to the other devices it will not be able to block the full DC bus voltage

and will fail [58]. The precautions to prevent this become increasingly burdensome and leads to a restriction in the DC voltage that can be achieved with this design and subsequently limits the power transfer capability of the converter.

The three-level converter switched between the positive and negative DC bus voltage and zero to produce the AC waveforms. As the number of levels increases, each level requires an additional two semiconductor switches per phase [61]. ABB's second generation of HVDC Light used three-level converters with power losses in the region of 2 %, which was still still more than twice the losses of the CSC [25]. The use of Selective Harmonic Elimination (SHE) PWM for two-levels VSCs improved their loss figure to 1.5 % ABB [25]. The lower loss figure is a result of the SHE PWM lowering the switching frequency and thus reducing the switching losses of the converter [62].

Increasing the number of DC voltage output levels available from the converter can reduce the Total Harmonic Distortion (THD) in the AC waveforms and thus reduce the filtering requirement for the converter, and reduce the switching frequency required [21]. A new topology of VSC was introduced in the early 2000s, the Modular Multilevel Converter (MMC) [63]. The MMC creates an staircase waveforms by using hundreds of DC voltage levels available from the converter. The topology is described in Chapter 2.

### VSC for MTDC Grids

When considering MTDC networks, the VSC is better suited than the CSC for several reasons. The primary one being the ease of reversing power flow by changing the current polarity. DC switching arrangements are not required as the voltage polarity does not change [19]. Another advantage of the VSC is that it allows the use of cross-linked polyethylene (XLPE) cables which cannot be used with CSC technology as the breakdown strength of the cable is affected negatively by the

reversal of voltage polarity [64]. These cables are also lighter, cheaper and more environmentally friendly than oil-filled cables [28, 64]. As XLPE is lighter this means that longer cables can be made and more power can be transported per kilogram of cable [65].

Newer modular VSCs have a smaller footprint than the CSC, as they do not have the same filtering requirement [50]. This is advantageous in offshore applications where space is a premium. Additionally the VSC enables the connection of weak or islanded AC systems, such as offshore wind farms, and can thus be placed anywhere within an AC system [26].

At time of writing there were two MTDC VSC grids operating in the world, both in China. The first was the Nanao project with three terminals, it operates at ± 160 kV and the three terminals are rated for 200MW, 100 MW, and 50 MW [66]. The second operating scheme is the Zhoushan project, which is a five terminal network [67]. This project operates at ± 200 kV and the first three terminals are rated for 400 MW, 300 MW, and three terminals at 100 MW [68].

## 1.4. Research Motivation

The use of HVDC transmission is becoming increasingly popular for submarine applications to connect remote renewable generation and for international interconnection. HVDC is likely to play a key role in future transmission systems it is essential that the converter dynamics are well understood. This can be achieved through accurate simulation models of the converters. The formation of MTDC grids will be in stages and how these connections will be made is not yet well understood. The focus of this work is to identify some of the converter technologies that enable DC-side connections, while bearing in mind some of the restrictions that come with placing equipment in the offshore environment.

One technology gaining significant interest in recent years is the DC/DC converter. The review in this work intends to indicate the best suited converters for low to medium voltage conversion to connect HVDC systems in the offshore environment. A simple comparison shows how the different DC/DC converter designs can vary. AC/DC converters are the main building blocks for any MTDC grid and the leading topologies are described. The value of DC fault tolerant converters is also highlighted. A methodology to produce reduced order simulation models of the complex AC/DC converters is given to enable time efficient and accurate system level studies with multiple converters. The method focuses on reducing the complexity by not representing each switching device in the converter and it has been presented in a manner that allows the models to be replicated.

Any MTDC grid will evolve over through interconnection of adjacent networks, one possible evolution scenario is considered. Several simulations studies are used to show how these systems operate at each stage. The value of the reduced dynamic converter models is shown as multiple converter simulations are computed in the space of minutes. These simulations are intended to be the basis for future system

power flow analysis and MTDC grid control design. At present DC circuit breakers are not yet commercially available, an alternative DC-side protection method is proposed where the MTDC grids are sectioned by normally open points and DC/DC converters.

## 1.5. Thesis Outline

This thesis presents research on HVDC converters that can be used in an offshore MTDC grid. This includes an assessment of several different types of HVDC converter topologies that are suitable for offshore networks and simulating case study models to validate their operation in a case study network.

The topic area and motivation are introduced in Chapter 1. The benefits that an offshore DC network, and a European supergrid, can provide are outlined. The challenges facing such a network are also highlighted. The building blocks for MTDC networks, AC/DC converters are also introduced and it established that VSC technology is best suited to MTDC.

Chapter 2 introduces the key AC/DC converters for use in MTDC networks. The MMC is described in detail and alternative fault tolerant modular VSCs are discussed. A promising fault tolerant topology, the Alternate Arm Converter (AAC) is then described in detail and compared to the MMC. The comparison investigates the differences between the converters including a device count and an estimate of the volume of a converter submodule.

In Chapter 3 an assessment of different DC/DC converters for use in an offshore MTDC grid is made. Several DC/DC converter topologies are reviewed and a resonant DC/DC converter is studied in detail. An alternative mode of operation for the resonant converter is proposed. The chapter finishes with a comparison of the DC/DC converters reviewed and gives a recommendation of the best suited converter for offshore applications.

In order to simulate DC networks effectively an Average Value Model (AVM) of the AC/DC converter is needed. Chapter 4 begins with a short review of work to date on AVMs, and the methodology used for this research is introduced. An AVM is developed for the HB MMC and the AAC. It seen from the results that the

AVM reduces computation time while maintaining accuracy of the main converter waveforms. The AVM of the AAC is then verified using experimental hardware.

In Chapter 5 several MTDC systems are studied using the AVMs developed in Chapter 4. A four terminal network that consists of VSC with and without DC fault blocking capacbilities is modelled. A simple cost benefit case is presented for connecting two point-to-point links using DC. The link between the point-to-point schemes is operated as a normally open point allowing the grid to be reconfigured in the event of DC fault. This four terminal network is then expanded to include a connection to a bipole HVDC link between the UK and Norway. A DC/DC converter is used to interconnect the two systems. The system is simulated for normal operating conditions and for three DC fault scenarios.

Chapter 6 concludes the work from the research and highlights contributions from the author. A summary of potential future work arising from this research is also provided.

# 2. AC/DC Converters

## 2.1. Introduction

VSC topologies have been described in Section 1.3.2, and their suitability for MTDC grids is due to their characteristic of having a constant voltage whilst varying power flow by varying the current magnitude and direction. This chapter looks at the latest generation of VSC, which are modular multilevel converters that use hundreds of voltage steps to create the AC voltage waveform [69]. The Modular Multilevel Converter (MMC) is the preferred VSC topology for HVDC applications [70]. An advantage of this modular design is that it allows the converter to be easily scaled to higher voltages, allowing increased power transfer capability. A further advantage is that good quality AC waveforms, requiring little or no passive filtering, can be created while keeping switching power losses low.

## 2.2. Modular Multilevel Converter

The MMC design was introduced in the early 2000's by Lescinar et al [63]. The first commercial MMC was installed for the Transbay project in 2010, which consists of a pair of 400 MW converters operating at ± 200 kV [71]. The largest MMC to date is the DolWin 2 German offshore wind connection, which is a 916 MW, ± 320 kV converter in the North Sea [72]. The circuit diagram of an MMC is shown

in Figure 2.1. The converter consists of three phase legs, with two arms in each leg.

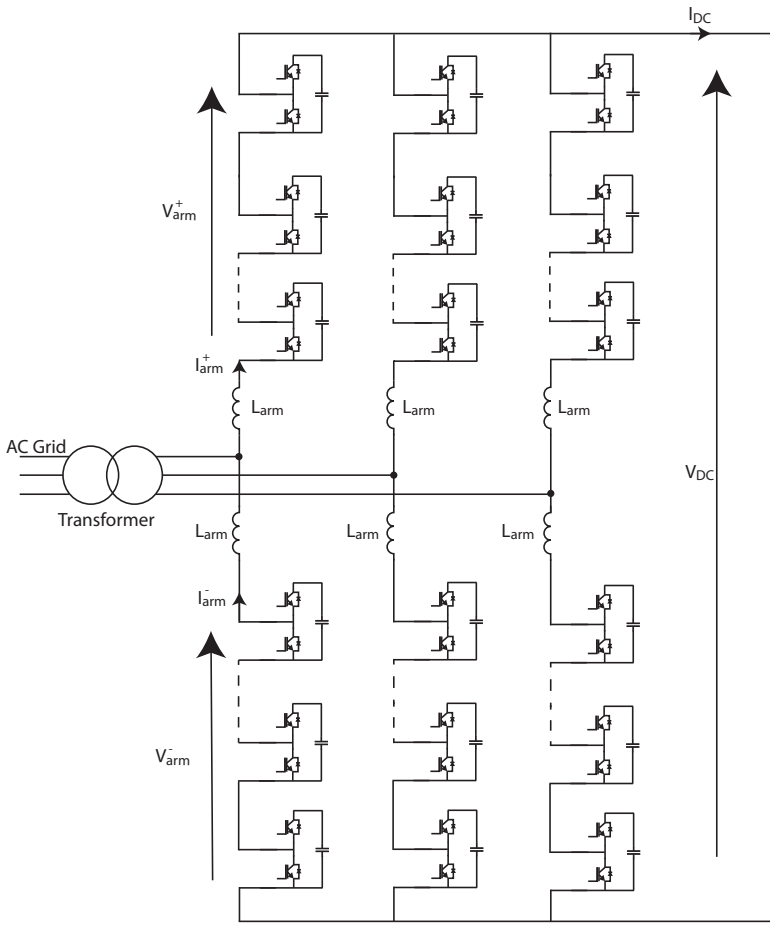
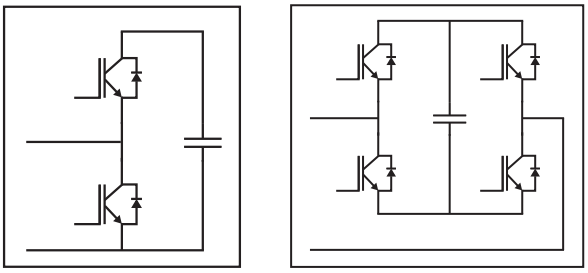



**Figure 2.1.:** Half-bridge MMC

Each arm is made up of a stack of submodules (SM) and an arm inductor. Each SM contains a capacitor and, typically, two IGBTs. The SM can be configured as a Half-Bridge (HB) circuit of two IGBTs or a Full-Bridge (FB) circuit of four IGBTs, both circuits are shown in Figure 2.2. The HB circuit is the most commonly used as it has fewer devices in conduction and thus has lower power losses [60]. The circuit can insert the capacitor voltage of the SM into the arm or bypass it. However, when the DC voltage is lower than the AC voltage, such as a DC fault event, the

HB MMC acts as an uncontrolled diode rectifier due to the anti-parallel diodes in the IGBT modules [60]. The FB SM can insert positive capacitor voltage, negative capacitor voltage, or bypass the SM. The advantage of the FB circuit is that it allows the converter to block DC side faults by enabling the converter to oppose the AC voltage using the negative capacitor voltage [73]. This capability comes at the cost of increased power losses as there are twice the number of IGBTs in conduction [74].



**(a)** Half-bridge SM **(b)** Full-bridge SM

**Figure 2.2.:** MMC SM circuits

The SMs are responsible for the shaping of the AC voltage waveform and they create a staircase waveform. The number of levels in the waveform is the number of SMs in a phase leg plus one, for zero volts. In a typical MMC there would be hundreds of SMs in the arm. The arm voltages for the upper and lower arms are given in (2.1) and (2.2) respectively.

$$V^{+}_{arm}(t) = -V_{AC}sin(\omega t) + \frac{V_{DC}}{2} \tag{2.1}$$

$$V^{-}_{arm}(t) = V_{AC}sin(\omega t) + \frac{V_{DC}}{2} \tag{2.2}$$

The current in the upper and lower arms of the converter can be defined as in (2.3) and (2.4), where $\theta_{AC}$ is the angle difference between the voltage and the current and $I_{Circ}$ is the circulating current to used to balance the energy in the converter. Energy balancing is described in the following subsection.

$$I^{+}_{arm}(t) = \frac{\hat{I}_{AC}}{2} sin\left(\omega t + \theta_{AC}\right) + \frac{I_{DC}}{3} + I_{Circ} \tag{2.3}$$

$$I^{-}_{arm}(t) = -\frac{\hat{I}_{AC}}{2} sin\left(\omega t + \theta_{AC}\right) + \frac{I_{DC}}{3} + I_{Circ} \tag{2.4}$$

The DC current is split equally between the three parallel phase legs, and each AC phase current is split between the upper and lower arms of that phase. The three AC phase currents at the positive and negative DC bus sum to zero [61]. Figure 2.3 shows example waveforms of the arm voltage and current of 20 MW, ± 10 kV MMC simulation model, with 14 levels, and the converter is acting as an rectifier.

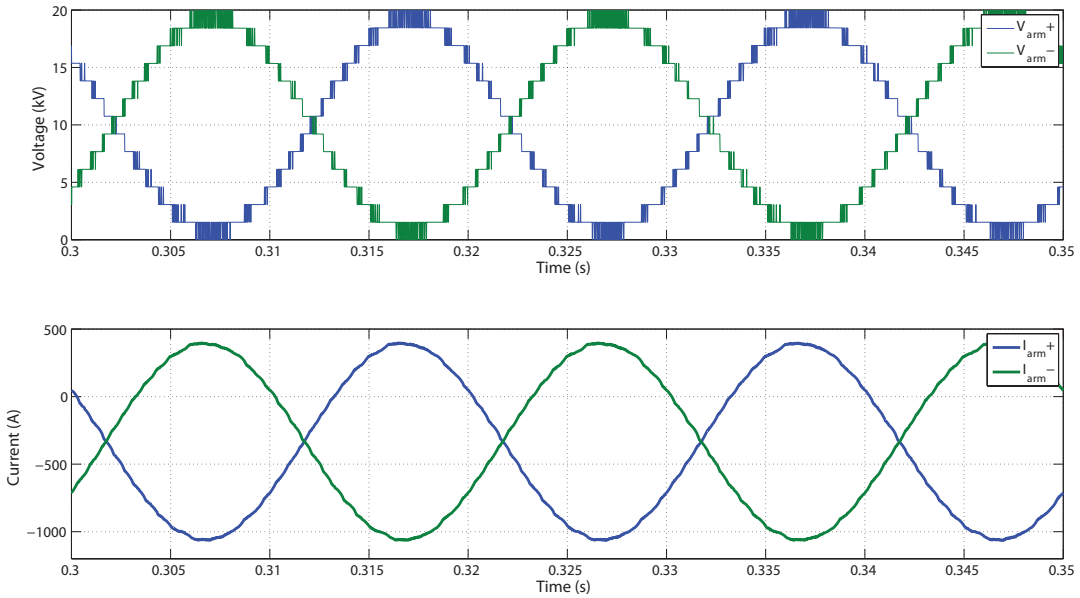



**Figure 2.3.:** Example MMC arm voltage and current waveforms

The voltage waveforms clearly shows the steps created by the SMs of the converter, and the DC voltage offset of 10 kV ($V_{DC}/2$) can be seen. The current waveform shows the converter is acting as a generator delivering current into the DC system. The arm current also clearly shows the DC current offset.

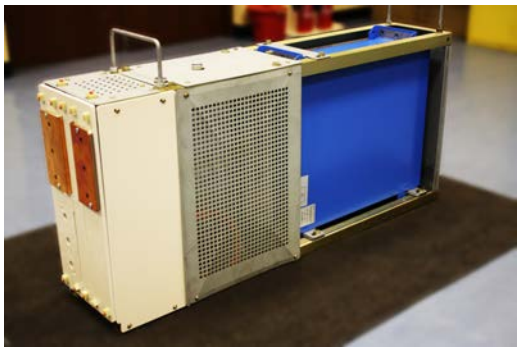
The arm inductor is present primarily as the component in which the arm and phase currents are controlled through imposing a voltage. It can also used to limit the rate of rise of fault current during a DC side fault [75]. The value of the arm inductor can be found by setting a desired rate of change of current, $di/dt$ in kA/ms, for a DC fault event and using (2.5) from [75].

$$L_{arm_{MMC}} = \frac{V_{DC}}{2\frac{di}{dt}} \tag{2.5}$$

The staircase waveform produced by the MMC results in the AC current requiring little or no filtering [60]. The reduced filtering requirement on the AC side reduces the power losses of the converter, and reduces the footprint of the MMC [76]. Also as the AC currents sum to zero at the DC bus, no filtering is required on the DC side. The switching losses for the MMC are much lower than for two-level VSCs as the IGBTs in the SM are no longer switching at several kilohertz. To further reduce the necessity of AC filtering phase shifted PWM can be used when switching the SMs, which can be seen in Figure 2.3, and this reduces the harmonic distortion in the AC voltage [77]. This PWM method is useful when there is a low number of levels in the stack and the average of the AC waveform is achieved by using PWM on each step of the staircase waveform. The power losses for a full scale MMC are typically less than 1%, which is comparable to the power loss figure of the CSC of approximately 0.7% [25, 52].

The leading manufactures all use the MMC topology, Alstoms VSCs are known as HVDC MaxSine and Siemens offering is called HVDC Plus. ABB's HVDC Light®

has in recent years used a variation of the MMC called the Cascaded Two-Level Converter (CTLC). The CTLC design uses large HB SMs, called cells, where an individual IGBT module in the SM is replaced with a string of series connected IGBT modules and the capacitor is replaced with a string of series connected capacitors. Figure 2.4 shows the SM used by Alstom, and the cell used in the CTLC.



**(a)** Alstom SM [78]

**(b)** ABB CTLC cell [25]

**Figure 2.4.:** Pictures of SM designs from Alstom and ABB from

This design of the CTLC is enabled by the use of press-pack IGBT modules, which are best suited for series connections. The use of press pack modules allows for compact design of the converter. In the event of IGBT failure, the press pack device fails short-circuit and this allows the rest of the IGBTs in the cell to continue operating [79]. Thus redundancy in the cell is achieved by adding additional series IGBTs per cell. Press pack IGBTs have ratings up to 4.5 kV and 2 kA, and these ratings allow converters of over 1 GW to be built.

### 2.2.1. Energy Balancing in the MMC

Each arm of the MMC is dealing with a single phase imbalance between AC and DC energy and this requires energy storage devices to store the energy during the conversion from AC to DC. Balancing the energy in the MMC is important to ensure

the capacitor voltages of the SMs do not fluctuate significantly from their nominal value. Should the capacitor voltage greatly exceed its nominal value, it risks the failure of the capacitor itself or the IGBTs [80]. Undercharging the capacitors results in reduced voltage availability from the stacks, which can result in the loss of current control in the arms and hence cause instability of the converter [81]. The energy flows of the converter are depicted in Figure 2.5.

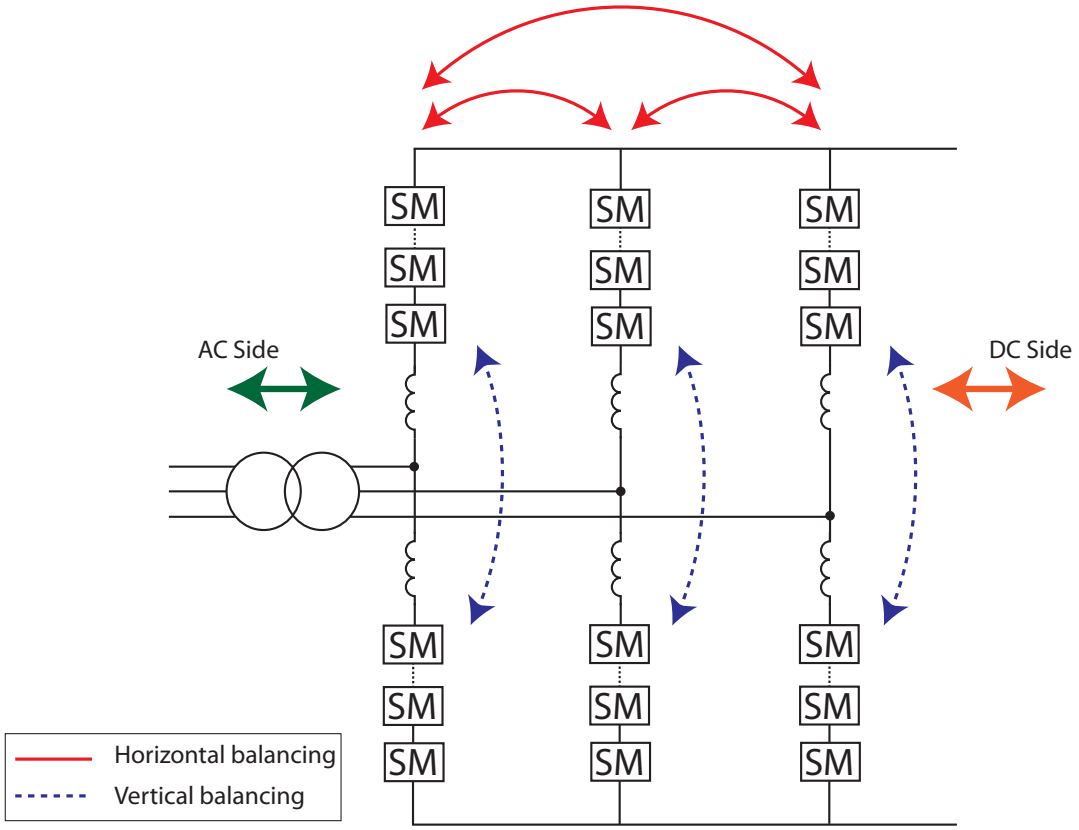



**Figure 2.5.:** MMC energy balancing

The instantaneous energy transfer from the AC-side caused by the phase currents is stored in the stack of SMs and then is transferred to the DC side through the DC current, or vice versa. Over a cycle the charge of the capacitors will fluctuate [69]. Thus the capacitors need to be sized such that there is enough energy stored in the SM so that the capacitor voltage does not deviate far from its nominal value. Capacitor voltage deviation of 10% is assumed to be a reasonable deviation [81]. The

minimum size that the SM capacitor can be to withstand this voltage fluctuation is given in (2.6) from [81].

$$C_{SM_{MMC}} \leq \frac{1.22\left|\bar{S}\right|}{3\omega V_{DC} V_{SM} \Delta V_{SM}} \tag{2.6}$$

The MMC needs an energy storage requirement, to maintain ± 10% voltage deviation of the SM voltage, of 39 kJ/MVA at a frequency of 50 Hz under sinusoidal modulation [81]. This energy storage value can be found by equating $^{1.22}/_{\omega \Delta V_{SM}}$, as the remainder of the equation is brought to the right hand-side and represents the energy over the apparent power (J/VA).

Additional circulating current are used to balance the energy in the converter as the SM voltages can deviate due to transients, such as power reference variations and fault events, in addition to varying cyclically with the AC current passing through them. These currents are determined from knowing the energy deviation of the converter. The energy deviation is the difference between the nominal energy and the actual energy, and is defined in (2.7).

$$\Delta E^{j}_{stack_M} = E^{j}_{stack_{M_{NOM}}} - E^{j}_{stack_{M_{MEAS}}} \tag{2.7}$$

$$E^{j}_{stack_{M_{NOM}}} = \frac{N_{SM}}{2} C_{SM} V^2_{SM_{NOM}} \tag{2.8}$$

$$E^{j}_{stack_{M_{MEAS}}} = \frac{1}{2} C_{SM} \sum_{i=1}^{N_{SM}} V^2_{SM_i} \tag{2.9}$$

$$M = \{A, B, C\}\ j = \{+, -\} \tag{2.10}$$

The energy deviation for the entire converter is the sum of the deviation for each

stack of SMs, defined explicitly below.

$$\Delta E_{MMC} = \sum \Delta E^{j}_{stack_M} \tag{2.11a}$$

$$= \Delta E^{+}_{stack_A} + \Delta E^{-}_{stack_A} + \Delta E^{+}_{stack_B} + \Delta E^{-}_{stack_B} + \Delta E^{+}_{stack_C} + \Delta E^{-}_{stack_C} \tag{2.11b}$$

When the converter is balanced the energy deviation of the converter is zero. If $\Delta E_{MMC}$ is greater than zero, then there is an energy deficit in the converter as the nominal energy is greater than the actual energy. This requires an energy injection into the converter. If $\Delta E_{MMC}$ is less than zero, then there is a surplus of energy in the converter as the actual energy is greater than the nominal. This requires a transfer of energy out of the converter. The net energy exchange with the stacks should be zero [61]. The energy to balance the converter can be taken from either AC or DC side depending on the characteristics of the controller.

In addition to balancing the total energy deviation in the converter, the deviation between the parallel phase legs and between the upper and lower arms of each phase leg must also balanced. The former is referred to as horizontal balancing, and the latter as vertical balancing. The individual SMs also need to be balanced to ensure that the energy is distributed evenly throughout all the SMs in the stack. This can be achieved by rotating which SMs are switched into the conduction path so that all SMs are used and that one SM is not over used, one rotation algorithm is described further in [82].

### Horizontal Balancing

Horizontal energy balancing aims to minimise the energy deviation between the phase legs of the converter. The error term is calculated by comparing the energy

deviation in a single phase leg to one third of the energy deviation of the entire converter and Equation (2.12a) shows the calculation for phase A.

$$\Delta E_{H_A} = \Delta E_A - \frac{\Delta E_{MMC}}{3} \tag{2.12a}$$

$$= \Delta E_A - \left(\frac{\Delta E_A + \Delta E_B + \Delta E_C}{3}\right) \tag{2.12b}$$

$$= \frac{2\Delta E_A}{3} - \frac{\Delta E_B}{3} - \frac{\Delta E_C}{3} \tag{2.12c}$$

Where

$$\Delta E_A = \Delta E^{+}_{stack_A} + \Delta E^{-}_{stack_A} \tag{2.13}$$

Similar equations can be derived for phase B and C. The sum of the three horizontal balancing energies should be equal to zero, so that the overall energy balance of the converter is not disturbed. To balance this horizontal energy a DC current is circulated through the converter. The current required for each phase leg should also sum to zero such that no DC current leaks out to the AC side of the converter. The horizontal balancing current can be defined as in (2.14), where $K_H$ is the proportional gain. The sum of the horizontal balancing currents should also be zero.

$$I_{H_A} = K_H \Delta E_{H_A} \tag{2.14}$$

$$I_{H_A} + I_{H_B} + I_{H_C} = 0 \tag{2.15}$$

### Vertical Balancing

Vertical balancing is used to ensure that the energy stored in the upper and lower arms of a phase leg are equal. For any phase, the vertical energy deviation can be defined as in (2.16).

$$\Delta E_V = \Delta E^+_{stack_M} - \Delta E^-_{stack_M} \tag{2.16}$$

If $\Delta E_V$ is greater than zero then the upper arm is more discharged than the lower arm, and energy must be transferred from the lower arm to the upper arm. The opposite is true when $\Delta E_V$ is less than zero. The vertical balancing current, for any phase, can be defined as in (2.17), where $K_V$ is the vertical balancing gain.

$$I_{V_M} = K_V \Delta E_V \tag{2.17}$$

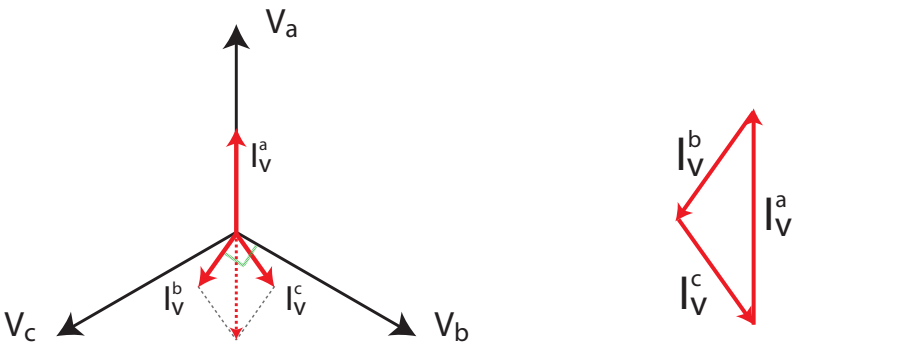
The vertical balancing current is a sinusoidal current, which transfers active power between the upper and lower arm [83]. This can result in AC components being transferred to the DC side of the converter. To remedy this, quadrature (reactive) currents are used in the other two phases, say B and C, to balance the transfer of energy between the arms of phase A. These quadrature currents are at 90 degrees to their phase voltage, as shown in Figure 2.6a.

For phase A, this would result in $I_V$ being defined as in (2.18).

$$\mathbf{I_V} = I_{V_A} + \bar{a} I_{V_B} + \bar{a}^2 I_{V_C} \tag{2.18}$$

$$\bar{a} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} = 1\angle 120^\circ \tag{2.19}$$

This results in the sum of the components of the vertical balancing current being




**(a)** Vertical quadrature currents **(b)** Sum of vertical currents

**Figure 2.6.:** Vertical balancing currents

equal to zero, as shown in Figure 2.6b. The final injected circulating current, $I_{Circ}$, is the sum of the horizontal and vertical balancing currents, shown in (2.20).

$$I_{Circ} = I_H + I_V \tag{2.20}$$

### 2.2.2. DC Fault Blocking Solutions

The HB MMC is the most power efficient design of MMC, but it cannot protect against DC side faults which is problematic in larger MTDC grids. The FB MMC design solves the DC fault issue but is often not considered due to the increased power losses [60]. An alternative is to use DC circuit breakers with the HB MMC. At the time of writing there were no DC circuit breakers commercially operational. Several proposals have been made that alter the MMC structure to enable the converter to block DC side faults. Two examples are described in the following sections.

#### Double Clamp Submodule

A new type of SM was proposed called the Double Clamp Submodule (DCS) [76]. The circuit diagram is shown in Figure 2.7.

During normal operation, the central IGBT, $S_3$, is always switched on which causes

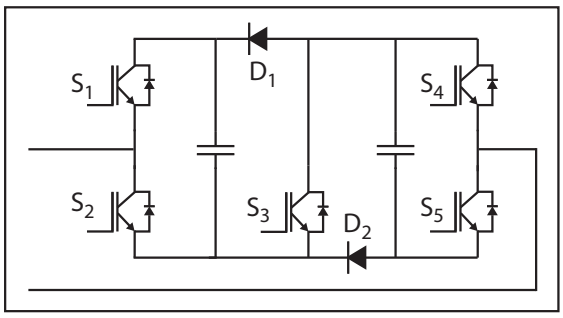



**Figure 2.7.:** Double clamp submodule

the two diodes to be reverse biased [69]. The DCS can output one or both capacitor voltages, or it can be bypassed. The voltages that are available from the DCS are obtained through the combination of switches below listed below.

**Double voltage:** $S_1$,$S_3$, and $S_5$ are on

**Single voltage:** $S_1$,$S_3$, and $S_4$, or $S_2$,$S_3$, and $S_5$ are on

**Bypass:** $S_2$,$S_3$, and $S_4$ are on

From this it can be seen that three devices are in conduction during normal operation. Comparing the DCS to two conventional SMs, because of its double voltage capability, its power losses are higher than two HB SMs, but lower than two FB SMs [84]. The DCS was compared to the HB SM, and the DCS was seen to be have a power loss figure of approximately 0.85% whereas the HB MMC was close to 0.5% losses [76]. In the event of a DC fault, the centre IGBT is switched off and the two diodes become forward biased. The circuit then acts in a similar fashion to a FB SM and the two capacitor voltages are connected in parallel and the average of the two voltages is inserted in a negative sense. This provides sufficient voltage to block or control the DC-side fault current. The DCS is likely to have a larger volume when compared to two HB SMs due to the higher number of devices in the circuit. It should have a lower volume compared to two FB SMs. This could make the DCS unsuitable for offshore HVDC applications.

### Hybrid MMC

Another proposed solution is to use a mix of HB and FB SMs in the arm of the converter [74]. This keeps the number of semiconductors in the converter low and reduces the power losses of the hybrid MMC compared to the FB MMC, while providing DC fault blocking capability. The ratio of HB to FB SMs can be varied to achieve the desired power capability and power losses of the converter. Splitting the stack into half HB SMs and half FB SMs results in a converter which has lower power losses than the FB MMC, but higher than that of the HB MMC topology. This arrangement has the lowest power losses while providing DC fault blocking capability [85]. The power capability of the hybrid MMC can be increased by adding FB SMs to the arm. By adding 50% more FB SMs to the stack the power capacity of the converter is doubled. The advantage of adding FB SMs is that they allow the AC voltage magnitude to be increased which in turn lowers the current magnitude and allowing increased power transfer [85]. Doing this results in the split of SMs in the arm being one third HB SMs and two thirds FB SMs. However this arrangement suffers from higher power losses than the 50/50 split configuration due to the higher number of SMs in the conduction path. A comparison of four different MMC topologies was carried out in [85], and some of the key results are given in Table 2.1.

| **Parameter** | **HB MMC** | **FB MMC** | **Hybrid MMC** | |
|---|---|---|---|---|
| | | | $N_{HB} = \frac{1}{2}N_{SM}$ $N_{FB} = \frac{1}{2}N_{SM}$ | $N_{HB} = \frac{1}{2}N_{SM}$ $N_{FB} = N_{SM}$ |
| No. SMs per arm | $N_{SM}$ | $N_{SM}$ | $N_{SM}$ | $1.5N_{SM}$ |
| $V_{AC_{MAX}}$(V) | $0.5V_{DC}$ | $0.5V_{DC}$ | $0.5V_{DC}$ | $V_{DC}$ |
| $V_{AC}$ under fault (V) | 0 | $0.5V_{DC}$ | $0.5V_{DC}$ | $V_{DC}$ |
| DC fault blocking | No | Yes | Yes | Yes |
| Power capacity | 1 pu | 1 pu | 1 pu | 2 pu |
| Device power losses | 0.6% | 1.1% | 0.8% | 1.0% |

**Table 2.1.:** MMC topology comparison [85]

This table shows the maximum reverse voltage that can be provided from the stack

of each MMC topology. The semiconductor power losses were calculated based on a 5 kV, 5 MW converter (10 MW for the second hybrid MMC arrangement as the power capacity is doubled) in [85]. The switching losses for the HB MMC, the FB MMC, and the 50/50 split hybrid MMC were shown to be the same where as the conduction losses were approximately twice that of the HB MMC for the FB MMC, and only 50% for the 50/50 split hybrid MMC. The second hybrid arrangement had a lower percentage conduction loss than the FB MMC. This hybrid MMC design could be used in applications where DC fault blocking is required, at the expense of additional power losses. The more power dense hybrid MMC, where adding 50% more SMs results in a doubling of the capacity of the converter, could be used where space is a premium, such as offshore applications, and DC fault blocking is required. However, the high power losses using more SMs could make it undesirable for other applications.

## 2.3. Alternate Arm Converter

A new family of hybrid modular multilevel VSCs was proposed by Alstom in [86], and one promising topology is the Alternate Arm Converter (AAC). Similar in structure to the MMS, each of the six arms of the converter consists of a stack of SMs, an arm inductor, and a director switch. The circuit diagram is shown in Figure 2.8.

The director switch is made up of a series connection of IGBTs and are used to alternate the current path between the upper and lower arms of the converter. The director switches disconnect the arm which is no longer in conduction, this means that the SMs do not have to block the AC peak to peak voltage as in the MMC [60]. This results in fewer SMs required in the stack compared to the MMC.

Similar to the MMC, the stack of SMs are responsible for producing the AC voltage waveform. The AAC is best operated with the AC voltage being higher than the DC

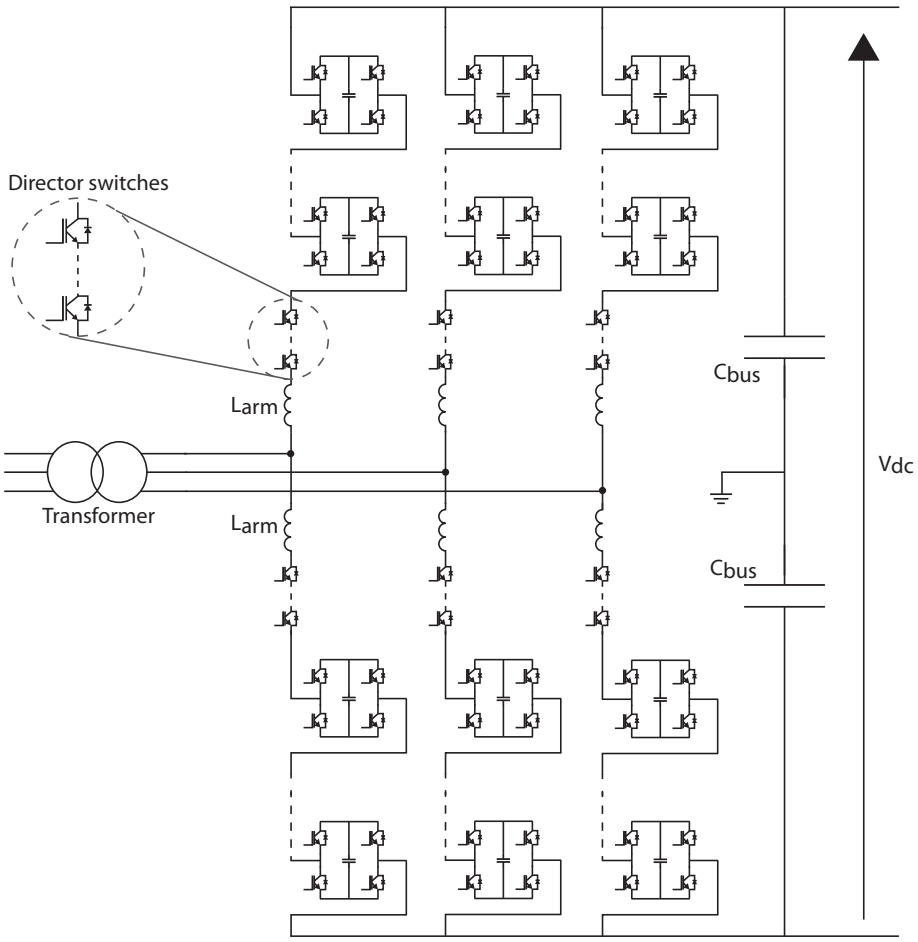



**Figure 2.8.:** AAC circuit diagram

voltage and this results in FB SMs being used in the stack, as FB SMs can provide a negative voltage [60]. The higher AC voltage magnitude reduces the magnitude of the arm current, lowering the conduction losses of the converter. The use of FB SMs also allows the converter to block DC-side faults. The anti-parallel diode of the IGBTs in the director switches do not contribute to a DC fault as the FB SMs control the currents in the converter during the fault. This DC fault blocking ability results in the size of the arm inductor being much smaller as it is no longer required to limit the rate of rise of fault current. The arm inductor of the AAC defines the arm currents and the phase inductance, which is often the leakage impedance of the transformer, facilitates control of the phase currents. Despite the use of FB SMs the

power losses of the converter are reduced compared to the FB MMC, as only one arm is in conduction for the majority of the switching cycle. There is a short time where both arms are in conduction allowing the current to commutate from the arm in conduction to the other arm, and this is known as the overlap period [87]. This overlap period is used to circulate energy balancing currents around the AAC, this is described in greater detail in the following subsection.

The AAC directly rectifies the AC current to a DC current and this results in a a six-pulse ripple on the DC current. A sizable DC bus capacitor is used to reduce the ripple seen in the DC network. The energy required in this DC bus capacitor is 4.4 kJ/MVA for a desired DC bus voltage fluctuation of ± 5% [81].

### 2.3.1. Energy Balancing in the AAC

Like the MMC, it is important to balance the energy stored in the SM capacitors of the AAC such that they do not fluctuate far away from their nominal value. However, the energy flows in the AAC are not as straight forward as for the MMC as there is generally only one arm of each phase leg in conduction at a time. In order to maintain energy balance within the converter it is necessary for the converter to operate in a fashion where the AC and DC energies are equal [81]. The AAC can be operated at a voltage ratio, known as the sweet-spot, where the energy between the AC and DC side naturally balance and the energy level in the stacks return to their initial value at the end of each cycle, defined as in (2.21) [69].

$$\hat{V}_{AC} = \frac{2}{\pi} V_{DC} \tag{2.21}$$

In practice the energy will vary in the converter away from the sweet-spot and the SM capacitor needs to be able to store enough energy to ensure the voltage fluctuation stays within a specified range. The minimum size of the SM capacitor

for the AAC is defined in (2.22). For a SM voltage fluctuation of ± 10%, the energy storage requirement for the AAC is 21 kJ/MVA [81].

$$C_{SM_{AAC}} \leq \frac{0.57\,|S|}{3\omega V_{DC} V_{SM} \Delta V_{SM}} \tag{2.22}$$

To ensure operation of AAC near the sweet-spot additional energy balancing currents are circulated during the overlap period to maintain a stable energy level within the stack [69]. Operating away from the sweet-spot incurs higher power losses in the converter as the magnitude of the balancing currents increase in order ensure the energy in the converter remains stable [69]. The average DC current of the can be varied by circulating a constant DC current during each overlap period, in addition to the horizontal balancing current. The horizontal and vertical balancing methods are similar to those used in the MMC and are discussed in the following sections.

### Horizontal Balancing

The horizontal balancing current for the AAC can be calculated in a similar fashion to that of the MMC. The only difference for the AAC is that the horizontal balancing gain is multiplied by a factor to account for the shorter time period over which it is applied. This is shown in (2.23), where $\phi_{overlap}$ is the overlap period in degrees.

$$I_H = K'_H \Delta E_H = \frac{K_H}{\frac{2\phi_{overlap}}{360^o}} \Delta E_H \tag{2.23}$$

The overlap cycle is multiplied by two, as it occurs twice every cycle.

### Vertical Balancing

To achieve vertical balancing, a square wave current is used to exchange energy between the upper and lower arms of the stack during the overlap period. As the arms of the AAC are not always in conduction, circulating AC currents cannot be

used to transfer energy between the arms. To achieve the correct energy transfer effect during the overlap period the current must change sign to follow the sign of the AC voltage. The sign of the vertical balancing current during the overlap is defined in (2.24).

$$I_V(t) = \begin{cases} +I_V & if\ \omega t\ \epsilon\ [-\phi_{overlap},\ \pi - \phi_{overlap}] \\ -I_V & if\ \omega t\ \epsilon\ [\pi - \phi_{overlap},\ 2\pi - \phi_{overlap}] \end{cases} \tag{2.24}$$

The magnitude of the balancing current is dictated by the length of the overlap period, the shorter the overlap the greater the magnitude of the balancing current. The final overlap current is the sum of the Figure 2.9 shows how the overlap current is formed.

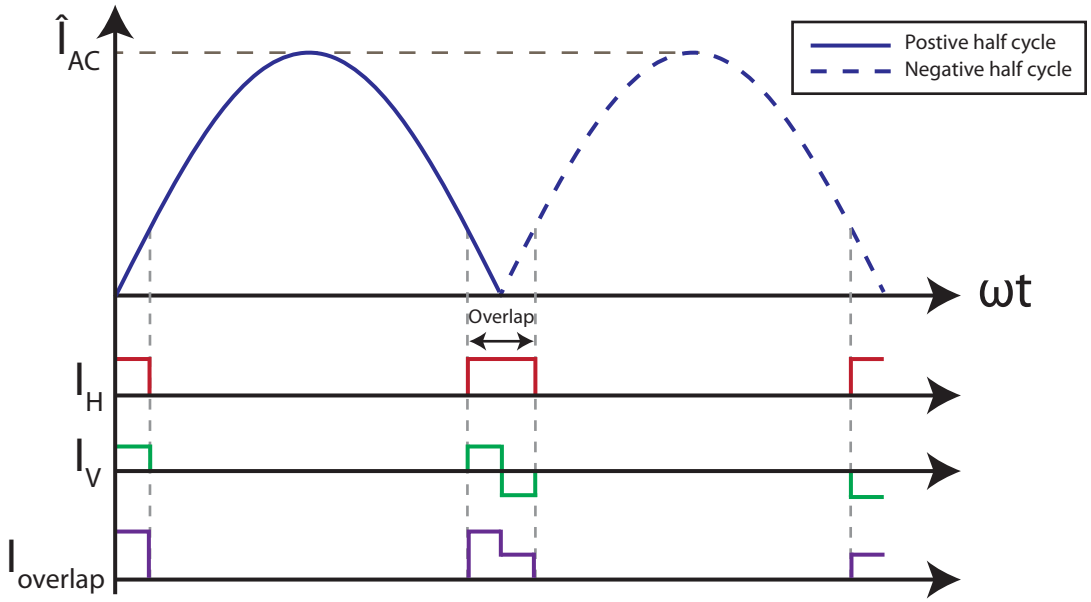



**Figure 2.9.:** Balancing currents in the AAC

## 2.3.2. Extended Overlap AAC

A new mode of operation was developed for the AAC which remedies some of the converters shortcomings. By operating the converter with an extended overlap pe-

riod of $60^{o}$ a DC current can be circulated continuously within the converter. This allows the six-pulse ripple in the DC current to be smoothed by control action, rather then with passive filters. Another advantage is the that the converter no longer needs to be operated at the sweet-spot, which decouples the AC and DC powers [88]. This mode of operation does require additional SMs in the stack in order to block the voltage, but this does not increase the power losses as the filtering requirement is removed and small inductors are required on the DC bus. It has these features in addition to the previously existing characteristics of the converter, such as DC fault blocking and STATCOM operation. This mode of operation was developed at Imperial College in collaboration with Alstom Grid and it is described in further detail in [88, 89].

## 2.4. Comparison of the MMC and AAC

At time of writing, the preferred VSC design was the MMC. However, this design acts as an uncontrolled diode rectifier in the event of DC side faults. It may become desirable in the future to use fault blocking converters in MTDC grids to limit the fault current in the event of a DC side fault. By using fault tolerant converters the duty on a DC circuit breaker could be reduced, potentially resulting in the use of smaller, or slower, DC circuit breakers or remove the need for additional DC protection. This section gives a brief comparison of the MMC and AAC. The converter characteristics are compared in Table 2.2. An estimate of the number of IGBTs in the converters and an SM volume is provided in the following sections.

This table shows that the AAC can achieve a similar power loss figure to the HB MMC and at the same time provide DC fault blocking capability. The AAC can also provide STATCOM services to the connected AC system during a DC fault, as it maintains control of the currents in the arms of the converter [60]. The reduced

| Characteristic | HB MMC | AAC |
|---|---|---|
| Semiconductor power losses (approx.)[90, 87] | 0.9% | 1.02% |
| DC fault blocking capability | No | Yes |
| Energy stored in the converter [81] | 39 kJ/MVA | 21 kJ/MVA |
| DC bus capacitor[81] | Negligible | 4.4kJ/MVA |

**Table 2.2.:** Comparison of the MMC and AAC

amount of energy storage required in the AAC implies that the SM capacitors would be more compact and this could result in a more compact stack of SMs. In addition to the smaller capacitor size, the use of the director switches reduces the number of SMs required in the stack of the AAC and this is illustrated further in the following section. The original AAC design required a DC bus capacitor to reduce the ripple on the DC current and this increases the amount of energy storage required by the AAC and increases the overall converter volume. The requirement for this DC bus capacitor is no longer necessary when the overlap period of the converter is extended.

### 2.4.1. Analytical Comparison

An analytical comparison of the converter was carried out for Arup and it was used in the electrical systems study for the Carbon Trust's Offshore Wind Accelerator. A symmetric monopole HVDC arrangement was used to compare the MMC and the AAC and one terminal of the converter is considered as the same calculations apply for both the onshore and offshore terminals. The comparison looks at the IGBT count for both converters, and an estimate of the volume of the SM. Reliability is built into the converter by adding redundant SMs to the stack, and this study assumes that adding 10% more SMs to improve the reliability of the converter is feasible. Table 2.3 shows the key parameters for the study.

| Parameter | Value |
|---|---|
| DC voltage | ±320 kV |
| Power | 1000 MW |
| MMC AC line voltage | 352 kV |
| AAC AC line voltage | 500 kV |
| SM voltage | 2 kV |
| SM redunancy | 10% |

**Table 2.3.:** Scenario parameters

### IGBT Count

The number of IGBTs required by the MMC is calculated using (2.25), where $n_R$ is the redundancy for the arm [69].

$$N_{SM_{MMC}} = \frac{V_{DC}}{V_{SM}}(1 + n_R) \tag{2.25}$$

For the AAC the voltage that the stack needs to withstand is less than the MMC thanks to the use of director switches. It is assumed that DC fault blocking is a desired function of the converter, and the number of required SMs and the number of series IGBTs in the director switch is found using (2.26) and (2.27) respectively.

$$N_{SM_{AAC}} = \frac{\hat{V}_{AC}}{V_{SM}}(1 + n_R) \tag{2.26}$$

$$N_{director} = \frac{V_{DC}}{2V_{SM}}(1 + n_R) \tag{2.27}$$

The number of SMs, and subsequently the number of IGBTs required for the converters are given in Table 2.4.

Although the AAC has twice the number of IGBTs per SM, the IGBT count shows that just over 50% more devices are required compared to the MMC. This shows the advantage of sharing the voltage blocking capability between the stack of SMs

| Parameter | Value | |
|---|---|---|
| Converter | HB MMC | AAC |
| No. SMs per arm | 352 | 224 |
| No. of IGBTs per SM | 2 | 4 |
| No. of arms | 6 | 6 |
| No. director switches | n/a | 176 |
| Total no. IGBTs | 4,224 | 6,432 |

**Table 2.4.:** Number of SMs and IGBTs

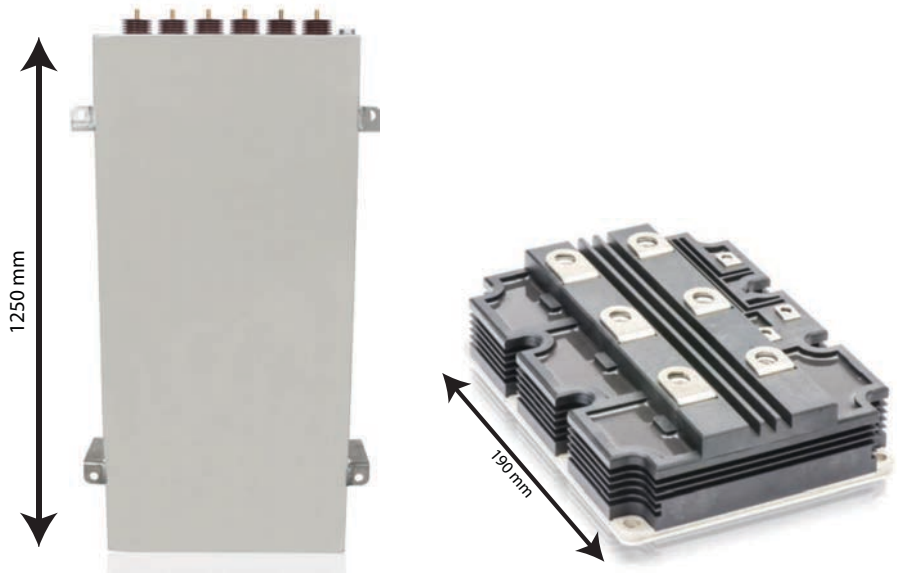
and the director switches in the AAC.

### Submodule Volume Estimate

When placing any equipment into the offshore environment space immediately becomes a premium as a platform is required to hold the equipment. The main component which accounts for the majority of the SM volume is the capacitor. From Figure 2.4a it can be observed that the capacitor, the blue section, accounts for approximately half the volume of the SM. Figure 2.10 shows the size difference between the IGBT/diode module and the capacitor is evident. The height given is for a capacitor value of 8.1 mF for a maximum voltage of 4 kV.

The capacitor values for both the MMC and AAC can be found using (2.6) and (2.22). The volume of the capacitor can be estimated using data from the ABB DryDCap which is designed specifically for use in VSCs. It has a high energy density, making the component compact, and has a high reliability [91]. Table 2.5 shows the difference in volume for the two capacitor values.

This table shows that the volume of the capacitor of the AAC is just over half the volume of the MMC capacitor. Assuming that half of the volume of the MMC SM is




**(a)** ABB DryDCap capacitor [91] **(b)** IGBT module [92]

**Figure 2.10.:** SM electrical components

| Parameter | Value | |
|---|---|---|
| Converter | MMC | AAC |
| Capacitor value (mF) | 10 | 4.7 |
| Capacitor volume ($m^3$) | 0.1203 | 0.0621 |

**Table 2.5.:** Capacitor volume estimate

occupied by the capacitor, the total power module, which includes components such the IGBT/diode modules, bypass switch, power supply units, and cooling, the total SM volume can be estimated to be approximately 0.2406 $m^3$. Table 2.6 shows the respective volumes of the MMC and AAC SMs, assuming the power module volume does not change. It should be noted that the volume of the director switches were not considered in this estimate.

| Parameter | Value | |
|---|---|---|
| Converter | MMC | AAC |
| Capacitor volume ($m^3$) | 0.1203 | 0.0621 |
| Power module volume ($m^3$) | 0.1203 | 0.1203 |
| SM volume ($m^3$) | 0.2406 | 0.1824 |

**Table 2.6.:** SM volume estimate

## 2.5. Summary

The MMC converter and its operation is described at the beginning of the chapter. The energy balancing mechanisms for the converter are also discussed. The MMC cannot protect against DC side faults, and alternative MMC designs were described that would provide DC fault blocking were described. The Diode-Clamped Submodule provides DC fault blocking but at the expense of increased power losses compared the HB MMC, but the losses are lower than the FB MMC topology. Another option is to have a hybrid stack in the MMC, where there are both HB and FB SMs in the stack. This solution can provide DC fault blocking with reduced power losses compared to the FB MMC but greater losses than the HB design. The hybrid design has lower losses than the Diode-Clamped submodule.

A promising DC fault tolerant topology, the AAC, was described. The topology is a hybrid VSC and uses a combination of FB SMs and director switches in the arm of the converter. This means that the voltage blocking capability of the arm is shared between the SMs and the director switches, reducing the number of SMs required. The use of FB SMs allows the converter to block DC side fault. The energy balancing mechanisms fo the AAC were also described.

The MMC and AAC characteristics were briefly compared and a comparison of the number of IGBTs in each converter and the SM volume was carried out. Despite having twice the number of IGBTs in each SM, the AAC requires approximately 50% more IGBTs than the MMC. This is due to the director switches in the AAC

sharing the voltage blocking capability with the SMs. The volume of the SM is dominated by the volume of the capacitor. As the AAC requires less energy storage, this results in a smaller capacitor value and hence a smaller capacitor volume. The volume of the AAC SM capacitor was just over half that of the MMC.

# 3. DC/DC Converters

## 3.1. Introduction

This chapter addresses the question of what DC/DC converters that are in the literature and could be made available for HVDC applications, with a particular focus on converters capable of low to medium voltage conversion ratio as defined in Table 3.1, where $V_H$ is greater than $V_L$ . There is no single device that can efficiently transform DC voltage for all scenarios [93]. There are many DC/DC converter topologies for low voltage, low power applications but as the voltage and power increase beyond the ratings of a single semiconductor device, these circuits become unsuitable. This is mainly due to high switching losses and high frequency operation of this type of DC/DC converter becomes unmanageable at high voltage, high power levels [38, 94].

| **Conversion Ratio** | $V_H/V_L$ |
|---|---|
| Low | $\leq$1.5 |
| Medium | 1.5 - 5 |
| High | $\geq$5 |

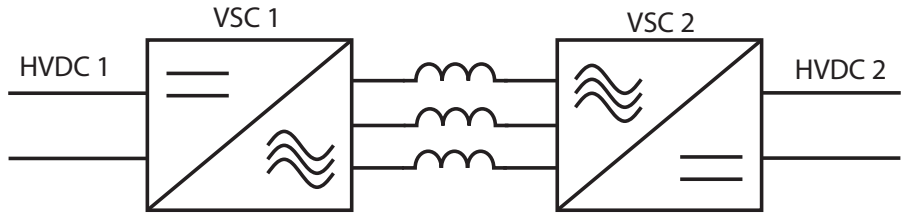
**Table 3.1.:** Voltage conversion ratio [93]

## 3.2. Background

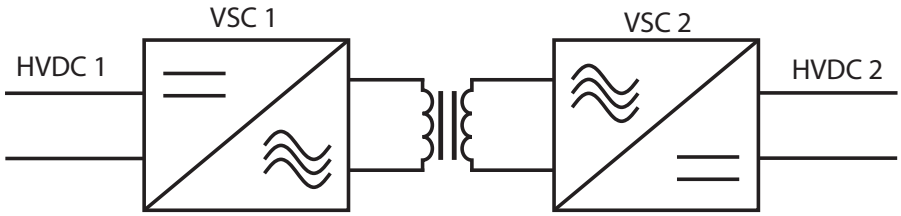
There are two ways of converting DC voltage; directly and via an AC stage. The former transfers the majority of the input power directly to the output and the rest is used for additional operating mechanisms which balances the energy in the converter. The latter converts all the input power into AC, which may not necessarily be sinusoidal, which is then rectified and sent to the output of the converter. A review of different DC/DC converters for low to medium voltage conversion ratio and high power applications, such as the interconnection of HVDC systems at similar voltage magnitudes, is provided in this section.

### 3.2.1. Front-to-Front Converter

The circuit topology which may be considered the most technology ready for HVDC use, as it utilises established converter technologies, is the front-to-front DC/DC converter. This converter comprises of two AC/DC converters connected through the AC side. Several examples of such converters are outlined in [93]. A low conversion ratio topology is elaborated upon in [95] and is depicted simply in Figure 3.1a and as a medium or high conversion ratio topology which uses a transformer is shown in Figure 3.1b.




**(a)** Inductor coupled




**(b)** Transformer coupled

**Figure 3.1.:** Front-to-front DC/DC converter

The converter can be coupled on the AC side using inductors or a transformer depending on the desired conversion ratio. The use of inductors limits the voltage conversion ratio of the topology as the DC bus voltage is related to the peak AC voltage and operating away from this condition can compromise the operation of the converter [95]. Alternatively a transformer can be used in the intermediary AC link to increase the voltage conversion ratio by allowing the AC voltage magnitude seen by each VSC to be optimal dependent on its DC bus voltage [44]. The two VSCs can be HB or FB MMCs or other modular VSCs such as those described in [87, 96]. A front-to-front converter based on the AAC is studied in [95]. DC fault current interruption can be achieved in the converter by breaking the current using a traditional circuit breaker in the AC stage, by blocking the VSC on the non-faulted DC-side thus disabling the AC link, or through the use of FB SMs in the converter. Full bridge SMs are only required in one VSC in the topology to achieve DC fault current interruption and they can be placed on the lower DC voltage side to keep the power loss figure low [95].

An issue with this arrangement is the two-stage conversion which presents several disadvantages. First the use of two AC/DC in the design increases the volume of the DC/DC converter, potentially prohibiting the converter from being used in space constrained applications such as offshore platforms. Secondly, each successive conversion stage increases the losses of the converter .

The intermediary AC link is independent of any other AC connection, this allows the freedom to choose the AC waveform shape and frequency. The use of a higher frequency could allow for optimisation of the volume of the passive components, such as the capacitors and phase inductors, thus reducing the converter volume. However, it was observed in simulation that as the frequency increases, so do the power losses for the converter which was mainly driven the switching losses in the semiconductors [44]. To illustrate, the power losses for an MMC based DC/DC converter (with MMCs on both sides) at 50 Hz was 1.5% and at 350 Hz it was 2.6%.

Another application for the front-to-front converter could be the interfacing of different HVDC technologies, such as in [93] where a topology is proposed to interconnect CSC and VSC HVDC systems. The converter is required to maintain the voltage polarity on the VSC side while allowing the reversal of voltage polarity on the CSC side when the flow of power changes direction.

### 3.2.2. HVDC Auto Transformer

An adaption of the front-to-front converter which is based on the direct conversion principle is presented in [97]. This topology also uses two VSCs but they are now stacked on top of each other, with the lower converter handling the lower voltage and the upper converter handling the voltage difference between the two DC buses. The VSCs are connected through a parallel transformer, as shown in Figure 3.2. In this converter arrangement the transformer does not transfer the total power

of the converter. The transformer is used solely for balancing the energy between the upper and lower converters which is inherent to the direct conversion process. Typically for low conversion ratios, the transformer would be rated for 50%, or less, of the total transferable power [97]. The equation to determine the power rating of the transformer, $P_{Tf}$, is given in (3.1), where $n$ is the conversion ratio and $P_{DC}$ is the DC power [97]. This equation shows that as the conversion ratio increases so does the power rating of the transformer.

$$P_{Tf} = \frac{n-1}{n} P_{DC} \tag{3.1}$$

This converter is also able to provide DC fault blocking capabilities and this is dependent on the number of FB SMs used in the upper converter. There are three voltage blocking requirements the upper converter must meet in order to provide the DC fault blocking capability, as given below [97]:

1. In the case of a fault on the lower DC bus voltage side, the upper stacks must have sufficient positive voltage capability in order to match the total higher DC bus voltage

2. In the case of a fault on the higher DC bus voltage side, the lower stacks must have sufficient positive voltage capability in order to match the total higher DC bus voltage

3. Sufficient voltage blocking capability in the forward direction to guarantee converter functionality in a fault scenario

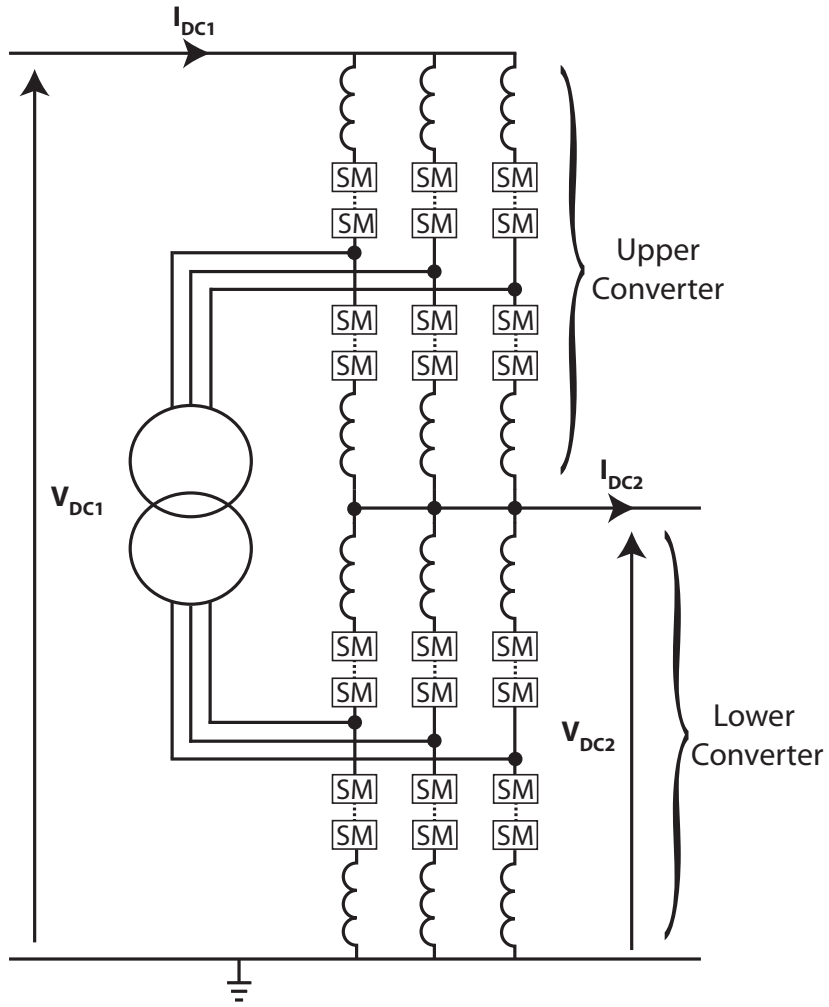



**Figure 3.2.:** HVDC auto transformer

In general only HB SMs are required in lower converter, as the lower converter has no influence on the fault on either DC bus [97]. A combination of FB and HB SMs are used in the upper converter to provide DC fault blocking, and the ratio of the FB to HB is dependent on the conversion ratio. For ratios less than two, there are more FB SMs required than HB SMs in the upper converter to ensure DC fault blocking capability. For example, a conversion ratio of 1.5 would require approximately 70% of the SMs in the upper converter to be FB and the rest to be HB [97]. As this topology requires fewer SMs than the front-to-front topology;

about the same number of SMs as in the MMC on the high voltage DC bus side of the front-to-front topology. This leads to lower power losses of around 0.6% for a 1.5 conversion ratio as estimated in [98].

### 3.2.3. Modular Multilevel DC/DC Converter

The modular multilevel DC/DC converter is detailed in [99]. This is a single stage DC/DC conversion that circulates AC currents within the converter to balance the SMs. The two-leg version of the converter is shown in Figure 3.3.

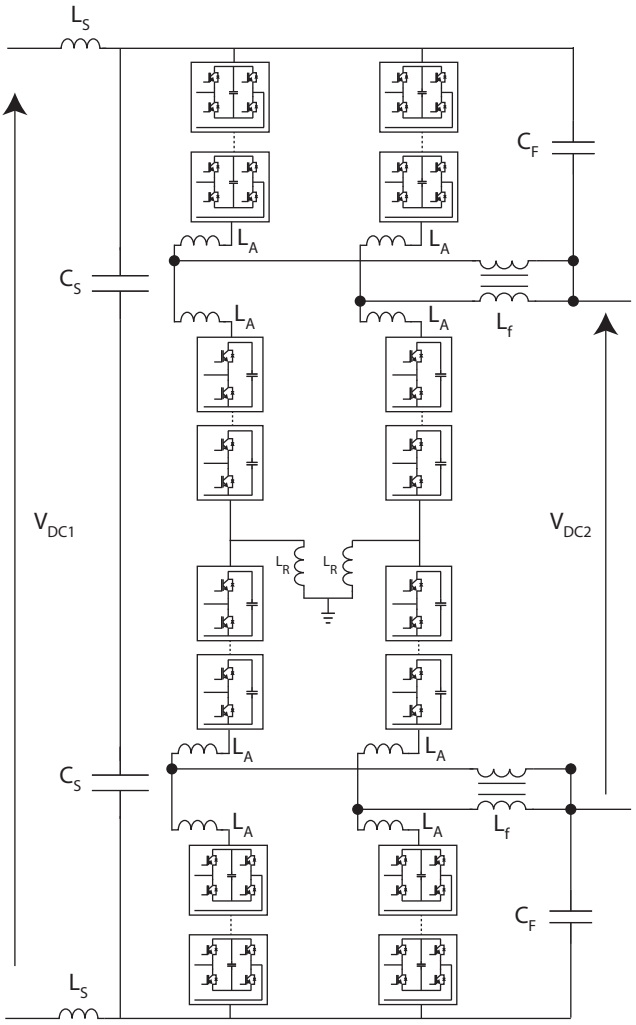



**Figure 3.3.:** Modular multilevel DC/DC converter

The converter can also be arranged in a three-leg structure, but the advantage of the two-leg design is that the filter inductors, $L_f$, can be arranged as a coupled pair [99]. The converter should be designed such that the inner converter controls the lower DC bus voltage and the outer converter controls the higher DC bus voltage. The ratio of HB SMs to FB SMs is determined from the voltage conversion ratio. FB SMs are used in the outer arms as they can insert a negative voltage which allows the converter to preform both step-up and step-down voltage conversion. Additionally by using FB SMs in the outer arms of the converter it is able to provide DC fault blocking capabilities [100].

The energy within the converter is balanced by circulating AC currents which is achieved by controlling each pair of arms to generate a net AC voltage. The AC currents are circulated within the upper and lower arms of the converter, and this enables power exchange between inner and outer arms to balance the voltage of the SM capacitors. The AC power required to balance the SMs, for the two-leg design is proportional to a quarter of the total power transfer capability of the converter [100]. An issue that arises from these circulating AC currents in that they need to be filtered from the DC current at the output terminals of the converter. This results in a substantial inductor, $L_f$, is needed to filter the DC current. To illustrate, in [100] a 14 MW converter is simulated with input bus voltage of 17.6 kV, $V_{DC1}$, and the filter inductor required is 990 mH with a maximum rms inductor winding current of 795 A.

### 3.2.4. LCL DC/DC Converter

A completely different DC/DC converter is described in [101]. The converter can be described as a two-stage converter as it has a high frequency intermediate AC stage.

The topology is shown in Figure 3.4. Previous iterations of this converter used thyristor devices and is studied in further detail in subsequent sections. The result of using IGBTs is better semiconductor utilisation compared with earlier designs, as the bridge on the low voltage ($V_1$) side does not need to be rated for the higher voltage ($V_2$). The converter operates by inverting the DC on the low voltage side through the switching of pairs of IGBT valves. This creates a resonant frequency between the passive elements, $L_1$, $L_2$, and $C_r$, in the centre of the converter which performs the voltage transformation. The high voltage bridge rectifies the voltage. A useful aspect of the symmetrical design is that converter is able to block DC side faults. The design was simulated for a high voltage conversion ratio in [101], stepping 20 kV to 300 kV and the power losses were estimated to be lower than 2% which is lower than the earlier thyristor based converter [38].

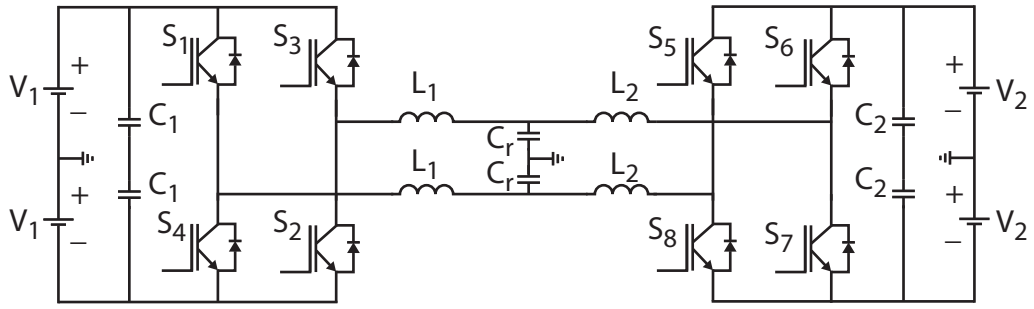



**Figure 3.4.:** LCL DC/DC converter

By having valves comprised of series connected IGBTs the converter may not be suitable for very high voltage applications, as switching all the IGBTs in the valve at the same instant becomes a challenge [58]. Another concern with this converter is the significant filtering that the DC current requires and implies the use of large DC bus capacitors on the terminals of the converter. The current waveform, prior to filtering, has the shape of classic diode-rectified sinusoidal waveform.

## 3.3. Resonant DC/DC Converter

At the start of this research, there were very few high voltage, high power DC/DC converters in the literature. One prominent topology was a resonant DC/DC converter described initially in [102].

### 3.3.1. Principle of Operation

This family of converters use resonance to transform the DC voltage and was originally introduced in [102]. The circuit diagram of the unidirectional converter is shown in Figure 3.5. The converter inverts the AC voltage using the bridge of thyristor valves on the low voltage side, $V_1$. The thyristors valves are switched in pairs to effectively rotate the voltage of the intermediary resonant capacitor and create a resonant path with the inductor $L_r$. This resonance brings the advantage of providing a natural zero-crossing of the current to turn the thyristors off.

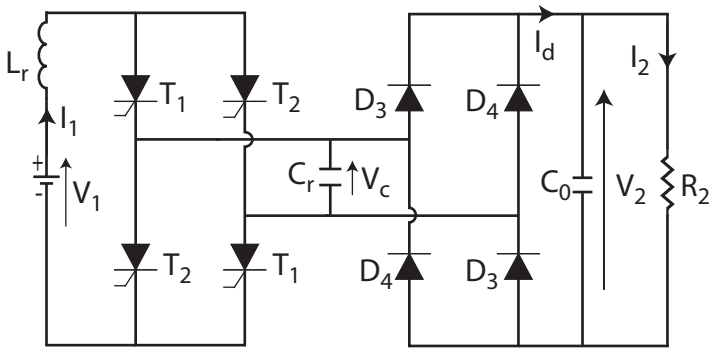



**Figure 3.5.:** Unidirectional resonant DC/DC converter

The benefit of using thyristor devices, when compared to the IGBT, is that device is more robust to fault events, has higher voltage and current ratings, and is more power efficient. This allows fewer devices to be used in the valve which lowers the

conduction losses of the converter. The converter can be designed to operate in Discontinuous Conduction Mode (DCM), which is where the current in the converter falls to zero and the waveform becomes discontinuous [103]. By switching the devices at zero current, termed soft-switching, the switching losses of the converter are reduced. The converter can also be operated in Continuous Conduction Mode (CCM) by increasing the switching frequency which results in the current being above zero and being a continuous waveform [103]. Using CCM increases the switching losses of the converter. Example CCM and DCM waveforms are shown below in Figure 3.6.

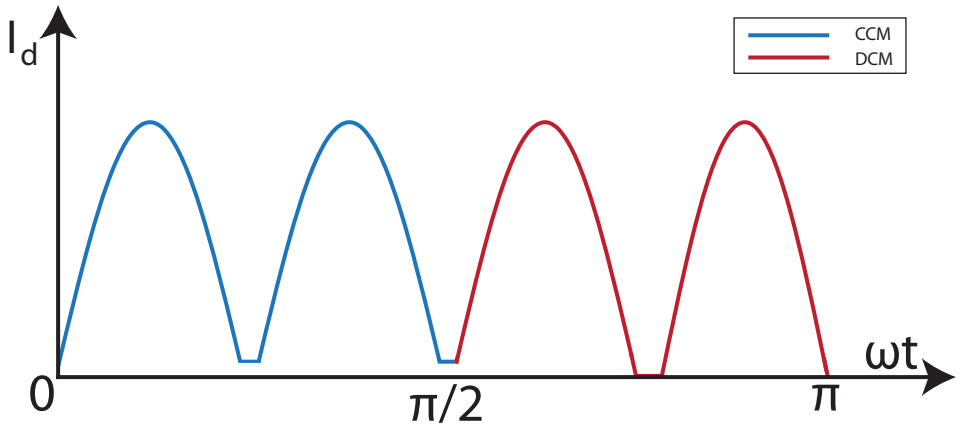



**Figure 3.6.:** Waveforms for CCM and DCM

There are several design criteria for this converter. In order to avoid commutation failure, where there is not sufficient time for the current to fall below the holding current allowing the thyristor to turn off, there is a maximum switching frequency limit which is given in (3.2), where $T_q$ is the extinction time of the thyristor.

$$\frac{1}{T_s} = f_s \leq f_{s_{MAX}} = \frac{1}{2T_q} \tag{3.2}$$

Once the switching frequency is defined, the terminal voltages and the power of the converter must be specified in order to determine the values of the passive elements. If the converter is assumed to be lossless, then the energy converted

over one cycle, $E_{DC}^{cycle}$, is equal to the total energy transferred through the resonant capacitor, $E_{Transfer}$. These energies, taken from [102], are defined below.

$$E_{DC_1}^{cycle} = I_1 V_1 T_s \tag{3.3}$$

$$E_{DC_2}^{cycle} = I_2 V_2 T_s \tag{3.4}$$

$$E_{Transfer} = \frac{2V_1 V_2^2 C_r}{(V_2 - V_1)} \tag{3.5}$$

Knowing that the energy transferred is equal to the average cycle energy, as shown in (3.6a), the value of the resonant capacitor, $C_r$, can be determined as derived below.

$$E_{cycle_{AVG}} = E_{Transfer} \tag{3.6a}$$

$$I_2 V_2 T_s = \frac{2V_1 V_2^2 C_r}{(V_2 - V_1)} \tag{3.6b}$$

$$\therefore\ C_r = \frac{I_2 (V_2 - V_1)}{2 f_s V_1 V_2} \tag{3.6c}$$

As this is a resonant system the value of the inductor, $L_r$, can be determined from the equation for resonant pulsation given in (3.7).

$$\omega_r = \frac{1}{\sqrt{C_r L_r}} \tag{3.7}$$

However, to ensure the converter operates in DCM the resonant frequency must be at least twice as fast as the switching frequency of the converter as defined in [102] giving the condition for $L_r$, shown in (3.8).

$$L_r \leq \frac{1}{\pi^2 f_s^2 C_r} \tag{3.8}$$

The converter is controlled using a Proportional Integral (PI) voltage controller

and a phase-lock loop is used to ensure the switching of the thyristors pairs are synchronised with voltage across the intermediary capacitor, $V_c$. The frequency reference is then used by the pulse generator to send firing signals to the thyristors. The firing signals are sent at a duty ratio of 50%, in order for each pair of thyristors to conduct for up to half the switching cycle. The control structure is shown in Figure 3.7.

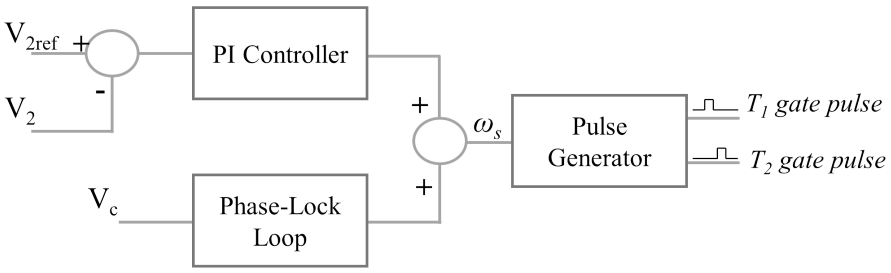



**Figure 3.7.:** Resonant converter control structure

In order to understand the converter further, it was was modelled in MATLAB Simulink, using the SimPowerSystems library. In [102], a 4 kV to 80 kV 5 MW step-up converter with a resistive load is presented; this model was replicated and simulated here. Several converter waveforms are shown in Figure 3.8. For this simulation the control variable was the output voltage.

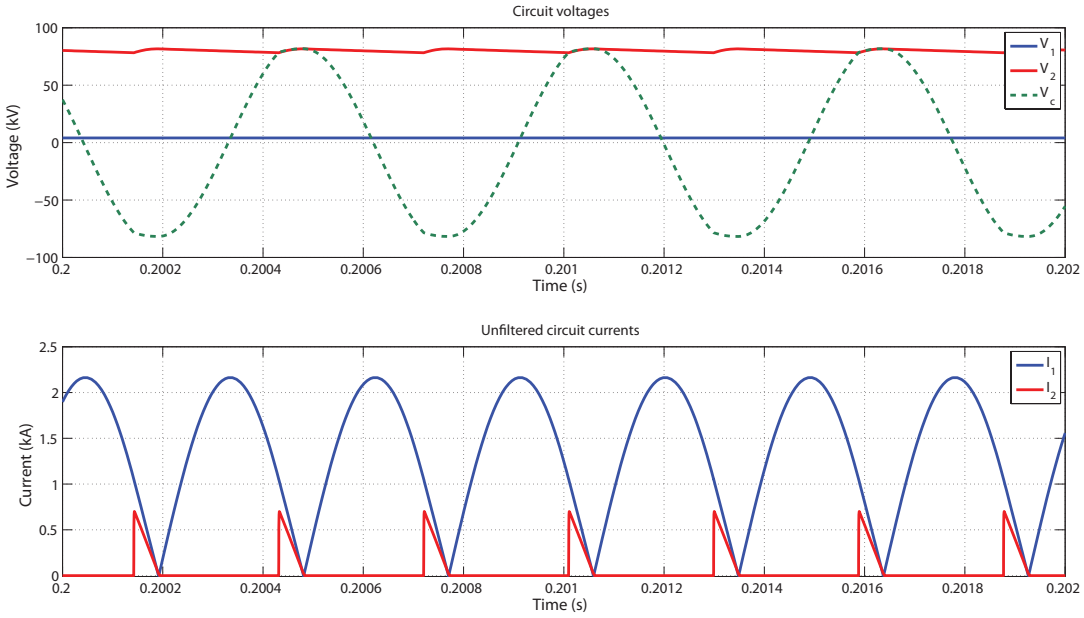



**Figure 3.8.:** Resonant converter waveforms

The intermediary AC stage of the converter can be seen in the capacitor voltage waveform, $V_c$. The peak voltage amplitude is the same at the output DC voltage of 80 kV and a ripple from the AC voltage can be seen in the output DC voltage as a diode rectifier is used. It can be seen from the current waveforms that there is a significant filtering requirement for the converter. It can also be seen that the peak current in the converter is much higher than the average DC current.

This converter design allows power flow in only one direction and this could be used in applications where a DC source produces energy and requires a step-up to a higher voltage magnitude. This converter would not be suitable for interconnections between HVDC systems as it would only be able to facilitate power flow in one direction.

### 3.3.2. Bidirectional Resonant DC/DC Converter

To create a MTDC grid it is desirable to have bidirectional power flow through out the network. To achieve this with the resonant DC/DC converter, the thyristor valve configuration is mirrored on the high voltage side and this was presented in [104]. The full circuit diagram is shown in Figure 3.9.

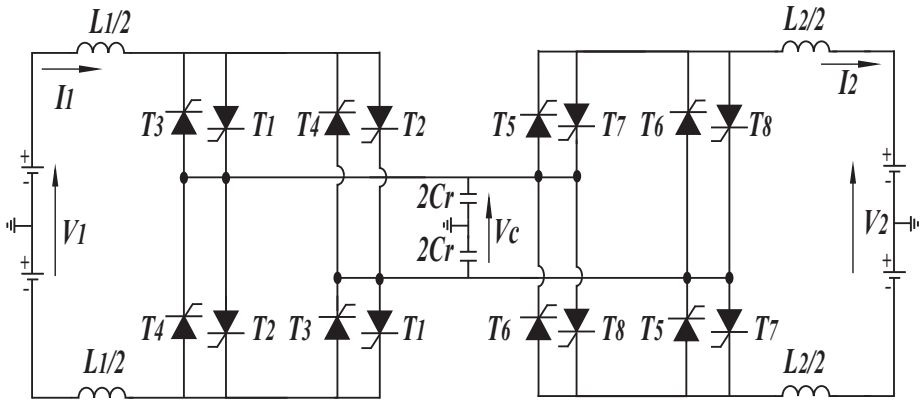



**Figure 3.9.:** Bidirectional resonant DC/DC converter

This resonant converter uses two LC circuits to transfer the energy through the converter. The resonant inductors are connected to the capacitor through the firing of the thyristors. The symmetry of this design allows the converter to easily change the power flow through, either by changing current polarity or changing the voltage polarity. The research in this thesis focuses solely on interconnection of VSC systems and so only the current polarity change will be used to change power flow. It should be noted that this topology could be used to interface different HVDC technologies, allowing a VSC system to be connected to a CSC system.

This converter design is able to provide DC fault blocking. To achieve this, it is necessary to have the same number of thyristors in all valves of the converter, i.e the low voltage bridge must be rated for the higher voltage in order to withstand

a collapse of the DC bus on the high voltage side. This has a penalty in terms of increased volume and conduction power losses.

In [105] it is shown that the losses for the converter significantly decrease the closer the voltage conversion ratio is to unity. Medium voltage conversion ratio converters, as defined in sec. 3.1, are studied in [104, 106] and the converter losses are estimated to be in the region of 5% to 1.2%. A prototype of this converter was developed at 30 kW, 200 V to 900 V and is detailed in [107]. The overall power losses of the experimental setup was observed to be 8% and the main contributor to this loss figure was the resistance of the resonant inductors.

### Simulations

It was decided to explore the properties of this converter topology further in order to determine its suitability for low to medium conversion ratio applications, as previous studies had considered only high conversion ratios. A 80 kV to 160 kV, 100 MW bidirectional converter was modelled in MATLAB Simulink. The thyristor device used in the simulation was the ABB 5STP 21H4240 phase control thyristor, and the parameters of the device are given in Table 3.2.

| **Parameter** | **Value** | **Unit** |
|---|---|---|
| $V_T$ | 4,200 | V |
| $I_m$ | 2,192 | A |
| $V_{TO}$ | 1.249 | V |
| $r_T$ | 0.191 | mΩ |

**Table 3.2.:** Phase control thyristor parameters of ABB 5STP 21H4240

The number of devices in the valve is dependent on the higher DC bus voltage, $V_2$, and the utilisation of the thyristors. In general high power semiconductors

are not operated at their rated voltage to allow voltage headroom for over-voltage transients at turn-off [108]. Thus in order to operate the thyristors safely they should be normally operated at just under half their rated voltage, approximately 45% according to [108]. Another consideration is the resonant voltage peak voltage in the circuit can be up to 30% higher than $V_2$, and should be accounted for when calculating the number of devices required in the valve [104]. Table 3.3 shows the parameter for the 100 MW simulation converter model.

| **Parameter** | **Value** |
|---|---|
| P | 100 MW |
| $V_1$ | 80 kV |
| $V_2$ | 160 kV |
| $f_s$ | 720 Hz |
| $f_{s_{max}}$ | 1250 Hz |
| $C_r$ | 4 uF |
| $L_1$ | 25 mH |
| $L_2$ | 1 mH |
| No. of devices per valve | 83 |

**Table 3.3.:** 100 MW resonant DC/DC converter parameters

The voltage and current waveforms for step-up operation are shown in Figure 3.10, and step-down operation in Figure 3.11, both cases using a resistive load and are observed from start-up.

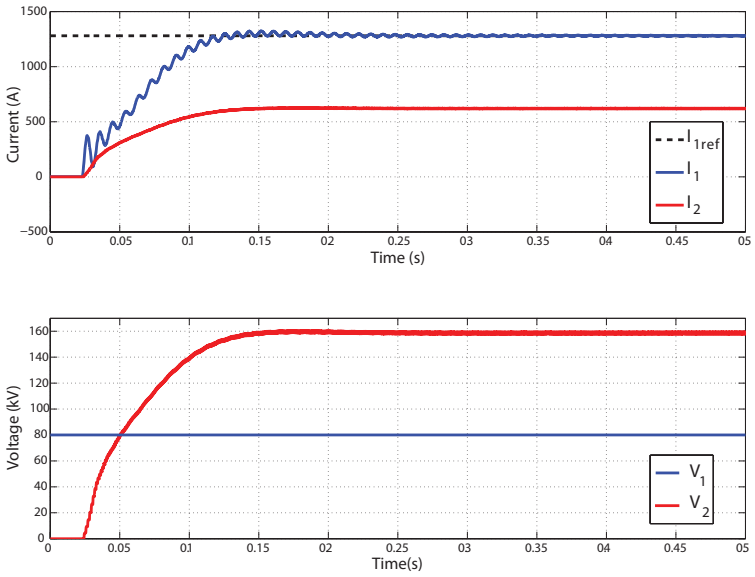



**Figure 3.10.:** Step-up converter waveforms

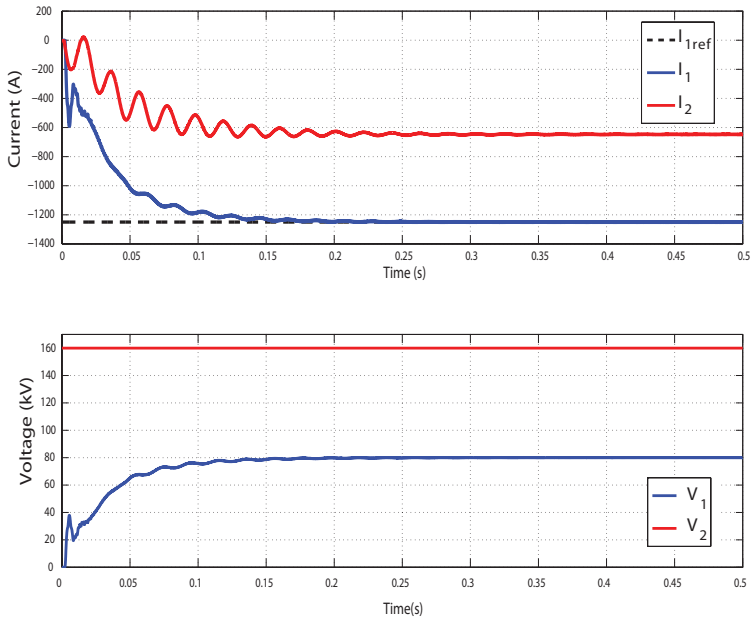



**Figure 3.11.:** Step-down converter waveforms

The oscillations at the beginning of the simulation are a result of the PI current controller.

The power losses for this circuit were estimated by using post-processing script in MATLAB. As the converter is soft-switched in DCM, it was assumed that the switching losses of the converter were negligible and thus only the conduction losses of the devices in the converter were considered. The thyristor valves were represented as fixed voltage sources with a series resistance when conducting, using the figures from Table 3.2. Thus the power losses can be found through analysing the current waveforms from the converter by post-processing the the simulation data. An example of the unfiltered current waveform shape of $I_2$ is shown in Figure 3.12.

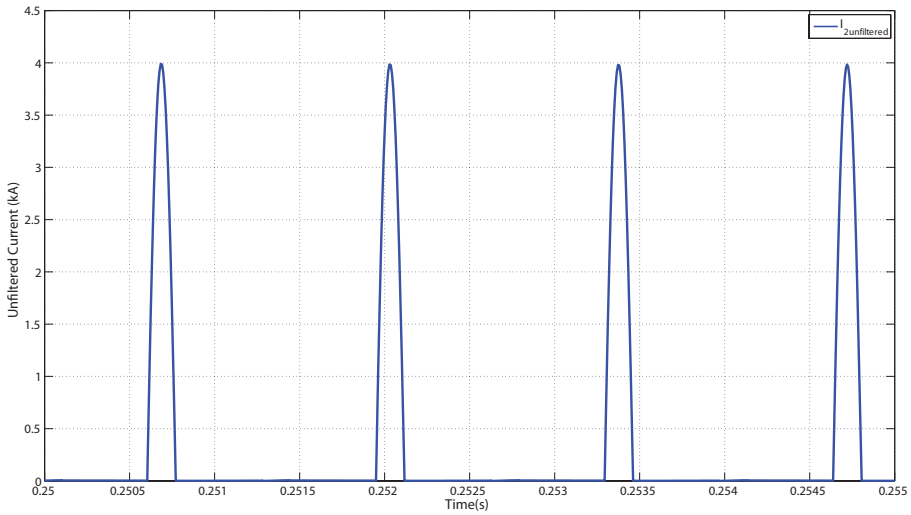



**Figure 3.12.:** Shape of unfiltered current waveform through thyristor valve

This process was carried out for the high and low voltage bridges and the estimated conduction losses are shown in Table 3.4, note that the losses from the inductors was not considered.

| | |
|---|---|
| HV side losses (kW) | 192 |
| LV side losses (kW) | 321 |
| Total losses (kW) | 513 |
| Total relative losses (%) | 0.52 |

**Table 3.4.:** Thyristor conduction losses for 100 MW converter

Through a literature review of this family of resonant converters, it was observed that the power losses increase as the voltage conversion ratio increases. Figure 3.13 shows that it is also the case with this converter where the power losses increase approximately linearly with conversion ratio. The first data point in the graph is for a conversion of two and uses the power loss figure from Table 3.4.

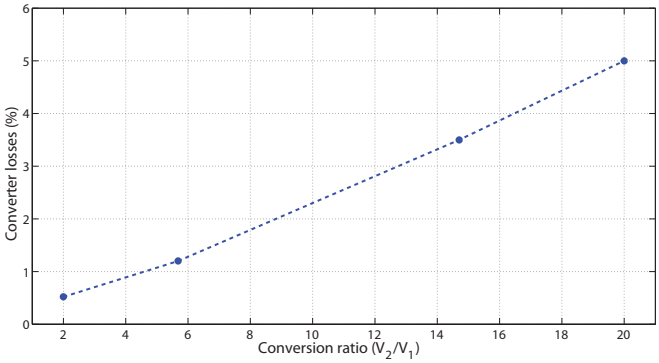



**Figure 3.13.:** Conversion ratio versus relative power losses [104, 109, 106]

These low power losses at low to medium conversion ratios implies that this converter is suitable for interconnecting HVDC systems operating at similar voltage magnitudes. A disadvantage of the converter is the poor utilisation of the thyristors devices in that as the low voltage bridge of the converter requires enough thyristors in each valve to block the higher DC bus voltage to ensure DC fault blocking. This penalty is small if the voltage conversion ratio is low. Additionally the converter currents require significant filtering and this would contribute negatively in terms of volume, cost, and power losses of the converter.

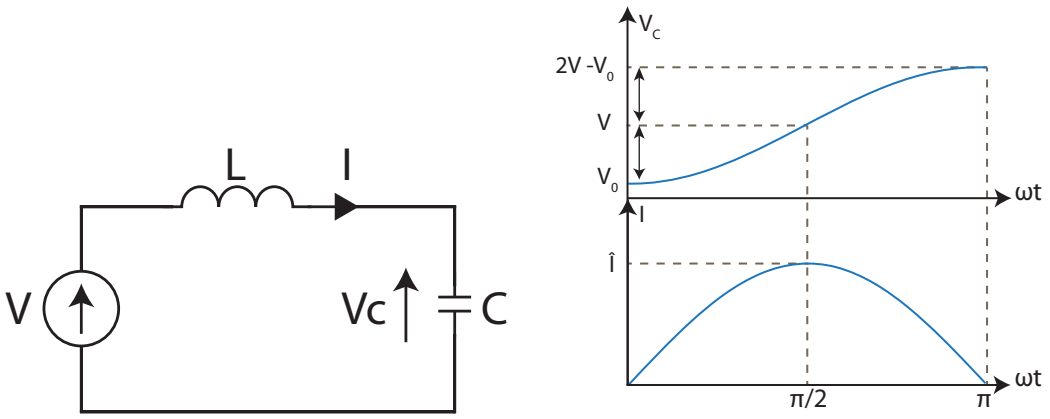
## 3.4. Alternate Discontinuous Mode Operation

In testing the effectiveness of the fault blocking operation of the converter it was observed that it is vulnerable to DC side faults if the conversion ratio is below two, where the DC bus voltages are similar in magnitude. This is because there is a stage in the conversion process when both bridges of the converter are connected and should the voltage on the low-voltage side decrease such that the conversion ratio were lower than two, such as a DC-side fault, then the turn-off time for the thyristors decreases and the thyristors will not have sufficient time to turn off, allowing the fault to propagate through the converter. This was reported in [106, 110].

A new method of operation for this converter was developed in a collaboration with Dr Merlin with a view to overcoming this weakness. It is termed the Alternate Discontinuous Mode (ADM) becasue the two bridges of the converter are alternately switched and the converter is run in DCM (as before) to achieve soft-switching conditions.

In ADM the converter can block DC side faults for all scenarios, as both sides of the converter are never connected together at the same instant, thus allowing the converter to be used in applications where a lower conversion ratio than two is required, such as interconnecting two HVDC links.

To understand this mode of operation fully, the operation of a simple LC circuit is considered, shown in Figure 3.14.




**(a)** LC circuit **(b)** Associated waveforms

**Figure 3.14.:** Simple LC circuit and waveforms

At $t = 0$ the capacitor voltage is equal to the initial voltage, $Vo$, and the inductor current is zero. The resonant frequency is given in (3.9).

$$\omega_r = \frac{1}{\sqrt{LC}} \tag{3.9}$$

At the end of the first half cycle, the current is back to zero after reaching its peak given in (3.10) and the capacitor voltage has risen by twice the voltage difference between the voltage source defined and the initial voltage, $V_0$, as shown in (3.11).

$$\hat{I} = C\omega(V - V_0) = \sqrt{\frac{C}{L}}(V - V_0) \tag{3.10}$$

$$\hat{V}_c = V_0 + 2(V - V_0) = 2V - V_0 \tag{3.11}$$

The entire converter can be thought of as two LC circuits which share a common capacitor. The capacitor is connected alternately to each inductor by using the

corresponding pairs of thyristors. The connection order for one cycle is detailed below:

- $V_1$ with $L_1$ through switching pair $T_1$ or $T_3$
- $V_2$ with $L_2$ through switching pair $T_5$ or $T_7$
- $-V_1$ with $L_1$ through switching pair $T_2$ or $T_4$
- $-V_2$ with $L_2$ through switching pair $T_6$ or $T_8$

It can be seen that the capacitor voltage will oscillate around the four points listed above. The final waveform centres around zero volts due to control action or parallel resistance losses. The initial voltage at the beginning of the cycle is defined in (3.12).

$$V_0 = V_1 - V_2 \tag{3.12}$$

The maximum capacitor voltage is defined as the sum of the two DC bus voltages, as shown in (3.13).

$$\hat{V}_c = 2V_1 - V_0 = V_1 + V_2 \tag{3.13}$$

Using this equation the peak currents through each bridge of the converter can be determined as shown below.

$$\hat{I}_1 = C_r\omega_1(V_1 - V_0) = \sqrt{\frac{C_r}{L_1}}V_2 \tag{3.14}$$

$$\hat{I}_2 = C_r\omega_1(V_0 - V_2) = \sqrt{\frac{C_r}{L_2}}V_1 \tag{3.15}$$

By assuming that the converter is lossless, the power transfer can be defined as twice the energy per half cycle multiplied by the frequency of these cycles, shown in

(3.16).

$$P = 2Ef_s \tag{3.16}$$

Over one cycle the energy transferred through the converter can be described by the following equations.

$$\begin{aligned}
\Delta E &= \frac{1}{2}C_r\hat{V}_c^2 - \frac{1}{2}C_rV_0^2 && (3.17a)\\
&= \frac{1}{2}C_r(\hat{V}_c^2 - V_0^2) && (3.17b)\\
&= \frac{1}{2}C_r\left[(2V_1 - V_0)^2 - V_0^2\right] && (3.17c)\\
&= \frac{1}{2}C_r\left[4V_1^2 - 4V_1V_0 + V_0^2 - V_0^2\right] && (3.17d)\\
&= \frac{1}{2}C_r\left[4V_1^2 - 4V_1V_0\right] && (3.17e)\\
&= 2C_rV_1\left[V_1 - V_0\right] && (3.17f)
\end{aligned}$$

Substituting this in to (3.16) gives:

$$\begin{aligned}
P &= 2\Delta Ef && (3.18a)\\
&= 4C_rV_1\left[V_1 - V_0\right]f_s && (3.18b)\\
&= 4C_rV_1V_2f_s && (3.18c)
\end{aligned}$$

From these equations, it can be seen that the power transfer is directly proportional to the frequency. Equation (3.18c) allows the value of the intermediary capacitor to be found simply from the specifications of the converter.

The frequency is used to determine the delay between each gate pulse sequence sent to the thyristor pairs in the two bridges of the converter. Each pulse sequence

will result in the same amount of energy being passed through the converter thus increasing the time between two pulse sequences will proportionally decrease the average power transfer of the converter.

To ensure the converter operates in DCM the maximum operational frequency is the inverse sum of the two resonant circuits in the converter, given in (3.19) and (3.20).

$$T_1 = \frac{\pi}{\omega_1} = \pi\sqrt{L_1 C_r} \tag{3.19}$$

$$T_2 = \frac{\pi}{\omega_2} = \pi\sqrt{L_2 C_r} \tag{3.20}$$

The frequency limit is defined in (3.21).

$$f_{max} = \frac{1}{T_1 + T_2} = \frac{f_1 f_2}{f_1 + f_2} = \frac{1}{2\pi\sqrt{C_r}(\sqrt{L_1} + \sqrt{L_2})} \tag{3.21}$$

The converter may be operated in CCM by increasing the frequency beyond the DCM limit to allow for greater power transfer. However, this would come at the penalty of increased switching losses as the converter would no longer be soft-switched.

The dominant power losses for this converter when operated in ADM are the conduction losses and the equation is defined in (3.22), where $I$ is the current through the thyristor and $V_{TO}$ and $R$ are the on-state voltage and the resistance of the thyristor respectively.

$$P_C = V_{TO} I + R I^2 \tag{3.22}$$

As conduction through a resonant pair of thyristors occurs for only half the cycle, and the number of series thyristors in a valve is $N$, the conduction loss equation can

be written as in (3.23).

$$P_C = 2N\left(V_{TO}I + RI^2\right) \tag{3.23}$$

The conduction loss for both bridges over a complete cycle is given in (3.24).

$$P_{C_T} = 2f\left[2N\left(V_{TO}I_1 + RI_1^2\right) + 2N\left(V_{TO}I_2 + RI_2^2\right)\right] \tag{3.24}$$

The average and rms current over half a cycle is found by integrating over the period from zero to π, these currents are used to determine the conduction losses using Equation (3.23). A complete derivation is shown in Appendix A, and the average and rms currents for the thyristor are defined below.

$$\langle I\rangle = \frac{2\hat{I}}{\omega_R} \tag{3.25}$$

$$\left\langle I^2\right\rangle = \frac{\pi\hat{I}^2}{2\omega_R} \tag{3.26}$$

Substituting these average current values into (3.24) gives the final conduction loss equation below.

$$P_{C_T} = 2fN\left(\frac{4V_{TO}\hat{I}_1}{\omega_1} + \frac{2R\pi\hat{I}_1^2}{2\omega_1} + \frac{4V_{TO}\hat{I}_2}{\omega_2} + \frac{2R\pi\hat{I}_2^2}{2\omega_2}\right) \tag{3.27a}$$

$$= 2fC_rN\left(4V_{TO}V_1 + \pi R\sqrt{\frac{C_r}{L_2}}V_1^2 + 4V_{TO}V_2 + \pi R\sqrt{\frac{C_r}{L_1}}V_2^2\right) \tag{3.27b}$$

The final parameters that need to be defined are the inductor values, and they need to be selected in order to operate at the maximum switching frequency when maintaining high power transfer capabilities. The chosen values can be optimised to

minimise the conduction losses of the converter, in (3.27b), since all parameter are known apart from the two inductors. The optimisation problem is outlined below:

$$\min_x f(x) \mid g(x) = 0 \tag{3.28a}$$

$$Let\, H(x) = f(x) + \delta g(x) \tag{3.28b}$$

$$\frac{\partial}{\partial x}(H(x)) = \frac{\partial}{\partial x} f(x) + \frac{\partial}{\partial x}(\delta g(x)) = 0 \tag{3.28c}$$

$$\frac{\partial}{\partial \delta}(H(x)) = \frac{\partial}{\partial \delta}(\delta g(x)) = g(x) = 0 \tag{3.28d}$$

The value of $f(x)$ needs to minimised such that $g(x)$ is equal to zero (3.28a) and $\delta$ is a dummy variable used to simplify the calculations shown in (3.28b). For ADM operation of this converter, we want to minimise $P_{C_T}$ such that Equation (3.21) is true. To simplify the calculation the following substitutions are made:

$$\mathcal{L}_1 = \sqrt{L_1} \tag{3.29a}$$

$$\mathcal{L}_2 = \sqrt{L_2} \tag{3.29b}$$

The optimisation parameters are defined below, it should be noted that the additional terms, e.g. $4V_{TO}V_1$, in Equation (3.27b) are neglected in the optimisation as they are non-dependent on either $L_1$ or $L_2$.

$$f\left(\mathcal{L}_1, \mathcal{L}_2\right) = P_{C_T}\left(\mathcal{L}_1, \mathcal{L}_2\right) \equiv \frac{V_2^2}{\mathcal{L}_1} + \frac{V_1^2}{\mathcal{L}_2} \tag{3.30}$$

$$g\left(\mathcal{L}_1, \mathcal{L}_2\right) = f_{max} - \frac{1}{2\pi\sqrt{C_r}\left(\mathcal{L}_1 + \mathcal{L}_2\right)} = 0 \tag{3.31}$$

$$H(x) = f\left(\mathcal{L}_1, \mathcal{L}_2\right) + \delta g\left(\mathcal{L}_1, \mathcal{L}_2\right) \tag{3.32}$$

Partially differentiating $H(x)$ with respect to $\mathcal{L}_1$, $\mathcal{L}_2$, and $\delta$ gives:

$$\frac{\partial}{\partial \mathcal{L}_1}(H(x)) = -\frac{V_2^2}{\mathcal{L}_1^2} + \frac{1}{2\pi\sqrt{C_r}\,(\mathcal{L}_1 + \mathcal{L}_2)} = 0 \tag{3.33}$$

$$\frac{\partial}{\partial \mathcal{L}_2}(H(x)) = -\frac{V_1^2}{\mathcal{L}_2^2} + \frac{1}{2\pi\sqrt{C_r}\,(\mathcal{L}_1 + \mathcal{L}_2)} = 0 \tag{3.34}$$

$$\frac{\partial}{\partial \delta}(H(x)) = f_{max} - \frac{1}{2\pi\sqrt{C_r}\,(\mathcal{L}_1 + \mathcal{L}_2)} = 0 \tag{3.35}$$

By rearranging Equations (3.33) and (3.35) a value can be found for $\mathcal{L}_1$ and thus $\mathcal{L}_2$. From this values can be found for the two inductor values. Defined in (3.36) and (3.37).

$$L_1 = \left(\frac{V_2}{2\pi f_{max}\sqrt{C_r}\,(V_1 + V_2)}\right)^2 \tag{3.36}$$

$$L_2 = \left(\frac{V_1}{2\pi f_{max}\sqrt{C_r}\,(V_1 + V_2)}\right)^2 \tag{3.37}$$

From these inductor definitions, it can be seen that the inductor value is dependent on the voltage conversion ratio of the converter. If the voltage conversion ratio were very high, such that $V_1 \ll V_2$ the value of $L_2$ would be very small. This would then result in a high resonant frequency which may be too high to ensure the thyristors turn off. This implies that for higher conversion ratios a trade-off may be required between switching frequency and conduction losses to ensure the converter operates in ADM.

Another observation from these inductor values is that when substituted in to the equations for peak current, (3.14) and (3.15), is that both current peaks are equal, as defined in (3.38).

$$\hat{I}_1 = \hat{I}_2 = 2\pi f_{max} C_r \left(V_1 + V_2\right) \tag{3.38}$$

### 3.4.1. ADM Simulations

This mode of operation was analysed using three different simulation scenarios and for each scenario two thyristor devices were used to highlight the relationship between power and maximum cycle frequency. A fast thyristor and a phase control thyristor were investigated, their information can be seen in Table 3.5. The advantage of the fast thyristor is that the higher frequency allows for optimisation of the volume of the passive elements. This may be significant if the application is in an offshore environment. The phase control thyristor has significantly higher current and voltage ratings meaning fewer devices in the valve compared to the fast thyristor but it operates at a lower switching frequency.

| **Thyristor Device** | **Fast** | **Phase Control** |
|---|---|---|
| ***Datasheet*** | 5STF 11F3010 | 5STP 42U6500 |
| ***Optimum frequency*** | 5 kHz | 500 Hz |
| ***Maximum voltage*** | 3 kV | 6.5 kV |
| ***Current*** | 1.1 kA | 4.2 kA |
| ***Rated voltage*** | 1.5 kV | 3.5 kV |

**Table 3.5.:** Thyristor data

The parameters for three simulation cases are given in Table 3.6. Case A is a high voltage conversion ratio scenario where a low voltage DC network, such as a photovoltaic array, is connected to a HVDC network. For this case the value for the inductor, $L_2$, was chosen to be larger than the previous optimisation suggested as the voltage conversion ratio was too high. The original optimised value of $L_2$ resulted in the resonant period being too short to allow the converter current to

fall below the thyristor holding current and the thyristor remained on. The second scenario looks at a medium voltage conversion ratio, that could be used to connect a DC collector network to a HVDC grid. The final scenario looks at a low voltage conversion ratio, where two HVDC networks can be connected. From Table 3.5 it can be seen that the phase control thyristor can approximately carry four times as much current as the fast thyristor. Paralleling of the thyristor devices was not considered and so the comparison results in a difference of a factor of four in the power for each case.

| **Scenario** | **Parameter** | **Unit** | **Fast Thyristor Case** | **Phase Control Thyristor Case** |
|---|---|---|---|---|
| A ± 2.5 kV ± 150 kV | Power | MW | 5 | 20 |
| | $L_1$ | mH | 2.7 | 6.9 |
| | $L_2$ | mH | 0.65 | 1.6 |
| | $C_r$ | $\mu$F | 0.14 | 6.7 |
| | $N_{valve}$ | | 204 | 88 |
| B ± 25 kV ± 150 kV | Power | MW | 50 | 240 |
| | $L_1$ | mH | 1.71 | 9.3 |
| | $L_2$ | mH | 0.19 | 0.26 |
| | $C_r$ | $\mu$F | 0.33 | 8.0 |
| | $N_{valve}$ | | 134 | 100 |
| C ± 150 kV ± 250 kV | Power | MW | 300 | 1200 |
| | $L_1$ | mH | 4.0 | 9.9 |
| | $L_2$ | mH | 1.4 | 3.6 |
| | $C_r$ | $\mu$F | 0.1 | 4.0 |
| | $N_{valve}$ | | 534 | 229 |

**Table 3.6.:** Simulation scenarios parameters

The converter was simulated with the firing sequence set by a fixed clock in MATLAB Simulink. The results from the three cases are given in Table 3.7. These results show that the phase control thyristor can transfer more power per cycle than the fast thyristor. It can also be seen, that as the voltage conversion ratio decreases, the power losses reduce. This reiterates the point that this converter topology is best suited to low to medium voltage conversion ratios.

| Case | | Fast Thyristor | Phase Control Thyristor | Unit |
|---|---|---|---|---|
| **A** | $P$ | 1 | 40 | kW/Hz |
| | $P_{C_T}$ | 0.22 | 3.45 | kW/Hz |
| | $\frac{P_{C_T}}{P}$ | 21.8 | 8.6 | % |
| **B** | $P_{C_T}$ | 10 | 480 | kW/Hz |
| | $P$ | 0.18 | 5.29 | kW/Hz |
| | $\frac{P_{C_T}}{P}$ | 1.80 | 1.1 | % |
| **C** | $P$ | 600 | 24000 | kW/Hz |
| | $P_{C_T}$ | 0.91 | 14.77 | kW/Hz |
| | $\frac{P_{C_T}}{P}$ | 1.5 | 0.6 | % |

**Table 3.7.:** Power transfer and conduction loss results

In Figure 3.15 the linear relationship between the switching frequency, power transfer capability, and conduction losses of the converter for Case C are shown. At 500 Hz the converter starts operating in CCM. This implies increased losses in the converter, however only conduction losses were considered as CCM operation was beyond the scope of the study.

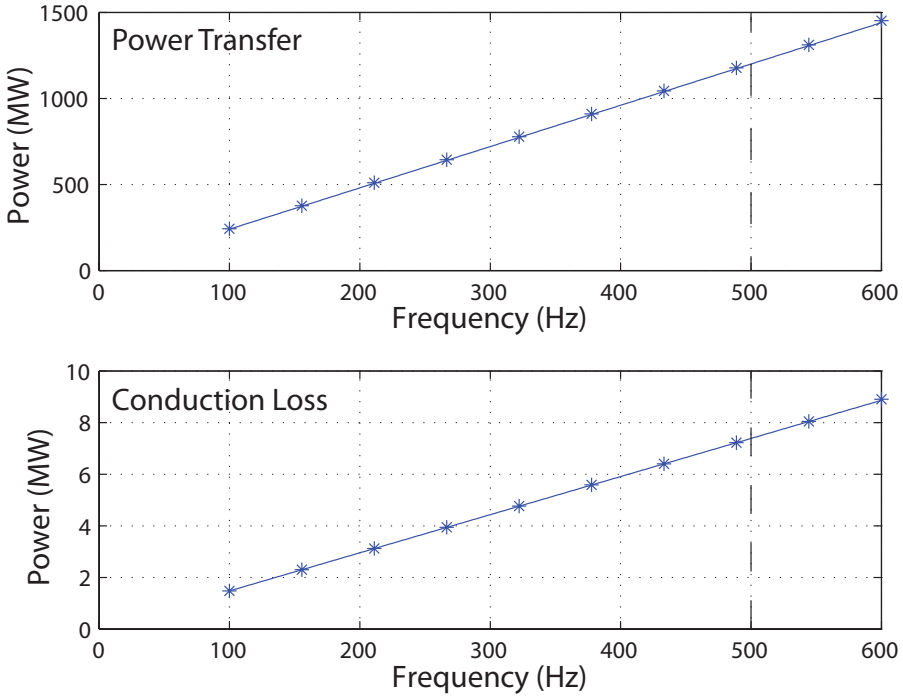



**Figure 3.15.:** Relationship between power transfer and conduction loss with switching frequency for Case C

Figure 3.16 shows the capacitor voltage and the unfiltered currents. It can be seen that the peak currents, $\hat{I}_1$ and $\hat{I}_2$, have their peak at the same magnitude and the peak capacitor voltage is the sum of the two DC bus voltages (300 + 500 = 800 kV). The dead time during the operation is also seen in capacitor voltage waveform. It is during this dead time that the intermediary capacitor stores the energy to be transferred through the converter. Additionally the four voltage points outlined earlier can be clearly seen.

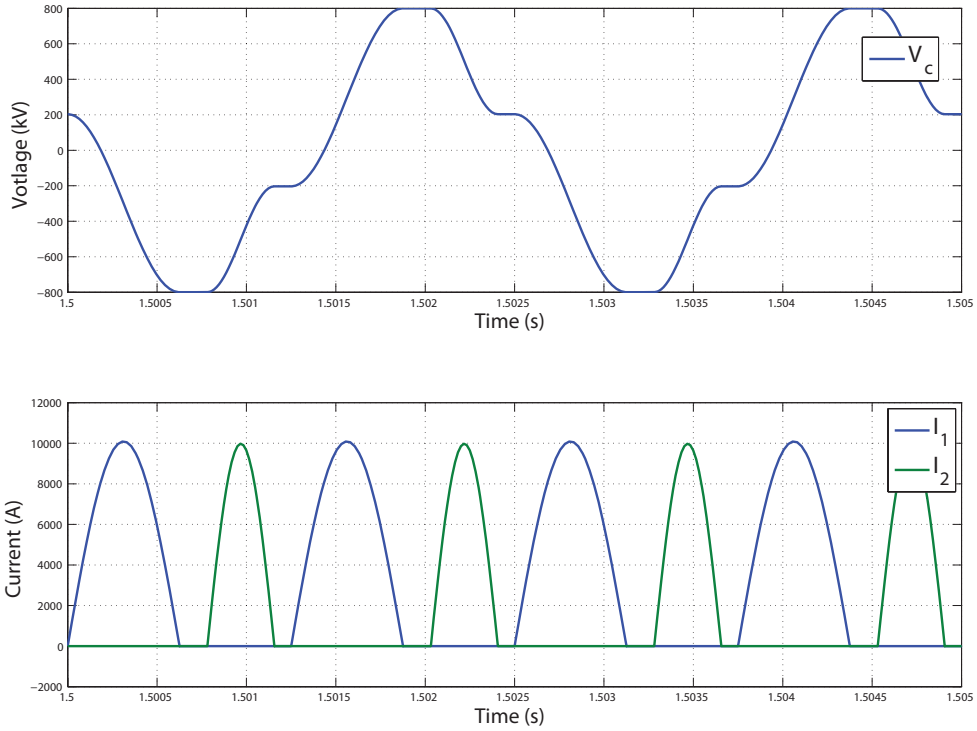



**Figure 3.16.:** Voltage and current waveforms for Case C

These results confirm that the converter topology could be used for interfacing two HVDC systems when operated in ADM. However, for medium voltage applications there are significant conduction losses and a transformer-based topology may be better suited. Additionally the phase control thyristor exhibited improved loss figures and fewer devices in the valve compared to the fast thyristor.

## 3.5. Comparison of DC/DC Converters

In order to evaluate the DC/DC converters described in this chapter, a common scenario was used to compare them. The parameters are given in Table 3.8. These voltage magnitudes were chosen as the lower voltage represents the dominant system voltage that has been used in recent years for offshore wind developments and the higher voltage corresponds to the ABB announcement of the development of higher voltages levels for XLPE cables [111].

| Parameter | Value |
|---|---|
| Conversion ratio | 1.5625 |
| Low voltage (kV) | ± 320 |
| High voltage (kV) | ± 500 |
| SM voltage (kV) | 2 |
| Power (MW) | 900 |
| Redundancy (%) | 10 |

**Table 3.8.:** Comparison parameters

Two scenarios are presented for the front-to-front converter, a non-fault blocking case where two HB MMCs are used and a fault-blocking case where a fault blocking converter is used on the low voltage side as in [95]. The latter uses a FB MMC on the lower DC voltage bridge. The converters are numbered as follows:

1. Front-to-front converter (no DC fault blocking)
2. Front-to-front converter (DC fault blocking)
3. HVDC auto transformer
4. Modular multilevel DC/DC
5. LCL converter
6. Resonant converter (ADM operation)

Note that the non-DC fault blocking converter is included to illustrate the difference in requirements between a fault blocking and non-fault blocking converter. For all converters the highest rated devices were used. For the IGBT based converters a 4.5 kV device was chosen and operated at 2 kV nominal voltage, and for the thyristor based converter device a 8 kV device was chosen and operated at 4.5 kV nominal voltage. A summary of the results is shown in Table 3.9, full details can be found in Appendix B.

| **Converter** | **Device** | **Devices** | **Capacitors** | **Inductors** | **Filter** |
|---|---|---|---|---|---|
| ***1*** | IGBT | 10,824 | 5,412 | 9 | No |
| ***2*** | IGBT | 15,048 | 5,412 | 9 | No |
| ***3*** | IGBT | 8,264 | 3,300 | 24 | No |
| ***4*** | IGBT | 2,992 | 1,100 | 10 | Yes |
| ***5*** | IGBT | 3,608 | 2 | 4 | Yes |
| ***6*** | Thyristor | 1,968 | 2 | 4 | Yes |

**Table 3.9.:** Comparison results

Table 3.10 shows the energy stored in the capacitors of the different converters for the same case. It should be noted that for the resonant converters, 5 and 6, that the energy is transferred through the converter and the capacitor voltage varies over time. The value for the capacitor for the LCL DC/DC converter, which uses IGBTS, was found using the set of equations from [101] and the workings are detailed in Appendix B. The other converter capacitors hold a constant DC voltage and constantly store energy in the converter.

| Converter | Capacitor Value (mF) | | Energy Storage (kJ/MVA) |
|---|---|---|---|
| **1** | HV | LV | 39 |
| | 5.8 | 9.1 | |
| **2** | HV | LV | 39 |
| | 5.8 | 9.1 | |
| **3** | 2.6 | | 19 |
| **4** | 11.5 | | 28 |
| | **Capacitor Value ($\mu$F)** | | **Energy Transferred (kJ/MVA)** |
| **5** | 0.13 | | 900 |
| **6** | 1.41 | | 3600 |

**Table 3.10.:** Capacitor energy storage comparison

It can be seen from these results that the HVDC-DC auto transformer stores the least energy and has the smallest capacitor value of the modular based topologies. Table 3.11 outlines key advantages and disadvantages for each converter.

| DC/DC Converter | Advantages | Disadvantages |
|---|---|---|
| ***Front-to-front*** | Technology ready | Large volume |
| | DC fault blocking | High power losses |
| | Little filtering | |
| ***Auto transformer*** | DC fault blocking | Low technology readiness |
| | Low power losses | |
| | Small volume | |
| ***MMC DC/DC*** | DC fault blocking | Large filter inductors |
| | Small volume | High power losses |
| | | Low technology readiness |
| ***LCL*** | Low number of devices | Significant filtering |
| | DC fault blocking | Series switching of IGBTs |
| | | High power losses |
| ***Resonant*** | Mature thyristor technology | Significant filtering |
| | Low power losses | Low device utilisation |
| | DC fault blocking | Difficult to design for $L_2$ |
| | | Large volume |

**Table 3.11.:** DC/DC converter comparison

It can be seen that a frontrunner for use in applications for interconnecting HVDC networks is the HVDC auto transformer. This is because of the single stage conversion, the arrangement of the arms of the converter, and the use of transformer to

balance the energy in the stacks leading to a small volume and to efficient operation. This topology also does not require large filters to remove the AC components from the DC current, which reduces the space requirement of the converter and lowers the overall power losses of the design. Additionally the converter provides DC fault blocking and thus could ensure that a DC fault does not propagate through the converter.

## 3.6. Summary

Several DC/DC converters suitable for use in low to medium voltage conversion ratio applications, such as HVDC system interconnection, were reviewed. Four topologies were reviewed and a fifth topology was studied in detail. The mode of operation of each topology was detailed and the circuit diagram provided.

A resonant family of DC/DC converters using thyristor valves were examined in detail. The bidirectional converter was modelled in MATLAB Simulink to observe how the converter operated for a medium voltage conversion ratio. The conduction losses for the converter were estimated and compared with the literature. This revealed that the losses for this family of converters increase as voltage conversion ratio increases. This showed that this topology is suitable for interconnecting HVDC systems and has the additional capability of DC fault blocking for most but not all scenarios.

An alternative mode of operation was developed for this resonant converter with the aim of blocking DC faults for all scenarios. It was termed Alternate Discontinuous Mode (ADM). It ensures that the two bridges of the converter are never connected at the same instant, and that the intermediary capacitor holds all the energy for a short period before transferring it to the output bridge. This mode of operation was investigated for three simulation scenarios and two thyristor types. It was seen that phase control thyristor, with higher voltage and current ratings, had the lowest losses for all scenarios. This study also confirmed that the topology is best suited to applications with low voltage conversion ratio, as this results in the lowest losses.

Finally all the DC/DC converters were compared for a specific scenario. The converters were compared on device count, number of passive devices, and capacitor energy storage. The advantages and disadvantages of each converter were presented

and a possible solution for interconnection of HVDC systems was the HVDC auto transformer. This design does not require significant filtering and arrangement of the converter allows for efficient operation, while providing DC fault blocking capability.

# 4. Average Models of AC/DC Converters

## 4.1. Background

The objective for the work described in this chapter was the development of converter simulation models which can be used to efficiently simulate MTDC systems. Simulating detailed switching models of converters is very time consuming, taking tens of minutes, or even hours to acquire only a few seconds of data [112]. Creating large DC systems including several converters using these models is impractical and alternative representations of the converters are required [112]. For example, a full-scale HB MMC with a DC bus voltage of ± 320 kV would require 3,840 IGBTs[1] and simulating all these devices and their switching instances is computationally intensive. Other modular converters may require even more switching elements, such as the FB MMC.

Reduced order models of converters can be used to enable time efficient system simulations which maintain reasonable accuracy of the converter dynamics. Also, as MTDC networks are likely to be multi-vendor and use varying converter technologies, having a library of computationally efficient converter models can aid understanding of larger networks and provide insight into how different converters interact

[1] Assuming 2 kV SM voltage

with each other.

Different types of MMC models are listed and described in detail by a Cigré working group B4-57 [113]. Different models can be used to carry out different studies, and there is a trade-off between converter detail and the simulation time. Table 4.1 gives a summary of the converter model definitions.

| Model Type | Model Description |
|---|---|
| 1 | Full physics model |
| 2 | Full detailed model |
| 3 | Simplified switchable resistance |
| 4 | Detailed equivalent model |
| 5 | Average value model (AVM) |
| 6 | Simplified AVM |
| 7 | RMS load-flow |

**Table 4.1.:** Summary of simulation models for simulating MMCs

Model types 1, 2, and 3 are very detailed, computationally intensive and generally used for internal converter studies. Model 1 is a full physics model where the semiconductor devices are represented by differential equations, these models would typically be created in circuit simulation software packages [113]. The full detailed model, type 2, represents the IGBTs as an ideal switch with two non-ideal diodes as depicted in Figure 4.1b. Full detailed models can be used for accurate loss calculations, and for investigating abnormal operation of the SMs.

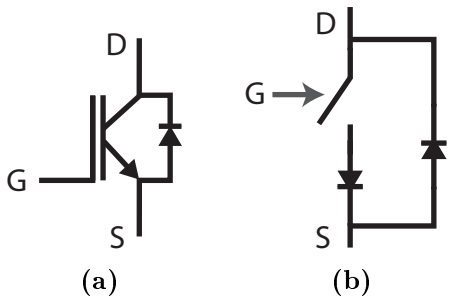



**Figure 4.1.:** Type 2 IGBT representation

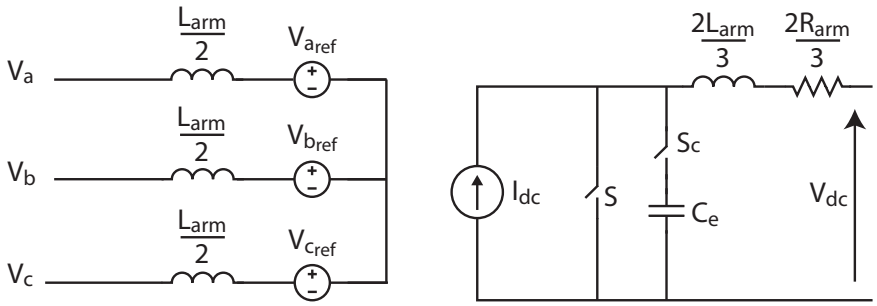
The type 3 model reduces the complexity of the switching device by modelling the IGBTs as switchable resistances with two values, a low resistance for when the IGBT is on, and a high resistance when it is off. This model can simulate quicker than the type 2 model, but every device in the converter is still modelled. Model types 1, 2, and 3 can be used to verify simplified models.

The type 4 model reduces the complexity of the converter by using a Thevinin equivalent to represent each SM and thus each SM capacitor voltage is still observable. Type 5 uses controllable voltage and current sources to represent the converter and does not provide individual SM voltages. This model assumes the SM capacitor voltages in each arm are balanced. Type 6 models also use controllable current and voltage sources but do not include any of the switching harmonics, and can be used for large system simulations. Finally type 7 represents only steady-state converter outputs and theses models are used for load-flow studies where the high frequency transients are not modelled.

The research presented here will focus mainly on model types 3 and 5. All the converter models are developed using the SimPowerSystems library in MATLAB Simulink® and power electronic devices are represented as switchable resistances depending on the gate command of that specific device. Thus any switching model developed in MATLAB is a type 3 model and can be used to verify reduced order models. The type 5 converter model, termed an Average Value Models (AVM), was chosen as the reduced model to develop, as the SM capacitor voltages are required for system level studies. Model types 6 and 7 are not considered as they do not retain enough detail to produce the internal converter waveforms such as the arm voltage and current.

### 4.1.1. Average Value Models of the MMC

In general, AVMs use controllable voltage and current sources to represent the active elements of the converter, one such model is described in [112]. The AC-side and DC-side of the converter are represented separately and thus the arm voltage and current waveforms are not modelled. Figure 4.2 shows the AC and DC side representation of the converter from [114].




**(a)** AC side **(b)** DC side

**Figure 4.2.:** AVM representation of MMC

The AC side is represented by three controllable voltage sources, one for each phase, and an equivalent arm inductance for each phase. These voltage sources are provided with voltage references from a current vector control strategy which transforms the real and reactive power references into voltage commands for the converter [115]. The DC side is represented by a controllable current source in parallel with an equivalent capacitance. The current source represents the DC current from the converter. The DC losses of the converter are accounted for, approximately, by the equivalent arm inductance and resistance at the output of the DC terminal. The equivalent capacitance represents the energy that is stored in the converter and the capacitor value is expressed in (4.1).

$$C_E = \frac{6C_{SM}}{N_{arm}} \tag{4.1}$$

Additional switches can be added to the DC side of the AVM to enable representation of the MMC waveforms during a DC-side fault. During a DC-side fault, all the IGBTs are opened leaving the anti-parallel diodes to conduct current, thus the converter acts at an uncontrolled diode rectifier bridge. Typically the SMs are fitted with a thyristor across the input terminals to protect the SM in the event of a DC-side fault. The thyristor is used as it is able to withstand the high surge currents during faults [112]. As only the equivalent phases of the converter are represented the blocked state of the converter cannot be modelled. During a DC-side fault, the equivalent capacitance is disconnected using switch $S_c$ and the current source is short-circuited by switch S [114].

This AVM was compared to the other MMC model types in [114] and it is seen that this AVM closely matches the other model types for steady state operation and a three-phase AC fault, however the model does not correctly characterise a DC side fault. For the first millisecond after the DC fault, this AVM accurately represents the characteristics of the DC fault. However, after 1 ms, the accuracy deteriorates as the blocked state of the MMC is not adequately modelled. It is noted that this AVM is best suited for transient AC system studies and for designing high level DC network controllers [113].

#### Continuous AVM of the MMC

An alternative modelling approach is described in [116, 117], where each arm of the MMC is represented by a controllable voltage source in series with an arm inductor and a resistor. The inclusion of the series resistance models the average conduction losses that result from the semiconductor devices. The AC and DC

sides are connected in this model. The model is termed continuous because of the smooth output waveforms. It has been assumed that the switching frequency high relative to the frequency of the AC output waveforms of the converter [116]. The model is derived by obtaining a state-space model of the converter and using the switching sequence of the SMs to provide a voltage reference for each arm. This reference is then used as the input to a controllable voltage source. The continuous AVM was compared to a discrete switching model of the MMC and it was shown that the waveforms of the continuous model closely matched the discrete switching model but the staircase waveform associated with the MMC was not provided by the continuous model as ideal sinusoidal references were given to the voltage sources [116].

The continuous model was also compared to an experimental setup and was observed to match closely, and represented the low order harmonic spectrum accurately. However, high frequency harmonics were not described as the the model ignores out the switching patterns of the SM. In order to represent the converter accurately during the blocked state, additional circuitry is added to the arm, and is shown in Figure 4.3. The switch is closed during normal operation and the switch is opened in scenarios when the converter needs to be blocked, such as start-up and DC fault scenarios. The parallel bypass diode allows the fault current to flow through the converter during the blocked operation.

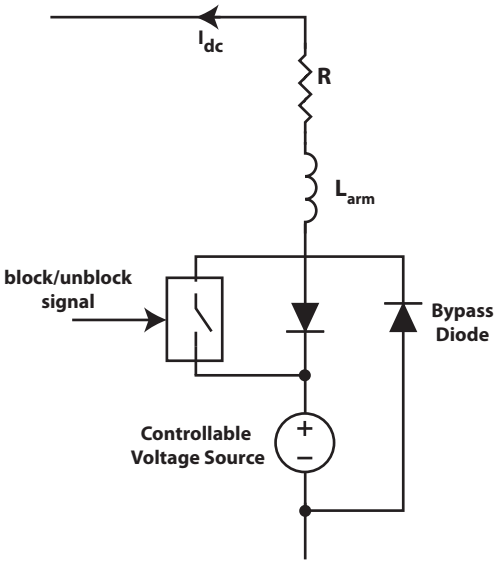



**Figure 4.3.:** Continuous model MMC arm representation

This method of modelling the MMC reduces the complexity while maintaining the internal converter waveforms such as the arm current and voltage. The main difference with the continuous model and the AVM discussed at the beginning of this section, is that it can provide the internal converter waveforms.

## 4.2. Chosen AVM Methodology

The model developed here is based on the literature for the continuous model described in the previous section, where the AC and DC sides are not represented separately and the arm current and arm voltage waveforms are generated. The model developed here falls under the type 5 model described by Cigré in [113], and will be referred to as an AVM. The focus was mainly on reducing the computation time that is related to the switching devices of the simulation models, by representing the stack of SMs by a controllable voltage source. The models developed here will also include quantization of the converter waveforms, to show the stair-

case waveform, and control feedback regarding the amount of energy available from the stack. The controller lessens in complexity naturally as the low-level control, which is responsible for producing the firing commands for the individual SMs, is no longer required. However, the controller was not further optimised here as it is the switching devices which significantly affect the computation time.

As the converters act as voltage sources, it is logical to then represent each stack of SMs as a controllable voltage source. The arm also has associated conduction losses due to the on-state voltage of the IGBTs and diodes and can be approximately modelled as a lumped resistance. The value of the series resistance is the number of SMs times the equivalent resistance of an individual IGBT, because there is always an IGBT or diode in the conduction path regardless of the switching state of the SM. Figure 4.4 shows the representation for a single arm of a HB MMC used in this research.

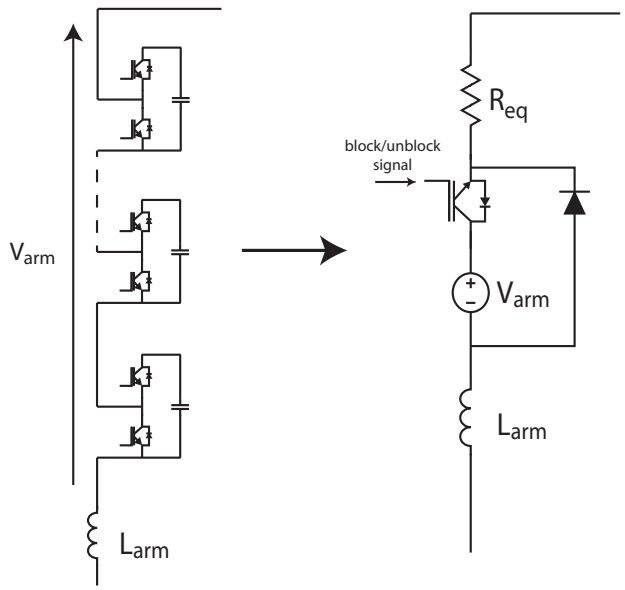



**Figure 4.4.:** HB MMC AVM arm representation

There is additional circuitry in the AVM arm representation which is used to

improve the response of the AVM in the event of DC side faults. Each arm of the converter can simply be replaced by this representation. The low level control, which is responsible for providing the SMs with firing commands can be removed as it is no longer required in the AVM. The input to the low level control is the arm voltage reference which can be given directly to the controllable voltage source. It is assumed for the AVM that a good SM rotation algorithm is in place. In the detailed model the SM rotation ensures that the individual SM voltages are balanced and do not drift from their nominal voltage.

It is important to monitor and balance the energy within the arms of this style of VSC [83]. In the Full Switching Model (FSM) (model type 3 from Table 4.1), each SM capacitor voltage is directly represented and used to evaluate the energy stored in the stack of SMs. The energy deviation is calculated simply using (2.7), derived in Chapter 2. In an AVM, the individual SMs are not explicitly modelled, thus the arm energy deviation can be found by taking the integral of the power generated by the arm using the arm voltage and current, shown in (4.2b), where $V_{arm}$ is the arm voltage, $I_{arm}$ is the arm current, and $R_{eq}$ is the equivalent series resistance of the arm.

$$P_{arm} = V_{arm}(t)I_{arm}(t) + P_{loss} \tag{4.2a}$$

$$P_{arm} = V_{arm}(t)I_{arm}(t) + R_{eq}I_{arm}^2(t) \tag{4.2b}$$

The $P_{loss}$ term accounts, approximately, for the conduction losses in the arm of the converter. Equation (4.3b) shows the expression for determining the energy

deviation for an AVM.

$$\Delta E_{AVM} = \int P_{arm} dt \tag{4.3a}$$

$$\triangle E_{AVM} = \int \left( V_{arm}(t) I_{arm}(t) + R_{eq} I_{arm}^2(t) \right) dt \tag{4.3b}$$

### 4.2.1. Voltage Limitation of the Voltage Sources

From Figure 4.4 it can be seen that the capacitor is not directly represented in the AVM arm representation. In other AVM methodologies the DC-side dynamics are represented separately by using an equivalent lumped capacitor, $C_{SM}/N_{SM}$, for each arm connected in parallel with a current source [114]. The current source value is the arm current multiplied by the switching function, which dictates how many SMs are inserted. This method requires additional components to be added the AVM arm representation. Alternatively, the energy in the arm can be used to determine an average SM voltage which can then be used to add the capacitor dynamics.

The arm voltage that is available from a stack of an MMC is limited by the sum of the voltages in the SM capacitors, and is thus linked to the energy stored in the stack of SM capacitors. In order to represent the DC dynamics of the stack of capacitors the voltage command for the controllable voltage source must be constrained. This then reflects the energy stored in the arm and the available voltage from the stack at any instant. The DC dynamics in the models developed in this research make use of the internal arm current and voltage waveforms to estimate the energy deviation in the arm. This energy deviation, calculated in (4.3b), can be used to determine the average SM voltage of the converter arm using the full expression given in (4.4).

$$V_{SM_{AVG}} = \sqrt{V_{SM_{NOM}}^2 - \left( 2 \frac{\Delta E_{AVM}}{N_{SM} C_{SM}} \right)} \tag{4.4}$$

Knowing the average SM voltage, a limit can be placed on the control command for the converter stack. This ensures the voltage generated does not exceed the maximum available voltage. The block diagram in Figure 4.5 shows how this limit is applied to the arm voltage reference.

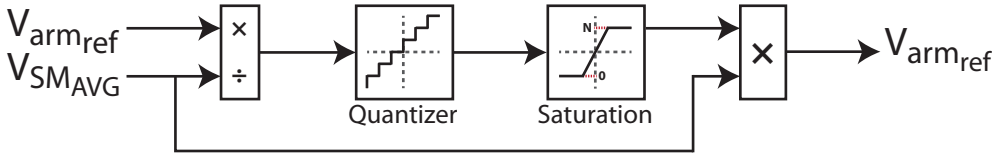



**Figure 4.5.:** Block diagram of voltage limit control

The original arm voltage reference is divided by the average SM capacitor voltage to give the number of SMs required. This signal is then quantized, which rounds the number of SMs required to an integer. A limit is applied to recognise that only $N$ SMs are available and limited to positive values since only the HB SMs are considered. The signal from the limit block is then multiplied by the average SM voltage to provide the final voltage command for the controllable voltage source. An additional feature of these control blocks is that the staircase waveform, associated with the MMC, is produced rather than an ideal AC waveform. By using method, additional electrical components are not required in the AVM. This model can be easily modified to represent the FB MMC topology by removing the diode and IGBT from the arm representation and changing the limit in the voltage limit controller to N to -N.

### 4.2.2. Modified AVM

A modified AVM (MAVM) paper was written in conjunction with Dr Tony Beddard, a visiting researcher at Imperial College from Manchester University. The MAVM

makes modifications to the previously described AVM in order to improve the accuracy and functionality of the AVM [118]. Some of the key modifications are the inclusion of the AC side arm resistance to account for the losses of the converter on the AC side. A blocking module (BM) can be added to the MAVM to improve its DC fault response. Different BMs are proposed and they greatly improve the accuracy of the MAVM, compared to the AVM, during DC faults. The BMs increase in complexity and the easiest BM to implement is a six-pulse diode bridge. The MAVM with a six-pulse diode bridge BM is shown in Figure 4.6.

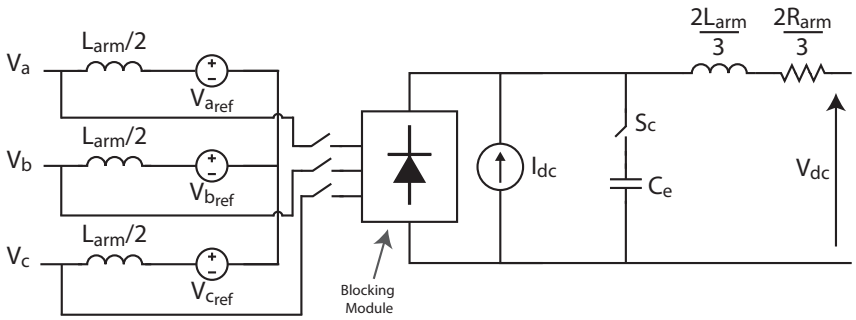



**Figure 4.6.:** AVM with six pulse diode rectifier BM

It can be seen from the diagram that the AC and DC sides can be connected. During normal operation, the MAVM is unaffected by the BM as the diode bridge is disconnected during normal operation. In the event of a DC fault the converter is blocked and the switches to the diode bridge close, and the diode bridge becomes forward biased leading to the AC system contributing to the DC fault current. This greatly improves the accuracy of the MAVM for a DC fault scenario and the results are given in [118]. At time of writing the paper was still under review.

## 4.3. Verification of the AVM

### 4.3.1. Converter Simulations

The first model to be developed was of the HB MMC. The model was developed in MATLAB Simulink® using the SimPowerSystems library. The AVM was verified by comparing it directly to a FSM and the parameters for both models are given in Table 4.2. The low voltage and power ratings were chosen to allow a direct comparison with a FSM that had a reasonable simulation duration, e.g. 10 minute computation time for 1 second of system operation.

| Parameter | Value |
|---|---|
| Power | 20 MW |
| DC voltage | ± 10 kV |
| Line-line converter AC voltage | 11 kV |
| AC frequency | 50 Hz |
| No. of SMs per arm | 14 |
| SM voltage | 1.5 kV |
| SM capacitor | 8.3 mF |
| Phase inductor | 1.9 mH |
| Arm inductor | 2 mH |
| Cable resistance | 11.3 mΩ/km |
| Cable inductance | 0.362 mH/km |
| Cable capacitance | 0.212 μF/km |

**Table 4.2.:** MMC model parameters

All simulations were carried out on an Windows 7 PC with an Intel Xeon 2.4 GHz and 12 GB memory. A simple block diagram of the simulation setup for both models is shown in Figure 4.7 and the parameters of the cable section are given in the table above. The cable parameters were taken from [119]. The cable was modelled using the distributed parameter line with lumped losses from the SimPowerSystems library in MATLAB.

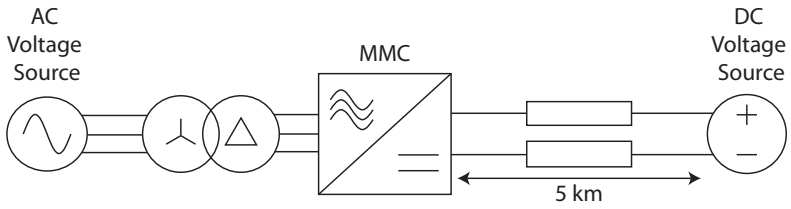



**Figure 4.7.:** MMC simulation block diagram

Figure 4.8 and Figure 4.9 show the DC and AC waveforms for both models. It can be seen from these waveforms of the AVM match closely to the FSM waveforms. The power is ramped to -20 MW in 0.1 s, and a power flow reversal to 20 MW occurs at 0.5 s. The DC voltage waveform shows the voltage drop due the cable resistance.

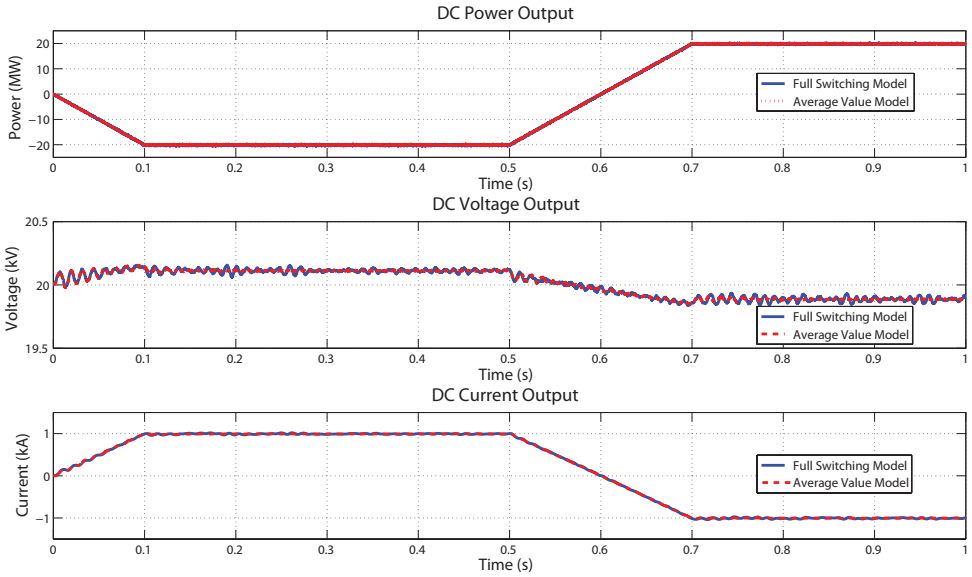
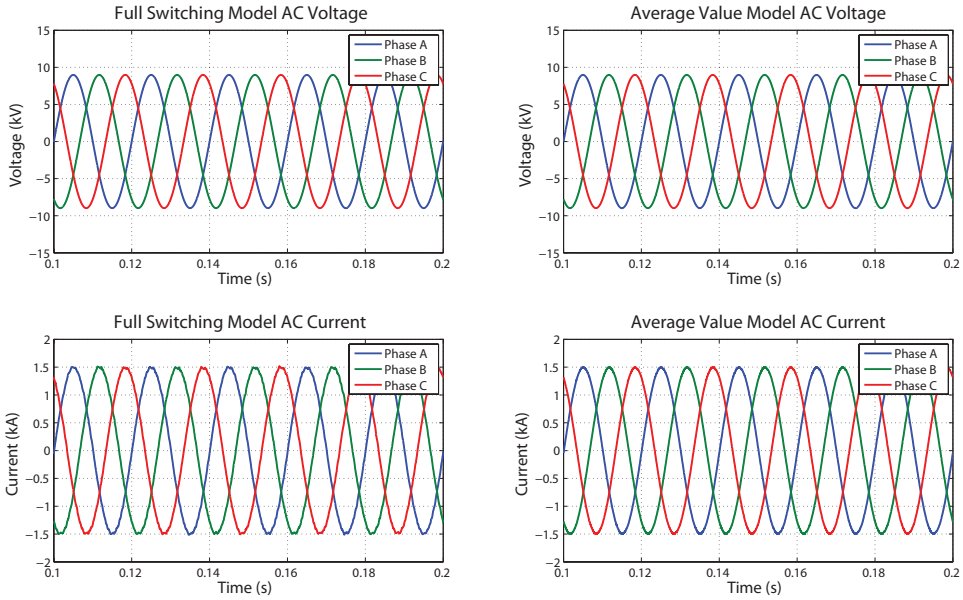



**Figure 4.8.:** DC waveforms for the HB MMC




**(a)** FSM wavforms **(b)** AVM wavforms

**Figure 4.9.:** AC waveforms for the HB MMC

The accuracy of the AVM was determined by finding the percentage difference between the AC and DC current and the DC voltage waveforms using (4.5). This allowed the accuracy of the AVM to be quantified. For the AC current a limit was placed on values considered where magnitudes outside 0.1 pu current were not used in the comparison. This prevented the occurrence of division by zero errors when the current is crossing the zero point. The difference was calculated over the entire simulation duration of 1 second worth of signal data. $X$ denotes the signal that is used.

$$Difference(\%) = \left( \left| \frac{X_{FSM} - X_{AVM}}{X_{FSM}} \right| \right) \times 100 \tag{4.5}$$

The AVM was simulated at different time-steps and the results were compared to the FSM simulated at a time-step of 1 µs for maximum accuracy. Figure 4.10 shows a plot of the percentage difference for the AC and DC currents for the two models.

It can be seen that for time-steps lower than 100 µs the AVM maintains reasonable accuracy. For time steps greater than 100 µs, the accuracy of the AVM deteriorates significantly, showing that the AVM is a good approximation of the FSM, simulated at 1 µs, for time steps lower than 100 µs.

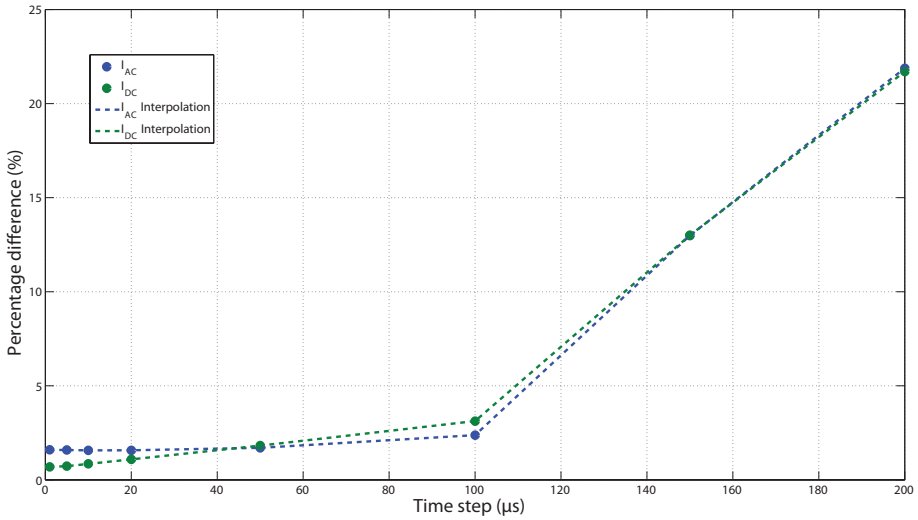



**Figure 4.10.:** Current percentage difference with time step

Figure 4.11 shows the percentage difference for the DC voltage. This figure shows that the accuracy diminishes below 100 µs and that the AVM is better suited to simulations at 50 µs. Further analysis is required to ascertain the cause of the change in accuracy.

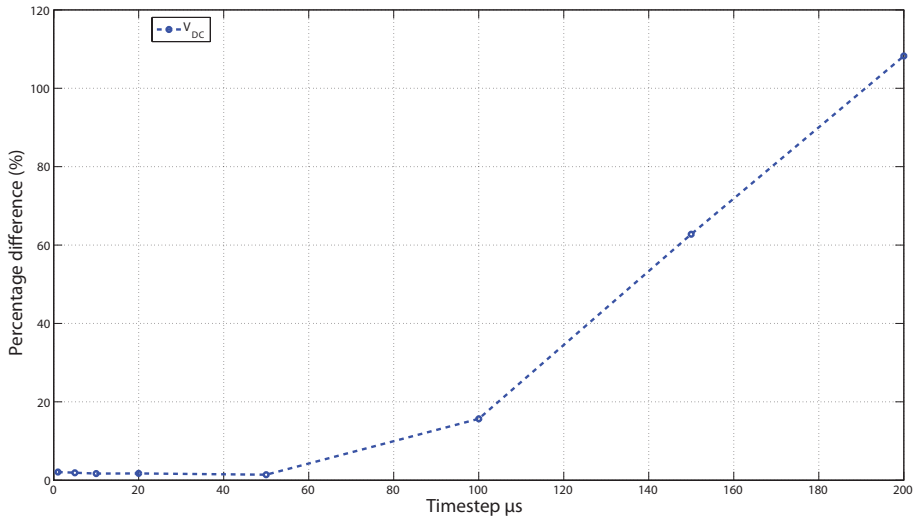



**Figure 4.11.:** DC voltage percentage difference

The next metric studied was the comparison in computation time between the AVM and FSM. Both models were simulated for the same duration at the same time step and the results can be seen in Figure 4.12. It should be noted that the comparison stopped at 50 µs as the FSM became unstable for time steps beyond this, whereas the AVM remained stable up to 200 µs which can be seen in Figure 4.10.

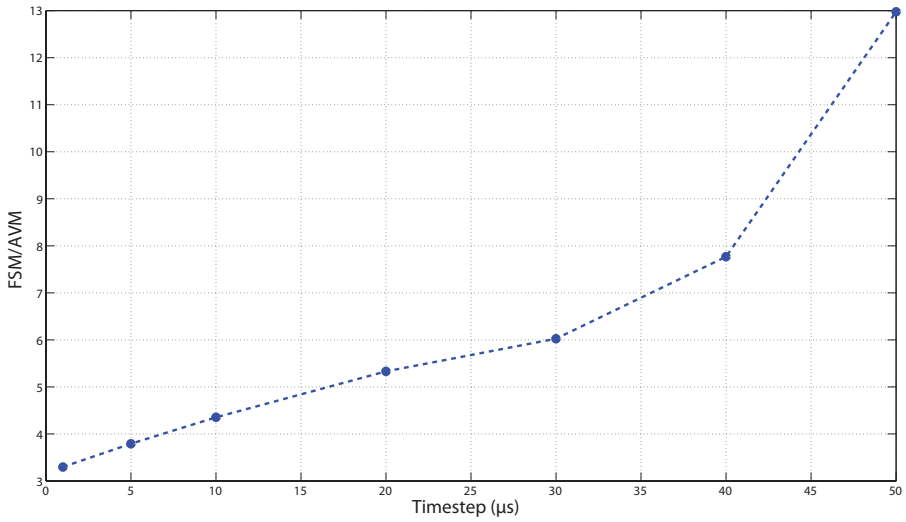



**Figure 4.12.:** Computation time versus time step

Figure 4.12 shows that increasing the time step improves the computation time, and as the time-step becomes larger the AVM simulates faster than the FSM. From this set of results it can be seen that the AVM can accurately model the MMC with good accuracy and with faster computation times than the FSM for different time steps up to 50 µs.

### 4.3.2. System Simulations

In order to validate the AVM of the MMC for abnormal operating conditions the converter was placed in a HVDC point-to-point link shown in Figure 4.13. The cable was modelled using a distributed parameter cable from the SimPowerSystems library and the parameters for the cable are provided in Table 4.3.

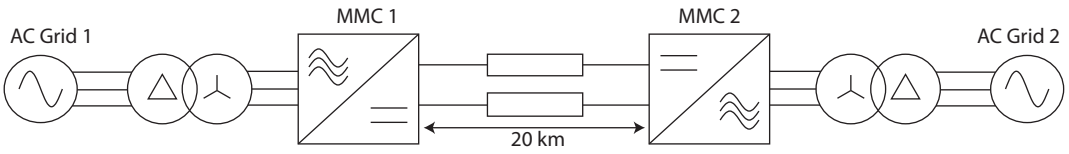



**Figure 4.13.:** Point-to-point HVDC link

| Parameter | Value | Unit |
|---|---|---|
| Resistance | 11.3 | mΩ/km |
| Capacitance | 0.212 | µF/km |
| Inductance | 0.362 | mH/km |
| Length | 20 | km |

**Table 4.3.:** Cable parameters

The MMC AVM was tested in normal operating conditions to verify that the models operated correctly. All of the system simulations were simulated at a time step of 1 µs. The DC cable voltage and the power from the two MMCs, for both the FSM and the AVM, is shown in Figure 4.14.

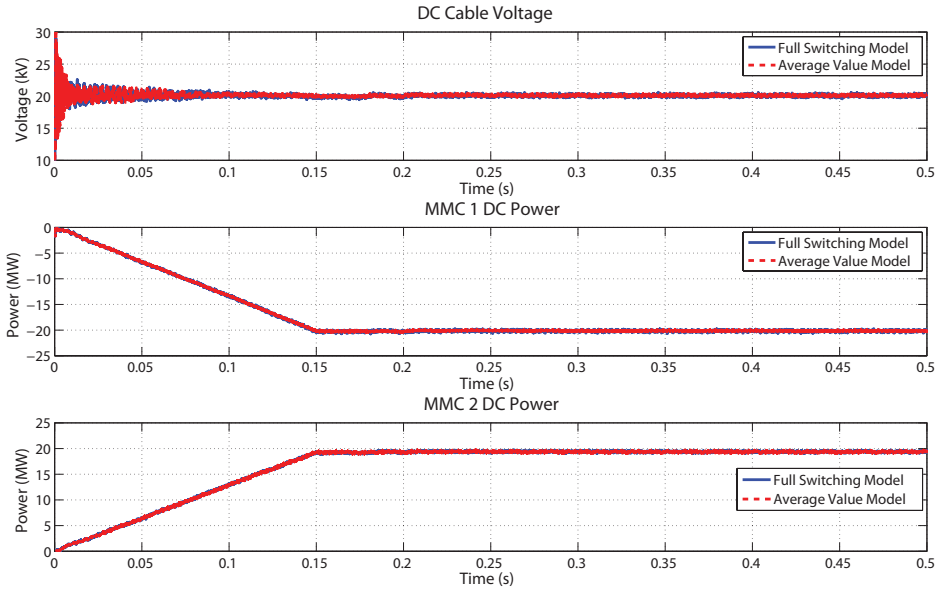



**Figure 4.14.:** MMC point-to-point normal operating conditions

The DC cable voltage was measured half way along the cable, and the DC power was measured as the terminals of the converter. It is seen from this figure that the results obtained from the two models match closely. The DC voltage shows cable ringing at the beginning of the simulation which is the result of voltage reflections in the cable, as the cable is not pre-charged.

A symmetrical three-phase fault was placed on MMC 1 at 0.25 s into the simulation for 100 ms. The symmetrical AC fault was applied by dropping the AC voltage of the programmable three-phase AC voltage source to 0.3 pu which can be seen in Figure 4.15. The fault was applied in this manner in order to control the magnitude of the AC voltage during the fault.

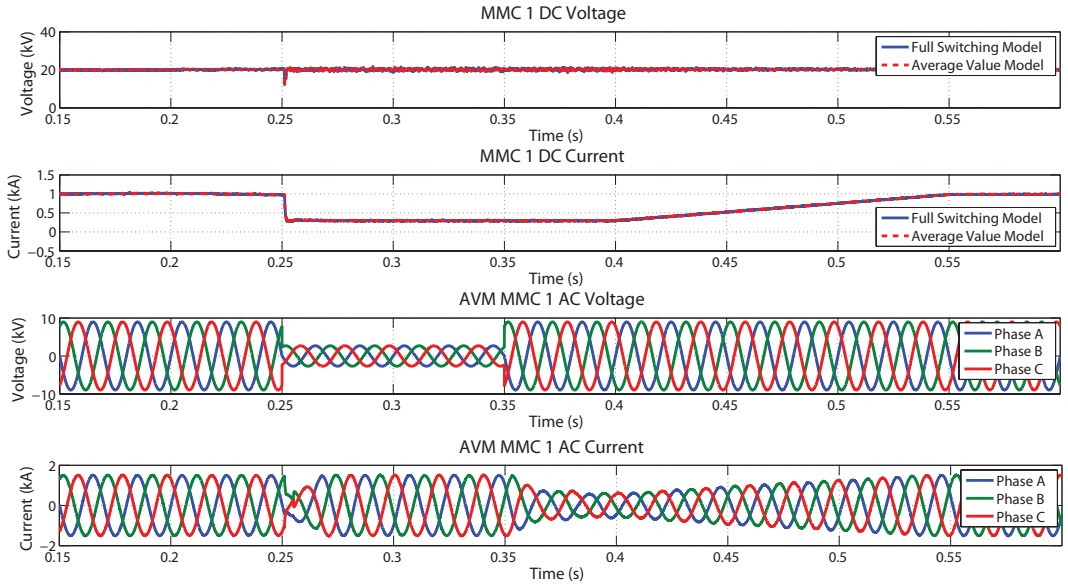
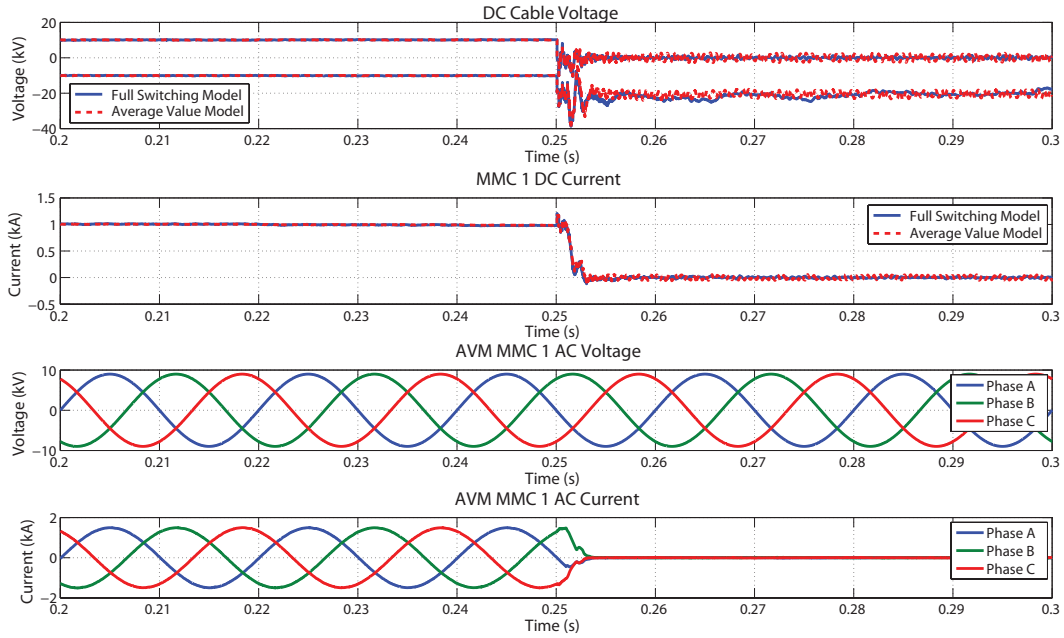


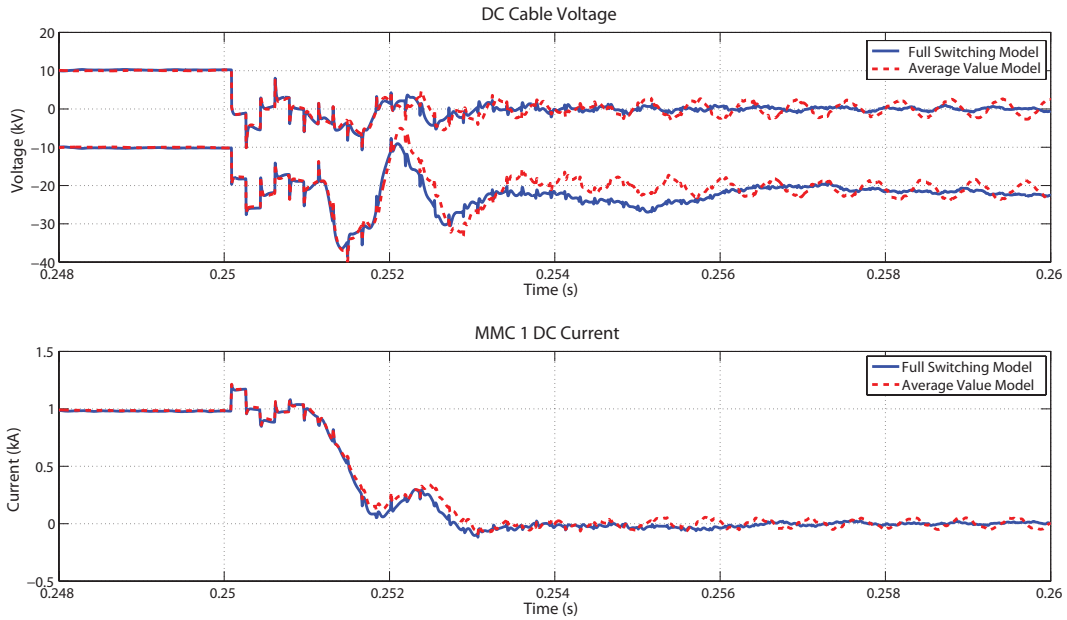

**Figure 4.15.:** Three-phase AC fault MMC response

For the AC fault, 0.3 pu power is transferred during the fault. The current is a 1 pu and the voltage is at 0.3 pu and thus the converter is providing 0.3 pu power. MMC 1 is also providing 6 MVA of reactive power from 0.255 s until the end of the simulation. The waveforms show that the MMC AVM closely matches the FSM and that the AVM is able to model AC-side faults. This figures also show that the MMC can provide support to the AC network during AC-side faults.

The next fault scenario considered was a permanent DC line-to-ground fault, placed half way along the cable at 10 km. The results are shown in Figure 4.16. The fault was applied at 0.25 s into simulation.




**(a)** DC line-to-ground fault waveforms




**(b)** Zoom of DC voltage and DC current response

**Figure 4.16.:** DC line to ground fault results

As the fault is a line-to-ground fault there is no large DC current but one pole voltage collapses and the other reaches 2 pu voltage, which is seen in the results. This comes from the point-to-point link not being solidly grounded and so the volt-

age shifts from ± 10 kV to 0 V to - 20 kV. The general response of both models represent the fault response well. For the first 2 ms the AVM closely follows the response of FSM, as shown in the close up in Figure 4.16b. After 2 ms the AVM shows oscillations on the DC voltage and current which are not present in the FSM waveforms. A similar response, where the accuracy deteriorated after a millisecond of a DC fault was shown for the AVM described in [114]. This DC fault simulation did not use any AC-side circuit breakers to disconnect the HVDC link, whereas in practice the AC circuit breakers would be used to clear the fault. It has been noted that the number of levels in the MMC can affect the DC-side response during transients for different model types [114]. In particular a lower number of levels in the MMC results in larger voltage deviations between the individual SMs in the stack. A FSM might show the additional oscillations due to the fluctuation of the SM capacitor voltages, whereas an AVM may not. When compared with other AVMs, additional oscillations were observed in [112] for DC line-to-line fault but the overall response of the AVM compared to the detailed model was correct.

| **Scenario** | **Computation Speed (FSM/AVM)** | $\mathbf{I_{AC}}$ (%) | $\mathbf{I_{DC}}$ (%) | $\mathbf{V_{DC}}$ (%) |
|---|---|---|---|---|
| Normal operation | 8.87 | 1.53 | 0.88 | 2.44 |
| AC three-phase fault | 8.12 | 2.32 | 2.32 | 2.75 |
| DC line-to-ground fault | 8.29 | 13.60 | 31.61 | 31.61 |
| DC line-to-ground fault with AC circuit breaker | | 2.16 | 22.18 | 22.18 |

**Table 4.4.:** Computation and accuracy comparison for system simulation

Table 4.4 shows the computation time and percentage difference between the AVM and FSM for AC and DC currents. When the AC side circuit breakers are opened the accuracy of the model improved. As once the breaker is opened the current in the network is zero and the oscillations observed in Figure 4.16b would no longer occur. It can be seen from this table that the AVM simulated faster than the FSM and

maintained reasonable accuracy for normal operation and AC fault case. However, for the DC fault scenario it can be seen that the accuracy diminished significantly, which is visible from Figure 4.16, but improved with the use of the AC breaker to clear the DC fault. It should be noted that the accuracy was calculated for the entire simulation time of 0.5 s. Thus, for the AC circuit breaker assisted DC fault case, the window length of the accuracy calculation could be altered to take into account that the opening of the AC breaker.

## 4.4. AVM of the Alternate Arm Converter

The same methodology, described in Section 4.2 , was used to develop an AVM of the AAC, described in Chapter 2. The main difference between the arm of the AAC and the MMC is the inclusion of director switches. The AAC AVM arm representation is shown in Figure 4.17.

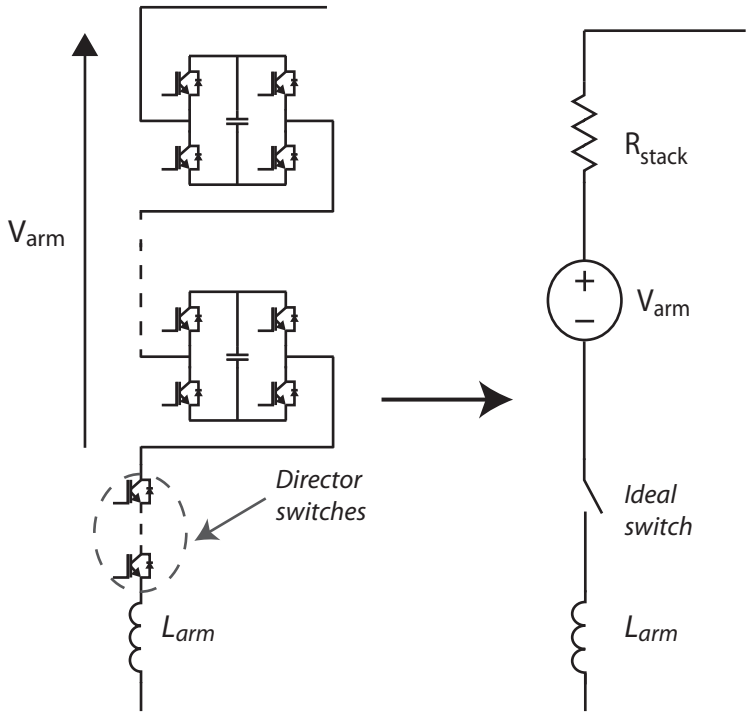



**Figure 4.17.:** Circuit diagram of the AVM of the AAC

The director switches are simply modelled using an ideal switch. Additional components are not necessary to improve the DC fault response of the AVM of the AAC, as the voltage source can now insert negative voltage. As with the MMC the energy balancing plays an important role in the control of the AAC, where the amount of voltage available from the arm is related to the energy stored in the stack of SMs. Thus the same voltage limiting block set was used to limit the voltage source command. The block diagram is shown for the AAC in Figure 4.18.

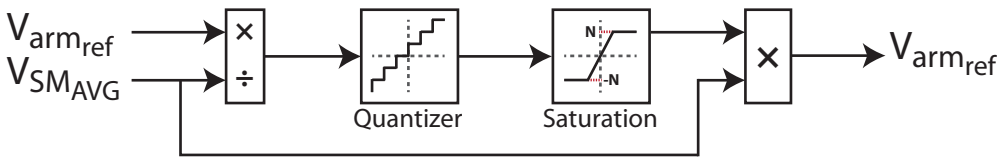



**Figure 4.18.:** Voltage control limit block diagram for the AAC

The key difference between this block set and the earlier one for the MMC, is that the SMs can insert a negative capacitor voltage as the AAC uses FB SMs and the limits after the quantizer are ± N.

### 4.4.1. Converter Simulations

An individual converter was simulated and directly compared with a FSM. The parameters of both models, FSM and AVM, are given in Table 4.5.

| Parameter | Value |
|---|---|
| Power | 20 MW |
| DC voltage | ± 10 kV |
| Line-line Grid AC voltage | 11 kV |
| Line-line Converter AC voltage | 16 kV |
| AC frequency | 50 Hz |
| No. of SMs per arm | 9 |
| No. of series IGBTs in director switch | 5 |
| SM voltage | 1.5 kV |
| SM capacitor | 4 mF |
| Phase inductor | 4.1 mH |
| Arm inductor | 100 μH |

**Table 4.5.:** AAC model parameters

Once again a scaled down model was studied to allow a direct comparison to the FSM. The converter models were simulated in a similar setup to Figure 4.7. Figure 4.19 shows the DC converter waveforms for start-up, power ramp-up, and power flow reversal.

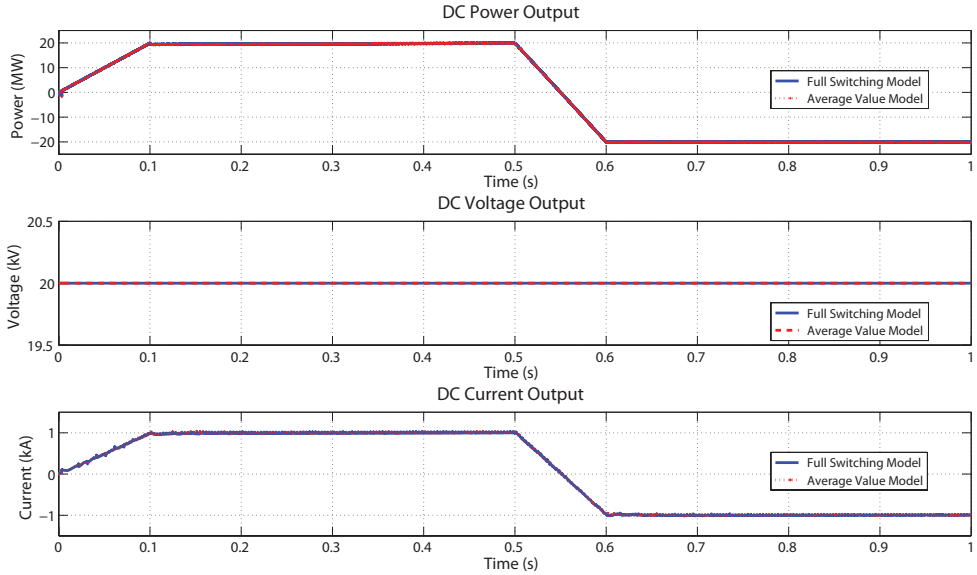



**Figure 4.19.:** AAC DC converter waveforms

In Figure 4.20, several cycles of the AC voltage are shown and it can be seen that

the waveforms match closely.

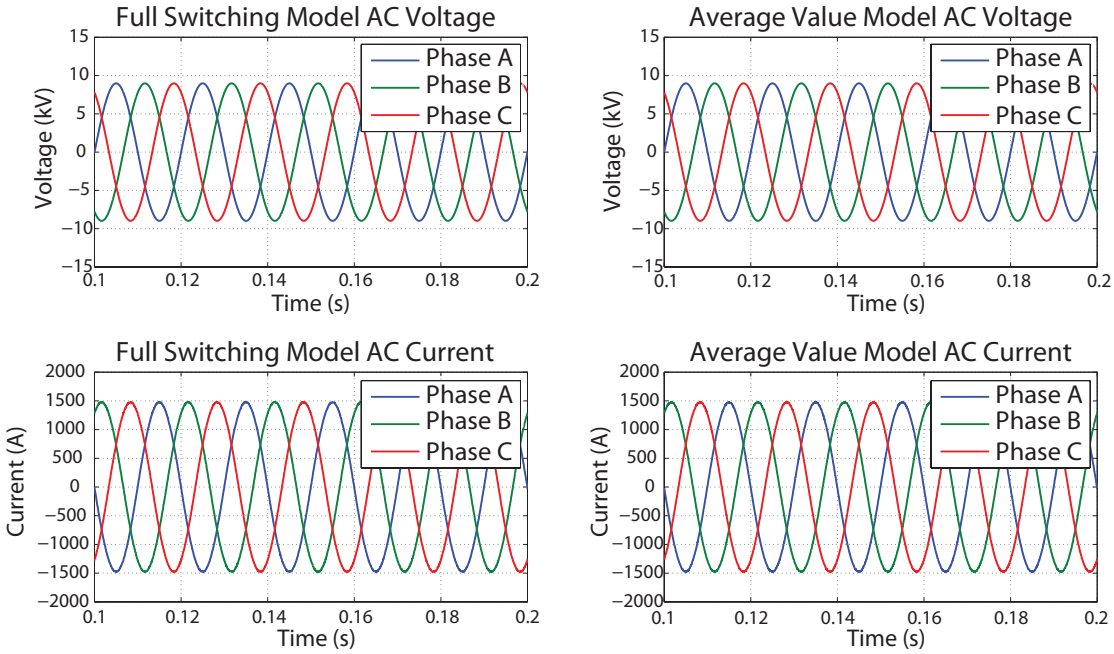



**Figure 4.20.:** AAC AC converter waveforms

The energy deviation for the two models is shown in Figure 4.21, for a simulation time step of 1 µs. It can be seen that for slow transients that the AVM closely matches the FSM.

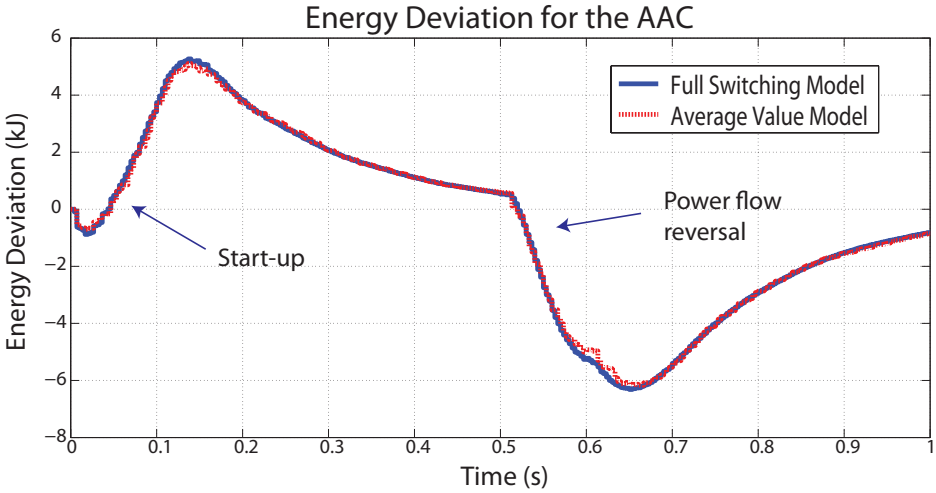



**Figure 4.21.:** AAC energy deviation waveform

The accuracy was determined for the AC current and DC voltage and current

using equation (4.5), and the same condition was applied to the AC current, as in Section 4.3.1., was used in the comparison to avoid division by zero errors in the calculation. Figure 4.22 shows the results of a comparison of the AVM AAC at several time step sizes compared with the FSM simulated at 1 μs time-step.

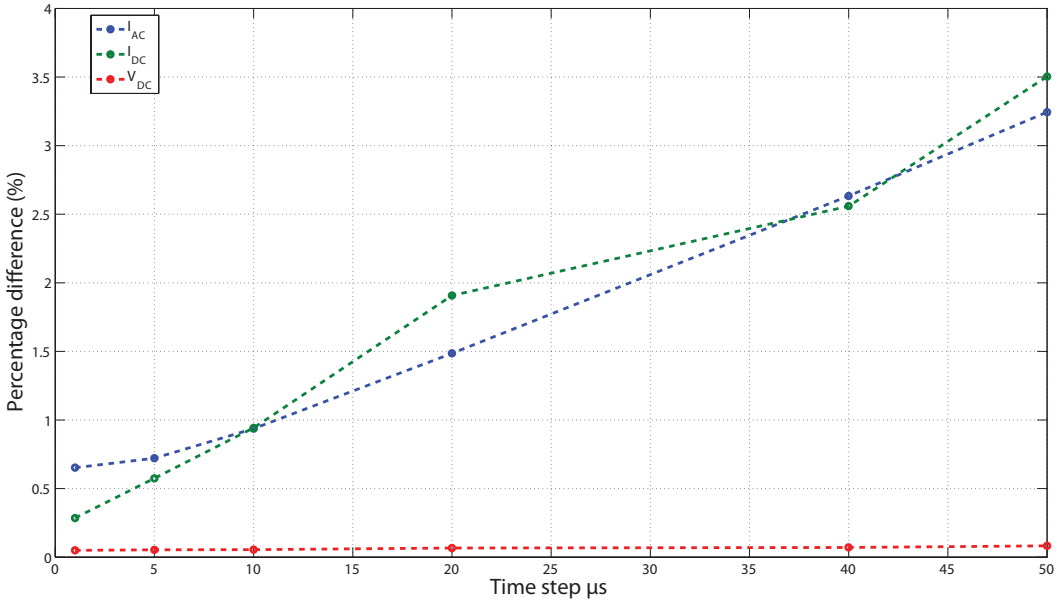



**Figure 4.22.:** AAC current percentage difference plot

Figure 4.22 shows that the AVM maintains reasonable accuracy up to a 50 μs and that an approximately linear relationship can be seen between time-step and accuracy. The figure also shows that the accuracy for the DC voltage is high for each time-step simulated. The AVM was not tested for higher time steps because of the need to represent the overlap period of the AAC. At higher time steps the current controller has too few time points to control the DC circulating current during the overlap.

The next metric to be studied was the time saving obtained from the AVM. This comparison was done for several different time steps for 1 s of data, using the same

computer as outlined in Section 4.3.1.. Figure 4.23 illustrates the data obtained.

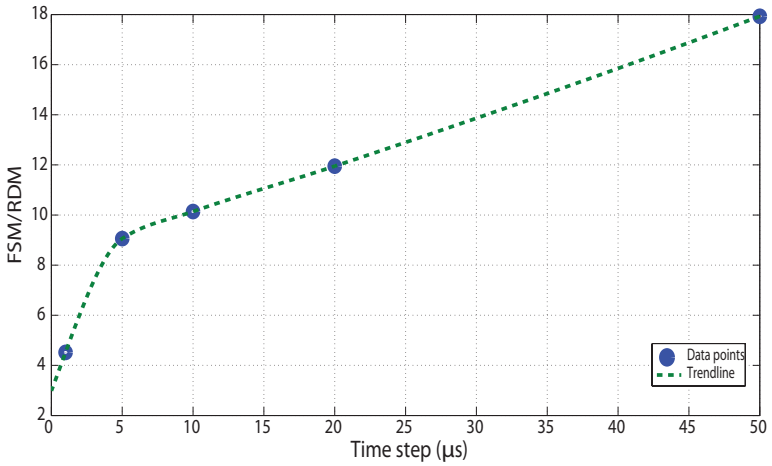



**Figure 4.23.:** AAC computation speed gain versus time step

The figure shows a step in computation time difference followed by a linear relationship from 5 µs onwards. This is a good computation time improvement and the converter results show that the AVM of the AAC is a good representation of the converter.

### 4.4.2. System Simulations

In order to test the AVM for abnormal operating conditions the AVM was placed in the same point-to-point HVDC link used to validate the HB MMC AVM, as in Section 4.3.2. All the system simulations had a time step of 1µs. The models were first verified for normal operating conditions the results of which are shown in Figure 4.24. The DC cable voltage waveform clearly shows the six-pulse ripple associated with the AAC.

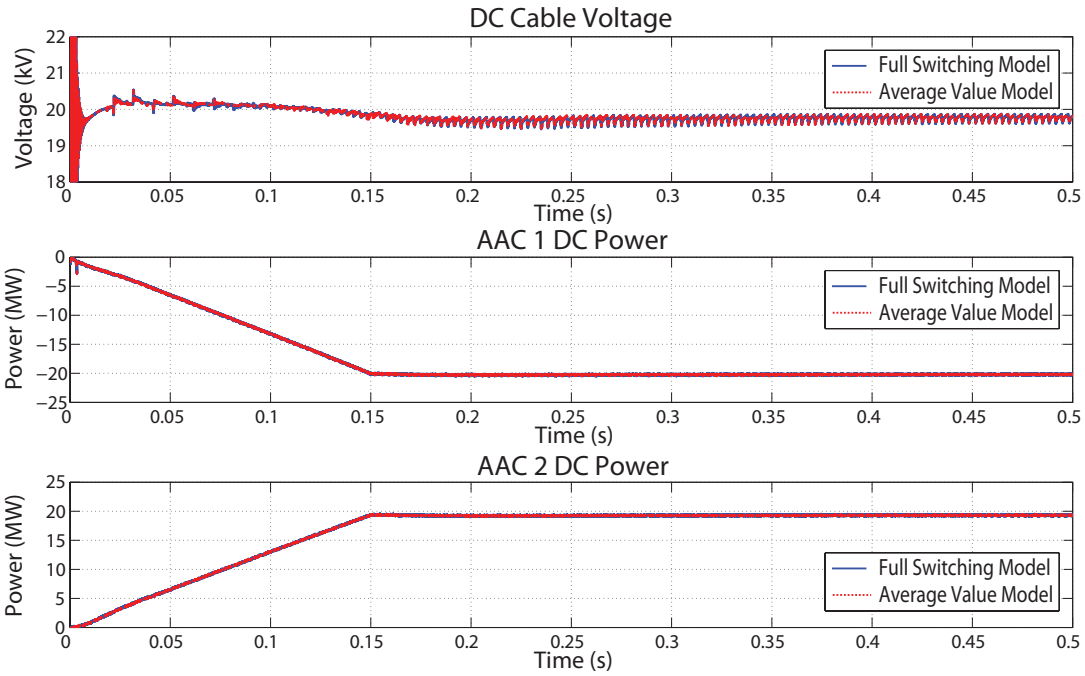



**Figure 4.24.:** Voltage and power waveforms for normal operating conditions

Three fault scenarios were tested in the point-to-point link: two faults were applied on AC grid 1 and one on the DC line. All faults were applied at 0.25 seconds and lasted for 100 ms. The AC faults were simulated by reducing the voltage of the AC source to 0.3 pu voltage for on all three phases for the symmetrical three-phase fault and the voltage was reduced on phase A for the single-phase fault. The first AC fault tested was a symmetrical three-phase fault and the results are shown in Figure 4.25. For this fault the power is reduced to 0 pu power during the fault at 0.251 seconds, accounting for time to fault detection, and the power reference returns to 1 pu at 0.4 s.

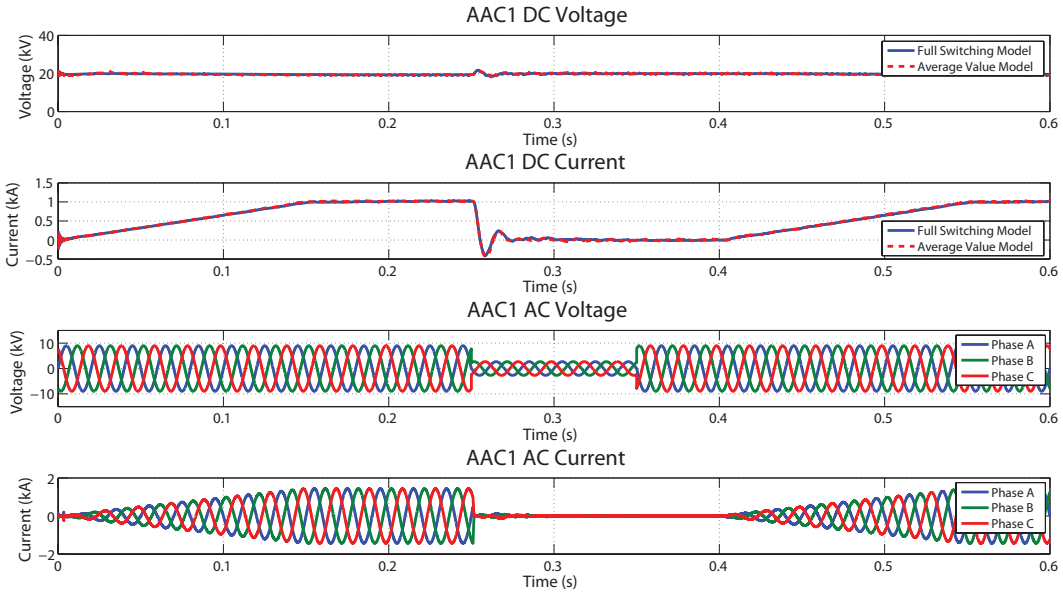



**Figure 4.25.:** Three-phase AC fault

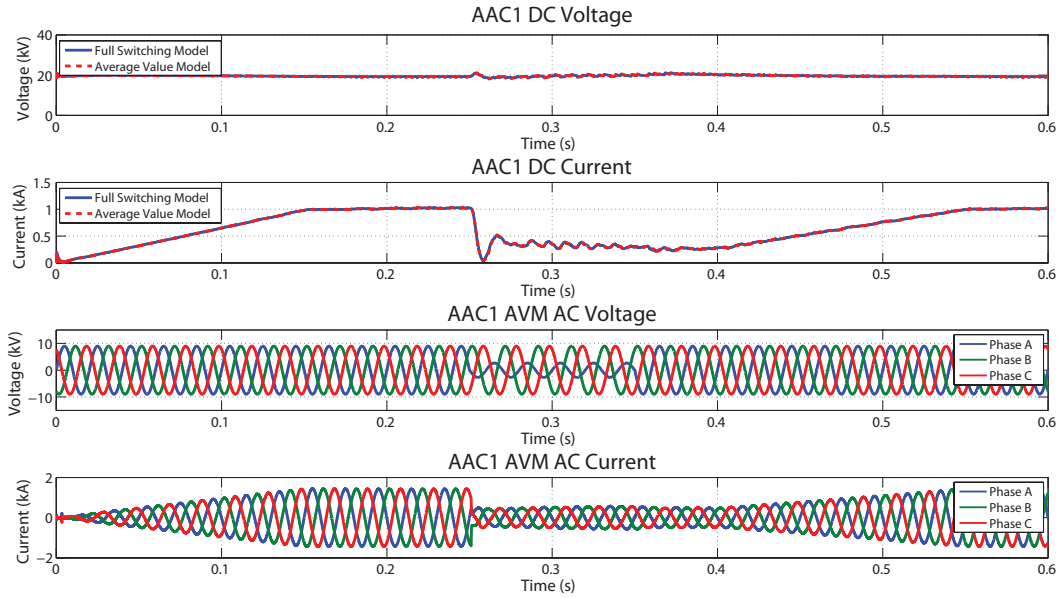



**Figure 4.26.:** Single-phase-to-ground AC fault

The single-phase AC fault supplies 0.3 pu power to the AC network during the fault. It can be seen that both AC fault scenarios match quite closely. The DC current shows oscillations which are caused by the sudden change in power reference in both the FSM and the AVM.

A DC line-to-ground fault was placed halfway along the DC link, at 10 km, the power reference was reduced to zero after 1 ms, to account for a detection algorithm, and like the AC fault tests the power ramps back to 1 pu at 0.4s. It should be noted that this power restoration time at 0.4 s may not be representative of real life systems and was used to show that the converter can continue operating after fault events. The results are shown in Figure 4.27. The STATCOM operation of the AAC is also demonstrated in the AC current plot of Figure 4.27, where a reactive power set point of of 1.7 MVAr was supplied to the AC grid.

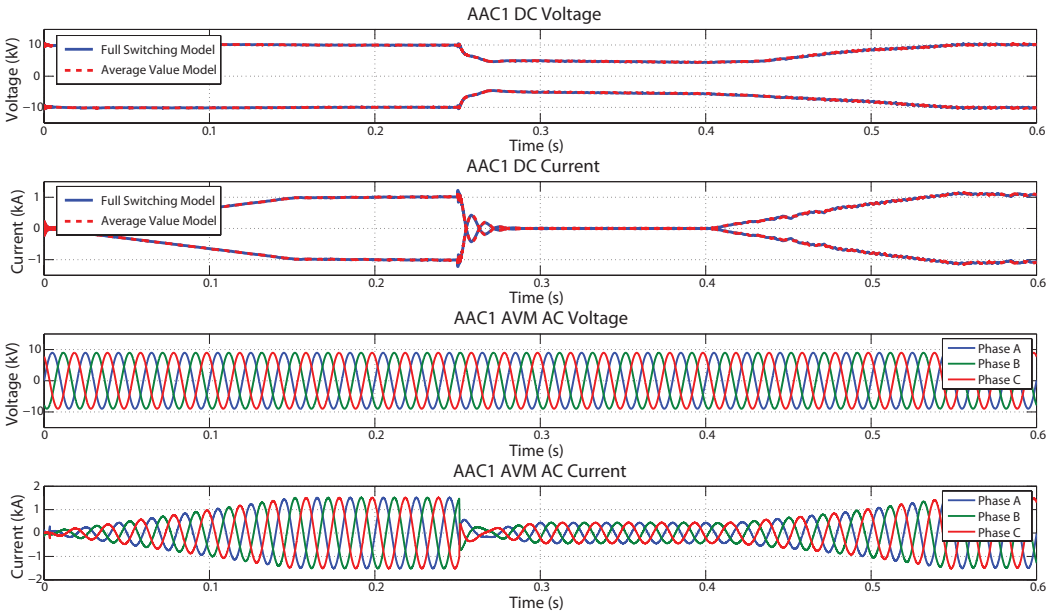



**Figure 4.27.:** DC line to ground fault

Table 4.6 shows the data for the computation time improvement and current percentage difference for the four scenarios simulated. For this point-to-point link, it was observed that the AVM system simulated over six times faster than the FSM system, which illustrates the usefulness of the reduced models in carrying out time efficient simulations of larger systems while maintaining high accuracy of the external converter waveforms. This table shows that the AVM that has been developed provides a faster computation without a significant compromise on the accuracy of

the external converter waveforms.

| Scenario | Computation Speed FSM/AVM | $I_{AC}$(%) | $I_{DC}$(%) | $V_{DC}$ (%) |
|---|---|---|---|---|
| Normal operation | 6.69 | 0.61 | 0.13 | 0.07 |
| Three-phase AC fault | 7.66 | 2.71 | 2.78 | 3.13 |
| Phase-to-ground fault | 7.44 | 1.07 | 0.96 | 0.21 |
| DC line to ground fault | 7.63 | 1.71 | 1.86 | 0.51 |

**Table 4.6.:** Accuracy and computation time difference data

## 4.5. Hardware Verification of the AAC AVM

### 4.5.1. Lab Converter Description

An experimental multilevel converter was designed and built at Imperial College to be reconfigurable so that it can operate as an MMC or an AAC. It was used to further verify the AVM of the AAC. The converter is a 15 kVA, ± 750 V with 10 SMs per arm. The converter specifications are given in Table 4.7. The experimental setup is described in further detail in [88].

| Parameter | Value |
|---|---|
| Power | 15 kVA |
| DC voltage | ± 750 V |
| AC line voltage (RMS) | 1170 V |
| SM voltage | 110 V |
| No. of SMs | 10 |
| SM capacitor | 0.5 mF |
| Phase inductor | 24 mH |
| Arm inductor | 1.3 mH |
| DC inductor | 3.7 mH |
| DC capacitor | 210 μF |

**Table 4.7.:** Hardware converter specifications

### 4.5.2. Comparison of Results

Some preliminary comparison results are shown in Figure 4.28. The figure shows an active power transfer of 1 pu and a reactive power of 0.2 pu.

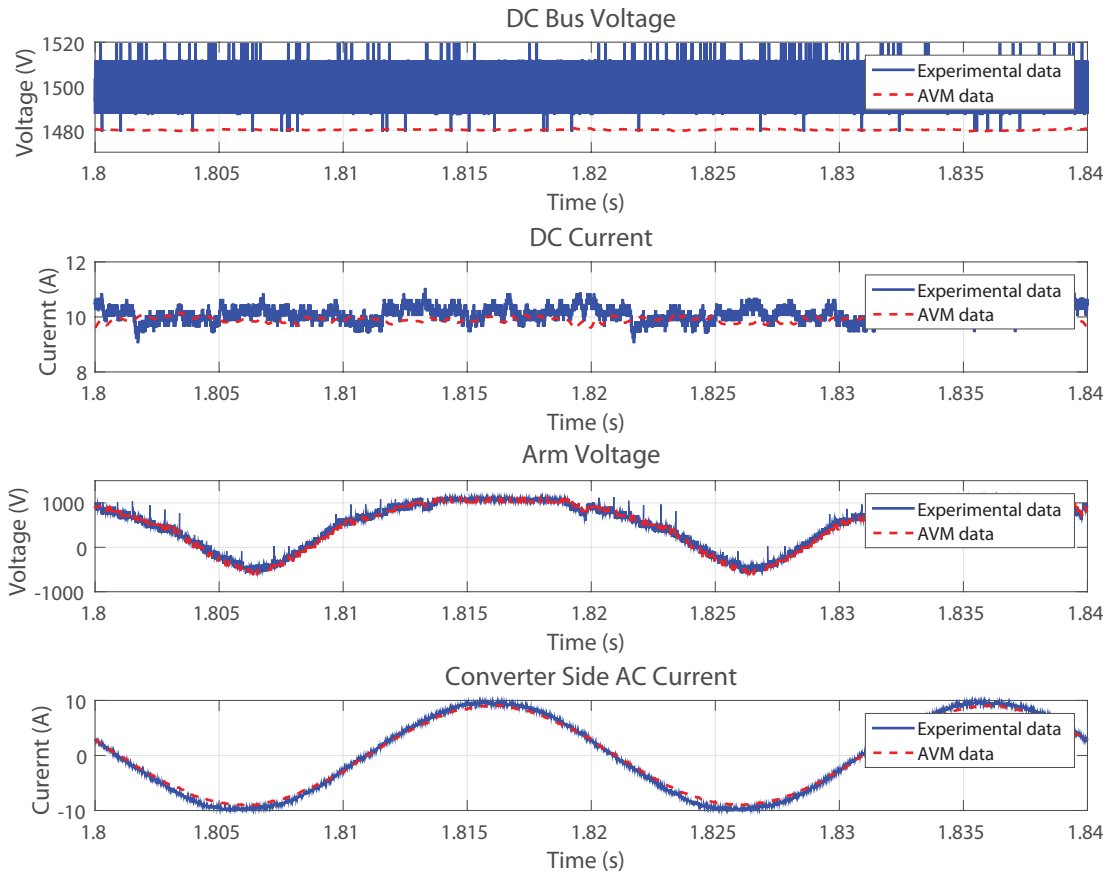



**Figure 4.28.:** Comparison of experimental and AVM data

These plots show that the AVM is a good representation of a real AAC. The experimental data has noise on the waveform which is picked up by the sensors used to measure the waveforms. It can be seen from the DC voltage plot that the AVM has a smoother waveform as the the model does not contain any switching elements. Additionally the experimental measurement shows the quantization from the oscilloscope. The AVM requires improvement to improve how accurately it can reproduce the experimental data. It will, in future work, be compared with several operating points and fault scenarios.

## 4.6. Summary

The case for using reduced dynamic models was provided, given that they can provide efficient computation times for large system studies while maintaining high accuracy of the external converter waveforms. The definition for several different types of converter model was provided. This research focused on the use of average value models. Two differing approaches, or methodologies, to develop AVMs of multilevel converters were presented. The first represents the AC and DC side of the converter separately, while the second uses a single representation for the converter. The AVM described allows for fast computation time, but the converter arm current and voltage waveforms are not observable. The second AVM approach represents each arm of the converter with a controllable voltage source, which allows the internal converter waveforms to be produced and then, potentially, utilised to improve the response of the converter.

The latter methodology was adopted for this research and was used to develop the AVM for an MMC. The focus was on reducing the complexity of the hardware computation of the converter model. The converter arm was represented by a controllable voltage source with a series resistance, to represent the losses in the arm, and an arm inductor. Additional components were added, a diode in parallel to the voltage source and a series IGBT/diode to improve the response of the AVM to DC faults. A voltage limit block was developed to ensure that the voltage command to the controllable voltage source does not exceed the available voltage in the stack of SMs. This was achieved by deriving the instantaneous energy in the arm from the arm current and voltage waveforms, and knowing the energy allows the available voltage from that arm to be determined.

An AVM for the HB MMC was compared directly to a FSM and was observed to run significantly faster. A reasonable accuracy was maintained for the several time

steps. The AVM was also tested for normal and abnormal operating conditions. The AVM maintained good accuracy of the converter for a symmetric AC-side fault. In the case of the DC-side fault, the AVM of the MMC was seen to match the FSM only for a couple of milliseconds after the DC fault after which a small oscillation developed.

An AVM for the AAC was also developed. The AVM was once again compared to the FSM and was observed to simulate significantly faster and maintained reasonable accuracy. The AVM was then tested for normal and abnormal operating conditions in a point-to-point link. The AVM matched closely for the three fault scenarios tested, two AC-side faults and a DC line-to-ground fault.

The AVM of the AAC was experimentally verified against a lab-scale converter. Preliminary results showed that the AVM matched closely with the experimental data. The AVM hardware verification is to be expanded to include fault scenarios.

# 5. Offshore MTDC Networks

## 5.1. Introduction

This chapter looks at two MTDC systems which are simulated using the AVMs presented in the previous chapter. The MTDC networks are based in the North Sea, and the case study wind development is the Dogger Bank development which is likely to be one of the largest wind farms in the world once completed. There are six zones available for development in the Dogger Bank zone each with a potenital capacity of 1.2 GW and they are shown in Figure 5.1.

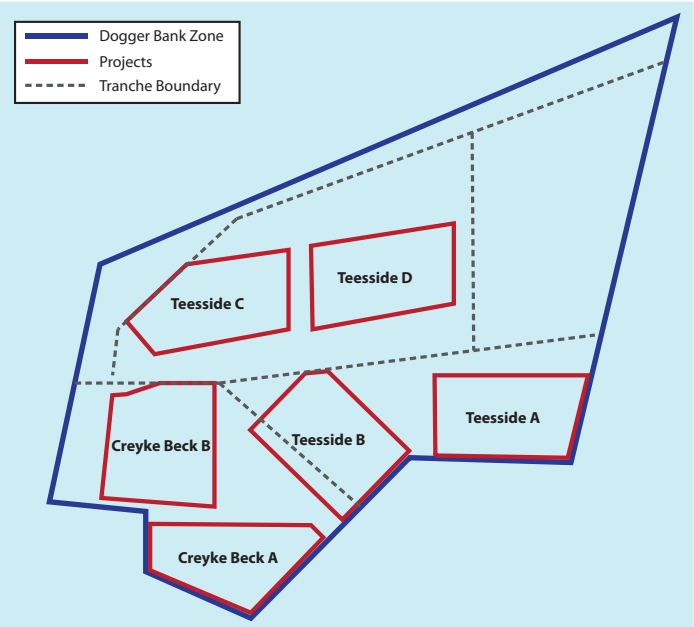



**Figure 5.1.:** Dogger Bank tranches adapted from [120]

At its closest, Dogger Bank is 125 km from shore and 250 km at its furthest, with a total area of 8660 $km^2$ [121]. The vast area of this development implies that there is likely to be HVDC converter platforms at significant distances from each other and that connection between them may require the use of DC. Using maps provided in [120], estimates of the distances between converter platforms were made and it was observed that a connection between Creyke Beck A and Teesside D, with 75 km between them, could be economically made using DC cables. Connecting these two wind farms through a DC link would create a four terminal MTDC network. Such a network is the first MTDC system studied in this chapter. The study investigates a protection method for the network and evaluates the case for the interconnection.

In addition to its large size, Dogger Bank is also positioned such that a link to Norway could start from the wind farm, this was proposed by National Grid in [122]. The development is also situated, at it closest point, approximately 200 km from the NSN link between Norway and the UK. An advantage of connecting with Norway is the potential use of the pumped hydro storage to store surplus renewable generation [123]. The NSN link is to be configured as a bipole VSC link and would have power transfer capability of 1400 MW [124]. The second MTDC study builds on the earlier four terminal study and links it with the NSN bipole link through a DC/DC converter.

## 5.2. Four Terminal Network Study

A simple four terminal network is illustrated in Figure 5.2. The network has a total maximum infeed power of 2.4 GW (1.2 GW per wind farm).

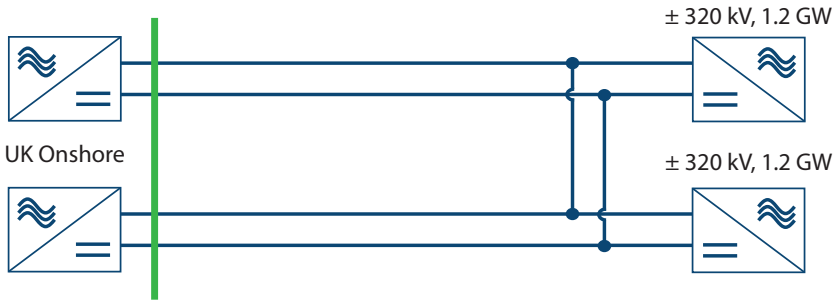



**Figure 5.2.:** Four terminal network

By simply connecting the two point-to-point links, the total infeed power to shore could exceed both the normal and infrequent loss of infeed limit of the GB transmission system, which are 1320 MW and 1800 MW respectively, in the event of a cable fault [125]. These infeed loss limits are in place to ensure that the system frequency, following a loss of generation, does not fall below the critical frequency limit of 49.2 Hz [125]. Using only AC-side protection, a fault on any of the cables would result in the entire grid being disconnected in order to isolate the fault, thus potentially exceeding the loss of infeed limits [126]. Therefore this network would require DC-side protection to ensure the loss of generation is kept within these limits. There are several degrees of DC-side protection that could be used, and they are briefly described below.

To fully protect the network, a DC circuit breaker would be required at each terminal and on the connecting DC link. At present the volume and weight of DC circuit breakers for commercial applications is unknown. Some designs require the use of a sizeable inductor to limit the rate of rise of current and this could result in the breaker requiring a separate offshore platform if the existing platforms do not have adequate space for the device. Placing this many DC circuit breakers in an MTDC network may have a high capital cost, and in a heavily meshed MTDC network with a DC circuit breaker placed at the end of each cable would have a higher capital cost than any other MTDC protection arrangement [126].

An alternative would be to sectionalise the grid and place a DC circuit breaker on the joining DC link only [127]. This would allow the link with the fault to be disconnected without interrupting the healthy link. This solution could have a lower capital cost, by having fewer breakers, but could suffer from having nowhere suitable to place the DC circuit breaker offshore without commissioning a separate platform. Although the cost of the DC breaker platform may not be comparable to the high cost of a HVDC converter platform.

Another option is to section the network using Normally Open Points (NOPs) and reconfigure the network in the case of DC-side fault. This solution would not require DC circuit breakers and the network could be disconnected using the AC-side circuit breakers. Alternatively DC fault blocking converters could be used in the network to limit the fault current fed into the fault from the AC networks, and provide reactive support to the AC network during the fault. A four terminal network using a NOP and DC fault blocking converters is studied in the following section.

### 5.2.1. Study Description

The four terminal system studied is shown in Figure 5.9. The system consists of two existing point-to-point links, which connect offshore wind from Dogger Bank to the UK, and the interconnecting link is operated as a NOP, which consists of two sets of DC switches, NOP1 and NOP2.

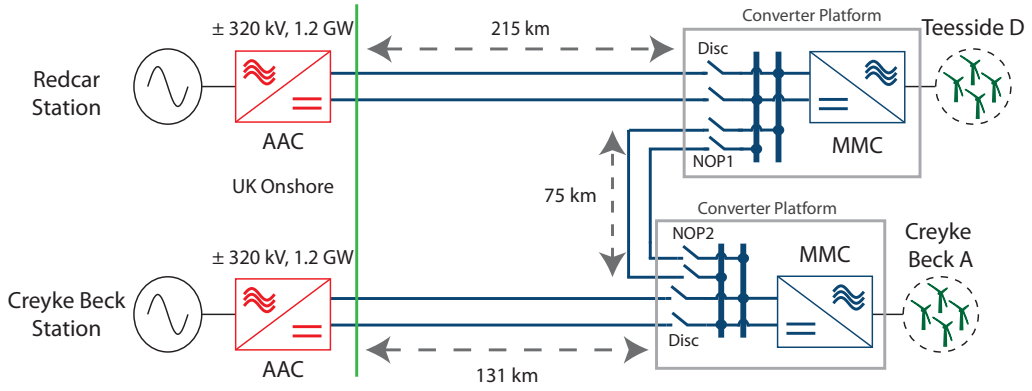



**Figure 5.3.:** Four terminal case study system

Two different VSC topologies are used, the HB MMC and the AAC. The MMCs are placed offshore and fault tolerant converters are placed onshore. There are two main reasons for placing the fault tolerant converter onshore. Firstly an increasing number of offshore wind turbines use fully rated converters to feed power into an AC collection network. This implies that the wind turbines can limit their output current in the case of a fault in the DC network hence are able to maintain the stability of the offshore AC network and reduce the inrush of fault current into the DC network [128]. This study assumes that the wind turbines use fully rated converters and thus allows a non-fault tolerant converter to be placed offshore. The onshore converters are at greater risk of large fault currents because they are connected to the national AC grid.

The second reason is the higher technology readiness level of the MMC, particularly for offshore applications, compared to that of DC fault blocking VSCs which have only recently been proposed and have yet to be built. To date, the MMC is the preferred choice for long distance offshore wind connection projects and has been used in several German projects [129]. Therefore, using the MMC offshore is a more convincing choice given that the technology is better understood and has operational experience offshore. By placing the newer technology onshore, operational experience can be obtained in a convenient and accessible environment.

As there are no DC circuit breakers commercially operational at present, and in order to ensure that the loss of infeed limit is not breached, the interconnecting link is configured as a NOP. In the event of a DC-side fault, the AAC limits the fault current, the MMC is blocked, and the wind turbine converters limit the fault current from the offshore wind farm. The network is then reconfigured, where the faulted cable is disconnected and the interconnecting link is brought into use, allowing power transfer from both wind farms to shore through one cable. The effectiveness of this scheme will illustrated after first examining its value.

### 5.2.2. Cost Benefit Case for the Interconnecting Link

This section outlines a simple cost benefit case for installing the interconnecting link between the two existing point-to-point links. It was assumed that the lifetime of the project is 25 years. The interconnecting link is estimated to be approximately 75 km in length. Two cost estimates from different data sources were used for the interconnecting link and its installation and they are given in Table 5.1. The first cost estimate used data from National Grid's ten year electricity statement [130]. The cost figure for second estimate was recommended by Arup and takes into account the increased water depth in the Dogger Bank development zone, leading to a higher cable installation cost.

| Cable Length | Estimate | Cable Cost - pair (£M/km) | Total (£M) |
|---|---|---|---|
| 75 km | 1 | 1.32 | 99 |
| | 2 | 2.5 | 187.5 |

**Table 5.1.:** Interconnecting link cost estimate

It should be noted that [130] provides a price range, and the highest price in the range was used to provide a conservative estimate. In order to determine the expected number of cable failures, a failure rate of 0.00052 /km/yr was determined

from [131] for offshore XLPE cables, and this was used to calculate the availability. Table 5.2 shows the data for the three cables in the case study system, including the Mean Time Between Failure (MTBF) and Mean Time To Repair (MTTR). The availability is found using (Equation 5.1), where the MTBF and MTTR are in hours.

$$A = \frac{MTBF}{MTBF + MTTR} \tag{5.1}$$

| Parameter | Creyke Beck | Teesside | Link |
|---|---|---|---|
| Cable length (km) | 131 | 215 | 75 |
| Failure rate | 0.068 | 0.112 | 0.039 |
| MTBF (years) | 14.79 | 8.94 | 25.64 |
| MTTR (days) | 65 | 65 | 65 |
| Availability | 0.988 | 0.9801 | 0.9931 |
| Unavailability | 0.012 | 0.0199 | 0.0069 |

**Table 5.2.:** Availability data

Over the project lifetime there is a high probability of three cable fault events, one for the Creyke Beck link, two for the Teesside link, and none for the interconnecting link.

To determine the amount of energy lost during a cable outage period a wind regime, with a Rayleigh probability density function, was used. It was assumed that as the two offshore wind farms are geographically close that the wind speed experienced at both wind farms would be approximately the same. The amount of energy supplied for a year, with no fault events, and the amount of energy produced over the specified MTTR duration was determined and the method is outlined in Appendix D. The amount of energy produced by a single wind farm over the project lifetime was found to be 160 TWh. The amount of energy that is not supplied during the repair time of a cable from a single wind farm is approximately 1.14 TWh. The cost of energy is assumed to be £140/MWh and this figure is the forecasted strike price

set for the year 2018/2019 by the UK Department for Energy and Climate Change [132]. These cost and energy values were then used to determine the cost of Expected Energy Supplied (EES), defined in (Equation 5.2), where $A$ is the availability, $E_{WF}$ is the energy from the wind farm, and $C_{energy}$ is the price of energy. The cost of Expected Energy Not Supplied (EENS) is given in (Equation 5.3), where $U$ is the unavailability.

$$C_{EES} = E_{WF} \times C_{energy} \times A \tag{5.2}$$

$$C_{EENS} = E_{WF} \times C_{energy} \times U \tag{5.3}$$

Table 5.3 shows the cost data for the four terminal network with and without the interconnecting link. The $C_{EENS}$ without the interconnecting link shows how much revenue is lost, due to energy not supplied, over the lifetime of the project because of cable failures. When the interconnecting link is used it should be noted that a fault on one cable results in the other healthy cable being used to transfer energy from both wind farms with a limit of 1,200 MW. For example a fault on the cable connecting Redcar and Teesside D would result in increased power transfer on the Creyke Beck cable. This is illustrated for clarity in Figure 5.4. The maximum amount of potential energy recovered through network reconfiguration is approximately 490 GWh during the outage and repair time. This energy figure does not take into account the event of wind curtailment due to the power capacity limit of the interconnecting link. The cost data in Table 5.3 shows the maximum revenue that could be recovered in the event of a fault. The $C_{EES}$ during the MTTR is calculated using (Equation 5.2) and the availability values for the interconnecting link and the healthy link.

| **Without Interconnecting Link** | | |
|---|---|---|
| **Project** | Creyke Beck | Teesside |
| **$C_{EENS}$ for 25 years** | £268.8M | £445.8M |
| **With Interconnecting Link** | | |
| **Fault event on** | Teesside cable | Creyke Beck cable |
| **$C_{EES}$ during MTTR** | £67.3M | £66.8M |
| **No. of faults** | 2 | 1 |
| **Increased revenue** | £134.6M | £66.8M |
| **Combined increased revenue** | £201.4M | |

**Table 5.3.:** Cost data for the four terminal network over a 25 year lifetime

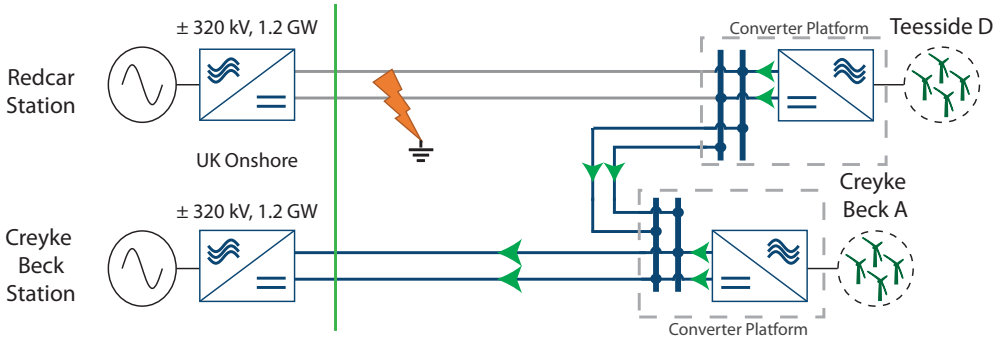



**Figure 5.4.:** Power routing after a fault on the Redcar - Teesside link

Table 5.3 shows that the interconnecting link is paid back by just two cable fault events in the four terminal network for cost estimate 1. This would result in additional revenue of £102.4M, which takes the cable cost into account, in the likely event of three cable faults. For cost estimate 2, all three fault events on the cables would need to occur to recover the cost of the cable and its installation. The additional revenue would be £13.9M for three fault cases for this cable cost estimate. Although the increased revenue for both cases is not be substantial, this analysis shows that the installation of the interconnecting link has a positive economic benefit. The NOP could also be used to deliver power from both wind farms in the event of an outage at one of the onshore converter, whether forced or scheduled.

### 5.2.3. Simulation

To show the technical feasibility of the scheme, the four terminal case study was simulated in MATLAB Simulink, and the converters were modelled using the AVMs developed in Chapter 4. The cable was modelled using a distributed parameter line. The data for the simulation is given in Table 5.4. The offshore wind farms were represented simply as AC voltage sources, with very close correlation such that the power from both wind farms is the same. Two scenarios were simulated, a normal operating scenario and a DC fault scenario.

| Parameter | Value |
|---|---|
| DC bus voltage | ± 320 kV |
| Rated power (at each terminal) | 1200 MW |
| Cable resistance | 11.3 mΩ/km |
| Cable inductance | 0.212 μH/km |
| Cable capacitance | 0.632 mF/km |

**Table 5.4.:** Four terminal case study data

#### Normal Operation Scenario

The system was simulated for normal operating conditions to show the MMC and the AAC operating in a point-to-point link. Figure 5.5 shows the cable voltage and power at the two terminals of the Creyke Beck link. The power is ramped from zero to full power and then down to 600 MW (0.5 pu). The MMC is in power control mode and the AAC is in DC voltage control mode. The oscillation of the DC voltage is a result of the voltage controller of the AAC, which is a PI controller. As the power increases the DC voltage can be seen to reduce due to the resistivity of the cable. The difference in power between the offshore and onshore terminals shows the power loss to the cable.

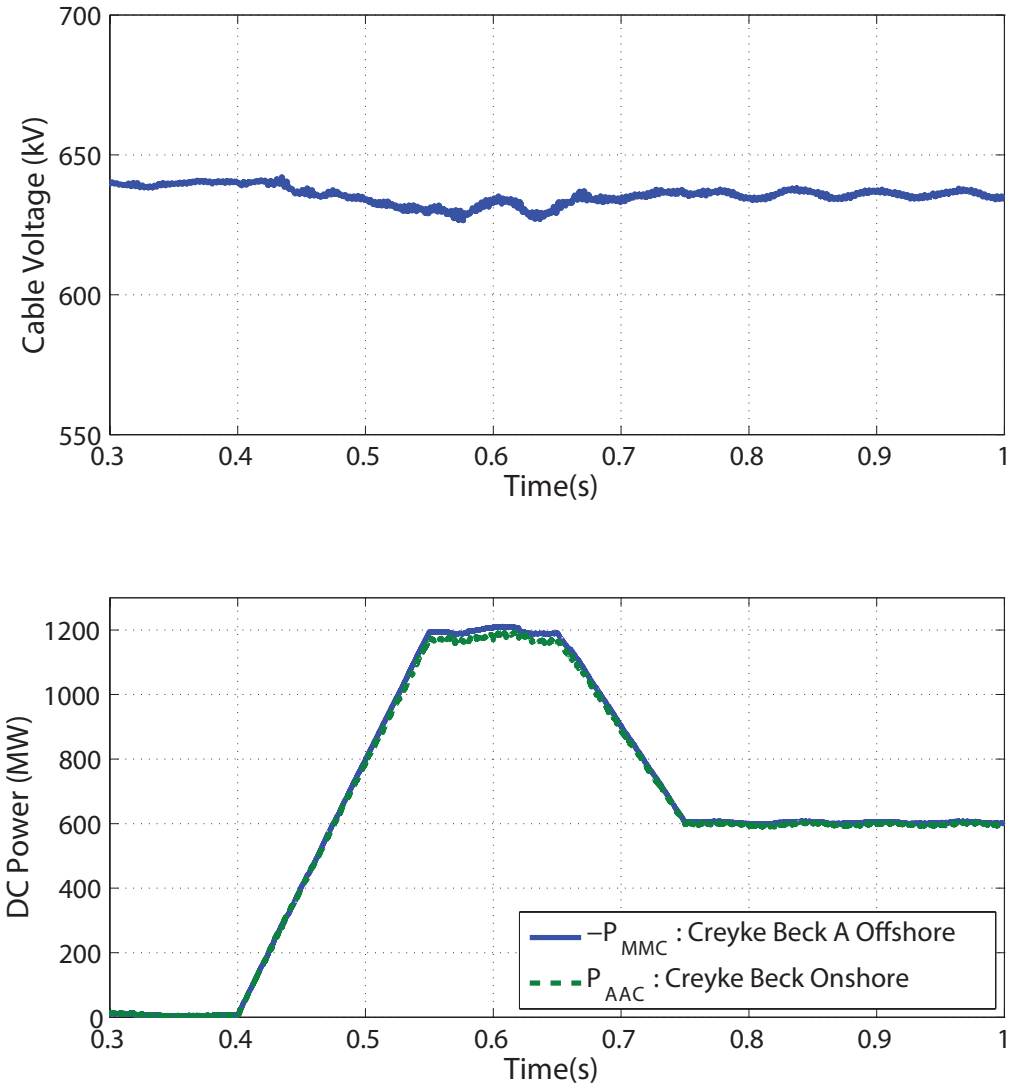



**Figure 5.5.:** Power transfer on Cryeke Beck link

### DC Fault Scenario

A permanent DC line-to-line fault was placed half way along the cable between Redcar station and the wind farm at Teesside D. It is assumed that both wind farms are producing 600 MW each prior to the fault. The fault was applied at 0.55 s into the simulation, as shown in Figure 5.6. Table 5.5 describes the switching sequence of the DC switches and the MMC blocking instances after the fault.

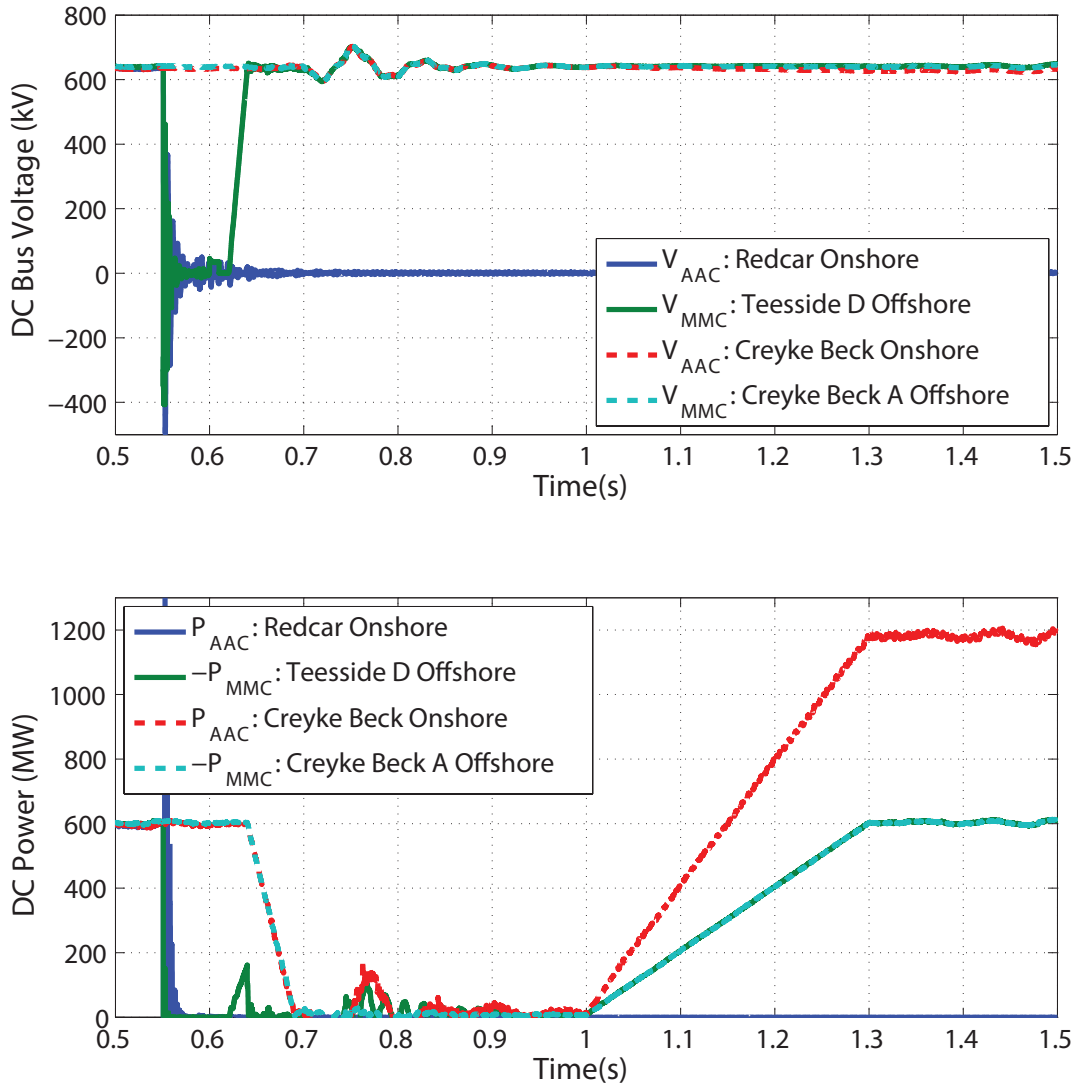



**Figure 5.6.:** DC line-to-line fault simulation sceanrio

| Time (s) | Action |
|---|---|
| 0.55 | Fault happens on Redcar - Teesside link |
| 0.551 | Block MMC at Teesside |
| | Power ramped down at Teesside wind farm |
| 0.6 | Open DC disconnector at Teesside MMC |
| | Unblock MMC at Teesside |
| 0.61 | Close NOP1 |
| 0.62 | Charge DC bus and interconnecting cable section |
| 0.64 | Power ramped down at Creyke Beck wind farm |
| 0.7 | Close NOP2 |
| 1 | Power ramped back to 600 MW from both offshore wind farms |

**Table 5.5.:** Switching sequence post fault

At the instant of the DC fault, the voltage of the faulted cable falls to zero and oscillates due to reflections of the voltage in the cable. It is assumed that the fault is detected quickly and the offshore MMC is blocked 1 ms after the fault, the offshore wind farm limits the fault current and the power from Teesside D wind farm is ramped down to zero. At 50 ms post fault, when the faulted cable voltage is zero, the disconnector between the MMC and the faulted cable section is opened, disconnecting the faulted cable section. This allows the MMC at Teesside D to be de-blocked. Following this NOP1, which connects the Teesside D MMC to interconnecting link, is closed. This enables the DC bus capacitor of the MMC and the 75 km cable section of the interconnecting link to be charged from the energy stored in the MMC and the wind farm. The power of the healthy link is ramped down to zero to allow the interconnecting link to connect in order to reduce the voltage oscillations on the cable. On the closing of NOP2, at 0.7 s, the DC voltage of the network fluctuates as the DC voltage controller at the AAC in Creyke Beck adjusts to the additional cable impedance that has been added to the system. At 1 s, the power of both wind farms is ramped up to 600 MW at each wind farm, and a power transfer of 1200 MW is seen at the onshore station in Creyke Beck. In practice, the timings of the switch events are likely to be much greater to ensure

the network is safely reconfigured and limiting the impact of any voltage transients during disconnection or reconnection. Additionally the switching sequence may be altered to prevent the power on the healthy link from being reduced to allow interconnection. Figure 5.7 shows the onshore AAC at Redcar station providing 0.4 pu reactive power support to the AC network just after the DC fault. This figure also shows that the AAC successfully blocks the DC-side fault.

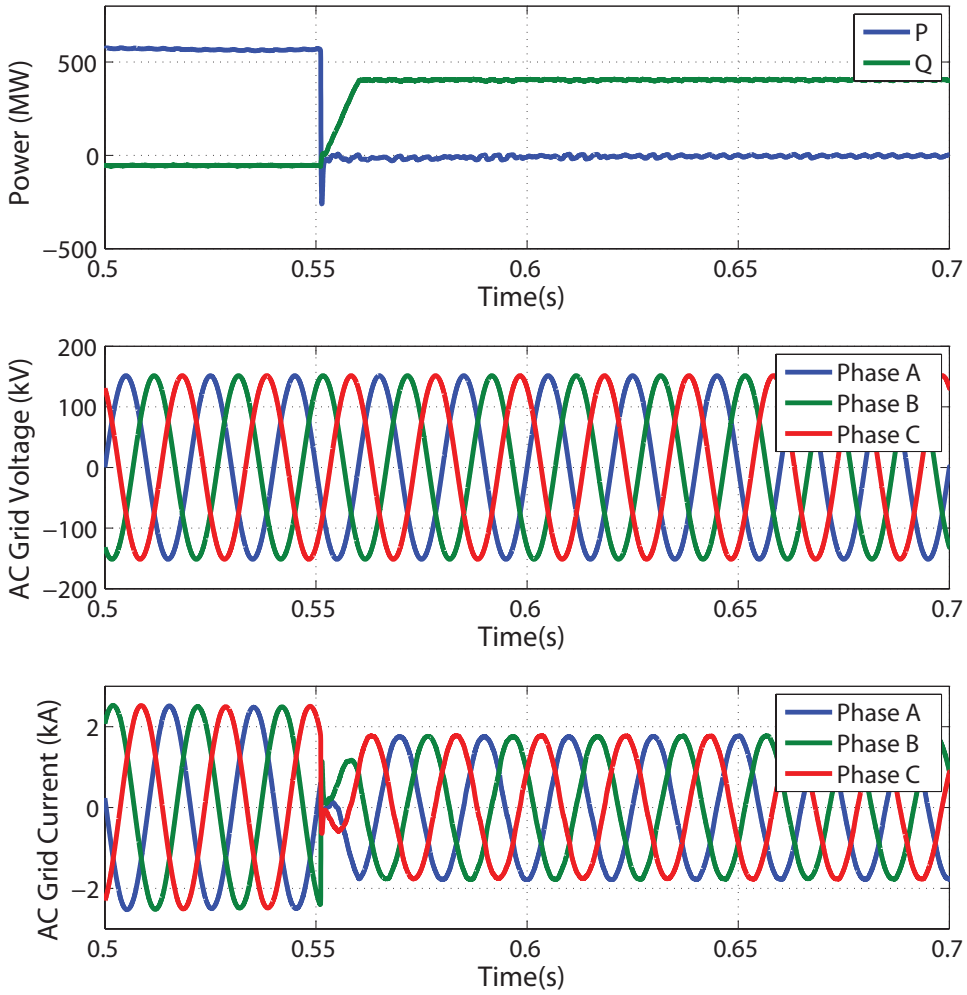



**Figure 5.7.:** STATCOM operation of the AAC at Redcar station

These simulations show that operating an interconnecting link as a NOP can increase the availability of energy of the four terminal network by allowing the network to be reconfigured in the event of a cable fault. This reconfiguration could also be

used during scheduled maintenance when the onshore converters are being serviced or repaired. This study also shows the merit of using fault blocking converters in a MTDC network to limit the DC fault current and provide STATCOM services to the AC system. This simulation study assumes that both links prior to the fault are operating at 0.5 pu power each. Capacity factor is used to measure the amount of delivered energy over time from a generator compared to its maximum energy potential. The capacity factor for offshore wind is approximately 40 % [133]. Given this capacity factor much of the energy that would otherwise be curtailed can be transported to shore by reconfiguring the network. If the capacity factor was much lower then there would be little to no economic merit of installing an interconnecting link. If the capacity factor were much greater than 50 %, more energy would need to be curtailed in the event of a fault a the wind farms would be operating closer to their rated power output on average.

## 5.3. MTDC Network Studies

### 5.3.1. Offshore Interconnections

The NSN link is likely to pass relatively closely with the Dogger Bank development of Teesside D, shown in Figure 5.8, and there could be a potential gain to connecting the offshore wind farm developments in Dogger bank to the NSN link. The benefit of connecting the offshore wind farm directly with an international interconnector is enabling the direct trade of renewable energy with that country, without having to route that generation to shore first. It continues on the idea of the offshore grid evolving over time and thus the four terminal network, studied previously, is used as the offshore wind network for this system. The MTDC network is shown in Figure 5.9.

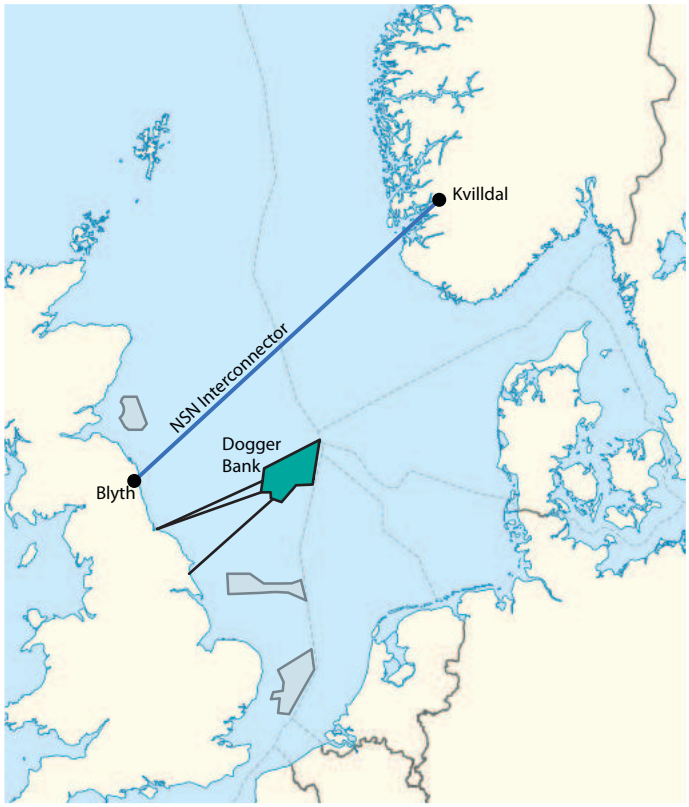



**Figure 5.8.:** North Sea offshore wind and NSN link

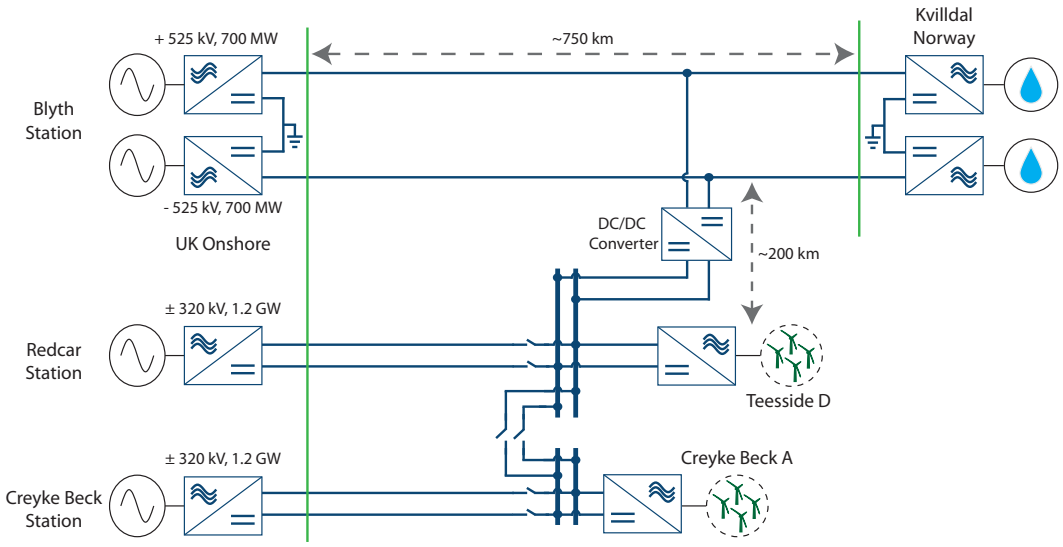



**Figure 5.9.:** Case study system

The system shows a HVDC link between the four terminal network and the bipole VSC link between the UK and Norway. The VSC technology that is likely to be used

is the HB MMC, and AVMs of the converters are used in this simulation study. The bipole link voltage was chosen to be ± 525 kV and each converter rated for 700 MW, and thus to connect the two systems a DC/DC converter is required. The preferred DC/DC converter topology is the design highlighted in Chapter 3, the HVDC auto transformer. The requirement of the DC/DC converter in the offshore environment means that an offshore platform would be required. The platform would house the DC/DC converter and would be the point where the cables are brought up from the seabed. Alternatively the DC/DC converter could be placed onshore in close proximity to the Blythe converter station to reduce cost. This would require overhead lines onshore, which may be opposed by the public, underground cables onshore, or placing the cables offshore while the converter remains on land. By connecting the DC/DC converter onshore in the event of a submarine cable failure the offshore wind power would need to be rerouted by closing the NOP and would not be able to be directly sent to Norway. Placing the DC/DC converter offshore allows the power to be directly routed to Norway and could relieve pressure on the AC system by rerouting power on the DC network. The DC/DC converter can also provide DC fault blocking capabilities which provides a firewall between the two DC networks. This research assumes that the DC/DC converter is placed offshore at the point where the NSN link is closest to the Teesside D wind farm. The distance between these two points was estimated to be approximately 200 km.

### 5.3.2. AVM of a DC/DC converter

The HVDC auto transformer converter configuration for interconnecting bipole links to symmetric monopole links is shown in Figure 5.10. In order to enable efficient computation time of the case study system an AVM of the DC/DC converter was developed. This was done to reduce complexity of the system model and to save time

in developing a full converter model and controller of the HVDC auto transformer.

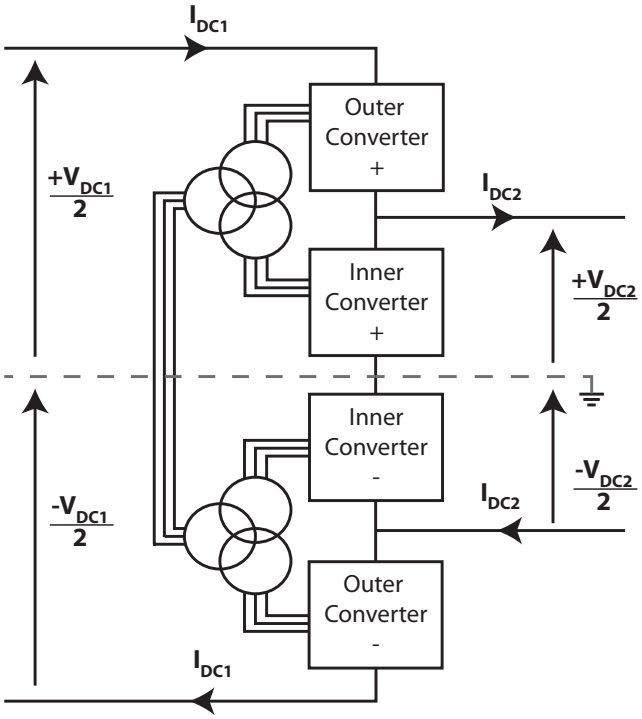



**Figure 5.10.:** HVDC auto transformer converter for interconnection of bipolar and monopolar HVDC

For bipolar interconnection three phase transformers can be used to improve energy transfer between the inner and outer converters. Both outer converters require the use of 70 % of the stack using FB SMs to block DC faults. The use of converter per pole enables the HVDC auto transformer converter to transfer power during a DC line-to-ground fault on the bipole [134]. Assuming good energy balancing within converter allows the AVM of the converter to be modelled as four controllable current sources, arranged as in Figure 5.11.

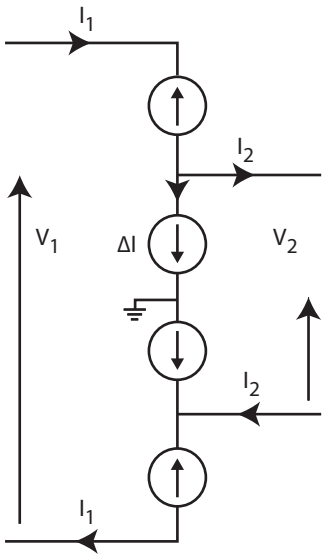



**Figure 5.11.:** AVM of the HVDC auto transformer converter

The two outer current sources maintain the current on the high voltage side of the converter, and the inner current source accounts for the difference in current between the two sides of the converter. This is illustrated in the following equations.

$$n = \frac{V_{high}}{V_{low}} = \frac{V_1}{V_2} \tag{5.4}$$

$$\therefore I_2 = nI_1 \tag{5.5}$$

$$\Delta I = I_1 - I_2 \tag{5.6}$$

$$\Delta I = I_1 - nI_1 \tag{5.7}$$

$$\triangle I = (1 - n)I_1 \tag{5.8}$$

From (Equation 5.8) it can be seen that only one current for the DC/DC converter AVM needs to be controlled to enable power transfer through the converter and this was done with a PI controller. The power rating of the DC/DC converter was limited to the power capacity of the cables in the four terminal network which was 1.2 GW.

### 5.3.3. Normal Operation Simulations

The system was simulated for different power references in normal operating conditions. The upper HVDC system is the bipole HVDC system between the UK and Norway, and the lower HVDC system is the four terminal network, from the earlier study, below the DC/DC converter. The four terminal network operates as described the previous section. In the bipole HVDC system the converters which are sending power are operated in power control mode and the terminals receiving power are operated in voltage control mode. The power flow scenarios that were considered are outlined below:

1. All converters ramp to full power, and there is no power transfer through the DC/DC converter, all other terminals at full power

2. Fall in wind power to 600 MW, and 600 MW of power is transferred from Norway to Redcar through the DC/DC converter

3. Wind power still at 600 MW and 600 MW power is routed from Blythe to Redcar through the DC/DC converter

4. Wind power producing 1200 MW and a power transfer of 600 MW is made from Teesside D to Blythe through the DC/DC converter

5. Assumed low UK demand and wind farms are producing 1200 MW, 600 MW power is transferred from Dogger Bank to Norway to be stored through the DC/DC converter

Figure 5.12 shows the power for each terminal for all five scenarios and shows the power transfer through the DC/DC converter.

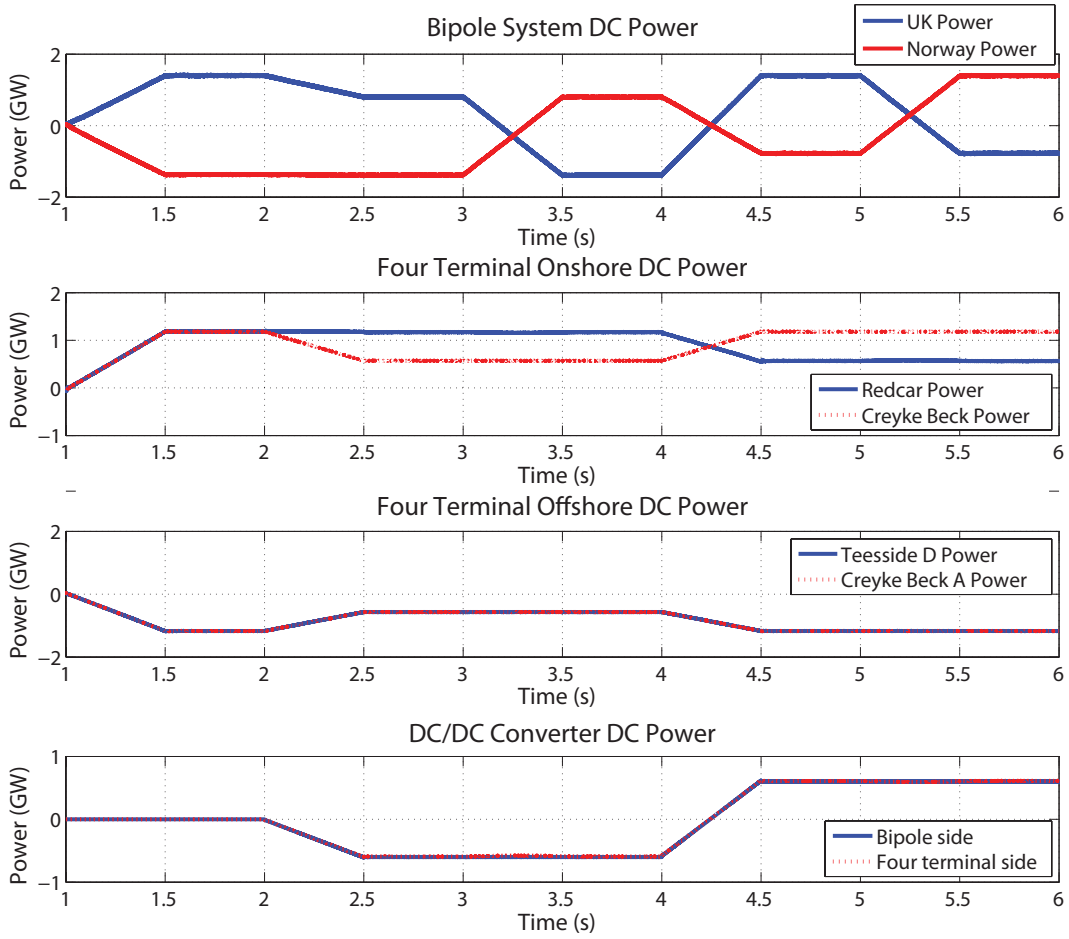



**Figure 5.12.:** Power transfer scenarios

Scenario 1 starts at 1 s into the simulation, scenario 2 at 2 s into the simulation and so on for the remaining scenarios. This figure shows that the DC/DC converter enables power transfer between the two HVDC networks and can enable the rerouting of power on the UK network. It was assumed that the two wind farms are closely correlated, this is shown in the third graph in Figure 5.12. The power at Creyke Beck onshore station is always what the wind farm is producing due to the NOP. So only the power from Teesside D is transferred through the DC/DC converter in these scenarios

### 5.3.4. DC Fault Scenarios

Three DC fault simulation scenarios were chosen to show how the MTDC might operate under fault conditions. The three fault scenarios which were considered are briefly outlined below:

1. Show firewall capability of DC/DC converter, while it is transferring power between the networks, with a DC-side line-to-ground fault in the bipole system

2. Power rerouting after a DC-side line-to-line fault on the cable connecting Redcar station and Teesside D wind farm through the DC/DC converter to Blythe, no power through the DC/DC converter prior to the fault

3. Power rerouting after a DC-side line-to-line fault on the bipole near the UK and rerouting power through the DC/DC converter to Redcar station, no power through the DC/DC converter prior to the fault

The fault is placed on the relevant network at 2 s in to the simulation for each scenario.

#### Scenario 1

A DC fault was placed on the positive pole of the bipolar link between the UK and Norway, half way along the cable. The system is operating with power being transferred from Norway to UK through the DC/DC converter, as in power transfer scenario 2 from the previous section. The total power transfer from Norway to the UK is 800 MW through the bipole, and 600 MW from Norway is routed through the DC/DC converter to Redcar. The offshore wind farms are producing 600 MW each.

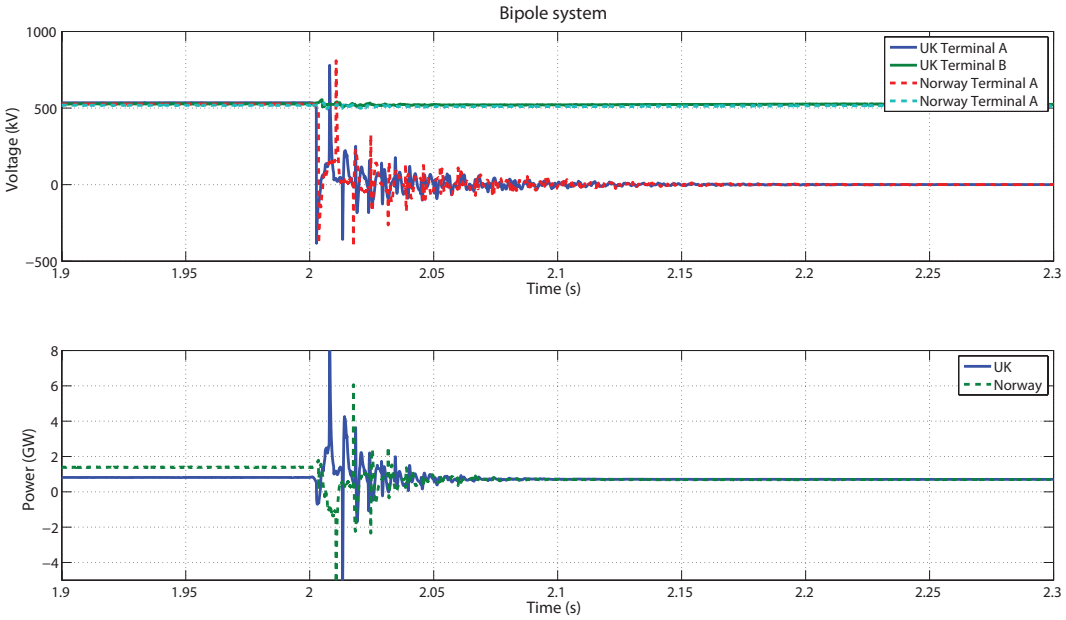



**Figure 5.13.:** Bipole voltage at each converter and total power at each terminal for scenario 1

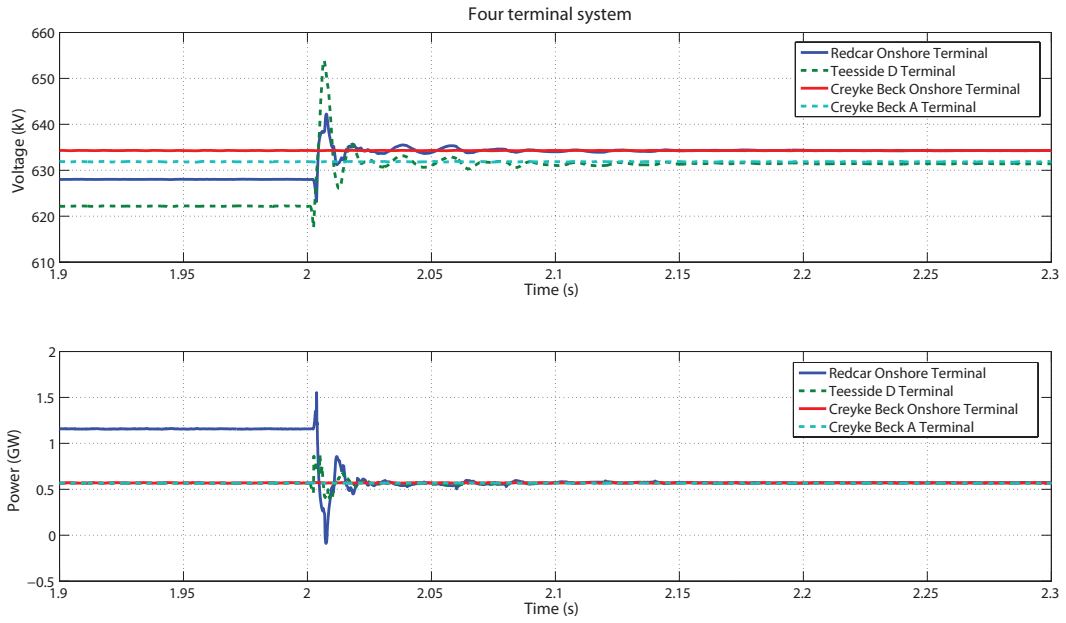



**Figure 5.14.:** Four terminal voltage and power at converter terminals for scenario 1

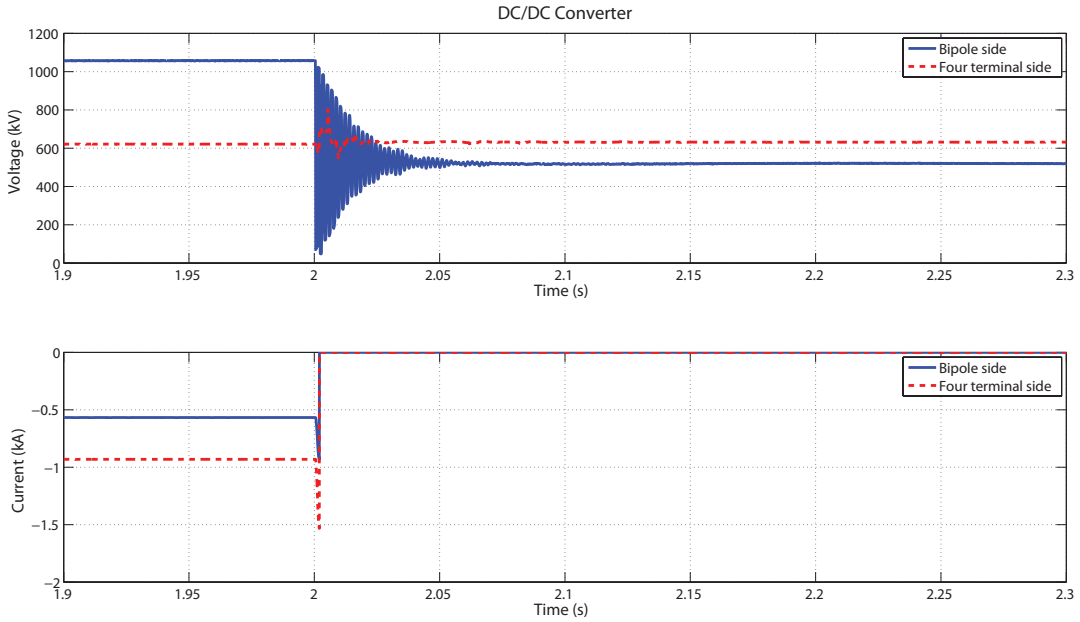



**Figure 5.15.:** DC/DC converter terminal voltage and current for scenario 1

The current reference through the DC/DC converter is set to zero to prevent the fault propagating through the converter. The oscillations of the voltage on the bipole network, , show the reflections of the voltage in the cable, where the voltage at Norway A (dashed red line) shows a similar response to the voltage at UK A (solid blue line) but with a delay in Figure 5.13. A disturbance is seen on the Redcar - Teesside link due to the sudden loss of power, with a maximum peak voltage of 1.0234 pu and then settles to its nominal in under 50 ms. Due to the sectioning of the four-terminal network by using a NOP, the Creyke Beck system sees no effect of the loss of power. The healthy link of the bipole continues to transfer power from Norway to the UK, and the power transfer between the two countries is 400 MW. This simulation shows that the DC/DC converter acts as a fire wall between the two HVDC networks.

### Scenario 2

This simulation scenario looks at the response of a DC line-to-line fault on the cable section between Redcar and Teesside D, the power is then routed through the DC/DC converter to the UK station at Blythe. A total power of 550 MW is being transferred from Norway to the UK, and both wind farms are producing 600 MW. The line-to-line fault is placed half way along the cable connecting Teesside D to shore. There is no power being routed through the DC/DC converter prior to the fault. The following figures show the power rerouting in the network.

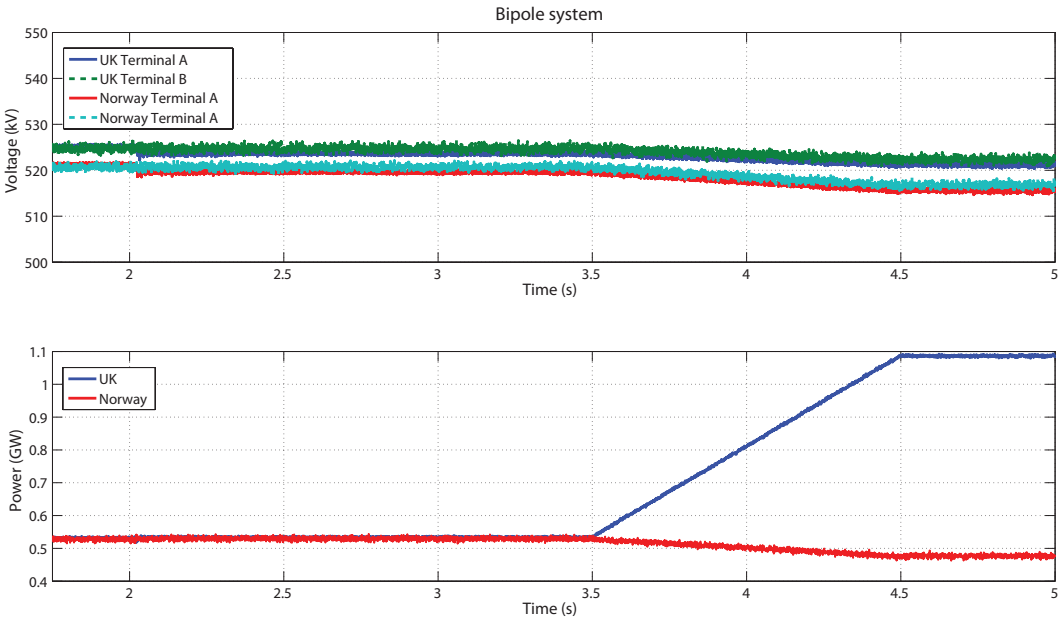



**Figure 5.16.:** Bipole voltages at each converter and power at each terminal for scenario 2

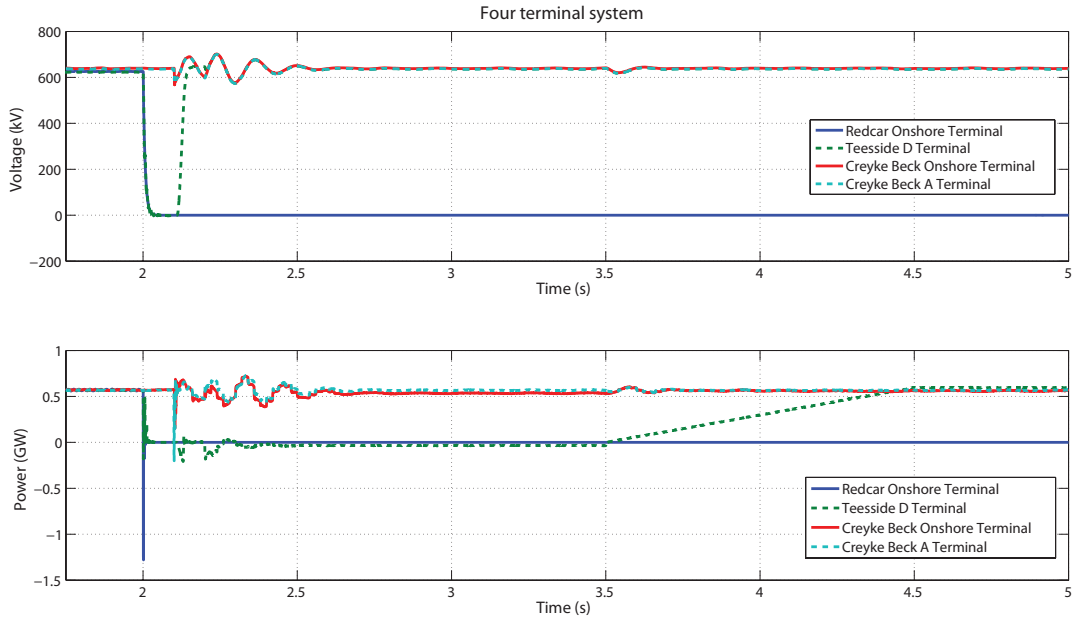



**Figure 5.17.:** Four terminal voltage and power at each converter terminal for scenario 2

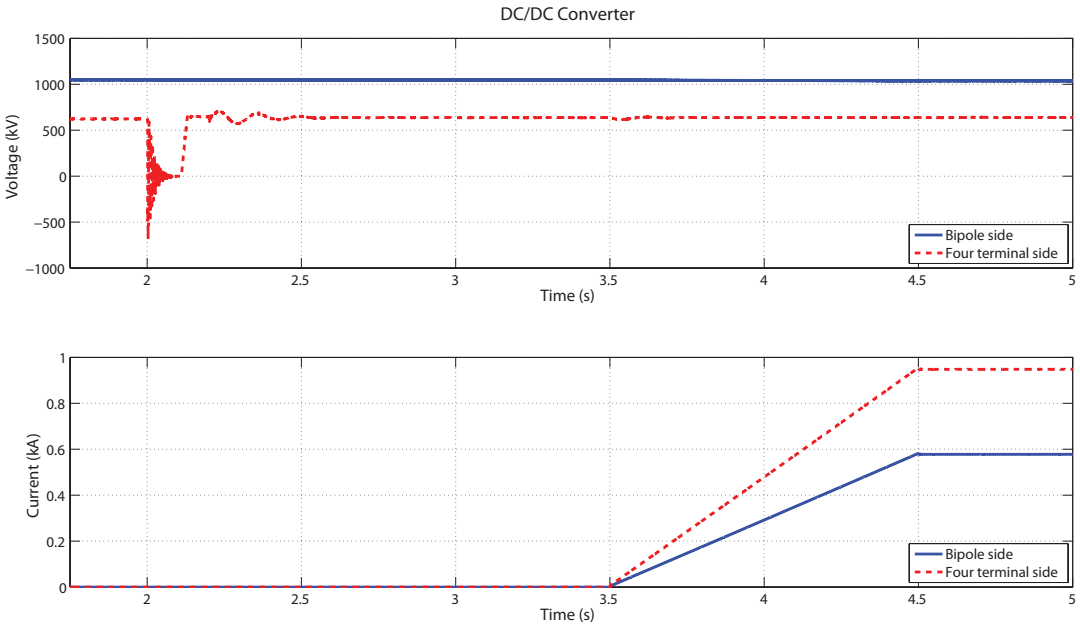



**Figure 5.18.:** DC/DC converter voltage and current for scenario 2

Figure 5.16 shows the converter DC voltages and terminal power for the UK Norway interconnection. These waveforms show that the fault does not propagate through the DC/DC converter. As power is transferred on to the bipole the cable

voltage of drops due to the action of the voltage controller at the UK terminal. In Figure 5.17 the voltage of the cable between Redcar and Teesside D falls to zero at the instant of the fault. The faulted cable section is disconnected using disconnectors, which are modelled as ideal switches, and the NOP is closed to connect the Creyke Beck link. Once the cable voltage has returned to its nominal voltage power is transferred from Teesside D to the UK through the DC/DC converter. The DC/DC converter waveforms, in Figure 5.18, further illustrate the fault blocking capability of the converter.

### Scenario 3

This fault scenario shows a line-to-line fault on the UK to Norway bipole HVDC link, and the power is then routed through the DC/DC converter to Redcar station. The power transfer to the UK is 1000 MW, and the wind generation is approximately 150 MW prior to the fault.

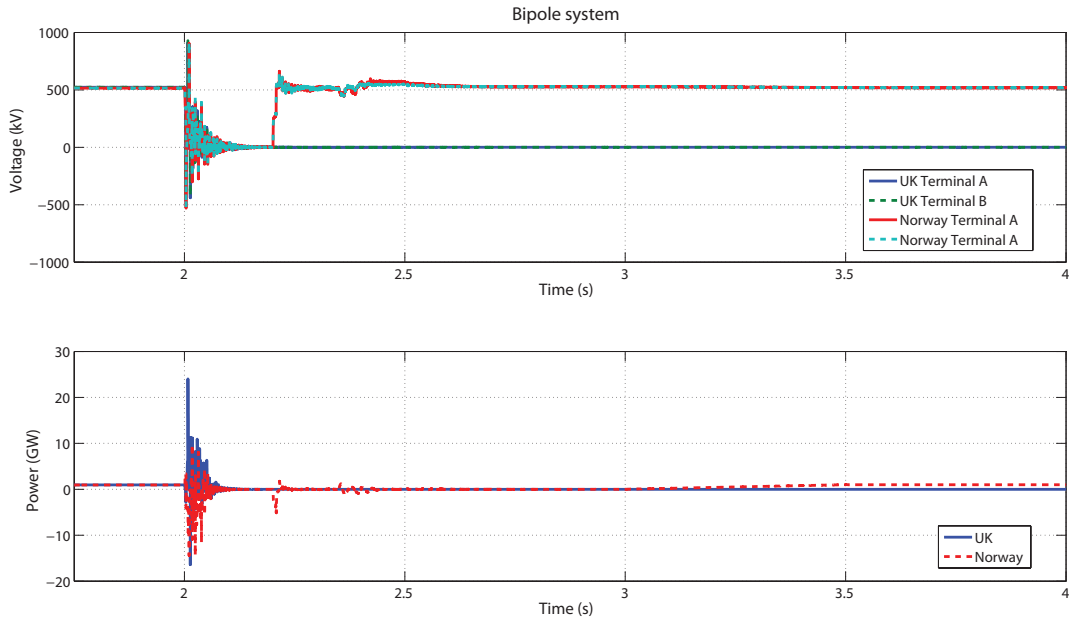



**Figure 5.19.:** Bipole voltage at each converter and total power at each terminal for scenario 3

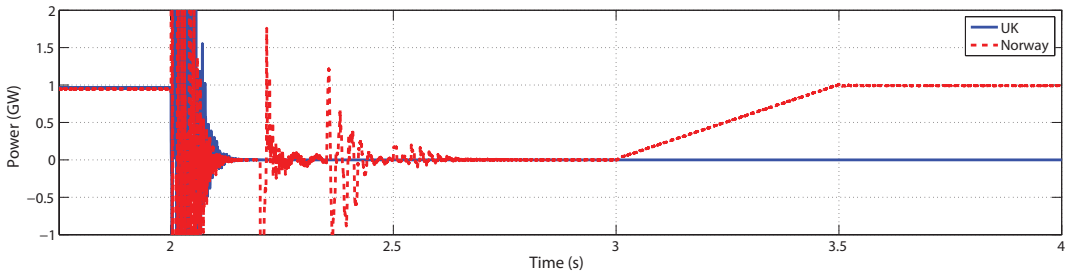



**Figure 5.20.:** Zoom in of terminal power of bipole network

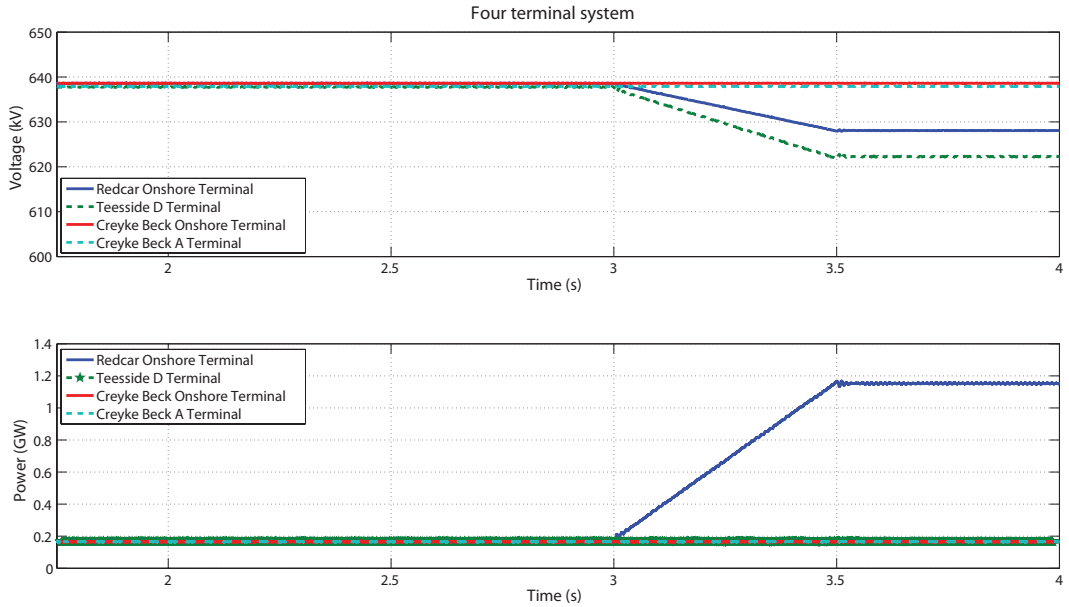



**Figure 5.21.:** Four terminal voltage and power at converter terminals for scenario 3

The response of the bipole network to the DC fault is shown in Figure 5.19, and a zoom in of the power plot is given in . The DC voltage collapses to zero and the entire network is isolated using AC-side protection. The faulted cable section is disconnected through DC disconnectors and the AC circuit breakers at the Norwegian terminal are closed to allow the healthy section of the network, between the DC/DC and the Norway terminals, to be restarted. The power is then returned to its pre-fault set-point and transferred through the DC/DC converter to Redcar station. The waveforms of the four terminal system, in Figure 5.21, show that the

fault does not propogate through the DC/DC converter and that the power ramps up to 1150 MW at the Redcar onshore station.

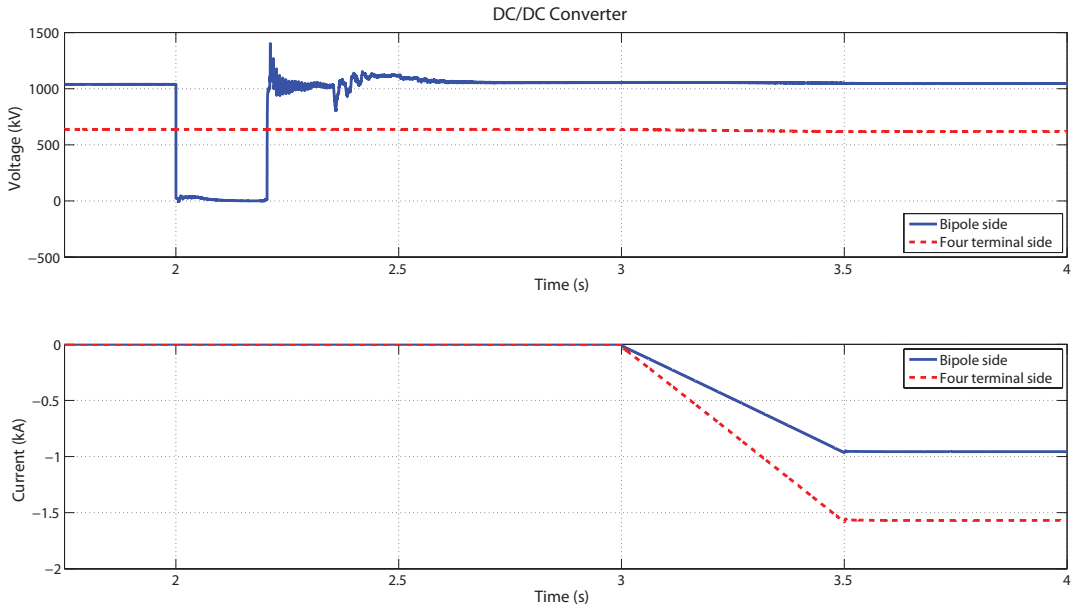



**Figure 5.22.:** DC/DC converter terminal voltage and current for scenario 3

### Discussion

This set of simulations illustrate the use of the DC/DC converter to provide a firewall between the two networks, thus sectioning the two networks and reducing the necessity for DC circuit breakers. The power flow control ability of the DC/DC converter is also shown. This feature may be advantageous as MTDC grids become larger and only the impedance of the line dictates the direction of power flow [135]. These simulations also show that the AVM of the HVDC auto transformer that was developed for the studies was able to provide the main characteristics of the converter. However, a more detailed model may be required to investigate the affect that DC faults have on the control of the converter.

## 5.4. Summary

This chapter demonstrates the benefit of modelling of MTDC networks using AVMs of the power electronic converters. Two MTDC networks are studied though simulation, a four terminal network and a larger MTDC network.

The four terminal network consists of two point-to-point links connected through a Normally Open Point (NOP). The NOP also allows the network to be sectioned during normal operation, and then to be reconfigured in the event of a DC fault on either point-to-point link. A simple cost benefit case is made for the installation of the NOP interconnecting link, which shows the possibility of a small economic benefit to having such a link. Both the MMC and the AAC are used in these networks. The MMC is used offshore and the AAC is placed onshore to limit fault current in the event of a DC fault. The four-terminal network is verified through simulation for normal operation, to show the MMC and AAC operating in the same network, and for a DC fault case. A DC line-to-line fault was placed on the four terminal network, the AAC limited the fault current allowing a DC switch to be opened to disconnect the faulted section of cable. The network was reconfigured to allow both MMCs to transmit power through one cable link to shore.

A larger MTDC network was also studied, where the four terminal network was connected to a bipole link through a DC/DC converter. The bipole considered was based on the link that is proposed between the UK and Norway. The DC/DC converter used was the HVDC auto transformer, which was highlighted in Chapter 3. An average model of the converter was developed to enable time efficient simulations. The system was tested for normal operating conditions to show power transfer through the DC/DC converter. Three DC fault scenarios were simulated to show the how the DC/DC converter could allow power rerouting after fault events, and that it could provide DC fault blocking capabilities.

# 6. Conclusion

## 6.1. General Conclusion

The work in this thesis looks at High Voltage DC (HVDC) converter topologies that could be used to develop a Multi-Terminal DC (MTDC) grid. The research is focused on the developments of offshore wind generation in the North Sea, in particular the UK Round 3 projects, and how they might be used as the starting point for an offshore MTDC grid.

A small study was carried out comparing two AC/DC converters, the Modular Multi-level Converter (MMC) and the Alternate Arm Converter (AAC). The MMC is a modular converter that produces an AC waveform with very little harmonic content, but the design is susceptible to DC-side faults. The AAC is a hybrid topology that maintains high power efficiency, comparable to the MMC, while providing DC fault blocking capabilities. The AAC requires only 52% more devices in the converter despite having four switching devices per submodule (SM). This is due to the use of director switches which are also responsible for blocking some of the arm voltage. The AAC was seen to require a smaller SM capacitor and thus requires less energy storage in the converter. Given that the capacitor can make up almost half the volume of the SM it is beneficial to have smaller capacitors.

One of the potential future enabling technologies to MTDC grids is the DC/DC converter, which could enable HVDC systems operating at different voltage magni-

tudes to be interconnected. An assessment of suitable converters for use in low to medium voltage conversion ratios was carried out. Six different topologies were assessed based on their operating principles, DC fault blocking capabilities, and power efficiency.

One of the prominent topologies at the beginning of the research was a resonant DC/DC converter that uses thyristors as the semiconductor device. This resonant topology offers DC fault blocking capabilities and low power losses for low conversion ratios. On further study of the resonant DC/DC converter, it was observed that for low conversion ratios the converter became susceptible to DC-side faults during a brief period of its switching cycle. A new mode of operation, termed the Alternate Discontinuous Mode (ADM), was developed to alleviate this problem. In doing this work, a new set of simpler design equation were developed for the passive components of the converter. This work was done in collaboration with Dr. Michaël Merlin. In general this resonant converter topology was found to be have higher power losses than other topologies, ruling it out from further system studies.

All of the DC/DC converter topologies were compared for a specific scenario and the number of semiconductor devices required, number of passive elements, and the size of the energy storage components were assessed. One converter, the HVDC auto transformer, had some advantages over the other converters. The HVDC auto transformer has low power losses, and requires little filtering on the output DC waveforms. Compared to other modular based topologies, the HVDC auto transformer topology had the lowest number of devices and required the smallest amount of energy storage, implying that the design would have a lower volume. This topology was deemed to be the most suitable design in theory for offshore applications for low to medium voltage conversions.

The importance of time efficient converter modelling was outlined and a method-

ology to develop Average Value Models (AVM) of AC/DC converters based on a literature review of research in the area. The arm of the MMC was represented using a voltage source in series with a resistor, an arm inductor, and a switch, and in parallel with a diode. The switch and diode were added to improve the response of the MMC AVM in DC fault conditions. By removing all the switching components, the controller was also reduced as the low level firing control was no longer necessary. The voltage command from the current controller was sent to the controllable voltage source. The voltage source in simulation can produce whatever voltage is asked of it, while in a physical converter there is a limit on the amount of voltage available depending on the energy stored in the stack of SMs. The energy in the stack is directly related to the capacitor voltage of each SM, and in a FSM the energy of each SM is monitored and is used to place a limit on the voltage control command improving the accuracy of the converter. This energy feedback is neglected in some average value converter models.

The MMC AVM was directly compared to a Full Switching Model (FSM), this allowed the converter model to be verified for both steady state and fault conditions. It was seen that the AVM of the MMC simulated up to 14 times quicker than the FSM. The accuracy of the AVM was calculated by comparing the difference between the AC and DC currents of the two model types. The AVM maintained a reasonable accuracy of approximately 3.5% for both AC and DC currents for a time step of 50 $\mu$s . The MMC AVM was then compared to the FSM in a point-to-point link, for normal operating conditions and three fault scenarios. The AVM was seen to simulate faster than the FSM system, with a further improvement over the single converter simulation. The AVM results matched closely with the FSM for a three-phase AC fault and a single-phase-to-ground AC fault. The AVM was also tested for a DC line-to-ground fault, and the AVM matched the FSM for the first two

milliseconds post fault after which there was a significant error between the two models. In practice the AC-side breakers would be used to clear the fault in the DC network, and implementing this in a network would improve the accuracy of the AVM for a DC fault.

This AVM methodology was used to developed an AVM of the AAC. The arm representation for this converter required a controllable voltage source with a series resistance, an arm inductor, and a single switch for the director switches. Additional circuitry was not required to represent the converter for DC faults scenarios as the controller allows the AVM to apply the negative stack voltage required to block a DC-side fault. The AAC AVM was also compared directly to a FSM and was observed to simulate up to 17 times faster. The accuracy was again measured by looking at the percentage difference between the AVM and FSM currents and a the difference was below 3.5% for the AC and DC current. The AVM was then placed in a point-to-point link and compared with the FSM for three fault scenarios. The AAC AVM provided a close match to the FSM for an AC line to ground fault, a single phase to ground AC fault, and a DC line to ground fault. The AVM of the AAC was also verified with a lab scale experimental setup.

Several converter models have been developed and a library of models was available to simulate larger HVDC networks. The first HVDC network to be studied was a four terminal network, consisting of two connected point-to-point links. It is likely that any MTDC network in Europe will develop over time through interconnection of preexisting point-to-point links. For the UK simply connecting two point-to-point links together could violate the loss of infeed limits, and would thus require additional protection. The two point-to-point links were connected through a normally open point (NOP) which allowed the system to be reconfigured in the event of a DC-side fault. A simple cost benefit analysis was performed to show the

value of adding the interconnecting link, and operating it as a NOP. The analysis showed that there is a very small monetary benefit to including this interconnecting link.

The four terminal network used both the MMC and the AAC topologies. The MMC was placed offshore, as there is presently operational experience placing this design offshore, and many wind turbines now use fully rated converters. This implies that the wind turbine converters can limit fault current in the event of a DC fault, allowing a non-fault tolerant converter to be placed offshore. The AAC was placed onshore as the topology was only recently proposed and any operational experience should be gained from a known, and easily accessible, environment. A normal operation simulation showed the MMC and AAC operating in the same link. The network was simulated for a DC fault scenario and the network was reconfigured to enable power transfer from both wind farms through a single link to shore. This demonstrated that NOP can be used to interconnect existing HVDC links and facilitate MTDC grids, potentially reducing the immediate commercial need for a DC circuit breaker.

Following from the four terminal network study, a larger DC system was simulated. The system expanded on the four terminal network by connecting it to a bipolar HVDC interconnector between the UK and Norway. This continued the idea of an evolving grid. The two HVDC systems were assumed to operate at different voltage levels and were connected through a DC/DC converter. The DC/DC converter model that was used was an average model of the HVDC auto-transformer converter recommended for low to medium conversion ratios from Chapter 3. The system was simulated for different power transfer scenarios to show the DC/DC converter transferring energy between the two systems. Several DC fault scenarios were also simulated to show that the DC/DC converter can prevent disturbances from one

system propagating into the other. They also showed the benefit of using average value models, the average simulation time for 5 s of data, with a time step of 50 µs, was 4:30 minutes. These simulation studies showed how a MTDC grid in the North Sea might evolve and how DC/DC converters enable increased interconnection and provide additional functionality through DC fault blocking.

## 6.2. Contributions from the Author

Within the research presented in this thesis, the author has made the following contributions:

**Assessment of DC/DC converters for MTDC:** An assessment of potential DC/DC converter topologies for use in high voltage, high power operations was carried out for low to medium conversion ratios. Several aspects of the converters were assessed including mode of operation, power efficiency, fault blocking capability, and potential volume. For the application considered the HVDC auto-transformer converter was deemed to be the most suitable topology.

**Development of Alternative Discontinuous Mode:** An alternative mode of operation was developed for a resonant DC/DC converter, termed Alternate Discontinuous Mode (ADM). This mode of operation ensures that the converter can block DC faults at all times during the switching period. An additional outcome of designing for this mode of operation was the derivation of simpler design equations for all of the resonant passive components of the converter.

**AVM Voltage Limiter:** In a physical MMC the amount of voltage available from each arm is related to the amount of energy stored in the SM capacitors in the arm. In the average models developed in this thesis the stacks of SMs is represented by a controllable voltage source. A voltage does not accurately

represent the dynamics of a stack of capacitors. A voltage limiter was developed to allow feedback of the amount of energy in the capacitors in the arm and prevent the voltage source from producing unrealistic voltages. The limiter uses the measured stack energy to estimate the average SM capacitor voltage for the arm. The voltage command from the controller is divided by this average SM voltage and passed through a quantizer and a saturation block to ensure the voltage command does not exceed the number of SMs that are in the stack. This is then multiplied by the average SM voltage and the command is sent to the voltage source.

**Development of an AVM of the AAC:** An AVM of the AAC was developed. The AAC is a recently proposed topology which can block DC-side faults. This AVM was shown to maintain accurate representations of the external converter waveforms, for normal operation and for AC-side and DC-side faults. This model is intended to made available for public download.

**Protection Method for a Four Terminal Network:** A protection method for a four terminal network was proposed that uses readily available DC switches. The network is sectionalised using a normally open point between the two main power corridors. By using DC fault blocking converters at two of the terminals the fault current in the event of a DC fault can be limited and the DC bus voltage can be controlled to zero. The normally open point can be closed allowing the network to be reconfigured and can reroute power from the affected wind farm through the healthy cable.

**Analysis of MTDC Network:** MTDC networks are expected to develop over time and adjacent systems may not operate at similar voltage magnitudes. Analysis of a developing MTDC network off the UK coast was carried out. This network

used a DC/DC converter to interconnect a four terminal network with a bipolar HVDC scheme between the UK and Norway. The network was shown to have the ability to reroute power in normal operating conditions. The DC/DC converter acted as a buffer between the networks in the event of a DC-side fault, by preventing a fault on one side of the converter from propagating to the other side.

This research has led to the publication of the following papers listed below:

- **Journal Paper**
  - C. E. SHERIDAN, P. R. CLEMOW, G. CHAFFEY, P. D. JUDGE, M. M. C. MERLIN, AND T. C. GREEN, "*Experimental Verification of an Average Value Model of the Alternate Arm Converter*," Power Delivery, IEEE Transactions on. To be submitted in March 2016.
  - A. BEDDARD, C. E. SHERIDAN, M. BARNES, AND T. C. GREEN, "*Average Value Models of Modular Multilevel Converters for HVDC Systems*," Power Delivery, IEEE Transactions on, under review as of August 2015.
- **Conference Paper**
  - C. E. SHERIDAN, M. M. C. MERLIN, AND T. C. GREEN, "*Benefits of Operating a Four Terminal HVDC Network with a Normally Open Point*," International High Voltage Direct Current 2015 Conference, Cigré, 2015.
  - C. E. SHERIDAN, M. M. C. MERLIN, AND T. C. GREEN, "*Reduced Dynamic Model of the Alternate Arm Converter*," in Control and Modelling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on, 2014.

- C. E. SHERIDAN, M. M. C. MERLIN, AND T. C. GREEN, "*Study of a Resonant DC / DC Converter in Alternate Discontinuous Mode*," in Power and Energy Society General Meeting (PES), 2013 IEEE, 2013
- C. E. SHERIDAN, M. M. C. MERLIN, AND T. C. GREEN, "*Assessment of DC / DC Converters for use in DC Nodes for Offshore Grids*," in 10th IET International Conference on AC and DC Power Transmission (ACDC 2012), 2012

## 6.3. Future Work

Following from research described here, there are several avenues of future work that could be followed. One is the continued investigation of DC/DC converters for use in HVDC schemes. There have been very few studies which look at the operation of the DC/DC converter in large MTDC networks. Further exploration of the converters ability to provide additional power flow control to improve the operation of a MTDC network is also needed. This could also be expanded to add converter detail to studies of DC collection solutions for offshore wind farms.

For the MMC-based DC/DC topologies, the transformer stage is isolated from other AC networks, and thus does not have to operate with sinusoidal waveforms or at 50 Hz. A study on the effect of frequency on the operation of the front-to-front DC/DC has been carried out in [44]. A similar study for the HVDC auto-transformer converter could result in the optimisation of the internal converter transformer volume. Additionally the waveform shape does not need to be sinusoidal, and a study of alternative waveforms for the transformer is needed.

Further improvement of the AVM of the AAC is necessary to enable the model to be used in other software packages. In particular, a model for use in load flow packages, such as DIgSILENT PowerFactory, would allow the AAC to be included

in larger AC power system analysis. This would require the elimination of all power electronic components in the model, a single switch is used to represents the director switches in the AVM developed in this work. The model described in this work uses an ideal switch to model the director switches. There is also an opportunity to optimise the operation of the controller to further reduce the simulation time of the average model.

A single DC fault scenario was looked at in the simulation study of the four terminal network. Additional DC fault simulation studies are required to show that the system can operate for all cases. In the event of a DC line to ground fault on the bipolar link, the healthy line can still be operated and the system then looks like an asymmetric monopole. The HVDC auto-transformer with a return path can theoretically enable power transfer between the faulted bipole link and four terminal network [134]. Additional simulation studies are needed to assess feasibility of the MTDC suggested at the end of Chapter 5 and improved control algorithms could be applied to the network to improve operation. One interesting fault scenario would be to investigate the transfer of power for a DC line-to-ground fault on the bipole link. The faulted cable section, say the positive pole between the UK and the DC/DC converter, of the bipole link would be disconnected and both healthy sections of cable, both positive and negative, from the DC/DC converter to Norway would operate and transfer power through the DC/DC converter and through the negative pole from the DC/DC converter to the UK.

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# A. Current Derivations for ADM

In general a sinusoidal current can be described as in (A.1).

$$I(t) = \hat{I}sin(\omega t) \tag{A.1}$$

Thus to find the average current we can take the integral, from zero to $\pi$, of (A.1) and using the substitution $\omega t = \theta$:

$$\int_0^\pi I(t)dt = \int_0^\pi \hat{I}sin(\omega t)dt \tag{A.2a}$$

$$\frac{1}{\omega}\int_0^\pi I(\theta)d\theta = \frac{1}{\omega}\int_0^\pi \hat{I}sin(\theta)d\theta \tag{A.2b}$$

$$= \frac{1}{\omega}\left[-\hat{I}cos(\theta)\right]_0^\pi \tag{A.2c}$$

$$= \frac{1}{\omega}\left[-\hat{I}cos(\pi) - (-\hat{I}cos(0))\right] \tag{A.2d}$$

$$= \frac{2\hat{I}}{\omega} \tag{A.2e}$$

Squaring (A.1) gives:

$$I^2(t) = \hat{I}^2sin^2(\omega t) \tag{A.3}$$

To find the average current for the square of the current, or the rms current, again

the integral can be taken, from zero to $\pi$, of (A.3) and using the substitution $\omega t = \theta$:

$$\int_0^{\pi} I^2(t)dt = \int_0^{\pi} \hat{I}^2 sin^2(\omega t)dt \tag{A.4a}$$

$$\frac{1}{\omega}\int_0^{\pi} I^2(\theta)d\theta = \frac{1}{\omega}\int_0^{\pi} \hat{I}^2 sin^2(\theta)d\theta \tag{A.4b}$$

$$= \frac{1}{\omega}\int_0^{\pi} \hat{I}^2 \frac{1}{2}(cos(2\theta))d\theta \tag{A.4c}$$

$$= \frac{1}{2\omega}\left[\hat{I}^2\left(cos(\theta - \frac{1}{2}sin(2\theta)\right)\right]_0^{\pi} \tag{A.4d}$$

$$= \frac{1}{2\omega}\left[\hat{I}^2\left(\pi - \frac{1}{2}sin(2\pi)\right) - \left(0 - \frac{1}{2}sin(0)\right)\right] \tag{A.4e}$$

$$= \frac{\pi\hat{I}^2}{2\omega} \tag{A.4f}$$

# B. DC/DC Converter Comparison Data

This appendix details the IGBT counts and calculations from Chapter 3.

## B.1. Front-to-Front Converter

| Parameter | HV Bridge | LV Bridge |
|---|---|---|
| VSC | HB MMC | HB MMC |
| $N_{level}$ | 500 | 320 |
| $N_{level}$+ redundancy | 550 | 352 |
| Total SMs | 3300 | 2112 |
| $N_{IGBT}$/SM | 2 | 2 |
| **Converter Total** | | |
| $N_{IGBT_{Total}}$ | 10824 | |
| $N_{Capacitor}$ | 5412 | |

**Table B.1.:** No DC fault blocking front-to-front converter data

| Parameter | HV Bridge | LV Bridge |
|---|---|---|
| VSC | HB MMC | FB MMC |
| $N_{level}$ | 500 | 320 |
| $N_{level}$+ redundancy | 550 | 352 |
| Total SMs | 3300 | 2112 |
| $N_{IGBT}$/SM | 2 | 4 |
| **Converter Total** | | |
| $N_{IGBT_{Total}}$ | 15048 | |
| $N_{Capacitor}$ | 5412 | |

**Table B.2.:** DC fault blocking front-to-front converter data

## B.2. HVDC Auto Transformer

| | |
|---|---|
| $N_{SM}$ | 3000 |
| $N_{level}$+ redundancy | 3300 |
| $N_{HB\ SMs}$ | 2468 |
| $N_{FB\ SMs}$ | 832 |
| $N_{IGBT_{Total}}$ | 10098 |
| $N_{Capacitor}$ | 3300 |

**Table B.3.:** HVDC auto transformer data

## B.3. DC MMC

| Parameter | Inner Arm | Outer Arm |
|---|---|---|
| $N_{level}$ | 320 | 180 |
| $N_{level}$+ redundancy | 352 | 198 |
| Total SMs | 704 | 396 |
| $N_{IGBT}$/SM | 2 | 4 |
| **Converter Total** | | |
| $N_{IGBT_{Total}}$ | 2992 | |
| $N_{Capacitor}$ | 1100 | |

**Table B.4.:** DC MMC data

## B.4. LCL Converter

| Parameter | HV Bridge | LV Bridge |
|---|---|---|
| $N_{valve}$ | 500 | 320 |
| $N_{valve}$+ redundancy | 550 | 352 |
| $N_{IGBT}$ | 2200 | 1408 |
| **Converter Total** | | |
| $N_{IGBT_{Total}}$ | 33608 | |

**Table B.5.:** LCL converter data

## B.5. Resonant Converter

| Parameter | HV Bridge | LV Bridge |
|---|---|---|
| $N_{valve}$ | 223 | 223 |
| $N_{valve}$+ redundancy | 246 | 246 |
| $N_{Thyristor}$ | 984 | 984 |
| **Converter Total** | | |
| $N_{Thyristor}$ | 1968 | |

**Table B.6.:** Resonant converter data

## B.6. LCL Converter Capacitor Calculation

The design equations for the LCL are derived in [101] and the key design equations are defined below:

$$s = \frac{V_1}{V_2} \tag{B.1}$$

$$k_1 = 1 - \omega^2 L_2 C \tag{B.2}$$

$$k_2 = 1 - \omega^2 L_1 C \tag{B.3}$$

$$k_3 = L_1 + L_2 - \omega^2 L_1 L_2 C \tag{B.4}$$

Where $s$ is the stepping ratio, which is the inverse of the conversion ratio, and $k_1$, $k_2$, and $k_3$ are coefficients used to determine the values for the passive components. The values of $k_1$ and $k_2$ can be varied in the design process to alter the values of the passive components. The variable $k_1$ is defined to be in the range shown in (B.5).

$$-\frac{1}{s} < k_1 < 1 \tag{B.5}$$

The variable $k_2$ and $k_3$ can be defined as

$$k_2 = k_1 s^2 \tag{B.6}$$

$$k_3 = \frac{-pV_{1_{ACM}} 2\sqrt{2} V_2 \sqrt{1 - s^2 k_1^2}}{P\omega\pi} \tag{B.7}$$

Where $p$ is the number of phase arms, which for this study was two, $V_2$ is the output voltage, which is the higher voltage magnitude, and $P$ is the power of the converter. The value of $s$ for this study was 0.64. The definition for the rms line-neutral AC voltage, $V_{1_{ACM}}$, for the low voltage side is given in (B.8). The angle $\pi/2$ is used as this gives the maximum AC voltage.

$$V_{1_{ACM}} = \frac{4V_1}{\sqrt{2}\pi} sin\left(\frac{\pi}{2}\right) \tag{B.8}$$

These equations produce a series of graphs for varying $k_1$ that can be used to determine the parameters of the converter. These plots are shown in Figure B.1.

The value for $k_1$ was chosen to be 0.5 and this gave the values for passive components shown in Table B.7.

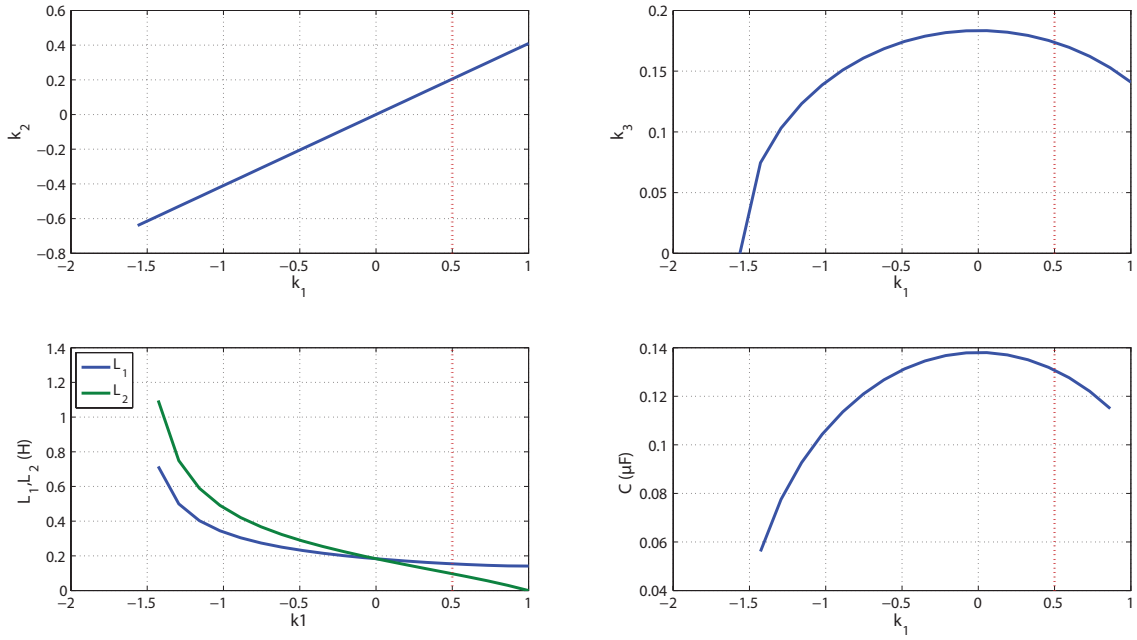


**Figure B.1.:** Plots showing parameter values for varying $k_1$

| Parameter | Value |
|---|---|
| $k_1$ | 0.5 |
| C | 0.13 $\mu$F |
| $L_1$ | 154 mH |
| $L_2$ | 96.8 mH |

**Table B.7.:** Passive component values for LCL DC/DC converter

# C. AVM Accuracy and Computation Data

## C.1. Half-Bridge MMC AVM

| Time-step ($\mu$s) | $I_{AC}$ (%) | $I_{DC}$ (%) | $V_{DC}$ (%) |
|---|---|---|---|
| 1 | 1.597 | 0.691 | 2.083 |
| 5 | 1.587 | 0.727 | 1.911 |
| 10 | 1.569 | 0.850 | 1.697 |
| 20 | 1.572 | 1.092 | 1.732 |
| 50 | 1.702 | 1.820 | 1.398 |
| 100 | 2.378 | 3.125 | 15.664 |
| 150 | 12.99 | 13.00 | 62.785 |
| 200 | 21.880 | 21.699 | 108.209 |

**Table C.1.:** Percentage difference data

| Time-step ($\mu$s) | FSM (s) | AVM (s) | Improvement (FSM/AVM) |
|---|---|---|---|
| 1 | 676.10 | 204.93 | 3.30 |
| 5 | 167.66 | 44.22 | 3.79 |
| 10 | 102.28 | 23.49 | 4.35 |
| 20 | 70.90 | 13.30 | 5.33 |
| 30 | 60.25 | 10.00 | 6.03 |
| 40 | 68.52 | 8.82 | 7.77 |
| 50 | 96.42 | 7.43 | 12.98 |

**Table C.2.:** Computation time comparison

## C.2. Alternate Arm Converter AVM

| Time-step ($\mu$s) | $I_{AC}$ (%) | $I_{DC}$ (%) | $V_{DC}$ (%) |
|---|---|---|---|
| 1 | 0.65 | 0.39 | 0.05 |
| 5 | 0.72 | 0.65 | 0.05 |
| 10 | 0.94 | 1.00 | 0.06 |
| 20 | 1.49 | 1.81 | 0.07 |
| 40 | 2.63 | 2.56 | 0.07 |
| 50 | 3.26 | 3.31 | 0.08 |

**Table C.3.:** Percentage difference data

| Time-step ($\mu$s) | FSM (s) | AVM (s) | Improvement (FSM/AVM) |
|---|---|---|---|
| 1 | 398.28 | 88.16 | 4.52 |
| 5 | 153.16 | 15.22 | 10.07 |
| 10 | 91.11 | 8.98 | 10.14 |
| 20 | 70.02 | 5.86 | 11.95 |
| 50 | 72.97 | 4.07 | 17.93 |

**Table C.4.:** Computation time comparison

# D. Wind Energy Calculations

The wind energy was calculated using a Weibull probability density function assuming Rayleigh statistics which provides a good first order approximation to a wind regime. The use of Rayleigh statistics results in a shape parameter, $k$, value of 2 and this gives a relationship between the scale parameter, $c$, and the average wind speed, $v_{wind_{AVG}}$, which is defined in (D.1).

$$c = \frac{2}{\sqrt{\pi}} v_{wind_{AVG}} \tag{D.1}$$

For the North Sea the average wind speed is approximately 10 ms$^{-1}$, and this gives a $c$ value of 11.28 [136].

The equation for the Weibull probability density function is given in (D.2).

$$f(v_{wind}) = \frac{k}{c}\left(\frac{v_{wind}}{c}\right)^{k-1} e^{-\left(\frac{v_{wind}}{c}\right)^{k}} \tag{D.2}$$

Inputting a wind speed range of 0 to 28 ms$^{-1}$ into (D.2) produces the probability density function shown in Figure D.1.

Using this curve the expected energy supplied for an offshore wind farm can be determined. A 6 MW wind turbine was assumed, resulting in the 1200 MW development requiring 200 wind turbines. The Siemens 6 MW offshore wind turbine was considered and the key parameters used in this calculation are provided in Table D.1 from [137].

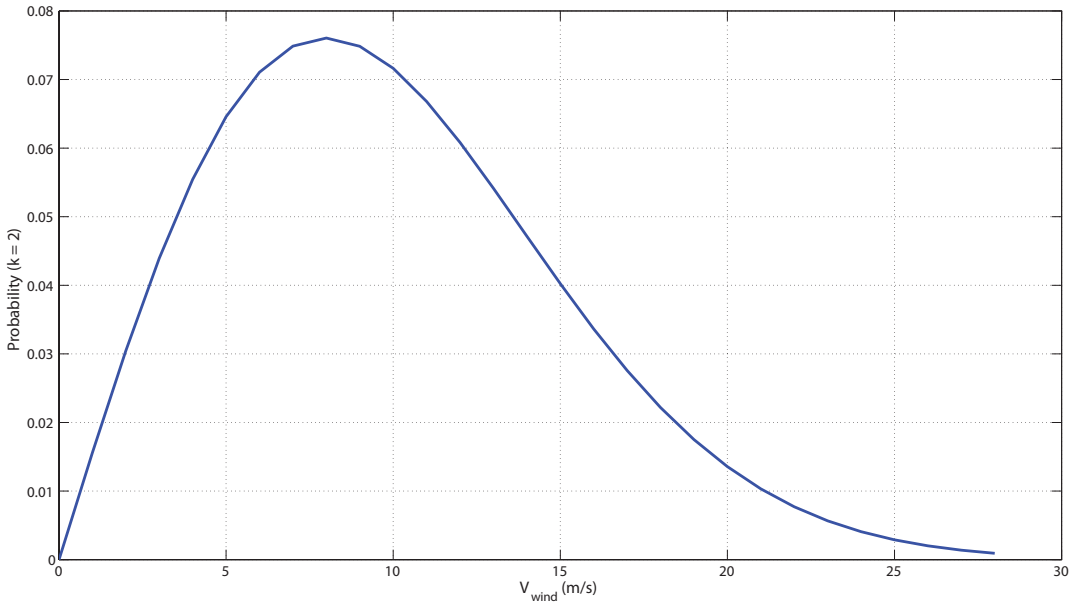


**Figure D.1.:** Probability versus wind speed

| Parameter | Value |
|---|---|
| Swept area | 18,600 $m^2$ |
| Cut in speed | 3-5 $ms^{-1}$ |
| Cut out speed | 25 $ms^{-1}$ |
| Nominal power at | 12-14 $ms^{-1}$ |

**Table D.1.:** 6 MW offshore wind turbine parameters

Using this data the expected hours and expected energy supplied for each wind speed can be determined. The expected hours for each wind speed is determined by simply multiplying the probability by the number of hours in the year. To determine the energy supplied the maximum power for each wind speed is calculated, using (D.3), and a limit of 6 MW is applied for wind speeds of 12 $ms^{-1}$ and higher. The density of air, $\rho_{air}$, was assumed to be 1.225 $kgm^{-3}$, and a power coefficient, $C_P$, of 0.47 was used.

$$P_{wind} = \frac{1}{2}\rho_{air} C_P A v_{wind}^3 \tag{D.3}$$

These calculations were done for a 1 year case shown in Figure D.2. The sum of

the energy gives a yearly energy output of the wind farm of approximately 6.4 $\times$ $10^6$ MWh, and for a project of 25 years the expected energy is 160 $\times$ $10^6$ MWh.

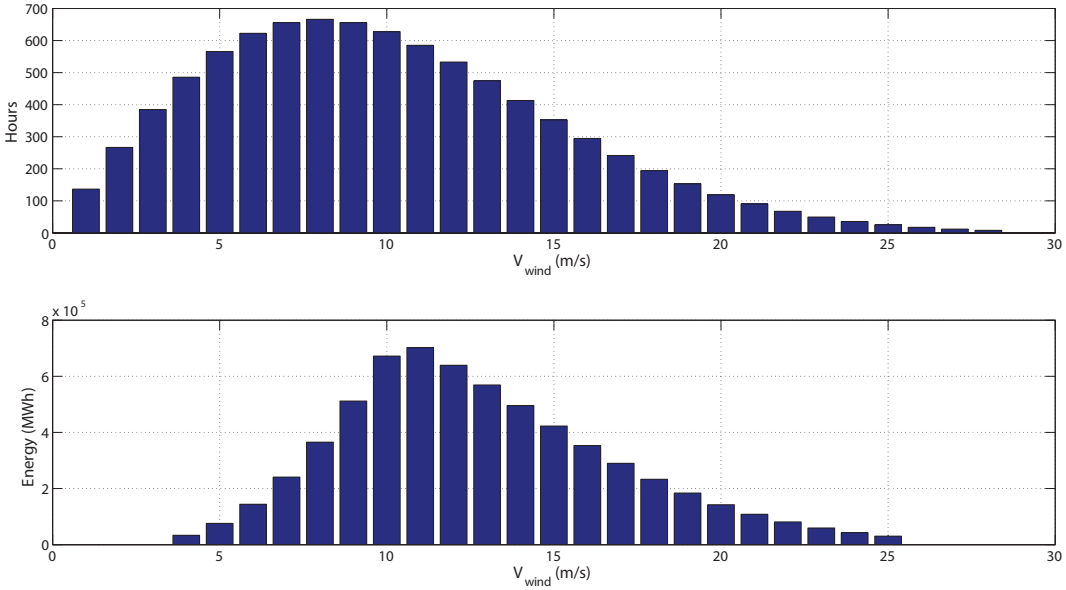


**Figure D.2.:** 1 year case of hours and energy per wind speed

This process was repeated for the MTTR case, which has a duration of 65 days (1560 hours) rather than a year, for a cable outage. The energy had to be strictly curtailed at the rated power wind speed of 12 $ms^{-1}$, as the cable is limited to supplying maximum of 1200 MW from both wind farms. Figure D.3 shows the results of these calculations.

The sum of the additional energy supplied during the repair time was found to be approximately 4.9 $\times$ $10^5$ MWh

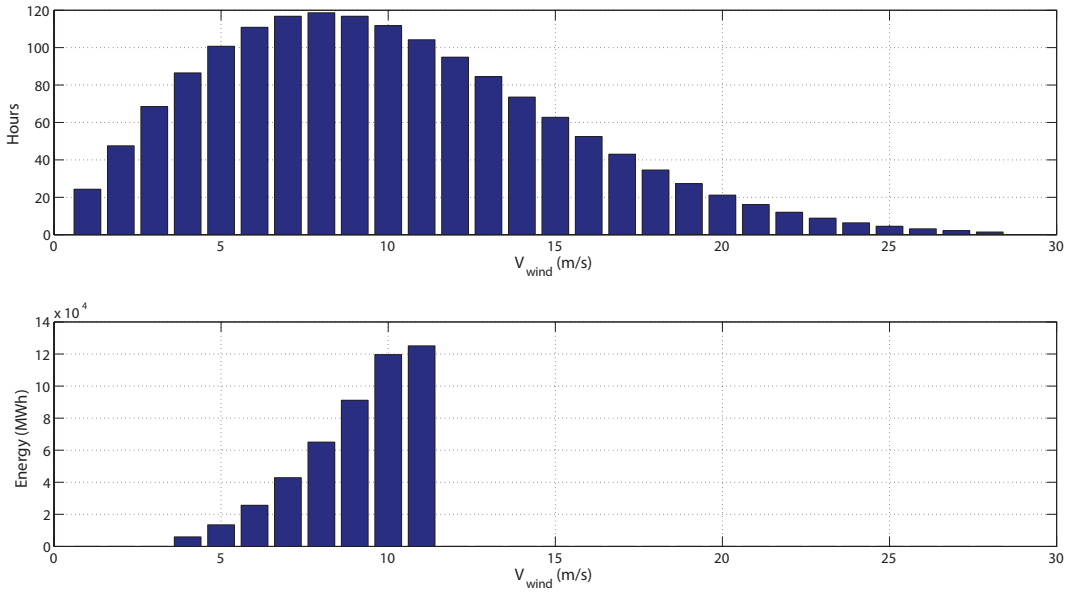


**Figure D.3.:** MTTR case of hours and energy per wind speed