Design and Development of a Class EF_2 Inverter and Rectifier for Multimegahertz Wireless Power Transfer Systems

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***Abstract*—This paper presents the design and implementation of a Class EF_2 inverter and Class EF_2 rectifier for two -W wireless power transfer (WPT) systems, one operating at 6.78 MHz and the other at 27.12 MHz. It will be shown that the Class EF_2 circuits can be designed to have beneficial features for WPT applications such as reduced second-harmonic component and lower total harmonic distortion, higher power-output capability, reduction in magnetic core requirements and operation at higher frequencies in rectification compared to other circuit topologies. A model will first be presented to analyze the circuits and to derive values of its components to achieve optimum switching operation. Additional analysis regarding harmonic content, magnetic core requirements and open-circuit protection will also be performed. The design and implementation process of the two Class-EF_2-based WPT systems will be discussed and compared to an equivalent Class-E-based WPT system. Experimental results will be provided to confirm validity of the analysis. A dc–dc efficiency of 75% was achieved with Class-EF_2-based systems.**

***Index Terms*—Class-EF inverters, class-EF rectifiers, wireless power transfer (WPT).**

I. Introduction

THE research in the wireless power transfer (WPT) field covers a wide range of topics and areas such as circuit topologies, device technologies and component packaging, coils and magnetic designs, control and system optimization methods, tuning and impedance matching techniques, development of accurate simulation models, and compliance with EMI regulations. One of the key interests in WPT technology is to increase the frequency of operation from the kilohertz range to the megahertz range to improve the tolerance to misalignment by allowing ferrite cores to be removed. A higher frequency also increases the reflected resistance seen by the primary coil driver, therefore, power can be transferred at reduced current stresses. Similar to switched-mode power supplies, the additional benefits of operating at multimegahertz switching frequencies such as the ISM bands 6.78, 13.56, and 27.12 MHz are reduction in the values of the passive components, increased power density, improved performance and transient response, and lower coupling with nearby objects and devices.

Increasing the frequency of operation imposes additional challenges on the design and construction of the inverters that drive the wireless power link and the rectifiers that deliver the power to the load. At the circuit level, some of the challenges that are encountered when increasing the switching frequency of the inverters and rectifiers are the higher switching losses, increased difficulty in designing and laying out the printed circuit boards, the limited choice of the available of device technologies, and the reduced accuracies of measurement due to constraints on instrumentation.

The Class-D and Class-E topologies are two of the most common topologies that are employed in inductive and capacitive WPT systems [1]–[6]. The Class-D topology has been widely used in wireless charging solutions at frequencies up to 6.78 MHz and as RF sources at frequencies up to 13.56 MHz. Class-D circuits have a simple principle of operation and can be easily designed, they can deliver power efficiently over a wide load range and are tolerant to any variations or perturbations that may occur while the WPT system is operating. Class-D circuits, however, may become less efficient as switching frequencies increase. This is because the device parasitics become more significant and impact the performance of the circuit, the generation of the switching signals and their associate timings become more difficult to implement and control, and in addition, there is increased complexity in driving the high-side switch for the voltage-driven Class-D circuits.

Class-E circuits have a complex principle of operation and are not straightforward to design and implement, however, they can deliver more power for a given input voltage and load than Class-D circuits and at a higher efficiency for high-frequency applications. Class-E circuits can be designed to achieve zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZDS), which makes them operate efficiently at switching frequencies in the range of tens of megahertz. They are also less affected by the aforementioned factors that the limit Class-D circuits. They consist of a single low-side switch that can be easily driven and device parasitics, such as the output capacitance, are absorbed by the load network. However, Class-E circuits are tuned to operate at optimum switching conditions only for a fixed load impedance, therefore, in a WPT system they are less tolerant than Class-D circuits to variations in the reflected impedance, which occurs when load or the distance between the coils are changed. Another issue with Class-E inverter is

Manuscript received September 30, 2015; revised January 4, 2016; accepted January 18, 2016. Date of publication March 31, 2016; date of current version July 8, 2016. This work was supported by in part by Drayson Technologies Ltd., in part by EPSRC U.K. China Smart Grids and Electric Vehicles under Grant EP/L00089X/1, and in part by EPSRC Underpinning Power Electronics 2012: Components Theme under Grant EP/K034804/1. Recommended for publication by Associate Editor S. Y. (Ron) Hui.

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Digital Object Identifier 10.1109/TPEL.2016.2521060

that the maximum voltage developed across its switch is usually between 3.5 to 4 times the input voltage. This large voltage can be problematic, especially at higher switching frequencies and at low resistance loads, as it causes the switch's nonconstant output capacitance to vary significantly with the operating voltage, and thus, the Class-E inverter will have a different switching behavior depending on the dc input voltage [7].

It has been shown in [8]–[13] that the voltage stress across the switch in the Class-E inverter, in particular the circuit configuration introduced by Sokal and Sokal [14], can be reduced to 2–2.5 times the input voltage by connecting a series LC network, tuned to the second harmonic of the switching frequency, in parallel with the switch. The method of adding resonant networks in parallel with the switch is used in Class-F^{-1} inverter circuits and rectifiers [15], consequently the Class-E topology with this added LC network is referred to as the Class-EF_2 topology. The reduced voltage stresses in the Class-EF_2 topology means that the circuit can be designed at a higher operating dc voltage, which reduces the variation in the switch's nonlinear output capacitance as shown in [8]. Another benefit of the Class-EF_2 topology is that the switch's drain voltage and the output load current does not contain a second-harmonic component, and therefore, has an improved EMI performance, whereas the Class-E topology contains a strong second-harmonic component, which may make it more difficult to meet EMI regulations.

It is known that link efficiency of an inductive-based WPT system can be maximized when the secondary coil is either series or parallel tuned to resonate at the fundamental frequency and the current drawn by the load is sinusoidal [4], [16]. It also know that parallel resonance allows for the parasitic capacitance of the secondary coil to be absorbed by the added parallel capacitor, thus using parallel resonance is beneficial especially when operating at higher frequencies since the effect of parasitic capacitance becomes more significant [16]. Since most loads in WPT are dc loads a resonant rectifier is required to convert the high frequency ac voltage induced the secondary coil to a dc voltage. A resonant rectifier that draws a sinusoidal current is preferable since it simplifies tuning the inductive link for maximum efficiency. The work on resonant rectification in high-frequency applications dates back to 1979 [15], and Class-E rectifiers were introduced afterwards for dc/dc conversion [17]. Various configurations of the Class-E rectifier were also introduced in [18]. A particular Class-E rectifier configuration that is of interest in WPT is the voltage-driven Class-E resonant low dv/dt rectifier introduced in [18] and analyzed in detail in [6] and[19]. This rectifier configuration consists of a single diode, a shunt capacitor, and an inductor at its terminal. The inductor and capacitor are tuned to resonate at the fundamental frequency. This configuration is directly compatible with parallel resonant secondary coils as it is voltage driven, draws a near sinusoidal current, its diode's junction is absorbed into the shunt capacitor and any leakage and parasitic inductances are also absorbed by the inductor. Due to these features, this configuration has been used in kilohertz and multimegahertz WPT systems with parallel resonant secondary coils at power levels and rectification efficiencies exceeding 100 W and 90%, respectively, [6], [20]–[22].

It has been found in previous work that the voltage-driven Class-E resonant low dv/dt rectifier configuration can require a relatively large inductance at its input terminals for multimegahertz operation. This inductance is usually in the order of several microhenrys and is usually constructed using magnetic cores. Air core inductors can be used, however, they will be physically large to get the required inductance and quality factors, and therefore, can be impractical. As a result, the inductor can contribute to the majority of the losses in the circuit, especially when operating at frequencies in the megahertz range due to the losses associated with magnetic cores. In addition, the circulating dc current in the rectifier can cause the magnetic core to saturate, and therefore, the power that it can handle is limited.

This paper will present a Class-EF_2 inverter and a Class-EF_2 rectifier for two inductive-based 25-W parallel tuned secondary WPT systems that operate at 6.78 and 27.12 MHz, respectively. In Section II, a model will be presented and will be used to analyze the Class-EF_2 inverter and rectifier circuits. The maximum power-output capability and the voltage and current stresses in addition to the harmonic content will be investigated. Section V will describe the design and implementation process of the experimental setup of the Class-EF_2-based WPT systems, and component values and performance parameters will be compared to equivalent Class-E-based WPT systems. Section VI presents experimental results confirm the accuracy of the analysis and the design of the Class-EF_2 circuits. Finally, a summary and conclusions are given in Section VII. It will be shown that the Class-EF_2 inverter results in an improved efficiency due to its lower current stresses and achieves a lower THD than the Class-E inverter. It will also be shown that the Class-EF_2 rectifier can be constructed using physically smaller air core inductors since it can be designed with a lower input inductance, and can deliver power to a load at a lower diode voltage stress.

II. Modeling and Analysis

The Class-EF_2 inverter circuit and the Class-EF_2 rectifier circuit are shown in Fig. 1. In both circuits, inductor L_2 and capacitor C_2 are the added series LC network, which is tuned to resonate at the second harmonic of the circuits' switching frequency. Both circuits are the dual of each other, that is the inverter circuit takes an input dc voltage ($V_{\rm IN}$) and outputs an ac current (I_o), and the rectifier circuit takes an input ac current ($I_{\rm IN}$) and rectifies it into an output dc voltage (V_o). The equivalent circuit shown in Fig. 2 can be used to represent both inverter and rectifier circuits. The voltage and current notations references for inversion and rectification are described Table I, and the switch S is either a MOSFET for inversion or a diode for rectification. The equivalent circuit for analysis was defined based on the following assumptions:

1) In inversion, the transistor and its body diode form an ideal switch whose ON resistance is zero, OFF resistance is infinity, and switching times are zero. Similarly in rectification, the diode is an ideal switch whose ON resistance is zero, forward voltage drop is zero, OFF resistance is infinity, and reverse-recovery time is zero.

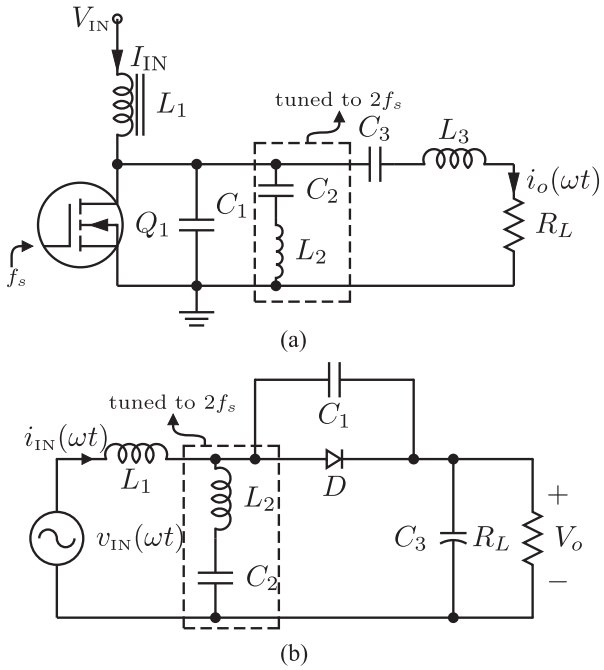

Fig. 1. Circuit diagrams of the Class-EF$_2$ inverter and rectifier.

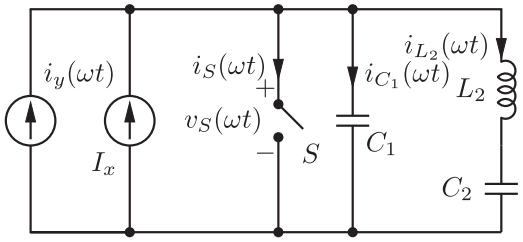

Fig. 2. Class-EF$_2$ equivalent circuit for inversion and rectification.

TABLE I
DESCRIPTION OF THE VOLTAGE AND CURRENT ANNOTATIONS

	Inversion	Rectification
S	MOSFET	Diode
V_x	Input dc voltage ($V_{\rm IN}$)	Output dc voltage (V_o)
I_x	Input dc current ($I_{\rm IN}$)	Output dc current (I_o)
i_y	Output ac current (i_o)	Input ac current ($i_{\rm IN}$)
v_s	Drain voltage ($v_{\rm DS}$)	Anode voltage (v_D)
i_s	Drain current ($i_{\rm DS}$)	Anode current (i_D)

2) In inversion, inductance L_1 is high enough such that the input current $I_{\rm IN}$ is a dc current. In rectification inductance, L_1 is high enough such that the input ac current i_y is sinusoidal with a frequency equal to the switching frequency.
3) In inversion, the loaded quality factor of the $L_3C_3R_L$ branch is high enough such that the output current i_y through it is sinusoidal with a frequency equal to the switching frequency. In rectification, the filter capacitance C_3 is high enough such that the output voltage is a dc voltage and the output current is dc current.
4) In inversion and rectification, the shunt capacitance C_1 is assumed to be constant and independent of its voltage and absorbs the output capacitance of the transistor and the diode in inversion and rectification, respectively.
5) There are no losses in the circuits, all the power supplied by the sources is delivered to the load R_L.

The current i_y is sinusoidal and is given by

$$i_y(\omega t) = I_m \sin(\omega t + \phi) \tag{1}$$

where I_m is the output current's magnitude and ϕ is its phase. It is assumed that switch is ON for the period $0 \le \omega t < 2\pi D$ and OFF for the period $2\pi D \le \omega t < 2\pi$. Beginning with the ON period, the switch's voltage and the current in capacitor C_1 are zero. By applying the KCL at the switch's drain node, the current in the switch is

$$i_S(\omega t) = I_x - i_{L_2}(\omega t) - i_y(\omega t), \text{ for } 0 \le \omega t < 2\pi D. \tag{2}$$

Since the switch is ON, the total voltage across the series tuned L_2C_2 network is zero. The L_2C_2 network now is a source-free undamped circuit and its current (i_{L_2}) normalized with to the dc current (I_x) is given by

$$\frac{i_{L_2}}{I_x}(\omega t) = A_1 \cos(2\omega t) + B_1 \sin(2\omega t). \tag{3}$$

The coefficients A_1 and B_1 are to be determined based on equation's boundary conditions.

For the period $2\pi D \le \omega t < 2\pi$, the switch is turned OFF, therefore, $i_S(\omega t) = 0$. By applying the KCL at the drain node, the current in the series tuned L_2C_2 network is

$$\begin{aligned} i_{L_2}(\omega t) &= I_x - i_y(\omega t) - i_{C_1}(\omega t) \\ &= I_x - I_m \sin(\omega t + \phi) - \omega C_1 \frac{dv_s(\omega t)}{d\omega t}. \end{aligned} \tag{4}$$

The switch's voltage is equal to the total voltage across the L_2C_2 network and is given by

$$\begin{aligned} v_S(\omega t) = {} & \omega L_2 \frac{di_{L_2}(\omega t)}{d\omega t} \\ & + \frac{1}{\omega C_2} \int_{2\pi D}^{\omega t} i_{L_2}(\omega t) d\omega t + v_{C_2}(2\pi D). \end{aligned} \tag{5}$$

Differentiating the aforementioned equation gives

$$\frac{dv_s(\omega t)}{d\omega t} = \omega L_2 \frac{d^2 i_{L_2}(\omega t)}{d\omega t^2} + \frac{1}{\omega C_2} i_{L_2}(\omega t). \tag{6}$$

Substituting (6) into (4) and normalizing with respect to the current I_x gives

$$\begin{aligned} \frac{i_{L_2}}{I_x}(\omega t) = {} & 1 - \frac{I_m}{I_x} \sin(\omega t + \phi) \\ & - \omega^2 L_2 C_1 \frac{\frac{d^2 i_{L_2}}{I_x}(\omega t)}{d\omega t^2} - \frac{C_1}{C_2} \frac{i_{L_2}}{I_x}(\omega t). \end{aligned} \tag{7}$$

The aforementioned equation is a linear nonhomogeneous second-order differential equation, which has the following

general solution:

$$\frac{i_{L_2}}{I_x}(\omega t) = A_2\cos(q_2\omega t) + B_2\sin(q_2\omega t) - \frac{q_2^2 p}{q_2^2-1}\sin(\omega t+\phi) + \frac{1}{k+1} \tag{8}$$

where

$$k = \frac{C_1}{C_2} \tag{9}$$

$$q_2 = \frac{1}{\omega}\sqrt{\frac{C_1+C_2}{L_2C_1C_2}} = 2\sqrt{\frac{k+1}{k}} \tag{10}$$

$$p = \frac{C_2}{C_1+C_2}\frac{I_m}{I_x} = \frac{1}{k+1}\frac{I_m}{I_x} \tag{11}$$

and the coefficients A_2 and B_2 are to be determined based on the equation's boundary conditions. The boundary conditions are determined from the current and voltage continuity conditions when the switch turns ON and OFF, which can be described by

$$i_{L_2}(2\pi D^-) = i_{L_2}(2\pi D^+) \tag{12}$$

$$i_{L_2}(0) = i_{L_2}(2\pi) \tag{13}$$

$$\left.\frac{di_{L_2}(\omega t)}{d\omega t}\right|_{\omega t=2\pi D^-} = \left.\frac{di_{L_2}(\omega t)}{d\omega t}\right|_{\omega t=2\pi D^+} \tag{14}$$

$$\left.\frac{di_{L_2}(\omega t)}{d\omega t}\right|_{\omega t=0} = \left.\frac{di_{L_2}(\omega t)}{d\omega t}\right|_{\omega t=2\pi}. \tag{15}$$

Using (9), the normalized current through capacitor C_1 for the period $2\pi D \le \omega t < 2\pi$ is

$$\frac{i_{C_1}}{I_x}(\omega t) = 1 - p(k+1)\sin(\omega t+\phi) - \frac{i_{L_2}}{I_x}(\omega t). \tag{16}$$

The drain voltage for the period $2\pi D \le \omega t < 2\pi$ is

$$v_S(\omega t) = \frac{I_x}{\omega C_1}\int_{2\pi D}^{\omega t}\frac{i_{C_1}}{I_x}(\tau)d\tau \tag{17}$$

where τ is a dummy variable. The drain voltage can also be written as

$$v_S(\omega t) = \frac{I_x}{\omega C_1}\beta(\omega t) \tag{18}$$

where

$$\beta(\omega t) = \int_{2\pi D}^{\omega t}\frac{i_{C_1}}{I_x}(\tau)d\tau. \tag{19}$$

The dc component (or average) of the drain voltage is equal to the dc voltage V_x, i.e.,

$$V_x = \frac{I_x}{2\pi\omega C_1}\int_{2\pi D}^{2\pi}\beta(\omega t)d\omega t. \tag{20}$$

By substituting (20) into (18), the normalized drain voltage with respect to the voltage V_x can be written as

$$\frac{v_S}{V_x}(\omega t) = \begin{cases} 0, & \text{for } 0 \le \omega t < 2\pi D \\ \dfrac{2\pi\beta(\omega t)}{\displaystyle\int_{2\pi D}^{2\pi}\beta(\omega t)d\omega t}, & \text{for } 2\pi D \le \omega t < 2\pi. \end{cases} \tag{21}$$

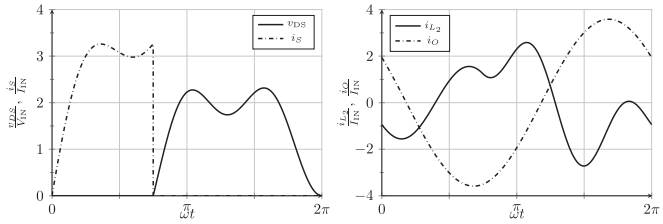

Fig. 3. Voltage and current waveforms for the Class-EF$_2$ inverter ($k = 0.867$, $D = 0.375$).

Using (11), the normalized switch current with respect to the dc current I_x can be written as

$$\frac{i_S}{I_x}(\omega t) = \begin{cases} 1 - p(k+1)\sin(\omega t+\phi) & -\big(A_1\cos(2\omega t) \\ +B_1\sin(2\omega t)\big), & \text{for } 0 \le \omega t < 2\pi D \\ 0, & \text{for } 2\pi D \le \omega t < 2\pi. \end{cases} \tag{22}$$

III. Class-EF$_2$ Inversion

A. Analysis

A detailed analysis of Class-EF$_2$ inverters has been performed in [8]. Three cases of operation were identified based on the values of the duty cycle and k: the maximum power-output capability case, the maximum frequency of operation case, and the maximum power operation case. Here, only the maximum power-output capability case will be considered since it results in the highest efficiency operation for the devices chosen here and only a summary of the analysis and results will be included.

1) Voltage and Current Waveforms: Fig. 3 shows switch's voltage and current waveforms, the current of inductor L_2 and the output current. It can be noticed that the peak voltage across the switch is about 2.3 times the input voltage, compared to 3.5 times the input voltage for that of the Class-E inverter, and the switch's current is increased to approximately 3.2 times the input current compared to 2.8 times the input current for the Class-E inverter. More specifically the peak voltage and current stresses of the Class EF$_2$ when $k = 0.867$ and $D = 0.375$ are

$$\frac{V_{\mathrm{DS\,max}}}{V_o} = 2.3162 \tag{23}$$

$$\frac{I_{\mathrm{DS\,max}}}{I_o} = 3.2632. \tag{24}$$

2) Input Resistance and Output Power: The normalized value of I_m with respect to the input dc current

$$\frac{I_m}{I_x} = \frac{I_m}{I_{\mathrm{IN}}} = \frac{2\pi(1-D) + \frac{A_1}{2}\sin(4\pi D) + \frac{2B_1}{2}\sin^2(2\pi D)}{\cos(2\pi D+\phi) - \cos\phi} \tag{25}$$

and the input dc resistance seen by the source

$$\frac{R_{\mathrm{DC}}}{R_L} = \frac{1}{2}\left(\frac{2\pi(1-D) + \frac{A_1}{2}\sin(4\pi D) + \frac{2B_1}{2}\sin^2(2\pi D)}{\cos(2\pi D+\phi) - \cos\phi}\right)^2 \tag{26}$$

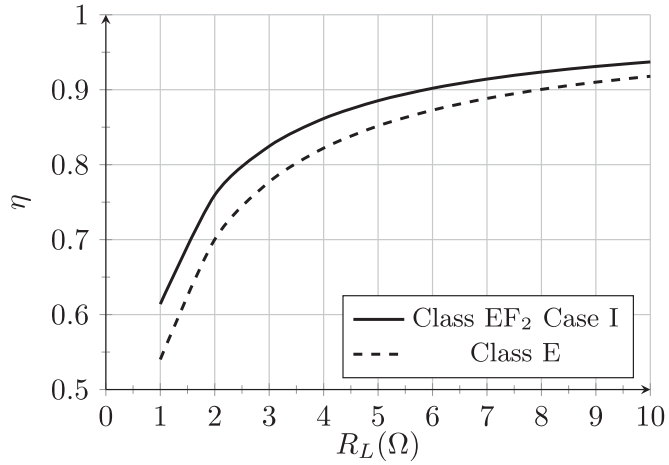

Fig. 4. Comparison between the efficiencies of the Class-EF_2 inverter operating at maximum c_p [8] and the Class-E inverter. The values of the of $r_f = 0.1\,\Omega$, $r_{\rm DS} = 0.2\,\Omega$, $r_{C_1} = 0.076\,\Omega$, $r_{L_2} + r_{C_2} = 0.1\,\Omega$, $r_{L_3} + r_{C_3} = 0.5\,\Omega$, $tf = 1.5\,$ns, and $f = 27.12\,$MHz.

where R_L here represents the reflected load of the inductive link and the rectifier. Assuming all the power supplied by the source will be consumed in the reflected load, thus

$$\begin{aligned} P_{\rm IN} &= P_o \\ V_{\rm IN} I_{\rm IN} &= \frac{1}{2} I_m^2 R_L. \end{aligned} \tag{27}$$

The normalized output power is, therefore

$$\frac{P_o R_L}{V_{\rm IN}^2} = \frac{1}{2}\left(\frac{I_m}{I_{\rm IN}}\frac{R_L}{R_{\rm DC}}\right)^2 = 0.1556. \tag{28}$$

B. Comparison With Class-E Inverter

1) Efficiency: It was shown in [8] that efficiency of the Class-EF_2 inverter when operated at the maximum power-output capability case can be higher than that of the Class-E inverter, especially with devices that have a relatively large on resistance and with high quality factor passive components. This is because for certain output power and load, the Class-EF_2 in maximum power-output capability case operates at high-voltage low-current regime, and therefore, the conduction and ohmic losses are reduced. Fig. 4 compares the drain efficiency between the Class-E inverter and the Class-EF_2 inverter and it can be noticed that the Class-EF_2 inverter has a higher overall efficiency. These efficiency plots were obtained using the mathematical expressions in [8] and [23].

2) Harmonics: The harmonic content of the drain waveform of the Class-EF_2 inverter is investigated by performing a Fourier analysis. Using (21), the Fourier components of the drain voltage are

$$A_n = \frac{1}{\pi}\int_{2\pi D}^{2\pi} \frac{v_{\rm DS}}{V_{\rm IN}}(\omega t)\sin(n\omega t + \phi) d\omega t \tag{29}$$

$$B_n = \frac{1}{\pi}\int_{2\pi D}^{2\pi} \frac{v_{\rm DS}}{V_{\rm IN}}(\omega t)\cos(n\omega t + \phi) d\omega t \tag{30}$$

$$C_n = \sqrt{a_n^2 + b_n^2}. \tag{31}$$

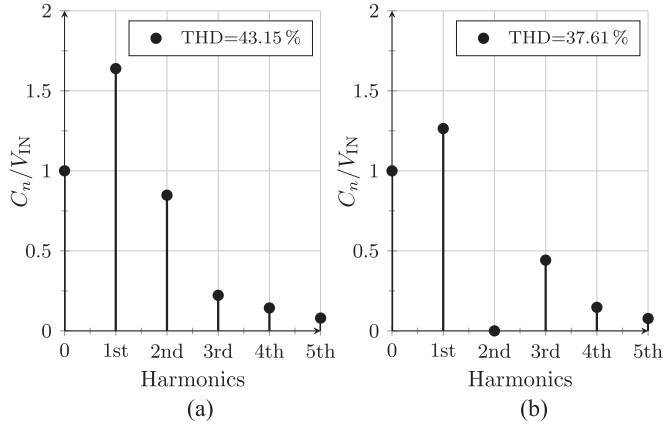

Fig. 5. Harmonic content of the switch's voltage.

The first five components are used to calculate the THD as follows as there is so little power in the higher harmonics

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{6} C_n^2}}{C_1}. \tag{32}$$

A comparison of the harmonic content in the voltage across the switch between the Class-EF_2 inverter and the Class-E inverter is shown in Fig. 5. It can be seen that the Class-E inverter has a strong second-harmonic component, which contributes significantly to the THD factor. Whereas the Class-EF_2 inverter does not contain a second-harmonic component, and therefore, has a lower THD.

IV. Class-EF_2 Rectification

A. Analysis

Similar to the inversion case, the voltage across the diode at the end of the switching period is zero, which results in the following equation:

$$\begin{aligned} 2\pi\frac{k}{k+1}(1-D) &+ p\big(\cos(2\pi D+\phi) - \cos\phi\big)\left(\frac{q_2^2}{q_2^2-1} - (k+1)\right) \\ &+ \frac{A_2}{q_2}\big(\sin(2\pi D q_2) - \sin(2\pi q_2)\big) \\ &+ \frac{B_2}{q_2}\big(\cos(2\pi q_2) - \cos(2\pi D q_2)\big) = 0. \end{aligned} \tag{33}$$

The ZDS in rectification occurs at $\omega t = 2\pi D$ ($i_{C_1}(2\pi D) = 0$, giving the following equation:

$$\begin{aligned} 1 &- A_2\cos(2\pi D q_2) - B_2\sin(2\pi D q_2) - \frac{1}{k+1} \\ &- p\sin(2\pi D+\phi)(k+1) + \frac{q_2^2 p}{q_2^2-1}\sin(2\pi D+\phi). \end{aligned} \tag{34}$$

In the analysis section of the Class-EF_2 inverter, the independent parameters were the duty cycle and k. Here, the output load current I_o and k can be set as the independent parameters since this is a rectification circuit and will most likely employ a diode rather than a synchronous switch. The duty cycle cannot be

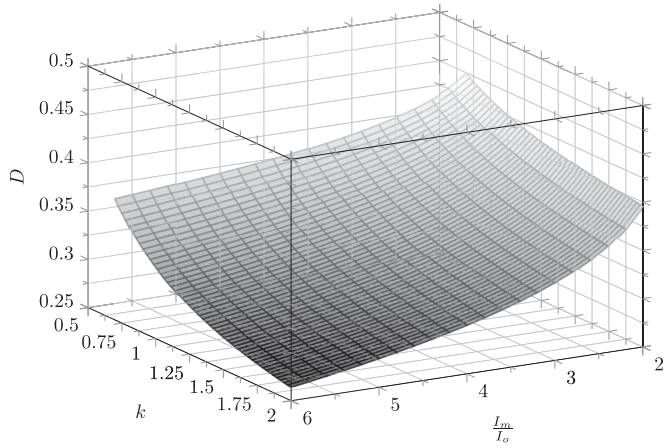

Fig. 6. Solutions of the duty cycle as a function of normalized output load current and k for the Class-EF$_2$ rectifier.

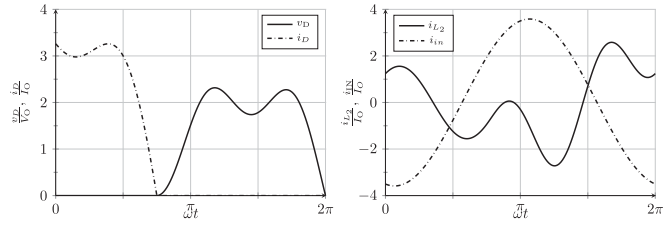

Fig. 7. Voltage and current waveforms for the Class-EF$_2$ rectifier ($k = 0.867$, $p = -1.9204$).

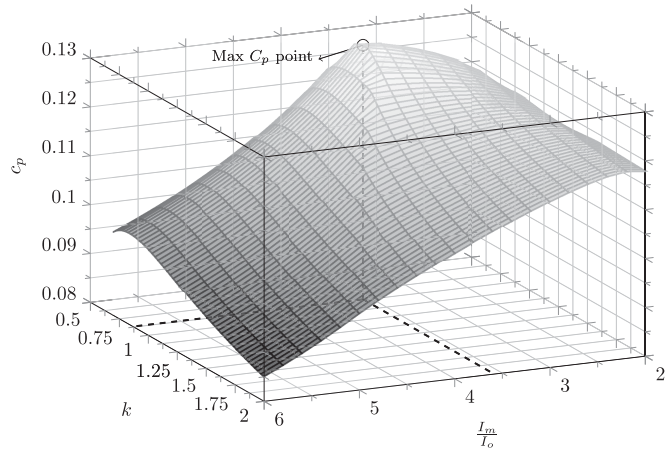

Fig. 8. Power-output capability of the Class-EF$_2$ rectifier as a function of normalized output load current and k.

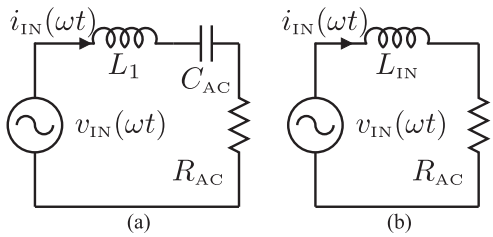

Fig. 9. Class-EF$_2$ rectifier equivalent circuit and input impedance at the fundamental switching frequency. (a) equivalent circuit seen by v_{IN} and L_1 (b) input impedance circuit

controlled will, therefore, need to be calculated. From (11), the ratio of the amplitude of input ac current I_m to the output dc current I_o can be written as

$$\frac{I_m}{I_o} = p(k+1). \tag{35}$$

This ratio approaches infinity as the load resistance decreases and approaches zero as the load resistance increases. Equations (33) and (34), in addition to (12)–(15) are now six simultaneous equations that can be solved for A_1, A_2, B_1, B_2, D, and ϕ for a given $\frac{I_m}{I_o}$ and k. Fig. 6 shows the solutions for the duty cycle D as a function of normalized load current and k.

1) Voltage and Current Waveforms: By using the numerical solutions for A_1, A_2, B_1, B_2, p, and ϕ, the voltage and current waveforms throughout the rectifier can be plotted for given values of $\frac{I_m}{I_o}$ and k. Fig. 7 shows the diode's voltage and current waveforms and the current of inductor L_2 for selected values of normalized load current and k.

2) Maximum Stresses and Power-Output Capability: The same process and equations that were used in determining the maximum voltage and current stresses for inversion can also be applied for rectification. Fig. 8 shows the variation of the power-output capability with normalized load current and k. Similar to the inversion case, the maximum c_p is 0.13231, which occurs when $k = 0.867$ and $\frac{I_m}{I_o} = 3.5853$ corresponding to the following voltage and current stresses:

$$\frac{V_{D\max}}{V_o} = 2.3162 \tag{36}$$

$$\frac{I_{D\max}}{I_o} = 3.2632. \tag{37}$$

B. Input Impedance

The input impedance of the rectifier can be calculated by first finding the equivalent circuit seen by the input voltage after inductor L_1 [see Fig. 9(a)]. Inductor L_1 can then be included with the equivalent circuit to reach the input impedance of the rectifier as shown in Fig. 9(b). The fundamental Fourier component of the diode voltage is given by

$$\begin{aligned}\frac{v_{D1}}{V_o}(\omega t) &= V_{R_{\mathrm{AC}}}\sin(\omega t+\phi) + V_{C_x}\cos(\omega t+\phi)\\ &= I_m R_{\mathrm{AC}}\sin(\omega t+\phi) + \frac{I_m}{\omega C_x}\cos(\omega t+\phi)\end{aligned} \tag{38}$$

where $V_{R_{\mathrm{AC}}}$ and $V_{C_{\mathrm{AC}}}$ are the Fourier coefficients, which are also the magnitudes of the voltages across the equivalent ac resistance (R_{AC}) and the equivalent ac capacitance (C_{AC}) of the rectifier, respectively. Using (11), the voltage magnitudes

TABLE II
EQUIVALENT IMPEDANCE OF THE CLASS-EF_2 RECTIFIER AT EACH HARMONIC

Harmonic	$\frac{R_{AC}}{R_L}$	$\frac{C_{AC}}{C_1}$
1	0.1556	3.7293
2	0	∞
3	0	14.7787
4	0	41.0689
5	0	10280

are equal to

$$p(k+1)R_{\rm AC} = \frac{1}{\pi}\int_{2\pi D}^{2\pi}\frac{v_{\rm DS}}{V_{\rm IN}}(\omega t)\sin(\omega t+\phi)d\omega t \quad (39)$$

$$\frac{p(k+1)}{\omega C_{\rm AC}} = -\frac{1}{\pi}\int_{2\pi D}^{2\pi}\frac{v_{\rm DS}}{V_{\rm IN}}(\omega t)\cos(\omega t+\phi)d\omega t. \quad (40)$$

Using the solutions for operation at maximum c_p ($k = 0.867$ and $\frac{I_m}{I_o} = 3.5853$), the ratios of the input resistance to the load resistance and equivalent capacitance $C_{\rm AC}$ to capacitor C_1 are

$$\frac{R_{\rm AC}}{R_L} = 0.1556 \quad (41)$$

$$\frac{C_{\rm AC}}{C_1} = 3.7293. \quad (42)$$

Following the process to calculate the normalized value of C_1 for the inverter case, the normalized value of C_1 for the Class-EF_2 rectifier is

$$\frac{1}{\omega R_L C_1} = 1.1801. \quad (43)$$

The value of inductor L_1 should be large in order to ensure the input current is near sinusoidal with minimal harmonics. A suitable inductance value of this can be deduced by calculating the equivalent impedance in Fig. 9 at each harmonic. Table II list the values of the $R_{\rm AC}$ and $C_{\rm AC}$ for the first five harmonics. The input voltage $V_{\rm IN}$ is sinusoidal and only delivers power at the fundamental frequency, therefore, the input resistance is zero at each harmonic, whereas the value of $C_{\rm AC}$ for higher harmonics becomes increasingly capacitive. Consequently, the rectifier circuit needs to appear inductive to the input voltage at each harmonic to ensure a near sinusoidal input current. In order to create a design process similar to that of the Class-E rectifier in [19], the value of L_1 can be set to resonate with C_1 at the fundamental switching frequency, i.e.,

$$L_1 = \frac{1}{\omega_o^2 C_1}. \quad (44)$$

With this value of inductance, the resonant frequency of the complete circuit (ω_r) is

$$\omega_r = \frac{1}{\sqrt{L_1 C_{\rm AC}}} = 0.5178\omega_o \quad (45)$$

and the rectifier circuit is now highly inductive at each harmonic. The input impedance at the fundamental frequency is

$$Z_{\rm IN} = R_{\rm AC} + j\frac{1}{\omega C_1}\left(1 - \frac{C_1}{C_{\rm AC}}\right) = R_{\rm AC} + j\omega L_{\rm IN} \quad (46)$$

where $L_{\rm IN}$ is now the equivalent input inductance. Using (44), the ratio of the input inductance to L_1 is

$$\frac{L_{\rm IN}}{L_1} = 1 - \frac{C_1}{C_{\rm AC}} = 0.7319. \quad (47)$$

C. No-Load Protection

In a real-world application, the WPT system is expected to function if no load was connected to the rectifier. In the Class-E resonant low dv/dt rectifier, the maximum output dc voltage and the maximum voltage across the diode are expected to increase indefinitely since the rectifier circuit resonates at the switching frequency. The voltages will continue to increase until either the maximum blocking voltage of the diode or the maximum rated voltage of the dc filter capacitor are reached at which then the rectifier fails. It should be noted that nonresonant voltage-driven Class-E rectifiers do not have this issue.

Also, the Class-EF_2 rectifier presented here is immune to this issue since the circuit is not resonant at the switching frequency according to (45). The maximum voltage across the diode for the Class-EF_2 rectifier during an open circuit (assuming L_1 is resonant with C_1 at the fundamental switching frequency) is

$$V_{D\,\max} = |v_{\rm IN}|\frac{3k}{2} \quad (48)$$

and the maximum output voltage across the filter capacitor is

$$V_{o\,\max} = |v_{\rm IN}|\frac{3k}{4}. \quad (49)$$

V. SUMMARY AND DESIGN

A. Summary of Design Equations

Table III summarizes all the design equations and parameters for maximum c_p operation for the Class-EF_2 inverter and the Class-EF_2 rectifier, respectively, in comparison with the Class-E inverter and the Class-E resonant low dv/dt rectifier.

B. Class-EF_2 Inverter and Inductive Link Design

This section will describe the design of two Class-EF_2 inverters to drive the primary coil of an inductive WPT system at 6.78 and 27.12 MHz, respectively. The maximum power that the inverters will operate at is 25 W.

In our previous work [8], we explained in detail the design process of a Class-EF_2 inverter that was required to deliver up to 25 W to a 5-Ω resistive load at 6.78 MHz. It was also shown that the efficiency of the Class-EF_2 inverter was about 3% higher than when operated as a Class-E inverter. Usually the inverter is designed to drive the inductive link of a specific WPT system with known parameters such as the Q factors of the coils and the coupling coefficient. To simplify the design and implementation process, the approach that will be taken here is to create an inductive link that will reflect a load of 5 Ω to the Class-EF_2 inverter that was implemented back in our previous work. Beginning with the 6.78-MHz WPT system, the primary coil of its inductive link system was formed using two turns of a multistrand eight AWG copper wire and had a diameter of 18 cm, its inductance was measured to be 1.45 μH at 6.78 MHz. The

TABLE III
SUMMARY OF ALL DESIGN EQUATIONS AND PERFORMANCE PARAMETERS FOR THE CLASS-EF$_2$ INVERTER AND THE CLASS-EF$_2$ RECTIFIER

	Inversion		Rectification	
Parameter	Class EF$_2$	Class E	Class EF$_2$	Class E
D	0.375	0.500	0.375	0.500
k	0.867	-	0.867	-
q_2	2.935	-	2.935	-
$\frac{L_m}{I_x}$	3.5853	1.8623	3.5853	1.8623
$\frac{1}{\omega R_L C_1}$	7.5851	5.4466	1.1813	2.5747
$\frac{1}{\omega R_L C_2}$	6.5762	-	1.3625	-
$\frac{\omega L_3}{R_L} - \frac{1}{\omega C_3}$	2.0339	1.1525	-	-
$\frac{f L_{1\min}}{R_L}$	24.1024	8.6685	0.1880	0.4098
$\frac{R_{\rm IN}}{R_L}$ (series)	6.4273	1.7337	0.1556	0.5358
$\frac{L_{\rm IN}}{L_1}$ (series)	0	0	0.7319	0.7431
$\frac{R_{\rm IN}}{R_L}$ (parallel)	6.4273	1.7337	4.9597	7.3669
$\frac{L_{\rm IN}}{L_1}$ (parallel)	0	0	0.7556	0.8014
c_p	0.1323	0.0981	0.1323	0.0981
$\frac{P_o R_L}{V_{\rm IN}^2}$	0.1556	0.5768	265.46	6.0404
$\frac{v_S}{V_x}\max$	2.3162	3.5620	2.3162	3.5620
$\frac{i_S}{I_x}\max$	3.2632	2.8620	3.2632	2.8620

TABLE IV
IMPLEMENTED COMPONENT VALUES OF THE 6.78 AND 27.12-MHZ CLASS-EF$_2$ INVERTERS

Component	Class-EF$_2$ Inv. (6.78 MHz)	Class-EF$_2$ Inv. (27.12 MHz)	Description (6.78 MHz/27.12 MHz)
C_1 (pF)	$260 + C_o$	$40 + C_o$	AVX NP0 MLC capacitors
C_o (pF)	80 pF	60 pF	MOSFET output capacitance at $V_{\rm IN}$
C_2 (pF)	667	120	Murata GQM series capacitors
C_3 (pF)	500	46	AVX NP0 MLC capacitors
L_1 (μH)	22	22	Wurth Elektronik WE-PD
L_2 (nH)	215	66	Coilcraft 2014VS
L_3 (L_p) (μH)	1.45	0.36	2/1 turn, 8 AWG, 18 cm diam.
R_L (Ω)	5.00	7.00	reflected resistance
$V_{\rm IN}$ (V)	5-35	10-40	-
Q_1	Fairchild FDMC86116LZ (100 V, 7.5 A) MOSFET		

secondary coil was formed with the same copper wire and had a diameter of 13.5 cm and consisted of two turns, its inductance was measured to be 1.10 μH at 6.78 MHz. After connecting the Class-EF$_2$ rectifier, which its design process will be explained in the next section, to the secondary coil, the desired reflected resistance of 5 Ω was then achieved by varying the distance between the coils while observing the MOSFET's drain voltage until the Class-EF$_2$ voltage waveforms were realized. Table IV lists the values of the components of the Class-EF$_2$ inverter for operation at 6.78 MHz. The separation distances between the coils were 8 and 12 cm for the 6.78- and 27.12-MHz systems, respectively.

For the 27.12-MHz WPT system, the primary coil of the inductive link had the same dimensions of that of the 6.78-MHz WPT system, however, it only consisted of a single turn. Initial

TABLE V
IMPLEMENTED COMPONENT VALUES OF THE 6.78- AND 27.12-MHZ CLASS-EF$_2$ RECTIFIERS

Component	Class-EF$_2$ Rec. (6.78 MHz)	Class-EF$_2$ Rec. (27.12 MHz)	Description (6.78 MHz/27.12 MHz)
L_1 (μH)	4	1	21 turns, 16 AWG, T106-2 core/ four Coilcraft 2014VS 255 nH
L_2 (nH)	870	215	21 turns, 16 AWG, T106-2 core/ Coilcraft 2014VS 215 nH
C_1 (pF)	128 + C_o	25 +C_o	Murata GQM series capacitors
C_o (pF)	9	9	Diode junction capacitance at $V_{\rm IN}$
C_2 (pF)	158.2	39.56	AVX NP0 MLC capacitors
R_L (Ω)	145	145	Vishay thick film 25 W resistors
V_o (V)	up to 60	up to 60	-

experiments did not achieve the desired results when using two turns due to the excessive ESR and the large stray capacitances. The primary coil was then reduced to a single turn, which had an inductance of 0.36 μH. The secondary coil, however, had the same dimensions and number of turns of that of the 6.78-MHz system. The inverter here was designed to operate at a reflected load of 7 Ω instead of 5 Ω to reduce the output current in order to decrease the higher ohmic losses. Table IV lists the values of the components of the Class-EF$_2$ inverter for operation at 27.12 MHz.

The MOSFETs used for both Class-EF$_2$ inverters was the FDMC86116LZ (100 V, 7.5 A) MOSFET from Fairchild, which was driven by the ISL55111 MOSFET Driver from Intersil. The switching signals for both circuits were derived from crystal oscillators running at 6.78 and 27.12 MHz, respectively, and a logic circuit was implemented to adjust their duty cycles.

C. Class-EF$_2$ Rectifier Design

This section will describe the design and implementation process of two Class-EF$_2$ rectifiers to convert the ac voltage induced at the secondary coil to a dc voltage. The output power that they should be able to deliver to a 145-Ω resistive load is up to 25 W at a dc voltage of 60 V.

Beginning with the 6.78-MHz WPT system, the first step is determine which diode to use. From Table III, the maximum voltage and current that will be developed across the diode is approximately 140 V and 1.35 A, respectively, and the value of the shunt capacitance C_1 is 137.2 pF. With these parameters and values, the CSD01060 diode (600 V, 2 A) from Wolfspeed was found to be suitable, its junction capacitance is below the calculated value of C_1 over its entire voltage range and is about 9 pF at the maximum anode voltage. Therefore, the actual implemented value of C_1 was approximately 128 pF. The TO-220 package of the diode was used since it can dissipate heat more effectively than the other available packages. The values of C_2 and L_2 are 158.2 pF and 870.7 nH, respectively, and the value of the input inductance is 4 μH. Inductors L_1 and L_2 were implemented using 21 turns and 6 turns, respectively, of 16 AWG magnet wire wound on T106-2 iron powder core from Mircometals. Table V lists the values of the components and parameters of the Class-EF$_2$ rectifier and Table VI compares them with those

TABLE VI
COMPARISON BETWEEN THE CLASS-EF_2 RECTIFIER AND THE CLASS-E RESONANT LOW dv/dt RECTIFIER FOR THE SAME DC LOAD AND INPUT AC VOLTAGE

	Class EF_2	Class E	$\Delta\left(\frac{EF_2-E}{E}\right)$
V_{IN} (VAC)	250	250	0%
R_L (Ω)	145	145	0%
V_o (V)	60	60	0%
V_D max (V)	139.0	237.5	−41%
I_D max (A)	1.350 A	1.149 A	+17%
P_o (W)	25	25	0%
c_p	0.1320	0.1	32%
C_1 (pF) (6.78 MHz)	137.2	62.85	118%
C_1 (pF) (27.12 MHz)	34.29	15.72	118%
L_1 (μH) (6.78 MHz)	4.017	8.764	−54%
L_1 (μH) (27.12 MHz)	1.004	2.191	−54%
R_{AC} (Ω)	22.560	77.70	−71%
L_{IN} (μH) (6.78 MHz)	2.940	6.512	−58%
L_{IN} (μH) (27.12 MHz)	735.0	1.756	−58%

of an equivalent Class-E resonant low dv/dt rectifier. It can be seen that the Class-EF_2 rectifier has a 41% lower voltage stress on the diode and only a 17% increase in current stress. Inductance L_1 is about 54% smaller than the Class-E rectifier for the same output power level. A lower L_1 inductance results in a smaller and more efficient inductance. Also, the value of capacitor C_1 in the Class-EF_2 rectifier is about 118% larger than that of the Class-E rectifier, this means that the Class-EF_2 rectifier can operate at a higher switching frequency than the Class-E resonant low dv/dt rectifier before being limited by the junction capacitance of the diode.

For the 27.12-MHz system, by following the same design process mentioned for the previous system the value of capacitor C_1 is now 34.29 pF. The diode C3D1P7060Q (600 V, 1.7 A) from Wolfspeed was found suitable to operate for this particular system. Its junction capacitance is approximately 9 pF at the maximum anode voltage, therefore, the actual implemented value of C_1 was 25 pF. The diode is available in a low-inductance QFN package, which makes it more suitable to be used at 27.12 MHz, however, its thermal performance will limit the maximum power that the circuit can operate. The values of C_2 and L_2 are 39.56 pF and 217.7 nH, respectively, and the value of inductance L_1 is 1.00 μH. With these relatively low inductance values, air core inductors can be used, which are generally more efficient since they do not exhibit core losses and do not saturate by the circulating dc current in the rectifier. Table V lists the values of the components of the 27.12-MHz Class-EF_2 rectifier and Table VI compares them with an equivalent Class-E resonant low dv/dt rectifier. In addition to the observations that were made when comparing the 6.78-MHz Class-EF_2 and Class-E rectifiers, it can be noticed here that the required value of inductor L_1 if the Class-E rectifier was used should be 2.19 μH. This inductance value may be practically difficult to implement using an air core inductor since it will be physically large compared to the dimensions of the board, and therefore, it will have to implemented using a magnetic core. Finding a suitable magnetic core that can be efficient at 27.12 MHz maybe a difficult task. It can also be noticed from the table that the value of the shunt capacitor C_1 in the Class-E rectifier is 15.72 pF, which is relatively low. Consequently, finding a diode that has junction capacitance below this capacitance over a wide voltage range may not be commercially available.

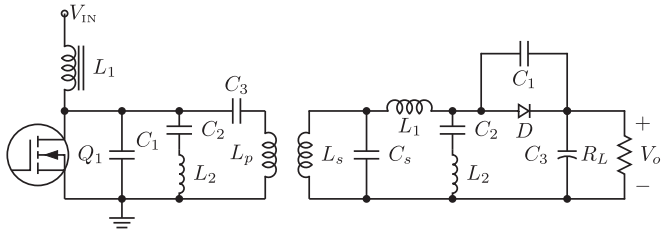

Fig. 10. Circuit diagram of the experimental setup.

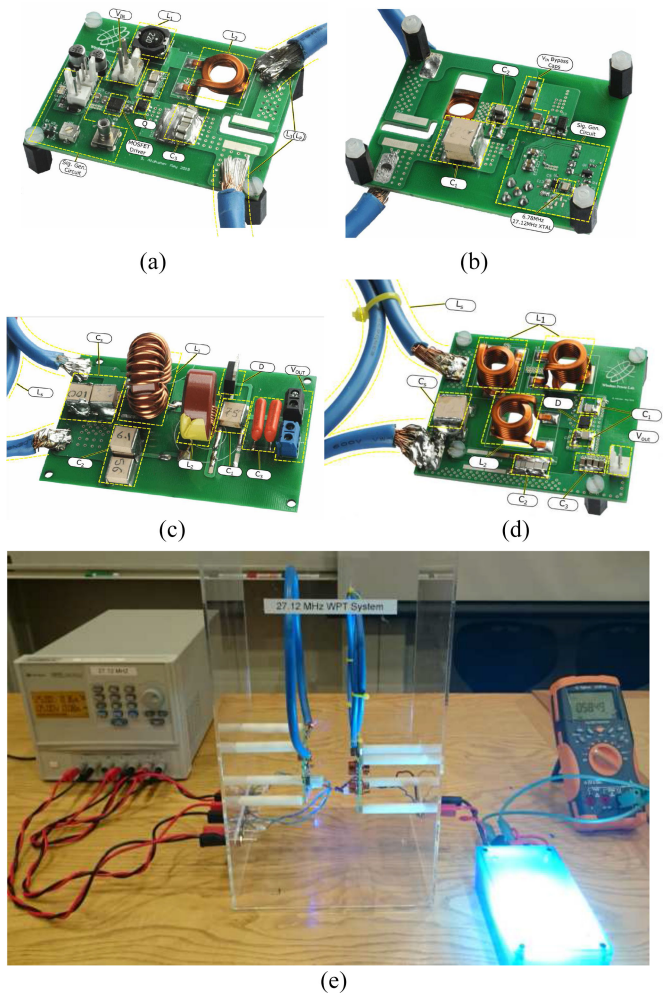

Fig. 11. Photograph of the individual circuits and the setup. (a) 6.78/27.12MHz Class EF_2 inverter (top side) (b) 6.78/27.12MHz Class EF_2 inverter (bottom side) (c) 6.78MHz Class EF_2 rectifier (d) 27.12MHz Class EF_2 rectifier (e) the 27.12MHz WPT system setup

VI. RESULTS

A. Setup

Fig. 10 shows the circuit diagram of the experimental setup of the 6.78 and 27.12-MHz inductive WPT systems and Fig. 11 shows photographs of the individual circuits and the setup.

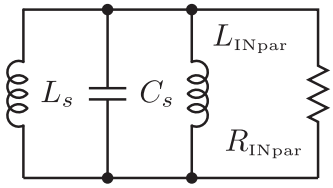

Fig. 12. Equivalent circuit of the secondary coil side.

Inductors L_p and L_s represent the self-inductance of the primary and secondary coils, respectively. The value of the parallel capacitor C_s was chosen such that the reflected impedance seen by the primary coil consists of a real component only for dc a load resistance of 145 Ω. This means that the impedance of C_s should eliminate the impedance of the rectifier and resonate with self-inductance of the secondary coil. Fig. 12 shows the equivalent circuit diagram of the secondary coil including the input impedance of the rectifier. Capacitor C_s can be split into C_{s1} and C_{s1} such that C_{s2} resonates with the input inductance L_{IN} of the rectifier and C_{s1} resonates with the secondary coil inductance. The value of C_{s1} is equal to

$$C_{s1} = \frac{1}{\omega_o^2 L_{\mathrm{INpar}}} \tag{50}$$

where L_{INpar} is the parallel inductance equivalent of L_{IN} and R_{IN} at the operating frequency. From the inductive link theory [16], the value of C_{s2} is

$$C_{s2} = \frac{1}{2\omega_o^2 L_s}\left(1 + \sqrt{1 - \frac{4\omega_o^2 L_s^2}{R_{\mathrm{INpar}}^2}}\right) \tag{51}$$

where R_{INpar} is the parallel resistance equivalent of L_{IN} and R_{IN} at the operating frequency. The value of the capacitor C_s that should be implemented is

$$C_s = C_{s1} + C_{s2}. \tag{52}$$

The implemented values of C_s for the 6.78-MHz WPT and the 27.12-MHz WPT systems were 680 and 74 pF, respectively.

The Class-EF$_2$ inverters for the 6.78- and 27.12-MHz WPT systems were powered from a current limited dc power supply, a Teleyne LeCroy HDO4054-MS oscilloscope was used to observe and record the MOSFET drain voltage and the N2783A Keysight Technologies current probes was used to observe the output current in the primary coil of the inductive link. The secondary coil was aligned with the primary coil and its distance was varied while observing the MOSFET drain voltage until the Class-EF$_2$ waveforms were achieved. A resistive power load was connected to the output of the Class-EF$_2$ rectifier and the diode's anode voltage and secondary coil voltage were observed using the same oscilloscope. The voltage and current waveforms of the Class-EF$_2$ inverter and the Class-EF$_2$ rectifier were not observed simultaneously, initial attempts to do so resulted in significant detuning of the inductive link, which degraded the overall efficiency.

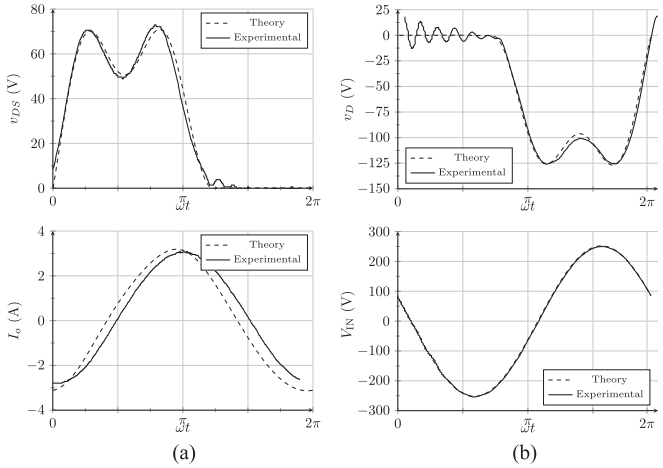

Fig. 13. Voltage and current waveforms for the 6.78-MHz Class-EF$_2$ WPT system. (a) Class EF$_2$ inverter (b) Class EF$_2$ rectifier

B. Waveforms

Beginning with the 6.78-MHz WPT system, Fig. 13(a) and (b) shows the voltage and current waveforms of the Class-EF$_2$ inverter and the Class-EF$_2$ rectifier, respectively, at 20-W output load power. It can be seen that the waveforms match closely to the theoretical waveforms. The phase shift in the primary coil's current is due to the delayed time response of the current probe, and the ringing observed in the diode anode voltage when it is forward biased is due to the lead inductance of the voltage probe. Fig. 14 compares the harmonic content of the MOSFET's drain voltage waveform when the inverter is operated as a Class-E inverter and as a Class-EF$_2$ inverter. It can be seen that the magnitude of second-harmonic component at 13.56 MHz is clearly present in Class-E operation, whereas it is significantly reduced when in Class-EF$_2$ operation. The calculated THD is shown in the figure and is lower by about 19% for the Class-EF$_2$ inverter.

Moving to the 27.12-MHz WPT system, Fig. 15(a) and (b) shows the voltage and current waveforms of the Class-EF$_2$ inverter and the Class-EF$_2$ rectifier, respectively, at 20-W output power. The primary coil's current was not observed due to the bandwidth limit of the current probe, and the secondary coil's voltage was also not observed since the capacitance of the voltage probe can detune the system and result in inaccurate measurements. It can be seen that the waveforms match closely to the theoretical waveforms. Fig. 16 shows the harmonic content of the MOSFET's drain voltage and it can also be seen that the second-harmonic component at 54.24 MHz is significantly reduced. The calculated THD may be lower than that of the 6.78-MHz WPT system due to the lower output current in addition to bandwidth limitations of the voltage probe.

C. Power and Efficiency

Due to the derating limitations of the voltage and current probes available, in addition to their effect on the circuits' performance, it has not been possible to obtain an accurate calculation of the efficiency of each section of the WPT sys-

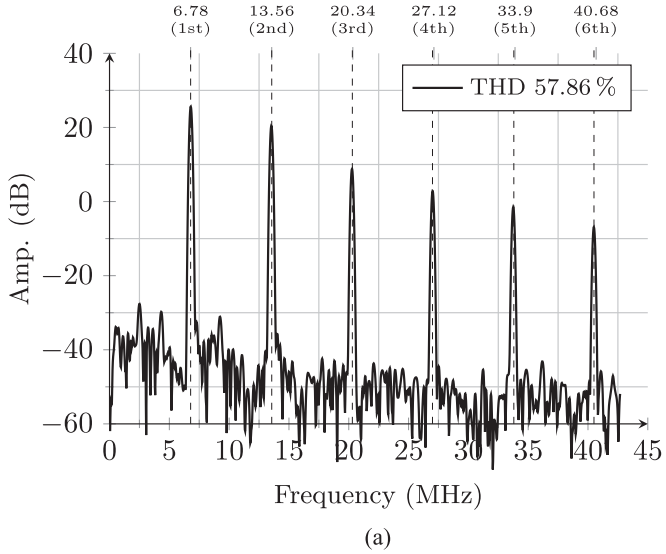

Fig. 14. Harmonic content of the drain voltage for the 6.78-MHz Class-EF_2 WPT system when delivering 10 W in comparison with a similar Class-E WPT system. (a) Class E (b) Class EF_2

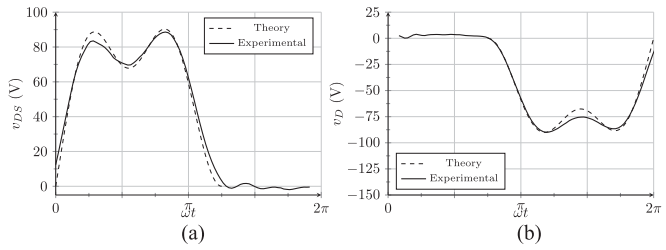

Fig. 15. Voltage waveforms for the 27.12-MHz Class-EF_2 WPT system.

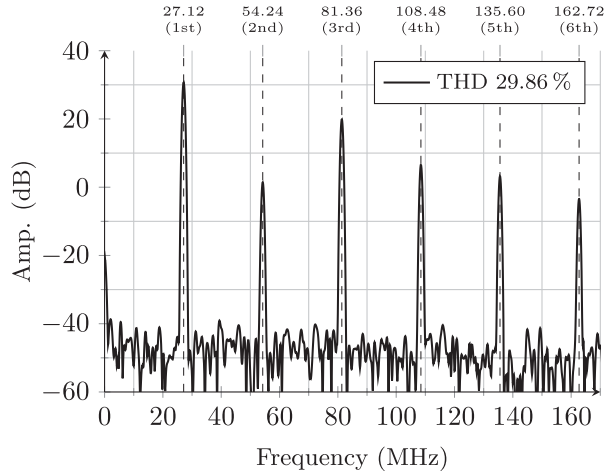

Fig. 16. Harmonic content of the drain voltage for the 27.12-MHz Class EF_2 WPT system when delivering 10 W.

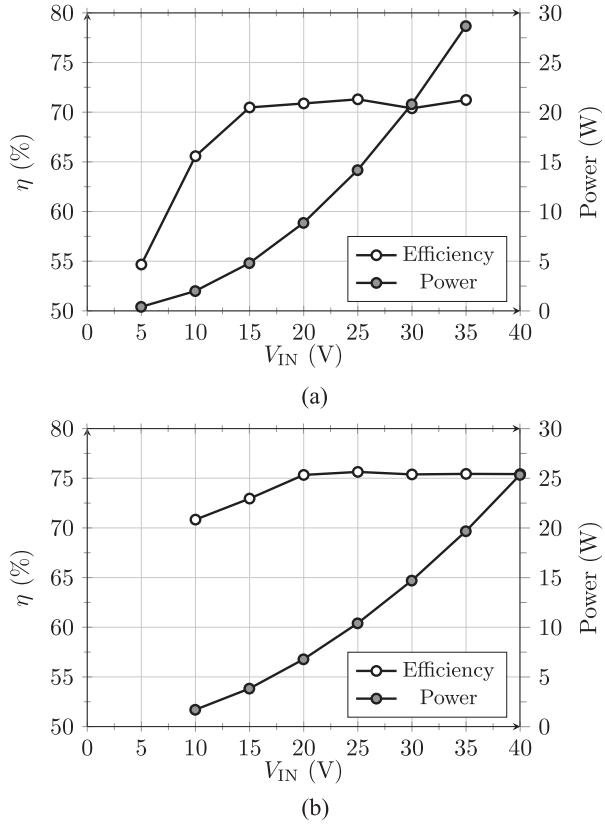

Fig. 17. Load power and dc-to-dc efficiency of the two WPT systems.

tem. Only the dc-to-dc efficiency of both Class-EF_2 6.78 and 27.12-MHz WPT systems was calculated as the input voltage to the systems was varied from 5 to 40 V for a fixed load resistance and fixed coil separation distance. We expect the efficiency of each section, inversion, rectification, and the inductive link, to be around 90%. Fig. 17 shows the load power and dc-to-dc efficiency of both systems. Similar to switched-mode circuits, the efficiency starts at low values for lower input voltages and low power levels and then starts to rise as the input voltage and power increase. The peak dc-to-dc efficiency of the 6.78-MHz WPT system is 71% at 29-W load power, and the peak dc-to-dc efficiency of the 27.12-MHz WPT system is 75% at a 25-W load power. The efficiency of the 27.12-MHz WPT system is higher

since a single turn coil was used, which has a lower ESR, and the fact that the system was operated at a smaller coil separation distance to achieve the higher reflected resistance as initially described in Section VI-A.

VII. Conclusion

This paper presented the analysis, design process, and implementation of a Class-EF_2 inverter and a Class-EF_2 rectifier topology for WPT systems that operate at multimegahertz frequencies. A detailed mathematical analysis was performed on the Class-EF_2 topology to derive its component parameters for optimum switching conditions and other performance parameters such as voltage and current stresses, power-output capability, and harmonic content. The Class-EF_2 inverter and Class-EF_2 rectifier were implemented in two inductive WPT systems that operated at 6.78- and 27.12-MHz frequencies. The design and the obtained experimental results were compared to an equivalent WPT based on a common circuit configuration of the Class-E topology system. The results and conclusions are summarized as follows. It should be noted that these conclusions apply only to the specific circuit configurations of the Class-E and Class-EF_2 topologies that were discussed in this paper and for the particular parameters of the WPT systems in this study.

1) Unlike Class-E circuits, Class-EF_2 circuits have no second-harmonic component in the switch voltage. Therefore, the THD of the switch's voltage waveform and the output current is lower compared to the Class-E, and that makes Class-EF_2 circuits more likely to meet EMI regulations.
2) It has been shown for this application that Class-EF_2 inverters can have similar or higher efficiencies than Class-E inverters because the current stresses in the switch are reduced. The efficiency improvement becomes more significant for switches with high on resistances. Therefore, the Class-EF_2 inverter may be a better topology to use at switching frequencies in the range of tens of megahertz and at higher power levels since the on resistances of available power switches rise with the designed frequency of operation.
3) The Class-EF_2 rectifier introduced in this paper has up to 40% lower voltage stresses across the diode than the voltage-driven Class-E resonant low dv/dt rectifier. Since the forward voltage of a diode becomes large for higher voltage ratings, a lower voltage stress means that diodes with a lower forward voltage can be used, which will improve the overall efficiency and will, therefore, require a smaller heatsink.
4) The Class-EF_2 rectifier can operate at approximately twice the maximum frequency than that of the Class-E resonant low dv/dt rectifier since the required shunt capacitance is twice as large.
5) The Class-EF_2 rectifier requires a 55% lower input inductance than the Class-E resonant low dv/dt rectifier, therefore, the magnetic core requirements are less, and consequently, the losses are reduced. For higher frequencies, air core inductors can be used which will further improve performance and overall efficiency.
6) Unlike some resonant Class-E rectifier configurations, the output voltage of the Class-EF_2 rectifier does not unlimitedly increase when no load is present therefore improving the robustness of such circuits in real-world operating scenarios.

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