ZERO PHASE SEQUENCE VOLTAGE INJECTION FOR THE ALTERNATE ARM CONVERTER

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Abstract

The Alternate Arm Converter (AAC) is a voltage source converter being developed as an alternative to the Modular Multilevel Converter (MMC) for HVDC power transmission and reactive power compensation. Each Arm of the converter contains high voltage series IGBT Director Switches and full-bridge cells, which enables the VSC to ride through AC and DC network faults. This paper describes how the AAC can be optimised by modulating the converter terminal voltages with zero-phase sequence triplen harmonic components. The optimisation reduces the ratio of the number of the full-bridge cells compared to the simpler Director Switches which offers a valuable improvement in footprint and efficiency.

1 Introduction

The uptake of projects using Voltage Source Converters (VSC) for HVDC power transmission is increasing as the new technology offers: faster build times, lower costs, reduced footprint and improved reactive power support. VSC provides several advantages over traditional thyristor based LCC converters [1]; in particular they operate with a high fidelity sinusoidal terminal converter voltage; so there is no need for the large harmonic filters associated with LCC. In addition VSC can be used to both source and sink reactive power in a controlled manner and offers improved dynamic performance. Further, unlike LCC, the DC output voltage of a VSC converter remains unipolar for both forward and reverse power flows, which results in reduced cable costs and enables DC multi-terminal capability. However, although VSC offers significant benefits over thyristor based LCC converters, their use of IGBT devices makes them unable to compete with the voltage and current ratings of thyristor based LCC.

The AAC shown in figure 1 and belongs to a new family of voltage sourced converters using high voltage self-commutated switches and chain link cells [2].

In its basic form, the AAC offers an improvement over the traditional MMC station designs because the number of full bridge cells (and hence large reservoir capacitors) can be reduced by 30-40% and the VSC can ride through pole-pole DC faults. There is also the option to exchange reactive power with the AC network during the DC network disturbance [3] [4] while offering reduced losses and footprint over a FB-MMC.

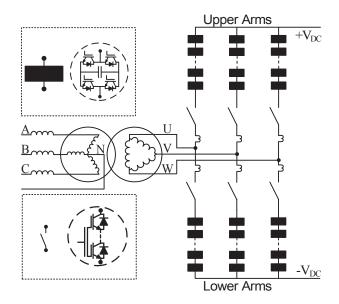


Figure 1: The Alternate Arm Converter.

The full-bridge cells within each Arm are used to shape the voltage at the AC terminal such that high quality sinusoidal currents are drawn from the attached AC network. In addition, inserting the cells in a reverse direction to inject an "opposing" voltage enables the VSC to limit and extinguish DC fault current flow. It is this wave-shaping capability and opposing voltage injection requirement that dictates the minimum number of cells required in each AAC station. The voltage appearing across each Arm of the AAC is the difference between the nominally fixed voltage at the positive or negative DC terminal and the changing voltage at the AC terminal. This is higher than the voltage required for waveshaping or DC fault current blocking and the difference may be supported by the off-state Director Switches. It is this sharing of the voltage stress between cells and Switches that enables the reduction in the number of cells compared to the MMC, where the arms have to be rated for the full DC voltage.

The effect of adding zero-phase sequence triplen harmonic components to the voltage waveform generated by the wave-shaping cells in each Arm will be examined and the changes in the ratio of cells to switches quantified. The associated change in ratio has a positive impact on converter volume and cost while extending the length of the period when both Upper and Lower Director Switches are closed, called overlap, that would otherwise penalise those attributes [5]. A longer overlap period in turn provides an improvement in the performance of the energy balancing of the converter, increasing the amount of reactive power that can be provided by the converter.

2 Cell and Director Switch Voltage Rating

2.1 DC Fault Blocking

When operating at unity power factor at the terminals of the VSC, the AAC is designed with a peak AC phase voltage $4/\pi \times 0.5 V_{DC}$, which for a $\pm 320~kV_{DC}$ network would mean VPK = 407kV. This equates to a RMS phase to ground voltage = 288~kV and RMS line voltage = 499kV as determined from equation (1). Operation at this DC to AC voltage ratio, ensure a natural balance between the average power flow on the AC and DC sides of the VSC and thus energy balance of the cell capacitors [3].

$$V_{DC_{opt}} = \frac{\pi}{2} \hat{V}_{AC} = \frac{\pi}{\sqrt{6}} V_{Line-to-line}$$
 (1)

For DC fault blocking, the cells in two Arms of the AAC must provide a voltage equal to (or larger than) the line to line AC voltage driving the DC fault current. For DC fault current control at 1.0 per-unit AC network voltage condition, this equates to a total voltage of $706kV_{PK}$ or 353kV voltage injection from each converter Arm as shown in figure 2.

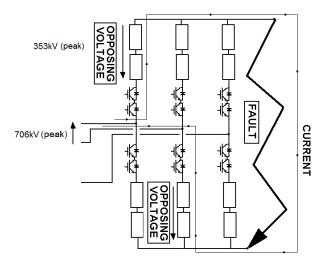
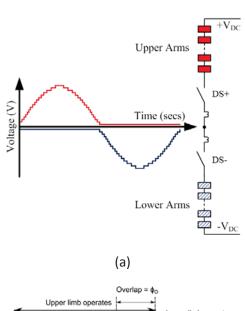


Figure 2: AAC DC Fault Response

2.2 Voltage Wave-shaping and Control

In the AAC, the AC voltage is synthesized in a step-wise manner by adding or subtracting the finite voltage steps available from each cell to the voltage at the positive and negative DC terminal and is performed alternatively by the upper and lower Arms as shown in figure 3(a). During the positive half cycle, the Director Switch in the upper Arm (DS+) will be closed, that in the lower Arm (DS-) opened and the AC voltage will be constructed by switching the cells in the upper Arm. Similarly, during the negative half cycle, DS-will be closed, DS+ opened and the AC voltage will be constructed by switching the cells in the lower Arm. The maximum voltage that each Arm has to produce is approximately half the DC link voltage and at the AC terminal of the VSC appears as a line to ground voltage.



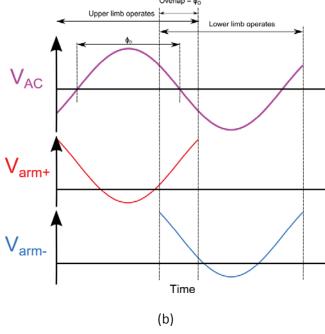


Figure 3: AAC Voltage Wave-Shaping and Operation.

In practice, the voltage that each stack of cells will have to generate will be higher than half the DC voltage. This is due to the need for an overlap period around the zero crossing point where the Director Switches in the upper and lower Arms are both closed and means the voltage generated by the upper Arm will need to continue for some time into the negative half cycle and vice versa. This overlap period ϕ_0 (figure 3b), facilitates handover of the current from one Arm to the other and enables commutation of the Director Switches at zero current (i.e. soft switching). In addition, the overlap period provides a time when a controlled current may circulate between the DC network and the cells in both the upper and lower Arms of the AAC which enables cell energy management and, if desired, active filtering of the current flowing to the DC network [6].

The voltage rating of the cells required in each Arm is therefore critically dependent on the length of the overlap period which in turn determines the depth of voltage transition into the respective opposite half cycle of voltage. The voltage rating of the Director Switches is reduced with increasing overlap period simply because there is more voltage capability from the cells to support the off-state voltage stress.

Increasing the overlap angle provides a longer period of time to control the hand-over of current between the upper and lower Arms of the AAC, equalize the energy of the multilevel cells and enables enhanced levels of DC active filtering. However, the increase in the relative number of cells compared to Director Switches to satisfy the voltage rating requirements has a negative impact on converter footprint and efficiency. The footprint is affected because each cell contains a large high voltage DC capacitor, which dominates the size of the module and is much larger than a Director Switch of equal voltage rating.

3 Triplen Harmonic Voltage Injection

It is explained above that each Arm of the AAC synthesizes a voltage by adding and subtracting the small voltage steps available from the full-bridge cells present in each Arm. At the three AC terminals, these voltages are phase to ground quantities. It is well known that adding zero-phase sequence triplen harmonic components can be used to alter these quantities (for example by adding 3rd, 9th 15th harmonics), which is not seen in the differential line to line voltage of the converter if the triplen harmonic component is added equally to each phase.

In the AAC, the addition of such Zero-Phase Sequence (ZPS) components may be used to reduce the voltage rating of the chain link cells whilst increasing the relative rating of the Director Switches. Figure 4 shows operation with a large overlap angle of \pm 30 electrical degrees and explains how the AAC may be used to track a sinusoidal 50Hz voltage waveform with only part (\sim 27%) of the full-bridge cell voltage rating used to add or "push-up" against the DC network voltage. The voltage rating of the cells is clearly

dictated by the requirement to subtract or "pull-down" against the DC network voltage.

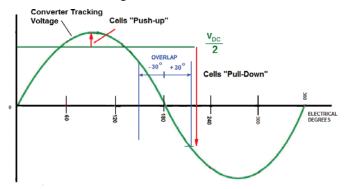


Figure 4: AAC Operation with Sinusoidal Voltage Tracking

In contrast, figure 5 shows how the voltage "pull-down" requirement is reduced when a 3rd harmonic component is added to the tracking voltage waveform.

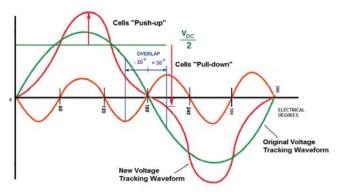


Figure 5: AAC Operation with Sinusoidal and 3rd Harmonic Voltage Tracking

The penalty for adding the triplen harmonic component is a higher peak voltage, however since the full-bridge cells are only partially used in the "push-up" mode, this additional voltage requirement is satisfied without additional rating.

The concept shown in figure 5 may be extended to include other higher order zero-phase sequence components and in the limit tends to the waveform shown in figure 6. Here the waveform is optimised for the large overlap angle of \pm 30 degrees and shows a minimum voltage rating for the cells.

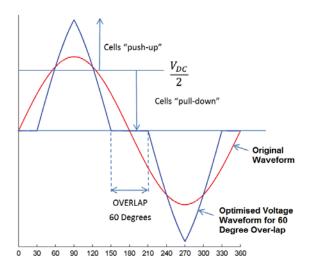


Figure 6: AAC Operation with Sinusoidal and Triplen Harmonic Voltage modulation

4 Effects and Benefits of Zero-Phase Sequence Modulation

4.1 Cell and DS requirements

The cell and DS voltage ratings for sinusoidal modulation can be deduced from the considerations on section 2. If only the DC fault blocking criteria is considered, the Arm cell rating for an AC voltage of 1.1 per-unit is described by:

$$V_{\text{Cell-DCF}} = \frac{1.1 \cdot \widehat{V}_{\text{Line}}}{2}$$
 (2)

And if the voltage wave shaping criteria is considered (i.e. "Pull-Down" voltage):

$$V_{\text{Cell-WS}} = \frac{V_{\text{DC}}}{2} + 1.1 \cdot \widehat{V}_{\text{Phase}} \cdot \sin\left(\frac{\phi_0}{2}\right)$$
 (3)

Thus, if both criteria have to be taken into account, the absolute maximum cell rating would be:

$$V_{Cell-Max} = max(V_{Cell-DCF}, V_{Cell-WS})$$
 (4)

Regarding the Director Switch voltage rating, it will be dependent on the absolute maximum cell rating:

$$V_{DS} = 1.1 \cdot \hat{V}_{Phase} + \frac{V_{DC}}{2} - V_{Cell-Max}$$
 (5)

Thus, for the AAC operating without triplen harmonic injection as described by figure 3, table 1 summarizes the relative rating of the cells and Director Switches in each Arm of the AAC for a DC network operating at \pm 320kV $_{DC}$ and producing a nominal AC terminal voltage of 407 kV. Also, the total Cell and DS count is calculated assuming 1.8 kV device utilization.

Table 1: Relative Full-Bridge Cell and Director Switch Voltage Rating For Different Overlap Angles.

OVERLAP ANGLE (Degrees)	CELL RATING	DS RATING	N _{Cell}	N _{DS}
0	388 kV	380 kV	216	212
± 7.5	388 kV	380 kV	216	212
± 15	436 kV	332 kV	243	185
± 30	544 kV	224 kV	303	125

In table 1, it can be observed that for lower overlap angles, the fault blocking requirement dominates over the wave shaping, but for higher overlap angles, the amount of cells dominates and thus the volume of the converter increases.

However if the voltages are generated with triplen harmonic injection as pictured in figure 7 and the same criteria stated above, the cell and DS ratings experience a significant change, becoming completely independent of overlap angle, as summarized in table 2. The peak of the triplen harmonic injected in this case is equal to $0.25 \cdot \widehat{V}_{Phase}$.

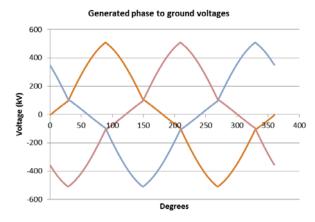


Figure 7: AAC voltages with triplen harmonic injection.

Table 2: Ratings for different overlap angles with ZPS.

OVERLAP ANGLE (Degrees)	CELL RATING	DS RATING	N _{Cell}	N_{DS}
0	388 kV	604 kV	216	336
± 7.5	388 kV	604 kV	216	336
± 15	388 kV	604 kV	216	336
± 30	388 kV	604 kV	216	336

As can be observed in the table, the triplen harmonics cancel the effect of the wave shaping requirement. While for low overlap angles this is actually counterproductive, it reduces the number of cells up to a 28% for higher overlap angles. The cell capacitors constitute a significant part of the total volume of the converter compared to the Director Switches, thus this reduction has a considerable impact.

4.2 Effect of a longer overlap on the energy balancing

In [4] and [5] two methods to control the energy stored in the cells were presented. The energy exchanged by one of the methods, the overlap current, is proportional to the length of the overlap angle, as described in equations (6) and (7) from [5].

$$E_{over}^{+} = -V_{DC}^{+}I_{over}\frac{\phi_{O}}{\omega} \tag{6}$$

$$E_{over}^{-} = -V_{DC}^{-}I_{over}\frac{\phi_{O}}{\omega} \tag{7}$$

In previous variants of the topology, the effectiveness of the overlap current as an energy balancing method was severely limited by the length of the overlap and its impact in the volume of the converter. However, with the addition of the triplen harmonic voltage injection, this limitation can be dismissed without the need of special transformer configurations, additional connections or need for additional harmonic filtering on the DC.

5 Simulations

The operation of the AAC with the voltage modulation shown in figure 7 and a ± 30 degree overlap has been compared against the alternative presented in figure 4 with a ± 7.5 degree overlap using a Simulink ® based model.

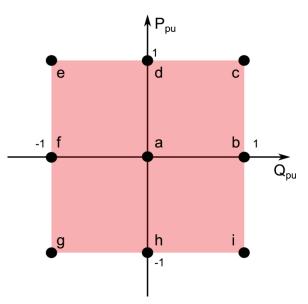


Figure 8: Operation envelope tested in simulations.

Both configurations are simulated moving through the operation envelope pictured in figure 8 and the settling time of the energy in the arms is measured.

In both cases the power references follow the $a \rightarrow c \rightarrow d \rightarrow e \rightarrow f \rightarrow g$ sequence detailed in figure 8. A value of 1 p.u. in P and Q in this case refers to a power factor of 0.9.

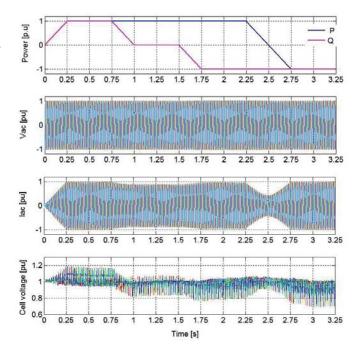


Figure 9: Simulation results with $\pm 7^{\circ}$ Overlap.

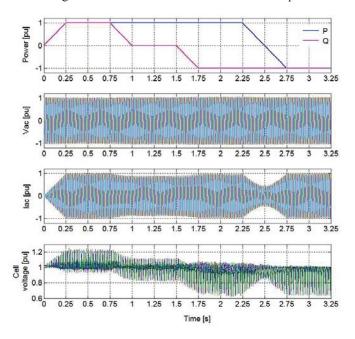


Figure 10: Simulation results with $\pm 30^{\circ}$ Overlap.

As can be seen in figure 10, the energy in the converter for the long Overlap variant stabilizes almost instantaneously even when the power is ramped from positive to negative.

6 Comments on Insulation Voltage Stress

It is clear from the techniques described above that the addition of zero-phase voltage modulation to the voltage waveforms produced by the arms of the AAC has a positive impact on number full-bridge cells required in each converter station. The main effect on plant operation is an increase in the AC terminal to ground voltage stress and will have a direct impact on the steady-state insulation stress.

This is particularly relevant to the converter transformer; although it is important to note that the effects of voltage modulation are not seen across the main windings of the transformer (i.e. do not affect the inter-turn voltage duty). Discussions with a major transformer manufacturer suggests the additional insulation stress will have minimal impact on the design or cost, since in practice there is significant overvoltage capability built into the insulation to satisfy normal application requirements, faults conditions and testing standards.

7 Conclusions

The Alternate Arm Converter is a new type of converter developed for HVDC power transmission and reactive power compensation composed of Full-Bridge Cells in series with Director Switches. This combination allows the converter to ride through DC faults with a limited number of cells in the stacks. However, due to the operation of the Director Switches, the energy balancing of this type of converter becomes challenging and is usually limited by length of an "overlap" period when both DS are closed. The novel modulation technique presented in this paper, allows the use of a long overlap period without impacting on the footprint and cost of the converter, while maintaining the ability to perform DC fault blocking.

The model with the proposed modulation scheme and the overlap current energy balancing technique shows improved stability when transitioning between points inside the operation envelope.

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