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Power Electronic Interfaces for Piezoelectric Energy Harvesters

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Declaration

I herewith declare that the work produced here was either conducted by myself or where collaborative work occurred, it is indicated. References where I have already presented the work in either conference or journal papers have been indicated. All other information has been attributed to its original source. This thesis has not previously been presented in identical or similar form to any other British or foreign examination board.

The work was conducted from October 2011 to August 2015 under the supervision of Dr Paul D. Mitcheson at Imperial College London.

Abstract

Motion-driven energy harvesters can replace batteries in low power wireless sensors, however selection of the optimal type of transducer for a given situation is difficult as the performance of the complete system must be taken into account in the optimisation. In this thesis, a complete piezoelectric energy harvester system model including a piezoelectric transducer, a power conditioning circuit, and a battery, is presented allowing for the first time a complete optimisation of such a system to be performed. Combined with previous work on modelling an electrostatic energy harvesting system, a comparison of the two transduction methods was performed. The results at 100 Hz indicate that for small MEMS devices at low accelerations, electrostatic harvesting systems outperform piezoelectric but the opposite is true as the size and acceleration increases. Thus the transducer type which achieves the best power density in an energy harvesting system for a given size, acceleration and operating frequency can be chosen.

For resonant vibrational energy harvesting, piezoelectric transducers have received a lot of attention due to their MEMS manufacturing compatibility with research focused on the transduction method but less attention has been paid to the output power electronics. Detailed design considerations for a piezoelectric harvester interface circuit, known as single-supply pre-biasing (SSPB), are developed which experimentally demonstrate the circuit outperforming the next best known interface's theoretical limit. A new mode of operation for the SSPB circuit is developed which improves the power generation performance when the piezoelectric material properties have degraded. A solution for tracking the maximum power point as the excitation changes is also presented.

Acknowledgement

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Publications

Journal Papers

Under review L. M. Miller, A. D. T. Elliott, P. D. Mitcheson, E. Halvorsen, I. Paprotny, and P. K. Wright. Maximum Effectiveness of Piezoelectric Energy Harvesters When Coupled to Interface Circuits. IEEE Transactions on Circuits and Systems - Part 1, Under Review, 2015

Conference Papers

J. Dicken, P. D. Mitcheson, A. D. T. Elliott, and E. M. Yeatman. Single-Supply Pre-Biasing Circuit for Low-Amplitude Energy Harvesting Application. In PowerMEMS, pages 46-49, Seoul, South Korea, December 2011.

A. D. T. Elliott and P. D. Mitcheson. Implementation of a Single Supply Pre-biasing Circuit for Piezoelectric Energy Harvesters. In Eurosensors XXVI, Krakow, Poland, September 2012.

A. D. T. Elliott and P. D. Mitcheson. Power Density Improvement of a Piezoelectric Energy Harvester through use of a Micropower Switch-mode Interface.In IEEE Sensors 2012, Taipei, Taiwan, October 2012.

A. D. T. Elliott, D. Zhu, S. P. Beeby, and P. D. Mitcheson. Multilayer Piezoelectric Energy Harvesting Using Single Supply Pre-biasing for Maximum Power Generation. In PowerMEMS, pages 141-144, Atlanta, Georgia, December 2012.

A. D. T. Elliott, M. R. Trice, and P. D. Mitcheson. Implementation of Single Supply Pre-Biasing with Sub-35W Control Overhead for Piezoelectric Energy Harvesting. In PowerMEMS,

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A. D. T. Elliott, J. Dicken, L. M. Miller, P. K. Wright, and P. D. Mitcheson. Scheme for Improved Integration and Lifetime for Piezoelectric Energy Harvesters. In IEEE Sensors 2013, Baltimore, USA, November 2013.

A. D. T. Elliott and P. D. Mitcheson. Piezoelectric energy harvester interface with real-time MPPT. In PowerMEMS, pages 1-5, Awaji Island, Japan, November 2014.

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A. D. T. Elliott, L. M. Miller, E. Halvorsen, P. K. Wright, and P. D. Mitcheson. Which is best, Electrostatic or Piezoelectric Energy Harvesting Systems? Accepted In PowerMEMS, 2015.

Notation

Symbol	Definition
1:a	Transformer winding ratio
1:n	Turns ratio representing coupling between electrical and mechanical domain
AlN	Aluminium Nitride
A_{input}	Mechanical input acceleration
A_{semi}	MOSFET semiconductor area
Au	Gold
BJT	Bipolar junction transistor
c	Ratio of inductor resistance to MOSFET on-state resistance ($R_{\text{L}}/R_{\text{mos}}$)
CDRG	Coulomb damped resonant generator
C_{j}	Parasitic capacitance
C_{max}	Maximum capacitance of electrostatic transducer
C_{min}	Minimum capacitance of electrostatic transducer
C_{p}	Capacitance of piezoelectric transducer
C_{par}	Parasitic capacitance
C_{T}	Output terminal capacitance
C_{v}	Variable capacitance controlled by the applied mechanical excitation
D	Electrical displacement
d_{31}	Piezoelectric coefficient
DisTimer	Discharge timer period

Symbol	Definition
D_{p}	Parasitic damping
d	Piezoelectric coefficient
E	Electric field
$E_{\mathrm{C,loss}}$	Energy loss associated with charge redistribution
E_{coup}	Energy generated by the piezoelectric transducer as a result of coupling to the mechanical input vibrations
E_{dis}	Energy extracted when discharging
E_{harv}	Energy harvested after the interface circuit losses are accounted for
E_{in}	Energy required to pre-bias the piezoelectric beam
$E_{\mathrm{I,loss}}$	Energy loss associated with current leakage
E_{o}	Elastic modulus of oxide material
E_{out}	Energy extracted by the harvester
E_{p}	Elastic modulus of piezoelectric material
E_{PB}	Energy required for pre-bias
$E_{\mathrm{R,loss}}$	Energy loss associated with conduction
E_{s}	Elastic modulus of substrate
$E_{\mathrm{TRIACperCycle}}$	Elastic modulus of piezoelectric material
F	Reciprocal force from the transducer
FPGA	Field programmable gate array
FRTZ	Forced Return To Zero
f_0	Excitation frequency
F_{optcz}	Optimal Coulomb damping force
H_{m}	Proof mass thickness
$i_{\mathrm{cx}}(t)$	MOSFET capacitive leakage current as a function of time where x indicates the MOSFET
$i_{\mathrm{Cp}}(t)$	Piezoelectric transducer capacitive leakage current as a function of time
I_{F}	Current required by the infrared diode in a optically isolated TRIAC

Symbol	**Definition**
i_{L}	Inductor current
I_0	Magnitude of induced sinusoidal current
$I_0\omega$	Current source representation of a piezoelectric energy harvester
$i_{\mathrm{lx}}(t)$	MOSFET current leakage current as a function of time where x indicates the MOSFET
k	Spring constant
k_{cj}	Parasitic capacitance constant (1.1 x10^{-3} C m^{-2})
k_{epiN}	Constant, n-type (2 x$10^{-11}\Omega$ m^2 V^{-2})
k_{epiP}	Constant, p-type (6 x$10^{-11}\Omega$ m^2 V^{-2})
k_{ll}	MOSFET parasitic diode current leakage constant (3.9 x10^{-4} $\mathrm{m}^{-2}\Omega^{-1}$)
K_{L}	Inductor constant (0.23 $\mathrm{Hm}^{-2}\Omega^{-1}$)
L	H-bridge circuit inductance
L_{arm}	Parasitic inductance
L_{m}	Mass length
m	Proof mass
MEMS	Micro-Electro-Mechanical Systems
MESO-scale	Intermediate scale
MOSFET	Metal Oxide Silicon Field Effect Transistor
MPPT	Maximum Power Point Tracking
NegPk	Negative peak detection signal
N_{events}	Number of switching events
N_{switch}	Number of switches in the H-bridge circuit
n	Coupling coefficient (1:n) between mechanical and electrical domains
OPAMP	Operational amplifier
P_{diode}	Power transferred to battery via bridge rectifier
P_{max}	Theoretical maximum available power
PosPk	Negative peak detection signal

Symbol	Definition
P_{out}	Final output power
$P_{\text{R}_{\text{load}}}$	Power dissipated in a resistive load
P_{SSPB}	Power extracted by SSPB technique
P_{TRIAC}	Power consumption of a TRIAC
PZT	lead zirconate-titanate
Q	Q-factor of inductor-capacitor current path
Q_{j}	Charge on the parasitic diode of the MOSFET
R_{arm}	Parasitic resistance
R_{L}	Inductor resistance
R_{Load}	Load resistance
R_{mos}	Total on-state switch resistance
S	Length of each side of volume constrained harvester
S_{x}	Electrical switch where x indicates the switch
SPICE	Simulation Program with Integrated Circuit Emphasis
SSHI	Synchronised Switch Harvester on Inductor
SSPB	Single-Supply Pre-Biasing
t_{o}	Oxide layer thickness
t_{p}	Piezoelectric layer thickness
V_{Bx}	MOSFET blocking voltage where x indicates the device
V_{batt}	Battery voltage
V_{cc}	Voltage on intermediate capacitor
V_{D}	Diode voltage drop
VDRG	Velocity Damped Resonant Generator
V_{end}	Voltage across the piezoelectric beam before discharge
$V_{\text{end}_{\text{actual}}}$	V_{end} predicted allowing for parasitic resistances and leakage currents
$V_{\text{end}_{\text{ideal}}}$	V_{end} predicted before allowing for parasitic resistances and leakage currents
V_{F}	Forward voltage drop (e.g. across an infrared diode)

Symbol	Definition
V_{in}	Voltage (from a pre-charged capacitor or rechargeable battery)
V_{L}	Inductor volume
V_0	Diode threshold voltage (0.7 V)
$V_{\text{operation}_{\text{x}}}$	Reverse bias voltage across diode where x indicates the device
V_{out}	Voltage of energy storage device
V_{PB}	Pre-bias voltage
V_{PBend}	Final pre-bias voltage after charge redistribution
V_{PBstart}	Pre-bias voltage before charge redistribution
V_{piezo}	Voltage across piezoelectric capacitance
V_{po}	Induced open-circuit voltage across piezoelectric capacitance
V_{rem}	Remaining voltage across the piezoelectric beam after discharge
W_{b}	Beam width
W_{m}	Mass width
$y(t)$	External excitation with respect to time
Y	Young's Modulus of a material
Y_0	Input vibration amplitude
Z_{l}	Vertical displacement of the mass
$z(t)$	Mass displacement with respect to time
$\dot{z}(t)$	Mass velocity with respect to time
Γ	Transduction factor
γ	Circuit inversion factor determined as the fractional capacitor voltage conserved by an RLC circuit with a quality factor, Q, ($\gamma \approx \exp^{-\frac{\pi}{2Q}}$)
Δt	On-state conduction time
δ	Mechanical strain
ϵ	Dielectric constant
ϵ_{p}	Piezoelectric dielectric constant
η_{conv}	Conversion efficiency of stored energy from harvested energy

Symbol	Definition
η_{coup}	Coupling efficiency of energy generated by transducer from maximum theoretically available energy
$\eta_{\text{extraction}}$	Extraction efficiency of harvested energy from energy generated by transducer
η_{system}	System effectiveness
θ_{c1}	Rotation per angle per unit vertical displacement from neutral position
μ_{e}	Electron mobility (0.15 $\text{m}^2\ \text{Vs}^{-1}$)
μ_{h}	Hole mobility (0.05 $\text{m}^2\ \text{Vs}^{-1}$)
ρ_{mass}	Density of mass material
σ	Mechanical stress
τ	Switch on-time period
ω	Angular frequency
ω_{input}	Mechanical excitation input frequency

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1 Introduction

Wireless sensors are being continuously improved in terms of functionality, device size and power usage. Presently data transmission further than 10 metres dominates the device's power consumption [1], necessitating the development of multi-hop wireless data networks to increase the operational distance between the sensor and the receiver.

Battery powered wireless sensor networks have been shown to work [2], but are limited by the battery's finite power supply, resulting in the need for regular maintenance. Hence energy harvesters are being developed to provide the benefit of a portable power supply akin to batteries, but without the finite stored energy issue. Conveniently energy harvesters also remove the need for access to the power source and the associated maintenance cost [3].

There are several different types of energy harvesting technologies, which are selected depending on the application's environment. For instance the temperature of bananas being transported must be carefully maintained to ensure they do not ripen early [4]. Clearly wired sensors are impractical. However both the vibrations through the ship from its engines and the rocking due to the water can be converted into electrical energy using vibrational energy harvesters.

There are three main types of vibrational harvesters; electromagnetic, electrostatic and piezoelectric. Electromagnetic have received a lot of attention, but their performance and ease of manufacture do not scale when reduced in size [5]. Conversely, electrostatic harvesters are very easy to manufacture at small scales but their power output at this level is poor. Piezoelectric energy harvesters are a compromise between the two as they can be manufactured on a range

of scales and have a reasonable power output. However in order to improve the power output, a power conditioning circuit must be connected to the output, which along with a full harvester system optimisation is the subject of this thesis.

The thesis is structured as follows:

Chapter 2 provides a broad overview of energy harvesting before focussing on piezoelectric resonant energy harvesting and power conditioning circuits which can be used to maximise power generation. From this literature review it was clear that applying a pre-biasing voltage to piezoelectric energy harvesters can improve their power extraction performance. However the best technique, single-supply pre-biasing (SSPB) [6], had not been practically demonstrated.

Chapter 3 examines the requirements of implementing the SSPB circuit and the challenges this presents. Possible circuit solutions were both simulated in SPICE and experimentally measured. Their performance was compared with the theoretical power extraction limits of each technique and the final SSPB circuit design generated 14 % more power, after the control power overhead was accounted, for than the next best known technique.

Energy harvesters are expected to operate for long periods of time which can result in hundreds of millions of mechanical cycles, which can lead to degradation in performance [7]. Chapter 4 presents a special mode of SSPB circuit operation which is shown to decrease the loss in harvester power output as the piezoelectric material degrades over time.

Using the knowledge gained from the practical implementation and the special SSPB operating case, a collaboration with the University of California, Berkeley, Buskerud and Vestfold University College, Horten, Norway and the University of Illinois, Chicago was formed. A coupled electromechanical model of a full piezoelectric vibration energy harvesting system, including a piezoelectric transducer, a power conditioning circuit, and a battery, was developed, allowing for the first time a complete optimisation of such a system to be performed. The results of this enable an engineer to optimally design piezoelectric energy harvesting systems. The equations and results from this model are presented in Chapter 5.

In some applications the input excitation force may vary over time. To ensure maximum power

is always extracted from a piezoelectric energy harvester, a maximum power point tracking (MPPT) circuit is required to optimise the power conditioning circuit extracting the energy. Chapter 6 presents a methodology to implement this for any piezoelectric power conditioning technique and demonstrates its effectiveness on a simple passive bridge rectifier.

The final chapter presents the conclusions from this research and suggests future fields of research based on the results presented here.

2 Literature Review

In this chapter, the motivation for energy harvesting research is presented and electromagnetic, electrostatic and piezoelectric transduction methods used in resonant vibrational energy harvesting are introduced. The possible output power interface circuits for piezoelectric energy harvesters are then compared in order to identify which one theoretically achieves the highest maximal power extraction. The best circuit will then be implemented and optimised in the later chapters.

2.1 Motivation for Energy Harvesters

Energy harvesters are usually limited in the amount of power they can extract from their environment whilst wireless sensors need sufficient power to achieve both sensing and reliable wireless communication tasks. Many wireless sensor applications, such as monitoring the temperature of bananas [4], can therefore be operated for short periods of activity with consequent higher peak power demand thus the measurement and data reporting is scheduled over periods with long intervals on inactivity. In these circumstances, providing the mean power demand is less than mean power harvested, a solution based on harvesters plus energy storage devices may be feasible.

Power storage devices for such applications include microbatteries previously reported [8] so the challenge for the system designer is to ensure that the harvester, energy storage device and load (wireless sensor) are all carefully matched and designed to achieve the required system performance with the limited input power available. This implies that ideally the energy harvester,

the electronics connected to its output, the energy storage device including any interfacing circuitry, and the load should all be involved in the optimisation process. This thesis concentrates on research work to improve the energy harvesting effectiveness and converting the resulting power into a useful form for typical wireless sensor.

2.2 Resonant Vibrational Energy Harvesting Technology

There are several categories of energy harvester including: solar energy, thermoelectric, acoustic, and mechanical vibrations [9]. The last group can then be subdivided into non-resonant (very low frequency vibrations) and resonant energy harvesters [9], the latter of which this research will focus on.

Resonant vibrational energy harvesters harness mechanical vibrations from the environment through three transduction methods: electromagnetic, electrostatic, and piezoelectric. Each technique has advantages and disadvantages in terms of scalability, electrical output, ease of manufacture, and reliability. They can all be modelled as a mass-spring-damper system (Figure 2.1) [10, 11] which provides a convenient framework for comparison [6, 12, 13] and can be represented by (2.1).

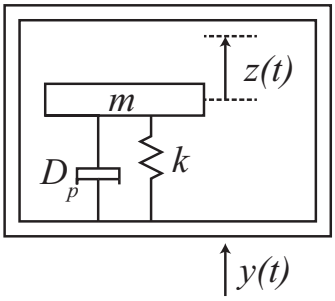


Figure 2.1: Generic damped spring model that can be used to model all three resonant vibrational transduction techniques.

$$m\ddot{z}(t) + c\dot{z}(t) + kz(t) + F = -m\ddot{y}(t) \tag{2.1}$$

where D_{p} is the parasitic damping force exerted by the mechanical and electrical systems, m is the proof mass, k is the spring stiffness, F is the damping force from the transducer, and $y(t)$ and $z(t)$ are the external excitation and mass displacement with respect to time.

When evaluating each transduction method, the physical space required is an important factor. It enables the efficiency and effectiveness of the harvester in extracting power from a mechanical excitation to be evaluated and compared (2.2).

$$\eta_{system} = \frac{E_{\mathrm{out}}}{E_{\mathrm{max}}} \tag{2.2}$$

where E_{out} is the energy extracted by the harvester and E_{max} is the maximum energy per cycle that can be harvested from a given mechanical excitation by a harvester in a given volume.

2.2.1 Electromagnetic

Electromechanical energy harvesters use the relative motion between a conductor and magnetic flux to induce a voltage. This can be achieved by attaching a magnet to a cantilever and oscillating it through a fixed coil (Figure 2.2). In this case the magnet acts as the proof mass, m, however the coil and magnet arrangement can be swapped [14].

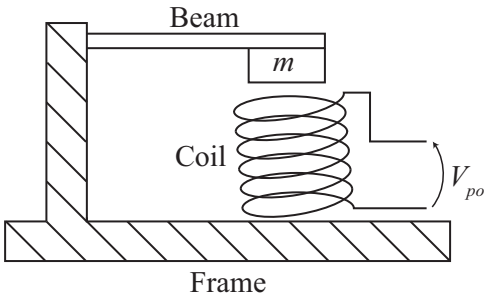


Figure 2.2: High level diagram for electromagnetic energy harvesting.

Two scales of devices have been successfully demonstrated, wafer and macro-scale, with power generation measured in the nanowatts and microwatts respectively [12]. Wafer devices are made by etching the energy harvester structure into silicon (Figure 2.3). However they suffer from

relatively poor performance compared to macro-scale devices due to planar magnetics having poor magnetic properties, limited number of coil turns and restricted vibrational amplitude. Macro-scale electromagnetic harvesters are much more reliable and proven devices with relatively high output currents but at the expense of low voltages compared to other transduction methods [12].

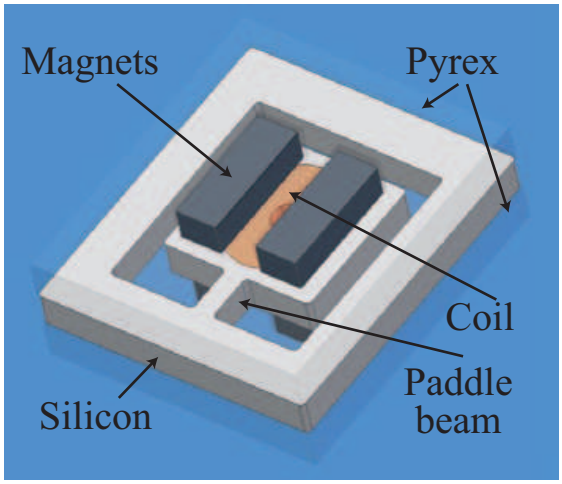


Figure 2.3: Wafer-scale silicon electromagnetic energy harvester from [15]

The electromagnetic energy harvester can be modelled as a transformer with the mechanical domain on the primary side and the electrical domain on the secondary side (Figure 2.4). The primary side consists of a current source ($\omega^2 m Y_0$) in parallel with a resistor (D_p) for the parasitic damping, an inductor (k) for the spring constant, and a capacitor (m) for the proof mass. The transducer is formed by the transformer ($1 : a$ winding ratio) with a series connected inductor and resistor representing the parasitic inductance (L_arm) and resistance (R_arm) respectively. A typical electrical load is modelled by a resistor R_{load} connected to the secondary windings, however an inductor and capacitor can be added as a reactive load as well [16].

2.2.2 Electrostatic

Electrostatic harvesters are constructed from two metal plates separated by air similarly to a capacitor. Charge is placed on the plates then the mechanical force applied by the vibration

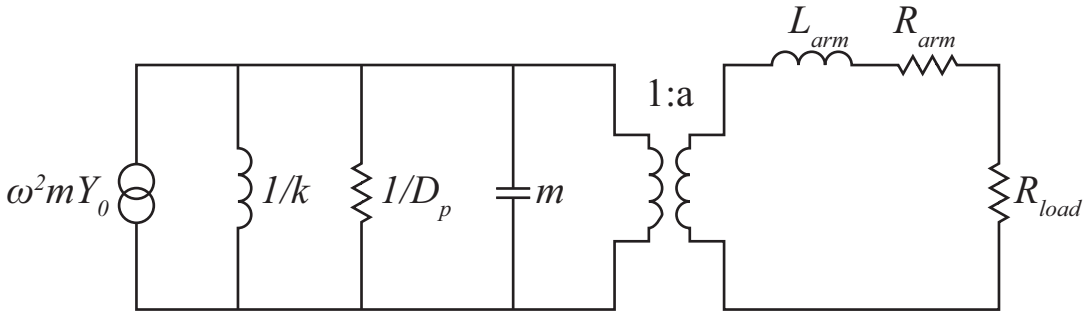


Figure 2.4: Electromagnetic energy harvester model [16]

source, causes the plates to separate. This causes work to be done against the electrostatic attraction of the two plates, thereby generating power [3]. Figure 2.5 is a simplified model representing a charge constrained electrostatic harvester to demonstrate the electrostatic energy harvester princeiple. V_{in} is a pre-charged capacitor or rechargable battery, C_{v} is the variable capacitance controlled by the applied mechanical excitation, C_{par} is the parasitic capacitance, and C_{store} is the storage capacitor. When C_{v} is at its greatest separation (C_{max}), the left hand switch, S_1, is closed, energy is transferred from V_{in} to C_{v}. S_1 is then opened and the mechanical excitation force moves the plates of C_{v} to the minimum separation point, C_{min}, causing the energy on C_{v} to increase. S_2 is then closed transferring the energy stored on C_{v} to the storage capacitor [17, 18].

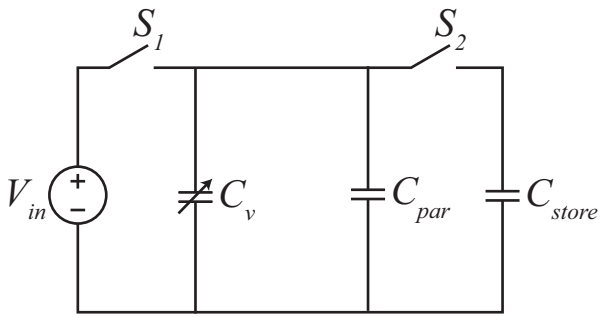


Figure 2.5: Electrostatic energy harvester model [18]

Two forms of electrostatic energy harvesters have been developed, switched and continuous. Switched electrostatic harvesters operate by reconfiguring the transducer and itss connecting

circuitry through the use of a switch at different points in the generation cycle [3] whilst continuous electrostatic harvesters have the transducer permanently connected to load resistance [19]. In the latter case, the variation in capacitance as the plates are moved causes work to be done as charge is transferred between the electrodes. A further classification of switched harvesters can be performed into fixed charge and fixed potential depending whether a fixed voltage is applied to the plates.

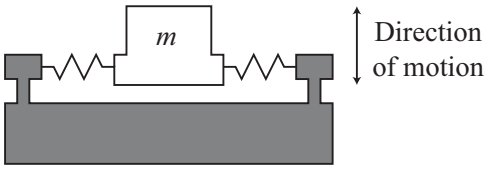


Figure 2.6: An out-of-plane gap closing electrostatic energy harvester re-drawn from [12].

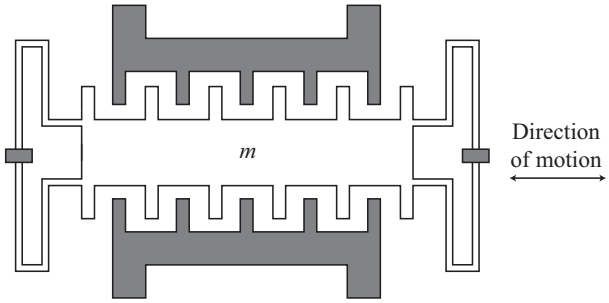


Figure 2.7: An in-plane gap closing electrostatic energy harvester re-drawn from [12].

Figure 2.6 and 2.7 illustrate two mechanical setups where there is no lateral variation and negligible fringing field between the two plates. The electric field's energy density therefore is independent of the plate separation as the field strength is proportional to the constant charge [3]. Alternatively, if the separation between the plates remains constant and the plates move laterally with respect to each other, the work is done against the fringing field (Figure 2.8). As the plate overlap decreases, the electric field strength also increases and thus the stored electrical energy increases [3].

Electrostatic transducers need a pre-charge voltage in order to operate. This can be implemented using an electret transducer (Figure 2.9), which has a permanent charge buried in the

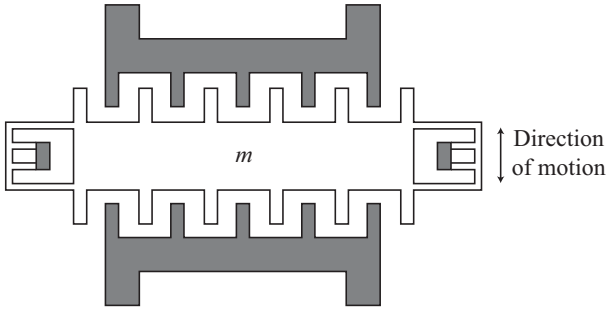


Figure 2.8: An in-plane overlap varying electrostatic energy harvester re-drawn from [12].

dielectric layer of the device [20]. Alternatively, an active pre-charge system can be used to provide the necessary voltage. This allows the pre-charge voltage to be optimised to the excitation force, but increases system complexity and control power overhead [3].

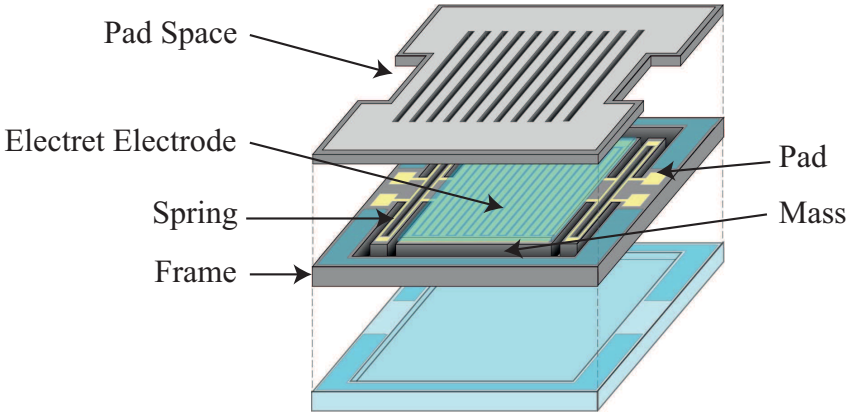


Figure 2.9: An electrostatic energy harvester using an electret material to provide the pre-charge voltage from [21].

Figure 2.10 is an electrical model of both the mechanical system and the electrical output. The primary side consists of a voltage source ($\omega^2 m Y_0$) in series with a resistor (D_p) for the parasitic damping, an inductor (m) for the proof mass, and a capacitor ($\frac{1}{k}$) for the spring. The output consists of a terminal capacitor (C_T) and a typical load resistance (R_Load).

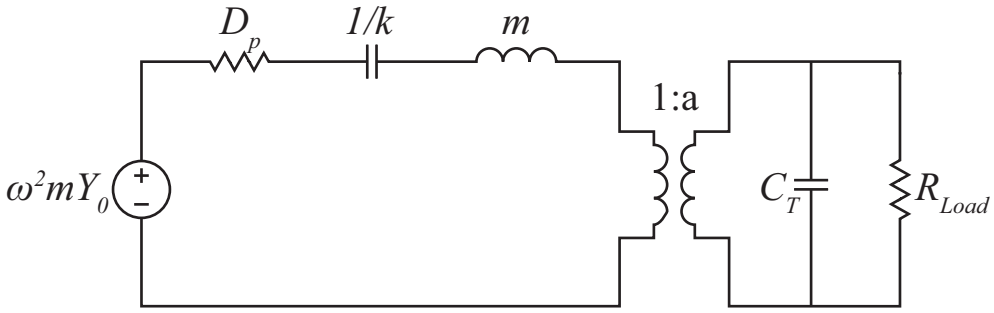


Figure 2.10: Electrostatic energy harvester model [22]

Maximum power generation and system effectiveness for electrostatic energy harvesters was modelled in [23]. The paper explored both the electrical and mechanical elements, and their interactions, in order to optimise the complete system. The analysis parameterises the properties of the key elements in the devices such as the semiconductor power switches [23]. The results concluded that when both the transducer and the power electronics interface are considered, the constant voltage topology is effective over a much wider range than the constant charge topology. This is because the coupling effectiveness in the constant voltage configuration is not reduced by charge leakage during the generation stroke, unlike in the constant charge configuration [23]. Figure 2.11 and Figure 2.12 shows the maximum power output and system effectiveness at 1 kHz for both the constant voltage and constant charge cases using (2.2).

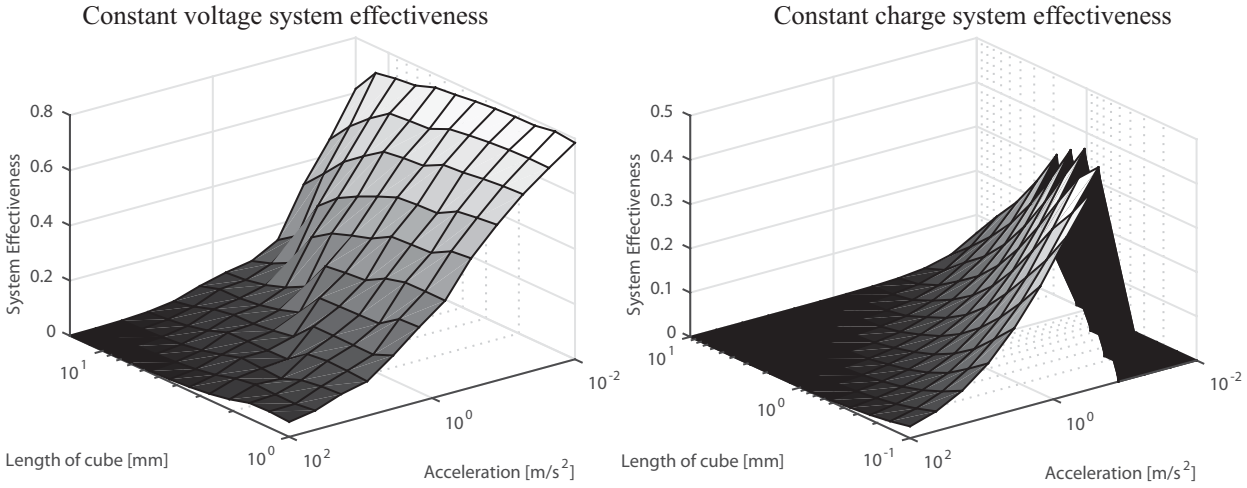


Figure 2.12: Electrostatic energy harvester system effectiveness at 1 kHz for both constant voltage and constant charge topologies from [23].

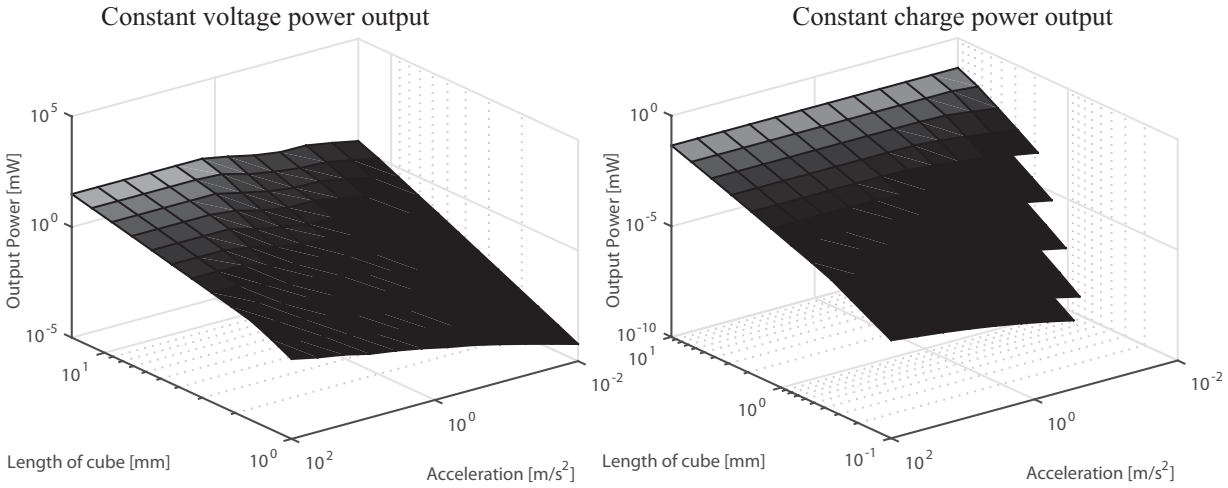


Figure 2.11: Electrostatic energy harvester power output at 1 kHz for both constant voltage and constant charge topologies from [23].

2.2.3 Piezoelectric

Piezoelectric materials display asymmetrical charge across their structure. Applying either a mechanical stress or strain to piezoelectric material induces a charge in the material. The

constitutive equations used to describe piezoelectric devices are given in [24].

$$\delta = \frac{\sigma}{Y} + dE \tag{2.3}$$

$$D = \epsilon E + d\sigma \tag{2.4}$$

Where δ is the mechanical strain, σ is the mechanical stress, Y is the Young's Modulus of the material, d is the piezoelectric coefficient, E is the electric field, D is the electrical displacement, and ϵ is the dielectric constant.

A load may be placed across the material to draw a current which neutralises the net charge [3]. The amount of energy extracted by the transduction method depends upon the electromechanical coupling between the material and the vibrational source. High electromechanically coupling materials tend to be ceramics with the most common being aluminium nitride (AlN) and lead zirconate-titanate (PZT)[25, 3].

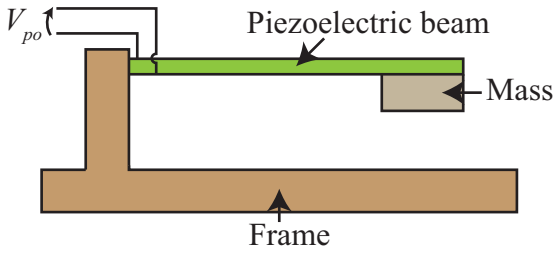


Figure 2.13: A piezoelectric energy harvester constructed from a cantilever with a mass attached at the tip.

The simplest piezoelectric energy harvester structure is a cantilever with a mass attached to the tip in order to tune the beam's resonance frequency (Figure 2.13). The harvester's characteristics can be improved in terms of bandwidth [26, 27], power generation [28], or mechanical wear [29] by changing the piezoelectric material, cantilever design and fabrication process [30].

Figure 2.14 (a) is an electrical equivalent model of a piezoelectric energy harvester's mechanical and electrical properties [6]. The left hand side of the transformer represents the mechanical properties consisting of a voltage source representing the voltage induced across the piezoelec-

tric material ($\omega^2 m Y_0$) at a frequency ω and mass displacement amplitude Y_0, a resistor for the parasitic damping (D_p), a capacitor for the spring constant ($1/k$), and an inductor for the mass (m). A transformer with turns ratio ($1 : n$) represents the coupling between the mechanical and electrical domain. The secondary side of the transformer is shunted to a capacitor, C_p, representing the piezoelectric transducer's in-built capacitance.

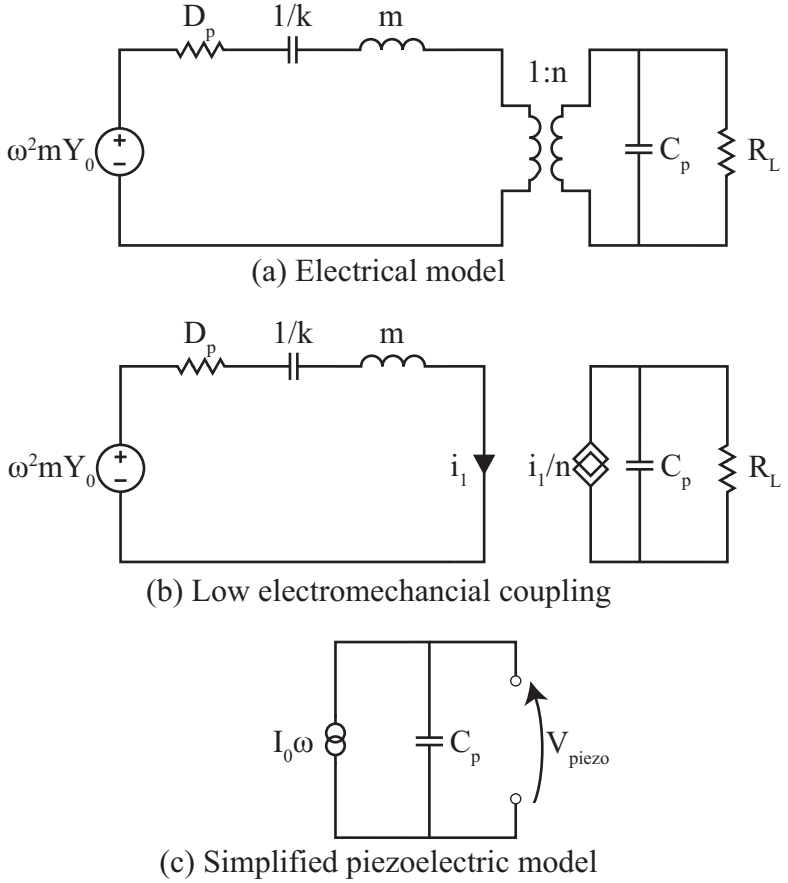


Figure 2.14: (a) Piezoelectric energy harvester model [22], (b) Piezoelectric energy harvester model with low electromechancial coupling, (c) Simplified piezoelectric energy harvester model [6].

Figure 2.14(b) is a re-arrangement of Figure 2.14(a) due to the relatively low coupling factor present in most piezoelectric materials. The low coupling factor causes the proof mass to be relatively unaffected by connections on the secondary side. This enables the transformer to be replaced by a current controlled current source (i_1/n). At mechanical resonance the circuit can

be further simplified to a current source ($I_0\omega$) shunt connected to the in-built capacitance with an induced open-circuit voltage, V_{po}, where ($I_0 = V_{\text{po}}\omega C_{\text{p}}$). For more details on the derivations see [6, 31, 32].

During the course of this research, two types of piezoelectric harvesters were used to test the effectiveness of the power electronics, a diaphragm harvester in the form of a piezoelectric loud speaker (Figure 2.15) [33] and a screen printed bimorph harvester (Figure 2.16) [28]. These harvesters were chosen as representative examples of contemporary technology which are low cost and available off the shelf.

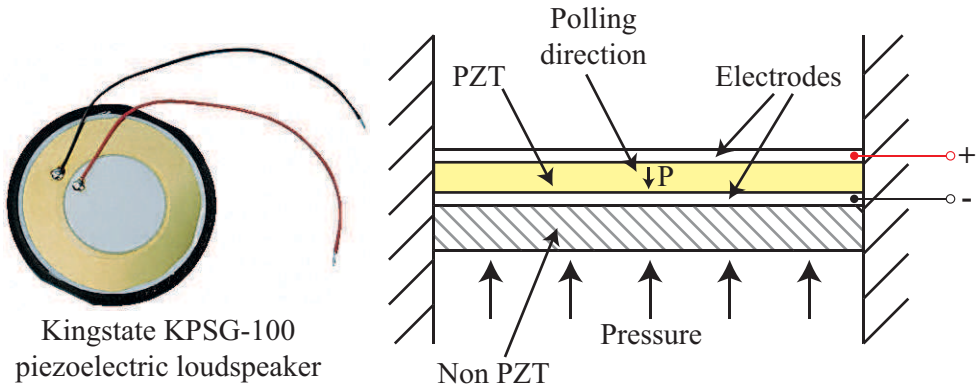


Figure 2.15: A Kingstate KPSG-100 piezoelectric loudspeaker (right) and it's internal construction (left) [33].

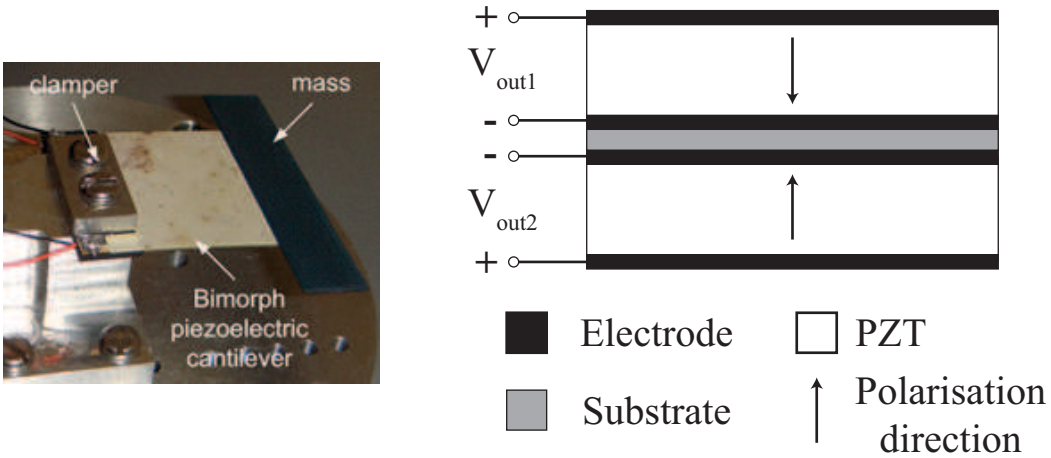


Figure 2.16: A single-layer screen printed bimorph (left) with it's construction (right) [28].

2.3 Maximal Power Extraction Circuits

Piezoelectric transducers were shown in Figure 2.14 to be equivalent to current sources with shunt capacitance. Maximisation of power extraction from these harvesters therefore requires an interface circuit forming an electrical load which matches the load of the transducer.

2.3.1 Resistive load

The simplest way of extracting real power is to connect a resistive load across the output (Figure 2.17) [34]. The power extracted using this technique when the mechanical excitation induces a sinusoidal current of magnitude I_0 at a frequency ω is:

$$P_{\mathrm{R_{Load}}} = \frac{1}{2}\left(\frac{{I_0}^2 R_{\mathrm{Load}}}{1 + {R_{\mathrm{Load}}}^2 \omega^2 {C_{\mathrm{p}}}^2}\right) \tag{2.5}$$

where R_{Load} is the resistive load.

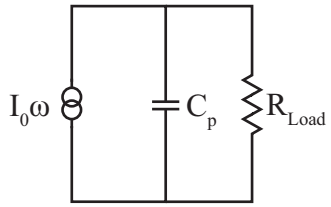


Figure 2.17: Piezoelectric circuit with matched resistive load [22].

Maximum power extraction occurs when the optimal R_{Load} is used. This value can be found by differentiating (2.5) with respect to R_{Load}:

$$R_{\mathrm{Load_{opt}}} = \frac{1}{\omega C_{\mathrm{p}}}. \tag{2.6}$$

The maximum power extracted by this technique is therefore

$$P_{\mathrm{R_{Load_{opt}}}} = \frac{1}{4}\frac{{I_0}^2}{\omega C_{\mathrm{p}}} \tag{2.7}$$

However a wireless sensor expects a DC voltage, thus it is more useful to store the harvested energy in a battery or capacitor enabling the use of a higher power wireless sensor with a low duty cycle. Since the piezoelectric energy harvesters induce a sinusoidal output voltage, the voltage waveform needs to be rectified.

2.3.2 Bridge rectifier

This simplest form of rectification is achieved using a passive diode bridge rectifier with its output connected directly to the storage device (Figure 2.18).

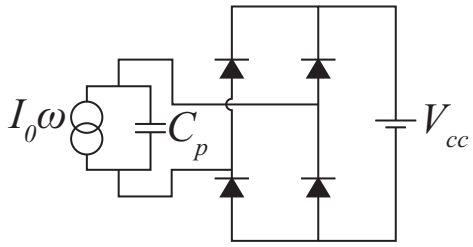


Figure 2.18: A diode bridge rectifier circuit connected to an optimal output voltage.

Figure 2.19 shows that for a mechanical excitation which induces a sinusoidal current, the voltage across the piezoelectric capacitor is constrained by the output voltage, V_{cc}, and the voltage drop across the diode, V_{D}. The diodes in the bridge rectifier will only conduct when the piezoelectric capacitor voltage exceeds $V_{\mathrm{cc}} + 2V_{\mathrm{D}}$ thus the output current into V_{out} is half the rectified induced current [6]. The power extracted by this technique is therefore equal to:

$$P_{\mathrm{diode}} = \frac{2}{\pi} I_0 V_{\mathrm{cc}} \left(1 - \frac{V_{\mathrm{cc}} + 2V_{\mathrm{D}}}{V_{\mathrm{po}}}\right) \tag{2.8}$$

where $V_{\mathrm{po}} = \frac{I_0}{\omega C_{\mathrm{p}}}$ is the open circuit piezoelectric voltage and V_{D} is the voltage drop across a diode.

Maximal power extraction can be achieved by setting V_{out} to an optimal voltage, V_{opt}, which

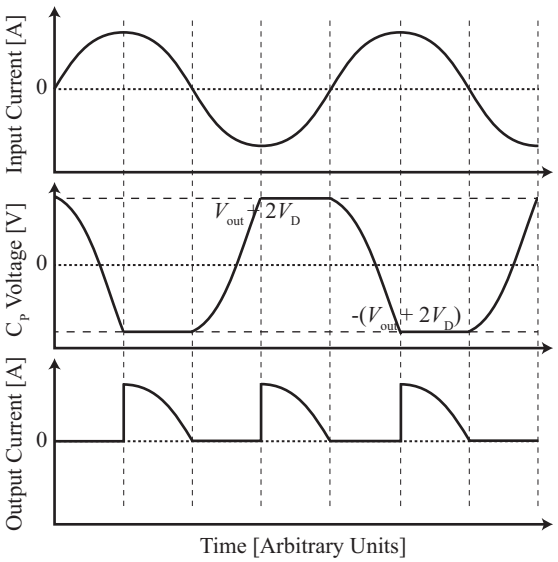


Figure 2.19: Input current, induced voltage across the piezoelectric capacitor and output current into a voltage source when a diode bridge rectifier circuit is connected to a piezoelectric energy harvester.

can be found by differentiating (2.8) with respect to V_{out} [35].

$$V_{\text{opt}} = \frac{1}{2}\left(V_{\text{po}} - 2V_{\text{D}}\right) \tag{2.9}$$

$$P_{\text{diode}_{\text{max}}} = f_0 C_{\text{p}}\left(V_{\text{po}} - 2V_{\text{D}}\right)^2 \tag{2.10}$$

where f_0 is the excitation frequency and C_{p} is the piezoelectric capacitance.

2.3.3 Switched Resistive Load

Piezoelectric energy harvesters can be operated as velocity damped resonant generators (VDRGs) (Figure 2.1) [36]. Optimal damping of VDRGs occurs when the resistive load is inversely proportional to the piezoelectric capacitance. It is clear from the maximum power transfer theorem [37], that increasing the resistive load beyond this point causes the magnitude of power extracted to decrease, as the current flow is reduced. Similarly decreasing the resistive load will cause an increase in current flow, however most of the power will be dissipated in the harvester. The level

of damping, which is determined by the velocity of the harvester's vibrating mass, $\dot{z}(t)$, and a constant of proportionality, c, is therefore non-constant and difficult to control. However piezoelectric energy harvesters can be operated as Coulomb damped resonant generators (CDRGs) [38]. These apply a fixed damping force which opposes the motion of the harvester's mass, and are therefore much easier to control [36]. Piezoelectric CDRG can be implemented by modifying the charge on the beam at the extreme points of its motion [38]. This was first demonstrated by simply connecting a resistive load across the harvester via a switch (Figure 2.20) when the beam reaches either of its extreme points of motion [39]. The induced voltage waveform across the resistive load is given in Figure 2.21 [6].

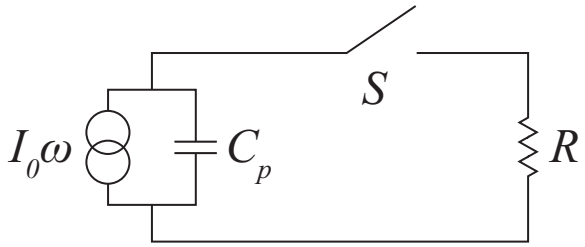


Figure 2.20: Synchronous switched extraction circuit [6].

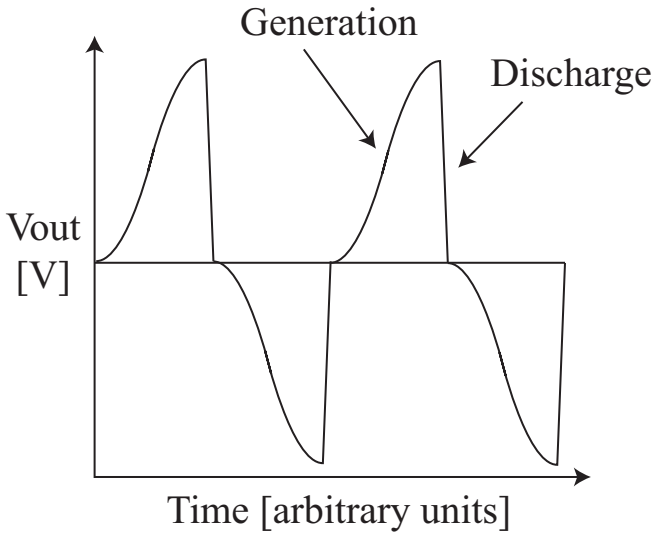


Figure 2.21: Synchronous switched extraction circuit voltage waveform [6].

In order to charge an energy storage device, a diode bridge rectifier can be connected instead

of the resistor. A buck converter can be connected on the output as well to smooth the charging waveform applied to the storage capacitor, C_{store}, shown in Figure 2.22

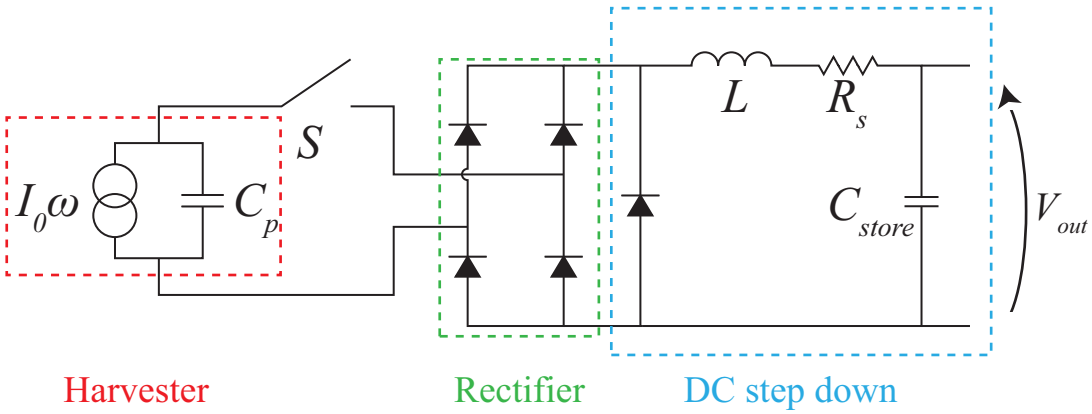


Figure 2.22: Modified switched resistive load circuit to provide DC output to charge an energy storage device [6].

This technique has been shown to provide a maximum power generation improvement factor of $\frac{8}{\pi}$ compared to a simple resistive load [6]. However greater power gains have been shown to be achievable by applying a fixed amount of charge to the piezoelectric beam in order to induce a piezoelectric force as demonstrated by Synchronised Switch Harvester on Inductor (SSHI) [40, 41] and pre-biasing [42, 6] techniques.

2.3.4 Resonant Charge Transfer

All extraction techniques which use a switch to flip the charge on a piezoelectric capacitor or transfer the charge to a second capacitor for storage, do so by resonant charge transfer (also known as charge flipping). This is achieved by briefly closing a switch, shorting the capacitance. The period of time the switch is closed for, will determine the amount of charge transferred. An inductor is used to limit the peak current thus slowing the rate of charge transfer.

Figures 2.23 and 2.24 demonstrate charge being transferred between a capacitor and battery via a switch, inductor and resistor in series. The resistor represents any parasitic losses in the circuit (e.g. inductor resistance, switch on-state resistance). When the switch is closed for

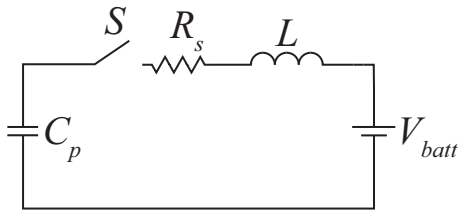


Figure 2.23: Resonant charge transfer between piezoelectric capacitance, storage capacitor, inductor and switch with parasitic resistance.

half of the electrical resonance period, τ, the proportion of charge transferred to the secondary capacitor is determined by the circuit inversion factor, γ. Thus γ can be defined as the fractional capacitor voltage conserved by an RLC circuit with a quality factor, Q, and has been shown to be approximated as (2.12) in [6].

$$Q = \frac{1}{R_{\mathrm{s}}}\sqrt{\frac{L}{C_{\mathrm{p}}}} \tag{2.11}$$

$$\gamma \approx \exp^{-\frac{\pi}{2Q}} \tag{2.12}$$

Figure 2.24 shows the results of a PSPICE simulation of the change in voltage across a 55 nF capacitor when resonantly connected to a 3 mH inductor and 0 V battery by a switch with an on state resistance of 1 nΩ. The circuit inversion factor and thus the Q-factor is varied by increasing the value of the series resistor, R_{s}.

As the inversion factor decreases more charge is conserved on C_{p} hence the final voltage can be calculated as the product of the initial capacitor voltage, $V_{\mathrm{C_p,init}}$, and γ:

$$V_{\mathrm{C_p,final}} = V_{\mathrm{C_p,init}}\gamma \tag{2.13}$$

Similarly if the capacitor initially has no charge and is resonantly connected for a half cycle through an inductor to a battery of voltage V_{batt}, the final voltage (also known as the pre-bias

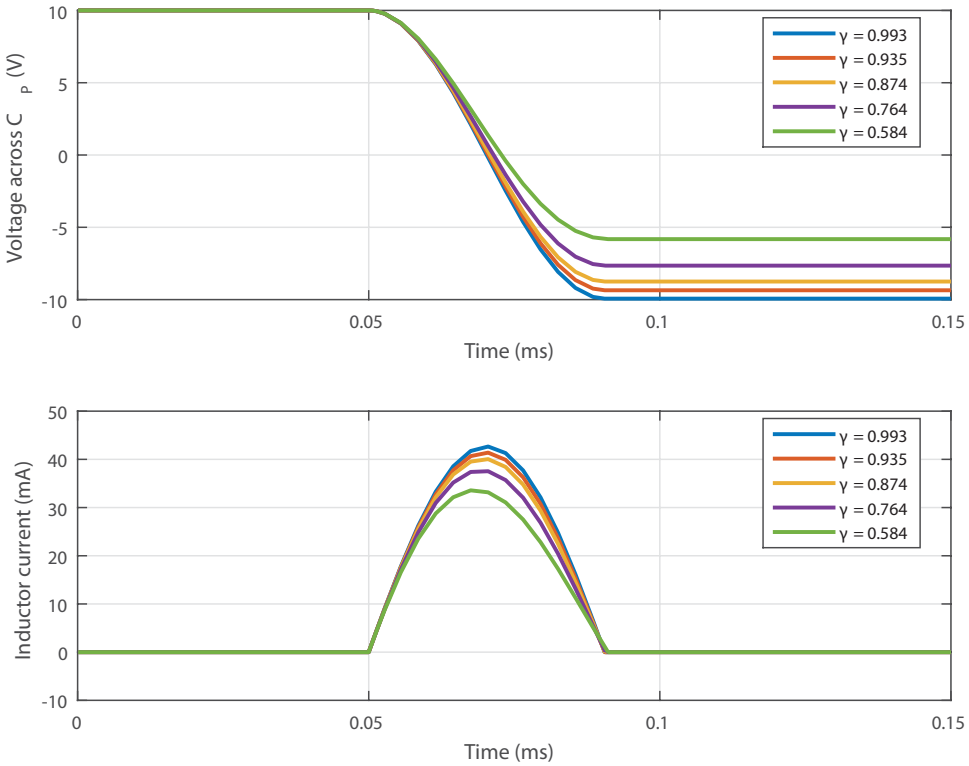


Figure 2.24: Waveforms for the voltage across the capacitor and inductor current when switched is closed for half an electrical resonance cycle with different circuit inversion factors.

voltage), V_{PB} is equal to the sum of V_{batt} plus the product of V_{batt} and γ [34].

$$V_{\mathrm{PB}} = V_{\mathrm{batt}} + V_{\mathrm{batt}}\gamma \tag{2.14}$$

$$V_{\mathrm{PB}} = V_{\mathrm{batt}}(1 + \gamma) \tag{2.15}$$

2.3.5 Synchronised Switch Harvester on Inductor

Figures 2.25 and 2.26 illustrate the SSHI circuit topology and corresponding piezoelectric voltage waveform [40]. The circuit operates as follows, assuming a piezoelectric beam is mechanically excited at a fixed frequency and magnitude. When the piezoelectric beam reaches the point of maximum displacement, the voltage across the piezoelectric material is greatest. Briefly closing switch S causes the charge on the piezoelectric beam to be resonantly flipped by the inductor. This causes the voltage across the piezoelectric material to invert. Since the charge on the beam will induce a piezoelectric force, the inverted charge will act in the opposite direction to beam's new direction of travel as it moves towards the opposite point of maximum displacement. The induced piezoelectric force is thus increasing the electrical damping and the work done by the motion of the beam. The diode bridge rectifier on the output is then required to rectify the piezoelectric output voltage in order to charge the storage capacitor, C_{out}. Whilst control of the switch requires some power, this can be offset by the significant increase in applied electrical damping and thus power generated. Note that the on-state resistance of the switch and parasitic resistance of the inductor used to perform the charge flipping should be minimised in order to achieve good results.

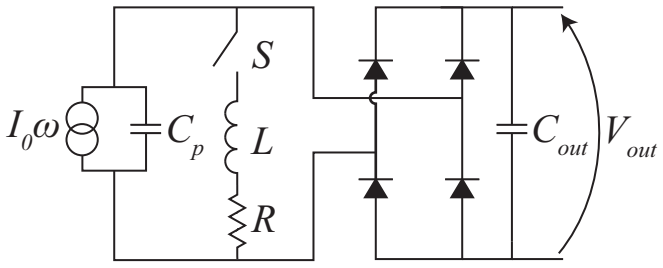


Figure 2.25: A Parallel SSHI-DC circuit.

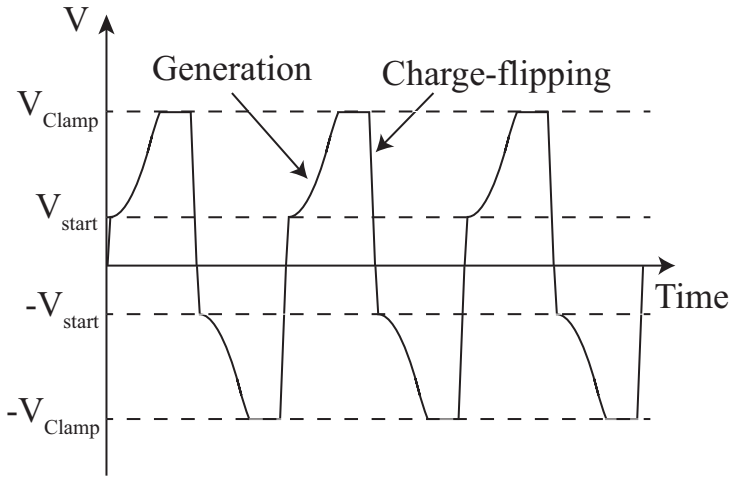


Figure 2.26: Voltage waveform for a parallel SSHI DC circuit.

The position of the rectification circuit can be altered to be either in parallel with the switching circuit (Figure 2.25) or in series with the inductor and switch. However the parallel SSHI-DC circuit has been theoretically shown to achieve a slightly greater power output than the series SSHI-circuit [6] and hence will be the topology for future power extraction circuit comparisons within this thesis.

The theoretical maximum power output for the SSHI-DC circuit derived in [6] is given by

$$P_{\mathrm{SSHI}_{\max}} \approx {V_{\mathrm{po}}}^2 f_0 C_{\mathrm{p}} \left(\frac{4Q}{\pi} \right) \tag{2.16}$$

where Q is the Q-factor of the switch-capacitor-inductor current path for the charge inversion process, which can be approximated by $Q = \approx \pi/(2\ln(\gamma))$, where γ is the circuit inversion factor defined in Section 2.3.4.

In a practical implementation of the SSHI circuit [43], the maximum power extracted was 917 μW using a 420 nF piezoelectric transducer with a γ of 0.55 at 300 Hz, inducing a open-circuit voltage of 1.70 V. Compared with the theoretical power generation limit for a diode bridge rectifier (2.10) with 0.23 V diode drop, this is 3.37x improvement. Note this does not include the power overhead required to operate the SSHI circuit. Compared with the SSHI

theoretical power limit (2.16), the implementation achieves 75 % of its theoretical value.

However the SSHI-DC technique can be improved on by removing the voltage clamp on the piezoelectric output voltage by the bridge rectifier on the output, $V_{\text{clamp}} = \pm (V_{\text{out}} + 2V_{\text{D}})$. To overcome this limitation a new technique known as pre-biasing was proposed by [42].

2.3.6 Piezoelectric Pre-biasing

Piezoelectric pre-biasing increases electrical damping by transferring a small amount of charge from the energy storage device, V_{cc}, to the piezoelectric beam through synchronous switching (Figure 2.27) [42]. The charge generates a piezoelectric force which opposes the motion of the beam as it bends, thus increasing the work done and the power generated. When the beam reaches the opposite extreme point of travel, both the pre-bias and beam bending induced charge is transferred to the energy storage device, V_{out}, before a small amount of charge with the opposite polarity is transferred onto the piezoelectric beam from V_{cc} and the process repeats (Figure 2.28). Switches are required to control the charge transfer between the piezoelectric beam, the pre-bias voltage supply, V_{cc}, and the energy storage device, V_{out}.

Figure 2.27 shows a circuit diagram used to implement the pre-biasing technique. The pre-bias charge, depending on the direction of the beam has deflected to, is transferred from V_{cc} to the piezoelectric capacitor through either switch pair $S_1 - S_4$ or $S_2 - S_3$. The inductors in each path enable near lossless charge transfer to the piezoelectric capacitance through either diodes, D_1 or D_2. To extract power, charge is transfered from the piezoelectric material to an the storage device, V_{out}, through a buck converter controlled by either switches S_5 or S_6depending on the polarity of the voltage across the piezoelectric capacitor.

Under optimal voltage control the peak voltage across the piezoelectric material is not clamped by diodes, thus more energy can be extracted than SSHI-DC (Figure 2.28). If a non-optimal voltage is applied then diodes $D_{\text{A}}, D_{\text{B}}, D_{\text{C}}$ and D_{D} are necessary to provide free-wheeling current paths and the applied pre-bias voltage is clamped at V_{cc} by D_1 and D_2 [6].

Whilst the circuit shown in Figure 2.27 can extract more power than other techniques, it

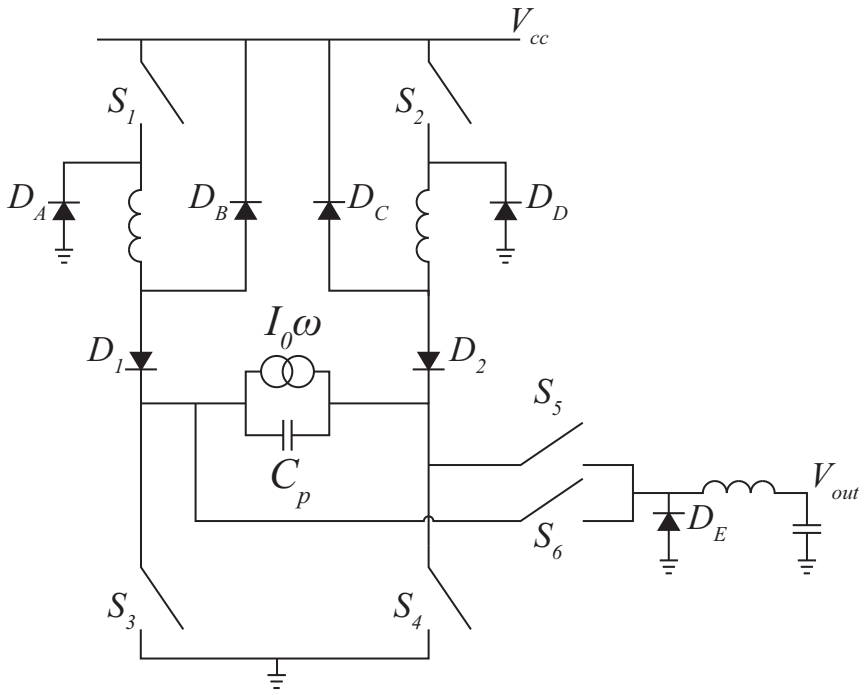


Figure 2.27: Pre-biasing circuit topology with Buck output stage [42].

requires six switches, seven diodes and three inductors in order to pre-bias and discharge the piezoelectric energy harvester into a battery. This is significantly more than other topologies require [34], however Figure 2.29 shows one efficient implementation known as Single Supply Pre-biasing (SSPB) which requires less components than the original circuit [42]. The SSPB circuit also applies a pre-bias voltage from a battery however unlike Figure 2.27 the extracted power is returned to the same battery through the top pair of switches. Note a switch mode power supply circuit could also be added to the SSPB topology similar to Figure 2.27 if the required V_{cc} voltage is different to the target battery voltage.

The SSPB circuit is constructed from a H-bridge with an inductor connected in series with the piezoelectric harvester across the centre of the H-bridge. Switches are fired in pairs ($S_1 - S_4$ and $S_2 - S_3$) to control the current flow between the pieoelectric harvester and the pre-bias V_{cc} rail. When the cantilever is at maximum deflection, one pair of switches are closed to place a charge on the piezoelectric capacitor over half the LC resonance cycle. The switches are

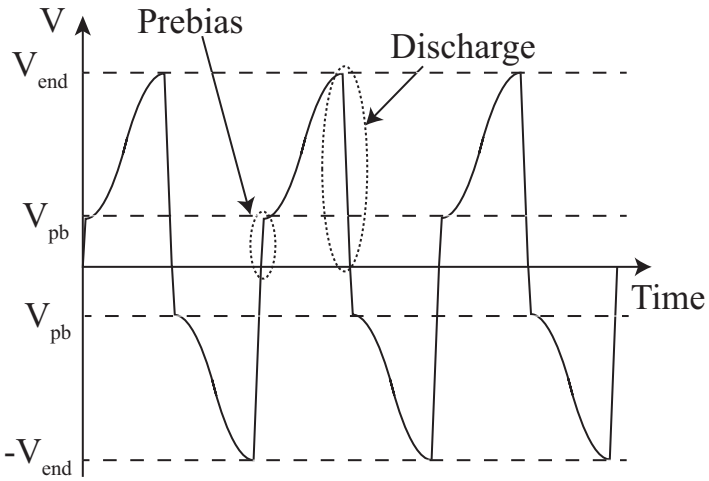


Figure 2.28: Charge and discharge waveform.

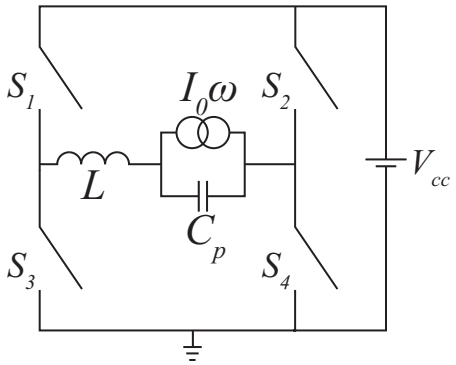


Figure 2.29: Single supply pre-biasing circuit.

then opened, electrically isolating the piezo as the beam deflects in the opposite direction. The deflection causes stress across the piezoelectric material inducing an increase in voltage until the maximal point of deflection in the opposite direction is reached. The same set of switches close for half an LC resonance cycle discharging the piezoelectric capacitor, C_{p} into the V_{cc} supply. The material is then pre-charged with the opposite polarity through the second set of switches and the cycle repeats (Figure 2.28).

The maximum theoretical power that can be generated using the SSPB technique was derived in [6] and included here for completeness. Expressions for the energy required to pre-bias the piezoelectric beam, E_{in}, and the energy returned on discharge, E_{dis}, are found by considering

the energy transfer between the piezoelectric capacitance and the voltage supply.

$$E_{\text{in}} = C_{\text{p}} {V_{\text{cc}}}^2 (1+\gamma) \tag{2.17}$$

$$E_{\text{in}} = C_{\text{p}} V_{\text{PB}} V_{\text{cc}} \tag{2.18}$$

$$E_{\text{dis}} = C_{\text{p}} V_{\text{end}} V_{\text{cc}} \tag{2.19}$$

Where γ is the fractional capacitor voltage conserved by an RLC circuit with a quality factor Q and V_{end} is the voltage across the piezoelectric beam before discharge. V_{end} can be written as the sum of the pre-bias voltage applied (V_{PB}) and twice the induced open-circuit voltage ($2V_{\text{po}}$). Therefore the discharge energy expression can be re-written as (2.20).

$$E_{\text{dis}} = C_{\text{p}}(2V_{\text{po}} + V_{\text{PB}})V_{\text{cc}} \tag{2.20}$$

Subtracting the energy required for the pre-bias away from the energy returned during discharge gives the overall energy change (2.22).

$$\Delta E = E_{\text{dis}} - E_{\text{in}} \tag{2.21}$$

$$\Delta E = 2C_{\text{p}} V_{\text{cc}} V_{\text{po}} \tag{2.22}$$

The optimal voltage to set the V_{cc} supply occurs when no charge remains on the piezoelectric beam after discharge. Thus the remaining voltage, V_{rem}, across the piezoelectric beam after discharge is zero.

$$V_{\text{rem}} = V_{\text{cc}}(1+\gamma) - \gamma(V_{\text{PB}} + 2V_{\text{po}}) \quad (2.23)$$

$$0 = V_{\text{cc}}(1+\gamma) - \gamma(V_{\text{PB}} + 2V_{\text{po}}) \quad (2.24)$$

$$V_{\text{cc}}(1+\gamma) = \gamma(V_{\text{PB}} + 2V_{\text{po}}) \quad (2.25)$$

$$V_{\text{cc}} = \frac{\gamma}{(1+\gamma)}(V_{\text{PB}} + 2V_{\text{po}}) \quad (2.26)$$

The pre-bias voltage term (V_{PB}) can be replaced with the expression $V_{\text{cc}}(1+\gamma)$ to give (2.32).

$$V_{\text{cc}} = \frac{\gamma}{(1+\gamma)}(V_{\text{cc}}(1+\gamma) + 2V_{\text{po}}) \quad (2.27)$$

$$V_{\text{cc}} = \frac{\gamma}{(1+\gamma)}2V_{\text{po}} + \frac{\gamma}{(1+\gamma)}V_{\text{cc}}(1+\gamma) \quad (2.28)$$

$$V_{\text{cc}} = \frac{\gamma}{(1+\gamma)}2V_{\text{po}} + \gamma V_{\text{cc}} \quad (2.29)$$

$$V_{\text{cc}}(1-\gamma) = \frac{\gamma}{(1+\gamma)}2V_{\text{po}} \quad (2.30)$$

$$V_{\text{cc}} = \frac{\gamma}{(1+\gamma)(1-\gamma)}2V_{\text{po}} \quad (2.31)$$

$$V_{\text{cc}} = \frac{\gamma}{(1-\gamma^2)}2V_{\text{po}} \quad (2.32)$$

Inserting (2.32) into (2.22) gives the maximum amount of energy that can be extracted in a single half cycle.

$$\Delta E = 2C_{\text{p}}\frac{\gamma}{(1-\gamma^2)}2V_{\text{po}}V_{\text{po}} \quad (2.33)$$

$$\Delta E = 4C_{\text{p}}{V_{\text{po}}}^2\frac{\gamma}{(1-\gamma^2)} \quad (2.34)$$

Multiplying the change in energy per half cycle by twice the mechanical excitation frequency, f_0, gives the theoretical maximum power limit for the SSPB technique.

$$P_{\max} = 8 f_0 C_{\mathrm{p}} {V_{\mathrm{po}}}^2 \frac{\gamma}{(1-\gamma^2)} \tag{2.35}$$

Using the approximation $\gamma \approx e^{-\frac{\pi}{2Q}}$ for the fraction of voltage conserved on the capacitor of an RLC oscillator [34] and truncating the expansion after the first order ($\gamma \approx 1 - \frac{\pi}{2Q}$), the theoretical maximum power limit can be written in terms of electrical Q-factor.

$$P_{\max} = {V_{\mathrm{po}}}^2 f_0 C_{\mathrm{p}} \left(\frac{8Q}{\pi} \right) \tag{2.36}$$

Equation 2.36 shows that the SSPB circuit has twice the theoretical maximum power extraction compared to the SSHI DC implementation (Equation 2.16). This can be attributed to the fact that in the SSHI implementation, the entire charge must be flipped on the piezoelectric material whereas in the SSPB circuit, only half the energy must travel through the inductive paths [6].

2.4 Effectiveness of Practical Implementation of Harvesters

Tables 2.1, 2.2 and 2.3 show the power density and system effectiveness for manufactured electromagnetic, electrostatic and piezoelectric energy harvesters made between 2006 and 2013. The collection of data was undertaken by the author, M. R. Trice and P. D. Mitcheson [3].

The power density is calculated from the reported output power at any frequency and displacement, then divided by the volume. Therefore a device's power density should only be compared against another device under similar test conditions.

$$\text{Power density} = \frac{\text{Output power}}{\text{Volume}} \tag{2.37}$$

A more useful metric to compare performance of energy harvesters is system effectiveness [23]. This compares the reported power output against the maximum possible power available to be harvested for a set of conditions [36]. Therefore different devices can be compared by

their effectiveness to extract the most power available to them.

$$\text{Available power} = \frac{1}{2} {Y_0}^2 \omega^3 m \frac{Z_\text{l}}{Y_0} \tag{2.38}$$

$$\text{System effectiveness} = 100 \times \frac{\text{Output power}}{\text{Available power}} \tag{2.39}$$

where Y_0 is the input excitation displacement, ω is the excitation frequency, m is the mass and Z_l is the maximum displacement allowed by the design.

Year	Volume [cm^3]	Frequency [Hz]	Input displacement [μm]	Proof Mass [g]	Output power [μW]	Power density [μWcm^{-3}]	System Effectiveness [%]	
2003	2.10E+00	700	6.5	5.40E-01	4.00E-04	1.90E-04	5.46E-08	[44]
2003	7.30E+00	85	7500.0	1.40E-01	8.30E+02	1.14E+02	5.13E-02	[45]
2004	8.40E-01	322	360.0	0.00E+00	3.70E+01	4.40E+01	8.67E-03	[46]
2006	6.00E-02	350	217.0	4.40E-01	2.85E+00	4.75E+01	3.68E-01	[47]
2006	6.80E-02	9500	240.0	2.80E-02	1.22E-01	1.79E+00	4.21E-04	[47]
2007	3.60E-02	100	5200.0	3.20E-02	1.44E+00	4.00E+01	1.95E-01	[48]
2008	1.35E+00	300	15.0	1.60E+00	5.00E+01	3.70E+01	2.00E-02	[49]
2009	2.10E+00	10	500.0	9.00E+00	5.80E+00	2.76E+00	7.31E-02	[50]

Table 2.1: Comparison of electromagnetic energy harvesters.

Year	Volume [cm^3]	Frequency [Hz]	Input displacement [μm]	Proof Mass [g]	Output power [μW]	Power density [μWcm^{-3}]	System Effectiveness [%]	
2002	1.49E+01	6	9000.00	7.80E+02	3.60E+01	2.42E+00	1.93E-02	[51]
2003	6.00E-01	743	0.64	7.00E-01	7.40E-06	1.23E-05	2.11E-09	[44]
2004	4.00E-01	10	1000.00	6.52E-01	6.00E+00	1.50E+01	7.72E-01	[52]
2006	1.80E+01	50	90.00	1.04E+02	1.76E+03	5.56E+01	7.15E-02	[53]
2006	6.00E-01	20	1125.79	1.20E-01	2.40E+00	4.00E+00	2.00E-02	[54]
2008	1.35E+00	1460	1.50	6.47E-04	1.32E+00	9.78E-01	5.25E-05	[55]
2008	1.80E+01	6	2758.00	0.00E+00	6.00E+01	3.33E+00	5.91E-01	[56]
2008	1.00E+01	9	92.00	0.00E+00	1.30E-07	1.30E-08	2.49E-08	[57]
2008	7.20E-01	1090	3.00	3.30E-03	2.93E-02	4.07E-02	3.24E-06	[58]
2009	1.53E+00	63	125.00	1.00E-01	1.00E+00	6.55E-01	5.04E-03	[59]
2010	1.53E+00	63	62.61	4.00E-01	0.00E+00	0.00E+00	0.00E+00	[60]
2010	1.60E+00	30	41.00	3.60E+00	1.00E+02	6.25E+01	1.34E+01	[61]
2010	1.60E+00	45	46.00	3.00E+00	1.70E+01	1.06E+01	6.00E-01	[62]
2011	1.80E+00	40	21.70	8.50E-02	6.00E+00	3.33E+00	5.46E-01	[63]
2011	2.00E+00	190	13.80	2.68E-01	6.74E+01	3.37E+01	7.82E-02	[64]

Table 2.2: Comparison of electrostatic energy harvesters.

Year	Volume [cm^3]	Frequency [Hz]	Input displacement [μm]	Proof Mass [g]	Output power [μW]	Power density [μWcm^{-3}]	System Effectiveness [%]	
2003	1.00E+00	120	4.00	8.50E+00	8.00E+01	8.00E+01	9.57E-01	[65]
2003	1.00E+00	85	7.90	7.50E+00	2.07E+02	9.00E+01	1.53E+00	[65]
2003	1.00E+00	60	16.00	8.20E+00	3.65E+02	1.80E+02	4.31E+00	[65]
2003	4.80E+00	40	36.00	5.22E+01	1.70E+03	1.46E+02	3.10E+00	[66]
2006	6.16E-04	609	4.40	1.56E-03	2.16E+00	3.51E+03	3.43E+00	[67]
2005	2.00E-01	100	184.15	9.60E-01	3.55E+01	8.17E+01	6.28E-02	[68]
2008	3.75E+00	870	2.60	4.20E-03	1.32E+00	3.01E+02	1.09E-05	[69]
2008	2.00E+00	70	31.00	2.30E+00	1.17E+02	5.85E+01	3.61E-01	[70]
2008	1.00E+00	571	1.52	8.77E-03	6.00E+01	6.00E+01	1.75E-02	[71]
2008	3.60E-01	8810	0.40	4.20E-04	4.18E-04	1.16E-03	4.93E-10	[72]
2009	2.00E+00	49.6	20.00	4.80E-01	7.20E+00	3.60E+00	9.68E-02	[73]
2009	3.13E+00	50	10.00	1.47E+00	1.00E-01	3.20E-02	1.45E-03	[74]
2010	7.50E-01	205	0.60	2.80E-01	7.56E+00	1.01E+01	1.77E-01	[75]
2011	7.20E-02	59	103.00	9.45E-03	8.98E-03	1.25E-01	1.17E-03	[76]
2011	8.00E+00	27.4	99.00	3.07E-03	1.12E-03	1.40E-04	2.83E-06	[77]
2011	2.00E+00	247	4.10	2.08E-02	3.71E+01	1.86E+01	1.97E-02	[78]
2011	3.38E+00	268	3.46	8.37E-03	6.50E-01	1.93E-01	1.59E-04	[79]

Table 2.3: Comparison of piezoelectric energy harvesters.

2.5 Summary

In this chapter, a preliminary literature review on energy harvesting introduced 3 vibrational energy harvesting transduction methods (electromagnetic, electrostatic and piezoelectric). For piezoelectric harvesters, the interface circuit options were explored and the SSPB circuit was identified as theoretically outperforming the next best known technique SSHI by a factor of two. The next chapter therefore will look at how the SSPB technique can be implemented.

3 Implementation of the Single-Supply Pre-biasing Circuit

In the previous chapter, the single-supply pre-biasing (SSPB) circuit was identified as theoretically achieving twice the maximum power of the next best known technique, synchronised switch harvesting on inductor (SSHI). However it has never been experimentally implemented. This chapter presents a high level design required to implement the SSPB circuit. For each component of the high level design, possible solutions are presented and evaluated. Experimental results and the best performing design are presented at the end of the chapter.

3.1 Implementation overview

The basic topology of the SSPB circuit is a piezoelectric energy harvester connected in series to an inductor across the centre of a H-bridge circuit consisting of switches capable of blocking and conducting in both directions to a voltage source (Figure 3.1). The piezoelectric harvester needs to be isolated from the voltage source whilst the beam is moving from one point of maximum displacement to the other. When the beam reaches its maximum displacement, the switches need to be closed and re-opened in pairs $(S_1 - S_4)$ and $(S_2 - S_3)$ in the correct sequence depending upon which extreme point of motion has been reached and for the correct length of time equal to ensure the LC resonant circuit switches under zero current conditions.

In practical situations, such as a car journey the vehicles engine power and/or vehicle accelerations will vary throughout its journey, causing the mechanical excitation force, A_{input},on the

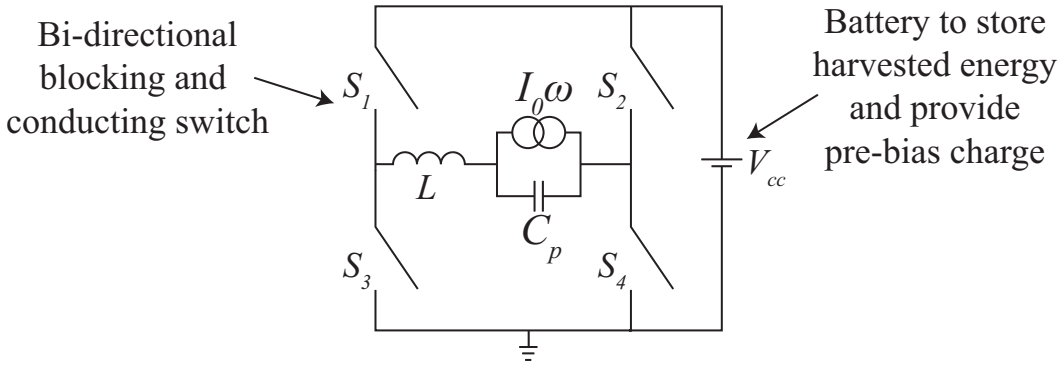


Figure 3.1: Single supply pre-biasing circuit.

beam to correspondingly vary significantly in timing and frequency, f_0 [80]. For maximum power extraction, the SSPB circuit must be able to continuously adapt the switching cycle timing to match the timing of this mechanical excitation. Similarly, the voltage of the battery should be variable so that the SSPB circuit can apply the appropriate voltage to the piezoelectric material to achieve the optimal stiffness for coupling the maximum amount of mechanical energy into the beam. Finally, to maximise the overall circuits efficiency, the power consumption required to operate the SSPB circuit, device power loss and control system power consumption must be minimised.

Implementation of the SSPB circuit can be considered as four sub-circuits plus the piezoelectric beam itself (Figure 3.2). The peak detection circuit detects when the beam is at its extreme points of travel to enable the switching operations to be synchronised to the motion of the beam. The H-bridge circuit constructed from bidirectionally conducting and blocking switches to pre-bias and discharge the piezoelectric beam H-bridge circuit. The control circuit implements the switching sequence and conduction time. The energy storage circuit is responsible for charging the battery and providing the pre-bias energy.

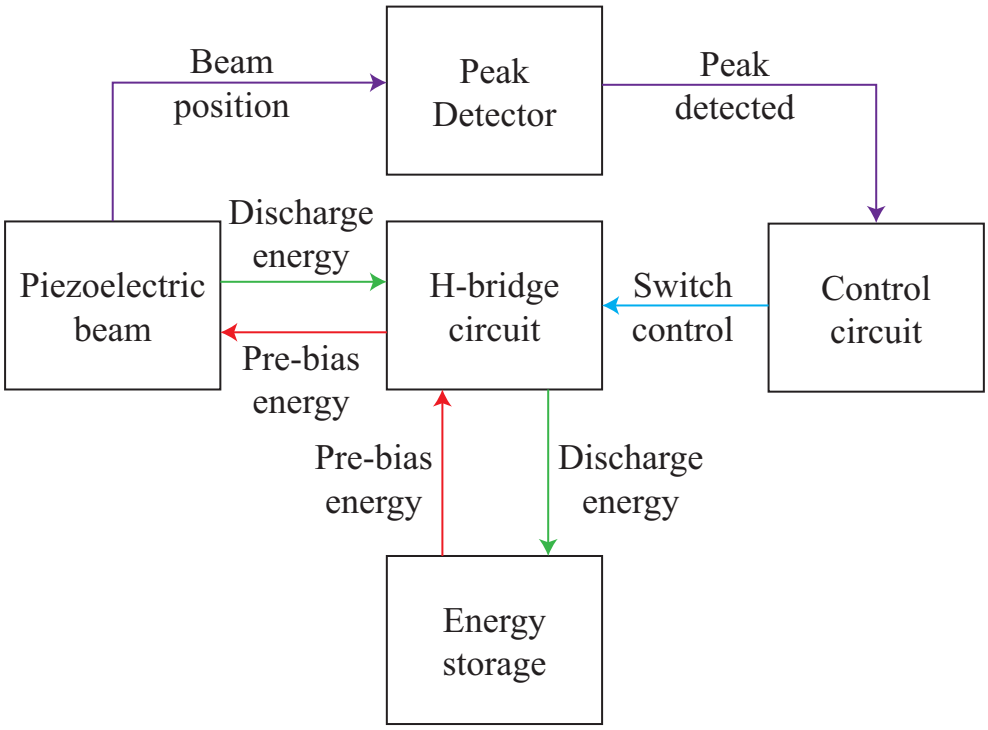


Figure 3.2: High level design of the single supply pre-biasing circuit. The red arrows indicate energy transferred from the energy storage device (e.g. a capacitor or battery) to the piezoelectric energy harvester, whereas the green arrows indicate energy transferred from the harvester to the energy storage circuit. The purple arrows indicate the direction of the sense signal used for peak detection and the blue arrow shows the direction of the switch control required to implement the SSPB scheme.

3.2 Peak Detection Circuit

Maximum power extraction is achieved when the piezoelectric beam is discharged and pre-biased at the extreme point of travel. It is therefore imperative to detect when this event occurs. The extreme point of travel occurs when the induced voltage across the piezoelectric material is at a peak and the induced piezoelectric current is equal to zero. In order to measure these parameters a secondary "sense" piezoelectric beam was mechanically coupled to, but electrically isolated from, the piezoelectric energy harvester beam. This was necessary as it reduced the voltage range the detection circuits had to operate in and it was found that the glitches occurred when using the harvesting piezoelectric beam as a sense voltage when the SSPB technique was

applied. Several methods of peak detection were subsequently designed, tested and evaluated against there accuracy, immunity to noise, and power consumption.

3.2.1 Analogue to Digital Converter

An analogue to digital converter (ADC), combined with a microcontroller for data processing, may be used for peak detection (Figure 3.3). Analogue to digital conversion algorithms sample the continuous time voltage waveform and assign a discrete value to the voltage at regular time intervals [81]. The microcontroller then processes the data to find the peaks and troughs in the voltage waveform to trigger switching operation.

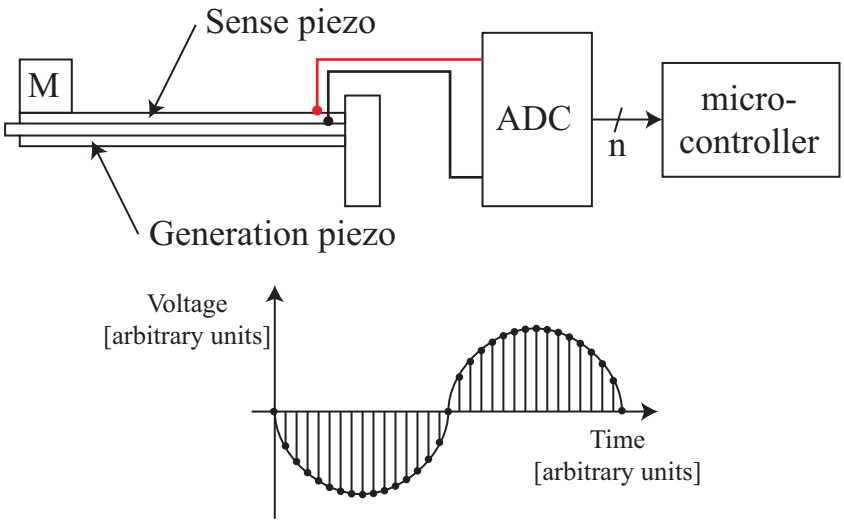


Figure 3.3: Beam displacement measurement system using sense piezoelectric beam monitored by an ADC and microcontroller peak detector.

The use of an ADC in energy harvesting is problematic due to the power required to sample and process the data in real-time. The analogue input is restrictive in terms of frequency and amplitude since the sampling frequency must be significantly higher than the mechanical excitation frequency to accurately detect the peaks and troughs. The ADC is subject to noise so some form of filtering is required to accurately detect the peak, increasing circuit complexity and power consumption.

3.2.2 Zero crossing detector with fixed time delay

A peak detector for a waveform of a known fixed frequency can be made from a zero crossing detector with a fixed time delay added. The zero crossing detection circuit changes it's output to high when the voltage across the piezoelectric beam crosses either above or below zero volts depending on the configuration. It was assumed that the mechanical excitation frequency would be at approximately the same frequency and hence a fixed time delay after the zero crossing event could be added by the microcontroller to predict the peak or trough. To minimise capacitive loading of the piezoelectric beam, the voltage across the sense piezoelectric beam was measured using an instrumentation amplifier with a very high input impedance and very small input capacitance. (Figure 3.4) [35].

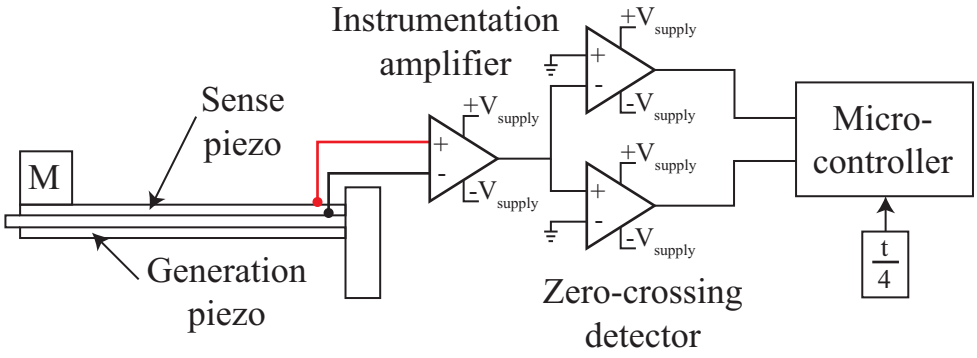


Figure 3.4: Peak detector made from a zero crossing circuit with fixed delay.

This implementation, which was reported at PowerMEMS 2011 [35], successfully implemented the SSPB circuit to improve power extraction. However the instrumentation amplifier had to operate over the full piezoelectric induced voltage range, requiring a dual supply (±18 V), and drawing a large quiescent current. Thus a large amount of energy was used to power the control circuitry.

3.2.3 Low-power peak detector

A more power efficient implementation which was independent of the excitation frequency was required. A low-power peak detection circuit was developed which compared the instantaneous voltage against a lossy peak-hold copy held on a capacitor (Figure 3.5). The piezoelectric sense signal was level shifted using a potential divider and the differential voltage was measured using a single-supply low power OPAMP (Analog AD8500 [82]). The instantaneous voltage from the OPAMP is then split by a pair of forward and reverse facing diodes connected to two low power comparators (Microchip MCP6542 [83]) to detect both the peaks and troughs in the waveform. Capacitors in parallel with resistors were placed on one of the inputs to each comparator to create a lossy peak-hold of copy of the voltage. The comparator compares the instantaneous voltage with the peak-held voltage and determined when a peak or trough occurred (Figure 3.6).

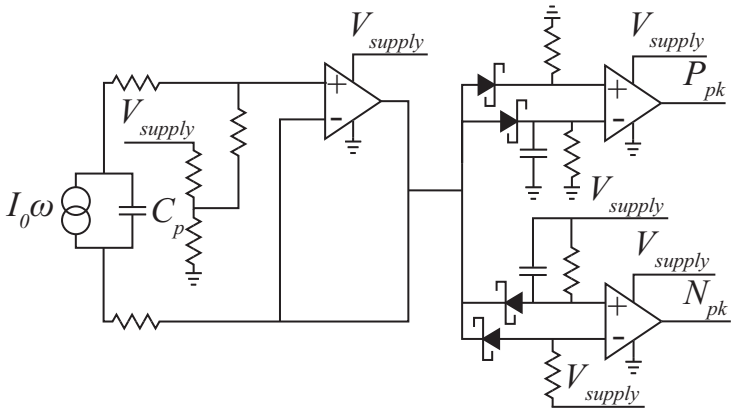


Figure 3.5: Low power peak detection circuit which compares the instantaneous voltage against a lossy peak-hold copy held on a capacitor [84].

This circuit successfully implement SSPB, as reported at Eurosensors 2012 [84] and IEEE Sensors 2012 [85], although the power consumption of the circuit (96 μW [85]) needed to be reduced to improve the power efficiency. The power losses in the circuit were analysed and the current drawn by the output of the OPAMP was identified to as the main power loss. The lossy peak-hold capacitor and resistor circuit was therefore modified to minimise this current and the new power consumption was measured at 8.64 μW, a 91 % saving in power [86].

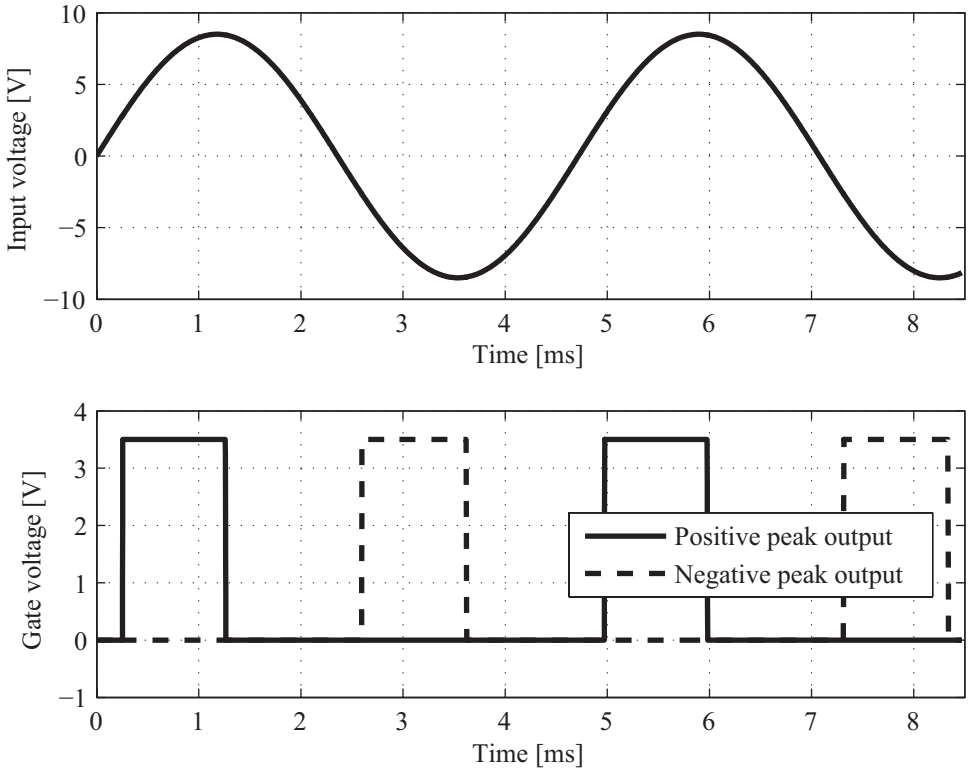


Figure 3.6: Low power peak detection circuit which compares the instantaneous voltage against a lossy peak-hold copy held on a capacitor [84].

3.2.4 Level-shifted peak detector

Another peak detection circuit which was considered and tested was a level-shifted peak detector (Figure 3.7) [87]. The circuit was designed to minimise power consumption by removing the need for the differential OPAMP. The piezoelectric beam was connected to a diode bridge rectifier circuit with a capacitor. The rectifier circuit caused the voltage to be level shifted up by half the induced open-circuit voltage of the piezoelectric beam, without requiring any additional power. Two zero crossing detectors were connected to either side of the piezoelectric beam resulting in the comparators measuring inverted signals to each other. Since the original signal had been level shifted the extreme points of motion of the beam now conincided with the zero crossings of the comparators.

Power consumption was further minimised by connecting the drain and gate pins of an n-

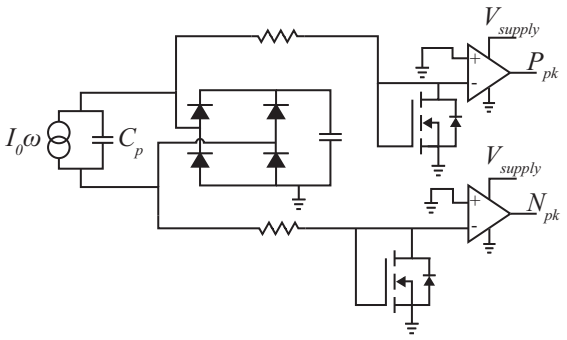


Figure 3.7: Level shift peak detection circuit [87].

type enhancement mode MOSFET to the either side of the piezoelectric beam and the source to ground. The induced voltage across the sense piezoelectric beam is therefore pinned to the MOSFET gate turn-on voltage thereby protecting the comparator's input pin from over-voltage and minimising the supply voltage rail required to run the device. This peak detector, whose PSpice simulation and experimental voltage waveforms are shown in Figure 3.8 consumed 2.72 μW when used with SSPB circuit. However this circuit requires the sense piezoelectric beam to remain in-phase with the generation piezoelectric beam but unaffected by the pre-biasing applied to the generating piezoelectric beam.

3.2.5 Period measured peak detector

The SSPB implementations demonstrated so far, all require a secondary sense piezoelectric beam to provide a reference voltage, which reduces the achievable power density of the energy harvester. An alternative design was simulated which replaced the need for the secondary sense beam by isolating the power generating piezoelectric beam for a cycle and measuring its period (Figure 3.9). This value can then be used to estimate the timing of several subsequent peaks and troughs, before remeasuring the period.

The period is measured by comparing the voltage across the piezoelectric beam with a copy halved by a potential divider. A comparator then detects the zero crossings and the time between events is measured by a counter. Figure 3.9b shows the simulated output from the circuit. Using

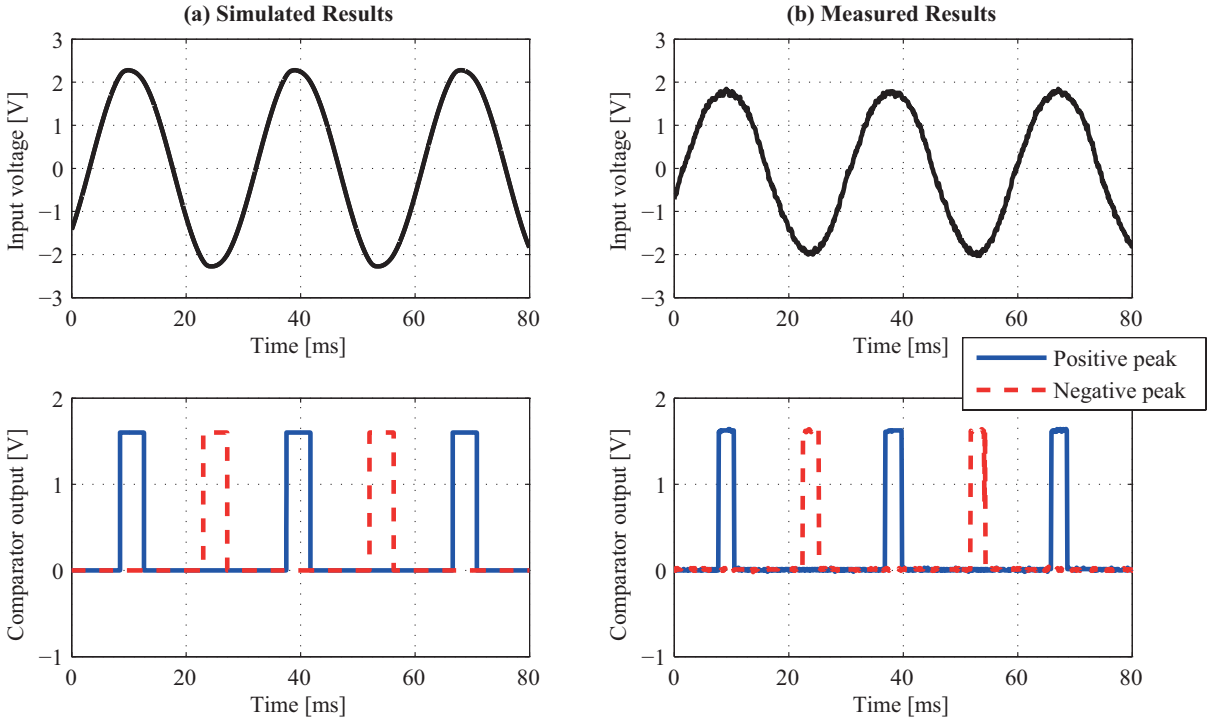


Figure 3.8: Level shift peak detection circuit output from (a) Orcad's PSpice simulation, and (b) experimental measurement [87].

this prediction method in the SSPB circuit is more complicated as the resolution of the clock needs to be carefully selected to balance power consumption against timing accuracy. A very fast clock will accurately measure the period of the induced voltage and any offset errors when estimating the timing will be minimised. However this will be highly power intensive reducing the efficiency of the system. Conversely a slow clock will consume very little power, but will lead to a much higher degree of inaccuracy in measuring the period. When the inaccurate period is used over several cycles it will lose synchronisation with the incoming peaks.

3.3 Switch design

Pre-biasing and discharging the piezoelectric beam with the pre-biasing capacitor requires switches capable of conducting current and blocking voltages in both directions. The on-time of

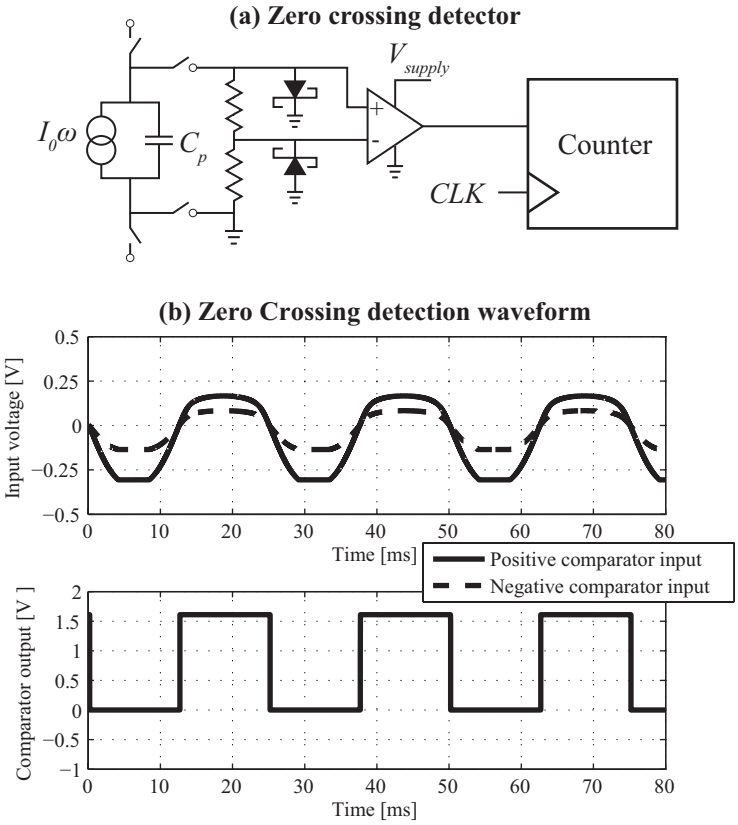


Figure 3.9: Period measured peak prediction circuit [87].

the switches must be precisely set to ensure switching occurs when there is zero current flowing through the inductor. The turning on and off times of the switches must therefore be as short as possible. Power consumption of the switches must be also be taken into account to maximise system efficiency.

3.3.1 TRIACs

The initial requirement was to find a switch capable of conducting current and blocking voltages in both directions. Mechanical based switches such as relays were ruled out due to their slow switching speed and mean time to mechanical failure when being oscillated at several hundred hertz (e.g. a reed relay rated at 1 billion cycles [88], oscillated at 200 Hz will last less than 58 days). Instead electronic switches capable of controlling an alternating current (TRIAC)

were initially considered.

TRIACs are three terminal devices (anode 1, anode 2, and gate) which act as bidirectional thyristors (Figure 3.10). When a current is injected into or drawn from the gate terminal of the TRIAC, the device is switched on and current can flow in either direction through the device. Once triggered, the TRIAC will switch off when the current through the anode terminals falls below a minimum holding current. The sinusoidal nature of the pre-bias and discharge current therefore lends it self to the use of TRIACs.

Figure 3.10: TRIAC schematic symbol.

In [35] TRIACs were used with a microcontroller to demonstrate the single-supply pre-biasing technique. Figure 3.11 shows how the H-bridge circuit configuration can be constructed from Fairchild MOC3011 optically isolated TRIACs [89]. These use an infrared diode to trigger the gate signal on the TRIAC when a voltage is applied to their input.

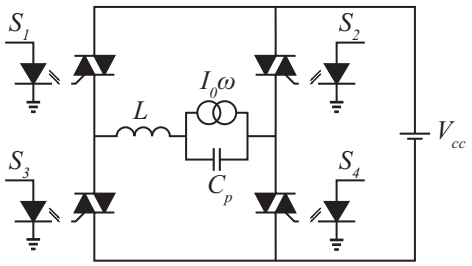


Figure 3.11: SSPB circuit implemented with a TRIAC.

A SSPB H-bridge circuit constructed solely from optically isolated TRIACs will consume a large amount of power due driving four infrared diodes. An estimation based on values in [35], can be made since each TRIAC typically requires 1.15 V at 10 mA [89] for a period of 2.5 μs to switch the device on. The energy consumed per cycle is equal to both TRIAC switch pairs

($S_1 - S_4$, $S_2 - S_3$) being switched on twice (3.2). Multiplying the energy per cycle by the mechanical frequency (45 Hz in [35]) results in switch power consumption:

$$E_{\text{TRIACperCycle}} = N_{\text{events}} N_{\text{switch}} \tau V_{\text{F}} I_{\text{F}} \tag{3.1}$$

$$E_{\text{TRIACperCycle}} = 2 \times 4 \times 2.5\mu\text{s} \times 1.15\text{V} \times 10\text{mA} \tag{3.2}$$

$$E_{\text{TRIACperCycle}} = 230\ nJ \tag{3.3}$$

where N_{events} is the number of switching events required for a pre-bias and discharge, N_{switch} is the number of switches in the H-bridge circuit, τ is the switch on-time, V_{F} is the forward voltage drop across the infrared diode, and I_F is the current required by the infrared diode.

$$P_{\text{TRIAC}} = E_{\text{TRIACperCycle}} f_0 \tag{3.4}$$

$$P_{\text{TRIAC}} = 230\text{nJ} \times 45 \tag{3.5}$$

$$P_{\text{TRIAC}} = 10\ \mu W \tag{3.6}$$

where f_0 is the mechanical excitation frequency.

The TRIAC power consumption estimate assumes the controller voltage output is the same as the forward voltage drop across the infrared diode, hence no protective resistor is required to step the voltage down and limit the current. If this is not the case, the power loss estimation will be an under estimate.

An improvement to the power consumption of the TRIACs can be made by replacing the low side TRIACs with MOSFET switches. The high side TRIACs prevent a current path forming as they can block in both directions whilst the low-side MOSFETs prevent shoot through and minimise on-state voltage drop. This configuration (Figure 3.12) was used in [35].

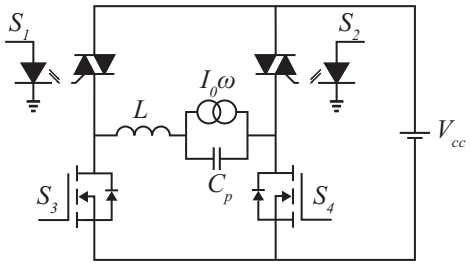


Figure 3.12: SSPB H-bridge circuit implementation with high side TRIACs and low side MOSFETs.

3.3.2 BJTs

A switch design used to demonstrate the SSHI technique [41] was considered (Figure 3.13). It is comprised of an n-type bipolar junction transistor (BJT) series connected with a diode then parallel connected to p-type BJT with a series connected diode [41]. This has the advantage of a much faster response than the TRIAC design, but requires many more devices to implement (Figure 3.14) and the extracted power from the harvester is reduced due to the voltage drops across the diodes. This technique also limits the minimum induced voltage by the piezoelectric harvester reducing the SSPB's usable range.

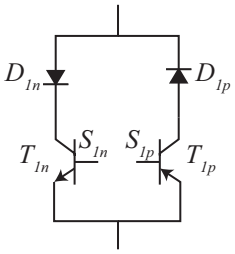


Figure 3.13: Bidirectional switch made from two BJTs and two diodes [41].

3.3.3 MOSFETs

The voltage drops across the diodes is clearly an undesirable characteristic, therefore replacing the BJTs with another switch is necessary. An improved solution is to use series connected n-type and p-type metal-oxide-semiconductor field-effect transistors (MOSFETs) Metal-Oxide-

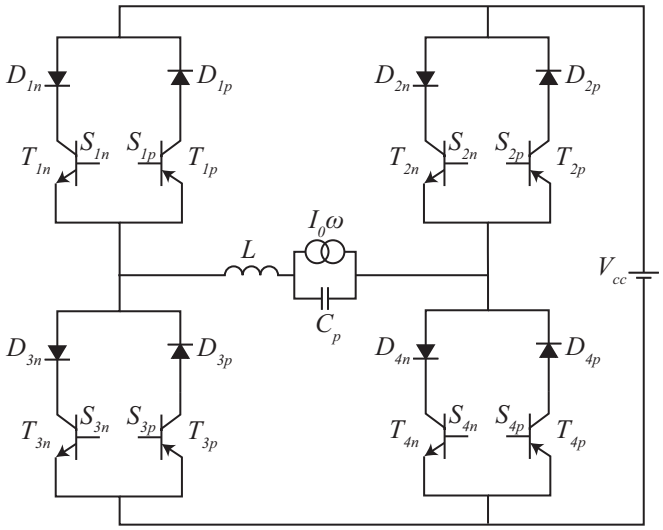


Figure 3.14: SSPB implementation using a bidirectional BJT based switch.

Semiconductor Field-Effect Transistors (Figure 3.15).

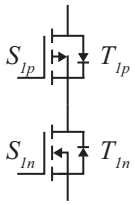


Figure 3.15: Bidirectional switch made from two series connected MOSFETs [84].

Figure 3.16 shows the SSPB circuit with the MOSFET switches. On the low-side the proposed MOSFET based switch is used, however on the high side, only a single device is required as the low-side switch prevents a conduction path from forming [84]. This arrangement has the advantage of very fast switching speeds, with low on-state voltage drop provided the on-state resistance of the MOSFETs is small.

The on-time for the switches is very short (due to a high frequency electrical RLC resonant path) compared with the relatively slow mechanical excitation frequency. Thus the duty cycle of the switches is very low. The low side n-type MOSFETs require a positive voltage greater than their threshold voltage across the gate-source terminals to switch the devices on. Conversely the p-type MOSFETs require a negative voltage across their gate-source terminals. These signals

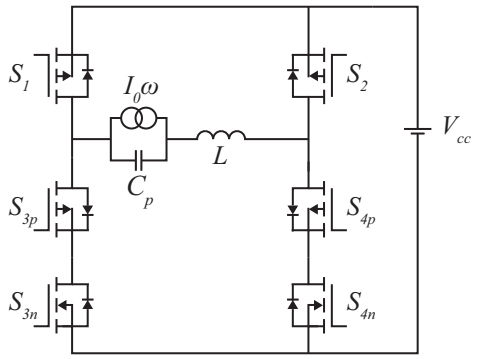


Figure 3.16: SSPB implementation using a bidirectional MOSFET based switch.

can be generated by gate driver chips (e.g. National Semiconductor LM5109 [90]), but their quiescent current requirements can be too power intensive for micropower applications (e.g. a single LM5109 draws 185 μA at 8V [90]).

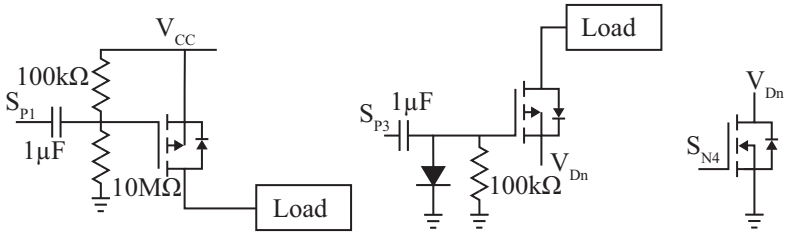


Figure 3.17: Gate drive circuit for MOSFET SSPB circuit [84].

The n-type MOSFET can be driven directly from a controller provided the voltage exceeds the MOSFET threshold voltage, however for the p-type MOSFETs, instead of a gate driver chip, level shifting circuits can be used constructed from capacitors, diodes, and resistors (Figure 3.17). The low side p-type MOSFET signal can be inverted by the controller with respect to the series connected n-type MOSFET's signal, removing the need for a negative supply rail. The inverted gate signal can be level shifted using a 1 μF capacitor and a diode with a large resistor (100 kΩ) in parallel. A large capacitor compared with the MOSFET's gate capacitance is used to ensure the device remains fully on whilst conducting. When the inverted gate signal is high, the diode clamps the voltage on the p-type MOSFET's gate terminal to one diode voltage drop above zero volts. However when the gate signal is pulled low, the voltage on the

gate terminal is pulled negative by the same amount, creating a negative voltage across the MOSFET's gate source terminals, switching the device on.

The high side p-type MOSFET uses a potential divider constructed from a 100 $k\Omega$ resistor and a 10 $M\Omega$ resistor connected in series to the pre-bias storage battery, V_{cc}. The values of the resistors are large to minimise power losses. The centre point of the potential divider connects to the MOSFET gate terminal and a 1 μF decoupling capacitor. The value of the decoupling capacitor is a compromise between ensuring the switch remains fully on and switching losses. The larger the value, the longer the on-time of the switch can be however, the higher the switching losses become. The same inverted controller signal for the low side p-type MOSFET is fed through the high side decoupling capacitor. When the signal is high, the MOSFET gate terminal is held at the supply rail voltage. When the signal is pulled low, the DC capacitor is now referenced to ground. The gate voltage is reduced by the same amount of voltage as the signal since the voltage across the capacitor is zero, hence generating a negative voltage across the gate-source terminals.

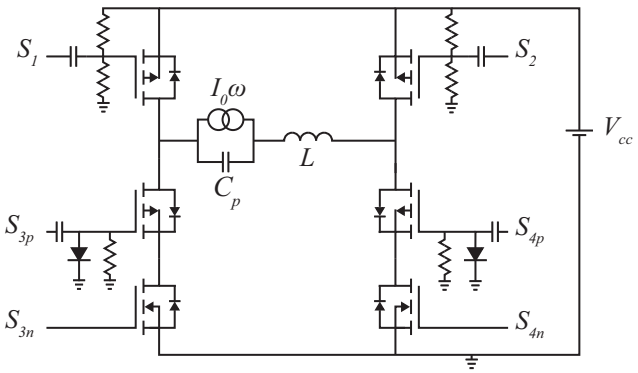


Figure 3.18: SSPB implementation using a bidirectional MOSFET based switch.

Selection of the MOSFETs requires consideration of several parameters. The off-state blocking voltage must be great enough to block the voltages shown in Table 3.1 [85]. These were derived by considering the voltage across the piezoelectric harvester during a complete excitation cycle. However increasing the blocking voltage requires the length between the source and drain to increase. This in turn increases the on-state resistance of the switch which needs to be

minimised to maximise power extraction efficiency. Minimising the MOSFETs' gate capacitance reduces the switching power losses, but increases the size of the device.

Table 3.1: MOSFET voltage blocking requirements

MOSFET	Voltage Rating	Current Rating
High side p-type	$2 \times V_{\mathrm{po}} + V_{\mathrm{pb}}$	I_{p}
Low side p-type	$2 \times V_{\mathrm{po}} + V_{\mathrm{pb}} - V_{\mathrm{cc}}$	I_{p}
Low side n-type	V_{cc}	I_{p}

3.4 Control Circuit

A control circuit is required to provide the gate signals for the SSPB H-bridge switches. Trigger signals from the peak detection circuit are used to turn on the switches and start the switch on-time timer. The gates remain switched on until the on-time timer expires. The period of the on-time, τ, is determined by electrical resonant frequency of the piezoelectric capacitance, C_{p}, and the inductance, L, used in the H-Bridge circuit (3.7).

$$\tau = \pi\sqrt{LC_{\mathrm{p}}} \tag{3.7}$$

Three control circuit implementations (microcontroller, discrete logic gates, and FPGA) were designed, built and evaluated in terms of power consumption, complexity, and physical size.

3.4.1 Micro-controller

Micro-controllers, such as the Arduino micro-controller series [91], provide a fast method of implementing system algorithms. In the first demonstration of the SSPB circuit [35], the Arduino Mega 2560 was used to provide the gate signal for the switches. It was triggered by either the positive or negative peak detection circuits. An output pin was then held high for a pre-set time equal to half the resonant period of the inductor-piezoelectric capacitance charge path, whilst the piezoelectric capacitor was discharged. The timing was performed using the 16 MHz clock

available on the Arduino Mega 2560 circuit board. A second output pin corresponding to the opposite pair of switches on the SSPB circuit was then held high for the same time whilst the pre-biasing voltage was applied. Figure 3.19 shows the set-up and the basic algorithm used.

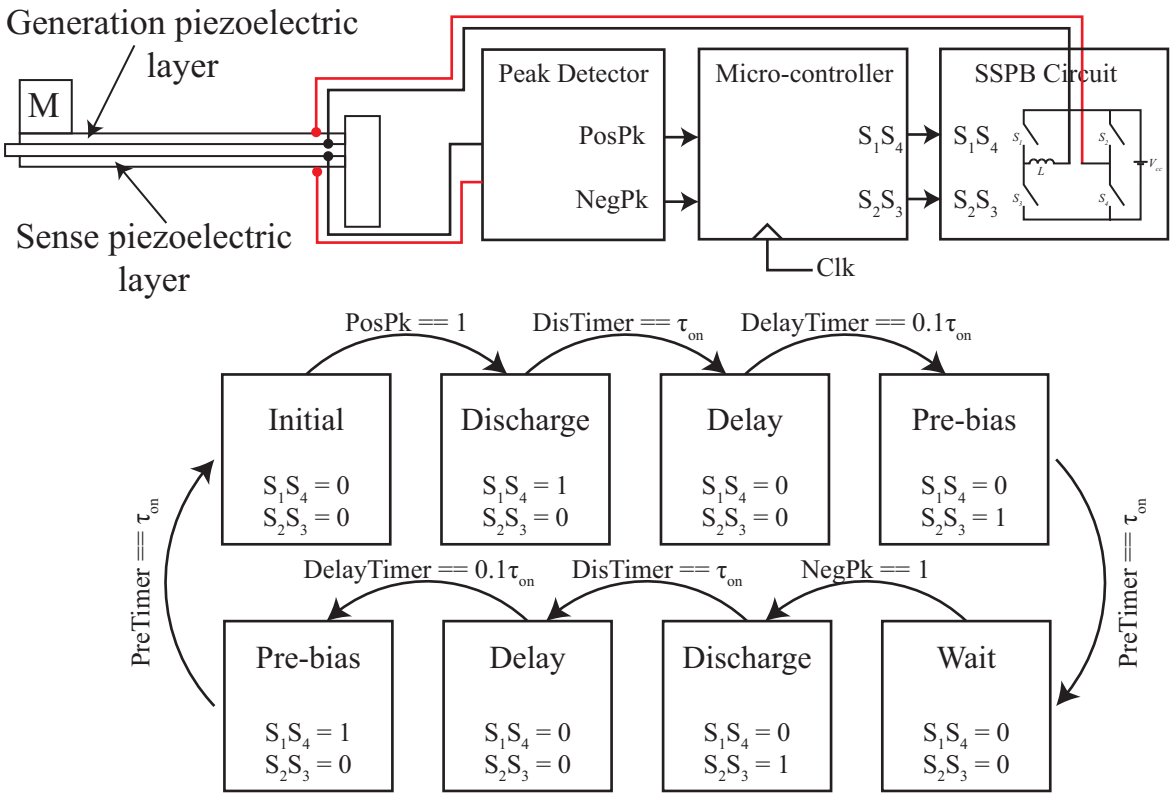


Figure 3.19: Micro-controller and algorithm used to implement the SSPB technique [35].

The on-state timing of the switches was set by varying an integer time delay allowing for simple tuning to be performed. A delay between the discharge and pre-bias signals had to be added to prevent V_{cc} being shorted to ground.

The micro-controller provided a fast method of implementing the SSPB circuit, but required a large power supply overhead due to the need of having a high speed clock. Minimising control power overhead is a key requirement for the power electronics of energy harvesters, therefore methods of implementing the controller without the use of a clock were investigated.

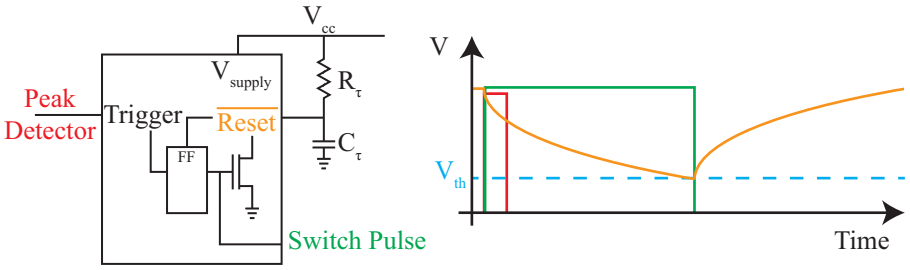


Figure 3.20: Operation of a monostable vibrator.

3.4.2 Discrete Logic Gates

Asynchronous designs use events instead of clock signals to trigger events. In the SSPB circuit's case, the peak detectors can therefore trigger the start of timer to hold the switches closed during their on-state. The length of the on-time can also be controlled using monostable multivibrators (e.g. Texas Instruments CD74HC221 [92] [84]). When monostables are triggered, the corresponding output is then held high until the voltage on the timing pin falls to a set threshold. The rate of voltage fall is set by a series connected resistor and capacitor (Figure 3.20).

The complete control circuit is shown in Figure 3.21 and was presented in [84]. When a positive peak is detected, the peak detection circuit generates a pulse. The falling edge of the pulse can then be used to trigger the positive discharge monostable. Once the RC time constant has expired, the discharge monostable's output triggers a second monostable for the pre-bias gate signal. An identical arrangement is used for the negative peak and the outputs of the positive discharge and negative pre-bias, and positive pre-bias and negative discharge monostable vibrators are connected to OR gates respectively. See Figure

Power consumption of the complete system was measured at 400 μW with the control circuit consuming approximately 200 μW of this [84]. Whilst low power consumption was achieved, the use of multiple discrete components requires a large amount of physical space. Therefore it was desirable to find a method of reducing the number of physical components.

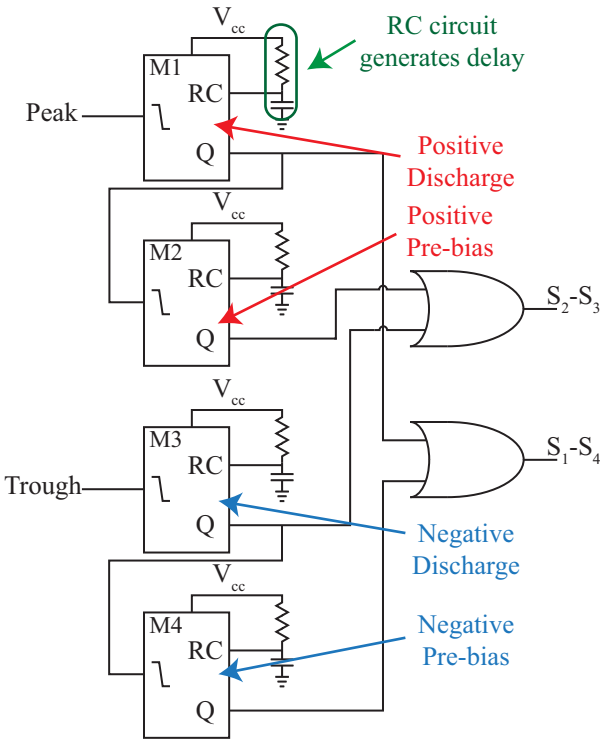


Figure 3.21: Circuit used to generate control timing signals generated from monostable vibrators and OR gates [84].

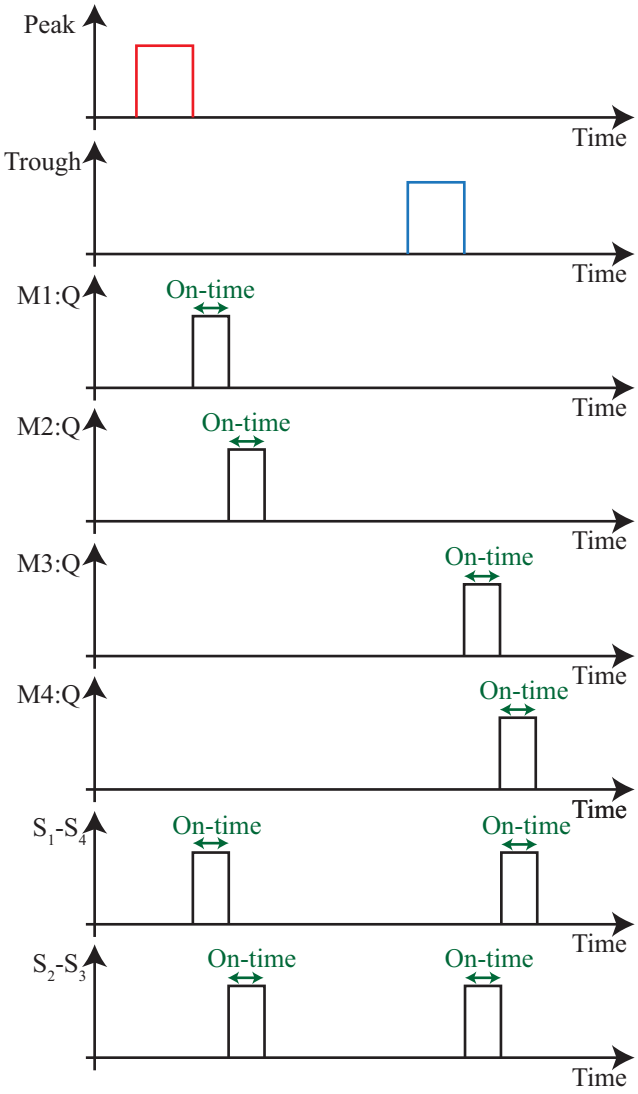


Figure 3.22: Control circuit timing diagram [84].

3.4.3 Low Power FPGA

A FPGA (Field Programmable Gate Array) is made up of programmable cells which emulate logic gates. The control signals for the SSPB technique can therefore be generated by describing the logic circuit required. Figure 3.23 shows the architecture used to demonstrate the control of the SSPB circuit on an FPGA [85].

The positive and negative peak detection signals are passed into the peak and trough input ports respectively. AND gates are used to prevent multiple triggers by the same detector. D-type flip flops provide the appropriate enable signals to the AND gates. The output of the AND gates is then passed to an OR gate. This reduces the need to have separate peak and trough control paths, thus reducing the complexity of the FPGA design, the number of external components and the power consumption of the controller. The output of the OR gate triggers the first D-type flip flop on its negative falling edge, setting the output of the D-type flip flop high ($Start_{\text{dis}}$). This drives a pin on the FPGA connected to a resistor and capacitor in series. The time taken for the capacitor voltage to rise to the FPGA threshold level on port $Done_{\text{dis}}$ provides the timing for the on-state on the discharge pulse.

The $Done_{\text{dis}}$ port signal resets the discharge D-type flip flop, which sets the output to zero triggering the second D-type flip flop,. This generates the delay pulse to prevent shoot through of the switches. The falling edge of the delay signal D-type flip flop output triggers the pre-biasing D-type flip flop, generating the pre-bias switch pulse. On completion of a discharge, wait and pre-bias cycle, the enable signals are switched ready for the opposite peak detection. This status is held in another D-type flip flop and is used to set the multiplexors for gate signals so that the switches are closed in the correct order.

The FPGA used was Actel Igloo Nano AGLN250 mounted on the Igloo Nano Starter kit (Figure 3.24) [93]. The consumption of the controller including peak detection circuits was measured as 126 μW [85]. The core operation and timing generation used 13 μW and 4 μW respectively, whilst the gate drive and peak detection circuits used 13 μW and 96 μW. The design required 13 I/O pins and 28 of the FPGA's 6144 core tiles, hence an even smaller FPGA

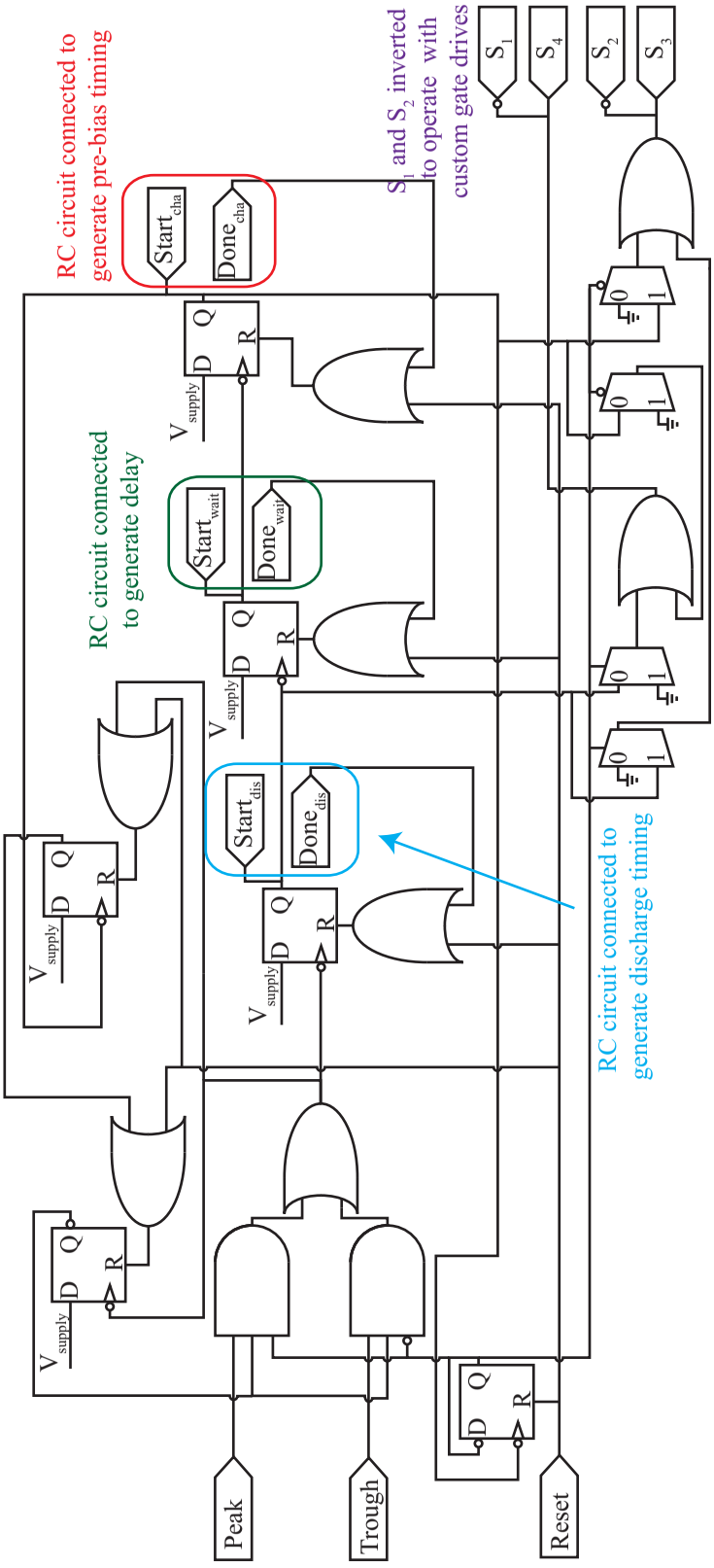


Figure 3.23: FPGA control design for implementing the SSPB technique [85].

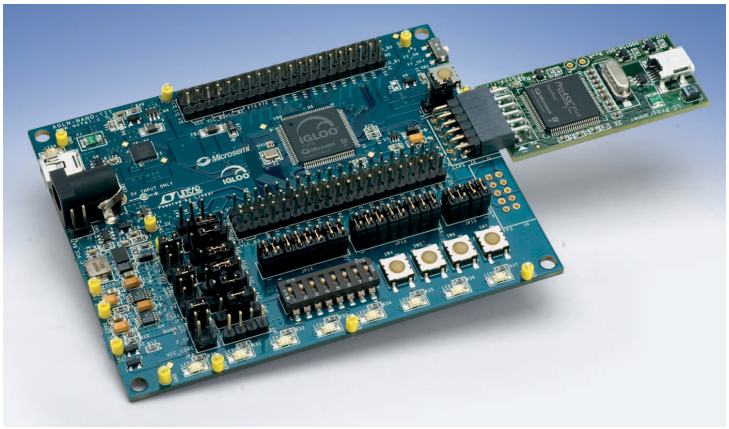


Figure 3.24: Igloo Nano Starter kit [93].

could be used [85].

The power consumption of the FPGA controller was measured as a 68.5 % reduction compared with using discrete logic gates. It is also much easier to adapt the controller to incorporate new features such as the forced return to zero mode which is discussed in detail in Chapter 4. It was therefore chosen as the basis for subsequent designs [87, 86, 94, 95, 96].

3.5 Inductor

The SSPB circuit uses an inductor across the centre of the H-bridge circuit to resonantly discharge and pre-bias the piezoelectric capacitance. The choice of inductor therefore determines the Q-factor of the resonant path, which affects the maximum power generation (see equation 2.36). The Q-factor of the resonance path can be calculated from the inductor's resistance R_{L} and inductance, L, as well as the piezoelectric capacitance, C_{p}, and total on-state switch resistance,R_{mos}.

$$Q = \frac{1}{R_{\mathrm{L}} + R_{\mathrm{mos}}} \sqrt{\frac{L}{C_{\mathrm{p}}}} \tag{3.8}$$

Physical limitations in inductor volume also limit the maximum achievable Q-factor as the volume available dictates the relationship between L and R_{L}. Inductance increases with the square of the number of turns, implying that an increase in inductance within a fixed volume

requires the wire to be made thinner and longer. Constraining the inductor to a fixed volume and adjusting the wire thickness accordingly, results in R_{L} also being proportional to the square of the number of turns. Consequently, for a fixed volume, L is proportional to R_{L}, and an optimal inductance to resistance ratio can be found by inserting (3.8) into the maximum power generation by SSPB equation (2.36) and differentiating with respect to L.

$$P_{\max} = {V_{\mathrm{po}}}^2 f_0 C_{\mathrm{p}} \left(\frac{8Q}{\pi} \right) \tag{3.9}$$

$$P_{\max} = {V_{\mathrm{po}}}^2 f_0 C_{\mathrm{p}} \left(\frac{8}{\pi(R_{\mathrm{L}} + R_{\mathrm{mos}})} \sqrt{\frac{L}{C_{\mathrm{p}}}} \right) \tag{3.10}$$

$$\frac{dP_{\max}}{dL} = {V_{\mathrm{po}}}^2 f_0 C_{\mathrm{p}} \left(\frac{4}{\pi(R_{\mathrm{L}} + R_{\mathrm{mos}}) \sqrt{\frac{L}{C_{\mathrm{p}}}}} \right) \tag{3.11}$$

The relationship between inductance and series resistance depends on many factors (e.g. core material, wire material, etc.). For commercial inductors this can be found empirically and the effect on power generation can be predicted using (3.11). For example, in [87], the relationship for a Coilcraft inductor was found to vary as $R_{\mathrm{L}} = 6117.9L$ [87].

Figure 3.25 shows the theoretical power generated when the inductance and inductor resistance are scaled using this relationship, given a 58.9 nF piezoelectric capacitance excited at 35 Hz, inducing $V_{\mathrm{po}} = 3\ V$ and a total switch resistance $R_{\mathrm{mos}} = 8.7\ \Omega$ [87]. Power generation increases as inductance decreases from 7 mH until such a point (1.4 mH) that the resonance path behaviour is dominated by the on-state resistance of the MOSFETs causing the Q-factor and power generation to fall.

The trend shown in Figure 3.25 was verified by selecting the LPS6225 series of inductors from Coilcraft [97], all with the same volume (86.4 mm^3), and analysing their performance with respect to Q-factor and power extraction in an SSPB circuit. The Q-factor was calculated by measuring the oscillatory damping of the piezoelectric-inductor voltage when a step excitation

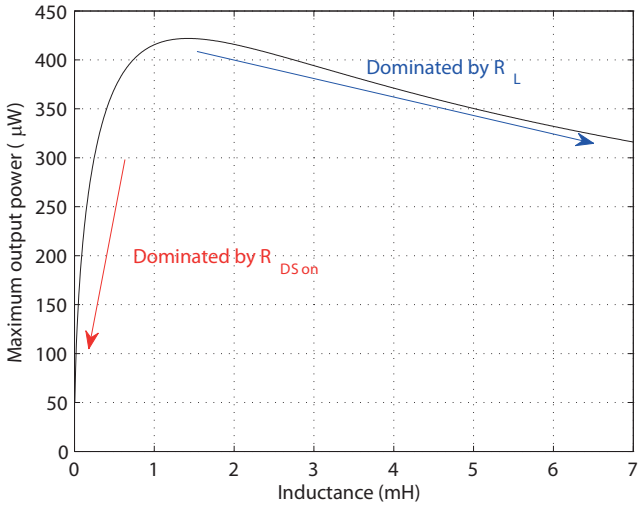


Figure 3.25: Inductance versus maximum output power for a 58.9 nF piezoelectric harvester excited at 35 Hz, inducing $V_{\text{po}} = 3\ V$. The MOSFET $R_{\text{DSon}} = 8.7\ \Omega$ with the inductor series resistance empirically found to vary as $R_{\text{L}} = 6117.9L$ [87].

was applied (Figure 3.26).

$$Q_{measured} = \frac{-\pi}{2 \ln \frac{V_2}{V_1}} \tag{3.12}$$

where V_1 and V_2 are the first peak and first trough voltages respectively.

The Q-factors were measured with a 58.9 nF Kingstate KPSG-100 piezo [98] and 8.6 Ω resistor in series to represent the on-state resistance of the switches (R_{mos}). Figure 3.27 compares the measured Q-factors with inductance and shows at low inductances, the R_{mos} causes the Q-factor to fall, however large inductances suffer from high effective series resistance (R_{L}) in the inductor causing the Q-factor to decrease.

Each inductor was inserted into a SSPB circuit with an FPGA controller (Section 3.4.3) using the peak detection circuit described in Section 3.2.3 [85]. Two Kingstate KPSG-100 piezoelectric loudspeakers [98] were mechanically connected together to form the sense and generation piezoelectric transducers with a measured capacitance of 58.9 nF and 46.6 nF respectively. A mass was added to lower the mechanical resonance frequency to 50 Hz and an excitation force capable of inducing 5.0 V open circuit voltage across the piezoelectric transducer was applied.

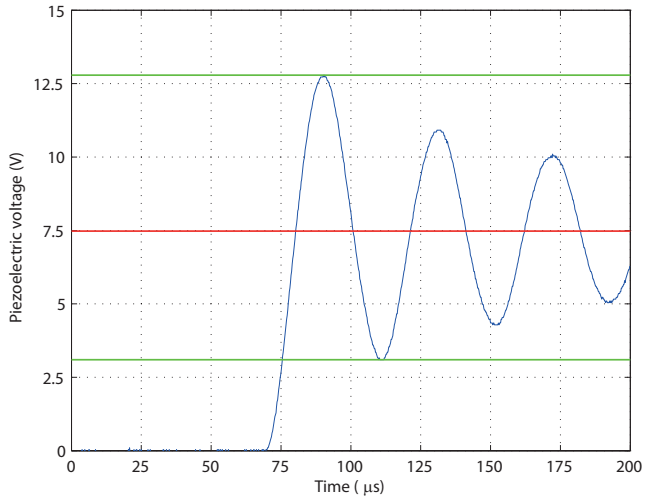


Figure 3.26: Piezoelectric-inductor voltage oscillatory damping when a step excitation is applied [87].

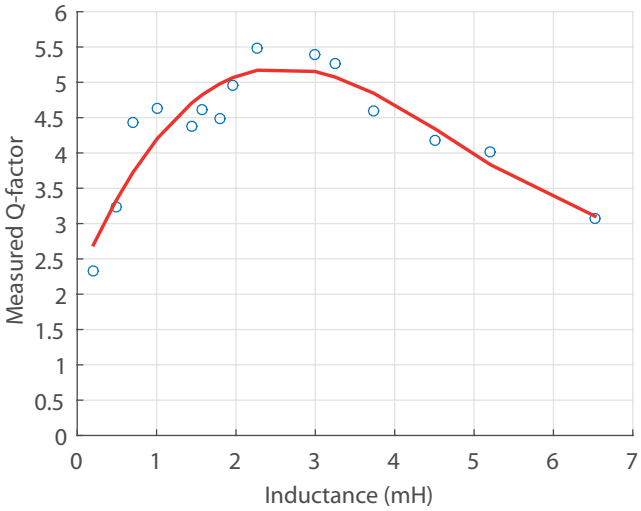


Figure 3.27: Measured Q-factor versus inductance for Coilcraft LPS6225 series inductors with a fixed 86.4 mm^3 volume, $C_{\mathrm{p}} = 58.9\ nF$ [87].

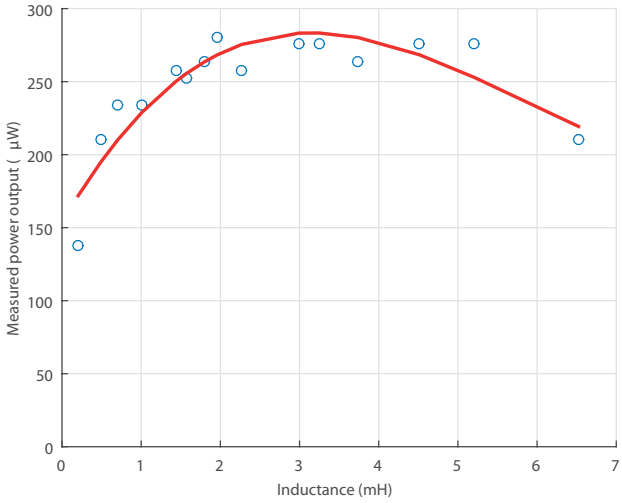


Figure 3.28: Measured power generation into the battery versus inductance for Coilcraft LPS6225 series inductors with a fixed 86.4 mm^3 volume, $C_\mathrm{p} = 58.9\ nF$ [87].

Figure 3.28 shows the power generation by each inductor measured using a Yokogawa WT210 power meter. It can be seen that the peak power occurs close to that predicted by the model in Figure 3.27 due to Q-factor being greatest at this point. The generated power is less than expected for a SSPB circuit (2.36) due to the peak detection firing early, resulting in a loss of power.

3.6 Implementation results

This chapter has described various techniques that can be used to implement the SSPB circuit. This section now compares the power output and control power consumption of the following configurations. Section 3.6.1 utilises a microcontroller, a zero cross detector and a TRIAC switched H-bridge [35]. Section 3.6.2 utilises discrete logic, low power peak detection circuit and a MOSFET switched H-bridge [84]. Section 3.6.3 utilises an FPGA, low power peak detection circuit and a MOSFET switched H-bridge [85]. The schematic and corresponding PCB layout for the best implementation in terms of controller % overhead are presented last.

3.6.1 Microcontroller with TRIAC switched H-bridge implementation

The pizeoelectric transducer was constructed from 0.9 nF piezolectric bimorph [99] with a small mass attached on the tip. The mechanical excitation was generated by an IMV PET-01-0A amplifier and shaker system [100] operated in closed loop mode. Figure 3.29 shows the configuration of the piezoelectric bimorph, the AD620 instrumentation amplifier [101] and LMV762 comparator [102] used to make the zero crossing point detector, an Arduino Mega 2560 [91] which adds a quarter of the mechanical excitation time period delay to the switching signals when a zero crossing point is detected, and the MOC3011 TRIACs [89] with 0.7 mH inductor used to implement the SSPB H-bridge.

The excitation was adjusted to induce an open circuit voltage 3.75 V across the piezoelectric transducer. Figure 3.30 shows the voltage waveform across the piezoelectric transducer demonstrating the successful implementation.

3.6.2 Discrete logic gates with MOSFET switched H-bridge implementation

In this configuration, two Kingstate KPSG-100 piezoelectric loudspeakers [98] were mechanically connected to form the sense and generation signals. They were attached to a fixed frame and the centre of the loudspeaker was mechanically actuated by a pc speaker who's frequency and

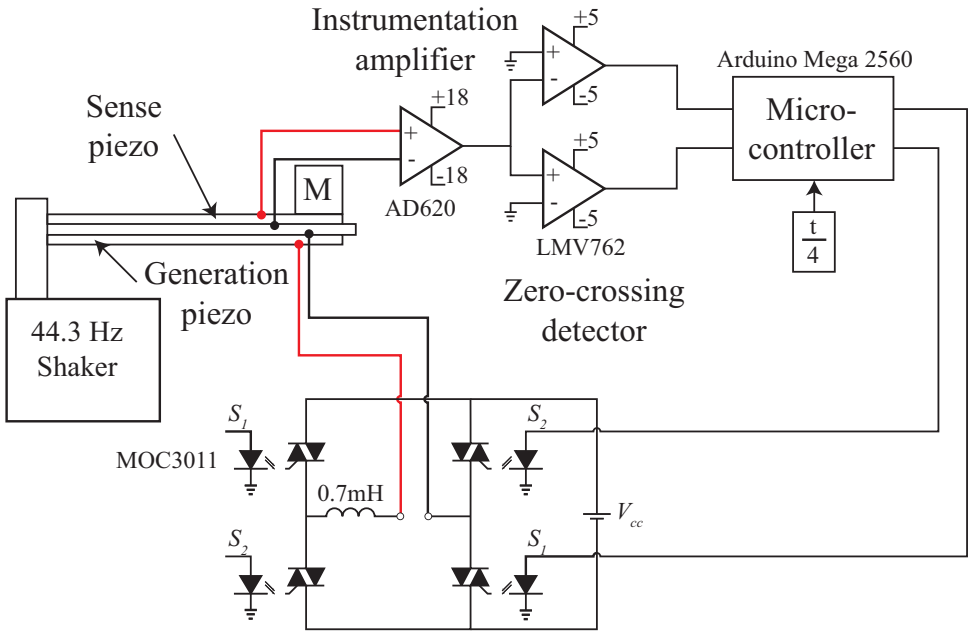


Figure 3.29: Circuit diagram of microcontroller with TRIAC switched H-bridge [35].

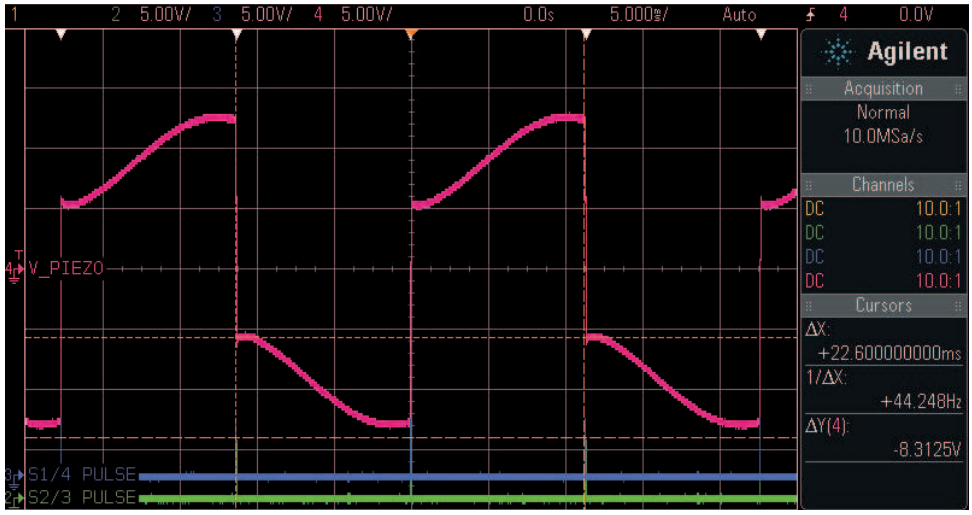


Figure 3.30: Piezoelectic voltage waveform across bimorph for SSPB circuit using a microcontroller and TRIAC switched. $C_{\mathrm{p}} = 0.9\ nF$, $L = 0.7\ mH$, $L_{\mathrm{R}} = 1.2\ \Omega$ and $V_{\mathrm{po}} = 3.75\ V$ [35].

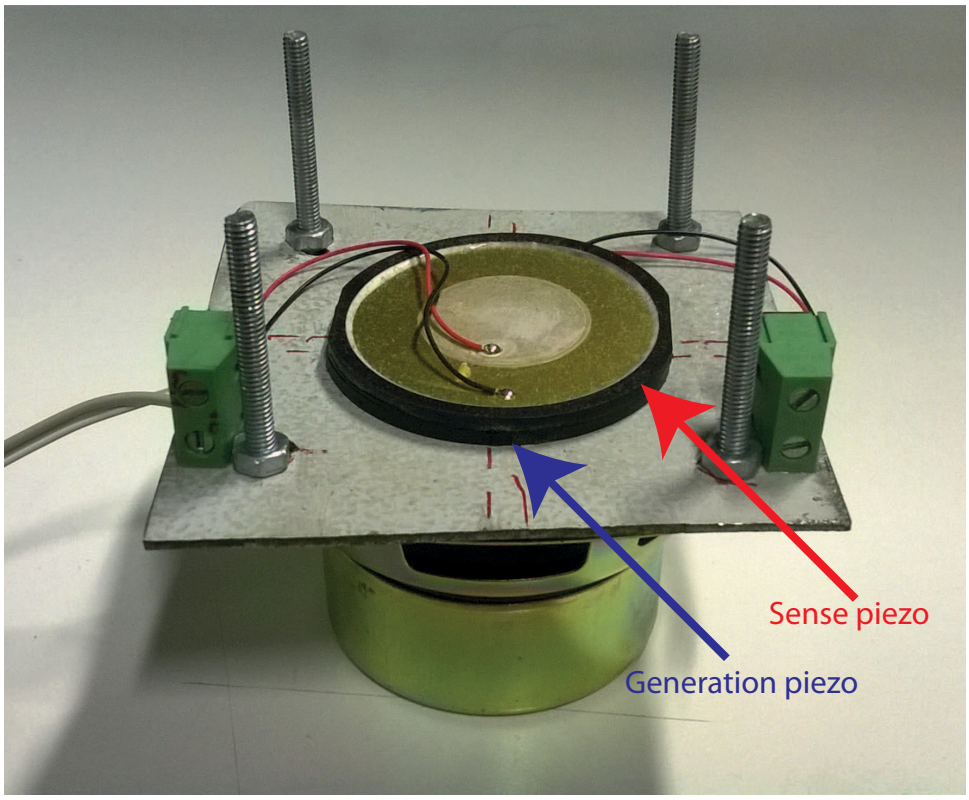


Figure 3.31: Sense and generation piezoelectric loud speakers driven by loudspeaker for test purposes.

amplitude was controlled by a signal generator (Figure 3.31). A mass was used to reduce the resonant frequency. Figure 3.32 shows the configuration using an AD8500 operational amplifier [82] and MCP6542 comparator [83] to form the peak detection circuit. The control logic is made from CD74HC221 monostables [92] and HEF4071B OR gates [103]. The SSPB H-bridge is made from BSH201 and BSS138, p-type and n-type MOSFETs [104, 105] respectively with a hand made 7.5 mH inductor.

The circuit was both simulated in OrCAD PSpice v16.3 (using a capacitor and sinusoidal current source to represent the piezoelectric harvester) and experimentally measured by applying a mechanical excitation at 212 Hz which induced an open circuit voltage of 6.3 V across the piezoelectric transducer. Figure 3.33 shows the close similarity between the theoretical and measured voltage across the piezoelectric transducer. The inductor current (Figure 3.34) is

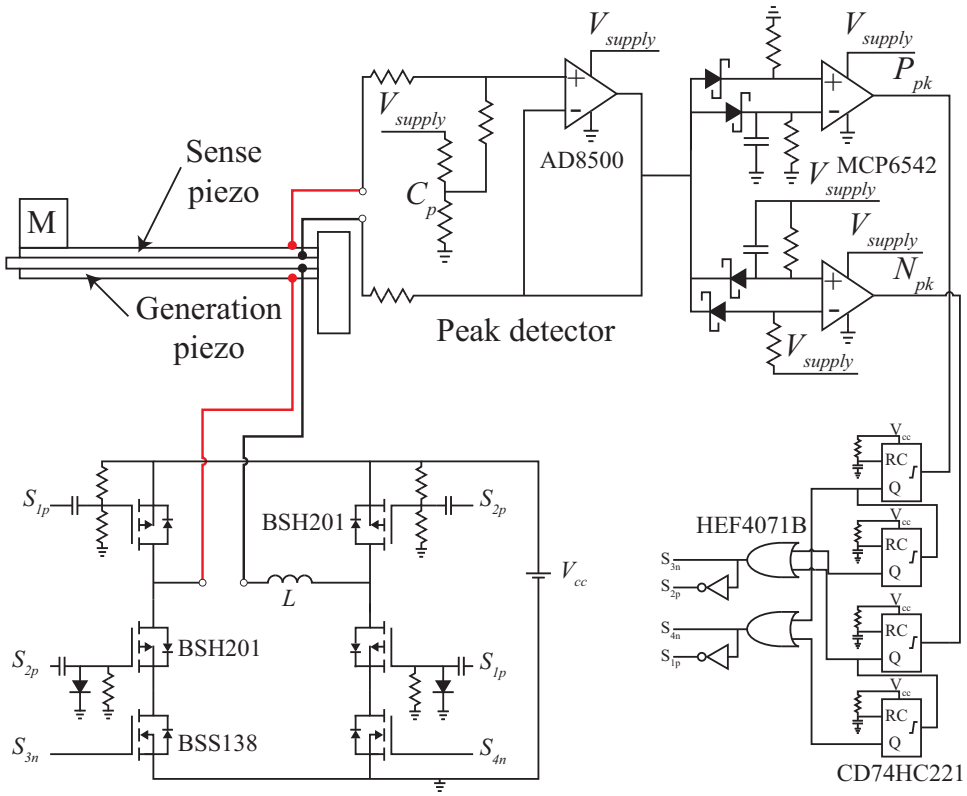


Figure 3.32: Circuit diagram of logic gates with MOSFET switched H-bridge [84].

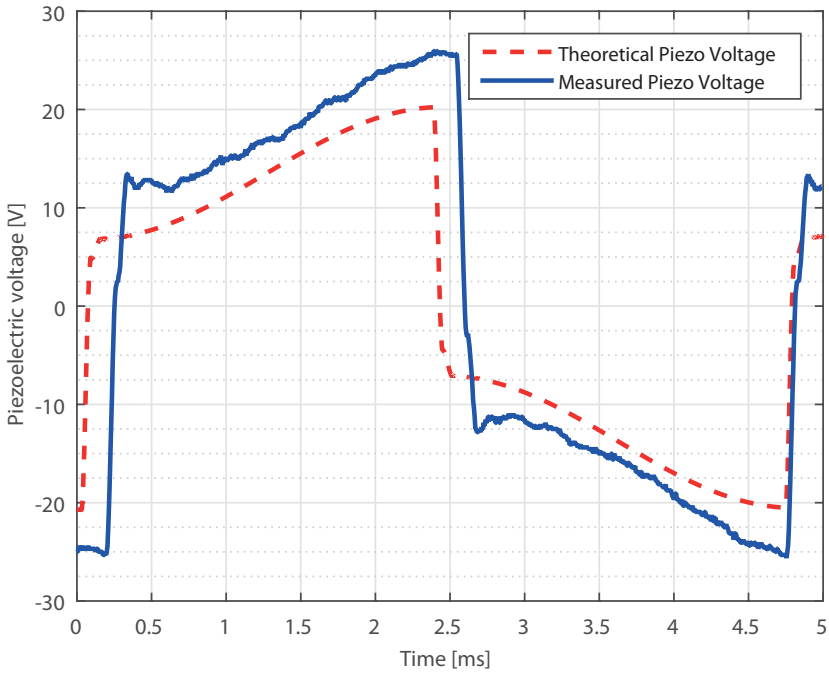


Figure 3.33: Measured and simulated voltage across the piezoelectric capacitance at 212 Hz [84].

shown with the same time scale. The first peak is the discharge current, which is significantly larger than the second peak corresponding to the pre-bias current, hence a net gain in energy is achieved.

A Yokogawa WT210 Digital Power Meter was used to measure the power generated by the harvester into the voltage supply, V_{cc}. At excitation of 200 Hz, 3 mW of power was generated. The control circuit, peak detection circuit and gate drives were measured to consume 400 μW of power during operation giving a useful power output of 2.6 mW [84].

The Q-factor of the circuit was measured by applying a step voltage and observing the ring-down envelope (3.12). The piezoelectric transducer was found to have a capacitance of 52.9 nF with a resonant circuit Q-factor of 5.8. The excitation force frequency of the experimental implementation was kept at 212 Hz whilst the input amplitude was varied to induce different open circuit voltages. The power extraction circuits under test were connected to an Agilent U8032A power supply and the voltage was adjusted to the optimal value for each induced open circuit

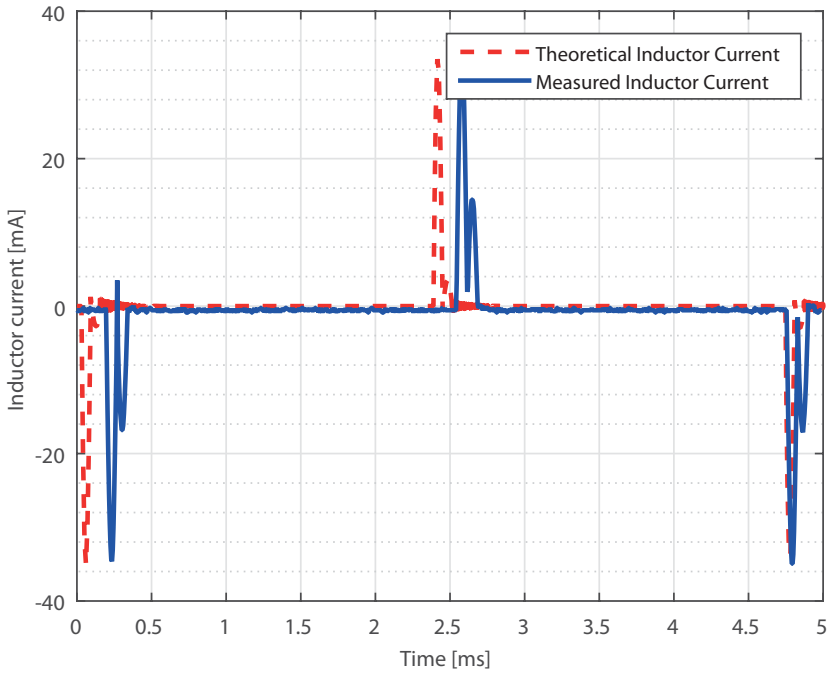


Figure 3.34: Measured and simulated inductor current at 212 Hz [84].

voltage. The power for the SSPB circuit and an optimally biased bridge rectifier was measured and plotted in Figure 3.35. The theoretical limits of a bridge rectifier, SSHI circuit, and SSPB circuit from (2.10), (2.16) and (2.36) respectively were also plotted for comparison. For the SSPB and bridge rectifier experimental results, the power overhead has not bee subtracted, however the SSPB implementation can be seen to be performing as well as the theoretical limit of the next best technique (SSHI).

3.6.3 FPGA with MOSFET switched H-bridge implementation

This configuration also has two Kingstate KPSG-100 piezoelectric loudspeakers [98] mechanically connected to form the sense and generation signals actuated by a pc speaker controlled by a signal generator. Figure 3.36 shows the implementation using an AD8500 operational amplifier [82] and MCP6542 comparator [83] to form the peak detection circuit and BSH201 and BSS138, p-type and n-type MOSFETs [104, 105] with 7.5 mH inductor. The controller used

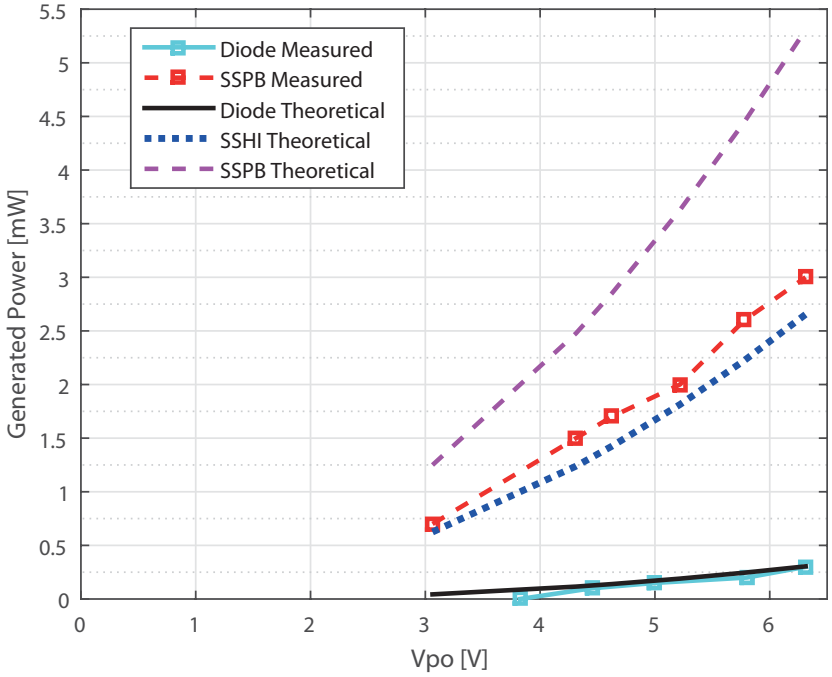


Figure 3.35: Power generation technique comparison without control overhead [84].

Igloo Nano Starter kit [93] with an AGLN250 FPGA.

The voltage across the piezoelectric transducer and the current through the inductor were compared with a simulation on OrCAD PSpice v16.3 (Figure 3.37).

Figure 3.38 is a comparison of the experimental implementation of using discrete logic (SSPB Discrete Measured) and FPGA controlled implementation (SSPB FPGA Measured) after their control overheads, 400 μW and 126 μW respectively, have been included. The circuit components were a piezoelectric loudspeaker of capacitance 52.9 nF with a Q-factor of 5.8 when in series with a 7.5 mH inductor. The power generation was measured when the excitation frequency was 212 Hz and the input amplitude was varied to induce different open circuit voltages. The theoretical power generation limits of the bridge rectifier (Diode Theoretical), the SSHI technique (SSHI Theoretical) and the SSPB technique (SSPB Theoretical), corresponding to (2.10), (2.16) and (2.36) respectively, have also been plotted for comparison. It can be seen that the experimentally measured results for the FPGA controlled implementation outperforms the

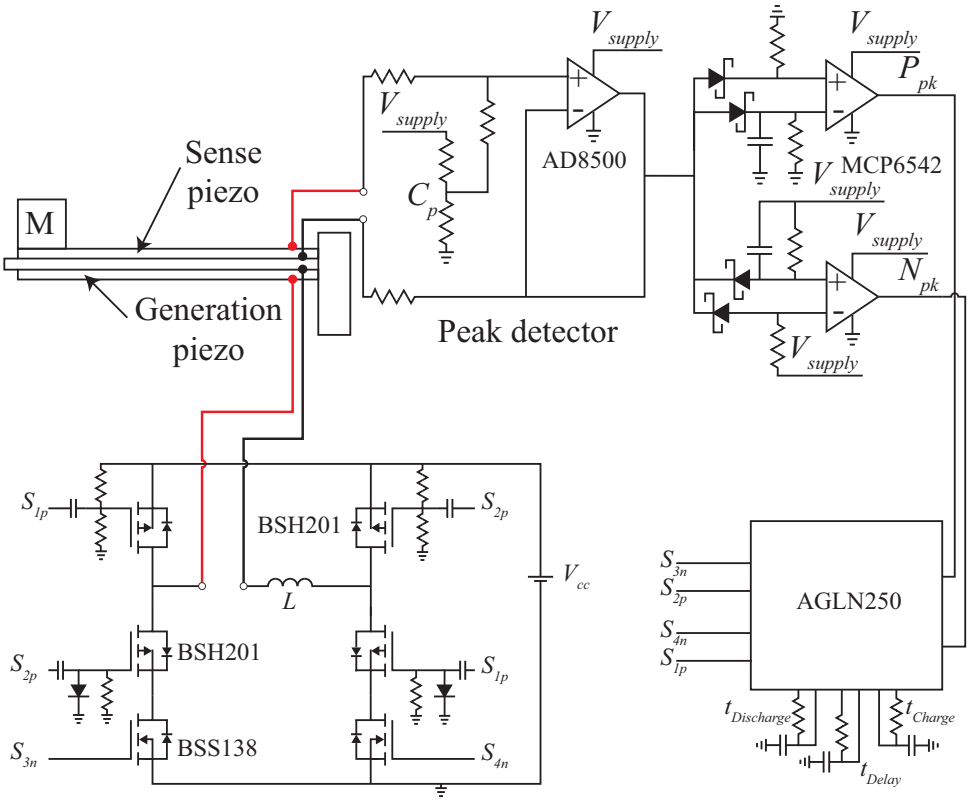


Figure 3.36: Circuit diagram of FPGA with MOSFET switched H-bridge [85].

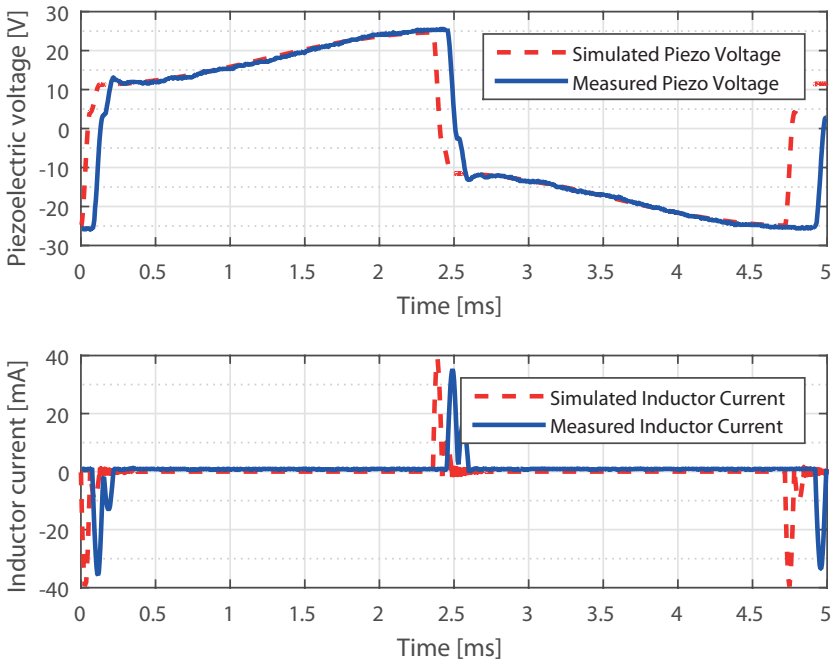


Figure 3.37: Measured and simulated voltage across the piezoelectric capacitance and inductor current at 212 Hz using FGPA controller [85].

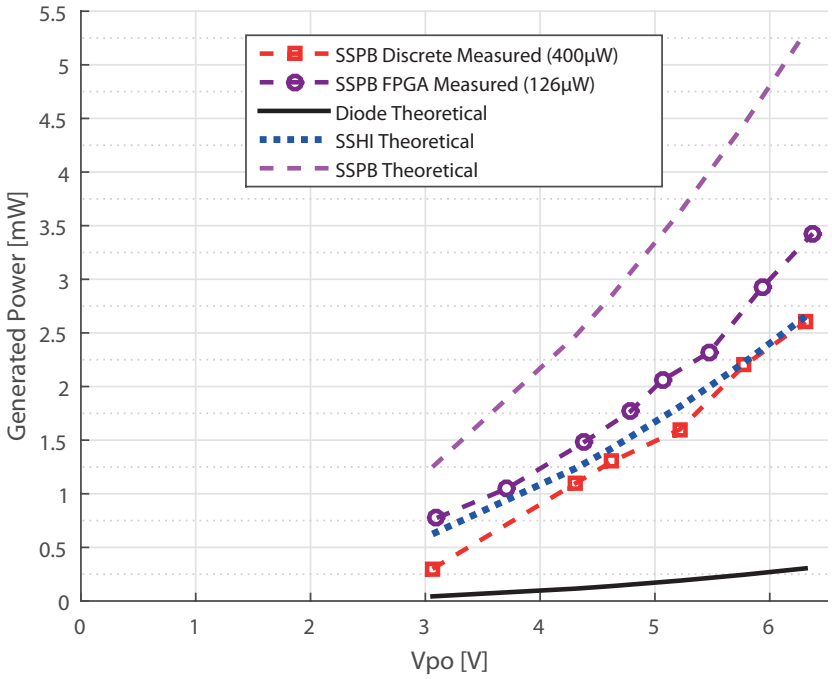


Figure 3.38: Power generation technique comparison with control overhead for experimental implementations [85].

theoretical limit of the SSHI technique by 14 % and generates 11.3 times as much power as the bridge rectifier.

3.6.4 Schematic and PCB layout for FPGA with MOSFET switched H-bridge implementation

It has been shown that the FPGA implementation has the best performance in terms of useful power output and requires minimal components to operate. A custom PCB was designed and fabricated with a smaller FPGA to demonstrate the feasibility of manufacturing the system to be a similar scale to the energy harvester. Figure 3.39 shows the populated devices and Appendix 8.1 is a copy of the schematic with component values and PCB layers.

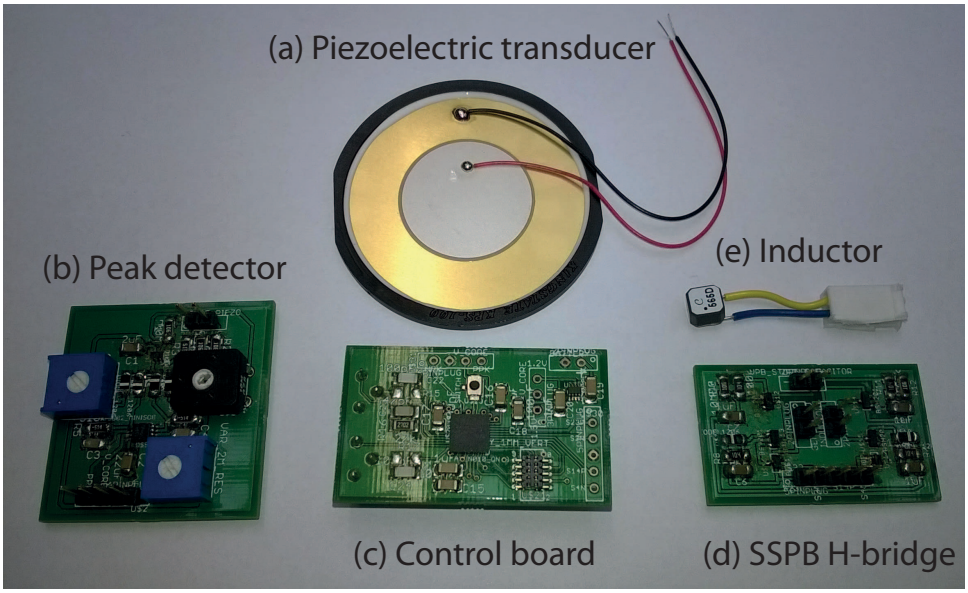


Figure 3.39: (a) Peak detection, (b) control board with SSPB.

3.7 Summary

In this chapter various design choices for the peak detector, control circuit and H-bridge switching circuit are presented. In each case power consumption was minimised in order to maximise the useful power output of the harvester. The best implementation using a low power peak detection circuit, FPGA controller and MOSFET switching circuit was able to generate 14 % more power than the theoretical limit of the next best known technique, SSHI. However it was noted during testing that the optimal pre-biasing voltage did not always result in the voltage across the piezoelectric transducer returning to zero after discharge. This was especially prevalent in harvesters which had been operating for a long period of time. In the next chapter a modification to the operation of the SSPB circuit is presented to improve the harvester's performance when the piezoelectric material has degraded.

4 Forced Return To Zero SSPB Circuit

In Chapter 2, a theoretical maximum power extraction limit (4.1) for the SSPB technique was presented [6]. However during experimental implementation of the SSPB circuit in Chapter 3, it was noted that the voltage across the piezoelectric transducer did not always return to zero after discharge. Subsequently it was shown in [38] that in some cases the optimal pre-bias voltage resulted in charge being left on the piezoelectric beam after the discharge phase. When the beam was subsequently pre-biased with the opposite polarity, the residual charge had to be overcome reducing the system efficiency. An improvement (termed Forced Return To Zero (FRTZ)) was implemented to mitigate this problem and is presented in this chapter.

4.1 SSPB limitation

The theoretical limit for power extraction by SSPB is given in (4.1) and derived in [6]. It assumes no power is required for the control circuit and that the optimal voltage occurs when all the energy on the piezoelectric beam is removed in the discharge phase, thus the voltage across the piezoelectric material prior to pre-biasing is equal to zero (Figure 4.1).

$$P_{\mathrm{SSPB}} = 8 f_0 C_{\mathrm{p}} {V_{\mathrm{po}}}^2 \frac{\gamma}{1-\gamma^2} \tag{4.1}$$

where f_0 is the excitation frequency, C_{p} is the piezoelectric capacitance, V_{po} is the induced open-circuit voltage across the piezo, and γ is the fractional capacitor voltage conserved by an RLC circuit with a quality factor Q after $\frac{1}{2}$ resonant cycle operation, $\gamma \approx \exp^{\frac{-\pi}{2Q}}$.

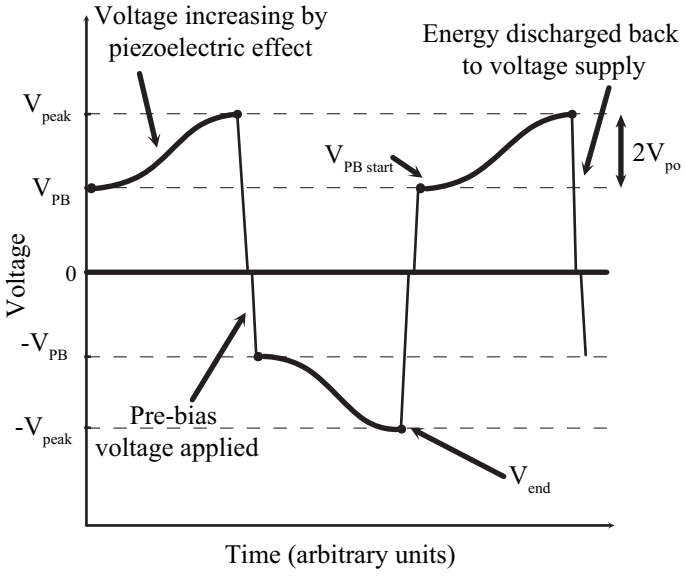


Figure 4.1: Original SSPB piezoelectric waveform assuming return to zero [35].

However it was shown by [38] that in some cases an increase in power output can be achieved if the constraint on the voltage returning to zero at the end of the cycle is relaxed. This is due to the inversion factor, γ, which is determined by the Q-factor of the LC resonant current path, being less than one. Thus not all of the energy is transferred to and from the piezoelectric capacitance during pre-biasing and discharging. As a consequence the circuit has to overcome the charge left on the beam, V_{rem}, by the discharging phase when pre-biasing, thus reducing the power extraction efficiency.

4.2 Forced Return To Zero SSPB Theory

The SSPB circuit was adapted to include a phase which removed the remaining charge on the beam before pre-biasing. In doing so, a small amount of harvested energy is wasted, however more energy would have to taken from the V_{cc} source (e.g. battery) to overcome this charge, hence a net energy saving is gained. The charge removal was achieved by placing a switch across the piezoelectric beam and closing it briefly after the discharge phase, shorting the two sides of the piezoelectric material together (Figure 4.2). Figure 4.3 shows the timing of the new switch

events.

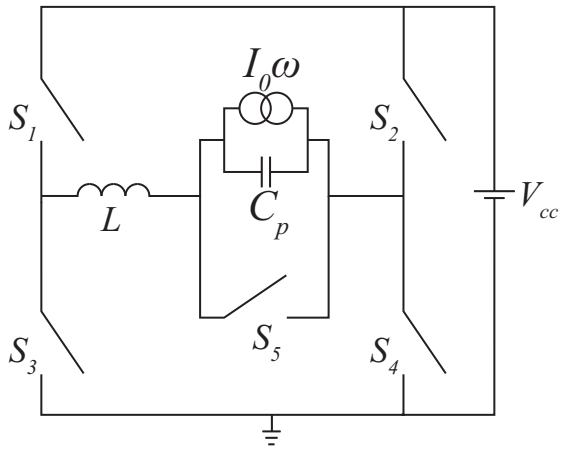


Figure 4.2: An adaptation of the SSPB circuit to include an extra switch across the piezoelectric beam to remove any remaining charge after the discharge phase.

Power generation using the FRTZ SSPB technique can be derived in the same way as the original SSPB circuit [35] by considering the extracted energy from the discharge phase versus the energy required to apply the optimal pre-bias voltage [94].

The voltage remaining, V_{rem}, after discharge is equal to:

$$V_{\text{rem}} = V_{\text{cc}} - (V_{\text{end}} - V_{\text{cc}})\,\gamma \tag{4.2}$$

where V_{cc} is the supply voltage, $V_{\text{end}} = 2V_{\text{po}} + V_{\text{PB}}$, V_{po} is the open circuit voltage across the piezoelectric beam, and V_{PB} is the applied pre-bias voltage given in (4.3).

$$V_{\text{PB}} = V_{\text{cc}}\,(1 + \gamma) \tag{4.3}$$

where γ is the fractional capacitor voltage conserved by an RLC circuit with a quality factor Q.

The energy required to pre-bias a piezoelectric beam of capacitance, C_{p}, is given in (4.4) as:

$$E_{\text{in}} = C_{\text{p}} V_{\text{PB}} V_{\text{cc}} \tag{4.4}$$

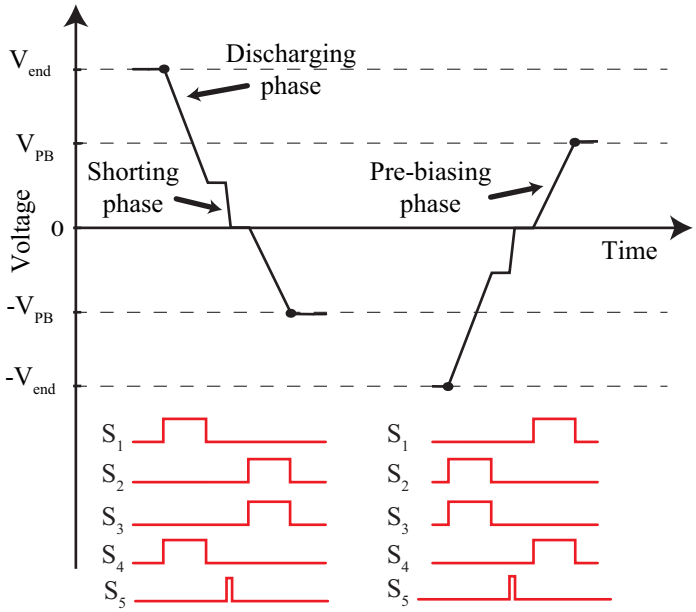


Figure 4.3: Piezoelectric voltage and timing waveforms for the FRTZ SSPB circuit using an extra shorting phase during the discharge and pre-bias phases.

whilst the energy extracted when discharging the beam is given in (4.5) as:

$$E_{\text{out}} = C_{\text{p}} \left(V_{\text{end}} - V_{\text{rem}} \right) V_{\text{cc}} \tag{4.5}$$

The change in energy is therefore given by subtracting (4.4) from (4.5):

$$\Delta E = E_{\text{out}} - E_{\text{in}} \tag{4.6}$$

$$\Delta E = C_{\text{p}} V_{\text{cc}} \left(V_{\text{end}} - V_{\text{rem}} - V_{\text{PB}} \right) \tag{4.7}$$

$$\Delta E = C_{\text{p}} V_{\text{cc}} \left(2V_{\text{po}} + V_{\text{PB}} - V_{\text{rem}} - V_{\text{PB}} \right) \tag{4.8}$$

$$\Delta E = C_{\text{p}} V_{\text{cc}} \left(2V_{\text{po}} - V_{\text{rem}} \right) \tag{4.9}$$

In order to find the voltage which maximises the change in energy with respect to the supply voltage, V_{cc}, the expressions for V_{rem} (4.2) needs to be inserted into (4.9).

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(2V_{\mathrm{po}} - V_{\mathrm{cc}} + \left(V_{\mathrm{end}} - V_{\mathrm{cc}}\right)\gamma\right) \tag{4.10}$$

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(2V_{\mathrm{po}} - V_{\mathrm{cc}} + \left(2V_{\mathrm{po}} + V_{\mathrm{PB}} - V_{\mathrm{cc}}\right)\gamma\right) \tag{4.11}$$

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(2V_{\mathrm{po}}\left(1+\gamma\right) - V_{\mathrm{cc}}\left(1+\gamma\right) + V_{\mathrm{PB}}\gamma\right) \tag{4.12}$$

In (4.3), V_{PB} was written in terms of V_{cc} and thus can be replaced in (4.12).

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(2V_{\mathrm{po}}\left(1+\gamma\right) - V_{\mathrm{cc}}\left(1+\gamma\right) + V_{\mathrm{cc}}\left(1+\gamma\right)\gamma\right) \tag{4.13}$$

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(1+\gamma\right)\left(2V_{\mathrm{po}} - V_{\mathrm{cc}} + V_{\mathrm{cc}}\gamma\right) \tag{4.14}$$

$$\Delta E = C_{\mathrm{p}} V_{\mathrm{cc}} \left(1+\gamma\right)\left(2V_{\mathrm{po}} - \left(1-\gamma\right)V_{\mathrm{cc}}\right) \tag{4.15}$$

This results in (4.15) which can be differentiated with respect to V_{cc} to find the optimal supply voltage.

$$\frac{\delta \Delta E}{\delta V_{\mathrm{cc}}} = \frac{\delta}{\delta V_{\mathrm{cc}}}\left(C_{\mathrm{p}}\left(1+\gamma\right)2V_{\mathrm{po}}V_{\mathrm{cc}} - C_{\mathrm{p}}\left(1+\gamma\right)\left(1-\gamma\right){V_{\mathrm{cc}}}^{2}\right) \tag{4.16}$$

$$\frac{\delta \Delta E}{\delta V_{\mathrm{cc}}} = C_{\mathrm{p}}\left(1+\gamma\right)2V_{\mathrm{po}} - C_{\mathrm{p}}\left(1+\gamma\right)\left(1-\gamma\right)2V_{\mathrm{cc}} \tag{4.17}$$

The result of setting $\frac{\delta \Delta E}{\delta V_{\mathrm{cc}}}$ equal to zero and re-arranging to make V_{cc} the subject gives the optimal V_{cc} voltage.

$$\frac{\delta \Delta E}{\delta V_{\mathrm{cc}}} = 0 \tag{4.18}$$

$$C_{\mathrm{p}} (1+\gamma) 2V_{\mathrm{po}} - C_{\mathrm{p}} (1+\gamma)(1-\gamma) 2V_{\mathrm{cc}} = 0 \tag{4.19}$$

$$C_{\mathrm{p}} (1+\gamma)(1-\gamma) 2V_{\mathrm{cc}} = C_{\mathrm{p}} (1+\gamma) 2V_{\mathrm{po}} \tag{4.20}$$

$$(1-\gamma) 2V_{\mathrm{cc}} = 2V_{\mathrm{po}} \tag{4.21}$$

$$V_{\mathrm{cc}} = \frac{2V_{\mathrm{po}}}{(1-\gamma) 2} \tag{4.22}$$

$$V_{\mathrm{cc}} = \frac{V_{\mathrm{po}}}{(1-\gamma)} \tag{4.23}$$

The result of (4.23) can then be inserted into the original change of energy equation given in (4.15).

$$\Delta E = C_{\mathrm{p}} \frac{V_{\mathrm{po}}}{(1-\gamma)} (1+\gamma) \left(2V_{\mathrm{po}} - (1-\gamma) \frac{V_{\mathrm{po}}}{(1-\gamma)} \right) \tag{4.24}$$

$$\Delta E = C_{\mathrm{p}} {V_{\mathrm{po}}}^2 \frac{(1+\gamma)}{(1-\gamma)} \tag{4.25}$$

The total power generated by FRTZ SSPB technique can then be found by multiplying (4.25) by twice the excitation frequency, f_0.

$$P_{\mathrm{SSPB_{FRTZ}}} = 2 f_0 C_{\mathrm{p}} {V_{\mathrm{po}}}^2 \frac{(1+\gamma)}{(1-\gamma)} \tag{4.26}$$

The fractional capacitor voltage, γ, when approximating close to 1 and taking a truncated series expansion, can be approximated by $1 - \frac{\pi}{2Q}$ [6]. Inserting this expression into (4.26) gives the power generated in terms of the circuit's Q-factor (4.30).

$$P_{\mathrm{SSPB_{FRTZ}}} = 2f_0 C_\mathrm{p} {V_\mathrm{po}}^2 \frac{\left(1+1-\frac{\pi}{2Q}\right)}{\left(1-1+\frac{\pi}{2Q}\right)} \tag{4.27}$$

$$P_{SSPB_{FRTZ}} = 2f_0 C_\mathrm{p} {V_\mathrm{po}}^2 \frac{\left(2-\frac{\pi}{2Q}\right)}{\left(\frac{\pi}{2Q}\right)} \tag{4.28}$$

$$P_{\mathrm{SSPB_{FRTZ}}} = 2f_0 C_\mathrm{p} V_\mathrm{po}^2 \frac{(4Q-\pi)}{\pi} \tag{4.29}$$

$$P_{\mathrm{SSPB_{FRTZ}}} = f_0 C_\mathrm{p} V_\mathrm{po}^2 \frac{82Q-2\pi}{\pi} \tag{4.30}$$

The original SSPB theoretical power generation limit (4.31) was derived in [6]. For high Q-factors ($\gamma \approx 1$), the (4.30) $\approx$ (4.31). However as Q-factor decreases, -4π in the original SSPB implementation has a greater effect than the -2π term in the FRTZ SSPB implementation.

$$P_{\mathrm{SSPB}} = f_0 C_\mathrm{p} {V_\mathrm{po}}^2 \frac{8Q-4\pi}{\pi} \tag{4.31}$$

Figure 4.4 shows a comparison between the power generated using the original SSPB circuit compared with the FRTZ case as γ varies from 1 (lossless system) to 0 (maximum loss). At very high γ the systems perform almost equally well because V_rem naturally tends to zero for the original SSPB mode, however as the loss tangent increases and γ tends to zero, the FRTZ SSPB circuit significantly outperforms the original circuit.

Performance at low inversion factors is of particular importance when considering the usable lifetime of piezoelectric material. It has been shown by [7] that cyclically applying a mechanical loading to piezoelectric material causes the material's loss tangent, $tan\ \delta$, to increase. In the report, several different piezoelectric materials were all investigated and displayed similar behaviour to Figure 4.5. However the actual physics which cause the piezoelectric material degradation are still not fully understood.

The increase in the loss tangent value as the number of mechanical cycles increases, causes the voltage inversion factor to decrease. Figure 4.6 compares the power generation against

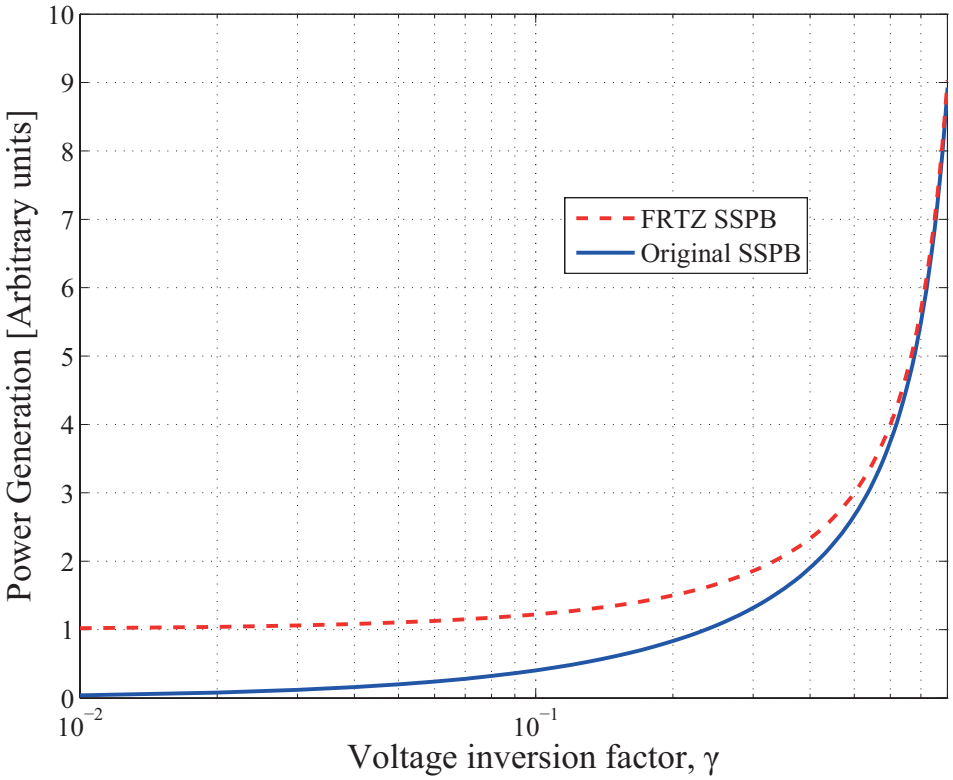
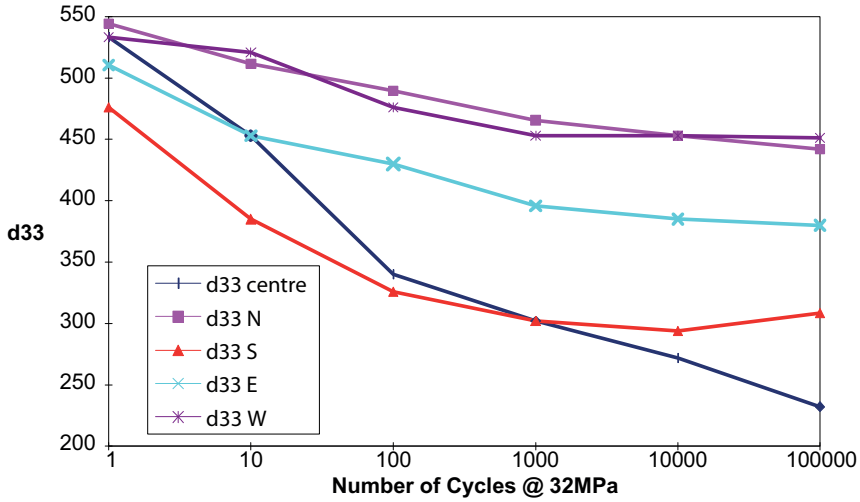
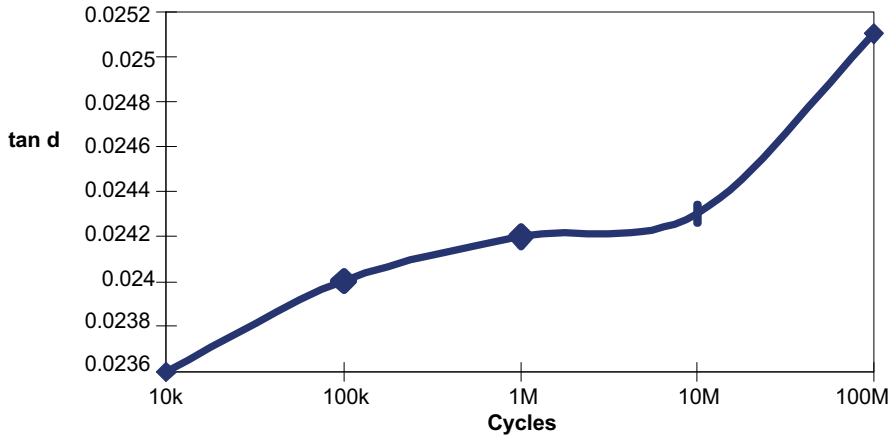


Figure 4.4: Comparison of power output under the original SSPB and the FRTZ SSPB techniques [94].

voltage inversion factor for the SSHI technique, original SSPB and FRTZ SSPB techniques using typical parameters of an energy harvester. The piezoelectric capacitance is 50 nF, the excitation frequency is 50 Hz, the induced peak current is 50 μA and γ is varied between 0 and 0.99.



(a) Berlincourt measurements of d33 at various points on a 10mm diameter PZT-5A disc sample after mechanical cycling at 32MPa



(b) Increase in loss tangent due to electrical cycling

Figure 4.5: Effect of mechanical cycling on piezoelectric materials properties [7].

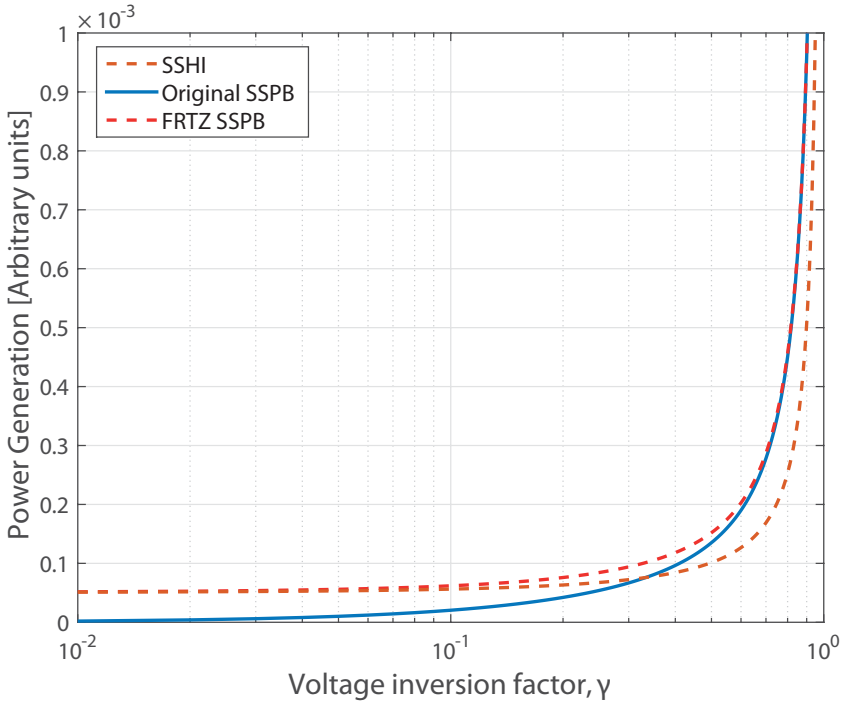


Figure 4.6: Comparison of power output versus voltage inversion factor for the SSHI, original SSPB, and FRTZ SSPB techniques using a 50 nF piezoelectric capacitance, 50 Hz excitation frequency, 50 μA peak induced current and 0 and 0.99 γ values [94].

4.3 FRTZ SSPB Circuit Theory Verification

The power generation improvement for the FRTZ SSPB circuit predicted in Figure 4.4 was verified both in OrCAD's PSpice v16.5 and experimentally.

4.3.1 PSpice Simulation

For the PSpice simulation, it was noted that moving the inductor from the centre of the H-bridge switching circuit to be in series with both high-side switches and V_{cc} (Figure 4.7) created the FRTZ circuit without the need for an extra switch [94]. The piezoelectric material could be short-circuited by closing either the high-side or low-side switches.

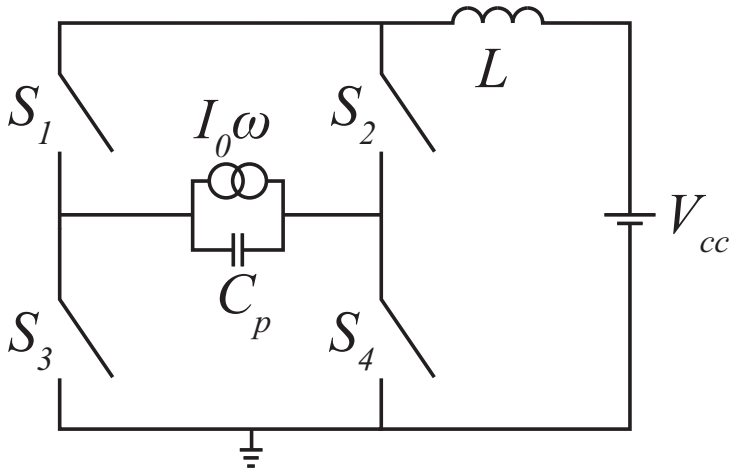


Figure 4.7: FRTZ SSPB circuit without an extra switch [94].

The values for simulation were picked based on circuit values measured in previous SSPB circuits [85, 86] and presented in [94]. The four H-bridge switches were modelled with an on-state resistance of 1 Ω and the piezoelectric harvester was modelled by a 500 μA at 80 Hz current source in parallel with a 65 nF capacitor. The inductor was 5 mH and a 98 Ω resistance was connected in series with the piezoelectric harvester representing a degradation in the piezoelectric material (effectively reducing the inversion factor). The voltage supply used to apply the pre-bias voltage was varied whilst the power generated was measured by integrating the power

over a single cycle and multiplying by the frequency.

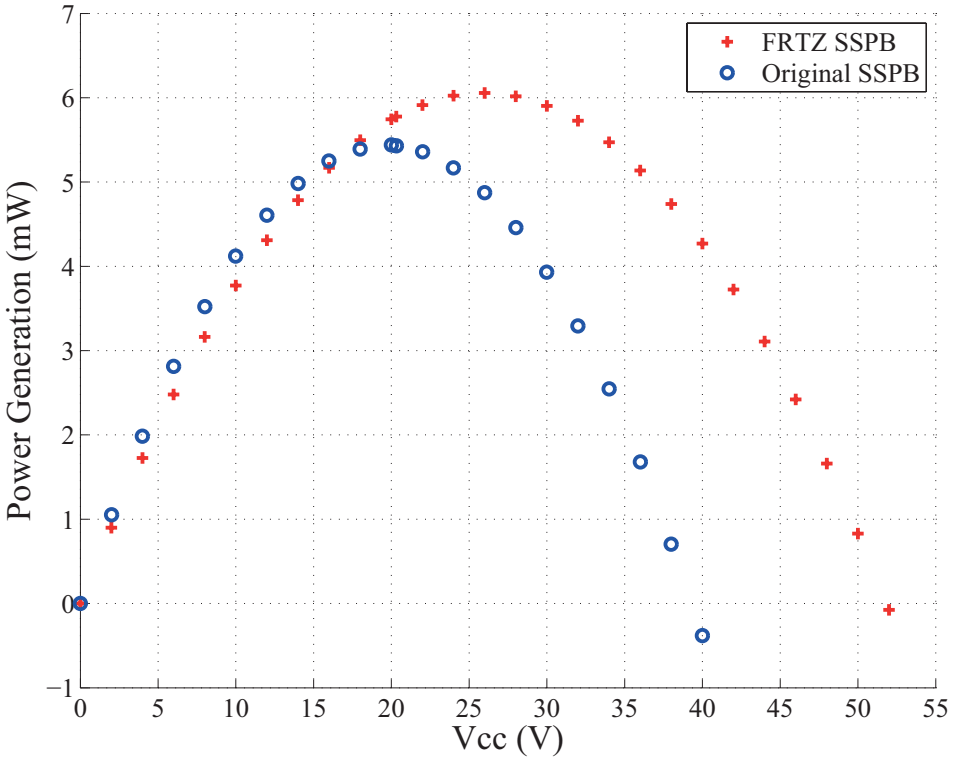


Figure 4.8: PSpice simulated power generation comparison between the original and FRTZ SSPB circuits when the supply voltage is varied [94]

A clear increase in peak power was measured using the FRTZ SSPB circuit (Figure 4.8) as energy used to apply the pre-bias voltage no longer needs to be wasted to over-come charge left on the piezoelectric capacitor between cycles. The FRTZ SSPB circuit is also shown to be less sensitive to supply voltage when required to achieve maximum power generation. This is very useful when considering that the source of mechanical vibrations may vary in amplitude and the system would need a maximum power point tracking circuit to follow the optimal supply voltage thus increasing the control circuit overhead.

4.3.2 Experimental Results

Practical implementation of the SSPB circuit has several challenges outlined in Chapter 3. These include design of bi-directional blocking and conducting switches, detecting when the beam has reached the maximum point of travel and generating the correct timing pulses whilst minimising the power consumption of the control circuit. The practical low power demonstration implemented in [85] was used as a basis for the FRTZ experimental results.

In the PSpice simulations, the inductor was moved from the centre of the H-bridge switching circuit to be in series with both high-side switches and the pre-bias voltage supply, V_{cc} as shown in Figure 4.7. However when implementing this modification to the SSPB circuit present in [85], the inductor causes the high-side gate drivers to no longer be referenced to a fixed voltage and thus no longer work. Similarly, placing the inductor in series with the low-side switches causes the same gate drive problem.

Instead, an inductor can be placed between each of the low-side switches and the centre of the H-bridge switching circuit (Figure 4.9). This arrangement enables the use of the low power gate drives designed in [85], however it comes at the cost of a more complex circuit requiring similar inductors. If the inductors' coil resistance and inductance are too dissimilar then the electrical resonance current path will have different Q-factors and thus require different on-times for the switches.

The inductors were thus selected to have the same inductance (5 mH) and series resistance, and hence the electrical resonant frequency through both sides of the H-bridge is the same. To minimise losses due to the extra charge clearing switch operation, the high side switches were operated instead of the low side switches, and were held on for 1 μs.

Two 48 nF Kingstate KPSG-100 piezoelectric loudspeakers mechanically coupled but electrically isolated were used to generate the sense voltage signal (required to detect when the piezoelectric speaker reached the extreme point of motion). The mechanical excitation force was at 170 Hz and induced an open-circuit peak voltage of 3.22 V across the piezoelectric device. The peak detector, H-bridge switching circuit and control circuit are described in Sections 3.2.3,

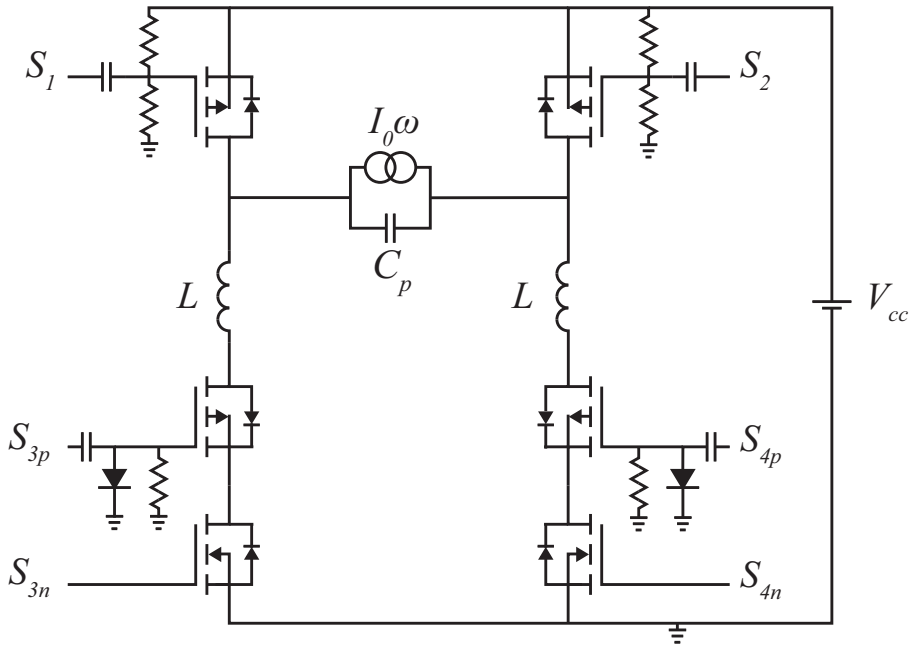


Figure 4.9: SSPB FRTZ H-bridge switching circuit practical implementation [85]

3.3.3 and 3.4.3 respectively. The components used for the n-type and p-type MOSFETs were Fairchild Semiconductor BSS138 and NXP BSH201. The differential amplifier was Analog Devices AD8500 and the FPGA was an Actel IGLOO Nano ALGN250.

Power generation by the original SSPB and FRTZ SSPB implementations was calculated by measuring the energy transferred to the power supply over one minute using the Yokogawa WT210 power meter. The applied supply voltage was swept to find the optimal voltage and any variation in the sensitivity to the supply voltage between the two methods.

As expected an initial sweep showed very little variation between the two methods as the piezoelectric transducer was new, thus the system had a high inversion factor and the voltage discharged to zero. A 100 Ω resistor was then added in series with the piezoelectric device to represent degradation of the piezoelectric transducer over time, thus reducing the inversion factor. The same voltage supply sweep and mechanical excitation was applied, however this time the FRTZ case outperformed the original and achieved a higher peak power generation as well as a decreased sensitivity to the voltage supply rail (Figure 4.10).

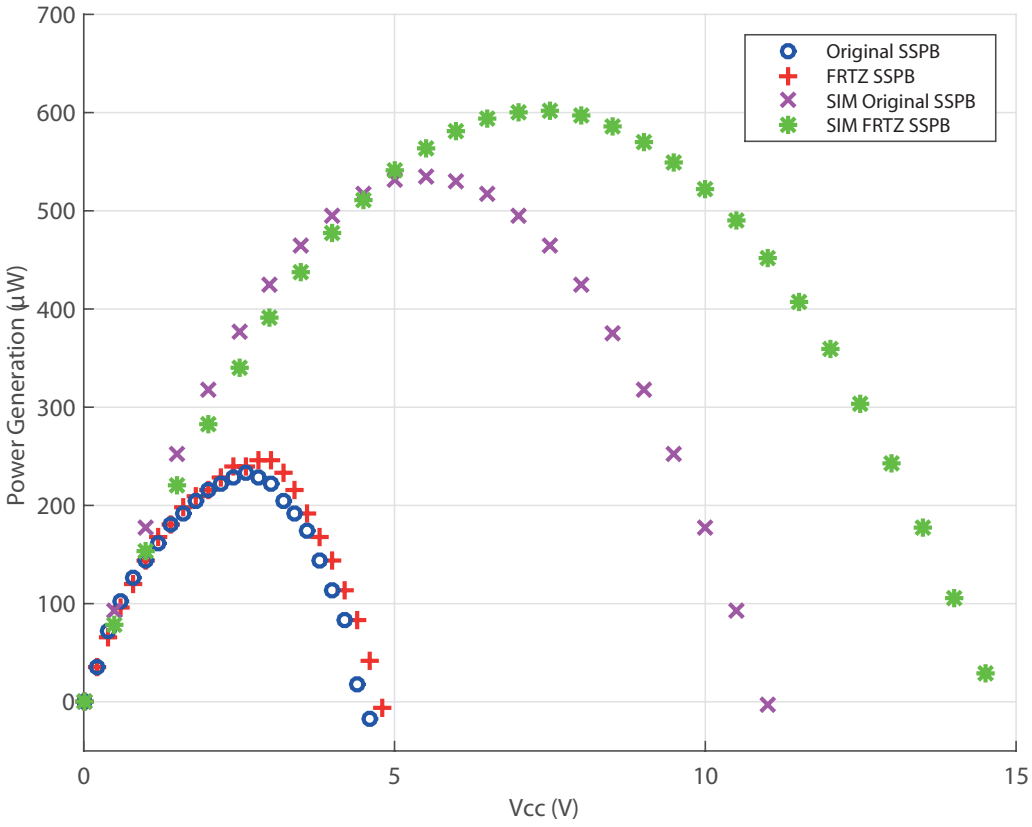


Figure 4.10: Comparison of the simulated and measured power generated by the FRTZ and the original SSPB implementations as the supply voltage applying the pre-bias voltage is swept [94].

The experimental results were also verified using PSpice in OrCAD's Capture. The degraded piezoelectric harvester was represented by a 100 Ω resistor. The results have been included in Figure 4.10. The difference in power is attributed to imperfect peak detection in the experimental set-up resulting in a halving of the expected power [84, 85].

4.4 Conclusion and Summary

A new mode of operation for single supply pre-biasing termed Forced Return To Zero (FRTZ) has been presented which is designed to improve power generation when the piezoelectric energy

harvester's inversion factor was low corresponding to degradation of the piezoelectric film due to wear-out over many cycles of use. The inversion factor of piezoelectric material was previously shown to deteriorate when repeatedly mechanically stressed, although the reason for this is not fully understood. However by improving the power generation capability at low inversion factors, the usable lifetime of the energy harvester can be extended.

Using the new FRTZ SSPB circuit mode operation and requirements for the SSPB circuit described in Chapter 3, a complete piezoelectric energy harvesting system parametrisation and optimisation can be performed. The methodology and results of this are presented in the next chapter.

5 Analytical Optimisation of Piezoelectric Harvesting Systems

The previous chapters have identified the requirements of the SSPB circuit and a new mode of operation, FRTZ, which improves power generation performance when residual charge is left on the piezoelectric transducer after the SSPB discharge phase. In this chapter, a coupled electromechanical model of a full piezoelectric vibration energy harvesting system is presented. The chapter is based on work for a journal paper written in conjunction with the University of California, Berkeley, Buskerud and Vestfold University College, Norway, and University of Illinois, Chicago [106].

The model implements a complete optimisation including the piezoelectric transducer, a power conditioning circuit, and a battery for the first time. A SSPB circuit was used for optimal electrical damping of the piezoelectric transducer. The model was implemented in MATLAB and verified with time domain simulations in SPICE. The mechanical and electrical system parameters required to maximise the power output under a given set of operating conditions are reported.

The system was constrained in terms of volume, acceleration, frequency and material properties. For each combination of volume and acceleration, the optimisation was solved numerically using ideal equations to provide a starting point then adding losses and iterating until steady state conditions were found. The viable parameter solution with highest power generation was then selected as the solution for that combination of volume and acceleration. Material

properties for both MEMS scale and MESO scale devices were investigated.

From the MEMS scale results, a conference paper written in conjunction with University of California, Berkeley, and Buskerud and Vestfold University College, Norway [107], was written comparing complete electrostatic [23] and piezoelectric [106] energy harvesting systems. The results enable an engineer to choose an optimal transduction method as a function of harvesting operating frequency, acceleration and device size.

This chapter is organised as follows. Section 5.1 presents theory behind the model including the scope of the analysis and material limitations, the mechanical structure of the harvester, the power conditioning circuit, the energy storage circuit, and the system effectiveness. Section 5.2 details the algorithm used by the model. Sections 5.3 to 5.6 derive the equations used for the algorithm and Section 5.7 presents the simulation results followed by the chapter's conclusions.

5.1 Theory

5.1.1 Scope of Analysis

The aim of the model was to determine the energy harvesting systems maximum power output and required system parameters as a function of input acceleration, frequency and system volume. The applied mechanical acceleration was varied between 0.01 ms^{-2} and 100 ms^{-2} at 1 Hz, 10 Hz, 100 Hz and 1 kHz. The volume was constrained to a cube of side length S varying from 1 mm to 15 mm. For each acceleration and volume combination at a given frequency, an optimal combination of mechanical dimensions (beam thickness and length, and mass thickness and length) and electrical components (circuit topology, semiconductor device area and inductor size) was found. The target battery voltage was 1.5 V.

5.1.2 Mechanical Structure of the Harvester

The mechanical structure of the energy harvester was a simple cantilever formed of a substrate with one layer of piezoelectric material and second layer oxide fixed to it. A proof mass made of

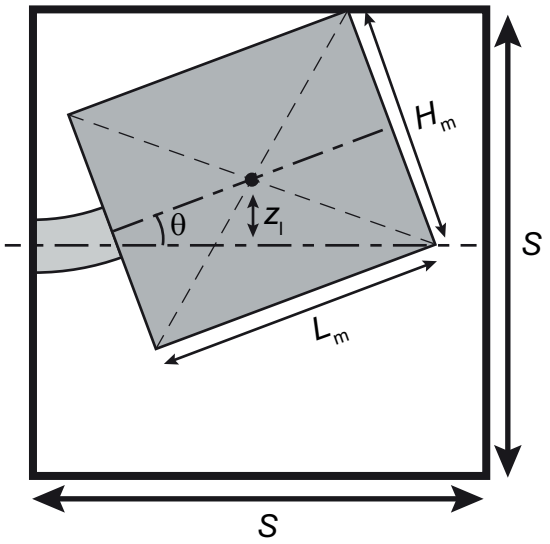


Figure 5.1: Geometry of piezoelectic energy harvesters, where S is the length of the volume, L_{m} is the mass length, H_{m} is the mass height, Z_{l} is the vertical displacement, and θ is the angular displacement [106].

gold was attached at the tip of the cantilever. The mass and beam's widths are assumed equal to the width of the available side length, S. The proof mass thickness, H_{m}, is set at $S/2$ such that the proof mass occupies close to half of the volume available, which is the optimal fraction for resonant operation in the displacement constrained case [36]. The harvester's geometry is shown in Fig. 5.1 [106]. The magnitude of the ideal mass deflection is found by numerically solving for each for each combination of volume and acceleration:

$$\frac{S}{2} = Z_{\mathrm{l}} + \sqrt{\frac{{L_{\mathrm{m}}}^2}{4} + \frac{{H_{\mathrm{m}}}^2}{4}} \sin\left(\theta_{c1} Z_{\mathrm{l}} + \tan^{-1}\left(\frac{H_{\mathrm{m}}}{L_{\mathrm{m}}}\right)\right) \tag{5.1}$$

where Z_{l} is the vertical displacement of the mass, L_{m} is the mass length, H_{m} is the mass thickness, and θ_{c1} is the rotation per angle per unit vertical displacement from the neutral position.

The materials the mechanical structure can be made out of vary with the size of device. In this study, both MEMS scale and MESO-scale devices were considered (Table 5.1). The length of the cantilever was varied between 1 % and 70 % of S while L_{m} was set to the remaining

portion. The thickness of the substrate was also varied between 1 μm and 200 μm. These parameters were used to find cantilever lengths and thicknesses that had a resonant frequency within 1% of the target mechanical frequency. For beam length-thickness combinations which achieved this, the mass, m, the beam's spring constant, k, the piezoelectric capacitance of the beam, C_{p}, and the transduction factor, Γ, were then calculated.

Table 5.1 lists the parameters used in the study. The thickness of the piezoelectric material and oxide were chosen based on what current technology a fabrication lab could achieve. The piezoelectric material chosen was Lead Zirconate Titanate (PZT) as it was MEMS process compatible and has been used previously to make piezoelectric energy harvesters Table 2.3. For the proof mass, gold was used due to its high density and MEMS process compatibility.

Table 5.1: Mechanical parameters

Parameter	Variable	MEMS Value	MESO Value	Units
Thickness of piezoelectric	t_{p}	1.5	380	μm
Thickness of oxide	t_{o}	1.0	0.1	μm
Thickness of mass	H_{m}	$S/2$	$S/2$	mm
Width of beam	W_{b}	S	S	mm
Width of mass	W_{m}	S	S	mm
Elastic modulus, piezoelectric	E_{p}	300	62	GPa
Elastic modulus, oxide	E_{o}	60	60	GPa
Elastic modulus, substrate	E_{s}	170 (Silicon)	100 (Brass)	GPa
Density of mass material (Au)	ρ_{mass}	19320	19320	kg m^{-3}
Piezoelectric coefficient	d_{31}	2	190	pm V^{-1}
Dielectric constant, piezoelectric	ϵ_{p}	92	1593	pF m^{-1}

The resonant frequencies achievable using MEMS and MESO scale material properties as a function of S with a gold proof mass is shown in Figures 5.2 and 5.3 respectively. It is shown that the transducers made from the MESO material have much higher resonant frequencies for a given volume than the MEMS scale material. This is due to the piezoelectric layer being much thicker as the piezoelectric material is a ceramic, which is very brittle and likely to break below this level using current manufacturing processes. The MEMS piezoelectric thickness is based on the upper limit for both sol-gel deposition and sputtering [106]. A consequence of this is

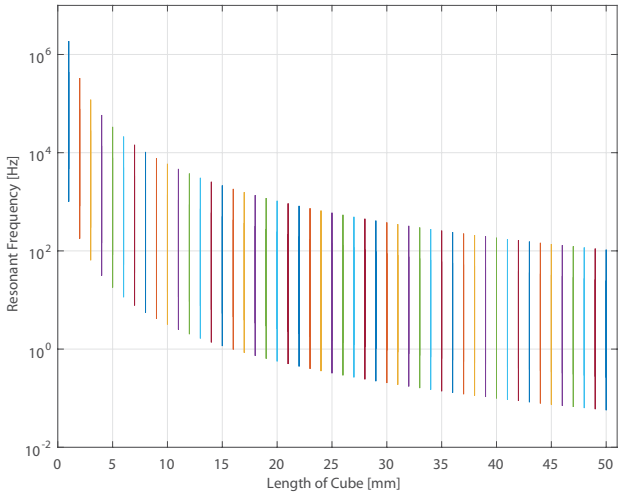


Figure 5.2: Resonant frequencies achievable for a given side length using MEMS material properties .

a trade-off currently exists between small MEMS-scale devices with poor electrical properties, compared with large MESO-scale devices with good electrical properties [108].

5.1.3 Power Conditioning Circuit

Figure 5.4 shows the SSPB circuit used to extract energy from the harvester to the battery. The SSPB circuit [35] was used as the power electronic interface since it uses the fewest number of components and is capable of performing the necessary operations to achieve controlled optimal Coulomb damping [6]. A bridge rectifier circuit was also considered but either the damping force generated on the mass was too small to ensure the mass stayed within the given volume or the power generated was significantly less than the SSPB circuit. The models used to calculate the performance and parameters for the SSPB circuit and bridge rectifier circuit were based on [35], [85], [6] and [38], and D'Hulst's thesis in 2012 [109] respectively. The FRTZ (see Chapter 4) circuit was implemented when the charge left on the piezoelectric capacitor after discharge opposed the polarity bias required for the pre-bias voltage, V_{PB}.

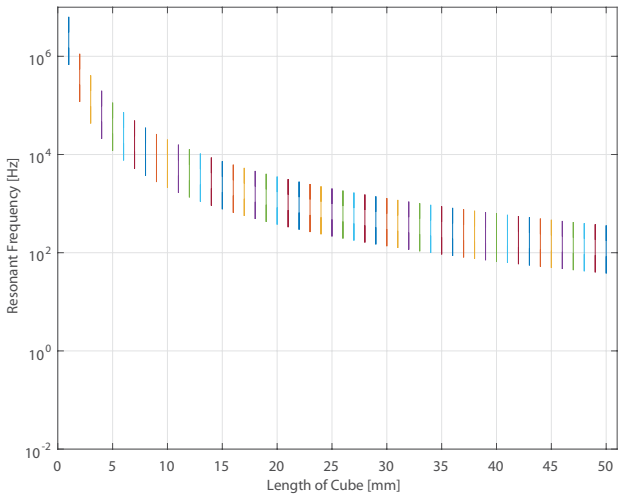


Figure 5.3: Resonant frequencies achievable for a given side length using MESO material properties .

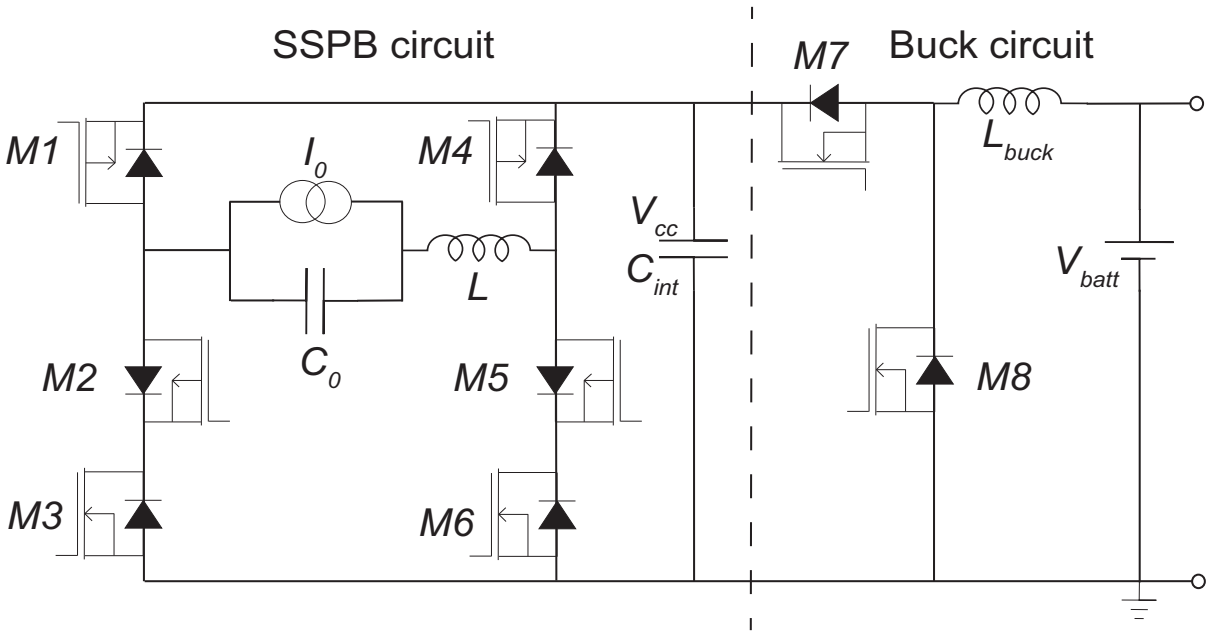


Figure 5.4: Equivalent circuit of the piezoelectric energy harvester (current source and capacitor) connected to SSPB power conditioning circuit [6].

5.1.3.1 Optimal pre-bias voltage

To ensure the mass displacement (5.1) is constrained in a CDRG harvester operating at resonance, an optimal Coulomb damping force of

$$F_{\mathrm{opt_{CZ}}} = \frac{\pi}{4} m \omega_{\mathrm{input}}^2 Y_0 = \frac{\pi}{4} m A_{\mathrm{input}} \tag{5.2}$$

is required, where m is mass, ω_{input} is input frequency, Y_0 is input vibration amplitude, and A_{input} is input acceleration [38]. If the cantilever is assumed to be at its maximum positive point of displacement, the optimal force, $F_{\mathrm{opt_{CZ}}}$, must be equal to the product of -1 times the Coulomb damping component of the force on the cantilever given in (2.4) as the Coulomb damping opposes the motion of the cantilever[38].

$$\frac{\Gamma}{C_0} q = -F_{\mathrm{opt_{CZ}}} \tag{5.3}$$

$$\frac{\Gamma}{C_0} q = -\frac{\pi}{4} m A_{\mathrm{input}} \tag{5.4}$$

Thus rearranging to make the charge, q, the subject gives the relation,

$$q = -\frac{\pi}{4} m A_{\mathrm{input}} \frac{C_0}{\Gamma} \tag{5.5}$$

which can be used with (2.4) to find the pre-bias voltage, V_{PB}, needed to obtain this damping force:

$$V_{\mathrm{PB}} = \left(\frac{\pi}{4} m A_{\mathrm{input}} - \frac{\Gamma^2 Z_{\mathrm{l}}}{C_{\mathrm{p}}} \right) \frac{1}{\Gamma} \tag{5.6}$$

where Γ is the transduction factor [38]. This expression allows the optimal damping to be set based on the harvester's design.

The voltage on the intermediate capacitor, V_{cc}, sets the applied pre-bias voltage. To determine the required V_{cc}, it is necessary to look at the voltage in two phases of the circuit operation: first, from V_{end} to V_{rem}, and then from V_{rem} to V_{pb}. Equations for these two phases are found

by considering a simple circuit with the V_{cc} as a battery, an open switch, and inductor, and a capacitor initially with either V_{end} or $-V_{rem}$ on it. When the switch is closed, a resonant path from the capacitor to the battery via the inductor and switch is formed. Note when calculating V_{cc}, the polarity of V_{pb} must be taken into account since it may be negative for small accelerations. V_{cc} cannot however be negative, as this would require V_{pb} to be less than $-|\Gamma|Z_l/C_p$ which would result in a forced oscillator.

5.1.3.2 Positive pre-bias voltage

Figure 5.5 shows the positive pre-bias case, assuming V_{rem} is significant. In this case, the resonant discharge path causes the capacitor voltage, V_{end}, to decrease by the voltage difference across the capacitor, $V_{cc} - V_{end}$, multiplied by $1 + \gamma$, where γ is the fractional capacitor voltage conserved by an RLC circuit with a quality factor Q. Note in a circuit with an infinite Q-factor, γ will tend to 1.

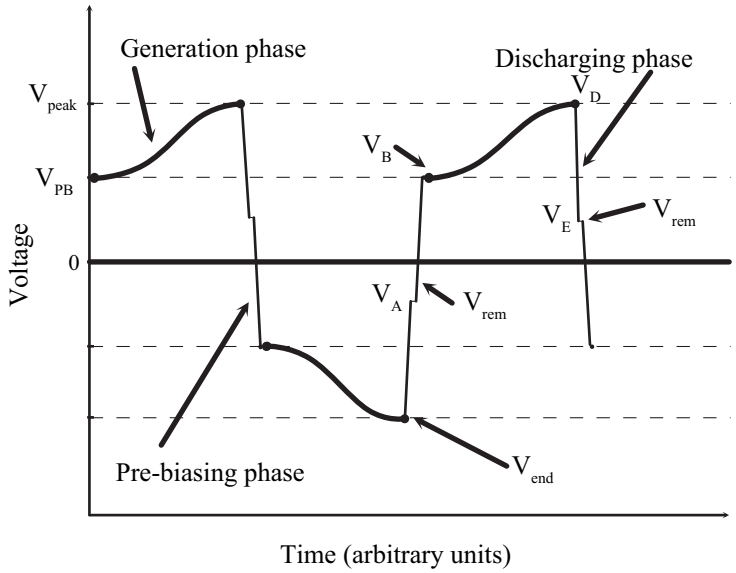


Figure 5.5: Piezoelectric voltage waveform for positive pre-bias case assuming V_{rem} is significant.

The equation for the circuit operation from V_{end} to V_{rem} is therefore:

$$V_{\text{rem}} = -V_{\text{end}}\gamma + V_{\text{cc}}(1+\gamma) \tag{5.7}$$

For the second part of the circuit operation from $-V_{\text{rem}}$ to V_{PB}, the equation takes the form

$$V_{\text{pb}} = V_{\text{rem}}\gamma + (V_{\text{cc}})(1+\gamma). \tag{5.8}$$

Substituting (5.7) into the second expression and simplifying gives

$$V_{\text{pb}} = (-V_{\text{end}}\gamma + V_{\text{cc}}(1+\gamma))\gamma + V_{\text{cc}}(1+\gamma). \tag{5.9}$$

Substituting V_{end} with $V_{\text{pb}}+2V_{\text{po}}$ and rearranging, gives the V_{cc} required for the positive pre-bias case:

$$V_{\text{pb}} = (-(V_{\text{pb}} + 2V_{\text{po}})\gamma + V_{\text{cc}}(1+\gamma))\gamma + V_{\text{cc}}(1+\gamma) \tag{5.10}$$

$$V_{\text{pb}} = V_{\text{cc}}\gamma^2 - V_{\text{pb}}\gamma^2 - 2V_{\text{po}}\gamma^2 + 2V_{\text{cc}}\gamma + V_{\text{cc}} \tag{5.11}$$

$$V_{\text{cc}} = \frac{\gamma^2 2V_{\text{po}} + V_{\text{pb}}(\gamma^2+1)}{(1+\gamma)^2} \tag{5.12}$$

5.1.3.3 Negative pre-bias voltage

Figure 5.6 shows the voltage waveform for the negative pre-bias case which occurs at low accelerations.

The equation for the circuit operation from V_{end} to V_{rem} remains the same:

$$V_{\text{rem}} = -V_{\text{end}}\gamma + V_{\text{cc}}(1+\gamma) \tag{5.13}$$

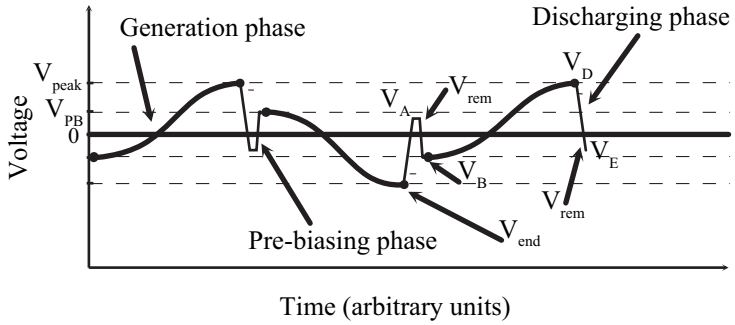


Figure 5.6: Piezoelectric voltage waveform for negative pre-bias case assuming V_{rem} is significant.

However for the second part of the circuit operation from $-V_{\text{rem}}$ to V_{PB}, V_{PB} is negative hence:

$$V_{\text{pb}} = -(V_{\text{rem}}\gamma + (V_{\text{cc}})(1+\gamma)) \tag{5.14}$$

Substituting (5.7) into this expression and simplifying gives

$$V_{\text{pb}} = -(-V_{\text{end}}\gamma + V_{\text{cc}}(1+\gamma))\gamma - V_{\text{cc}}(1+\gamma). \tag{5.15}$$

Thus substituting V_{end} with $V_{\text{pb}} + 2V_{\text{po}}$ and rearranging, gives the V_{cc} required for the negative pre-bias case:

$$V_{\text{pb}} = -(-(V_{\text{pb}} + 2V_{\text{po}})\gamma + V_{\text{cc}}(1+\gamma))\gamma + V_{\text{cc}}(1+\gamma) \tag{5.16}$$

$$V_{\text{pb}} = -V_{\text{cc}}\gamma^2 + V_{\text{pb}}\gamma^2 + 2V_{\text{po}}\gamma^2 - 2V_{\text{cc}}\gamma - V_{\text{cc}} \tag{5.17}$$

$$V_{\text{cc}} = \frac{\gamma^2 2V_{\text{po}} + V_{\text{pb}}(\gamma^2 - 1)}{(1+\gamma)^2} \tag{5.18}$$

5.1.3.4 Zero pre-bias voltage

The pre-bias voltage may also be equal to 0 V (Figure 5.7), in which case setting $V_{\text{pb}} = 0$ in either (5.12) or (5.18) results in the same solution:

$$V_{\text{cc}} = \frac{\gamma^2 2V_{\text{po}}}{(1+\gamma)^2}. \tag{5.19}$$

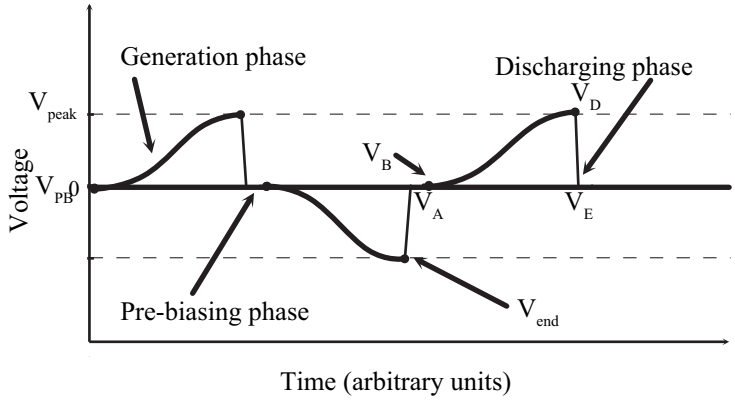


Figure 5.7: Piezoelectric voltage waveform for zero pre-bias case.

5.1.3.5 Electrical Parameters

Table 5.2 shows the electrical parameters used to size the MOSFET semiconductor area and inductor used for both the power conditioning circuit and the buck converter.

Table 5.2: Electrical parameters

Parameter	Variable	Value	Units
Electron mobility	μ_{e}	0.15	$\mathrm{m}^2\ (\mathrm{V\ s})^{-1}$
Hole mobility	μ_{h}	0.05	$\mathrm{m}^2\ (\mathrm{V\ s})^{-1}$
Constant, n-type	k_{epiN}	2 x10^{-11}	$\Omega\mathrm{m}^2\ \mathrm{V}^{-2}$
Constant, p-type	k_{epiP}	6 x10^{-11}	$\Omega\mathrm{m}^2\ \mathrm{V}^{-2}$
Inductor constant	K_{L}	0.23	$\mathrm{H\ m}^{-2}\Omega^{-1}$
Inductor volume	V_{L}	0.5 S^3	m^3
Leakage current constant	k_{ll}	3.9 x10^{-4}	$\mathrm{m}^{-2}\Omega^{-1}$
Parasitic capacitance constant	k_{cj}	1.1 x10^{-3}	$\mathrm{C\ m}^{-2}$
Diode threshold voltage	V_{o}	0.7	V
Battery voltage	V_{batt}	1.5	V

5.1.4 Energy Storage

The target battery voltage is 1.5 V however V_{cc} required for the optimal pre-bias voltage may be much greater than this. Therefore a buck converter is used (Figure 5.4) to both step the voltage down to charge the battery and maintain the V_{cc} at the optimal value else the voltage

will rise each cycle as energy is harvested. The buck circuit is assumed to operate once per cycle, however this could be reduced if the intermediate capacitor was made larger which would reduce the variation in V_{cc} per cycle. If the voltage was less than 1.5 V, a boost circuit could be used to step the voltage up.

5.1.5 Effectiveness, Efficiency and Power

The system effectiveness of the harvester, η_{sys}, is defined as the fraction of final power outputted (including buck converter circuit losses), P_{out}, from the theoretical maximum available energy, P_{max}, available from the acceleration, A_{input}, and frequency, ω_{input}, of the vibration source for a given available volume and mass density, ρ_{mass}.

$$\eta_{\text{sys}} = \frac{P_{\text{out}}}{P_{\text{max}}} \tag{5.20}$$

where the theoretical maximum available energy [36] is determined by:

$$P_{\text{max}} = \rho_{\text{mass}} A_{\text{input}} \omega_{\text{input}} \frac{S^4}{16}. \tag{5.21}$$

The system effectiveness can also be defined as the product of the coupling efficiency, η_{coup}, extraction efficiency, $\eta_{\text{extraction}}$, and conversion efficiency (from the harvester into the storage element), η_{conv},

$$\eta_{\text{coup}} = \frac{E_{\text{coup}}}{E_{\text{max}}} \tag{5.22}$$

$$\eta_{\text{extraction}} = \frac{E_{\text{harv}}}{E_{\text{coup}}} \tag{5.23}$$

$$\eta_{\text{conv}} = \frac{E_{\text{out}}}{E_{\text{harv}}}. \tag{5.24}$$

E_{coup} is the energy generated by the piezoelectric transducer as a result of coupling to the mechanical input vibrations, E_{harv} is the energy harvested after the losses of the interface

circuit are accounted for. E_{out} is the final output energy from the system in to the energy storage element. In order to achieve the highest system effectiveness, it is therefore necessary to maximise the product of each of these efficiencies.

5.2 Optimisation algorithm overview

Figure 5.8 shows the algorithm used to calculate the power generated by the SSPB technique (the bridge rectifier algorithm is given in 9). The algorithm requires the side length range (e.g. 1 mm to 15 mm), the acceleration (e.g. 0.01 ms^{-2} to 100 ms^{-2}), the mass material and density (e.g. Gold, 19320 $kg\ m^{-3}$ [110]), driving frequency (100 Hz) and the number of length and acceleration combinations (e.g. 15x15=225 points) to be specified. The optimisation is solved numerically using ideal equations to provide a starting point then adding losses and iterating until steady state conditions are found. The viable parameter solution with highest power generation is then selected as the solution for that combination of volume and acceleration.

Initially combinations of beam lengths and thicknesses which result in a resonant frequency within 1 % of the target resonant frequency are found. The pre-bias voltage, V_{pb}, required to ensure the mass stays within the confines of the volume, is then calculated. The dielectric breakdown voltage (determined by the piezoelectric material and layer thickness) is then checked to ensure that the pre-bias voltage plus twice the induced voltage, $2V_{\text{po}}$, do not exceed it. If the voltage is exceeded, V_{po} is reduced by decreasing the mass displacement. If this results in negative V_{po}, then no solution can be found and the beam length-thickness combination is skipped, however if the combination is viable then the SSPB modelling is implemented.

Each element in the vector of circuit inversion values (γ) is tested for performance in the SSPB circuit. An initial estimate of the intermediate supply voltage, V_{cc}, is made using (5.12) and (5.18). This is used to calculate the blocking voltage of the MOSFETs, V_{B}, the MOSFET semiconductor area, A_{semi}, and the inductance, L.

The pre-bias voltage, V_{pb}, and end voltage, V_{end} assume no charge redistribution or leakage

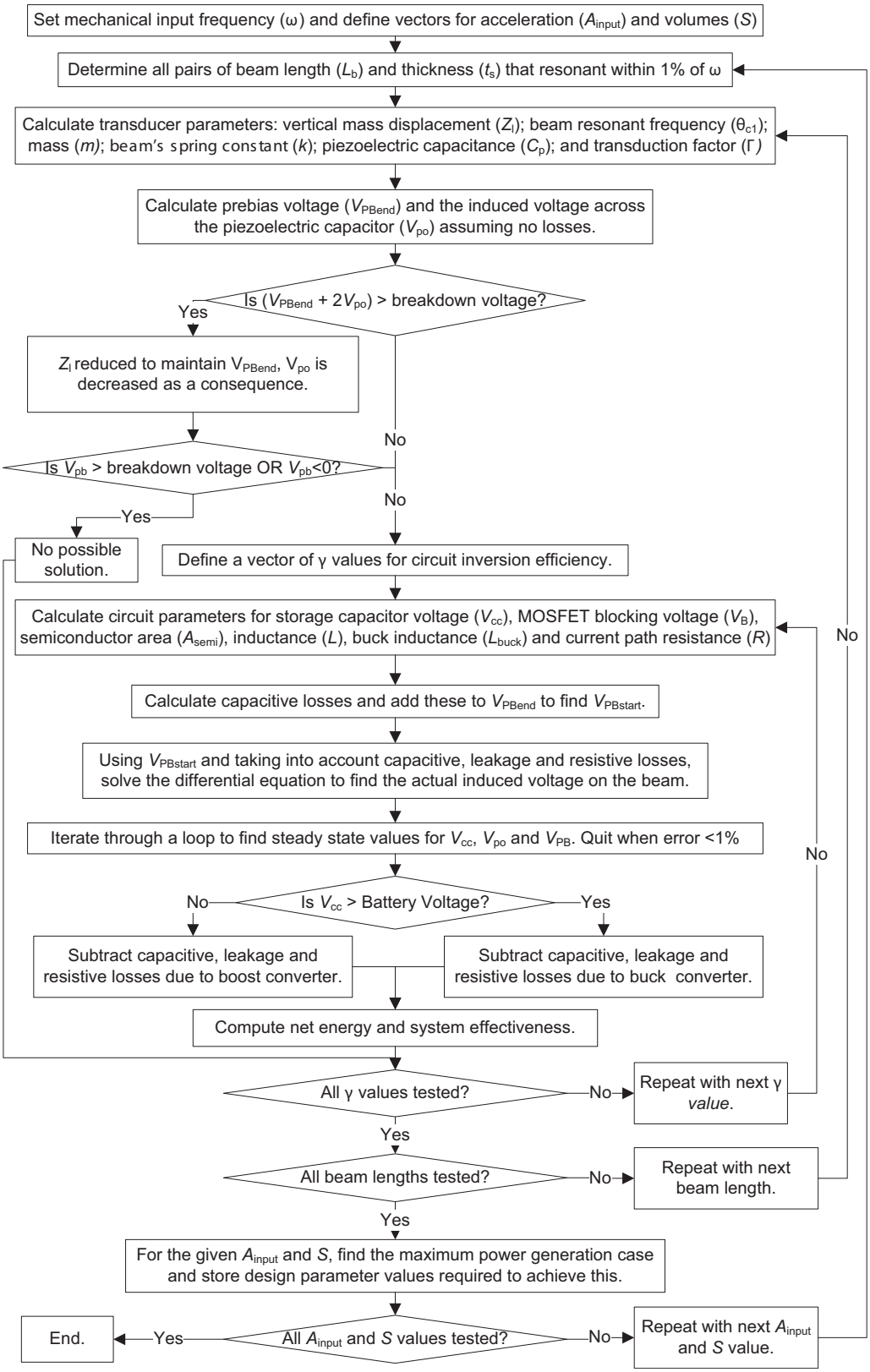


Figure 5.8: Algorithm used to calculate power generation using an SSPB circuit.

current losses. Therefore an iterative numerical solution is used to recalculate the circuit parameters to allow for these non-idealities. The charge redistribution results in the final pre-bias voltage V_{PBend} being less than the pre-bias voltage start voltage, V_{PBstart}, as shown in Figure 5.9. Similarly the $V_{\mathrm{end}_{\mathrm{ideal}}}$ is reduced to $V_{\mathrm{end}_{\mathrm{actual}}}$.

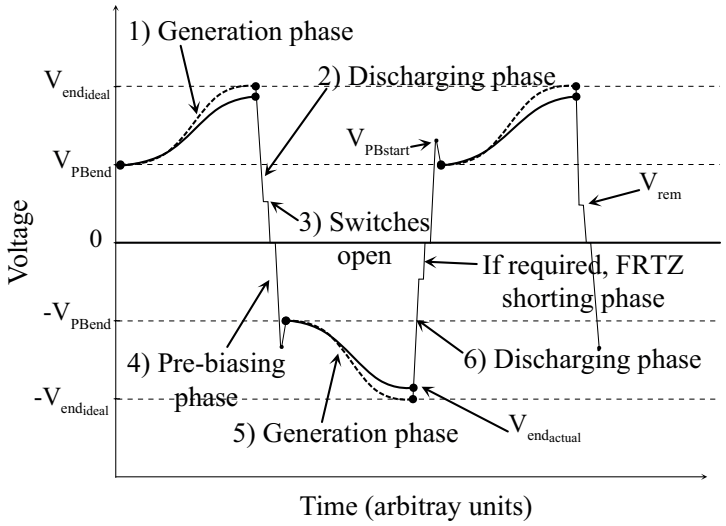


Figure 5.9: The voltage losses due to charge redistribution cause the difference between V_{PBstart} and V_{PBend}, while parasitic resistances and leakage currents are responsible for the voltage reaching only $V_{\mathrm{end}_{\mathrm{actual}}}$ instead of $V_{\mathrm{end}_{\mathrm{ideal}}}$. The remaining voltage after discharge, V_{rem}, which may be zero or nonzero, is also illustrated.

Once the iteration error is less than 1 %, the losses for the buck or boost circuit used to step the voltage down or up respectively, are calculated. The net energy and system effectiveness are then calculated and the combination of beam length and thickness which produce the highest power output is reported for that acceleration and volume combination along with their associated parameters.

5.3 Model Parameters

This section details the derivations for the MOSFET and inductor sizing used in model's algorithm.

Section 2.3.6 stated that the Q-factor of the electrical path determines the amount of charge moved between the piezoelectric capacitance and the intermediate storage capacitor. However this value is determined by the series resistance of the MOSFETs, R_{mos},which is the sum of the on-state resistances of the high and low side p-type MOSFETs, and a low side n-type MOSFET. The on-state resistance of a MOSFET, R_{on}, is given as

$$R_{\text{on}} = \frac{k_{\text{epi}} {V_{\text{B}}}^2}{A_{\text{semi}}}, \tag{5.25}$$

where k_{epi} is constant ($k_{\text{epiN}} = 2 \times 10^{-11}\ \Omega\text{m}^2\text{V}^{-2}$, $k_{\text{epiP}} \approx 3k_{\text{epiN}}$), V_{B} is the blocking voltage for each MOSFET as stated in Table 3.1, and A_{semi} is the cross sectional area of the MOSFETs [111].

This would therefore suggest that maximising A_{semi} would yield the highest Q-factor and thus the greatest power generation. However increasing A_{semi} also increases the semiconductor device's parasitic capacitances, thus an optimal solution for A_{semi} exists and was found iteratively. Since all the MOSFETs conduct the same peak and average currents, the same value of A_{semi} was used for all devices.

Q-factor is also affected by the inductor which we assume takes the form of a Brooks coil [3] (Figure 5.10). The inductance is calculated as

$$L = K_{\text{L}} R_{\text{L}} {V_{\text{L}}}^{\frac{2}{3}} \tag{5.26}$$

where K_{L} is a constant (Table 5.2), V_{L} is the inductor volume and R_{L} is the inductor resistance. R_{L} is specified through the ratio $c = R_{\text{L}}/R_{\text{mos}}$.

The Q-factor of a series RLC circuit is defined as $Q = \sqrt{L/C_{\text{p}}}/(R_{\text{mos}} + R_{\text{L}})$ which, by use of the definitions above, can be solved with respect to the semiconductor area as follows. Substituting (5.26) into Q

$$Q = \sqrt{\frac{K_{\text{L}} R_{\text{L}} {V_{\text{L}}}^{\frac{2}{3}}}{C_{\text{p}}}} \frac{1}{R_{\text{mos}} + R_{\text{L}}}, \tag{5.27}$$

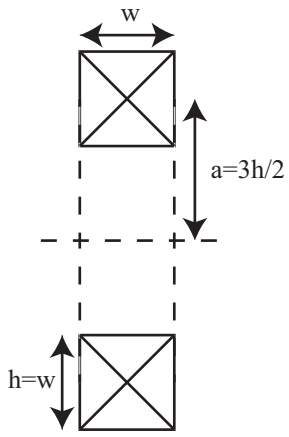


Figure 5.10: The optimum shape for a multi layer coil - Brooks coil [112].

then setting $R_{\mathrm{L}} = R_{\mathrm{mos}}c$ to form

$$Q = \sqrt{\frac{K_{\mathrm{L}} R_{\mathrm{mos}} c {V_{\mathrm{L}}}^{\frac{2}{3}}}{C_{\mathrm{p}}}} \frac{1}{R_{\mathrm{mos}} + R_{\mathrm{mos}}c}. \tag{5.28}$$

Simplifying

$$Q = \sqrt{\frac{K_{\mathrm{L}} R_{\mathrm{mos}} c {V_{\mathrm{L}}}^{\frac{2}{3}}}{C_{\mathrm{p}}}} \frac{1}{R_{\mathrm{mos}}(1+c)}, \tag{5.29}$$

and rearranging to make $1/R_{\mathrm{mos}}$ the subject

$$\frac{1}{R_{\mathrm{mos}}} = \frac{C_{\mathrm{p}} Q^2 (c+1)^2}{K_{\mathrm{L}} {V_{\mathrm{L}}}^{\frac{2}{3}} c}. \tag{5.30}$$

Substituting $R_{\mathrm{mos}} = \sum R_{\mathrm{on}}$ using the definition (5.25) gives

$$\frac{A_{\mathrm{semi}}}{\sum k_{\mathrm{epi}} {V_{\mathrm{B}}}^2} = \frac{C_{\mathrm{p}} Q^2 (c+1)^2}{K_{\mathrm{L}} {V_{\mathrm{L}}}^{\frac{2}{3}} c}, \tag{5.31}$$

which can be rearranged to

$$A_{\mathrm{semi}} = \frac{(1+c)^2 Q^2 C_{\mathrm{p}} \sum (k_{\mathrm{epi}} {V_{\mathrm{B}}}^2)}{c K_{\mathrm{L}} {V_{\mathrm{L}}}^{2/3}} \tag{5.32}$$

where the summation accounts for the different resistances of each MOSFET due to differing required blocking voltages and differences between carrier mobilities. The constants used are $k_{\text{epiN}} = 2 \times 10^{-11}\ \Omega\text{m}^2\text{V}^{-2}$, $k_{\text{epiP}} \approx 3k_{\text{epiN}}$, $K_{\text{L}} = 0.23\ \text{H}\Omega^{-1}\text{m}^{-2}$ and c = 1 [111, 23]. Both the SSPB inductor and the buck inductor are assumed to occupy half of the volume $V_{\text{L}} = 0.5S^3$.

5.4 Energy loss calculations

This section details the equations used to calculate the losses due to leakage currents, charge redistribution and conduction in the SSPB circuit. They can be calculated using the expressions derived in Section 5.3. Reverse recovery losses in the MOSFETs' anti parallel diodes are zero due to the fact the diodes never conduct. The general form of the equations used to calculate energy losses associated with leakage, $E_{\text{I,loss}}$, charge redistribution, $E_{\text{C,loss}}$, and conduction, $E_{\text{R,loss}}$, are

$$E_{\text{I,loss}} = I_{\text{l}} V_{\text{cc}} \Delta t \tag{5.33}$$

$$E_{\text{C,loss}} = Q_{\text{j}} V_{\text{cc}} \tag{5.34}$$

$$E_{\text{R,loss}} = {i_{\text{L}}}^2 (R_{\text{mos}} + R_{\text{L}}) \Delta t \tag{5.35}$$

where I_{l} is the leakage of MOSFET in the off-state, Q_{j} is charge on the MOSFET, i_{L} is current in the inductor and Δt is the on-state conduction time.

5.4.1 Current Leakage

The general form of the current leakage loss, I_{l}, of a MOSFET in the off-state is given by

$$I_{\text{l}} = k_{\text{I}_{\text{l}}} A_{\text{semi}} \sqrt{V_0 - V_{\text{operation}}} \sqrt{V_{\text{B}}} \tag{5.36}$$

where $k_{\text{I}_{\text{l}}} = 3.9 \times 10^{-4}\ \text{m}^{-2}\Omega^{-1}$, V_0 is the diode threshold voltage of 0.7 V, $V_{\text{operation}}$ is the reverse bias voltage across the diode, and V_{B} is the MOSFET blocking voltage [23].

The general form of the parasitic capacitive leakage loss, I_{c}, is given by:

$$I_{\mathrm{c}} = C_{\mathrm{j}} \frac{dV}{d(t)} \tag{5.37}$$

where C_{j} is the parasitic capacitance from [23]:

$$C = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{operation}})\, V_{\mathrm{B}}}}. \tag{5.38}$$

The losses will vary depending on the respective voltages V_{piezo} (voltage across the piezoelectric capacitance) and V_{cc} as different devices will be in the on and off-states as the cantilever deflects. Therefore all of this analysis will be done in the following case order.

$$\begin{aligned}
\text{Case1} &: V_{\mathrm{piezo}} > V_{\mathrm{cc}} \\
\text{Case2} &: 0 < V_{\mathrm{piezo}} < V_{\mathrm{cc}} \\
\text{Case3} &: -V_{\mathrm{cc}} < V_{\mathrm{piezo}} < 0 \\
\text{Case4} &: V_{\mathrm{piezo}} < -V_{\mathrm{cc}}
\end{aligned}$$

Note that the same polarity across the piezoelectric transducer will be taken, hence V_{cc} may be negative when the beam is deflecting in the opposite direction.

5.4.1.1 Current Leakage Case 1

Figure 5.11 shows the derivation of the leakage currents present in Case 1 ($V_{\mathrm{piezo}} > V_{\mathrm{cc}}$) by considering the parasitic diodes across the MOSFET switches. Since node Y is clamped to V_{cc}, diodes D_3, D_4 and D_5 are forced into conduction whilst D_1, D_2 and D_6 are blocking. D_6 is only blocking V_{cc} and thus can be ignored when calculating the leakage from the piezoelectric capacitance as the supply leakage current is calculated in Section 5.4.1.5. The inductor also appears as a short, resulting in the simplified leakage current diagram shown.

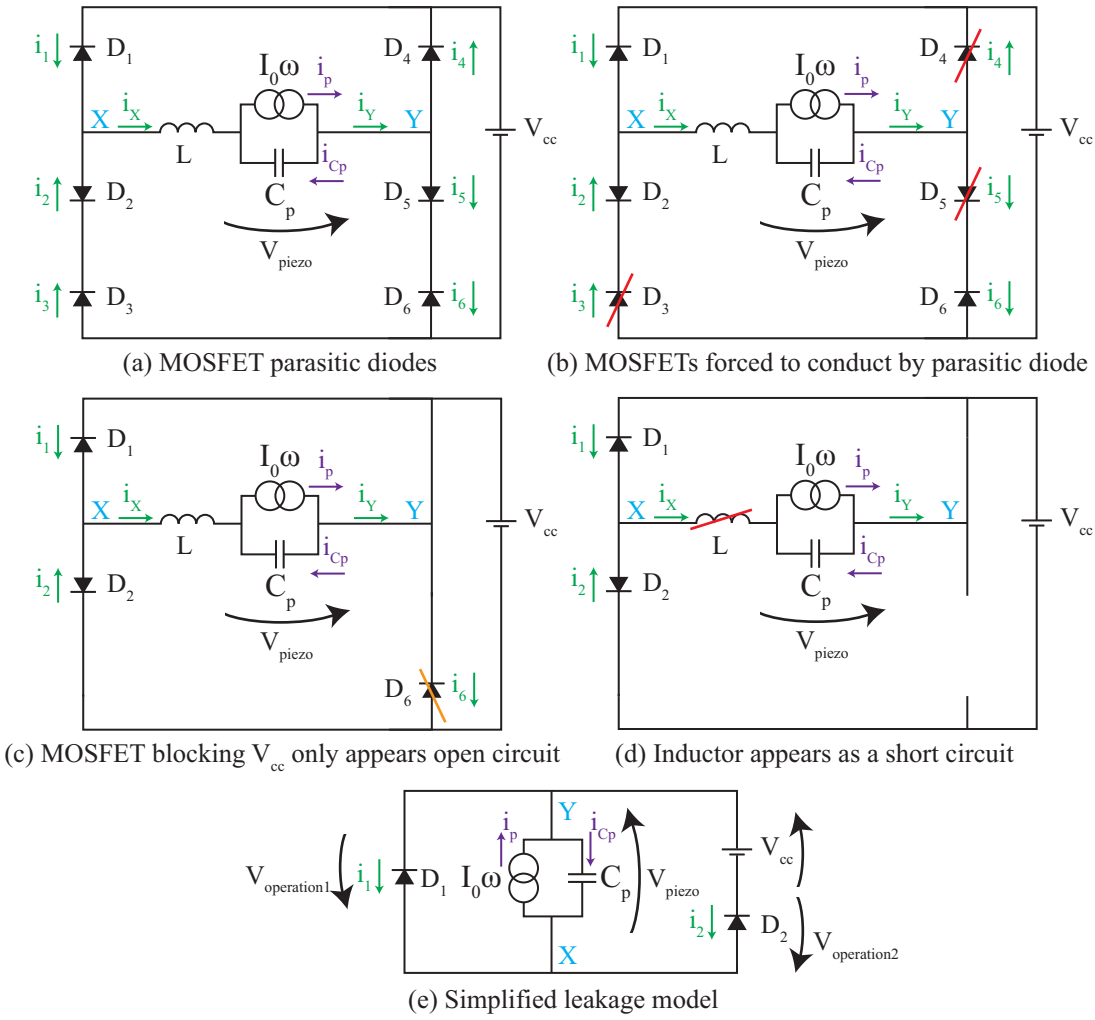


Figure 5.11: Leakage currents in H-bridge for case 1.

The current leakages from (5.36) therefore are:

$$i_{l1}(t) = k_{I_l} A_{\text{semi}} \sqrt{V_0 - V_{\text{operation}_1}} \sqrt{V_{B1}} \tag{5.39}$$

$$i_{l2}(t) = k_{I_l} A_{\text{semi}} \sqrt{V_0 - V_{\text{operation}_2}} \sqrt{V_{B2}} \tag{5.40}$$

where:

$$V_{\text{operation}_1} = -V_{\text{piezo}}(t) \tag{5.41}$$

$$V_{\text{operation}_2} = -V_{\text{piezo}}(t) + V_{\text{cc}} \tag{5.42}$$

where $V_{\text{piezo}}(t)$ is the voltage induced across the piezoelectric capacitance. Therefore:

$$i_{\text{l1}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 + V_{\text{piezo}}(t)} \sqrt{V_{\text{B1}}} \tag{5.43}$$

$$i_{\text{l2}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 + V_{\text{piezo}}(t) - V_{\text{cc}}} \sqrt{V_{\text{B2}}} \tag{5.44}$$

The capacitive leakage currents from (5.37) and (5.38) therefore are:

$$i_{\text{c1}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{operation}})\, V_{\text{B1}}}} \frac{dV}{d(t)} \tag{5.45}$$

$$i_{\text{c2}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{operation}})\, V_{\text{B2}}}} \frac{dV}{d(t)} \tag{5.46}$$

$$i_{\text{Cp}}(t) = C_{\text{p}} \frac{dV_{\text{piezo}}(t)}{d(t)} \tag{5.47}$$

Substituting in (5.41) and (5.42) gives:

$$i_{\text{c1}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 + V_{\text{piezo}}(t))\, V_{\text{B1}}}} \frac{dV}{d(t)} \tag{5.48}$$

$$i_{\text{c2}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 + V_{\text{piezo}}(t) - V_{\text{cc}})\, V_{\text{B2}}}} \frac{dV}{d(t)} \tag{5.49}$$

$$i_{\text{Cp}}(t) = C_{\text{p}} \frac{dV_{\text{piezo}}(t)}{d(t)}. \tag{5.50}$$

Applying Kirchoff's current law at node Y gives the total leakage current:

$$i_{\text{p}}(t) = i_{\text{l1}}(t) + i_{\text{c1}}(t) + i_{\text{l2}}(t) + i_{\text{c2}}(t) + i_{\text{Cp}}(t) \tag{5.51}$$

where $i_{\mathrm{p}}(t)$ is the product of the piezoelectric transduction Γ and the mass velocity $\dot{z}(t)$ thus:

$$\begin{aligned}
\Gamma\dot{z}(t) &= i_{\mathrm{p}}(t) \qquad (5.52)\\
\Gamma\dot{z}(t) &= k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0+V_{\mathrm{piezo}}(t)}\sqrt{V_{\mathrm{B1}}}\\
&+ \frac{k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{(V_0+V_{\mathrm{piezo}}(t))\,V_{\mathrm{B1}}}}\frac{dV}{d(t)}\\
&+ k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0+V_{\mathrm{piezo}}(t)-V_{\mathrm{cc}}}\sqrt{V_{\mathrm{B2}}}\\
&+ \frac{k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{(V_0+V_{\mathrm{piezo}}(t)-V_{\mathrm{cc}})\,V_{\mathrm{B2}}}}\frac{dV}{d(t)}\\
&+ C_{\mathrm{p}}\frac{dV_{\mathrm{piezo}}(t)}{d(t)}
\end{aligned}$$

5.4.1.2 Current Leakage Case 2

Figure 5.12 shows the derivation of the leakage currents present in Case 2 ($0 < V_{\mathrm{piezo}} < V_{\mathrm{cc}}$) by considering the parasitic diodes across the MOSFET switches. Since node Y is clamped to V_{cc}, node X will now vary between 0 V and V_{cc}, thus diodes D_2, D_4 and D_5 are forced into conduction whilst D_1, D_3 and D_6 are blocking. D_6 is now only blocking V_{cc} and thus can be ignored when calculating the leakage from the piezoelectric capacitance (see Section 5.4.1.5 for supply leakage current loss). The inductor also appears as a short, resulting in the simplified leakage current diagram shown.

The current leakages from (5.36) therefore are:

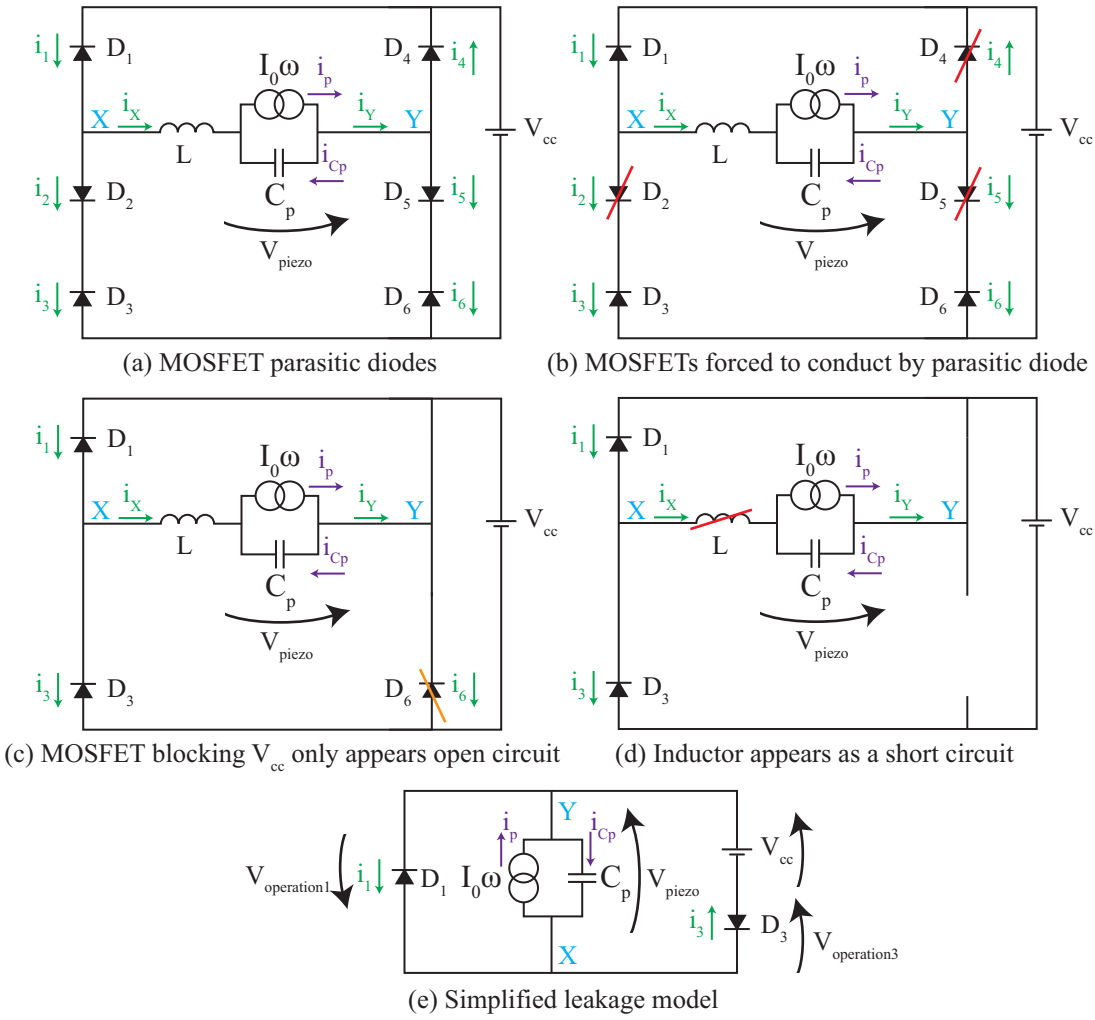
$$i_{\mathrm{l1}}(t) = k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0-V_{\mathrm{operation_1}}}\sqrt{V_{\mathrm{B1}}} \qquad (5.53)$$

$$i_{\mathrm{l3}}(t) = k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0-V_{\mathrm{operation_3}}}\sqrt{V_{\mathrm{B3}}} \qquad (5.54)$$

where:

$$V_{\mathrm{operation_1}} = -V_{\mathrm{piezo}}(t) \qquad (5.55)$$

$$V_{\mathrm{operation_3}} = V_{\mathrm{piezo}}(t) - V_{\mathrm{cc}} \qquad (5.56)$$



(a) MOSFET parasitic diodes

(b) MOSFETs forced to conduct by parasitic diode

(c) MOSFET blocking V_{cc} only appears open circuit

(d) Inductor appears as a short circuit

(e) Simplified leakage model

Figure 5.12: Leakage currents in H-bridge for case 2.

where $V_{\text{piezo}}(t)$ is the voltage induced across the piezoelectric capacitance. Therefore:

$$i_{\text{l1}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 + V_{\text{piezo}}(t)} \sqrt{V_{\text{B1}}} \tag{5.57}$$

$$i_{\text{l3}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 - V_{\text{piezo}}(t) + V_{\text{cc}}} \sqrt{V_{\text{B3}}} \tag{5.58}$$

The capacitive leakage currents from (5.37) and (5.38) therefore are:

$$i_{\mathrm{c1}}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{operation}})\, V_{\mathrm{B1}}}} \frac{dV}{d(t)} \tag{5.59}$$

$$i_{\mathrm{c3}}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{operation}})\, V_{\mathrm{B3}}}} \frac{dV}{d(t)} \tag{5.60}$$

$$i_{\mathrm{Cp}}(t) = C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)} \tag{5.61}$$

Substituting in (5.55) and (5.56) gives:

$$i_{\mathrm{c1}}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 + V_{\mathrm{piezo}}(t))\, V_{\mathrm{B1}}}} \frac{dV}{d(t)} \tag{5.62}$$

$$i_{\mathrm{c3}}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}})\, V_{\mathrm{B3}}}} \frac{dV}{d(t)} \tag{5.63}$$

$$i_{\mathrm{Cp}}(t) = C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)}. \tag{5.64}$$

Applying Kirchoff's current law at node Y gives the total leakage current:

$$i_{\mathrm{p}}(t) = i_{\mathrm{l1}}(t) + i_{\mathrm{c1}}(t) - i_{\mathrm{l3}}(t) - i_{\mathrm{c3}}(t) + i_{\mathrm{Cp}}(t) \tag{5.65}$$

where $i_{\mathrm{p}}(t)$ is the product of the piezoelectric transduction Γ and the mass velocity $\dot{z}(t)$ thus:

$$\begin{aligned}
\Gamma \dot{z}(t) &= i_{\mathrm{p}}(t) \qquad (5.66)\\
\Gamma \dot{z}(t) &= k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 + V_{\mathrm{piezo}}(t)} \sqrt{V_{\mathrm{B1}}} \\
&+ \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 + V_{\mathrm{piezo}}(t))\, V_{\mathrm{B1}}}} \frac{dV}{d(t)} \\
&- k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}}} \sqrt{V_{\mathrm{B3}}} \\
&- \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}})\, V_{\mathrm{B3}}}} \frac{dV}{d(t)} \\
&+ C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)}
\end{aligned}$$

5.4.1.3 Current Leakage Case 3

Figure 5.13 shows the derivation of the leakage currents present in Case 3 ($-V_{cc} < V_{piezo} < 0$) by considering the parasitic diodes across the MOSFET switches. In this case node X is now clamped to V_{cc} and node Y will now vary between 0 V and V_{cc}, thus diodes D_1, D_2 and D_5 are forced into conduction whilst D_3, D_4 and D_6 are blocking. D_3 is only blocking V_{cc} and thus can be ignored when calculating the leakage from the piezoelectric capacitance (see Section 5.4.1.5 for supply leakage current loss). The inductor also appears as a short, resulting in the simplified leakage current diagram shown.

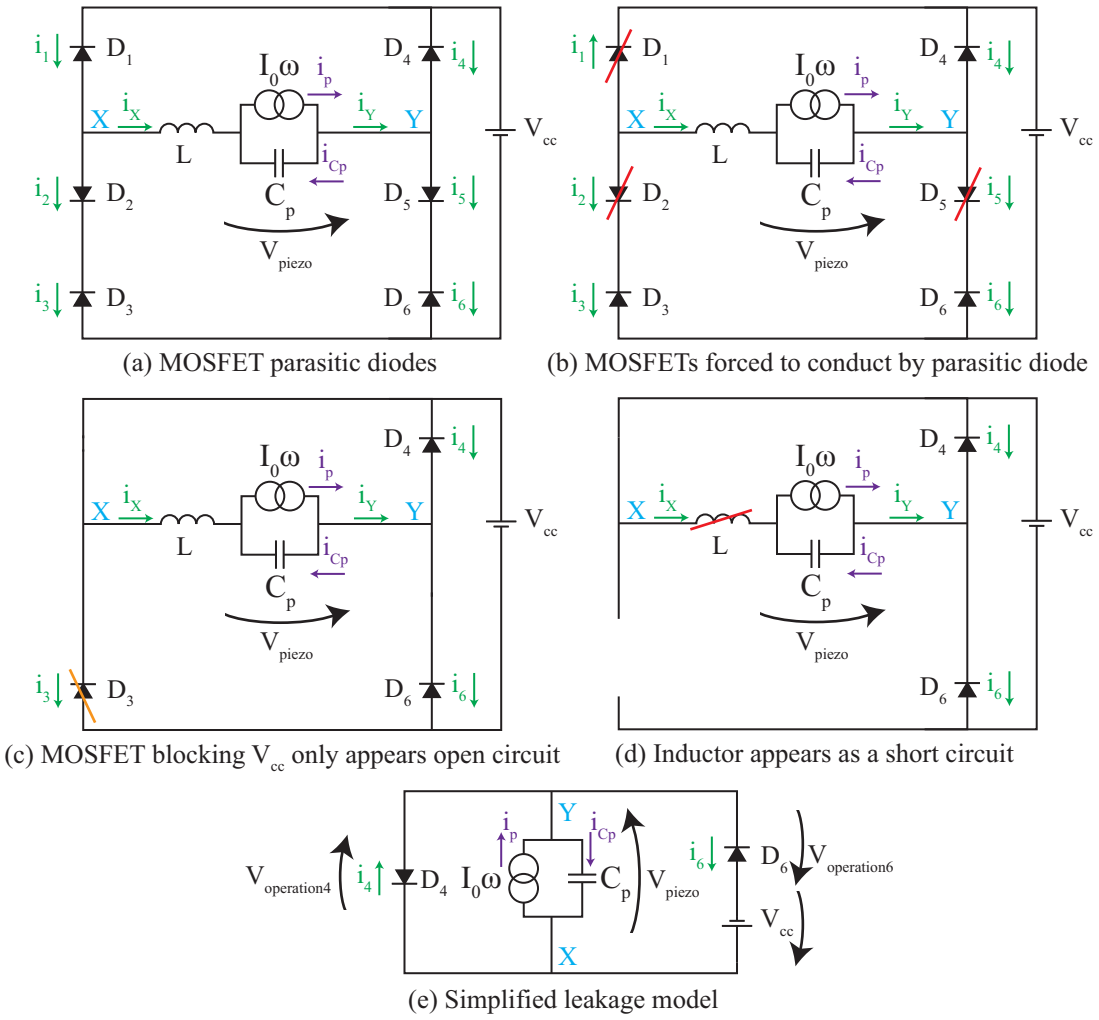


Figure 5.13: Leakage currents in H-bridge for case 3.

The current leakages from (5.36) therefore are:

$$i_{\mathrm{l}4}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{operation}_4}} \sqrt{V_{\mathrm{B4}}} \tag{5.67}$$

$$i_{\mathrm{l}6}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{operation}_6}} \sqrt{V_{\mathrm{B6}}} \tag{5.68}$$

where:

$$V_{\mathrm{operation}_4} = V_{\mathrm{piezo}}(t) \tag{5.69}$$

$$V_{\mathrm{operation}_6} = -V_{\mathrm{piezo}}(t) - V_{\mathrm{cc}} \tag{5.70}$$

where $V_{\mathrm{piezo}}(t)$ is the voltage induced across the piezoelectric capacitance. Therefore:

$$i_{\mathrm{l}4}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{piezo}}(t)} \sqrt{V_{\mathrm{B4}}} \tag{5.71}$$

$$i_{\mathrm{l}6}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 + V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}}} \sqrt{V_{\mathrm{B6}}} \tag{5.72}$$

The capacitive leakage currents from (5.37) and (5.38) therefore are:

$$i_{\mathrm{c}4}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{operation}})\, V_{\mathrm{B4}}}} \frac{dV}{d(t)} \tag{5.73}$$

$$i_{\mathrm{c}6}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{operation}})\, V_{\mathrm{B6}}}} \frac{dV}{d(t)} \tag{5.74}$$

$$i_{\mathrm{Cp}}(t) = C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)} \tag{5.75}$$

Substituting in (5.69) and (5.70) gives:

$$i_{\mathrm{c}4}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t))\, V_{\mathrm{B4}}}} \frac{dV}{d(t)} \tag{5.76}$$

$$i_{\mathrm{c}6}(t) = \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 + V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}})\, V_{\mathrm{B6}}}} \frac{dV}{d(t)} \tag{5.77}$$

$$i_{\mathrm{Cp}}(t) = C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)}. \tag{5.78}$$

Applying Kirchoff's current law at node Y gives the total leakage current:

$$i_{\mathrm{p}}(t) = -i_{\mathrm{l4}}(t) - i_{\mathrm{c4}}(t) + i_{\mathrm{l6}}(t) + i_{\mathrm{c6}}(t) + i_{\mathrm{Cp}}(t) \tag{5.79}$$

where $i_{\mathrm{p}}(t)$ is the product of the piezoelectric transduction Γ and the mass velocity $\dot{z}(t)$ thus:

$$\begin{aligned}
\Gamma\dot{z}(t) &= i_{\mathrm{p}}(t) \qquad (5.80)\\
\Gamma\dot{z}(t) &= -k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{piezo}}(t)} \sqrt{V_{\mathrm{B4}}} \\
&- \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t))\, V_{\mathrm{B4}}}} \frac{dV}{d(t)} \\
&+ k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 + V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}}} \sqrt{V_{\mathrm{B6}}} \\
&+ \frac{k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{(V_0 + V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}})\, V_{\mathrm{B6}}}} \frac{dV}{d(t)} \\
&+ C_{\mathrm{p}} \frac{dV_{\mathrm{piezo}}(t)}{d(t)}
\end{aligned}$$

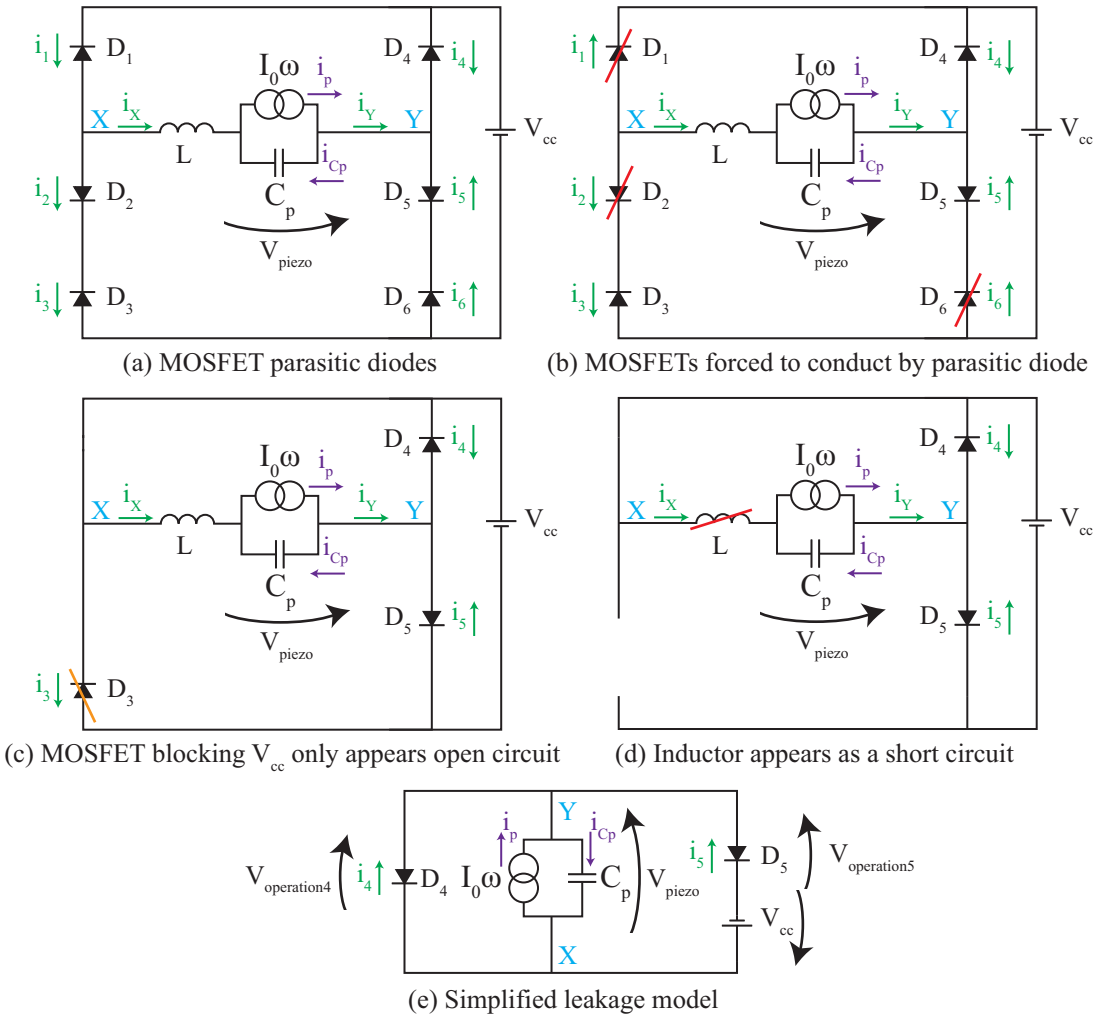
5.4.1.4 Current Leakage Case 4

Figure 5.14 shows the derivation of the leakage currents present in Case 4 ($V_{\mathrm{piezo}} < -V_{\mathrm{cc}}$) by considering the parasitic diodes across the MOSFET switches. In this case node X is clamped to V_{cc} and node Y will be less than 0 V, thus diodes D_1, D_2 and D_6 are forced into conduction whilst D_3, D_4 and D_5 are blocking. D_3 is only blocking V_{cc} and thus can be ignored when calculating the leakage from the piezoelectric capacitance (see Section 5.4.1.5 for supply leakage current loss). The inductor also appears as a short, resulting in the simplified leakage current diagram shown.

The current leakages from (5.36) therefore are:

$$i_{\mathrm{l4}}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{operation_4}}} \sqrt{V_{\mathrm{B4}}} \tag{5.81}$$

$$i_{\mathrm{l5}}(t) = k_{\mathrm{I_l}} A_{\mathrm{semi}} \sqrt{V_0 - V_{\mathrm{operation}}} \sqrt{V_{\mathrm{B5}}} \tag{5.82}$$



(a) MOSFET parasitic diodes

(b) MOSFETs forced to conduct by parasitic diode

(c) MOSFET blocking V_{cc} only appears open circuit

(d) Inductor appears as a short circuit

(e) Simplified leakage model

Figure 5.14: Leakage currents in H-bridge for case 4.

where:

$$V_{\text{operation}_4} = V_{\text{piezo}}(t) \tag{5.83}$$

$$V_{\text{operation}_5} = V_{\text{piezo}}(t) - V_{\text{cc}} \tag{5.84}$$

where $V_{\text{piezo}}(t)$ is the voltage induced across the piezoelectric capacitance. Therefore:

$$i_{\text{l4}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 - V_{\text{piezo}}(t)} \sqrt{V_{\text{B4}}} \tag{5.85}$$

$$i_{\text{l5}}(t) = k_{\text{I}_\text{l}} A_{\text{semi}} \sqrt{V_0 - V_{\text{piezo}}(t) + V_{\text{cc}}} \sqrt{V_{\text{B5}}} \tag{5.86}$$

The capacitive leakage currents from (5.37) and (5.38) therefore are:

$$i_{\text{c4}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{operation}})\, V_{\text{B4}}}} \frac{dV}{d(t)} \tag{5.87}$$

$$i_{\text{c5}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{operation}})\, V_{\text{B5}}}} \frac{dV}{d(t)} \tag{5.88}$$

$$i_{\text{Cp}}(t) = C_{\text{p}} \frac{dV_{\text{piezo}}(t)}{d(t)} \tag{5.89}$$

Substituting in (5.83) and (5.84) gives:

$$i_{\text{c4}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{piezo}}(t))\, V_{\text{B4}}}} \frac{dV}{d(t)} \tag{5.90}$$

$$i_{\text{c5}}(t) = \frac{k_{\text{cj}} A_{\text{semi}}}{\sqrt{(V_0 - V_{\text{piezo}}(t) + V_{\text{cc}})\, V_{\text{B5}}}} \frac{dV}{d(t)} \tag{5.91}$$

$$i_{\text{Cp}}(t) = C_{\text{p}} \frac{dV_{\text{piezo}}(t)}{d(t)}. \tag{5.92}$$

Applying Kirchoff's current law at node Y gives the total leakage current:

$$i_{\text{p}}(t) = -i_{\text{l4}}(t) - i_{\text{c4}}(t) - i_{\text{l5}}(t) - i_{\text{c5}}(t) + i_{\text{Cp}}(t) \tag{5.93}$$

where $i_{\mathrm{p}}(t)$ is the product of the piezoelectric transduction Γ and the mass velocity $\dot{z}(t)$ thus:

$$\begin{aligned}
\Gamma\dot{z}(t) &= i_{\mathrm{p}}(t) \qquad (5.94)\\
\Gamma\dot{z}(t) &= -k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0 - V_{\mathrm{piezo}}(t)}\sqrt{V_{\mathrm{B4}}}\\
&- \frac{k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t))\,V_{\mathrm{B4}}}}\frac{dV}{d(t)}\\
&- k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{V_0 - V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}}}\sqrt{V_{\mathrm{B5}}}\\
&- \frac{k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{(V_0 - V_{\mathrm{piezo}}(t) + V_{\mathrm{cc}})\,V_{\mathrm{B5}}}}\frac{dV}{d(t)}\\
&+ C_{\mathrm{p}}\frac{dV_{\mathrm{piezo}}(t)}{d(t)}
\end{aligned}$$

5.4.1.5 MOSFET Supply leakage

Now that all the current leakage losses have been calculated, there is a final leakage current to be calculated which occurs continuously through either of the low side n-type MOSFET reverse diodes ($D3$ or $D6$) and the resulting energy loss over 1 mechanical harvester cycle is given by

$$i_{3\mathrm{l}} = i_{6\mathrm{l}} = k_{\mathrm{I_l}}A_{\mathrm{semi}}\sqrt{(V_0 + V_{\mathrm{cc}})V_{\mathrm{B,LoN}}} \qquad (5.95)$$

$$E_{i_{3\mathrm{l}},\mathrm{loss}} = E_{i_{6\mathrm{l}},\mathrm{loss}} = \frac{i_{6\mathrm{l}}V_{\mathrm{cc}}}{2f_0} \qquad (5.96)$$

where f_0 is the resonant frequency of the energy harvester.

5.4.2 Charge redistribution Losses

Immediately after piezoelectric capacitance is charged by the pre-bias voltage, the MOSFET switches open and charge redistribution occurs with the parasitic diodes across the MOSFET switches. The voltage on the piezoelectric capacitance therefore decreases from $V_{\mathrm{PB_{start}}}$ to $V_{\mathrm{PB_{end}}}$. To operate the piezoelectric harvester as a CDRG, $V_{\mathrm{PB_{end}}}$ is set to the calculated pre-bias voltage, V_{PB}. Therefore the circuit must allow for this redistribution when pre-biasing the piezoelectric capacitance by applying the V_{cc} required for $V_{\mathrm{PB_{start}}}$. To calculate $V_{\mathrm{PB_{start}}}$, the

charge sharing is calculated as follows.

The charge at the start, Q_{start} must equal the charge at the end Q_{end} of charge redistribution, therefore

$$V_{\text{PBstart}}C_{\text{p}} = V_{\text{PBend}}C_{\text{p}} + \sum Q_{\text{diodes}}, \tag{5.97}$$

where $\sum Q_{\text{diode}}$ is the total charge on the parasitic diodes. Using (5.38) and the identity $Q = CV$, the charge on a diode junction can be calculated:

$$Q_{\text{j}} = \frac{k_{\text{cj}}A_{\text{semi}}}{\sqrt{V_{\text{B}}}} \int_{V_{\text{operation1}}}^{V_{\text{operation2}}} \frac{1}{\sqrt{V_0 - V_{\text{operation}}}} dV_{\text{operation}} \tag{5.98}$$

Computing this integral with respect to the operating voltage, $V_{\text{operation}}$, over the region 0 V to $V_{\text{operation}}$, is the charge redistributed on a MOSFET parasitic diode:

$$Q_{\text{j}} = \frac{k_{\text{cj}}A_{\text{semi}}}{\sqrt{V_{\text{B}}}} \int_{V_{\text{operation}}}^{0} \frac{1}{\sqrt{V_0 - V_{\text{operation}}}} dV_{\text{operation}} \tag{5.99}$$

$$Q_{\text{j}} = \frac{k_{\text{cj}}A_{\text{semi}}}{\sqrt{V_{\text{B}}}} \left[-2\sqrt{V_0 - V_{\text{operation}}}\right]_{V_{\text{operation}}}^{0} \tag{5.100}$$

$$Q_{\text{j}} = \frac{2k_{\text{cj}}A_{\text{semi}}}{\sqrt{V_{\text{B}}}} \left[-\sqrt{V_0} + \sqrt{V_0 - V_{\text{operation}}}\right] \tag{5.101}$$

$$Q_{\text{j}} = \frac{2k_{\text{cj}}A_{\text{semi}}}{\sqrt{V_{\text{B}}}} \left(\sqrt{V_0 - V_{\text{operation}}} - \sqrt{V_0}\right) \tag{5.102}$$

For each V_{piezo} case, the amount of charge redistributed will depend on which switches become open circuit and their state of charge during the pre-bias stage.

5.4.2.1 Charge redistribution Case 1

Figure 5.15 shows the derivation of the charge redistribution present in Case 1 ($V_{\text{piezo}} > V_{\text{cc}}$) by considering the parasitic diodes across the MOSFET switches. Immediately before the switches open, the voltage on C_{p} is V_{PBstart}, the voltage across diodes D_1 and D_6 is V_{cc} and D_5 is a short circuit. MOSFETS 4, 2 and 3 open, however due to the MOSFET parasitic diodes, D_4, D_5 and D_3 remain short circuit. D_6 is blocking V_{cc}, however it was already charged to this voltage, so

does not effect charge redistribution and hence can be ignored along with the inductor.

Since the total charge before and after redistribution must be the same:

$$V_{\mathrm{PB}_{\mathrm{start}}} C_{\mathrm{p}} + Q_{\mathrm{D1}_{\mathrm{V_{cc}}}} = V_{\mathrm{PB}_{\mathrm{end}}} C_{\mathrm{p}} + Q_{\mathrm{D1}_{\mathrm{operation1}}} + Q_{\mathrm{D2}_{\mathrm{operation2}}} \tag{5.103}$$

where

$$\mathrm{operation1} = -V_{\mathrm{PB}_{\mathrm{end}}} \tag{5.104}$$

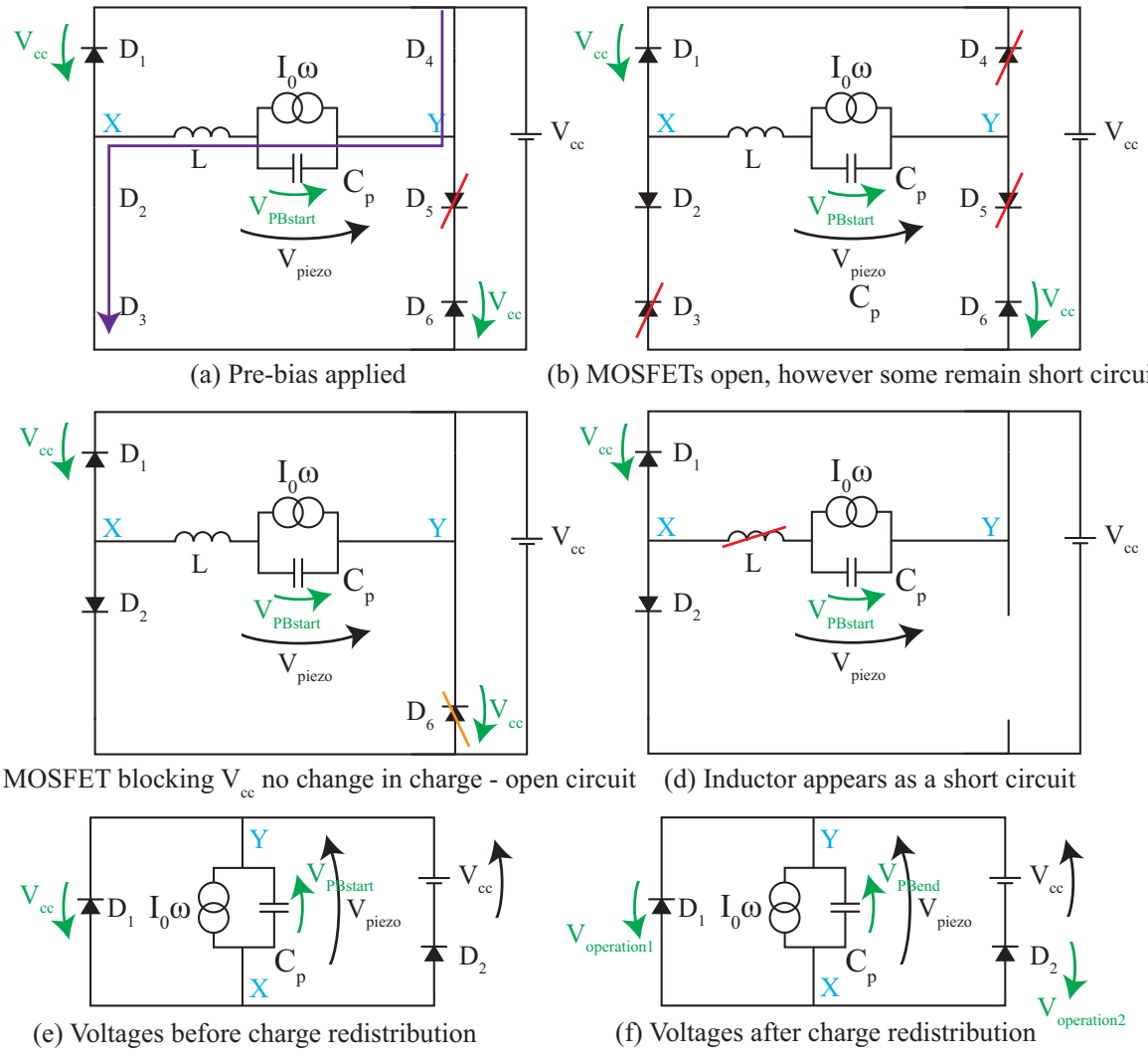
$$\mathrm{operation2} = -V_{\mathrm{PB}_{\mathrm{end}}} + V_{\mathrm{cc}}. \tag{5.105}$$

Therefore substituting (5.102):

$$\begin{aligned} V_{\mathrm{PB}_{\mathrm{start}}} C_{\mathrm{p}} &+ \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B1}}}} \left(\sqrt{V_0 + V_{\mathrm{cc}}} - \sqrt{V_0} \right) \\ &= V_{\mathrm{PB}_{\mathrm{end}}} C_{\mathrm{p}} \\ &+ \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B1}}}} \left(\sqrt{V_0 + V_{\mathrm{PB}_{\mathrm{end}}}} - \sqrt{V_0} \right) \\ &+ \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B2}}}} \left(\sqrt{V_0 + V_{\mathrm{PB}_{\mathrm{end}}} - V_{\mathrm{cc}}} - \sqrt{V_0} \right) \end{aligned} \tag{5.106}$$

Then rearranging to make $V_{\mathrm{PB}_{\mathrm{start}}}$ the subject:

$$\begin{aligned} V_{\mathrm{PB}_{\mathrm{start}}} &= V_{\mathrm{PB}_{\mathrm{end}}} \\ &- \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{C_{\mathrm{p}} \sqrt{V_{\mathrm{B1}}}} \left(\sqrt{V_0 + V_{\mathrm{cc}}} - \sqrt{V_0} \right) \\ &+ \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{C_{\mathrm{p}} \sqrt{V_{\mathrm{B1}}}} \left(\sqrt{V_0 + V_{\mathrm{PB}_{\mathrm{end}}}} - \sqrt{V_0} \right) \\ &+ \frac{2k_{\mathrm{cj}} A_{\mathrm{semi}}}{C_{\mathrm{p}} \sqrt{V_{\mathrm{B2}}}} \left(\sqrt{V_0 + V_{\mathrm{PB}_{\mathrm{end}}} - V_{\mathrm{cc}}} - \sqrt{V_0} \right) \end{aligned} \tag{5.107}$$



(a) Pre-bias applied

(b) MOSFETs open, however some remain short circuit

(c) MOSFET blocking V_{cc} no change in charge - open circuit

(d) Inductor appears as a short circuit

(e) Voltages before charge redistribution

(f) Voltages after charge redistribution

Figure 5.15: Redistribution of charge in H-bridge when switches open after pre-bias phase for case 1.

5.4.2.2 Charge redistribution Case 2

Figure 5.16 shows the derivation of the charge redistribution present in Case 2 ($0 < V_{\text{piezo}} < V_{\text{cc}}$) by considering the parasitic diodes across the MOSFET switches. Immediately before the switches open, the voltage on C_{p} is V_{PBstart}, the voltage across diodes D_1 and D_6 is V_{cc} and D_5 is a short circuit. MOSFETS 4, 2 and 3 open, however due to the MOSFET parasitic diodes, D_4, D_5 and D_2 remain short circuit. D_6 is blocking V_{cc}, however it was already charged to this voltage, so does not effect charge redistribution and hence can be ignored along with the inductor.

Since the total charge before and after redistribution must be the same:

$$V_{\text{PB}_{\text{start}}} C_{\text{p}} + Q_{\text{D1}_{\text{V}_{\text{cc}}}} = V_{\text{PB}_{\text{end}}} C_{\text{p}} + Q_{\text{D1}_{\text{operation1}}} + Q_{\text{D3}_{\text{operation3}}} \tag{5.108}$$

where

$$\text{operation1} = -V_{\text{PB}_{\text{end}}} \tag{5.109}$$

$$\text{operation3} = V_{\text{PB}_{\text{end}}} + V_{\text{cc}}. \tag{5.110}$$

Therefore substituting (5.102):

$$\begin{aligned} V_{\text{PB}_{\text{start}}} C_{\text{p}} &+ \frac{2k_{\text{cj}} A_{\text{semi}}}{\sqrt{V_{\text{B1}}}} \left(\sqrt{V_0 + V_{\text{cc}}} - \sqrt{V_0} \right) \\ &= V_{\text{PB}_{\text{end}}} C_{\text{p}} \\ &+ \frac{2k_{\text{cj}} A_{\text{semi}}}{\sqrt{V_{\text{B1}}}} \left(\sqrt{V_0 + V_{\text{PB}_{\text{end}}}} - \sqrt{V_0} \right) \\ &+ \frac{2k_{\text{cj}} A_{\text{semi}}}{\sqrt{V_{\text{B3}}}} \left(\sqrt{V_0 - V_{\text{PB}_{\text{end}}} - V_{\text{cc}}} - \sqrt{V_0} \right) \end{aligned} \tag{5.111}$$

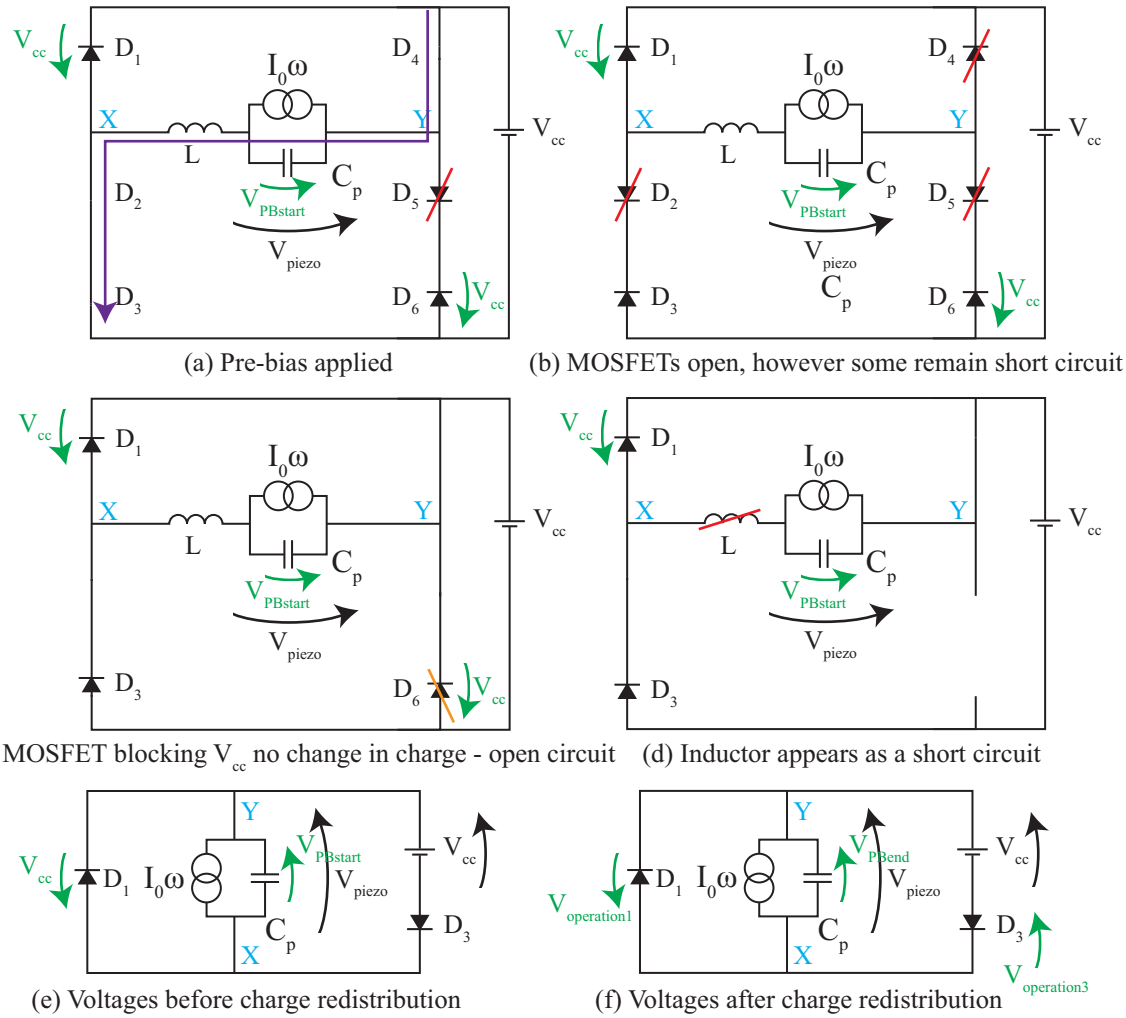


Figure 5.16: Redistribution of charge in H-bridge when switches open after pre-bias phase for case 2.

Then rearranging to make $V_{\mathrm{PB}_{\mathrm{start}}}$ the subject:

$$\begin{aligned} V_{\mathrm{PB}_{\mathrm{start}}} &= V_{\mathrm{PB}_{\mathrm{end}}} \\ &- \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B1}}}}\left(\sqrt{V_0+V_{\mathrm{cc}}}-\sqrt{V_0}\right) \\ &+ \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B1}}}}\left(\sqrt{V_0+V_{\mathrm{PB}_{\mathrm{end}}}}-\sqrt{V_0}\right) \\ &+ \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B3}}}}\left(\sqrt{V_0-V_{\mathrm{PB}_{\mathrm{end}}}-V_{\mathrm{cc}}}-\sqrt{V_0}\right) \end{aligned} \tag{5.112}$$

5.4.2.3 Charge redistribution Case 3

Figure 5.17 shows the derivation of the charge redistribution present in Case 3 ($-V_{\mathrm{cc}} < V_{\mathrm{piezo}} < 0$) by considering the parasitic diodes across the MOSFET switches. Immediately before the switches open, the voltage on C_{p} is V_{PBstart}, the voltage across diodes D_1 and D_6 is V_{cc} and D_5 is a short circuit. MOSFETS 4, 2 and 3 open, however due to the MOSFET parasitic diodes, D_5 and D_2 remain conducting. D_1 will be forced into conduction as well whilst D_3 will be held at V_{cc} so does not effect charge redistribution and hence can be ignored along with the inductor.

Since the total charge before and after redistribution must be the same:

$$V_{\mathrm{PB}_{\mathrm{start}}}C_{\mathrm{p}} + Q_{\mathrm{D6}_{\mathrm{V_{cc}}}} = V_{\mathrm{PB}_{\mathrm{end}}}C_{\mathrm{p}} + Q_{\mathrm{D4}_{\mathrm{operation4}}} + Q_{\mathrm{D6}_{\mathrm{operation6}}} \tag{5.113}$$

where

$$\text{operation4} = V_{\mathrm{PB}_{\mathrm{end}}} \tag{5.114}$$

$$\text{operation6} = -V_{\mathrm{PB}_{\mathrm{end}}} - V_{\mathrm{cc}}. \tag{5.115}$$

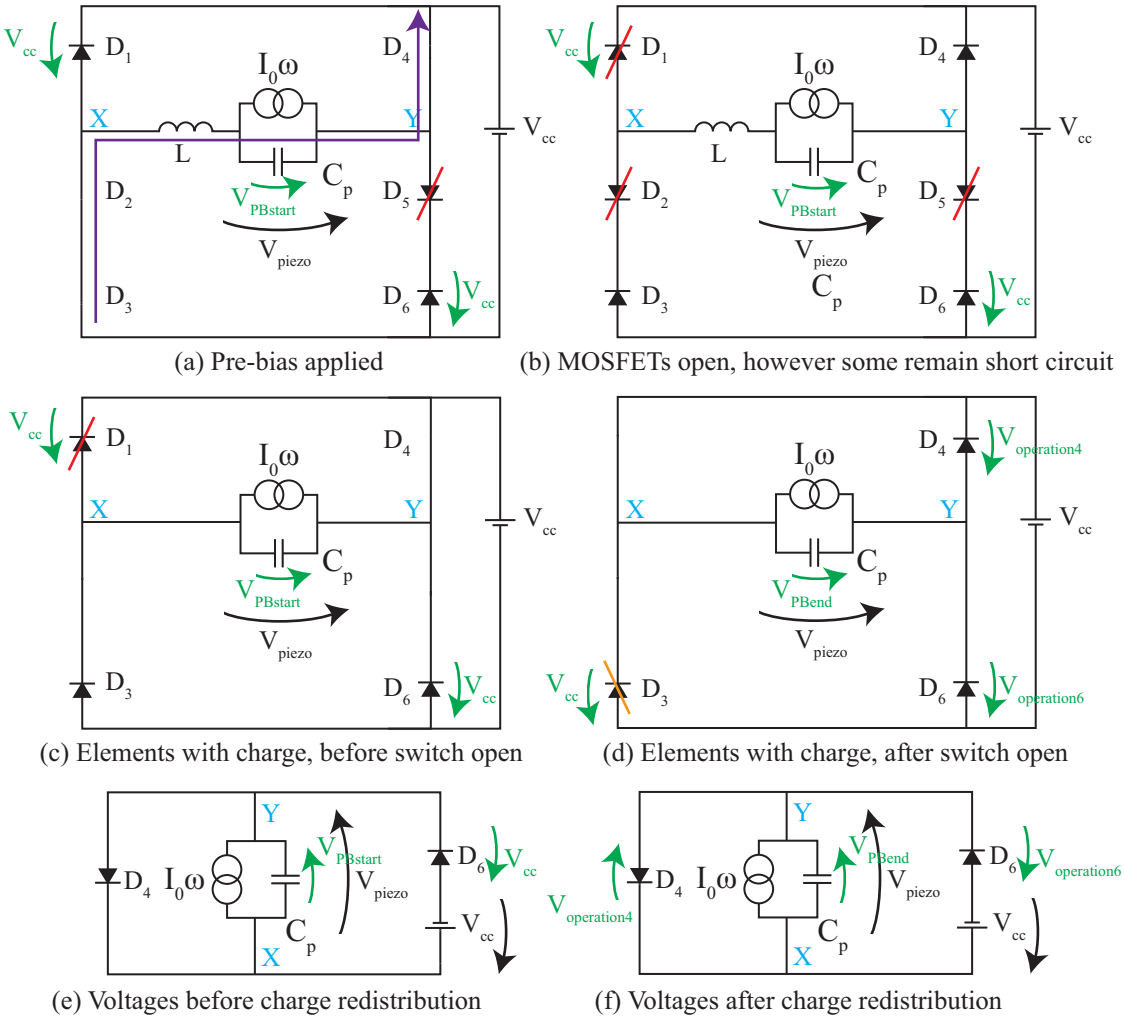


Figure 5.17: Redistribution of charge in H-bridge when switches open after pre-bias phase for case 3.

Therefore substituting into (5.102):

$$\begin{aligned} V_{\mathrm{PB_{start}}}C_{\mathrm{p}} &+ \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B6}}}}\left(\sqrt{V_0+V_{\mathrm{cc}}}-\sqrt{V_0}\right) \\ &= V_{\mathrm{PB_{end}}}C_{\mathrm{p}} \\ &- \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B4}}}}\left(\sqrt{V_0-V_{\mathrm{PB_{end}}}}-\sqrt{V_0}\right) \\ &+ \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{\sqrt{V_{\mathrm{B6}}}}\left(\sqrt{V_0+V_{\mathrm{PB_{end}}}+V_{\mathrm{cc}}}-\sqrt{V_0}\right) \end{aligned} \tag{5.116}$$

Then rearranging to make $V_{\mathrm{PB_{start}}}$ the subject:

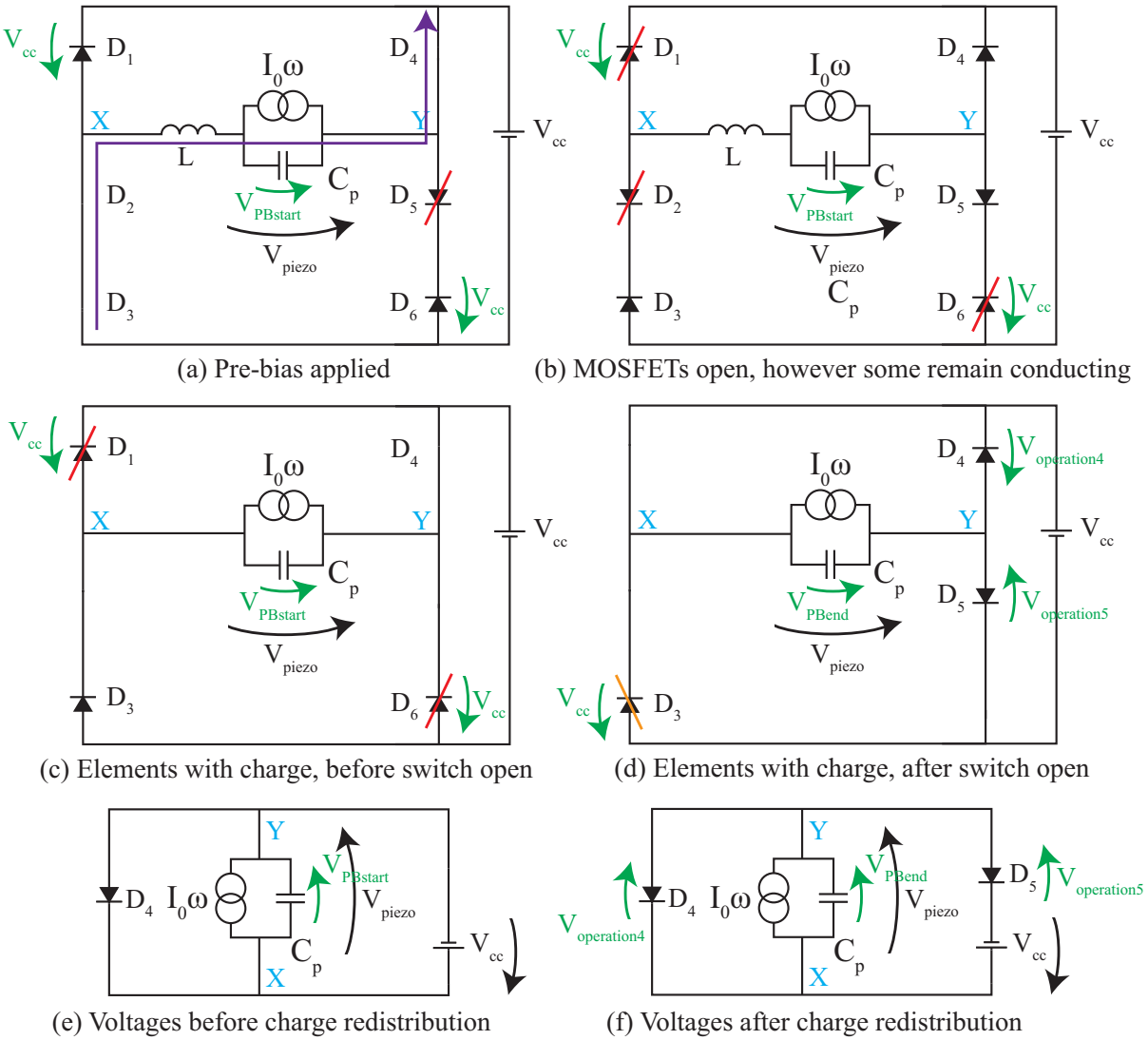
$$\begin{aligned} V_{\mathrm{PB_{start}}} &= V_{\mathrm{PB_{end}}} \\ &- \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B6}}}}\left(\sqrt{V_0+V_{\mathrm{cc}}}-\sqrt{V_0}\right) \\ &- \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B4}}}}\left(\sqrt{V_0-V_{\mathrm{PB_{end}}}}-\sqrt{V_0}\right) \\ &+ \frac{2k_{\mathrm{cj}}A_{\mathrm{semi}}}{C_{\mathrm{p}}\sqrt{V_{\mathrm{B6}}}}\left(\sqrt{V_0+V_{\mathrm{PB_{end}}}+V_{\mathrm{cc}}}-\sqrt{V_0}\right) \end{aligned} \tag{5.117}$$

5.4.2.4 Charge redistribution Case 4

Figure 5.18 shows the derivation of the charge redistribution present in Case 4 ($V_{\mathrm{piezo}} < -V_{\mathrm{cc}}$) by considering the parasitic diodes across the MOSFET switches. Immediately before the switches open, the voltage on C_{p} is V_{PBstart}, the voltage across diodes D_1 and D_6 is V_{cc} and D_5 is a short circuit. MOSFETS 4, 2 and 3 open, however due to the MOSFET parasitic diodes, D_5 and D_2 remain conducting. D_1 will be forced into conduction as well whilst D_3 will be held at V_{cc} so does not effect charge redistribution and hence can be ignored along with the inductor.

The charge on D_1 and D_6 is removed due to the diode being forced into conduction therefore since charge before and after redistribution must be the same:

$$V_{\mathrm{PB_{start}}}C_{\mathrm{p}} = V_{\mathrm{PB_{end}}}C_{\mathrm{p}} + Q_{\mathrm{D4_{operation4}}} + Q_{\mathrm{D5_{operation5}}} \tag{5.118}$$



(a) Pre-bias applied

(b) MOSFETs open, however some remain conducting

(c) Elements with charge, before switch open

(d) Elements with charge, after switch open

(e) Voltages before charge redistribution

(f) Voltages after charge redistribution

Figure 5.18: Redistribution of charge in H-bridge when switches open after pre-bias phase for case 4.

where

$$\text{operation4} = V_{\text{PB}_{\text{end}}} \tag{5.119}$$

$$\text{operation5} = V_{\text{PB}_{\text{end}}} + V_{\text{cc}}. \tag{5.120}$$

Therefore substituting (5.102):

$$\begin{aligned} V_{\text{PB}_{\text{start}}} C_{\text{p}} &= V_{\text{PB}_{\text{end}}} C_{\text{p}} \\ &- \frac{2k_{\text{cj}} A_{\text{semi}}}{\sqrt{V_{\text{B4}}}} \left(\sqrt{V_0 - V_{\text{PB}_{\text{end}}}} - \sqrt{V_0} \right) \\ &- \frac{2k_{\text{cj}} A_{\text{semi}}}{\sqrt{V_{\text{B5}}}} \left(\sqrt{V_0 - V_{\text{PB}_{\text{end}}} - V_{\text{cc}}} - \sqrt{V_0} \right) \end{aligned} \tag{5.121}$$

Then rearranging to make $V_{\text{PB}_{\text{start}}}$ the subject:

$$\begin{aligned} V_{\text{PB}_{\text{start}}} &= V_{\text{PB}_{\text{end}}} \\ &- \frac{2k_{\text{cj}} A_{\text{semi}}}{C_{\text{p}} \sqrt{V_{\text{B4}}}} \left(\sqrt{V_0 - V_{\text{PB}_{\text{end}}}} - \sqrt{V_0} \right) \\ &- \frac{2k_{\text{cj}} A_{\text{semi}}}{C_{\text{p}} \sqrt{V_{\text{B5}}}} \left(\sqrt{V_0 - V_{\text{PB}_{\text{end}}} - V_{\text{cc}}} - \sqrt{V_0} \right) \end{aligned} \tag{5.122}$$

5.4.3 Conduction losses

Conduction losses, $E_{\text{R,loss}}$, occur when the piezoelectric transducer is either pre-bias or discharged as the current must flow though the inductor and MOSFETs. The inductor resistance (R_{L}) and the on-state drain-source resistance of the MOSFETs (R_{mos}) are summed together and multiplied by the square of the inductor current (i_{L}) and the on-state conduction time (Δt).

$$E_{\text{R,loss}} = {i_{\text{L}}}^2 (R_{\text{mos}} + R_{\text{L}}) \Delta t \tag{5.123}$$

5.5 Energy equations

The energy generated and the efficiencies can now be calculated from the parameters described earlier in the chapter. The mechanical coupling energy generated, E_{coup}, in the intermediate storage capacitor, C_{int}, (Figure 5.4) due to mechanical excitation of the harvester is given by

$$E_{\text{coup}} = \frac{1}{2} C_{\text{p}} \left((V_{\text{PBend}} + 2V_{\text{po}})^2 - {V_{\text{PBend}}}^2 \right). \tag{5.124}$$

where C_{p} is piezoelectric capacitance, V_{PBend} is the required pre-bias voltage and V_{po} is the induced voltage across the transducer when deflected.

The pre-bias energy, E_{PB}, used to pre-bias the piezoelectric capacitor, depends on whether the FRTZ method has been implemented. If the FRTZ method has been used then it is the energy required to increase the voltage on C_{p} from 0 V to V_{PBstart} using a voltage source V_{cc}:

$$E_{\text{PB}} = C_{\text{p}} V_{\text{cc}} V_{\text{PBstart}} \tag{5.125}$$

else the remaining voltage on the piezoelectric capacitance, V_{rem}, must be overcome,

$$E_{\text{PB}} = C_{\text{p}} V_{\text{cc}} (V_{\text{PBstart}} + V_{\text{rem}}) \tag{5.126}$$

where V_{PBstart} is the pre-bias voltage before charge redistribution.

The energy generated in discharging the piezoelectric capacitor from V_{end} to V_{rem} is

$$E_{\text{extract}} = C_{\text{p}} V_{\text{cc}} ((V_{\text{PBend}} + 2V_{\text{po}}) - V_{\text{rem}}) \tag{5.127}$$

such that the energy harvested, as in energy put back into the power supply per half cycle is calculated as

$$E_{\text{harv}} = E_{\text{extract}} - E_{\text{PB}} - E_{i_{6\text{l}},\text{loss}} \tag{5.128}$$

where $E_{i_{61},\text{loss}}$ is the n-type MOSFET leakage current (5.96).

The final output energy per half mechanical cycle, E_{out}, is equal to the E_{harv} minus the losses due to the buck converter described in Section 5.6.

$$E_{\text{out}} = E_{\text{harv}} - E_{\text{buck,loss}} \tag{5.129}$$

Multiplying (5.129) by twice the mechanical frequency, f_0, calculates the power output, P_{out}.

$$P_{\text{out}} = 2f_0 E_{\text{out}} \tag{5.130}$$

Having obtained expressions for energy generated by the piezoelectric transducer, energy required for pre-biasing, and energy losses through all parts of the system, it is now possible to calculate the system effectiveness. The maximum possible theoretical power available to be harvested [36] is given by

$$P_{\text{max}} = \frac{1}{2}{Y_0}^2\omega^3 m\frac{Z_{\text{l}}}{Y_0} = \frac{1}{16}\rho_{\text{mass}}A_{\text{input}}\omega_{\text{input}}S^4 \tag{5.131}$$

where the following substitutions were used:

$$A_{\text{input}} = Y_0\omega^2, \quad m = \rho_{\text{mass}}\frac{S}{2}S^2, \quad Z_{\text{l}} = \frac{S}{4}. \tag{5.132}$$

The system effectiveness is then found by dividing P_{out} by the maximum theoretically available power

$$\eta_{\text{system}} = \frac{P_{\text{out}}}{P_{\text{max}}} = \frac{E_{\text{out}}}{E_{\text{max}}} = \eta_{\text{coup}} \times \eta_{\text{extraction}} \times \eta_{\text{conv}}. \tag{5.133}$$

5.6 Energy Storage losses

The voltage on the intermediate capacitor, C_{int}, is kept constant by periodically transferring energy to the battery through a buck converter circuit. The voltage and frequency have been

selected as 1.5 V and every mechanical cycle respectively. Note that if the required $V_{\rm cc}$ is less than the desired battery voltage, a boost circuit with a similar derivation of the losses can be used.

The energy losses in the buck converter (Figure 5.4) occur due to current leakage $E_{i_{\rm buck},\rm loss}$, charge sharing $E_{C_{\rm buck},\rm loss}$ and conduction losses $E_{R_{\rm buck},\rm loss}$. In order to operate the SSPB circuit in steady state operation, only the amount of charge from $C_{\rm int}$ should be transferred into the battery as was put onto $C_{\rm int}$ during that mechanical cycle, a quantity given by

$$Q_{\rm req} = \frac{E_{\rm harv}}{V_{\rm cc}}. \tag{5.134}$$

The required peak buck inductor current therefore required for steady state operation is

$$I_{\rm req} = \left(\frac{2E_{\rm harv}}{L_{\rm buck}}\right)^{\frac{1}{2}}, \tag{5.135}$$

where $L_{\rm buck}$ is the value of the inductor in the buck converter circuit. The inductor's characteristics can be found using the same method as the SSPB circuit described in Section 5.3.

$$R_{L_{\rm buck}} = c\frac{k_{\rm epi,N}{V_{\rm B,LoN}}^2}{A_{\rm semi}} \tag{5.136}$$

$$L_{\rm buck} = (K_{\rm L}V_{\rm L}R_{L_{\rm buck}})^{\frac{1}{2}}, \tag{5.137}$$

where $R_{L_{\rm buck}}$ is the resistance in the inductor of the buck converter circuit [3, 23].

The buck circuit is operated in synchronous mode so there are four sources of losses. First, since one MOSFET is always off, a constant leakage current exists that is given by twice the value of the expression in equation (5.96)

$$E_{i_{\rm buck},\rm loss} = \frac{2i_{6\rm l}V_{\rm cc}}{2f_1}. \tag{5.138}$$

Second, one MOSFET is always on, so the charge sharing loss on the blocking junctions gives:

$$E_{C_{\text{buck}},\text{loss}} = 4k_{\text{cj}}A_{\text{semi}}V_{\text{cc}}, \tag{5.139}$$

which comes from [111]. Third and fourth, there are conduction losses in the inductor and semiconductor devices during charging and freewheeling to account for. To calculate these losses, it must first be determined at what time the buck converter switches from discharging C_{int} charging the battery to freewheeling, t_{switch}, and at what time the current falls to zero during freewheeling, $t_{\text{L=0}}$. The differential equation is first solved for current through the inductor during C_{int} discharging phase, given by

$$\frac{di_{\text{ind,ch}}}{dt} = \frac{V_{\text{cc}} - V_{\text{batt}}}{L_{\text{buck}}} - \frac{i_{\text{ind,ch}}R_{\text{tot}_{\text{buck}}}}{L_{\text{buck}}}, \tag{5.140}$$

$$R_{\text{tot}_{\text{buck}}} = (1+c)\frac{k_{\text{epi,N}}{V_{\text{B,LoN}}}^2}{A_{\text{semi}}} \tag{5.141}$$

where $R_{\text{tot}_{\text{buck}}}$ is the total resistance in the buck converter circuit.

This gives the values for current into the inductor over time, $i_{\text{ind,ch}}$, which are then compared with the current required for steady state operation, I_{req}. The time at which these currents are equal is the time when the switches flip to begin the freewheeling phase. A differential equation for the inductor current during the freewheeling phase is then solved

$$\frac{di_{\text{ind,fw}}}{dt} = \frac{-V_{\text{batt}} - i_{\text{ind,fw}}R_{\text{tot}_{\text{buck}}}}{L_{\text{buck}}} \tag{5.142}$$

and the time at which the current falls to zero in the inductor is determined by observing when the current $i_{\text{ind,fw}} = 0$. The total resistive losses are thus calculated by integrating these two

time periods:

$$\begin{aligned} E_{R_{\text{buck}},\text{loss}} &= \int_0^{t_{\text{switch}}} {i_{\text{ind,ch}}}^2 R_{\text{tot}_{\text{buck}}} dt \\ &+ \int_{t_{\text{switch}}}^{t_{\text{L=0}}} {i_{\text{ind,fw}}}^2 R_{\text{tot}_{\text{buck}}} dt. \end{aligned} \tag{5.143}$$

Thus the losses due to the buck converter are:

$$E_{\text{buck,loss}} = E_{i_{\text{buck}},\text{loss}} + E_{C_{\text{buck}},\text{loss}} + E_{R_{\text{buck}},\text{loss}}. \tag{5.144}$$

During these calculations, checks are done to ensure that $V_{\text{cc}} > V_{\text{batt}}$, that $E_{\text{harv}} > 0$, and that the intermediate capacitor was discharged enough to maintain steady state operation. Subtracting the buck converter energy losses from E_{harv} gives the net energy and power generated according to

$$E_{\text{out}} = E_{\text{harv}} - E_{\text{buck,loss}} \tag{5.145}$$

$$E_{\text{out}} = E_{\text{harv}} - E_{i_{\text{buck}},\text{loss}} - E_{C_{\text{buck}},\text{loss}} - E_{R_{\text{buck}},\text{loss}} \tag{5.146}$$

$$P_{\text{out}} = 2 f_0 E_{\text{out}}. \tag{5.147}$$

5.7 Results

The model was run in MATLAB 2015a and verified with OrCAD PSpice v16.3 for both MEMS and MESO scale devices. The optimisation swept the size between 1 to 15 mm and the acceleration between 0.01 to 100 ms^{-2}. A 15 x 15 matrix of size and acceleration values were used. The inversion factor, γ, was swept between 0.5 to 0.99 as values under 0.5 result in a very poor system performance and above 0.99 are not practical. The frequency was tested at 1 Hz, 10 Hz, 100 Hz and 1 kHz as these represent the full limits of the range that occur for ambient vibration sources [9, 113].

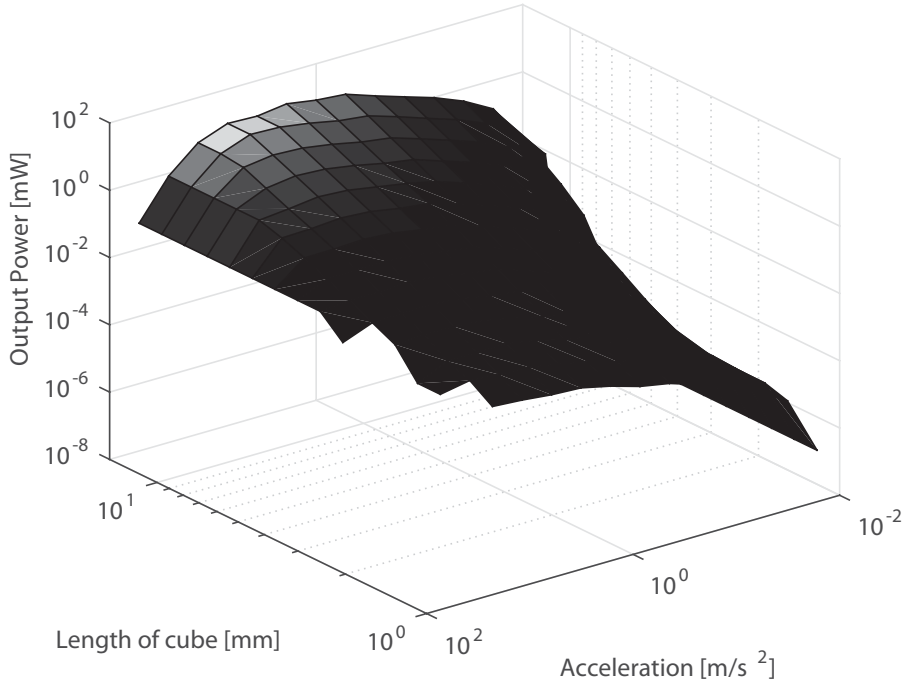


Figure 5.19: Power output at 100 Hz [106].

5.7.1 MEMS scale devices

The plots in Figures 5.19, 5.20, 5.21, 5.22, and 5.23 show the power output, system effectiveness (output energy/available energy), coupling effectiveness (transducer generated energy/available energy), extraction efficiency (harvested energy/transducer generated energy), and conversion efficiency (output energy/harvested energy), respectively, at 100 Hz input frequency with a gold proof mass.

Figures 5.24, 5.25, 5.26, 5.27, 5.28 and 5.29 show power and system effectiveness of the same system operating at 1 Hz, 10 Hz and 1000 Hz. It is clear that at very low or very high frequencies, the range of box size and accelerations at which the system is functional is greatly diminished. In the 1 Hz case, there is only a limited range of large box sizes and small accelerations which are viable due to two reasons. First, for small values of S, no combination of beam length and thickness exists that can satisfy the requirement that the transducer resonant frequency match the low driving frequency. This prevents any functional systems until S is greater than

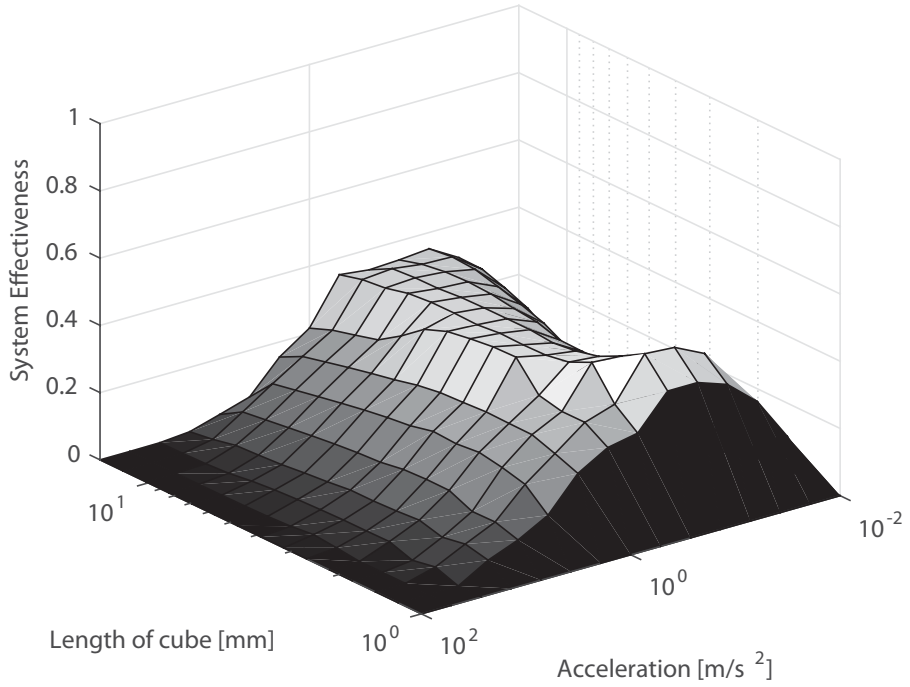


Figure 5.20: System effectiveness at 100 Hz [106].

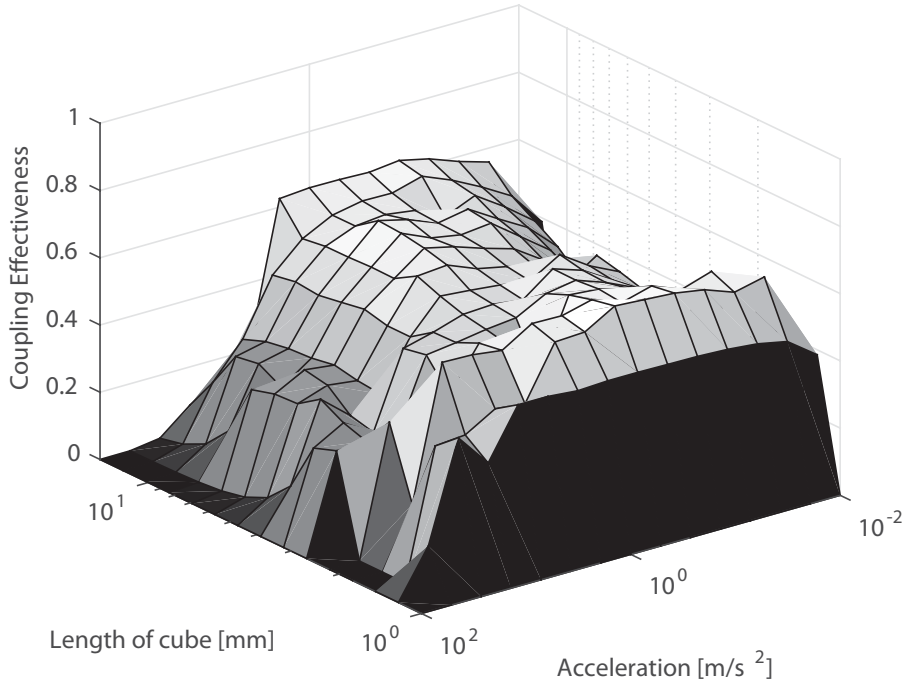


Figure 5.21: Coupling effectiveness at 100 Hz [106].

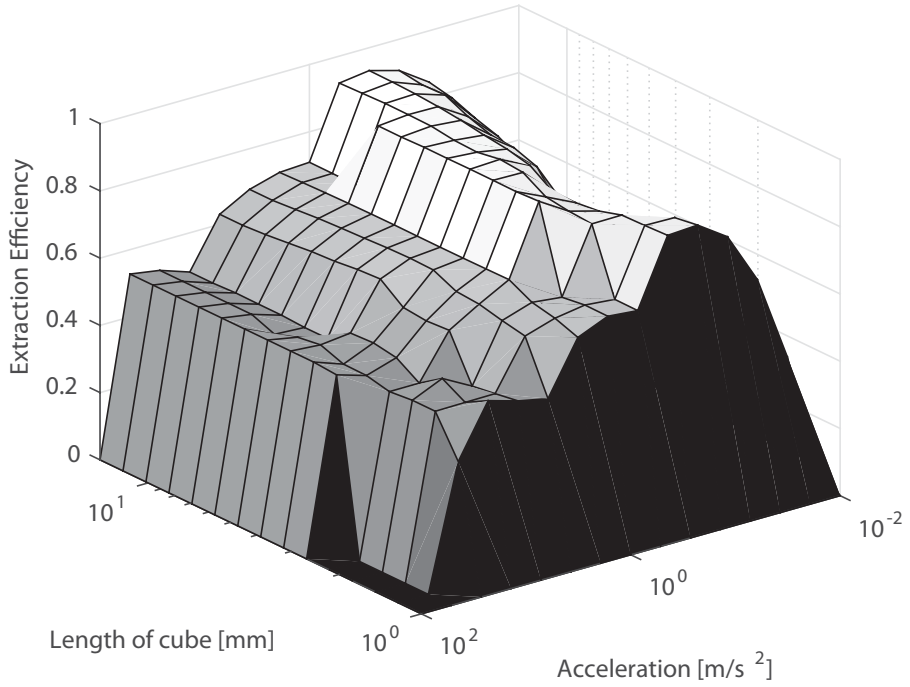


Figure 5.22: Extraction efficiency at 100 Hz [106].

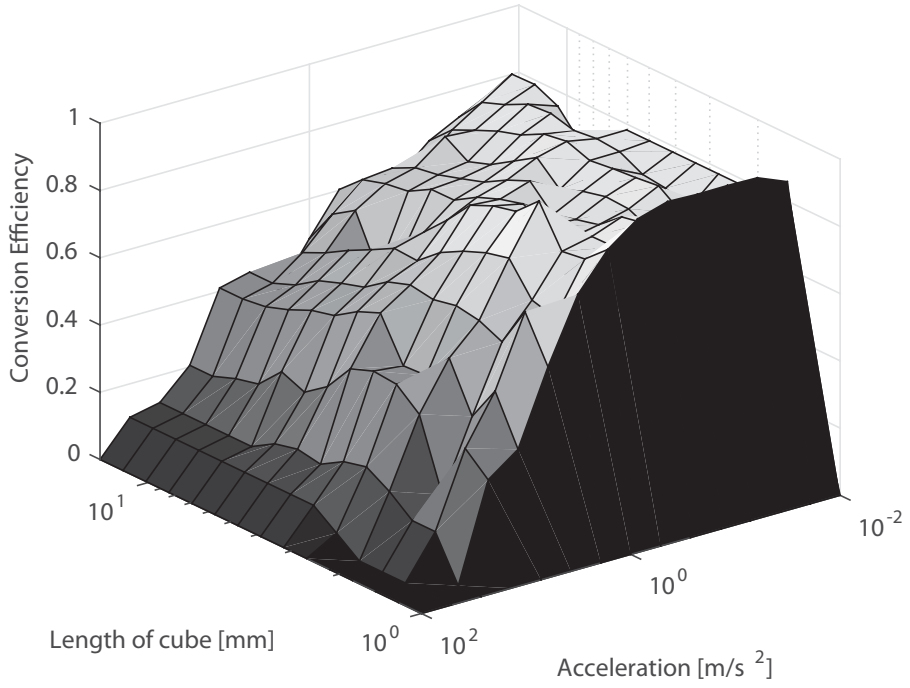


Figure 5.23: Conversion efficiency at 100 Hz [106].

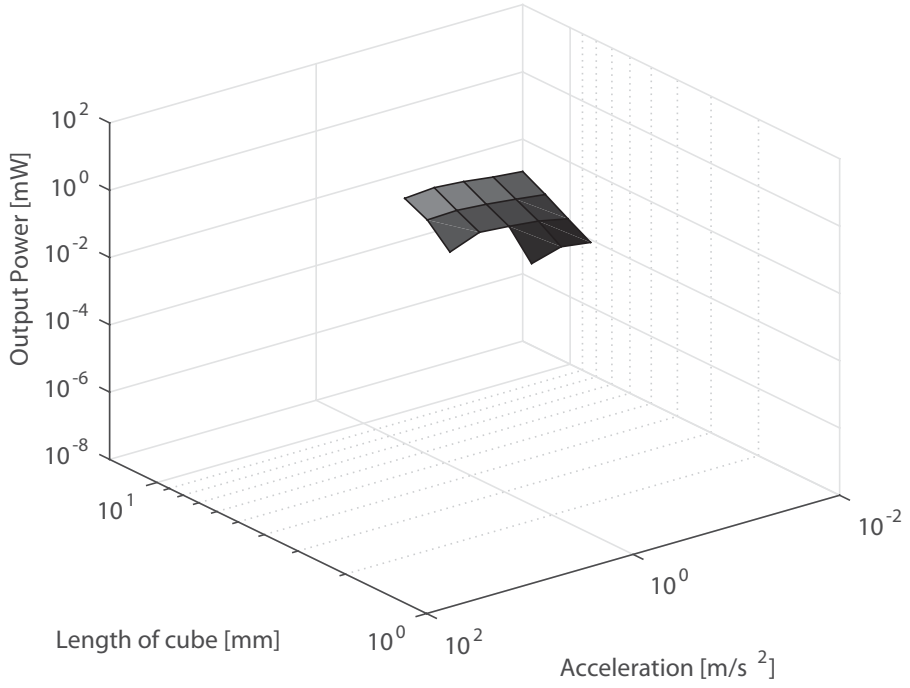


Figure 5.24: Power output at 1 Hz [106].

approximately 1 cm. Second, at accelerations above a certain threshold, the system is unable to provide enough electrical damping to prevent the harvester from hitting the end-stops, which is not allowed in this model due to the damage this would cause. This is due in part to the large mass required at low frequencies requiring a very large damping force. Figures for coupling effectiveness, extraction efficiency, and conversion efficiency for the 1 Hz, 10 Hz and 1000 Hz case can be found in Appendix 10.

In the 10 Hz case, more beam length and thickness combinations exist so more viable solutions are available, however at high accelerations, the required electrical damping is still unachievable limiting power generation.

The 1000 Hz case also has limited functionality for two main reasons. At low accelerations, a net loss in power occurs due to the losses in the SSPB and buck circuit caused by device leakage, capacitive sharing and conduction. As the level of acceleration increases, the extracted energy increases, overcoming these losses, and so power can be extracted. A maximum length

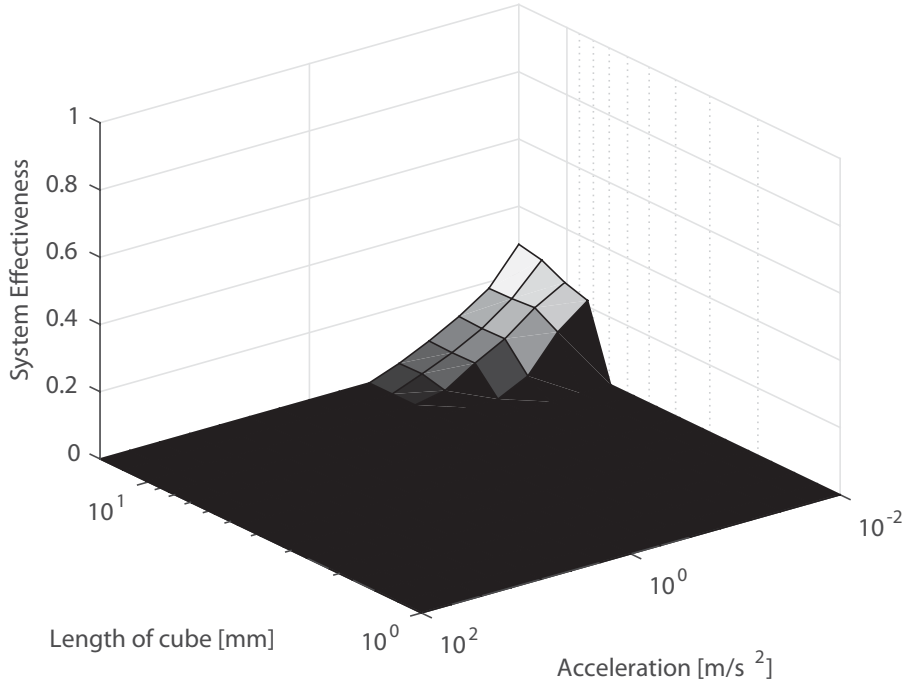


Figure 5.25: System effectiveness at 1 Hz [106].

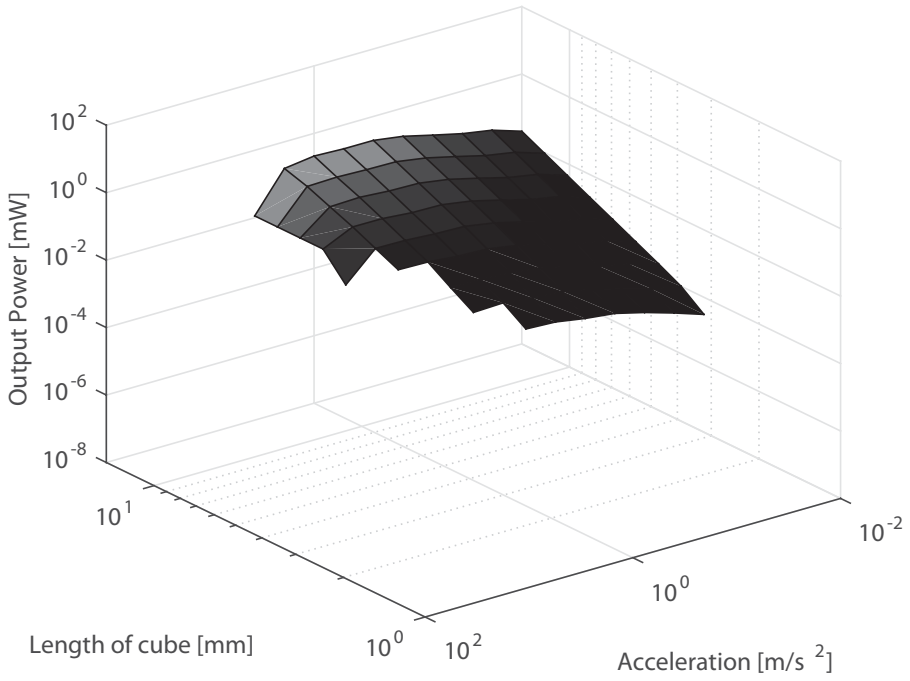


Figure 5.26: Power output at 10 Hz [106].

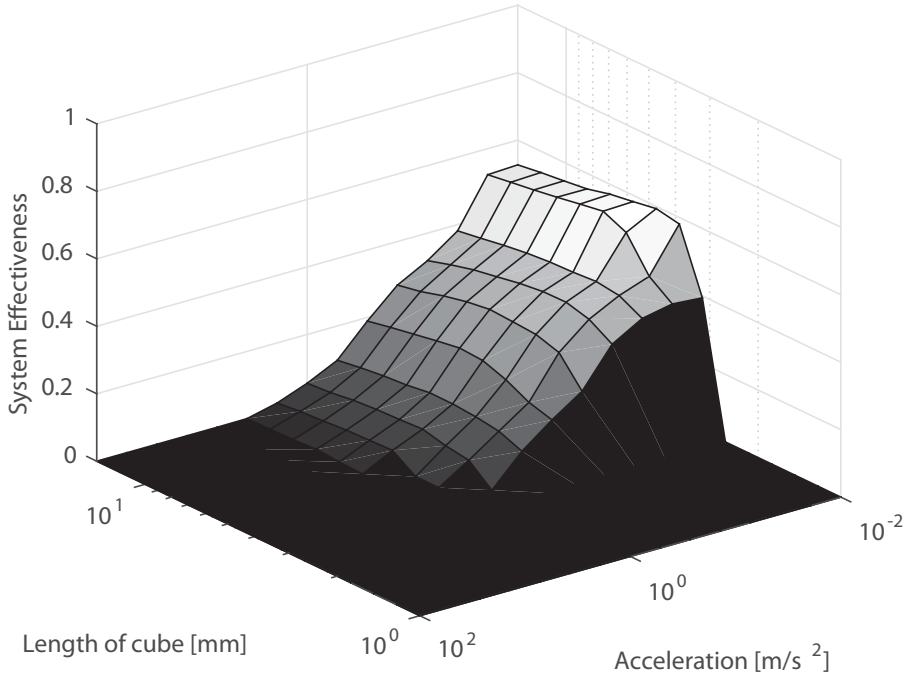


Figure 5.27: System effectiveness at 10 Hz [106].

of S also exists due to no combination of beam length and thickness existing to resonate at the high driving frequency. However unlike in the 1 Hz case, the beam can be assumed shorter than S and therefore will resonate, but the system effectiveness is severely reduced due to the underutilisation of the volume.

The limitations discussed in the preceding paragraphs apply to the limits in operating regime for the 100 Hz case as well, but to a far lesser extent. One other factor relating to the reason for the drop off in system effectiveness and power generation at large accelerations at 100 Hz is that the limit for dielectric breakdown voltage is surpassed, meaning that the displacement of the mass must be reduced to decrease the piezoelectric induced voltage and the required pre-bias voltage.

The optimization was run using gold for the mass material because of its high density (19320 kg m^{-3}) and compatibility with MEMS processing. However, the results with a silicon proof mass at 100 Hz are shown in Appendix 10. The results are compared with gold in

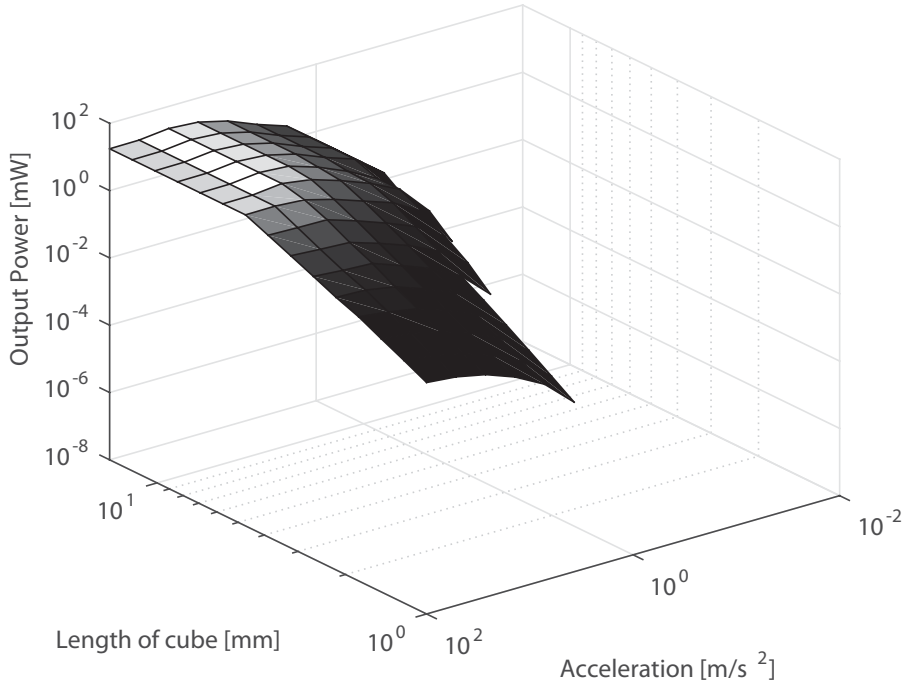


Figure 5.28: Power output at 1000 Hz [106].

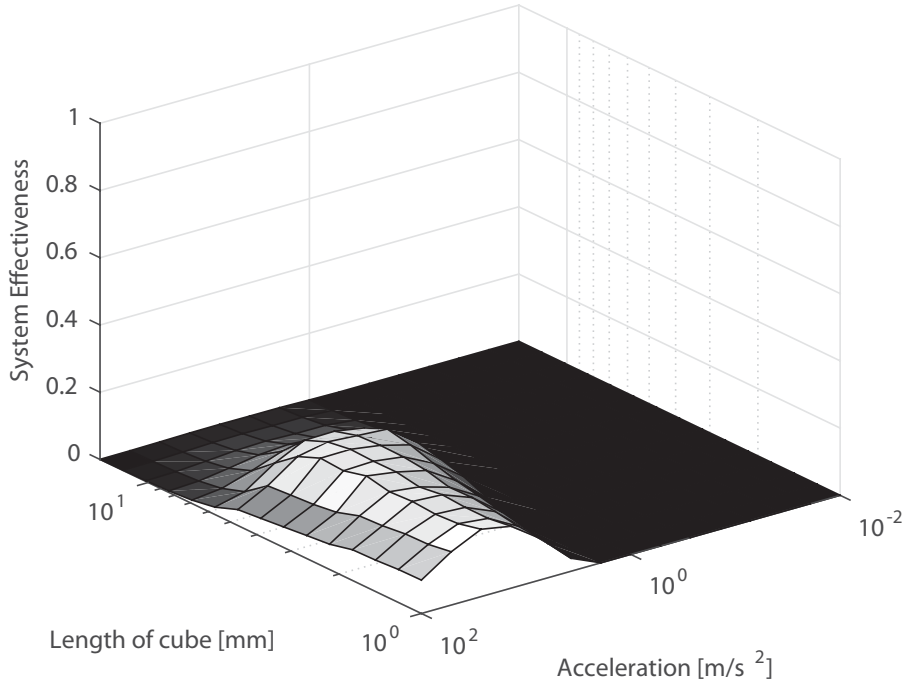


Figure 5.29: System effectiveness at 1000 Hz [106].

Table 5.3. If cost is a concern, and silicon is not dense enough to get the desired performance, tungsten (19300 kg m^{-3}) or nickel (8900 kg m^{-3}) may be used instead of gold. As expected, power output from a transducer with a gold proof mass is higher than that with a silicon proof mass. However, system effectiveness from the silicon mass is higher than the gold, because a greater pre-bias voltage is required to damp the motion of the heavier proof mass within the confined volume, and that requires a larger supply voltage and more energy for the pre-biasing, undermining system effectiveness.

Table 5.3: Optimal system parameters at 100 Hz for systems with a silicon versus gold proof mass. Values are shown for both maximum η_{sys} and maximum P to illustrate their difference [106].

			Silicon Mass		Gold Mass	
		unit	max η_{sys}	max P	max η_{sys}	max P
System Effectiveness	η_{sys}	%	56	12	48	16
Output Power	P	mW	0.0003	7.4	0.46	11.5
Beam Length	L_b	mm	0.25	8.15	0.13	2.12
Silicon Layer Thickness	t_s	μm	1	121	1	200
Electrical Q-factor	Q		23.58	23.58	12.41	23.58
Buck Inductance	L_{buck}	nH	15	334	19	847
Semiconductor Area	A_{semi}	m^2	1.2e-9	5.2e-6	1.2e-9	4.1e-6
Volume Side Length	S	mm	2.2	15.0	15.0	15.0
Acceleration	A_{input}	ms^{-2}	0.27	13.90	0.27	1.93

The optimal design parameters at 100 Hz for the beam thickness, beam length, inductance, semiconductor cross sectional area and Q factor are shown in Figures 5.30, 5.31, 5.32, 5.33 and 5.34. It can be seen that the beam thickness increases with harvester volume to achieve the required resonant frequency. Beam length also increases with volume to maximise the piezoelectric layer area and thus maximise power. As the applied acceleration increases, the maximum voltage across the piezoelectric material (pre-bias voltage plus induced voltage) increases, thus the MOSFETs' semiconductor area increases to block the voltage.

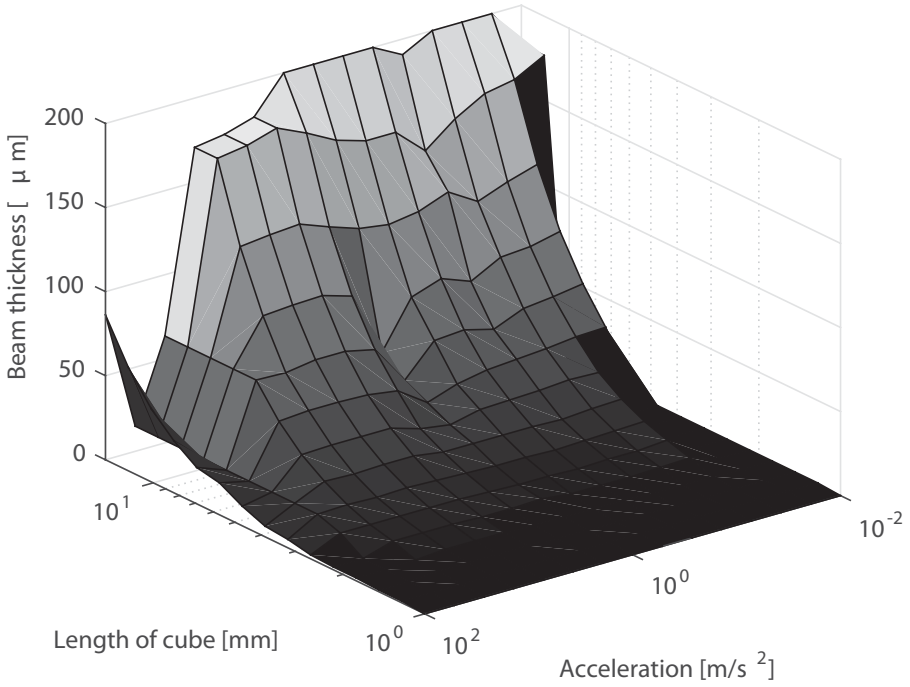


Figure 5.30: Beam thickness at 100 Hz.

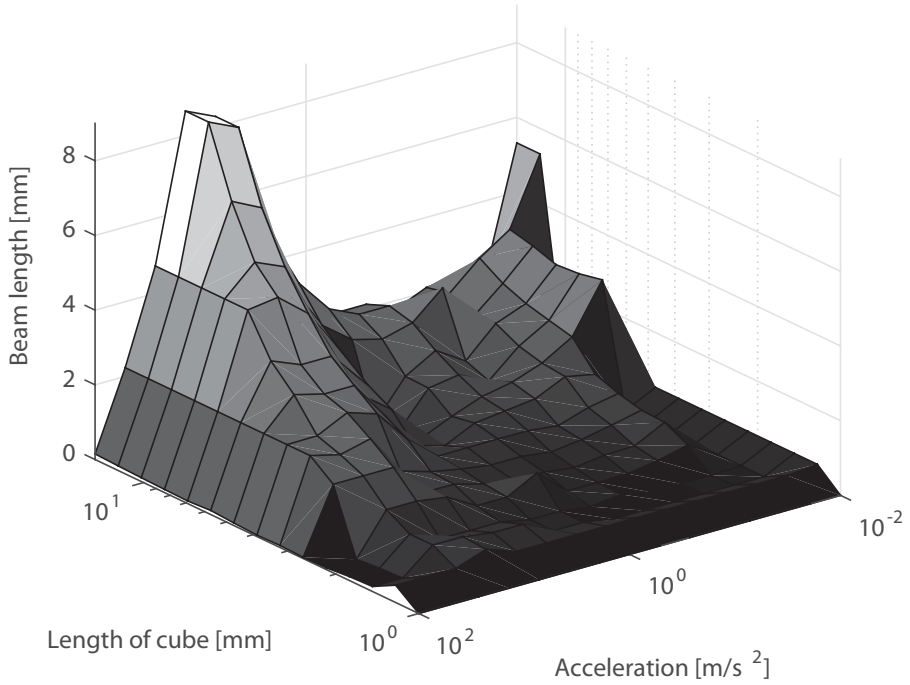


Figure 5.31: Beam length at 100 Hz.

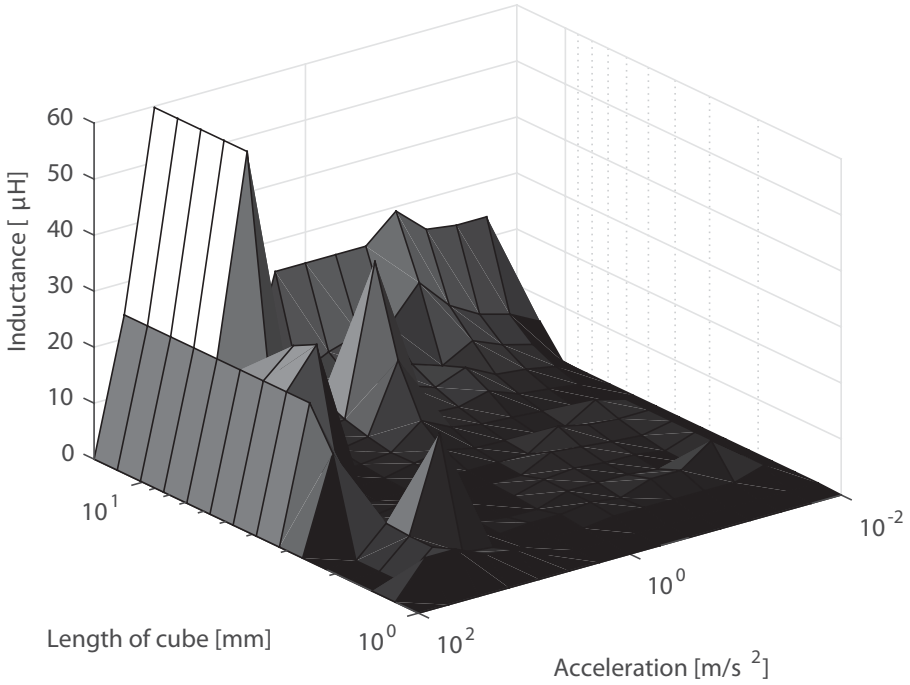


Figure 5.32: Inductance at 100 Hz.

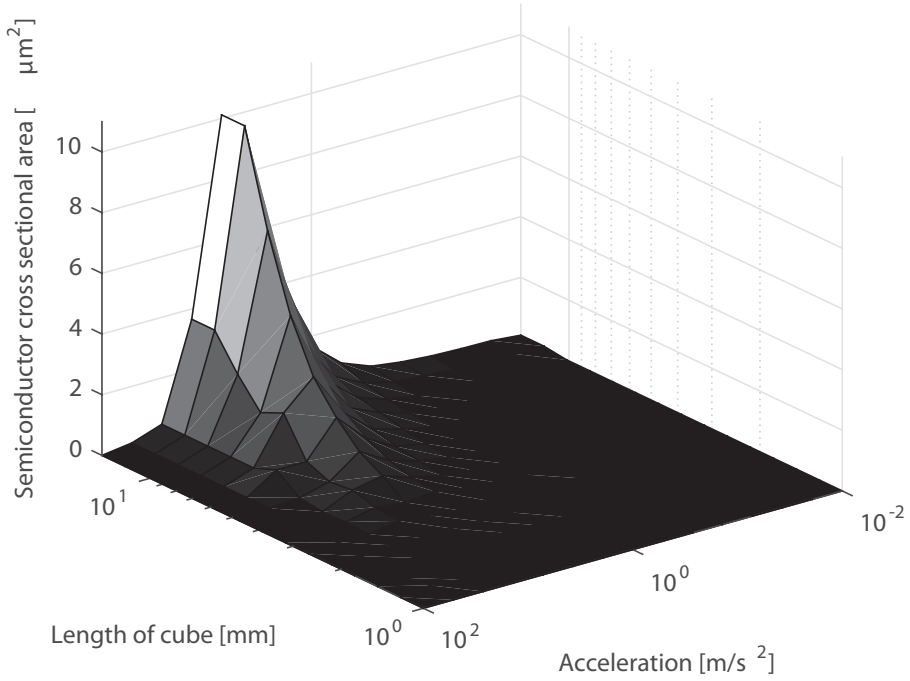


Figure 5.33: Semiconductor cross sectional area at 100 Hz.

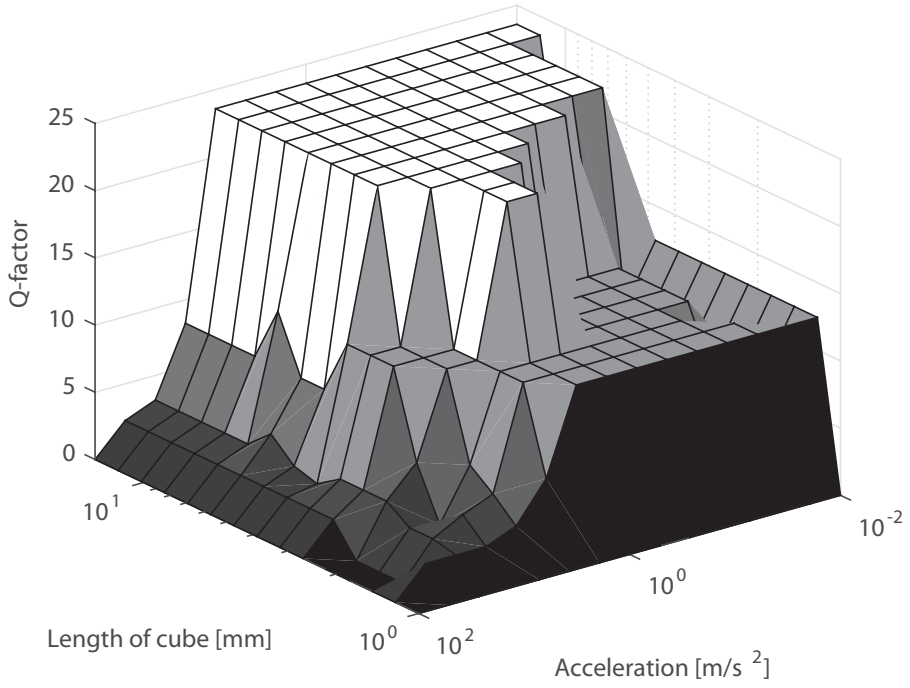


Figure 5.34: Q-factor at 100 Hz.

5.7.2 MESO devices

The model was run using MESO scale piezoelectric properties for 1 Hz, 10 Hz, 100 Hz and 1 kHz, however solutions for only the 1 kHz case were found (Figures 5.36 and 5.35). This was due to the much thicker piezoelectric layer on the beam, increasing the stiffness of the beam and the proof mass being too small to reduce the resonant frequency. The power output however is higher for small to medium size accelerations in the MESO scale case thus a compromise must be struck between device size and power generation.

Figure 5.37 is a comparison of the resonant frequencies achievable using MEMS and MESO scale piezoelectric material when the available volume's side length constraint is increased to 50 mm. It can be seen that no solutions can be found at 100 Hz with MESO devices until the volume side length exceeds 16.25 mm.

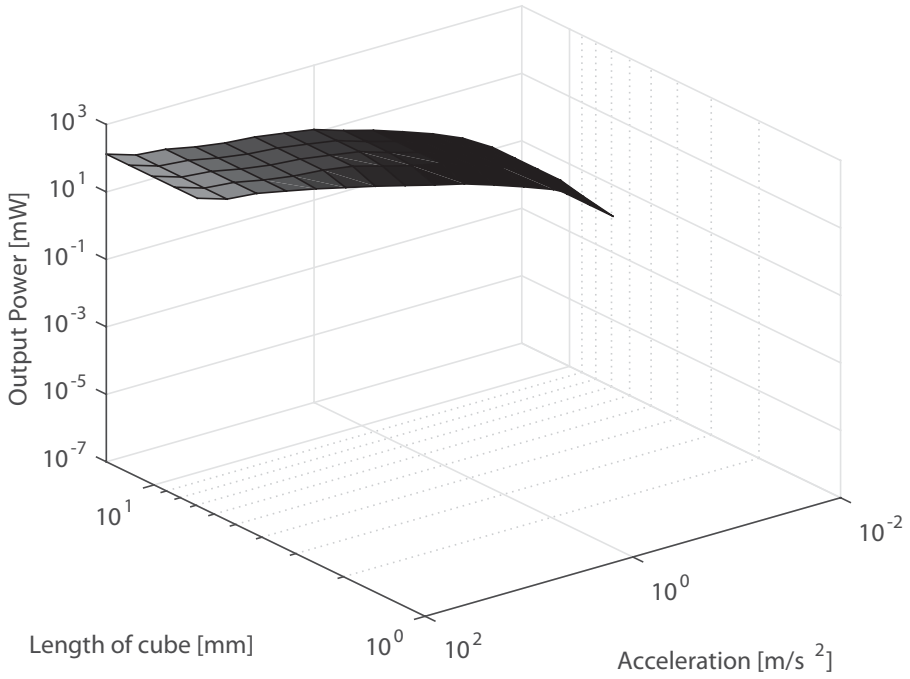


Figure 5.35: Power output at 1000 Hz using MESO scale materials.

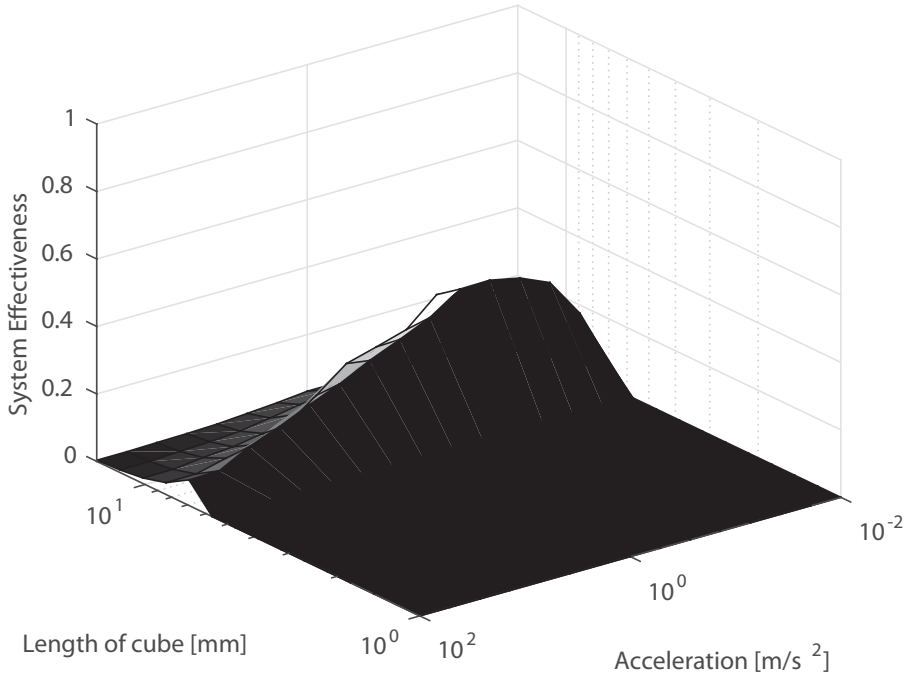


Figure 5.36: System effectiveness at 1000 Hz using MESO scale materials.

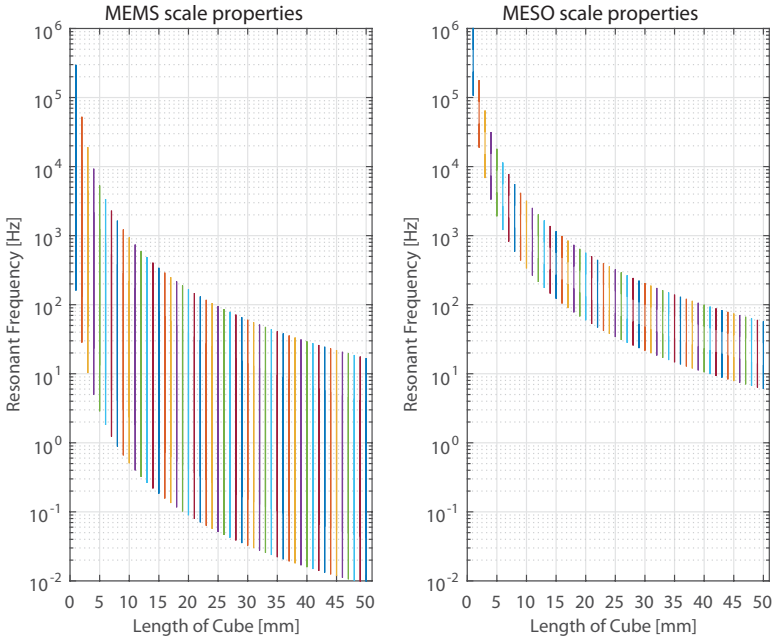


Figure 5.37: Comparison of resonant frequencies using MEMS and MESO scale piezoelectric properties.

5.7.3 Comparison with an electrostatic energy harvesting system

The parametrised results from the piezoelectric energy harvesting system model were compared with the results from the electrostatic energy harvesting system model presented in [23] to answer the often asked, and until now inadequately answered, question of which MEMS compatible transducer type achieves the best power density in an energy harvesting system [96]. For the electrostatic system model, the constant voltage implementation was chosen as the constant charge configuration was shown to have worse performance [23]. For details on the constant voltage model used see [23].

The comparison of the two systems was performed at 100 Hz with the volume constrained between 1 mm and 15 mm and the acceleration varied between 0.01 ms^{-2} to 100 ms^{-2} using a gold proof mass. MEMS scale material properties were used so the semiconductor device breakdown voltage was assumed to be 1.5 kV [114] and the piezoelectric dielectric breakdown

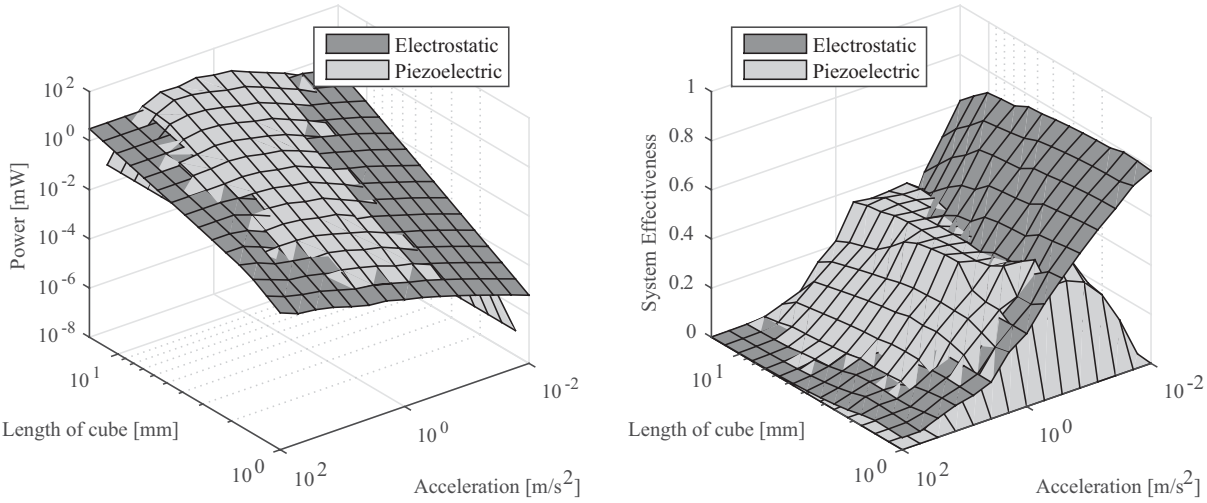


Figure 5.38: Comparison of the power output and system effectiveness between electrostatic and piezoelectric MEMS scale energy harvesting systems [107].

voltage was assumed to be 750 V [115].

Figure 5.38 compares the power output and system effectiveness for both energy harvesting systems. It can be clearly seen that the electrostatic system is preferred at low accelerations over the piezoelectric system as the energy losses (due to power conditioning and buck converter circuits) in the piezoelectric devices at low power levels severely reduces the output power. As mechanical acceleration is increased, the electrostatic system requires increasingly high biasing voltages, causing the semiconductor device on-state resistance to increase in order to block the higher voltage, resulting in increased conduction losses and a preference for the piezoelectric system. However at very high accelerations the power output of the piezoelectric system is severely limited as the dielectric breakdown voltage in MEMS scale devices forces the mass displacement to be decreased thus not utilising the maximum deflection possible, therefore the electrostatic devices are preferred in this case.

5.8 Conclusion

A parametrised model was developed to investigate the full system effectiveness of a piezoelectric transducer coupled to a SSPB circuit, a power conditioning circuit, and a battery, to maximise power generation within a specific volume. A parameter sweep over system geometric dimensions and circuit inversion coefficient was conducted to find the optimal system parameters for a given input size, operating frequency, and input acceleration. Subsequently, the size and acceleration were swept while holding frequency fixed at 1, 10, 100, and 1000 Hz to find the power output and effectiveness of the energy harvesting system over a range of operating conditions.

For MEMS scale devices, the operating envelope of the system has limits related to box size, S, input acceleration, A_{input}, and input frequency, ω_{input}. At low values of A_{input}, the energy losses in the system result in a negative net energy gain. At high values of A_{input} the system becomes non-functional when it is not able to provide a large enough pre-bias voltage to prevent the mass from crashing into the box limits, which would violate the requirements of the model. Alternatively, the system can become less effective when the mass displacement is constrained to reduce the induced voltage and pre-bias voltage, to ensure the total pre-bias and induce voltage does not exceed the dielectric breakdown voltage. Thus, larger A_{input} is not always better for system performance as might have been expected. The system operating envelope is also limited by the fact that some combinations of ω_{input} and S have no geometric solutions that meet the model requirement of the beam resonant frequency matching the input frequency. This is due to the fact that the resonant frequency is inversely proportional to harvester length and proof mass, which are defined with respect to S.

Piezoelectric devices made using MESO scale techniques were shown to have no geometric solutions at low frequencies due to the thickness of the beam. However at high frequencies, the MESO scale devices generated several times as much power as MEMS scale devices as dielectric breakdown voltage is much higher, thus the optimal damping force can be implemented.

These limitations of piezoelectric systems lead to the finding that, generally, electrostatic

harvesting systems produce more power from a 100 Hz driving frequency when acceleration or device box size are low, while piezoelectric systems generate more power when acceleration is relatively high or device size is large. However at very high accelerations, piezoelectric MEMS scale devices are sub-optimal as the biasing voltage required to dampen the transducer exceeds the dielectric breakdown voltage. It is interesting to note that, unlike electrostatic harvester systems, the resonator and transducer elements are the same structure for piezoelectric systems, thus limiting geometric design choices.

5.9 Summary

In this chapter a complete system model of a piezoelectric energy harvester was presented. Using these results the optimal design parameters for any range of harvester size, acceleration and operating frequency can be found. The parametrised model was also compared with an equivalent electrostatic energy harvester model enabling for the first time the optimal transduction method to be chosen for a given set of conditions. However in some applications such as a car journey, the mechanical excitation may vary, thus the damping force needs to be altered in real-time to maintain optimal performance. In the next chapter a technique is developed and demonstrated which implements maximum power point tracking.

6 Maximum Power Point Tracking Circuit

In the previous chapters methods of optimisation and implementation have been demonstrated, however they all assume the mechanical excitation remains constant. In this Chapter, a technique is developed which enables the real-time adaptation of the optimal damping force, thus achieving maximum power point tracking (MPPT).

6.1 Motivation for Maximum Power Point Tracking

Piezoelectric energy harvesters require a mechanical source of energy to drive them. For resonant harvesters, these sources are often motors or engines. Figure 6.1 shows vibrational data collected by [116] from a car engine (1999 Ford Focus 1.6 Petrol) during operation[1]. The figure shows that the amplitude of mechanical vibration can vary greatly during operation presenting a challenge when attempting to maximise power extraction. The power electronics interface circuit must therefore be able to adapt in real-time to these changes in excitation amplitude.

Maximum power point tracking (MPPT) circuits are typically used in photovoltaic cells [117, 118] although other forms of energy harvesting have also been demonstrated with MPPT[119, 120, 121]. An example of a piezoelectric energy harvester with MPPT was demonstrated in [122]. This implementation used a comparator with hysteresis to alter the frequency of energy transfer from an intermediate capacitor to a battery via a DC-DC converter. Initially no energy

[1]Data acquired by Joseph W. Matiko (financial support from Dar es Salaam Institute of Technology, http://www.dit.ac.tz) and analysed by Alex S. Weddell, University of Southampton (Next Generation Energy-Harvesting Electronics: Holistic Approach, http://www.holistic.ecs.soton.ac.uk/). Data downloaded via The EH Network Data Repository (ComparisonRealVibratationSources).

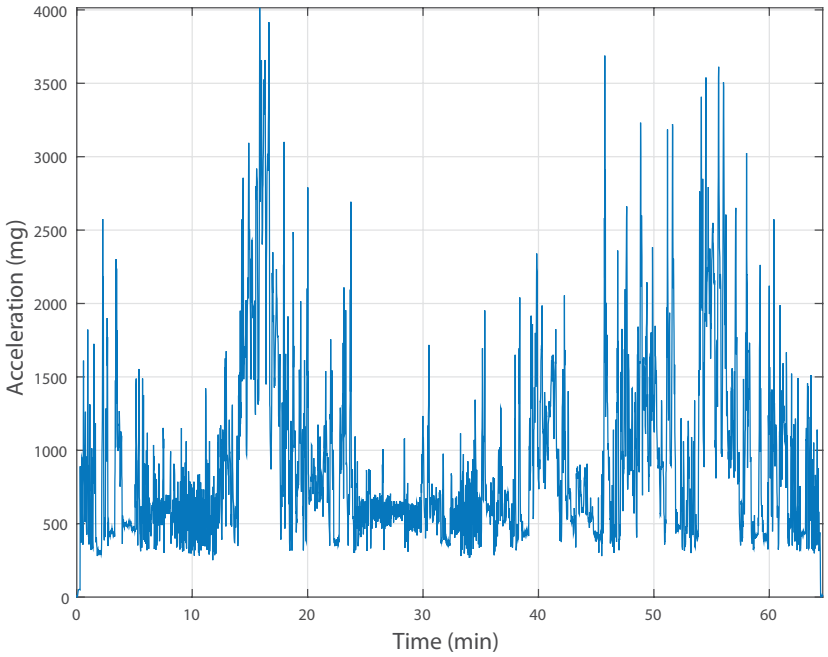


Figure 6.1: Vibration data for 1999 Ford Focus 1.6 Petrol car during typical operation [116].

is transferred from the capacitor until its voltage exceeds the comparator's high threshold voltage at which point the converter is enabled. When the capacitor voltage falls below the comparator's low threshold voltage, the converter is disabled. This ensures the voltage applied to the bridge rectifier oscillates around the optimal. However if the required optimal voltage strays too far from the fixed operating point, the circuit will be severely hampered and MPPT will not be achieved.

This chapter first identifies the requirements of a MPPT system for piezoelectric energy harvesters. An implementation of the system is then suggested and demonstrated in PSpice. An experimental verification is finally implemented using the bridge rectifier as the power conditioning circuit. All the work in this chapter is based on [96].

6.2 MPPT System Requirements

The MPPT system must first rectify the output voltage of a piezoelectric energy harvester induced by the sinusoidally mechanical driving force in order to charge a battery. Two different interface circuits both capable of rectification were therefore considered when designing the MPPT system. The first was a bridge rectifier circuit as it has the simplest implementation but suffers from poor power extraction [6]. The second is the SSPB circuit as its ability to change the piezoelectric harvester from a VDRG to CDRG enables the maximum power to be extracted although its implementation is more complex.

The power extracted by the diode bridge rectifier is determined by the conduction angle. This is set by the difference in the peak open-circuit voltage induced across the piezoelectric harvester, V_{po}, and the biasing capacitor voltage, V_{bias}. The conduction angle must be set to an optimal value to achieve maximum power extraction. Thus the voltage on the intermediate capacitor must be maintained at V_{optBR} (6.1) where V_{D} is the voltage drop across a diode.

$$V_{\mathrm{optBR}} = \frac{1}{2}\left(V_{\mathrm{po}} - 2V_{\mathrm{D}}\right) \tag{6.1}$$

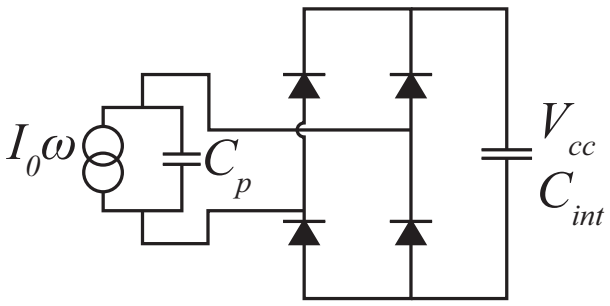


Figure 6.2: Piezoelectric energy harvester with bridge rectifier output.

The SSPB technique uses the voltage on the biasing capacitor to set the amount of charge transferred to the piezoelectric beam thus applying the optimal damping force. An expression

for optimal biasing voltage, V_{optSSPB}, is derived in [6] given in (6.2).

$$V_{\text{optSSPB}} = 2V_{\text{po}}\frac{\gamma}{1-\gamma^2} \tag{6.2}$$

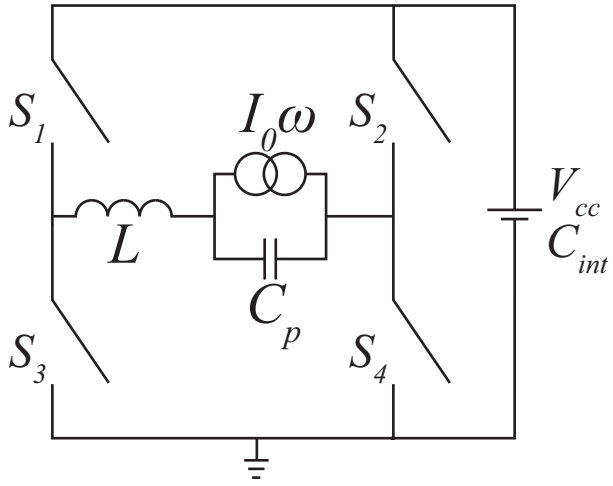


Figure 6.3: Piezoelectric energy harvester with SSPB circuit output.

The MPPT system for piezoelectric energy harvesters must therefore be capable of monitoring the harvester and adjusting the conduction angle (rectifier case) or damping force (SSPB case) applied. The system must detect a change in the piezoelectric induced voltage, quantify the magnitude of the change, and apply an appropriate response.

6.3 Implementation

Since both the bridge rectifier and SSPB techniques use a voltage on an intermediate capacitor to apply the optimal conduction angle and damping force respectively, adding a buck converter with battery enables the capacitor voltage to be independently set. The MPPT scheme can operate by adjusting the off-time of the buck converter causing the energy on the intermediate capacitor to be more or less frequently transferred, resulting in a decrease or increase in voltage respectively.

Figures 6.4 and 6.5 show the suggested topologies to adjust the voltage applied for both the

bridge rectifier and SSPB circuit respectively. The voltage on the intermediate capacitor, C_{int}, is controlled by varying the power transferred through the buck converter. If the time between energy transfers is increased, C_{int} voltage will rise and a greater damping force will be applied to the piezoelectric material.

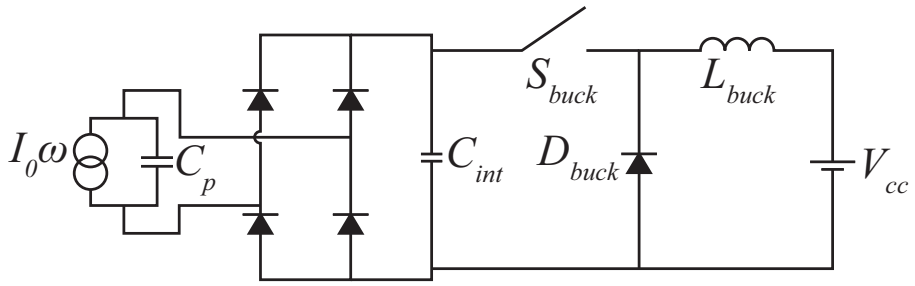


Figure 6.4: Piezoelectric energy harvester with bridge rectifier, buck converter and battery [96].

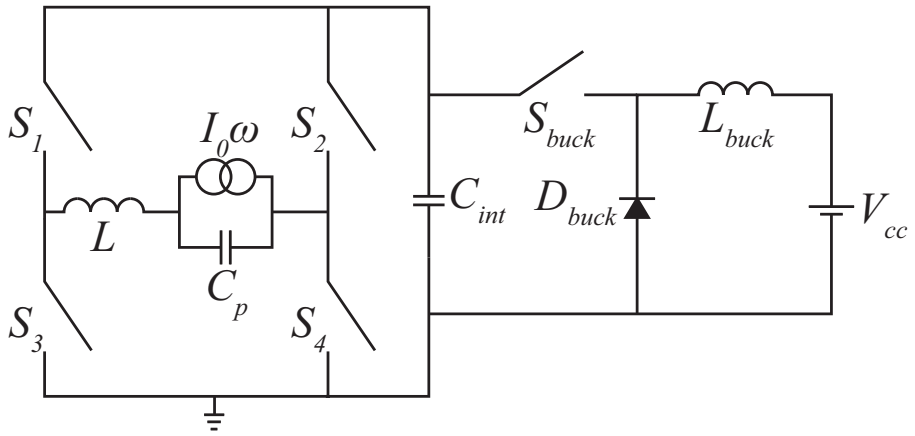


Figure 6.5: Piezoelectric energy harvester with SPPB circuit, buck converter and battery [96].

A PSpice simulation of the effect on power generation as energy is transferred from the intermediate capacitor to the storage battery is shown in Figure 6.6. The induced current was increased representing an increase in mechanical excitation. The power per cycle was measured over four energy transfer periods for two different buck converter off-times. The results show that the system with the longer buck converter off-time generated more power on average.

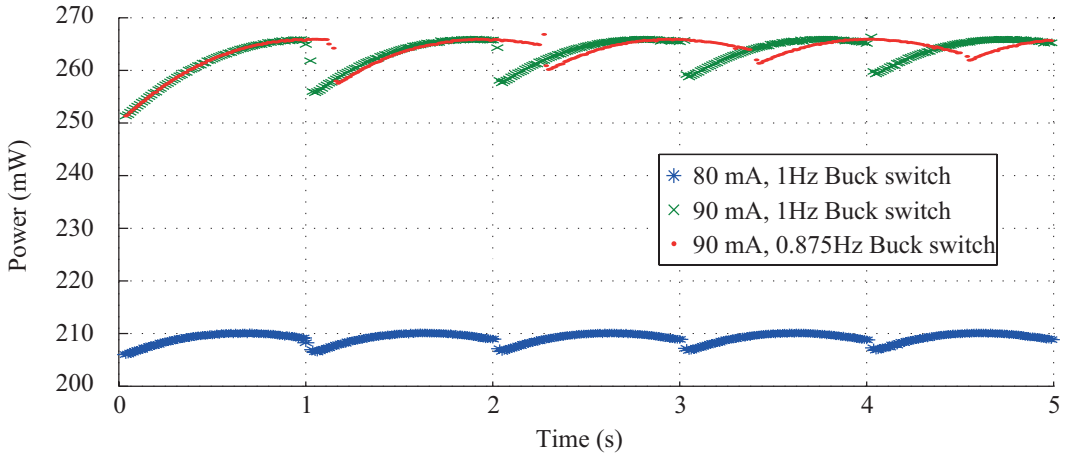


Figure 6.6: PSpice simulation of the effect of adjusting the off-time of the buck converter on the power generated by a SSPB circuit for two different mechanical excitation forces [96].

6.4 Experimental Implementation

The proposed MPPT scheme requires three elements, a circuit capable of measuring the power generated, a controller to decide whether the power has increased or decreased since the previous measurement and a buck converter to transfer the energy from the intermediate capacitor to the battery. Figure 6.7 shows a circuit possible circuit topology which can be used for either the SSPB or bridge rectifier circuit. Figure 6.8 is the algorithm for the FPGA shown in Figure 6.7 [96]. The operation is described in detail in the following sections.

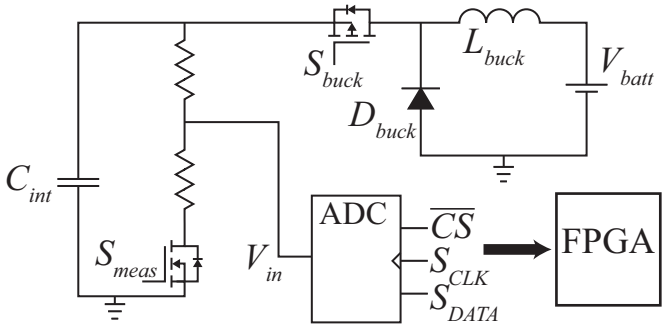


Figure 6.7: Piezoelectric energy harvester MPPT circuit [96].

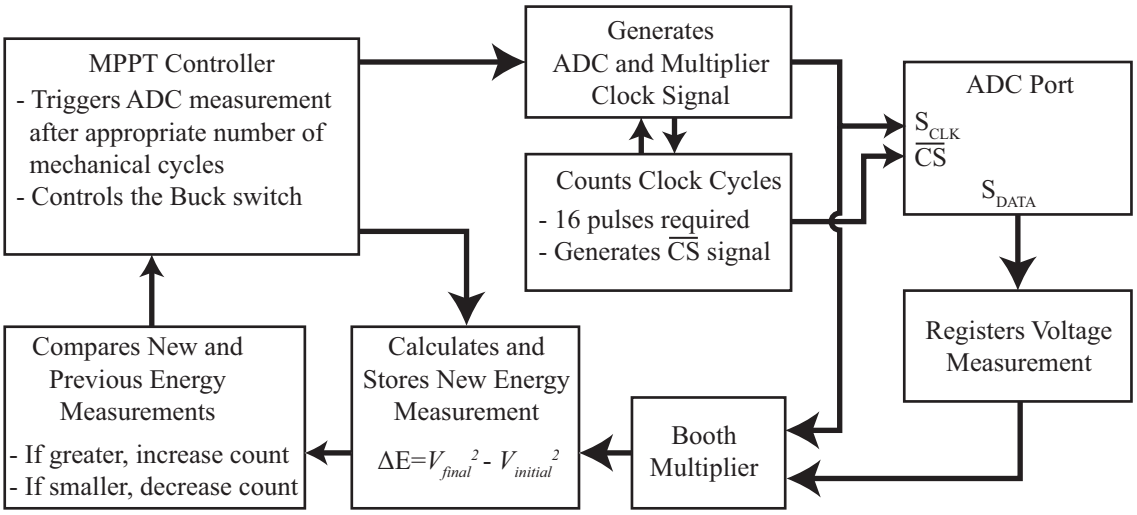


Figure 6.8: Piezoelectric energy harvester MPPT algorithm [96].

6.4.1 Change detection

The system needs to identify when the damping force needs to be adjusted due to a change in the mechanical excitation force to maintain maximum power extraction. A change can be detected by periodically measuring the energy transferred to the intermediate capacitor, C_{int}. The energy being generated is found by comparing the square of C_{int} voltage at the start, V_{init}, and end, V_{end}, over a set number of cycles (6.3). This result can then be compared to a previous measurement taken many cycles ago so that the trend for increasing or decreasing power extraction can be determined.

$$\Delta E = \frac{1}{2} C_{\text{int}} \left({V_{\text{end}}}^2 - {V_{\text{init}}}^2 \right) \tag{6.3}$$

Accurately measuring the voltage on the capacitor presents several difficulties which have to be overcome. Any power consumption used to measure the voltage detracts from the efficiency of the energy harvester. The measurement and control circuitry therefore should operate at the lowest voltage possible, however the voltage on the biasing capacitor maybe several times larger than this. A potential divider can be switched in across C_{int} during a measurement (Figure 6.7).

In the experimental implementation, an n-type MOSFET (BSS138 [105]) which can be driven by a low power FPGA (Igloo Nano [93]) was used. Conveniently the FPGA can also be used to implement the SSPB scheme [85]. A low power Analog-to-Digital Converter (ADC AD7468 [123]) can then be used to measure the voltage and a Booth Multiplier algorithm [124] on the FPGA can square the value.

6.4.2 Controller

The control algorithm shown in Figure 6.8 was implemented on the low power FPGA for MPPT. The controller works as follows: initially the buck converter transfers energy once per second, (e.g. every 80 cycles at 80 Hz), therefore just before and just after half second (e.g. at a count of 38 and 42 cycles), the voltage is measured as V_{init} and V_{end} respectively. Both values are squared and V_{init} is subtracted from V_{end}. The result is compared against the previous energy measurement, one second (80 cycles) previous. If the new result is greater than the former, the count is increased allowing the voltage to rise and increase the damping force. If the result is less, the counter is decreased, reducing the voltage the intermediate capacitor will attain, decreasing the damping force. However if it is the same, the counter stays the same and the damping force is not altered. The cycle counter signal for the SSPB signal is naturally generated by the switching pulses used to implement the scheme. The bridge rectifier however requires a secondary sense piezoelectric beam to be mechanically coupled to the generating beam and a zero crossing detector with an over-voltage protection MOSFET to generate the same signal (Figure 3.9 [87]).

The ADC and Booth Multiplier algorithm both need a clock signal in order to operate. The simplest solution is to use a crystal oscillator [125]. However the required clock signal may only be operating for a few microseconds, once a second, thus the oscillator's required start-up time and power consumption renders this solution undesirable. Instead it is more efficient to generate the clock signal using a RC circuit. This technique is also used in SSPB circuit to generate the on-time pulses for the switches [85].

6.5 Results

The MPPT circuit was tested with a bridge rectifier circuit connected to a buck converter with a 1.2 V power supply representing the battery. The on-time for the buck switch was set to 118 μs and the off-time was varied by an Igloo Nano FPGA. A 50 nF piezoelectric loudspeaker was used to represent the harvester. It was mechanically excited at 200 Hz with different accelerations causing different induced open-circuit voltages, V_{po}, across the piezoelectric capacitance. Power generation on the intermediate capacitor was measured using a Yokogawa WT210 power meter at 5 second intervals. The results were compared with the theoretical limit given in (2.10) demonstrating the circuit's functionality (Figure 6.9). The power consumption of the controller was measured as 50 μW when the piezoelectric transducer was inducing an open-circuit voltage of 6.75 V, however this has not been subtracted from the results in Figure 6.9 as it is expected with further work the power consumption can be greatly reduced.

It can be seen at high degrees of acceleration (corresponding to large V_{po}), the system achieves close to the theoretical limit. However at lower excitation levels, performance is degraded due to the number of cycles between transfers and the number of cycles between measurements converging. This issue could be alleviated by increasing the resolution of the ADC so fewer cycles are required between measurements.

The algorithm and implementation enabled the piezoelectric energy harvester to automatically adapt to variation in mechanical excitation. The system tracked the maximum power point by adjusting either the conduction angle of the bridge rectifier. The MPPT system could be implemented with other power conditioning circuits such as the SSHI-DC or SSPB as they both require an intermediate capacitor with an optimal voltage determined by the input acceleration. The MPPT system could be improved by reducing the power consumption of the algorithm and increasing the resolution of the ADC to improve performance at low acceleration levels.

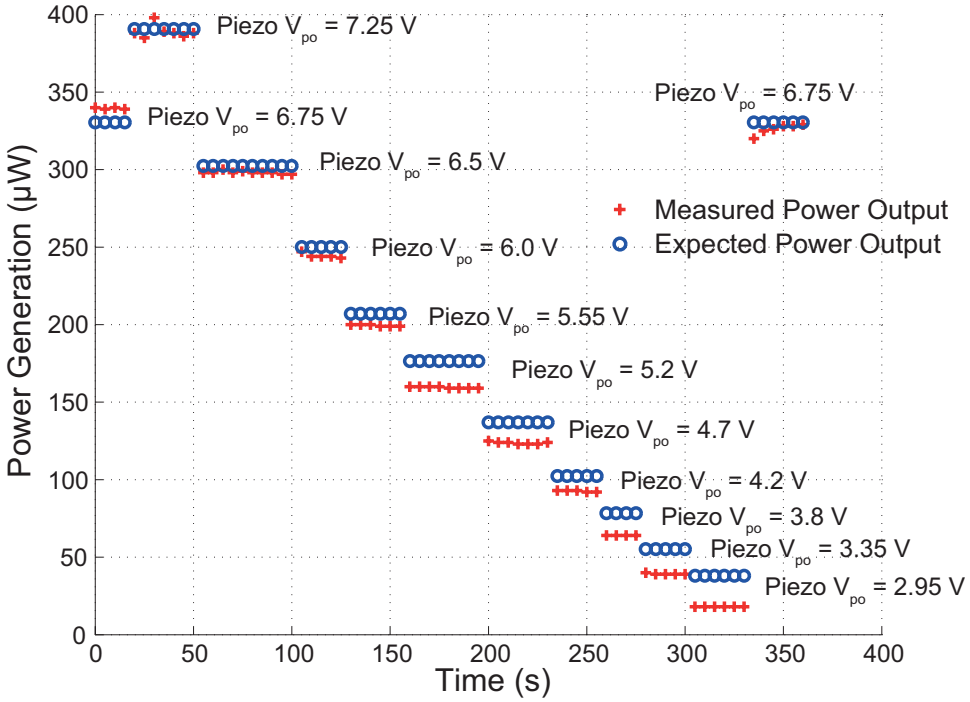


Figure 6.9: Comparison between measured power generation using MPPT implementation and bridge rectifier theoretical maximum power limit for several different excitation forces [96].

6.6 Summary

In this chapter a circuit was demonstrated which provdided real-time adaptation to variation in the excitation force. The circuit was experimentally demonstrated with the bridge rectifier but could be adapted for the SSPB circuit. In the next chapter, the conclusions of all the work in this thesis are presented and summarised.

7 Conclusion

7.1 Main research purpose

This Ph.D research had two main purposes. First, to invent a low-power circuit capable of implementing the optimal damping force to apply to a piezoelectric energy harvester to maximise power extraction. Second, to develop a model capable of fully optimising a complete piezoelectric energy harvesting system, including a piezoelectric transducer, a power conditioning circuit, and a battery.

7.2 Summary and contributions

Maximum power is extracted by a piezoelectric energy harvester when it is operated as a Coulomb damped resonant generator (CDRG). The single-supply pre-biasing (SSPB) circuit is the most compact way of implementing this type of damping. An implementation of the SSPB circuit was developed which experimentally generated 14 % more power than the theoretical limit of the next best technique including the 126 μW of power required for the control circuitry. To achieve this a low power peak detection circuit, a non-synchronous FPGA design, and high and low side gate drives were developed.

The original SSPB circuit enabled the power extraction to be optimised. However, a new mode of SSPB operation, known as forced return to zero (FRTZ) was developed and demonstrated. This extended the usable lifetime of piezoelectric energy harvesters by compensating for the degradation in electrical properties due to repeated mechanical stress being applied over millions

of cycles. This enables the extension of the usable lifetime of wireless sensors as the harvester power output degrades at a much slower rate, and increases the maximum power available at the high input energy range.

Piezoelectric energy harvesting systems are principally made up of the transducer, power conditioning circuit and the battery charging circuit. Traditionally research has focussed on optimising one of these components, however they are all dependent on each other, therefore it is necessary to fully model the system when optimising. An interdisciplinary collaboration was undertaken to fully parametrise the system, enabling an engineer to choose the optimal sizing of the mass, beam length and thickness, inductor and MOSFET semiconductor area. This hugely complex model enables for the first time the often asked, and until now inadequately answered, question of which MEMS compatible transducer type achieves the best power density in an energy harvesting system.

Power generation by resonant piezoelectric harvesters can be severely limited if the damping force cannot be dynamically altered as the mechanical excitation level changes. An algorithm and implementation were therefore developed which enabled real-time adaptation to variations in the mechanical force, by altering frequency of energy transfer between an intermediate storage capacitor and battery. This enables the voltage on a capacitor to be adjusted to the optimal value for maximum power extraction using either a diode bridge rectifier or SSPB circuit. Therefore maximum power point tracking (MPPT) for piezoelectric energy harvesters has been achieved.

The author's contributions are:

- The first experimental implementation of the SSPB circuit.
- Experimental verification of the SSPB circuit outperforming the theoretical limit of the SSHI technique.
- Invention and demonstration of a new mode of operation (FRTZ) for the extension of the usable lifetime of a piezoelectric energy harvester.

- A complete model parametrisation and optimisation of piezoelectric energy harvesting system.
- Answering the question of which MEMS compatible transducer type achieves the best power density in an energy harvesting system.
- Invention and demonstration of a method of MPPT for piezoelectric energy harvesters.

7.3 Future Work

A sub 40 μW implementation of the SSPB circuit was demonstrated, which would be more effective than a simple diode bridge rectifier for harvesters capable of generating more than 50 μW. However, from the performance predicted by the piezoelectric energy harvesting system model analysis, many harvesters generate much less power than this. Therefore further work into reducing the power consumption of the control circuit is necessary. This improvement will partly occur as technology advances, as the devices used will reduce in quiescent current and leakage. A big improvement should also be achievable through the development of a custom integrated chip (IC). This will enable optimisation of all components for energy harvesting rather than standard off the shelf parts currently used. A custom IC will also improve the reliability and provide a simple way for future piezoelectric transducers to be tested.

Whilst the degradation of piezoelectric material due to repetitive mechanical cycling has been investigated, the long-term effects of charge modification techniques on the characteristics of piezoelectric energy harvesters has not been considered. This may result in further constraints being placed on the design of future piezoelectric energy harvesting systems. Implementation of the FRTZ technique also needs further research to achieve a single inductor implementation thus increasing power density.

Complete analytical models of both electrostatic and piezoelectric energy harvesting systems have been made, enabling direct comparison of the two transducers. These two systems were compared directly as the most appropriate approaches for energy harvesting systems in the

micro to mesa scale range. This comparison could now be extended into the larger scale energy harvesting systems based on electromagnetic transducers. A complete parametrised system model for electromagnetic energy harvesters would be required to enable a full comparison of resonate vibration driven energy harvesters to be completed.

The MPPT circuit for piezoelectric energy harvesting has only been demonstrated for the bridge rectifier circuit. This approach could be extended to investigate the other power conditioning circuits (e.g. SSHI, SSPB). On the basis of the present and further research it should then be possible to construct a comprehensive model to enable future designers to predict the optimal system approach.

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8 Appendix A

8.1 SSPB schematic and PCB

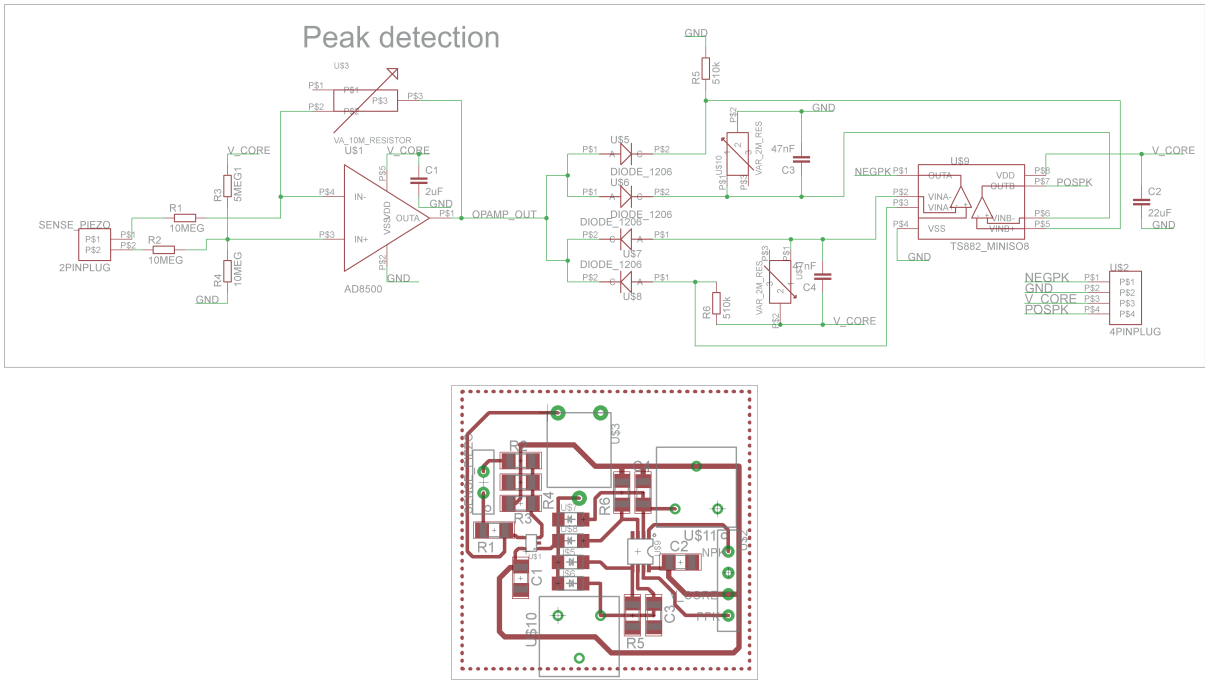

Figure 8.1: Peak detection schematic and PCB design.

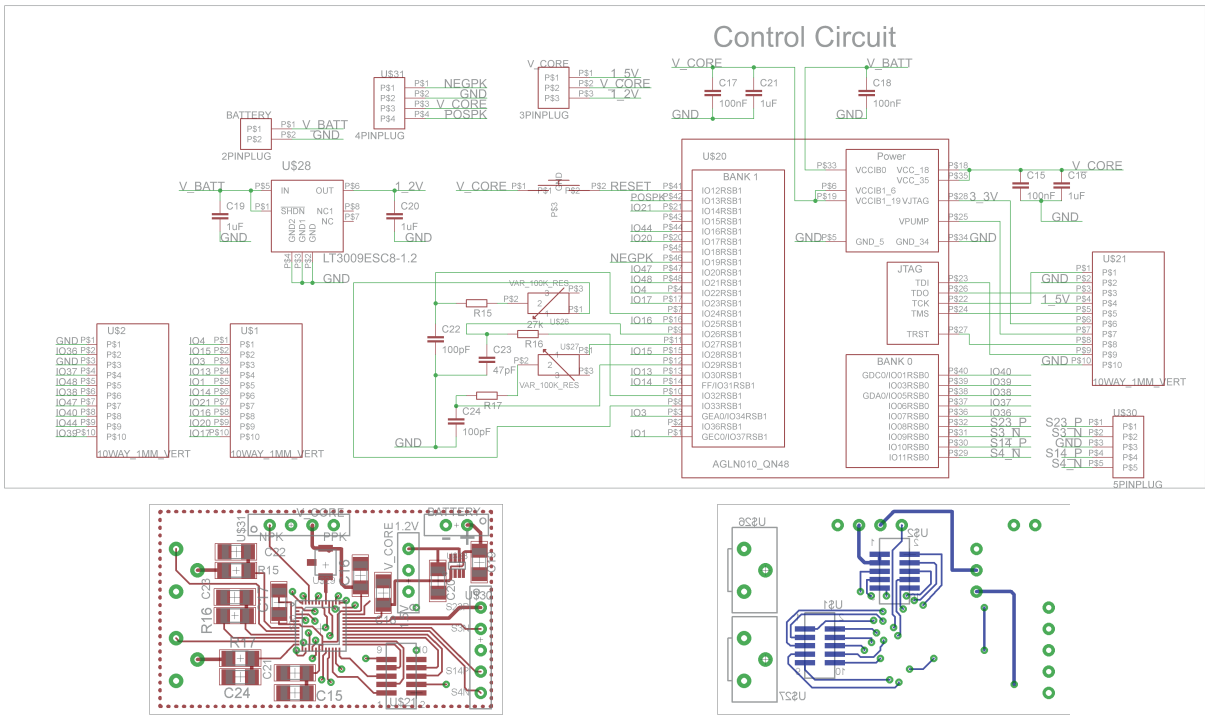

Figure 8.2: SSPB control circuit schematic and PCB design.

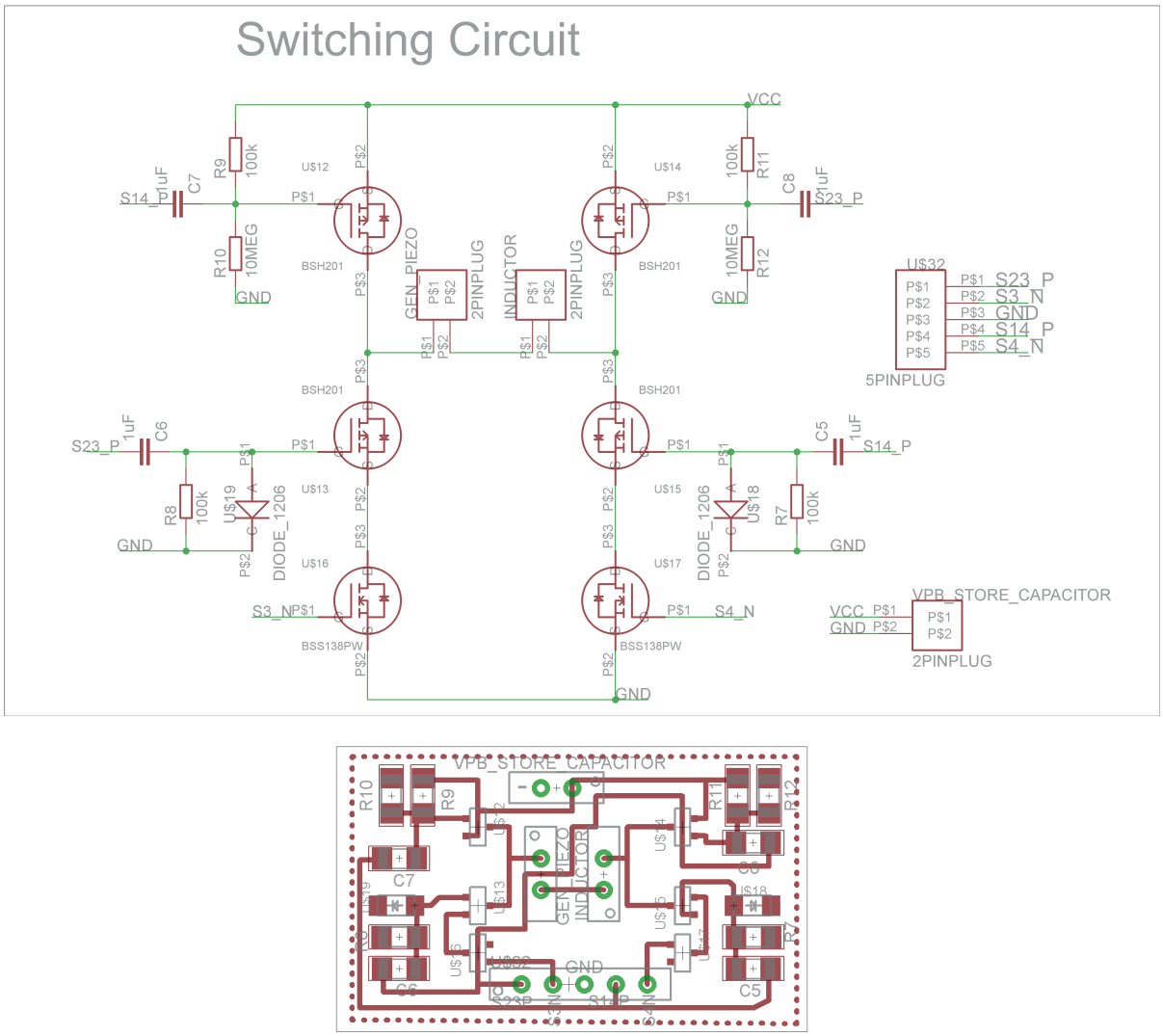

Figure 8.3: SSPB H-bridge circuit schematic and PCB design.

9 Appendix B

The algorithm for the bridge rectifier is based on the work presented in [109]. The algorithm starts by finding beam length and thickness pairs which resonant at the target operating frequency. The transducer's parameters are then calculated.

To calculate the optimal resistive load value a loop is entered where resistance is doubled and the output power is calculated. If the output power for the current resistive load value has increased compared with the previous output power, then the increase in resistance is doubled and the loop repeats. If the output power has decreased, then the resistance is reduced by half the previous increased value. The voltage across the piezoelectric material is checked for dielectric voltage breakdown. If the voltage has been exceeded, then no solution exists which will ensure the mass stays within the harvester volume and the next beam length and thickness pair is tried. If the piezoelectric voltage is less than the dielectric breakdown voltage. The loop exits when the power generation variation is less than 0.01 %.

The losses for either the buck or boost converter circuits are then accounted for and the next beam length and thickness pair is tested. Once all pairs for a given volume and acceleration have been tested, the design parameters which generated the most power are stored and the next volume and acceleration pair are tested.

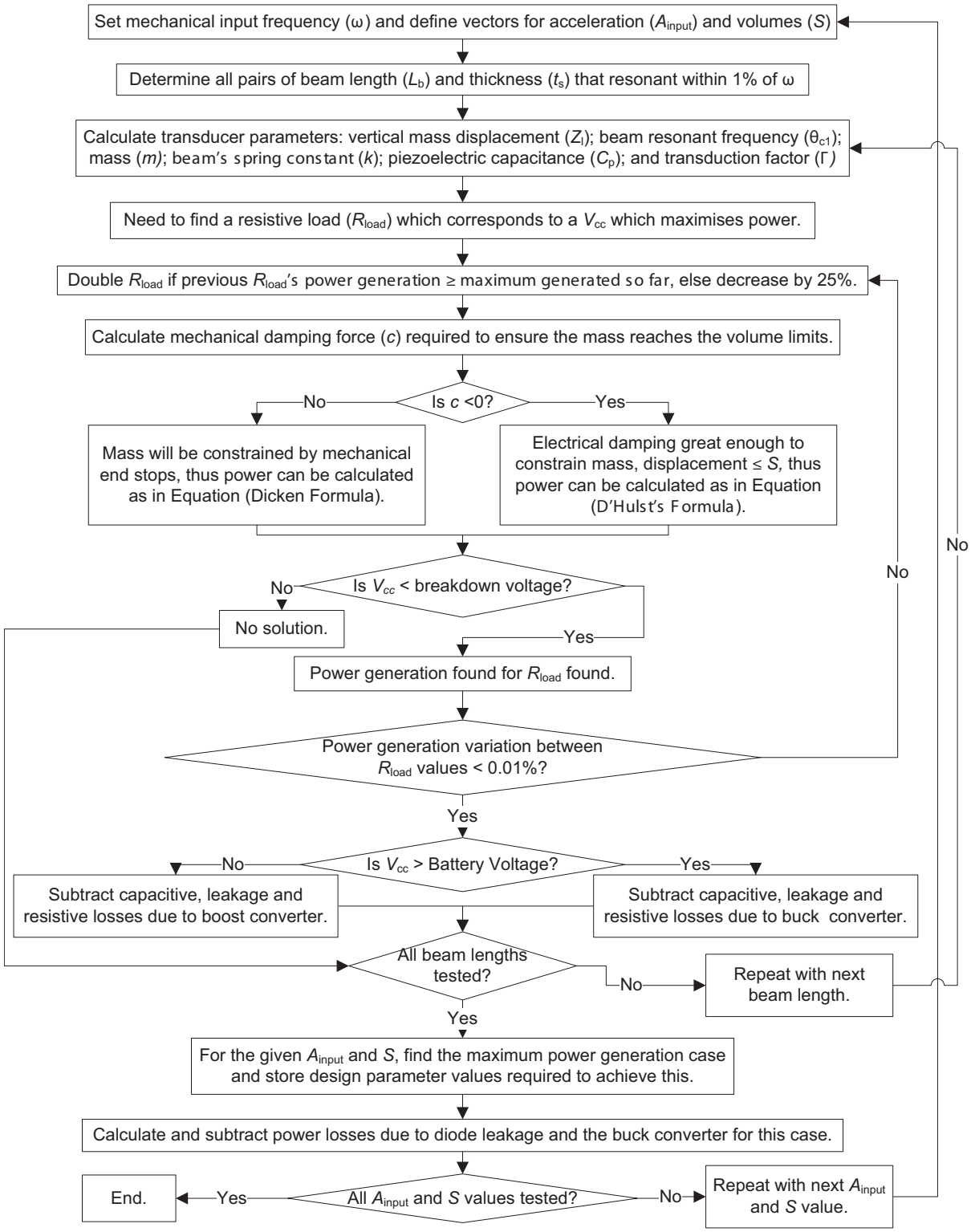

Figure 9.1: Algorithm used to calculate power generation using a bridge rectifier circuit.

10 Appendix C

10.1 1 Hz results

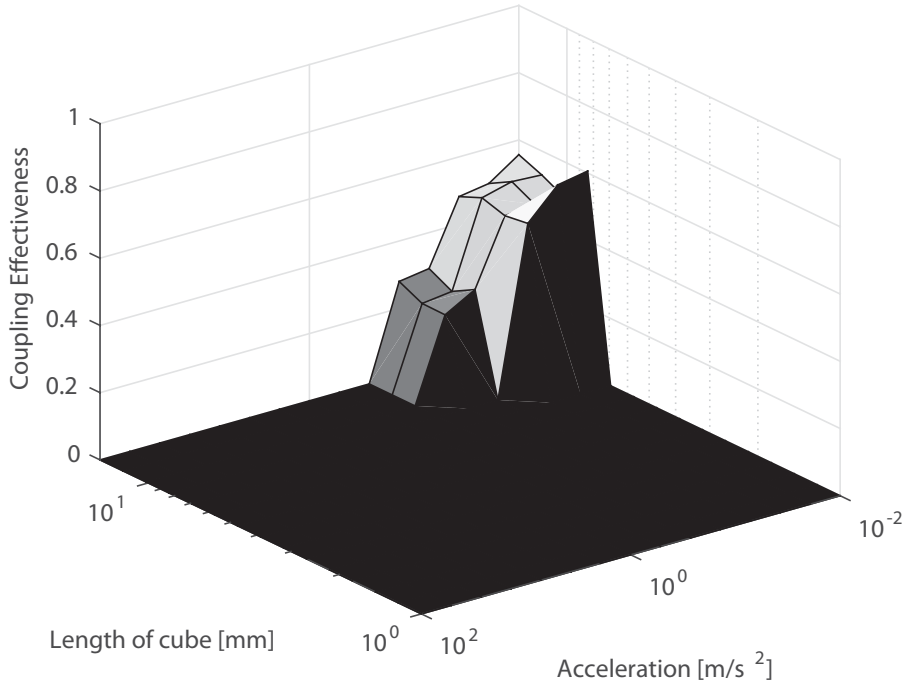

Figure 10.1: Coupling effectiveness at 1 Hz.

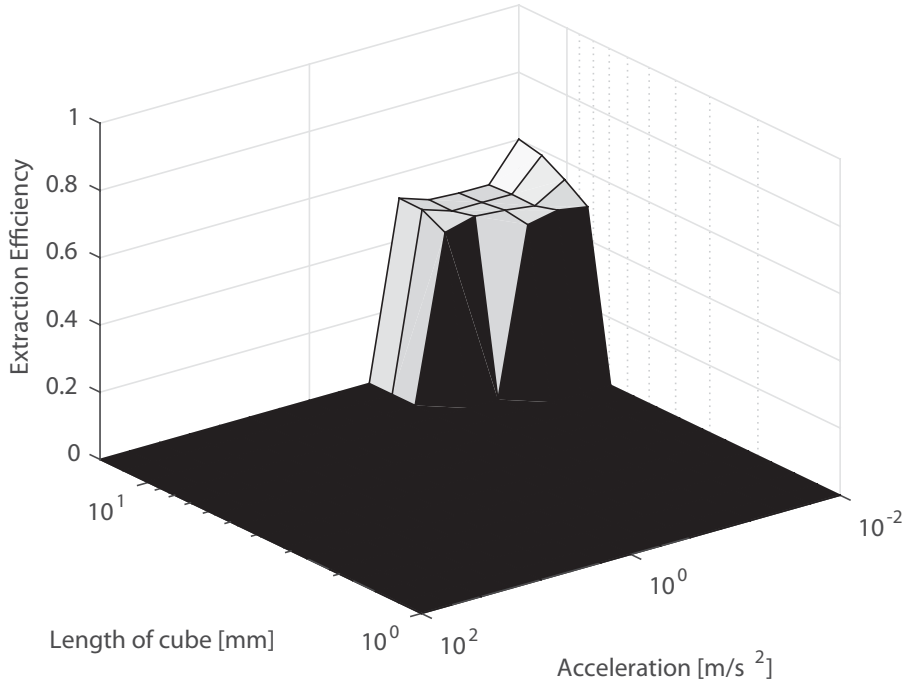

Figure 10.2: Extraction efficiency at 1 Hz.

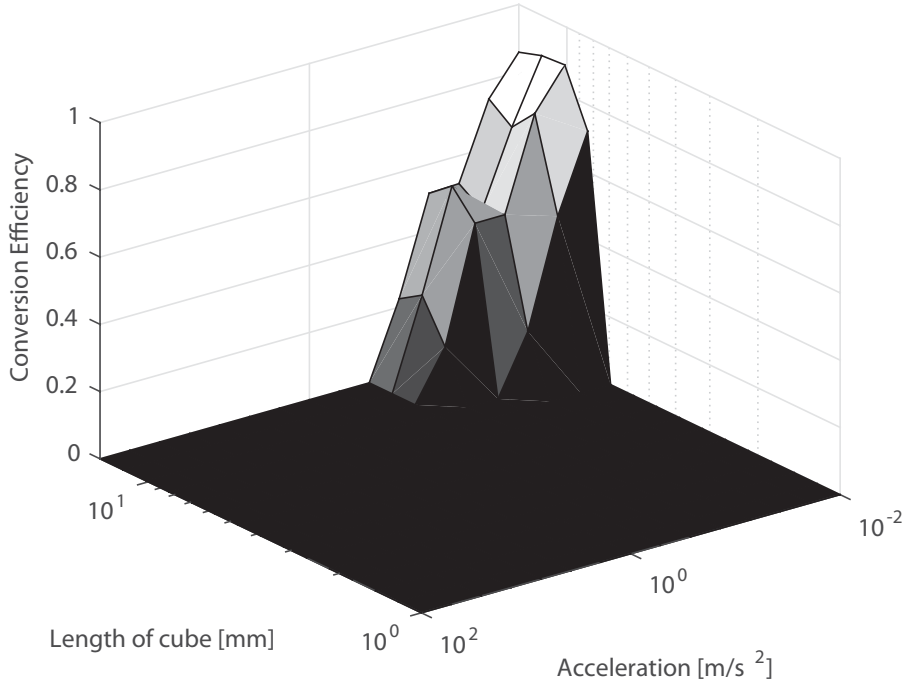

Figure 10.3: Conversion efficiency at 1 Hz.

10.2 10 Hz results

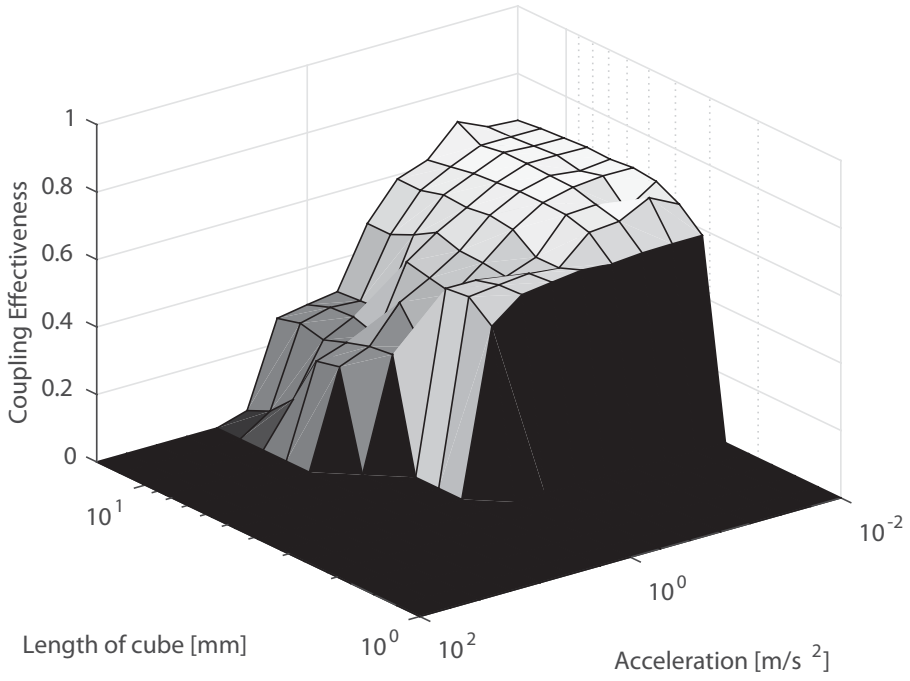

Figure 10.4: Coupling effectiveness at 10 Hz [106].

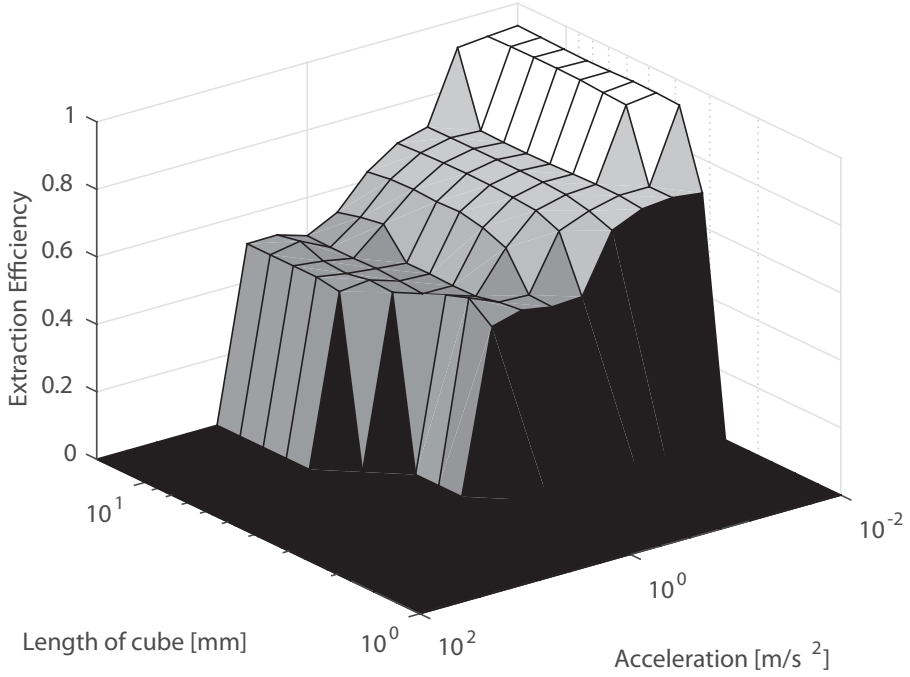

Figure 10.5: Extraction efficiency at 10 Hz [106].

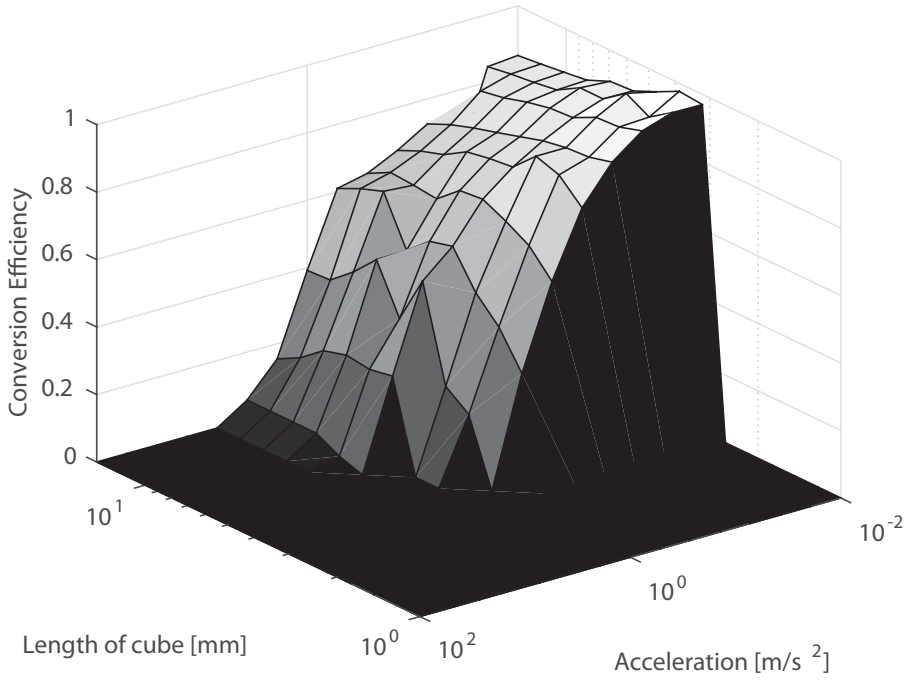

Figure 10.6: Conversion efficiency at 10 Hz [106].

10.3 1000 Hz results

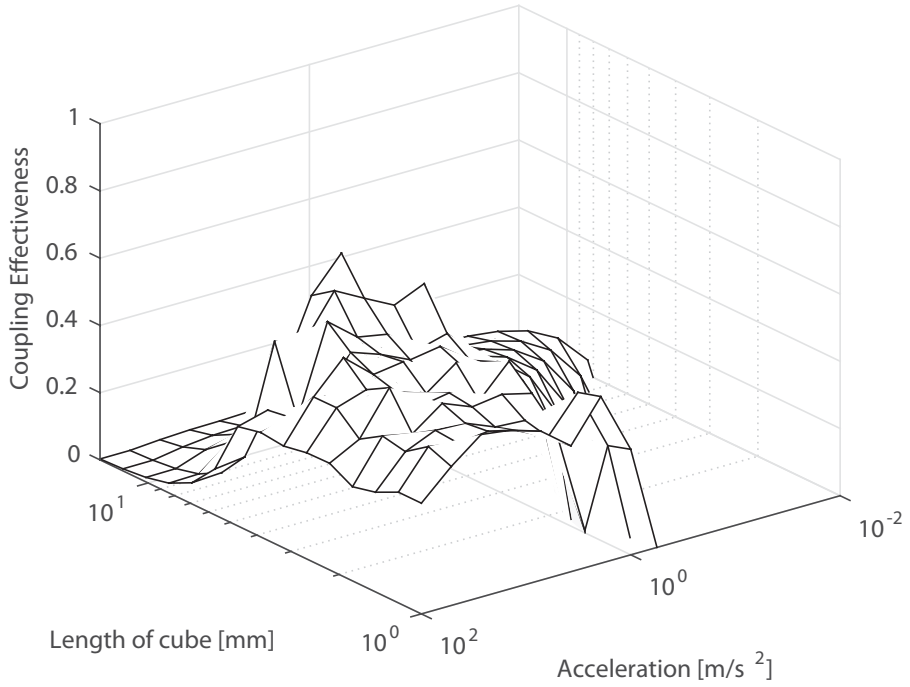

Figure 10.7: Coupling effectiveness at 1000 Hz.

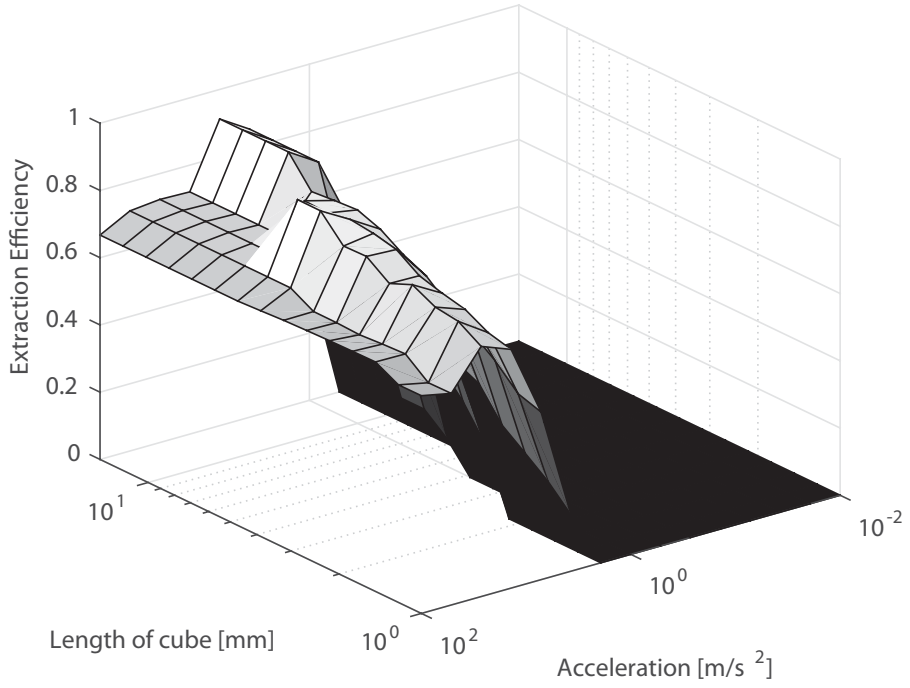

Figure 10.8: Extraction efficiency at 1000 Hz.

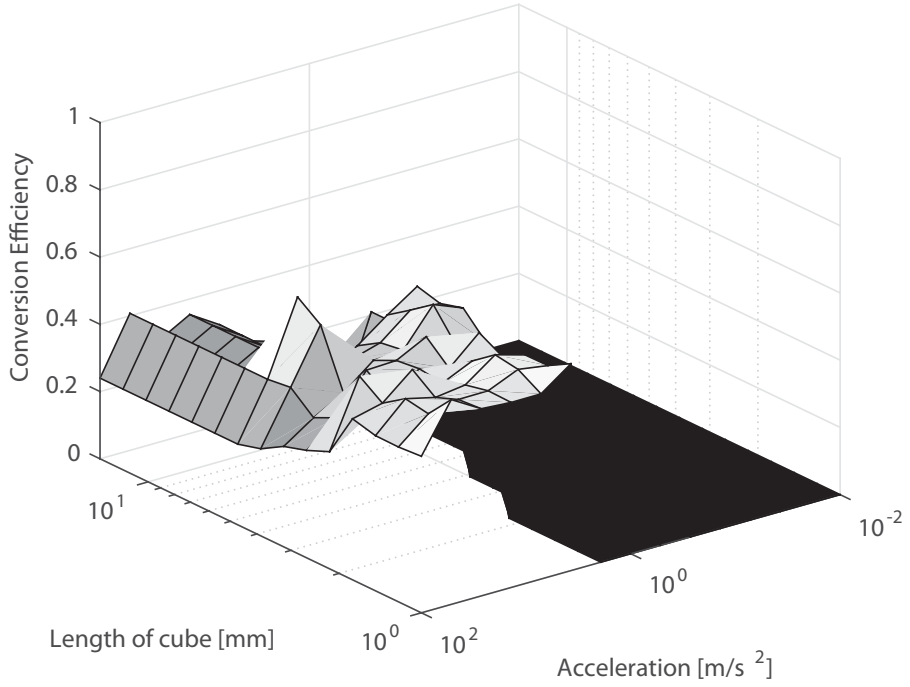

Figure 10.9: Conversion efficiency at 1000 Hz.

10.4 Silicon 100 Hz results

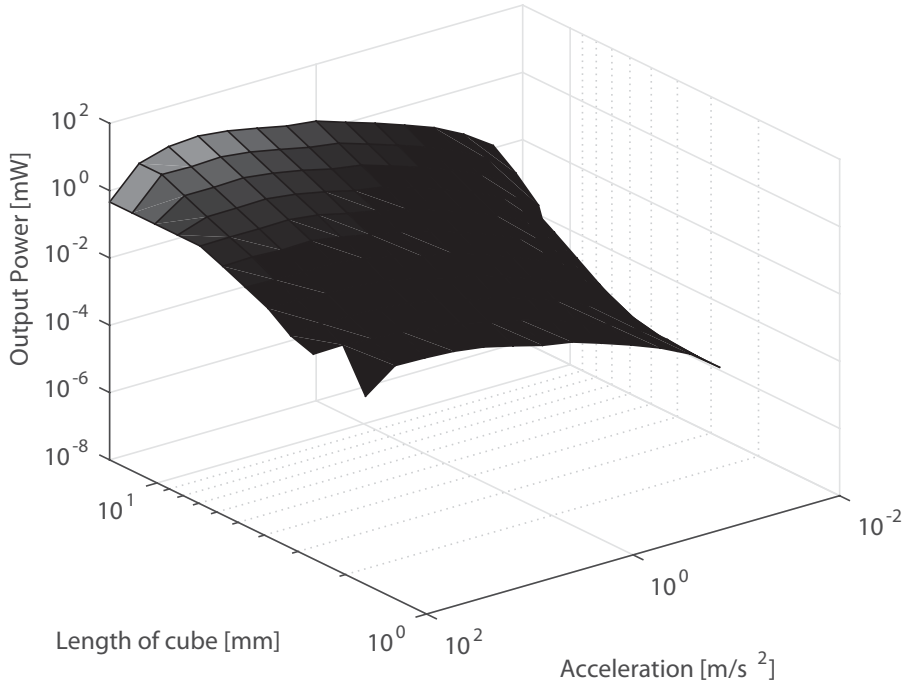

Figure 10.10: Power output at 100 Hz [106].

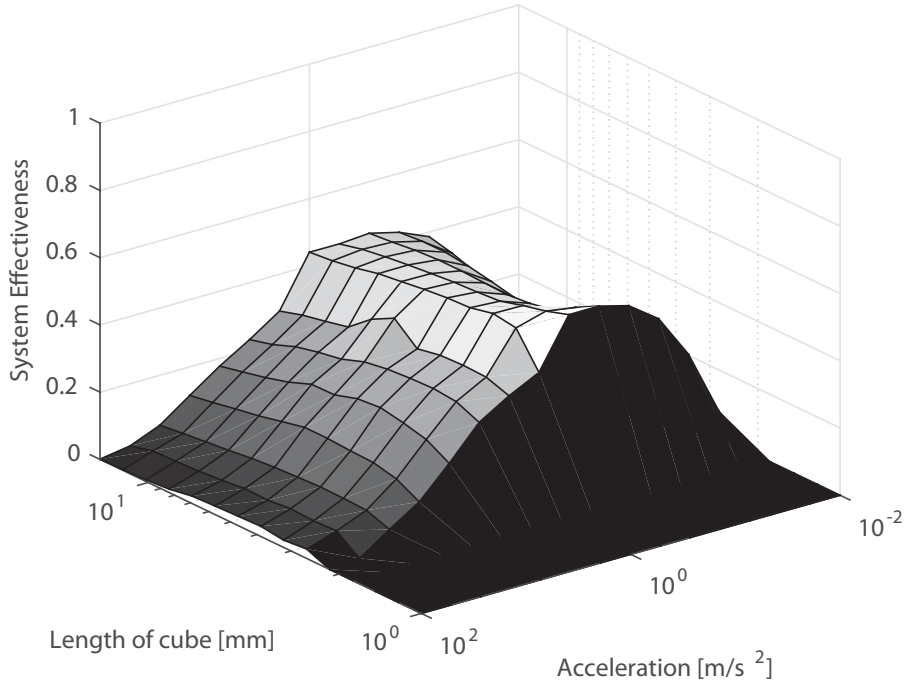

Figure 10.11: System effectiveness at 100 Hz [106].

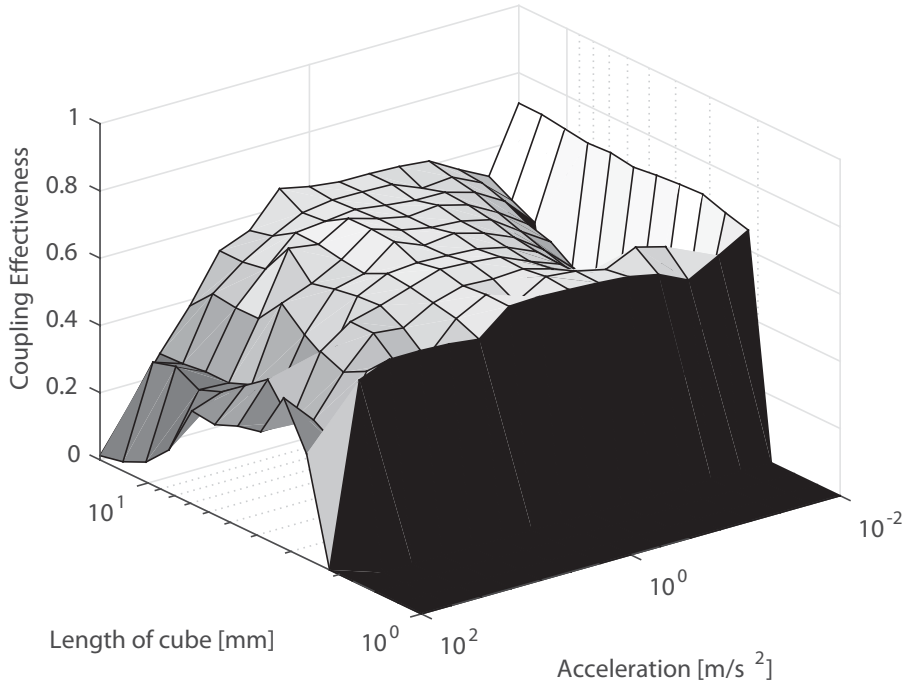

Figure 10.12: Coupling effectiveness at 100 Hz [106].

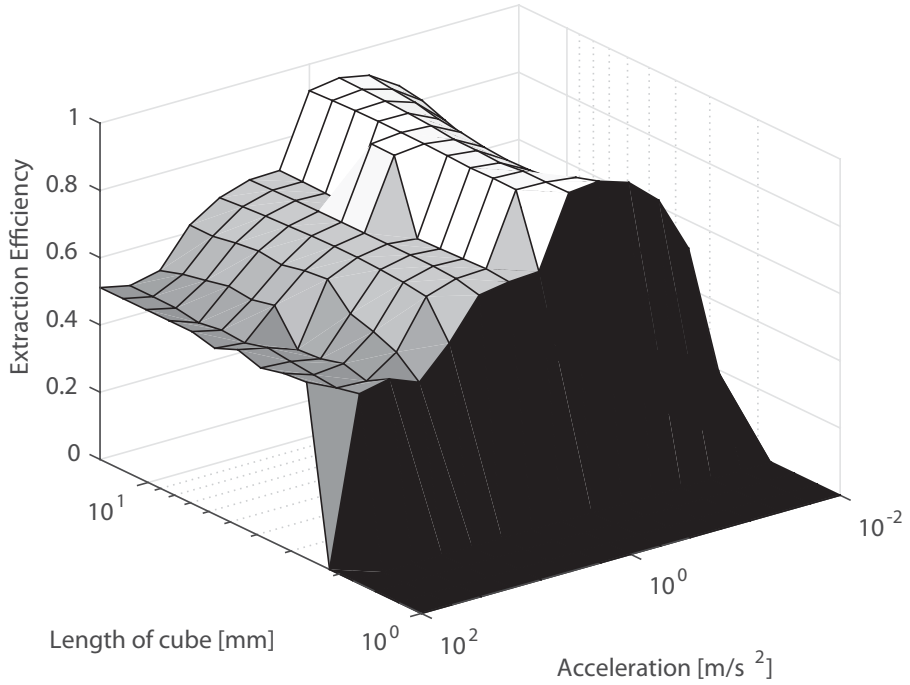

Figure 10.13: Extraction efficiency at 100 Hz [106].

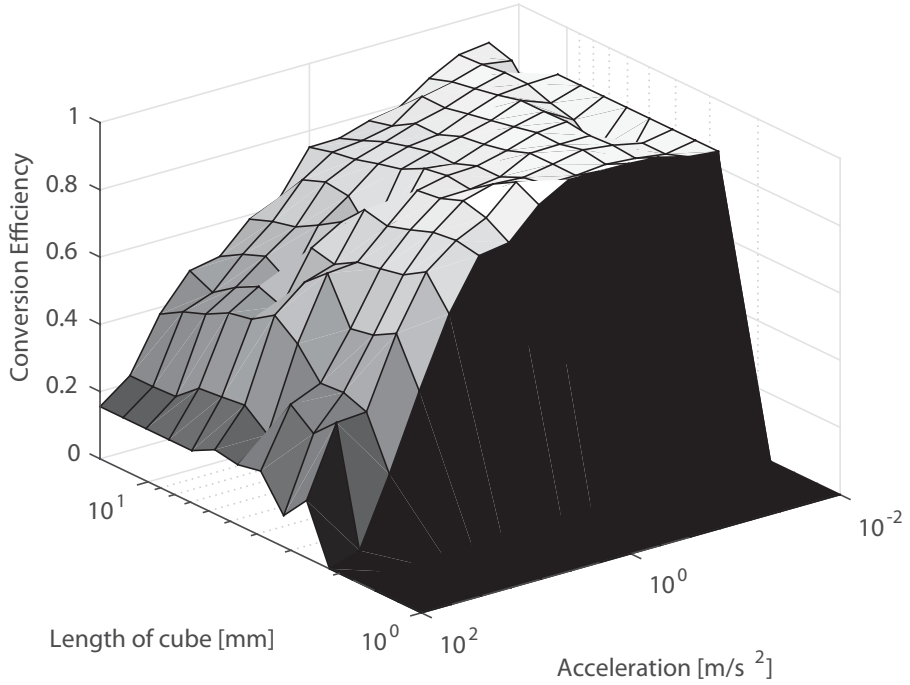

Figure 10.14: Conversion efficiency at 100 Hz [106].