Large-Area Flexible Electronics Based on Low-Temperature Solution-Processed Oxide Semiconductors

by Yen-Hung Lin

A thesis submitted in partial fulfilment of the degree of

Doctor of Philosophy

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Department of Physics

April 30, 2015

In memory of my late father, Ching-Yung Lin.

DECLARATION

This thesis describes the work carried out between October 2011 and December 2014 in the Experimental Solid State Physics group of Imperial College London, under the supervision of Prof Thomas D. Anthopoulos. The material in this thesis has not been previously submitted for a degree at any University and except where explicitly stated is the product of my own work.

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ABSTRACT

Due to their high charge carrier mobility, optical transparency and mechanical flexibility, thin-film transistors (TFTs) based on metal oxide semiconductors represent an emerging technology that offers the potential to revolutionise the next-generations of large-area electronics. This thesis focuses on the development of high-performance TFTs based on low-temperature, solution-processed metal oxide semiconductors that are compatible with inexpensive flexible plastic substrates.

The first part of the dissertation describes an ultraviolet light assisted processing method suitable for room-temperature activation of ZnO nanoparticles and their application as semiconducting channels in TFTs. The impact of the semiconductor/dielectric interface on electrical performance is studied using different device configurations and dielectric surface-passivation methods. Furthermore, a nanocomposite concept is proposed in order to assist electron transport between different crystalline domains. Using this approach, TFTs with electron mobilities of ~3 cm^2/Vs are demonstrated.

The second part of this work explores a carbon-free, aqueous-based Zn-ammine complex route for the synthesis of polycrystalline ZnO thin-films at low temperature and their subsequent use in TFTs. Concurrently, the development of a complementary high-κ oxide dielectric system enables the demonstration of high-performance ZnO TFTs with electron mobilities >10 cm^2/Vs and operation voltage down to ~1.2 V. This low-temperature aqueous chemistry is further explored using a facile n-type doping approach. Enhancement in electrical performance is attributed to the different crystallographic properties of the Al-doped ZnO layers.

The final part of the thesis introduces a novel TFT concept that exploits the enhanced electron transport properties of low-dimensional polycrystalline quasi-superlattices (QSLs), consisting of sequentially spin-cast layers of In_2O_3, Ga_2O_3 and ZnO deposited at temperatures <200 °C. Optimised oxide QSL transistors exhibit electron mobility values of >40 cm^2/Vs - an order of magnitude higher than devices based on single binary oxide layers. Based on temperature dependent electron transport and capacitance-voltage measurements, it is reasoned that the enhanced electrical performance arises from the presence of quasi two-dimensional electron gas-like systems formed at the carefully engineered oxide heterointerfaces buried within the QSLs.

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INTRODUCTION

1.1 Background

In the early twentieth century, a *vacuum tube* (or *valve*) was the basic building block for electronics. The working principle is based on thermal emission of electrons from a heated cathode to an anode in a vacuum-sealed container. One type of the vacuum tubes that operates in a similar way to the modern three-terminal field-effect devices is *triode*, which was invented by Lee de Forest in 1907. A triode utilises a voltage-controlled grid that is placed in-between the cathode and the anode to adjust the flow of electrons from the cathode. However, the numerous drawbacks of vacuum tubes, such as large size, inefficient power usage, limited lifespan, high manufacturing cost, etc., provided a significant obstacle in pushing this technology forward. Therefore, the vacuum tube was later replaced by the *transistor*, which possesses advantages over the vacuum tube in all of the aforementioned aspects. The earliest "transistor-like" concept was proposed by Julius Edgar Lilienfeld in the 1920s [1-3]. In addition to Lilienfeld's works, in 1935 Oskar Heil filed a patent, which suggested a number of possible ways in order to control the resistance in a semiconducting material by applying an electric field [4]. In 1947, the first transistor was made from a germanium (Ge) crystal (schematically illustrated in Figure 1.1) at Bell Laboratories by John Bardeen, Walter Brattain and William Shockley [5, 6].

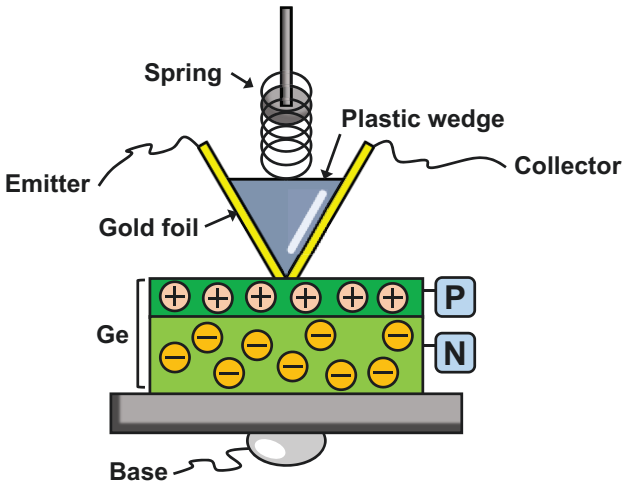


Figure 1.1: Schematic illustration of the first transistor demonstrated in Bell Laboratory. The transistor consisted of an n-type Ge crystal whilst a thin p-type inversion layer formed near the crystal surface. The latter can be controlled by the base bias. The point contacts were made of gold foil and closely positioned in a distance of <0.05 mm between each other with the assistance of a plastic wedge. When applying a DC bias to the emitter, an electric current can flow through the inversion layer to the collector side [5, 7].

Going from the vacuum tube to the transistor, the key to the success of the 'solid-state' transistor was the use of semiconductors that possess the property of becoming a controllable switch. Silicon (Si) is the most well-known semiconductor, and its use is widespread in all aspects of people's daily lives. The first Si transistor was demonstrated in the 1950s using single silicon crystals, a few years after the invention of the first transistor [8]. Since then, the rapid development of Si-based technologies from the pioneers at Bell Laboratories and Texas Instruments pushed electronics into what has become known as the "Silicon Age".

In the mid-twentieth century, several different types of transistor structures were proposed, and among these thin-film transistors (TFT) was one kind that relied only on evaporated thin-film layers to create the device structure [9]. This thin-film form enables opportunities for building a transistor on a variety of substrates. The first demonstration of TFTs utilised a 1-in glass plate as the substrate (see Figure 1.2), and the evaporated cadmium sulfide (CdS) and Si monoxide layers were employed as the semiconductor and the gate insulator, respectively [9]. Just over ten years later in 1973, Thomas Peter Brody and his colleagues demonstrated the first active-matrix liquid-crystal display (LCD) with cadmium selenide (CdSe) TFTs [10].

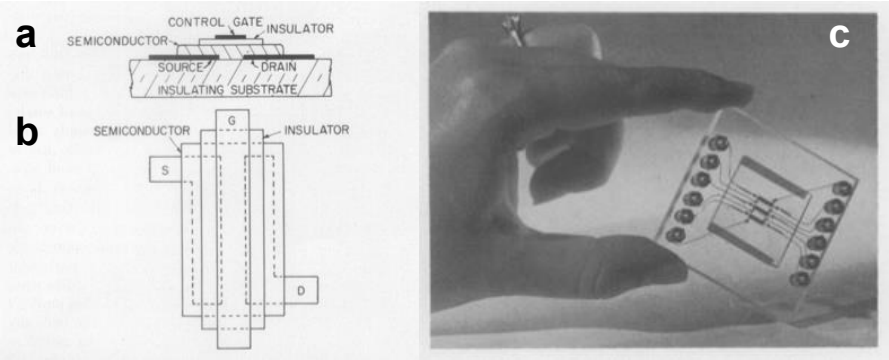


Figure 1.2: (a) Cross-sectional and (b) top views of the first TFT fabricated in 1962 by Paul Weimer. (c) Photo of the CdS TFTs deposited on a 1-in square glass substrate. Adapted from ref. [9], copyright © 1962, IEEE.

The breakthrough for TFT applications was the demonstration of functional TFTs that employed amorphous Si (a-Si) as the active material in 1979 [11]. Apart from its air stability at room temperature, a-Si does not require a complex fabrication process. This material soon gained the attention of numerous major electronic

companies. Flourishing activities in research and development followed with a common goal that was to realise its application in mass production for high-performance flat panel displays. To this day, the display technology has since been the most important application for TFTs, and in the 1980s large-area, colour TFT LCDs were successfully mass produced [12].

Due to the flexibility of TFT compositions and processing, there are many more choices in selecting semiconductor materials for transistors when compared to conventional crystalline semiconductor families. In 1987, Koezuka et al. demonstrated the first organic TFT on silicon wafers using polymer of thiophene molecules as the active material whilst the resulting hole mobility was measured of 2 × 10^{-5} cm^2/Vs [13]. This work has inspired many scientists to dedicate themselves to the development of new organic materials with better charge-transport properties in order to achieve higher electrical performance for practical applications [14-16]. In 2014, Yuan et al. reported organic TFTs based on a blend of C8-BTBT and polystyrene, exhibiting an average hole mobility of ~25 cm^2/Vs — a value around 20 times higher than that obtained from a-Si TFTs [17]. Moreover, scientists and researchers in Interuniversity Microelectronics Centre (IMEC, Belgium) and Holst Centre (The Netherlands) together developed a first organic-based 8-bit flexible microprocessor (see Figure 1.3) [18].

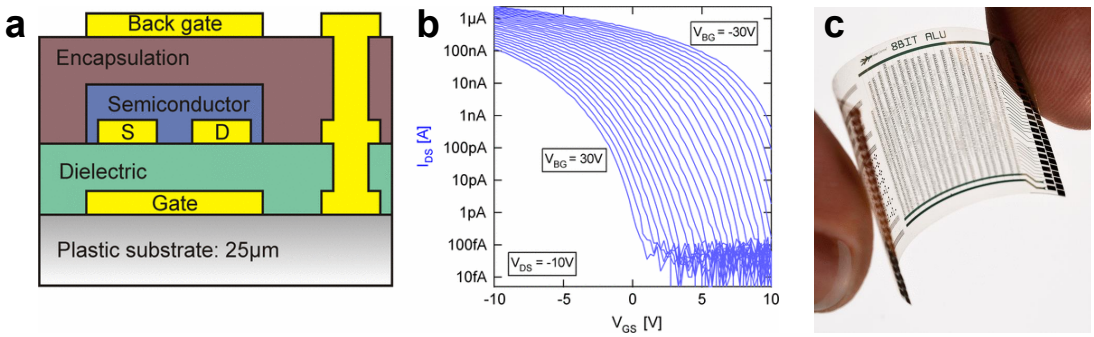


Figure 1.3: (a) Cross-sectional view of a dual-gate organic TFT whilst the current-voltage characteristics shown in (b). (c) Photo of an 8-bit organic-based arithmetic and logic unit on a plastic foil. Adapted from ref. [18], copyright © 2012, IEEE.

However, the extensive development in organic-based TFTs is yet to make their way into the consumer electronics market mainly because of the poor

environmental stability. The rapid growth of materials science and nanotechnology has advanced the discovery and invention of many more interesting materials in the last two decades. Another promising material family are the carbon-based materials: fullerene and graphene. Carbon-based field-effect transistors (FETs) were realised between the end of the twentieth century and the beginning of the twenty-first century: With C_{60}/C_{70} fullerene FETs in 1993 [19], carbon nanotube FETs in 1998 [20, 21] and graphene FETs in 2004 [22]. The operations and structures for carbon-based transistor are the same as those for a TFT, and their applications in the field of field-effect devices show tremendous electrical performance and properties [23-25], greatly overshadowing other materials used for TFTs. Even a conceptual carbon-nanotube based "computer" was demonstrated in 2013 by researchers in Stanford University [26].

At nearly the same time as the discovery of the first two-dimensional material based transistor — i.e. graphene FETs — post-transition-metal oxides, such as zinc oxide (ZnO) [27] and indium-gallium-zinc oxide (IGZO) [28, 29], were demonstrated in TFT applications in the early 2000s. These oxide TFTs exhibit many attractive features, including high transparency across the visible spectrum, large electron mobility (>10 cm^2/Vs), simplicity in their fabrication process, potential for mass production and importantly, high stability under atmospheric conditions. Similar attractive properties were also found in a-Si based TFTs during their discovery, which eventually led to a-Si becoming the 'go-to' material during the flat panel display technology boom during the first decade of the twenty-first century. As expected, major electronics and chemicals companies are now involved in researching and developing oxide-based technologies for their applications in display panels. Indeed, only few years after their invention, the first oxide-based display was produced for the mass market [30]. The display industry has again been revolutionised, and the success of oxide TFTs possibly demonstrates one of the most rapid transfer of academic/fundamental research works to mass-produced electronic products in human history. To sum up this information from a transistor-relevant standpoint, the milestones for early transistor history and TFT related developments are shown in Figure 1.4.

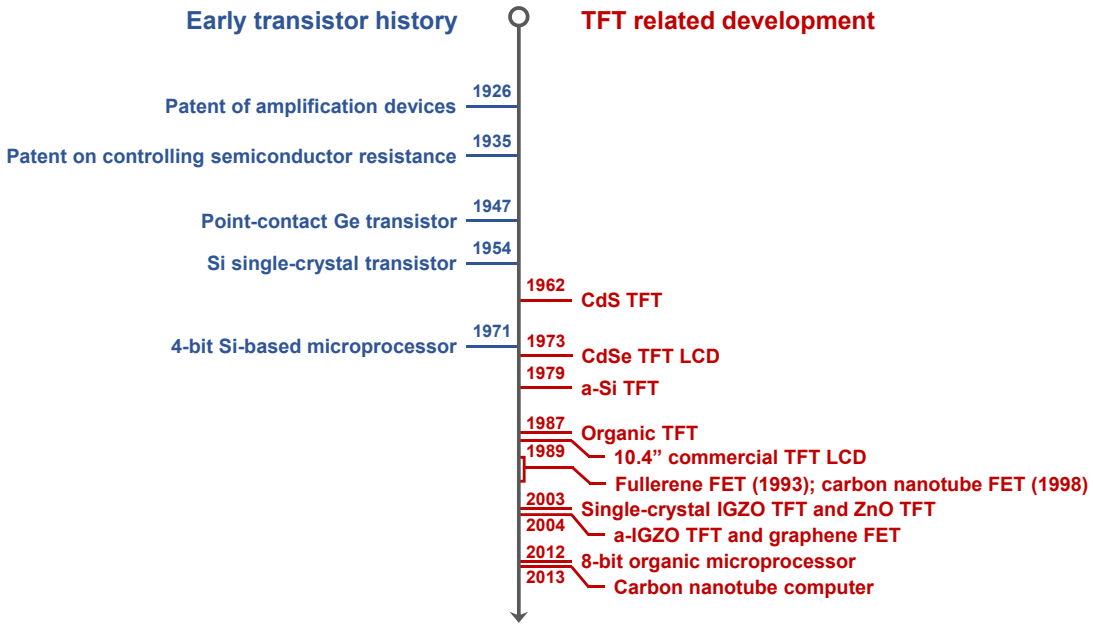


Figure 1.4: Timeline and milestones for early transistor history and TFT related development.

The flexibility in TFT compositions also gives rise to several different types of geometric configurations in their device architecture. This unique property provides the possibility for a range of potential electronic applications beyond display technologies. By choosing suitable functional semiconductors, dielectrics or even electrode materials for target applications, all in combination with applicable device geometric configurations, TFTs offer overwhelming opportunities for a variety of applications — some examples are listed here in Table 1.1.

Table 1.1: List of several non-display applications using different areas of a TFT and primary working principles for each application.

Functional area	Application	Working principles
Device structure	LEFET [31]	Hybrid materials with source-buried configurations
	Memory [32]	Floating-gate configurations
Gate electrode	Sensor [33]	Electrolyte-gated devices
Gate dielectric	Memory [34]	Ferroelectric dielectric materials
Semiconductor	Sensor [35, 36]	Functional materials in response to external stimuli
	Photodetector [37, 38]	Fermi-level engineering/dye-sensitised semiconductors
	Spin valve [39]	Single-molecule magnets
Source/drain electrode	DNA Sensor [40]	Contact resistance modification

1.2 Motivation

As far as TFT technology goes, the development of semiconductor materials is still the most essential element in obtaining a highly-functional device, which is critical in all types of applications. To date, only few years since their initial functional suitability has been accomplished, the excellent electrical characteristics of oxide-based semiconductors have led them to outperform the performance of incumbent technologies such as a-Si and they are fast approaching that of polycrystalline Si (poly-Si). Recently, high-end display panels based on the use of oxide TFTs have been demonstrated and mass produced for the consumer electronics market. The constant drive toward the next-generation of high-definition, large-area displays has driven the display industry to search for increasingly cost-effective fabrication methods to replace the existing expensive vacuum-based techniques. Importantly, although the latter may provide the performance advantages, vacuum-based methods are limited when it comes to the development of new materials with a step-change in their performance characteristics. To this end, solution-based fabrication methods are now starting to receive increasing attention for the synthesis of oxide semiconductors.

Solution-processable oxide precursors have the potentials to offer low-cost fabrication due to the requirement for less restrictive deposition environments [41, 42]. The early development on solution-grown ZnO TFTs showed an electron mobility of 85 cm^2/Vs [43, 44], a value close to that can be obtained from poly-Si TFTs. However, to achieve such high performance, a thermal calcination process of >400 °C is required. The latter largely limits the processability of solution-grown oxide materials in TFT applications for "unconventional" flexible displays (e.g. e-paper) and other flexible electronic products. As listed in Table 1.1, many of these potential TFT applications (e.g. sensors and other disposable electronics) requires an inexpensive manufacturing process to maintain their viability in terms of cost, yet at the same time not compromise their electrical properties. The use of flexible substrates not only reduces material costs but also opens up possibilities allowing us to bring technology into every corner of daily life. Therefore the primary goal in this work is to develop an oxide-based material system that can address the needs of low-cost large-area flexible electronics. In doing so, the benefit of this work need not be

limited to conventional high-end displays, but will also be advantageous to a whole new range of unconventional flexible electronic applications capable of enhancing our everyday lives.

1.3 Thesis outline

This thesis focuses on the development and study of low-temperature solution-processed metal oxide TFTs that are compatible with temperature-sensitive inexpensive substrate materials, such as plastic. To this end, the general requirement for processing onto such temperature-sensitive substrates is to maintain the critical precursor conversion temperature to <200 °C without compromising the electrical performance of the resulting devices.

Following this introductory chapter, Chapter 2 offers an overview of the theoretical foundation for commonly used semiconducting oxide materials. It starts with band structures of post-transition-metal oxides, and the mechanism for charge transport in oxides is given in detail. This chapter finishes with a brief explanation of working principles of TFTs. Chapter 3 describes the electrical and material characterisation techniques employed in this work as well as the experimental methods used for film deposition and device fabrication.

Chapters 4–7 comprise the bulk of this research and reports key experimental findings in the area of low-temperature solution-processed oxide TFTs. A brief conclusion is also given at the end of each chapter. The content in each chapter is specifically explained as follows.

Chapter 4 describes nanocrystalline ZnO-based TFTs fabricated using a photochemical process, which enables realisation of functional transistors at room temperature. Trap density analysis for these films and devices, reveals the limitations on performance in these ZnO TFTs. To overcome the identified materials bottlenecks, a nanocomposite concept is proposed and implemented.

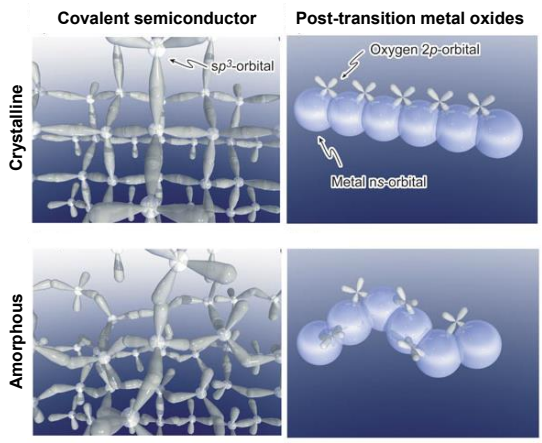
Chapter 5 reports on an aqueous-based zinc-ammine complex approach used for the growth of high quality ZnO layers and TFTs. As-prepared TFTs exhibit a maximum electron mobility exceeding 10 cm^2/Vs at process temperatures <180 °C. In

addition, a UV-irradiation process is explored to effectively convert the ZnO precursor without the need for any thermal-annealing step. Furthermore, a low-temperature hybrid high-κ dielectric is developed enabling the demonstration of low operating voltage ZnO TFTs. The aqueous-based approach is further extended in the work described in Chapter 6. In the latter chapter, a simple, facile aluminium (Al) doping process is proposed and implemented for thin layers of ZnO. Transistors based on Al-doped ZnO layers exhibit enhanced electrical performance highlighting the potential of this method. Extensive material characterisations provide insight into the evolution of ZnO microstructure as a function of Al-doping concentration.

Chapter 7 presents a novel TFT concept that exploits the enhanced electron transport properties of low-dimensional polycrystalline multi-layer oxide systems processed from solution. The multi-layer systems are composed of alternating layers of In_2O_3, Ga_2O_3 and ZnO grown at temperatures <200 °C. Importantly, oxide superlattice-based TFT exhibit dramatically enhanced electrical performance with maximum electron mobility close to 50 cm^2/Vs. The dramatic increase in electrical performance is believed to originate from the formation of low-dimensional electron gas-like systems in close proximity to the carefully engineered oxide heterointerfaces. Temperature-dependent electron transport and capacitance-voltage measurements support this assumption. Finally, Chapter 8 summarises the key results of this research work and provides the outlook for the future work and applications of solution-processed oxide TFTs.

2

THEORY FOR TRANSPARENT METAL-OXIDE SEMICONDUCTORS AND THIN-FILM TRANSISTOR OPERATIONS



In contrast to conventional covalent semiconductors, chemical bonds in transparent oxide semiconductors (TOSs) are significantly ionic, and the conduction band is mainly composed of metal ns orbitals. This highly disperse energy band structure results in electrons with small effective mass, and the charge transport mechanism is dominated by so-called percolation conduction. The tail states winthin the bandgap are found to distribute closely to the conduction band edge. The latter is believed to be the main reason for the excellent transport behaviour observed. In addition to the TOS theory, this chapter also provides an overview of thin-film transistor operation and commonly used methods for extracting key device performance metrics. (Left panel: Illustrations of the semiconductor electron orbitals. Adapted by permission from Macmillan Publishers Ltd: Nature [29], copyright © 2004.)

2.1 Electronic structure of transparent metal oxides

2.1.1 Band structures

Transparent conductive materials have two characteristics that appear to be contradictory to each other. A transparent material is typically insulating and possesses filled valence and empty conduction bands with a large bandgap, making them transparent across the visible spectrum. However they can be engineered to become metallically conductive when the Fermi level is displaced to within a band where a large density of states (DoS) exists, allowing the generation of a high concentration of mobile charge carriers [45]. For post-transition metal oxides to fulfil these requirements, a stoichiometric insulating oxide host [see Figure 2.1(a)], e.g. In_2O_3, ZnO and SnO_2, needs to be highly-doped to lift the Femi level above the conduction band minimum (CBM) [see Figure 2.1(b)] [46, 47], giving rise to the term, transparent conductive oxide (TCO). Degenerate doping in oxide material with highly-dispersed conduction bands enables the high mobility of charge carriers and small effective masses, with low optical absorption, owing to its DoS distribution [45, 48]. In addition, the nature of these highly-dispersed energy bands leads to the Fermi level displacement well beyond the CBM — i.e. the Burstein-Moss band-filling effect [49, 50], which increases the broadening of optical bandgap [Figure 2.1(b)].

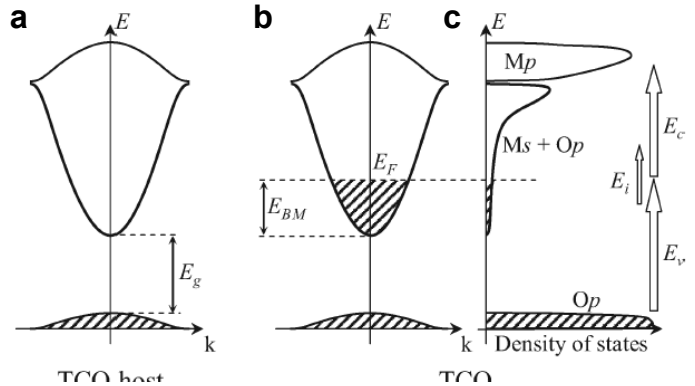


Figure 2.1: (a) Schematic of band structure of an insulating oxide host with a bandgap E_g. The highly-dispersed band structure originates from interactions between metal *ns* and oxygen *2p* orbitals. Schematic of (b) band structure and (c) density of states of a degenerately-doped oxide material, where E_F is the Fermi level, and E_{BM} indicates a Burstein-Moss shift. Three possible optical absorption mechanisms include two types of inter-band optical transitions — from the state within the valence band E_v or the partially-filled conduction band to the next available energy state, and one intra-band transition within the conduction band E_i. Adapted from ref. [45] with permission from John Wiley and Sons, copyright © 2010.

On the other hand, the large carrier concentrations needed to acquire high conductivity can also result in the reduction in optical transparency because of the inter-band optical transition from the partially-filled conduction band and the intra-band transition within the conduction band [Figure 2.1(c)]. The former could cause an increase in optical absorption at shorter wavelengths whilst for the latter optical absorption may increase at longer wavelengths. Plasma oscillation can also affect the absorption spectra under plasmon frequency, which is in the far-infrared or mid-infrared spectra for semiconductors with doping level in the range of $n = 10^{17}$~10^{20} cm^{-3} [51]. Nevertheless, for oxide transistors a moderate number of charge carriers, i.e. $n = 10^{17}$~10^{18} cm^{-3}, are required in order to maintain semiconducting properties and, hence, provide feasible electrical current modulation [52-55]. For transparent semiconducting metal-oxide materials, namely transparent oxide semiconductor (TOS), neither of these aforementioned optical absorption mechanisms is likely to be observed in the studies presented in this thesis. Importantly, although semiconducting amorphous/polycrystalline metal oxide will be the focus of this thesis, the crystalline electronic structures discussed here still provide valuable insight owing to their similarity (see below for further information).

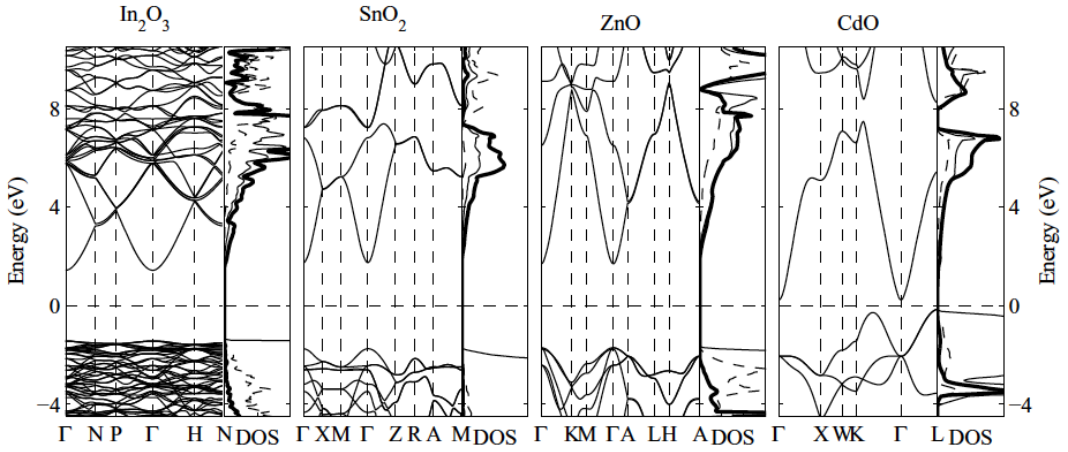


Figure 2.2: Band structures and partial density of states of In_2O_3, SnO_2, ZnO and CdO obtained using screened-exchange local-density approximation method. Adapted from ref. [45] with permission from John Wiley and Sons, copyright © 2010.

A distinct part of a TOS material is that its ionicity results in electronic structures different from Group IV semiconductors that are based on covalent bonds. The difference in electronegativity and ionisation energies of the metal and oxygen

atomic species induces charge transfer from the metal to the oxygen atoms and results in electrostatic potentials, forming chemical bonds with the significant contribution of ionic character. Most of TOS materials are oxides of the heavy post-transition metals with electronic configurations of $(n-1)d^{10}ns^2$ in which strong interactions between the metal *ns* and oxygen *2p* orbitals giving rise to the formation of similar band structures as shown in Figure 2.2. The CBM is formed by the antibonding between metal *ns* and oxygen *2p* states [see Figure 2.1(c)] whilst the bonding and nonbonding oxygen *2p* states lead to the formation of the valence band maximum (VBM). As such, the energy difference in bonding states opens a large bandgap, which is transparent to the visible spectrum. Furthermore, the empty *p* states of metal ions account for the formation of the bands at higher energies.

The electron transport paths are determined by the electronic structure of the conduction band. The largest M*s*–O*p* overlap is obtained when the octahedral molecular geometry is formed by coordinating the oxygen atom with the metal cations [see Figure 2.3(a)]. However, owing to the spherical symmetry of the cation *s* orbitals there is only minor effect on the M*s*–O*p* overlap even if some variations appear in the oxygen coordination that cause structural distortions and result in polyhedral-like configurations [Figure 2.3(b)]. As a result, there is no significant change observed in effective electron mass (m_e^*) of TCOs (≤15%) [45]. This M*s*–O*p* network that is insensitive to atomic structures can ensure small m_e^*, which leads to the successful electronic applications using non-crystalline TOS materials. In particular, optical and electrical properties in the amorphous state have been observed remaining similar to those measured in the crystalline state [28, 29, 52].

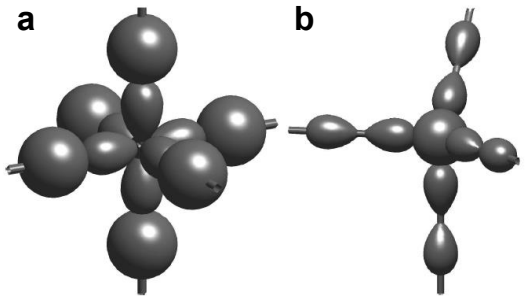


Figure 2.3: (a) Illustration of octahedral coordination of oxygen atoms by cations shows the largest M*s*–O*p* overlap. (b) Illustration of coordination of cations by oxygen atoms with the existence of local distortion. Adapted from ref. [45] with permission from John Wiley and Sons, copyright © 2010.

In the case of non-crystalline TOS materials it is also widely accepted that the spatially extended metal *ns* orbitals in a spherical shape induce larger overlaps between the neighbouring metal orbitals (see Figure 2.4) [52, 56]. Such a result causes the electronic structure to form favourable transport paths for electrons, regardless of the crystalline state and as long as the number of constituent cations can overcome the percolation threshold [29, 57]. However, in TOS m_e^* is known to be nearly isotropic whether from theoretical calculation and experimental observation, indicating the *s–s* interactions might not be the only factor to dominate the charge transport [45]. Nevertheless, the exact relations between charge transport and electronic band structures still require further studies to clarify. This thesis adopts the viewpoint of the overlap between metal *s* orbitals resulting in small m_e^* and effective charge-carrier pathways for analysis of the TOS charge transporting properties hereafter. This is because numerous successful non-crystalline TOS-based transistors have been demonstrated [41], and the proposed percolation model explains the characteristics of charge transport well [52-55].

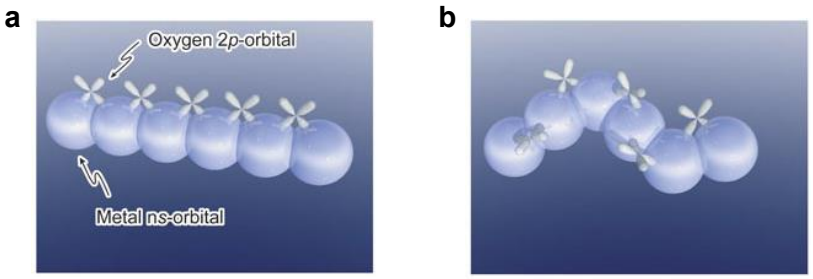


Figure 2.4: Illustration of orbitals for (a) crystalline and (b) amorphous post-transition metal oxides. The formation of direct overlap between neighbouring metal *ns* orbitals could contribute to electron pathways, even in an amorphous structure. Adapted by permission from Macmillan Publishers Ltd: Nature [29], copyright © 2004.

In contrast to the conventional TCO/TOS materials, oxides of light post-transition metals, e.g. Al and Ga, the CBM is influenced by interactions not only between metal *s* and oxygen *p* states but also the metal *p* or *d* states. The latter is energetically suitable for the doping-induced electrons to form strong bonding with the states of the neighbouring oxygen atoms. Therefore, such strong localisation behaviour eventually results in the insulating properties of light post-transition metal oxides.

2.1.2 Carrier generation

The main content of this section is based on the seminal work by Lany and Zunger [58], who extensively studied the origin of conductivity in transparent metal oxides via formation energy ΔH derived from first-principles calculations. To date, a widely-accepted concept for intrinsic metal oxides, such as In_2O_3 and ZnO, is that they possess high conductivity because of the existence of native point defects, such as oxygen vacancies (V_O) or cation interstitials (In_i or Zn_i). Figure 2.5 shows defect and carrier (electron) densities for In_2O_3 and ZnO under two different growth conditions: (i) the chemical potentials $\Delta\mu_{In} = 0$, $\Delta\mu_{Zn} = 0$ for the metal-rich conditions; (ii) oxygen pressure $p(O_2) = 1$ atm and $\Delta\mu_O = 0$ for the oxygen-rich (i.e. O-rich) conditions. It is clear that oxygen-deficient non-stoichiometry, i.e. V_O, is the most abundant point defect in both In_2O_3 and ZnO under the equilibrium growth conditions. For In_2O_3 the concentration of V_O is around $\sim 2\times10^{20}$ cm^{-3}, i.e. 0.4 % of the oxygen lattice site, at 1673 K whilst the V_O concentration in ZnO is $\sim 4\times10^{19}$ cm^{-3} (0.1 %) at 1373 K. Both of these calculated results have shown good agreement with the experimental data reported in the literature [59-62].

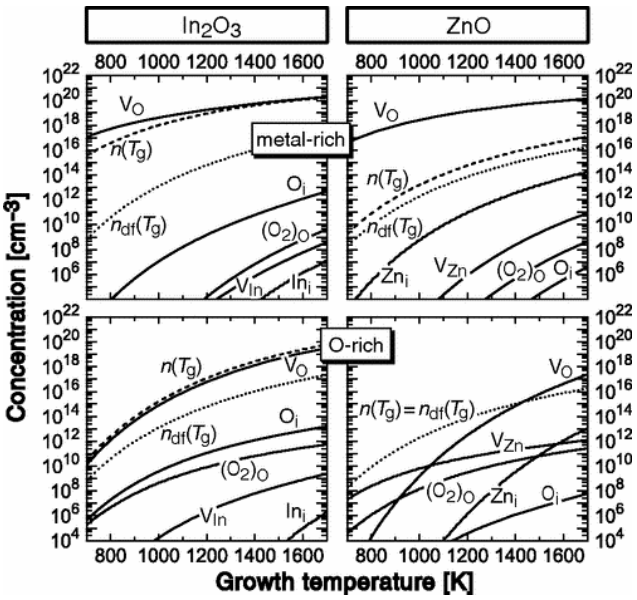


Figure 2.5: Calculated defect and electron (n) densities as a function of growth temperature T_g for In_2O_3 and ZnO. The thermal-excited electron density $n_{df}(T_g)$ is shown for comparison. Reprinted figure with permission from ref. [58]. Copyright (2007) by the American Physical Society.

It should be noted that the calculated electron density at room temperature is very low for both In_2O_3 (<10^{14} cm^{-3}) and ZnO (<10^{7} cm^{-3}). The reason for this is attributed to the fact that V_O generally lies at a deep level within the bandgap so that it cannot generate free charge carriers (see Figure 2.6). On the other hand, the formation of stable metal-metal bonds between the In or Zn cations neighbouring V_O results in the lower formation energy of the oxygen vacancies [63]. In contrast to this, the high formation energy for cation interstitials is because the electrons introduced by In_i or Zn_i occupy a shallow level located close to the CBM. The latter leads to a large formation energy when E_F is displaced to higher energies within the bandgap (see Figure 2.6). As a result, the cation interstitials become extremely insufficient whilst oxygen vacancies increase to around ~10^{20} cm^{-3} (see Figure 2.5). On the basis of the simulation data, the intrinsic point defects cannot cause n-type conductivity in In_2O_3 and ZnO under the equilibrium conditions. In spite of this, one should also note that metastable V_O can still be induced to generate significant persistent photoconductivity under the equations of $V_O \rightarrow V_O^{+} + e$ and $V_O^{+} \rightarrow V_O^{2+} + e$. The process only requires photon energies of 1.6–1.8 eV and 2.4–2.8 eV for In_2O_3 and ZnO, respectively [63].

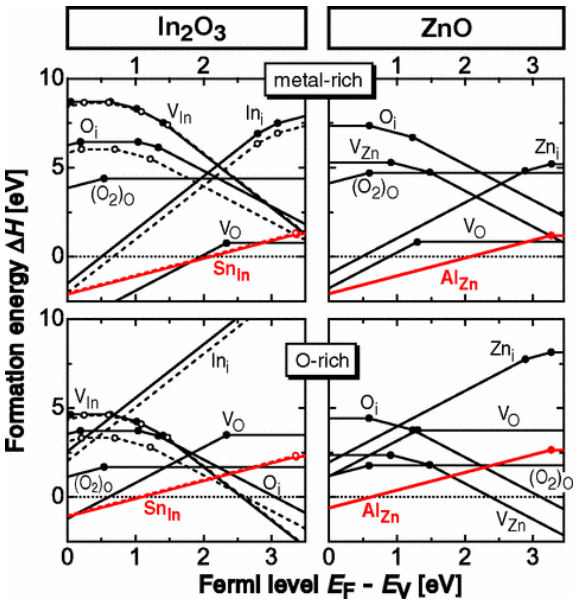


Figure 2.6: Calculated defect formation energy as a function of E_F. The dots mark the transition energies between different charge states. The metal-rich and oxygen-rich conditions were taken under $\Delta\mu_{In} = \Delta\mu_{Zn} = 0$ and $\Delta\mu_O = 0$, respectively. Reprinted figure with permission from ref. [58]. Copyright (2007) by the American Physical Society.

Although intrinsic defects do not likely lead to the formation of abundant donors as predicted by the theoretical analysis, Hall-effect measurements have however shown oxygen deficiency plays an important role for charge carrier generation [53, 64]. Figure 2.7 shows the impacts of partial oxygen pressure during the deposition processes on the carrier concentration in two TOS systems: amorphous $InGaZnO_4$ (a-$InGaZnO_4$) and amorphous $In_2Zn_3O_6$ (a-$In_2Zn_3O_6$) [52]. It can be clearly seen that the carrier concentrations are reduced with increasing oxygen pressure in both of the TOS systems. This finding indicates oxygen deficiency is indeed closely-related to carrier generation and hence conductivity in such TOS materials. More interestingly, the carrier concentration in a-$InGaZnO_4$ dramatically decreases to $<10^{13}$ cm^{-3} under oxygen pressure of 8 Pa whilst it remains at around 10^{18} cm^{-3} in a-$In_2Zn_3O_6$ using the same deposition condition. It is therefore suggested that incorporation of Ga^{3+} can effectively suppress carrier generation owing to its smaller ionic radius and +3 valence as mentioned in the previous section.

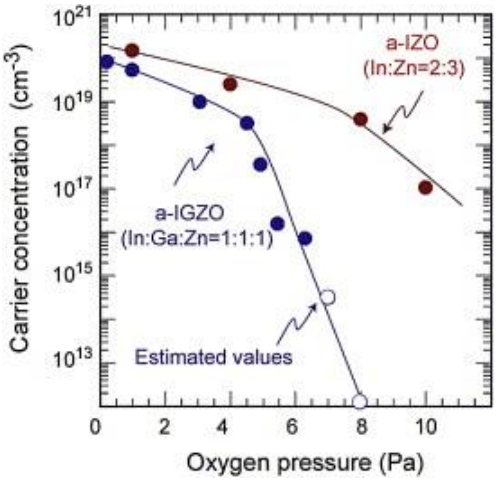


Figure 2.7: Carrier concentration as a function of partial oxygen pressure during the depositions for a-$InGaZnO_3$ and a-$In_2Zn_3O_6$. Reproduced from ref. [52] with permission from Elsevier, copyright © 2006.

To generate a large number of charge carriers, an important strategy is to introduce extrinsic dopants. As shown in Figure 2.6, Sn and Al can be used for doping In_2O_3 and ZnO, respectively since both Sn_{In} and Al_{Zn} play a role as shallow donors. In Figure 2.8, the doping concentration remains unchanged under a wide range of oxygen pressures during the growth for In_2O_3 (i.e. electron densities ≈ Sn

concentrations) whilst in ZnO the doping effect is not compensated under metal-rich conditions. However, for the latter a significant compensation effect takes place under oxygen-rich conditions owing to the strong formation of Zn vacancies V_{Zn} (Figure 2.8). On the other hand, although oxygen interstitials O_i are also considered to be detrimental to electron generation, this phenomenon is insignificant due to their high formation energy (Figure 2.6).

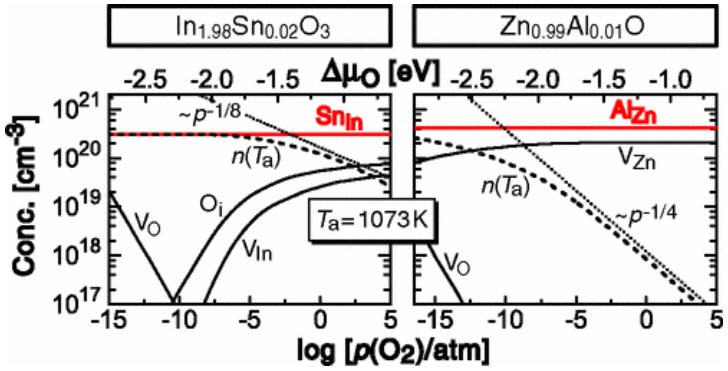


Figure 2.8: Carrier (electron) densities and defect concentrations for In_2O_3:Sn and ZnO:Al under different oxygen pressures at growth temperature T_a = 1073 K. The thermodynamic simulations are constrained to a constant doping level of 1%. Reprinted figure with permission from ref. [58]. Copyright (2007) by the American Physical Society.

2.2 Charge transport in transparent conductive oxide

2.2.1 Conduction pathway and percolation threshold

Today's enormous success of the applications of TOS in consumer electronics is achieved by dedicated material and device engineering. Before the seminal works reported by Hosono's group in Tokyo Institute of Technology in 2003 and 2004 [28, 29], the optimisation process of the constituent elements for optimal material design had been thoroughly studied by the same group in order to achieve efficient charge transporting properties [57]. Since these properties are closely-related to the electronic structures of a TOS material to begin with, the effectiveness of charge transport is investigated through the point of view of the CBM compositions in heavy post-transition metal oxides. The latter is known to possess $(n-1)d^{10}ns^2$ electronic configurations, in which the CBM is mainly governed by metal *s* orbitals. In a

disordered system, i.e. amorphous materials, the early findings suggested that only cations with 5*s* orbitals showed good conductivity, such as amorphous In_2O_3 and Cd_2SnO_4 [57]. This was attributed to the larger 5*s* orbitals that can form effective conduction paths whilst oxides with 4*s* orbitals failed to deliver similar performance owing to the smaller orbital radius [see Figure 2.9(a)].

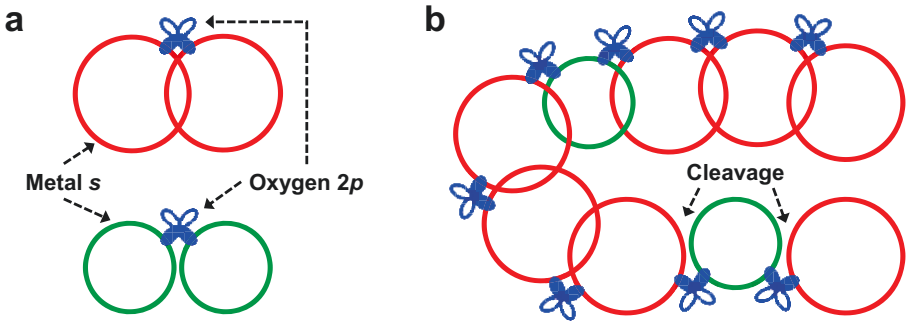


Figure 2.9: (a) Overlap of *s* orbitals of post-transition metal oxides shown in M–O–M bonds, where M and O denote the metal and oxygen, respectively. The larger red circles are metal 5*s* orbitals whilst the smaller green circles are displayed for metal 4*s* orbitals. Pairs of ellipsoids represent the oxygen 2*p* orbitals. (b) Conduction pathways in multicomponent $InGaO_3(ZnO)_m$, where cleavages are shown as a result from the use of light metals [57].

In order to explore whether the 4*s* orbitals of Zn cations can act as conduction paths in multicomponent metal oxide structures [$InGaO_3(ZnO)_m$], Orita et al. studied amorphous $InGaO_3(ZnO)_m$ by limiting the content of In ions in the range of 8–14 %, which are below the percolation threshold (20 %), i.e. not sufficient to form conduction paths (hence good conductivity) from In components [57]. It should be noted that the percolation threshold of 20 % is obtained from the calculation for close-packed face-centred cubic systems [65]. The overlap of orbitals of $InGaO_3(ZnO)_m$ is then illustrated in Figure 2.9(b), in which the possible existence of cleavages due to the use of the metal with 4*s* orbitals is considered to be detrimental to charge transport. However, the electrical characterisations still showed that good conductivities of 170–400 S cm^{-1} was obtained with Hall-effect mobilities of 12–20 cm^2/Vs and carrier densities of 10^{19}–10^{20} cm^{-3} in amorphous states, i.e. $m \leq 4$ for $InGaO_3(ZnO)_m$. A better understanding of this finding was acquired using the calculations for overlap of n*s* orbital wave-functions. The latter showed a threshold of 0.4 for the overlap integral as the criterion for obtaining good conductivity. The value obtained for Zn 4*s* orbitals was found to be beyond this criterion for M–O–M bond

angles in a wide range of 80°–140°. Such a result suggests that Zn 4*s* orbitals can indeed act as effective conduction pathways. The finding presented here ultimately has led to the extraordinary developments on $InGaZnO_4$ based transistors [28, 29] and, hence their use in high-resolution optical displays used nowadays.

One might still be puzzled by the slow progress in developing solution-processed TOS materials as compared to the advances achieved using vacuum-based deposition techniques [41, 42]. To explain this, the overlap for conduction pathways in solution-based oxides is better illustrated in Figure 2.10, where residual impurities and/or environmental impurities are displayed. The latter is considered to be the main obstacles to the formation of effective charge transport in the final film formation stage. In addition, the interplay between the chemicals during precursor decomposition and film formation increases the difficulties in developing an ultimate solution-based oxide recipe for electronic applications. As such, if the research community is to put forward a solution-processable technology, solution-processed metal oxides still require a lot more effort on material development and processing compared to vacuum-based approaches.

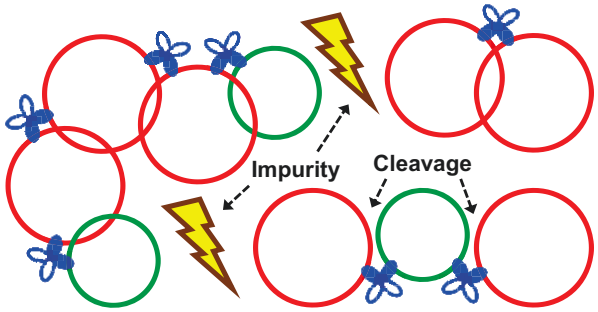


Figure 2.10: Conduction pathways for solution-based post-transition metal oxides in M–O–M bonds. In addition to the existence of cleavages, the impurities from precursors and/or environments are detrimental to the formation of charge transporting routes.

2.2.2 Transport mechanism — percolation conduction

Following the discussion on the formation of conduction pathway in In_2O_3/ZnO based TOSs, the details of the charge-transporting mechanism, i.e. percolation conduction (PC), are studied in this section. In 2004, Nomura et al. studied temperature-dependent charge-transporting properties for single-crystalline $InGaO_3(ZnO)_5$ (sc-IGZO) and polycrystalline $InGaO_3(ZnO)_5$ (pc-IGZO) [66]. The obtained results of

Hall-effect mobilities (μ) and carrier concentrations (N_e) for pc-IGZO and sc-IGZO are plotted in Figure 2.11(a) and (b), respectively. In the case of pc-IGZO, the temperature-dependence for μ can still be observed at $N_e > 2\times10^{19}$ cm^{-3}. In fact, the Fermi level already exceeds the CBM under the condition of $N_e > 10^{18}$ cm^{-3}. As such, the pronounced temperature-dependent behaviour shown in Figure 2.11(a) is attributed to the formation of double-Schottky barriers at grain boundaries, which is commonly observed in polycrystalline semiconductor materials [67-69]. In contrast to this, the condition for sc-IGZO to show temperature-independent behaviour only requires $N_e = 2\times10^{18}$ cm^{-3} [see Figure 2.11(b)]. This observation suggests the grain-boundary limiting effect is not likely to exist in sc-IGZO. Therefore, sc-IGZO could provide a pristine platform for analysing charge transport.

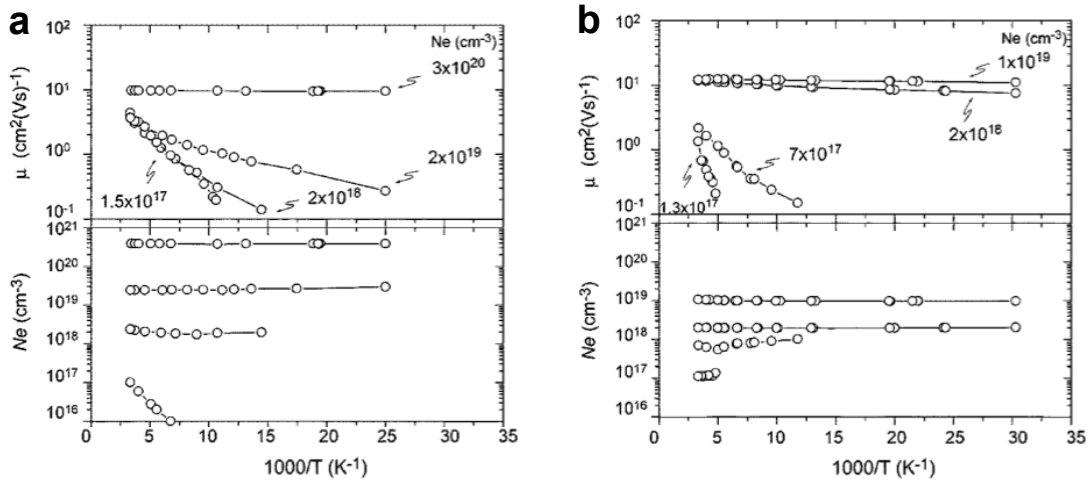


Figure 2.11: Arrhenius plots of Hall-effect mobilities (μ) and carrier concentrations (N_e) for (a) pc-IGZO and (b) sc-IGZO. Reproduced from ref. [66] with permission from AIP Publishing, copyright © 2004.

The analysis of the Arrhenius plots and the dependence of $1/T^{1/4}$ (T: temperature) on conductivity for sc-IGZO seemed to have good agreement with the prediction based on the variable-range-hopping model for N_e in the range of ~10^{17} cm^{-3} [66]. However, the observation of definite Hall voltages in Figure 2.11(b) indicates the charge carriers in the tail states that locate closely to the conduction band edges should not be localised, and the carrier mean free path is much greater than the chemical bond distances [70]. A consistent model that fits the experimental data is the PC in combination with the existence of Gaussian-like potential barriers. Figure

2.12(a) and (b) schematically display the illustration of the energy diagram near the conduction band edges for sc-IGZO and pc-IGZO, respectively. The DoS for the tail states exhibit an exponential decay from the conduction band edge. The energy for the latter is denoted by E_0 in Figure 2.12. The height of the potential barriers, E_σ in Figure 2.12(a), around the conduction band edge leads to PC via "detouring-around-barrier" or "tunnelling-through-barrier" in turn lowering electron mobilities when N_e is obtained of $< 3\times10^{18}$ cm^{-3}, i.e. a threshold carrier concentration N_{th} to trigger degenerate conduction (the corresponding energy denoted by E_{th} in Figure 12). For pc-IGZO, the potential barriers from the grain-boundary effects, i.e. E_σ in Figure 2.12(b), have an influence on charge transport under degenerate conduction (because $E_\sigma > E_{th} - E_F$). The latter results in the thermally-activated behaviour for μ in pc-IGZO as seen in Figure 2.11(a) at high carrier concentrations ($> 10^{18}$ cm^{-3}), in which the Fermi level appears to be higher than the mobility edge.

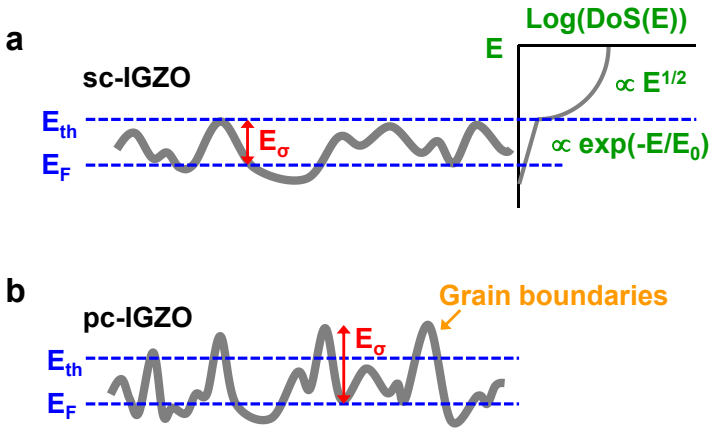


Figure 2.12: Illustration of energy diagram for (a) sc-IGZO and (b) pc-IGZO, where E_F and E_{th} represent the Fermi level, the threshold energy between percolation conduction and degenerate conduction (at the threshold of carrier concentration), respectively. Besides, E_σ is the activation energy required to overcome the maximum potential barrier [66].

Figure 2.13 shows the results of Hall effect measurements for amorphous-IGZO (a-IGZO) reported by Takagi et al. [71]. As seen in sc-IGZO [Figure 2.11(b)], the observation of the definite Hall voltage signals, again, implies that the carriers are not localised in a-IGZO [Figure 2.13(a)]. Besides, no temperature-dependence is observed when $N_e \geq 10^{17}$ cm^{-3} [Figure 2.13(b)]. Figure 2.13(a) also shows clear temperature-activated mobilities μ_{Hall} when N_e equals 10^{17}–10^{19} cm^{-3}. Such a result suggests the existence of potential barriers in a-IGZO that is qualitatively similar to

that in sc-IGZO [see Figure 2.12(a)]. The possible reason could be attributed to that Ga and Zn cations randomly sit in the structural sites and alter the electronic structures, hence, the conduction band edges. It should be noted that since Ga and Zn share the same ionic sites, even in sc-IGZO, the phenomenon of the structural randomness can still be observed [28].

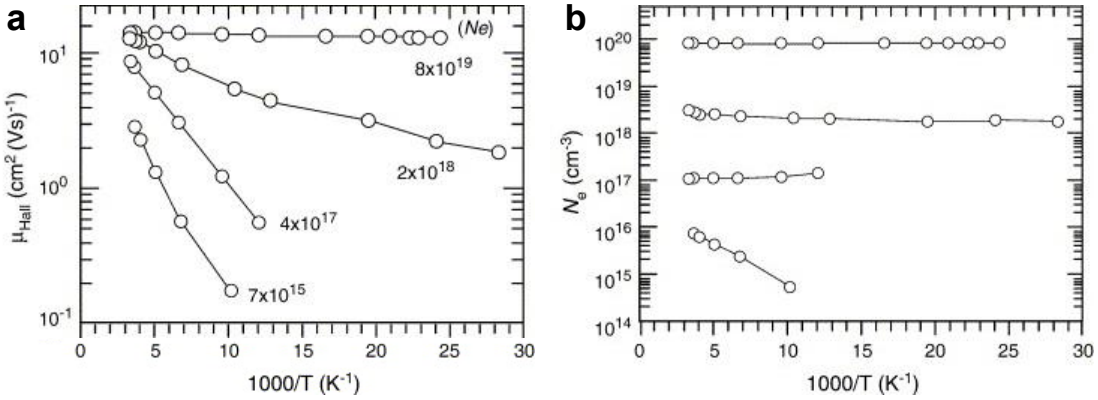


Figure 2.13: Arrhenius plots of Hall-effect mobilities (μ_{Hall}) and carrier concentrations (N_e) for a-IGZO. Reproduced from ref. [71] with permission from Elsevier, copyright © 2005.

Figure 2.14(a) shows the Hall-effect mobilities and carrier concentration for a-IGZO [with different concentrations of constituent elements — Figure 2.14(b)] and crystalline In_2O_3/ZnO [52]. It is evident that In_2O_3 plays a role in determining charge transport as the highest mobility obtained with the highest In_2O_3 content. Most importantly, this result coincides with the assumption of PC for IGZO systems.

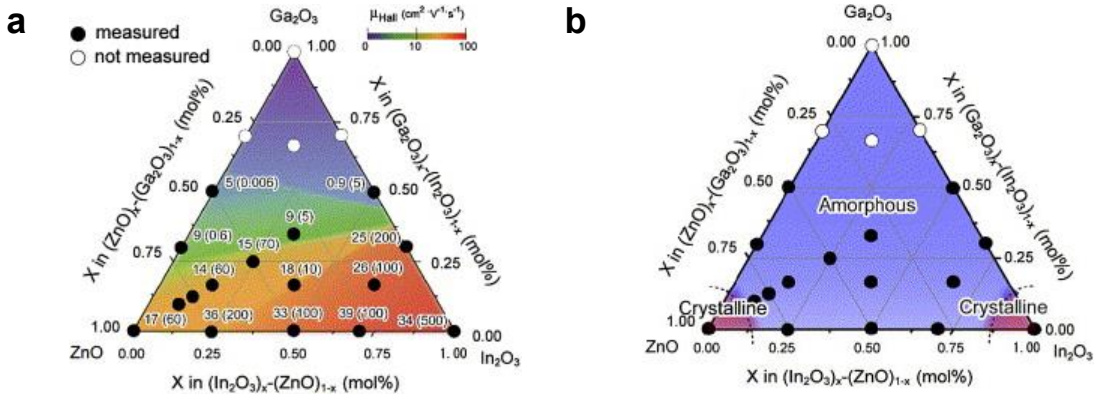


Figure 2.14: Triangular contour maps show (a) Hall-effect mobilities and (b) constituent element concentrations in the amorphous/crystalline In_2O_3–Ga_2O_3–ZnO systems. Number displayed in the parenthesis denotes carrier (electron) concentration ($\times 10^{18}$ cm^{-3}). Reproduced from ref. [52] with permission from Elsevier, copyright © 2006.

2.3 Thin-film transistor operation principles

2.3.1 The linear model

Thin-film transistors (TFTs) are a type of field-effect transistors (FETs) that utilises thin films of active semiconductor materials over a supporting substrate. In comparison the active material in FETs such as metal–oxide–semiconductor field-effect transistors (MOSFETs) generally constitutes part of the substrate. Figure 2.15(a) schematically shows the basic operating principle of a TFT, in which the conductive channel is induced and formed capacitively by applying a voltage V_G to the gate (G). Meanwhile, a small voltage V_D is applied to the drain (D) to collect the charge carriers from the grounded side, i.e. the source (S), via the field-induced channel, resulting in a channel current I_D. Figure 2.15(b) displays a set of typical current-voltage characteristics (namely output characteristics) corresponding to the operations shown in Figure 2.15(a). The linear relations between I_D and V_D can be modulated by V_G so that the channel behaviour is similar to a variable resistor. In other words, the channel resistance is controlled by the voltage applied to the gate.

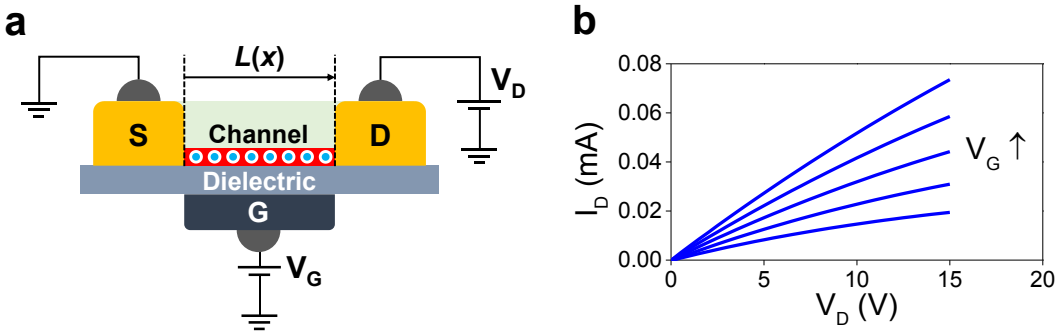


Figure 2.15: (a) Illustration of linear operation for a transistor. A thin slab-like uniform channel is formed when a small V_D is applied (i.e. $V_D \ll V_G - V_T$). (b) Corresponding output characteristics for (a), in which I_D is described by the linear model, i.e. Equation 2.5.

The device behaviour shown in Figure 2.15 is only valid under the conditions of $V_D \ll V_G - V_T$ and $V_G > V_T$, where V_T is threshold voltage for accumulating a sufficient number of mobile charges (electrons) in the channel region to form a

conductive pathway between the source and the drain. The mobile charge Q_{mob} per area is then given by

$$Q_{mob} = C_d(\mathrm{V_G} - \mathrm{V_T}) \tag{2.1}$$

where C_d represents the geometric capacitance of the dielectric layer. Equation 2.1 in fact implies that the field-induced channel is uniform across the entire channel area. This can only exist when the condition $\mathrm{V_D} \ll \mathrm{V_G} - \mathrm{V_T}$ is applied because a larger $\mathrm{V_D}$ increases the channel resistance in the proximity of the drain contact and, hence, results in the formation of a non-uniform conductive channel.

The channel current $\mathrm{I_D}$ can be expressed as the Q_{mob} divided by the travelling time t for the charge carriers to flow from the source to the drain:

$$\mathrm{I_D} = \frac{Q_{mob}WL}{t} \tag{2.2}$$

where L and W are the channel length [along the in-plane direction in Figure 2.15(a)] and width [along the out-of-plane direction in Figure 2.15(a)], respectively. Assuming the velocity v of the carriers is constant, the travelling time t can be written as

$$t = \frac{L}{v}. \tag{2.3}$$

The latter is equal to the product of the mobility μ and the electric field E:

$$v = \mu E = \mu\frac{\mathrm{V_D}}{L}. \tag{2.4}$$

Therefore, by replacing Q_{mob}, t and v in Equation 2.2 using Equation 2.1, 2.3 and 2.4, respectively, the linear model for the $\mathrm{I_D}$ is frequently written in the following form:

$$\mathrm{I_D} = \mu C_d\frac{W}{L}(\mathrm{V_G} - \mathrm{V_T})\mathrm{V_D}. \tag{2.5}$$

2.3.2 The quadratic model

When V_D increases and no longer fulfils the condition of $V_D \ll V_G - V_T$, the channel becomes tapered, and its resistance increases correspondingly [see Figure 2.16(a)]. The local potential at the drain end of the channel is equal to $(V_G - V_T - V_D)$ whilst the source remains grounded. If V_D keeps increasing and reaches $V_D = V_G - V_T$, the channel depth at the drain end eventually becomes zero.

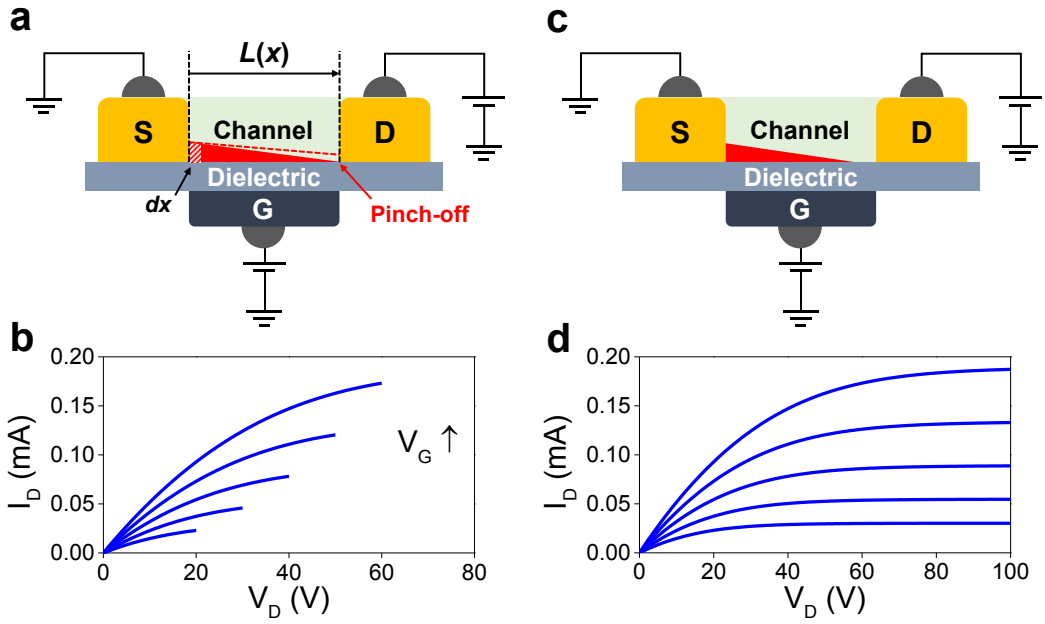


Figure 2.16: (a) Illustration of operating regime for transistors, where a tapered channel formed indicates an increase in channel resistance due to a larger V_D applied. The channel depth can become zero, i.e. "pinch-off", whilst $V_D = V_G - V_T$ is applied. (b) Corresponding output characteristics for (a), in which I_D is defined by the quadratic model, i.e. Equation 2.8. (c) Illustration of transistor operation with even a higher V_D ($>V_G - V_T$) applied — channel pinches off before reaching the drain end. (d) Corresponding output characteristics for (c). I_D remains its maximum, which is the same value as the channel pinches off at the drain end, and can be described by Equation 2.9.

The linear model from Equation 2.5 can be modified to fit the tapered channel shown in Figure 2.16 by considering a small segment *dx* of the entire channel:

$$I_D = \mu C_d \frac{W}{dx}(V_G - V_T - V_C)dV_C \tag{2.6}$$

where V_C is the voltage for the local potential in the channel. Equation 2.6 can be integrated from the source to the drain:

$$\int_0^L I_D dx = \mu C_d W \int_0^{V_D} (V_G - V_T - V_C) dV_C , \tag{2.7}$$

then yielding:

$$I_D = \mu C_d \frac{W}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right]. \tag{2.8}$$

From Equation 2.8, the channel current starts decreasing with a larger V_D applied, as shown in the current-voltage characteristics in Figure 2.16(b). Once V_D increases to a values equal to $(V_G - V_T)$, the channel then becomes "pinched-off" at the drain end [Figure 2.16(a)]. Therefore, a depletion region starts forming from the drain end of the channel if applying a V_D larger than $(V_G - V_T)$ [see Figure 2.16(c)]. However, the formation of the depletion region does not usually cause the decrease in the channel current. Instead, the current reaches its maximum value and maintains that value for higher V_D [see Figure 2.16(d)]. This is attributed to a strong electric field built by V_D in the depletion region between the drain and the end of the channel. As such, the carriers (electrons) can still get swept across from the drain and hence electric current flows even after the "pinch-off" effect. The corresponding operation is generally referred to as the saturation regime. The saturation drain current can then be obtained by replacing V_D in Equation 2.8 with $(V_G - V_T)$,

$$I_D = \mu C_d \frac{W}{L} \cdot \frac{(V_G - V_T)^2}{2}. \tag{2.9}$$

2.3.3 Extraction of key performance metrics

The important TFT performance metrics are linear mobility μ_{LIN}, saturation mobility μ_{SAT}, subthreshold swing *S.S.* and drain (channel) current on/off ratio. These parameters are usually extracted from the TFT I_D–V_G relations by measuring I_D as a function of V_G at a fixed V_D (Figure 2.17). For the condition $V_D \ll V_G - V_T$, μ_{LIN} can be calculated from the gradient of I_D versus V_G using Equation 2.5:

$$\mu_{LIN} = \frac{1}{C_d V_D} \cdot \frac{L}{W} \cdot \frac{\partial I_D}{\partial V_G}. \tag{2.10}$$

Similarly, the saturation mobility μ_{SAT} can be extracted from the second derivative of I_D versus V_G using Equation 2.9:

$$\mu_{SAT} = \frac{1}{C_d} \cdot \frac{L}{W} \cdot \frac{\partial^2 I_D}{\partial V_G^2}. \tag{2.11}$$

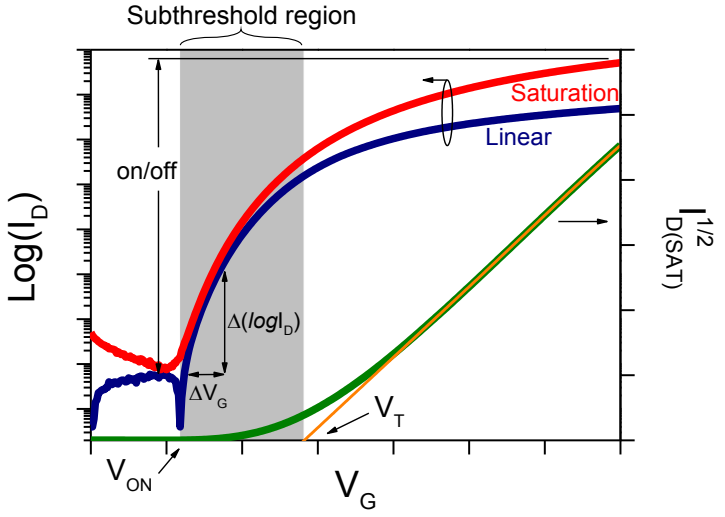


Figure 2.17: Transfer characteristics showing linear and saturation I_D on a logarithmic scale on the left and the square root of the saturation current on a linear scale on the right, as a function of the gate voltage bias V_G. When the transistor is considered to be operating in the on state, V_G is equal to the maximum voltage applied to the device. The onset voltage V_{ON} is when the gate voltage induces abruptly increased I_D from the off state. The subthreshold region is defined by V_G between V_{ON} and V_T. The latter can be obtained by extrapolating the linear fit to $I_{D(SAT)}^{1/2} = 0$.

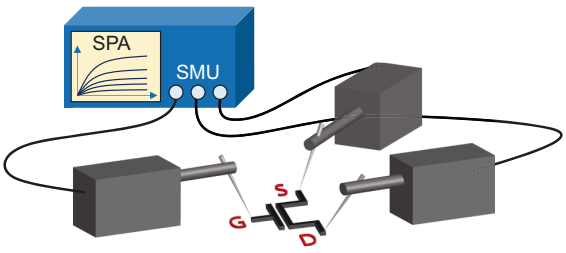
In the semi-log plot of Figure 2.17, the onset voltage V_{ON} for a TFT is when I_D abruptly increases above the off-current level. On the other hand, V_T is obtained by extrapolating the linear fit to the square root of the saturation drain current $I_{D(SAT)}$ to the horizontal axis V_G. As such, the region between V_{ON} and V_T is called subthreshold region, and the corresponding transistor operation is subthreshold conduction. An important device parameter is subthreshold swing *S.S.*, which is defined by

$$S.S. = \frac{\partial V_G}{\partial (log I_D)}. \tag{2.12}$$

Using *S.S.* can give the information regarding trap density, which is closely related to the semiconductor material used in a TFT. The relevant content for this topic will be discussed in the later chapters. In general, a smaller value for *S.S.* is desired for electronic applications since it indicates a fast and distinct transition during the transistor operation. For the on/off ratio in the drain current level, the on-state current mainly depends on the mobility of the semiconductor and the capacitance of the gate dielectric. The magnitude of the off-state current is directly determined by the gate dielectric material used. A robust dielectric material can prevent a large leakage current through itself during transistor operation. However, a higher gate leakage can also be arisen from un-patterned gate electrodes and semiconductor layers, via the conduction pathways at the substrate interface and by the bulk conductivity of the semiconductor, respectively. A transistor with a high on/off ratio is desired for the clean and clear switching behaviour. In general, an on/off ratio of 10^6 are typically needed in TFTs and a large value is often required for their successful usage as electronic switches.

3

Solution-Based Fabrication Process and Characterisation Methods



This chapter describes the deposition techniques used in this thesis and provides an overview of the working principles of several characterisation techniques. For electrical characterisation of transistors, current-voltage characteristics were obtained using semiconductor parameter analyser whilst impedance spectroscopy was used for performing capacitance measurements. Material properties, including optical absorption, morphology, surface potential, surface chemical analysis, crystalline analysis and structural analysis, were acquired using UV-Vis-NIR spectroscopy, atomic force spectroscopy, scanning Kelvin Probe, photoelectron spectroscopy, grazing-incidence X-ray diffraction, X-ray reflectometry, transmission electron microscopy and time-of-flight secondary ion mass spectroscopy, respectively.

3.1 Device fabrication techniques

3.1.1 Spin-coating of thin solid films

To date there are numerous solution-based techniques that have been established and can be used for deposition of a thin film on a substrate [72]. In this thesis, the depositions of solution-processable materials were carried out using a spin-coating technique in which a viscous solution is poured onto a substrate surface, and a (thin) film layer can then be formed by spinning the substrate. The final film thickness is determined by a number of factors, such as the viscosity of a solution, the spin-speed and duration of spin, the ambient conditions of deposition, etc. As such, it is necessary to optimise spin-coating parameters for different materials in order to acquire a smooth and uniform film. For each individual study presented in the later chapters in this thesis, the deposition parameters will be described in detail in each chapter.

Figure 3.1 shows the evolution of material deposition from a solution form to a thin film via a spin-coating process. After pouring the solution onto a substrate surface [Figure 3.1(a)], the solution can be spread over the surface due to centrifugal force during the early stage in the spinning process [Figure 3.1(b)]. In the following, a film starts to form with the ongoing spinning process, and it gets thinner due to the solvent evaporation [Figure 3.1(c)]. After a suitable spinning period, a solid thin film is therefore obtained [Figure 3.1(d)].

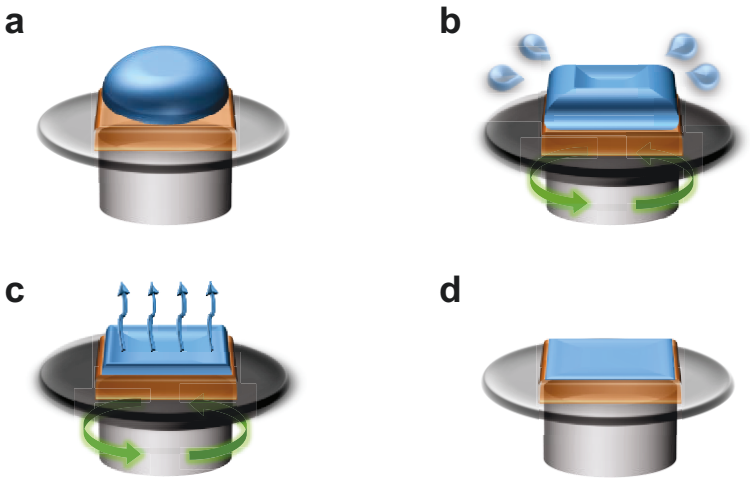


Figure 3.1: Schematic representation of a spin-coating process. (a) Solution is poured onto a substrate. (b) Excess solution is spun off due to centrifugal force. (c) Solvent evaporates during late stage of spinning process. (d) A final solidified thin film is obtained.

It should be noted that the surface tension of a viscous solution can recoil the coating. This effect leads to a film formed thinner at the centre and thicker towards the edge (i.e. an edge bead). Existence of an edge bead could result in changes in the electrical characteristics of a semiconducting film. As such, the measurements presented in this thesis were all performed using devices located at the central area of the substrates to avoid large variation.

3.1.2 Substrate preparation and cleaning procedure

In the present study, the devices were fabricated on either thermally-grown silicon dioxide (SiO_2) on silicon (Si) wafers, glass slides or plastic foils (i.e. flexible substrates). Si wafers <100> were highly n-doped (arsenic, resistivity <0.005 Ω·cm) with SiO_2 of 400 nm ± 5% (Active Business Company GmbH). The former was used as a common gate in transistors with bottom-gate configurations whilst the latter served as gate dielectrics (polished surface, geometric capacitance C_i = 8.6 nF/cm^2). Glass substrates were highly-transparent, thermally-resistive and chemically-durable borosilicate glass (BOROFLOAT®). Plastic substrates were polyethylene naphthalate (PEN, Q65HA) films supplied by Teijin Dupont Films.

The standard cleaning procedure for Si wafer and glass was the same. Prior to spin casting semiconductor layers, substrates were cleaned by ultra-sonication in a solvent bath lasting 10–15 min for four times. The four steps were: (1) sonication in deionized (DI) water with Decon 90 detergent (Decon Laboratories) 1–3% v/v followed by thoroughly washing with DI water to remove Decon 90 from substrates, (2) sonication in DI water, (3) sonication in acetone and (4) sonication in isopropanol (IPA). The residual solvent was then dried by blowing dry nitrogen over substrate surface. For the final step, substrates were subject to an ultraviolet (UV) ozone cleaning process (using UVOCS® model T0606E) for 10–15 min to remove residual hydrocarbons from substrate surface, whilst also improving surface energy for solution-based depositions.

For flexible PEN films, only a rinsing process with DI water and IPA was adapted for their cleaning procedure in order to remove dust particles without causing any damage. The residual water and solvent were dried with nitrogen. The films were

then flattened by a thermal treatment using a pre-heated hot plate at a temperature of ~120 °C. Following the rinsing step, the side with the hydrophilic pre-treatment on PEN films was always kept clean with extra care to ensure smooth, clean and consistent semiconductor depositions.

3.1.3 Metal contact deposition

Thermal evaporation under high vacuum was used to deposit metal contacts onto sample substrates. The evaporated metal vapours pass through shadow masks (made of thin steel sheets) in order to acquire specific patterns. For transistor design, channel lengths and widths were of 20–100 µm and 0.2–1.5 mm, respectively. The deposition process is described in detail hereafter. Samples are loaded into a substrate holder and placed at the top of a vacuum chamber whilst metals to be evaporated are loaded into a source crucible held by a heating element at the bottom of the chamber (see Figure 3.2). The chamber is then pumped down to high vacuum (~5×10^{-6} mbar) to be ready for metal evaporation/deposition. By applying suitable voltages across the heating element, the electrical current slowly increases over a period of ~5 min to avoid damage to the crucible from thermal shock.

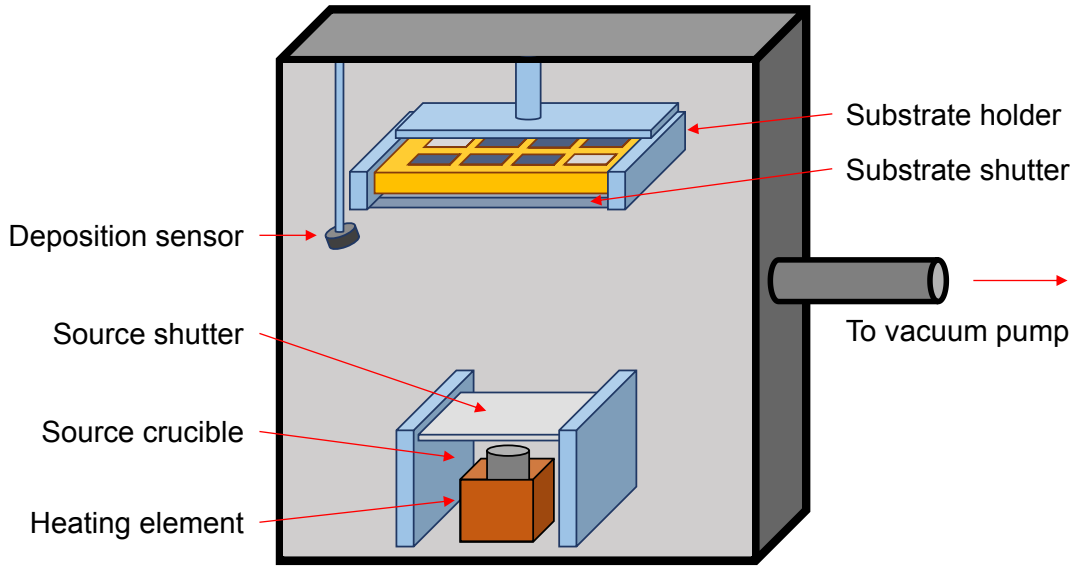


Figure 3.2: Schematic representation of a thermal evaporation system used for the deposition of metal contacts.

After completing this pre-heating step, a crystal sensor monitors the deposition rate and the power supply to the crucible is adjusted accordingly. The current (hence temperature) was controlled using a proportional integral derivative controller. When the evaporation rate reaches the required value (typically around 0.05–0.1 nm/sec), the substrate shutter opens in order to start the deposition. Once the target thickness has been deposited, the substrate shutter is then closed. When using aluminium, the evaporation continues until there is no material left in the crucible. This step is not needed when using gold due to the difference in crucible design. After a cooling period, the chamber is vented with nitrogen to atmospheric pressure, and the samples are then removed from the chamber.

3.2 Electrical characterisation

3.2.1 Current-voltage measurements

The TFT performance is primarily assessed through analysis of experimentally acquired current-voltage measurements. Based on these data, the parameters of interest discussed in Chapter 2 can be determined and/or extracted. To carry out the current-voltage measurements a Keithley 4200-SCS or an Agilent B2902A semiconductor parameter analyser (SPA) was used in combination with a probe station. An SPA is an instrument with a number of source/measure units (SMUs) that can be connected to the terminals of an electronic device and provides simultaneous high accuracy and high resolution current-voltage measurements.

To test an individual TFT, contact is made with the electrodes via a set of micro-positioning needles, in turn connected to the SPA (Figure 3.3). Testing conditions are either under high vacuum (~10^{-5} mbar) or in an inert gas atmosphere (with O_2 and H_2O both <10 ppm), and at room temperature in a dark environment. For temperature-dependent measurements, a cryogenic probe station (Janis ST-500) was used to cool samples with liquid nitrogen under high vacuum (~10^{-5} mbar). The obtained measurement results at each of the SMUs were recorded and saved into a spread sheet file followed by a thorough analysis using Origin (OriginLab).

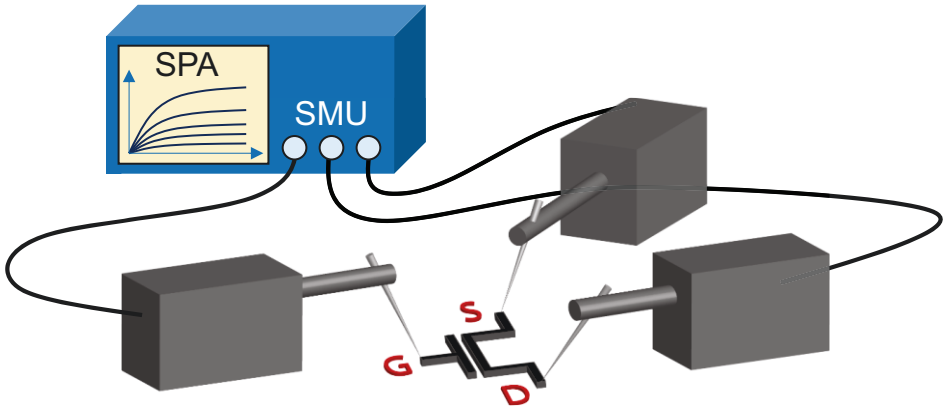


Figure 3.3: Illustrations of current-voltage measurements for a transistor using a SPA. The connections from transistor terminals to SMUs are via micro-position needles.

3.2.2 Capacitance measurement

Impedance spectroscopy is used to determine geometrical capacitance values of gate dielectric layers as well as the charge profiles (distributions) within semiconductor layers. The impedance of a device/circuit is characterised by the difference in phase (δ) between sinusoidal alternating voltages (i.e. $\mathbf{V} = V_0 e^{i\omega t}$ where ω and t are frequency and time, respectively) and currents ($\mathbf{I} = I_0 e^{i(\omega t+\delta)}$). An ideal capacitor is defined as the ratio of the charge ±Q on its terminals to the applied voltage, i.e. $C = Q/V$. After rearranging this equation as $V = Q/C$ and differentiating V with respect to t, the impedance $\mathbf{Z}$ can be obtained as $\mathbf{Z} = \mathbf{V}/\mathbf{I} = -i/\omega C$. By applying a sinusoidal voltage at a fixed current, the imaginary part of the impedance of a circuit measured by an impedance analyser represents the capacitance of the capacitor. The geometric capacitance is therefore obtained using $C_i = -1/A\omega[\mathrm{Im}(\mathbf{Z})]$ in a parallel-plate configuration (where A is the surface area of the plate). On the other hand, in combination with the parallel-plate model for geometric capacitance charge profiles can be obtained using a metal-insulator-semiconductor (MIS) structure with [73]

$$N_{C\text{-}V} = -\frac{2}{\varepsilon\varepsilon_0 A^2 \frac{d(C^{-2})}{dV}} \tag{3.1}$$

as a function of depth (x) within the semiconductor layer:

$$x(\mathrm{V}) = \mathrm{A}\varepsilon\varepsilon_0\left(\frac{1}{\mathrm{C(V)}} - \frac{1}{\mathrm{C_{oxide}}}\right) \tag{3.2}$$

where ε is the permittivity of the semiconductor, ε_0 is vacuum permittivity and C_{oxide} is the capacitance value of the insulator layer.

3.3 Material characterisation

3.3.1 Atomic force microscopy

Atomic force microscopy (AFM) is a technique for determining surface roughness as well as studying surface morphology at the nanoscale. Figure 3.4 schematically shows an AFM system, which is composed of a cantilever, a helium-neon laser and a quadrant photodiode. AFM typically acquires topographic profiles from sample surfaces with an atomically sharp tip at the front end of the cantilever. The topography image is obtained by detecting the deflection of the cantilever. This is done by measuring the reflected laser beam with the photodiode. A feedback mechanism, utilising a piezoelectric actuator is used to control the set point of the cantilever.

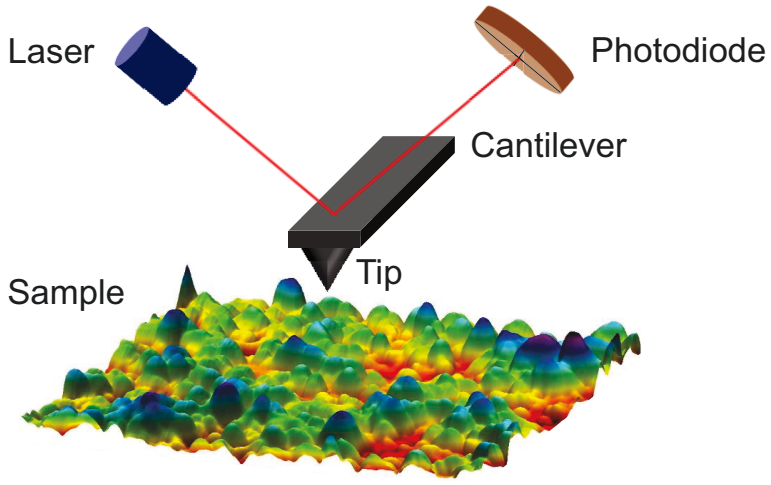


Figure 3.4: Schematic of an AFM system. By irradiating the laser at the front end of the cantilever, the photodiode measures the vertical deflection to provide feedback for the control system. A piezoelectric actuator (not shown) is used to keep the tip at a predetermined set point (i.e. distance in the tapping mode) at the sample surface, and the profile images can then be derived from the drive signals applied to the actuator.

Tapping mode (or AC mode) AFM is one of the most common methods used to image surface topography. In the tapping mode, the cantilever oscillates near to its resonant frequency and is brought down to the vicinity of the surface. The interactions between the surface and the cantilever cause the change in vibrating frequency. As such, a topographical image can be constructed by scanning across the sample surface. Amplitude and phase information of the applied signals can be also obtained to examine the shape and difference of the surface composition. The advantages of tapping mode AFM measurements are a reduced likelihood of damage to the sample surface, and minimising any short-range forces that may cause the tip to stick to the sample surface. In the present study, all the AFM measurements were carried out in tapping mode using an Agilent 5500 AFM in ambient environment. The resonance frequency of the cantilever used was ~325 kHz and the force constant was ~46 Nm^{-1}.

3.3.2 Scanning Kelvin Probe

The working principle of the Kelvin Probe is based on the use of a vibrating capacitor to measure the work function of conducting materials or surface potentials of semiconductor/insulating surfaces in a non-contact and non-destructive manner. Due to the energy differences (i.e. work functions and Fermi levels) between the Kelvin Probe tip and the samples, when electrical contact is made, the equalisation of the Fermi levels results in the generation of electrical charges on the respective surfaces (see Figure 3.5). Therefore, the ability to detect these charges allows the Kelvin Probe to determine surface potentials.

During the measurement, the vibrating tip is typically at a distance of 0.2–2.0 mm away from the sample surface, and an electrical contact is connected to another part of the sample and/or sample holder in order to form the vibrating capacitor. The results obtained from a surface are typically defined by the topmost 1-3 layers of atoms or molecules. The work function is extremely sensitive to surface conditions and is affected by adsorbed or evaporated layers, surface reconstruction, surface charging, oxide layer imperfections, surface and bulk contamination, etc. With this in mind, Kelvin Probe measurements for metal-oxide layers (made on ITO-glass substrates) were performed in a dry nitrogen atmosphere at room temperature right

after the fabrication process in order to minimise these environmental impacts. The specific Kelvin Probe system used in this work was a KP Technology scanning Kelvin Probe system SKP5050.

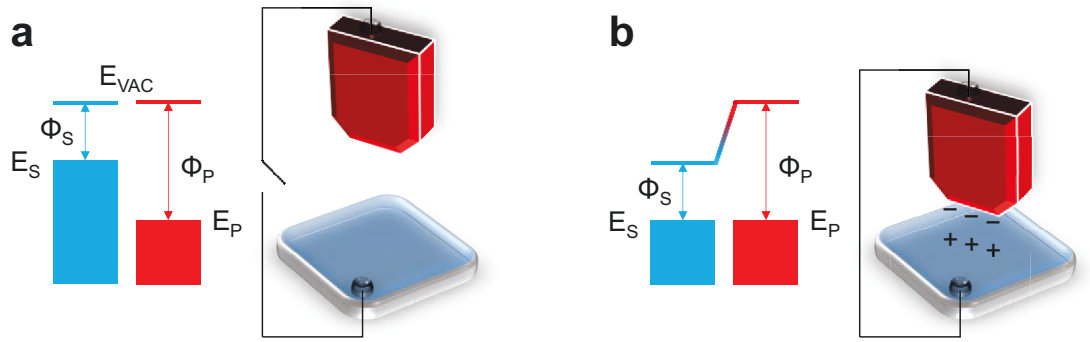


Figure 3.5: Schematic representation of a Kelvin Probe system and energy levels for a Kelvin Probe tip (red) and a sample (blue). (a) displays the tip and the sample with differing Fermi levels before electrical contacts whilst (b) shows the charge flow allows the Fermi levels to equalise and gives rise to surface charges after the contact is made.

3.3.3 Ultraviolet-visible-near-infrared absorption spectroscopy

To study the optical properties of oxide thin films, the optical transmission was measured using the ultraviolet-visible-near-infrared (UV-Vis-NIR) spectroscopic technique. The measurement principle is based on a beam of monochromatic light passing through a sample and a reference at the same time so that the transmitted light intensity can be measured and plotted as a percentage. UV-Vis-NIR spectroscopy can be used not only for examination of the transparency of oxide thin films but also for determination of their optical energy bandgaps. All measurements presented in this work were recorded using a Shimadzu UV-2600 spectrophotometer equipped with an ISR-2600Plus integrating sphere. Samples were made on quartz substrates in order to acquire accurate measurements owing to the nature of wide-bandgap properties in oxide materials.

3.3.4 X-ray and ultraviolet photoelectron spectroscopy

Photoelectron spectroscopic techniques are commonly used for surface chemical analysis. By applying a high-energy photon source onto a sample, the resulting photoelectric effect leads to the release of photoelectrons which possess information of the original electronic states, i.e. the orbital character. This information is acquired with respect to emission angles and kinetic energies using an electrostatic analyser. Due to the use of an X-ray source, X-ray photoelectron spectroscopy (XPS) allows the study of core-level states at higher binding energies and hence the chemical compositions of the sample [Figure 3.6(a)] whilst ultraviolet photoemission spectroscopy (UPS) utilising a UV light for the photon source is mainly used for the investigation of valence band states derived from the liberation of the valence electrons [Figure 3.6(b)].

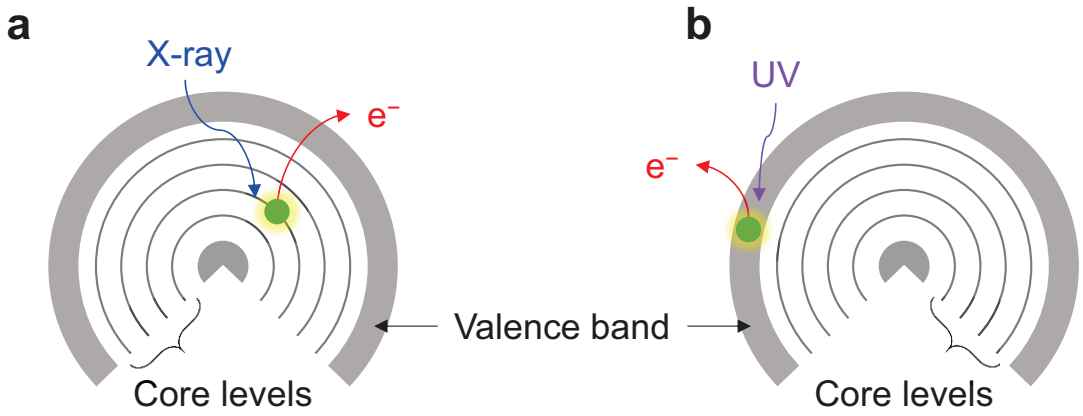


Figure 3.6: Schematic of mechanism for photoelectron spectroscopy: (a) XPS provides the investigation of core-level states via X-ray light source whilst (b) UPS adapts UV light source for the investigation of valence band states.

The experimental details are described hereafter. The photoelectron spectroscopic measurements were taken in a UHV chamber ($<10^{-9}$ mbar) at room temperature. In Chapter 6, the X-ray photoelectron spectra were acquired in a KRATOS Axis Ultra DLD system equipped with a monochromated Al Kα X-ray source using 20 eV pass energy. In Chapter 7, the XPS measurements were carried out using non-monochromatic aluminium Kα X-ray radiation under the following

conditions optimised for maximum signal: constant ΔE mode with pass energy of 36 eV giving a full width at half maximum (FWHM) of 0.9 eV for the Au 4f7/2 peak. The analysed area was an ellipsoid with dimensions 2.5×4.5 mm^2 with a SPECS LHS-10 hemispherical electron analyser. The XPS core level spectra were analysed using a fitting routine, which allows the decomposition of each spectrum into individual mixed Gaussian-Lorentzian components in combination with a Shirley background subtraction.

The spectra for the UPS measurements were obtained using HeI irradiation with hν = 21.23 eV produced by a UV source (model UVS 10/35). During UPS measurements, the analyser was working at the Constant Retarding Ratio (CRR) mode, with CRR = 10. The work function was determined from the UPS spectra by subtracting their widths (i.e. the energy difference between the analyser Fermi level and the high binding energy cutoff) from the HeI excitation energy. For these measurements a bias of −12.29 V was applied to the sample in order to avoid interference of the spectrometer threshold in the UPS spectra.

In this thesis, the photoelectron spectra were performed by collaborators from two different institutes. For the work presented in Chapter 6, the XPS measurements were carried out by Prof. Panos A. Patsalas and his colleagues at Aristotle University of Thessaloniki, Greece whilst the XPS and UPS data presented in Chapter 7 were obtained by Dr. Emmanuel Stratakis and his colleagues at Foundation for Research and Technology-Hellas (FORTH) and University of Crete, Greece.

3.3.5 Grazing-incidence diffraction and X-ray reflectivity

Grazing incidence diffraction (GID) is a technique used to determine the crystalline structures of materials based on Bragg's law. In particular, GID adapts small incident angles for the incoming beam to a sample surface, so diffractions are generally surface sensitive. Therefore, this characteristic makes GID a powerful tool to study surfaces and layers since wave penetration is limited. The resolvable distances are on the order of nm. X-ray reflectivity (XRR) is operated in a similar manner to GID, i.e. the use of smaller incident angles. The working principle requires reflecting a beam from a flat surface and measuring the reflected intensity in the specular direction.

XRR is useful for analysis of a multi-layered structure since the reflected intensity from imperfect interfaces can separate following the law of Fresnel reflectivity. Therefore, the data can be analysed to acquire the density profile of the interface along a surface normal. Figure 3.7 displays a general experimental setup for both GID and XRR measurements.

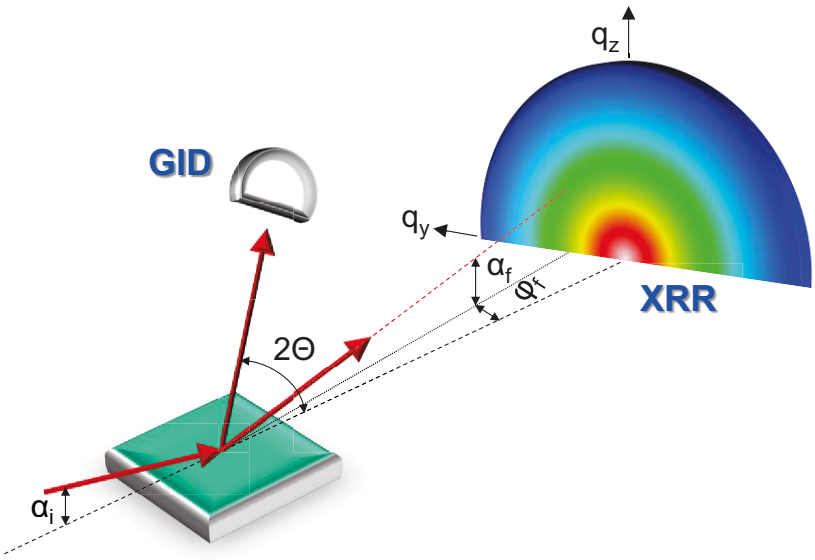


Figure 3.7: Schematic representation of GID/XRR measurements where α_i and α_f are the incident and exit angle of the X-ray beam, respectively; φ_f is the scattering in-plane angle; 2Θ is the diffraction angle; q_y and q_z are the horizontal and the vertical scattering vector, respectively.

In this work, both GID and XRR were carried out on beamline G2 in Cornell High Energy Synchrotron Source (CHESS) by Dr. Ruipeng Li at Cornell University, USA. The samples were aligned on a Kappa diffractometer with the X-ray energy of 10.038 keV (λ = 0.123511, Chapter 6) or 13.65 keV (λ = 0.0908 nm, Chapter 7) through a Be single-crystal monochromator. The data was collected using a 640-element 1D diode-array detector, with a set of 0.1° Soller slits mounted on the detector arm to provide an in-plane resolution of 0.16°. The grazing incident angle was fixed at 0.1° in grazing incident diffraction. The XRR results were simulated by Parratt32 software program developed at HMI in Berlin, Germany.

3.3.6 Transmission electron microscopy

Transmission electron microscopy (TEM) is a microscopy technique that obtains images from beam of electrons transmitted through an ultra-thin specimen. An image can be formed from the interaction of the electrons transmitted through the specimen. The small de Broglie wavelength of electrons allows a TEM to acquire high-resolution images at the nanoscale. In addition, an imaging mode of the TEM named high-resolution TEM (HRTEM) is often used for direct imaging atomic structures of a sample via phase contrast imaging techniques. Additionally, TEM can be used to obtain electron diffraction pattern for investigating the crystal structures of a solid sample.

In this thesis, the TEM imaging was performed by Prof. Aram Amassian and his colleagues at King Abdullah University of Science and Technology (KAUST), Saudi Arabia. A transmission electron microscope operating at an accelerating voltage of 300 kV (Titan 80-300 Super Twin, FEI Company) was used to acquire cross-section micrographs. Charged couple device (CCD) camera (Model: US4000, Gatan Inc.) was used to record HRTEM images. Samples were prepared on a focused ion beam (FIB; Helios 400s, FEI) equipped with a nanomanipulator (Omniprobe, AutoProbe300) using a lift-out method. Electron beam assisted carbon and platinum deposition was performed on the sample surface to protect the thin film surface against the ion beam bombardment during ion beam milling. Ga ion beam (30 kV, 9 nA) was first used to cut the sample from the bulk (30 kV, 9 nA), and then it was attached to a Cu grid using a lift-out method. The sample was subsequently thinned down to ca. 50 nm thickness (30 kV, 93 pA) and cleaned (2 kV, 28 pA) to get rid of areas of the sample damaged during the thinning process.

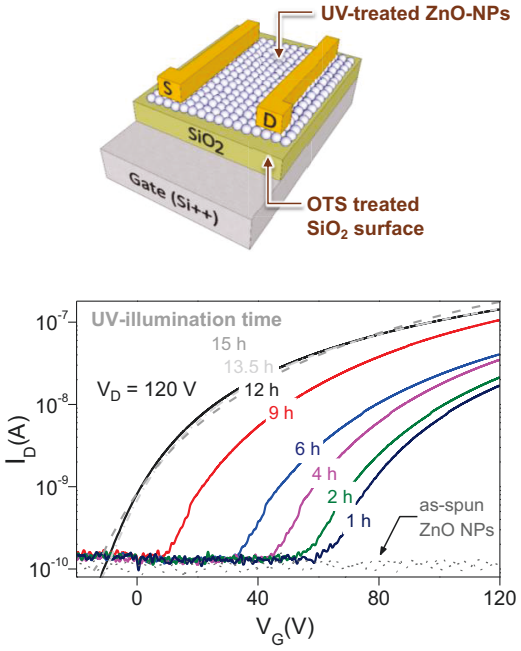
3.3.7 Time-of-flight secondary ion mass spectrometry

Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is a surface analytical technique in which a solid sample surface is sputtered with a focused primary ion beam, and the ejected secondary ions are collected for analysis of the sample composition by a time of flight mass analyser. In this work, an IONTOF TOF-SIMS[5]

at 10^{-8} torr was used to measure depth profiles with a 2kV Cs^+ (~75 nA) sputter beam rastered across a 400 × 400 μm^2. Positive ions were collected from the central 100 × 100 μm^2 of the sputter crater using a Bi^{3+} (~1 pA) beam with charge compensation. The TOF-SIMS measurements were carried out by Dr. Neil D. Treat at Imperial College London, UK.

4

NANOPARTICLE-BASED ZNO THIN-FILM TRANSISTORS



Rather than using thermal calcination, an alternative ultraviolet (UV) light irradiation process is developed to fabricate solution-processed nanoparticle (NP)-based ZnO thin-film transistors. The resulting devices exhibit n-type conductivity with electron mobilities on the order of ~10^{-3} cm^2/Vs — a value comparable to that normally obtained from NP-based devices thermally annealed at >250 °C. Importantly, the UV photochemical process can be performed close to room temperature. This enables facile fabrications of ZnO-based devices using temperature-sensitive substrates for applications in inexpensive flexible/plastic electronics. In addition, the impact on the quality of the interface between semiconductor layers and the gate dielectric on the transistors' electrical performance is studied through the use of different device geometries and dielectric surface passivation methods. (Left panel: Transfer characteristics for UV-photochemical activated NP-based ZnO TFTs.)

4.1 Introduction

A variety of solution-processable semiconducting metal-oxide materials have been demonstrated to date that promise to revolutionise the field of large-area opto/electronics [45, 74, 75]. However, the majority of these materials require a high-temperature annealing step that is generally incompatible with most of flexible/plastic substrates [43, 76-78]. In principle, this low temperature processing requirement could be addressed through the use of suspensions of crystalline nanoparticles (NPs) [79], to replace the commonly used precursor formulations that require high annealing temperatures. In particular, oxide-semiconductor ZnO has attracted the most attention owing to the fact that ZnO is non-hazardous and exhibits excellent electrical and optical properties (i.e. high electron mobility and high optical transparency) [80, 81]. More interestingly, the shape and size of ZnO NPs can be tailored through the choice of appropriate synthetic parameters and conditions [82]. To this end, additives and dispersing aids are commonly used to assure the quality and stability of NP inks. Typical examples include ligand shells directly attached to the particles [83], counter ions [84], and also longer carbon/polymer chains added in the dispersing medium [85].

Although these approaches ensure simple processing during solution-based thin-film depositions, they usually introduce a large number of electrically insulating materials that act as energy barriers to hinder charge transport between adjacent NPs. Hence, removal of such additives and simultaneous improvement of inter-particle electrical conductivity is required to improve device performance. To fulfil this purpose, a room-temperature ultraviolet (UV) photochemical process is adapted for the elimination of unwanted insulating products and restores/activates the conductivity in the NP-based solution-processed ZnO films. The effectiveness of the UV treatment is investigated with different UV irradiation durations. Meanwhile, the effects of different surface passivation agents for SiO_2 dielectrics as well as the effect of device architecture on the overall transistor performance are both studied. Although a similar UV process has recently been reported for the conversion of metal nitrate/acetate-based precursors to form multi-component metal-oxide films at ~160 °C [86], the role played by this high-processing temperature, in addition to the UV

irradiation, remains unclear and somewhat convoluted. Therefore, the process of fully functional NP-based ZnO transistors utilising UV irradiation at room-temperature could represent a significant step towards applications in flexible opto/electronics.

4.2 Review on nanoparticle-based thin-film transistors

Before looking into the UV photochemical process, a brief review of previous works on solution-processed NP-based ZnO TFTs is provided in this section. One of the earliest works that adapted ZnO NPs for the active layer of a TFT was done by Volkman et al. [87], in which NPs were synthesised by reacting zinc acetate with sodium hydroxide in 2-propanol and then encapsulated by 1-dodecanethiol to avoid agglomeration. As such, the NP size was limited down to 3 nm. The as-prepared ZnO NPs were then suspended in chloroform and spun-cast onto the Si/SiO_2 substrates, followed by annealing at 150 °C. Afterwards, a 400 °C forming-gas annealing process was carried out to passivate dangling bonds. In this work, the on/off ratio of nearly 10^3 was claimed, and the highest mobility obtained was 0.1–0.2 cm^2/Vs. Whilst the reported electron mobility was relatively good back in 2004 compared to alternative solution-processing approaches [88, 89], the process temperature was far beyond the thermal budget that can typically be handled by a printing process. The latter is the main purpose and application claimed in ref. [87].

As described in Section 4.1, for ZnO NP suspensions the addition of surfactants plays an important role to avoid NP agglomeration, but it could block charge transport between NPs. In the work by Hirschmann et al. [90], TFTs based on ZnO NPs derived from zinc acetate and zinc 2-ethylhexanoate were investigated. The results revealed the impact of the use of different ligand shells on the electrical properties of the NPs. Functionality in the Zn-acetate based TFTs was attributed to the electrically inactive particle to particle junctions bridged by smaller acetate ligands. The larger size in 2-ethylhexanoate caused a larger particle to particle distance, increasing resistivity, and hence restricted any semiconducting property of the ZnO-NPs. Due to the fact that semi/insulating ligand shells might be detrimental to electrical property after the implementation of ZnO NPs into TFT structures, Faber et

al. [91] introduced oxygen plasma treatment in order to remove the organic ligand shells as well as reduce the number of defects in the NPs. Higher current modulation and less hysteresis were obtained in the TFT electrical characterisation after the oxygen plasma treatment.

Morphology of the thin-film layers, on the other hand, is another important factor to determine the device performance. Okamura et al. [92] observed that different NP agglomerate sizes were obtained by adding different stabilisers in NP suspensions. From SEM measurements, the obtained NP films exhibited significant differences in roughness at the semiconductor-dielectric interface. As a result, the NP-based TFTs utilising suitable stabilisers and smoother films showed an improvement of two orders of magnitude in electron mobility, compared to those made without stabilisers and rougher interfaces. Therefore, it was concluded that interfacial roughness is crucial to the performance of NP-based transistors. To overcome the poor interface morphology caused by the spherical shape of NPs, the work by Faber et al. [79] showed that the electrical performance could in principle be improved by altering device geometry. Surprisingly, ZnO NP-based memory devices with an exceptional mobility of 2.5 cm^2/Vs were obtained using transistors in TG-BC configuration whilst TFTs in BG-TC configuration showed only low mobility (8×10^{-3} cm^2/Vs) and did not exhibit any memory effect. For the TG-BC ZnO-NP TFTs, the interesting memory behaviour was mainly attributed to mobile ions from the gate dielectric of poly(4-vinylphenol) (PVP) trapped at the ZnO/PVP interfaces whilst the enhanced electron mobility was because of the use of the solution-processed PVP dielectric that provided full coverage of the ZnO NPs and left no “gaps” between the NP films and the gate dielectric.

Bubel and Schmechel proposed a mechanical rolling process to achieve a densely-packed ZnO NP films with improved layer morphology and transistor performance. One important advantage of this process is its compatibility with roll-to-roll processing [93]. As a result, the surface roughness was reduced to form a much more compact layer after the rolling process. Moreover, the change in the film morphology directly increased the saturation mobility in the rolled TFTs (10^{-3}~10^{-4} cm^2/Vs) by one order of magnitude as compared to that obtained in the as-deposited TFTs (5×10^{-5} cm^2/Vs). From this review of prior work, one should note that the

performance of ZnO-NP based transistors is mainly limited by inter-particle conductivity and interfacial morphology. To overcome these issues, in the following sections the aforementioned UV-photochemical process, as well as engineering of the semiconductor-dielectric interfaces, will be introduced and discussed in detail.

4.3 UV light-activated nanoparticle-based ZnO transistors

4.3.1 Device fabricated via a UV photochemical process

The ZnO NP dispersion (40% w/w in ethanol) used in this work was provided by NanoMaterials Technology. The as-received dispersion was diluted to 2% w/w and used directly for the deposition of the thin film. The semiconductor films were grown by spin casting of the diluted ZnO NP dispersion on top of the octadecyltrichlorosilane (OTS)-treated Si/SiO_2 substrates. The details about the preparation and passivation of SiO_2 with the OTS molecule will be discussed in Section 4.4.1. The spin-casting process was carried out at 2000 rpm for 30 sec under inert gas environment. In order to improve the ZnO NP layer morphology, film thickness and hence device performance, the NP films were formed using a double spin-cast step where the spin-casting step was carried out twice using the same process parameters as described above.

After spin casting, the UV-photochemical process was applied to the as-deposited ZnO NP films using a low-pressure mercury lamp. The latter emitted at wavelengths of 253.7 nm (97% of overall power) and of 184.9 nm (3% of overall power) at total output power of approximately 5 mW/cm^2 at a distance of 2 cm. The entire process was performed in ambient air for different periods of time (0–15 h). The sample temperature during UV illumination was monitored and found to remain at room temperature, ensuring no unintentional heating effect involved in this study. The conversion is purely achieved by UV irradiation. Transistor fabrication was completed with the deposition of Al source and drain (S-D) electrodes by thermal evaporation through shadow masks in high vacuum (10^{-6} mbar). The resulting transistors had channel length (L) and width (W) of 20 μm and 200 μm, respectively.

Figures 4.1(a) and (b) show representative AFM topography images of single and double spin-cast ZnO NPs films. Single spin-cast films appear less uniform and contain a number of voids whilst double-cast films appear significantly denser. Both images reveal the presence of ZnO NPs with diameter ~20 nm in good agreement with the product specification (i.e. average particle diameter ~18 nm) provided by the manufacturer. The associated distributions of surface height are plotted in Figure 4.1(c), revealing that the double spin-cast film is only slightly rougher with values of root mean squared roughness (R_{RMS}) of 1.03 nm as compared to R_{RMS} of 0.98 nm in the case of the single spin-cast film. Figure 4.1(d) shows a set of UV-Vis-NIR spectra (corrected to the blank substrate spectrum) measured from the two types of films before and after the UV treatment (12 h). There exist clear excitonic absorptions from the UV-processed films in the range of 350–380 nm, which is a signature of blue shift with respect to the absorption edge taking place in small-size ZnO NPs [94], whilst the non-UV processed films only show a bulk-like adsorption. In addition, the higher absorption measured for the double spin-cast film is attributed to the denser and thicker nature of the ZnO NPs-based layers.

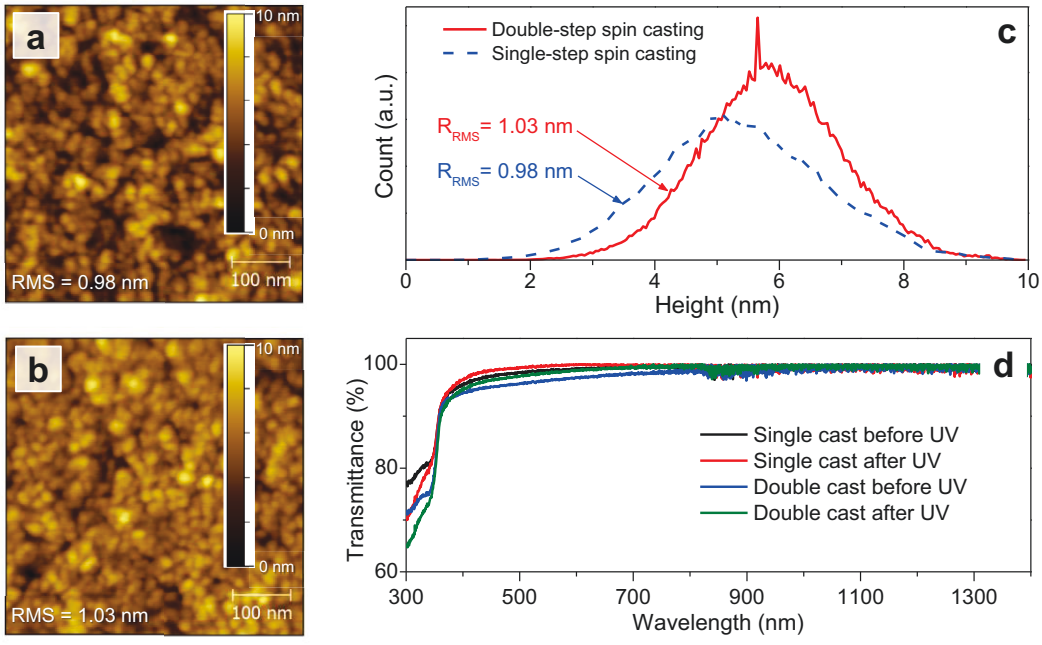


Figure 4.1: (a) and (b) show AFM topography images of ZnO NPs films spun onto Si/SiO_2 substrates using single-step and double-step spin-casting processes, respectively. (c) Statistical distributions of surface height and associated root mean squared surface roughness (R_{RMS}). (d) A set of UV-Vis-NIR spectra were measured before and after the UV irradiation for single-cast and double-cast ZnO NPs films. (Adapted from ref. [95] with permission from American Institute of Physics.)

Figure 4.2(a) shows the schematic of the transistor architecture used whilst the transfer characteristics of ZnO-NP based transistors with a single and double spin-cast process before and after the UV-photochemical treatment for 12 h are displayed in Figure 4.2(b). For this optimised UV irradiation time, the experimental process and results will be provided in the next section. It can be seen that prior to UV irradiation there is no field-effect induced channel current existing in the transistors. On the other hand, the UV-treated devices show clear n-type transistor behaviour with strong electron accumulation when applying a positive gate-bias. In particular, transistors based on a single spin-cast step exhibit on/off current ratios in the range of 10^3–10^4 and threshold voltages (V_T) around 20 V. The electron mobility, evaluated in the saturation regime, is found to be on the order of 10^{-4} cm^2/Vs. For the devices prepared by a double spin-cast step, significantly larger channel currents and lower V_T were measured. As a result, the electron mobility of these devices is higher and on the order of 10^{-3} cm^2/Vs. The results obtained here highlight the importance of uniformity of the ZnO NP layers on the overall transistor performance. Therefore, all following experiments in this chapter were carried out using double spin-cast ZnO-NP layers.

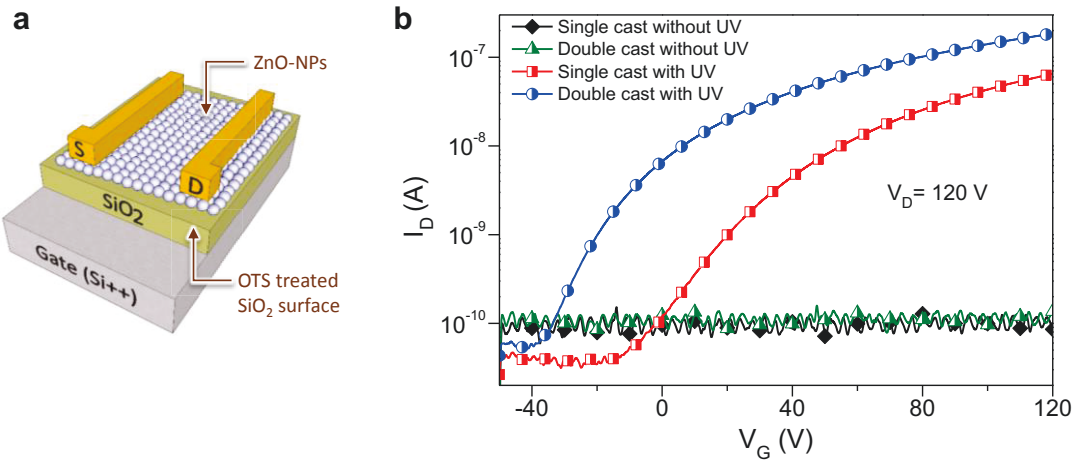


Figure 4.2: (a) Schematic of the BG-TC ZnO NP transistor structure employed. (b) Transfer characteristics of ZnO NP transistors based on single and double spin-cast ZnO-NP films with or without the UV-photochemical treatment. In the case of the UV-treated devices, as-spun ZnO-NP layers were irradiated with the UV light in air, followed by the evaporation of the Al S-D top electrodes in high vacuum. For the untreated devices, the S-D electrodes were deposited right after spin-casting of the ZnO-NP layer. All devices studied here were based on OTS-treated SiO_2 gate dielectric.

4.4 Impact of UV light irradiation duration on device performance

The functional transistors shown in Figure 4.2(b) after UV irradiation could be attributed to that the photochemical treatment under the UV wavelengths of 253.7 nm and 184.9 nm has provided sufficient light intensity and irradiation time to induce a photocatalytic removal of the electrically inactive organic-ligand shells from the surfaces of ZnO NPs in combination with the presence of reactive atomic oxygen and ozone molecules [96-98]. However, another possible effect that needs to be considered is the significant n-type photo-doping behaviour often observed in ZnO-based materials upon UV irradiation [99]. The mechanism can be attributed to a photoconductivity-like process and/or the photo-induced desorption of oxygen from the ZnO-NP surface. In the former case, the photoconductivity-like effect can be disregarded in this study since the effect of the UV-treatment was found to persist for months and was not temporary. The latter, on the other hand, was not likely to happen due to the fact that the UV treatment was performed in ambient environment, in which oxygen was expected to be re-adsorbed within a short period of time without the presence of the UV-light source. Based on the experimental findings, neither of these two photo-doping processes mentioned here was responsible for the formation of the n-type conductivity observed in these UV-treated ZnO-NP transistors.

In order to further understand the UV photo-conversion mechanism, the effect of different UV-illumination time (from 0 to 15 h) on the electrical performance of ZnO-NP transistors (made on OTS-treated Si/SiO_2 substrates) was investigated by carrying out a series of current-voltage characterisations, and the corresponding transfer characteristics are shown in Figure 4.3. From the results, it can be seen that the drain current increases with increasing illumination time and saturates after ~12 h of illumination. The onset voltage is found to reduce from 70 V to −10 V for the illumination periods of 1h and 15 h, respectively. On the contrary, for the devices treated with this UV process in nitrogen environment, a very small amount of channel current (nearly unidentifiable) can be observed only after a much longer irradiation time (>1 day). This finding directly indicates that the presence of oxygen is crucial for this photo-conversion process. In fact, the observed gradual increase in channel

current could suggest that the removal of ligands/surfactants dominates the conversion process because this successive process is in agreement with the time-dependent ozone-cleaning process [97, 98]. The highest electron mobility measured in the saturation regime is 1.7 × 10^{-3} cm^2/Vs for devices treated for ~12 h. This result is attributed to the reduced number of NP ligands/surfactants could enhance the inter-particle electrical conductivity [96]. Moreover, the effectiveness of the UV treatment is expected to reach a maximum once all existing ligands/surfactants in the area where the UV light can reach are removed. This assumption is in good agreement with the present finding in which there is no significant improvement observed in the device performance after carrying out the UV-irradiation time of >12 h (see Figure 4.3).

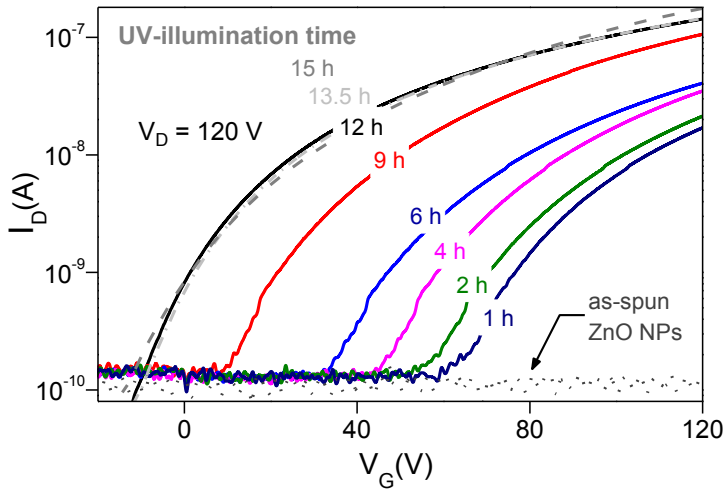


Figure 4.3: Transfer characteristics for ZnO-NP based transistors prepared using different UV-illumination time from 0 h to 15 h.

In addition to electrical performance, the evolution of the trapping concentrations in ZnO-NP films with different UV-illumination time was studied by the analysis of transfer characteristics of the transistors shown in Figure 4.3. To be noted that the contact resistance for each transistor was relatively small as compared to the overall channel resistance since the Ohmic behaviour was observed in the output characteristics (for more information, see ref. [95]). Figure 4.4 displays the evolution of interfacial surface trap density (N_{tr}), relative surface trap density (ΔN_{tr} — evaluated against the 12-h UV-treated device) and trap concentration per unit energy

(D_{tr}) [100, 101]. All three parameters were calculated directly from the transfer characteristics shown in Figure 4.3 using

$$N_{tr} = \frac{C_i|V_T - V_{ON}|}{e}, \tag{4.1}$$

$$\Delta N_{tr} = \frac{C_i|\Delta V_T|}{e}, \tag{4.2}$$

$$D_{tr} = \frac{C_i}{e^2}\left(\frac{eS}{kT\ln(10)} - 1\right) \tag{4.3}$$

where e is the elementary charge, V_{ON} is the onset voltage, k is the Boltzmann constant, T is the temperature, S is the subthreshold swing, and C_i is the geometric capacitance of the gate dielectric. Both D_{tr} and ΔN_{tr} show descending trends with increasing UV-illumination time. These results suggest the UV treatment effectively reduces the number of trapping carriers, most likely, at the interface between NPs and on the NP top surfaces. N_{tr}, however, appears to be independent from the illumination time. The reason could be attributed to that the interfacial morphology between ZnO NPs and OTS-treated SiO_2 remains the same before and after the UV treatment since the UV irradiation is not likely to cause direct impact in such regions by penetrating through a densely-packed NP layer.

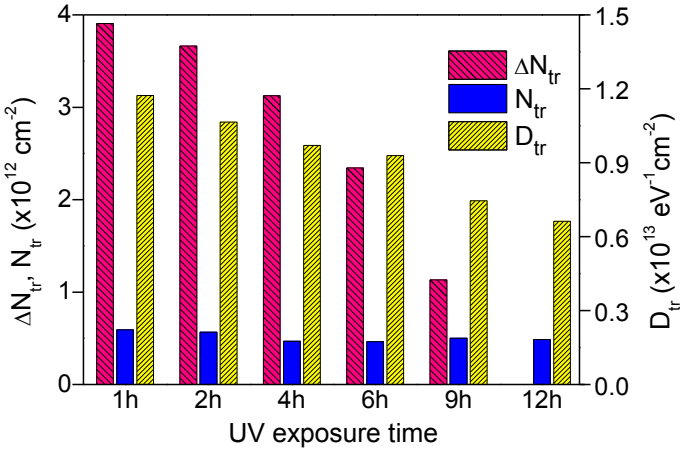


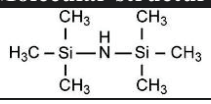
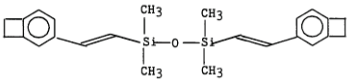
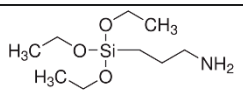
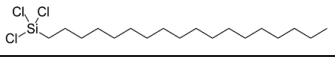
Figure 4.4: Analysis of interface trap density (N_{tr}), relative surface trap density (ΔN_{tr}), and trap concentration per unit energy (D_{tr}) for the transistor data shown in Figure 4.3.

4.5 Importance of semiconductor-dielectric interface

4.5.1 Influence of surface passivation agent

In the previous section, the comparison of trapping concentrations between different UV-illumination durations is based on the use of the same surface treatment (i.e. OTS) on the gate dielectric. However, one important factor regarding a field-effect device is that the channel is formed in the vicinity of the interface between ZnO NPs and SiO_2 gate dielectric [102]. As such, in this section the effect of several commonly-used SiO_2 passivation agents, including OTS, bis(trimethylsilyl)amine (also known as hexamethyldisilazane, i.e. HMDS), (3-aminopropyl)triethoxysilane (APTES) and divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) (see Table 4.1 for molecular structures of each passivation agents), are studied for their properties on the subjects of improving charge carrier mobility and reducing trapping concentrations.

Table 4.1: Names and molecular structures of materials used for passivating the SiO_2 surface.

Material	Acronym	Molecular structure
Hexamethyldisilazane (≥99%, Sigma-Aldrich)	HMDS	
Divinyltetramethyldisiloxane-bis(benzocyclobutene) (CYCLOTENE 3022-35, The Dow Chemical Company)	BCB	
(3-aminopropyl)triethoxysilane (99%, ACROS Organics)	APTES	
Octadecyltrichlorosilane (≥90%, Sigma-Aldrich)	OTS	

Before the deposition of the ZnO NPs onto the Si/SiO_2 substrates, the substrates were cleaned following the standard cleaning procedure described in Chapter 3, and the SiO_2 gate dielectrics were then treated with the following surface passivation steps. To carry out the HMDS treatment [95], the cleaned Si/SiO_2 substrates and a Petri dish containing HMDS of 20 mL were both placed on a pre-heated hot plate (70 °C) in a large glass dome forming a closed system. After 15-20 min, the HMDS solution was removed from this system, and the substrates remained

on the hot plate for another 30-min thermal-annealing process at the same temperature. For the BCB treatment [95], a diluted BCB solution (5% v/v in trimethylbenzene) was spin-cast onto the SiO_2 surface at 3000 rpm for 60 sec. The substrates were then subjected to the following thermal-annealing process: 30-min ramping to 200 °C and 60-min soaking at 200 °C. The whole process of the BCB treatment was carried out under inert gas environment. For the APTES treatment [95], the cleaned substrates were first submerged into an APTES solution (1% v/v in toluene). Then the whole system was sealed and placed on a pre-heated hot plate at 75 °C for 60 min. At the end of this reaction time, the substrates were removed from the APTES solution and thoroughly washed with toluene. The substrates were then annealed at 90 °C for 30 min in order to dry residual solvent. To perform the OTS surface treatment [95], the substrates were submerged into the OTS solution (0.2% v/v in toluene) at room temperature for 30 min and washed with toluene. Substrates were then dried using a thermal annealing process at 90 °C for 30 min. In order to reduce the effect of humidity during the OTS formation, the whole process of the OTS treatment was carried out in inert gas atmosphere.

The transfer characteristics obtained from ZnO-NP transistors with a 12-h UV-irradiation using different surface-passivation agents are displayed in Figure 4.5. Evidently from these results, it can be concluded that ZnO-NP transistors based on surface-passivated SiO_2 substrates can deliver better performance as compared to those fabricated on bare SiO_2. The reason is attributed to that SiO_2 surface tends to contain Si-OH defects and water molecules [16, 103], especially after a standard UV-cleaning process. In the present study, these defects, together with some possible alkali ions in oxide layers, have a significant influence on device characteristics, especially when considering interface trapping and hysteresis [104]. The large difference in transfer characteristics between ZnO-NP TFTs based on different passivation methods provides direct evidence for the electrochemical hydroxyl electron-trapping mechanism [103]. As a result, the interface becomes charged by a layer of immobile negative ions that compensates the gate-induced electric field and leads to a dramatic increase in the threshold voltage to a level that is well beyond the measurement window (if higher gate voltages are applied, the devices tend to break because of gate-dielectric breakdown). Among the different molecules used as

passivation agents, the OTS-treated samples show the highest field effect performance. This is most likely attributed to its long aliphatic hydrocarbon chain that provides better passivation and high barriers for tunnelling to electron-trapping sites at and/or near the SiO_2 surface.

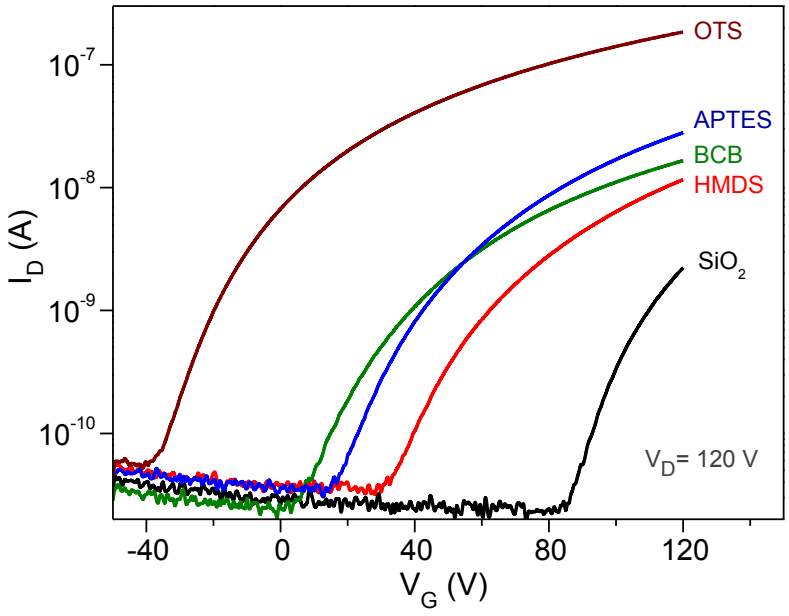


Figure 4.5: Influence of different dielectric surface passivation agents on transfer characteristics of TFTs based on ZnO NPs. Double spin coated layers of the ZnO-NP dispersion onto the treated/untreated Si/SiO_2 substrates.

The trapping concentrations of different SiO_2 surface passivation is illustrated in Figure 4.6 where N_{tr}, ΔN_{tr} (calculated against the OTS-treated sample), and D_{tr}, are plotted against the different passivation agents used here. Clearly, the OTS treated devices show the lowest concentration of electron traps in line with the best field-effect performance (Figure 4.5). It is noted that for all of the samples the obtained N_{tr} still remains at the same level as seen in Section 4.4. This is likely due to the fact that the morphology of ZnO-NP layers at the SiO_2-dielectric surface has already been determined after the film deposition. As such, regardless of how many free charge carriers exist in the ZnO-NP layers (i.e. V_{ON}), the difference between V_{ON} and the starting voltages for the formation of the current channels (i.e. V_T) were similar among the samples although different passivation agents were already applied.

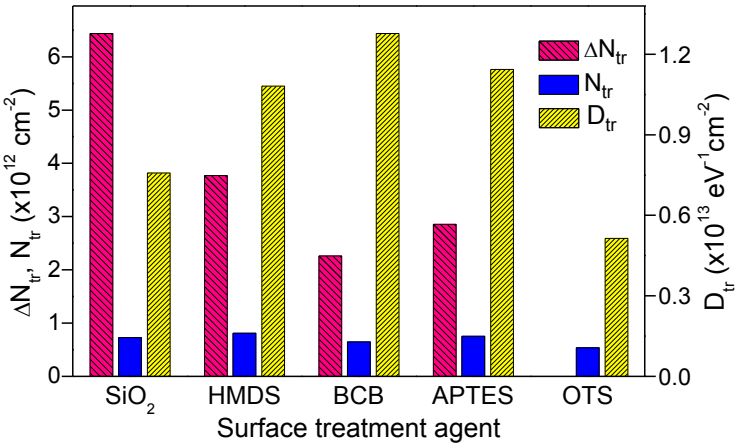


Figure 4.6: Estimated interface trap density (N_{tr}), relative surface trap density (ΔN_{tr}), and trap concentration per unit energy (D_{tr}) for different surface passivation agents in ZnO-NP based transistors shown in Figure 4.5.

4.5.2 Impact of device architecture on electrical properties

As seen in the brief review of Section 4.2, the poor packing and the rough interface caused by the spherical shape of ZnO NPs could be the main reason for poor performance in NP-based transistors. This speculation is further investigated by adapting alternative device architectures, i.e. bottom-gate top-contact (BG-TC) and top-gate bottom-contact (TG-BC) transistor structures with solution-processed polymer-based dielectrics. This approach might disentangle the influence of the interaction effects between SiO_2 and NP layers, and therefore the intrinsic properties of NP-based layers could be obtained.

For the TG-BC TFTs, 40-nm thick Al S-D electrodes were deposited by thermal evaporation through a shadow mask (L = 20 µm, W = 1500 µm) on glass substrates. ZnO NP layers were deposited via a double spin-cast step using the same process parameters described earlier (Section 4.3.1), followed by the UV-illumination process for 12 h in ambient air. The epoxy-based negative photoresist SU-8 (MicroChem) was used as the gate dielectric. A thin layer of SU-8 was deposited by spin-casting at 2000 rpm for 1 min under inert gas atmosphere. The obtained thickness was ~2 µm (measured with profilometer) and the geometric capacitance of the SU-8 dielectric layer was estimated to be around 2.1 nF/cm^2 (measured using an impedance analyser). A pre-exposure baking process at 100 °C for 30 min was carried

out right after the deposition of SU-8 layer onto the substrates. The samples were then exposed to 254-nm UV light for 30 min to perform the crosslinking process, followed by a post-exposure baking process at 100 °C for 30 min. The TG-BC TFTs were completed by thermal evaporation of 50 nm thick Al gate electrodes through a shadow mask. For the BG-TC TFTs the Al gate electrodes were deposited first, followed by the deposition of the SU-8 gate dielectric, the ZnO NP semiconductor layer and finally the Al S-D contacts. The processing parameters for semiconductor thin films in the BG-TC TFTs were exactly the same as for the TG-BC TFTs.

The current-voltage characteristics of the BG-TC and TG-BC ZnO-NP based TFTs are shown in Figure 4.7. The BG-TC transistor exhibits large hysteresis, low current on/off ratios and poor electron mobility whilst the TG-BC device shows a strong field-effect current modulation. These results directly demonstrate that the semiconductor-dielectric interfacial morphology could be key in obtaining high-performance ZnO-NP based TFTs. In the present study, the electron mobility extracted for the TG-BC TFTs was of the order of 10^{-3}–10^{-4} cm^2/Vs, which is one order of magnitude larger than that measured in the BG-TC devices.

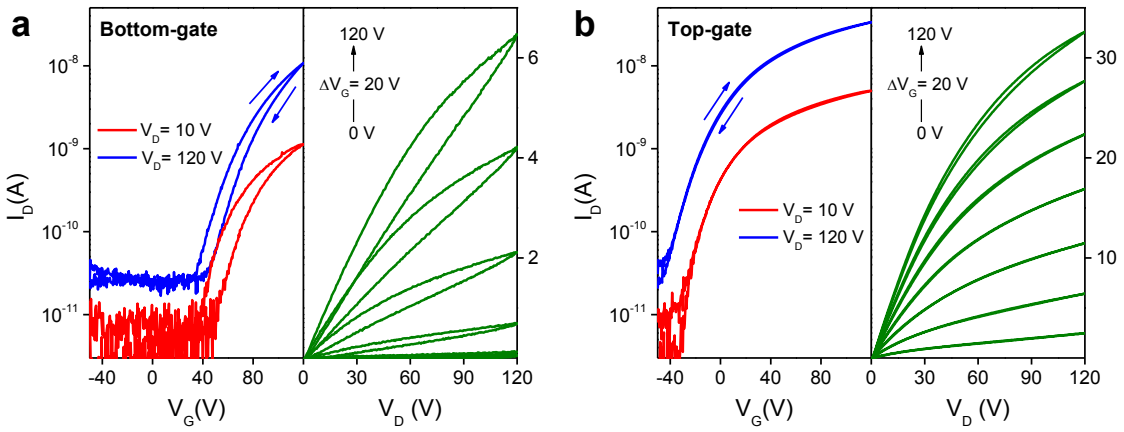


Figure 4.7: Current-voltage characteristics of (a) BG-TC and (b) TG-BC ZnO-NP based TFTs utilising SU-8 as the gate dielectric.

The UV-illumination process could in principle be used for manufacturing ZnO-NP based TFTs on most plastic substrates due to the capability of activating transistor functions at room temperatures. However, the electrical characterisation results of the attempts to fabricate UV-treated transistors (in TG-BC configuration

with CYTOP dielectric) on plastic foils exhibited rather low performance (electron mobility $<10^{-4}$ cm^2/Vs) and small current modulation (an on/off ratio of $<10^2$). Such low mobilities and on/off ratios could be attributed not only to the non-optimised process of the polyethylene terephthalate (PET) substrates, but also to the poor intrinsic inter-particle transport of NPs. This is because the lateral transport of the NP-based device is still limited by the "spherical" shape of NPs and non-organised (random) distribution after solution-based deposition. These factors are the main obstacles to find a breakthrough in the present study as well as other works reported in the literature (see Section 4.2). Therefore, the next section introduces a nanocomposite approach to resolve the difficulty in inter-particle transport by filling voids between NPs with a "bridging" semiconductor material.

4.6 Nanocomposite-based ZnO transistors

The main advantage of using low-dimensional nanocrystals, e.g. nanoparticles (NPs) and nanowires (NWs), to achieve low-temperature solution process is the controllable crystallinity of the semiconducting films (as this is determined during chemical synthesis) without the need of the high thermal budget to convert any form of precursor materials. In the previous sections, the commercial ZnO-NP dispersion was used as the active material in the ZnO TFTs. Owing to the void space existing between the NPs, the obtained device performance was low ($\mu_{SAT} \approx 10^{-3}$–$10^{-4}$ cm^2/Vs). Therefore, in this study a larger-aspect ratio nanocrystalline material, i.e. ZnO NW [105], was used to replace ZnO NP as the active channel material.

The ZnO NWs (1~4 μm in length, supplied by Harp Engineering) were dispersed into chloroform/methanol (3/1, V/V) at a concentration of 10 mg/mL [105]. Butylamine (≥99%, Sigma-Aldrich) was added as a ligand to coat the NWs' surface. The dispersion was processed using an ultrasonic bath for 20 min to break apart any large agglomerates. Finally, the ZnO NW dispersion was rigorously stirred at room temperature for 12-15 h before use. For the fabrication of ZnO NW-based transistors, the semiconductor films were deposited by spin casting the ZnO NW dispersion onto the Si^{++}/SiO_2 substrates (without applying any surface treatment) at 2000 rpm for 30

sec, followed by a post-deposition thermal-annealing process for 60 min at 180 °C in ambient air. The transistors were completed by thermal evaporation of 40-nm thick Al top S-D electrodes through a shadow mask.

Figure 4.8 shows a set of the transfer and output characteristics measured from a BG-TC ZnO-NW TFT with a channel length of 100 µm and a channel width of 1000 µm, respectively. The electron mobility derived is on the order of 10^{-2}–10^{-3} cm^2/Vs, which is around one order of magnitude higher than the TFTs based on ZnO NPs. However, the non-linear increase of I_D as a function of V_D at low bias [Figure 4.8(b)], indicates poor electron injection from the contacts to the ZnO-NW film. This could be attributed to the large dimension of the ZnO NWs (1–4 µm, dimensions provided by the material supplier) causing a non-uniform formation at the metal contacts. In both ZnO NP and NW TFTs, one of the most challenging parts is controlling the distribution and orientation of the nanocrystals to avoid gaps/voids between the nano-crystalline domains.

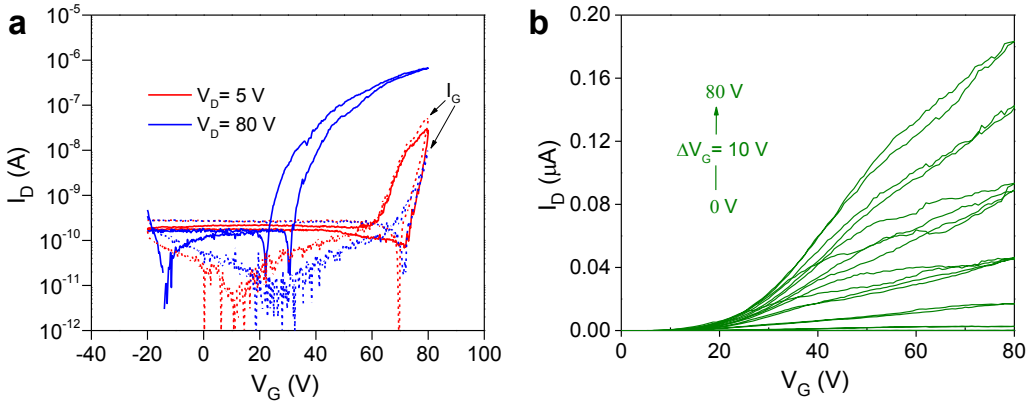


Figure 4.8: (a) Transfer characteristics (drain current: solid line, gate current: dashed line) of a ZnO-NW based TFT. (b) Corresponding output characteristics for the NW-based transistor shown in (a).

The concept of nanocomposites is based on the use of pre-formed (i.e. no need for chemical conversion of the precursor at high temperatures) highly crystalline NPs/NWs as the main charge transporting domains and/or suitable binder-materials for bridging the voids between NPs/NWs and hence assisting current percolation/conduction. In order to form the ZnO-based nanocomposites, in this study the ZnO NW films were spin-cast, followed by three additional depositions of Zn-

ammine-complex based ZnO layers on the top of the ZnO NW layer (detailed information are given in Chapter 5) before Al S-D evaporation. The transfer and output characteristics of the ZnO-nanocomposite TFT are shown in Figure 4.9(a) and (b), respectively. The linear and saturation mobilities calculated using the gradual channel approximation provided in Chapter 2 are on average of 0.87 and 2.85 cm^2/Vs, respectively. These results represent a great improvement over pristine NP and NW films and suggest the concept of nanocomposite could be the solution for achieving high-performance flexible transistors at low temperature. Moreover, the nonlinear injection is no longer observed in the output characteristics of the nanocomposite device, most likely indicating improved electron injection.

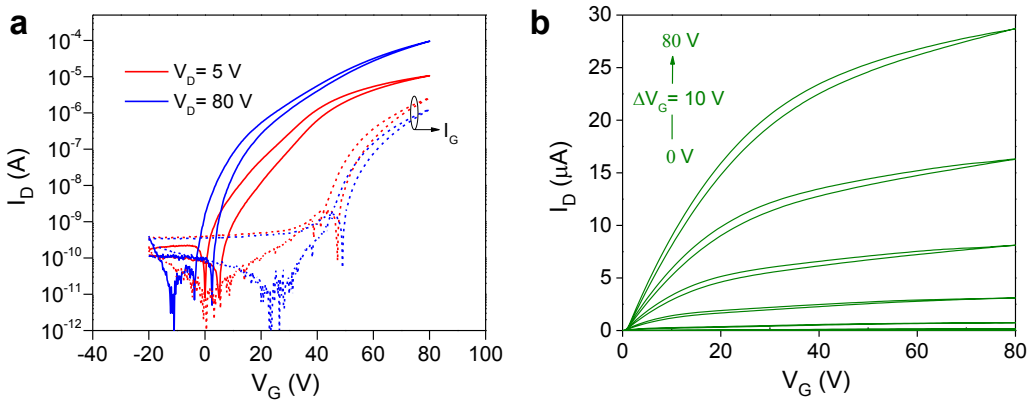


Figure 4.9: (a) Transfer characteristics (drain current: solid line, gate current: dashed line) of a ZnO-nanocomposite based TFT. (b) Corresponding output characteristics for the nanocomposite-based transistor shown in (a).

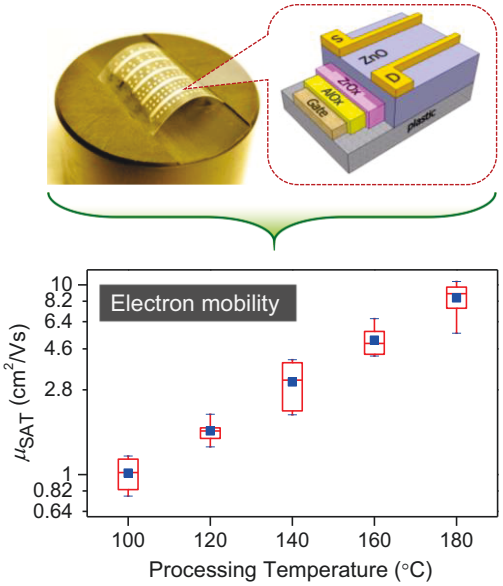
4.7 Conclusions

In summary, the use of UV light irradiation has been demonstrated as a simple post-deposition treatment for ZnO NP layers as a replacement to the traditional high-temperature annealing step often used. The mechanism for this UV illumination is to induce effective elimination of insulating impurities, such as ligands and surfactants, from the NPs' surface. This versatile photochemical conversion method enables room-temperature fabrication of n-type ZnO NP-based transistors with electron mobilities in excess of 10^{-3} cm^2/Vs. Apart from the electron mobility estimation, the

studies of trapping concentrations as a function of different UV-illumination time, surface-passivation agents and alternative device architectures, provide an insightful understanding into the limitations of charge-transport in these ZnO-NP films. Furthermore, a nanocomposite approach has been proposed to overcome the limitations for effective long-range conductivity in NP and NW films by connecting separate nanocrystalline domains with the aid of a binding semiconductor materials. As a result, promising performance ($\mu_{SAT} \approx 3$ cm^2/Vs, $I_{ON}/I_{OFF} \approx 10^6$) can be achieved from ZnO-nanocomposite TFTs.

5

An Aqueous Route to Solution-Processable ZnO Thin-Film Transistors



An aqueous and carbon-free metal-oxide precursor route is used to manufacture solution-processed low-temperature high-performance ZnO-based transistors. By controlling the deposition environment, a maximum electron mobility exceeding 10 cm²/Vs can be achieved. In-depth studies reveal that film morphology is directly related to device performance. In combination with hybrid high-κ dielectrics, low-power ZnO TFTs can be fabricated on plastic foils with a low operation-voltage of 1.2V. Furthermore, the UV light-irradiation process described previously is explored to effectively convert ZnO precursors without involving any thermal-annealing step. Functional ZnO transistors with electron mobility of ~1 cm²/Vs can be obtained. (Left panel: Flexible ZnO TFTs made by Zn-ammine complex.)

5.1 Introduction

To overcome the technology bottleneck of efficient low-temperature, solution-processing of oxide electronics, significant research effort has been focused on developing and exploring new material formulations [106] as well as novel processing methodologies [86, 107] with two main objectives: (i) improving the electronic transport in the metal oxide, and (ii) lowering the processing temperature in order to ensure compatibility with commoditized substrate materials, such as plastic foils.

Recent and noteworthy studies in these directions include processing of metal oxides by: ultraviolet (UV) photochemical activation of sol–gel precursors [86, 108], combustion chemistry of various precursors [107], sol-gel on chip [106], spray pyrolysis [109] and a number of colloidal nanoparticle-based approaches [79, 91, 93, 95]. The use of pre-formed colloidal metal oxide nanocrystals (NCs) and nanoparticles (NPs), offers numerous advantages over thermally convertible sol-gel routes as seen in the last chapter where a room-temperature UV illumination was adapted for the activation of functional ZnO-NP based transistors. However, because of the presence of insulating ligands/surfactants combined with the difficulties in controlling morphology, uniformity and continuity of NP-based layers over large-area substrates, the reported performance of NPs-based transistors to date has still been modest and is often much inferior to most of sol-gel based approaches [106-110].

As proposed in Chapter 4, a preliminary, but encouraging, result was obtained using a nanocomposite approach, which can be seen as a simple way to develop high-performance low-temperature solution-processable oxide-based thin-film transistors. However, during the studies of the electronic properties of the binding material, i.e. Zn-ammine complex, had shown even greater potential to accomplish this goal on its own. This Zn-based metal-ammine complex is prepared from an aqueous route, which allows for the growth of ultra-thin (4–5 nm), high-quality polycrystalline ZnO films on a large scale. Transistors fabricated using this approach show electron mobilities of up to ≈ 11 cm^2/Vs at ≤180 °C. Further reduction in the processing temperature <90 °C are achieved with a UV light photo-activation step. Moreover, flexible ZnO transistors utilising high-κ materials as the gate dielectric are manufactured on plastic foils and exhibit electron mobility of >4 cm^2/Vs with a channel current on/off ratio of $>10^4$.

5.2 Review on Zn-ammine complex-based electronics

5.2.1 Pioneers of aqueous-based precursors for ZnO TFTs

The very first demonstration of the use of inorganic aqueous ink for the fabrication of oxide-based electronic devices can be traced back to the work published by Meyers et al. in 2008 [111]. Zn-ammine complex was synthesised from the reaction of Zn nitrate hexahydrate with sodium hydroxide in distilled water to form Zn hydroxide [$Zn(OH)_2$] precipitate, followed by dissolving the precipitate in ammonia solution [111]. With this precursor solution, the authors demonstrated ZnO TFTs on Si^{++}/SiO_2 wafers using the deposition techniques of spin casting and thermal ink-jet printing. Under a thermal calcination temperature of 300 °C, the obtained ZnO TFTs exhibited saturation mobilities of 3.1~4.6 cm^2/Vs and an on/off ratio of 10^6. In 2008, such a result was a milestone for low-temperature solution-processed metal oxide TFTs, and similar performance was not achieved until 2011 when the combustion methods (i.e. exothermic reactions) and alkoxide-based precursor systems were proposed by Marks' group at Northwestern University (USA) and Sirringhaus' group at University of Cambridge (UK), respectively, further decreasing the process temperatures [106, 107].

However, 300 °C is still too high to fabricate electronic devices on temperature-sensitive substrates such as inexpensive plastic materials. The Zn-ammine-complex solution, in principle, is likely converted at much lower temperatures since its decomposition only involves water and volatile ammonium hydroxide. In addition, during the thermogravimetric analysis (TGA) measurement on the precipitate obtained from the dehydrated Zn-ammine-complex solution, there was only a mass loss of <1.5% observed in the temperature range between 50 °C and 600 °C (at a rate of 10 °C/min) [111]. This finding, i.e. no significant mass loss at a certain temperature range, indicates that thermal calcination should not be that critical for the conversion of the complex solution. Meyers and his colleagues then tried to reduce the process temperature down to 150 °C, but the TFT current-voltage characteristics exhibited larger hysteresis and lower mobilities [111]. Therefore, more efforts were required to achieve plastic-friendly deposition temperatures. In spite of this

disappointment, it was found in the same study that as-prepared devices showed better performance when carrying out the post-fabrication thermal-annealing process under an inert gas flow [N_2(g) or Ar(g)] in a tube furnace. This interesting finding provided valuable information on the fabrication process conditions and was subsequently realised to be a critical step for the development of low-temperature (<180 °C) high-mobility ZnO transistors [112].

A similar study on oxide TFTs using the Zn-ammine complex chemistry was carried out by Theissmann et al. in 2011 [113]. The starting material used for the formation of the complex was ZnO hydrate ($ZnO \cdot xH_2O$), and the preparation involved simply dissolving this material in an aqueous ammonia solution. This one-step process greatly reduces the complexity of the tedious material preparation, synthesis and purification mentioned in the first study by Meyers et al. [111]. This is in fact not a new chemical route but it derives from a known chemical reaction (i.e. ligand exchange) in coordination chemistry. To make this point clearer, the reaction will be revisited in detail in the later sections. In the work of Theissmann et al. [113], the deposition technique used was spin casting, and Zn-ammine complex was processed at a series of different temperatures. To push the Zn-ammine-complex approach to the limit of thermal calcination, the working ZnO TFTs were successfully demonstrated at a temperature of only 125 °C, and the best devices exhibited a moderate mobility of 0.25 cm^2/Vs and a large on/off ratio of 10^6. In addition, the authors pointed out that a double deposition/formation process of the oxide layer is a key to higher-performing devices. This finding is actually in line with other studies on how to accomplish a highly-dense film with a double/multiple deposition process [114, 115], and similar results have also been discussed in the previous chapter on NP-based devices (see Chapter 4 and ref. [95]). Using this approach, Theissmann et al. [113] obtained an oxide layer of thickness of ~7 nm. On the other hand, with just one deposition process the obtained device performance was lower since it might not form a continuous and/or highly-dense layer. From the device characteristics, it is surprising that such a thin layer of only few nanometres, especially in contrast to the work of Meyers et al. [111] in which a thickness of nearly 100 nm was used, is enough for excellent charge transport, and hence highly-functional transistors. The

use of such a thin metal oxide layer is adapted in this chapter and its full potential will be explored and discussed in the following sections.

Interestingly, both of these two pioneering works explored the device performance at high processing temperatures, but controversial results were reported. In the work of Meyers et al. [111] the channel became highly conductive when thermal annealing process was carried out >300 °C, and the conductivity kept increasing with the increase in annealing temperatures. However, Theissmann et al. [113] observed the opposite trend where a significant drop in mobility values was recorded for annealing temperatures >350 °C. In the latter case, it was believed that a crystallisation process took place at elevated temperatures and then caused the decrease in film smoothness and homogeneity as seen in the TEM image of a chunky ZnO crystallite found in the oxide film annealed at 500 °C. From this point of view, since the active channel was composed of a few nanometre-thick layer, formation of such a crystallites could possibly induce aggregation of the material, which might result in films with non-uniform features, and hence negatively impacting the charge-transport. This phenomenon is in agreement with the studies carried out in this chapter and Chapter 6, and further discussions on the impact of film smoothness on device performance will be presented later [112]. On the other hand, it should not be a surprise that Meyers and his colleagues observed the behaviour of increased conductivity in a rather thick film whilst a higher process temperature was used; this is because higher annealing temperatures could lead to the formation of higher density of oxygen vacancies under a condition that there is no concern of homogeneity and uniformity in the films [111, 116].

5.2.2 Additional studies based on Zn-ammine complex chemistry

The promising results were achieved when Zn-ammine complex was used for the fabrication of ZnO transistors for the first time [111]. Since then, there have been an increasing number of research works using this approach to explore its potential for practical applications in large-area flexible electronics [117-121], and the search for low-thermal-budget precursors could eventually end here. Fleischhaker et al. made the

first attempt to fabricate flexible devices using Zn-ammine complex as the precursor for the active material [122]. In this work, the process temperature was kept under 150 °C in order to process the materials on polyethylene naphthalate (PEN) foils. Although the transistors made on the rigid substrates (Si/SiO_2 wafers) exhibited a mobility of 1.2 cm^2/Vs, similar performance was not achievable from the transistors fabricated on plastic foils, and the mobility dropped by two orders of magnitude. This dramatic decrease in performance was attributed to the incompatibility between the ZnO film and the organic polymer dielectrics, diminishing the crystallisation of ZnO, and hence lowering the electron mobility of these plastic devices.

The low conversion temperature of Zn-ammine complex was supported by the initial TGA measurement carried out by Meyers et al. [111], in which there was only 1.5% mass loss been observed. However, in contrast to this, when Jun et al. [123] carried out the TGA tests on the as-coated Zn-ammine-complex thin-film layers, there was mass loss of 8% and 5% that can be identified at 134 °C and 240 °C, respectively. The cause of the former was attributed to the dihydroxylation, and for the latter the loss of mass was owing to the decomposition of Zn-amine complex. The current-voltage characteristics obtained from the devices made with the thermal-annealing process in ambient atmosphere exhibited non-negligible hysteresis and low mobility. As such, the authors proposed an alternative method for improvement, which was carrying out the annealing process in a closed system equipped with microwave radiation (2.45 GHz). In this way, the field-effect mobility was increased by a factor of 3–6 [123]. Meanwhile, it was found that, with the assistance of microwave, the grain size was twice as large as that prepared in ambient environment. Therefore, the improvement in the device performance was attributed to a better charge transport pathway through the larger crystalline domains.

Although there is still a lot of room for improvement on the performance of plastic devices based on the use of Zinc-ammine complex, the development of this Zn-based metal-ammine complex for the applications in low-temperature flexible electronics is highly promising. In the following sections, the discussion will focus on the approach adapted in this work for achieving high-performance ZnO transistors (>10 cm^2/Vs) on both rigid substrates and plastic foils using a simple low-temperature solution-based process.

5.3 ZnO film growth and device fabrication

5.3.1 Dissolution of precipitate: a ligand-exchange reaction

An inorganic complex is defined by the following description: an inorganic molecule contains several atoms that includes one or more metal atoms [124]. Due to the availability of *s*, *p* and *d* orbitals in the electronic structures of the transition metals, it has been found that this characteristic leads to the formation of stable complexes of these types of materials [124]. As such, in aqueous solutions metals exist not only a hydrated form but also in the form of other types of complexes with different ligands, depending on presence of other chemical elements and type of metals.

For the solubility of ZnO or Zn hydroxide in aqueous ammonia solution, the presence of ammonia groups leads to the following reaction:

$$Zn^{2+} + 4NH_3 \rightleftarrows Zn(NH_3)_4{}^{2+} \tag{5.1}$$

where Zn^{2+} is used for the expression of the ion species $Zn(H_2O)_4{}^{2+}$ to simplify the equation. When there is sufficient amount of ammonia in the solution, Zn could exist in the form of Zn-ammine complex instead of forming the precipitate of Zn hydroxide. On the other hand, Zn ions could also form Zn-hydroxide complexes in aqueous solutions [124] as shown in the following reactions

$$Zn^{2+} + 2OH^- \rightleftarrows Zn(OH)_2 \tag{5.2}$$

$$Zn(OH)_2 + 2OH^- \rightleftarrows Zn(OH)_4{}^{2-}. \tag{5.3}$$

Therefore, these three chemical equations govern the dissolution of the Zn hydroxide precipitate, and depending on the *p*H value of solutions different Zn complexes could co-exist at the same time in the solutions.

5.3.2 Material preparation, film deposition and device fabrication

In principle, Zn-ammine-complex solution can be prepared from any type of ZnO products or Zn hydroxide derivative, such as ZnO nanoparticle powder, hydrated ZnO, Zn hydroxide, etc. [120], with aqueous ammonia solution following the condition that sufficient ligands are present to prevent the formation of Zn hydroxide precipitate. In this chapter, the chosen material for the Zn-ammine-complex solutions was ZnO hydrate ($ZnO \cdot H_2O$, 97% Sigma-Aldrich). The metal ammine complex solution was prepared by dissolving the ZnO hydrate precursor in ammonium hydroxide (28–30%, Sigma-Aldrich) to molar concentrations in the range of 0.03–0.09 M [112]. The solutions were then stirred rigorously at room temperature for 4–6 h, and this process yielded a clear transparent solution.

The as-prepared Zn-ammine-complex solution was spun onto the solvent/O_3 cleaned quartz or Si/SiO_2 substrates at 3000 rpm for 30 sec in air or nitrogen environment (O_2, H_2O <10 ppm), followed by thermal annealing for 1 h at temperatures between 80–180 °C in the same environmental condition. The ZnO film deposition cycle was carried out 2–3 times in order to form dense and continuous layers. For the fabrication of the ZnO TFTs, the device structures were completed with the thermal evaporation of 50 nm-thick Al top source-drain (S-D) electrodes through shadow masks.

5.4 ZnO film and device characterisations

5.4.1 Optical properties of ZnO thin-films

The optical properties of ZnO films fabricated at different annealing temperatures (90–180 °C in nitrogen environment) as well as as-spun Zn-ammine complex were investigated using UV-Vis-NIR spectroscopy. A complex solution with a molarity of 0.07 M was used here and in the following sections, unless stated otherwise. The reason for this will be further discussed later in Section 5.4.4. The obtained transmission spectra of the films (on quartz substrate) and the blank substrate are

shown in Figure 5.1. Unlike the as-spun film, which appears to be highly transparent without strong absorption features, the oxide films annealed at 90–180 °C show an onset absorption at around 380 nm, which is in agreement with other studies on ZnO optical properties [43].

It is worth mentioning that the films exhibit substrate-corrected transparency (400–1400 nm) of ≥97%, which indicates the film thickness is likely to be extremely thin. This point will be confirmed in the following section by TEM-based technique. On the other hand, the films annealed in different environmental conditions (i.e. either nitrogen or ambient environment) exhibit similar absorption characteristics without significant difference.

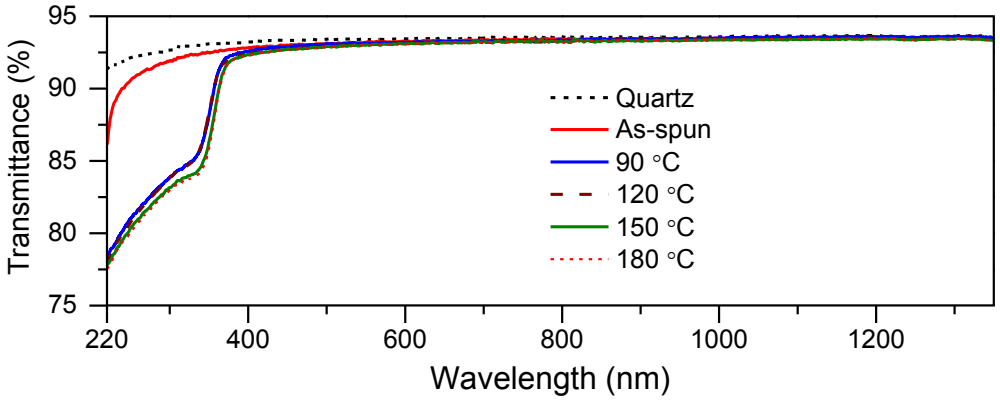


Figure 5.1: UV-Vis-NIR transmission spectra measured for the blank substrate used (quartz), the as-spun Zn-ammine complex film (without thermal annealing) and the ZnO films after annealing at 90, 120, 150, and 180 °C in nitrogen environment.

5.4.2 Microstructural analysis of ZnO thin-films

To gain further insights into the microstructural properties of the ZnO films, HRTEM was used to analyse the nanostructure and elemental composition of the oxide films. Figure 5.2 displays a series of HRTEM images (lower to higher magnification from left to right) of the SiO_2/ZnO cross-section revealing the presence of polycrystalline ZnO domains for which the lattice spacing of ≈ 0.244 nm can be extracted. This finding agrees with the X-ray diffraction measurements reported by Cho et al. [125], which showed that the ZnO films using the same aqueous approach exhibited a similar crystalline-like phase.

Though the process carried out here is somewhat similar to the work by Theissmann et al. [113], the obtained thickness of the oxide layer is however further reduced by 50% (from ~7 nm down to ~4 nm). Despite the fact that material condensation is likely to take place during thermal-annealing process in a solution-based procedure, the ultra-thin (≈4 nm) nature of these solution-processed ZnO films still appears to be extremely uniform and continuous across the entire substrate surface (see Figure 5.2). Most importantly, this low-dimensional feature has opened up an opportunity for realising quantum-based electronic devices (devices that explore energy quantisation phenomena) using solution-processable metal oxide materials for the first time [126].

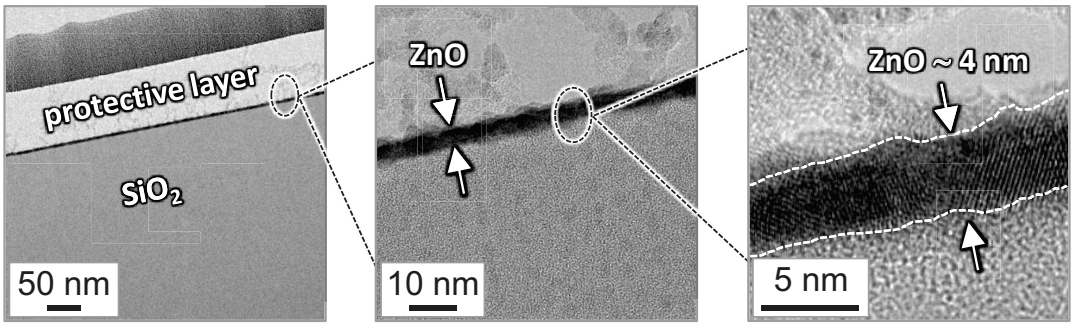


Figure 5.2: HRTEM images of the SiO_2/ZnO cross-section: from low magnification (the leftmost panel) to high magnification (the rightmost panel). White dash lines are guides to the eye.

5.4.3 Impact of process environment on device performance

As seen and confirmed from the TEM results (Figure 5.2), the ZnO films exhibit polycrystalline features, and it is well known that in these types of materials grain boundaries can have a significant great impact on the property of charge transport [78, 127-130]. As such, before looking into how the processing environment could affect current-voltage characteristics in transistors, the oxide films prepared in different environments were first studied using AFM. Figures 5.3(a) and (b) show surface topography images for ZnO films spin-casted and deposited from a 0.07 M complex solution onto the Si^{++}/SiO_2 substrates at room temperature followed by thermal annealing at 180 °C in both nitrogen and ambient air. Both films feature very smooth surfaces with the root-mean-square surface roughness (R_{RMS}) values of 0.46 nm and

0.51 nm for films annealed in nitrogen and ambient air, respectively. In addition, there only exists minor difference in the height distribution for both of the films [Figure 5.3(c)]. Despite their similar R_{RMS} values, further analysis of the AFM images in Figure 5.3(a) and (b) reveals significant differences in the grain sizes between the ZnO films prepared in the different environments. In particular, the number of grains — estimated directly from Figure 5.3(a) and (b) — is approximately 30–40% lower for the film annealed in nitrogen than that for the film annealed in air. Such a result could have notable impacts on charge transporting properties as discussed in Section 5.2.2 and ref. [122] where the improved device performance was observed from the ZnO films with larger gain sizes.

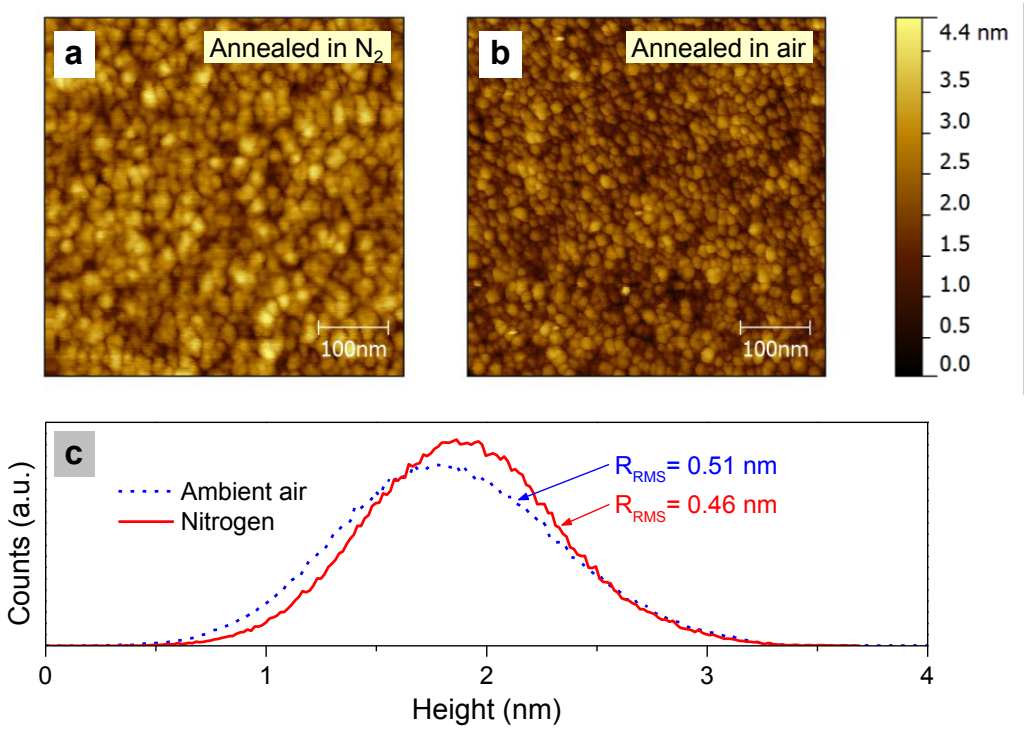


Figure 5.3: AFM topography images of ZnO films spin-casted on Si/SiO_2 substrates followed by thermal annealing in nitrogen (a), and ambient air with relative humidity ≈50% (b). (c) Statistical distributions of surface height and associated root mean square surface roughness (R_{RMS}) calculated from the ZnO AFM images shown in (a) and (b). All ZnO films were prepared using a 0.07 M concentration of Zn-ammine-complex solution.

To further understand the impact of the film morphology on long-range charge transport in these ZnO films, they were investigated using TFTs based on a bottom-gate, top-contact (BG-TC) architecture (see Section 5.3.2 for details). Figure 5.4(a) displays a set of representative transfer characteristics for ZnO TFTs annealed at 180

°C in nitrogen and ambient environment. Compared to ZnO transistors prepared in air, the field-effect mobility extracted is increased by a factor of 3–4 (a maximum value was measured of ≈ 11 cm^2/Vs) whilst the turn-on voltage (V_{ON}) is found to shift towards a more negative gate bias. This phenomenon suggests that there might be a higher concentration of free electrons present in the film [95]. This could be attributed to the presence of fewer grain boundaries, which not only leads to better charge transport but also attracts less oxygen at/on the surface of the film, since grain boundaries are generally considered to behave like electron trapping sites [131, 132].

To gain better insights into the differences of charge transport between the two ZnO film morphologies, the gate-dependent field effect mobility (μ_{FE}) has been analysed using the following formula:

$$\mu_{FE} = K(V_G - V_{T,P})^{\gamma} \tag{5.4}$$

where V_G, V_T, and V_P are gate bias, threshold and percolation voltages, respectively, chosen with the appropriate values for K and γ [133]. From the empirical data collected from a typical TOS-based device, it is found that a γ value close to 0.7 would indicate a trap-limited charge (TLC) transport process whilst a value close to 0.1, transport mechanism is dominated by a percolation conduction (PC) process [133].

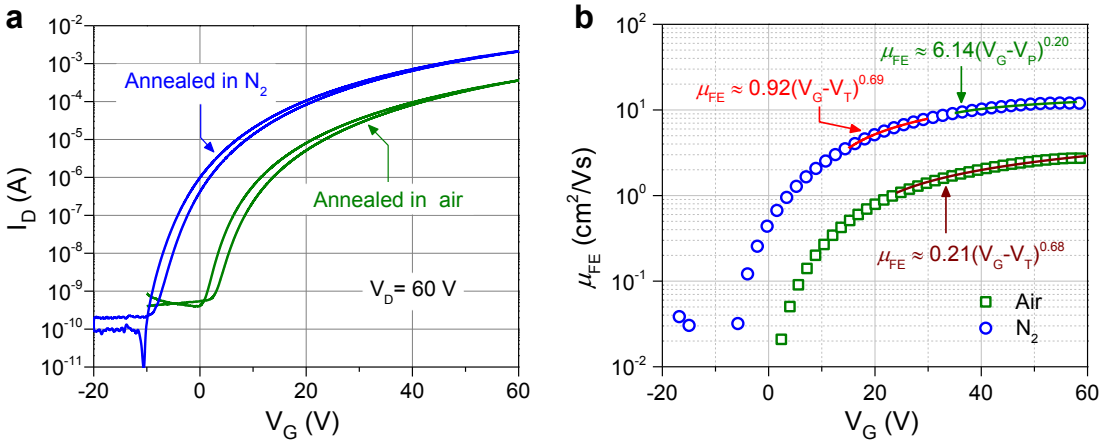


Figure 5.4: (a) Transfer characteristics of ZnO transistors (channel width/length = 1000 µm/50 µm) fabricated in nitrogen and ambient air. (b) Field-effect mobility (μ_{FE}) as a function of gate voltage (V_G) calculated directly from the transfer characteristics in (a) using Equation 5.1. Open symbols are experimental data whilst lines represent the fitting.

Figure 5.4(b) displays the fits of Equation 5.4 to the transfer characteristics shown in Figure 5.4(a). For transistors annealed in air, the charge transport appears to be dominated by the TLC mechanism since $\gamma = 0.68$ is obtained across the entire operation voltages. On the other hand, for the devices annealed in nitrogen there exist two different regimes with the exponent γ dropping from 0.69 at $V_G < \sim 30$ V, down to 0.20 at $V_G > \sim 30$ V. These results suggest that electron transport in ZnO transistors prepared in nitrogen could be first dominated by TLC then by the PC mechanism at higher gate voltages [133]. In other words, the traps can be filled much quicker in these devices. This difference observed in the charge transport mechanism between ZnO films annealed in nitrogen and those in air, is in agreement with the findings in the film morphology [Figures 5.3(a) and (b)]. This is, as stated before, because the presence of more grain boundaries in the oxide film is likely to trap more charge carriers and hence result in poorer charge transport. The same reason could be considered as a valid explanation for similar observations seen in the ZnO transistor characterisations from the study of Meyers et al. [111].

5.4.4 Impact of precursor concentration on device performance

As reported in recent studies [113, 114], precursor concentration could have a strong impact on the current-voltage characterisations in a transistor. In this section the dependence, if any, of the device performance on concentrations of Zn-ammine-complex solutions is investigated. A range of solution molarities (0.03–0.08 M) was used to study its impact on ZnO TFT performance. Using the Si/SiO_2 substrates and the experimental procedure described in Section 5.3.2 for the TFT fabrication, the transfer characteristics measured from each TFT are shown in Figure 5.5. The important device performance parameters (i.e. onset voltage V_{ON}, saturation mobility μ_{SAT}, subthreshold slope S.S., and drain current on/off ratio I_{ON}/I_{OFF}) are summarised in Table 5.1.

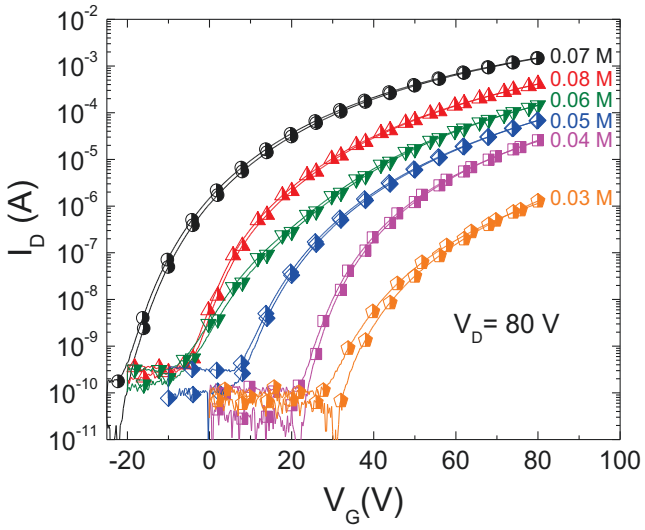


Figure 5.5: Influence of Zn-ammine complex concentrations on the transfer characteristics of ZnO TFTs. The optimum performance is obtained from films prepared at 0.07 M.

Table 5.1: Summary of ZnO TFT performance parameters processed from different precursor concentrations as shown in Figure 5.5.

Molarity (M)	μ_{SAT} (cm²/Vs)	I_{ON}/I_{OFF}	V_{ON} (V)	V_T (V)	S.S. (V/dec)
0.03	0.02	1×10^4	27.2	53.8	5.99
0.04	0.24	2×10^5	20.8	44.0	3.74
0.05	0.48	5×10^5	7.8	29.3	4.00
0.06	1.17	1×10^6	-5.5	22.6	5.51
0.07	5.56	1×10^7	-14.5	6.7	1.78
0.08	2.72	3×10^6	-3.3	18.1	1.97

As can be seen, the mobility increases monotonously whilst increasing solution concentration from 0.03 M to 0.07 M, and reaches a maximum value of 5.56 cm²/Vs at 0.07 M. Further increase in the solution concentration (e.g. 0.08 M) is found to degrade the performance with the electron mobility reducing significantly. Apart from electron mobility, the same trends also appear in other transistor parameters. From these measurements one can conclude that optimum performance is obtained from devices prepared using a precursor solution concentration around 0.07 M.

In order to further understand these results, the ZnO film morphology, obtained from different solution concentrations (0.03, 0.05, 0.07, and 0.09 M), was

investigated using AFM. The recorded phase images are depicted in Figure 5.6 whilst the surface roughness R_{RMS} are obtained of 0.31, 0.36, 0.45, 0.47 nm for the solution concentrations of 0.03, 0.05, 0.07 and 0.09 M, respectively. All of them are very smooth, but there does exist some difference in the surface features. In Figure 5.6 grain boundaries for films processed using solution concentrations 0.05–0.09 M, can be observed; for the concentration 0.03 M, few large crystals were formed and the surface feature does not look similar, even in the 1 μm 1 μm scanning area resolution. Therefore, the film might not have good coverage over the entire device area, and this is most likely due to an inadequate amount of material for full coverage of the entire substrate surface.

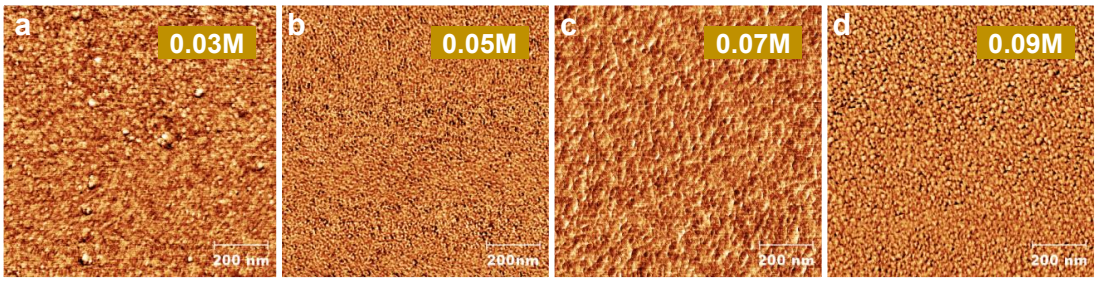


Figure 5.6: AFM phase images of different Zn-ammine complex concentrations: from 0.03 M to 0.09 M.

More interestingly, the optimum ZnO film that shows smooth surface morphology with larger grains was obtained from the concentration of 0.07 M, in which the transistors have also shown the best performance among the series of different solution concentrations. In polycrystalline-channel TFTs, the magnitude of the electrostatic barrier resulting from electron-trapping defects localised at grain boundaries causes difficulties in carrier transport [128]. As such, when fewer grain boundaries are present within the channel area, the device is expected to show improved performance. Indeed, the present findings are in agreement with this assumption since optimum device performance is obtained from films showing the largest crystalline domains. The surprising observation from these measurements is that once the concentration reaches the solubility limit, it cannot form a denser film, losing the potential of forming a film comprised of larger ZnO crystalline grains [114]. The increase in porosity leads to poor charge transport and the decrease in

transistor performance. The possible reason could be attributed to poor film morphology formed during thermal annealing. Once as-deposited films are placed on a pre-heated hot plate, the volatile ammonia groups are most likely evaporated much faster than the ZnO crystals are formed. Such a process causes more nucleation sites, and hence the crystallization of Zn complex with smaller grain sizes (this effect appears to be a preferable process at high solution concentrations). In our case, the optimised concentration was found to be around 0.07 M for the specific experimental conditions. However, this speculation is only based on the result from the AFM measurements, and this point could be further supported using complementary characterisation methods such as X-ray diffused scattering for the measurements of film density and/or other microstructure analysis techniques.

5.4.5 Impact of process temperature on device performance

As discussed earlier in this chapter, mass loss of as-deposited Zn-ammine complex is nearly non-observable across a wide range of temperatures during the TGA measurement [111], and numerous studies have supported this observation and shown full ZnO conversion and formation are expected to take place at <200 °C [113, 117, 118, 121, 122]. To explore the lower limit of the conversion temperature for Zn-ammine complex, device performance is investigated at different annealing temperatures. Figure 5.7(a) displays a set of transfer characteristics measured under high vacuum (10^{-5} mbar) for several un-encapsulated ZnO transistors annealed between 100–180 °C in nitrogen environment. The overall improvement in electron transport is better illustrated in Figure 5.7(b) where the electron mobility, measured from several transistors, is plotted as a function of annealing temperature. In addition, the films annealed at higher temperatures lead to higher channel current on/off ratios, lower threshold voltages and smaller sub-threshold swing, and all of these indicate a significant improvement in electron transport [Figure 5.7(c)–(e)]. Although the ZnO TFT annealed at 100 °C shows the lowest performance, it still exhibits an appreciable field effect with high modulation in channel current. Most importantly, the temperature range examined here (100–180 °C) is fully compatible for processing most of flexible/plastic substrates.

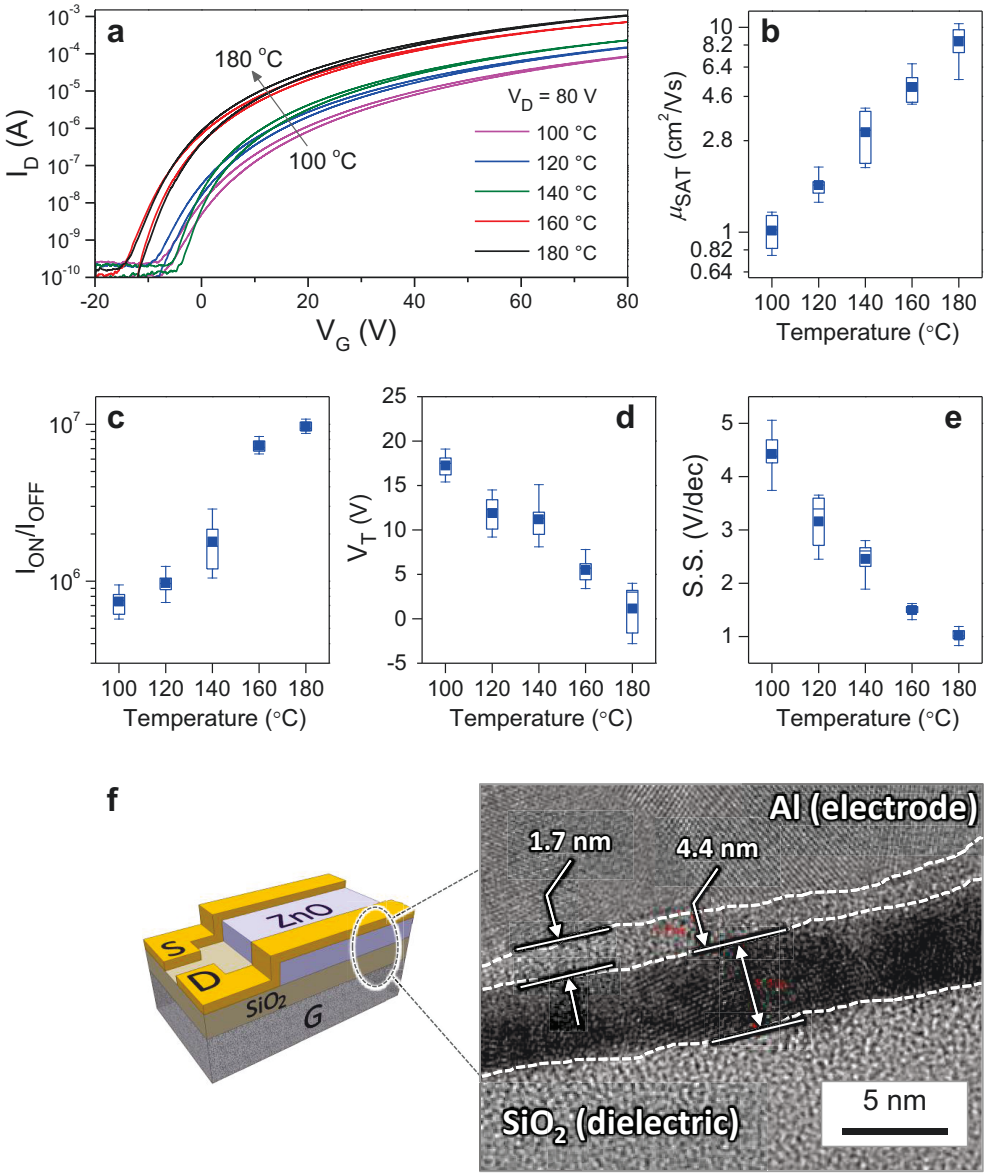


Figure 5.7: (a) Transfer characteristics of solution-processed ZnO transistors annealed at temperatures in the range of 100–180 °C. (b), (c), (d) and (e), respectively, show evolution of the saturation mobility (μ_{SAT}), drain current on/off ratio (I_{ON}/I_{OFF}), threshold voltage (V_T) and subthreshold swing (S.S.) with annealing temperature. The data were acquired from several devices. (f) HRTEM image of the SiO_2/ZnO/Al cross-section from a ZnO transistor revealing the ultra-thin nature of the ZnO film as well as the formation of a thin (≈1.7 nm) AlO_X layer between the Al electrode and ZnO. White dashed lines in (f) are guides to the eye.

Thanks to the nature of the Zn-ammine complex, it is possible to convert this material at low temperatures. Additionally, an ultra-thin layer composed of high-quality polycrystalline ZnO could play an important role and serves as an excellent charge-transporting platform. This point is illustrated in the HRTEM cross-section

image of an Al/ZnO/SiO_2 interface of a BG-TC transistor shown in Figure 5.7(f). Analysis of the HRTEM data reveals the presence of polycrystalline ZnO regions with clearly visible lattice fringes (similar to Figure 5.2) in the regions located underneath the Al S-D electrode. Elemental analysis of the cross-section, also reveals the formation of an ultra-thin (1.7 nm) layer of AlO_X in close proximity to the Al/ZnO interface. A likely cause responsible for this, in addition to oxygen diffusion from oxide layers, could be attributed to the oxidation taking place during transistor characterisations. The latter is because the channel current could generate large amounts of heat whilst passing through the area where the electrode and semiconductor overlap [134]. It should be noted that this AlO_X appears not to affect electron injection (to a great extend) from the electrodes to the ZnO layer owing to its ultra-thin and non-stoichiometric nature.

5.5 Low-voltage high-performance ZnO transistors

5.5.1 Process and characterisation of high-κ gate dielectrics

The increasing density of electrical elements and devices in a single electronic product has caused some concerns regarding ever rising power consumption and consequent heat dissipation [135-138]. The use of high-κ dielectric materials to reduce operation voltages will be important for the future design of field-effect devices [44, 139]. Furthermore, with low-cost deposition techniques the applications of these high-κ materials could also benefit large-area electronic in the near future. In this section, UV light-assisted and solution-processed high-κ dielectrics are introduced and characterised, followed by their application in low-voltage ZnO transistors.

During initial attempts, the experiments focused on irradiating evaporated Al gate electrodes with a low-pressure mercury UV lamp, which emits at wavelengths of 253.7 nm (97% of overall power) and of 184.9 nm (3% of overall power) at total output power of approximately 5 mW/cm^2 in a distance of 2 cm, to accelerate the growth of the native AlO_X layer on the surface of Al. The entire UV irradiation process was performed in ambient environment and lasted for 12 h. For

characterisation of the AlO_X dielectric, a metal-insulator-metal (MIM) structure was made on glass with Al metal electrodes to obtain its geometric capacitance (C_i) value. Figure 5.8 displays the result from the capacitance-frequency measurement using impedance analyzer, and a value of 2 μF/cm^2 was measured for the AlO_X dielectric layer. Using the thickness obtained from the TEM measurement [see Figure 5.9(a)], the dielectric constant was calculated to be approximately 9. A similar approach was carried out using oxygen plasma to grow a thin Al_2O_3 layer as the gate dielectric in pentacene-based TFTs [140]. However, those devices exhibited low on/off ratios, and such a result most likely indicated there existed high leakage through the self-grown Al_2O_3 layer.

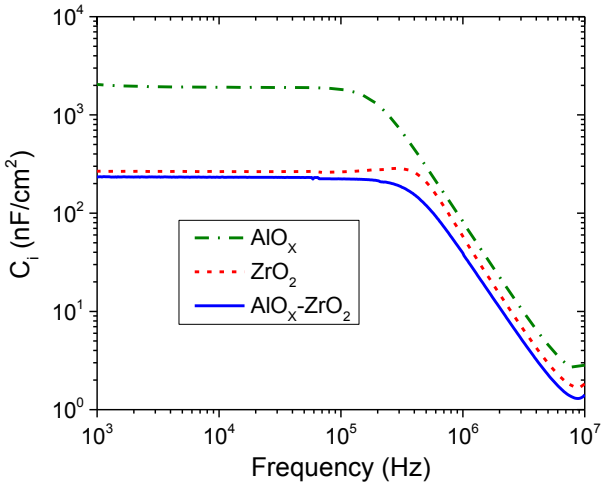


Figure 5.8: Geometric capacitances measured for the AlO_X, ZrO_2, and AlO_X/ZrO_2 dielectrics as a function of small AC signal frequency. Geometric capacitances of 2 μF/cm^2, 267 nF/cm^2 and 235 nF/cm^2 are measured for AlO_X, ZrO_2, and AlO_X/ZrO_2 hybrid dielectrics, respectively. Characterization was carried out using the MIM (Al/dielectric/Al) structure with impedance analyser.

Another approach used in this study is based on the work by Park et al. [141, 142]. A ZrO_X precursor solution was synthesized by dissolving Zr(IV) acetylacetonate [$Zr(C_5H_7O_2)_4$)] (98%, Sigma–Aldrich) in N,N-dimethylformamide, (DMF, C_3H_7NO) (99.8%, Sigma–Aldrich), at a concentration of 0.2 M in inert gas atmosphere with the addition of an equal molar concentration of ethanolamine (MEA, C_2H_7NO) (≥99%, Sigma–Aldrich). The solution was stirred at 70–80 °C for 1 h in order to enhance hydrolysis. The ZrO_2 film was deposited by spin-coating the precursor solution at 3000 rpm for 60 sec in nitrogen followed by curing the samples using a metal halide

lamp of 250 mW/cm^2 with an UVA spectrum filter for 90 min in ambient air. To enhance dielectric strength, a hybrid high-κ dielectric was also developed by first growing an AlO_X layer of 4–5 nm on top of Al followed by depositing ZrO_2 precursor onto this AlO_X layer. The current-voltage characterisations for the corresponding transistors will be presented later. Using MIM structures, C_i is obtained of 267 nF/cm^2 and 235 nF/cm^2 (Figure 5.8) for ZrO_2, and AlO_X/ZrO_2 hybrid dielectrics, respectively. For ZrO_2, the film thickness of 20~25 nm was determined using AFM. The dielectric constant of ZrO_2 was then calculated yielding ~9.05 — a value similar to those reported previously [117, 141, 142].

5.5.2 Electrical characterisation of low-voltage ZnO transistors

For AlO_X-based low-voltage ZnO transistors, 40 nm-thick Al gate electrodes were thermally evaporated under high vacuum onto glass substrates, followed by the UV-assisted self-grown process as described earlier. The ZnO layer was then grown by spin casting of the precursor solution (0.07 M) followed by thermal annealing at 180 °C in nitrogen. Device fabrication was completed with the deposition of top Al S-D electrodes directly onto ZnO by thermal evaporation in high vacuum. Figure 5.9(a) shows the HRTEM cross-section image of a representative $Al/AlO_X/ZnO$ stack prepared by this method. The thickness of ~4.4 nm and ~3.9 nm was obtained for AlOx and ZnO, respectively. Figure 5.9(b) shows the transfer characteristic for a ZnO TFT based on the UV-grown AlO_X dielectric. The device exhibits clear n-channel behaviour with a maximum electron mobility of ≈9 cm^2/Vs and channel current on/off ratio in the range 10^2–10^3. The relatively low value of the on/off ratio is attributed to the significant gate leakage current. As discussed in the previous section, similar results were obtained by Kim and Song [140]. In spite of the high off-current level, the operation of ZnO transistors in such small ranges (±1.2 V) demonstrates the potential and capability of establishing low-power electronic technologies.

The high leakage current in AlO_X could be a result of its imperfect atomic structures and the thin layer (~4.4 nm). In an effort to reduce gate leakage current to a lower level, the hybrid high-κ dielectric of an AlO_X/ZrO_2 film stack, as described

previously, was used as the gate-dielectric layer in ZnO TFTs. Figure 5.9(c) displays typical transfer characteristics measured for a low-voltage ZnO TFT based on the hybrid high-κ AlO_X/ZrO_2 dielectric. As expected, the obtained devices exhibit lower gate leakage current, by more than one order of magnitude, as well as a higher electron mobility (≈ 11 cm^2/Vs) whilst the current on/off ratio has been increased by one order of magnitude and obtained of ~10^4. Similar mobility enhancement has been reported recently for solution-processed transistors based on the combination of oxide semiconductors and high-κ oxide dielectrics [44, 107, 139]. Therefore, the finding in the present study can be attributed to an improved interface formed between the polycrystalline ZnO and the dielectrics.

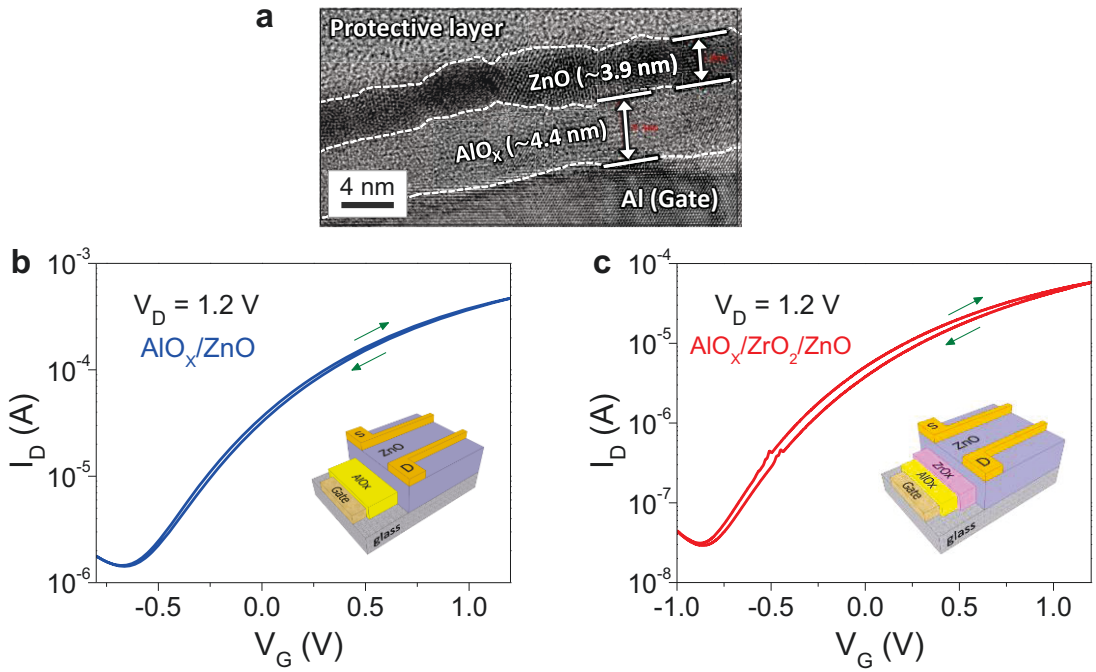


Figure 5.9: (a) HRTEM image of a low-voltage ZnO TFT with AlO_X as the gate dielectric cross-section revealing the existence of a ≈4.4 nm thick layer of AlO_X formed onto Al gate electrode upon UV irradiation in ambient air. White dashed lines are guides to the eye. (b) Transfer characteristic measured for a ZnO transistor based on a UV-assisted self-grown AlO_X layer as the gate dielectric. (c) Transfer characteristic measured for a ZnO transistor based on a hybrid high-κ AlO_X/ZrO_2 film stack as the gate dielectric. In both devices the ZnO layer was annealed at 180 °C in nitrogen followed by the deposition of Al S-D electrodes. Insets: Schematics of the device architectures employed.

One of the advantages of using this high-κ AlO_X/ZrO_2 film stack is that the entire fabrication is a thermal-annealing free process, and it could easily be applied to devices made on temperature-sensitive substrates like plastic foils. However, the UV

lamp used for ZrO_2 conversion is relatively powerful, so an unintentional heating effect elevated the process temperature to 80–90 °C. Nevertheless, this is still far below temperature tolerances for most of plastic foils. Moreover, the use of this oxide-based dielectric provides a highly flexible method allowing control of the surface energy, which is crucial for solution-based deposition techniques.

To demonstrate the compatibility of this technology with temperature-sensitive substrates, ZnO TFTs using AlO_X/ZrO_2 as gate dielectric were fabricated on flexible PEN films. To ensure that the mechanical properties of the PEN substrates were not compromised during the process, the thermal-annealing temperature was carefully monitored and maintained at 160 °C. Figure 5.10(a) and (b), respectively, show a set of the transfer and output characteristics obtained from a flexible low-voltage ZnO transistor, whilst Figure 5.10(c) displays a photograph of the flexible transistor arrays containing >35 ZnO TFTs fabricated on a PEN substrate. The transistors exhibit excellent operating characteristics with electron mobility in the range of 4–5 cm^2/Vs, channel current on/off ratio of $>10^4$, threshold voltage close to 0.05 V and a small sub-threshold swing of ≈ 100 mV/dec. The work here demonstrates that the proposed materials are not only suitable for low thermal-budget fabrication process, but that high performance can also be delivered without any limitation on substrate choice, even using plastic foils.

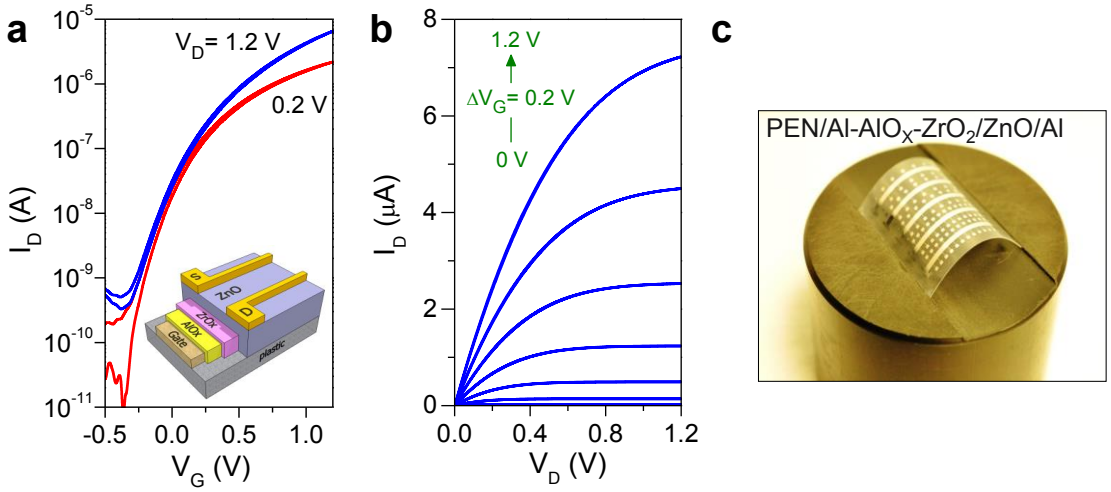


Figure 5.10: Transfer (a) and output (b) characteristics measured for a ZnO transistor based on a hybrid high-κ AlO_X/ZrO_2 gate dielectric and Al source-drain electrodes. Inset in (a): Schematic of the bottom-gate, top-contact transistor architectures used here. The entire device was fabricated on PEN substrates with the ZnO layer annealed at 160 °C. (c) Photograph of an actual transistor array containing >35 flexible ZnO TFTs.

5.6 ZnO transistors via UV light conversion

In an effort to explore a method for further reducing processing temperatures, UV irradiation was used as a post-deposition step instead of the conventional thermal annealing for the conversion of the Zn-ammine complex. The UV system used for oxide precursor conversion utilises the combination of a low-pressure mercury lamp and a metal halide lamp with a UVA filter, which yields an irradiation with a range of wavelengths from ~185 nm to ~400 nm. After the Zn-ammine complex was deposited onto the Si/SiO_2 substrates (see Section 5.3.2), the samples were placed in this system for 1 h in ambient environment. In order to form dense and continuous ZnO films, the spin casting and UV irradiation steps were repeated for 2–3 times. The sample temperature during UV curing process was monitored and found to vary between 80–90 °C. TFT fabrication was completed with the deposition of top Al S-D electrodes through shadow masks under high vacuum. A representative set of the transfer characteristics measured from the UV-converted transistors is shown in Figure 5.11. The devices show comparable performance, in terms of electron mobility (~1.0 cm^2/Vs), with those produced by thermal annealing at 100 °C (>1.0 cm^2/ Vs), whilst they outperform those produced by annealing at 90 °C (<0.3 cm^2/ Vs).

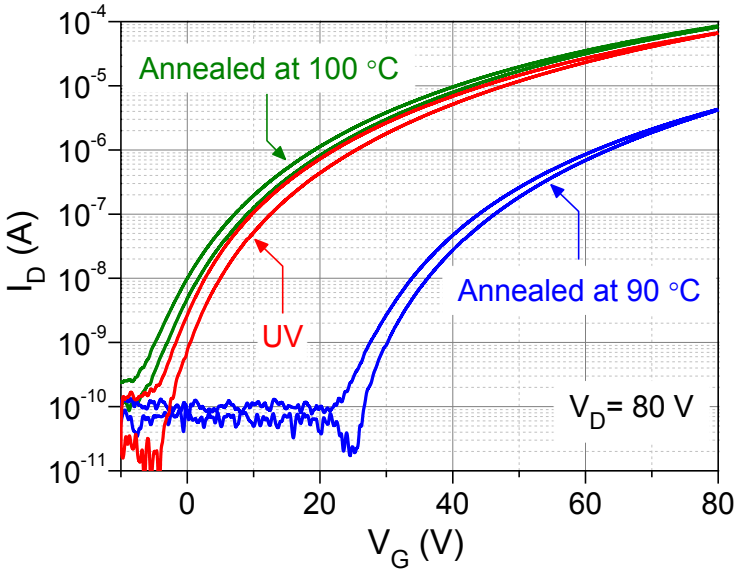


Figure 5.11: Transfer characteristics measured from ZnO transistors in which the as-spun precursor films were annealed at 90 °C, 100 °C in nitrogen and irradiated with UV light in ambient environment. Electrical characterisation was performed in high vacuum at drain voltage V_D = 80 V.

For this low-temperature UV-conversion process, one plausible mechanism involves photo-excitation of Zn-ammine complex by the UV light which leads to a ligand-to-metal charge transfer followed by decomposition into Zn and hydroxyl groups [86, 141]. The excited atomic oxygen created by the absorption of the UV light in air and the presence of water in the as-deposited film lead to the formation of hydroxyl radicals [143, 144]. Under these conditions, UV light is expected to continuously decompose the hydroxyl groups to hydroxyl radicals. These short-lived hydroxyl radicals then decomposed to hydroxyl peroxide, water and oxygen. The excess oxygen can then be reabsorbed by the metal ion to form a metal-oxygen network [86]. Therefore, due to the strong oxidizing property of this particular UV irradiation, the energy required for the ZnO conversion could be much lower than thermal calcination, and the process of the formation of ZnO then becomes much more effective [145].

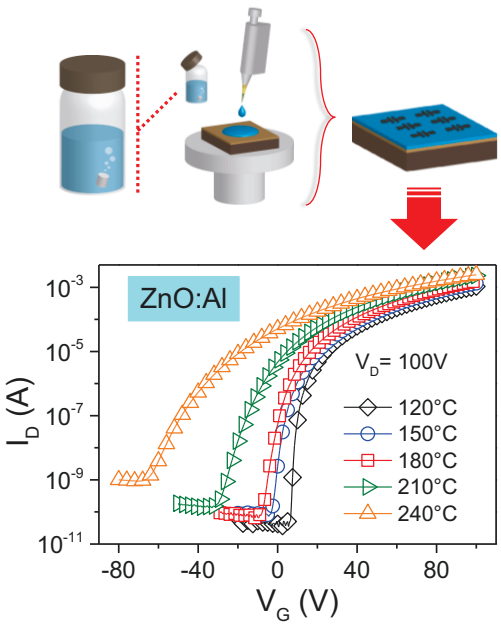
5.7 Conclusions

In summary, high-performance ZnO transistors based on Zn-ammine complex were fabricated using a simple and low-cost solution-based process. The approach enables deposition of continuous, ultra-thin (~4 nm) and highly transparent (>97% in the wavelength range of 400–1400 nm) ZnO layers on large-area substrates at temperatures ≤180 °C. With a careful control of deposition environment, the size of the polycrystalline domains in ZnO films can be modified. The best device performance was obtained by thermal-annealing in an inert-gas environment (i.e. nitrogen in the present study). This improvement is attributed to the presence of fewer grain boundaries. On the other hand, the studies on transfer characteristics for these transistors revealed the charge transport follows the mechanism of percolation conduction and is no longer limited by deep trapping sites. Meanwhile, using different Zn-ammine-complex solution concentrations, a close relation was observed between device performance and film morphology, and as a result the highest device performance was obtained from an optimised concentration of 0.07 M.

In an effort to further reduce the processing temperature, an alternative post-deposition UV light illumination process has been demonstrated for the growth of ZnO films at temperatures ≤90 °C, and the resulting devices exhibited electron mobilities of ≈ 1 cm^2/Vs. A similar UV light irradiation process has also been adapted for fabricating solution-processable high-κ dielectric materials. The combination of these materials and processing methodologies has enabled the fabrication of high electron mobility (>10 cm^2/Vs), low-voltage ZnO transistors on a variety of substrates, including plastic foils. In addition to the excellent device performance, the ultra-thin nature of these ZnO layers could provide a unique device platform for other applications, such as chemical sensors, due to the back-channel surface being in such close proximity to the modulated field-effect region. The processing route described here could, in principle, be applied to other precursor materials and lead to the development and improvement of both n-type and p-type metal-oxide semiconductors and devices, suitable for a whole host of existing applications.

6

ALUMINIUM-DOPED ZNO THIN-FILM TRANSISTORS



Enhanced performance of n-type Al-doped ZnO thin-film transistors is demonstrated. The process relies on the use of an aqueous route for efficient Al-doping of Zn-ammine complex in solution. The doping method requires only a simple timing-related stage without changing any of the process steps developed and described in the previous chapter. In addition, this approach does not require any fine control of the environmental conditions during thermal-annealing. Film characterisation reveals a time-dependent evolution in the Al-doped ZnO (ZnO:Al) structures. As a result, a full picture is obtained showing the fabrication of high-quality polycrystalline ZnO:Al thin films from solution and their use in high-performance transistors at low temperatures. Electron field-effect mobility of >5 cm²/Vs is demonstrated at a plastic-friendly temperature of 180 °C. Moreover, the process temperature can be reduced as low as 120 °C, and the ZnO:Al transistors still exhibit a maximum field-effect mobility value of ~3 cm²/Vs. (Left panel: Current-voltage characteristics for ZnO:Al TFTs.)

6.1 Introduction

The rising demand for large-area electronics has led to the development of many novel solution-based processing methods for oxide semiconductor transistors in the last decade [41, 42]. Various ternary/quaternary oxide materials, such as IZO, ZTO, IZTO and IGZO [146-149], have shown high solution processability, and the resulting device performance is fast approaching that of the highest reported vacuum-processed oxide TFTs to date [43, 44]. However, to obtain such electrical performance the conversion temperature typically needs to be over 400 °C for solution-based oxide semiconductors, which is not feasible for potential application in flexible electronics [43, 44, 76-78, 139, 150]. In an effort to reduce the required conversion energy, different approaches have been proposed in the past few years few of which includes the use of UV light-assisted conversion and oxide deposition under strict environmental control [86, 106, 110].

On the other hand, several different types of aqueous routes to synthesise oxide precursors have been proposed and have demonstrated their effectiveness on delivering functional TFTs at much lower temperatures (<250 °C) [111-113, 151, 152]. As seen in Chapter 5, Zn-ammine complex is one of the most promising precursor materials since its conversion temperature can be as low as ~100 °C [112]. Using this approach, a typical ZnO TFT shows a moderate mobility of >1 cm^2/Vs at processing temperatures of 150–200 °C [111-113]. On the other hand, with the addition of careful control of the environmental conditions, to reduce the presence of O_2 and H_2O during film depositions, the electron mobility can reach as high as ~10 cm^2/Vs at 180 °C [112]. In spite of this promising performance, these requirements on environmental controls could be obstacles for high-throughput manufacturing. Processability in an ambient environment is considered to be a more time-efficient and cost-effective approach towards the fabrication of large-area electronics. As such, an alternative strategy is needed to maintain high electrical performance, without complicating process protocols for ZnO TFTs using the Zn-ammine complex approach.

The use of extrinsic dopants generally leads to an increase in carrier concentrations in a TOS material [153]. Once this increase above a threshold value, it

could eventually lead to an enhancement in electron mobilities [53]. In this chapter, a simple and facile Al-doping method for Zn-ammine complex is introduced for the formation of Al-doped ZnO (ZnO:Al). The evolution of ZnO structures is investigated using various characterisation techniques, including UV-Vis, AFM, XRD and XPS whilst an in-depth study of the influence of different Al-doping levels on electrical performance is acquired from ZnO:Al TFT characterisations. Importantly, the processability of the Al-doped Zn-ammine complex precursor solution remains the same as the intrinsic Zn-ammine complex solution without any compromise on the processing versatility. Moreover, there is no requirement for any stringent environmental control during film growth. For optimised devices, the electron mobility can reach >5 cm^2/Vs at 180 °C. Even at 120 °C the ZnO:Al-based TFTs show remarkably high electron mobility with maximum values ~3 cm^2/Vs. The obtained results highlight the potential of the proposed process for high performance TFTs that can be manufactured onto inexpensive and temperature sensitive substrates, such as plastic foils.

6.2 Review of known doping method for Zn-ammine complex

Most of the doping methods utilising Zn-ammine complexes reported to date are based on using extrinsic dopants in the form of metal compounds, such as indium nitrate, lithium hydroxide, sodium hydroxide, etc., to achieve higher carrier concentrations, and hence better device performance [154-159]. Among these studies, the work carried out by Park et al. [155] looked into four different alkali metals (including Li, Na, K and Rb) for doping ZnO and provided a comprehensive overview of electrical properties of alkali-metal doped ZnO TFTs. In the latter study, the authors optimised the doping by fabricating a series of Li-doped ZnO (ZnO:Li) transistors with dopant concentrations in the range of 1–15 mol% Li. It was found that electron mobilities for the ZnO:Li devices improved from 1.6 to 7.3 cm^2/Vs as the Li doping concentration was increased from 1 to 10 mol%. Beyond 10 mol%, it was found that introducing more Li dopants did not enhance the electrical properties any further, instead a significant drop in the electron mobility (2.7 cm^2/Vs) was observed

from ZnO:Li devices approaching 15 mol% Li doping ratio. This was attributed to an excessive number of impurities that were likely to introduce more charge traps. Using the same procedure, Park and his colleagues optimised the doping levels for ZnO using other alkali-metal dopants, and the resulting electron mobilities obtained were 5.9, 3.7 and 4.3 for Na, K and Rb-doped ZnO devices, respectively. All dopants appeared to have enhanced the electron mobilities. The result was attributed to the introduction of alkali-metal dopants in the ZnO that preferably occupy the interstitial sites as electron donors over the substitutional sites (acceptor). The authors also fabricated low-voltage ZnO:Li devices utilising ion gels as the gates, and these devices combined with suitable passive electronic components (i.e. resistors) were used to fabricate an operational inverter-like circuit. This simplified approach in the latter case demonstrated the possibility for practical applications of the doping technology in oxide integrated circuit.

However, the fabrication process proposed by Park et al. [155] still requires thermal annealing at 300 °C, and none of the studies listed in ref. [154-158] demonstrated processing temperatures being plastic-friendly (<200 °C). It is likely that the dopant formulations requires higher conversion temperatures, since studies have suggested ZnO formation using Zn-ammine complex alone can be achieved even at very low temperature of ~100 °C [111, 112]. Nevertheless, the study by Weber et al. [159] reported that gallium-doped ZnO (ZnO:Ga) and gallium, indium-doped ZnO (ZnO:Ga,In) were prepared by dissolving their hydroxide species in ammonia aqueous solution, and the depositions were carried out at a temperature of 160 °C. From the measurements of inductively coupled plasma atomic emission spectroscopy (ICP-AES), the gallium signals were found to exist in both the precursor solutions and the resulting oxide films whilst there was no detectable indium signals in the films, or in the precursor solutions. The gallium dissolution is likely attributed to the amphoteric nature of gallium hydroxide. On the other hand, a much higher pH environment is required to form indium. This may be the cause for the inability to detect indium in the ICP-AES measurements [159]. Despite this, the XRD results showed the strongest signal for a peak (002) obtained from the ZnO:Ga,In samples whilst there was a weak peak (002) signal for the ZnO:Ga and an undetectable diffraction signal for the ZnO alone. The obtained ZnO:Ga,In TFTs exhibited the highest performance with an

electron mobility of 0.62 cm^2/Vs, which suggests a strong dependence of electron mobility on the signal intensity of the (002) diffraction peak. Similar findings have been reported by others workers in the literature [111, 160].

Among the metal-ammine complex species, Zn-ammine complex is the only one that has been reported to form semiconducting oxides at low temperatures. However, the unique property of ammonium hydroxide makes doping of Zn-ammine complexes with extrinsic dopants, such as Al, a rather non-trivial task. One of the main reasons is that ammonium hydroxide precipitates metal salts by forming insoluble metal hydroxide species. As reported in the work by Weber et al. [159], choosing either an amphoteric material or a suitable pH condition could be a key to resolving this issue. In a similar manner, Hagendorfer et al. [161] doped Zn-ammine complex with pure Al foils (rather than Al compounds or Al salts) in an ammonia solution of pH > 11. This is because aluminate anion tends to form in a highly basic condition due to the amphoteric property of Al.

With the addition of ammonium citrate into the precursor solution, the authors fabricated densely-packed transparent Al-doped ZnO (ZnO:Al) films of sheet resistance 200 kΩ/sq at a temperature of 80 °C, and this value was further reduced to 25 Ω/sq by employing a post-deposition UV treatment. In particular, this UV treatment not only reduced the hydroxide species, due to a shift in binding energies towards lower energies that are highly related to metal-oxygen bonding, but also induced more free carriers as a greater absorption is observed in the infrared spectrum. To demonstrate their applications, the ZnO:Al films were utilised as the front electrodes for $Cu(In,Ga)Se_2$ solar cells that exhibited high current density of 33.4 ± 0.5 mA cm^{-2} and low series resistance of 1.1 ± 0.1 Ω cm^2.

6.3 A novel time-dependent Al-doping process

Inspired by the work of Hagendorfer et al. [161], the Al doping method introduced in the present study is based on the unique property of ammonium hydroxide, which is highly oxidising to many metals. Figure 6.1 schematically illustrates the experimental processes of the solution synthesis and device fabrication. For preparing Al-doped Zn-

ammine complex solution, a high-purity Al pellet of a specific size (cylinder of 3 mm diameter × 3 mm height, 99.999% Kurt J. Lesker) was added into a complex solution of 8 mL for a certain period. Since Al and aluminium sub/oxides are amphoteric, the highly-basic ammonium hydroxide used in this work (pH > 13) can turn both of them into aluminate anions. The reactions continue for a set time until Al metals are removed from the solutions. Therefore the doping level is controlled in time domain. On completion of the Al-doping steps, the resulting precursors were filtered through 0.45 μm PTFE membrane filters to remove any impurities or residues. The subsequent film depositions and thermal calcination were carried out in ambient air with the same parameters and procedure described in Chapter 5. The fabrication of ZnO:Al TFTs was completed by evaporating Al 40-nm source-drain (S-D) electrodes through shadow masks under high vacuum. To prevent potential degradation of device performance from O_2 and H_2O during ambient storage, the completed ZnO:Al transistors were encapsulated with a layer of CYTOP (an organic fluoropolymer) deposited via spin casting in nitrogen environment, followed by a brief thermal-annealing step at a temperature of 100 °C for 10 min.

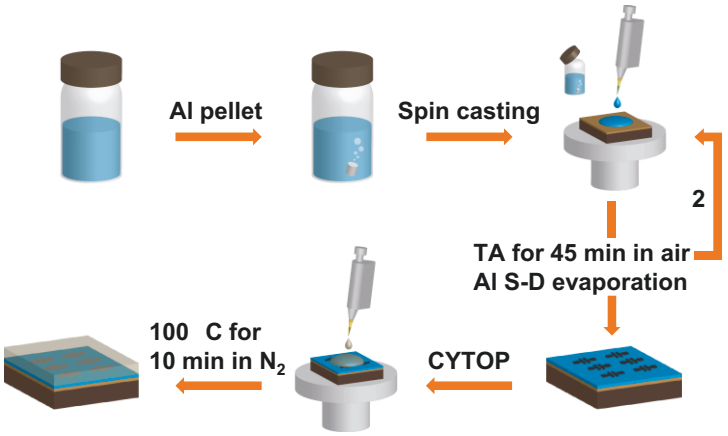


Figure 6.1: Schematic of experimental process: an Al metal pellet is added in as-prepared Zn-ammine complex solution for a predetermined period of time. Upon completion of the doping process, film deposition is performed spin casting, followed by thermal annealing (TA) in air. Transistor structures are completed by thermal evaporation of Al as top source-drain (S-D) electrodes, and an encapsulation layer of CYTOP is then deposited to protect devices from oxygen and water.

Figure 6.2 shows a series of photographs of the precursor solutions taken at different Al pellet immersion time. Upon oxidation the Al pellet surface color changes. Specifically, the Al pellet starts becoming darker after immersion time of

~30 min, and it had turned almost completely black after 24 h (see the rightmost panel in Figure 6.2). In the present study, the doping time was limited to ~30 min in order to retain a solution with minimal presence of oxidation by-products, such as aluminium suboxide and hydroxoaluminates, since their existence in the solution could lead to severe degradation of the properties of oxides and potentially lower the electrical performance of the resulting transistors.

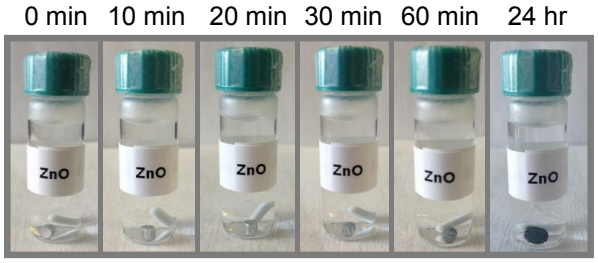


Figure 6.2: Photos of a series of Al-doped Zn-ammine complex solution taken at different Al pellet immersion time.

6.4 ZnO:Al thin-film characterisation

6.4.1 Optical characterisation and energy bandgap analysis

The doping effect was first investigated by optical transmission measurements on intrinsic ZnO (i-ZnO) and Al-doped ZnO (ZnO:Al). Using spin casting, i-ZnO and ZnO:Al films with various doping time of 4 min, 8 min and 16 min (i.e. ZnO:Al-4m, ZnO:Al-8m and ZnO:Al-16m, respectively) were deposited onto quartz substrates at different annealing temperatures in the range of 120–240 °C. The obtained total optical transmittance spectra for these films (measured with blank quartz substrates) are displayed in Figure 6.3. The results directly reflect the ultra-thin nature of the ZnO films from the use of the aqueous approach that has been seen in Chapter 5 [112]. From Figure 6.3, the absorption characteristics take part in the UVA region between 350–400 nm, which is expected from the interband absorption in ZnO.

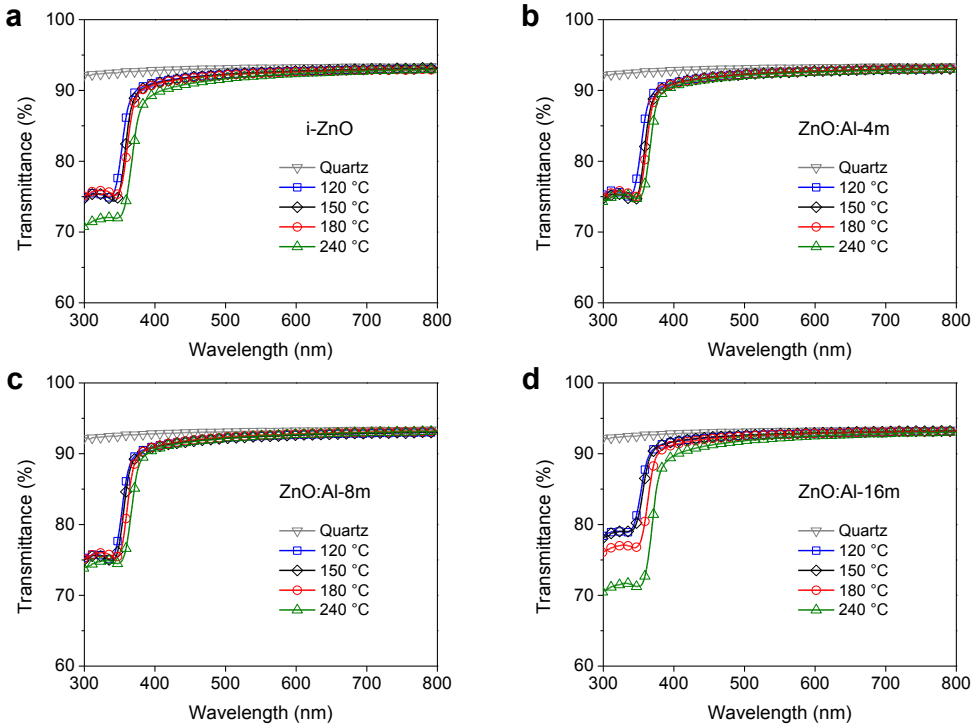


Figure 6.3: UV-Vis transmission spectra measured for oxide films (on quartz substrates) based on (a) i-ZnO, (b) ZnO:Al-4m (c) ZnO:Al-8 min and (d) ZnO-16 min. For each doping condition and the intrinsic sample, the film depositions were carried out at different annealing temperatures of 120 °C, 150 °C, 180 °C and 240 °C in ambient air.

The energy bandgap values were extracted via Tauc analysis [162], and the obtained values are plotted in Figure 6.4 and summarised in Table 6.1. In particular, one should notice that even for the i-ZnO samples there exists a significant change in the bandgap values [see Figure 6.4(a) and Table 6.1] when the deposition temperature increases from 120 °C to 240 °C. This could be attributed to the fact that the thickness of solution-processed ZnO is likely temperature-dependent. As described in the early work reported by Meyers et al. [111], it was found that at low deposition temperatures it was harder to form a thicker layer even via multiple depositions. In the present study, the deposition process was carried out twice to complete ZnO film depositions. In fact, applying a second deposition could dissolve part of the existing layer, i.e. in the proximity of the top surface of the first layer. This is because of the potential chemical reaction of ligand exchange between $ZnO/Zn(OH)_2$ and ammonium hydroxide. On the other hand, increasing deposition temperatures could lead to the formation of a more robust ZnO layer owing to stronger formation of oxide and

reduction/decomposition of other unwanted residues such as hydroxyl and ammine groups [123]. The resulting ZnO films are able to resist ammonium hydroxide for a short period of time during the deposition process. Therefore, at higher deposition temperatures the film thickness sees a larger increase with each deposition than those processed at lower temperatures.

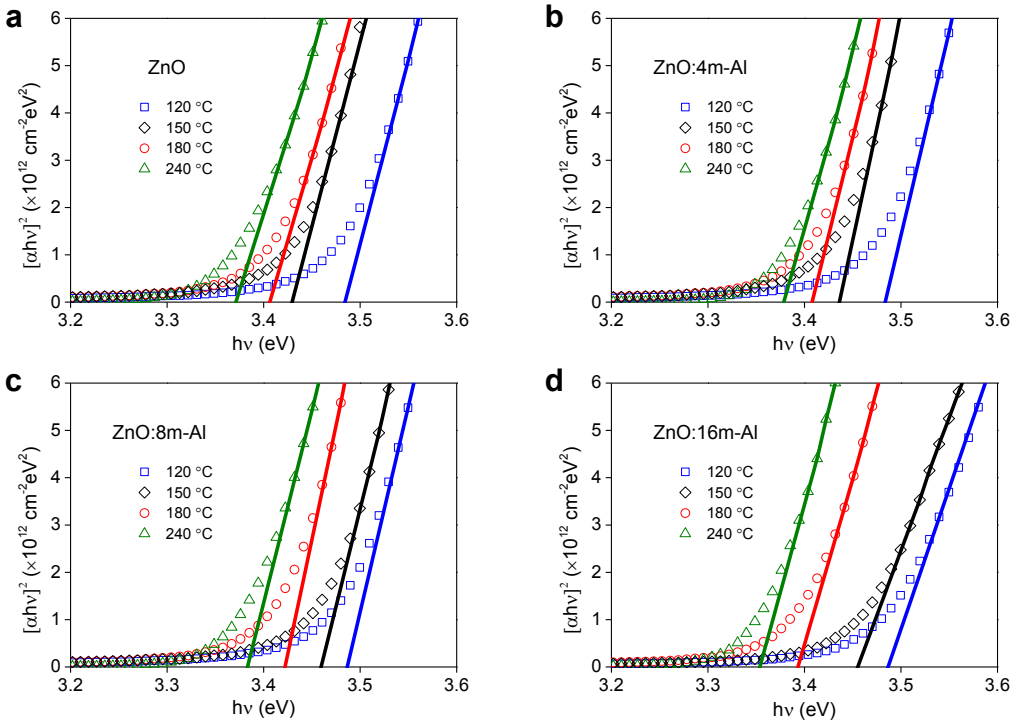


Figure 6.4: Tauc plots calculated from the optical spectra of the ZnO films shown in Figure 6.3 to determine the optical bandgaps of the ZnO layers.

Table 6.1: Summary of energy bandgaps of i-ZnO and doped ZnO calculated via Tauc analysis of the data shown in Figures 6.3 and 6.4.

	Bandgap (eV)			
Temperature (°C)	i-ZnO	ZnO:Al-4m	ZnO:Al-8m	ZnO:Al-16m
120	3.484	3.485	3.487	3.486
150	3.429	3.436	3.460	3.455
180	3.406	3.410	3.423	3.394
240	3.371	3.379	3.385	3.354

Importantly, if the film thickness forms in the range of few nanometres, the onset of absorption in the ZnO optical spectrum should show a blue shift, and the corresponding bandgap could be extracted as a slightly larger value due to the

quantisation effect [126, 163]. From Table 6.1, for the i-ZnO samples the widest bandgap was measured from the film processed at 120 °C with the largest increase of 113 meV in bandgap as compared to that annealed at 240 °C. On the other hand, in Chapter 5 the ZnO film of ~5 nm was obtained at a processing temperature of 180 °C using the same approach [112] so that lower deposition temperatures used in the present study could result in film thicknesses <5 nm. Moreover, recent studies on various oxide semiconductors materials have shown that similar quantisation phenomena are indeed profound in low-dimensional systems, i.e. films being a few nanometres thick [126, 163]. Therefore, one can conclude that this observation, i.e. the lower the conversion temperature the larger the bandgap, is at least partly linked to band energy quantisation effects taking place in the thin oxide film.

Apart from quantisation effects caused by the ultra-thin nature of the oxide layer, an increase in bandgaps could be due to the increase in carrier concentration, which is known as the Burstein-Moss band-filling effect [49, 50]. In the case of Al-doped ZnO, several workers have reported relevant observations [161, 164-167]. From Table 6.1, it is found that the ZnO:Al-4m and ZnO:Al-8m samples have larger bandgaps than those obtained from the i-ZnO samples when comparing films processed at each individual temperature (in the range 150-240 °C). However, at a thermal annealing temperature of 120 °C there is no significant change in bandgap for the samples with different doping time. The possible reasons could be due to the thermal energy not being high enough for complete formation of ZnO:Al [168, 169] and/or changes in ZnO:Al structures were under the detection limits imposed by the optical characterisation instrument. On the other hand, for the ZnO:Al-16m samples a notable increase in bandgap is observed at 150 °C whilst for deposition temperatures ≥180 °C the extracted bandgaps are even smaller than all other samples. More interestingly, at each processing temperature the extracted bandgap values do not monotonically increase with longer doping time; instead, there exists a maximum value at doping time of 8 min. Such a result suggests that other mechanisms may have some influence on the bandgap widening and narrowing phenomena.

Another well-known bandgap narrowing effect is the Mott transition [170, 171], which is a characteristic insulator/semiconductor to metal transition related to the interplay between the Coulomb repulsion and the localization degree of electrons,

especially in the case of degenerately doped semiconductors. However, in the present case, the largest change in bandgap obtained is only 0.031 eV that is classified within the domain of low electron concentration ($\leq 4.2 \quad 10^{19}$ cm^{-3}) [165, 167]. To induce the Mott transition, this number of charge carriers is still beyond the required criteria and the material itself is classified as a non-degenerate semiconductor. It should be noted that, although principles similar to the previous work reported by Hagendorfer et al. [161] were employed here, a higher doping concentration obtained in ref. [161] was a result of the use of the extra incorporation of seeding layers and UV-assisting illumination in order to fabricate transparent electrodes. On the other hand, for the targeted applications in the present study, i.e. high-performance functional TFTs, such a "moderate" number of carrier concentrations ($<10^{19}$ cm^{-3}) are needed and crucial to achieve high current modulation in transistor operation [54, 55]. Experimental results on transistors that will be presented later to demonstrate the importance of this point.

Taking a closer look at the time-dependent doping process in the present study, when the Al pellet is immersed in the ammonia aqueous solution, aluminium hydroxide [$Al(OH)_3$] is formed in the first instance. Due to its amphoteric property, aluminium hydroxide turns into hydroxoaluminates [$Al(OH)_4^-$] in the high-pH Zn-ammine complex solution (50% v/v in water, pH > 13). Owing to the dynamic nature of this process, there is an increasing concentration of oxidation by-products with time. If fewer hydroxyl groups are present in the solution, the trend of forming aluminium hydroxide becomes stronger. As a result, this could cause degradation of the precursor (see Figure 6.2). Therefore, the dopant level needs to be carefully controlled as longer immersion time is likely to cause unwanted precipitation of hydroxoaluminates in the precursor solution. This could be the main reason responsible for the formation of a thicker film and hence the observation of smaller bandgaps in the ZnO:Al-16m samples.

6.4.2 Grazing incident X-ray diffraction measurements

Grazing-incident X-ray diffraction (GID) measurements were carried out to further study as-grown ZnO layers. The wavelength employed for this investigation is λ= 0.123511 nm (see Chapter 3 for the experimental details), and the obtained GID

images and full scans are shown in Figure 6.5(a) and (b), respectively. The ZnO films were deposited on the Si/SiO_2 substrates at a temperature of 150 °C. It can be seen that there is no significant difference between the samples prepared with Al doping time ≤8 min, and all of them exhibit three distinct peaks at 2θ values of (100), (002) and (101). However, when the doping time increases to 16 min, the crystallographic structure becomes very different: a very strong signal from peak (100) is present in this ZnO:Al sample. Meanwhile, the intensity of peak (101) becomes stronger, but the signal associated with the (002) peak seems to disappear or is barely resolvable in the GID measurements. Contrary to this, the ZnO:Al samples with ≤8 min doping time remain at a similar crystallinity to i-ZnO.

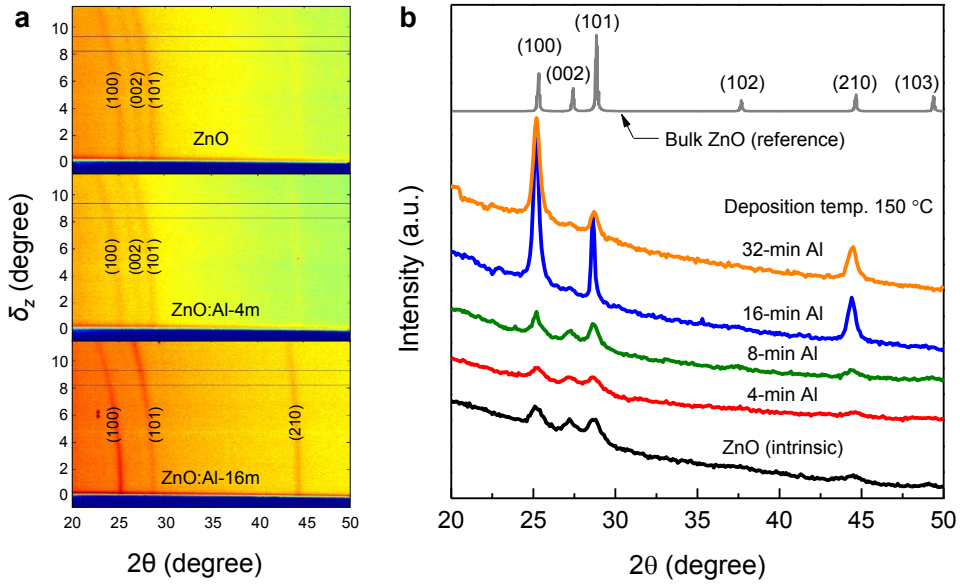


Figure 6.5: (a) and (b) show grazing incident X-ray diffraction images and data of ZnO, respectively. The ZnO thin-film samples were prepared with different doping time and all processed at 150 °C in ambient air. The reference obtained using bulk ZnO sample is shown for the comparison of peak positions.

The same trends in crystalline orientations are also observed in samples prepared at the higher temperature of 180 °C (see Figure 6.6). Since different intensities of the peaks in the GID scans refer to different degrees of crystallographic orientations, the change in the crystallinity related to peak (100) may suggest that Al dopant plays a role as a mineralizer or surfactant [172]. Such an effect has been observed in ZnO:Al using sputtering techniques as well as during the growth of

germanium on silicon using molecular beam epitaxy with the addition of antimony as a surfactant [172, 173]. Moreover, this behaviour was also observed in a previous work via a sol-gel route for ZnO:Al [169]. Similarly, during the growth of the solution-processed ZnO:Al films here, a tendency to follow preferable crystalline orientations, i.e. peaks (100) and (101) may exists.

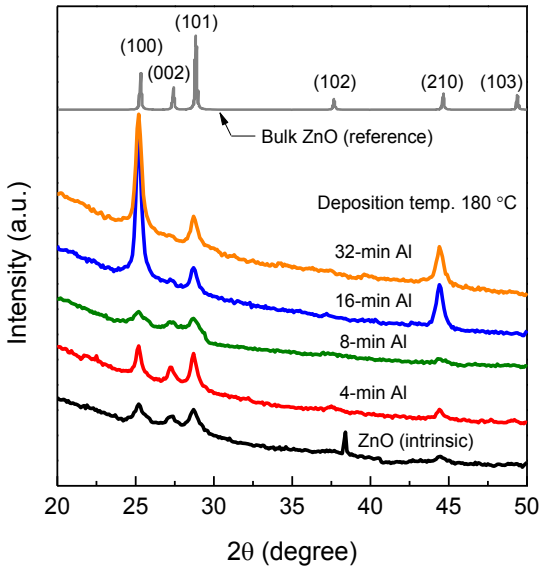


Figure 6.6: Grazing incident X-ray diffraction data of ZnO thin-film samples prepared with different doping time and processed at a temperature of 180 °C. The reference obtained using bulk ZnO sample is shown for the comparison of peak positions.

To gain further insight into the (100) peak, its position as a function of Al doping time (in mins) at 150 °C and 180 °C was plotted in Figure 6.7. As can be seen, no profound trend is visible. This perhaps due to the fact that the degree of change in the lattice constant to lattice distortion was rather small or negligible. Besides, in order to understand how the thermal process impacts the ZnO crystallinity, the GID measurement was carried out on the ZnO:Al-8m samples processed at temperatures in the range between 120 °C and 240 °C. The results for the positions of the (100), (002) and (101) peaks are shown in Figure 6.8(a). It can be seen that there is no significant increase in the signal intensities, i.e. the degree of crystallinity remains the same for the different processing temperatures. However, from Figure 6.8(b) the evolution of the (100) peak position towards higher angles with increasing temperatures, is observed. This phenomenon could be attributed to the Zn sites in the ZnO structures

being substituted by the Al atoms. Therefore, lattice distortion could take place and in turn cause shrinkage of lattice constant owing to the difference in the Al and Zn ion sizes [168, 174].

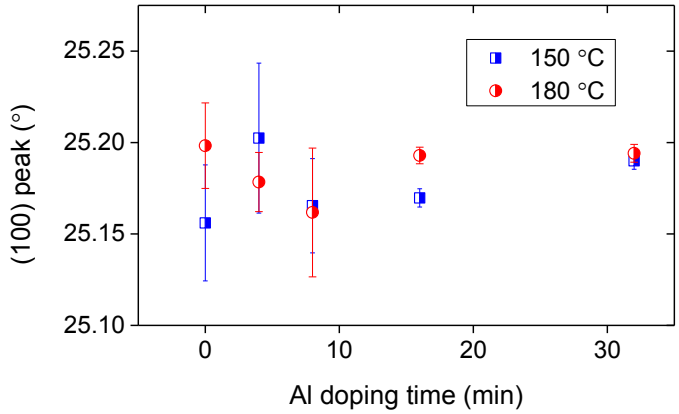


Figure 6.7: The positions of the peak (100) in the ZnO:Al samples as a function of various doping time (0-32 min) at two different deposition temperatures (150 °C and 180 °C).

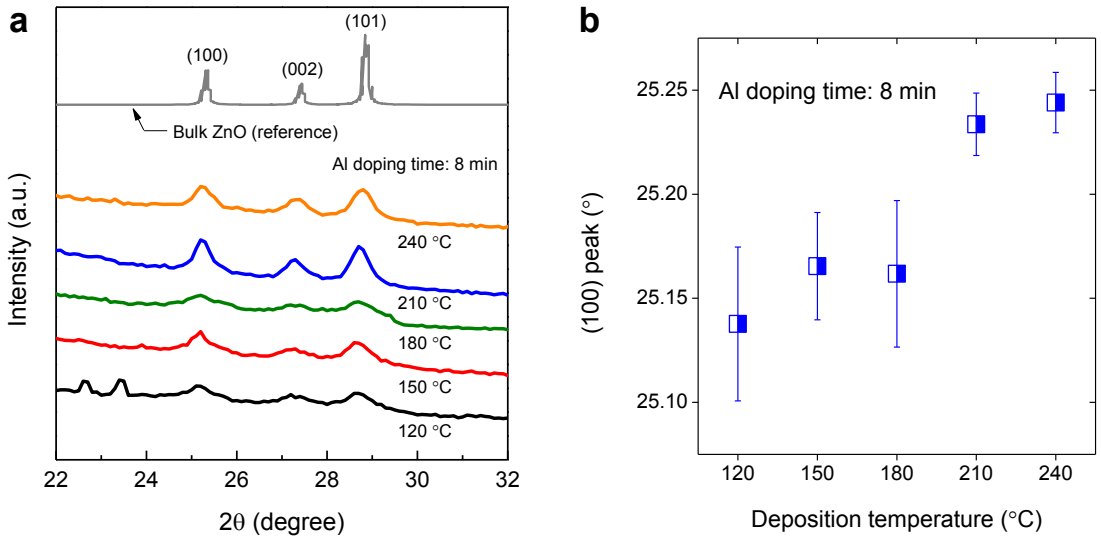


Figure 6.8: (a) Grazing incident X-ray diffraction data of ZnO:Al-8m around the (100), (002) and (101) peak positions. The samples were processed at temperatures in the range between 120 °C and 240 °C. The reference obtained using bulk ZnO sample is displayed for the comparison of peak positions. (b) The position of the peak (100) as a function of deposition temperatures.

6.5 Morphological engineering for ZnO:Al layers for transistors

6.5.1 Evolution of layer morphology and performance in ZnO:Al transistors via different doping levels

As seen in Chapter 5, high-quality film morphology is key to high-performance TFTs [95, 111, 112, 175]. For a polycrystalline material, low surface roughness and fewer grain boundaries are important for efficient charge percolation [78, 175-177]. It has been reported that the growth rate and morphology of ZnO:Al can be significantly affected by the Al dopant concentration in the precursors [161, 166, 178]. Therefore the study of the impact of film morphology on transistor characteristics could provide an effective way to improve and optimise film synthesis and overall device performance. As such, before looking into electrical characterisation results the ZnO:Al samples are first investigated using AFM to study the evolution of film morphology at different doping levels.

Figure 6.9(a) shows a series of AFM surface topography images for the ZnO:Al films with doping time in the range of 0–32 min. The ZnO samples were annealed at temperatures of 150 °C and 180 °C in ambient air. The corresponding height distribution for each sample is shown in Figure 6.9(b) and (c) for the deposition temperatures of 150 °C and 180 °C, respectively. It can be seen that ZnO:Al films with longer Al doping time, exhibit larger grains, higher surface roughness and broader height distribution at both processing temperatures. This observation could be attributed to the formation of higher crystallinity in the ZnO:Al structures with longer Al doping time [see Figure 6.5(b) and Figure 6.6]. Furthermore, if one considers the dynamic nature of the doping process combined with the un-intentional generation of various by-products, another possible reason is that the precursor degradation could lead to the formation of more hydroxide and/or hydroxoaluminate species and affect the overall film morphology. Moreover, during the doping process only a certain number of Al dopants can be incorporated into ZnO; in other words, excessive Al species might result in intragrain congregation and/or grain-boundary segregation and hence the formation of aluminium suboxide (AlO_X) and/or Al-Al clusters [165, 166, 179].

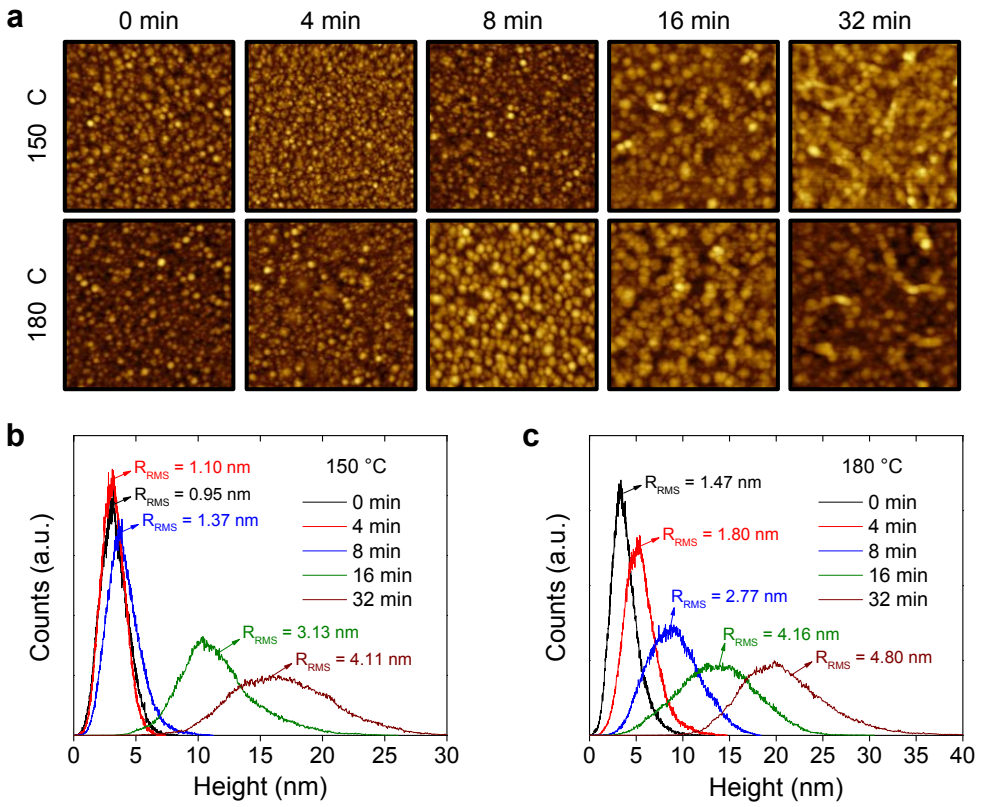


Figure 6.9: (a) AFM topography images (scan size: 1 µm 1 µm) of ZnO:Al films with different doping time of 0, 4, 8, 16 and 32 min. Film deposition was carried out using spin casting on Si/SiO_2 substrates followed by thermal annealing at temperatures of 150 °C (first row) and 180 °C (second row) in ambient air. The corresponding statistical distributions of surface height and associated root mean square surface roughness (R_{RMS}) calculated from the AFM images of the ZnO samples processed at 150 °C and 180 °C are shown in (b) and (c), respectively.

A series of i-ZnO and Zno:Al TFTs were fabricated on Si/SiO_2 substrates at a temperature of 150 °C (see Section 6.3 for experimental details). The transfer characteristics are shown in Figure 6.10, and the key device parameters are summarised in Table 6.2. It can be seen that increasing Al doping time up to 8 min leads to a notable improvement in device performance [see Figure 6.10(a) and Table 6.2], including higher linear and saturation mobilities (i.e. μ_{LIN} and μ_{SAT}), ascending drain current (I_D) levels and smaller turn-on voltage (V_{ON}) values whilst for longer Al doping time (≥8 min) the devices start showing lower performance [see Figure 6.10(b) and Table 6.2]. The former is believed to be due to an increase in the concentration of Al dopants with longer time. On the other hand, a turnaround in the latter case is not a surprise if one takes into account the earlier observations and relevant discussions.

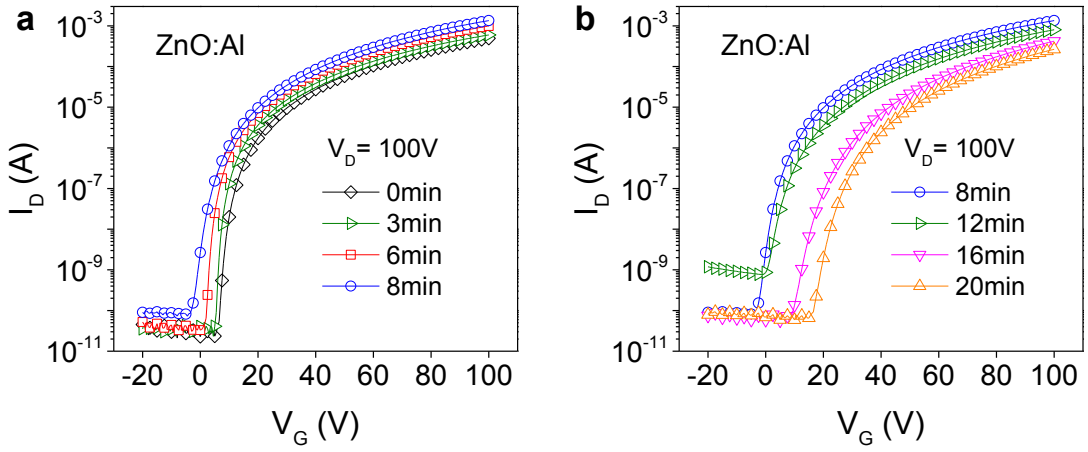


Figure 6.10: (a) and (b) display the transfer characteristics of the ZnO:Al transistors (channel width/length = 1000 µm/50 µm) with doping time in the range of 0–8 min and 8–20 min, respectively. The devices were processed at a temperature of 150 °C in ambient air.

From the UV-Vis and GID measurements [see Table 6.1 and Figure 6.5(b)] there exist effects from Al dopants (i.e. blue shift in bandgap and stronger signal in crystallinity) for the ZnO:Al-16m samples processed at 150 °C. In addition, the AFM results show that the ZnO:Al-16m film surface is much rougher than the ZnO:Al-8m layer [see Figure 6.9(a) and (b)]. In fact, better crystallinity in specific orientations is not necessary to benefit charge transport in ultra-thin films. This is because high crystallinity could cause high surface roughness and then reduce smoothness and homogeneity of thin films, which is often very crucial for charge transport. One representative example is that of ZnO:Al-16m layer, for which the surface roughness reaches >50 % of the total film thickness [Figure 6.9(b): R_{RMS} = 3.13 nm; thickness ≈ 5 nm] [112]. In this case, long-range charge transport in lateral directions is likely to be diminished by the characteristic non-uniformity [175] and most likely presence of grain boundaries. A similar case can be found in the work reported by Theissmann et al. [113]. On the other hand, from Table 6.2 the trap concentrations (D_{tr}) analysed using Equation 4.3 suggests more defects might be formed in the ZnO:Al structures with longer doping time. Moreover, the existence of excessive Al derivatives could induce a significant change in the precursor composition and then introduce unwanted residues and impurities in the resulting films. Contrary to this, the ZnO:Al-8m samples not only exhibit Al doping effects, but also remains ultra-smooth with large apparent grains. As a result transistors based on the latter layers exhibit the best

performance with a saturation mobility value of ~4 cm^2/Vs and a drain current on/off ratio of ~10^7. On the basis of this discussion and in view of the relevant transistor results, it is concluded that the optimised doping levels is obtained from Al doping time of 8 min.

Table 6.2: Summary of device parameters: saturation mobility (μ_{SAT}), linear mobility (μ_{LIN}), turn-on voltage (V_{ON}), subthreshold swing (S.S.) and trap concentration (D_{tr}) for ZnO:Al TFTs with different Al doping time. All TFTs were processed at a temperature of 150 °C in ambient environment.

	μ_{SAT} (cm^2/Vs)	μ_{LIN} (cm^2/Vs)	V_{ON} (V)	S.S. (V/dec)	D_{tr} ($eV^{-1}cm^{-2}$)
0 min	1.34	0.73	5.5	1.41	1.22×10^{12}
3 min	1.62	0.88	3.9	1.68	1.46×10^{12}
6 min	2.71	1.47	1.1	2.03	1.78×10^{12}
8 min	4.01	2.58	-3.6	2.26	1.99×10^{12}
12 min	2.54	1.28	-0.3	3.71	3.29×10^{12}
16 min	2.03	1.14	8.4	3.98	3.54×10^{12}
20 min	1.48	0.98	15.2	4.06	3.61×10^{12}

To gain insight into the impacts of Al dopants on elemental compositions in the resulting films, XPS measurements were carried out on i-ZnO and ZnO:Al-8m layers. The samples were solution deposited and annealed at 180 °C in ambient air. During the measurements, the Zn2p and O1s core levels were detected in both samples. On the other hand, no traces of Al in the ZnO:Al-8m samples could be detected. As a result the chemical states of the Al dopants cannot be resolved for Al-doped ZnO layers. This is attributed to the low concentration of Al dopants in ZnO structures and/or a low-ionisation number of Al dopants [180].

Since the O1s core level spectra are extremely sensitive to the chemical bonds between O and Zn (much more sensitive than Zn2p) core levels, the XPS O1s spectra shown in Figure 6.11 are used for studying the compositions of the ZnO and ZnO:Al samples. The O1s envelope can be deconvoluted into three individual peaks located below 530 eV (O^{2-} in ZnO wurtzite structures, oxygen ions surrounded by Zn or the substitution of Al), around 531 eV (O^{2-} in the oxygen deficiency regions within the ZnO matrix and/or composition imperfections at the ZnO surface regions) and over 532 eV (aqueous adsorbates on the surface of ZnO) [180, 181]. It is evident that the incorporation of Al dopants has a significant impact on the reduction of the medium binding-energy component of ~531 eV. This is mainly attributed to better formation

of ZnO, i.e. fewer trap sites, at the surface results in fewer oxygen ions in the oxygen deficiency regions. It should be noted that oxygen vacancies in solution-processing approaches for oxide semiconductors materials are generally related to thermal calcination temperatures [116, 123]. Therefore, the XPS results reflect the AFM observations in which the existence of more grains in the un-doped (intrinsic) ZnO films relates to the formation of more trap sites and hence more defect-related oxygen ions. On the other hand, substantial grain enlargement with Al dopants in the ZnO samples leads to elimination of grain boundaries and hence reduction in the number of defect-related oxygen ions as seen in the XPS results in Figure 6.11.

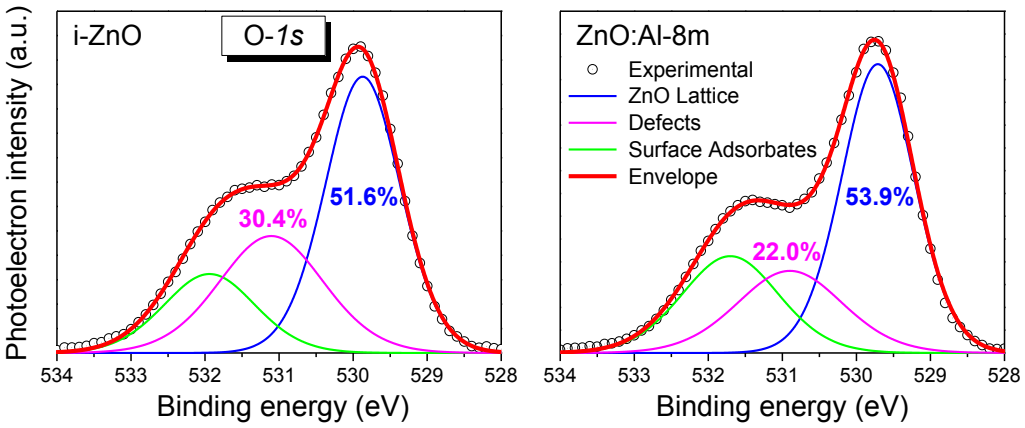


Figure 6.11: XPS spectra of the O1s core level line for the i-ZnO (left panel) and ZnO:Al-8m (right panel) samples. Both were prepared at 180 °C in ambient air.

6.5.2 Evolution of ZnO:Al layer morphology and transistor performance with annealing temperature

For solution-processed ZnO:Al, the electrical properties of the resulting layers are often determined by the annealing temperatures following solution processing [169, 182, 183]. It is also known that the performance of oxide-based TFTs is highly related to processing temperatures [109, 111-113]. In an effort to understand how Al dopants affect electrical performance under different annealing conditions, a series of ZnO:Al transistors were fabricated at temperatures in the range of 120–240 °C. The doping time was fixed to 8 min for all ZnO:Al samples. As seen earlier, the TFT performance is related to surface morphology. To study this effect the impact of film morphology on the resulting ZnO:Al-based transistor parameters were investigated. The measured

surface topography and phase images are shown in Figure 6.12(a), whilst Figure 6.12(b) displays the derived mean grain size plotted as a function of annealing temperature.

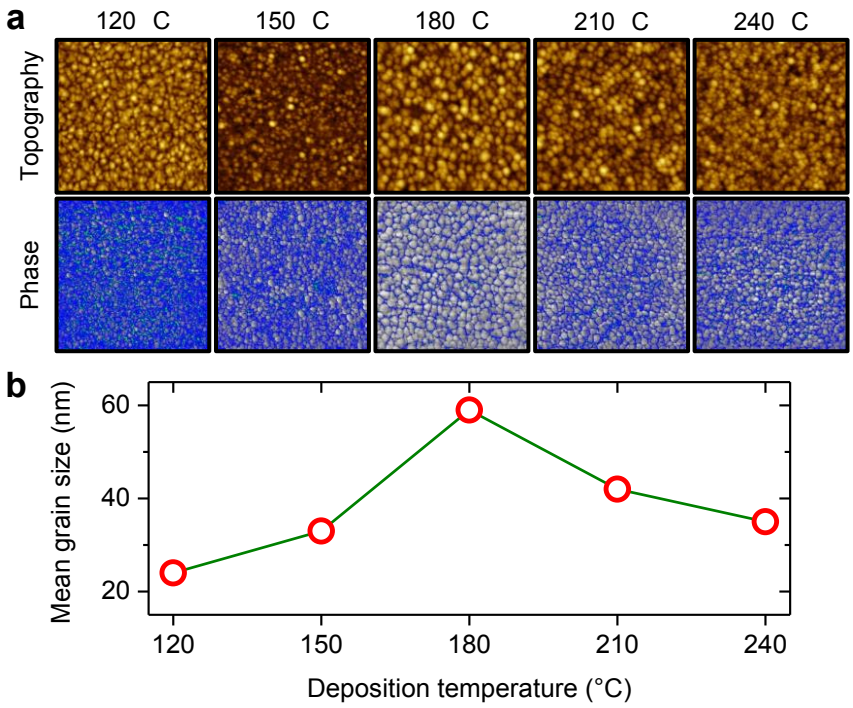


Figure 6.12: (a) AFM topography (first row) and phase (second row) images of ZnO:Al films with doping time of 8 min (scan size: 1 μm 1 μm). The films were formed by spin casting on Si/SiO_2 substrates followed by thermal annealing at temperatures of 120, 150, 180, 210 and 240 °C in ambient air. (b) Mean grain size derived from AFM topography images in (a) plotted as a function of annealing temperatures.

Interestingly, the maximum grain size is achieved at an annealing temperature of 180 °C, and the grain size decreases with increasing (decreasing) temperatures higher (lower) than 180 °C [Figure 6.12(b)]. On the contrary, it has been reported that solution-processed ZnO exhibits large grains with elevated annealing temperatures [77, 78]. However, if a temperature ramping is involved in the process, a fast ramping step for solution-processed ZnO:Al could cause the formation of finer microstructures, i.e. smaller grain size, and then a more porous film [166]. This is mainly due to the segregation of Al dopant at grain boundary [165]. Whilst in the present study there were no dedicated heat-ramping steps involved during the annealing process, faster thermodynamic equilibrium at higher annealing temperatures could have a similar effect and result in smaller grains.

The transfer and output characteristics of the ZnO:Al-8m TFTs prepared from different annealing temperatures are displayed in Figure 6.13 and 6.14, respectively, whilst the key device parameters are summarised in Table 6.3. The highest performance is achieved from the transistors processed at 180 °C, which exhibit a saturation mobility of 5.35 cm^2/Vs with a current on/off ratio of 10^7. Even at 120 °C the ZnO:Al TFT still shows a maximum mobility value of 3.11 cm^2/Vs. It can be seen that increasing the annealing temperature largely affects the current-voltage behaviours and leads to a normally-on, depletion mode type transistor, i.e. a negative V_{ON} value, which generally results from a large number of free electrons originated from shallow donor states in a metal oxide material. Therefore, the results presented here, i.e. the existence of an excessive number of free charge carriers, provide clear evidence of the influence of Al dopant on channel conductivity. It should be noted that transistor functionality is no longer feasible using the processing temperatures >210 °C because of the existence of extremely-negative V_{ON}. The reason for such negative values is attributed to the high concentration of Al dopants incorporated within ZnO at elevated temperatures [Figure 6.8(b)]. Apart from this, the integration of more dopants also leads to the formation of a higher number of defects in the host structures as a dramatic increase in trap concentrations is observed from the ZnO:Al-8m samples processed at higher temperatures [184]. Finally, no increase in transconductance is observed and as such no improvement on the overall devices' performance for higher processing temperatures.

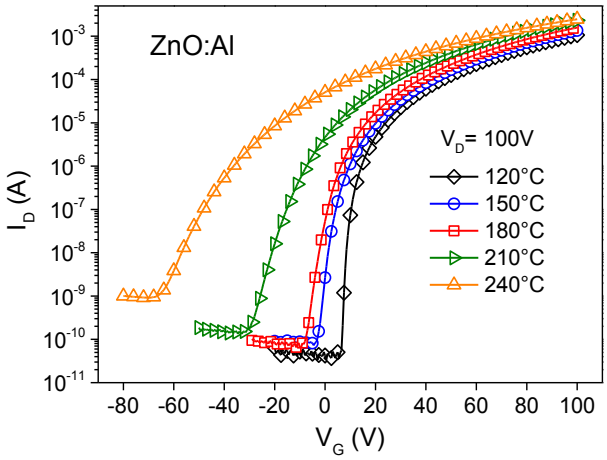


Figure 6.13: Transfer characteristics of ZnO:Al transistors (channel width/length = 1000 µm/50 µm) annealed at temperatures in the range of 120–240 °C in ambient air. For all the devices, the doping time was fixed to 8 min.

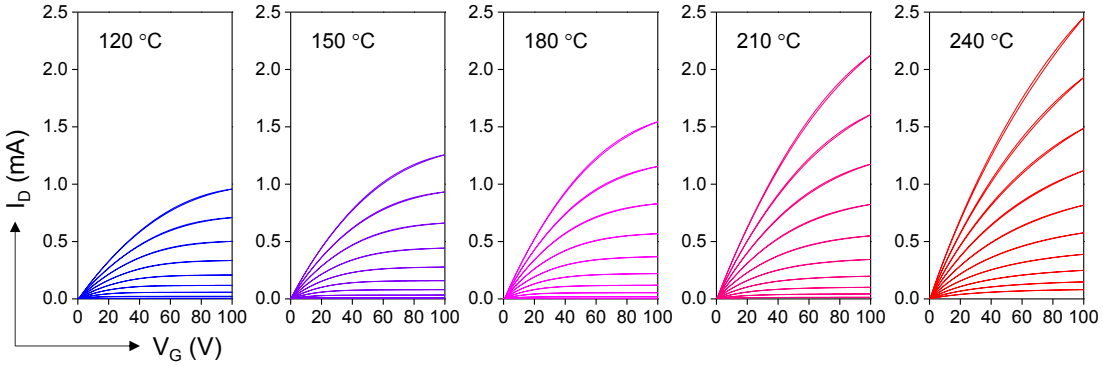


Figure 6.14: Corresponding output characteristics for the ZnO:Al-8m based TFTs in Figure 6.13. For each measurement, the gate bias (V_G) were set to the voltages in the range of 0–100 V at intervals of 10 V.

Table 6.3: Summary of device parameters: saturation mobility (μ_{SAT}), linear mobility (μ_{LIN}), turn-on voltage (V_{ON}), subthreshold swing (S.S.) and trap concentration (D_{tr}) for ZnO:Al-8m TFTs annealed at various temperatures in the range of 120–240 °C in ambient air.

	μ_{SAT} (cm^2/Vs)	μ_{LIN} (cm^2/Vs)	V_{ON} (V)	S.S. (V/dec)	D_{tr} ($eV^{-1}cm^{-2}$)
120 °C	3.11	1.53	4.5	1.19	1.02×10^{12}
150 °C	4.01	2.58	-3.6	2.10	1.84×10^{12}
180 °C	5.35	3.22	-8.1	2.68	2.36×10^{12}
210 °C	5.07	2.95	-30.7	4.88	4.35×10^{12}
240 °C	1.76	2.93	-66.8	8.03	7.19×10^{12}

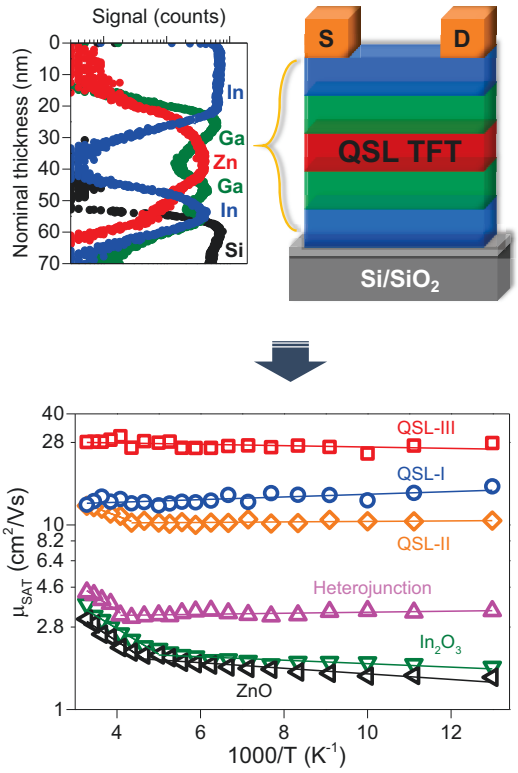
6.6 Conclusions

In this chapter, an effective and simple approach that allows doping of Zn-ammine complex solutions with Al, has been demonstrated. The approach not only retains the advantages of carbon-free aqueous Zn-ammine complex solution, i.e. low energetic metal-ammine dissociation and hydroxide condensation/dehydration, but also yields ZnO:Al transistors with enhanced performance (electron mobility >5 cm^2/Vs) at a low process temperature of 180 °C. From spectroscopic measurements, the Al doping effects have been observed to cause widening of the bandgap, i.e. blue shift, in the ZnO:Al samples. Diffraction measurements have revealed that the evolution of ZnO structures depends on the doping time and deposition temperature. In addition, the film morphology of both doped and un-doped samples has been examined with AFM.

The obtained results reveal that the surface topography, including surface roughness and grain size, has direct impact on the resulting TFT current-voltage characteristics. Moreover, XPS analysis indicate that ZnO:Al samples exist fewer trap sites than intrinsic ZnO layers. Through the incorporation of a variety of highly complementary characterisation tools, the present study provides an important insight into the structural and crystallographic properties of solution processed ZnO and Al-ZnO. The new aqueous-based doping route demonstrated here for the case of ZnO can be viewed as a simple and highly efficient method for enhancing the electrical performance of oxide-based devices.

7

QUASI-SUPERLATTICE METAL OXIDE THIN-FILM TRANSISTORS



In this chapter, a novel concept for thin-film transistors exploiting the enhanced electron transport properties of low-dimensional polycrystalline quasi-superlattices (QSLs), is presented. The QSLs consist of alternating layers of In_2O_3, Ga_2O_3 and ZnO grown by sequential spin casting of different precursors at low temperatures (180-200 °C) in ambient air. The prototype QSL transistors exhibit band-like transport with electron mobilities tenfold greater than binary-oxide based devices. From the results of temperature-dependent electron transport and capacitance-voltage measurements, the enhanced performance is believed to arise from the presence of quasi two-dimensional electron gas-like systems formed at the carefully engineered oxide heterointerfaces. The extraordinary electrical performance of the QSL-based transistors raises the possibility that one day this concept could revolutionise the field of thin-film transistors and the general field of large-area electronics. (Left panel: TOF-SIMS analysis of QSL and temperature-dependent characteristics.)

7.1 Introduction

Similar to many other transistor technologies, the performance and electrical characteristics of oxide TFTs depend on the properties of the employed materials. As such, the achievable field-effect mobility is ultimately dominated by the intrinsic carrier mobility of the semiconductor materials employed [66]. Nevertheless, for group IV and group III–V semiconductors-based devices this intrinsic limitation has successfully been overcome through the use of epitaxially grown heterostructures that consist of un-doped (intrinsic) and doped semiconductor layers [185-191]. In these heterostructures the majority carriers tend to diffuse out from the doped layer into the un-doped one through the mechanism of energy minimisation. As such, the dopant impurities are kept spatially separate from the field-effect channel, and the impact of scattering from impurity ions can be largely reduced. The migrating charge carriers are geometrically confined in a triangular-like quantum well in close proximity to the heterointerface, so they are free to move in a two-dimensional plane [187, 192].

These carriers originating from quantisation effects are generally referred to two-dimensional electron gases (2DEGs), and are able to trigger staggering charge-transport properties. As a result, an interesting physical phenomenon — the quantum Hall effect, was first observed in a 2DEG system [193], likewise the electrical performance of these heterostructures can easily outperform that of their constituent materials [190, 191]. Based upon this 2DEG effect a revolutionary device, namely the modulation-doped high electron mobility transistor (HEMT), was invented and is one of the most common semiconductor devices used nowadays [194]. The most notable advantage in using HEMTs lies in the ability to generate enormous carrier mobilities with maximum values in excess of 30,000,000 cm^2/Vs [195].

Developments in epitaxial growth techniques also enable the layer-by-layer formation of perovskite oxides with atomically-flat terminating planes [196, 197]. Such interfaces possess an isolated positively or negatively charged plane which, and in the absence of charge re-distribution, would give rise to the so-called polar catastrophe (gating) effect [197, 198]. The latter is the most common hypothesis explaining that as the thickness of polar perovskite increases over a critical value, the electrostatic potential attracts electrons to accumulate in available states at/near the

interfaces. Such a result resembles two-dimensional charge transport and opens a door to new rich physics [199-203]. Although very promising, from the viewpoint of technological applications, its dedicated fabrication process is very complex, and the resulting field-effect mobilities reported to date are only ≤10 cm^2/Vs at room temperature [204, 205], which is far below those offered by other semiconductor families [17, 41].

Another oxide interface system which has been extensively studied is the wide-bandgap semiconducting heterostructures of ZnO and Mg-doped ZnO (MgZnO or $Mg_xZn_{1-x}O$) [200, 206, 207]. Unlike the perovskite oxide interfaces, in the case of ZnO and $Mg_xZn_{1-x}O$ it is believed that the piezoelectric property causes a strain-induced mismatch in their electrical polarisation, resulting in localised charge accumulation at their interfaces [200, 207, 208]. The carrier density at the interface can be adjusted by changing the magnesium content in the $Mg_xZn_{1-x}O$ layer [200]. A Hall mobility of 5,500 cm^2/Vs as well as the quantum Hall effect were initially measured in this system [200]. Recent results have even shown mobilities of ~700,000 cm^2/Vs can be achieved following improvement of the materials purity [209, 210]. Moreover, the fractional quantum Hall effect has also been observed in this system [211].

The ZnO/MgZnO heterointerface has also been utilised as the active channel in TFT structures [212], which advances the technologies of oxide-based 2DEG towards practical applications in large-area thin-film electronics [42, 45, 213]. The emphasis of this chapter will be on the development of high performance TFTs based on low-dimensional multi-layered structures — namely quasi-superlattices (QSLs). A highly scalable and cost-effective solution-based fabrication process utilising oxide semiconductor materials is presented as a method to achieve such results. These structures were grown by sequential depositions of different metal oxides using spin casting and thermal annealing at temperatures in the range of 180–200 °C. Structural characterisation of the solution-based QSLs reveals the existence of discrete layers as well as the presence of high quality heterointerfaces. Remarkably, the implementation of the QSLs as the active channels in TFTs exhibits highly enhanced electron mobility with an increase of approximately one order of magnitude. Moreover, charge transport analysis shows temperature-independent behaviour, resembling band-like transport

characteristics — this observation is the first of its kind reported in oxide-based TFTs. Apart from the interesting electrical characteristics and improved device performance, the entire fabrication process is also demonstrated using temperature-sensitive substrates (i.e. plastic foils), and the resulting devices show highly promising field-effect mobilities of >10 cm^2/Vs.

7.2 Review on hetero-structured metal oxides and TFTs

7.2.1 Evidence of 2DEG formation in disordered semiconductors

In order to achieve cost-effective large-area electronics, one must look away from single crystalline material systems owing to their high costs and low-throughput manufacturing techniques. In 2010 Chin et al. used RF sputtering to fabricate $Mg_xZn_{1-x}O/ZnO$ heterostructures in an attempt to produce a disordered version of the well-studied, crystalline $Mg_xZn_{1-x}O/ZnO$ interfaces described above [214]. The measurements of Hall mobility in this disordered system showed temperature-independent behaviours, which was attributed to the 2DEG formation at $Mg_xZn_{1-x}O/ZnO$ interfaces from the spontaneously-induced polarisation effects. Using the same fabrication technique, Cheng et al. demonstrated a coplanar top-gate TFT based on the $Mg_{0.2}Zn_{0.8}O/ZnO$ structures that exhibited an enhanced electron mobility of 84.2 cm^2/Vs whilst the reference ZnO TFT only showed an inferior mobility of 1.5 cm^2/Vs [212]. Despite these promising findings, the behaviour of two-dimensional charge transport taking place in polycrystalline or amorphous TFTs is still an intriguing topic that needs further study to confirm its existence. On the other hand, Frenzel et al. fabricated metal-semiconductor field-effect transistors (MESFETs) using an $Mg_{0.1}Zn_{0.9}O$:Ga/ZnO/$Mg_{0.1}Zn_{0.9}O$:Ga quantum well that resembles the idea behind HEMTs [215], with high transconductance being observed from this MgZnO:Ga/ZnO/MgZnO:Ga MESFET. However there was no functional devices measured using this approach, mainly because of the use of the 100-nm thick MgZnO:Ga layers resulted in high potential barriers stopping charge injection from the electrodes.

For perovskite oxide families, the disordered equivalent of the $LaAlO_3/SrTiO_3$-type interface was investigated by Chen et al. [216]. In this work a metallic like interface was observed when depositing amorphous $LaAlO_3$, $SrTiO_3$ or yttria-stabilised zirconia deposited onto (001)-oriented single crystalline $SrTiO_3$ substrates with TiO_2-termination. The metallic conductivity was attributed to the formation of oxygen vacancies at/near the interface due to redox reactions taking place at the $SrTiO_3$ substrate surface. As a result, this study has shown that the formation of low-dimensional charge carrier systems in amorphous materials is indeed possible.

7.2.2 Quantisation effects in oxide semiconductor family

Although the existence of strongly-correlated electrons in a disordered system is unclear and requires much more evidence, the formation of quantised energy states in an imperfect disordered system is a thought-provoking idea worth further interrogation, in particular for electrical-performance improvement using low-cost processing manufacturing [217]. As dictated by the Schrödinger equation, carriers can spatially be confined in a low-dimensional potential well and have access to discreet energy states. Therefore, the confinement effect should still be expected to exist even in polycrystalline or amorphous materials as long as the low dimensionality can be possessed in a potential well. The main difference is that an ensemble of electrons in a potential well with a finite roughness would likely experience broadened available energies because of the well-width distribution. Nevertheless, one can still evaluate the probability of electrons in such a disordered system to have access to certain energies as long as the information for the width distribution of the well is available.

Taking an example of an infinite potential solution-processed ZnO well with a Gaussian distribution in its thickness, the energy distribution was calculated and shown in Figure 7.1 [126]. Although there exists a clear broadening of available energies as going from a perfect quantum well to that formed of structurally rough semiconductors, a large range of forbidden energies can still be found in this circumstance. Such a result suggests that one could indeed expect quantisation to take place in semiconductors of finite roughness.

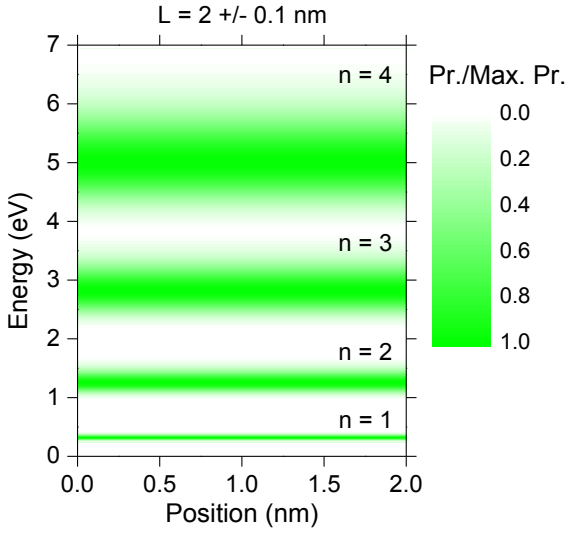


Figure 7.1: Probability distribution of lowest energy states of infinite quantum well with a mean thickness of 2 nm, a thickness standard deviation of 0.1 nm and an effective electron mass of 0.29 m_e. Green darker shade represents the most likely energy for a given sub-band state — see the scale bar for the ratio of probability (Pr.) to maximum probability (Max. Pr.).

For conventional III–V semiconductors, quantisation effects within GaAs/AlGaAs systems can be simply studied optically — when a bulk semiconductor undergoes a transition to two dimensional form, the quantisation of permitted energies taking place results in a blue-shift in the optical absorption spectrum of the system [218]. The same observation of this effect from an amorphous oxide superlattice (SL) structure made by radio frequency (RF) sputtering was reported by Abe et al. [163]. The SL structure was composed of alternating amorphous IGZO (a-IGZO) and amorphous Ga_2O_3 (a-Ga_2O_3) layers as the wells and barriers, respectively, and from the Tauc plots a clear blue-shift was observed with the reduction of the IGZO layer thickness. In particular, the measured blue-shift in optical bandgap was found to be in good agreement with the theoretical results from the Krönig-Penney model for such SL structures. This study, in line with finding for hydrogenated amorphous-Si based SL [219], has indicated that energy quantisation, regardless of the material crystallinity, could take place as long as the well thickness is comparable to the phase relaxation length. In a similar manner, optical blue-shift was also observed in the ultra-thin ZnO films obtained from Zn-ammine complex, and this quantisation effect was further realised for developing a so-called resonant tunnelling diode (RTD) for the first time using solution-based process [126].

7.2.3 Metal oxide semiconductor-based hetero-structured thin-film transistors

To provide feasible technologies for application in next-generation ultra-high-definition displays and other high-performance large-area microelectronics, device physicists and engineers continue to push for higher-and-higher field effect mobilities in oxide-based TFTs, and the approach of multi-layered superlattice-like TFTs has been proposed to fulfil this purpose [220]. The superlattice TFTs consisted of alternating layers of semiconducting ZnO and insulating Al_2O_3 deposited by atomic layer deposition (ALD). The mobility of these devices was found to increase from 4.8 cm^2/Vs to 27.8 cm^2/Vs when replacing the single-layer ZnO film with the ZnO/Al_2O_3 superlattice for the TFT channel layer. Since the insulating layers of Al_2O_3 can form a high potential barrier that causes difficulty for charge injection as seen in a similar study using a ZnO/MgZnO:Ga configuration [215], the electrodes in the superlattice TFT structure were grown on the sides of the entire film stack to guarantee an effective injection for each ZnO channel. Given the fact that the thickness of each oxide layer was reduced down to only ~5 nm, the charge transport was believed to change from bulk to two dimensional, and the electrical performance was therefore enhanced. Although the ALD method used here cannot be considered either a cost-effective fabrication process or a high-throughput large-area manufacturing technique, the superlattice concept has demonstrated its potential to improve electrical performance for the targeting applications mentioned above, and the research community surely would like to take a step further to fabricate such structures using scalable low-cost deposition techniques.

Rather than building a complex superlattice-like structure, recently some attempts have been carried out using solution-based approaches to develop bilayer metal oxide TFTs [115, 221]. Rim et al. reported bilayer heterostructure TFTs based on the solution-processed semiconductive InGaZnO (IGZO) and InSnZnO (ITZO) layers [115]. By stacking IGZO on top of ITZO, the bilayer transistors exhibited electron mobilities of ~22 cm^2/Vs that was approximately an order of magnitude higher than that obtained from a single-layer IGZO device meanwhile a high on/off ratio of $\sim 10^7$ was achieved using the bilayer approach. Such a dramatic improvement

was attributed to the main charge carriers being confined within the ultra-thin highly-dense ITZO bottom layer whilst a deeper Fermi level possessed by IGZO created a barrier to reduce the off-current level and at the same time enlarge the on/off ratio. The work reported by Rim et al., though very interesting, however requires a thermal annealing process at temperatures >400 °C [115]. This is not compatible with any temperature-sensitive substrates; in addition, there have been many other approaches proposed to achieve similar electrical performance under such conditions [43, 44, 76-78, 139]. Yu et al. also fabricated bilayer TFTs that were composed of a bottom indium oxide (In_2O_3) layer and a top indium gallium oxide (IGO) layer via a solution-processed low-temperature combustion process at 200–300 °C [221]. The improvement was attributed to the Femi level of the In_2O_3 layer in close proximity to the conduction band edge being able to induce the charge transfer to pre-fill empty traps in the IGO film.

So far, the solution-based approaches for oxide TFTs have not shown any evidence of low-dimensional charge transport. In addition, the performance of the optimised bilayer devices reported to date were often a compromise between those obtained from the use of a highly-conductive material and a material with moderate/poor charge-transporting properties. Rather, a heterosturucture-based TFT is expected to outperform those made with its constituent materials. In the following, the focus will be placed on the newly-proposed QSL concept as described in Section 7.1, and an in-depth study, from material synthesis to flexible device applications, will be provided.

7.3 Low-dimensional metal oxide layer grown from solution phase

7.3.1 Material preparation, film deposition and device fabrication

Similar to Section 5.3.2, Zn ammine complex solutions were prepared by dissolving ZnO hydrate ($ZnO \cdot xH_2O$, 97% Sigma-Aldrich) in ammonium hydroxide (Alfa Aesar, 50% v/v) at 7.5 mg/mL. As-prepared solutions were then stirred rigorously at room

temperature for 2 h. This process yielded a clear transparent Zn-ammine complex solution. For the growth of In_2O_3 layers, the precursor solution was prepared by dissolving anhydrous indium nitrate [$In(NO_3)_3$, 99.99% Indium Corporation] in deionized (DI) water at a concentration of 30 mg/mL. The solution was subjected to rigorous stirring at room temperature for 60 min before use. For solution-processable gallium oxide (Ga_2O_3), the precursor solution was prepared by dissolving gallium nitrate hydrate [$Ga(NO_3)_3 \cdot xH2O$, 99% Sigma-Aldrich] in DI water at a concentration of 8 mg/mL. The solution was also stirred at room temperature for 1 h just before use.

For the In_2O_3 and ZnO TFTs, the film deposition was carried out by spin-casting the precursor solutions onto the Si^{++}/SiO_2 substrates at 4000 rpm for 30 sec in ambient air, followed by a post-deposition thermal-annealing process for 30 min at 180–200 °C in ambient air. The overall layer thickness was controlled by the number of deposition steps performed. For single-oxide ZnO and In_2O_3 transistors, semiconductors were grown using a double-deposition step in order to match the overall thickness of the channel layer in the QSL structures. Fabrication of the In_2O_3 and ZnO transistors was completed with the thermal evaporation of 40-nm thick Au and Al top source and drain (S-D) electrodes through a shadow mask in high vacuum (~10^{-6} mbar), respectively.

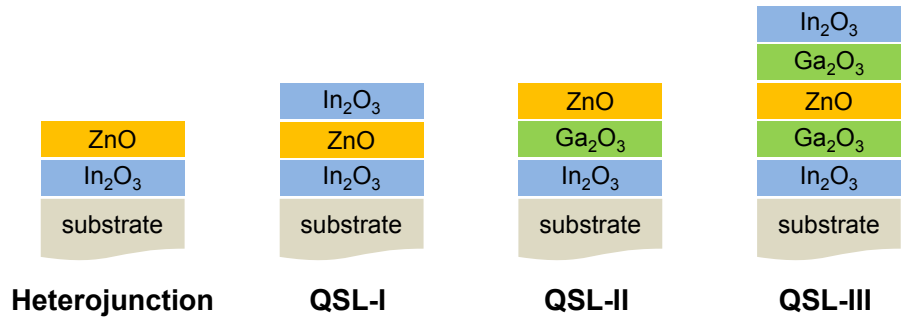


Figure 7.2: Schematics of the different layered structures studied in this work, including heterojunctions (In_2O_3/ZnO, In_2O_3/Ga_2O_3, ZnO/Ga_2O_3) and multilayer QSLs consisting of In_2O_3/ZnO/In_2O_3 (QSL-I), In_2O_3/Ga_2O_3/ZnO (QSL-II) and In_2O_3/Ga_2O_3/ZnO/Ga_2O_3/In_2O_3 (QSL-III).

As shown in Figure 7.2 there were four different bilayer and multilayer transistor structures fabricated in the present study. The fabrication of heterojunction and QSL-based transistors was performed using identical spin-casting and thermal-annealing conditions to those used for the fabrication of ZnO and In_2O_3 transistors

with the exception that for QSL-I and QSL-III each In_2O_3 layer growth was performed using a single-step deposition in order to maintain a similar total thickness to other devices. Deposition of Ga_2O_3 layers was carried out using only one single-deposition step. Top S-D electrodes in QSL transistors were formed by thermal evaporation of 40-nm thick Au through a shadow mask in high vacuum for transistors prepared on Si^{++}/SiO_2 wafers.

7.3.2 Morphology, crystallinity and composition analysis of oxide layers

The cross-sectional high-resolution transmission electron microscopy (HRTEM) images of ZnO formed using the standard recipe for fabricating devices (see Section 7.3.1) are shown in Figure 7.3(a). It can be seen that the ZnO is polycrystalline, and the thickness is in the range of 4–6 nm. For surface morphology, the as-grown ZnO layers show clear crystalline domains with root mean square (rms) surface roughness of ~0.43 nm as determined by atomic force microscopy (AFM) [see Figure 7.3(b)]. Using grazing incident diffraction (GID) measurements, multiple crystalline peaks are confirmed existing in the ZnO films as seen in Figure 7.3(c). It is worth mentioning that the high-resolution GID results have revealed insightful information indicating the presence of highly crystalline domains within these ultra-thin ZnO layers – a feature never reported previously for such low-dimensional systems [222].

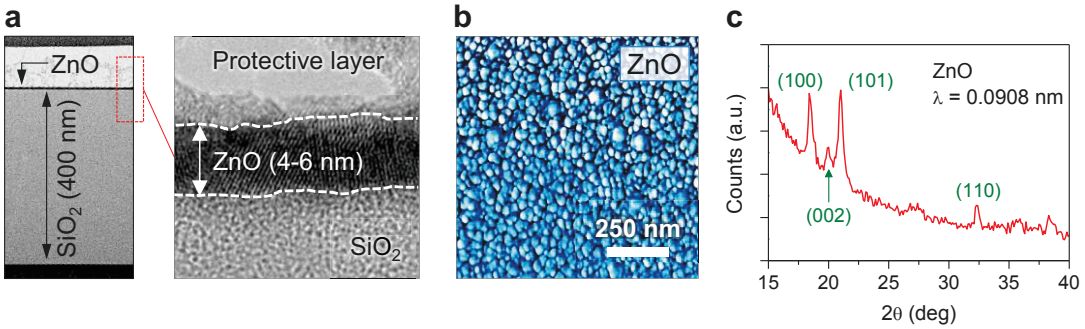


Figure 7.3: (a) HRTEM cross-sectional images of the SiO_2/ZnO interface. Left panel: low-magnification image confirms the existence of an ultra-thin and continuous ZnO film. Right panel: high-magnification image reveals the presence of polycrystalline ZnO regions with clear lattice fringes. (b) AFM phase images of ZnO film with clear grain features, the calculated rms surface roughness is of ~0.43 nm. (c) GID measurement (using X-ray wavelength $\lambda = 0.0908$ nm) shows powder-like crystallisation coexisting in the ZnO film.

For In_2O_3, the ultra-thin layers (5–10 nm) were grown by a double spin-casting step as described in Section 7.3.1. The HRTEM images shown in Figure 7.4(a) reveal large crystalline domains >10 nm in the In_2O_3 films, whilst it is also found that the films are continuous and ultra-smooth (rms ~0.2 nm) as seen in the AFM results in Figure 7.4(b). The polycrystalline nature of In_2O_3 is confirmed by the GID measurements [Figure 7.4(c)], and the obtained crystallinity of In_2O_3 has shown good agreement with the data reported in previous works [109]. Similarly, ultra-thin (2–5 nm) films of stoichiometric Ga_2O_3 were grown using the processing steps described above. However, unlike ZnO and In_2O_3, Ga_2O_3 layers appear to be largely amorphous with no signs of crystallinity (no detectable diffraction peaks).

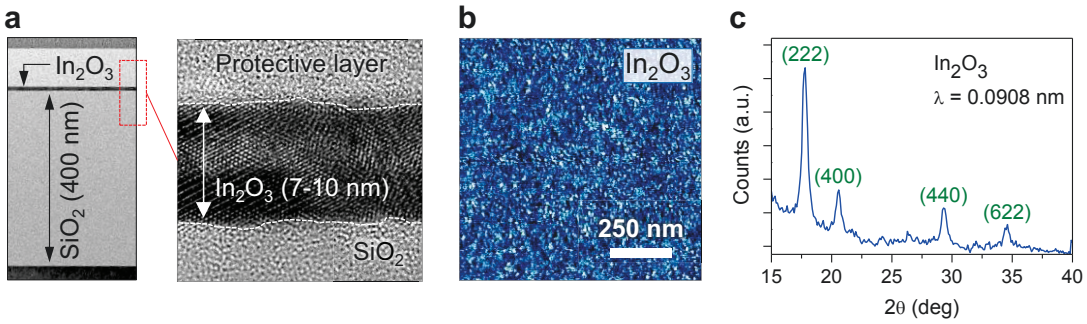


Figure 7.4: (a) HRTEM cross-section images of the SiO_2/In_2O_3 interfaces reveal the presence of an ultra-thin and smooth In_2O_3 film with highly-oriented large crystalline domains. (b) AFM phase image of the In_2O_3 film. The corresponding rms surface roughness is obtained of ~0.20 nm. (c) GID analysis (X-ray wavelength λ= 0.0908 nm) reveals powder-like crystallization characterising the In_2O_3 layers.

The elemental compositions of the discrete metal oxide films were verified by X-ray photoelectron spectroscopy (XPS) (Figure 7.5). For semiconducting ZnO and In_2O_3, O1s core level spectra are analysed in Figure 7.5(a) and (b) respectively in order to understand the chemical bonds between oxygen and metal. The O1s envelope obtained here can be deconvoluted into two main peaks that are located below 530 eV (O^{2-} in ZnO wurtzite structures) and over 532 eV (aqueous adsorbates on the surface of ZnO or Zn-hydroxide species) [180, 181]. The observation of hydroxide-related groups can be attributed to the re-adsorption of ambient moisture on the reactive ZnO surface and/or the existence of partial unconverted precursor impurities. Similarly, the O1s peak in In_2O_3 can be deconvoluted into three different components — ~530 eV: O in oxide lattices without vacancies, ~532.0 eV: O in oxide lattices with vacancies

and ~533 eV: O in hydroxide-related species [151]. From Figure 7.5(b) the obtained O1s peak consists of two main energies at ~530 eV and ~532 eV. Such a result reveals a high-quality In_2O_3 layer can be achieved with this aqueous-based precursor system since only a minimum (barely resolvable) hydroxide-related content could be found in the final film stage [109]. Figure 7.5(c) shows the XPS spectrum of Ga 3d core level peaks whilst the inset in Figure 7.5(c) displays the core level spectrum of Ga $2p_{3/2}$. The binding energy of Ga 3d peak can be deconvoluted into two components at ~18.5 eV and ~20.9 eV, which are assigned to metallic Ga and Ga–O bonds, respectively [223-225]. The inelastic mean free path, λ, of electrons with kinetic energy 367.8eV for Ga $2p_{3/2}$, $\lambda_{Ga2p3/2}$ ~ 0.9 nm, is three times less than that of electrons with kinetic energy 1066.7eV for Ga 3d, λ_{Ga3d} ~ 2.66 nm through an inorganic matrix. Furthermore, the Ga 2p peak at ~1118.8 eV is attributed to the presence of the Ga_2O_3 component. Owing to the fact that XPS is a surface-sensitive measurement technique the measured information obtained by XPS mainly comes within three attenuation lengths from the sample surface. Therefore, it is suggested that metallic Ga may exist deep within the Ga_2O_3 films.

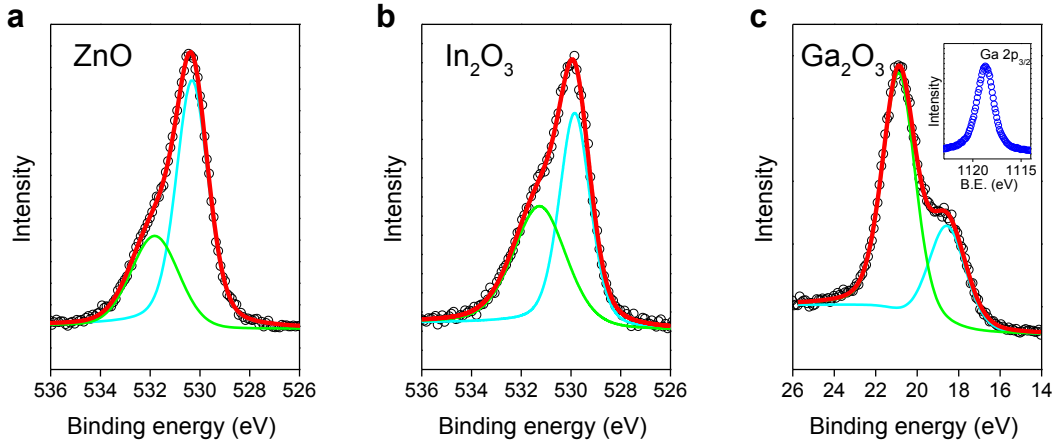


Figure 7.5: (a) and (b) show the core level spectrum for ZnO and In_2O_3, respectively. (c) and the inset show the XPS spectra of Ga 3d and Ga $2p_{3/2}$ core level, respectively.

The ultraviolet photoelectron spectroscopy (UPS) was used to determine the valence band edge from the vacuum level: ~6.99 eV, ~7.85 eV and ~8.38 eV for ZnO, In_2O_3 and Ga_2O_3, respectively (see Figure 7.6). The obtained ionized energies show good agreement with the data reported in the literature [226, 227].

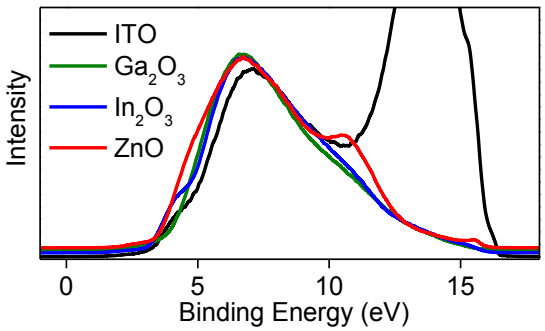


Figure 7.6: UPS spectra used to determine the valence band edge from the vacuum level for individual oxides. The work function of the reference ITO is ~4.73 eV.

7.3.3 Optical properties and energy-level quantisation

The absorption spectra for the discrete metal oxide layers are displayed in Figure 7.7(a) whilst Figure 7.7(b)–(d) show optical bandgaps (E_G) of each oxide using Tauc analysis (see below for more details regarding this technique) on the absorption spectra in Figure 7.7(a). The extracted optical bandgap for ZnO, In_2O_3 and Ga_2O_3 are 3.36 eV, 3.87 eV and 4.95 eV, respectively. These results show good agreement with those reported by others [227-229].

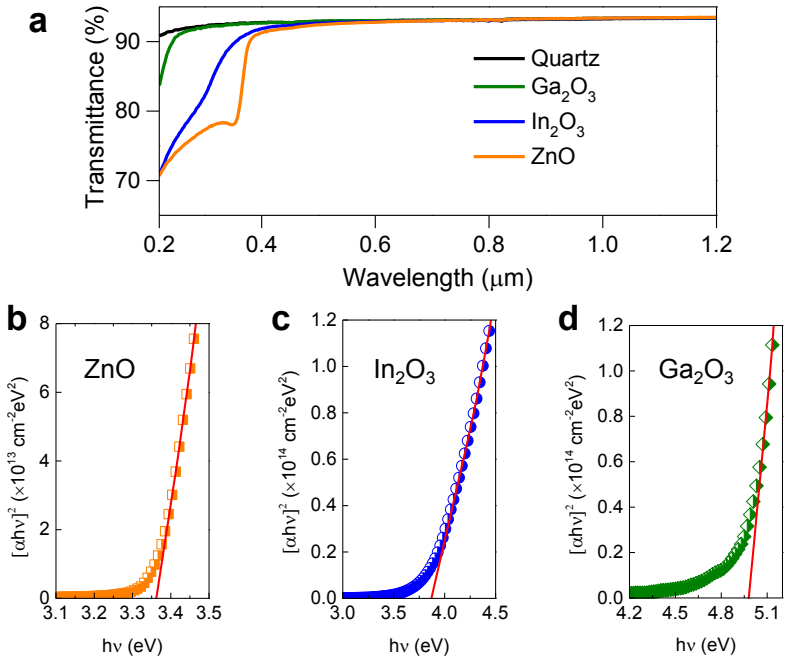


Figure 7.7: (a) UV-Vis-NIR transmission spectra of the blank quartz substrate, Ga_2O_3, In_2O_3 and ZnO films (all measured with quartz substrates and data shown here without substrate subtraction). Tauc plots of (b) ZnO, (c) In_2O_3 and (d) Ga_2O_3 thin-film layers. The extracted optical bandgaps are 3.36 eV, 3.87 eV, and 4.95 eV for ZnO, In_2O_3 and Ga_2O_3, respectively.

As mentioned in the previous section, reducing the semiconductor thickness to appreciable nanoscale dimensions is expected to impact the physical properties of the resulting oxide layers due to energy quantisation phenomena [126, 163, 230]. More specifically, a widening in the bandgap energy of the semiconductor is expected to be seen as the layer thickness reduces (t). To further investigate this effect several absorption measurements were carried out by depositing solution-processed ZnO and In_2O_3 layers of variable thickness onto quartz substrates [see Figure 7.8(a)], and the optical bandgap was calculated using Tauc analysis [162, 231]. This technique entails plotting $(\alpha h\nu)^X$ against the incident photon energy ($h\nu$) and then extrapolating the linear part of the plot to $(\alpha h\nu)^X = 0$ to acquire the bandgap value. Here, α is the optical absorbance of the material, and X is an exponent that depends on the nature of the semiconductor bandgap i.e. direct or indirect. For direct bandgap semiconductors X = 2 is used whilst for indirect bandgap semiconductors X = 1/2 is used. Since the nature of the band structure in In_2O_3 is still under debate [232-234], both direct- and indirect-bandgap approaches are investigated in the present study. ZnO is known to be a direct bandgap semiconductor [235] — thus the value of X = 2 was employed.

By defining the dimension perpendicular to the substrate surface as (z) [Figure 7.8(a)], the energy of conduction band and valence band states available to electrons $E_{n,e}$ and holes $E_{n,h}$, respectively, confined to an infinite quantum well (QW) can be described by [230]:

$$E_{n,e} = E_{xy} + \frac{n^2 h^2}{8 m_e^* t^2}, \tag{7.1}$$

$$E_{n,h} = E_{xy} - \frac{n^2 h^2}{8 m_h^* t^2} \tag{7.2}$$

where E_{xy} is the energy associated with the carrier in the (unconfined) xy-plane, n is a positive integer, h is the Planck constant, m_e^* is the effective mass of electrons in the semiconductor, m_h^* is the effective mass of holes in the semiconductor and t is the thickness of the quantum well in the z-direction [Figure 7.8(a)]. Since the energy of the first electron state (n = 1) increases with the reduction of t, thus the conduction

band minimum (CBM) increases. In a similar manner, the energy of the first hole state (n = 1), and hence the valence band maximum (VBM), decreases. As a result the energy of the first allowed transition from the VBM to the CBM in the confined direction increases resulting in a blue-shift in the onset of the optical absorption. Therefore, by assuming that the optical properties of layers with thickness >20 nm are representative of the bulk semiconductors, the increase in bandgap (ΔE_G) for each thin-film layer relative to the bulk state can be evaluated using Equation 7.1 and 7.2 to express ΔE_G as a function of t [218]:

$$\Delta E_{\mathrm{G}} = \frac{h^2}{8t^2}\left(\frac{1}{m_e^*} - \frac{1}{m_h^*}\right). \tag{7.3}$$

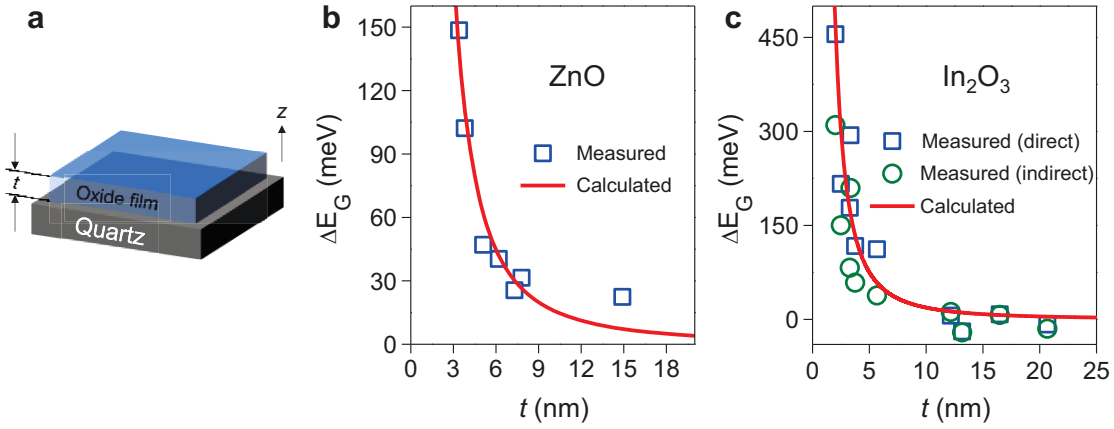


Figure 7.8: (a) Schematic illustration of the sample configuration used for the optical absorption measurements where t represents the layer thickness of the spin-coated oxide semiconductor. (b) Plot of the change in optical bandgap (ΔE_G) calculated via Tauc analysis as a function of film thickness (t) for several ZnO layers with respect to that of bulk ZnO (t > 20 nm). (c) Plot of ΔE_G calculated via Tauc analysis assuming a direct (squares) and an indirect (circles) bandgap, versus film thickness for several In_2O_3 layers with respect to that of bulk In_2O_3 (t > 20 nm). In both (b) and (c) plots the solid red lines represent the calculated ΔE_G for an infinite quantum well using Equation 7.3.

Due to the large bandgap of the quartz substrates (~8.9 eV) the single layers of ZnO and In_2O_3 can be modelled as infinite QW. Though finite QW energies were also calculated using known techniques [236], the results were found to be negligibly different from those evaluated using the infinite QW approximation (Equation 7.3).

The values for the effective mass of electrons m_e^* and holes m_h^* employed in In_2O_3 were $m_e^* = 0.3\ m_e$ and $m_h^* = 0.6\ m_e$ where m_e is the rest-mass of an electron in a vacuum [237], whilst the values of effective mass for ZnO were $m_e^* = 0.29\ m_e$ and $m_h^* = 1.2\ m_e$ [238, 239]. Figure 7.8 (b) and (c) display the measured increase in bandgap (ΔE_G) as a function of L extracted using the Tauc analysis as described above. The solid lines in each plot represent the theoretical values for ΔE_G calculated using Equation 7.3. Good agreement between the ΔE_G data determined experimentally and those predicted theoretically is observed for both material systems. In the case of ZnO layers, reducing t leads to ΔE_G values close to ~150 meV, whilst in the case of In_2O_3 this difference is much larger and approaches ~450 meV. More interestingly, for In_2O_3 layers the extracted ΔE_G values show good agreement, within experimental errors, with those calculated by assuming either a direct or an indirect bandgap. Based on the obtained data, it can be concluded that reducing the thickness of the ZnO and In_2O_3 layers results in a characteristic widening of the optical bandgap in line with theoretical predictions for energy quantisation in such oxide systems.

However, in Figure 7.8 one may notice that although the effective electron mass in ZnO is approximately the same with that in In_2O_3, the measured ΔE_G is not identical (~150 meV for ZnO vs ~450 meV for In_2O_3). The reason for this observation may be the fact that firstly, the effective hole mass is different in the two systems (for ZnO it is 1.2 m_e whilst for In_2O_3 it is 0.6 m_e) so that a slightly larger increase in bandgap is expected for the In_2O_3 system. Secondly, the theoretical lines calculated in Figure 7.8(b) and (c) employ the effective-mass approximation, which assumes that the semiconductor is crystalline. However, the films studied here are known to be polycrystalline (see Figure 7.3 and 7.4) so that the effective carrier mass will not be constant as a function of energy. Although such an approximation is not expected to substantially alter the trend, one would expect the differences in crystallinity between ZnO and In_2O_3 layers to manifest themselves in the measured ΔE_G values. Additionally, for the sake of conciseness, surface roughness is another factor that has not been considered in Figures 7.8(b) and (c). Finally, the infinite quantum well approximation was employed here despite the systems in fact being finite quantum wells (albeit extremely deep wells). Since the conduction band minima of ZnO and In_2O_3 are different (−3.63 eV for ZnO vs −3.98 eV for In_2O_3, see next section), the

depth of these wells will in fact be slightly different. As mentioned before, the data obtained by using a finite quantum well approximation is negligibly different from that obtained using the infinite quantum-well approximation in this study. These differences between the two systems are none-the-less noteworthy, despite being unlikely to affect data in a noticeable way.

7.4 Structural characterisation of oxide quasi-superlattices

7.4.1 X-ray reflectometry and atomic force microscopy analysis

Using the sequential spin-coating deposition method described previously (Section 7.3.1), heterojunction and QSL structures composed of oxide film stacks shown in Figure 7.2 were grown. The interface quality between In_2O_3, ZnO and Ga_2O_3 and surface quality of each oxide and multi-layered oxides were investigated using X-ray reflectometry (XRR). Figure 7.9 displays the obtained experimental data (blue solid lines) with the presence of clear interference fringes. The latter shows good agreement with the theoretical simulation results (red dashed lines in Figure 7.9) that were derived using the parameters summarised in Table 7.1.

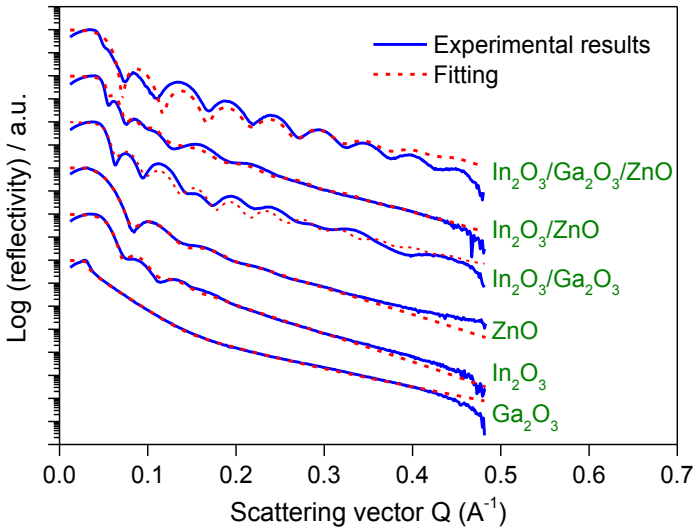


Figure 7.9: XRR measurements obtained from single, bilayer and multilayer oxide structures. Measured and calculated spectra are shown in blue solid lines and red dashed lines, respectively.

From Figure 7.9, one should notice that the individual oxide samples generally exhibit interference fringes in a shorter angular range than compared to those measured from stacked oxide films. The lower reflection edge implies the samples could contain higher roughness at either the surface or interface. From the AFM measurements in Figure 7.3(b) and Figure 7.4(b), the single-oxide films exhibit ultra-smooth surface morphology (rms < ~0.4 nm) and the roughness data used to fit the XRR measurements (i.e. Table 7.1) is expected to be in line with these AFM results. As such, the finding of a shorter angular range from the single-oxide films suggests that the interface roughness is significantly higher than the film surface roughness. Moreover, owing to the fact that the substrates roughness used here, i.e. SiO_2, is expected to be ≤5 Å, the extracted high interface roughness most likely originates from the composite SiO_2/In_2O_3 interface, rather than solely from the SiO_2 substrate.

Table 7.1: Summary of the fitting parameters namely, layer thickness (d), scattering length density (ρ) and surface/interface root-mean-square roughness (rms), used to fit the experimental XRR spectra for each oxide combination studied in Figure 7.9.

Single metal oxide layers						
Film	**ZnO**		**In_2O_3**		**Ga_2O_3**	
Layer	ZnO	SiO_2	In_2O_3	SiO_2	Ga_2O_3	SiO_2
d (Å)	93.6	N/A	122.04	N/A	35.89	N/A
ρ ($Å^{-2}$)	4.50×10^{-5}	1.87×10^{-5}	5.07×10^{-5}	1.87×10^{-5}	4.71×10^{-5}	1.87×10^{-5}
rms (Å)	4.272	11.104	4.66	17.218	3.045	14.217
Metal oxide bilayers						
Film	**ZnO/ In_2O_3**			**Ga_2O_3/ In_2O_3**		
Layer	ZnO	In_2O_3	SiO_2	Ga_2O_3	In_2O_3	SiO_2
d (Å)	134.47	85.66	N/A	33.04	116.5	N/A
ρ ($Å^{-2}$)	4.50×10^{-5}	5.19×10^{-5}	1.87×10^{-5}	5.60×10^{-5}	4.56×10^{-5}	1.87×10^{-5}
rms (Å)	3.969	15	24.555	3.379	6.5	6.175
Metal oxide QSL-II						
Film	**ZnO/ Ga_2O_3/In_2O_3**					
Layer		ZnO	Ga_2O_3	In_2O_3	SiO_2	
d (Å)		60.46	26.73	31.69	N/A	
ρ ($Å^{-2}$)		4.50×10^{-5}	4.72×10^{-5}	5.20×10^{-5}	1.87×10^{-5}	
rms (Å)		2.441	2.502	5.3	5.643	

More interestingly, the fitting parameters in Table 7.1 also suggest that incorporation of the Ga_2O_3 as an interlayer in-between In_2O_3 and ZnO (i.e.

$ZnO/Ga_2O_3/In_2O_3$ vs ZnO/In_2O_3) or a top layer on In_2O_3 (i.e. Ga_2O_3/In_2O_3 vs In_2O_3) leads to a significant reduction in the interfacial roughness. This observation is in qualitative agreement with the AFM data shown in Figure 7.10, in which the In_2O_3/ZnO heterojunction structure exhibits a higher surface roughness value (~21 Å) than that obtained from QSL-II (~12 Å). In addition, QSL-I and QSL-III stacks show ultra-smooth surfaces with rms values of only ~2.2 Å and ~4 Å, respectively. Such a result provides evidence that incorporation of Ga_2O_3 and In_2O_3 helps to planarise both the buried heterointerfaces and surfaces of the QSLs.

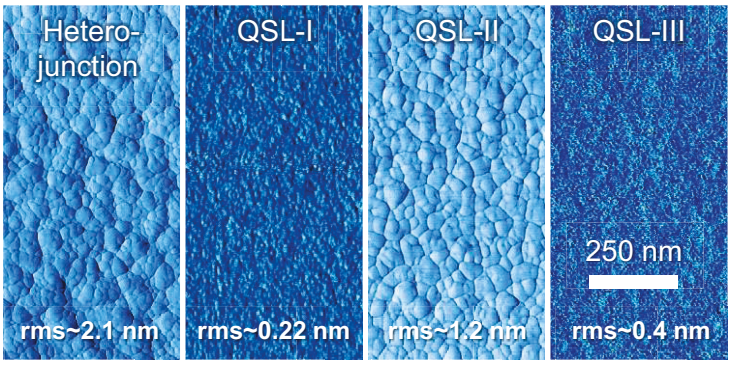


Figure 7.10: AFM surface phase images of the different structures namely; heterojunction, QSL-I, QSL-II and QSL-III.

7.4.2 Time-of-flight secondary ion mass spectrometry analysis

The elemental composition profiles as a function of depth was analysed using time-of-flight secondary ion mass spectrometry (TOF-SIMS) in order to examine whether chemically sharp interfaces do exist between the different oxide layers, processed from solution. In the present study, the TOF-SIMS measurement was carried out on the most complex QSL structure, i.e. QSL-III, and Figure 7.11 shows the Poisson corrected ion signals as a function of nominal thickness (air interface at x = 0 nm). It should be noted that the thickness of the entire QSL-III structure was measured at only ~20 nm (obtained from HRTEM, data not shown), and the thickness was <5 nm for each single-oxide layer [see Figure 7.3(a) and 7.4(a)]. Although the latter is in fact approaching the measurement limit of TOF-SIMS, the observation of the sharp increases in the leading and trailing edges of the ion signals indicates rather distinct

interfaces existing between the In_2O_3 and Ga_2O_3. In addition, the gradual increase in Zn ion signal within the Ga_2O_3 layer and concurrent loss of Ga ion dynamic range is a typical example of interfacial broadening due to interfacial roughness. Moreover, it is known the effect is more profound in relatively rougher crystalline state — a feature has been seen in the cross-sectional HRTEM images of the ZnO layers [Figure 7.3(a)]. Therefore, based on the XRR (Figure 7.9) and TOF-SIMS (Figure 7.11) data it is suggested that that the solution-grown oxide multilayers are composed of ultra-thin alternating layers separated by well-defined interfaces with relatively limited intermixing.

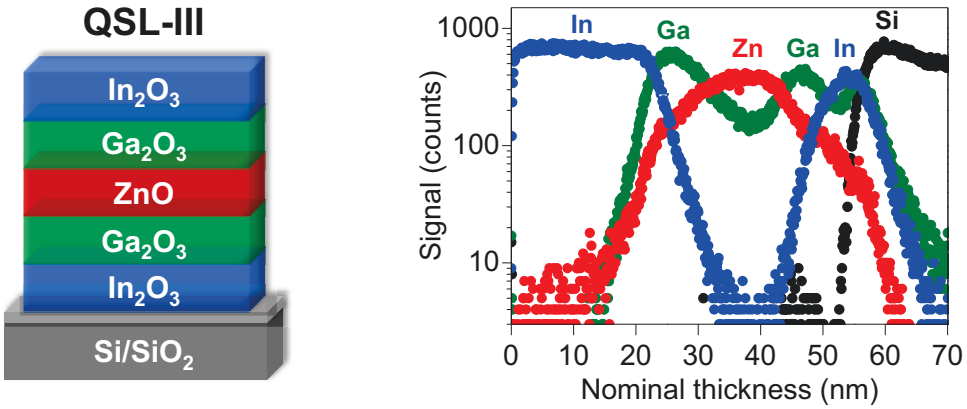


Figure 7.11: TOF-SIMS analysis for a QSL-III grown on Si^{++}/SiO_2 substrate. Here a thicker top layer of In_2O_3 (~25 nm) was employed in order to stabilize the ion beam during measurement.

7.4.3 Kelvin Probe characterisation and energy diagram

The Fermi energies (E_F) were acquired from the Kelvin Probe (KP) measurements performed in nitrogen (Figure 7.12), yielding E_F ~4.32 eV, E_F ~4.65 eV and E_F ~4.90 eV for ZnO, In_2O_3 and Ga_2O_3, respectively, whilst highly oriented pyrolytic graphite (HOPG) and Ag were used as the reference. To better understand how energy minimisation can result in charge transfer, the energy diagram displaying the measured energy levels of the individual oxide layers used to form the heterojunction and QSL-I, before contact, were constructed [Figure 7.13(a)]. In contrast to previously published studies in which bilayer metal oxide structures and transistor channels were formed using similar chemical elements [221, 240], the system here is based on two different oxides (i.e. ZnO and In_2O_3) with significant difference between their Fermi

energies (ΔE_F ~300 meV). Due to the latter, electrons transfer from ZnO to In_2O_3 upon physical contact [Figure 7.13(b)]. Since the available energy levels at the CBM in the ultra-thin In_2O_3 layer are known to be quantised [Figure 7.8(c)], the transferred electrons are likely confined in a two-dimensional potential well. On the basis of this discussion it can be argued, that the current system may resemble a 2DEG-like system that is found in the more conventional MgZnO/ZnO heterointerface [212]. However, owing to the polycrystalline nature of the In_2O_3 layer [Figure 7.4(c)] the confined electrons may not behave like traditional 2DEGs, since macroscopic conduction in the QSL-I is expected to be hindered by the presence of grain boundaries – experimental evidence for the latter can be found in the HRTEM images in Figure 7.4.

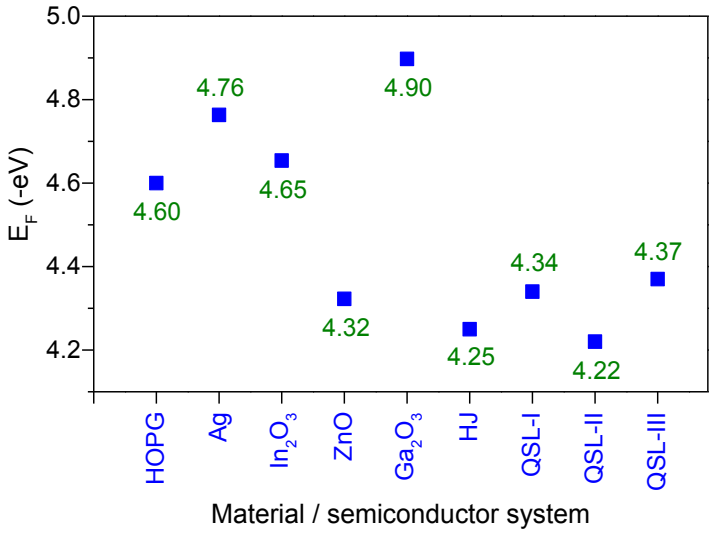


Figure 7.12: Kelvin Probe (KP) analysis of the Fermi energy levels of highly-ordered pyrolytic graphite (HOPG), silver (Ag), In_2O_3, ZnO, Ga_2O_3, heterojuction (HJ), QSL-I, QSL-II, and QSL-III.

In the case of QSL-II and QSL-III, insertion of the Ga_2O_3 interlayer with deeper Fermi energy [Figure 7.13(c)] may enhance electron migration from In_2O_3 and ZnO and at the same time improve electron confinement because of the higher interface planarity as mentioned earlier (Table 7.1). This process is illustrated in Figure 7.13(d) in the energy diagram of QSL-III after contact. Similar to the QSL structure shown in Figure 7.13(b), the QSL-III exhibit a shallower Fermi energy (against vacuum) as compared to the state before contact. This finding suggests the carriers could well occupy the states closer to the mobility edge [54, 55]. Moreover,

Ga is known to passivate interface electron trap states owing to the presence of oxygen and/or hydroxyl groups during Ga_2O_3 formation [116, 241, 242]. Therefore, the combination of these beneficial attributes may yield heterointerfaces with improved electron transporting properties as compared to simple In_2O_3/ZnO heterointerfaces [Figure 7.13(b)]. In view of these experimental findings, there exists a possibility that a confined electron system in In_2O_3/ZnO and QSL-I structures is expected to form in the vicinity of each In_2O_3/ZnO heterointerface due to the mismatch between the conduction and Fermi energies of the semiconductors. On the other hand, the presence of the deeper Fermi energy Ga_2O_3 layer in the QSL-II and QSL-III systems is expected not only to planarise the heterointerface(s) but also to improve the electron confinement due to its favourable energetics and trap passivation properties.

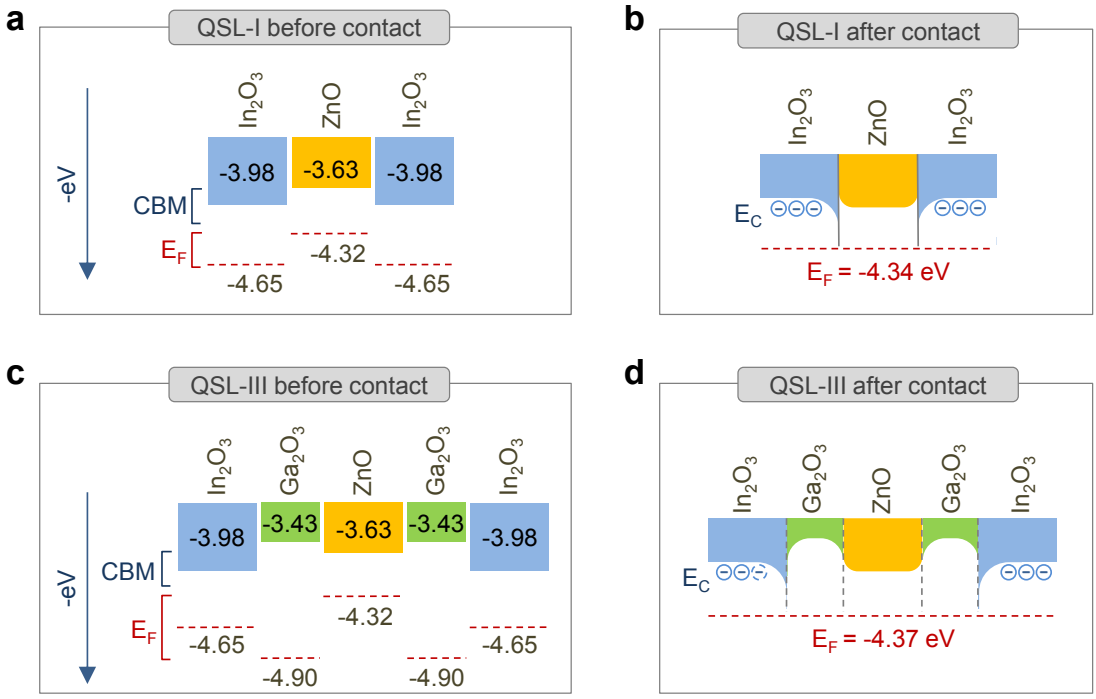


Figure 7.13: (a) Measured energy levels of the individual oxides used in QSL-I before contact. (b) Schematic energy band diagram of QSL-I after contact. (c) Energy levels of the individual oxides used in QSL-III before contact. (d) Schematic energy diagram of QSL-III after contact.

7.5 Electrical characterisations of quasi-superlattice oxide transistors

7.5.1 Temperature-dependent electron transport measurements

To study the nature of charge transport in these complex oxides structures, bottom-gate, top-contact (BG-TC) field effect transistors were fabricated using ZnO, In_2O_3, ZnO/In_2O_3, QSL-I, QSL-II and QSL-III as the channel layers [Figure 7.14(a)]. The representative transfer characteristics of all the oxide samples are shown in Figure 7.14(b). The room temperature saturation mobilities (μ_{SAT}) calculated for ZnO and In_2O_3 transistors were similar and in the range 2–4 cm^2/Vs whilst transistors based on In_2O_3/ZnO heterojunction channels exhibit slightly improved electron transport with maximum mobility values in the range 3–5 cm^2/Vs. It is found that remarkable μ_{SAT} values were obtained with increasing channel complexity, reaching values between 10–12 cm^2/Vs for QSL-I and QSL-II based devices and up to 25–30 cm^2/Vs for QSL-III based transistors. It is clear that insertion of the Ga_2O_3 interlayers between In_2O_3 and ZnO to form QSL-II is found to significantly improve the electron mobility of the devices as compared to the geometrically similar ZnO/In_2O_3 heterojunction-based ones whilst in the case of QSL-III transistors the impact of the Ga_2O_3 interlayer is even greater when compared to QSL-I, which bears high similarity to QSL-III. To this end the μ_{SAT} [Figure 7.14(c)] and the linear electron mobility (μ_{LIN}) [Figure 7.14(d)] measured for optimised QSL-III devices are amongst the highest reported to date for solution-based metal-oxide transistors processed at temperatures ≤200 °C.

It is worth mentioning that for QSL-I and QSL-III transistors the μ_{SAT} enhancement was accompanied by a threshold voltage (V_T) shift to more negative gate bias as compared to ZnO and In_2O_3 devices (Table 7.2). This observation indicates the presence of a higher density of free/mobile electrons within the transistor channel [95]. Taking into account the low-dimensional nature of QSL and the non-uniform electric-field distribution across the oxide film stacks, the additional free electrons could well be confined at the critical heterointerfaces [see Figure 7.13(b) and (d)] rather than distributed uniformly across the entire QSL structures. The increase in the off-current in QSL-III transistors [Figure 7.14(b)] supports this

assumption owing to the fact that the formation of parallel channel(s) further away from the gate-dielectric/semiconductor interface will be manifested as an increase in the off-current level. In spite of this, the devices continue to function as field-effect transistors with excellent operating characteristics including high carrier mobility and large current on/off ratios (>10^5). The latter is an essential requirement to prove the electrons are capable of being "free" and "mobile" within the confinement region since the controllability by an external electric field is a key feature of conventional 2DEG systems [243-245]. Moreover, capacitance-voltage measurements on different oxide structures provide additional evidence on the charge confinement effects, and the details for this part will be discussed in Section 7.5.2.

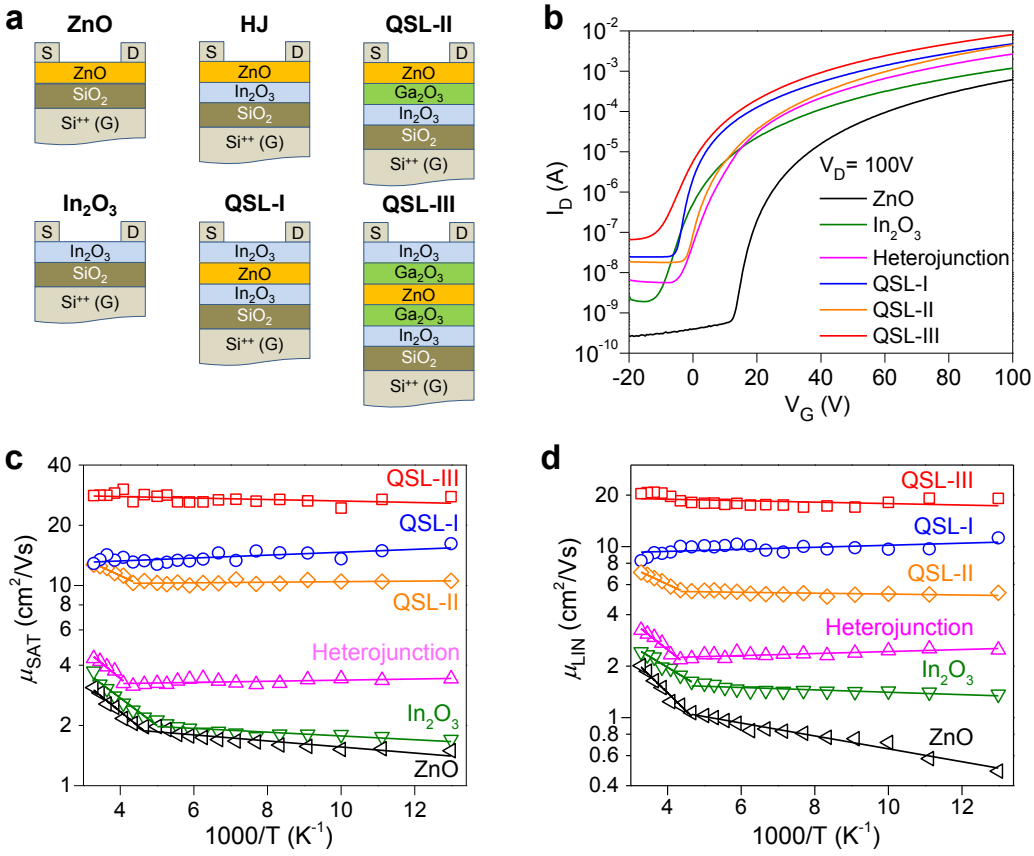


Figure 7.14: (a) Schematics of the heterojunction (HJ) and QSLs based metal oxide transistors developed using Si^{++} and SiO_2 (400 nm) as the gate and the gate dielectric, respectively. (b) Corresponding transfer characteristics measured from transistors in (a). Arrhenius plots of the temperature dependence of field-effect mobility in (c) saturation regime (μ_{SAT}) and (d) linear regime (μ_{LIN}) for ZnO, In_2O_3, In_2O_3/ZnO heterojunction, QSL-I, QSL-II and QSL-III based transistors measured at V_G = 80 V, V_D = 100 V and 15 V, respectively.

Table 7.2: Summary of threshold voltage (V_T), turn-on voltage (V_{ON}) and surface charge trap density (N_{tr}) calculated for the different types of transistors studied [95].

Device channel	V_T (V)		V_{ON} (V)		N_{tr} (cm^{-2})	
	293K	77K	293K	77K	293K	77K
In_2O_3	5.7	45.6	-13.0	18.9	1.01×10^{12}	1.19×10^{12}
ZnO	27.8	18.1	12.0	-4.0	8.48×10^{11}	1.43×10^{12}
Heterojunction	9.0	10.9	-6.0	-5.1	8.09×10^{11}	8.62×10^{11}
QSL-I	-0.6	4.8	-7.8	-6.5	3.87×10^{11}	6.09×10^{11}
QSL-II	5.8	10.0	-3.5	-2.0	4.98×10^{11}	6.47×10^{11}
QSL-III	-8.3	5.8	-15.1	-4.2	3.63×10^{11}	5.28×10^{11}

To study the origin of the enhanced electron mobility in QSLs transistors, temperature-dependent charge transport measurements were carried out for each oxide-based transistor shown in Figure 7.14(a). From Figure 7.14(c) and (d), it is clear that for ZnO and In_2O_3 devices both the μ_{SAT} and μ_{LIN} decrease with reducing temperature down to 77 K. In order to analyse activation energy (E_A) more accurate Arrhenius plots for each transistor were re-plotted by extracting of field-effect mobility at the same (V_G-V_T), which provides the same amount of field effect for each channel composition at different temperatures. In Figure 7.15(a), ZnO transistors showed consistently higher E_A with values in the range 28–37 meV as compared to In_2O_3 devices for which E_A is found to vary between 14–27 meV [Figure 7.15(a)–(b) and Table 7.3]. To be noted that in Figure 7.15 V_{ch} is defined as the difference in voltage between V_G and V_T, i.e. V_G-V_T.

Transistors based on In_2O_3/ZnO heterojunctions show similar thermally-activated transport behaviours but with a higher electron mobility value at temperatures in the range 77–250 K [Figure 7.14(c)–(d) and 7.15(c)]. This finding provides direct evidence that the field effect can penetrate deep into the bilayer oxide film stacks because of their ultra-thin nature, regardless of their high-κ properties. As discussed earlier, owing to the large difference between the Fermi energies the use of such a bilayer system could provide effective charge transfer from the ZnO layer into the low-dimensionally confined In_2O_3 layer. The Fermi level of the latter becomes shallower and hence can easily access high-mobility states. As such, the performance enhancement could be attributed to parallel electron conduction in close proximity to the In_2O_3/ZnO interface. On the contrary, electron transport in QSLs-based devices appear to remain significantly enhanced across the entire temperature range

investigated (77–300 K) with QSL-I and QSL-III transistors exhibiting a characteristic band-like temperature-independent electron mobility trend [Figure 7.14(c)–(d) and Figure 7.15(d) and (f)]. This unusual behaviour could well be that the double heterojunctions provide additional charge confinement within the other charge confinement layers as seen in Figure 7.13(b) and (d). Therefore, more free electrons could have access to the states close to the mobility edge, leading to the band-like behaviour. On the other hand, QSL-II devices are also found to exhibit consistently improved performance when compared to In_2O_3/ZnO heterojunction transistors [Figure 7.14(c)–(d) and Figure 7.15(e)]. The reason can be attributed to the improved structural and electronic quality of the critical oxide heterointerface due to the presence of the Ga_2O_3 interlayer.

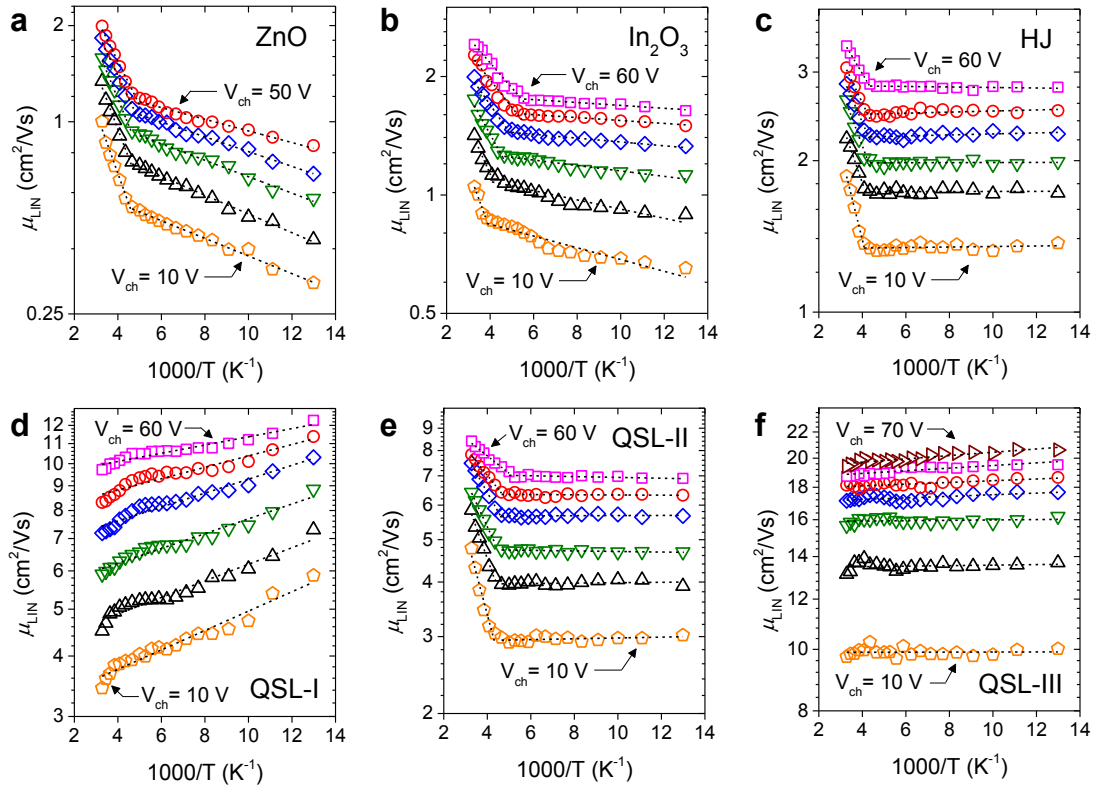


Figure 7.15: Arrhenius plots of the linear field-effect mobility (μ_{LIN}) calculated at different voltages V_{ch}, i.e. (V_G-V_T), for (a) ZnO, (b) In_2O_3, (c) In_2O_3/ZnO heterojunction (HJ), (d) QSL-I, (e) QSL-II and (f) QSL-III based transistor. The V_{ch} starts at 10 V with an increase of 10 V in every step, up to 50 V, 70 V and 60 V for ZnO, QSL-III and the others, respectively.

Taking a closer look, small but negative E_A values are calculated for the μ_{LIN} in QSL-I and under certain biasing conditions for QSL-III devices as well (Table 7.3).

This temperature-independent electron behaviour is unique to devices based on QSL-I and QSL-III. On the other hand, transistors based on any other layer configurations, including QSL-II, do not exhibit such interesting phenomena. These findings support the idea that the nature of electron conduction in QSLs-based devices is radically different from that in single metal-oxide based transistors. The difference is believed to originate from the presence of free electrons confined in the vicinity of the low-dimensional ZnO/In_2O_3 and $In_2O_3/Ga_2O_3/ZnO$ interface(s) that act as parallel channels to the conventional bottom SiO_2/In_2O_3 transistor channel.

One might also argue that the enhancement could be the result of the formation of additional "conventional" parallel channels. However, the latter cannot be solely responsible for the enhanced electron transport observed in QSL-III transistors since such assumption will imply the somewhat unrealistic co-existence of 5–10 parallel channels in order to account for the dramatically enhanced electron mobility measured — a fivefold to tenfold increase. In addition, co-existence of several parallel conventional channels is not likely to alter the temperature dependence of the electron transport which should remain temperature-activated and similar to that of single oxide transistors. Moreover, even if such multiple channels were to exist it would be difficult to manipulate the 5–10 parallel channels with the gate field owing to significant attenuation in electric field. Therefore, based on the discussion and experimental findings we argue that the nature of electron transport in QSLs-based transistors could well be fundamentally different from the transport processes in conventional single oxide channel devices.

Table 7.3: Summary of the activation energies (E_A) calculated at different gate voltages (V_G-V_T) for the different types of oxide transistors studied. To be noted that the E_A for the ZnO, In_2O_3, heterojunction, and QSL-II devices was calculated from the high temperature regime (T > 250 K).

		Thermal activation energy / E_A (meV)					
		In_2O_3	ZnO	Heterojunction	QSL-I	QSL-II	QSL-III
V_G-V_T (V)	10	26.8	37.9	34.6	-4.0	37.2	0
	20	22.2	35.8	24.9	-3.4	28.0	-0.1
	30	21.1	33.1	23.2	-3.0	21.2	-0.1
	40	18.8	28.7	19.8	-2.9	17.6	-0.2
	50	15.1	27.3	18.1	-2.3	12.5	-0.3
	60	13.5	-	14.5	-1.7	7.9	-0.4
	70	-	-	-	-	-	-0.5

To better understand the charge transport characteristics of the different oxide layers, the interplay between two key conduction mechanisms, namely trap-limited conduction (TLC) and percolation conduction (PC) as seen in Chapter 5, have been analysed for ZnO, In_2O_3, QSL-I and QSL-III based transistors. Using Equation 5.4, analysis of the gate-field dependence of μ_{LIN} shown in Figure 7.14(d) reveals that electron transport in single metal-oxide based transistors is dominated by a characteristic TLC mechanism whilst transport in QSL-I/III transistors is dominated by PC (see Figure 7.16). This difference is mainly attributed to the different electronic properties of the active channels as well as the Fermi energies. More specifically, in metal oxides the high-mobility states may become more accessible in systems where E_F is closer to the mobility edge [54, 55]. Since the E_F in QSLs is higher than that of In_2O_3 (Figure 7.13), i.e. the layer in which electron transport is believed to take place, access to those highly delocalised states becomes easier. The latter can directly lead to higher electron mobility. These findings further support the idea that electron conduction within the QSLs-based devices is significantly different from that in ZnO and In_2O_3 based devices, and the conduction mechanism in QSLs is likely determined by the nature of the low-dimensional oxide heterointerface(s).

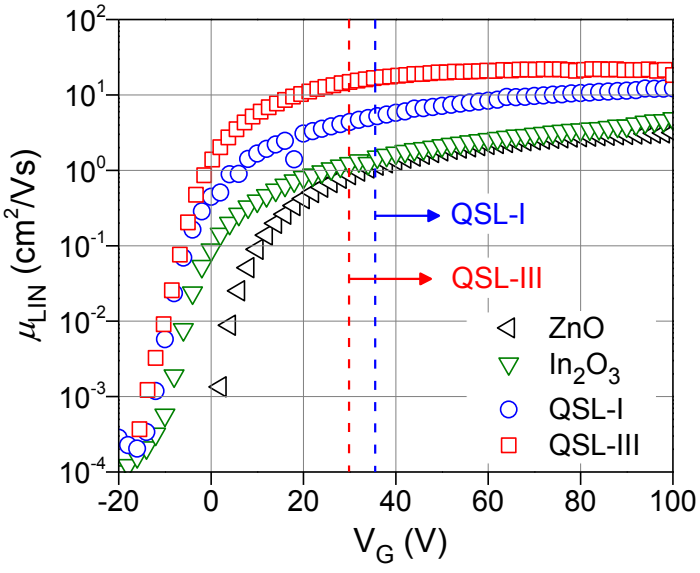


Figure 7.16: Electron transport in single oxide transistors is dominated by the TLC mechanism with γ values ~0.95 and ~0.86 for ZnO and In_2O_3, respectively. In contrast, QSL-I and QSL-III transistors show similar characteristics with a clear PC behaviour. The only apparent difference was a lower percolation voltage extracted for the QSL-III transistor.

For those devices that do not exhibit percolation conduction behaviour (e.g. ZnO, In_2O_3, heterojunction, and QSL-II based transistors), the percolation voltage (V_P) can be derived by plotting E_A as a function of (V_G−V_T), i.e. V_{ch}, and then linearly extrapolating to the intersection at $E_A = 0$ eV [246]. The extracted V_P values for ZnO, In_2O_3, heterojunction and QSL-II devices are 145 V, 110 V, 98 V and 72 V, respectively (see Figure 7.17). A clear improvement in charge transport (i.e. a lower V_P value) can be observed for heterojunction and QSL-II based transistors as compared to single oxide devices. These results provide further direct evidence on the beneficial role that the low-dimensional oxide heterointerfaces play on the overall transistor operation and performance.

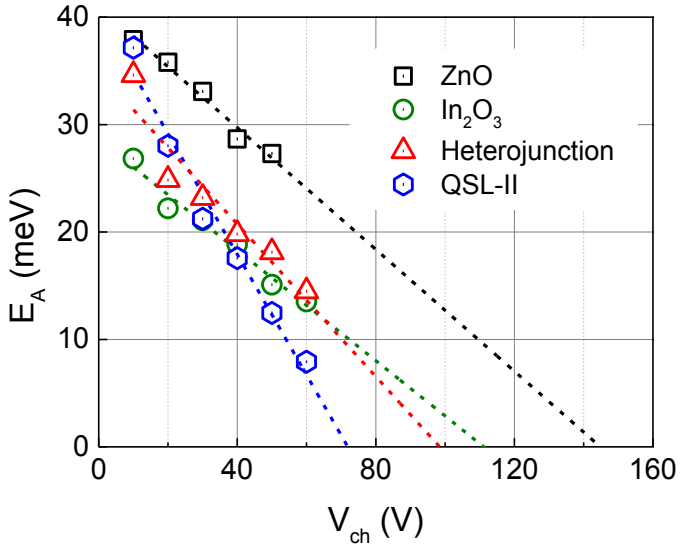


Figure 7.17: Percolation voltage (V_P) for ZnO, In_2O_3, heterojunction, and QSL-II based transistors derived by plotting E_A as a function of (V_G−V_T) and then using linear extrapolation to the intersection at $E_A = 0$ eV [246]. The V_P values for ZnO, In_2O_3, heterojunction and QSL-II devices are obtained of 145 V, 110 V, 98 V and 72 V, respectively.

7.5.2 Carrier depth profiling via capacitance-voltage measurement

In an effort to verify the existence of confined electrons within the oxide QSL structures, the capacitance-voltage (C-V) profiling technique was used to determine the concentration and depth-profile of electrons within the different oxide channels [187, 247-249]. In the present study, C-V measurements were carried out using the metal-insulator-semiconductor (MIS) device structure as schematically shown in

Figure 7.18(a). The hybrid AlO_X/ZrO_2 dielectric (see Section 5.5 for the details) was chosen since QSL-based transistors made with this system were found to yield optimum performance whilst the hybrid dielectric thickness is comparable to that of the semiconducting channels. For the latter, the transistor characterisations will be presented in Section 7.6. Using the parallel-plate model for geometric capacitance, the C-V technique enables the determination of the apparent free carrier concentration ($N_{C\text{-}V}$, see Equation 3.1), as well as the presence and location of the confined electrons within the heterostructure (see Equation 3.2). [187, 247-249]. Figure 7.18(b) displays the measured C-V characteristics at 77 K for MIS devices based on ZnO, In_2O_3, QSL-I and QSL-III. For ZnO and In_2O_3 devices, typical C-V behaviours are obtained with the clear accumulation ($V_G \geq 2$ V) and depletion regimes ($V_G \leq 0.5$ V). On the contrary, QSL-I and QSL-III devices exhibit the dramatic shift of the C-V curves to more negative V_G and the appearance of differently shaped depletion regimes.

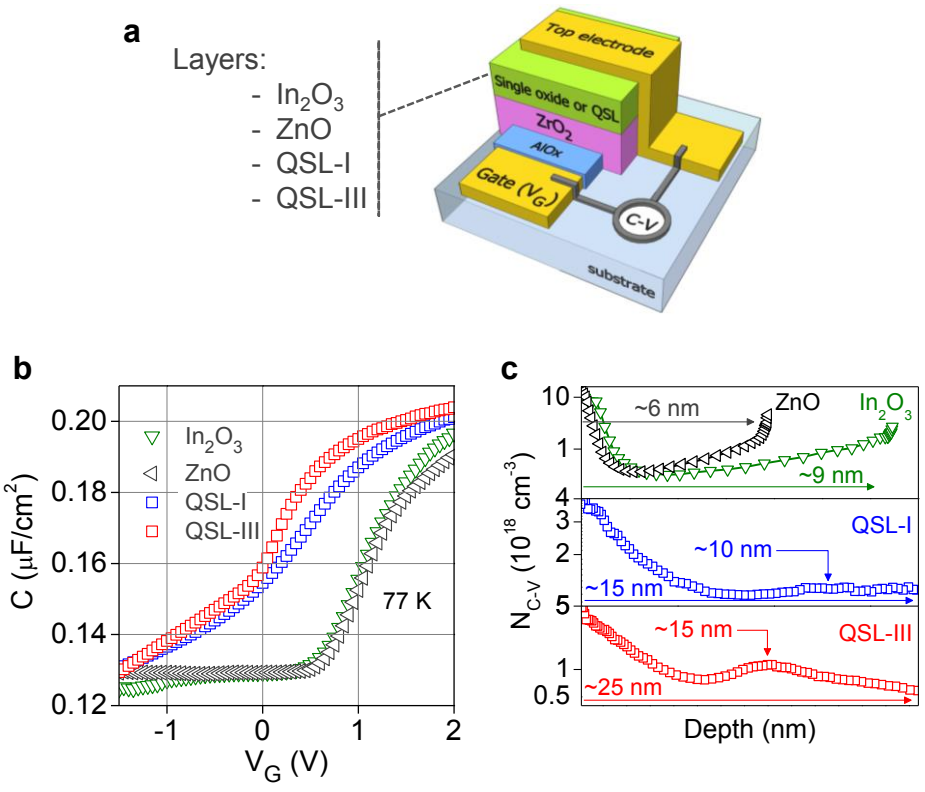


Figure 7.18: (a) Schematic of the MIS structures used for the C-V profile analysis. (b) Capacitance-voltage (C-V) measurements obtained at 77 K for ZnO, In_2O_3, QSL-I and QSL-III based MIS devices. (c) Apparent free electron ($N_{C\text{-}V}$) profiles as a function of depth for MIS devices based on the different semiconducting layers calculated from the C-V data in (b).

Figure 7.18(c) presents the N_{C-V} profiles as a function of depth, i.e. the distance from the top electrode [see Figure 7.18(a)]. In ZnO and In_2O_3 based devices N_{C-V} remains relatively low and uniform across the semiconductor layer, whilst the apparent electron density within QSL-I and QSL-III appears consistently higher and non-uniform within the structures. For QSL-I devices N_{C-V} exhibits a maximum at a depth of ~10 nm from the top electrode. This observation suggests the presence of confined electrons owing to their non-uniform distribution. For QSL-III based devices, a clear maximum in N_{C-V} indicates better electron confinement, which appears at a slightly increased depth of ~15 nm. The calculated depths for where the confinement effects take place in both QSLs coincide with the expected position of the critical heterointerfaces as depicted in Figure 7.13(b) and (d). For the latter one might argue that the presence of one N_{C-V} maximum for QSL-I/III devices mismatches the number of confinement peaks expected for such double heterointerfaces i.e. two. This discrepancy can be attributed to the rough nature (non-uniform thickness) of the central ZnO layer [Figure 7.3(a)], which makes resolving the two closely spaced (~5 nm) electron confinement layers extremely challenging. Besides, the complexity of QSLs is approaching the resolution limit of C-V profiling technique so that the N_{C-V} peak appears broader than expected. Nevertheless, it is still evident that a significant concentration of free electrons appears to be confined at the critical oxide heterointerfaces in accordance with the energy diagrams of Figure 7.13(b) and (d).

7.6 Flexible quasi-superlattice based transistors

The ability to grow ultra-thin layers of oxide dielectrics (see Section 5.5) and semiconducting QSLs at low temperatures could lead to development of transistors with state-of-the-art electron mobilities and low voltage operation on arbitrary substrate materials. In order to demonstrate the potential of the proposed oxide QSL-based technology, BG-TC transistors were fabricated on glass and plastic substrates employing the hybrid high-κ AlO_X/ZrO_2 gate dielectric discussed in Section 5.5. It should be noted that the staggered device geometry was similar to that used for

transistors made on Si/SiO_2 with the only exceptions being the gate electrode and gate dielectric materials employed. Therefore, one could expect both SiO_2 and high-κ based transistors possess similar physical and electrical properties. Thanks to the thin (~25 nm) and high-κ (~9) nature of the hybrid AlO_X/ZrO_2 gate dielectric (C_i ~235 nF/cm^2) [250], the QSL-I/III transistors operate at significantly reduced voltages [Figure 7.19(a)]. QSL-I transistors are found to exhibit consistently high mobility with a mean value ($\mu_{SAT(mean)}$) of ~37 cm^2/Vs whilst exceptional mobility values of $\mu_{SAT(mean)}$ ~40 cm^2/Vs are obtained for QSL-III devices [Figure 7.19(b)]. It should be noted that both mobility values are higher than those obtained for SiO_2-based transistors [Figure 7.14(c)]. The difference between SiO_2 and high-κ based transistors is attributed to improved microstructure of the semiconducting layers due to the epitaxial-like growth on top of the polycrystalline dielectric. Similar effects have been seen and reported by several others [44, 107, 142, 250, 251]. The low-voltage QSL transistors also exhibit respectable on/off drain-current ratios (~10^4) and small mean subthreshold swings (S.S. = $dV_G/d[\log(I_D)]$) of ~275 mV and ~160 mV for QSL-I and QSL-III devices [Figure 7.19(c)], respectively.

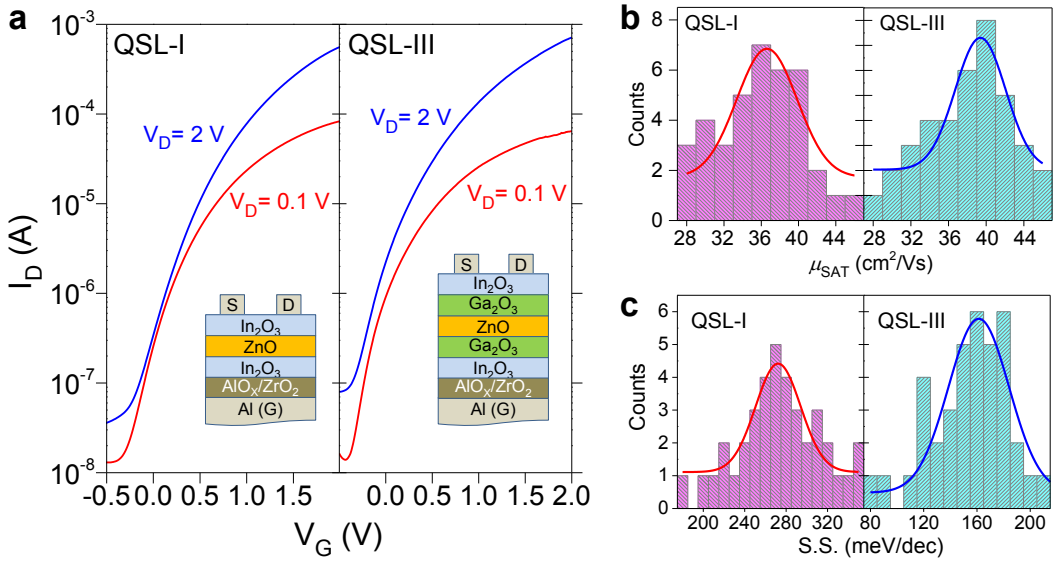


Figure 7.19: (a) Representative sets of transfer characteristics measured from transistors based on QSL-I and QSL-III channels. Histogram plots of (b) saturation mobility (μ_{SAT}) and (c) subthreshold swing (S.S.) calculated for a number of low-voltage QSL-I and QSL-III based transistors fabricated simultaneously on the same substrates. The Gaussian fitting curves are guides to the eye.

Using the same approach, low-voltage QSL-based transistors were also demonstrated on flexible polyethylene naphthalate (PEN) substrates [Figure 7.20(a)]. The resulting devices exhibited electrical performance with $\mu_{SAT(mean)}$ of ~8.5 cm^2/Vs and ~11 cm^2/Vs for QSL-I and QSL-III transistors, respectively [Figure 7.20(b)–(d)] whilst the S.S. were obtained of ~170 mV/dec and ~90 mV/dec for QSL-I and QSL-III based devices, respectively [Figure 7.20(e)]. One should notice that the mobility for flexible QSL devices is reduced as compared to that for non-flexible ones [see Figure 7.19(b) and 7.20(d)]. This is attributed to the lower annealing temperature (<175 °C, see Section 5.5) used in order to maintain the mechanical properties of the PEN substrate during the sequential spin cast-annealing steps for growing such complex QSL structures. Moreover, the rougher surface features of plastic foils might affect the quality of each QSL constituent layer. In spite of the reduction in field-effect mobility, the flexible QSL-based transistors still exhibit the highest electrical performance among work on solution-processed metal-oxide transistors reported to date [86, 106, 107].

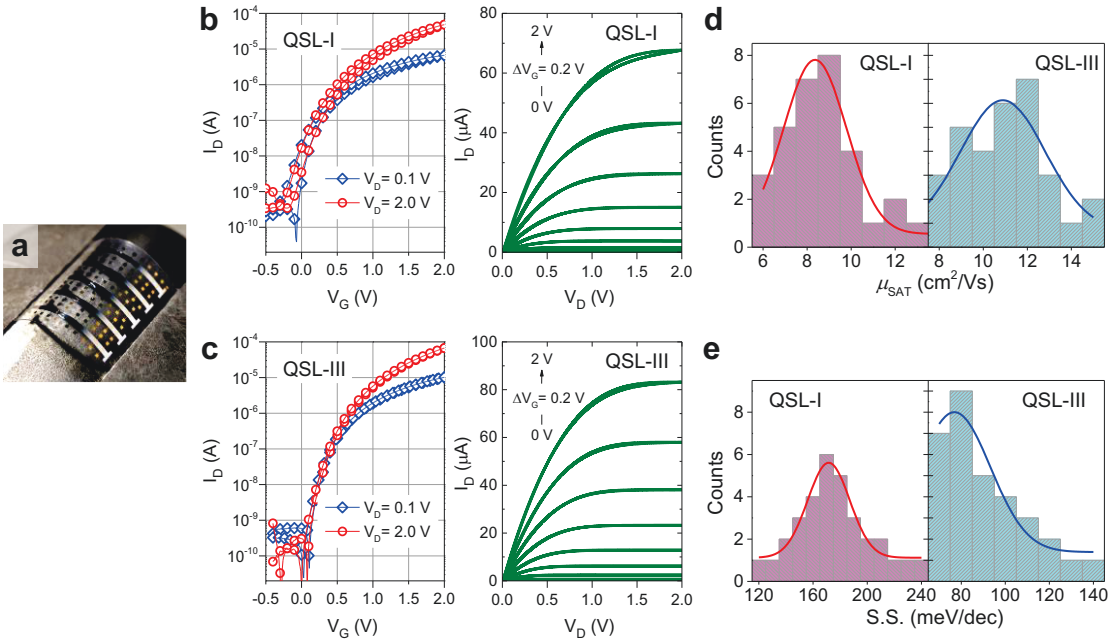


Figure 7.20: Photograph of an actual flexible QSL-based transistors array containing >35 devices fabricated on a plastic (i.e. PEN) substrate. Representative sets of transfer and output characteristics for (b) QSL-I and (c) QSL-III transistors fabricated on a PEN substrate. Histogram plots of (d) saturation mobility (μ_{SAT}) and (e) subthreshold swing (S.S.) calculated for a number of flexible low-voltage QSL-I and QSL-III based transistors fabricated simultaneously on the same substrates. The Gaussian fitting curves are guides to the eye.

In addition, the performance of the low-voltage QSL-based transistors is found to consistently outperform those based on ZnO and In_2O_3 channels, fabricated on either glass (μ_{SAT} ~ 3–5 cm^2/Vs) or PEN (μ_{SAT} ~ 1–3 cm^2/Vs) substrates (see Figure 7.21), respectively. These results clearly demonstrate the advantage of the proposed oxide QSL technology over conventional single oxide channel transistors.

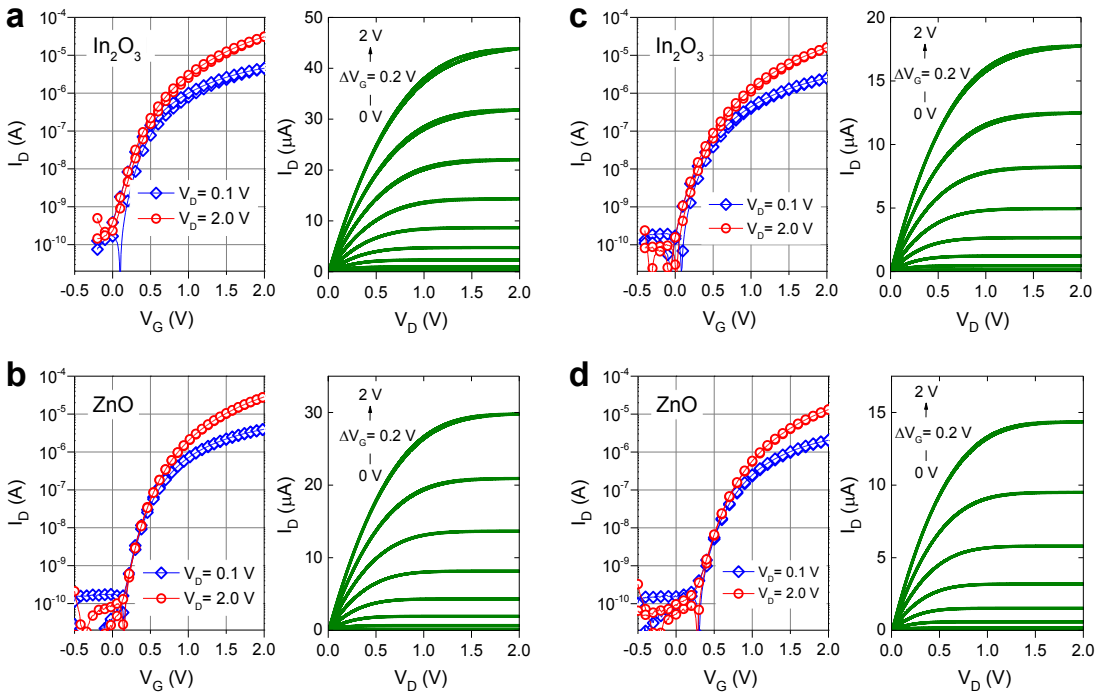


Figure 7.21: (a) Transfer (left) and output (right) characteristics measured for an In_2O_3-based transistor fabricated on a glass substrate. (b) Transfer (left) and output (right) characteristics measured for a ZnO-based transistor fabricated on a glass substrate. (a) Transfer (left) and output (right) characteristics measured for an In_2O_3-based transistor fabricated on a PEN substrate. (b) Transfer (left) and output (right) characteristics measured for a ZnO-based transistor fabricated on a PEN substrate.

7.7 Conclusions

In summary, a new concept of solution-processed metal oxide quasi-superlattice transistors has been demonstrated. In contrast to conventional metal oxide devices, the performance level of the QSL transistors is not limited by the carrier transporting properties of any of the constituent semiconductor(s) in the QSLs. Instead, the electrical characteristics are determined by the physical properties of the oxide heterointerfaces buried within the QSL. In this work, the conceptual QSL devices

have shown dramatically enhanced field-effect mobilities (>40 cm^2/Vs) that greatly surpass the electron mobility values reported for oxide transistors fabricated using solution process at ≤200 °C [41, 42, 252, 253]. Likewise, the discovery of energy quantisation effects in low-dimensional solution-processed oxide layers has helped to develop all solution-processed oxide-based resonant-tunnelling diodes for the first time [126]. Based on these preliminary but yet very promising results, it is believed that the concept of solution processed, low-temperature QSL-based structures could provide a unique path to a generic transistor technology that could potentially fulfil the ever increasing demand for high-performance TFTs for numerous existing as well as fast emerging large-area electronic applications. Furthermore, since the transport properties of the QSL systems are determined primarily by the electronic properties/dimensionality of the constituent materials/layers, oxide QSLs could in principle be fabricated by a range of alternative large-area manufacturing techniques, including spray pyrolysis, ink-jet printing, atomic layer deposition or even sputtering.

8

SUMMARY AND OUTLOOK

In this thesis we proposed several different approaches to address some of the current challenges facing large-area flexible electronics based on low-temperature, solution-processed oxide semiconductors. The primary purpose of Chapter 8 is to summarise the key findings that have been reported in the previous chapters but also discuss the future prospects for research in this field.

8.1 Summary

Beginning with Chapter 4, an ultraviolet (UV) light irradiation step to replace the conventional thermal-annealing process for fabricating nanoparticle-based (NP-based) ZnO thin-film transistors (TFTs) from solution, is introduced. This one-step UV process enabled the fabrication of functional transistors at room temperature. Resulting ZnO TFTs exhibit n-type conductivity with electron mobility on the order of $\sim 10^{-3}$ cm^2/Vs. Experimentation on ZnO NPs under different UV illumination periods has revealed that the activation mechanism is due to NP ligand and/or capping-layer annihilation. This finding clearly highlights that the electrical characteristics of NP-based thin-film layers are highly related to inter-particle electrical connectivity/conductivity. The impact of the semiconductor-dielectric interface has also been studied with the aid of different SiO_2 surface-passivation treatments and transistor geometric configurations. For dielectric surface passivation, the use of OTS molecules, whose long-aliphatic chain can effectively keep the semiconducting channel away from interfacial trapping sites, is found to offer the most significant improvement. In terms of device geometry, strong attenuation of the field effect is seen when using a bottom-gate configuration which is believed to be due to the spherical shape of NPs. On the other hand, transistors based on a top-gate configuration exhibit higher channel currents, larger on/off ratios and smaller operating hysteresis. This enhancement was argued to be due to the full coverage of the ZnO NPs by the solution-processed gate-dielectric. Toward the end of Chapter 4, a concept based on the use of metal oxide nanocomposite was proposed to overcome the inter-particle transport limitations with primary goal of improving the overall

long-range channel conductivity. Using this approach, well performing transistors with electron mobility close to 3 cm^2/Vs were demonstrated.

In Chapter 5, a carbon-free, aqueous-based oxide precursor route is used for the synthesis of ZnO layers at temperatures below 180 °C, and their subsequent use in high mobility TFTs is demonstrated. With careful control on the deposition environment, a "hero" ZnO TFT is shown to exhibit an electron mobility exceeding 10 cm^2/Vs. This was obtained by fabricating the devices entirely under inert-gas atmosphere. AFM studies reveal that the resulting ZnO film morphology has a strong impact on device performance. Likewise, the transistors made in a dry anaerobic condition have generally shown electrical performance two to three times better than those made in atmospheric environment. TEM characterisation confirmed that using this aqueous route for film fabrication lead to the formation of ultra-thin polycrystalline ZnO films. In an effort to reduce the operating voltage of the TFTs and enable their application in low-power electronics, the development of a UV-assisted hybrid high-κ dielectric was demonstrated. This work led to the demonstration of low-voltage ZnO TFTs operating at ~1.2 V. Importantly, the entire fabrication process is compatible with the use of temperature-sensitive substrates. In general, the devices made on glass using this approach exhibited excellent electrical performance with electron mobilities >10 cm^2/Vs. For the devices made on plastic foils, electron mobilities of ~4 cm^2/Vs were achieved. Finally, a UV-irradiation process was also explored to initiate the photochemical conversion of Zn-ammine complex at temperatures below 100 °C. The latter process does not require any thermal-annealing treatment and is able to produce functional ZnO transistors with electron mobility on the order of 1 cm^2/Vs.

The aqueous route for the synthesis of high-quality ZnO layers demonstrated in Chapter 5 has been further explored in Chapter 6 with emphasis on facile n-type doping of ZnO utilising Al as the dopant element with primary aim the enhancement of the electrical performance of ZnO TFTs. In this approach, the Al-doping concentration is controlled in the time domain and differs from conventional doping processes based on changing dopant precursor molar concentrations. Here, the doping mechanism is due to the amphoteric properties of Al and Al hydroxide that result in the release of Al ions into the Zn-ammine complex solution that can subsequently be

used for creating the Zn-amine based precursor solution. The impact of Al incorporation can be monitored by means of optical absorption and X-ray diffraction measurements, whilst AFM measurements reveal a clear evolution in the Al-doped ZnO (ZnO:Al) layers microstructure as a function of doping concentration. When this information is combined with current-voltage measurements from TFTs, the influence of the microstructural properties of the different ZnO:Al films can be seen to have a direct impact on transistor performance. Optimised ZnO:Al TFTs exhibited maximum electron mobilities of >5 cm^2/Vs. Importantly, the doping process can be carried out at ~180 °C and there are no constraints on the deposition environment. Moreover, the deposition temperature can be reduced to ~120 °C, a temperature compatible with highly inexpensive plastic foils. It is established that even at this exceptionally low processing temperature, ZnO:Al TFTs still exhibits a remarkable field-effect mobility value of around 3 cm^2/Vs.

Finally, Chapter 7 introduces a completely new transistor concept based on the use of low-dimensional metal oxide quasi-superlattice (QSL), which consists of alternating layers of In_2O_3, Ga_2O_3 and ZnO deposited by sequential spin casting at low temperatures of <200 °C. The chapter started with the demonstration of energy quantisation effects observed in solution-processed, ultra-thin layers of ZnO and In_2O_3. The largest bandgap increase is found to be over 300 meV for layer thicknesses <5 nm. Utilising several characterisation methods, including TEM, AFM and XRR, the results suggest that the as-processed oxide layers feature highly-smooth surfaces and large-crystalline domains. The principle idea behind this approach is to utilise the energy difference between each constituent metal oxide, along with the low dimensionality of each layer in order to facilitate electron confinement at the vicinity of the heterointerface. Such low-dimensional electron systems were expected to manifest as enhanced electron transport in the transistor channel. Indeed, the prototype QSL transistors are found to exhibit significantly enhanced mobility with an unusual temperature-independent characteristic described here as “band-like” in nature. Importantly, QSL TFTs exhibit maximum electron mobilities an order of magnitude greater than devices based on single layer binary oxides. Charge profiling utilising capacitance-voltage measurements suggests that within the QSL structures there exists a non-uniform charge distribution in agreement with the energy band

diagram in the presence of sharp interfaces. This finding is similar to characteristics observed in conventional two-dimensional electron gas systems. Therefore, the observations of temperature-independent electron transport together with this non-uniform charge profile indicate that the strongly enhanced transistor performance likely originates from the formation of a low-dimensional electron gas in close proximity to the critical heterointerface(s) buried within the QSL. Finally, by exploring the same approach for the growth of the hybrid high-κ dielectrics discussed in Chapter 5, QSL-based TFTs with low operating voltage characteristics were demonstrated on both glass and flexible plastic foils. The resulting TFTs exhibited electron mobilities of >40 cm^2/Vs for devices made on glass, and >10 cm^2/Vs for devices made on plastic foils.

8.2 Outlook

It is hoped that the results presented in this thesis may help to resolve the current technology bottleneck that exists in the field of low-temperature solution-processed oxide transistors. This work has helped to determine new approaches that can help us create oxide transistors with high enough electrical performance to meet current industrial requirements as well as enable key future developments. Specifically, transistors based on the nanocomposite approach, Zn-ammine complex or aqueous In nitrate precursor exhibit electron mobilites in the range of 1–10 cm^2/Vs, and the entire fabrication process can be used for devices made on temperature-sensitive substrates. Clearly, the effectiveness of the UV illumination methods on oxide conversion are quite pronounced, and could be further explored as a new paradigm for low-temperature manufacturing. Likewise, the flexibility of solution processing always offers higher convenience for synthesising functional oxide materials, which extend the possible applications of metal oxide-based transistors. Whilst in this thesis the only “functional” ZnO (i.e. ZnO:Al) transistors showing electrical performance improvement utilised Al as a dopant, the simplicity and universality of this method could easily be used with other potential dopants.

The most important development in this thesis is the demonstration of the oxide superlattice concept proposed in Chapter 7. Rather than relying on the intrinsic material properties, the QSL concept offers a way to access staggering charge-transport properties that significantly outperform the electrical performance of the constituent materials. The formation of such a low-dimensional oxide layer using solution processing can lead to an energy quantisation, which not only is thought provoking for the research community, but also advances the development of novel electronic devices for large-area applications. The demonstration of the superlattice transistors on plastic foils has proven this is a robust system that can address the needs of low-cost large-area electronics. In principle, the technology can be adapted for many potential applications that require high electrical performance, which cannot be currently met by incumbent technologies. Moreover, the proposed QSL concept should not be limited to specific material combinations or fabrication techniques and should be applicable to a range of other oxide material systems and fabrication methods (sputtering, atomic layer deposition, spray pyrolysis, roll-to-roll, etc.). One may also argue that hybrid superlattices composed of ultra-thin (low dimensional) layers of metal oxides and self-assembled organic molecules could one day also be developed. Depending on the exact choice of materials, such hybrid superlattice systems would exhibit not only tailored electronic transport properties but also optical and potentially thermo-electrical properties.

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Chapter 6: Y.-H. Lin, S. R. Thomas, H. Faber, R. Li, P. A. Patsalas, T. D. Anthopoulos, "Crystallographic Engineering of ZnO:Al towards Low-Temperature High-Performance Solution-Processed Thin Film Transistors". Submitted.

Chapter 7: J. G. Labram, Y.-H. Lin, K. Zhao, R. Li, S. R. Thomas, J. Semple, M. Androulidaki, L. Sygellou, M. McLachlan, E. Stratakis, A. Amassian, T. D. Anthopoulos, "Signatures of Quantized Energy States in Solution-Processed Ultrathin Layers of Metal-Oxide Semiconductors and Their Devices", *Advanced Functional Materials* **25**, 1727-1736 (2015). DOI: 10.1002/adfm.201403862

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