ELECTRON TRAPS IN THIN-FILM TRANSISTORS

by

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ABSTRACT

This study concerns the investigation of the properties of electron traps in thin-film transistors (TFT), by analysing thermally stimulated current (TSC) phenomena associated with these traps.

Simmons' TSC technique is used to identify and examine the traps. For the semiconductor - insulator interface traps, for instance, the method consists of biasing the TFT into the accumulation mode to fill the traps. A negative gate voltage is then applied at low temperature to drive the interface into the non-steady-state condition. Subsequent heating, at a uniform rate, results in the release of electrons from the traps. These electrons give the TSC. The TSC curve is recorded and yields information about the traps.

A trap level in the semiconductor bulk; the insulator - semiconductor interface traps and the grain boundary traps are identified and analysed. The application of a negative gate voltage results in an aging process which affects the properties of these traps. The explanation of how the magnitude of the density of the first bulk trap, leads to the prediction of the existence of another, is given. It is shown that slow as well as fast states exist at the semiconductor - insulator interface and that these exhibit Anderson splitting. Aging may result in a high enough density of grain boundary traps to pin the Fermi level of the thin film system at the grain boundary, and give TSC peaks

with current maxima at temperatures independent of the heating rate. Such peaks are analysed using the quasi-equilibrium TSC theory. The existence of a TSC peak corresponding to traps at the semiconductor - source interface is predicted and then verified experimentally. Electron microscopy shows that annealing the TFT results in the polycrystalline semiconductor film minimising its stored energy. Furthermore, it enables the active volume of the grain boundary to be determined.

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CHAPTER I. INTRODUCTION

The thin-film transistor (TFT) is a field effect device made entirely of sputtered or evaporated thin films. Hence it has an important part to play in thin-film circuits. The fundamental phenomena associated with the TFT are not well understood. This is because of a lack of knowledge of the properties of defects present in the TFT which have an important part to play in governing these phenomena.

Atomic defects give rise to electron traps. The traps present in the TFT are shown in Fig. 1. The device consists essentially of a polycrystalline film of CdSe, onto which chromium electrodes have been evaporated. The CdSe is the semiconductor and is insulated from an aluminium electrode by a film of SiO_2. Excess cadmium atoms within individual CdSe crystallites act as donors - these are referred to as the bulk traps. Lattice mismatch between the CdSe and SiO_2 gives rise to the interface traps. These are subdivided into the fast and slow traps, the former being located at the interface and the latter inside the SiO_2 close to the interface. Lattice mismatch between CdSe crystallites gives rise to the grain boundary traps. Traps also exist at the CdSe-Cr interface.

The importance of these traps becomes clear when it is realised that for the TFT to function as a transistor, a conducting channel of mobile carriers must exist at the semiconductor side of the CdSe-SiO_2 interface. The carriers are provided by the donors within the CdSe crystallites. Too high a density of traps at the CdSe-SiO_2 interface, or at grain boundaries, may capture and hence immobilise some of this charge and hence interfere with proper transistor action. Whereas

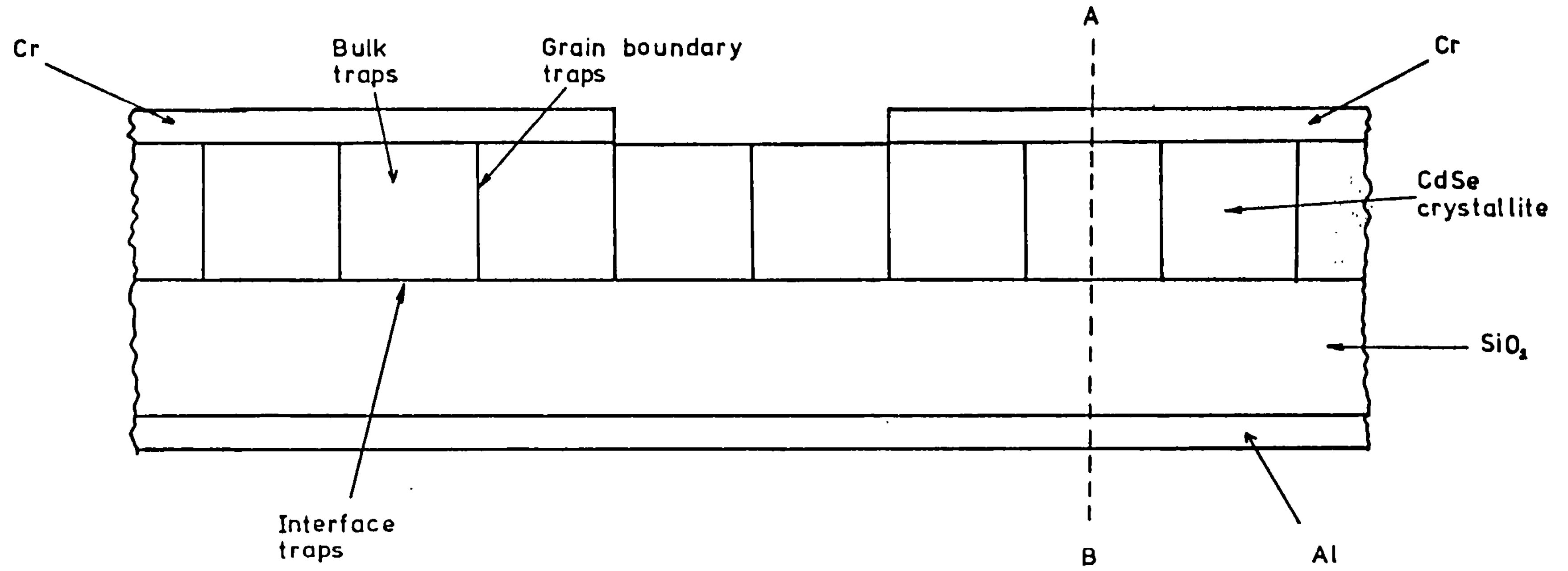


Fig.1

The traps in the TFT

fast interface traps capture electrons in less than a millisecond, slow ones go on capturing for longer, thus causing long term instabilities in the current that flows between the chromium electrodes. Furthermore, for proper transistor characteristics, the chromium electrode must make an ohmic contact with the semiconductor. The choice of the relative magnitudes of the work functions of the two materials ensures, under favourable TFT preparation conditions, for the contact to be ohmic. At other times, however, the traps at the CdSe-Cr interface determine the nature of the contact and give a blocking contact which affects the transistor characteristics adversely.

In the present investigation the electron traps in the TFT are examined using Simmons' thermally stimulated current (TSC) technique. TSC characteristics are current against temperature plots which exhibit peaks. From a current peak information can be derived about the corresponding trap. The existence of the multiplicity of traps in the TFT, however, means that all the peaks must be identified first before an attempt can be made at analysing individual traps. The existence of six different groups of traps makes the identification problem one of considerable complexity. The aim of the project is therefore to try to identify the traps and then to examine the properties of as many of the individual traps as time permits. The reason for the choice of Simmons' TSC technique lies in the efficacy of this diagnostic technique as a tool for both identifying and examining traps.

A critical review of the properties of the materials used in the TFT is presented in Chapter II. It is well known that SiO_2 reduces the density of "dangling" bonds on the "free" surface of Si. The relevant properties of the SiO_2 prepared in the present work are discussed in order to see what effect the insulator can have on the SiO_2 - CdSe interface of the TFT. The semiconductor is n-type CdSe. The literature on the structure of CdSe is examined in this chapter in order to determine

the nature of the point defects giving the donors within the bulk of CdSe cystallites. The reason for this investigation lies in the fact that films prepared by evaporation have stored energy which they subsequently tend to minimise. The energy may be stored in the form of point defects and minimisation of this energy is realised by the diminution of the density of defects by their diffusion out of the bulk of the crystallites, under the action of a high electric field or at elevated temperatures. In the case of the polycrystalline films used in the present work, the diffusing atoms eventually end up at grain boundaries and at the interfaces. The end result is that the distribution of bulk, grain boundary and interface traps may change as a result of this movement of atoms and hence, a knowledge of the origin and diffusion properties of the point defects causing this change is necessary in the identification of traps. A survey of the energies of traps obtained in previous investigations on single crystal CdSe is also included in this chapter. This helps the identification and separation of the peak due to bulk traps from other peaks, in the more complex TSC curves of the polycrystalline film used in the present work. The TSC results of previous investigations on polycrystalline CdSe is also included. These show that no attempt was made to determine the topography of the different groups of traps which exist in such films - grain boundary traps for instance have never been mentioned in the works reviewed. This inadequacy of the earlier investigations led to one of the aims of the present work i.e. that of identifying grain boundary traps.

Simmons was the first to stress the importance of trap topography and to identify the topography of traps in MOS devices. His work, however,

was on single-crystal - semiconductor devices where no grain boundary traps exist. One of the reasons for examining the TFT in the present work is because, in this device, Simmons' techniques can be extended to a more complex system, since the semiconductor, being polycrystalline in the TFT, includes grain boundary traps. The TSC technique is treated in Chapter III. Simmons' theory of the TSC is presented because it clarifies the basic concepts involved in the TSC method and can be used as the basis for the analysis of traps of varying topography.

The processes of emission and generation TSCs from fast interface traps are explained qualitatively. The concepts of traps under equilibrium steady-state, nonequilibrium steady-state and nonequilibrium non-steady-state conditions are gone into in Appendix D. These concepts are vital for a proper understanding and interpretation of TSC data. The use of the occupancy function for traps in the nonequilibrium non-steady-state condition as the starting point for the quantitative analysis of the emission and generation processes is then explained. The introduction of Appendix D conserves continuity between the qualitative and quantitative sections of the analysis of the emission and generation processes. A brief analysis of Simmons' theory of the TSC from bulk traps follows.

A knowledge of the energy band diagram of the TFT is necessary for a proper understanding and interpretation of TSC data. Hence, the one-dimensional energy diagram for the Al-SiO_2-CdSe-Cr system is developed in Chapter III. It is noted that variations in the nature of the CdSe-Cr contact may give TFTs with "good" or "bad" transistor characteristics and the corresponding energy band diagrams for "good" and "bad" TFTs is presented. To clarify the topography of grain boundary

traps in relation to that of other traps, a two-dimensional energy diagram is developed.

The novel behaviour of some of the TSC peaks obtained in the present work necessitated the development of new methods for analysing such peaks. The first of these peaks is the quasi-equilibrium TSC one and formulae developed by Anderson for analysing it are presented. The second is the TSC peak from interface traps containing slow as well as fast states. Anderson has extended Simmons' TSC theory for devices containing fast interface states alone, to those with fast and slow ones. The predictions of Anderson's analysis are very useful in identifying interface traps and are included in this chapter

Chapter IV describes the apparatus and method used to prepare TFTs. The method of testing TFTs is followed by the details of the construction and use of the cryostat built for making TSC measurements. This is followed by a description of the electrical circuit with special reference to the electrometer.

In Chapter V the results of transmission electron microscopy and transmission electron diffraction experiments on thin films of CdSe are presented and analysed. This is followed by the presentation and analysis of the TSC results of the TFT.

Chapter VI contains the summary of the present findings and proposals for further work.

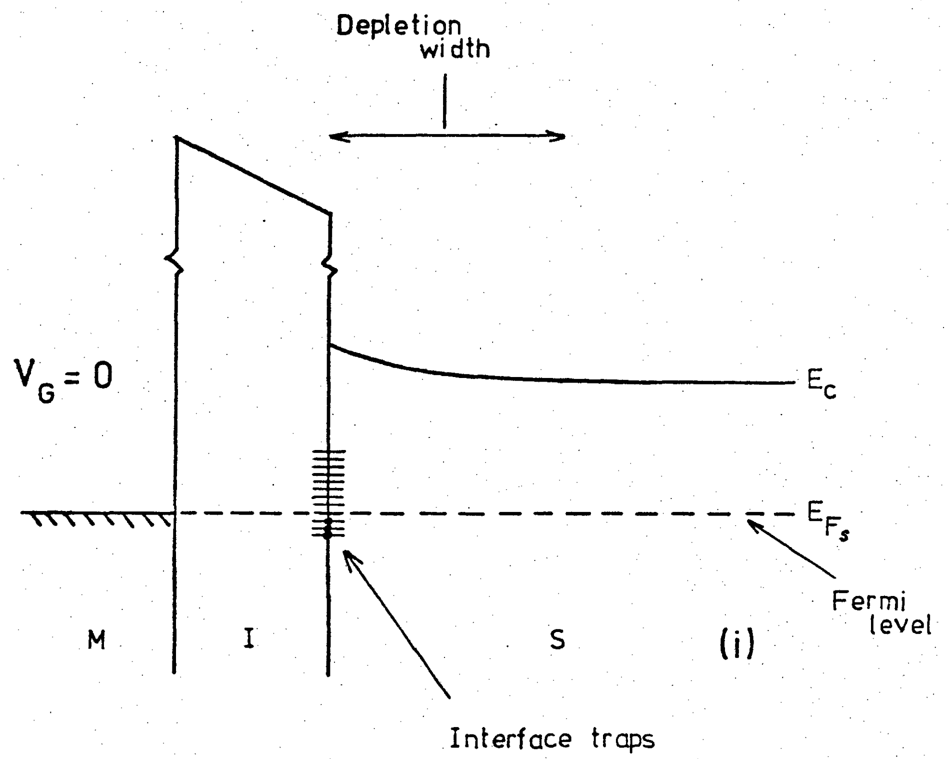
CHAPTER II. PROPERTIES OF TFT MATERIALS

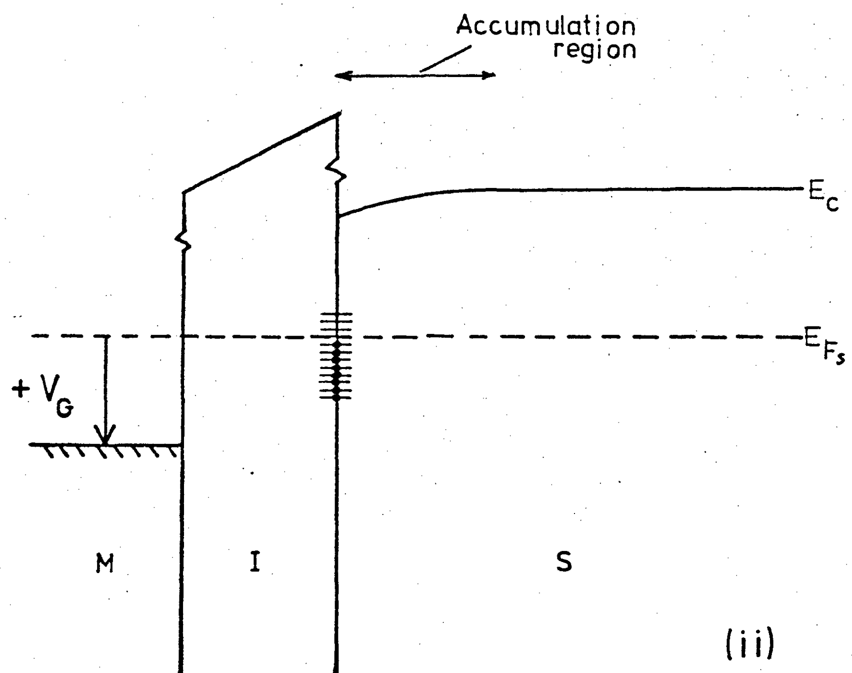
2.1. The Insulator - Semiconductor Interface - The Interface Traps

Fig. 2 shows the energy diagrams along AB of Fig. 1. In Fig. 2(i) the gate is short circuited to the drain. The interface states are acceptor - like traps i.e. neutral when empty and thus negatively charged when filled. In thermal equilibrium, the semiconductor at the interface is depleted of free electrons because these are trapped by the interface traps. In Fig. 2(ii) a positive voltage is applied to the gate with respect to the drain. The transfer of charge is best explained using the capacitance analogy. The gate is one plate with a net positive charge. The SiO_2 is the dielectric. The semiconductor near the interface acts as the second plate with a net negative charge of mobile electrons in the accumulation region to balance the net gate charge. These mobile electrons can take part in conduction when the device is operating as a TFT. In some TFTs the density of interface traps can be high enough, with respect to the bulk traps, to trap most of this charge giving a device with too low a density of mobile carriers which is undesirable. It is important, therefore, to know the parameters which affect the properties of interface traps, in particular their energy and density. Hence the properties of SiO_2 and CdSe relevant to the interface parameters of interest are treated in sections 2.1.1. to 2.1.6.

2.1.1. The Insulator

One of the parameters affecting the density of interface traps is the choice of insulator material. In the device used in the present work the insulator was sputtered SiO_2. To appreciate the reason for this choice the atomic structure of SiO_2 must be considered because this is related to the electronic properties of the interface.





Full trap
Empty trap

M=Metal (gate)
I = Insulator
S = Semiconductor

Fig. 2
TFT (i) in depletion (ii) in accumulation

2.1.2 The Atomic Structure of SiO_2

There are thirteen known forms of silica of which all but one (stishovite) consist of arrays of SiO_4 tetrahedra linked together by shared oxygen atoms at each vertex with silicon at the centre (1) as shown in Fig. 3. The bond lengths and bond angles differ slightly in the different lattice arrangements, but the local geometry of the tetrahedral units and their coupling remain the same in the absence of defects. The Si-O bond length varies from 1.52 to 1.69 Å with a mean of 1.612 Å.

2.1.3 The Si-O-Si Bond Angle

Bell and Dean (2) have built an actual physical model of vitreous silica to indicate the purely structural details of plausible atomic arrangements. The models are idealised in the sense that they contain no defects except at the surface. The basic structural units - the tetrahedral units of Fig. 3 - were linked together to form a continuous irregular three-dimensional network. Randomness was achieved by varying the relative orientation of adjacent tetrahedra throughout the structure, both by allowing the Si-O-Si angle to take any one of a range of values and by using the rotational freedom of adjacent tetrahedra about the connecting silicon - oxygen bonds. The Si-O-Si angle was found to vary from 120° to 160° with a mean of approximately 140°. (There is good agreement between this and the Si-O-Si bond angle for vitreous SiO_2 quoted by Revesz and Zaininger (3)). The O-Si-O angle, on the other hand, did not differ appreciably from the ideal tetrahedral angle of $\sin^{-1}\sqrt{\frac{8}{9}} \simeq 109.5^\circ$. The silicon - oxygen bond lengths also vary throughout the model but to a relatively smaller extent than the variation in the Si-O-Si angle. A Si-O bond length of 1.60 Å was used in the model which agrees well with the value of 1.612 Å of reference (1).

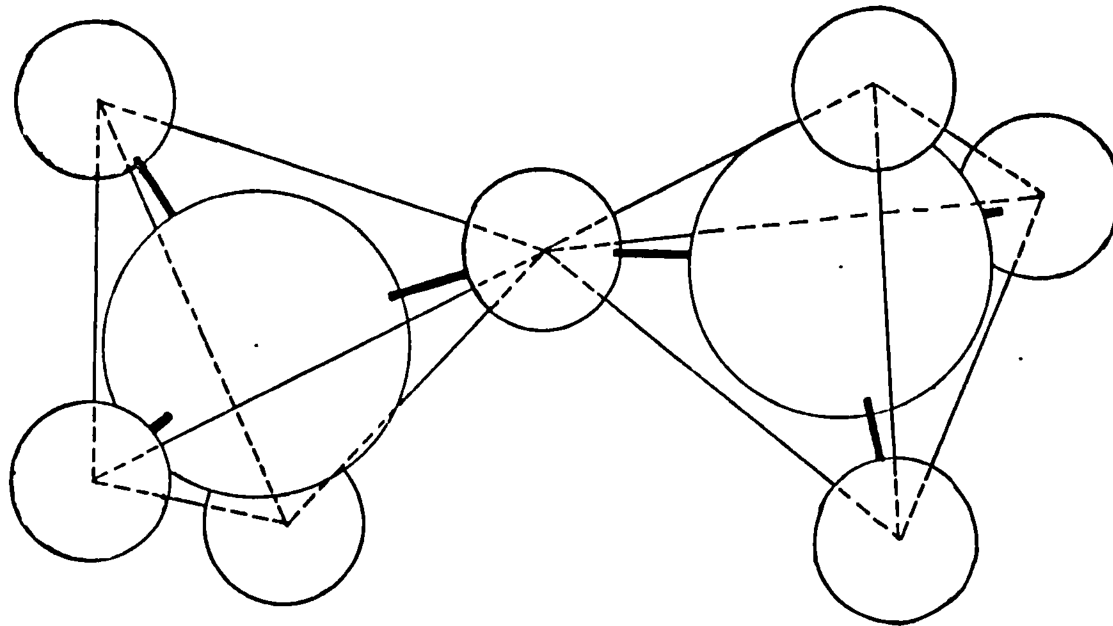


Fig. 3

Linked SiO_4 tetrahedral units in SiO_2. The larger atoms are silicon.

They estimate that models with the Si-O-Si bond angle with a mean of 150° will give better agreement between the density of the material using the model as a starting point and the actual density of SiO_2 of 2.20 g. cm^{-3}. The approximately constant bond lengths and bond angles in the basic tetrahedral building unit, results in the insulator exhibiting short range order, while the appreciable variation in the Si-O-Si bond angle leads to a lack of long range order and the SiO_2 being noncrystalline.

2.1.4. The SiO_2 - Semiconductor Interface - Atomic Structure

Mismatch exists between the insulator and semiconductor films because the two materials have different lattice parameters. This mismatch is taken up by a series of dislocations. Dislocations involve unsatisfied bonds or "dangling" bonds which can act as electron traps and constitute the interface traps. Further details on interfaces are given in Appendix A.

The TFTs used in this project were prepared by deposition on room-temperature substrates. The TFTs exhibited satisfactory field-effect transistor operation only after being annealed at 400°C, in dry nitrogen, for 1¼ hours. The reason for this is not fully understood, although it has been suggested that one of the effects of annealing might be the reduction in the density of states at the SiO_2 - CdSe interface, by a process similar to the reduction of the trap density at SiO_2 - Si interfaces, below that found on the "free" surface of Si. (4-7). This reduction is a result of the ability of the Si-O-Si bond angle to vary about a mean, without disrupting short range order, which confers a relatively large degree of freedom on the atomic positions of the SiO_2, hence providing accomodation of the insulator and semiconductor at the interface without the appearance of an

unacceptably high density of dislocations. Hence SiO_2 has the property of saturating "dangling" bonds during annealing. This is an application of Revesz's proposal (8) that the low density of interface traps between SiO_2 and Si is due to the structure of SiO_2 - it is noncrystalline but with a high degree of short range order, as discussed in section 2.1.3. In crystalline SiO_2 no freedom in bond angle or atomic position would exist, and the two crystalline solids cannot be accomodated at the interface without forming various structural defects which result in the deterioration of the interface properties.

2.1.5. Bulk Properties of the Insulator

It has been shown (7) that the insulator used in the present TFTs is stoichiometric SiO_2. The insulator films are stable, reproducible and have a high breakdown voltage. Furthermore, they do not appear to contain any impurities or imperfections (Appendix B). Unless care is taken, the vacuum deposited and sputtered oxides are often not characterised by a high degree of short range order and their composition often corresponds to SiO_x, where, depending on the conditions of deposition and post deposition treatments, x varies from one to about two (9). These films can be truly amorphous in the sense that both Si-Si and Si-O bonds occur. The use of SiO_x as an insulator film in interface devices was found to be unsatisfactory because of instability effects (7) resulting from a lack of short range order (8). It was found that to overcome this a 95% argon 5% oxygen mixture had to be used for the sputtering gas, in order to correct for the oxygen deficiency which occurs when pure argon is used. Such stable SiO_2 films have been analysed by Revesz (8) who attributes their desirable properties once more to their noncrystalline nature and high degree of short range order. Short range order is important in establishing a well defined structure that can easily be reproduced, and in which the bulk defect density is minimal. Non-

crystallinity prevents unwanted transport processes along grain boundaries which would occur in a polycrystalline film. Furthermore, crystallinity in SiO_2 results in the deterioration of the dielectric strength of the insulator. The intrinsic breakdown strength is 7 to 9 MV cm^{-1} in a pinhole-free noncrystalline SiO_2 film, but localised crystalline regions break down at 1 to 3 MV cm^{-1} fields (10). It is known that noncrystallinity is essential for obtaining the highest dielectric strength in dielectric oxide films (11). The degradation of a good quality noncrystalline oxide film to a polycrystalline one will be indicated by a fall in the dielectric stength of the insulator.

2.1.6. Experimental Results on Interface Traps

Consigny and Madigan (12, 13) have determined the energy and density of fast interface states between SiO and single crystal CdSe by measuring the capacitance-voltage characteristics of MIS capacitors. They report that at the SiO - CdSe interface, there is a band of acceptor-like states at 0.7 eV below the conduction band edge when the SiO is grown on the (0001) plane of CdSe - the basal plane - the band being about 0.2 eV wide. For the $(10\bar{1}0)$ plane - the cleavage plane - the acceptor-like traps are at 0.6 eV and about 0.05 eV wide. Their density is of the order of 10^{12} eV^{-1} cm^{-2}. They suggest that SiO reduces the surface state density below that found on the "free" CdSe surface which has about 7 x 10^{14} atoms cm^{-2}. Hence it appears that SiO has an effect on CdSe, similar to that of SiO_2 on Si.

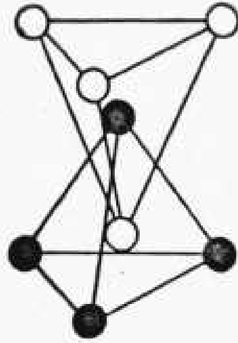
2.2. The Semiconductor

The semiconductor used in the TFT was polycrystalline CdSe.

2.2.1. Lattice Sites and Crystal Structure

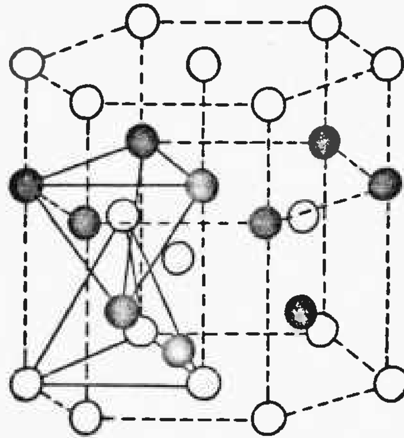
A single crystal of CdSe is considered here. The cadmium and selenium atoms occupy tetrahedral sites. A tetrahedral lattice site in a compound AB is one in which each atom A is surrounded symmetrically by four nearest neighbouring B atoms. For this to occur, the B atoms must sit on the corners of a tetrahedron with the A atom situated at its geometrical centre. The A and B sites are identical as far as their tetrahedral nature is concerned. The combination of the tetrahedral sites takes two possible forms which are relevant to the compound CdSe. Fig. 4(i) illustrates the situation when the base triangles of the interpenetrating tetrahedra are parallel and lined up normal to each other. Fig. 5(i) shows the base triangles again parallel but rotated through 60° about the normal to each other. These two combinations of the tetrahedral lattice sites leads to the two crystal structures, wurtzite and zinc blende. The wurtzite structure which is in the hexagonal crystal class has the combination of tetrahedral sites illustrated in Fig. 4(i). It consists of two interpenetrating close-packed hexagonal lattices, as illustrated in Fig. 4(ii), displaced with respect to each other by a distance $(\frac{3}{8})c$ along the hexagonal c-axis.

The combination of sites illustrated in Fig. 5(i) gives the zinc blende structure which is in the cubic crystal class. It is illustrated in Fig. 5(ii). It is composed of two interpenetrating cubic close-packed lattices translated with respect to each other by $\frac{1}{4}$ of a body diagonal. Both wurtzite and zinc blende forms of CdSe are known (14). The zinc blende form is metastable; conversion to wurtzite starts above



(i)

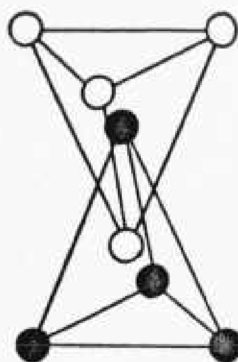
Tetrahedral sites with bases of tetrahedra parallel and in line vertically



(ii)

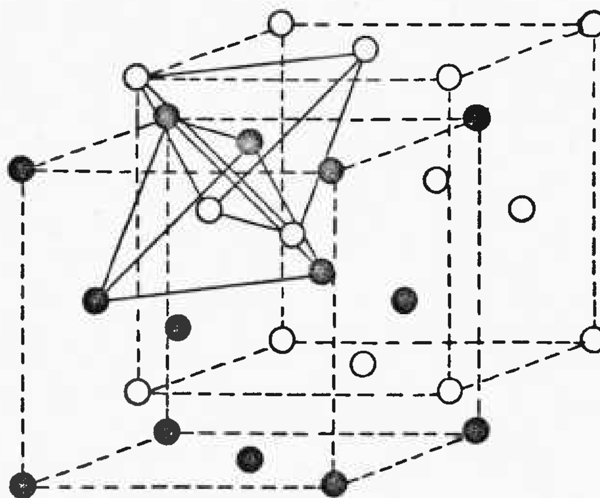
Fig.4

Wurtzite structure (ii) illustrating type (i) tetrahedral sites



(i)

Tetrahedral sites with bases of tetrahedra parallel and 60° out of line vertically



(ii)

Fig. 5

Zinc blende structure (ii) illustrating type (i) tetrahedral sites

$130^{\circ}C$. Single crystals grown at high temperature have the wurtzite structure.

2.2.2. Point Defects in Single Crystal CdSe

In the previous section the various arrangements of atoms in a perfect crystal of CdSe was discussed. It is important, however, to have some knowledge of the nature of atomic defects that may arise in the structure of real crystals of CdSe. The reason for this is threefold. Firstly, defects give rise to electron traps and secondly, the movement of defects at elevated temperatures, or under the influence of a high electric field, alters the energy distribution of traps in thin films of polycrystalline CdSe. Thirdly, a knowledge of the origin of point defects in single crystal CdSe is useful in identifying the larger number of defects which arise in polycrystalline CdSe - the separation of the single crystal defects from the rest facilitates the identification of the latter.

CdSe, whether single crystal or polycrystalline is always an n-type semiconductor (14-20, 25). Holes have not been detected during practical experiments on CdSe because the time constant for minority carrier generation is of the order of 25 hours (12).

A popular diagnostic technique that has been used to examine atomic defects in single crystal CdSe has been to monitor changes in the conductivity after an additional amount of cadmium or selenium has been diffused into the crystal. The conductivity is then related to the density of free carriers and this to the defects acting as donors.

In the work of Tubota et. al. (15) the samples were obtained by slow cooling from the melt of stoichiometric composition. Selenium or cadmium was evaporated on the surface of the crystals which were then heat-treated at various temperatures for various durations so that

the elements diffused into the bulk material. These treatments were performed in the vapour of the corresponding element. The changes in resistivity of the treated specimens are shown in Fig. 6. The result shown by the dashed curve was obtained for a specimen doped with selenium after doping with cadmium at 350°C. The other curves are for specimens treated with the one element shown. The results show that treating with selenium increases the resistance of the samples and hence the density of free carriers decreases and so the density of donors decreases; treating with cadmium decreases the resistivity, hence the density of carriers increases and so does the density of donors. They suggest that the defects contributing to electrical conduction are selenium vacancies and that the increase in resistivity due to the selenium treatment can be attributed to a decrease in selenium vacancies. Conduction due to selenium vacancies implies that the CdSe crystals obtained from the melt of stoichiometric composition have an excess of cadmium on lattice sites. Similar behaviour would be obtained for samples under selenium treatment if instead of selenium vacancies, the excess of cadmium was present as interstitial atoms. These could then be expected to act as donors. However, treatment under selenium vapour would not be expected to affect cadmium interstitials except in the surface region of the crystal where new CdSe would form. The heat treatment involved in the experiment could well lead to diffusion of the cadmium interstitials to vacant cadmium sites and this would reduce the density of donors. The only certain conclusion from this work is that both selenium vacancies and cadmium interstitials may act as donor impurities.

Shiozawa and Jost have conducted similar experiments and their work has been commented on by Woodbury (14). They have attributed an

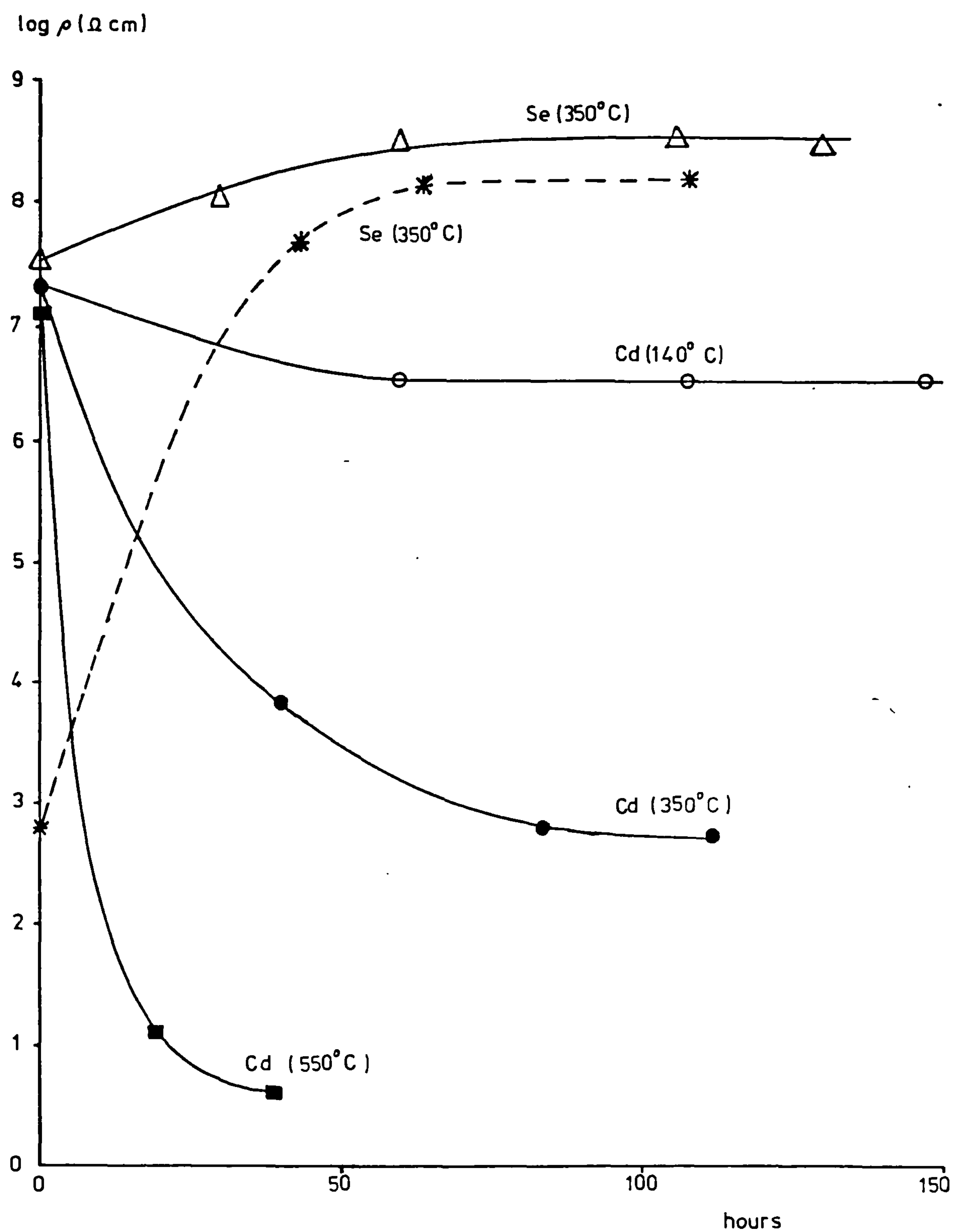


Fig. 6
Resistivity of CdSe doped with Cd and Se

increase in n-type conductivity under cadmium firing to interstitial cadmium.

It is concluded that single crystals of CdSe are excess in cadmium and that the atomic defects which arise are selenium vacancies (excess cadmium on tetrahedral lattice sites) or interstitial cadmium, or both. These defects act as donors.

2.2.3. Point Defects in Polycrystalline CdSe

In the case of thin films of polycrystalline CdSe, prepared by vacuum evaporation, as in the present work, the films result in a high carrier concentration - typically 10^{18} cm^{-3} (16) - if they are deposited on substrates held at room temperature. Before use, they are annealed at 395°C for 1¼ hours in dry nitrogen, to reduce the bulk carrier concentration to about 10^{16} cm^{-3} (7, 17). Woodbury (14) has reported that in II-VI compounds such as CdSe, significant diffusion of the excess atoms out of the sample can occur at 200°C or above. This has been used by Van Calster and Pauwels (18) to back their proposal, that the decrease in carrier concentration, as a result of annealing, is caused by the diffusion of excess cadmium in lattice sites i.e. (at selenium vacancies) out of the CdSe bulk. We conclude that interstitial cadmium would also diffuse out of the sample. This is supported by Woodbury's work and that of Burmeister and Stevenson (19), who report that the introduction of cadmium into interstitial sites in CdSe is reversible. Furthermore, at least some of the out-diffusing cadmium from the bulk crystallites can be expected to accumulate at the grain boundaries and may even form precipitated cadmium particles in the boundary. The diffusion of cadmium and selenium in CdSe may be estimated, by measuring the changes in the conductivity under cadmium or selenium firing. Shiozawa and Jost

have made such experiments and these have been commented on by Woodbury. Cadmium firing resulted in fast changes in conductivity, corresponding to rapid diffusion rates for cadmium, whilst selenium firing resulted in slow changes and hence slow diffusion rates. The results of Tubota et. al discussed in section 2.2.2. would support these results.

2.2.4. The Potential Energy of Point Defects in Single Crystal CdSe

The importance of a knowledge of the atomic defects in single crystal CdSe in the analysis of defects in more complex systems, such as polycrystalline films, has been mentioned before. Before this analysis is carried out, however, the energy of the donors below the conduction band edge, in single crystal CdSe, must be known. This is because the diagnostic technique frequently used to examine defects is the TSC method which gives the energy level of the defect.

Burmeister and Stevenson (19) have examined single crystal CdSe annealed under a high cadmium pressure at 900°C for a period of one week. Conductivity measurements were carried out on these specimens in the temperature range 4.2 to 300°K. The results were used to determine the concentration and ionisation energy of the dominant defect level. Samples annealed under a high cadmium pressure exhibited carrier concentrations in the range of 10^{6} to 10^{17} cm^{-3} at 295°K, while the concentration for as-grown unannealed samples was 10^{16} cm^{-3}. Carrier concentrations in samples used in the present work fall within this range. Only one energy level was found for donors at an energy of 0.014 eV below the bottom of the conduction band edge. They associated this level with interstitial cadmium. Most of the donors became ionised between 4.2 and 77°K. Workers whose work will now be discussed, have not reported this shallow donor level possibly because, unlike Burmeister and Stevenson, they have used liquid nitrogen cooled cryostats.

Manfredotti et. al. (20) have carried out TSC and space charge limited current (SCLC) measurements on single crystals of CdSe. Table 1 gives the energies of the various trap levels found.

Kindleysides and Woods (21) have conducted TSC measurements on single crystals of CdSe. Prior to each TSC run, the sample, which was in vacuum, was heated to 400°K in the dark and then cooled to 90°K. During the cooling the optical excitation was switched on when the sample reached some intermediate temperature T_r, and maintained to 90°K. They report a number of traps which they group into three - the low, intermediate and high-temperature groups - depending on which temperature range the corresponding peaks occur in, on the TSC characteristic. Their results appear in Table 2. The characteristic feature of the high-temperature traps was that their associated TSC peaks were not observed unless the crystal had been cooled under illumination from some temperature above a particular threshold immediately before the TSC curves were measured. Increasing the temperature at which illumination was begun resulted in an increase in all the high-temperature TSC peaks. The three peaks at 295, 335 and 365 °K had threshold temperatures of 250, 285 and 320 °K respectively. They suggest that the above may be due to photochemical effects caused by illuminating the crystal (22, 23) which may have led to changes in the existing trap density or to the creation of new traps. These changes may involve the dissociation of a defect complex and will not be gone into in detail in this work.

The intermediate-temperature traps were small or non-existent when the samples were cooled in the dark. However, peaks appeared with illumination. Heating at 400°K led to the complete disappearance of these traps. They suggested that this type of behaviour was the

E_t (eV) (From TSC experiments)	E_t (eV) (From SCLC experiments)	N_t (cm^{-3}) (Order of magnitude only)
	0.156	10^{13}
0.177	0.177	10^{13}
0.26	0.26	10^{11}
0.31	0.31	10^{11}
	0.36	10^{11}
0.38		10^{11}
0.4	0.41	10^{11}
	0.49	
	0.63	10^{10}

Table 1.

Energy E_t, and density N_t, of trap levels in single crystal CdSe after Manfredotti et. al. (23).

Trap group	Peak temperature (^{o}K)	Trap energy (eV)	Trap density (cm^{-3})
Low temperature	105	0.15	10^{12} to 10^{14}
	115	0.19	,,
	130	0.19	,,
	150	0.28	,,
	160	0.29	,,
	175	0.30	,,
	200	0.36	,,
Intermediate temperature	215	----	at least 10^{15}
	230	0.46	,,
	250	----	,,
	270	----	,,
High temperature	290	0.43	----
	335	0.52	10^{17}
	365	0.63	10^{19}

Table 2.

Energy and density of traps in single crystal CdSe after Kindleysides and Woods (24).

result of two competing processes, one which involved the photochemical creation of the traps and a second which was a process of thermal destruction. The appearance of a peak in the intermediate to high-temperature range, as a result of illumination has also been reported in CdS-CdSe crystals examined by Bube and commented on by Ray (24). The peak disappeared if excitation was at 90°K. The TSC curves are shown in Fig. 7.

The low-temperature traps which gave peaks between 105 and 200°K were not attributed to photochemical changes because the concentrations of these traps were independent of illumination history.

It is concluded from the above, that for measurements on CdSe in the dark, the only bulk traps that would appear would be the low-temperature ones giving peaks between about 105 and 200°K. An account of the illumination treatment to which the specimens have been subjected to during TSC measurements has only appeared in the paper just reviewed. This casts some doubt as to the nature of the origin of intermediate and high-temperature peaks in TSC characteristics of other workers i.e. whether these have resulted as a consequence of photochemical changes or are due to inherent traps in as grown CdSe that would appear in all CdSe crystals.

It is observed that there is very good agreement between trap densities reported by Manfredotti et. al. and Kindleysides and Woods for low energy traps up to about 0.2 eV. For higher energy traps the densities vary significantly. The discrepancy may be due to the different illumination histories the specimens were subjected to by the different workers resulting in photochemical changes which produced traps of different densities. The above comparison of results supports the earlier conclusion that it is only low temperature traps that are

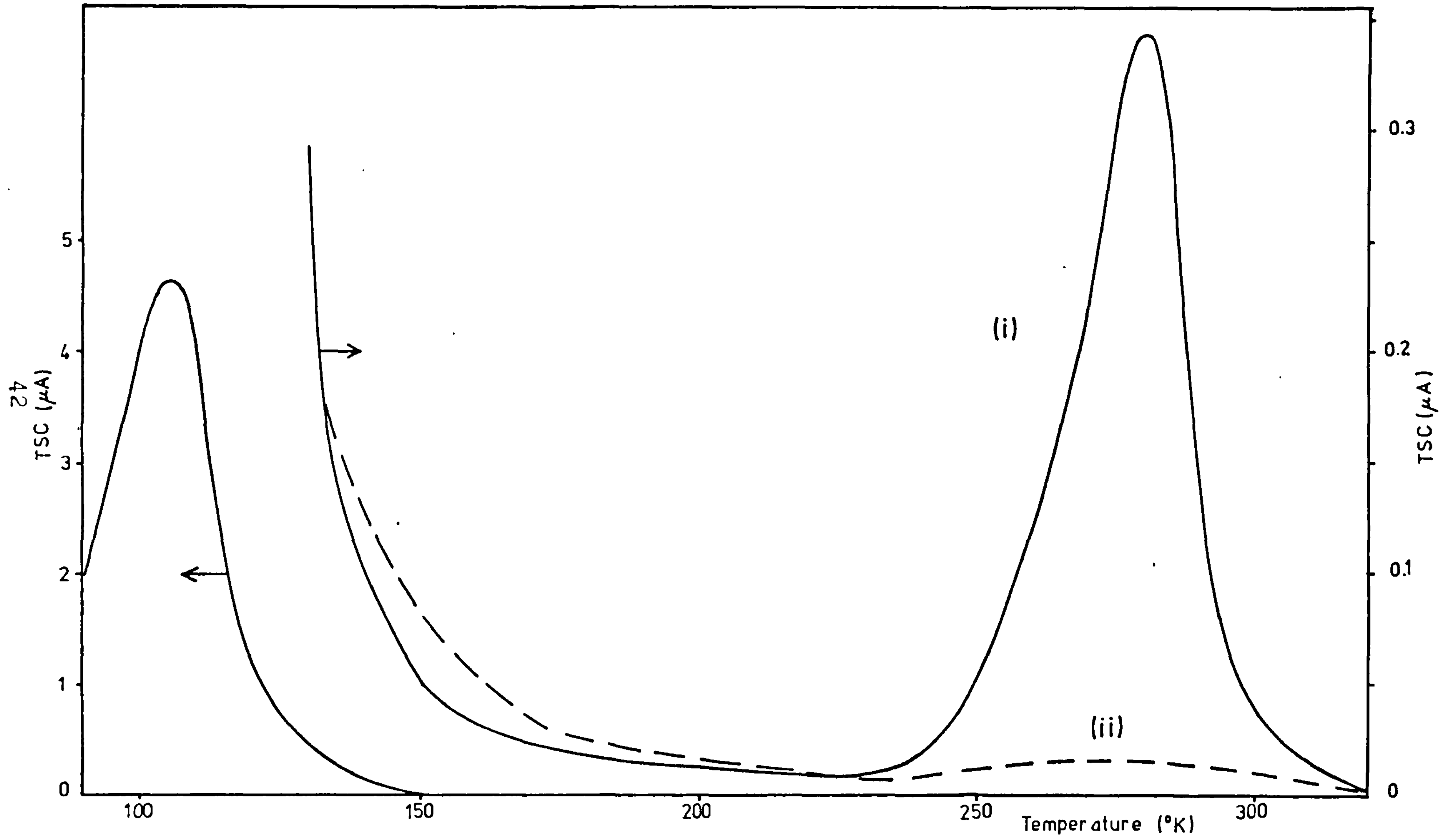


Fig. 7

TSC curves for sample illuminated (i) continuously while cooling (ii) at 90°K only

present in CdSe crystals that forgo illumination before TSC runs. There is agreement in trap energies between the two sets of results.

2.2.5. Polycrystalline CdSe

This section contains a review of the work on polycrystalline CdSe preceding the present one. In polycrystalline films both bulk and grain boundary traps occur. The main inadequacy of earlier investigations, however, has been the lack of the topographical identification of traps.

Shimizu (25) has evaporated films of CdSe 1 ± 0.1 microns thick on to substrates held at different temperatures. Those held at 100°C would be expected to exhibit properties closer to the as-deposited (i.e. unannealed) films of the present work and those at 300°C closer to the annealed films. Conductivity and TSC measurements were made but the temperature at which the sample was excited in the latter experiments is not mentioned. The TSC curves are shown in Fig. 8 and exhibit two peaks - one at about 145°K and the other at about 240°K. He has used the assumption that the concentration of trapped electrons, n_o, is constant during the initial rise of the TSC peak. Then the TSC is

$$I_{TSC} = n_o \, \nu \, \exp\left(-\frac{E_t}{kT}\right) \qquad (1)$$

where ν is the attempt-to-escape frequency for electrons and E_t is the energy of the trap below the lower edge of the conduction band. T is the temperature. By plotting the logarithm of the current against the reciprocal of temperature, he obtains a straight line for each TSC peak. From the slope of this line the depth of the trapping level can be determined. He finds two traps, at 0.13 eV for the first peak and 0.40 eV for the second, the first peak being the 145°K one. For films deposited

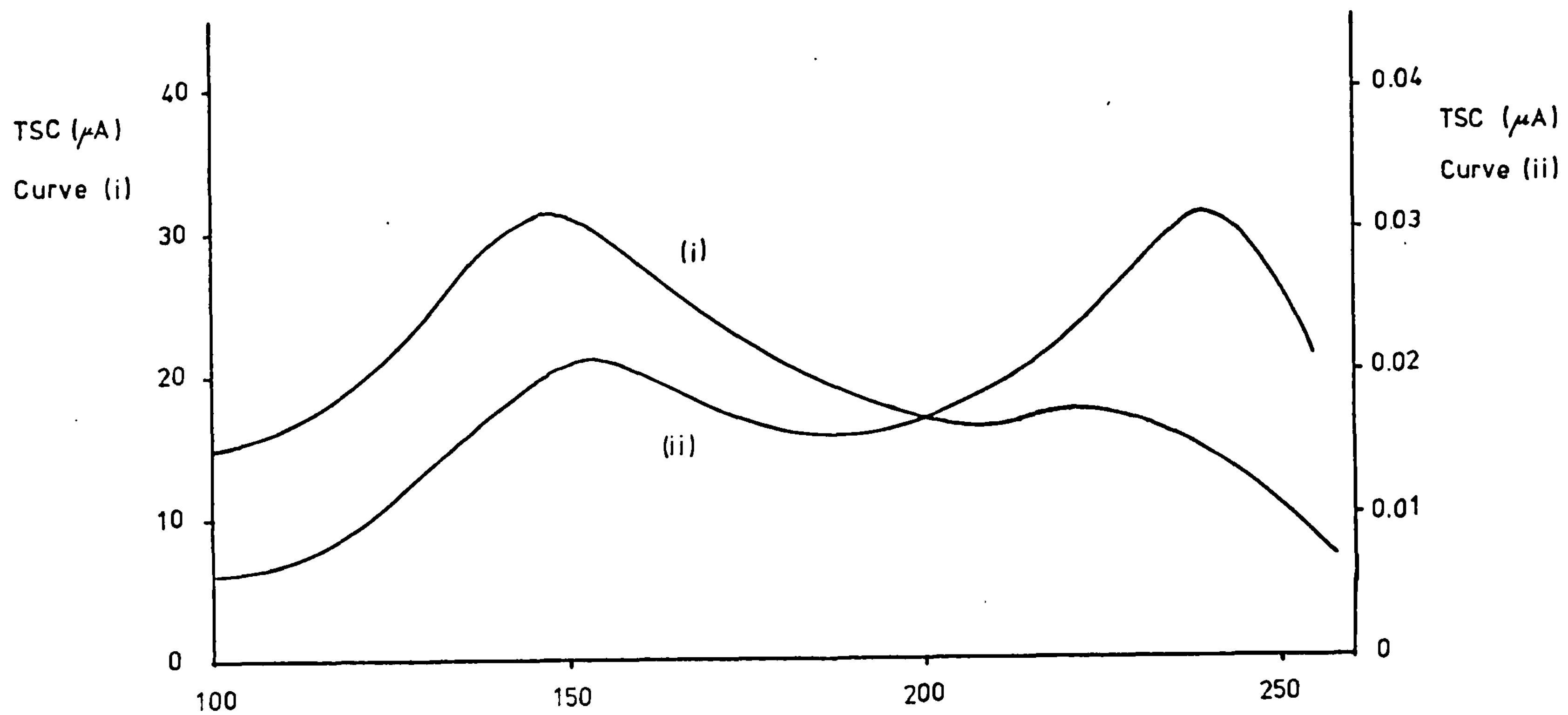


Fig. 8
TSC curves for CdSe films deposited at (i) 100°C (ii) 300°C

at the lower temperature, the charge associated with the first peak is greater than that of the second, charge being proportional to the area under a peak. Depositing films at the higher temperature results in the diminution of the charges associated with both peaks and the reversal of the relative magnitudes of these charges the charge of the second peak now being larger than that of the first. Although he associates the 0.14 eV level with selenium vacancies the origin of the second peak is unknown. It may be due to grain boundary traps. It may also be due to the creation of a trap due to photochemical changes but this is not certain as the illumination history of the samples is not stated.

More recently, Hino and Yamashita (26) have made TSC measurements on Al-CdSe-Al sandwiches. The CdSe was a film 5000 Å thick, produced by vacuum evaporation. The films were recrystallised by heating in vacuum. It is assumed that the CdSe was polycrystalline. Two TSC peaks were observed - one between 150 and 200°K, peaking around 180°K, and another between 250 and 350°K, peaking at about 300°K. They give the energy of the first peak as 0.13 eV but no mention is made of that corresponding to the second. No mention has been made of the temperature of excitation. The topography of traps is ignored completely.

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CHAPTER III. THE TSC TECHNIQUE

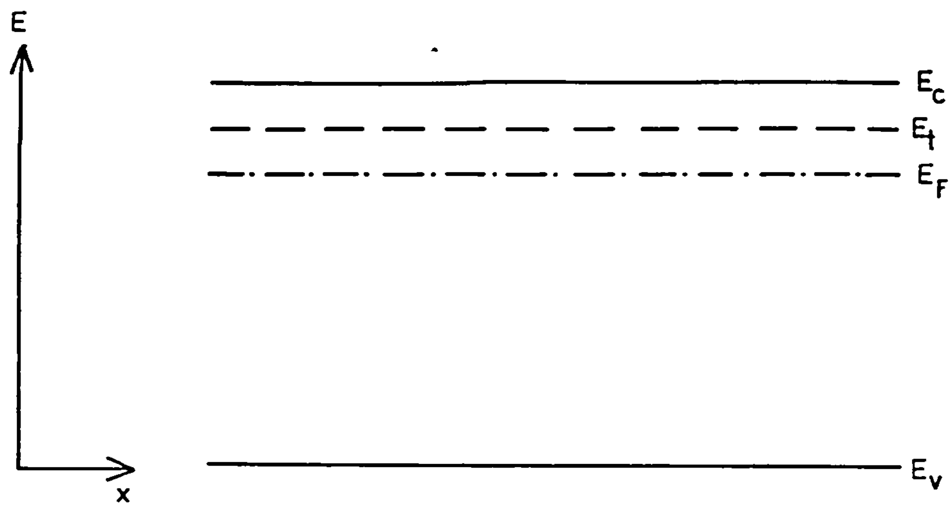
3.1. Earlier TSC Theory

Earlier TSC theory ignored the topography of traps. Simmons was the first to realise this and his theory will be dealt with later in this chapter. The earlier theory will now be gone into.

It will be assumed that all traps are monovalent and those in the upper-half of the bandgap of the semiconductor are neutral when empty, and thus negatively charged when filled (acceptor type) and those in the lower-half are neutral when filled (donor type) and thus positively charged when they loose their electrons (i.e. capture a hole). Consider traps to be at an energy E_t in a single crystal semiconductor at temperature T^oK with a density of N_t per m^{-3}. E_F is the energy of the equilibrium Fermi level and it is assumed that E_t lies above E_F as shown in Fig. 9(i). Since traps above E_F are essentially empty and those below full, E_t is an empty level. If the sample is now cooled to a low temperature - say liquid nitrogen temperature - and light of high enough energy is shone on it to excite electrons from the valence to the conduction band, the concentration of free carriers will increase and the Fermi level will be raised above E_t as shown in Fig. 9(ii). The traps are now full and the Fermi level is referred to as the quasi-equilibrium Fermi level. If the source of excitation is removed, the traps will remain full because the probability that they may emit their electrons to the conduction band at temperature T is given by

$$p = \nu \exp\left(- \frac{E_t}{kT}\right) \qquad (2)$$

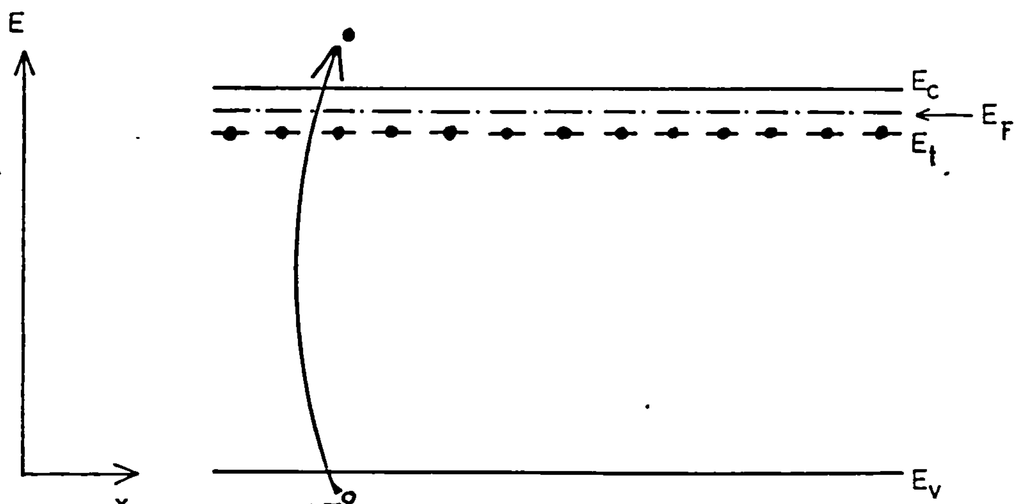
where ν is the attempt-to-escape frequency for electrons in s^{-1}. Because the temperature is low, p is very small and the time constant



(i)

— Empty trap

-●- Full trap



hf

(ii)

Fig. 9

Energy diagram for semiconductor (i) in the dark and (ii) under illumination

for the emission of the trapped electrons will be so high that the current due to electron emission will be negligibly small - this current will appear to be constant although it is a transient one. If the temperature of the sample is increased linearly with time, at a uniform rate β $^{o}K\ s^{-1}$, the probability of electron emission from the traps increases and they start emptying their electrons, hence giving rise to a current called the thermally stimulated current (TSC).

To describe the rate of change of the free carrier concentration giving the TSC, the relative magnitudes of the capture cross sections, S_t and S_r of the trapping and recombination centres must be considered. Three cases have been analysed in the literature depending on whether the recombination or retrapping of free electrons predominates or if both processes have an equal probability of occurring (1). The three analyses give differing equations for the conductivity. The TSC curves i.e. the TSC against temperature plots, exhibit peaks where each peak is associated with a trap level. A useful way of analysing TSC peaks is to use the method of Garlick and Gibson (2) who observed that in each of the three cases quoted above, the leading edge of the peak is proportional to exp ($- E_t/kT$). In analysing TSC peaks the three principal features made use of are:

1) ln TSC versus 1/T for the leading edge of the peak gives a straight line and E_t can be calculated from the slope;

2) The area under the TSC peak is proportional to the number of electrons released from the trap;

3) The temperature corresponding to a TSC maximum varies with heating rate β.

3.2. Simmons' TSC Theory

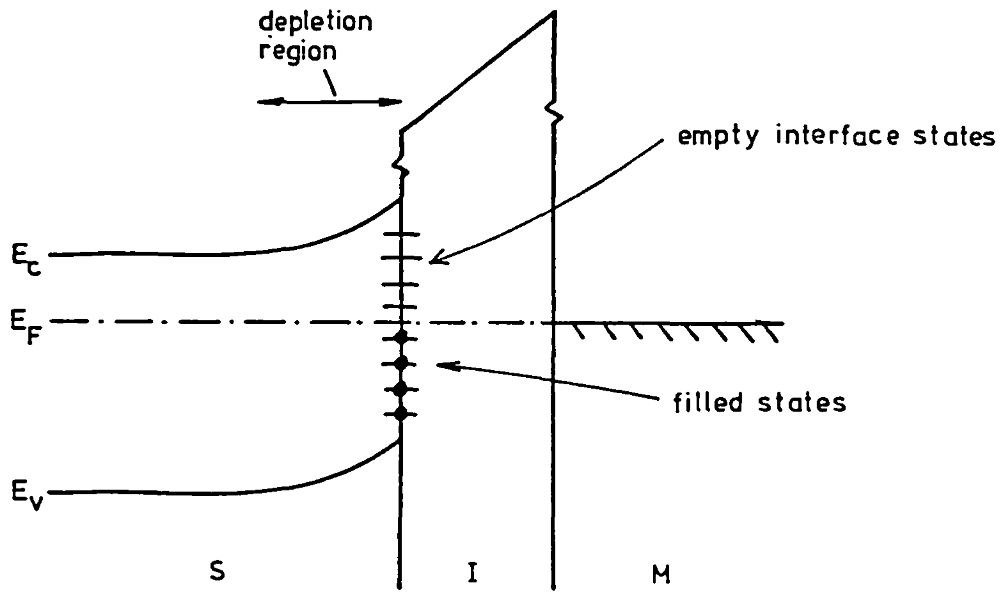
Simmons, Taylor, Wei and Mar (henceforth referred to as Simmons) have been the first to relate the topography of traps to TSC curves. Furthermore, they have analysed various types of traps in single crystal MIS devices and their analysis is included here, because it clarifies the basic concepts involved in the TSC method, and can be used as the basis for the analysis of the traps which occur in the polycrystalline MOS devices used in the present work.

3.2.1. Fast Interface States

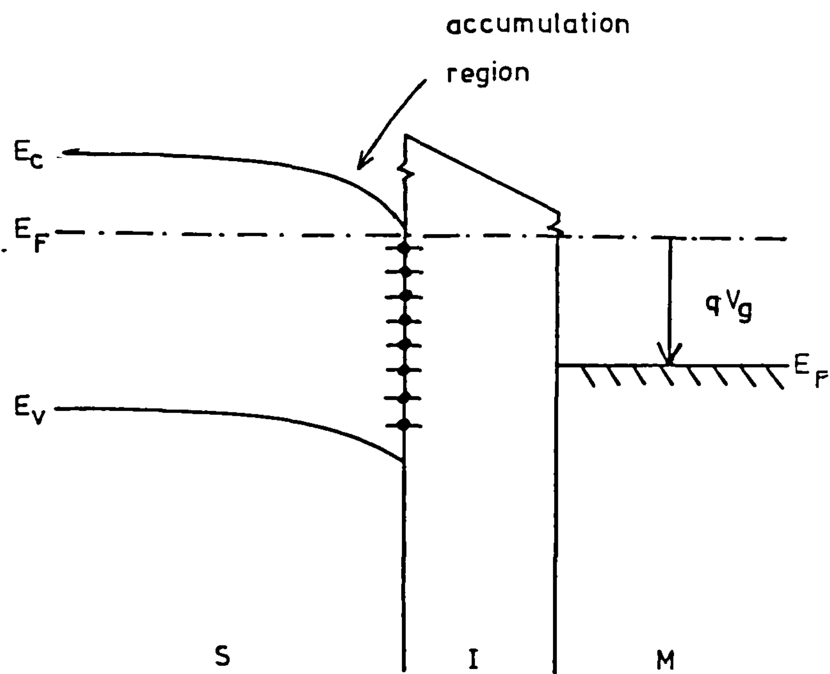
Simmons has considered an MIS device which is a metal-silicon dioxide insulator-single crystal silicon semiconductor system. He has developed the TSC theory for fast interface states, which are those states situated at the semiconductor-insulator interface and do not penetrate into the insulator. In this thesis "fast" states are defined as those which can capture or release electrons in less than a millisecond. They have a value of ν of the order of 10^{10} to 10^{12} s^{-1} (3,4).

3.2.2. Emission and Generation TSC from Interface States

Fig. 10(i) shows the MIS device with no gate (metal) voltage applied. In thermal equilibrium the acceptor type interface states cause the depletion of the n-type semiconductor,near the interface, of electrons. This is explained in Appendix C. To fill the empty states lying above the Fermi level, a positive voltage is applied to the gate as shown in Fig. 10(ii). The surface of the semiconductor is now in the accumulation mode i.e. a layer of free electrons exists on the semiconductor side of the interface. Traps previously above the system Fermi level are now depressed below it.



(i)



(ii)

Fig.10

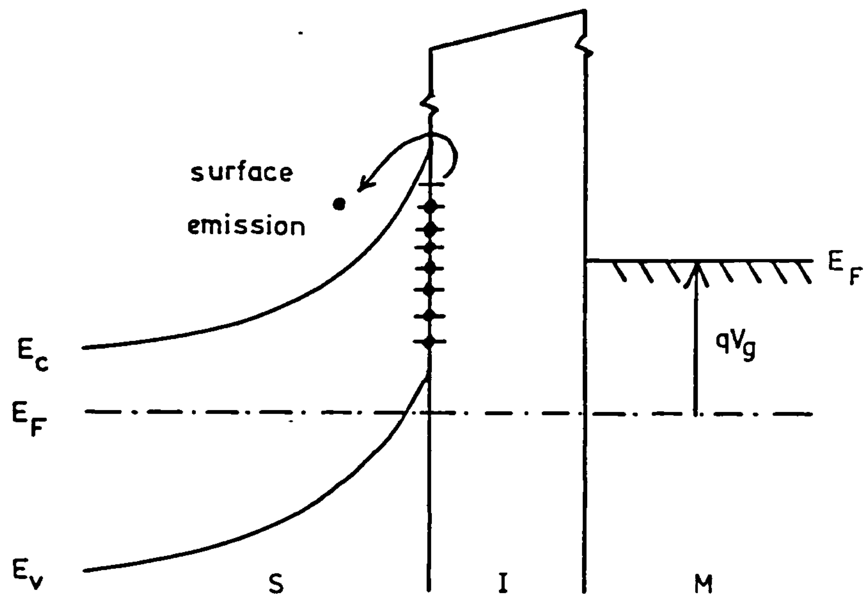
Energy diagram showing MIS system (i) in equilibrium with $V_g = 0$

(ii) in accumulation mode

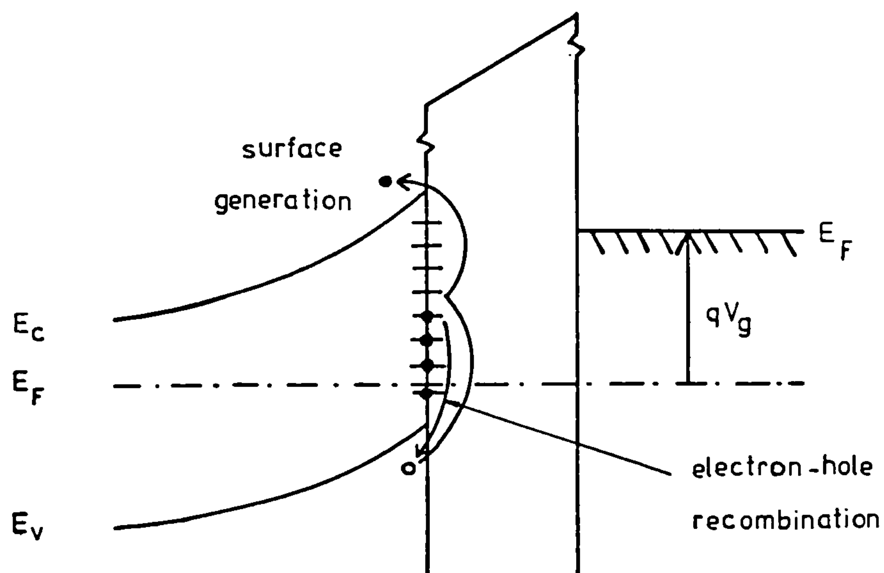
All states below the system Fermi level are essentially full while all states still above it are essentially empty of electrons. Hence in MOS devices, interface traps can be filled without shining light on the device and so the sample can remain in the dark throughout the experiment. In this way the generation of new traps by photochemical reactions is avoided.

If a large negative gate voltage is now applied, the surface of the device goes into the depletion mode. The interface states are raised above the Fermi level. If this is done at high temepraturе, the trapped electrons escape quickly. However, if the accumulation is done at room temperature and maintained down to liquid nitrogen temperature (or if the device is accumulated at liquid nitrogen temperature) and the device then driven into the depletion mode, the electrons trapped in states above E_F will only escape over an extremely long period of time (Fig. 11(i)). This is in agreement with equation (2). Two Fermi levels exist at the interface; the system Fermi level E_F determined by the semiconductor bulk and the non-steady-state Fermi level corresponding to the energy of the uppermost filled interface state, E_{fnss}. Since these two levels do not coincide at this low temperature we have a non-steady-state or transient situation. Hence when the device is switched into the depletion mode at the low temperature a small current flows corresponding to a very slow discharge of the traps, the magnitude of which remains constant over a very long period.

If the temperature of the device is now raised slowly, the probability of a trapped electron escaping from an interface state will increase and there will be a change in the current flowing between the metal and the semiconductor as more and more electrons are emitted giving rise to the thermally stimulated emission current the magnitude



(i)



(ii)

Fig.11

Energy diagram showing the MIS system in the non-steady-state mode during (i)electron emission, (ii)electron-hole generation and recombination

of which depends on the temperature and the trap density (Fig. 11(i)). As electrons are emitted E_{fnss} moves down towards E_F. The emitted electrons are collected by the gate via the semconductor conduction band and the external circuit. A TSC run results in the transfer of charge from the interface to the gate like the transfer of charge between the parallel plates of a capacitor.

The emission TSC may be followed by the generation TSC. The negative gate voltage may give rise to an inversion layer at the interface. This means that for the n-type device considered, holes may appear at the interface. The density of these holes is negligible at the initial low temperature but as the temperature is increased, the free hole density at the interface increases rapidly as a result of the generation of electron-hole pairs through the interface traps (Fig. 11(ii)). However, at the same time, the density of free holes at the interface is diminished through recombination with electrons in the interface traps. Thus, the net effect is that free electrons appear at the interface. Once free they find themselves in the depletion region and are swept away by the high field existing there to give the generation TSC. It is observed that the free holes cannot move because the direction of the field requires them to move through the insulator which is not possible and so no hole current is observed. Inversion is possible in silicon devices but in the CdSe ones used in the present work no holes have been detected, as explained in section 2.1.6. This means that in these devices the TSC will be an emission one and no generation TSC will be observed. Fig. 12 shows the device at the end of the TSC run.

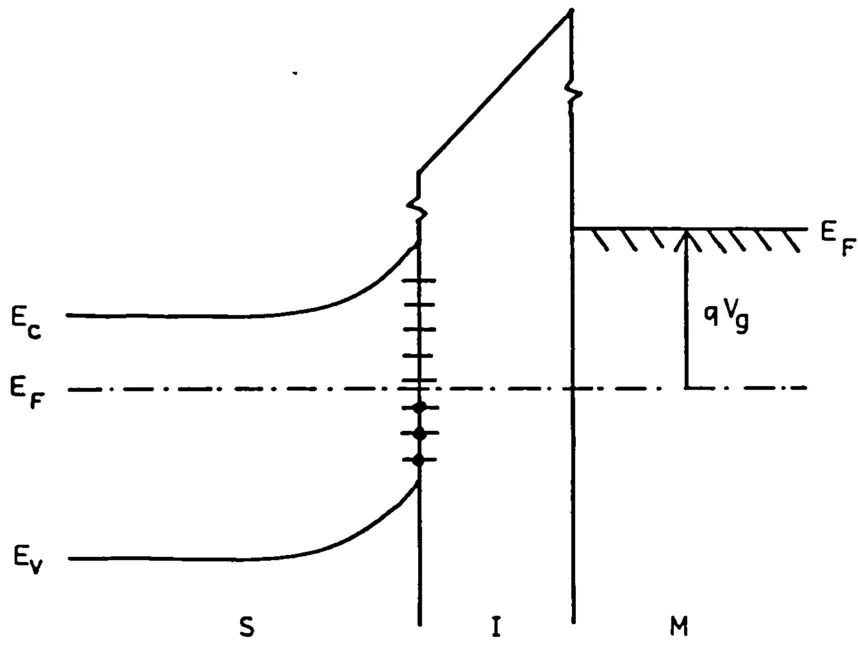


Fig.12

Energy diagram showing MIS system at end of TSC run.

3.2.3. Occupancy Function During Interface Emission and Generation

The rate equation which describes the occupancy of interface traps at an energy E in the nonequilibrium non-steady-state situation represented in Fig. 11, has been derived by Simmons et. al. (5,6) using Shockley-Read statistics (7). It is given by

$$\frac{df(E)}{dt} = (e_p + \overline{n}) - (e_n + e_p + \overline{n} + \overline{p})\ f(E) \tag{3}$$

where $\overline{n}$ and $\overline{p}$ are proportional to the interface densities of free electrons and holes respectively; e_n and e_p are the emission probabilities from the trap for electrons and holes respectively and f(E) is the occupancy function. The derivation of this rate equation is given in Appendix D.

In Fig. 11(i) the semiconductor at the interface is depleted of free electrons, hence $\overline{n}$ may be equated to zero. At the initial low temperature $\overline{p}$ is also zero, but at higher temperatures when generation occurs or when the device approaches the inversion mode, $\overline{p}$ plays a dominant role in silicon devices. Hence $\overline{p}$ will be retained in equation (3) which now becomes

$$\frac{df(E)}{dt} = e_p - (e_n + e_p + \overline{p})\ f(E) \tag{4}$$

If the temperature of the device is increased from the initial low temperature T_o, at a uniform rate β, so that this temperature is given by

$$T = \beta t + T_o \tag{5}$$

where t represents time, the solution to equation (4) is given by Simmons and Mar (6,8) to be

$$f(E) = \left(1 - \frac{e_p}{e_n+e_p}\right) e^{-\lambda} + \frac{e_p}{e_n+e_p+\overline{p}} \quad (6)$$

where

$$\lambda = \beta^{-1} \int_{T_o}^{T} (e_n + e_p + \overline{p})\, dT \quad (7)$$

For energy levels in the upper half of the bandgap

$$e_n >> e_p \quad (8)$$

and (6) becomes

$$f_{nss} \approx e^{-\lambda} \quad (9)$$

i.e. the contribution to f(E) in equation (6) is from the first term on the right hand side and the statistics are governed solely by the emission process, the generation process being negligible. Since the emission process is a non-steady-state one the occupancy function f(E) is called f_{nss}.

Simmons et. al. (3,8,9) have analysed λ and $e^{-\lambda}$. Fig. 13 shows how f_{nss} ($= e^{-\lambda}$) varies in the upper half of the band gap as temperature increases. It has a similar functional dependence on energy as that of a Fermi-Dirac distribution function. E* is therefore defined as the non-steady-state Fermi level at temperature T and $f_{nss} = \frac{1}{2}$ at E = E*. Thus traps more than about 2kT above E* are essentially empty, while those about 2kT below E* are full. As the temperature increases, E* moves down towards midgap. In so doing trap levels above E* empty by the emission process. In the process of being swept out of the depletion layer, these electrons give rise to the emission current. At some temperature T_4 at which E* reaches midgap, the function collapses rapidly about E_i for any further increase in

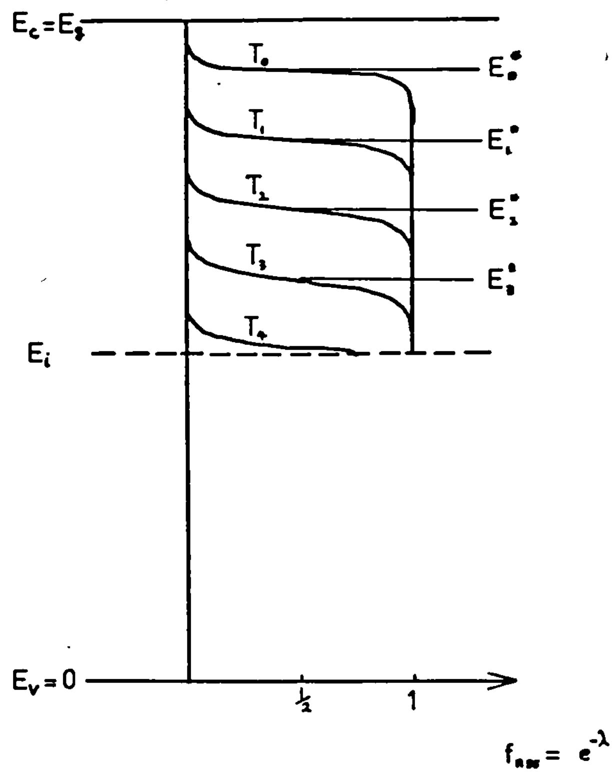


Fig.13

The term $e^{-\lambda}$ is shown plotted as a function of energy, with temperature as a parameter. The non-steady-state Fermi level, E^*, approaches midgap as temperature increases.

temperature. Hence above T_4 the first term of equation (6) becomes negligible in comparison with the second term. This means that the emission process ceases and the generation process takes over. It is observed that when the emission has ceased the occupancy function expressed by equation (6) collapses to a form that is identical to that defined by Simmons as the nonequilibrium steady-state case given in Appendix D with $\overline{n} = 0$ to account of the depletion of electrons.

Similarly, by repeating the above analysis for a p-type device, it can be shown that for such a device the emission process involves the moving of a non-steady-state Fermi level for trapped holes from near the top of the valence band to midgap as temperature increases and that the generation process follows the emission process. Hence in an n-type device, such as a CdSe TFT, traps in the upper half of the band gap will be examined. The reverse is true for a p-type device.

3.2.4. Quantitative Analysis of Emission TSC from Interface Traps in MIS Devices

In this section the quantitative analysis of Simmons et. al. (3,10) of the emission process from interface traps in MIS devices is discussed.

During the heating leg of the TSC run the emission TSC can be recorded against the temperature. The aim is to relate this curve to the electron trap distribution at the interface i.e. to transform the current against temperature plot to a density of traps against energy one. For an n-type device the emission TSC is due to the emptying of traps in the upper half of the band gap and hence traps in this energy range can be examined alone. The reverse is true for a p-type device. An n-type MIS device has been considered here. The emission process is governed by the electron emission rate, r_b

of electrons from traps (see equation (D2) of Appendix D). The analysis leads to an expression for the emission current I_e given by

$$I_e = \frac{qAC_I}{C_I + C_d} \int_{E_v}^{E_c} N_s(E)\ P\ (E,T)\ dE \tag{10}$$

where

$$P(E,T) = e_n \exp\ (-\beta^{-1} \int_{T_o}^{T} e_n\ dE) \tag{11}$$

and q is the electronic charge. C_I and C_d are the capacities of the insulator and the semiconductor depletion regions respectively. A is the active area of the device i.e. the area of overlap between the source (or the drain) and the gate, between which I_e flows (11). N_s (E) is the energy distribution of the interface states per unit area per eV. The rest of the symbols have already been defined. The function P(E,T) is shown plotted in Fig. 14 as a function of energy with temperature as a parametric variable. It is seen to exhibit a pronounced narrow peak that has a half width of approximately 2kT about the energy E_m at which the maximum occurs. Starting from (11) Simmons and Taylor also show that

$$E_c - E_m = 10^{-4}\ T\ [\ 1.92\ \log_{10}\ (\frac{\nu}{\beta}) + 3.2\ ]\ - 0.0155 \tag{12}$$

energies being measured in eV. By examining the non-steady-state occupancy function f_{nss} (E), they also show that the non-steady-state Fermi level E*, as defined previously, is related to the temperature by

$$E_c - E^* = 10^{-4}\ T\ [\ 1.92\ \log_{10}\ (\frac{\nu}{\beta})\ + 3.5\ ]\ - 0.015 \tag{13}$$

Comparing equations (12) and (13) it can be seen that E_m is essentially identical to E*, differing from E* at all temperatures by approximately kT/3 (see Fig. 14). Hence as the non-steady-state Fermi level moves

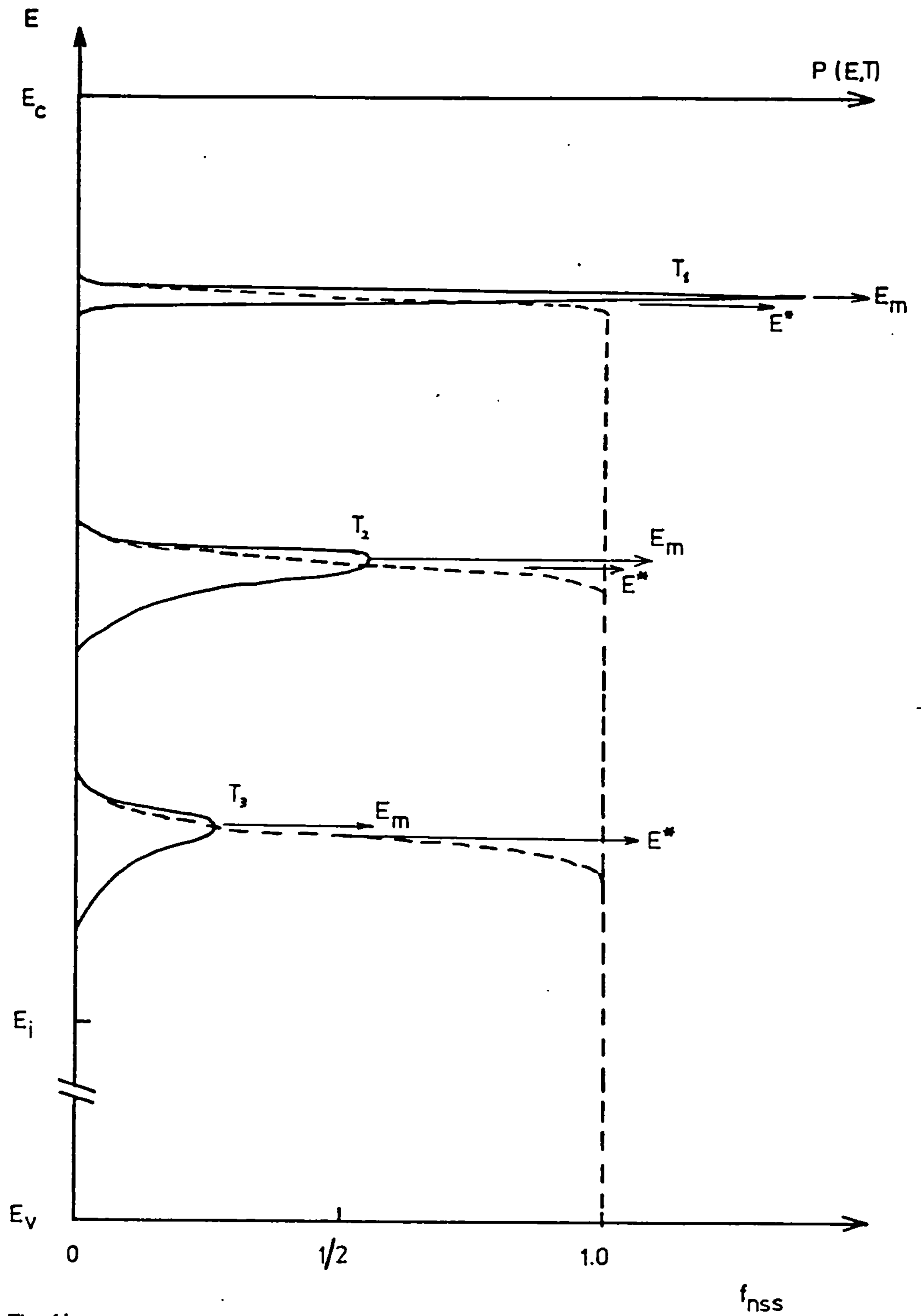


Fig. 14

The function P(E,T) for various constant temperatures.
The dotted lines illustrate $f_{nss}(E)$ for the temperatures quoted.
E_m and E^* are almost identical.

towards midgap, as the temperature rises, P(E,T) moves with it. Electrons are emitted as a result of this movement, giving I_e. Since P(E,T) has a half width of about 2kT about E_m, then it follows that only traps within about 2kT of the non-steady-state Fermi function contribute significantly to the emission current and that traps can be examined provided they cover an energy range of not less than 4kT. P(E,T) may be approximated by a delta function and since in the practical MIS devices examined by Simmons $C_I >> C_d$, equation (10) gives

$$I_e = 1.2qA\ 10^{-4} \left[1.92 \log_{10} \left(\frac{\nu}{\beta}\right) + 3.2 \right] N_s (E_m) \qquad (14)$$

$$\text{i.e. } I_e \propto N_s (E_m) \qquad (15)$$

This means that the trap density at energy E_m is proportional to the current at temperature T. But since, at this temperature, E_m is associated with the energy of traps contributing to the emission TSC, equation (12) can be used to find the energy of traps emptying. Equation (14) gives the trap density corresponding to this energy. Thus the I_e - T curve is a direct image of the interface trap distribution in the upper-half of the band gap. Hence, whereas the earlier TSC theory provided only one value of activation energy and trap density with any trap level, Simmons' method enables the whole trap distribution to be obtained.

The value of ν is found by recording the I_e - T curve at two heating rates β_1 and β_2 and measuring the temperatures T_1 and T_2 at which a prominent part of the characteristic (e.g. the maximum) corresponding to a particular energy, appears. Hence, from equation

(12), ν is determined from the expression

$$\nu = 10^{y} \tag{16}$$

where

$$y = \frac{T_2 \log_{10} \beta_2 - T_1 \log_{10} \beta_1}{T_2 - T_1} \tag{17}$$

The delta-function approximation of P(E,T) limits the analysis described above to traps distributed over 4kT or wider in energy. These are defined as distributed traps. Hence it is not applicable to a discrete trap. Simmons (3) defines a discrete trap of density N_t positioned at an energy E_t by

$$N_s = N_t \ \delta \ (E-E_t) \tag{18}$$

The I_e - T curve manifests a peak at temperature T_m and provided $C_I >> C_d$

$$E_c - E_t = 10^{-4} \ T_m [\ 1.92 \ \log_{10} (\frac{\nu}{\beta}) + 3.2 \ ] - 0.0155 \tag{19}$$

By obtaining two I_e - T curves corresponding to different heating rates and determining the temperature at which the two maxima occur, the trap energy and ν may be obtained. The trap density is in cm^{-2} and given by

$$N_t = \frac{2 \text{ x Area under curve}}{q\beta} \tag{20}$$

A check whether the trap is discrete is that

$$\Delta T = \frac{2kT_m^{\ 2}}{(E_c-E_t)} \tag{21}$$

where ΔT is the half-width of the peak. (i.e. the temperature width of the peak measured at half its maximum height)

3.2.5. TSC of Bulk Traps

In MIS type devices traps appear in the semiconductor bulk. Simmons and Mar have analysed the statistics of bulk traps in the context of the TSC technique (12). The approach is fundamentally the same as that used to derive the TSC transformation equations for interface states. The concepts of emission and generation TSC still apply (12,13). Bulk traps are usually donor centres in n-type MIS devices.

A positive gate voltage is applied to the device at room temperature so that the surface of the semiconductor is in the accumulation mode (Fig. 15(i)). In this mode all traps in the semiconductor located below the equilibrium Fermi level E_F are occupied, while those above are empty. The semiconductor is now cooled to a low temperature T_o in this condition (Fig. 15(ii)). During the cooling, traps at energy E_{t_1} which lay above the equilibrium Fermi level at room temperature, become filled provided T_o is low enough for E_F to rise above E_{t_1}. A reverse voltage is then applied to the metal electrode and the semiconductor goes into the non-steady-state depletion mode. This situation is shown in Fig. 16 and is characterised by two Fermi levels, the non-steady-state Fermi level of the filled states and the equilibrium Fermi level. Bulk generation, which is responsible for inverting the sample in silicon devices, is inhibited at the low temperature. When the temperature is raised at a uniform rate, traps in the upper half of the band gap begin to emit their electrons to the semiconductor conduction band (Fig. 16) and an emission current is observed to flow in the circuit as a result of the electrons being swept out of the depletion region. When the emission current ceases to flow and the traps in the upper half of the band gap are empty, generation of

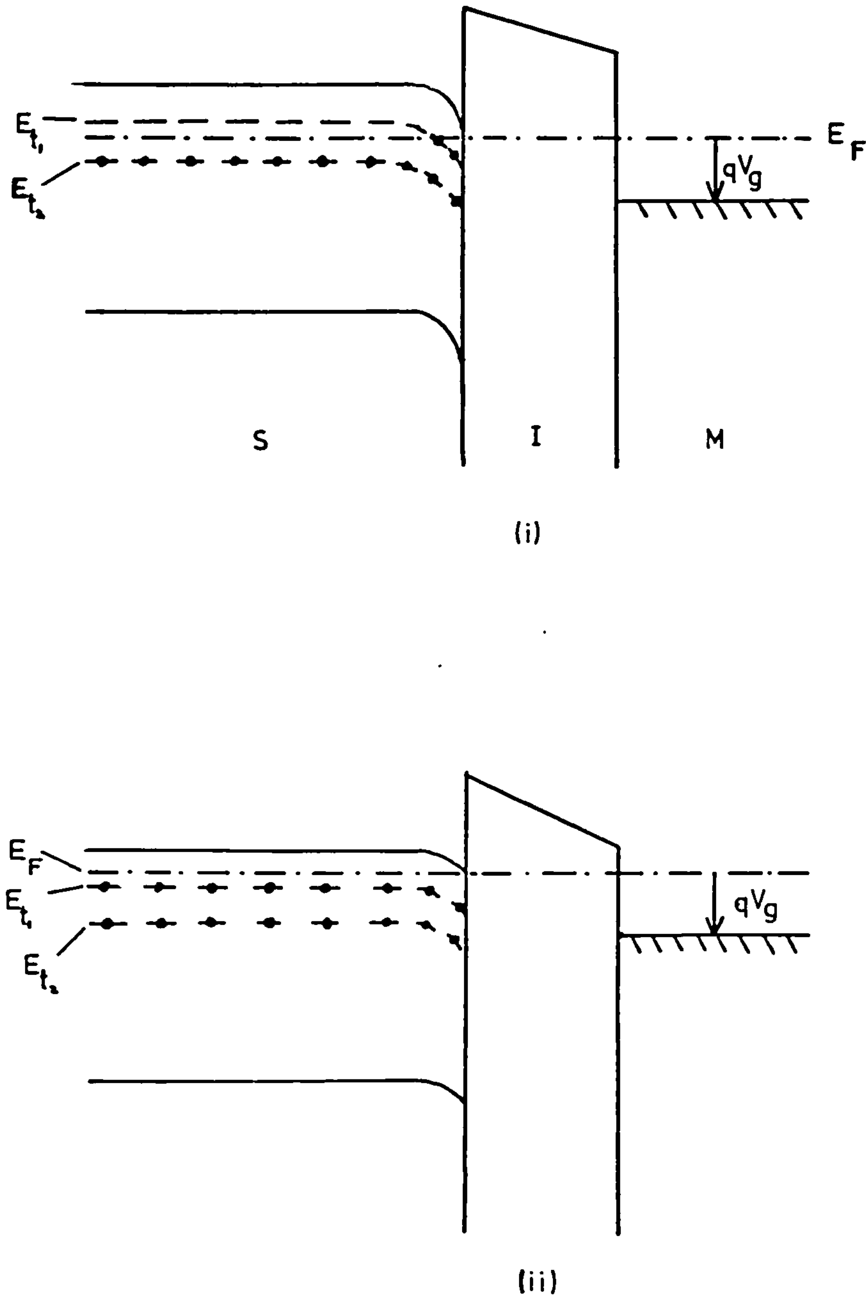


Fig.15

Energy diagram for the MIS system showing the traps in the n-type semiconductor with the system in the accumulation mode (i) at room temperature, (ii) at the initial low temperature

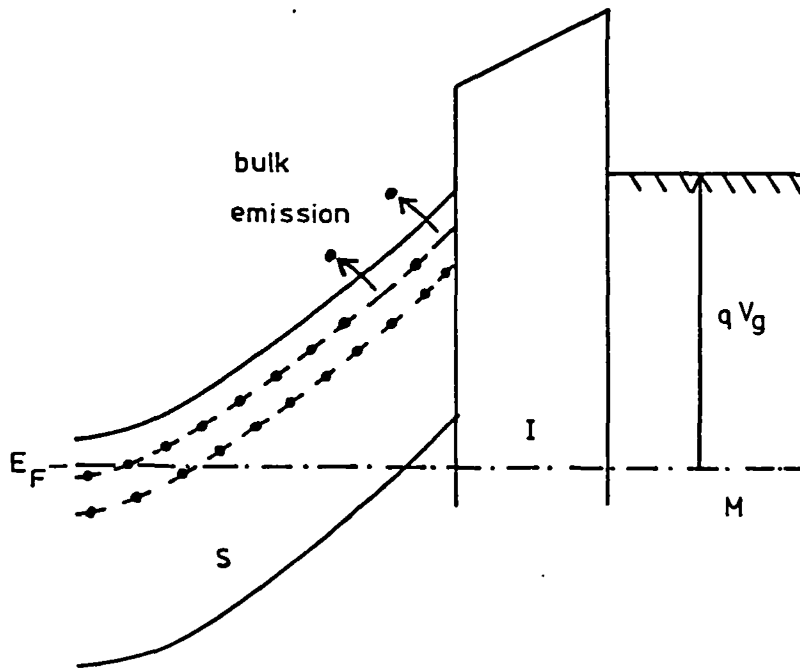


Fig. 16

Energy diagram for MIS system in deep-depletion mode showing electron emission

electron-hole pairs via these traps in the depletion region begins to be significant and a generation current is observed. The application of Shockley-Read statistics to the analysis of TSCs from bulk states is very similar in principle, to that for interface states, and no useful purpose will be served in repeating the steps here.

3.3. Energy Band Diagrams for the TFT

3.3.1. The Al-SiO_2 - CdSe - Cr System

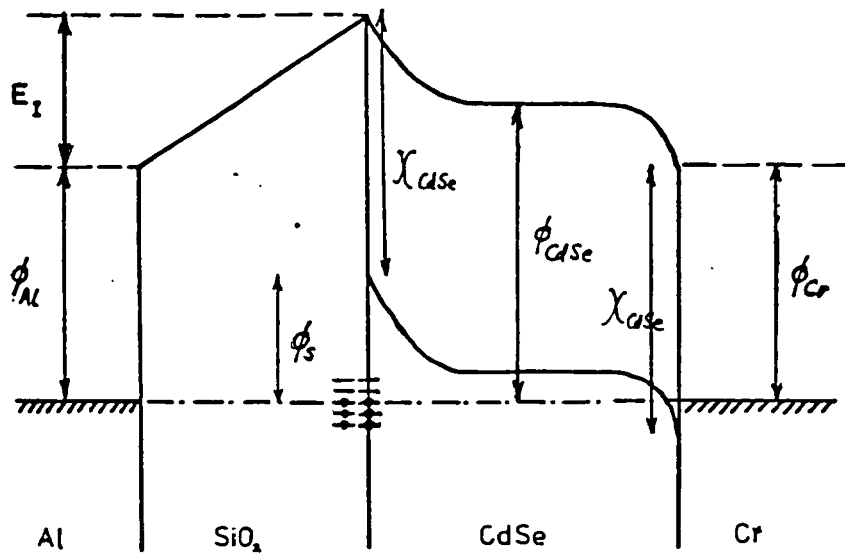
The energy diagram of the TFT with the aluminium and chromium electrodes short circuited is shown in Fig. 17(i). ϕ_{Al}, ϕ_{CdSe}, ϕ_{Cr} represent the work functions of the aluminium, CdSe and chromium films respectively. χ_{CdSe} is the electron affinity of the CdSe and ϕ_s the surface potential at the SiO_2 - CdSe interface. The states at the SiO_2 - CdSe interface are the fast states; those near the interface but inside the SiO_2 are the slow states. Slow and fast states being acceptor like states they deplete the semiconductor at the interface of free electrons. Some idea about the orders of magnitude involved may be obtained by using the results of Consigny and Madigan (section 2.1.6) that the fast states peak at 0.7 eV below the conduction band edge for the basal plane of CdSe. ϕ_s will be approximately equal to 0.7 eV; χ_{CdSe} equals 5.0 eV (14) and ϕ_{Al} varies from 3.4 to 4.3 eV (15). If E_I is the energy difference across the SiO_2, then balancing energies on either side of the insulator gives

$$E_I + \phi_{Al} = \phi_s + \chi_{CdSe} \qquad (22)$$

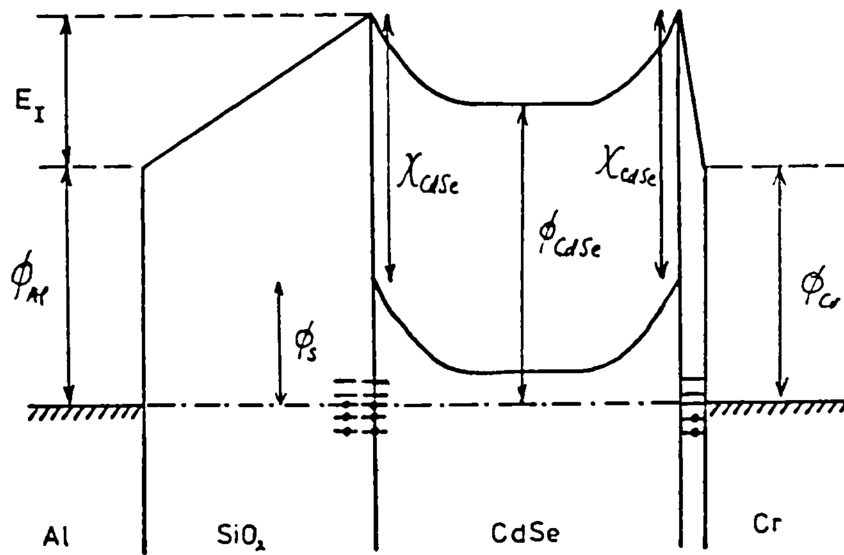
which gives E_I as varying between 1.4 and 2.3 eV. The electric field across the insulator is opposite in direction to that in the adjacent depletion region in the CdSe. A negative gate voltage must be applied before the two fields are in the same direction.

3.3.2. The CdSe - Cr Interface - "Good" and "Bad" TFTs

Fig. 17(i) shows the energy band diagram for a "good" TFT through the bulk of a CdSe crystallite i.e. away from grain-boundaries. A "good" TFT is a sample with an ohmic chromium to CdSe contact. This



(i)



(ii)

Fig.17
Energy band diagram for the (i)"good" (ii)"bad" TFT

arises because

$$\phi_{Cr} < \phi_{CdSe} \tag{23}$$

The work function of chromium, ϕ_{Cr}, is 4.4 eV (15) while that of CdSe, ϕ_{CdSe}, about 5.1 eV. Also, since

$$\chi_{CdSe} > \phi_{Cr} \tag{24}$$

degenerate conditions prevail at the CdSe surface. The ohmic contact characterises the "good" TFT, as it implies that the chromium electrode can readily supply electrons to the semiconductor as needed.

The energy band diagram for a "bad" TFT is shown in Fig. 17(ii). Here the chromium - CdSe contact is a blocking one. In the absence of interface states a blocking contact is obtained if the work function of the metal is greater than that of the semiconductor. But since this is not so in the chromium - CdSe case, depletion of the CdSe at the interface must be caused by interface states as explained by Simmons (16). Continuity between the CdSe and chromium vacuum levels is obtained by a potential drop across the interface as shown in Fig. 17(ii). The application of an increasing positive gate voltage eventually results in the transfer of charge to the semiconductor conduction band by tunneling through the potential barrier at the contact. A higher positive gate voltage would be required to fill the CdSe - SiO_2 interface traps in "bad" TFTs compared to "good" ones.

Whether the two depletion regions in the CdSe meet, depends on the magnitudes of the interface trap densities relative to that of the bulk traps - a high enough density of bulk traps may accommodate the depletion regions without complete depletion throughout the CdSe.

3.3.3. Two-Dimensional Energy Diagram for Polycrystalline CdSe

Since the grain boundary planes in polycrystalline CdSe are roughly perpendicular to the SiO_2 - CdSe interface, the topography of the different groups of traps in the TFT relative to one another is best described by reference to the two-dimensional energy diagram of Fig. 18. ABCD is the plane of the CdSe - SiO_2 interface while WXYZ and $W'X'Y'Z'$ represent two grain boundary planes. These planes define three of the four boundaries of the CdSe crystallite shown - the Cr-CdSe interface has been omitted for clarity. The contours mark depletion regions within the crystallite.

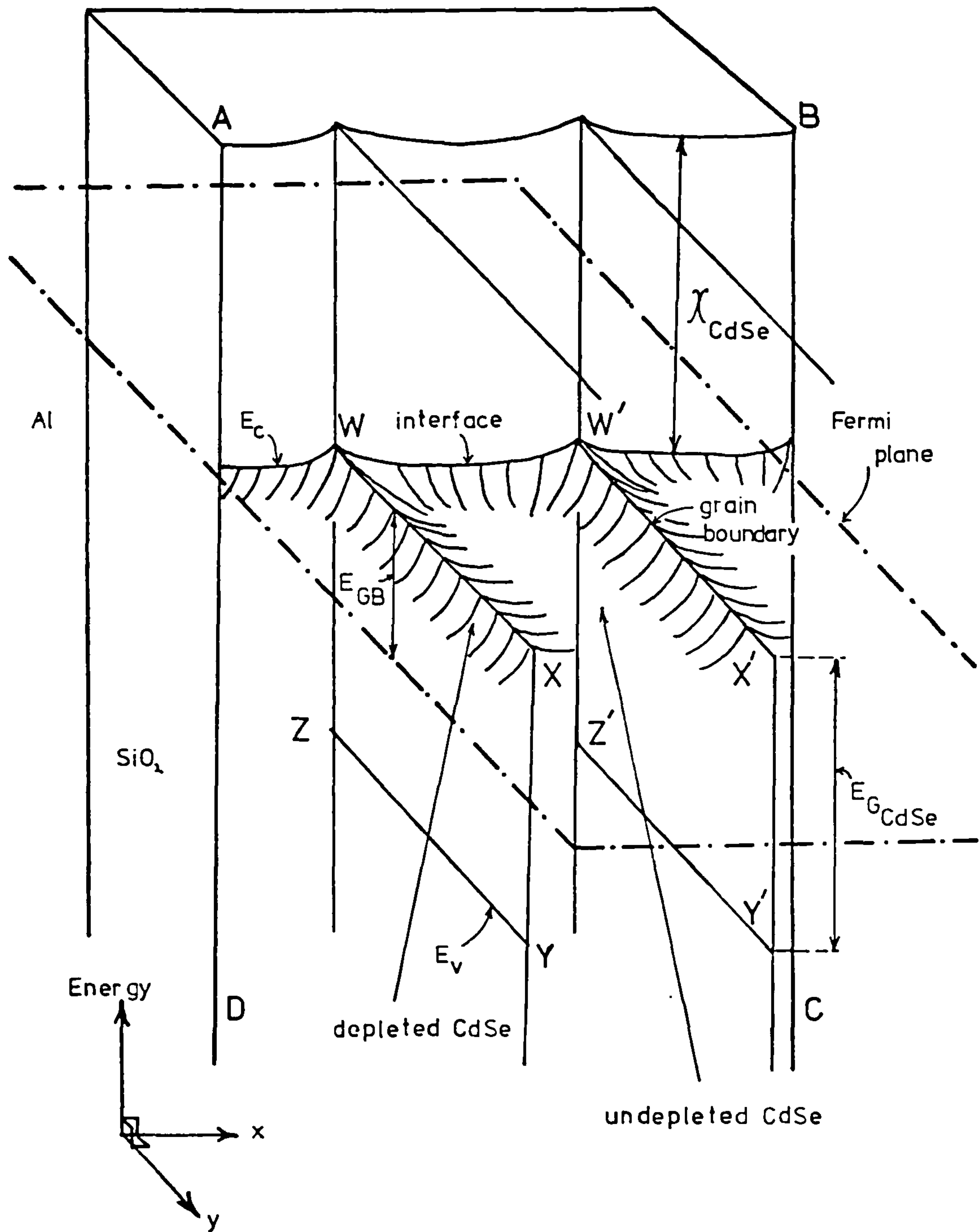


Fig. 18
Two-dimensional electron-energy diagram for TFT

3.4. Some TSC Features from TFTs

3.4.1. TSC Peaks of Slow and Fast States

Traps at the CdSe - SiO_2 interface of the TFT consist of fast traps at the CdSe - SiO_2 plane and slow ones which penetrate from 10 to 20 Å inside the SiO_2 (see Fig. 17 and Appendix A). Fast states follow Simmons' TSC theory. Electrons from slow states, however, first tunnel to a fast state and are then emitted to the conduction band. Anderson has extended the concepts of Simmons' TSC theory to include the contribution to the TSC of interface traps containing slow as well as fast states (17). Since the aim of this project is primarily one of trying to identify the multiplicity of traps present in the TFT, it is the predictions of Anderson's analysis, which may be used in identifying such TSC contributions which will be mentioned here. Anderson predicts that whereas at one value of the heating rate the contribution to the TSC of interface traps may be a single peak, if these traps contain a slow as well as a fast component, then at a different value of β, the single peak may split into two.

3.4.2. Quasi-Equilibrium TSC

A TSC peak with a maximum which occurs at a temperature independent of the heating rate was observed in the experimental results obtained. The contribution of the present work to the analysis of such a peak is in the two assumptions that the Fermi level is pinned by the trapping level and that the occupancy of the traps contributing to the TSC is determined by equilibrium Fermi Dirac statistics. The rest of the analysis is due entirely to Anderson who calls the process a quasi-equilibrium TSC one(18). He gives the current density as

$$J = 2qc\nu \exp(-E_{CD}/kT)\,(E_m I_1 - kTI_2) \qquad (25)$$

where c is the density of states in m^{-2} eV^{-1}; E_{CD} the energy of the conduction band edge from the Fermi level in eV and E_m is half the energy width of the states in eV. I_1 and I_2 are integrals. The rest of the symbols have their usual meaning. This expression gives a current against temperature plot which exhibits a current peak which occurs at a temperature independent of heating rate. Anderson predicts the shape of such a peak. There is very good agreement between the predicted and experimental peaks. Furthermore, $(E_m I_1 - kT I_2)$ is proportional to 1/T, hence plotting ln JT against 1/T for the leading edge of the peak, gives the energy of the traps, E_{CD}. Also, J falls to zero at temperature T_o when

$$E_m = 1.32\ kT_o \qquad (26)$$

Hence, knowing T_o, the spread in energy of the traps may be determined.

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CHAPTER IV. APPARATUS

4.1. Sample Preparation

The cross section of the thin-film structure of the TFT is shown in Fig. 19, while the sample viewed along the perpendicular to the plane of the thin films is shown in Fig. 20. A comparison of the dimensions of the thin films in these two figures shows that the film thicknesses have been greatly exaggerated in Fig. 19. Area ABCD in Fig. 20 would be the active area, between the gate and the source, in a TSC experiment.

The films were produced in a 19" vacuum plant containing a mask changer so that the complete TFT structure could be produced without breaking the vacuum, thus avoiding excessive contamination of interfaces between films. The liquid nitrogen trapped diffusion pump used a polyphenyl ether fluid to minimise contamination. Typical total vacuum pressures obtained during the run were in the range 2 to 7×10^{-7} Torr. Photographs of the outside and inside of the plant are shown in Plates I and II, while Plate III shows the substrate holder.

7059 glass was used as the substrate. This was first washed with detergent and water and then with IPA in an ultrasonic bath. It was then mounted on the substrate holder (see Plate III) and placed inside the plant (see Plate II) but not in the quartz station. Then pump-down commenced.

The quartz station, shown in Plate IV, was subjected to a 20 minute pre-sputtering period to clean the quartz target of any contaminants that would have been deposited on it, when the vacuum chamber was let up to nitrogen after the last run. The substrate was then moved over to the

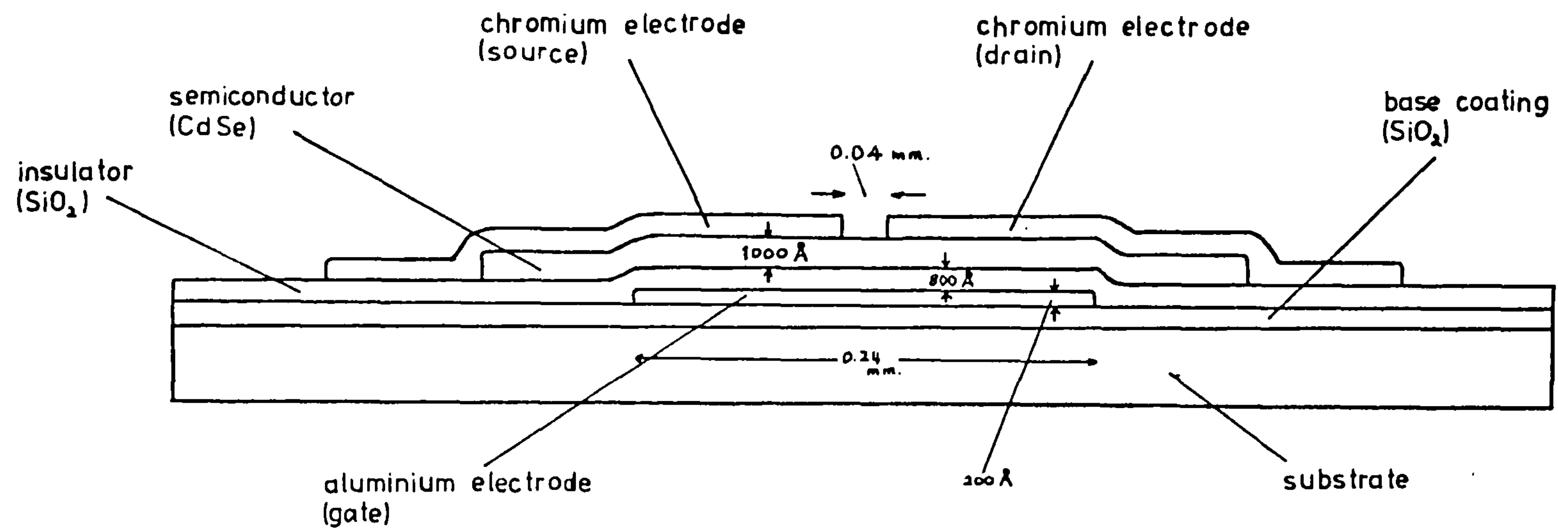


Figure 19

Cross-section of TFT

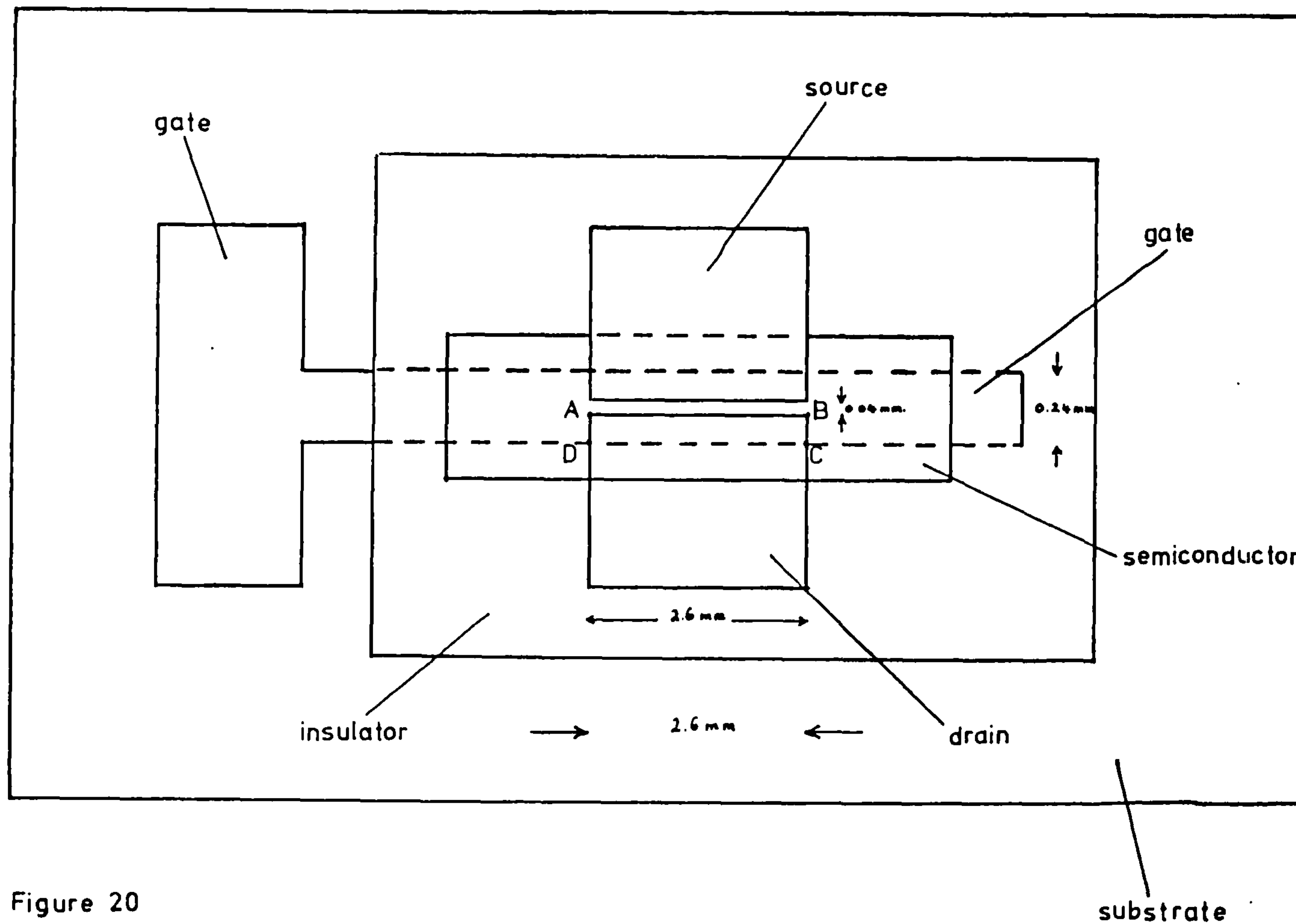


Figure 20

Top view of TFT

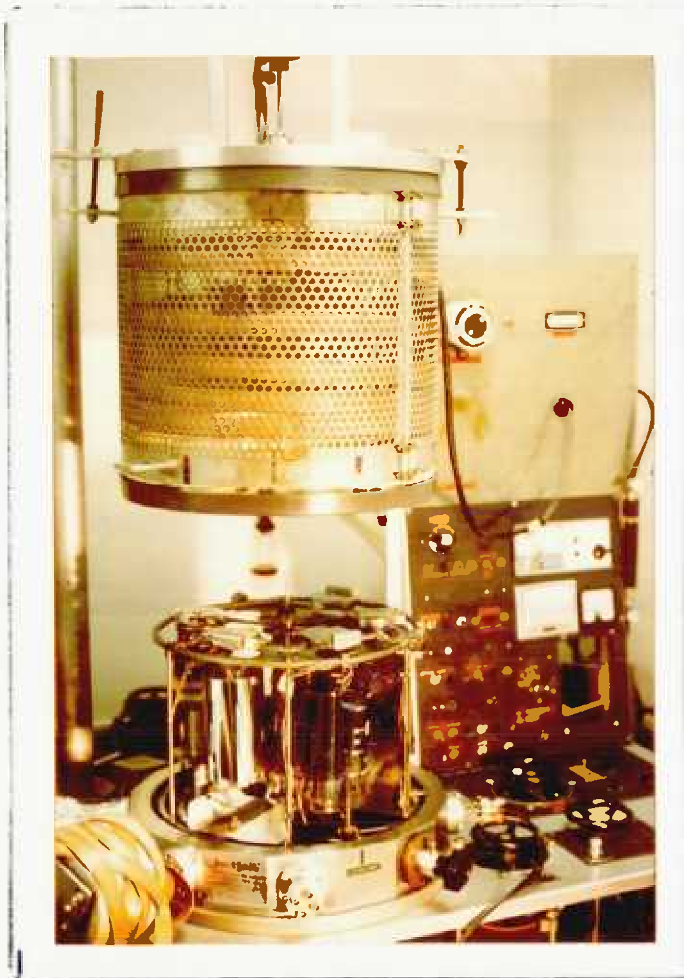


Plate I. Outside view of TFT plant.

Plate II. Inside view of TFT plant.

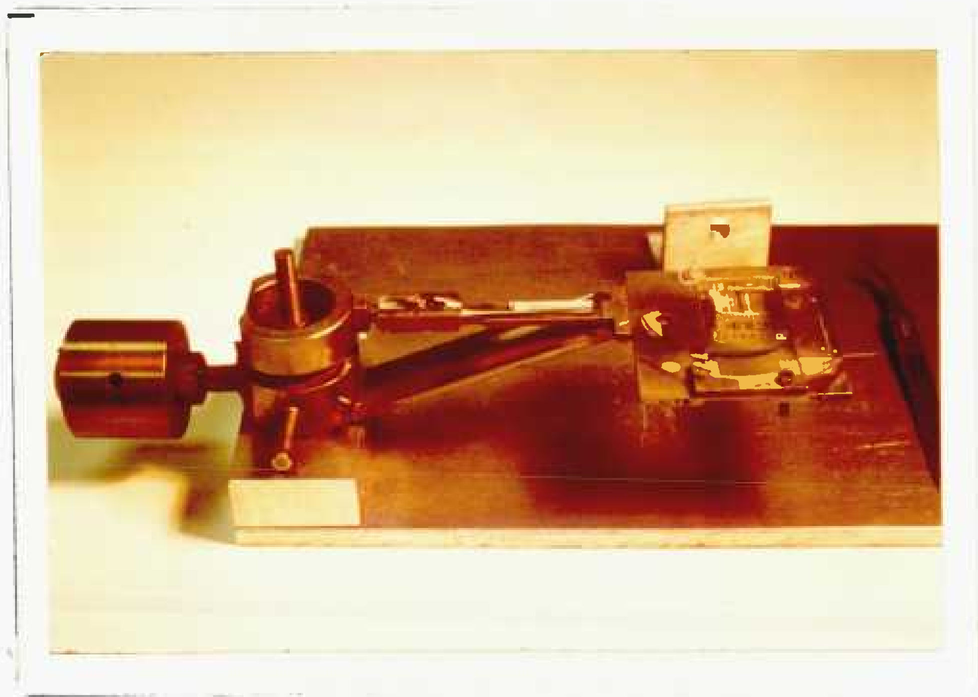


Plate III. Substrate holder.

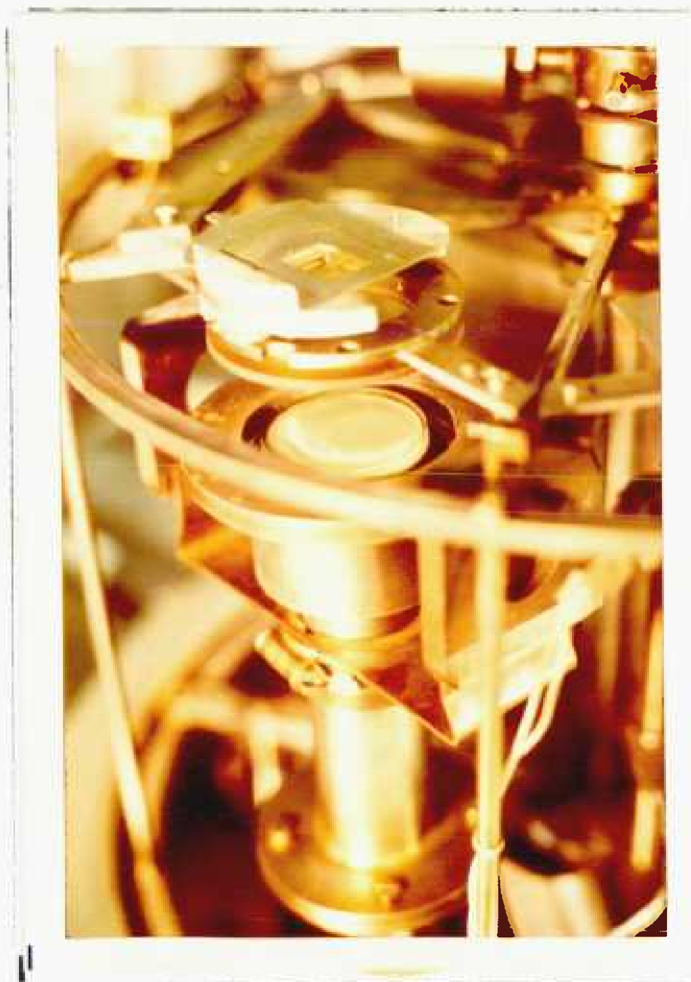


Plate IV. Quartz station.

quartz station and R.F. sputtering of the quartz target was used to deposit a base coating about 800 Å ± 100 Å thick. The deposition conditions used were those determined by Fisher (1) to give the most stable films of stoichiometric SiO_2. For this it was necessary to use a 95% argon 5% oxygen mixture for the sputtering gas in order to correct for the oxygen deficiency which occurred when pure argon was used. The sputtering gas pressure was one micron. The base coating provided a reproducible film with an uncontaminated surface for the rest of the thin-film structure of the TFT to be built on. Although the substrate was at room temperature at the start of the sputtering run, 22 minutes of sputtering raised this temperature and it was found that to produce good samples 15 minutes of cooling time had to be provided between the various deposition runs.

The substrate was then moved to the aluminium station, shown in Plate V, and aligned above the mask. The source consisted of a tungsten heater wire, about 1 mm in diameter, bent into a loop on which pieces of aluminium wire were hung and melted into a blob beforehand, to provide a degassed source of aluminium. The heater current was controlled by means of a variac. During evaporation, the thickness as well as the rate of deposition of the aluminium film was measured by means of an Edwards film-thickness monitor. The shutter between the source and the substrate was opened when the rate reached the required value.

An SiO_2 film 800 Å thick was then sputtered on top of the gate electrode under conditions identical to the sputtering of the base coating. This film was the insulator and had a resistance of about 10^{12} Ω for a typical TFT.

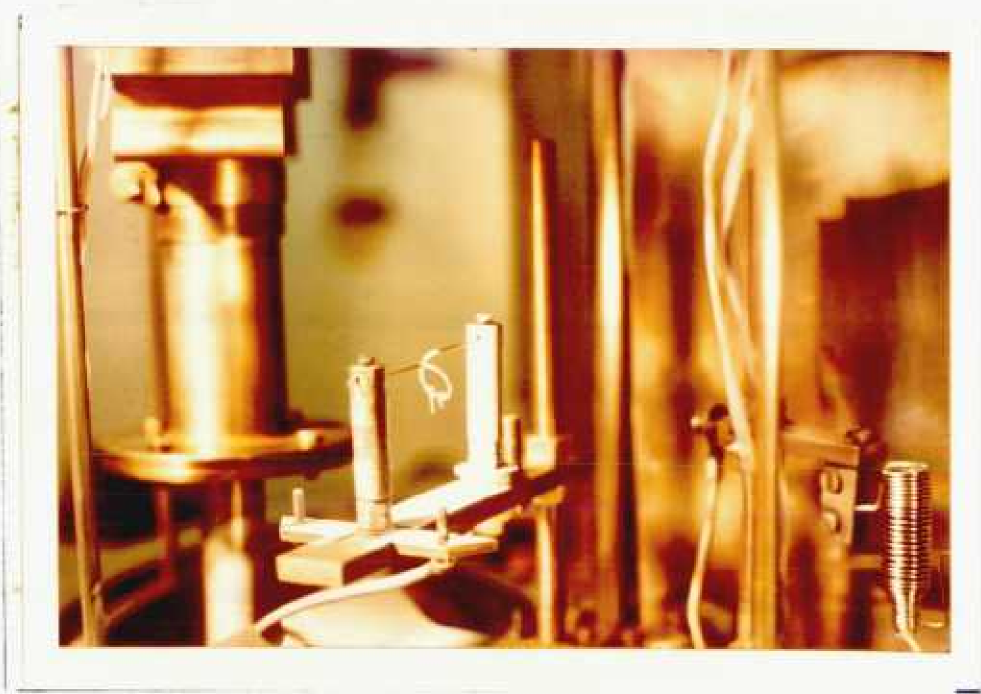


Plate V. Aluminium station.

Plate VI. CdSe station.

The CdSe film was vacuum evaporated. The source was a tantalum heated quartz crucible charged with CdSe powder and plugged with quartz wool to prevent spitting. The CdSe station is shown in Plate VI. The crucible was degassed before charging, by heating it in a separate vacuum chamber. The source to substrate distance was 15 cms. The substrate was at room temperature at the start of the evaporation. It was important to obtain and maintain an evaporation rate of 7.5 $\text{Å}\ s^{-1}$ for good working TFTs. The thickness of the film was 1000 ± 100 Å.

Using gold or chromium for the source and drain electrodes gave ohmic contact to the semiconductor, but it was found that chromium was the most reliable. Chromium does not scatter very much around the wire used as the mask to produce the source-drain gap, whilst the use of gold gave a poorly defined gap unless the mask wire was in perfect contact with the CdSe surface. The chromium was deposited by vacuum evaporation. The source used was a commercially available tungsten rod (acting as the heater) covered with chromium.

Due to the masks used, ten transistors could be produced on one substrate. The as-deposited samples had poor transistor characteristics. When annealed at 390°C for one and a quarter hours, however, the characteristics improved. The temperature profile the TFT was subjected to is shown in Fig. 21. The furnace used is shown in Plate VII. The annealing gas was dry oxygen-free nitrogen. The sample was placed next to the thermocouple junction in the furnace and the temperature taken up to about 125°C and kept there for half an hour while nitrogen was continuously flushed through the furnace. This was to remove water vapour from the inside walls of the furnace. The temperature was then taken up to 390°C (± 20°C) while the rate of nitrogen flow

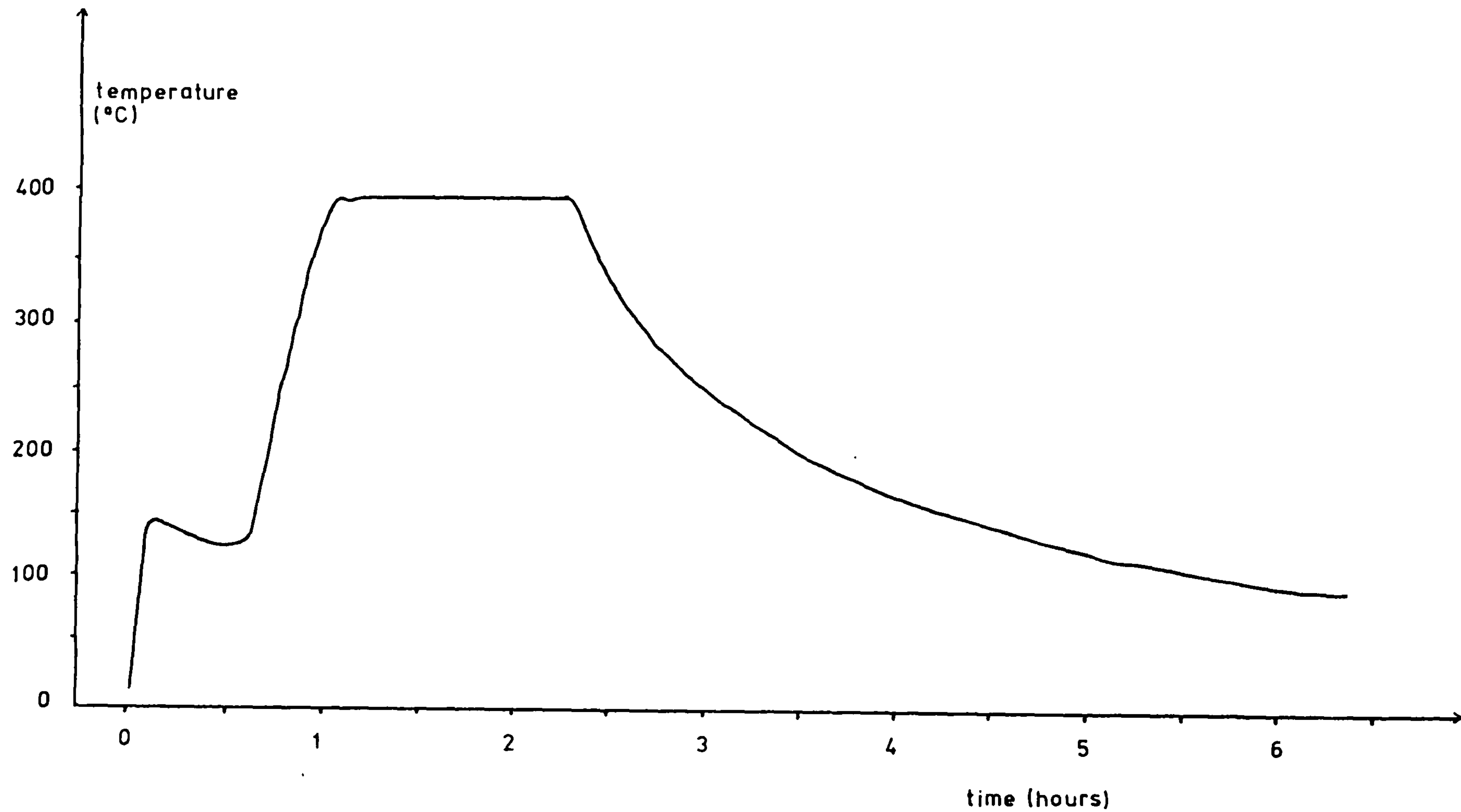


Fig. 21

Temperature anneal cycle for TFT

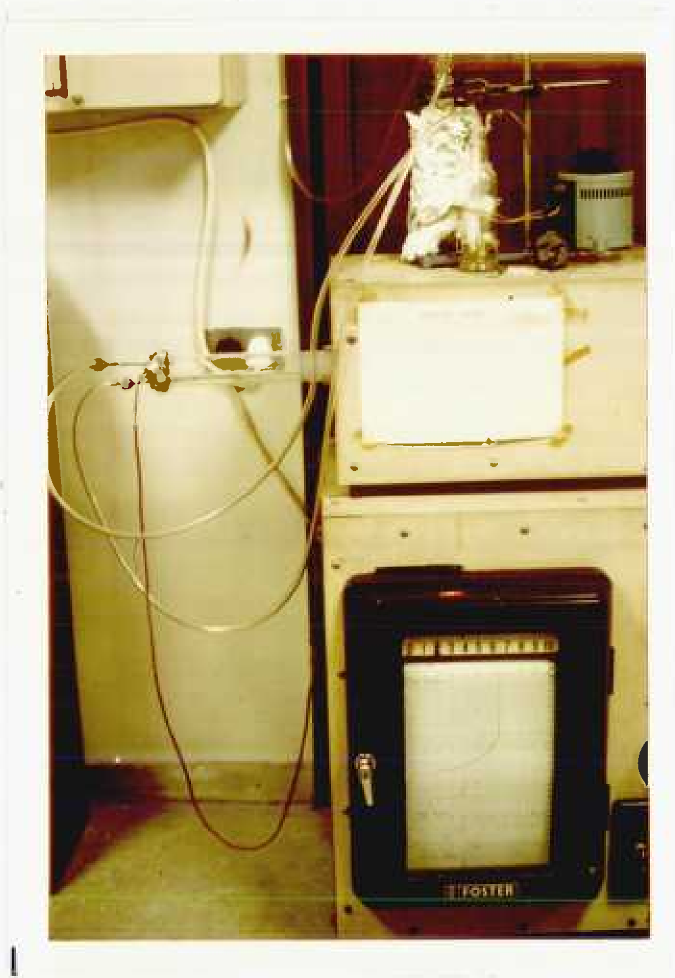


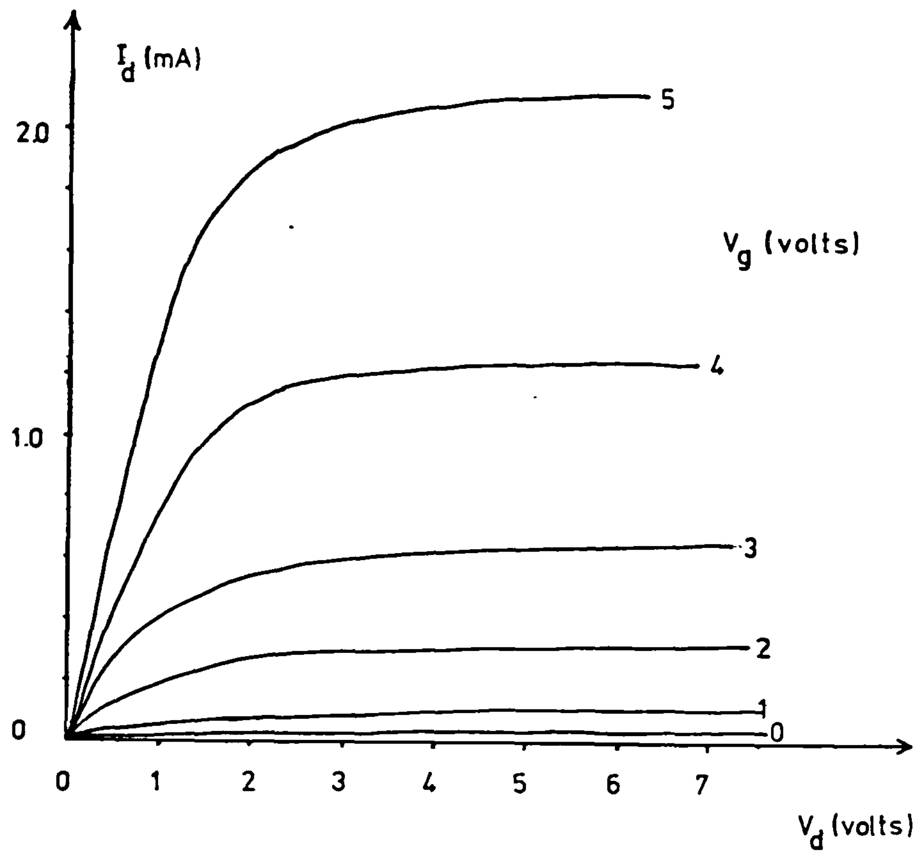
Plate VII. Furnace for annealing TFTs.

was reduced. This high temperature anneal was followed by a slow cool.

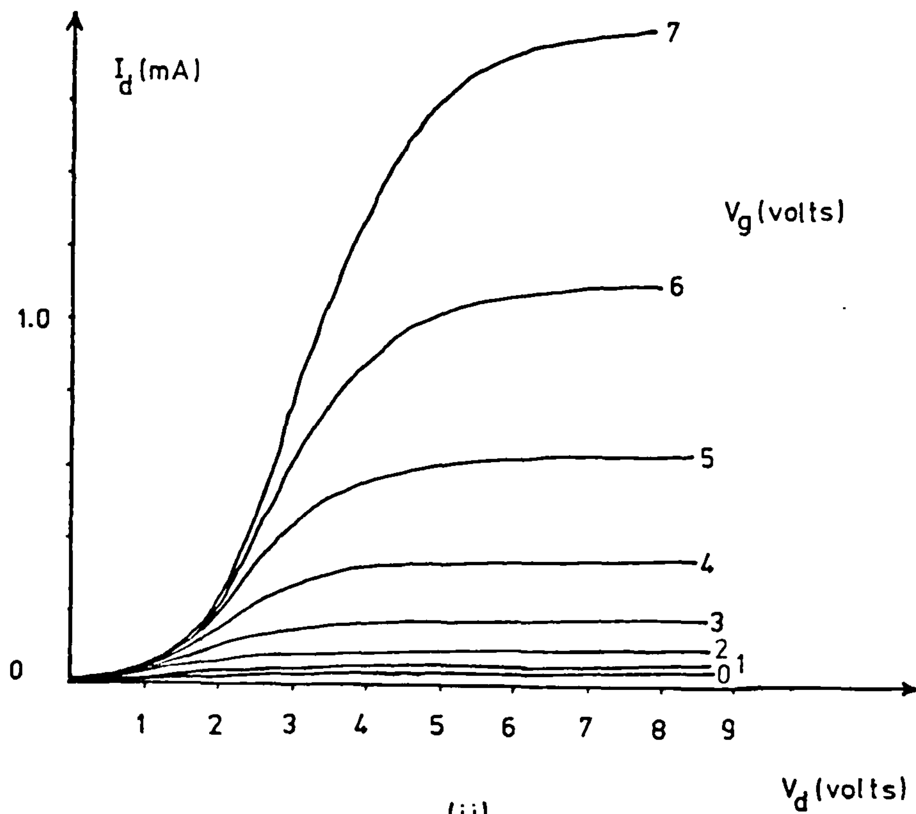
The substrate was then broken up into individual transistors using a specially designed substrate holder which enabled the scribing of the substrate between transistors by a diamond tipped scriber, without bringing pressure to bear on the adjacent transistor by the ruler used to direct the cut. Such pressure would have damaged the TFT.

The transistor characteristics of the TFTs were then obtained using a transistor curve tracer which gave the variation in the source to drain current, I_d, with the source to drain voltage, V_d, while the gate voltage, V_g (with respect to the source) was kept constant. A family of such curves was obtained by varying the gate voltage (see Fig. 22). The TFTs which had transistor characteristics as in Fig. 22(i) had source and drain electrodes making ohmic contact to the semiconductor - these were classified as "good" TFTs. Those having characteristics shown in Fig. 22(ii) had source and drain electrodes making blocking contact to the semiconductor and were classified as "bad" TFTs.

The active area of each sample was measured using a travelling microscope. A length of thin silver wire was then attached to each of the three electrodes, using silver dag, and when the dag had dried, the contacts were checked to ensure they adhered to the electrodes well.



(i)



(ii)

Fig 22

TFT characteristics for (i) ohmic (ii) blocking source-drain contacts

4.2. TSC Apparatus

The TSC apparatus had to measure the TSC flowing between the two electrodes of the sample and record it against its temperature, while the temperature of the sample was raised at a uniform rate from a low temperature.

4.2.1. The Cryostat

This was a vacuum chamber where the sample could be housed. Details of its construction appear in Fig. 23 and Plate VIII shows the inside of the chamber. The lowest pressure was about 6 microns when the rotary pump was used alone and lower when the diffusion pump was brought into the vacuum circuit. It was found convenient to use the rotary pump alone.

The volume inside the chamber was kept at a minimum, and the connecting copper tubes in the vacuum circuit as short as possible in order to minimise pumping time. Care was taken to eliminate leaks because otherwise, since the sample could be kept at low temperatures for long periods of time during the course of an experiment, the water vapour in the air leaking in would condense into a layer of ice on the sample.

A thin layer of ZnO paste was smeared on the bottom of the TFT substrate and pressed against the sample holder (see Fig. 23). The ZnO paste had a high thermal conductivity and high electrical resistivity and its purpose was to conduct heat to or away from the TFT quickly; to establish a low thermal gradient between the TFT and the sample holder; to keep the TFT in place in contact with the sample holder.

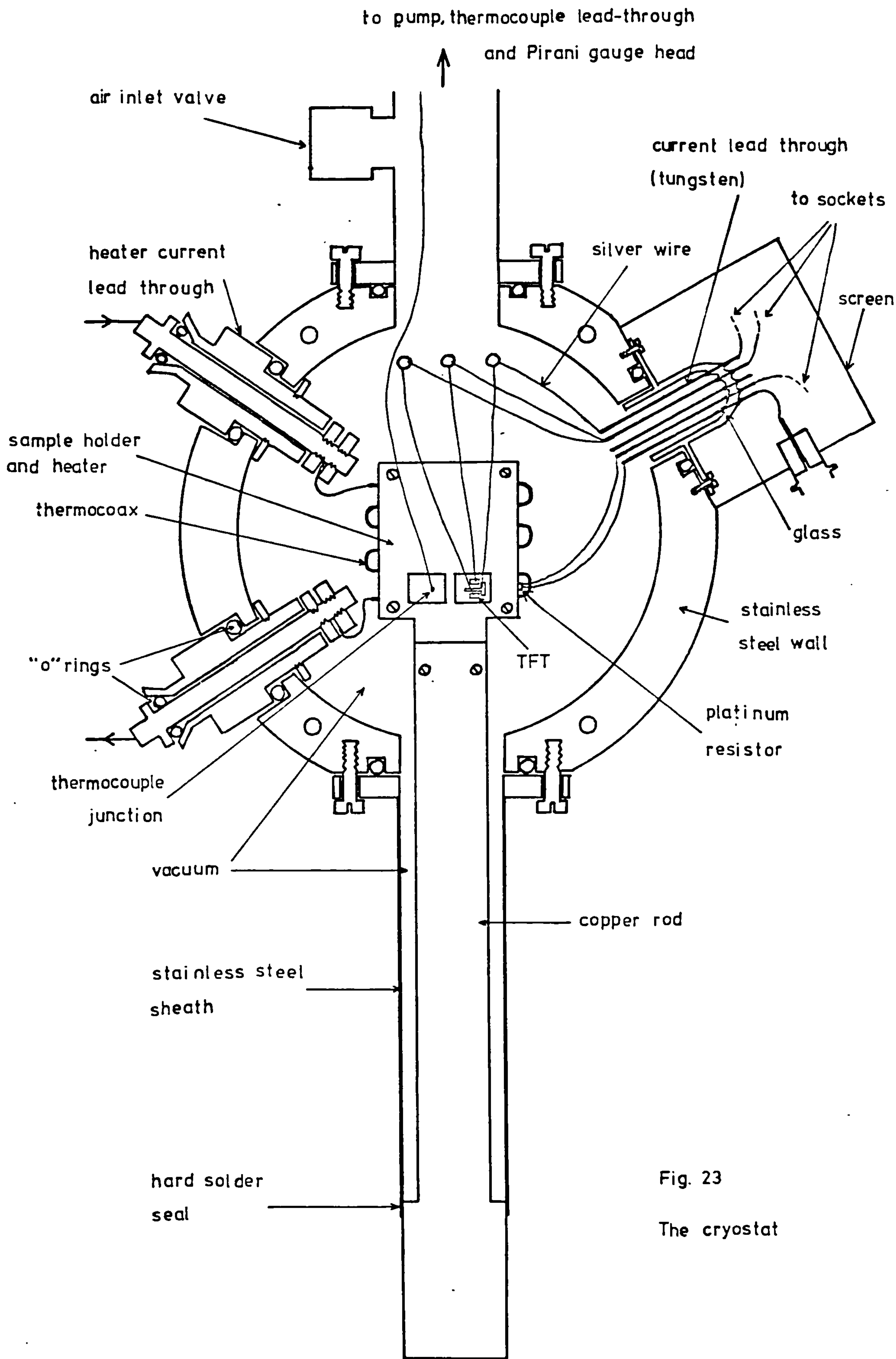


Fig. 23

The cryostat

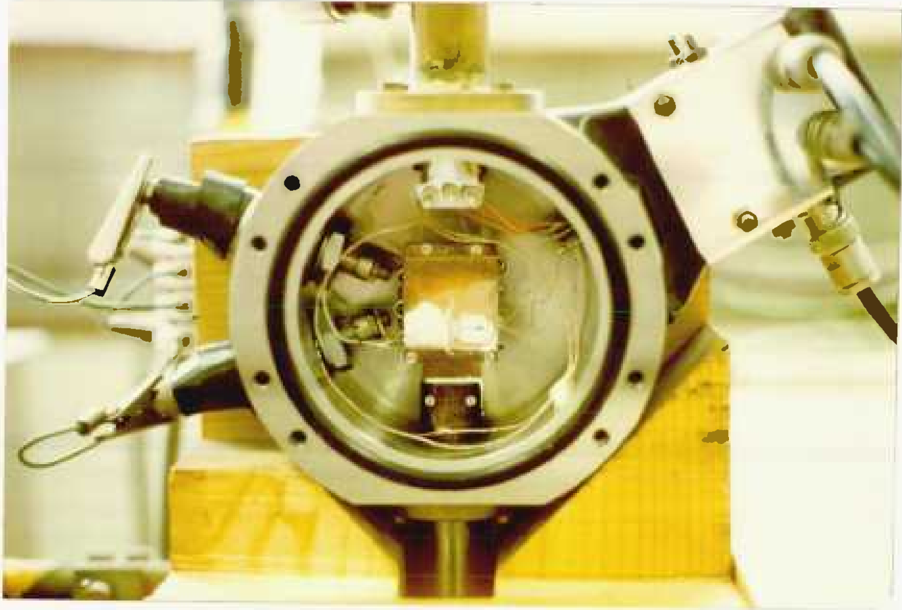


Plate VIII. The cryostat.

Plate IX. Cryostat and electrical instruments.

The sample holder consisted of two slabs of copper containing grooves through which the heater wire was threaded. ZnO paste was used to provide good thermal contact between the heater wire and the copper. The surfaces of the individual copper slabs were made as flat as possible to ensure good thermal contact, with the minimum amount of ZnO paste, when the slabs were screwed together. Also, the maximum number of grooves-compatible with the bending of the heater wire without breaking it - was used, to ensure a uniform value of temperature over all the surface of the sample holder.

The heater wire used was Philips thermocoax. It consisted of an inner conductor of nichrome wire of 12 Ωm^{-1} resistance. This carried the A.C. heating current. The resistance of the wire used in the cryostat was 7Ω. This inner conductor was insulated from an outer metal sheath by MgO. The thermocoax could be bent easily. The MgO being in intimate contact with both the inner conductor and the sheath, and the latter with the copper sample holder, ensured a faster response time for the temperature of the sample holder to changes in the heater current, than if other heater systems had been used. Another advantage of using thermocoax was that the sheath could be grounded. This was vital for making satisfactory TSC measurements, because the magnitude of the TSC is usually small and since it flows while the heater current is flowing, which is A.C., the heater current must be screened to prevent it interfering with the TSC. It was found that excellent screeening was provided by grounding the outer sheath of the thermocoax. Care was taken not to short circuit the inner conductor to the sheath at the two ends of the thermocoax, where the inner conductor

was bare. The heater current was carried in and out of the cryostat by standard Edwards current lead-throughs.

The sample holder fitted into a groove cut into the copper rod shown. The end of this rod was exposed and came into contact with the liquid nitrogen used to cool the sample holder. The exposed part of the rod had a large enough surface area to ensure quick cooling of the sample holder from room temperature to - 196°C in about thirty minutes. Copper was chosen where the quick transfer of heat was required because of its high thermal conductivity. The copper rod was hard soldered onto a stainless steel sheath. Hard rather than soft solder was used, because it gave a mechanically tougher, leak free joint, and enabled it to be cooled to a lower temperature, without it falling apart due to the larger discrepancy between the coefficients of contraction of the materials and the solder at the joint. The sheath did not touch the copper rod above the seal. Hence, after pump-down, a vacuum existed between the copper and the sheath, which minimised heat transfer between the two - this could occur by radiation but not convection. This meant that once the sample holder and the copper rod had been cooled, they would be kept at a low temperature with the minimum volume of liquid nitrogen being boiled off. Also, the temperature of the sample holder could be raised slowly i.e. - the rate of increase of temperature could be controlled by the heater current rather than the heat losses from the copper to the outside. The latter case would have given an unacceptably high rate of increase of temperature. The design enabled heating rates as low as one degree per minute to be obtained. Stainless steel was chosen as the sheath material because of its bad thermal conductivity.

This, together with the fact that the sheath wall was made as thin as possible (0.5 mm), resulted in preferential heat conduction along the copper rod, rather than the sheath, resulting in a lower consumption of liquid nitrogen.

The silver wires from the TFT were taken to stand off pins. These were silver plated pins insulated from the rest of the cryostat by PTFE. Contact was made using silver dag. The source and drain wires were connected together and the TSC measured between the source/drain and the gate electrodes. The pins were connected to tungsten current lead throughs which were in turn connected to the rest of the electrical circuit. There were five tungsten current lead throughs. Two of these carried a constant current of 1 mA from a temperature control unit, outside the cryostat, to a platinum resistor embedded in the copper slab directly underneath the TFT. This resistor came in a ceramic sheath and ZnO paste was used for good thermal contact between the ceramic and the copper. It was possible to determine the temperature of the copper sample holder knowing the resistance of this platinum resistor.

To measure the temperature at other points, three thermocouple junctions were introduced into the chamber. These could measure temperature to within $\pm 0.5^{o}$. By placing these junctions at various points on the surface of the copper sample holder it was found that the temperature was uniform throughout this surface. The lowest temperature reached by the sample holder was the boiling point of liquid nitrogen of $77^{o}K$. To measure the temperature of the actual TFT, however, a dummy sample was used with a thermocouple junction pressed firmly against and in good thermal contact with its upper surface.

It was found that the lowest temperature reached by the TFT was 110°K, giving a temperature lag of 33°K across the substrate. The accurate measurement of temperature was made possible by the introduction of the thermocouples into the vacuum chamber of the cryostat, without breaking the thermocouple wires. This was done by passing the thermocouple wires through alumina tubes and using Araldite to try to seal both ends of the tubes. The Araldite did not form a leak free seal with the insulating sheath of the thermocouple wires. To seal the leaks, molten tar (black Apiezon wax) was poured on top of the Araldite seals, while the cryostat vacuum chamber was being pumped. The molten tar was thus sucked into the cracks and solidified to give a permanent seal. A reference junction was used in the thermocouple circuit and kept in melting ice. The thermocouple output voltage was measured using a datron digital voltmeter.

The lid of the vacuum chamber had an optical window of quartz 3mm thick (see Plate IX). It allowed light to be shone on the sample. When experiments had to be carried out in the dark, the quartz window was replaced by a dural disc. The cryostat was constructed so that the sample could be mounted with the plane of its thin films along the vertical. This made the shining of light on the sample easier. Also, if Hall effect measurements were needed to be made, the cryostat would easily fit between the pole pieces of the electromagnet with the plane of the sample perpendicular to the magnetic field. The dimensions of the cryostat were made as small as possible, to enable the maximum and most uniform magnetic field to be obtained by having the pole pieces of the magnet as close together as possible. One

of the reasons for the choice of stainless steel as the cryostat material was because, it was only very mildly magnetic and would not interfere with Hall effect measurements. It was later decided, however, not to carry out Hall effect experiments.

The cryostat was light proof.

4.2.2. The Electrical Circuit

The electrical circuit used is shown in Fig. 24 and Plate IX. It consisted of the TFT in series with a power supply and a Keithley electrometer. The power supply consisted of a series of batteries and the voltage they could provide could be varied in steps of 1.6V. Since the magnitude of the TSC could be small, noise had to be minimised. Batteries were used because they were more stable and noise free than other power supplies available.

The Keithley electrometer used was either a 616 digital one, or the 602 model. Since the magnitude of the TSC was always less than 10^{-6} A, the electrometer was always used in the fast mode. The TSC was measured between the HI and the LO input terminals of the electrometer i.e. floating measurements were made.

The output terminals of the electrometer were connected to the y-axis of a chart recorder which enabled the electrometer readings to be recorded against time or temperature. The temperature signal could be provided by the thermocouple output fed into the x-axis of the recorder. The various units of the circuit were connected together using short coaxial cables. The entire circuit carrying the test signal was screened and grounded to eliminate interference. The grounding was only at one point to avoid ground loops which could carry currents which would upset the test signal.

The temperature of the sample was controlled using a Stanton Redcroft temperature controller model 681. This could provide

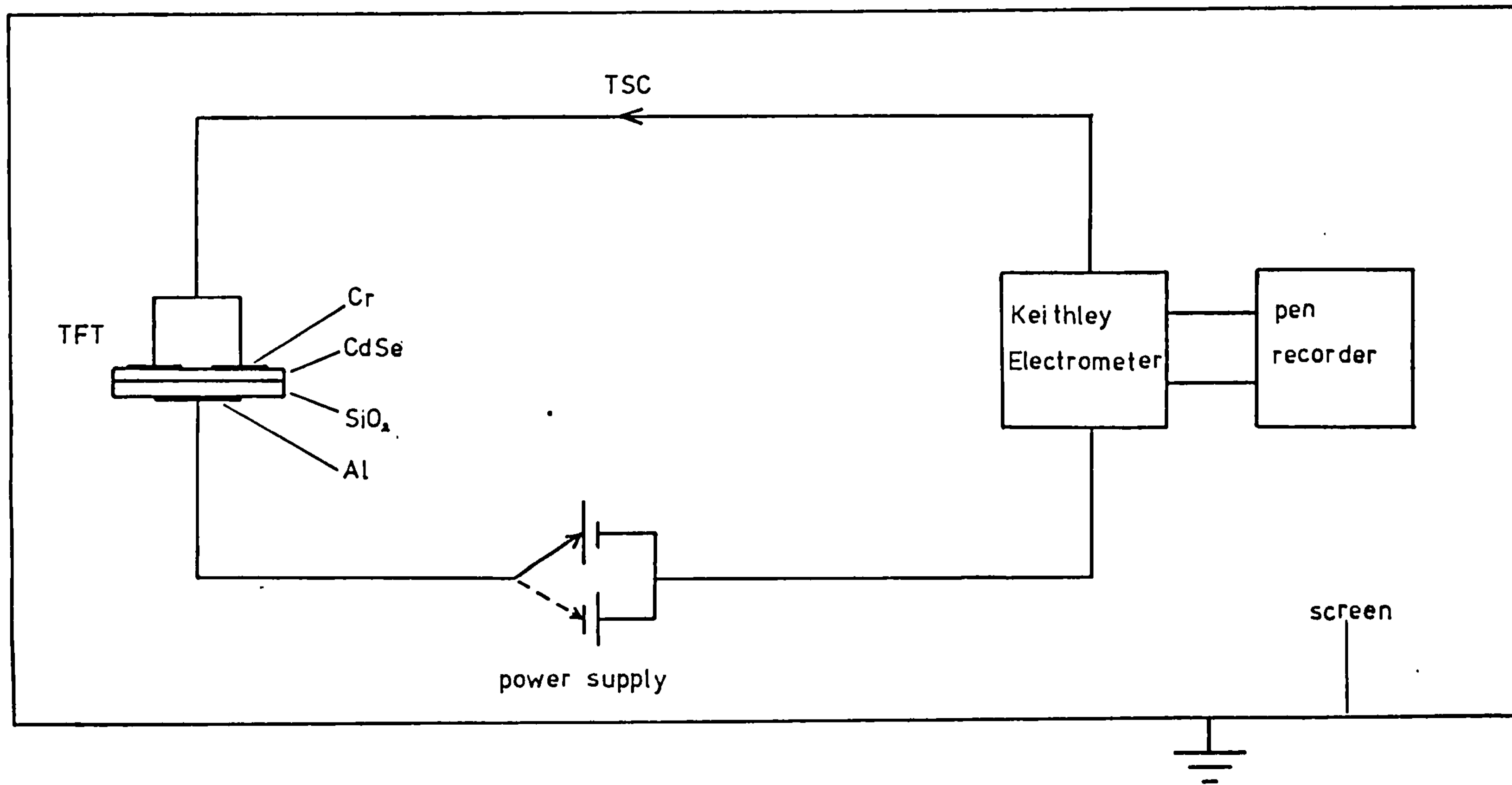


Fig. 24

Circuit for TSC measurements

temperature ramps of 1, 2, 3, 4, 5, 6, 10, 15 and 20° min^{-1} with an accuracy of ± 0.5^{o}.

4.2.2.1. The Electrometer

The electrometer is an instrument that can measure low currents. The heart of the electrometer is an operational amplifier with an input bias current which is much smaller (say less than 5%) of the current to be measured and an open loop gain of the order of 10,000. Hence, the input bias current determines the limit of the magnitude of the minimum current that can be measured without introducing too large an error.

Two techniques exist in making low current measurements, each involving a different circuit - the shunt-type circuit (electrometer in normal mode) and the feedback-type circuit (electrometer in fast mode). The relevant circuits are shown in Figs. 25 and 26. The feedback-type circuit was used to make fast electrometer measurements of TSC because, for the magnitude and the time dependent nature of the TSC measured, this method had two advantages over the shunt-type method (2). The first concerns the input resistance of the electrometer. For the shunt-type, this is of the same order of magnitude as the reciprocal of the TSC; for the feedback-type it is the reciprocal of the TSC divided by the gain of the amplifier which is of the order of 10,000. Hence, the input resistance of the electrometer in feedback-type measurements is much less than in shunt-type ones. But TSCs of the order of 10^{-11} A are common, implying an input resistance of 10^{11} Ω for the shunt-type but only 10^{7} Ω for the feedback-type electrometer. This means that insulation requirements in connecting cables and contacts do not have

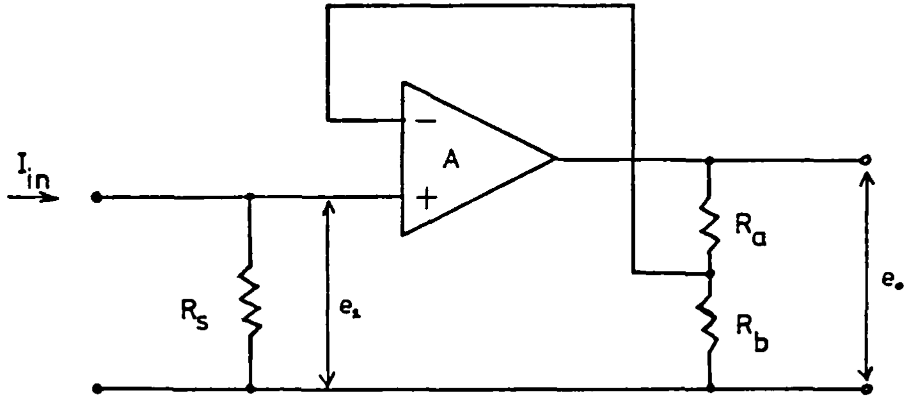


Fig. 25
Electrometer circuit for shunt-type("normal") measurements

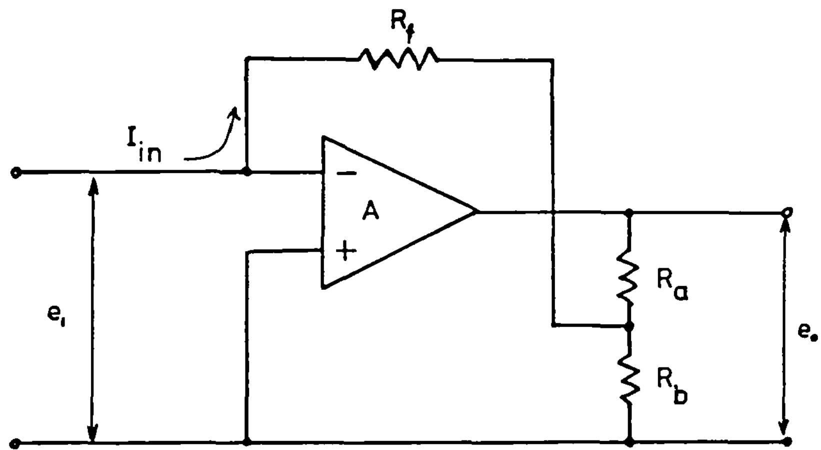


Fig. 26
Electrometer circuit for feedback-type("fast") measurements

to be stringent if the feedback-type electrometer is used, because then, the input resistance of the instrument is much less than the insulation resistance. Secondly, since the TSC is usually rich in structure i.e. it varies with time, the electrometer used must have a low response time to record changes in the TSC. The feedback-ype circuit has a shorter response time than the shunt-type one, hence the term fast mode.

For the instrument used, the response time in the fast mode is obtained by multiplying the value of the feedback resistor, R_f, by 1 pF i.e. the response time varies from 0.1 s (when the instrument reads 10^{-11} A full scale deflection) to 10^{-6} s (when it reads 10^{-6} A full scale deflection). The reciprocal of R_f is the full scale deflection of the instrument - the derivation of this and further details of the analysis of the electrometer circuit appear in Appendix E.

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CHAPTER V. RESULTS AND ANALYSIS

5.1. Annealing of CdSe Films

5.1.1. Sample Preparation

The effect on the size of grains, in polycrystalline films of CdSe, of annealing for different lengths of time, was investigated using the electron microscope. The films were deposited under conditions identical to the preparation of TFTs, except that no mask was used, which resulted in a continuous layer of CdSe on SiO_2, and the thickness of the CdSe was 400 Å instead of 1000 Å, because films thicker than 400 Å did not give good transmission electron micrographs with well defined grains. The sample was then cut up into smaller pieces approximately 5 mm square. Each piece was then annealed for different lengths of time. The temperature profile was identical to that used for normal TFTs.

The samples were then suspended in an atmosphere of hydrofluoric acid vapour. The acid fumes attacked the SiO_2 by penetrating through the sides of the CdSe film or through grain boundaries in the CdSe, diffuse enough to allow the penetration. The time taken to free the CdSe was of the order of several minutes in the case of as-grown (unannealed) films, but hours in the case of annealed ones. This indicated that annealing improved adhesion between the CdSe and SiO_2, or cohesion between CdSe grains, or both.

When the SiO_2 was etched, the CdSe film was floated in a dish of distilled water. It was found to have broken up into smaller islands, the edges of which marked the grain boundaries penetrated by the acid. These islands were picked up on electron microscope grids and allowed to dry. The transmission electron micrographs and electron diffraction patterns of the films were then obtained using

the electron microscope.

5.1.2. Results

Plates X to XII show the electron diffraction patterns. The transmission electron micrographs in Plates XIII to XX clearly show the polycrystalline nature of the films and the grain boundaries between the individual grains are visible.

Plates XIII and XVII show the grains in the unannealed films. Plate XIII shows that grains do not exceed about 200 Å in size. Plate XVII is much sharper than XIII and the unannealed crystallites are more clearly defined. From Plate XVII the typical size of unannealed crystallites is seen to be around 150 Å. Annealing for $1\frac{1}{4}$ hours results in an increase in the size of the grains as shown in Plate XIV. A histogram showing the crystallite size distribution was drawn for the film in Plate XIV. The histogram appears in Fig. 27. The crystallite size was taken as the mean of the longest and shortest distance across a crystallite. The accuracy with which the crystallite size could be determined was ± 50 Å. It can be seen that, although crystallite size varies from about 100 to over 1000 Å, the histogram peaks at a crystallite size of 200 Å and the mean size is given by

$$\frac{\Sigma \text{ (number of crystallites x crystallite size)}}{\Sigma \text{ (number of crystallites)}}$$

$$= 300 \text{ Å}$$

What looks an assymetrical distribution curve, referred to as skew, becomes approximately a normal curve when the frequency (the number of grains in this case) is plotted against the logarithm of the variable rather than the variable. Such a distribution is called a lognormal distribution. In plotting such a distribution it is convenient to use

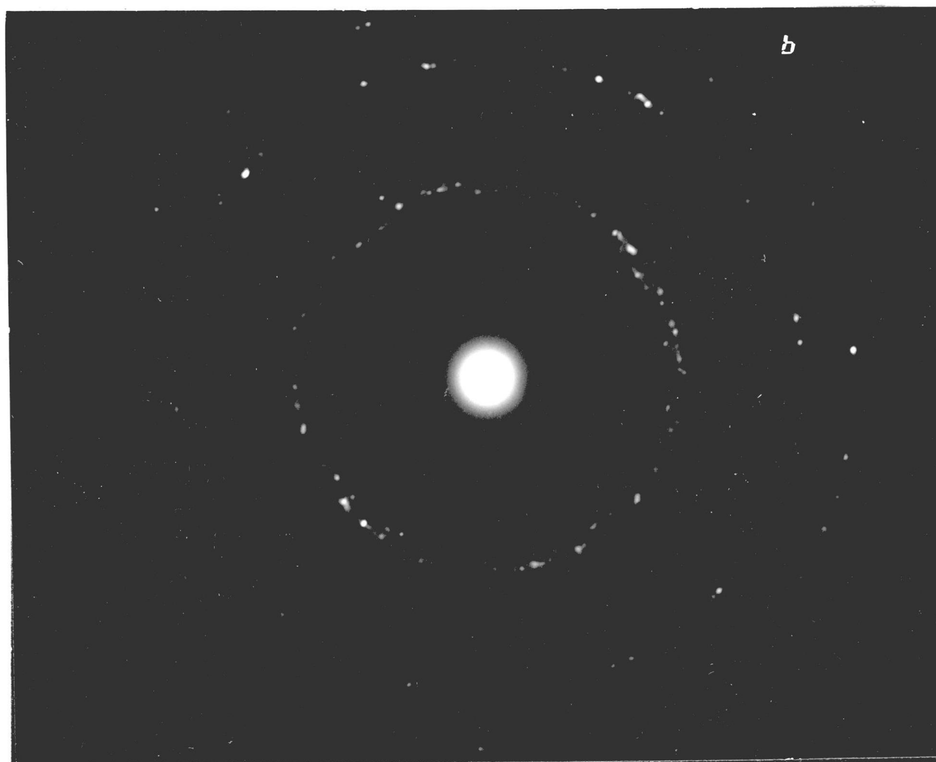


Plate X. Electron diffraction pattern for unannealed CdSe film.

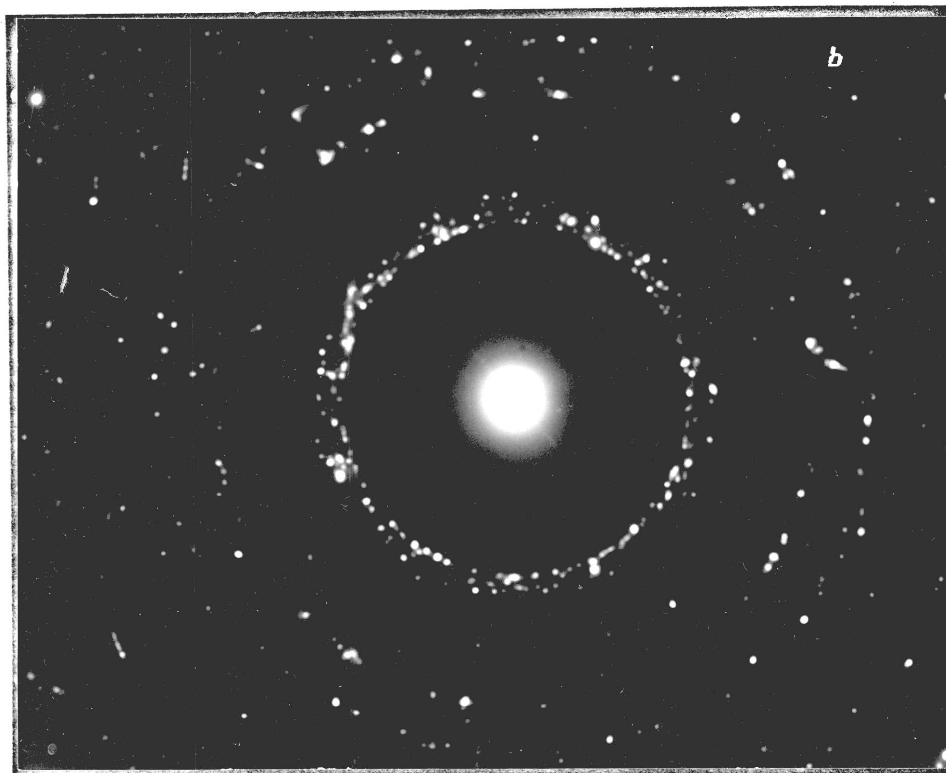


Plate XI. Electron diffraction pattern for CdSe annealed for $1\frac{1}{4}$ hours at $395^{\circ}C$.

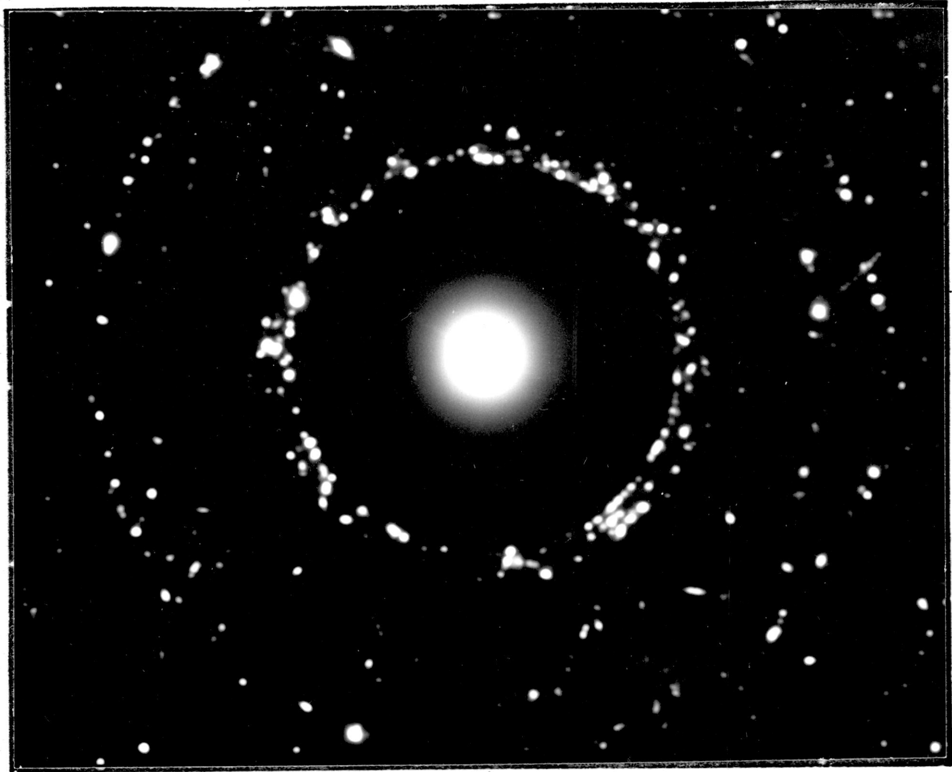


Plate XII. Electron diffraction pattern for CdSe annealed for 93.5 hours.

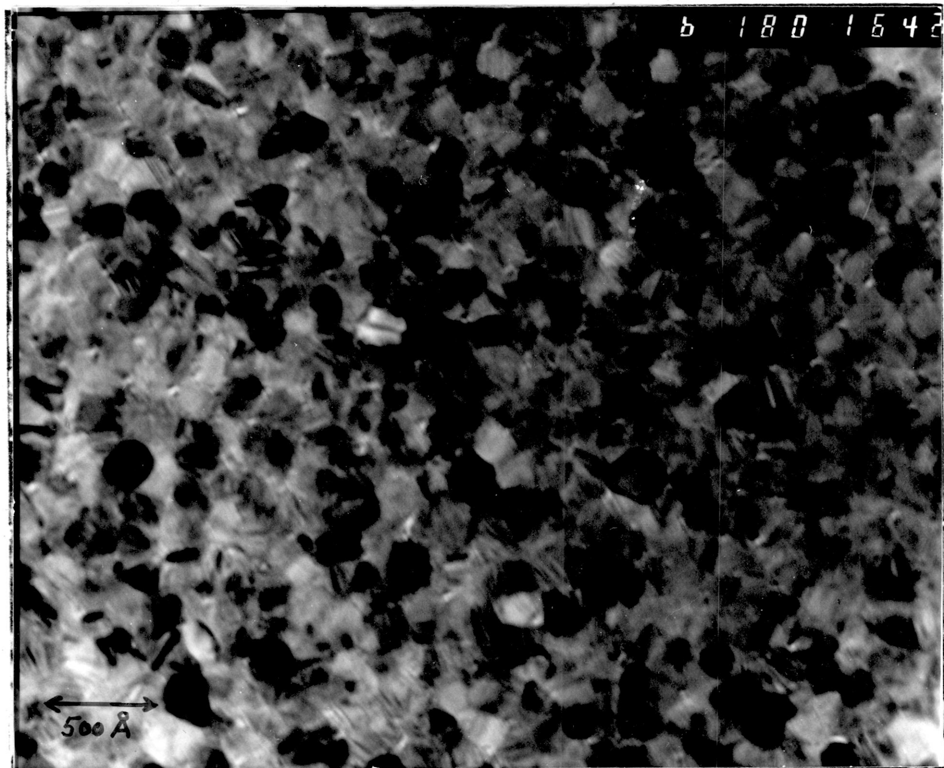


Plate XIII. Transmission electron micrograph for unannealed CdSe.

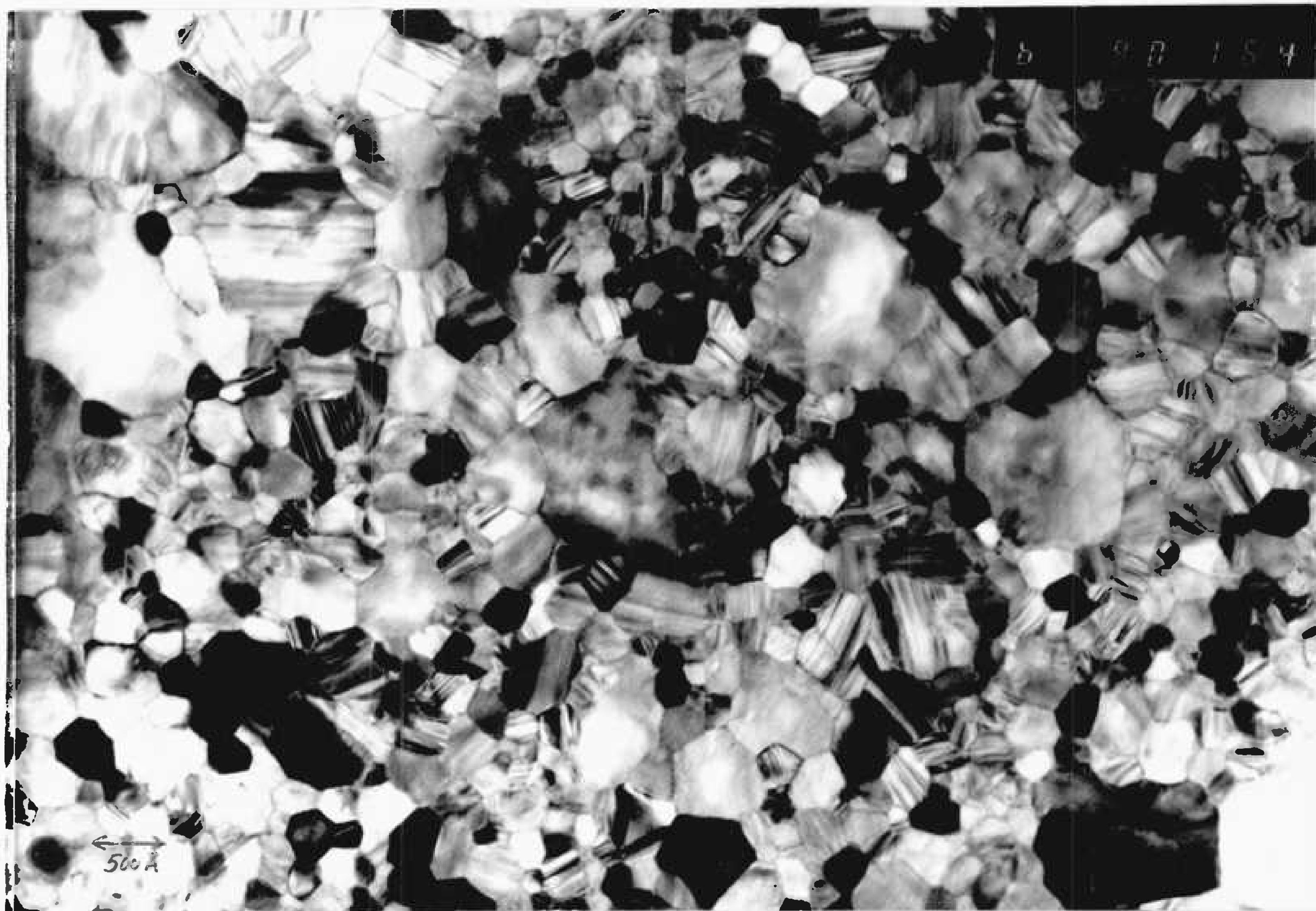


Plate XIV. Transmission electron micrograph for CdSe annealed for 1¼ hours.

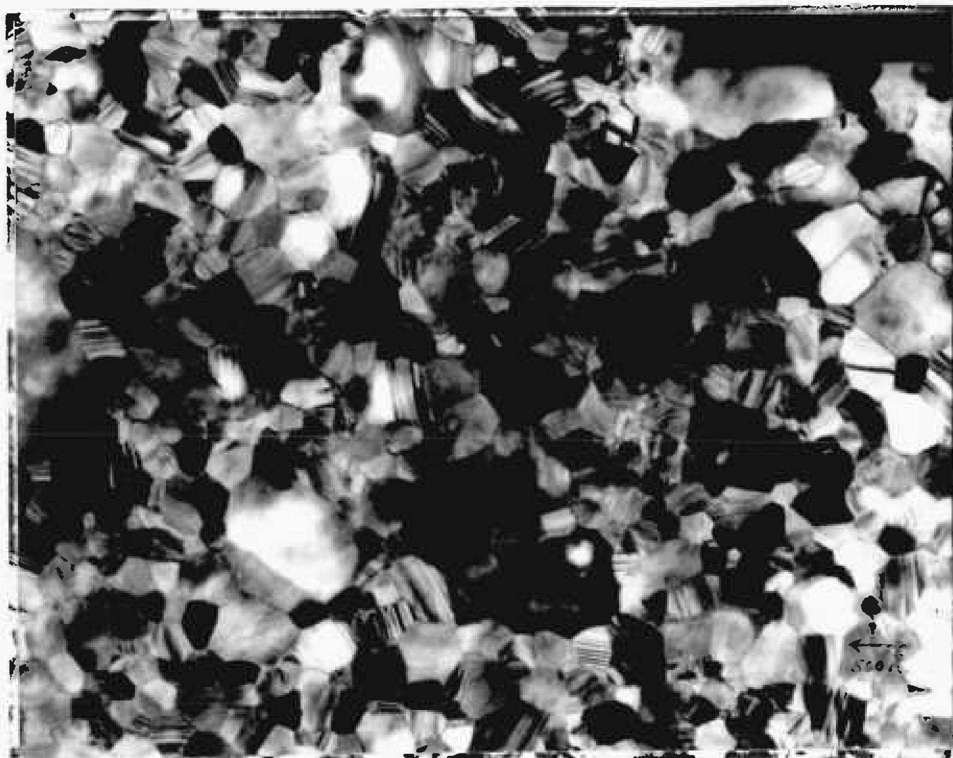


Plate XV. Transmission electron micrograph for CdSe annealed for 52 hours.

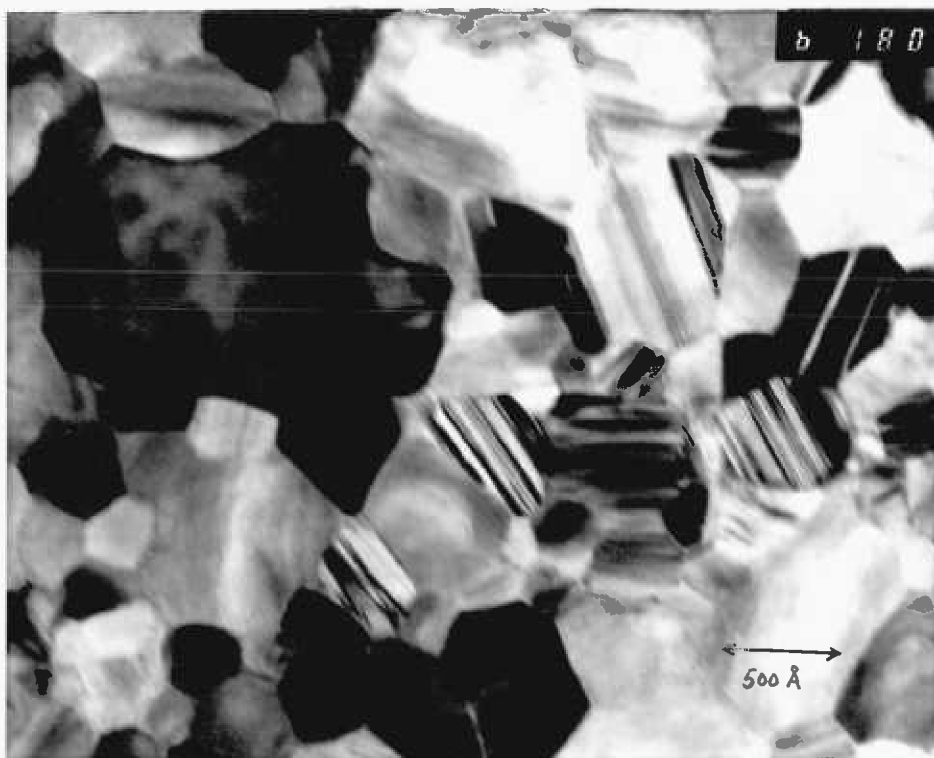


Plate XVI. Transmission electron micrograph for CdSe annealed for 93.5 hours.

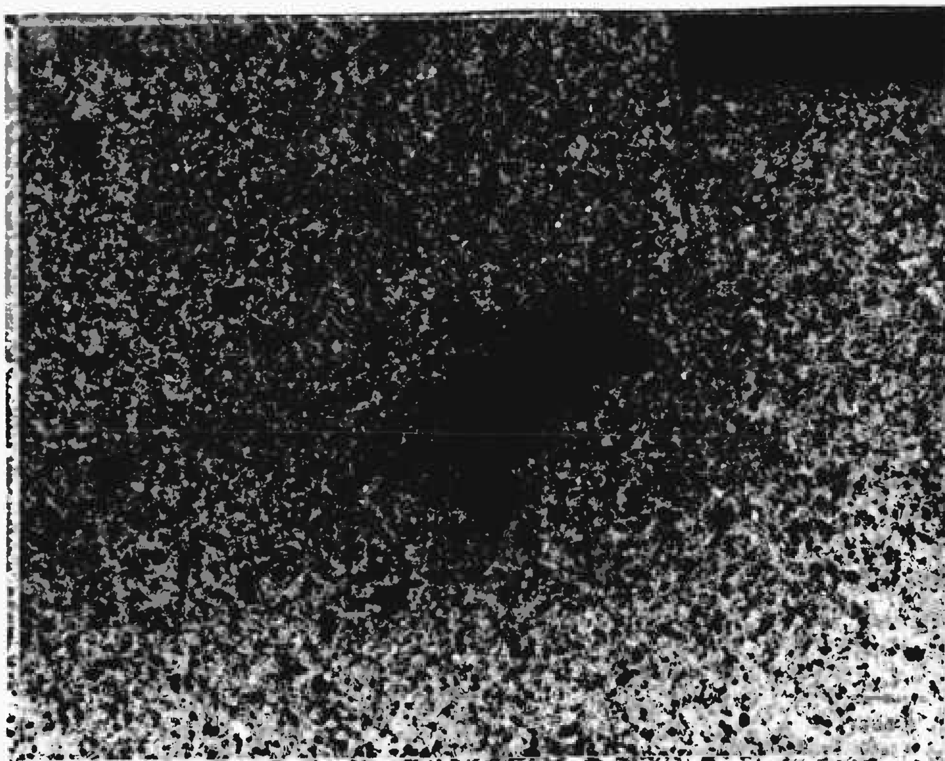


Plate XVII. Transmission electron micrograph for unannealed CdSe.

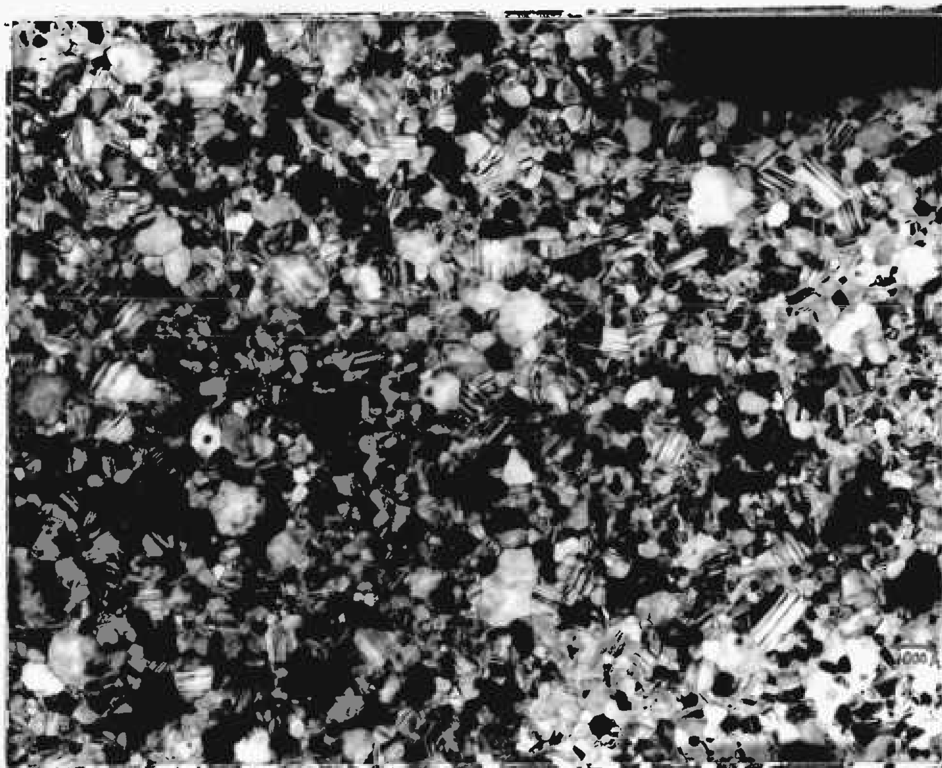


Plate XVIII. Transmission electron micrograph for CdSe annealed for $1\frac{1}{4}$ hours.

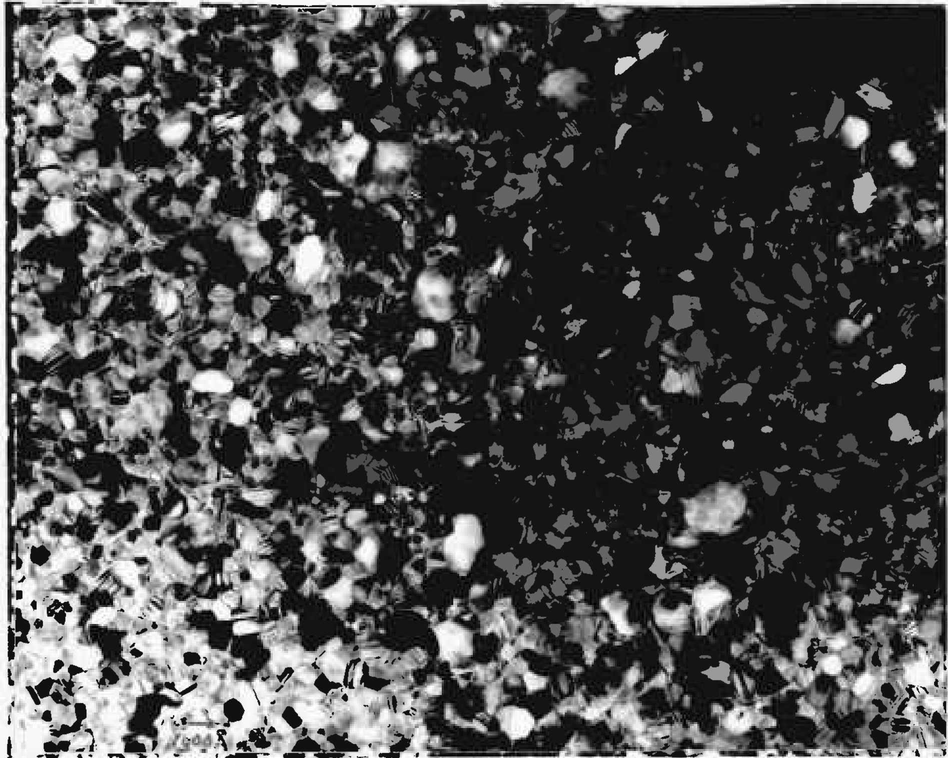


Plate XIX. Transmission electron micrograph for CdSe annealed for 52 hours.

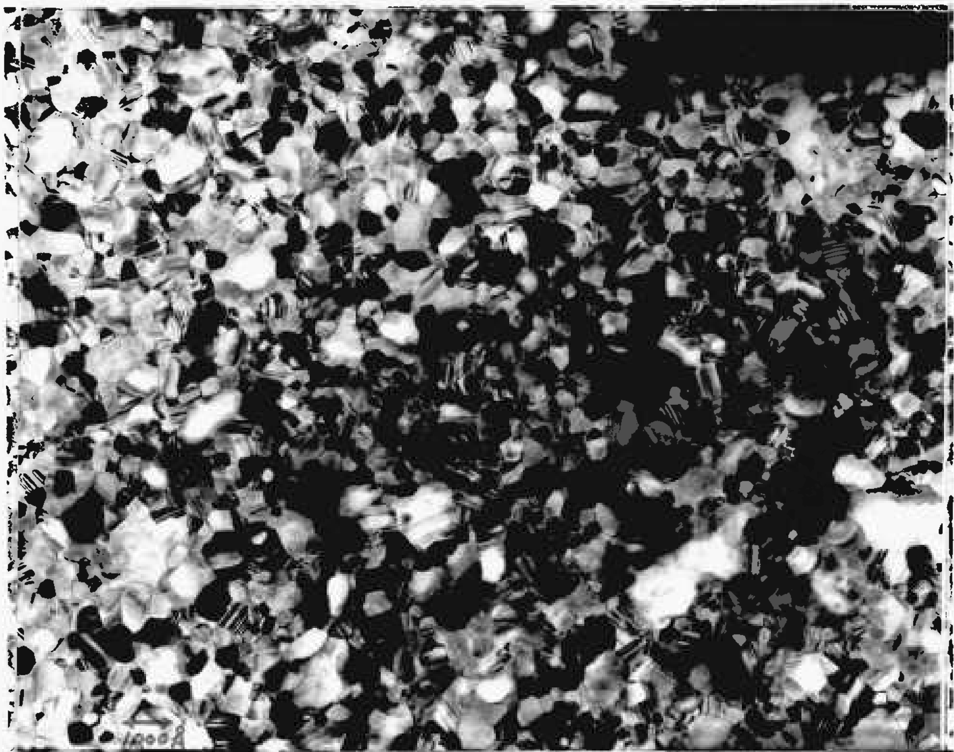


Plate XX. Transmission electron micrograph for CdSe annealed for 93.5 hours.

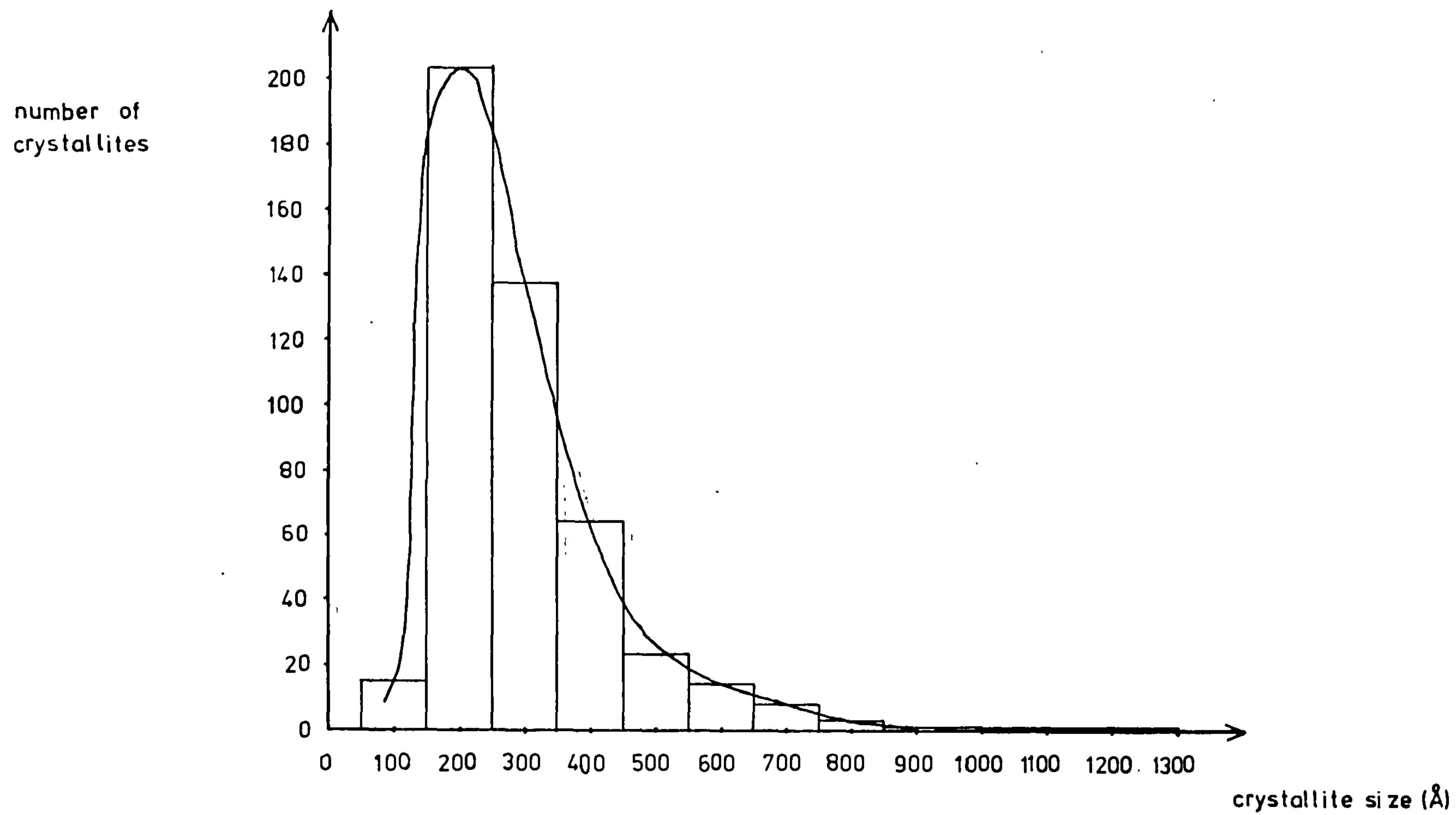


Fig. 27
Histogram showing crystallite size distribution for CdSe film

logarithmic probability paper (1). For a lognormal distribution, if the cumulative relative frequency is plotted against the logarithm of the variable on such paper, a straight line is obtained. Such a straight line has been obtained in Fig. 28 for the distribution of Fig. 27.

The pattern that seems to be prominent in Plate XIV, is that of a few large crystallites scattered about a background of clusters of smaller ones. Further annealing results in these smaller crystallites showing some growth but the larger ones remain approximately constant. This is shown in Plate XV where the annealing time was 52 hours. Plate XVI is the highest magnification obtained for a film annealed for the longest time of 93.5 hours. It shows that no drastic increase in crystallite size has occurred.

A qualitative comparison of the effect of the annealing time on the crystallite size can best be made with reference to Plates XVII to XX, all of which have the same magnification. These show that the most significant change in crystallite size occurs as a result of annealing for $1\frac{1}{4}$ hours, which is the time needed to produce working TFTs. The increase is small for longer annealing times.

5.1.3. Analysis of Annealing Experiments

The experimental results show that fast grain boundary migration takes place up to $1\frac{1}{4}$ hours of annealing time and migration is very slow after this time. This can be used to describe the structural changes undergone by the grain boundary during annealing. Simpson and Aust (2) have reviewed temperature activated grain boundary migration, and report on the dependence of activation energy for boundary migration on misorientation between crystallites. For

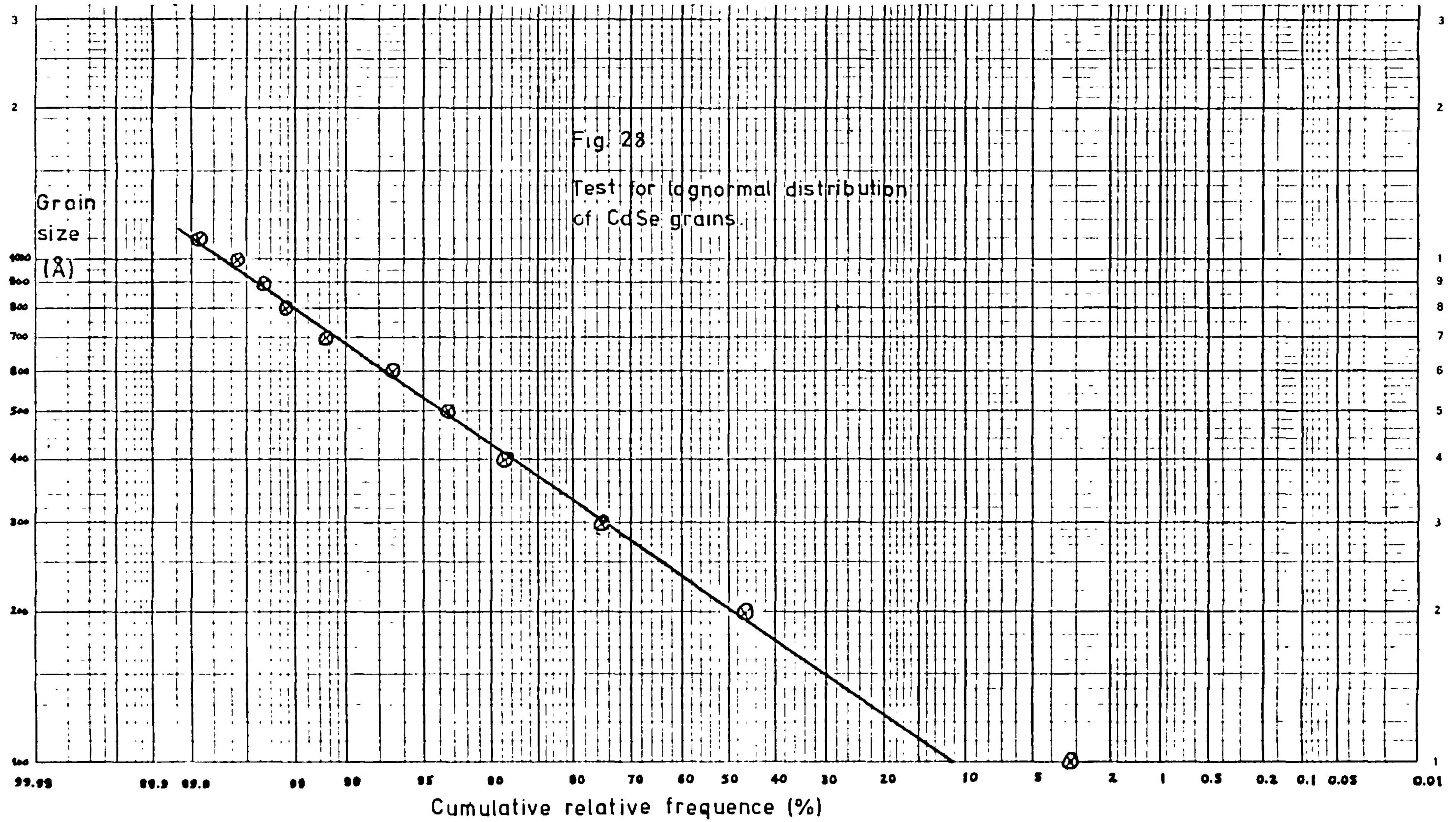


Fig. 28

Test for lognormal distribution of CdSe grains.

high-angle grain boundaries, the activation energy for grain boundary migration is low i.e. - fast migration can occur; for low-angle grain boundaries the activation energy for migration is high. It is concluded, therefore, that as-deposited, unannealed films of CdSe are characterised by high-angle grain boundaries and annealing for 1¼ hours converts these to low-angle ones with a high activation energy for migration. The process is one of energy minimisation. Because the atoms in them fit together well, low-angle grain boundaries have low energy and therefore grain boundaries tend to become as low-angle as possible as the film grows and during subsequent annealing.

The electron diffraction patterns for the unannealed films show a series of concentric spotty rings (see Plate X). Grains are clearly visible in the corresponding transmission electron micrographs, hence the as-grown films are polycrystalline and not amorphous. Annealing increases crystallite size, hence, if the area selected for the diffraction pattern is kept constant, as was the case for the three Plates X, XI and XII, the number of crystallites within that area decreases with longer annealing time, and the fussy rings of Plate X begin to break up into a spot pattern (3), as in Plates XI and XII.

The mean crystallite size for the 400 Å thick films analysed is 300 Å, when the annealing time is 1¼ hours. Fisher gives a mean of 500 Å for his 600 Å thick films, prepared and treated under identical conditions (4). The trend is, therefore, for the mean crystallite size to be slightly under the film thickness.

It would be sensible to assume that for the 1000 Å thick films in the working TFTs used in the present work, the mean size would be about 900 Å. As annealing proceeds, the mean size of crystallites

increases and tends to equal the thickness of the film. Although annealing for 1¼ hours almost equalises the size to the thickness, equalisation is probably not complete unless the annealing time exceeds a period of time of the order of tens of hours.

It has been assumed that the annealed TFTs used in the present work, contain polycrystalline semiconductor films, where the crystallites are approximately cubic in shape and of sides equal to the thickness of the films. This is a useful approximation because it means that the grain boundary area depends on the active interface (SiO_2 - CdSe) area - it equals twice this interface area - and is independent of the thickness of the film. Using this, together with the active interface area of the device of 5.2×10^{-7} m^2, the total grain boundary area is calculated to be 10.4×10^{-7} m^2. In practice, however, the grain boundary is not a plane but a volume. It is a region of disorder which may extend up to 50 Å into the adjacent crystallite (5). This would give a grain boundary volume of 10.4×10^{-15} m^3.

5.2. TSC Results

In what follows, the properties of the peaks in the TSC curves obtained in the present work, are stated. The complete set of experimental results are presented first, without any analytical comment on individual TSC characteristics, to avoid making the analysis fragmented, and because it is after the presentation of all the results that a coherent picture emerges, which is then treated in the analysis section.

Unless stated otherwise, the samples used were "good" TFTs, that had been annealed beforehand, and the TSC runs were conducted with the sample in the dark. The value of β, as well as those of the enhancing and depleting gate voltages V_{g_1} and V_{g_2} respectively; the temperatures they were applied at, and the times they were maintained for, are stated for the individual runs. For some runs V_{g_1} was applied at room temperature for 5 minutes and then still maintained while the sample was cooled to $110^{\circ}K$. The time taken for the cooling was approximately 40 minutes. V_{g_1} was maintained for a time of t_w minutes at $110^{\circ}K$, before the negative gate voltage, V_{g_2}, was applied and maintained for a time which was usually 20 minutes, t_w was usually 20 minutes. In other runs V_{g_1} was applied after the sample had been cooled to $110^{\circ}K$ and, unless stated otherwise, maintained for 20 minutes before V_{g_2} was applied.

5.2.1. The Three TSC Peaks

Fig. 29 shows the curve corresponding to the first TSC run on a sample with $V_{g_1} = 9.6$ V, applied at $110^{\circ}K$, for 20 minutes, and $V_{g_2} = -9.6$ V applied for the same time. The heating rate was $0.1^{\circ}\ s^{-1}$. Three, rather than one, current ranges are shown, for greater ease of detection

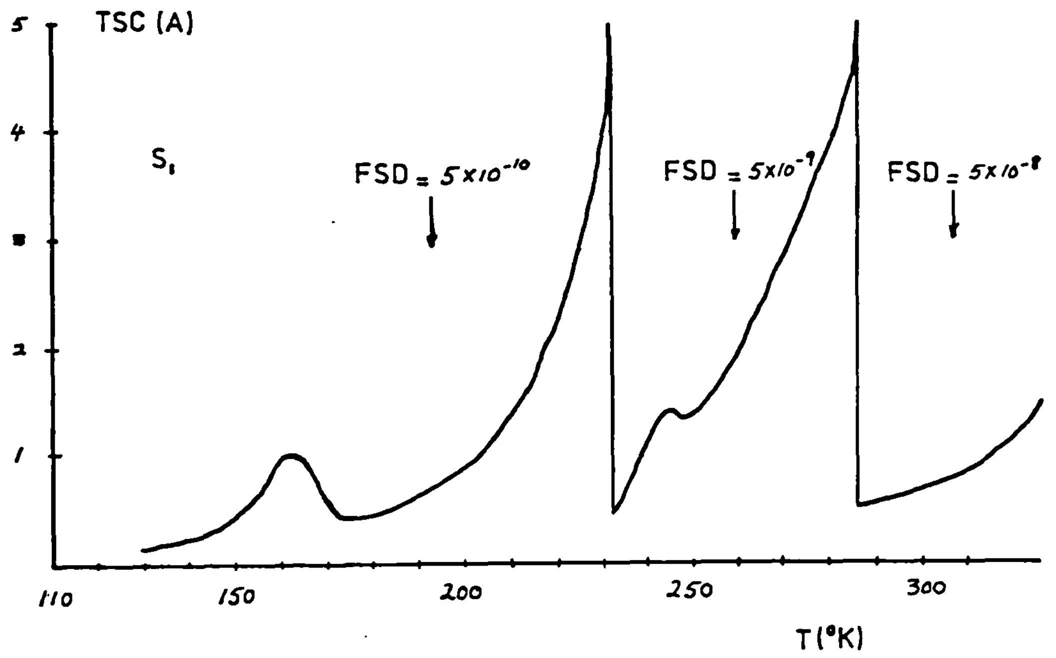


Fig. 29

TSC curve 1

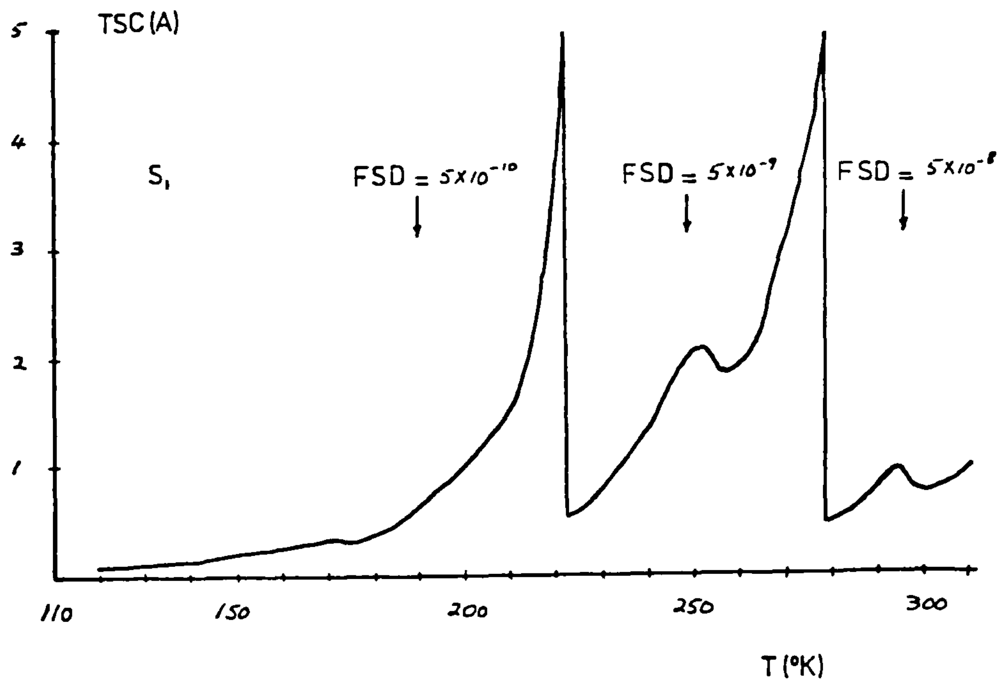


Fig. 30

TSC curve 2

of structure over the entire temperature range scanned.

A peak appears with a maximum at about $160^{\circ}K$ and another at $245^{\circ}K$. These are henceforth referred to as the first and second peaks respectively i.e. peaks are counted starting with the lowest temperature one. The curve shows no structure in the form of peaks above $250^{\circ}K$.

Before any subsequent runs, the sample was artificially $- V_g$ aged. By this is meant that a negative gate voltage was applied, during both the cooling and warming up legs of the TSC run. In this case, a voltage of - 9.6 V was applied to the gate, at room temperature, for 5 minutes. This voltage was maintained while the sample was cooled to $110^{\circ}K$ - the cooling took 40 minutes - and maintained at that temperature for 20 minutes. The sample was then heated up at $\beta = 0.1^{\circ}\ s^{-1}$ with the depleting voltage still on.

A second run was then carried out, on the sample, with conditions identical to those in the first run of Fig. 29. The resulting TSC curve is shown in Fig. 30. A new peak (the third) has appeared at $293^{\circ}K$, whilst the area under the first has diminished. The second peak has become more clearly defined; the area under it has increased, and its maximum has moved to a higher temperature.

It is concluded that the depleting voltage, applied during artificial $- V_g$ aging, results in the diminution of the first peak; the appearance of the third, and the growth of the second.

5.2.2. Effect of $- V_g$ Aging on the Third Peak

The third peak changes as a result of natural, as well as artificial $- V_g$ aging. The latter has been explained before. The former refers

to the change in the third peak between normal TSC runs. It is a result of the depleting voltage applied during the warming up leg of the run alone.

Fig. 31 shows the third peak, during the second TSC run on a new sample which had not been artificially $- V_g$ aged. The dotted line was the structureless background current, obtained during the first run. By the second run, the third peak had appeared due to natural $- V_g$ aging. The curve for the third run is shown in Fig. 32. Subsequent runs showed no further increase in the peak, provided the same value of depleting voltage V_{g_2} was used. In all the three runs V_{g_1} was + 9.6 V, initially applied at room temperature; V_{g_2} was - 4.8 V, while β was $0.1^\circ \ s^{-1}$ and t_w, 20 minutes.

When V_{g_2} was changed to - 9.6 V, all other conditions remaining as before, the peak grew further, and by the fifth run stabilised to that shown in Fig. 33. A comparison of this figure with Fig. 32, shows the effect of natural $- V_g$ aging.

The effect on the third peak, of artificial $- V_g$ aging, was then investigated. This was done with - 9.6 V. Subsequent runs, e.g. Fig. 34, were all reproducible. Furthermore, a comparison between Figs. 34 and previous runs, shows the effect of artificial $- V_g$ aging - it results in a marked increase in the area under the third peak. Around the current maximum of the peak, the electrometer pointer gave a series of sharp kicks, as shown in Fig. 34.

It is concluded, that the appearance and growth of the third peak, is a direct result of the application of the depleting gate voltage during normal TSC runs or during artificial $- V_g$ aging runs. The

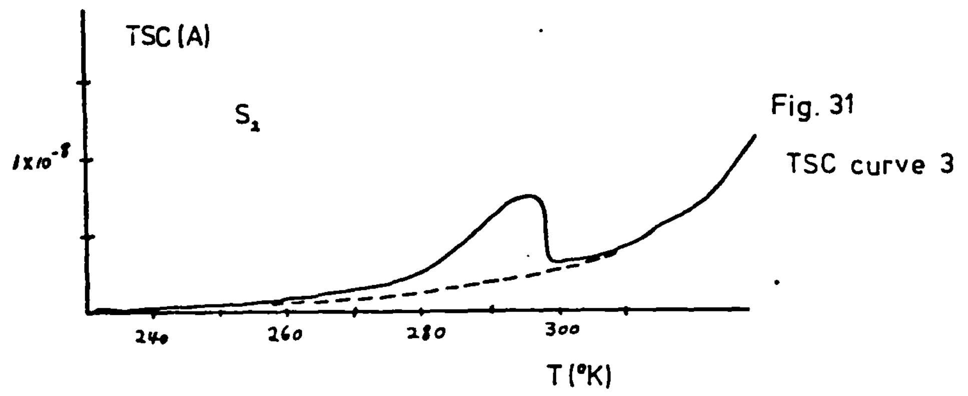


Fig. 31

TSC curve 3

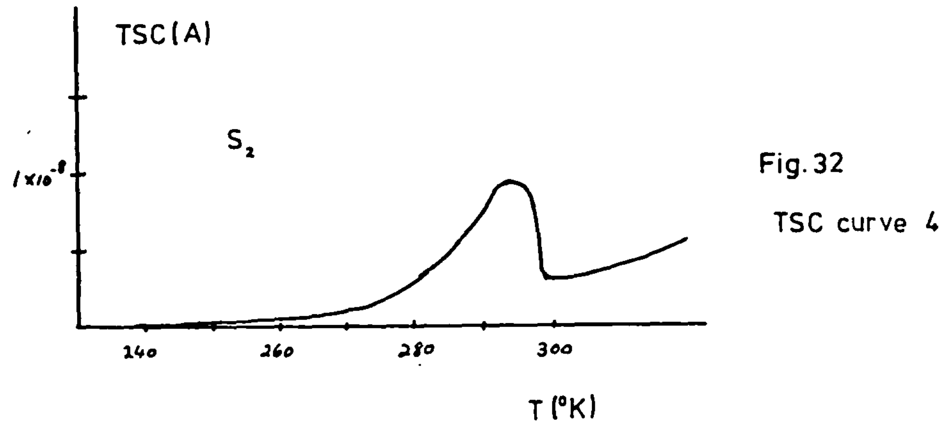


Fig. 32

TSC curve 4

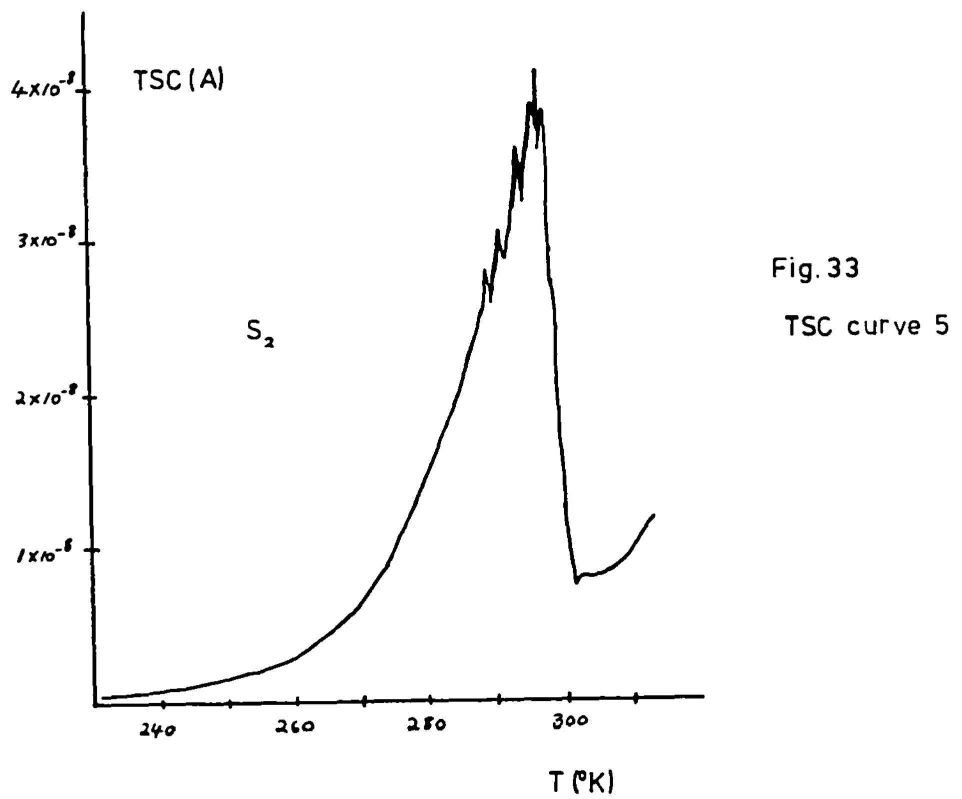


Fig. 33

TSC curve 5

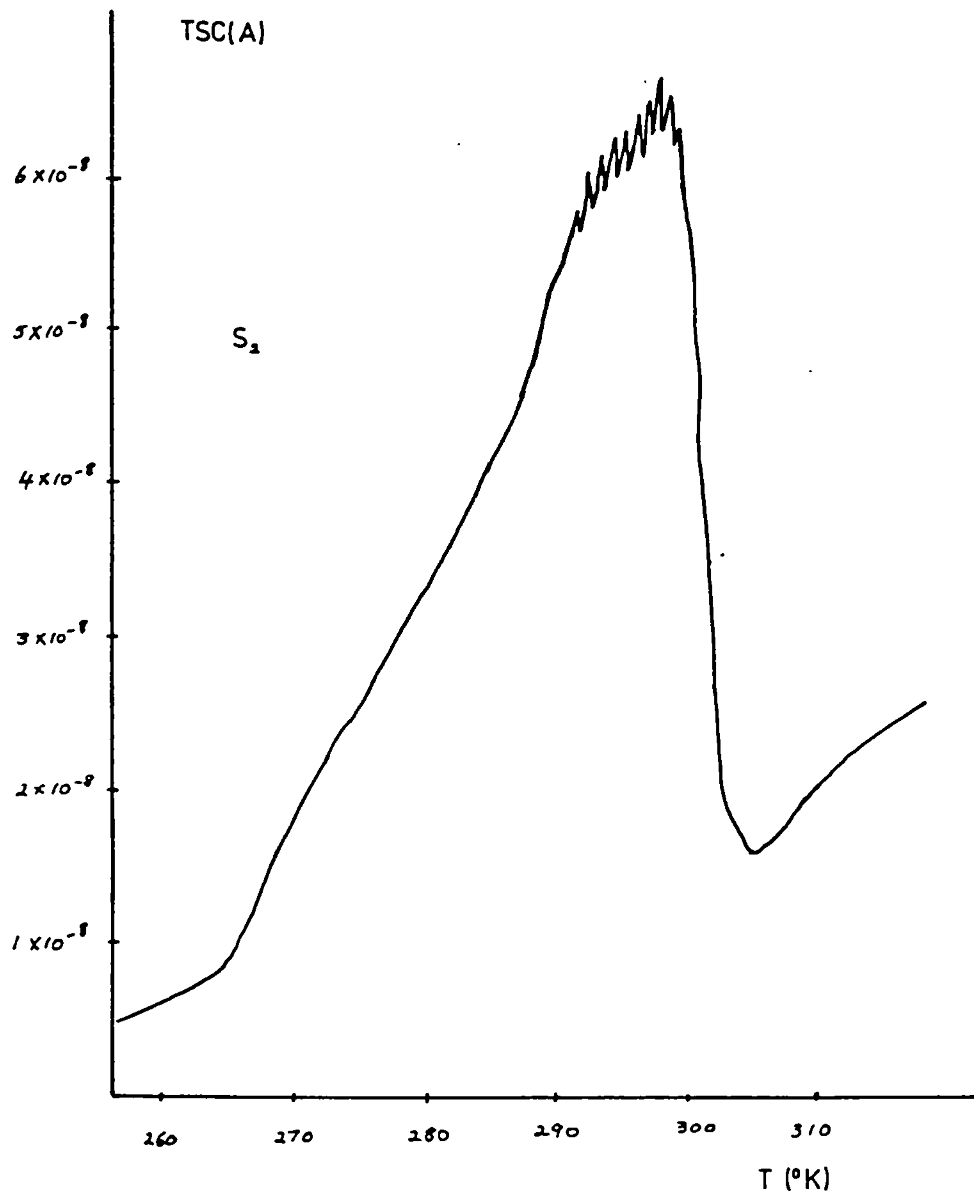


Fig. 34

TSC curve 6

effect of the latter is more pronounced than that of the former. An artificially - V_g aged sample gives reproducible TSC curves.

5.2.3. Effect of Varying Enhancing Gate Voltage

Figs. 35, 36 and 37 show the effect of varying the gate voltage applied before the TSC run. The sample used had previously undergone artificial - V_g aging.

For Fig. 35, - 9.6 V was applied at room temperature and maintained during the subsequent cooling and warming up stages of the run. β was $0.1^o\ s^{-1}$. Only one peak was observed at a temperature corresponding to that of the third peak.

For Fig. 36, V_{g_1} was + 1.6 V applied at 110^oK for 20 minutes. This was followed by a V_{g_2} of - 9.6 V, applied for 20 minutes, before starting warming up with $\beta = 0.1^o\ s^{-1}$. The resulting TSC curve gave a peak with a maximum at the same temperature as in the previous run, but the peak was now wider.

Increasing V_{g_1} to + 3.2 V, while keeping the biasing temperature, biasing times, V_{g_2} and β the same as in the previous run, resulted in the appearance of the second peak, as shown in Fig. 37. Sharp fluctuations at the third peak maximum were observed, as with the artificially aged sample, with the large third peak of Fig. 34, examined before. If, after any of these runs, i.e. when the traps had emptied, the depleting gate voltage was still maintained, and the cooling and warming up stages of the TSC run repeated, the dotted curve shown in Fig. 35 was observed. This was referred to as the background current.

The temperature corresponding to the third peak maximum remained unchanged within the accuracy of the experiment. The current correspond-

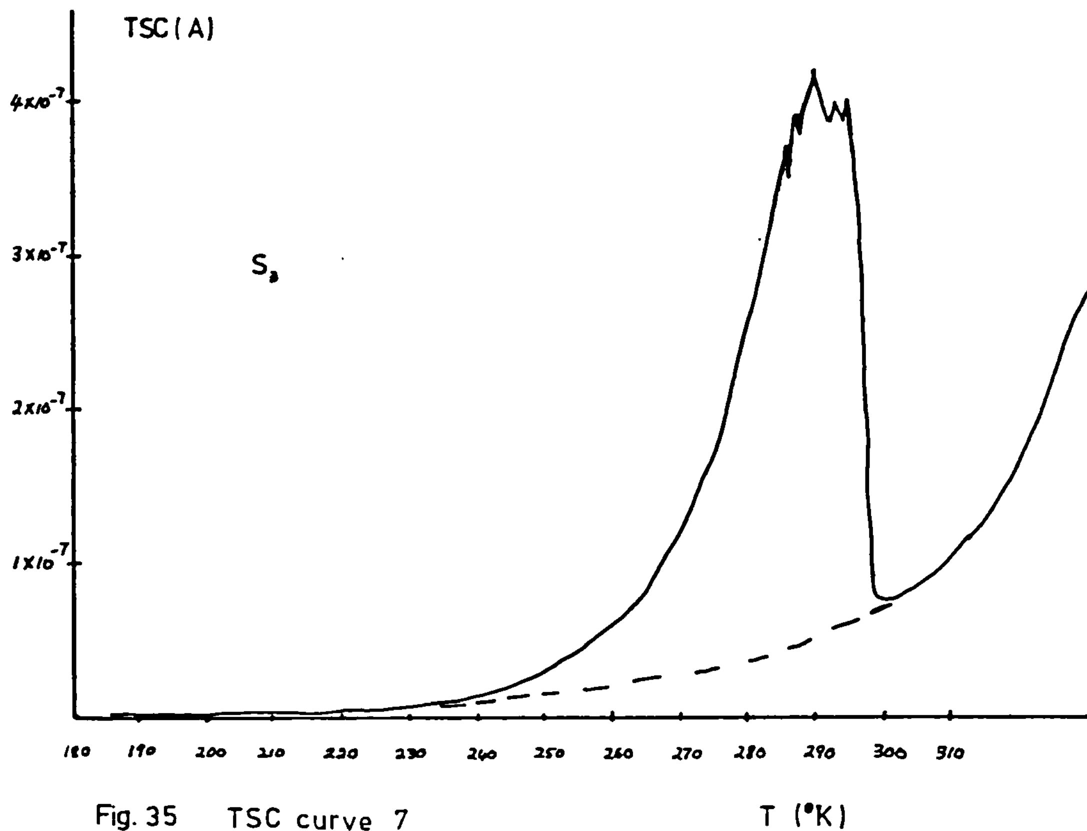


Fig. 35 TSC curve 7

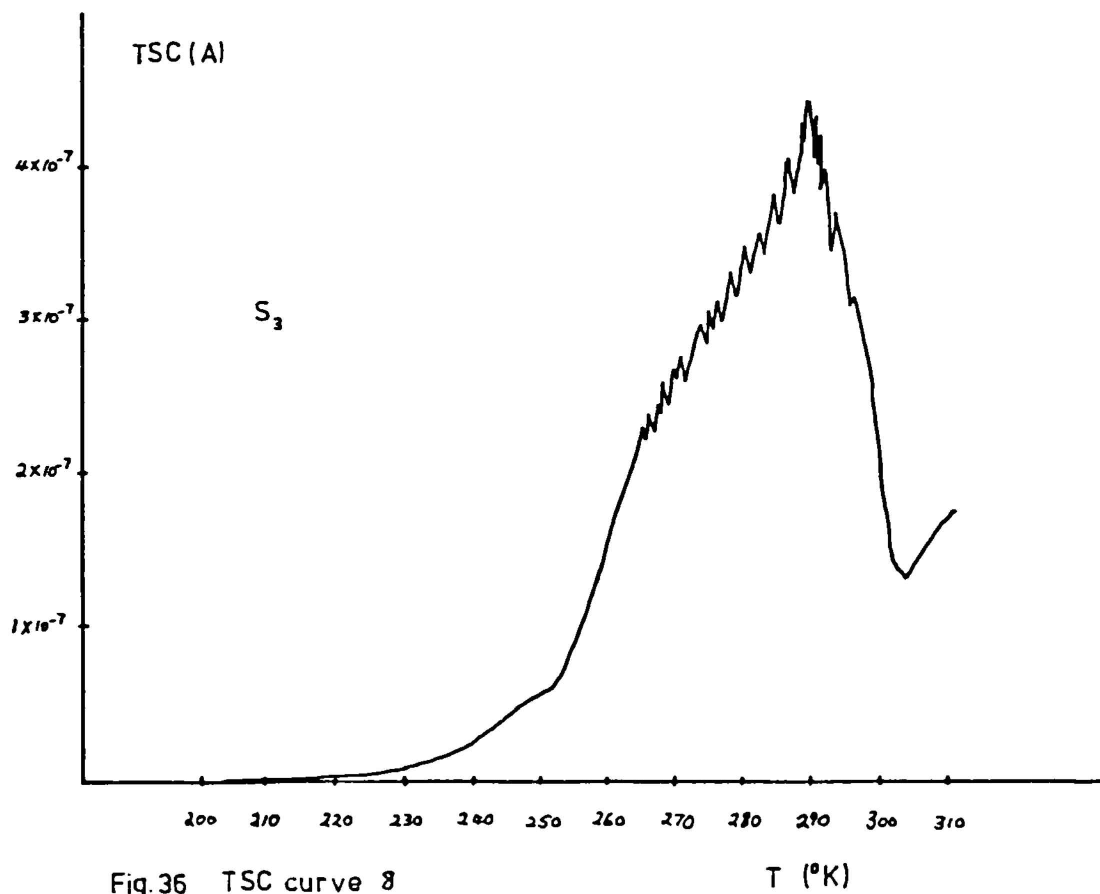


Fig. 36 TSC curve 8

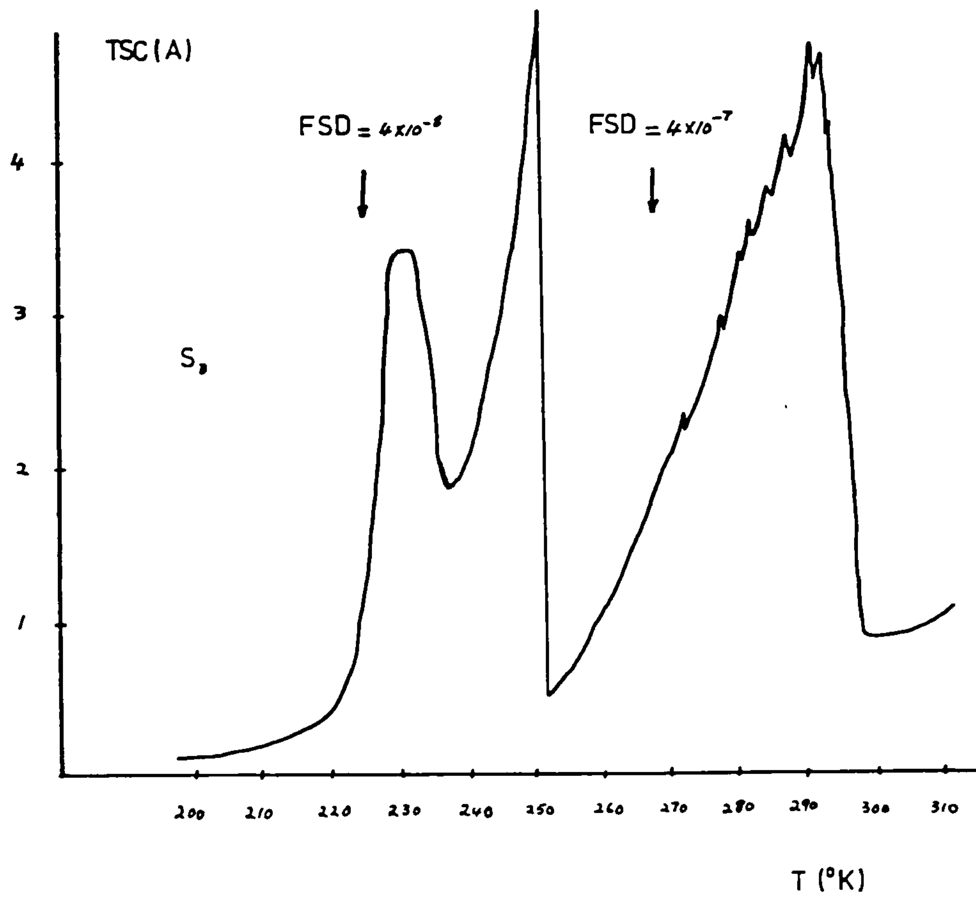


Fig. 37

TSC curve 9

ing to this maximum, however, increased slightly with increase in enhancing voltage.

5.2.4. Effect of Varying Enhancing Gate Voltage on the Third Peak

Figs. 38, 39 and 40, show the effect of varying V_{g_1}, on the third peak of another artificially - V_g aged sample. In Fig. 38 a V_{g_1} of + 1.6 V was applied at room temperature, for 5 minutes, and maintained during cooling. It was kept at 110°K for 20 minutes. V_{g_2} was - 9.6 V applied for 20 minutes and β 0.1° s^{-1}. In Figs. 39 and 40, V_{g_1} was + 4.8 and + 6.4 V respectively, all other parameters remaining the same as for Fig. 38.

It was observed that increasing V_{g_1} to 4.8 V resulted in the appearance of a sub-peak at 284°K, which was a noisy substructure on the leading edge of the third peak, and the maximum corresponding to the main peak increased slightly (Fig. 39). A further increase to + 6.4 V resulted in the sub-peak moving up in temperature, till it could no longer be distinguished from the main third peak (Fig. 40).

Furthermore, the maximum of this peak now became a noisy plateau and its magnitude was larger than in the previous run. No other peaks appeared at any lower temperature.

It is concluded that for some samples, the leading edge of the third peak may display what may be some structure, or a peak, on its leading edge, which moves up the third peak, with increase in enhancing gate voltage, till the two merge to give one indistinguishable peak, with a noisy maximum.

5.2.5. Effect of Varying the Depleting Voltage on the Third Peak

The effect of varying V_{g_2} on the third peak is shown in Figs. 41

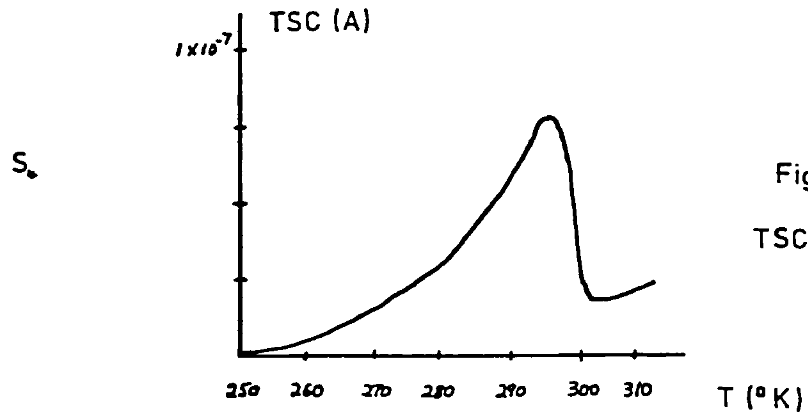


Fig. 38

TSC curve 10

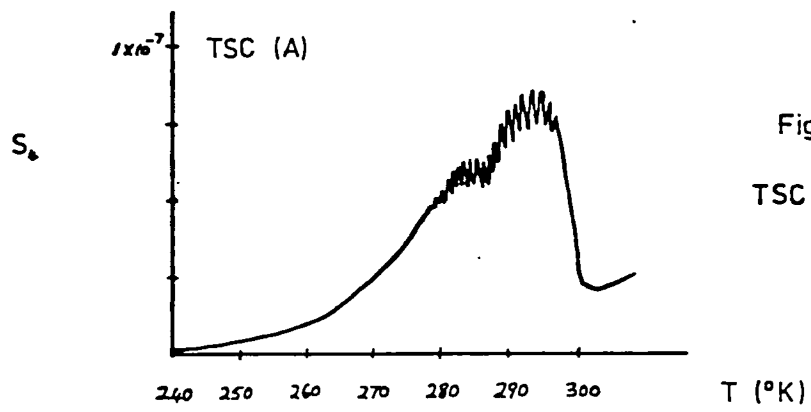


Fig. 39

TSC curve 11

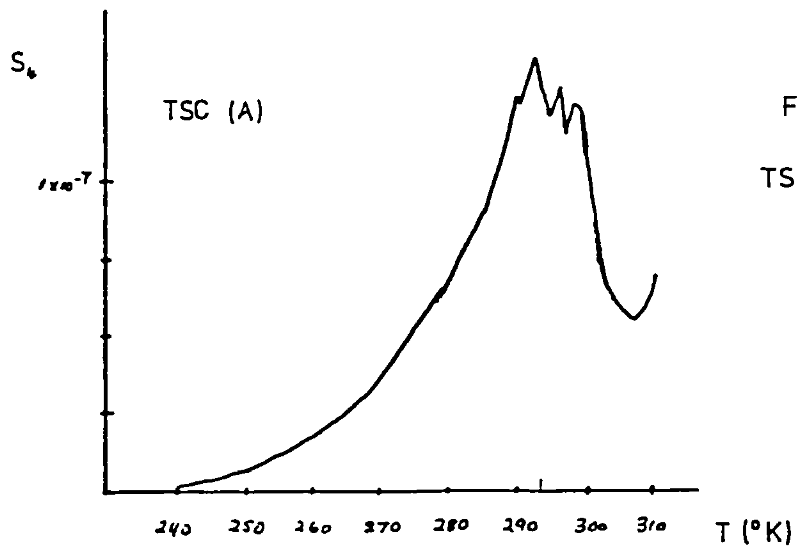


Fig. 40

TSC curve 12

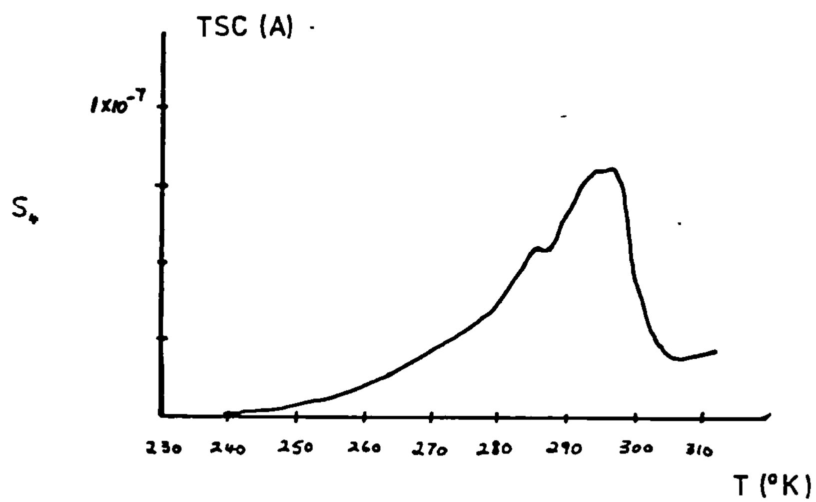


Fig. 41

TSC curve 13

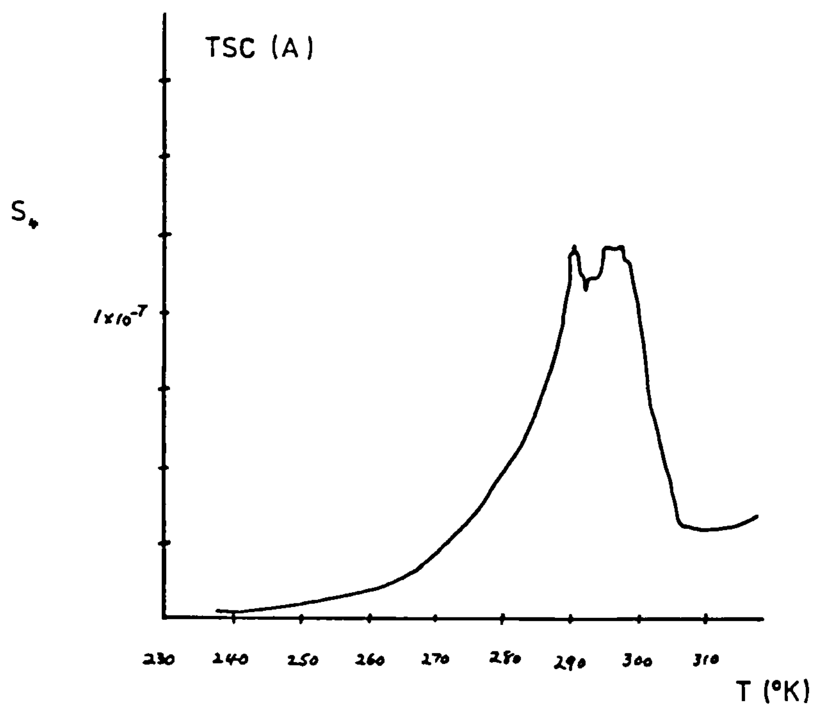


Fig.42

TSC curve 14

and 42. In both runs, V_{g_1} was + 6.4 V, applied initially at room temperature, while β was $0.1^\circ\ s^{-1}$. In Fig. 41, V_{g_2} was - 4.8 V, while in Fig. 42, it was - 9.6 V. Increasing the magnitude of the depleting voltage resulted in a higher current. The substructure or peak on the leading edge of the third peak, could be distinguished in Fig. 41. In Fig. 42, however, the third peak displayed a noisy plateau for its maximum. This might be interpreted as the two peaks having merged to become undistinguishable or had the same value of current maxima.

5.2.6. Effect of varying t_w

Figs. 43 and 44 show the effect of varying the waiting time, t_w, for which the enchancing voltage V_{g_1} was applied. In both runs V_{g_1} was + 9.6 V, applied at 110°K. In Fig. 43, t_w was 20 minutes, while in Fig. 44, t_w was increased to 60 minutes. V_{g_2} was - 9.6 V and β $0.1^\circ\ s^{-1}$ in both runs. The sample was an artificially - V_g aged one.

Increasing t_w resulted in a marked increase in the current corresponding to the maximum of the second peak, while no such increase was apparent in the third peak. Furthemore, increasing t_w resulted in the temperature corresponding to the maximum of the second peak moving to a higher temperature.

5.2.7. Effect of Varying β

Figs. 45 and 46 show the effect of varying the heating rate on the TSC curve. For Fig. 45 V_{g_1} was + 9.6 V, applied at 110°K for 20 minutes; β was $0.1^\circ\ s^{-1}$. For Fig. 46 V_{g_1} was + 9.6 V as before, but now it was initially applied at room temperature, and maintained during cooling; β was $0.012^\circ\ s^{-1}$. In both runs V_{g_2} was - 9.6 V.

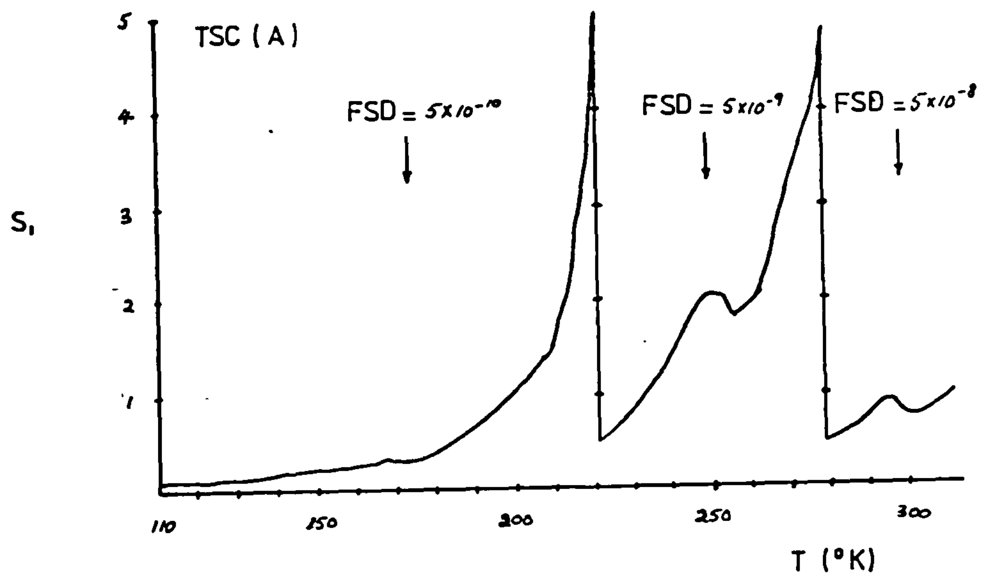


Fig.43

TSC curve 15

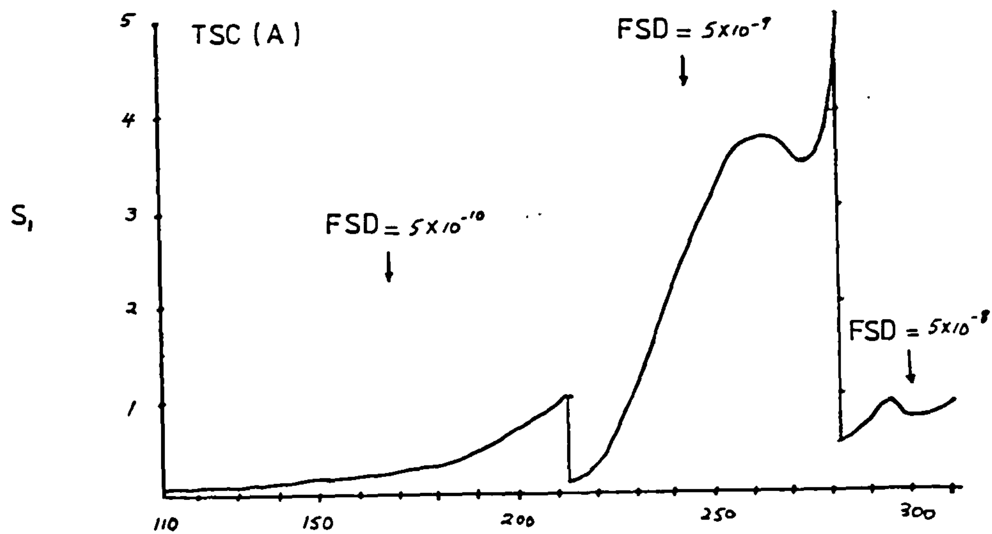
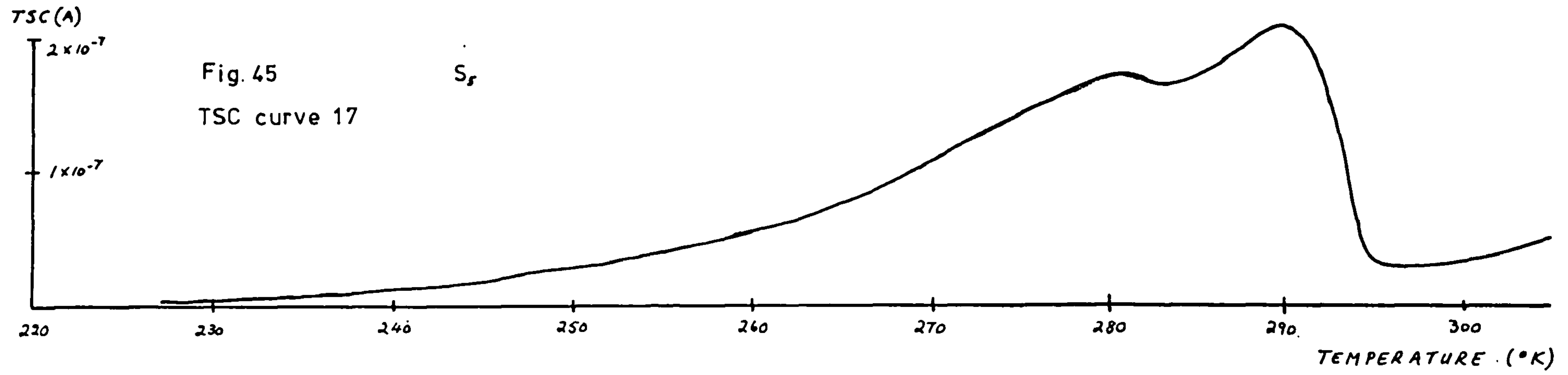
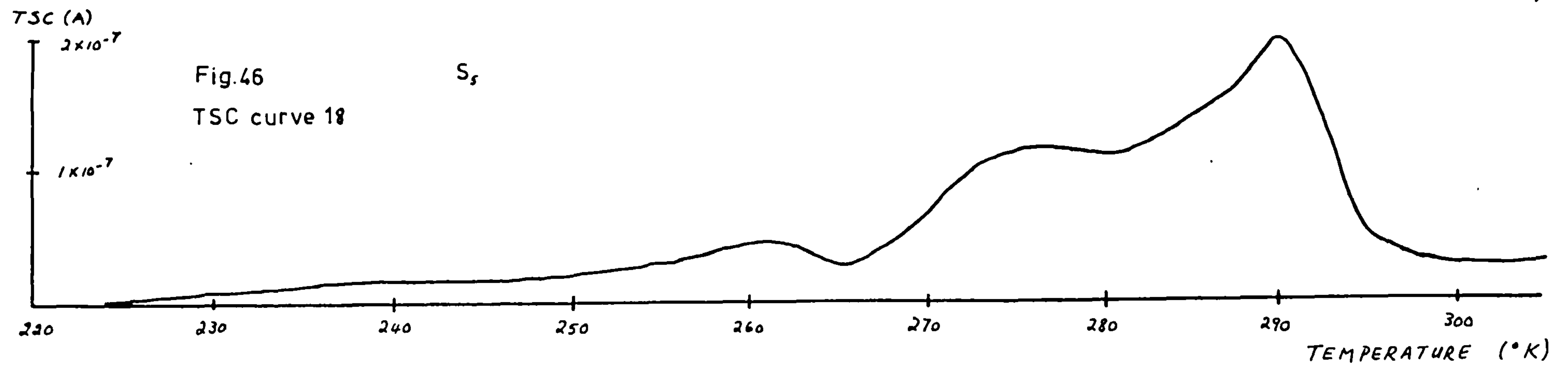


Fig.44

TSC curve 16


TSC (A)
2×10⁻⁷
1×10⁻⁷
Fig. 45
S_s
TSC curve 17
220
230
240
250
260
270
280
290
300
TEMPERATURE (°K)


TSC (A)
2×10⁻⁷
1×10⁻⁷
Fig.46
S_s
TSC curve 18
220
230
240
250
260
270
280
290
300
TEMPERATURE (°K)

5.2.8. Experiments with Light

For TSC runs on some samples, in the dark, the third peak did not appear above the background current, despite artificial $-V_g$ aging. The second peak was present. Exciting the sample by illumination, resulted in the third peak appearing, although its magnitude was small. Subsequent TSC runs without illumination, and the samples in the dark, resulted in the disappearance of this peak.

For Fig. 47 light was shone on such a sample,while it was cooled with an enhancing voltage V_{g_1}, of + 9.6 V, applied to the gate. The TSC curve was obtained in the dark with a V_{g_2} of - 9.6 V. For Fig. 48 the sample was illuminated while cooling with a small depleting voltage of - 3.2 V on the gate. The TSC curve shown was obtained in the dark, with a V_{g_2} of - 9.6 V as before. In both runs the dashed line corresponds to the background current and β was $0.1^{\circ}\ s^{-1}$.

It is observed that while the magnitude of the third peak is unaffected by the different treatments before warming up that of the second is - it diminishes significantly, but does not disappear altogether in the second run as compared to the first. The second peak of Fig. 48 would have disappeared altogether, if this run had been repeated, without illuminating the sample during cooling but maintaining the depleting voltage during this time. By the disappearance of the second peak is meant the coincidence of the TSC curve over the temperature range of this peak, with the background current.

5.2.9. TSC Curves of Bad TFTs

Fig. 49 shows the TSC curve of a bad TFT which had undergone natural $-V_g$ aging. V_{g_1} was + 19.6 V applied at room temperature and

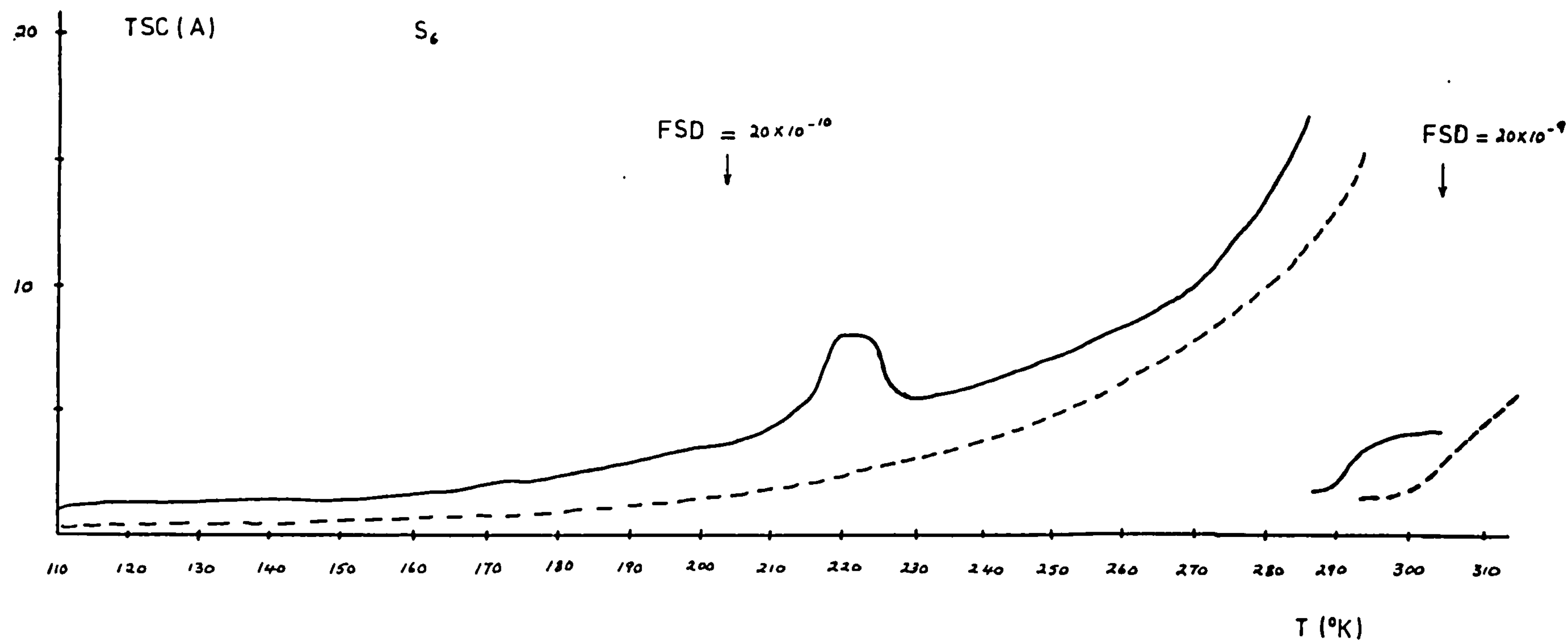


Fig. 47

TSC curve 19

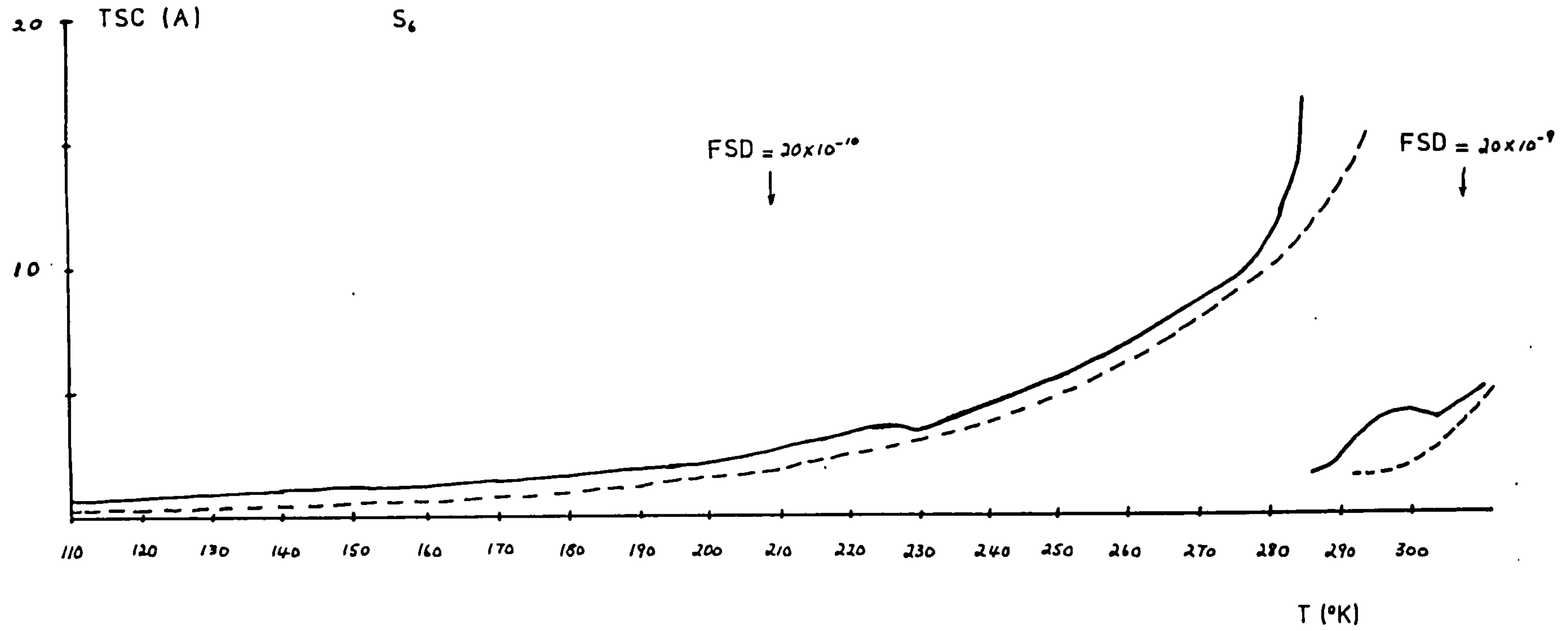


Fig. 48

TSC curve 20

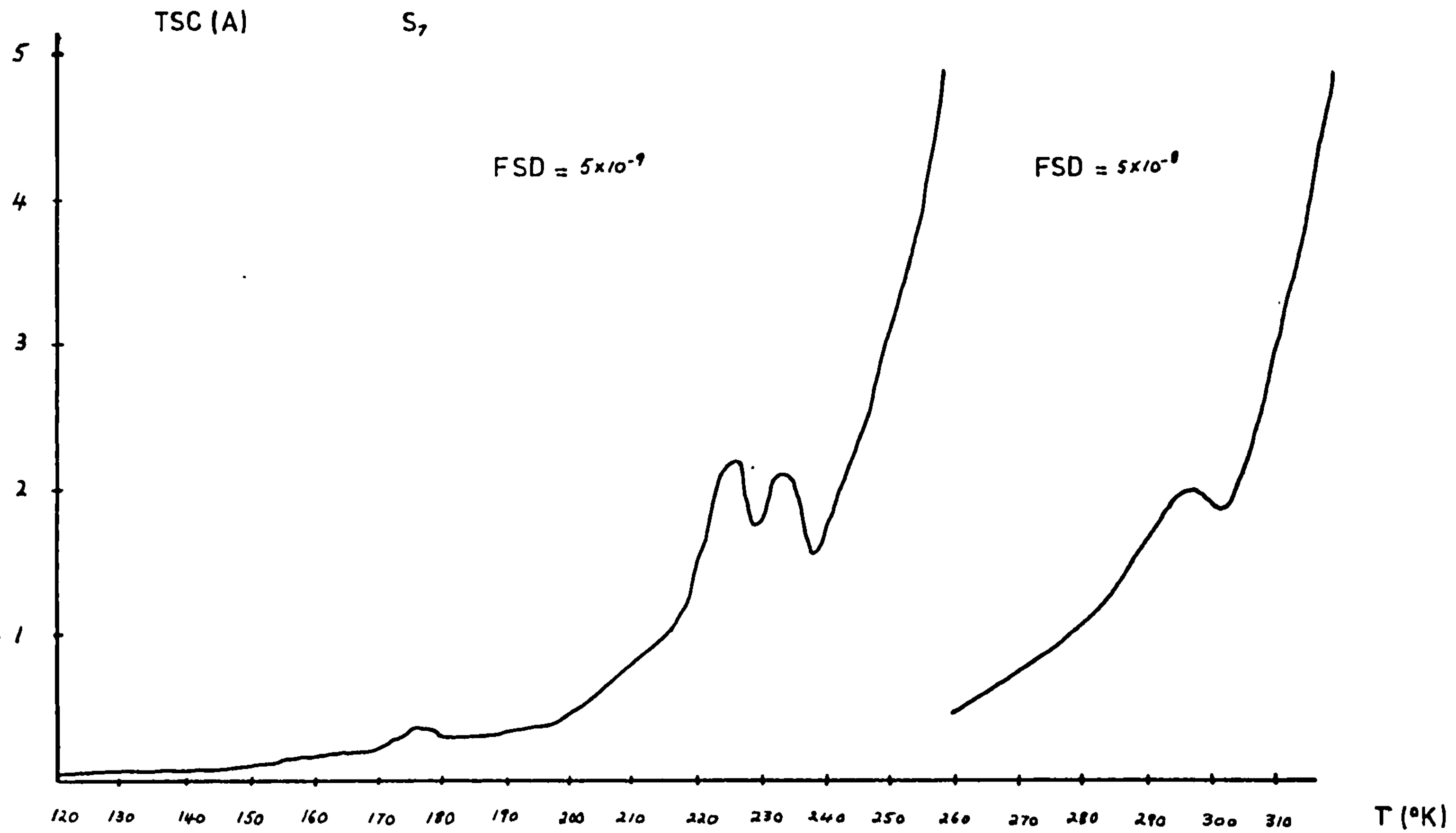


Fig. 49
TSC curve 21

maintained during cooling. V_{g_2} was - 9.6 V and β was 0.1° s^{-1}. The peaks observed were the same as those for good TFTs, except the second, which had a double hump; one peak appearing at about 226 and the other at 232°K. It was observed that the value of V_{g_1} needed to get all three peaks on the curve, was greater than in good TFTs - + 19.6 V as compared to + 9.6 V for good TFTs.

Fig. 50 shows the first TSC curve for another bad TFT which had not undergone any - V_g aging prior to this run. The double humped second peak was observed once more. V_{g_1} was + 11.2 V, first applied at room temperature and V_{g_2} was - 9.6 V. β was 0.1° s^{-1}. In Fig. 51, V_{g_1} was changed to + 1.6 V, while all other parameters were kept the same as in Fig. 50. A single humped second peak was observed at the peak temperature of 232°K.

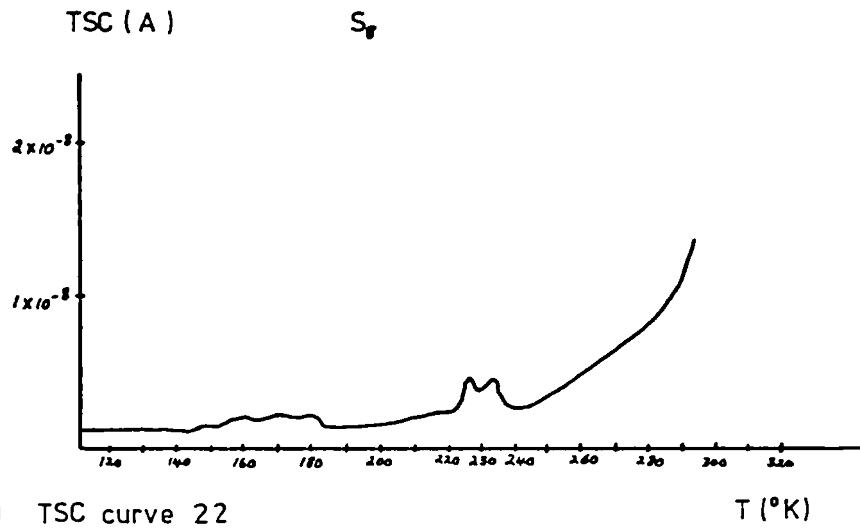


Fig. 50 TSC curve 22

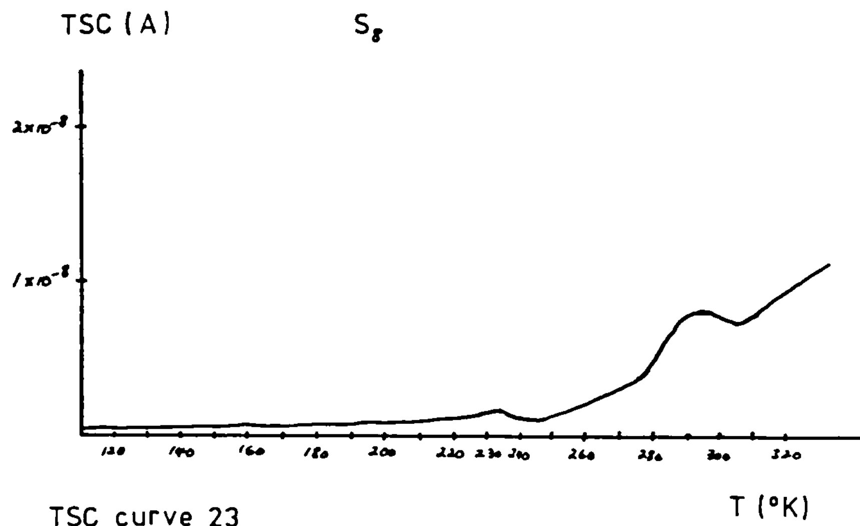


Fig. 51 TSC curve 23

5.3. Analysis of Results

In what follows the properties of the TSC peaks, the identification of traps, and their analysis is presented.

5.3.1. The First Peak

This is observed for the first run on an unaged good TFT, as in Fig. 29, where it has a maximum at 160°K and the charge associated with it, calculated from the area under the curve, is 17×10^{-9}C. Its activation energy is 0.17 eV (see later). During subsequent runs the area under this peak diminishes and then usually disappears. In Fig. 30 the charge associated with it has decreased to 2×10^{-9}C. No accurate values of the activation energy could be determined after the first run. The decrease and disappearance of the peak made the investigation of the effect of β on its behaviour impossible. The activation energy of this peak was obtained from the slope of a graph of ln (I_{TSC}) against 1/T as shown in Fig. 52, i.e. equation (1) was used. This was done to enable the comparison of the activation energy obtained in the present work, with those of previous workers on CdSe, all of whom used the above method of finding the activation energy. This comparison enables the identification of the peak. The value of 0.17 eV corresponds to the donor level of 0.15 or 0.19 eV, obtained by Kindleysides and Woods, and that of 0.177 eV, given by Manfredotti et. al., for single crystal CdSe (section 2.2.4.). This is the level corresponding to the 0.14 eV one of Shimizu and 0.13 eV of Hino and Yamashita (section 2.2.5.) who have used polycrystalline CdSe. Hence the first peak is considered to be due to donors in the bulk of CdSe

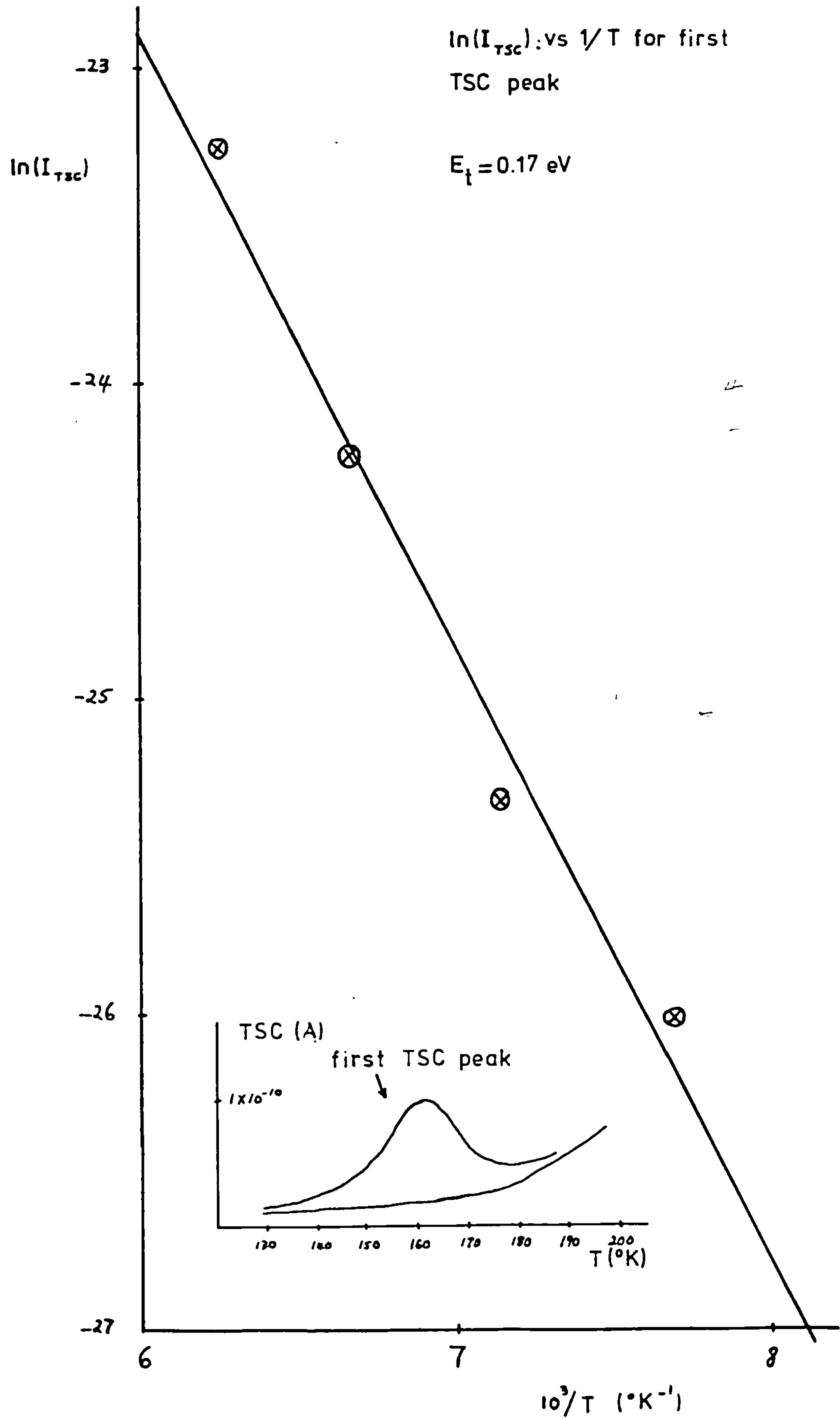


Fig. 52
ln(I_TSC) vs 1/T for first
TSC peak
E_t = 0.17 eV
ln(I_TSC)
-23
-24
-25
-26
-27
6
7
8
10³/T (°K⁻¹)
TSC (A)
first TSC peak
1x10⁻¹⁰
130
140
150
160
170
180
190
200
T (°K)

crystallites. Their activation energy is that identified with Se vacancies.

Since the active volume of the sample is 5.2×10^{-14} m^3, the density of bulk traps corresponding to this peak is 2×10^{24} m^{-3} or 2×10^{18} cm^{-3}. It has been shown by Anderson, however, that the density of free carriers in the films used is of the order of 10^{16} cm^{-3} and that it is constant for all temperatures between room temperature and 110°K (6). This means that the free carriers come from a donor level which is ionised throughout the temperature range scanned, and that this level cannot be that at 0.17 eV, because if this were ionised, it would have introduced a free carrier density two orders of magnitude higher than that observed. Hence, in thermal equilibrium, in that region of the CdSe bulk where no electric field exists, the Fermi level is at least 2kT above the donor level of 0.17 eV, and below another which is fully ionised between room temperature and 110°K. The latter is probably that at 0.014 eV observed by Burmeister and Stevenson (see section 2.2.4.) which has been attributed to Cd interstitials. Hence the Fermi level is about half way between 0.17 and 0.014 eV i.e. at approximately 0.09 eV. A check on this value of the Fermi level is provided by using the fact that when all donors are ionised, i.e. the electron density is a constant, independent of temperature, then equation (F5) of Appendix F gives the position of the Fermi level. Anderson gives the values of N_c and N_d as 1.17×10^{24} and 4.5×10^{22} m^{-3} respectively (7). Hence, at 300°K, the position of the Fermi level is given as 0.084 eV. This agrees

well with the estimate of 0.09 eV.

The order of magnitude of the density of this donor level at 0.17 eV, together with the position of the Fermi level above it, can now be used to explain a problem which has frequently arisen in TFT calculations. Interface and grain boundary traps being acceptor type, trap electrons from the CdSe bulk, causing a depletion region to stretch into the semiconductor. The surface potential at the interface or grain boundary may be such that this depletion region cannot be accommodated by the semiconductor, if the charge supplied by the CdSe were as low as 10^{16} cm^{-3} i.e. the charge were supplied by the free carriers due to the ionised donors at the 0.014 eV level alone. The existence of the second level, with its higher density, means that it can provide the charge necessary to fill the acceptor states while only a fraction of the thickness of the semiconductor crystallite is depleted. The traps at 0.17 eV will be full away from the depletion regions in the CdSe, but ionised in the depletion regions. The width of the depletion region λ_o for various values of surface potential ϕ_s has been calculated using the formula given by Simmons(8) i.e.

$$\lambda_o = \left[\frac{2\phi_s K \varepsilon_o}{e^2 N_d} \right]^{\frac{1}{2}} \qquad (27)$$

$$\lambda_o = \left[\frac{\phi_s}{N_d \; 905.08 \times 10^{-12}} \right]^{\frac{1}{2}} \qquad (28)$$

where K is the dielectric constant of the semiconductor (= 10 for CdSe); ε_o the permittivity of free space; N_d the density of traps in m^{-3},

and λ_o, as given by equation (28), is in meters.

The values appear in Table 3 and show that even quite high values of surface potential do not cause complete depletion of the semiconductor due to the relatively high density of electrons of $2x10^{24}$ m^{-3} provided by the donor level at 0.17 eV.

The decrease in the area under this peak as a result of $- V_g$ aging means that the application of the negative gate voltage results in the decrease in the density of donors. The explanation of this will be gone into further later.

5.3.2. The Second Peak

For most good TFTs, when a heating rate of 0.1^o s^{-1} is used, the second peak appears as a peak well separated from the first and third ones, with a maximum varying between 230 and 250^oK. In other samples it appeared very close to the third peak, for the above heating rate. In this case it could be distinguished as a distinct peak by lowering the heating rate or by keeping the enhancing gate voltage within a certain range when β was 0.1^o s^{-1}.

This peak is completely absent during TSC runs when a negative gate voltage is applied during cooling as well as warming up. This is shown in Fig. 35 where only the third peak appears. The negative gate voltage during cooling ensures that the CdSe - SiO_2 interface traps are empty prior to the run, so that they do not emit during warming up. Applying a positive gate voltage before the run, to fill the interface traps, results in the appearance of this peak (Figs. 37 and 30). The above suggests that the second peak is due to states at the CdSe-SiO_2

Surface potential ϕ_s (eV)	Depletion width λ_o (Å)
0.40	149
0.45	158
0.50	166
0.55	174
0.60	182
0.65	189
0.70	197
0.75	204
0.80	210

Table 3. Depletion widths in CdSe for different surface potentials and a trap density of 2×10^{24} m^{-3}.

interface. Further evidence is provided to back this, when use is made of the fact that these interface traps contain slow states, and maintaining a positive gate voltage for different periods of time at $110^{o}K$, results in the capture of different amounts of charge by these traps. Hence, for an artificially - V_g aged sample, increasing the waiting time t_w from 20 minutes in Fig. 43 to 60 in Fig. 44, results in an increase in the area under the second peak. The charge released in Fig. 43 is $100 \times 10^{-9}C$ and in Fig. 44, $550 \times 10^{-9}C$ showing the second peak is indeed due to interface traps. Furthermore, note is made of the importance of the slow state contribution to this peak - a contribution which seems to be prominent in the thin film device of the present work.

The experiments where light was used, in addition to various gate voltages, to alter the occupancy of the interface traps, provide further evidence to identify the second peak with interface traps. In Fig. 45 a positive gate voltage and light shining on the sample, resulted in a higher probability of interface traps being filled than in Fig. 46, when light was shone while cooling, as before, but this time with a negative gate voltage. In the latter case less of the interface traps would have been filled. This is because, although shining light would establish a quasi Fermi level above the equilibrium one, resulting in the filling of some of the interface traps, the total number of traps filled would be less than before, where additional filling resulted by the bending of the energy bands downwards, due to the positive gate voltage. The second peak in Figs. 45 and 46 - occurring at about $222^{o}K$ - behaves in such a manner. In Fig. 45 it makes a substantial contribution to the TSC; in Fig. 46

its contribution has decreased but not vanished. It would have vanished i.e. coincided with the background current - shown by the dashed line - had a negative voltage been applied prior to, as well as during warming up, and the sample been held in the dark throughout the whole run. This would have reduced the probability of occupancy of interface traps to effectively nil as demonstrated before.

Two TSC runs, on a sample in the dark, were reproducible if between these runs light was shone on the sample. This shows that the second peak was not the result of a photochemical change.

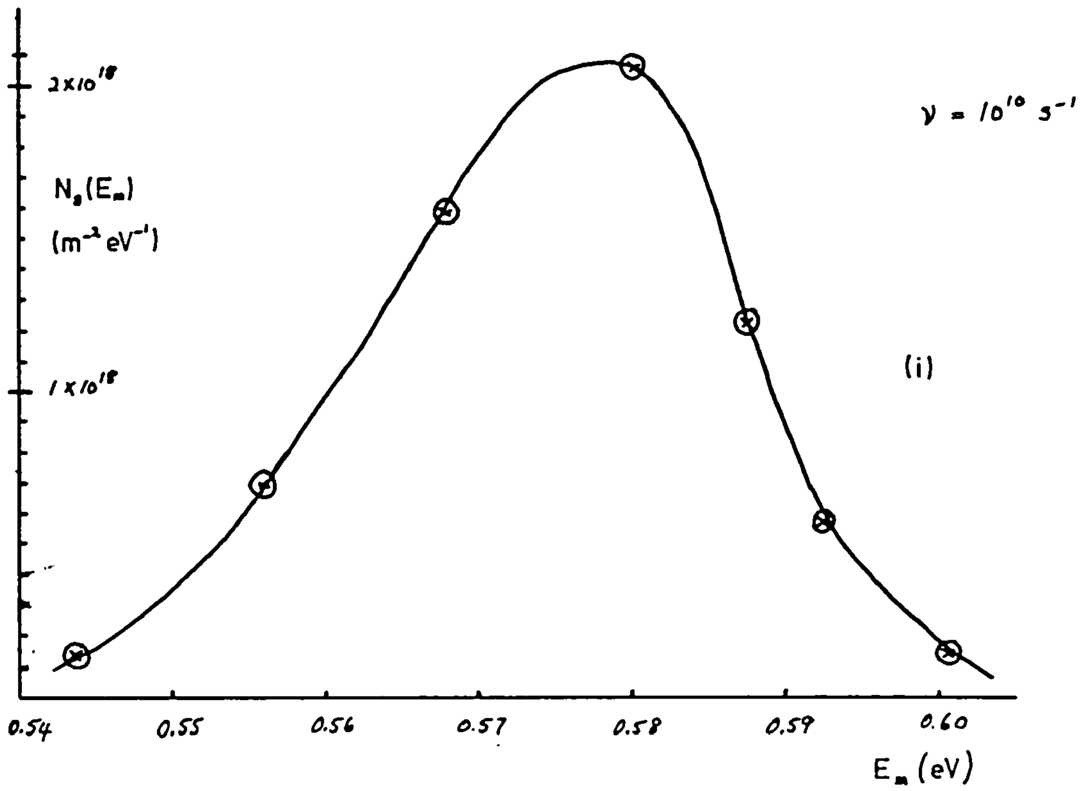
Figs. 29 and 30 show that whereas artificial - V_g aging, results in a decrease in the charge associated with the first peak, it causes an increase in that of the second and indeed the third. The charge released by the second peak is 50×10^{-9}C before aging (Fig. 29). After aging it rises to 100×10^{-9}C (Fig. 30). It is concluded, therefore, that - V_g aging results in an increase in the density of interface traps.

The density of these traps can be calculated, provided the physical dimensions of the source from which the charge released by them is known. In view of the important contribution to the interface peak of slow states, the interface cannot be considered a plane of no width as would have been the case if only fast states existed - but a volume extending from the SiO_2 - CdSe interface to about 20 Å inside the SiO_2. The active area of the sample being 5.2×10^{-7} m^2, a thickness of 20 Å gives a volume of 1.04×10^{-15} m^3. The density of traps, in m^{-3}, can now be calculated by dividing the charge released by the active volume and the electronic charge. The interface trap density is then calculated

to be 3×10^{26} and 6×10^{26} m^{-3} before and after artificial - V_g aging (from Figs. 29 and 30). In samples where the effect of artificial - V_g aging is more prominent- as in Fig. 37, the density is 1×10^{28} m^{-3} i.e. as high as the density of atoms. The above shows that - V_g aging damages the structure of the interface.

The application of Simmons' transformation equations (12) and (14) of section 3.2.4., to the interface peak of Fig. 29, gives the trap distributions shown in Fig. 53. The value of ν has been chosen as 10^{10} and 10^{12} s^{-1} in Figs. 53(i) and 53(ii) respectively. It can be seen that the trap distribution is altered by the value of ν chosen - the change in the energy being more significant than that in the density. The distribution of Fig. 53(ii) agrees with that expected from the results of Consigny and Madigan, who report energies of 0.6 and 0.7 eV as discussed in section 2.1.6. This treatment of the interface traps ignores the slow states. The further analysis of this peak, where both fast and slow states are considered, is one of the proposals for future work arising from the present investigation.

The second category of TFT, where the second peak appears very close to the third, will now be considered. Fig. 38 shows that when the initial enhancing voltage is small (+1.6V), then the third peak appears with a clean leading edge, while increasing this voltage to +4.8V, as in Fig. 39, results in the appearance of a peak on the leading edge of the third peak with a maximum at about $284^{\circ}K$, V_{g_2} was - 9.6V in both runs. This behaviour of the peak at $284^{\circ}K$, characterises it as an interface - like peak. No other distinct peak appears in the TSC



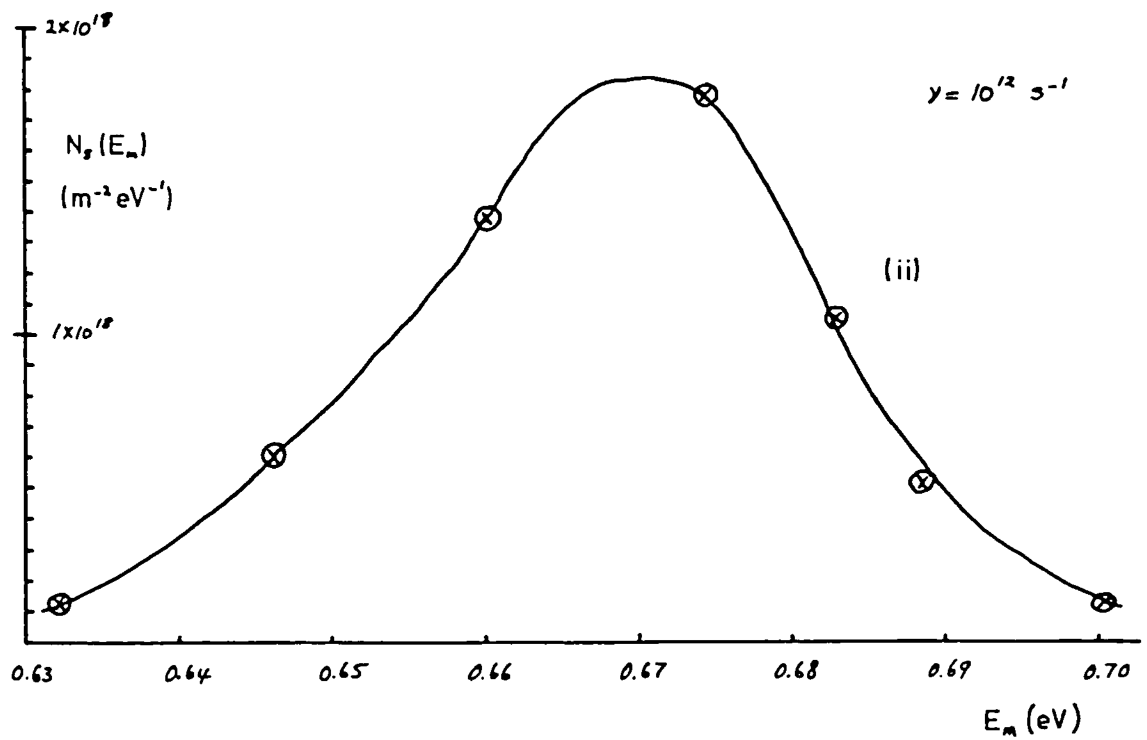


Fig. 53
$CdSe-SiO_2$ interface trap distributions for different values of ν

spectrum of this sample. Increasing V_{g_1} to + 6.4V, as in Fig. 40, results in the merging of this peak with the third, so that the two cannot be distinguished easily - the resulting peak appears as a single peak with a noisy plateau.

This peak appears again when the magnitude of the depleting voltage is changed. In Fig. 41, for instance, when V_{g_2} is - 4.8V, it can be distinguished at about 285.5°K. Lowering V_{g_2} to - 9.6V, as in Fig. 42, results in the two peaks once more appearing very close to one another. Whether the temperatures of the maxima of the two can be distinguished in this case (Fig. 42) is not certain, i.e. it is not certain whether the two peaks are real or due to a noisy plateau which, as will be shown later, the third peak is capable of displaying.

A similar sample was examined in Figs. 45 and 46. In Fig. 45 V_{g_1} was + 9.6V and it was applied at 110°K, for 20 minutes, rather than enhancing initially at room temperature, as was done with the other runs on similar samples. This resulted in the lowering of the maximum current and temperature of this peak so that it became distinguishable from the third peak - T_m of the second peak now appearing at about 280.5°K. This behaviour is the same as that displayed by the distinct interface peak examined in Figs. 43 and 44 and provides evidence to support that this peak is again due to interface traps, since applying V_{g_1} at 110°K, rather than at room temperature, resulted in the filling of less slow states, which resulted in a peak with a lower maximum current.

For Fig. 46 β was lowered to 0.012° s^{-1} and V_{g_1} was + 9.6V, initially applied at room temperature. The peak at about 280.5°K,

in Fig. 45, where β was $0.1^{o}\ s^{-1}$, may have split into the two at 261 and 275°K, in Fig. 46, as a result of lowering β, thus displaying "Anderson splitting". Anderson splitting of a TSC peak predicts, that interface states with a slow as well as a fast component which give a single peak at a particular value of β, may split into two distinct peaks when β is charged. This provides further evidence that the peak is an interface one.

The TSC curve for bad TFTs shows that when the enhancing gate voltage is high enough to ensure the filling of all groups of traps, the peaks which appear are the same as for good TFTs, except for the second, interface peak - this has two humps for its maximum as shown in Figs. 49 and 50. Since this is a feature observed only in bad TFTs, when β is $0.1^{o}\ s^{-1}$, it is concluded that one of these humps is due to the emptying of traps at the CdSe - Cr interface. Since it is only in bad TFTs that these traps contribute to the TSC. This is explained if reference is made to Figs. 17(i) and 17(ii) and section 3.3., where it is shown that a depletion region exists at the CdSe - Cr interface in bad TFTs only, and so it is in these samples, and not good TFTs, that CdSe - Cr traps can give a TSC peak.

The remaining hump would be due to the CdSe-SiO_2 interface traps, since these emit at about this temperature in good TFTs. The identification of the hump due to the CdSe - Cr interface traps was carried out by first applying a small enhancing voltage so that only one of the two humps was observed. This is shown in Fig. 51 where V_{g_1} was + 1.6V. This small gate voltage fills the CdSe - Cr interface traps - a higher value of enhancing voltage being needed to fill the CdSe - SiO_2 interface traps too, hence, these stay empty. It is concluded, therefore, that the single humped second peak at 232°K, in Fig. 51, is due to CdSe - Cr

interface traps and the one at 226°K, in Fig. 50, due to CdSe - SiO_2 ones.

5.3.3. The Third Peak

The third peak has a T_m lying between 290 and 300°K. It develops entirely as a result of - V_g aging, emerging above the background current after the first run, with say a charge of 7.5×10^{-7}C in Fig. 31. Natural - V_g aging increases this to 4.25×10^{-6}C in Fig. 33. and artificial aging to 10.5×10^{-6}C in Fig. 34. These increases show the importance of the depleting gate voltage, in causing the increase in the density of the third peak traps. The effect of - V_g aging is irreversible. The increase in this peak is more pronounced than that in the second, and once developed, the charge associated with the third peak is the largest of all the peaks observed. The growth of this peak means its behaviour in similar to that of the interface, i.e. the origin of the charge released behaves, in this respect, like a surface. Its behaviour is the opposite to that of the bulk peak, since the latter disappears with - V_g aging. A possible unified theory emerges, which accounts for the aging behaviour of all three peaks, if it is assumed that the third peak is due to grain boundary traps. This theory is best explained using the energy band diagrams of Figs. 17 and 18, and bearing in mind that the irreversible increase or decrease of TSC peaks with - V_g aging, is the result of the application of a negative gate voltage. This voltage increases the electric field in the semiconductor depletion region which stretches away from the interface and the grain boundary. In the depletion region, the donor atoms are ionised i.e. positively charged. The direction of the electric field is such that these

will tend to move towards the interface or grain boundary. This movement is made possible by the increased electric field in the depletion regions, when a negative gate voltage is applied, and the rapid diffusion rate of Cd in CdSe. Furthermore, the fact that the existence of excess Cd, giving the donors in CdSe, constitutes a crystal of higher energy - since point defects increase the energy of a crystal - means the crystals of CdSe will tend to eliminate these point defects to minimise energy. The cadmium atoms reaching the interface and grain boundary, introduce additional traps, by disrupting the atomic structure there. This explains the increase in the second and third peaks and the decrease in the first, as in Figs. 29 and 30.

Variations in the initial values of the interface, grain boundary and bulk trap densities between samples, result in the same gate voltage producing an electric field, in the depleting region, which varies from sample to sample. This means that the degree of $- V_g$ aging produced by the same gate voltage, varies between samples. This is supported by experiment, since artificial $- V_g$ aging with the same gate voltage, resulted in the third peak growing to different heights (for instance, compare Figs. 30 and 37).

In TSC runs in the dark, on some samples which had previously undergone $- V_g$ aging, the third peak did not appear, whereas the second did. Shining light on the sample, resulted in the appearance of the third peak, as shown in Figs. 47 and 48. This is explained if it is assumed that in these samples, the field due to the enhancing

gate voltage could control the occupancy of interface traps, but could not penetrate the grain boundary traps in order to help to fill these, since they lie away from the interface. It is also possible that the density of these grain boundary traps filled by the enhancing gate voltage alone, was not high enough to give a TSC which would appear above the background current.

It is likely that in these samples, the initial density of interface traps is large enough for the gate field to be screened from the bulk of the semiconductor. Hence it does not penetrate the film and no aging occurs. Hence in the absence of light, the case in hand is one of either a complete lack of or of partial penetration of the field and control of the occupancy of grain boundary traps. Shining light results in the filling of more grain boundary traps so that their TSC appears above the background current. Shining light while applying an enhancing gate voltage prior to the run, results in the appearance of both peaks, as shown in Fig. 47. Shining light with a small depleting voltage prior to the run, however, results in the reduction in the magnitude of the second peak but the third appears unaltered, as shown in Fig. 48, showing that in these samples the occupancy of grain boundary traps is unaffected by the gate voltage. These experiments also show that the third peak must lie away from the interface, thus providing more evidence to suggest that this peak is due to grain boundary traps, since these fulfil this requirement. The density of the grain boundary traps in this sample is calculated, using the area under the third peak of Fig. 47, and the active grain boundary area given in section 5.1.3. It is 7.5×10^{25} m^{-3}. Also, since the third peak disappeared, if these light experiments were

followed by one in the dark, the third peak was not due to the photochemical creation of traps.

In the sample of Figs. 29 and 30, the third peak did emerge above the background current as a result of $- V_g$ aging, and could be detected in TSC runs in the dark. It was not, however, a very large peak. The density of grain boundary traps is calculated from the third peak of Fig. 30, as $3 \times 10^{26}\ m^{-3}$.

In other samples, the effect of $- V_g$ aging on the growth and the final magnitude of the third peak was very pronounced. This resulted in a very large peak appearing above the background current in TSC runs in the dark. Such a sample was examined in Figs. 35 to 37. In Fig. 35, a negative gate voltage was first applied at room temperature and maintained during cooling and warming up. The third peak was clearly observed. Applying positive gate voltages before warming up, resulted in the wider third peaks of Figs. 36 and 37. These phenomena are explained by associating the third peak once more with grain boundary traps. In Fig. 35 the grain boundary traps away from the interface are screened from, and remain uneffected by, the gate voltage. Grain boundary traps near the interface, however, are emptied by the negative gate voltage before warming up and hence do not contribute to the TSC. In Figs. 36 and 37, however, the grain boundary traps near the interface are also full, and hence contribute to the TSC, by giving a wider third peak. The appearance of this peak at all in Fig. 35, is because the density of grain boundary traps in these samples is so high, that it is the grain boundary region, and not the adjacent semiconductor bulk,

that determines the position of the reference Fermi level of the thin film system. This is explained by comparing the densities of grain boundary and semiconductor bulk traps. The charge released by the third peak in Figs. 35 and 37, is 75×10^{-6} and 85×10^{-6} C, respectively. Assuming the latter is the total grain boundary charge released from the total active grain boundary volume, then the volume density of grain boundary traps is 5×10^{28} m^{-3} i.e. - as high as the density of atoms. Since the volume density of bulk traps is of the order of 10^{24} m^{-3}, the semiconductor film can be thought of as crystallites of relatively low bulk donor density (10^{24} m^{-3}) separated by grain boundaries about 100 Å thick with a much higher trap density (10^{28} m^{-3}). This results in the pinning of the reference Fermi level corresponding to the film as a whole, at the grain boundary. This means that the application of a gate field may move the energy bands of the crystallites by an appreciable amount, compared to the grain boundary where the Fermi level, which coincides with the uppermost filled trap, remains relatively unmoved.

The effect of varying β on the third peak of a sample with a large third peak, is shown in Figs. 45 and 46. It is observed that the temperature of the current maximum is unaffected by the change in the heating rate. The quantitative analysis of such a peak is due to Anderson and appears in the paper by Anderson and Norian. The analysis enables the energy of the centre of the band of traps to be found, from the slope of the graph of the product of the TSC and the temperature, against the reciprocal of the temperature, for the leading edge of the

peak. This has been done for the peak in Fig. 35. The graph appears in Fig. 54 and gives the energy as 0.53 eV. Table 3 gives a corresponding depletion width of about 170 Å into the CdSe on either side of the grain boundary. The analysis mentioned above considers the grain boundary as a plane, and gives the density (from equation (25)) and the energy width (from equation (26)) of grain boundary traps as 2.22×10^{17} m^{-2} eV^{-1} and 0.068 eV, respectively. The density is sufficient to pin the Fermi level at the grain boundary.

These values were calculated using Fig. 55, which shows the experimental curve corresponding to the third peak in Fig. 35 - after the background current has been subtracted - and the corresponding theoretical curve computed by Anderson. It is seen that the theoretical curve agrees very well with the leading edge of the experimental curve. It also predicts a sharp peaking maximum and a sharp cut off. The noisy maxima obtained in practice for this peak (Figs. 33 to 37, 39 and 40) are probably due to the efforts of the chart recorder in trying to respond to this sharply peaking maximum. The shape of Fig. 33 in particular, is in very good agreement with theory. The sharp cut off of the tail of the peak appears in Figs. 31 to 42. The above features give experimental support to Anderson's theoretical predictions.

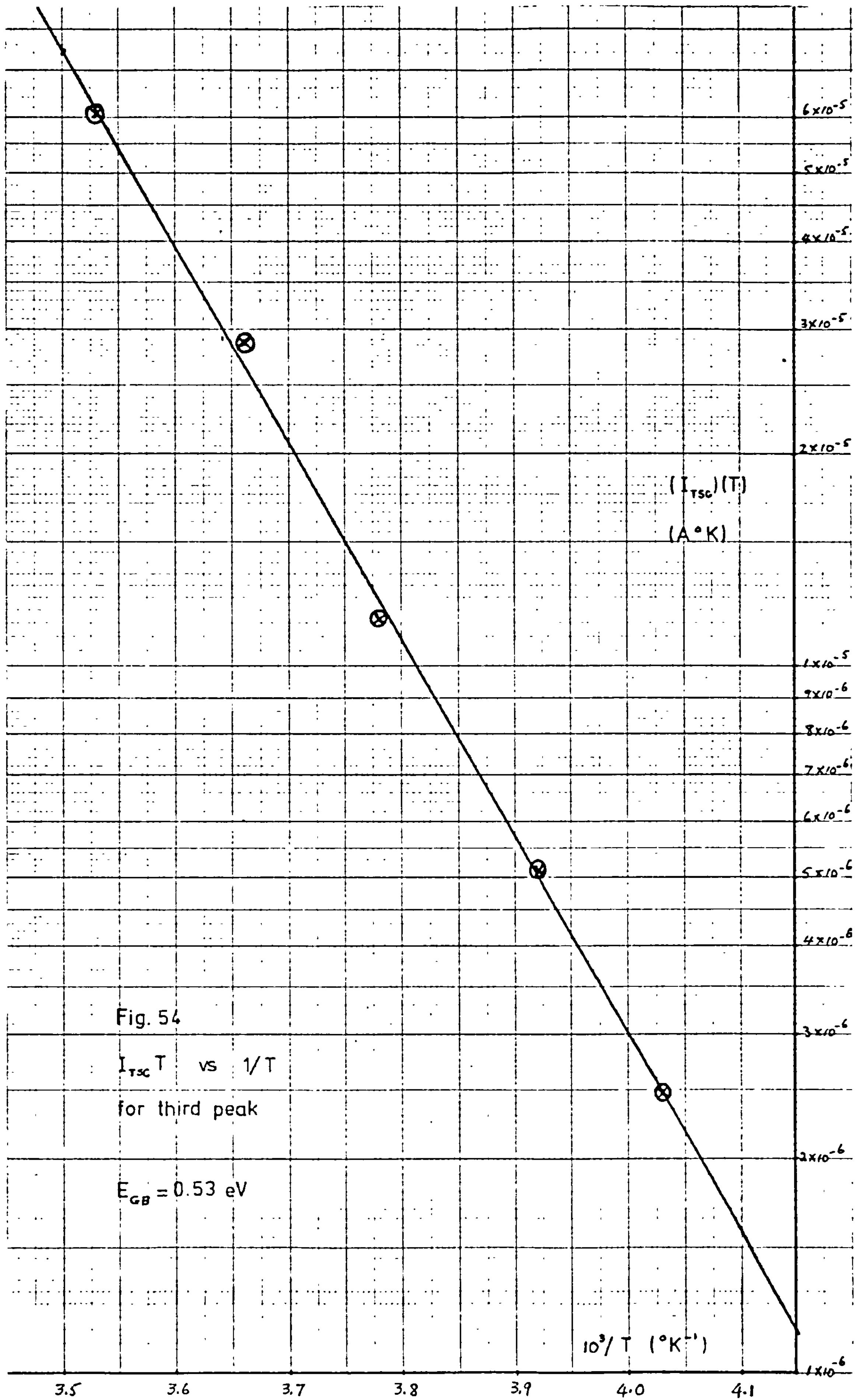


Fig. 54

$I_{TSC}T$ vs $1/T$

for third peak

$E_{GB} = 0.53$ eV

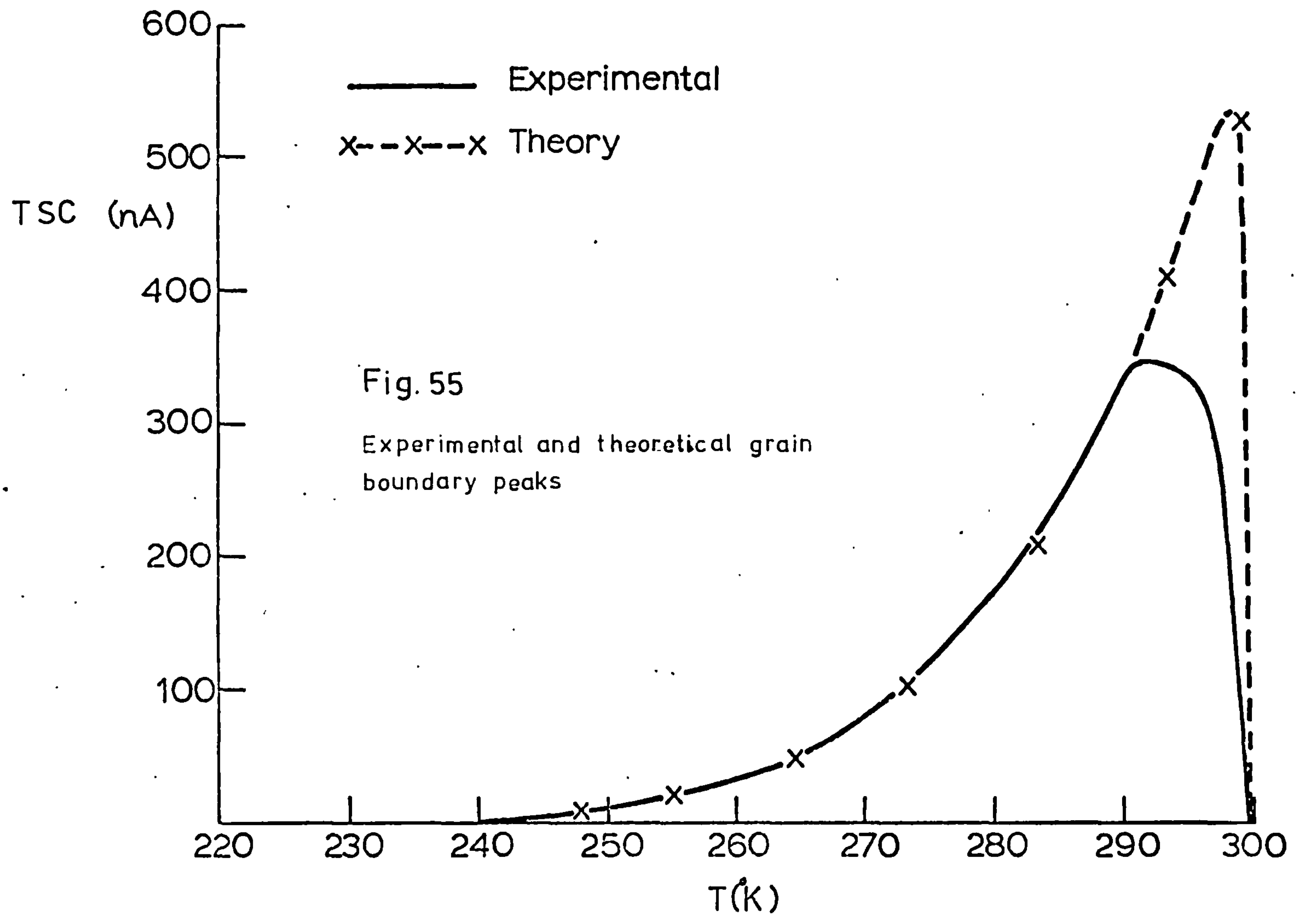


Fig. 55

Experimental and theoretical grain boundary peaks

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CHAPTER VI. CONCLUSION

To produce working TFTs, as-deposited samples have to be annealed at 390°C, for 1¼ hours. An investigation to determine the effect of annealing on the semiconductor shows that both as-grown (i.e. unannealed) and annealed films of CdSe are polycrystalline. Annealing results in the increase of the size of the crystallites. The most significant change in the crystallite size occurs as a result of annealing for 1¼ hours. The pattern which is prominent, in transmission electron micrographs of films annealed for 1¼ hours, is that of a few large crystallites scattered about a background of clusters of smaller ones. The crystallite size distribution in this case is a lognormal one. Annealing for longer times results in small changes in crystallite size. The results show that grain boundary migration is fast up to 1¼ hours of annealing time and slow after this. This can be used to describe the structural changes undergone by the grain boundary, as a result of annealing. For high-angle grain boundaries, the activation energy for grain boundary migration is low i.e. fast migration can occur; for low-angle grain boundaries, the activation energy for migration is high and so slow migration occurs. As-deposited, unannealed films of CdSe are characterised by high-angle grain boundaries and annealing for 1¼ hours converts these to low-angle ones with a high activation energy for migration. The process is one of energy minimisation. Because the atoms in them fit together well, low-angle grain boundaries have low energy and therefore, grain boundaries tend

to become as low-angle as possible, during the process of annealing.

The mean diameter of crystallites, in an as-deposited film of CdSe, is smaller than the thickness of the film. As annealing proceeds, the mean size of crystallites increases and tends to equal the thickness of the film. Annealing for $1\frac{1}{4}$ hours almost equalises the mean size to the thickness, although equalisation is probably not complete unless the annealing time exceeds a period of time of the order of tens of hours. The process is one of minimisation of the surface energy stored at the grain boundaries in the polycrystalline film.

It has been assumed that the annealed TFTs used in the present work, contain polycrystalline semiconductor films, where the crystallites are approximately cubic in shape and of sides equal to the thickness of the films. This is a useful approximation because it means that the grain boundary area depends on the active SiO_2 - CdSe interface area - it equals twice this interface area - and is independent of the thickness of the film. Since the active SiO_2 - CdSe interface area is 5.2×10^{-7} m^2, the total grain boundary area is calculated to be 10.4×10^{-7} m^2. In practice, however, the grain boundary is not a plane, but a volume. It is a region of disorder which may extend up to 50 Å into the adjacent crystallite. This would give a grain boundary volume of 10.4×10^{-15} m^3.

The first TSC run on a good TFT shows two peaks - the first peak, with a maximum at 160°K and the second, usually at about 240°K. During subsequent runs, the area under the first peak diminishes, while the second peak grows and a new peak (the third) appears at about 295°K.

The first peak has been identified as due to donor traps in the CdSe bulk; the second due to SiO_2 - CdSe interface traps and the third due to grain boundary traps. This irreversible change in the TSC curve is caused by the application of a negative gate voltage and is called - V_g aging. The negative gate voltage increases the electric field in the semiconductor depletion regions, which stretch away from the CdSe - SiO_2 interface and the grain boundary. The increased electric field then pushes the positively charged donor ions, which have a rapid diffusion rate in CdSe, out of the depleted CdSe bulk to the interface and the grain boundaries. The cadmium atoms reaching the interface and grain boundaries introduce additional traps, by disrupting the atomic structure there.

The first peak has an activation energy of 0.17 eV, which is the same as that for donors in single crystal CdSe. This identifies the first peak as due to traps in the bulk of CdSe crystallites. The point defects giving these donors are selenium vacancies i.e. excess cadmium on atomic sites.

The density of donors is 2×10^{24} m^{-3}, this leads to two important results. Firstly, since the density of free carriers in the CdSe films used, is of the order of 10^{22} m^{-3}, and it is constant for all temperatures between room temperature and $110^{\circ}K$, it means that the free carriers come from a donor level which is ionised throughout this temperature range and that this level cannot be that at 0.17 eV, because if this were ionised, it would have introduced a free carrier density two orders of magnitude higher than that observed. Hence,

the Fermi level in the CdSe bulk is above the donor level at 0.17 eV and below another which is fully ionised. It is proposed that the latter is that at 0.014 eV observed in earlier investigations and attributed to interstitial cadmium. The position of the Fermi level lies between these two levels and at room temperature is at 0.084 eV.

The second consequence is that, the magnitude of the donor level at 0.17 eV, together with the position of the Fermi level above it means that this level can provide the charge necessary to fill the acceptor type interface and grain boundary traps, while only a fraction of the thickness of the semiconductor crystallites is depleted. By supplying this charge the donors lose their electrons and the width of the depletion region is below 200 Å. Hence, depletion of the semiconductor film throughout its thickness of 1000 Å, is prevented.

In good TFTs the second peak appears if an enhancing gate voltage is applied prior to a TSC run to fill CdSe-SiO_2 interface traps. It disappears if a depleting gate voltage is applied to empty these traps prior to the run. Hence, this peak is due to CdSe-SiO_2 interface traps. The magnitude of this peak increases if the enhancing voltage is maintained for a longer time prior to the run. This shows the important contribution of slow states to this peak - a contribution which seems prominent in the thin film device investigated in the present study. In some samples the interface peak appeared as a distinct peak and in others it was quite close to the third peak. In both cases it gave a single peak when β was $0.1^{o}\ s^{-1}$. Varying β resulted in the splitting of this peak into two distinct peaks. This has been predicted to be

a property of interface states with a slow as well as a fast component. The existence of slow as well as fast interface states means that although fast states are located at the SiO_2 - CdSe plane, the slow ones penetrate about 20 Å inside the SiO_2 and hence the interface is thought of as a volume, rather than a plane. The interface trap density is then given as 3×10^{26} and 6×10^{26} m^{-3} before and after artificial - V_g aging. In samples where the effect of aging is more pronouned, the density is 1×10^{28} m^{-3} i.e. as high as the density of atoms. These trap densities show that - V_g aging damages the structure of the interface. Applying Simmons' fast interface state TSC theory to this peak, gives trap distribution with maximum trap densities at 0.58 and 0.67 eV, for values of ν of 10^{10} and 10^{12} s^{-1} respectively, the density being of the order of 10^{18} m^{-2} eV^{-1}.

The grain boundary peak appears above the background current as a result of - V_g aging. It develops into a large peak if the screening of the gate field from the bulk of the semiconductor, by the interface states, is small. In this case, the gate field can penetrate the bulk of the film and cause heavy aging, increasing the grain boundary trap density to as high as 5×10^{28} m^{-3}. This peak develops into a smaller one if screening is moderate - the density of traps can now be 3×10^{26} m^{-3}. It does not appear above the background current at all, in TSC runs in the dark, if screening is heavy. In this case, the initial density of interface traps is large enough for the gate field to be screened from the bulk of the semiconductor and hence, it does not penetrate the CdSe film and no aging occurs. Shining light on these samples

prior to the TSC run, results in the appearance of the grain boundary peak and the density of traps is then calculated to be 7.5×10^{25} m^{-3}. These volume densities give an estimate of the degree of structural damage caused by the cadmium atoms at the grain boundary.

In the heavily aged samples, the density of grain boundary traps is so high that it is the grain boundary region, and not the adjacent semiconductor bulk, that determines the position of the reference Fermi level of the thin film system. The semiconductor film can be thought of as crystallites of relatively low bulk donor density (10^{24} m^{-3}), separated by grain boundaries about 100 Å thick with a much higher trap density (10^{28} m^{-3}). This results in the pinning of the reference Fermi level corresponding to the film as a whole, at the grain boundary. TSC runs on TFTs with a large grain boundary peak show that, the temperature corresponding to the current maximum does not change with heating rate. The analysis of such a peak gives the energy of the grain boundary traps as 0.53 eV. This corresponds to a depletion region penetrating 170 Å into the adjacent CdSe crystallite. This analysis assumes the grain boundary to be a plane and gives the density and the energy width of grain boundary traps as 2.22×10^{17} m^{-2} eV^{-1} and 0.068 eV respectively. This density is high enough to cause the pinning of the Fermi level at the grain boundary.

Experiments where light was shone on the sample before the TSC run, support the identification of the second peak with CdSe - SiO_2 interface traps and the third with grain boundary ones. Furthermore, shining light on the TFT does not create new peaks and does not increase

the density of the traps mentioned above.

The TSC peaks of bad TFTs are the same as those of good ones, except for the second peak of bad TFTs - this has two humps for its maximum - provided a large enhancing voltage is used prior to the run. Since this is a feature observed only in bad TFTs, when β is $0.1^{o}\ s^{-1}$, and it is only in bad TFTs that CdSe - Cr interface traps contribute to the TSC, one of these two humps is due to the CdSe - Cr interface traps and the other due to the CdSe - SiO_2 interface ones. The application of a small enhancing voltage prior to the TSC run, which results in the filling of the CdSe - Cr interface traps, but not the CdSe - SiO_2 ones, identifies the former as peaking at $232^{o}K$, between the CdSe - SiO_2 interface hump at $226^{o}K$, and the grain boundary peak.

Two proposals for further work arise as a result of the present investigation. The first concerns the CdSe - SiO_2 interface traps. For the energy distribution of these traps to be found, an accurate value of ν must be determined first. This can usually be done by varying the heating rate, but in the case of TFTs these must first be $-V_g$ aged to get reproducible peaks. Furthermore, since slow states exist in the TFT, the waiting time t_w, for which the enhancing gate voltage is applied prior to the TSC run, must be exactly the same for different runs where β varies. The last two requirements were not known at the beginning of the present investigation and as a result, no accurate value of ν has been determined.

The second proposal concerns the further investigation of the shallow donor level within the CdSe bulk. It is known that it must lie

between the Fermi level and the conduction band edge. However, the exact value of the energy of this level is not known. It would be useful to know if this is the 0.014 eV level reported in earlier studies because it can then be identified as due to cadmium interstitials. Since this shallow level is still ionised at the lowest temperature reached in the liquid nitrogen cooled cryostat used in the present investigation, further work to detect its energy can be carried out using a liquid helium cooled cryostat.

APPENDIX A

Interfaces

There are two types of interface of interest in the TFT - that between the amorphous insulator and the polycrystalline semiconductor; and that between the individual grains of the semiconductor i.e. at the grain boundaries.

There is some ambiguity as to what is meant by the interface between two solids. One can draw the analogy between an interface and a surface and hence define the former in the manner of Gibbsian thermodynamics as a dividing plane between two bulk phases. In practice, however, the interface must generally be considered a region because the mutual interaction of the phases is not localised in a plane. The interface, in this sense, is a three-dimensional region of discontinuity between a number of different media in which one or more properties characterising each medium changes (the term medium is used here in a broad sense, and can refer to components, phases, crystallographic orientiation, or simply to a drastic difference in impurity content within a phase). The change usually occurs within a region that is narrow compared to the spatial extent of the system considered but since different properties will, in general, change in different manners, the depth of the interface region, even within a given system, depends on the property under consideration.

A common feature of interfaces is that the more or less perfect periodicity of the crystal potential (taking a single crystal as an example) is disturbed or even completely lost at the interface. Also

the surface atoms are usually displaced from their ideal lattice positions, thus giving rise to a two- or three-dimensional surface structure that deviates from the bulk. All these phenomena lead to the appearance of localised electronic states or traps. In the case of the insulator-semiconductor interface, the fast electron traps are those situated along the Gibbsian plane dividing the two films; slow interface states (which take longer than a millisecond to fill or empty) extend up to approximately 10 to 20 Å inside the insulator away from the Gibbsian interface (A1, A2). As far as grain-boundary traps are concerned, these are confined to a volume which may be about 100 Å wide (A3).

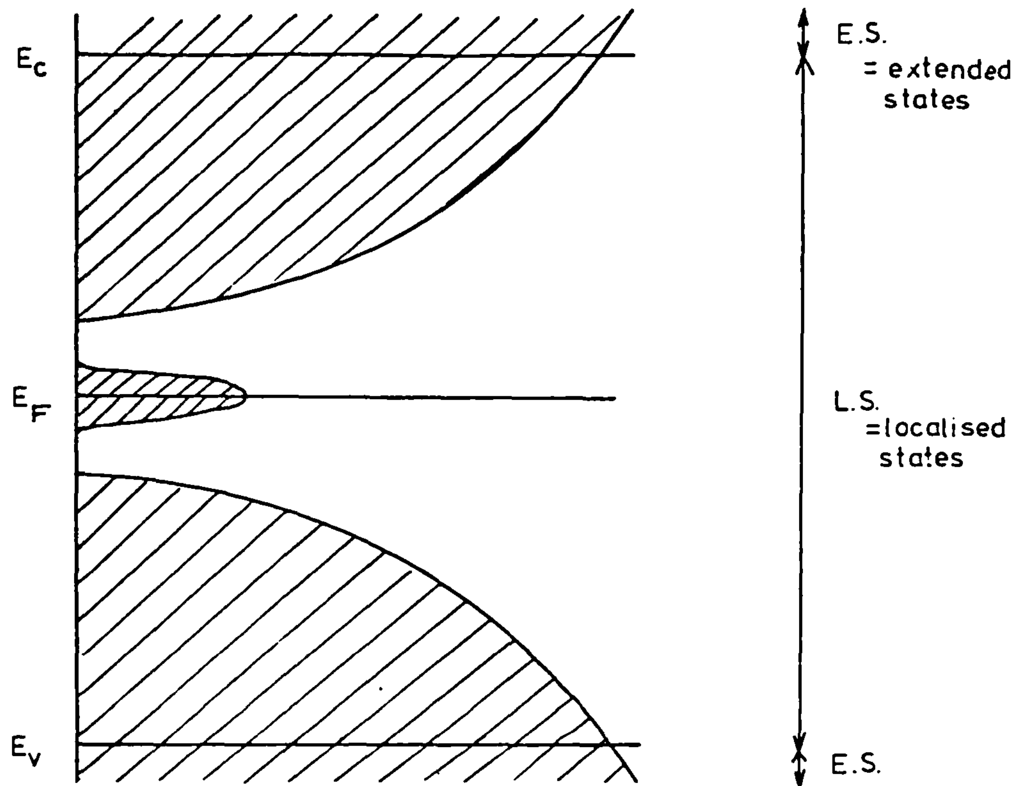
A knowledge, or at least a qualitative understanding of the trap densities and energies, the energy band diagrams and the statistics of electrons at interfaces is a prerequisite to an understanding of interface phenomena. The work is made difficult because our knowledge of the structure dependence of the electronic properties of interfaces is very rudimentary.

APPENDIX B

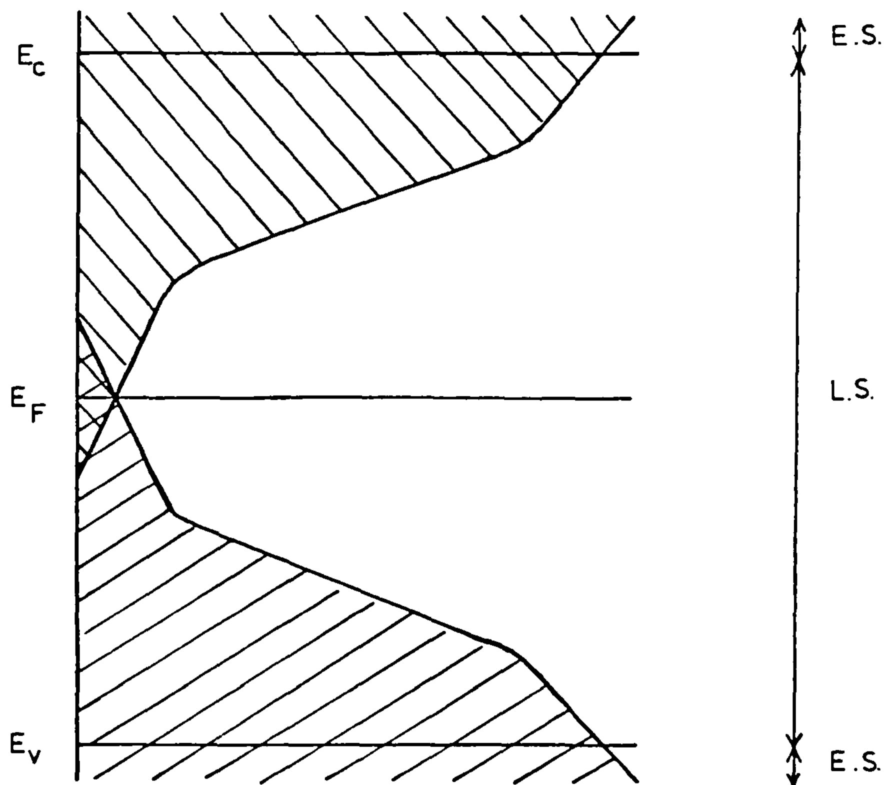
Energy Band Diagram of SiO_2

The energy band diagram of SiO_2 will be that associated with amorphous materials (B1 - B4) where the concept of an energy gap between bands of permitted energy levels (extended states) is replaced by that of a "mobility gap". When an electron has a sufficiently high energy, it occupies extended states characterised by a high mobility; at some critical energy the available levels become localised and the mobility drops abruptly. This fall at a well-defined energy, E_c, is characterised as the "band edge", equivalent to the conduction band edge in a single crystal.

There are two current theoretical models for the distribution of localised states in the mobility gap of an amorphous material. These are shown in Fig. B1. According to Davies and Mott (B5) a fairly narrow band (smaller than 0.1 eV) of localised states exists near the centre of the mobility gap. Cohen et. al. (B6) suggest a different distribution but this will not be gone into because Anderson's work (B7) on the SiO_2 films used in the present work shows, that the distribution of localised states supports the Davies and Mott model. Anderson's work shows that the SiO_2 used is in fact amorphous, since the measured density of states follows the distribution proposed to apply for amorphous insulators with short range order. Furthermore, the absence of any significant additional peaks superimposed on this distribution (which would have arisen if impurities and imperfections were present to disrupt short range order) suggests a material with



(i)



(ii)

Fig. B1

Distribution of localised states in the mobility gap of the insulator according to (i) Mott and Davies (ii) Cohen, Fritzsche and Ovshinsky

a high degree of short range order barely disrupted by imperfections.

APPENDIX C

Effect of Interface States on Energy Band Diagram

Fig. 10(i) of section 3.2.2 shows the MIS device with the interface and semiconductor in equilibrium with no gate voltage. The potential profile near the interface is an effect of the interface states as explained by Simmons (C1).

The interface states of density N_I (per unit area per unit energy) are assumed to be uniformly distributed throughout the energy gap of the semiconductor. Fig. C1(i) shows the energy diagram before the interface states reach equilibrium with the semiconductor bulk. When filled up to an energy E_o below the bottom of the conduction band edge, the interface is assumed to be electrically neutral, i.e. E_o is the Fermi level of the interface states. However, since the Fermi level associated with the interface states should coincide with that of the bulk, electrons from the conduction band fill up additional interface states up to ϕ_o. The result is that a sheet of negative charge resides on the surface and a positive space charge (depletion region) of depth λ_o exists just inside the semiconductor bulk (Fig. C1(ii)). This double-charge layer causes the conduction band to bend upwards until the highest filled interface state coincides with the Fermi level of the bulk.

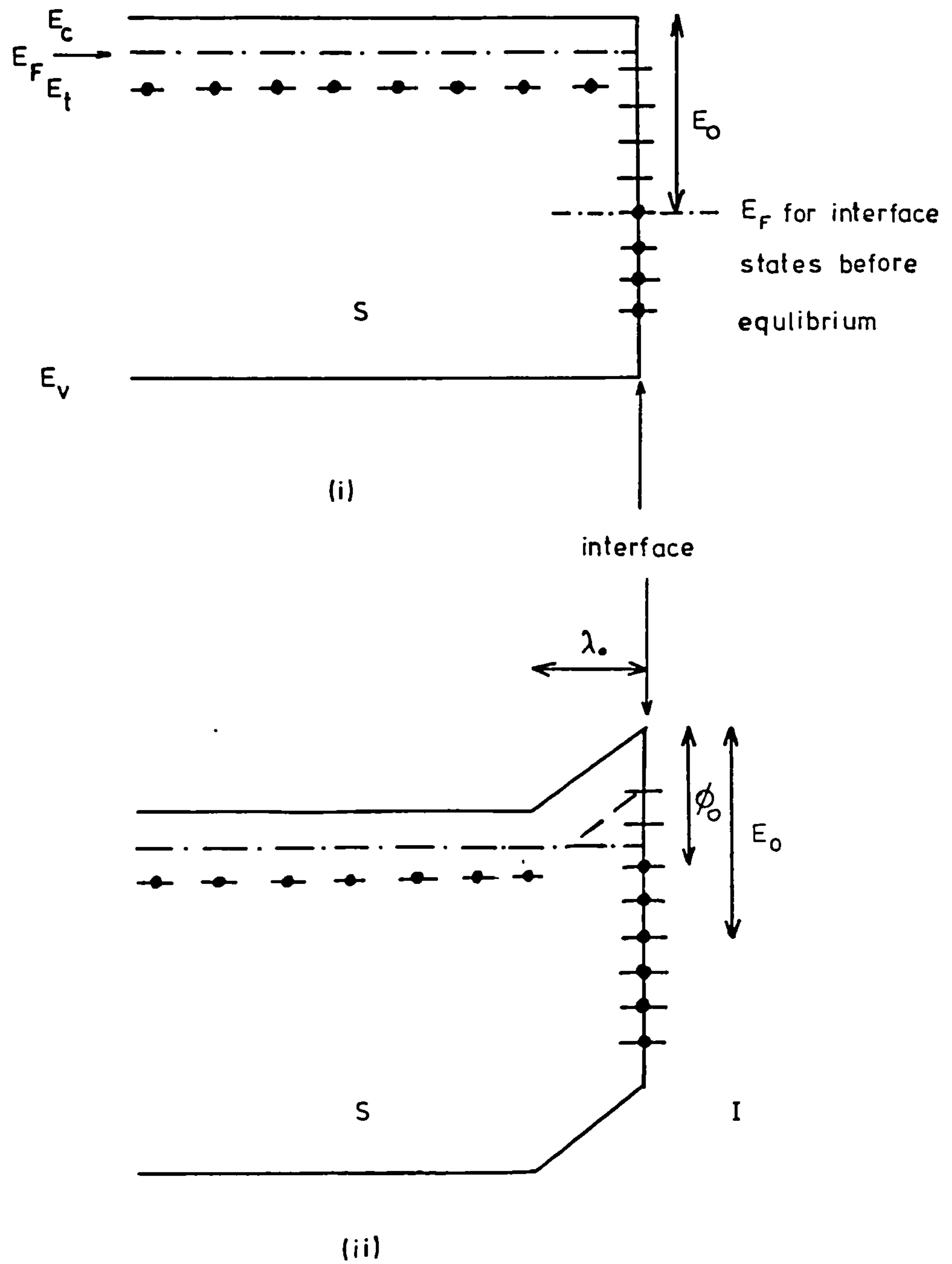


Fig. C1

Energy diagram showing the interface states (i)before,(ii)after they reach equilibrium with the semiconductor bulk

APPENDIX D

Equilibrium Steady-State; Nonequilibrium Steady-State and Nonequilibrium Non-Steady-State Statistics

Simmons, Taylor and Mar (D1, D2) have used Shockley-Read statistics (D3) to describe the occupancy of traps during the TSC run when "nonequilibrium non-steady-state" conditions prevail.

D(i) Equilibrium Steady-State Phenomena

The material is in the dark and all Fermi levels within the system have aligned. This represents the equilibrium situation. All free carriers have been thermally generated and they have made enough collisions for them to obey Fermi-Dirac or Maxwell-Boltzmann statistics.

Consider a trap at energy E_t and density N_t per unit volume. Four processes determine the trap occupancy of a discrete trapping level (see Fig. D1). Process a is the capture of electrons from the conduction band by the trap; its rate is

$$r_a = \upsilon \, \sigma_n \, n \, N_t \, (1-f) \qquad \text{(D1)}$$

where n is the free-electron density in the conduction band, υ is the thermal velocity of the electrons, σ_n is the capture cross-section of the trap for electrons and f is the probability of occupation of the trap level.

Process b is the rate of emission of electrons from the trap and its rate is

$$r_b = e_n \, N_t \, f \qquad \text{(D2)}$$

where e_n is the emission probability from the trap for electrons. Process c is the capture of holes from the valence band; its rate is

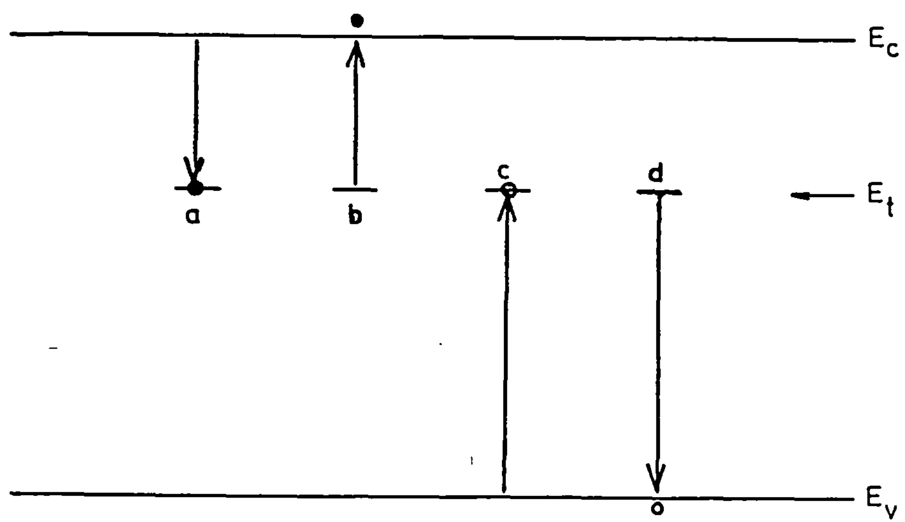


Fig. D1

Transitions taking place under equilibrium conditions

$$r_c = \upsilon\sigma_p \, p \, N_t \, f \tag{D3}$$

where p is the free hole density in the valence band and σ_p the capture cross-section for holes. Process d is the rate of emission of holes to the valence band given by

$$r_d = e_p \, N_t \, (1-f) \tag{D4}$$

where e_p is the probability of hole emission from the trap.

Since the system is in equilibrium the Fermi-Dirac occupancy function can be used i.e.

$$f = \frac{1}{1+\exp[(E_t-E_F) \, / \, kT]} \tag{D5}$$

where E_F is the equilibrium Fermi level. Furthermore, in thermal equilibrium, the rate of electron emission equals the rate of electron capture i.e.

$$r_b = r_a \tag{D6}$$

Hence

$$e_n = \upsilon\sigma_n \, n \, \exp[(E_t - E_F) \, / \, kT] \tag{D7}$$

But if

$$E_c - E_F >> kT \tag{D8}$$

Boltzmann statistics give

$$n = N_c \, \exp[\, - \, (E_c - E_F) \, / \, kT \,] \tag{D9}$$

where N_c is the effective density of states in the conduction band. Hence (D7) and (D9) give

$$e_n = \upsilon\sigma_n \, N_c \, \exp[(E_t - E_c) \, / \, kT \,] \tag{D10}$$

Similarly, the rate of hole emission equals the rate of hole capture. This gives

$$e_p = \upsilon\sigma_p \, N_v \, \exp[(E_v - E_t) \, / \, kT \,] \tag{D11}$$

ν_n is defined as the attempt-to-escape frequency for electrons and ν_p that for holes where

$$\nu_n = \upsilon\sigma_n N_c \tag{D12}$$

$$\nu_p = \upsilon\sigma_p N_v \tag{D13}$$

Hence

$$e_n = \nu_n \exp[(E_t - E_c)/kT] \tag{D14}$$

$$e_p = \nu_p \exp[(E_v - E_t)/kT] \tag{D15}$$

D(ii) Nonequilibrium Steady-State Statistics

Consider now the case of a semiconductor or insulator having an arbitrary distribution of traps N(E) per unit volume per unit energy throughout the energy gap, when the solid is uniformly illuminated resulting in a constant generation rate per unit volume G of electron-hole pairs (Fig. D2). A nonequilibrium situation now exists and the occupancy of states cannot be expressed in terms of Fermi-Dirac statistics. The concentration of free carriers is not the equilibrium one when the material was in the dark and these were thermally generated. The system is still in the steady-state, however, with all Fermi levels aligned and no transient currents flowing if the circuit is completed.

The nonequilibrium steady-state occupancy, f(E), is now derived. In this condition, the occupancy of any trap is constant and thus the four processes which fill and empty the trap are in balance. Therefore,

$$r_a - r_b - r_c + r_d = 0 \tag{D16}$$

substituting

$$\upsilon\sigma_n n N(E)[1-f(E)] - e_n N(E) f(E) - \upsilon\sigma_p p N(E) f(E) + e_p N(E)[1-f(E)] = 0 \tag{D17}$$

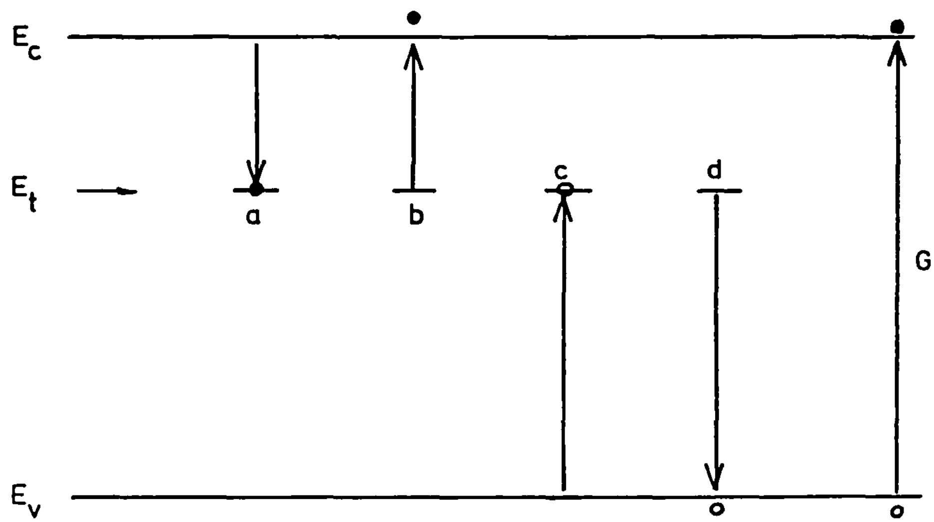


Fig. D2

Transitions taking place under nonequilibrium conditions

Let

$$\bar{n} = \upsilon\sigma_n n \tag{D18}$$

$$\bar{p} = \upsilon\sigma_p p \tag{D19}$$

Hence (D17) gives

$$f(E) = \frac{\bar{n} + e_p}{e_n + \bar{n} + \bar{p} + e_p} \tag{D20}$$

To plot f(E) it is noted that since by equations (D7) and (D18)

$$e_n = \bar{n} \exp[(E_t - E_F)/kT] \tag{D21}$$

and similarly

$$e_p = \bar{p} \exp[(E_F - E_t)/kT] \tag{D22}$$

above the equilibrium Fermi level E_F

$$e_p << e_n, \bar{n}, \bar{p} \tag{D23}$$

Hence equation (D20) becomes

$$f(E) = \frac{\bar{n}}{e_n + \bar{n} + \bar{p}} \tag{D24}$$

This can be expressed as

$$f(E) = \frac{\bar{n}}{\bar{n} + \bar{p}} \left\{ \frac{1}{1 + \exp[(E_t - E_{F_t}^n)/kT]} \right\} \tag{D25}$$

Hence, for the case in hand, f(E) has a modulated Fermi-Dirac form about an energy $E_{F_t}^n$. The quantity in the braces in equation (D25) will be recognised as the Fermi-Dirac function about an energy $E_{F_t}^n$.

The modulating factor $\left(\frac{\bar{n}}{\bar{n} + \bar{p}}\right)$ is a constant for a given light intensity. As a result of equation (D25) Simmons defines $E^n_{F_t}$ as the quasi-Fermi level for trapped electrons. This is because traps with energy greater than $E^n_{F_t}$ are essentially empty and below $E^n_{F_t}$ they are substantially occupied according to an occupancy given by

$$f(E) = \frac{\bar{n}}{\bar{n} + \bar{p}} \tag{D26}$$

The above enables f(E) to be sketched from E_c to E_F.

To complete the sketch between E_c and E_v, conditions below E_F must be considered where

$$e_n << e_p, \bar{n}, \bar{p} \tag{D27}$$

Hence, equation (D20) becomes

$$f(E) = \frac{\bar{n} + e_p}{e_p + \bar{p} + \bar{n}} \tag{D28}$$

which can be written as

$$1-f(E) = \frac{\bar{p}}{\bar{n} + \bar{p} + e_p} \tag{D29}$$

and leads to a Fermi-Dirac function for holes about $E^p_{F_t}$, the quasi-Fermi level for trapped holes. It enables the sketch of the occupancy of traps in the nonequilibrium steady-state condition to be completed (see Fig. D3).

An alternative derivation of the general occupancy function (equation D20) is the following. The electrons in the conduction band are first considered. In the nonequilibrium steady-state case,

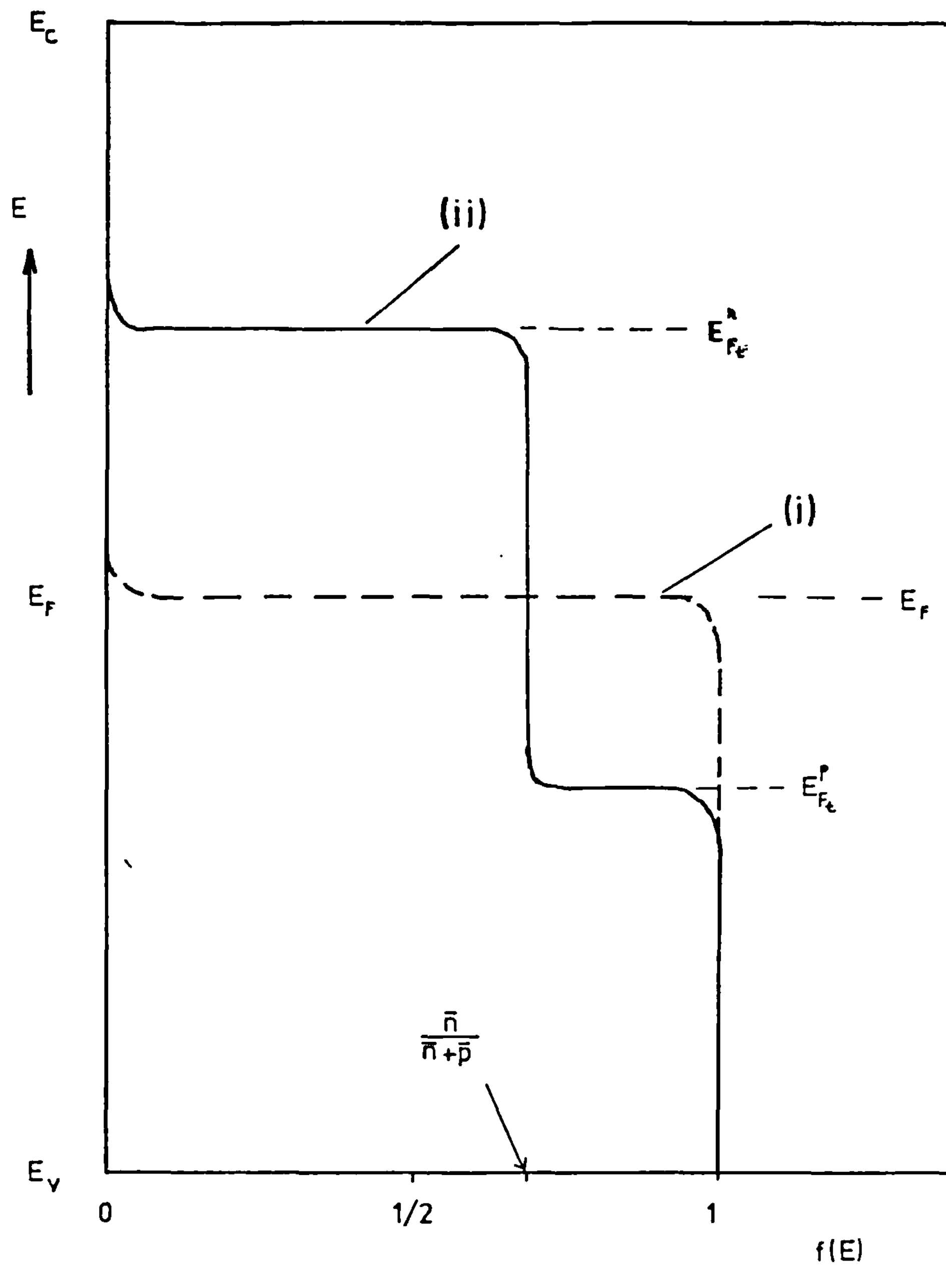


Fig. D3

Occupation function for an arbitrary distribution of traps (i) before (ii) after excitation.

the rate at which electrons enter the conduction band equals the rate at which electrons leave it. Hence

$$\frac{dn}{dt} = G - \int_{E_v}^{E_c} r_a \, dE + \int_{E_v}^{E_c} r_b \, dE = 0 \tag{D30}$$

Similarly, the rate at which holes leave the valence band equals the rate at which holes enter the valence band; that is

$$\frac{dp}{dt} = G - \int_{E_v}^{E_c} r_c \, dE + \int_{E_v}^{E_c} r_d \, dE = 0 \tag{D31}$$

where E_c and E_v are the energies corresponding to the bottom of the conduction band and the top of the valence band respectively. Equations (D30) and (D31) lead to equation (D16) and hence to equation (D20). It is worth noting that if the system is allowed to relax to the equilibrium steady-state

$$G = 0 \tag{D32}$$

Then equations (D30) and (D31) would give

$$r_a = r_b; \; r_c = r_d \tag{D33}$$

used in the equilibrium steady-state situation discussed previously.

D(iii) Nonequilibrium Non-Steady-State

The nonequilibrium non-steady-state situation arises at low temperature at the interface between the insulator and semiconductor of the TFT, when the device is switched from the accumulation to the depletion mode. This situation is a nonequilibrium one because the Fermi level corresponding to the interface traps is not aligned with the system or reference Fermi level. However, these two levels tend to align - although very slowly at the initial low temperature - and in doing so electrons formerly trapped in interface traps are released. These electrons give

rise to a transient current and so the situation has been called a non-steady-state one by Simmons. In this situation the system or reference Fermi level is defined as the Fermi level in the system with which all other Fermi levels (corresponding to the uppermost filled energy of a group of traps say) will be aligned in thermal equilibrium.

To account for the non-steady-state nature of the case in hand, in addition to the four emission and capture rates r_a, r_b, r_c and r_d, a time varying occupancy is introduced. This is because the occupancy f(E) is no longer constant and the difference between the four emission and capture processes is related to the rate of change of the occupancy with time, i.e.

$$(r_a - r_b) - (r_c - r_d) = \frac{d}{dt} N(E)\ f(E) \tag{D34}$$

$$\bar{n}\, N(E)[\,1-f(E)\,] - e_n\, N(E)\, f(E) - \bar{p}\, N(E)\, f(E) + e_p\, N(E)[\,1-f(E)] = N(E) \frac{d}{dt} f(E) \tag{D35}$$

$$\frac{d}{dt} f(E) = (\bar{n} + e_p) - (e_n + e_p + \bar{n} + \bar{p})\, f(E) \tag{D36}$$

(D36) is the differential equation giving the occupancy of traps in the nonequilibrium non-steady-state case.

APPENDIX E

Electrometer Circuit Analysis

Consider the feedback - type electrometer of Fig. 26. The input current I_{in} cannot flow into the amplifier because of its high input resistance and low input bias current. Therefore, it must entirely flow through the feedback resistor R_f. Furthermore, the input current is usually small compared to the current flowing through R_a and R_b. The voltage drop across R_f is given by $I_{in}R_f$ and the circuit analysis shows that

$$e_1 - I_{in}R_f = \left(\frac{R_b}{R_a + R_b}\right)e_o \qquad \text{(E1)}$$

Also

$$e_o = A(-e_1) \qquad \text{(E2)}$$

Combining equations (E1) and (E2) and remembering that A, the open loop gain of the amplifier, is very large and hence

$$\frac{1}{A} << \frac{R_b}{R_a + R_b} \qquad \text{(E3)}$$

gives

$$e_o = -\left(\frac{R_a + R_b}{R_b}\right) I_{in}R_f \qquad \text{(E4)}$$

Thus the output voltage, e_o, is a measure of the input current. Sensitivity is determined by the "ranging resistor" R_f and the "multiplier"

combination of R_a and R_b. It was found best to use the multiplier on 1 i.e. $R_a = 0$. This was because then the current measured was less noisy than with the more sensitive multiplier ranges. Then equation (E4) gives

$$R_f = -\frac{e_o}{I_{in}} \tag{E5}$$

Hence, for an output voltage from the electrometer of unity at full scale deflection, the value of the feedback resistor chosen must be the reciprocal of the current.

APPENDIX F

Position of the Fermi Level

When electrons originating from donors far exceed those excited across the gap

$$N_d >> n_i \tag{F1}$$

Also, when all donors are ionised

$$n_b = N_d \tag{F2}$$

Under these conditions the electron density is essentially a constant, independent of temperature. The position of the Fermi level can be determined using the charge neutrality condition.

$$n_b^- = N_d^+ \tag{F3}$$

$$N_c \exp[-(E_c - E_F)/kT] = N_d \tag{F4}$$

giving

$$E_c - E_F = kT \ln \left(\frac{N_c}{N_d}\right) \tag{F5}$$

where N_c is the effective density of states in the conduction band given by

$$N_c = 2 \left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{F6}$$

The other symbols have their usual meaning.

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