SOME THEORETICAL ASPECTS OF IMMITTANCE CONVERSION AND INVERSION IN THE CONTEXT OF ACTIVE RC NETWORKS

by

Manuel de Medeiros Silva

A Thesis submitted for the
Degree of Doctor of Philosophy
of the University of London

September 1976

Electrical Engineering Department
Imperial College of Science and Technology
London S.W.7

ABSTRACT

Two-port immittance (i.e. impedance or admittance) converters and inverters are important active units used, in signal processing applications, for the realization of active RC networks suitable for microelectronic implementation. In this thesis a generalization to multiports of the concepts of 2-port converters and inverters is proposed, the special case of 3-port converters and inverters suitable for floating inductor simulation is studied in some detail, the realization of inverters with a minimum number of active components is discussed, and the concept of anti-reciprocity (which has close associations with converters and inverters) is investigated.

According to the proposed generalization, conversion and inversion, which are scalar operations when performed by 2-ports, become matrix operations, when performed by multiports. One consequence is that a distinction, which does not exist for 2-ports, has to be made between multiport admittance and impedance converters or inverters.

Most of the circuits used for the active RC simulation of floating inductors can be interpreted as 3-port admittance inverters or converters. A classification of these inverters and converters, based on their terminal description (as distinct from their port description), is developed, which clarifies the relationships between known realizations and shows the possibility of new ones.

It is known that 2-port positive inverters containing resistors and only one operational amplifier can be realized if only one port is grounded. It is proved that this is impossible if both ports are grounded (a similar restriction concerning positive inverters using only one ideal

transistor is also proved). The consequences of this conclusion regarding the realization of 3-port inverters are examined.

Some converters and inverters (e.g. the gyrator) have been regarded as possessing a kind of extreme non-reciprocity or "anti-reciprocity". It is pointed out that two existing definitions of anti-reciprocity are incompatible. An investigation of this question leads to the introduction of a "complete set" of network properties related to the concept of reciprocity. Various rules concerning the interconnection of multiports possessing these properties are derived. A generalization of the definitions of reciprocity and anti-reciprocity is presented, and the consequences of the proposed generalization are evaluated.

ACKNOWLEDGEMENTS

I wish to express my deepest gratitude to Dr. W. Saraga for his advice and encouragement throughout every stage of the work reported in this thesis. Dr. Saraga has always been, not only an extremely kind and helpful supervisor, but also a very good friend. His contagious enthusiasm, patient guidance and friendly encouragement had a decisive influence in the work that led to the present thesis.

The work reported here has benefited from many helpful discussions with various members of the Communication Section. Particular mention is due to Mr. D. Haigh, Dr. A. G. Constantinides, Dr. R. Spence and Mr. D. Perry.

The encouragement provided by my colleagues and friends, especially Mr. R. W. Turpin, M. Ahmadi, M. Buckley, R. Galvão, K. Karna, D. Horn and N. Esteves is gratefully acknowledged.

I would like to express my gratitude to my colleague Mr. H. Abreu Santos who has been my representative in Lisbon during my absence, and to Dr. F. Borges da Silva who first stimulated my interest for Network Theory.

The work reported in this thesis was done while the author was on leave from Instituto Superior Técnico, Lisbon, supported by a grant from INVOTAN.

TABLE OF CONTENTS

TITLE PAGE ..... p. 1

ABSTRACT ..... p. 2

ACKNOWLEDGEMENTS ..... p. 4

TABLE OF CONTENTS ..... p. 5

NOTATION ..... p. 10

LIST OF FIGURES ..... p. 12

LIST OF TABLES ..... p. 17

CHAPTER 1 - INTRODUCTION

1.1 - IMMITTANCE CONVERTERS AND INVERTERS - GENERAL CONSIDERATIONS ..... p. 18

1.2 - OUTLINE OF THE THESIS ..... p. 20

1.3 - STATEMENT OF ORIGINALITY ..... p. 21

CHAPTER 2 - REVIEW OF SOME BASIC CONCEPTS

2.1 - MULTIPORTS

Definition ..... p. 23

General description of n-ports ..... p. 25

Hybrid descriptions ..... p. 28

Well-defined multiports ..... p. 29

Scattering description ..... p. 31

Separation of the ports into two sets: (n+k)-ports p. 35

2.2 - NULLORS

Nullators, norators and nullors ..... p. 39

Ideal transistors and ideal operational amplifiers .. p. 45

Node analysis of networks containing nullors ..... p. 47

2.3 - RESISTIVE MULTIPORTS ..... p. 50

2.4 - ACTIVITY ..... p. 52

2.5 - INTERRECIPROCITY

Interreciprocal multiports ..... p. 54

Interreciprocity of well-defined multiports ..... p. 57

The interreciprocity theorem ..... p. 59

Reciprocal multiports ..... p. 60

CHAPTER 3 - REVIEW OF 2-PORT IMMITTANCE CONVERSION AND INVERSION IN THE CONTEXT OF ACTIVE RC NETWORKS

3.1 - ACTIVE RC NETWORKS ..... p. 63

3.2 - SIMULATION OF DOUBLY TERMINATED LC LADDER FILTERS .... p. 67

3.3 - TWO-PORT CONVERTERS AND INVERTERS ..... p. 73

3.4 - ACTIVE REALIZATION OF CONVERTERS AND INVERTERS ..... p. 80

3.5 - SIMULATION OF GROUNDED AND FLOATING INDUCTORS ..... p. 88

3.6 - THE (ad, bc)-PLANE ..... p. 96

CHAPTER 4 - MULTIPORT CONVERTERS AND INVERTERS

4.1 - INTRODUCTION ..... p. 99

4.2 - DEFINITIONS ..... p. 101

4.3 - MATRIX DESCRIPTION ..... p. 104

4.4 - THE DIFFERENCE BETWEEN 'ADMITTANCE' AND 'IMPEDANCE' CONVERTERS AND INVERTERS ..... p. 108

4.5 - SOME PROPERTIES OF MULTIPORT CONVERTERS AND INVERTERS ..... p. 111

4.6 - MULTIPORT TRANSFORMERS AND GYRATORS ..... p. 113

4.7 - FLOATING INDUCTOR SIMULATION ..... p. 115

4.8 - HYBRID CONVERTERS ..... p. 120

4.9 - CONCLUSIONS ..... p. 122

APPENDIX ..... p. 124

CHAPTER 5 - REALIZATION OF MULTIPORT CONVERTERS AND INVERTERS USING 2-PORT CONVERTERS AND INVERTERS

5.1 - INTRODUCTION ..... p. 125

5.2 - A SIMPLIFIED REPRESENTATION OF THE INTERCONNECTION OF MULTIPORTS ..... p. 126

5.3 - REALIZATION OF WELL-DEFINED MULTIPORTS USING 2-PORTS ..... p. 130

5.4 - REALIZATION OF MULTIPORT CONVERTERS AND INVERTERS ..... p. 136

5.5 - MULTIPORT CONVERTERS AND INVERTERS USING GROUNDED 2-PORT CONVERTERS AND INVERTERS ..... p. 141

5.6 - CONCLUSIONS ..... p. 144

CHAPTER 6 - A CLASSIFICATION OF 3-PORT INVERTERS AND CONVERTERS USED IN THE SIMULATION OF FLOATING INDUCTORS

6.1 - INTRODUCTION ..... p. 149

6.2 - TERMINAL DESCRIPTION OF 3-PORT INVERTERS FOR FLOATING INDUCTOR SIMULATION ..... p. 152

6.3 - FOUR-TERMINAL INVERTERS ..... p. 156

6.4 - FLOATING INVERTERS ..... p. 158

6.5 - FLOATING 3-TERMINAL INVERTER ..... p. 162

6.6 - THE 'GENERAL' INVERTER ..... p. 164

6.7 - THREE-PORT CONVERTERS FOR FLOATING INDUCTOR SIMULATION ..... p. 169

6.8 - A FAMILY OF 3-PORT INVERTERS USING 3 OPERATIONAL AMPLIFIERS ..... p. 174

6.9 - CONCLUSIONS ..... p. 181

CHAPTER 7 - INVERTERS WITH A MINIMUM NUMBER OF ACTIVE COMPONENTS

7.1 - INTRODUCTION ..... p. 184

7.2 - A REVIEW OF POSITIVE INVERTERS WITH A MINIMUM NUMBER OF ACTIVE COMPONENTS ..... p. 186

7.3 - THE ADMITTANCE PARAMETERS OF A GROUNDED 2-PORT CONTAINING RESISTORS AND ONE OPERATIONAL AMPLIFIER ..... p. 195

7.4 - ON THE REALIZATION OF VARIOUS TYPES OF INVERTERS USING OPERATIONAL AMPLIFIERS ..... p. 204

7.5 - ON THE REALIZATION OF POSITIVE INVERTERS USING TRANSISTORS

Proof of the non-realizability of grounded positive inverters with one transistor ..... p. 207

An unsolved question ..... p. 213

7.6 - CONCLUSIONS ..... p. 216

CHAPTER 8 - A SET OF NETWORK PROPERTIES RELATED TO THE CONCEPT OF RECIPROCITY

8.1 - INTRODUCTION ..... p. 218

8.2 - RECIPROCITY ..... p. 220

8.3 - TWO TYPES OF ANTI-RECIPROCITY ..... p. 227

8.4 - BIRECIPROCITY ..... p. 234

8.5 - ANTI-BIRECIPROCITY ..... p. 236

8.6 - THE MEANING OF BIRECIPROCITY AND ANTI-BIRECIPROCITY ..... p. 238

8.7 - CASCADE CONNECTION OF VARIOUS TYPES OF MULTIPORTS ... p. 241

8.8 - MULTIPORT TRANSFORMERS AND GYRATORS ..... p. 244

8.9 - THE DETERMINANT OF THE TRANSMISSION MATRIX ..... p. 247

8.10 - RELATIONSHIPS WITH PASSIVITY AND ACTIVITY ..... p. 248

8.11 - CONCLUSIONS ..... p. 249

CHAPTER 9 - A GENERALIZATION OF RECIPROCITY AND ANTI-RECIPROCITY

9.1 - INTRODUCTION ..... p. 251

9.2 - GENERALIZED RECIPROCITY ..... p. 252

9.3 - GENERALIZED ANTI-RECIPROCITY ..... p. 259

9.4 - THE SPECIAL CASE OF (n + n)-PORTS ..... p. 262

9.5 - MISCELLANEOUS COMMENTS

Partition of ports into two sets ..... p. 264

The meaning of α ..... p. 265

Unilateral (n + k)-ports ..... p. 268

Multiport Converters and Inverters ..... p. 269

On the possibility of a further generalization ..... p. 270

9.6 - CONCLUSIONS ..... p. 272

CHAPTER 10 - CONCLUSIONS

10.1 - SUMMARY OF THE MAIN RESULTS ..... p. 275

10.2 - SUGGESTIONS FOR FURTHER WORK ..... p. 279

REFERENCES ..... p. 282

NOTATION

In this thesis matrices and vectors are denoted by capital letters and scalars by small letters. However, R, L and C are used to denote resistance, inductance and capacitance, respectively. The unit matrix of order n is denoted by 1_n; the subscript will be omitted when evident from the context. Zero matrices are denoted by O. A^t denotes the transpose of A and det A denotes the determinant of A.

The literal symbols corresponding to network variables (currents, voltages, scattering parameters) denote the Laplace-transformed or frequency-domain representation of these variables; for example,

$$I = \begin{bmatrix} i_1 \\ i_2 \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix}$$

denotes the vector of the Laplace-transformed currents. The instantaneous or time-domain values are denoted by indicating explicitly the dependence of time (t); for example,

$$I(t) = \begin{bmatrix} i_1(t) \\ i_2(t) \\ \cdot \\ \cdot \\ \cdot \\ i_n(t) \end{bmatrix}$$

Several auxilliary matrices are used in the thesis to write some equations in a compact form. Those that are used in more than one section are listed below:

$$\Theta = \begin{bmatrix} 1_n & 0 \\ 0 & -1_k \end{bmatrix}$$

$$\Phi = \begin{bmatrix} 0 & 1_n \\ -1_n & 0 \end{bmatrix}$$

$$\Psi = \begin{bmatrix} 0 & 1_n \\ 1_n & 0 \end{bmatrix}$$

$$\Theta_\alpha = \begin{bmatrix} 1_n & 0 \\ 0 & \alpha 1_k \end{bmatrix}$$

LIST OF FIGURES

Fig. 2-1 : A port ..... p. 24

Fig. 2-2 : An n-port ..... p. 24

Fig. 2-3 : An n-port with n+1 terminals ..... p. 24

Fig. 2-4 : An (n+k)-port ..... p. 36

Fig. 2-5 : Nullator, norator and nullor ..... p. 40

Fig. 2-6 : Equivalences of 2-terminal networks containing nullators and norators ..... p. 43

Fig. 2-7 : Equivalences of 3-terminal networks containing nullators and norators ..... p. 44

Fig. 2-8 : A nullor equivalence ..... p. 44

Fig. 2-9 : Nullor model of the ideal transistor ..... p. 46

Fig. 2-10: Nullor model of the ideal operational amplifier .. p. 46

Fig. 2-11: An n+1-node network with one nullor ..... p. 49

Fig. 2-12: Realization of a dominant matrix as the admittance matrix of an n-port with 2n terminals ..... p. 53

Fig. 2-13: The two n-ports in the definition of interreciprocity ..... p. 55

Fig. 3-1 : Linvill's method ..... p. 66

Fig. 3-2 : Cascaded second order sections ..... p. 66

Fig. 3-3 : Doubly terminated LC ladder network ..... p. 66

Fig. 3-4 : Active RC simulation of grounded and floating inductors ..... p. 69

Fig. 3-5 : Application of the impedance scaling method to a low-pass filter ..... p. 70

Fig. 3-6 : Definition of 2-port converters and inverters .... p. 74

Fig. 3-7 : Converter equivalences..... p. 79

Fig. 3-8 : An inverter equivalence ..... p. 79
Fig. 3-9 : Negative Immittance Converters (NIC's) ..... p. 83
Fig. 3-10: Negative Immittance Inverter (NII) ..... p. 83
Fig. 3-11: Simulation of a negative conductance ..... p. 83
Fig. 3-12: Negative immittance inverters ..... p. 84
Fig. 3-13: PII obtained by cascading the NII in Fig. 3-12a with the NIC in Fig. 3-9a ..... p. 84
Fig. 3-14: Two different operational amplifier realizations of the nullor circuit in Fig. 3-13 ..... p. 84
Fig. 3-15: A circuit that realizes various converters and inverters ..... p. 87
Fig. 3-16: A circuit that can be used to simulate inductors or FDNR's ..... p. 90
Fig. 3-17: Inductor simulation by an operational amplifier realization of the circuit in Fig. 3-16 ..... p. 90
Fig. 3-18: Inductor simulation by a circuit which cannot be interpreted as an inverter or converter ..... p. 93
Fig. 3-19: Simulation of a lossy inductor ..... p. 93
Fig. 3-20: Floating inductor simulation with two grounded inverters ..... p. 95
Fig. 3-21: Floating inductor simulation with two grounded converters ..... p. 95
Fig. 3-22: Converters and inverters in the (ad,bc)-plane .... p. 97
Fig. 4-1 : An (n+k)-port terminated by a k-port ..... p. 102
Fig. 4-2 : Example showing the difference between admittance and impedance inverters ..... p. 110
Fig. 4-3 : Floating inductor simulation ..... p. 116
Fig. 5-1 : Example of the simplified representation ..... p. 129

Fig. 5-2 : Realization of a multiport with an admittance description ..... p. 131

Fig. 5-3 : Realization of a multiport with an impedance description ..... p. 132

Fig. 5-4 : Realization of a multiport with an hybrid description ..... p. 133

Fig. 5-5 : Realization of 2-ports using converters and inverters ..... p. 135

Fig. 5-6 : Multiport admittance or impedance converter ..... p. 138

Fig. 5-7 : Multiport admittance inverter ..... p. 139

Fig. 5-8 : Multiport impedance inverter ..... p. 140

Fig. 5-9 : Admittance inverter using grounded 2-port inverters ..... p. 142

Fig. 5-10: Three-port inverter for floating inductor simulation ..... p. 143

Fig. 5-11: Some special cases of multiport converters using grounded 2-port converters ..... p. 145

Fig. 5-12: Thre-port converter for floating inductor simulation ..... p. 146

Fig. 5-13: Some special cases of multiport impedance inverters using grounded 2-port inverters ..... p. 147

Fig. 6-1 : Floating inductor simulation by admittance inversion ..... p. 153

Fig. 6-2 : Special case of Fig. 6-1 where terminals 4 and 1 coincide (4-terminal inverter) ..... p. 157

Fig. 6-3 : Four-terminal inverter using two grounded inverters ..... p. 157

Fig. 6-4 : Four-terminal inverter with 3 operational amplifiers (Deboo's circuit) ..... p. 157

Fig. 6-5 : Special case of Fig. 6-1 where $i_o = 0$ (Floating Inverter) .. .. p. 161

Fig. 6-6 : Two examples of floating inverters ..... p. 161

Fig. 6-7 : Special case of Fig. 6-1 where terminals 4 and 1 coincide (Floating 3-terminal inverter) ..... p. 163

Fig. 6-8 : A 3-port circulator ..... p. 163

Fig. 6-9 : A 'general' inverter ..... p. 166

Fig. 6-10: Another 'general' inverter ..... p. 168

Fig. 6-11: A circuit for floating inductor simulation which can be interpreted either as a converter or as an inverter ..... p. 168

Fig. 6-12: Floating inductor simulation by admittance conversion ..... p. 170

Fig. 6-13: Three-port converter using two grounded converters ..... p. 173

Fig. 6-14: Two grounded gyrators .... p. 176

Fig. 6-15: Circuit AA ..... p. 176

Fig. 6-16: Circuit BA ..... p. 177

Fig. 6-17: Circuit AB ..... p. 179

Fig. 6-18: Circuit BB ..... p. 180

Fig. 7-1 : Gyrator realizable with 2 operational amplifiers . p. 187

Fig. 7-2 : Gyrator realizable with 2 transistors ..... p. 187

Fig. 7-3 : Grounded gyrator realizable with 2 operational amplifiers ..... p. 187

Fig. 7-4 : Grounded positive inverter realizable with 2 transistors ..... p. 187

Fig. 7-5 : Grounded gyrator realizable with 2 operational amplifiers with grounded input and output ..... p. 187

Fig. 7-6 : Connection of one nullor to a resistive 4-port ... p. 189
Fig. 7-7 : Gyrayor with 3 nullors and only 2 resistors ..... p. 189
Fig. 7-8 : A positive inverter with only one operational amplifier (Orchard and Willson) ..... p. 191
Fig. 7-9 : Another positive inverter with only one operational amplifier (Schmidt and Lee) ..... p. 191
Fig. 7-10: Different types of 1-nullor positive inverters ... p. 193
Fig. 7-11: A positive inverter of type E ..... p. 194
Fig. 7-12: Grounded 2-port realizable with one operational amplifier ..... p. 196
Fig. 7-13: Realization of a 3-port admittance inverter for floating inductor simulation ..... p. 206
Fig. 7-14: Grounded 2-port realizable with one ideal transistor .....p. 208
Fig. 7-15: Connection of one ideal transistor to a resistive 4-port ..... p. 214
Fig. 8-1 : An (n + k)-port ..... p. 222
Fig. 8-2 : The (ad,bc)-plane ..... p. 232
Fig. 8-3 : Cascade connection of 2 multiports ..... p. 242
Fig. 9-1 : An (n + k)-port terminated by a k-port ..... p. 258
Fig. 9-2 : Model of a non-reciprocal 2-port using an 'anti-reciprocal transition' ..... p. 267
Fig. 9-3 : Model of a non-reciprocal 2-port ..... p. 267

LIST OF TABLES

Table 2-1 : Conversion chart of (n+k)-port matrices..... p. 38

Table 3-1 : The result of cascading positive and negative converters and inverters ..... p. 81

Table 4-1 : Definition and matrix description of multiport converters and inverters ..... p. 105

Table 5-1 : Simplified representation of the interconnection of multiports ..... p. 128

Table 8-1 : Reciprocity,anti-reciprocity, bireciprocity and anti-bireciprocity ..... p. 223

Table 8-2 : Reciprocity, anti-reciprocity, bireciprocity and anti-bireciprocity in terms of the scattering variables ..... p. 226

Table 8-3 : Rules concerning the cascade of an (n+q)-port and a (q+k)-port ..... p. 242

Table 8-4 : Rules concerning the cascade of two (n+n)-ports p. 242

Table 8-5 : Multiport transformers and gyrators ..... p. 246

Table 9-1 : Generalized reciprocity and generalized anti-reciprocity ..... p. 273

CHAPTER 1

INTRODUCTION

1.1 - IMMITTANCE CONVERTERS AND INVERTERS - GENERAL CONSIDERATIONS

This thesis is concerned with an investigation into various aspects of immittance (impedance and admittance) converters and inverters. These are specific types of linear and time-invariant multiports; they can, however, be active or passive, reciprocal or non-reciprocal.

Immittance converters and inverters have in the past been considered as 2-ports (an extension to multiports of the concepts of immittance conversion and inversion will be proposed in this thesis). The gyrator is a familiar example of an inverter; an example of a converter is the negative impedance converter (NIC). A detailed review of the formal definition and main properties of converters and inverters will be deferred until chapter 3. This section will be concerned with a discussion, in general terms, of the role played by these 2-ports in modern network theory.

What is of primary interest in a converter or inverter is the relationship between the immittance at one of the ports and the immittance of a 'load' 1-port connected to the other port: the two admittances (or impedances) are proportional in the case of the converter, and one is proportional to the inverse of the other in the case of the inverter. The simplicity of the mathematical relationships involved (direct proportionality and inverse proportionality) explains the extensive use that has been made of these 2-ports in various methods

of network synthesis.

The main application of converters and inverters is in the field of active RC networks (an example of application in a different field is the use of the gyrator in microwave systems). In the context of active RC networks the converters and inverters are always actively realized, i.e. realized using active components (although they may in some cases be passive as far as the ideal port behaviour is concerned). For this reason converters and inverters are usually classified as active units or sub-networks. They are 2-ports described by two non-zero parameters and are therefore less elementary than other active elements: controlled sources are described by one non-zero parameter only and both the transistor and the operational amplifier are, in the ideal case, described by zero-valued parameters.

Widespread interest in converters and inverters is contemporary with the development of microelectronic technology. Highly frequency-selective networks suitable for microelectronic implementation must be realized as Active RC networks. This becomes necessary due to the fact that microelectronic inductors are not available (except at very high frequencies) and RC networks are not selective enough. It has been found that active RC filters derived from doubly terminated LC ladder filters possess very low sensitivity (this will be discussed in greater detail in chapter 3). One method of obtaining these low-sensitivity active filters consists in the simulation of each inductor in an LC prototype filter (terminated by resistors) by an Active RC circuit. Many of the circuits available for this purpose are interpretable as immittance inverters (usually gyrators) terminated by a capacitor. Other circuits can be interpreted as immittance converters terminated by a resistor (some circuits can be regarded either as an inverter or as a converter, as discussed later). Another method of deriving active filters from

LC ladder filters requires the use of one-ports with admittances proportional to s^2 (s is the complex frequency variable). These special one-ports, often called FDNR's (Frequency Dependent Negative Resistors) can be obtained by using appropriate converters and inverters. Both these methods, simulation of inductors and use of FDNR's, have been intensively investigated in recent years and lead to active filters which are able to satisfy very demanding specifications.

In addition to being very useful in the realization of active networks, converters and inverters are also of great interest from a purely theoretical point of view. Some converters and inverters have always been regarded as typical examples of reciprocal and non-reciprocal 2-ports: the gyrator (which is an inverter) is usually considered as the prototype of a non-reciprocal 2-port, in contrast to the reciprocal transformer (which is a converter, when regarded as an ideal transformer).

1.2 - OUTLINE OF THE THESIS

The present general introduction will be followed by two chapters which are also of an introductory nature. One of these presents general background material consisting of a survey of some basic concepts of network theory which are extensively used in the thesis. The other provides more specific background by giving a review of 2-port converters and inverters and their application in active RC networks.

The presentation of the results of the research done by the author starts in chapter 4, where a generalizations to multiports of the concepts of 2-port conversion and inversion is proposed. In chapter 5 the possibility of realizing multiport converters and inverters with 2-port converters and inverters is investigated.

Most of the circuits proposed for the simulation of floating inductors can be identified as special cases of the multiport converters and inverters proposed in this theses: they are 3-port admittance converters or inverters. A comparative study of various methods of realization of these 3-port converters and inverters is presented in chapter 6.

The realization of various types of inverters with a minimum number of active components is considered in chapter 7; in particular, 2-port positive inverters with a grounded terminal common to both ports are investigated. The results obtained are used in the discussion of the realization of 3-port inverters for floating inductance simulation.

Some converters and inverters have often been considered as 'anti-reciprocal' 2-ports. It will be shown that the two definitions of anti-reciprocity given in the literature do not coincide. An investigation suggested by this incompatibility of the two definitions is reported in chapters 8 and 9. Some types of multiport converters and inverters play an important part in this investigation.

Finally, in the conclusions, the main results obtained in the thesis are summarized and a number of unsolved questions related to those investigated in the thesis, are pointed out.

1.3 - STATEMENT OF ORIGINALITY

A clear distinction is made throughout this thesis between new results obtained by the author and known results that can be found in literature.

It is believed that the results reported in chapters 4 to 9 are original. The main contributions contained in the thesis are, in the

author's opinion, the following:

Chapter 4: The generalization to multiports of the concepts of admittance and impedance converters and inverters; the discussion of their properties and in particular the difference between admittance and impedance converters and inverters; the introduction of the concept of multiport 'hybrid converter'.

Chapter 6: The classification, based on the terminal description, of active RC circuits simulating floating inductors by admittance inversion and conversion [104].

Chapter 7: The proof of the impossibility of 2-port positive inverters ('active gyrators') with both ports grounded, using only one operational amplifier with grounded output or using only one transistor [103].

Chapter 8: The generalization to multiports of one of the two existing definitions of anti-reciprocity and the introduction of a new network property related to the concept of reciprocity; the establishment of various rules concerning interconnections of two multiports when one or both possess one of these two properties [105].

Chapter 9: The generalization of reciprocity and antireciprocity in terms of a parameter which can assume different values and the establishment of rules concerning the interconnection of multiports possessing these generalized properties.

CHAPTER 2

REVIEW OF SOME BASIC CONCEPTS

2.1 - MULTIPORTS

Definition

A physical system is regarded as a multiport when all interaction with the outside of the system, namely the energy flow, only takes place at a certain number of locations called ports. With each port are associated two quantities, the port variables, whose product has the dimension of power. The internal constitution of the system is ignored (the system is regarded as a 'black box') and the multiport is characterized only in terms of the port variables.

In the multiports to be considered here a port is a terminal-pair with which a voltage and a current can be associated [1-6]. A terminal pair is only a port if the instantaneous value of the current flowing into one terminal is equal to the instantaneous value of the current flowing out of the other terminal (Fig. 2-1). It is assumed that this condition is a consequence of the external connections; it is not required to be a constraint imposed by the internal constitution of the multiport. Only the voltages between pairs of terminals that constitute ports are considered, the voltages between terminals of different ports being regarded as of no interest.

A multiport with n ports is called an n-port (Fig. 2-2). The reference directions for the voltage and current at each port will be chosen in such a way that when the instantaneous voltage and current are both positive the instantaneous power flows into

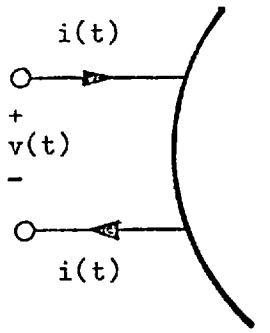


Fig. 2-1 : A port

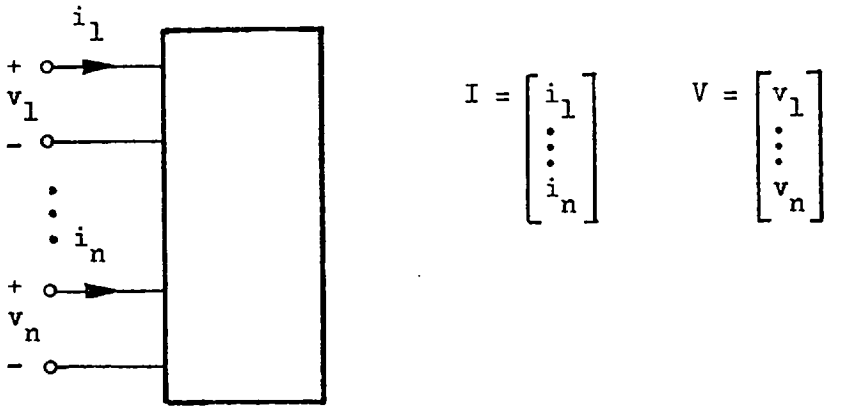


Fig. 2-2 : An n-port

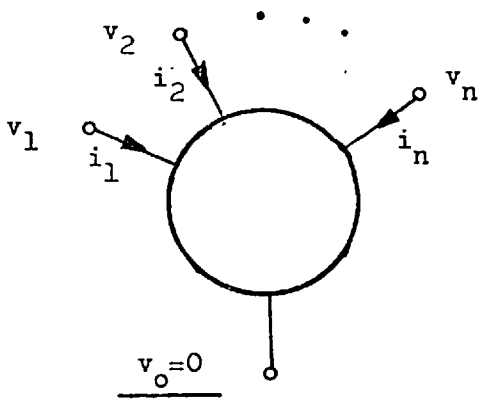


Fig. 2-3 : An n-port with n+1 terminals

the multiport (Figs. 2-1 and 2-2).

Two or more ports may share a common terminal. In particular, it is possible for all the ports to have a common terminal. In this case the n-port is an (n + 1)-terminal network described in terms of the currents at n terminals and the voltages between each of these n terminals and the remaining one (Fig. 2-3).

General description of an n-port

The multiports considered in this thesis are linear, time-invariant and contain only lumped components. Such multiports can be described, in terms of the Laplace transforms of the zero-state port-currents and port-voltages, by a set of linear homogeneous equations, whose coefficients are rational functions of the complex frequency variable s. By zero-state it is meant that all the initial conditions are zero. The equations describing the multiport can be written in matrix form(*) as

$$MI + PV = O \qquad (2\text{-}1)$$

where I and V are n-vectors whose components are the port-currents and port-voltages, respectively,

$$I = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix} \qquad V = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix}$$

(*) It should be noted that in this thesis matrices and vectors are denoted by capital letters.

and M and P are matrices(**) whose elements are rational functions of s. Both M and P have n columns. The number r of independent scalar equations in the description of the n-port is called the dimensionality of the n-port [5]. It will be assumed here that r = n since this is always the case for multiports with physical meaning [7] (for a detailed discussion of the cases where $r \neq n$, usually regarded as "pathological", see [5, 7, 8]). It will also be assumed that the matrix equation (2-1) contains only independent scalar equations, i.e. the number of rows of M and P is n (M and P are therefore n-square matrices).

A description in the form of equations (2-1) has the advantage of being the most general frequency-domain representation of lumped linear time-invariant n-ports. However this representation is not unique, since, if an n-port is represented by (2-1), it can equally be represented by the equation obtained by left-multiplying (2-1) by any non-singular square matrix (of appropriate dimension).

Since it is assumed that the n-port is described by n independent equations with 2n variables, it is possible to express n of the variables in terms of the n remaining variables. The choice of a specific set of n dependent variables is subject to the requirement that the columns of M and P which multiply these variables in (2-1) be linearly independent. This will be illustrated by means of an example:

(**) The coefficient matrices in (2-1) are denoted here by M and P instead of A and B which is the usual notation [4,5]. This is done in order to avoid confusion with the submatrices A and B of the transmission matrix of an (n + n)-port (to be introduced later).

The following description of a 3-port in the form MI + PV = 0,

$$\begin{matrix}(a) & (b) & (c) \end{matrix}$$
$$\begin{bmatrix} 0.5 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + \begin{matrix}(d) & (e) & (f) \end{matrix} \begin{bmatrix} -2 & 0 & -1 \\ 0 & 0 & -1 \\ 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = 0 \qquad (2\text{-}2)$$

becomes, after a rearrangement of the variables, accompanied by a corresponding interchange of columns in M and P,

$$\begin{matrix}(a) & (b) & (e) \end{matrix}$$
$$\begin{bmatrix} 0.5 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ v_2 \end{bmatrix} + \begin{matrix}(d) & (c) & (f) \end{matrix} \begin{bmatrix} -2 & 1 & -1 \\ 0 & 0 & -1 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_3 \\ v_3 \end{bmatrix} = 0 \qquad (2\text{-}3)$$

Since the first matrix in (2-3) is non-singular (the determinant is 0.5) it is possible to use its inverse to left multiply (2-3) leading to

$$\begin{bmatrix} i_1 \\ i_2 \\ v_2 \end{bmatrix} + \begin{bmatrix} 2 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} -2 & 1 & -1 \\ 0 & 0 & -1 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_3 \\ v_3 \end{bmatrix} = 0$$

or

$$\begin{bmatrix} i_1 \\ i_2 \\ v_2 \end{bmatrix} = \begin{bmatrix} 4 & -2 & 2 \\ 0 & 0 & 1 \\ -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_3 \\ v_3 \end{bmatrix}$$

This 3-port cannot be described by a set of equations having i_1, i_2, and v_3, as dependent variables, since the corresponding columns (a), (b) and (f) in (2-2) are not independent:

$$\begin{matrix}(a) & (b) & (f) \end{matrix}$$
$$\det \begin{bmatrix} 0.5 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 0 & 0 \end{bmatrix} = 0$$

Hybrid descriptions

Among the descriptions of an n-port where n variables are expressed in terms of the n remaining variables, the hybrid descriptions are particularly important. In a hybrid description the set of n dependent variables contains one variable (voltage or current) of each port (the same applies to the set of n independent variables).

A notation appropriate for dealing with hybrid descriptions will now be introduced. By E will be denoted an n-vector whose components are some currents and some voltages chosen among the n currents and n voltages at the n ports of the multiport (Fig. 2-2) in such a way that one (and only one) variable of each port is included. The n remaining port variables form another vector denoted by F. It will be assumed that the variables are arranged in E and F in such a way that the subscripts (which indicate the ports with which the variables are associated) appear in the same order. For example if $E = [i_1\ v_2\ v_3\ i_4\ v_5\ i_6]^t$, then $F = [v_1\ i_2\ i_3\ v_4\ i_5\ v_6]^t$; a different ordering of the variables might have been chosen, e.g. $E = [i_1\ i_4\ i_6\ v_2\ v_3\ v_5]^t$ and $F = [v_1\ v_4\ v_6\ i_2\ i_3\ i_5]^t$. It is not permitted to have, for example, $E = [i_1\ i_4\ v_4\ v_2\ v_3\ v_5]^t$ since two variables of the same port (i_4 and v_4) appear in E. Any hybrid description of the n-port will be of the form

$$E = HF \qquad (2\text{-}4)$$

where the n-square matrix H is called a hybrid matrix of the n-port.

When all the variables in E are currents, E = I, then all the variables in F are voltages, F = V, and (2-4) becomes the admittance description of the n-port:

$$I = YV \qquad (2\text{-}5)$$

Similarly, when all the dependent variables are voltages, E = V and

F = I, (2-4) becomes the impedance description of the n-port:

$$V = ZI \qquad (2\text{-}6)$$

Thus the admittance and impedance descriptions are regarded as limiting cases of hybrid descriptions where all the independent variables (and, consequently, all the dependent variables) are of the same nature (all currents or all voltages).

Well-defined multiports

A multiport that possesses at least one hybrid description is said to be well-defined [5]. The existence of a hybrid description has important consequences which will now be examined.

The set of independent variables in a hybrid description contains one variable of each port. A port whose voltage appears as an independent variable will be called a shunt port; a port whose current appears as an independent variable will be called a series port [5]. Since the value of the independent variables can be freely chosen, it is possible in a well-defined multiport to impose the voltage at the shunt ports and the current at the series ports. This means that a well-defined multiport can be driven by voltage sources at some of the ports (the shunt ports) and by current sources at the remaining ports (the series ports). In particular, any of the shunt ports can be short-circuited, since this corresponds to imposing $v = 0$, and any of the series ports can be open-circuited, which corresponds to the choice of $i = 0$.

It should be noticed that a multiport may possess different hybrid descriptions corresponding to different choices of the independent variables. A port which is a shunt port with respect to a specific hybrid description may be a series port with respect to a

different hybrid description. To each hybrid description corresponds an admissible pattern for the connection of voltage and current sources to the ports and, in particular, for the short and open-circuiting of the ports.

When a certain number of ports in a given multiport are rendered inaccessible by short-circuiting some of them and open-circuiting the others, it is often necessary to find the description of the reduced multiport from the description of the original one. This will be discussed now, assuming that the multiports are well-defined.

If a multiport has a hybrid description, it is always possible, as discussed above, to short-circuit shunt ports and open-circuit series ports (shunt and series ports associated with the hybrid description under consideration). The hybrid matrix of the reduced multiport is obtained from the hybrid matrix of the original multiport simply by deleting the rows and columns corresponding to the ports that have been eliminated. For example, given a 4-port described by

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} & h_{13} & h_{14} \\ h_{21} & h_{22} & h_{23} & h_{24} \\ h_{31} & h_{32} & h_{33} & h_{34} \\ h_{41} & h_{42} & h_{43} & h_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \\ i_4 \end{bmatrix}$$

if port 2 is short-circuited ($v_2 = 0$) and port 4 is open-circuited ($i_4 = 0$) the remaining 2-port (ports 1 and 3) is described by

$$\begin{bmatrix} i_1 \\ v_3 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{13} \\ h_{31} & h_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ i_3 \end{bmatrix}$$

A different situation arises when some shunt ports are not short-circuited but open-circuited and some series ports are short-circuited instead of open-circuited. The description of the reduced multiport can in this case be obtained following a procedure which will now be

explained. When the ports are divided into two sets, associated with subscripts 1 and 2, the hybrid description (2-4) can be written in the form of

$$\begin{bmatrix} E_1 \\ E_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} F_1 \\ F_2 \end{bmatrix} \tag{2-7}$$

or

$$E_1 = H_{11} F_1 + H_{12} F_2 \tag{2-7a}$$

$$E_2 = H_{21} F_1 + H_{22} F_2 \tag{2-7b}$$

If the shunt and series ports in set 2 are, respectively, open and short circuited, then

$$E_2 = 0 \tag{2-8}$$

(note that $E_2 = 0$ is not admissible if H_{22} is singular).

From (2-7b) and (2-8)

$$F_2 = -H_{22}^{-1} H_{21} F_1 \tag{2-9}$$

Substitution of (2-9) in (2-7a) yields:

$$E_1 = (H_{11} - H_{12} H_{22}^{-1} H_{21}) F_1 \tag{2-10}$$

which is the description of the reduced multiport. The matrix reduction in (2-10),

$$H_{11} - H_{12} H_{22}^{-1} H_{21}$$

may be regarded as the matrix equivalent of pivotal condensation [2].

Scattering description

The n-port descriptions considered so far are relationships involving the port currents and voltages. An alternative way of describing an n-port consists in the use of the scattering variables instead of the currents and voltages. Scattering variables are used for the description of both distributed and lumped networks. Many methods of synthesis of lumped networks have been given in terms of scattering variables [4, 5, 6].

Although all the results in this thesis are given in terms of currents and voltages some results are also given in terms of the scattering variables since it is believed that these results may be of interest in connection with methods of multiport synthesis that make use of the scattering description. Some definitions and relationships concerning scattering variables will be summarized here for reference purposes (a detailed treatment can be found, for instance in [6]).

The normalized current and voltage vectors I' and V' are defined in terms of the port current and voltage vectors, I and V, by the following equations:

$$I' = R_o^{\frac{1}{2}} I \tag{2-11a}$$

$$V' = R_o^{-\frac{1}{2}} V \tag{2-11b}$$

where

$$R_o = \text{diag}\ (r_{o1}, r_{o2} \cdots r_{on})$$

$$R_o^{\frac{1}{2}} = \text{diag}\ (r_{o1}^{\frac{1}{2}}, r_{o2}^{\frac{1}{2}} \cdots r_{on}^{\frac{1}{2}})$$

$$R_o^{-\frac{1}{2}} = \text{diag}\ (r_{o1}^{-\frac{1}{2}}, r_{o2}^{-\frac{1}{2}} \cdots r_{on}^{-\frac{1}{2}})$$

Although the normalization resistances or port normalization numbers $r_{o1}, r_{o2}, \cdots r_{on}$ can be selected arbitrarily, they are usually related to the parameters of the networks under consideration in order to obtain simple and easily interpretable expressions.

The normalized admittance matrix Y' defined by $I' = Y' V'$ is related to the non-normalized admittance matrix Y (defined by $I = YV$) by the following equation

$$Y' = R_o^{\frac{1}{2}} Y R_o^{\frac{1}{2}} \qquad (2\text{-}12)$$

which is easy to obtain using (2-11).

The normalized impedance matrix Z' defined by $V' = Z' I'$ is related to Z by

$$Z' = R_o^{-\frac{1}{2}} Z R_o^{-\frac{1}{2}} \qquad (2\text{-}13)$$

When a hybrid matrix is associated with the following ordering of the variables

$$\begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_q \\ v_{q+1} \\ \cdot \\ \cdot \\ \cdot \\ v_n \end{bmatrix} = H \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_q \\ i_{q+1} \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix} \qquad (2\text{-}14)$$

the corresponding normalized hybrid matrix H' (relating the normalized voltages and currents by an equation in the form of (2-14)) is

$$H' = \Omega\, H \tag{2-15}$$

where

$$\Omega = \mathrm{diag}\,(r_{o1}^{\frac{1}{2}}, \ldots, r_{oq}^{\frac{1}{2}}, r_{o(q+1)}^{-\frac{1}{2}}, \ldots, r_{on}^{-\frac{1}{2}})$$

The scattering variables(*) $\mathcal{a}$ and $\mathcal{b}$ are defined as

$$\mathcal{a} = \tfrac{1}{2}(V' + I') \tag{2-16a}$$

$$\mathcal{b} = \tfrac{1}{2}(V' - I') \tag{2-16b}$$

It follows immediately that V' and I' are expressed in $\mathcal{a}$ and $\mathcal{b}$ by

$$V' = \mathcal{a} + \mathcal{b} \tag{2-17a}$$

$$I' = \mathcal{a} - \mathcal{b} \tag{2-17b}$$

An n-port can be described by the scattering matrix S which relates $\mathcal{b}$ to $\mathcal{a}$:

$$\mathcal{b} = S\,\mathcal{a} \tag{2-18}$$

The scattering matrix can be expressed in terms of the normalized hybrid matrix H' (assuming that H' corresponds to the ordering of the variables in (2-14)) by [5]:

$$S = \Theta\,(1_n + H')^{-1}\,(1_n - H') \tag{2-19}$$

where

$$\Theta = \begin{bmatrix} 1_q & 0 \\ 0 & -1_{(n-q)} \end{bmatrix}$$

and 1_n is the unit matrix of order n. The expression of H' in terms of S is

$$H' = (1_n - \Theta S)\,(1_n + \Theta S)^{-1} \tag{2-20}$$

In particular, for the admittance matrix, $\Theta = 1_n$ and for the impedance matrix $\Theta = -1_n$; equations (2-19) and (2-20) yield for these special cases:

(*) The scattering variables are usually denoted by A and B. The decision to use here $\mathcal{a}$ and $\mathcal{b}$ is based on the fact that A and B are used to denote submatrices of the transmission matrix (which will be introduced later).

$$S = (1 + Y')^{-1} (1 - Y') \tag{2-21}$$

$$S = (Z' + 1)^{-1} (Z' - 1) \tag{2-22}$$

and

$$Y' = (1 - S) (1 + S)^{-1} \tag{2-23}$$

$$Z' = (1 + S) (1 - S)^{-1} \tag{2-24}$$

Separation of the ports into two sets: (n + k)-ports

There are several situations, some of which will occur frequently in this thesis, where the ports of a multiport are regarded as separated into two sets. In this case the multiport will be referred to as an (n + k)-port (Fig. 2-4). The set containing n ports will be called input, and the corresponding literal symbols will be denoted by subscript 1; the other set, containing k ports, will be called output, and the corresponding symbols will be denoted by subscript 2.

In the case of an (n + k)-port it is convenient to consider the current and voltage vectors (see Fig. 2-4) partitioned as:

$$I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2-25}$$

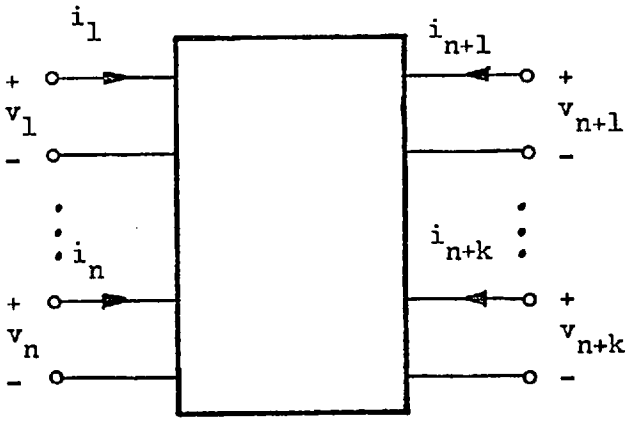
where

$$I_1 = \begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix} \quad I_2 = \begin{bmatrix} i_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ i_{n+k} \end{bmatrix} \quad V_1 = \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_n \end{bmatrix} \quad V_2 = \begin{bmatrix} v_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ v_{n+k} \end{bmatrix} \tag{2-26}$$

The admittance and impedance matrices will also be partitioned:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2-27}$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2-28}$$



$$I_1 = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix} \qquad V_1 = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix} \qquad I_2 = \begin{bmatrix} i_{n+1} \\ \vdots \\ i_{n+k} \end{bmatrix} \qquad V_2 = \begin{bmatrix} v_{n+1} \\ \vdots \\ v_{n+k} \end{bmatrix}$$

Fig. 2-4 : An (n+k)-port

where Y_{11} is n-square, Y_{22} is k-square, Y_{12} is n x k and Y_{21} is k x n (and similarly for the submatrices in Z).

A specific type of hybrid matrix that will often be used is the following:

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \tag{2-29}$$

This specific type of hybrid matrix will be referred to as the shunt-series hybrid matrix [5] since it corresponds to the assumption that all the input ports are shunt ports and all the output ports are series ports.

An important special case of (n + k)-port corresponds to n = k, i.e., the two sets contain the same number of ports. Such a multiport will be referred to as an (n + n)-port. Besides the various types of descriptions which can be applied to the general (n + k)-port, a new type of description can be defined for (n + n)-ports. This is the transmission description [3, 4] which is, by definition:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = T \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{2-30}$$

or, with the transmission matrix T partitioned,

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{2-31}$$

where the four submatrices A, B, C and D are all n-square.

A conversion chart for several matrices describing an (n + k)-port is given in Table 2-1. The admittance, impedance, shunt-series hybrid, and transmission matrices are considered (the transmission matrix being applicable only to (n + n)-ports). These matrices are defined in (2-27, 28, 29, 30).

TABLE 2-1 : Conversion chart of (n+k)-port matrices

	Y	Z	H	T (n = k)
Y		Z^{-1} (*)	$H_{11}-H_{12}H_{22}^{-1}H_{21}$ $\quad H_{12}H_{22}^{-1}$ $-H_{22}^{-1}H_{21}$ $\quad H_{22}^{-1}$	DB^{-1} $\quad C-DB^{-1}A$ $-B^{-1}$ $\quad B^{-1}A$
Z	Y^{-1} (*)		H_{11}^{-1} $\quad -H_{11}^{-1}H_{12}$ $H_{21}H_{11}^{-1}$ $\quad H_{22}-H_{21}H_{11}^{-1}H_{12}$	AC^{-1} $\quad -B+AC^{-1}D$ C^{-1} $\quad C^{-1}D$
H	$Y_{11}-Y_{12}Y_{22}^{-1}Y_{21}$ $\quad Y_{12}Y_{22}^{-1}$ $-Y_{22}^{-1}Y_{21}$ $\quad Y_{22}^{-1}$	Z_{11}^{-1} $\quad -Z_{11}^{-1}Z_{12}$ $Z_{21}Z_{11}^{-1}$ $\quad Z_{22}-Z_{21}Z_{11}^{-1}Z_{12}$		CA^{-1} $\quad -D+CA^{-1}B$ A^{-1} $\quad A^{-1}B$
T (n=k)	$-Y_{21}^{-1}Y_{22}$ $\quad -Y_{21}^{-1}$ $Y_{12}-Y_{11}Y_{21}^{-1}Y_{22}$ $\quad -Y_{11}Y_{21}^{-1}$	$Z_{11}Z_{21}^{-1}$ $\quad -Z_{12}+Z_{11}Z_{21}^{-1}Z_{22}$ Z_{21}^{-1} $\quad Z_{21}^{-1}Z_{22}$	H_{21}^{-1} $\quad H_{21}^{-1}H_{22}$ $H_{11}H_{21}^{-1}$ $\quad -H_{12}+H_{11}H_{21}^{-1}H_{22}$	

Note: Matrices on the same row are equal.

(*) $$\begin{bmatrix} Q_{11} & Q_{12} \\ Q_{12} & Q_{22} \end{bmatrix}^{-1} = \begin{bmatrix} (Q_{11}-Q_{12}Q_{22}^{-1}Q_{21})^{-1} & -Q_{11}^{-1}Q_{12}(Q_{22}-Q_{21}Q_{11}^{-1}Q_{12})^{-1} \\ -Q_{22}^{-1}Q_{21}(Q_{11}-Q_{12}Q_{22}^{-1}Q_{21})^{-1} & (Q_{22}-Q_{21}Q_{11}^{-1}Q_{12})^{-1} \end{bmatrix}$$

2.2 - NULLORS

Nullators, norators and nullors

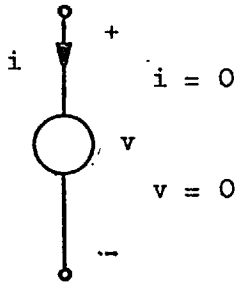
The nullator is defined as a 1-port for which both the current and the voltage are zero; the norator is a 1-port for which both the voltage and the current are arbitrary [9, 8]. These 1-ports will be represented by the symbols shown in Fig. 2-5 . The nullor is defined as a 2-port with zero current and zero voltage at one port and arbitrary voltage and current at the other port [8]; it is thus equivalent to a nullator-norator pair and will be represented as such (Fig. 2-5).

The number of independent equations describing the nullator is greater than the number of ports: the nullator is a 1-port described by two independent equations

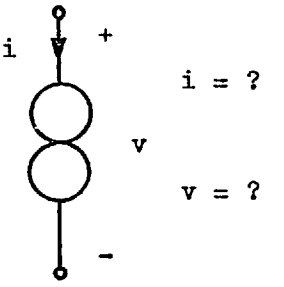
$$i = 0 \qquad (2\text{-}32a)$$

$$v = 0 \qquad (2\text{-}32b)$$

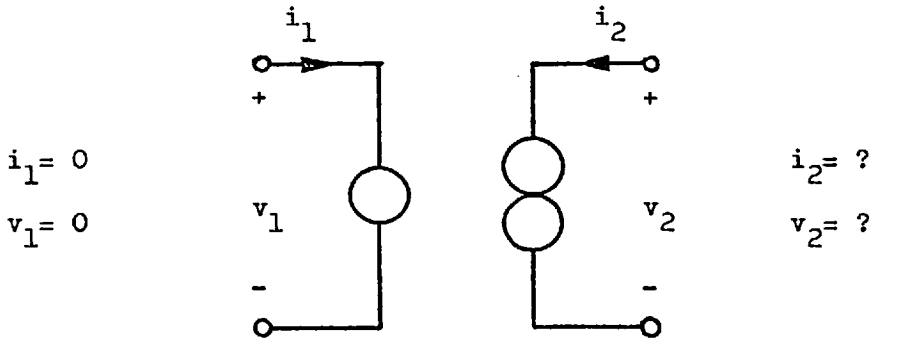
The number of equations describing the norator is smaller than the number of ports: the norator is a 1-port and the number of equations is zero, since nothing is known about the values of the current and voltage and these are unrelated. These 1-ports are 'pathological' in the sense that they differ from any 'normal' multiport, for which the number of independent equations equals the number of ports. The nullator and the norator cannot be obtained by a limiting process from any 1-port characterized by one equation on v and i [8]. Although the nullator and the norator can be represented by circuits containing normal circuit components (e.g. gyrators and positive and negative resistors), it has been shown [7, 8] that these circuits possess "infinite sensitivity" in the sense that a change, however small, of an element in the circuit prevents this from representing a nullator



NULLATOR



NORATOR



NULLOR

Fig. 2 - 5 : Nullator , norator and nullor

or norator, even as an approximation. The nullator and norator can therefore be regarded as mathematical concepts without physical meaning [7]. They are however very useful concepts as will be shown later.

The number of equations describing the nullor is equal to the number of ports: the nullor is a 2-port described by two independent equations

$$i_1 = 0 \qquad (2\text{-}33a)$$

$$v_1 = 0 \qquad (2\text{-}33b)$$

Thus the nullor is not 'pathological' and has physical meaning. It can be represented by equivalent circuits with finite sensitivity [7, 8].

The nullor provides an example of a 2-port which is not well-defined since it does not possess any hybrid description, as shown immediately by (2-33). It must be connected to a network that provides some transmission between the two ports [7] (otherwise the nullator and the norator would be isolated which cannot be accepted in view of the foregoing discussion). This requirement does not apply to well-defined multiports.

Networks containing nullors have physical meaning. Since a nullor is equivalent to a nullator-norator pair, networks with nullators and norators are acceptable provided that they contain an equal number of nullators and norators. Since nullors can be approximated by physical components and nullators and norators cannot, it might seem reasonable to disregard the concepts of nullator and norator and consider only nullors. However it is useful to consider the nullators and norators explicitly for several reasons which will now be discussed.

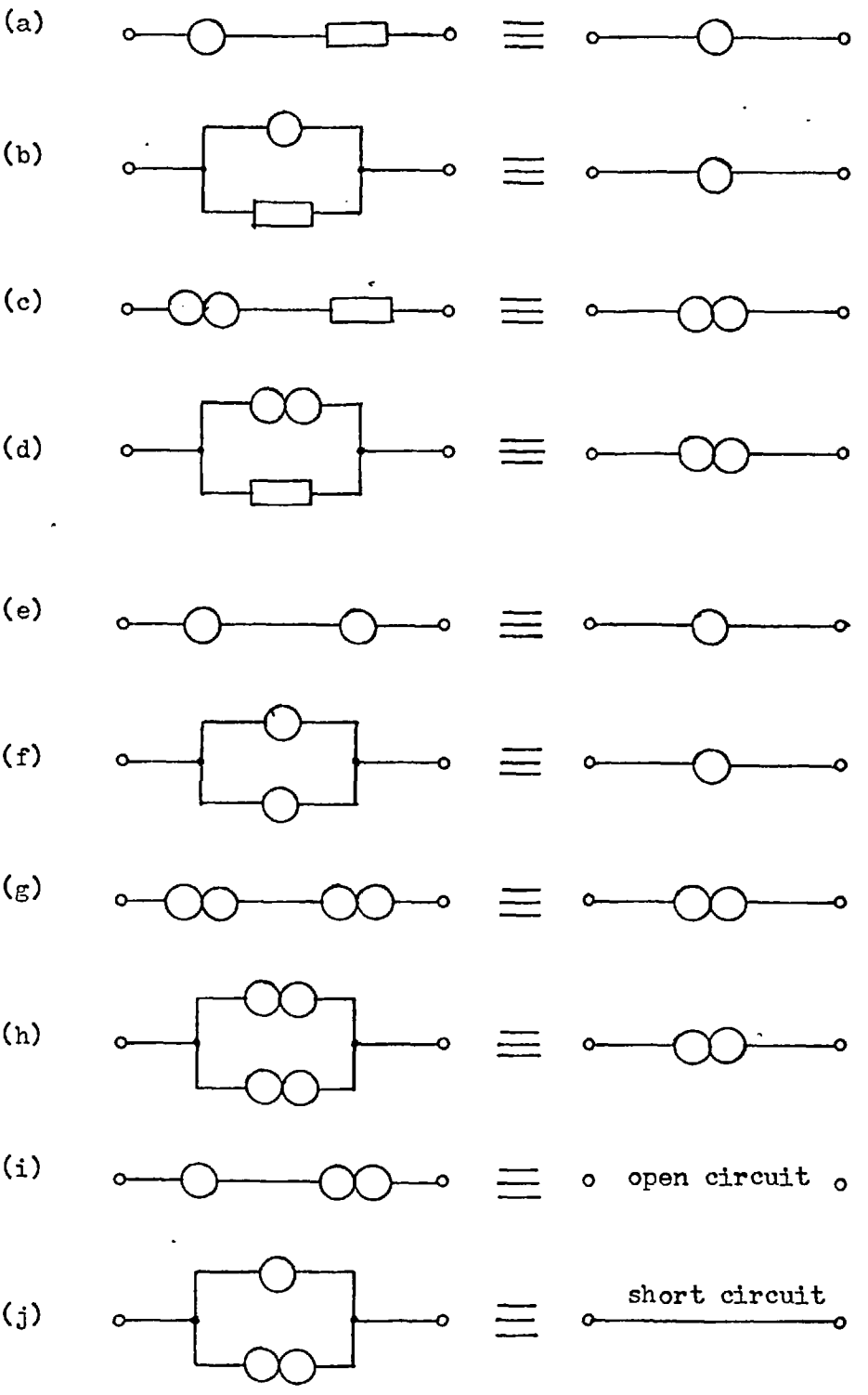
In a network containing n nullators and n norators, these can be

paired to form nullors in n! different ways. When the nullors are replaced by physical components, the networks corresponding to these different pairings have different non-ideal behaviour, including different stability properties. The different possibilities can be explored and the one that provides the best performance for a given application can be selected. This procedure has been applied to the realization of various types of inverters and converters [10, 11, 12, 13].

Another important justification to represent a network in terms of nullators and norators is the possibility of making use of various equivalences shown in Figs. 2 - 6, 7 and 8. By applying these equivalences to a given network, other networks with the same ideal performance are obtained which have different structure and different non-ideal performance. This method has also been proved very useful in connection with the realization of inverters and converters [13, 14].

In addition to these two objective reasons in favour of the use of nullators and norators there is another reason based on human factors: a network represented in terms of dissociated nullators and norators (1-ports) has a less cumbersome circuit diagram and is more readily interpreted than a network represented in terms of nullors (2-ports).

With reference to the equivalences in Fig. 2-6 e,f,g,h and Fig. 2-7 it should be noted that these cannot be used to increase either the number of nullators or the number of norators in a given network in order to achieve equal number of nullators and norators. The resulting network would remain equivalent to the original one and would be equally devoid of physical meaning.



Note: The symbol —▭— represents any 1-port excluding the nullator, the norator, the short and the open circuit.

Fig. 2-6 : Equivalences of 2-terminal networks containing nullators and norators.

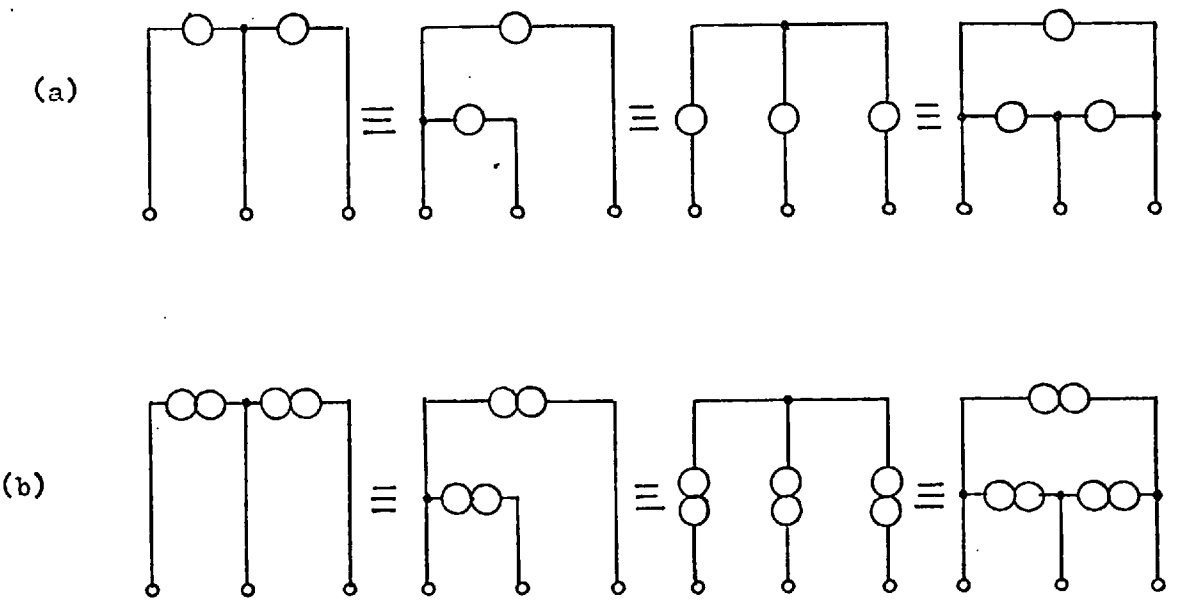


Fig. 2-7 : Equivalences of 3-terminal networks containing nullators and norators.

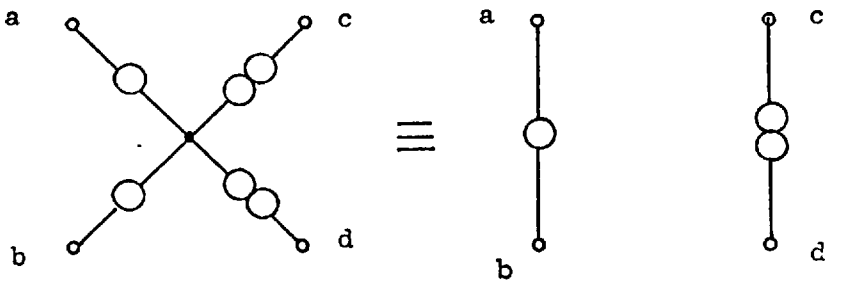


Fig. 2-8 : A nullor equivalence.

Ideal transistors and ideal operational amplifiers

Controlled sources are 2-ports described by:

CCCS - current controlled current source: $v_1 = 0$, $i_2 = \gamma i_1$

VCVS - voltage controlled voltage source: $i_1 = 0$, $v_2 = \mu v_1$

VCCS - voltage controlled current source: $i_1 = 0$, $i_2 = g v_1$

CCVS - current controlled voltage source: $v_1 = 0$, $v_2 = r i_1$

These four types of controlled sources can be represented by equivalent networks containing resistors and nullors (resistor-nullor networks) [15, 13]. It can be shown that all four types of controlled sources become equivalent to a single nullor when the forward transfer parameter (γ, μ, g, r) becomes infinite [11, 13].

The basic active components with reference to present technology are the transistor and the integrated circuit operational amplifier. These active components can be modelled by equivalent circuits containing passive components and controlled sources. Since the controlled sources can be replaced by their resistor-nullor equivalent networks, both the transistor and the operational amplifier can be modelled by networks containing nullors and passive components.

The simplest models of the transistor and the operational amplifier are controlled sources with infinite forward transfer parameters, which are equivalent to nullors. These simplified models are called ideal transistor and ideal operational amplifier.

In the nullor model of the transistor the nullator and the norator share a common terminal, as shown in Fig. 2-9.

In the case of an operational amplifier with grounded input and grounded output the nullator and norator must share a common ground

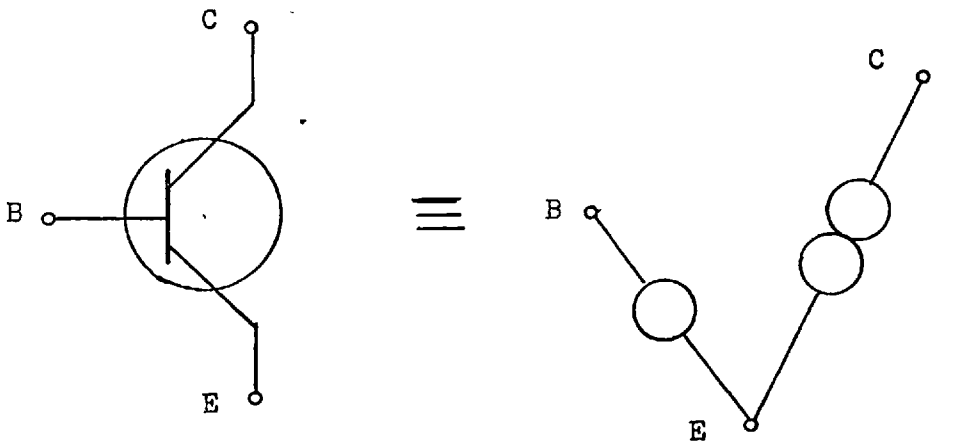


Fig. 2-9 : Nullor model of the ideal transistor.

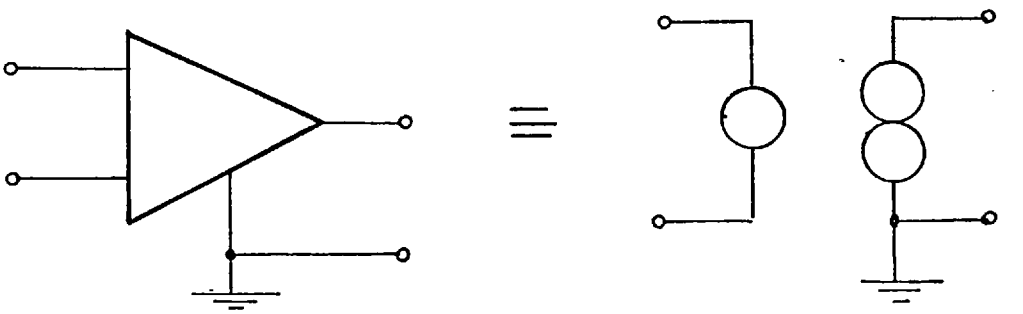


Fig. 2-10 : Nullor model of the ideal operational amplifier.

terminal. However the operational amplifiers commonly available have differential input and grounded output. In their nullor model the nullator and norator do not share a common terminal but one of the terminals of the norator must be grounded, as shown in Fig. 2-10. It will be assumed from now on that, unless otherwise stated, the operational amplifiers have differential input and grounded output.

Thus a network containing nullators and norators will only be realizable using transistors if it is possible to form nullator-norator pairs all having a common terminal, and it will be realizable with operational amplifiers if all the norators have a terminal in common which will be used as the ground terminal of the network.

In a network containing n nullators and n grounded norators which are to be paired and replaced by operational amplifiers there is no restriction on the formation of nullator-norator pairs. As mentioned above there are n! different ways of pairing the nullators and norators. The input of the operational amplifiers has polarity and therefore there are two possible ways of replacing a nullator by the input of an operational amplifier; there are 2^n different possibilities in the case of n operational amplifiers. Thus a network with n nullors can be realized by $2^n . n!$ different operational amplifier circuits [12]. It is necessary to investigate the non-ideal performance of these different realizations in order to decide which are to be preferred [12, 13] (in particular some realizations can be unstable).

Node Analysis of networks containing nullors

It will now be shown how the nodal admittance matrix of a network containing nullors can be related in a very simple way to the nodal admittance matrix of the same network with the nullors removed [16].

Consider an (n + 1)-node network which does not contain independent sources and assume that each node is accessible from the outside via a terminal as shown in Fig. 2-11a. This network can be connected to some external network containing independent sources. The definite admittance matrix Y [2] of the (n + 1)-node network relates the currents entering n terminals to the voltages between these n terminals and the remaining one (called reference terminal)

$$\begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix} = Y \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_n \end{bmatrix} \qquad (2\text{-}34)$$

If the network contains only 2-terminal components (excluding nullators and norators) the definite admittance matrix can be obtained very easily by inspection [2]: the main diagonal elements y_{ii} are the sum of all the admittances incident at node i, and each off-diagonal element y_{ij} is the negative of the admittance connected directly between nodes i and j.

It is now assumed that a nullator is connected between nodes i and j and that a norator is connected between nodes p and q, as shown in Fig. 2-11b.

Since the current through the nullator is zero, the equations expressing the currents i_i and i_j entering terminals i and j remain the same after the connection of the nullator. There is zero voltage across the nullator, and therefore $v_i = v_j$. This means that v_j can be dropped from the voltage vector and column j deleted and added to column i of Y in (2-34).

Since the current i' through the norator is arbitrary the new values of the currents entering terminals p and q, denoted by i'_p and i'_q are not defined, but their sum is,

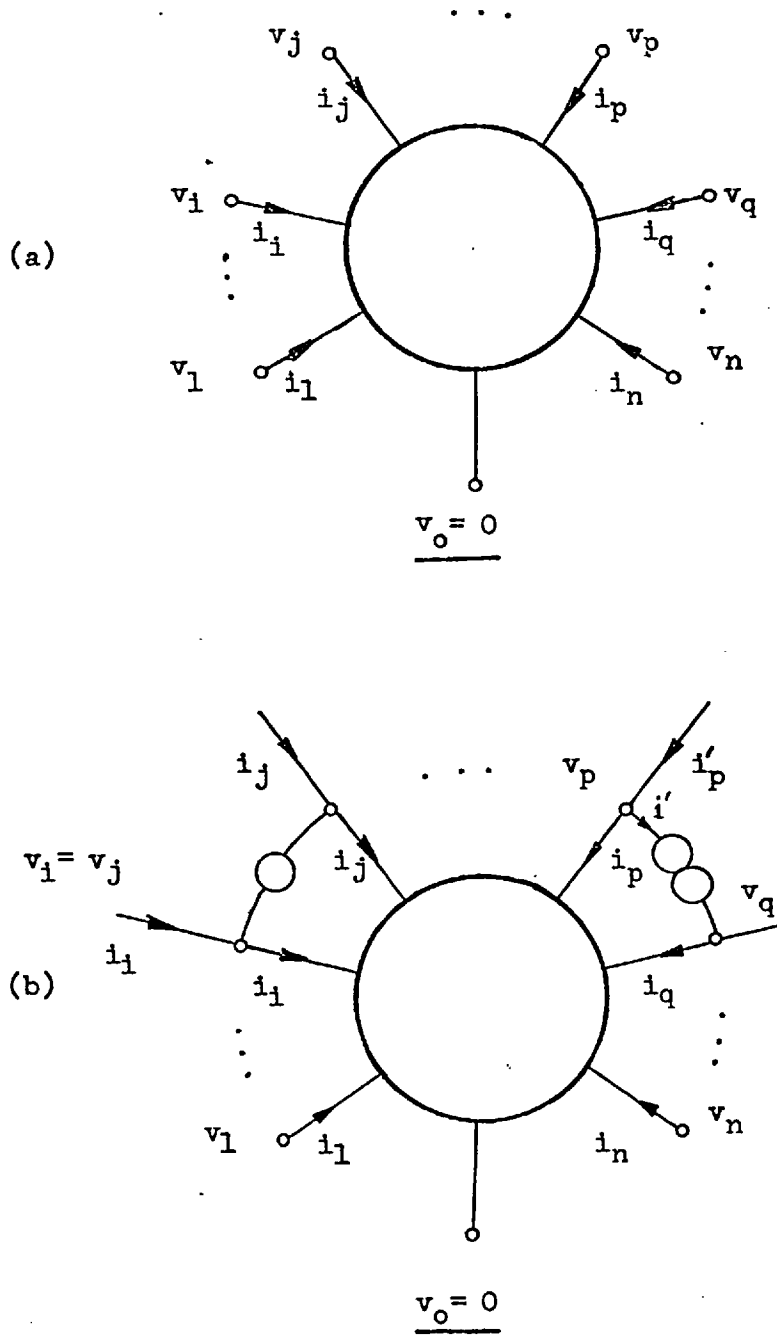


Fig. 2-11 : An (n+1)-node network with one nullor .

$$i'_p = i_p + i'$$

$$i'_q = i_q - i'$$

and

$$i'_p + i'_q = i_p + i_q$$

The nodal description taking into account the presence of the norator can be obtained from (2-34) by replacing i_p by $i'_p + i'_q$, adding row q to row P in Y, and deleting i_q and row q of Y.

The nodal admittance description of the network in Fig. 2-11b is obtained from the nodal admittance description of the network in Fig. 2-11a by performing both the operations that account for the presence of the nullator and those that account for the presence of the norator.

2.3 - RESISTIVE MULTIPORTS

A network containing resistors and active components (active R network) can be considered as a multiport containing only resistors (resistive multiport) with the active components connected to some of the ports. Thus the realization of a given type of active R network with a specified number of active components can be reduced to the synthesis of a suitable resistive multiport. This situation arises in the present thesis in connection with the investigation of positive inverters with a minimum number of active components. It is therefore appropriate to review here some results concerning the synthesis of resistive multiports.

The question which is of interest here can be formulated as follows: what are the necessary and sufficient conditions for an n-square matrix to be realizable as the admittance matrix of a resistive n-port with (n + p) terminals and a specified port structure. By port structure is

meant the particular selection of terminal pairs to form ports.

As far as the author knows the problem of the synthesis of resistive networks has been completely solved only for the case of n-ports with (n + 1)-terminals [17]. For the case of (n + p)-terminals with $p > 1$, although there are methods that can be applied to try to find an n-port with a given admittance matrix, there is no assurance that a definite conclusion will be reached (inability to obtain a solution does not guarantee that a solution does not exist) [18].

In order to present some of the partial answers which have been found for the question formulated above it is convenient to introduce the definitions of paramount matrix and dominant matrix.

An n-square symmetric matrix with real elements is a paramount matrix if each principal minor is not less than the absolute value of any minor of the same order, built from the same rows (or columns) [19, p.273].

An n-square symmetric matrix is a dominant matrix if each main diagonal element is not less than the sum of the absolute values of all the other elements in the same row [19, p.279].

Every dominant matrix is also paramount; a paramount matrix is not necessarily dominant [19, p. 372].

It is known that it is necessary but not sufficient for a matrix to be realizable as the admittance matrix of a resistive multiport that it be a paramount matrix [19, p.372]. It is also known that it is sufficient but not necessary for a matrix to be realizable as the admittance matrix of a resistive multiport that it be dominant [19, p.367]. It should be noted that in the statement of these conditions neither the number of terminals, nor the port structure is specified.

An n-square dominant matrix can be realized as the admittance matrix of an n-port with 2n terminals. The procedure consists in connecting resistors between each pair of ports according to the scheme shown in Fig. 2-12 [19, p.367].

The case of n-ports with n + 1 terminals and specified port structure has been completely solved [17]. The port structure in which all ports share a common terminal leads to particularly simple results: the necessary and sufficient conditions to be satisfied by the matrix are that it be dominant with non positive off-diagonal elements and the synthesis procedure is obvious in view of the well-known properties of the admittance matrix for this case (the off-diagonal elements g_{ij} are the negative of the conductances connected directly between terminals i and j; the main diagonal elements g_{ii} are the sum of all the conductances connected to terminal i).

2.4 - ACTIVITY

The instantaneous power flowing into an n-port is

$$p(t) = \sum_{i=1}^{n} i_i(t) v_i(t)$$

or

$$p(t) = I^t(t)\, V(t) \qquad (2\text{-}35)$$

A multiport is <u>passive</u> if the energy $\mathcal{E}(to)$ initially stored in the multiport plus the energy delivered to the multiport between to and t is non-negative for any to and t and for any admissible voltages and currents [20]:

$$\mathcal{E}(to) + \int_{to}^{t} I^t(\tau)\, V(\tau)\, d\tau \geq 0 \qquad (2\text{-}36)$$

A multiport is <u>active</u> if it is not passive.

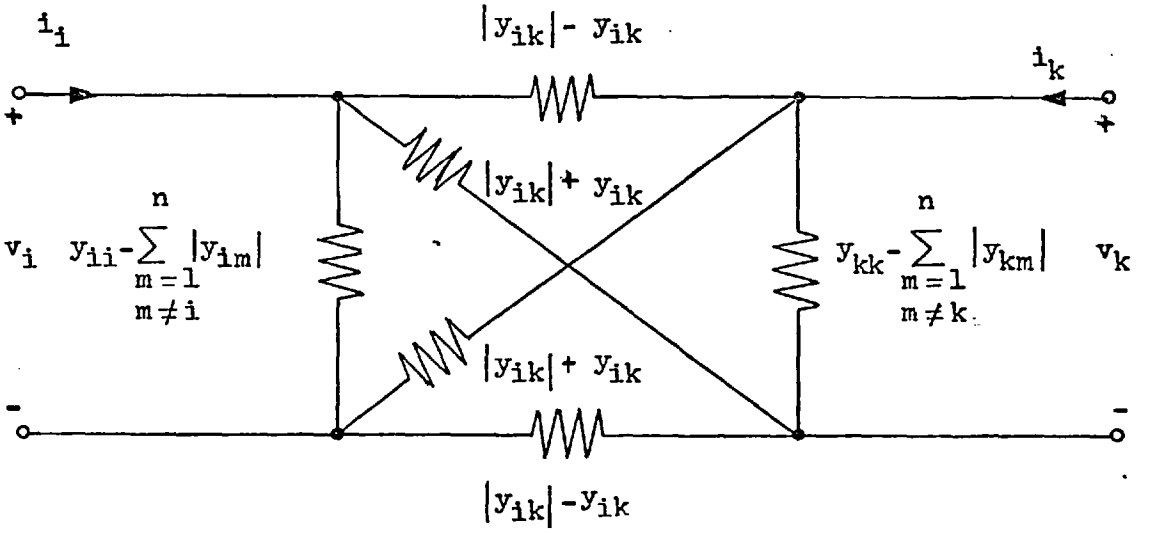


Fig. 2-12 : Realization of a dominant matrix as the admittance matrix of an n - port with 2n terminals.

In the case of the sinusoidal steady state, at a single frequency, the definition of passivity can be expressed by the requirement that the average power (average over a period) be non-negative [2]. It is necessary and sufficient that any hybrid matrix (including the admittance and impedance matrices) have an hermitian part positive semi-definite.

A multiport described by a matrix in which all the elements are real constants will be called non-reactive. The passivity condition in this case is that any hybrid matrix be positive semi-definite.

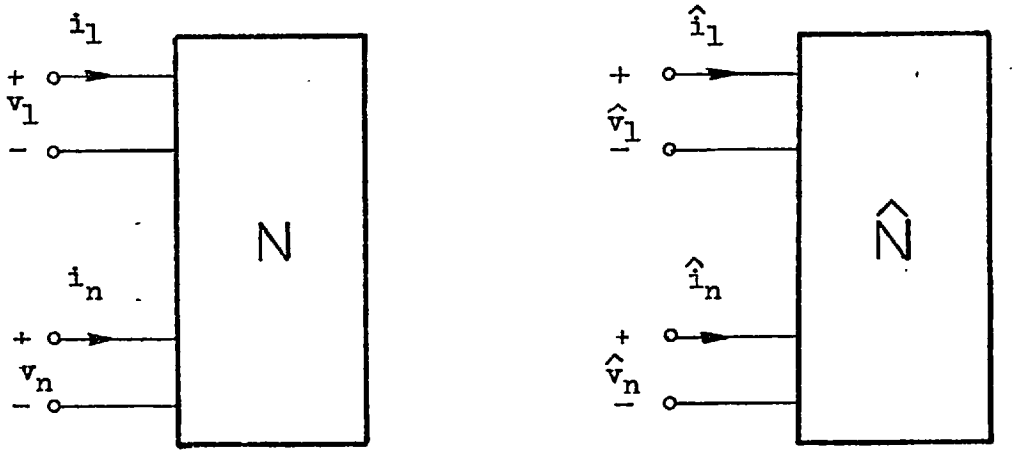
If the instantaneous power into a multiport is zero for any admissible voltages and currents, the multiport will be called non-energic.

It is important to note that the word active is often used to designate networks containing active components, even when these networks are used as multiports which are passive in the sense of the definition given above (for example an actively realized gyrator is passive as far as the ideal port behaviour is concerned). In order not to depart from well established terminology, in this thesis the designations active network and active filter will be used to refer to networks and filters containing active components. The designations 'externally active' and 'externally passive' will be used to refer to multiports which are active or passive according to the definition given above in terms of the port behaviour.

2.5 - INTERRECIPROCITY

Interreciprocal multiports

The concept of interreciprocity [21,5] involves two linear, time-invariant multiports N and $\hat{N}$ with the same number of ports (Fig. 2-13). The vector of the currents at the ports of N is denoted by I and the



$$I = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix} \qquad V = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix} \qquad \hat{I} = \begin{bmatrix} \hat{i}_1 \\ \vdots \\ \hat{i}_n \end{bmatrix} \qquad \hat{V} = \begin{bmatrix} \hat{v}_1 \\ \vdots \\ \hat{v}_n \end{bmatrix}$$

Fig. 2-13 : The two n-ports in the definition of interreciprocity.

voltage vector is denoted by V. Similarly $\hat{I}$ and $\hat{V}$ are the current and voltage vectors of $\hat{N}$.

The two multiports N and $\hat{N}$ are <u>interreciprocal</u> if, for all voltages and currents satisfying the equations of the multiports, the following relationship is satisfied:

$$I^t(s)\,\hat{V}(s) - V^t(s)\,\hat{I}(s) = 0 \qquad (2\text{-}37)$$

where the superscript t denotes transposition. I(s), V(s), $\hat{I}(s)$ and $\hat{V}(s)$ are the Laplace transforms of the voltages and currents when all initial conditions are zero (as in the definition of network functions). Equation (2-37) can be written equivalently as

$$\sum_{\text{all ports}} i_k(s)\,\hat{v}_k(s) - \sum_{\text{all ports}} v_k(s)\,\hat{i}_k(s) = 0$$

It should be noted that the designations <u>adjoint</u> and <u>transpose</u> are often used with the same meaning as interreciprocal.

The definition of interreciprocity can also be given in terms of the instantaneous values of the voltages and currents [22]

$$I^t(t) * \hat{V}(t) - V^t(t) * \hat{I}(t) = 0 \qquad (2\text{-}38)$$

where the symbol * means convolution. Equation (2-38) can be written in a more explicit way, as

$$\sum_{\text{all ports}} \int_0^t i_k(t-\tau)\hat{v}_k(\tau)d\tau - \sum_{\text{all ports}} \int_0^t v_k(t-\tau)\hat{i}_k(\tau)d\tau = 0$$

This time-domain definition using the convolution of the time functions is equivalent to the frequency-domain definition using the product of the Laplace transforms, in view of a well-known property of the Laplace transformation. In this thesis only the expression in terms of the Laplace transforms will be used. In accordance with the notation used in this thesis the dependence on s will not be explicitly indicated.

Interreciprocity of well-defined multiports

The interreciprocity conditions in terms of the hybrid matrix (all well-defined multiports possess a hybrid description) will now be derived. A similar derivation can be found in reference [5,p.72].

It is assumed that the two multiports N and $\hat{N}$ (Fig. 2-15) have hybrid descriptions of the form

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} \hat{I}_1 \\ \hat{V}_2 \end{bmatrix} = \begin{bmatrix} \hat{H}_{11} & \hat{H}_{12} \\ \hat{H}_{21} & \hat{H}_{22} \end{bmatrix} \begin{bmatrix} \hat{V}_1 \\ \hat{I}_2 \end{bmatrix} \quad (2\text{-}39)$$

where

$$I_1 = \begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_q \end{bmatrix} \qquad I_2 = \begin{bmatrix} i_{q+1} \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix}$$

and V_1, V_2, $\hat{I}_1$, $\hat{I}_2$, $\hat{V}_1$, $\hat{V}_2$ are similarly defined.

With the current and voltage vectors partitioned, equation (2-37) can be written as

$$\begin{bmatrix} I_1^t & I_2^t \end{bmatrix} \begin{bmatrix} \hat{V}_1 \\ \hat{V}_2 \end{bmatrix} - \begin{bmatrix} V_1^t & V_2^t \end{bmatrix} \begin{bmatrix} \hat{I}_1 \\ \hat{I}_2 \end{bmatrix} = 0$$

or

$$I_1^t \hat{V}_1 + I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (2\text{-}40)$$

Making use of (2-39) in (2-40) leads to

$$(H_{11} V_1 + H_{12} I_2)^t \hat{V}_1 + I_2^t (\hat{H}_{21} \hat{V}_1 + \hat{H}_{22} \hat{I}_2)$$
$$-V_1^t (\hat{H}_{11} \hat{V}_1 + \hat{H}_{12} \hat{I}_2) - (H_{21} V_1 + H_{22} I_2)^t \hat{I}_2 = 0$$

or

$$V_1^t (H_{11}^t - \hat{H}_{11}) \hat{V}_1 + I_2^t (H_{12}^t + \hat{H}_{21}) \hat{V}_1 +$$
$$I_2^t (\hat{H}_{22} - H_{22}^t) \hat{I}_2 - V_1^t (\hat{H}_{12} + H_{21}^t) \hat{I}_2 = 0 \qquad (2\text{-}41)$$

This equation must be satisfied for all possible values of the voltages and currents. Since the voltages and currents in (2-41) are the inde-

pendent variables in (2-39), they can be freely chosen. If $I_2 = 0$ and $\hat{I}_2 = 0$, equation (2-41) is reduced to

$$V_1^t (H_{11}^t - \hat{H}_{11}) \hat{V}_1 = 0 \qquad (2-42)$$

which means that it is necessary that

$$H_{11}^t - \hat{H}_{11} = 0$$

otherwise it would be possible to choose V_1 and $\hat{V}_1$ such that (2-42) would not be satisfied. Similar arguments lead to the conclusion that all the factors enclosed by brackets in (2-41) must be zero. Therefore the multiports N and $\hat{N}$ are interreciprocal iff

$$\hat{H}_{11} = H_{11}^t \qquad (2-43a)$$

$$\hat{H}_{12} = -H_{21}^t \qquad (2-43b)$$

$$\hat{H}_{21} = -H_{12}^t \qquad (2-43c)$$

$$\hat{H}_{22} = H_{22}^t \qquad (2-43d)$$

This result can be expressed in the more compact form

$$\hat{H} = \Theta H^t \Theta \qquad (2-44)$$

where Θ is an auxiliary matrix defined as

$$\Theta = \begin{bmatrix} 1_q & 0 \\ 0 & -1_{n-q} \end{bmatrix}$$

Since the admittance and impedance descriptions can be regarded as special types of hybrid descriptions, it follows from (2-43a) and (2-43d) that for interreciprocal multiports

$$\hat{Y} = Y^t \qquad (2-45)$$

and

$$\hat{Z} = Z^t \qquad (2-46)$$

The interreciprocity theorem

Before introducing the interreciprocity theorem some brief remarks will be made.

A k-terminal element can be regarded as a (k - 1)-port with a terminal common to all ports; two k-terminal elements will be considered as interreciprocal if they can be regarded as interreciprocal (k - 1)-ports. In the graph of a network, k-terminal elements can be represented by k - 1 branches having a common terminal (these branches correspond to the k - 1 ports); it should be noted that these k - 1 branches are coupled branches.

The interreciprocity theorem [21] can be stated as follows:

— Two multiports are interreciprocal if they are realized by networks with the same topology and if the elements placed in corresponding locations in the two networks are interreciprocal.

The interreciprocity theorem can be proved very easily using Tellegen's theorem [21]. Tellegen's theorem states that

$$I^t V = 0 \qquad (2\text{-}47)$$

where

(a) I is the vector of the branch currents associated with a given graph and these currents obey Kirchhoff's current law.

(b) V is the vector of the branch voltages associated with the same graph and these voltages satisfy Kirchhoff's voltage law.

If the port variables, I_p and V_p, are separated from the currents and voltages in the internal branches which are denoted by I_b and V_b, then equation (2-47) can be written as

$$I_p^t V_p = I_b^t V_b \qquad (2\text{-}48)$$

(note that the port currents have a reference direction opposite to that which is used when the ports are regarded as branches).

Consider two networks N and $\hat{N}$ with the same topology. If the currents in N and the voltages in $\hat{N}$ are used in (2-48), then

$$I_p^t \hat{V}_p = I_b^t \hat{V}_b \qquad (2\text{-}49)$$

If the currents in $\hat{N}$ and voltages in N are chosen, then (2-48) yields (after transposition):

$$V_p^t \hat{I}_p = V_b^t \hat{I}_b \qquad (2\text{-}50)$$

Subtraction of (2-50) from (2-49) leads to

$$I_p^t \hat{V}_p - V_p^t \hat{I}_p = I_b^t \hat{V}_b - V_b^t \hat{I}_b \qquad (2\text{-}51)$$

This equation shows that if the components in N are interreciprocal with the components in $\hat{N}$, i.e.,

$$I_b^t \hat{V}_b - V_b^t \hat{I}_b = 0$$

then the port variables of N and $\hat{N}$ satisfy the definition of interreciprocity. This proves the interreciprocity theorem.

One consequence of the interreciprocity theorem is that the multiport which is interreciprocal with a given multiport containing 2-terminal components and nullors is obtained by interchanging the nullators and norators in the given multiport. This follows from the fact that any non-pathological 2-terminal component is interreciprocal with itself and a nullor is interreciprocal with another nullor with the nullator and norator interchanged (it can easily be seen that the nullator and norator satisfy the definition of interreciprocity).

Reciprocal multiports

A reciprocal multiport is defined as a multiport which is interreciprocal with itself [21,5]. This means that all the equations

used in connection with interreciprocity are satisfied by reciprocal multiports if the symbol $\wedge$ instead of denoting the variables of a different multiport, denotes different values of the variables of the same multiport compatible with the equations describing the multiport. Thus a reciprocal multiport must satisfy (2-37), i.e.,

$$I^t \hat{V} - V^t \hat{I} = 0 \tag{2-52}$$

The definition of reciprocity by equation (2-52) has been used by several authors (see, for instance [2,21]); it has the advantage of not being tied to a specific type of network description.

The reciprocity conditions in terms of the hybrid matrix follow directly from (2-43):

$$H_{11} = H_{11}^t \qquad H_{22} = H_{22}^t \qquad H_{12} = -H_{21}^t \tag{2-53}$$

or, from (2-44),

$$H = \Theta H^t \Theta \tag{2-54}$$

In particular, for the admittance and impedance matrices

$$Y = Y^t \tag{2-55}$$

$$Z = Z^t \tag{2-56}$$

For 2-ports, these conditions become

$$y_{12} = y_{21} \qquad z_{12} = z_{21} \qquad h_{12} = -h_{21} \tag{2-57}$$

or, equivalently, in terms of the transmission matrix

$$\det T = ad - bc = 1 \tag{2-58}$$

The Interreciprocity Theorem leads, immediately to the Reciprocity Theorem [21,2]: a multiport made of reciprocal elements is itself reciprocal.

A multiport that does not satisfy (2-52) is said to be non-reciprocal. Several authors have considered the concept of anti-reciprocity as a kind of extreme non-reciprocity. Since an investigation of anti-reciprocity is one of the questions investigated in the present thesis, this subject will not be pursued here; a detailed discussion will be given in chapter 8.

CHAPTER 3

REVIEW OF 2-PORT IMMITTANCE CONVERTERS AND INVERTERS IN THE CONTEXT OF ACTIVE RC NETWORKS

3.1 - ACTIVE RC NETWORKS

The classical approach to the realization of frequency-selective networks (electrical filters) is based on the use of networks containing resistors, inductors and capacitors (RLC networks). Transformers are also used in some cases, and, in some particularly demanding applications, electromechanical resonators, such as crystals, have to be included. However, RLC filters are suitable for most applications. These filters are usually doubly terminated LC 2-ports (i.e., LC 2-ports with a resistor in series with the input - assuming that it is driven by a voltage source - and a resistor across the output). RLC filters have been used for many years and their theory and design techniques have been developed to a high degree of perfection.

However, RLC filters, which are easily implemented using classical discrete-component technology, cannot be realized using modern microelectronic technology. Although resistors and capacitors can easily be realized in microelectronic form, inductors cannot. Microelectronic components are realized either in thin layers or as small discrete components; inductors realized in this way have very small inductances and therefore are only useful at very high frequencies (in addition, such inductors have fairly low Q-factors). Since microelectronic circuits have very desirable properties (e.g. small volume and weight

potential low cost, increased reliability) it is justified to look for new types of frequency-selective networks, suitable for microelectronic realization.

The simplest inductorless frequency-selective networks are obviously networks containing only resistors and capacitors. However, the poles of the transfer function of an RC network are restricted to the negative real axis of the complex frequency s-plane and as a consequence an RC network can provide considerably less selectivity than an RLC network of a comparable degree of complexity [23]. Guillemin [24] and others [25, 26] have shown that the transfer function of an RC network can approximate any required filter characteristic, but, for high selectivity, the attenuation in the pass-band is very high and the network contains a large number of components arranged in a complicated structure. Apparently, the possibilities of this approach have never been fully evaluated and RC networks on their own have not been used in practice to obtain high selectivity.

The restriction of the poles of the transfer function of RC networks to the negative real axis can be removed by the inclusion of suitable active components. Since active components are easily realized in microelectronic form, a natural solution to the problem of realizing highly frequency-selective networks compatible with microelectronic technology consists in the use of active RC networks.

Before reviewing some of the approaches to the realization of active RC networks that have been proposed, it is useful to remember that high frequency-selectivity is obtained by high order filters. By high order it is meant that the degree of the denominator poynomial of the transfer function is greater than 2 or 3 (in the case of some of the filters used in frequency division multiplex (FDM) systems [27] the order is typically 10 or 12).

Historically, the first general methods proposed for the realization of active RC networks are based on the use of only one active unit. The method proposed by Linvill in 1954 [28] permits the realization of any transfer impedance using resistors, capacitors and only one active unit, namely one negative impedance converter (NIC) connected as shown in Fig 3-1. There are other synthesis methods also using only one active unit, for instance the methods proposed by Sandberg [29] and Saraga [30]. However, it was soon found that active RC networks with only one active unit are unsuitable for the realization of high order filters since the sensitivity of the transfer function to changes of the component parameters is intolerably high. This approach was abandoned and the search continued for other methods able to produce high order filters with acceptable sensitivity.

Another approach to the realizations of active RC filters consists in the factorization of the required transfer function into 2nd order transfer functions (and a 1st order factor if the order of the overall transfer function is odd). The filter is then realized as a cascade of 2nd order sections (Fig. 3-2). Following an early publication on this method by Sallen and Key [31] many circuits that realize 2nd order sections have been proposed and extensively studied (see, for instance, [22, 32]). Filters realized in accordance with this method have a sensitivity performance acceptable for many applications and are widely used at present. This method, however, is unable to produce high-performance filters, such as some of those required by FDM systems.

In 1966 Orchard [33] suggested that active filters with low sensitivity might be obtained by simulation of doubly-terminated LC ladder filters (Fig. 3-3), since these exhibit low sensitivity properties (it is pointed out in [33] that in a doubly-terminated LC filter the first order sensitivity of the amplitude characteristic to

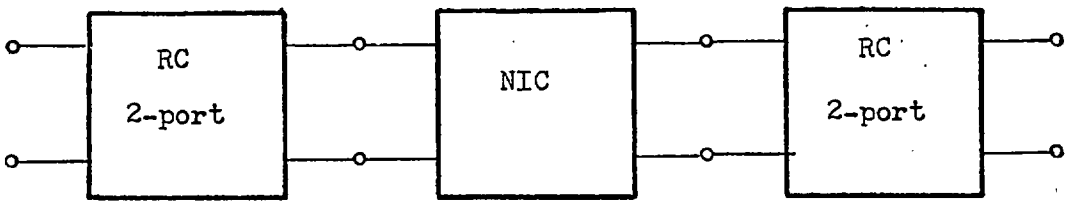


Fig. 3-1 : Linvill's method.

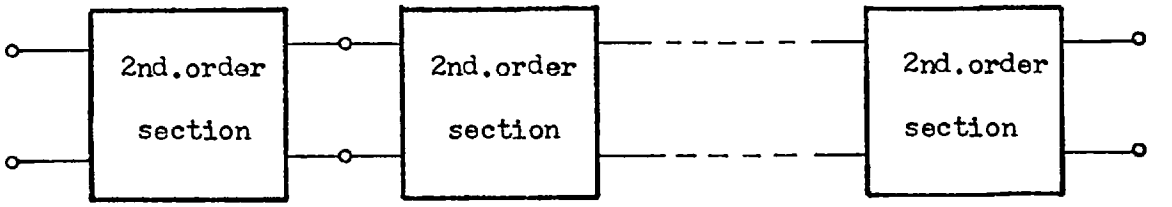
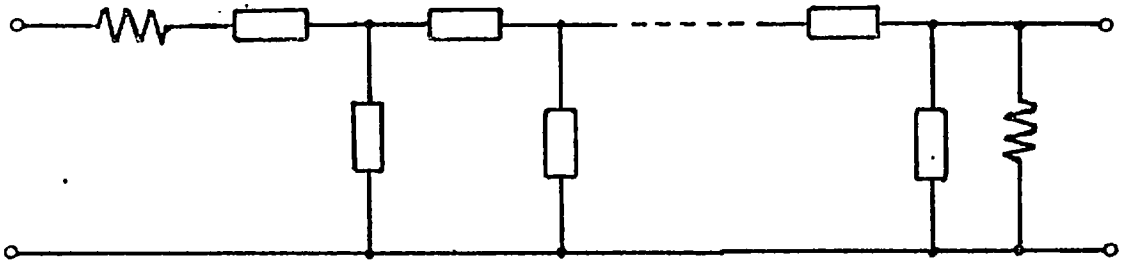


Fig. 3-2 : Cascaded second order sections.



Note : —▭— represents an LC 1-port.

Fig. 3-3 : Doubly terminated LC ladder network.

variations of any component is zero at those points in the pass-band for which the source delivers its maximum available power into the load). Various methods based on this approach have been proposed and intensively investigated in recent years. The results obtained have clearly confirmed Orchard's conjecture.

Since converters and inverters play a central part in some of the methods based on the simulation of doubly terminated LC filters, these methods will be discussed in some detail in the next section.

3.2 - SIMULATION OF DOUBLY-TERMINATED LC LADDER FILTERS

The first method proposed for the realization of inductorless filters based on the simulation of doubly-terminated LC ladder filters will be referred to as the inductor simulation method. It consists simply in retaining the resistors and capacitors in the ladder and using active RC circuits to simulate the inductors. The simulation of the inductors can be done either by replacing each inductor individually by an active RC circuit [33, 34, 35, 36] or by replacing the whole inductor sub-network by an appropriate multiterminal active RC network [37, 38, 39].

When the inductors are simulated one by one, it is important to distinguish between grounded inductors and floating inductors, as will now be explained.

It is desirable to use the same power supply for all the active components in a system. In this case all the active sub-networks will have one terminal in common which is called the ground terminal. A grounded port has one of its two terminals connected to the ground terminal of the system. The designation 'grounded 2-port' will be used in this thesis to refer to 2-ports in which both ports have a common

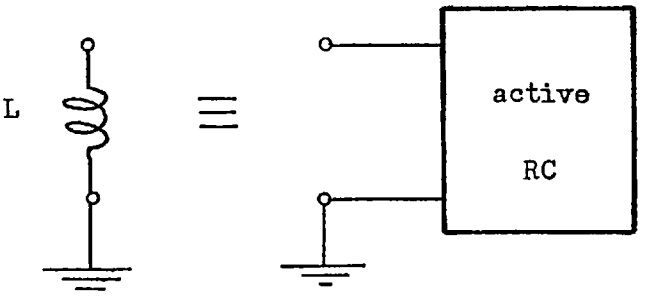
terminal connected to the ground.

If a ladder network (Fig. 3-3) is used as part of a system containing active components, the ground is normally the terminal which is common to input and output. When the inductors in the ladder are simulated by active RC networks, there is a distinction between simulated grounded inductors, which have 2 terminals and can thus be described as 1-ports (Fig. 3-4a), and simulated floating inductors, which are associated with 3 terminals (when the ground terminal is included) and are conveniently described as 2-ports (Fig. 3-4b). The circuits that simulate floating inductors are more complicated than those that simulate grounded inductors. Therefore the presence of floating inductors in the ladder filter to be simulated may influence the choice between the inductor simulation method and the other methods which will be mentioned next. A review of various active RC networks that can be used to simulate inductors, both grounded and floating, will be given later in this chapter, after the discussion of converters and inverters.

Another method of simulation of doubly-terminated LC ladder filters was originally introduced by Bruton [40] and will be referred to as the impedance scaling method. It is based on the fact that the voltage (or current) ratio of a filter, being a nondimensional quantity, is not affected if the impedances of all the components are multiplied by the same factor. Consider, as an example, the low-pass filter in Fig. 3-5a. If all the impedances are multiplied by s^{-1} (s is the complex frequency variable) the inductors become resistors, the resistors become capacitors and the capacitors become new components with an impedance proportional to s^{-2}. These new components are usually called frequency dependent negative resistors (FDNR's), since if $s = jw$ then $s^{-2} = -w^{-2}$. The more specific designation super-capacitor is perhaps to be preferred in order to distinguish these components from those

(a) GROUNDED INDUCTOR

$$y = \frac{1}{sL}$$



(b) FLOATING INDUCTOR

$$Y = \frac{1}{sL}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}$$

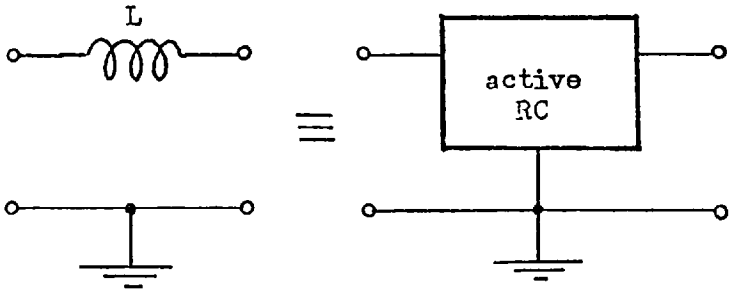


Fig. 3-4 : Active RC simulation of grounded and floating inductors.

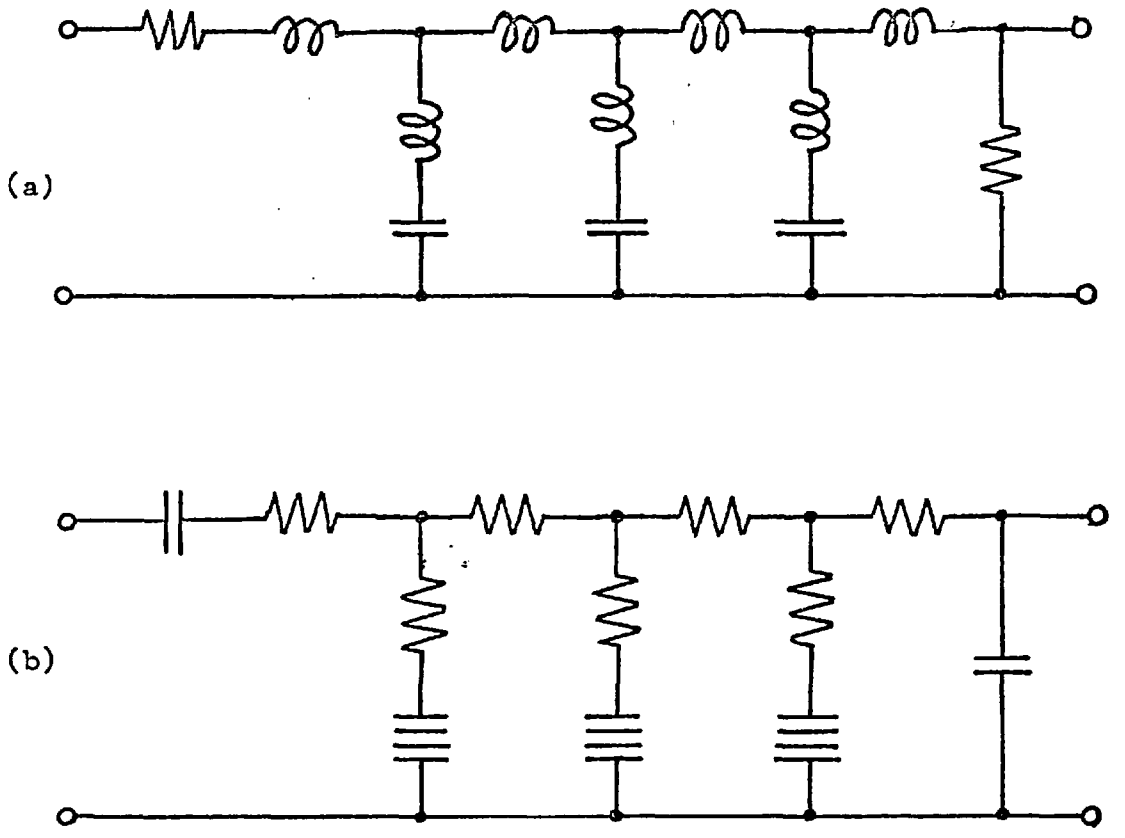


Fig. 3-5 : Application of the impedance scaling method to a low - pass filter.

with impedances proportional to s^2 which will be called super-inductors; both the super-capacitor and the super-inductor are FDNR's.

As a result of the impedance scaling, the network in Fig. 3-5a becomes the network in Fig. 3-5b, containing resistors capacitors and super-capacitors. The super-capacitors are then realized by active RC networks, usually immittance converters, as will be seen later.

In the impedance-scaled network (Fig. 3-5b) all the super-capacitors are grounded, whereas the original network (Fig. 3-5a) has several floating inductors; the number of inductors is larger than the number of super-capacitors and, because the inductors are floating, they are also more difficult to simulate.

Impedance scaling consisting of multiplication by s (instead of s^{-1}) has also been found useful in connection with high-pass filters when the inductors in the ladder are grounded (the advantage of this procedure with respect to the simulation of the inductors is that capacitors become resistors, which are easier to adjust). In this case grounded super-inductors are obtained, which can be simulated using appropriate impedance converters.

The realization of band-pass filters using impedance scaling can be based on a ladder network consisting of a low-pass section followed by a high pass section, each section being subject to the appropriate type of scaling (a suitable converter is used to impedance-match the two sections).

The impedance scaling method has recently been used to produce high-performance filters [41, 42, 43].

In the two methods discussed so far, inductor simulation and impedance scaling, the ladder structure of the passive network is maintained in the active network that simulates it; to any current in

the first corresponds a current in the second network and the same is true for the voltages. There are however other methods of simulating doubly-terminated LC ladder filters that reproduce the equations describing the original ladder but do not lead to active networks having a ladder structure. One of these methods leads to active filters which are usually called leapfrog feedback filters; another method leads to a class of filters which have been called wave active filters. Only a very brief reference to these methods will be made here, since they are not directly associated with the use of converters and inverters.

Leapfrog feedback filters and LC ladder filters can be represented by the same signal-flow graph, i.e. both filters are described by equations of the same form. However, the network topology is different and both voltages and currents in the ladder are represented by voltages in the leapfrog feeback realization. This method was originally proposed by Girling and Good [44]. Leapfrog feedback filters are usually included in a class designated as multifeedback filters (see, for instance [45-48]). Of the various multifeedback structures only the leapfrog has been derived from LC ladder filters; it appears that so far no relationship has been established between other multi-feedback structures and passive ladder filters.

Wave active filters is a designation that has been suggested for active filters which realize the equations, expressed in terms of scattering variables, of doubly-terminated LC ladder filters [49, 50]. This method is based on the same principles that have been previously used to realize wave digital filters (which are digital filters derived from LC ladder filters). A more general method, which includes wave active filters as a special case, has recently been proposed [51].

3.3 - TWO-PORT CONVERTERS AND INVERTERS

A 2-port admittance converter is defined as a 2-port which, when terminated at port 2 by any admittance y_2 (Fig. 3-6), presents at port 1 an admittance y_1 related to y_2 by

$$y_1 = k_c^y \; y_2 \tag{3-1}$$

where k_c^y depends only on the 2-port (i.e. is independent of y_2) [52]. The factor k_c^y will be referred to as the admittance conversion factor (in k_c^y the superscript denotes admittance and the subscript denotes conversion). The factor k_c^y is not necessarily a real constant: it is in general a rational function of the complex frequency variable s.

A 2-port admittance inverter is a 2-port which, when terminated at port 2 by any admittance y_2 presents at port 1 an admittance y_1 related to y_2 by

$$y_1 = k_i^y \; y_2^{-1} \tag{3-2}$$

where k_i^y depends only on the 2-port [52]. The designation 'admittance inversion factor' will be used to refer to k_i^y which, in general, is a rational function of s.

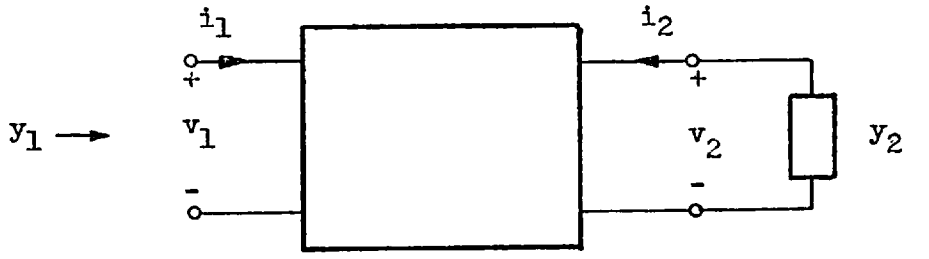
The definition of impedance converter and impedance inverter is obtained by replacing the word admittance by impedance in the above definitions. For the impedance converter

$$z_1 = k_c^z \; z_2 \tag{3-3}$$

and k_c^z is designated as the impedance conversion factor. In the case of the impedance inverter

$$z_1 = k_i^z \; z_2^{-1} \tag{3-4}$$

and k_i^z is the impedance inversion factor.



$$y_1 = \frac{i_1(s)}{v_1(s)} \qquad y_2 = -\frac{i_2(s)}{v_2(s)}$$

CONVERTER

$$y_1 = k_c^y \, y_2$$

INVERTER

$$y_1 = k_c^y \, y_2^{-1}$$

Fig. 3-6 : Definition of 2-port converters and inverters.

By taking the inverse of both sides of (3-1) of (3-2) it is seen that if a 2-port is an admittance converter (or inverter) it is also an impedance converter (or inverter). Therefore the designations admittance, impedance, and immittance converter (or inverter) are entirely equivalent. The impedance conversion and inversion factors are the inverse of the admittance conversion and inversion factors, respectively.

Equation (3-1) can be written (see Fig. 3-1) as

$$\frac{i_1}{v_1} = k_c^y \left(- \frac{i_2}{v_2} \right)$$

or

$$\frac{i_2}{v_2} = (k_c^y)^{-1} \left(- \frac{i_1}{v_1} \right)$$

which means that if port 1 is terminated by an admittance y_1 the admittance y_2 presented at port 2 is

$$y_2 = (k_c^y)^{-1} y_1$$

Thus, if in a 2-port converter the ports are interchanged the resulting 2-port is also a converter; the value of the admittance or impedance conversion factor when the converter is used in one direction is the inverse of the value when it is used in the other direction. Thus when specifying a conversion factor it is necessary to indicate with which direction it is associated. This can be done, in a diagram, by using the labels $\vec{k}_c^y$ or $\overleftarrow{k}_c^y$ (similarly $\vec{k}_c^z$ or $\overleftarrow{k}_c^z$) where the arrow points towards the port to which the load immittance is to be connected (with reference to equations (3-1) or (3-3)).

In a similar way it follows from (3-2) that if a 2-port is an inverter in one direction it is also an inverter in the other direction. However, the admittance or impedance inversion factors have the same value in both directions.

A necessary and sufficient condition for a 2-port to be a converter is that it possesses a hybrid description of the form:

$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & h_{12} \\ h_{21} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix} \qquad (3\text{-}5a)$$

where h_{12} and h_{21} are related to the admittance conversion factor k_c^y by

$$k_c^y = -h_{12}\, h_{21} \qquad (3\text{-}5b)$$

(a proof of this condition is not given here since it follows immediately from a more general result in terms of multiport converters, which will be presented in chapter 4).

Converters do not have an admittance or impedance description; they have a transmission description

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} a & 0 \\ 0 & d \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \qquad (3\text{-}6a)$$

where

$$a = 1/h_{21} \quad \text{and} \quad d = -h_{12}$$

and hence

$$k_c^y = \frac{d}{a} \qquad (3\text{-}6b)$$

When the admittance conversion factor is a real constant the converter is called Positive Immittance Converter (PIC) if k_c^y is positive, and Negative Immitance Converter (NIC) if k_c^y is negative (some authors have used a different definition of PIC that includes, for instance, converters with k_c^y proportional to s or s^2 [37]). The simplified designations positive converter and negative converter will often be used in this thesis.

The ideal transformer is a non-reactive converter (i.e., a converter

for which h_{12} and h_{21} in (3-5) are real constants) with $h_{12} = -h_{21}$ (or ad = 1). It will sometimes be found convenient in this thesis to use the designation Positive Transformer (PT) instead of ideal transformer and introduce the name Negative Transformer (NT) to designate a non-reactive converter for which $h_{12} = h_{21}$ (ad = -1).

The power flowing into a non-reactive converter is

$$p = i_1(t)v_1(t) + i_2(t)v_2(t)$$

or, making use of (3-5a)

$$p = (h_{12} + h_{21})\, v_1(t)i_2(t) \qquad (3\text{-}7)$$

This shows that the ideal transformer, for which $h_{12} + h_{21} = 0$, is non-energic, i.e., the instantaneous power flowing into it is always zero. In all other cases ($h_{12} + h_{21} \neq 0$) the converter is active since v_1 and i_2 can be chosen to make $p < 0$ (note that v_1 and i_2 in (3-7) can be freely chosen since they are the independent variables in (3-5a)).

A necessary and sufficient condition for a 2-port to be an inverter is that it possesses an admittance description of the form

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & y_{12} \\ y_{21} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \qquad (3\text{-}8a)$$

The admittance conversion factor is given by

$$k_i^y = -y_{12}\, y_{21} \qquad (3\text{-}8b)$$

(this follows from a more general result to be proved in chapter 4). Inverters have both an admittance and an impedance description and do not have a hybrid matrix (excluding the interpretation of the admittance and impedance matrix as special hybrid matrices). It is possible to describe inverters by a transmission matrix:

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & b \\ c & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{3-9a}$$

where $b = -1/y_{21}$ and $c = y_{12}$ and therefore

$$k_i^y = \frac{c}{b} \tag{3-9b}$$

When the admittance inversion factor is a real constant the inverter is called Positive Immittance Inverter (PII) if k_i^y is positive, and Negative Immittance Inverter (NII) if k_i^y is negative. The simplified designations positive inverter and negative inverter will often be used in this thesis.

The gyrator is a non-reactive inverter with $y_{12} = -y_{21}$ ($bc = 1$). In a similar way as in the case of the transformer, the gyrator will be sometimes referred to as Positive Gyrator (PG), and the designation Negative Gyrator (NG) will be used for a non-reactive inverter with $y_{12} = y_{21}$ ($bc = -1$).

The power flowing into a non-reactive inverter is given by

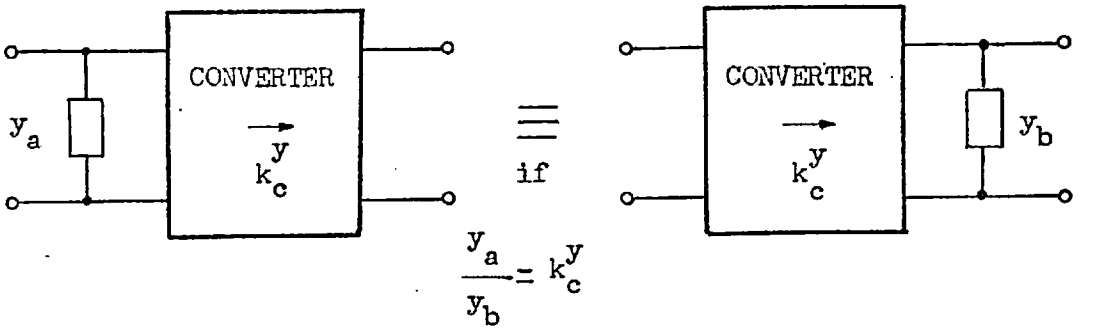
$$p = (y_{12} + y_{21})\, v_1(t) v_2(t) \tag{3-10}$$

which shows that the positive gyrator for which $y_{12} + y_{21} = 0$, is non-energic. It is therefore externally passive, even when realized using active components. All other non-reactive inverters are active since v_1 and v_2 can be chosen in such a way that p becomes negative (note that v_1 and v_2 are the independent variables in (3-8a)).

By making use of equations (3-5) it is easy to prove the equivalences shown in Fig. 3-7. The connection of a 1-port with admittance y_a in parallel with port 1 of a converter is equivalent to the connection of a 1-port with admittance y_b in parallel with the output (Fig. 3-7a) if

$$\frac{y_a}{y_b} = \vec{k}_c^y$$

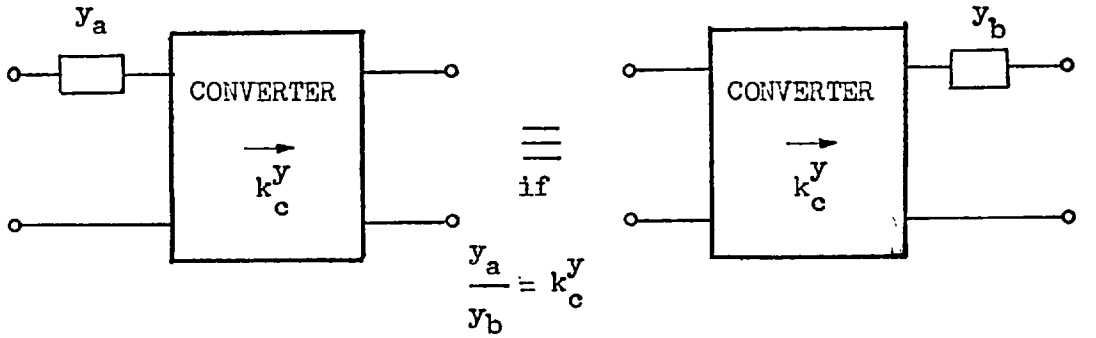
(a)



$$\frac{y_a}{y_b} = k_c^y$$

(or $z_a/z_b = k_c^z$)

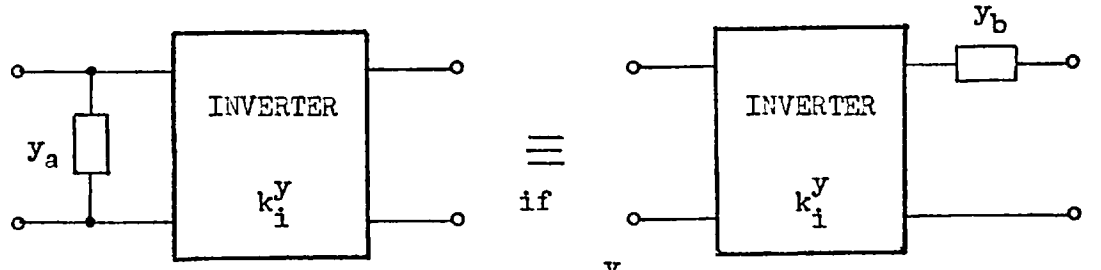
(b)



$$\frac{y_a}{y_b} = k_c^y$$

(or $z_a/z_b = k_c^z$)

Fig. 3-7 : Converter equivalences.



$$y_a\, y_b = k_i^y$$

(or $z_a\, z_b = k_i^z$)

Fig. 3-8 : An inverter equivalence.

or, in terms of impedances

$$\frac{z_a}{z_b} = \vec{k}_c^{z}$$

A similar equivalence applies to the connection of a 1-port in series with the ports of a converter (Fig. 3-7b). Using equations (3-8) it can be proved that the connection of a 1-port with admittance y_a in parallel with one of the ports of an inverter is equivalent to the connection of a 1-port with admittance y_b in series with the other port (Fig. 3-8) if

$$y_a\, y_b = k_i^{y}$$

or, in terms of impedances

$$z_a\, z_b = k_i^{z}$$

(since an inversion factor has the same value in both directions, it does not matter which of the ports is port 1 and which is port 2).

It follows immediately from the definitions (3-1) and (3-2) that (a) the 2-port resulting from the cascade connection of two converters or two inverters is a converter and (b) the 2-port resulting from the cascade connection of a converter and an inverter is an inverter. For converters and inverters with real and constant conversion and inversion factors the result of cascading any two of these 2-ports is as indicated in Table 3-1. This table shows that the set of four 2-ports {PIC, NIC, PII, NII} is a commutative group with respect to the operation of cascading, the PIC being the unit element [53]. A group with the structure shown in Table 3-1 is known as Klein's 4-group [54].

3.4 - ACTIVE REALIZATION OF CONVERTERS AND INVERTERS

In the context of active RC networks, converters and inverters are

TABLE 3-1 : The result of cascading positive and negative converters and inverters.

	PIC	NIC	PII	NII
PIC	PIC	NIC	PII	NII
NIC	NIC	PIC	NII	PII
PII	PII	NII	PIC	NIC
NII	NII	PII	NIC	PIC

realized using active components, i.e., transistors or operational amplifiers. A very large number of circuits that realize converters and inverters can be found in the literature. A few simple examples will be given here using a nullator-norator representation of the active components. In all the circuits shown the nullors can be replaced by operational amplifiers with differential input and grounded output (it should be noted that the ground may not be the terminal which is common to input and output).

Negative immittance converters (NIC's) can be realized by the simple circuits in Fig. 3-9, which contain only one nullor and two resistors.

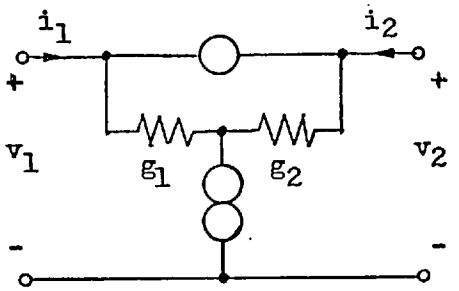
The circuit in Fig. 3-10 is a negative immittance inverter (NII) and it also contains only one nullor and two resistors.

A negative resistor can be obtained by terminating with a resistor any one of the three circuits in Figs. 3-9a, 3-9b or 3-10. The resulting circuit, shown in Fig. 3-11, is the same in all three cases. The circuit in Fig. 3-11 can be regarded either as the NIC of Fig. 3-9a terminated by g_d, or as the NIC of Fig. 3-9b terminated by g_b, or as the NII of Fig. 3-10 terminated by g_c.

The four circuits shown in Fig. 3-12 are NII's. The negative resistors might be realized by the circuit of Fig. 3-11.

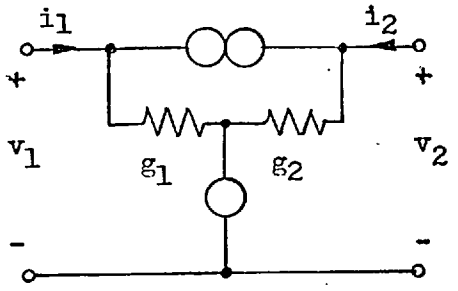
A positive immittance converter (PIC) can be obtained by cascading two NIC's or two NII's. Similarly, a positive immittance inverter (PII) can be realized as the cascade of a NIC with a NII. An example is the PII circuit of Fig. 3-13, obtained by cascading the NII of Fig. 3-12a with the NIC of Fig. 3-9a. This circuit is a gyrator if $g_1 = g_2$.

The simple circuits presented so far will now be used to illustrate several comments that can be made concerning realizations of converters



$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & g_1/g_2 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$$

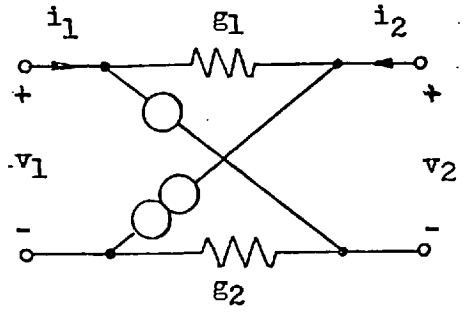
(a)



$$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ -g_1/g_2 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$$

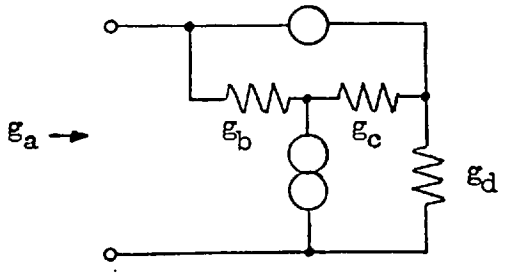
(b)

Fig. 3-9 : Negative Immittance Converters (NIC's).



$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & -g_1 \\ -g_2 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

Fig. 3-10 : Negative Immittance Inverter (NII).



$$g_a = -\frac{g_b\, g_d}{g_c}$$

Fig. 3-11 : Simulation of a negative conductance.

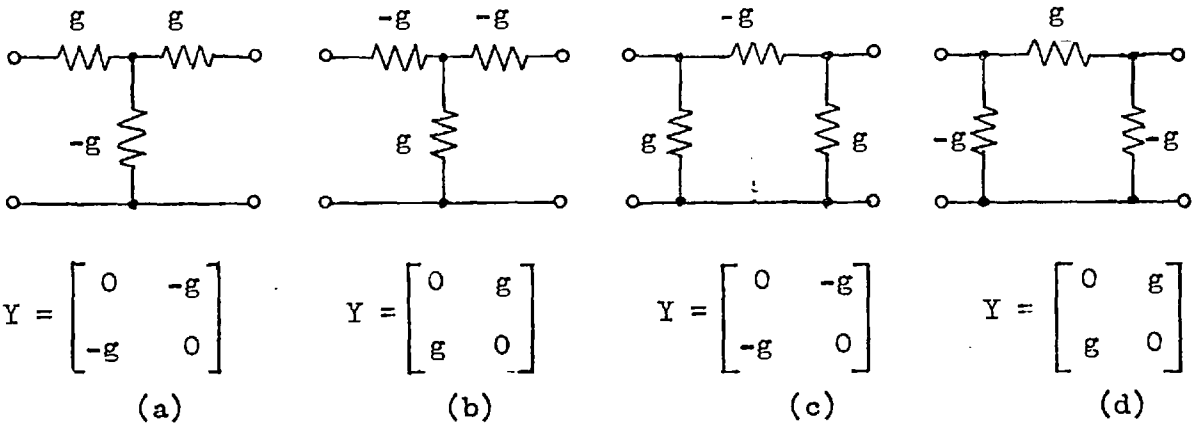


Fig. 3-12 : Negative immittance inverters.

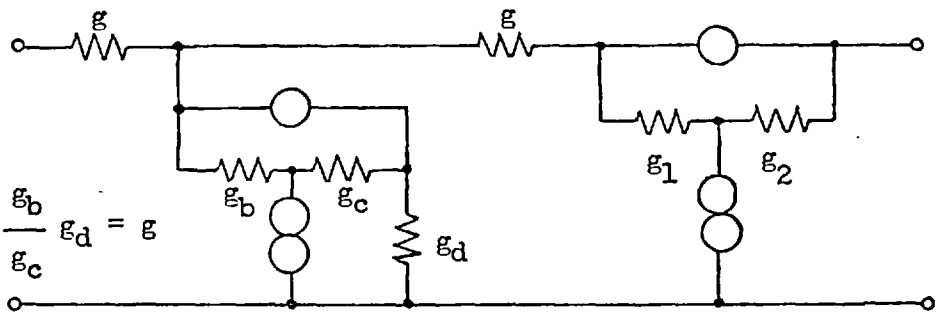


Fig. 3-13 : PII obtained by cascading the NII in Fig. 3-12a with the NIC in Fig. 3-9a.

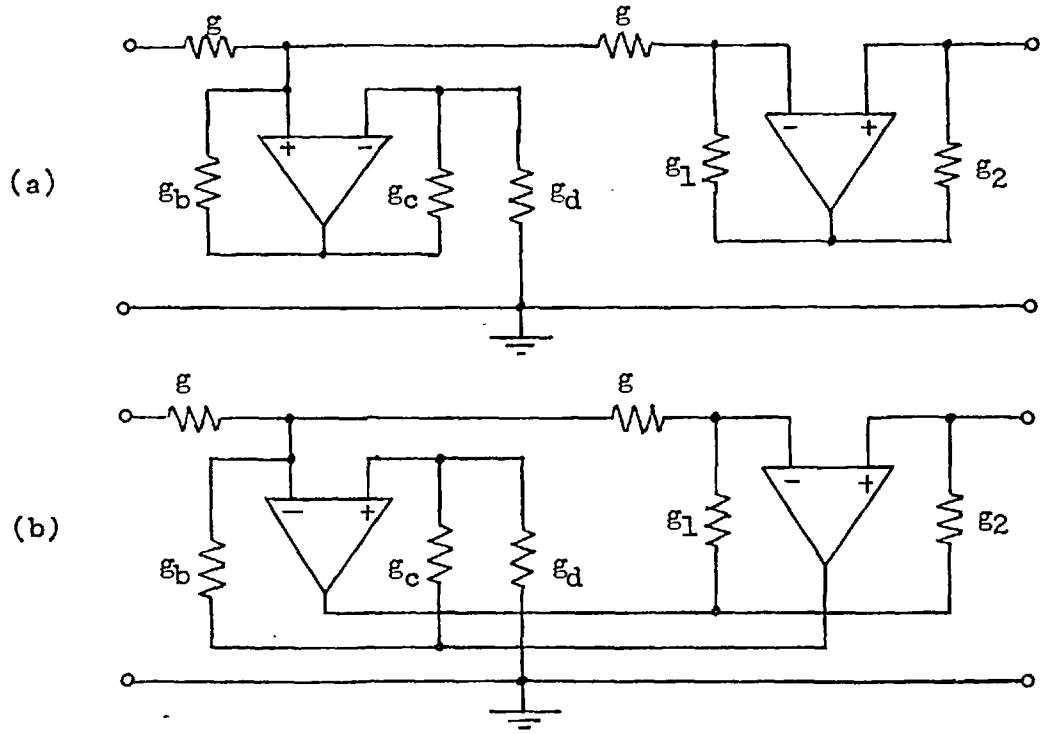


Fig. 3-14 : Two different operational amplifier realizations of the nullor circuit in Fig. 3-13.

and inverters.

In most applications, converters and inverters must have at least one grounded port; there are applications (some of them will be discussed later) in which converters and inverters with both ports grounded are required. When the nullor is replaced by an operational amplifier (with grounded output) the NIC of Fig. 3-9a will have both ports grounded, whereas in the NIC of Fig. 3-9b only one port will be grounded. Whereas the NII of Fig. 3-10 will have only one grounded port, the NII's in Figs. 3-12a and 3-12d will have both ports grounded if the negative resistors are realized by the circuit of Fig. 3-11 (with the nullor replaced by an operational amplifier). The PII in Fig. 3-13 will have both ports grounded; however a PII obtained by cascading the NIC of Fig. 3-9a with the NII of Fig. 3-10 will have only one grounded port.

Some circuits realizing converters or inverters require that the components be related in a specific way; if one component changes (for instance the value of a resistor changes) the circuit is no longer a converter or inverter. This is the case with the NII's of Fig. 3-12 which are only inverters when the conductances are related as indicated in the circuit diagrams. There are other circuits which remain converters or inverters independently of the values of some or all the components; only the value of the conversion or inversion factor will be affected if one component changes. Examples of this are the circuits of Fig. 3-9 which are converters for any values of g_1 and g_2, and the circuit of Fig. 3-10 which is an inverter for any g_1 and g_2. The circuit of Fig. 3-13 remains an inverter for any values of g_1 and g_2 but the remaining conductances in the circuit must be related as shown in the diagram.

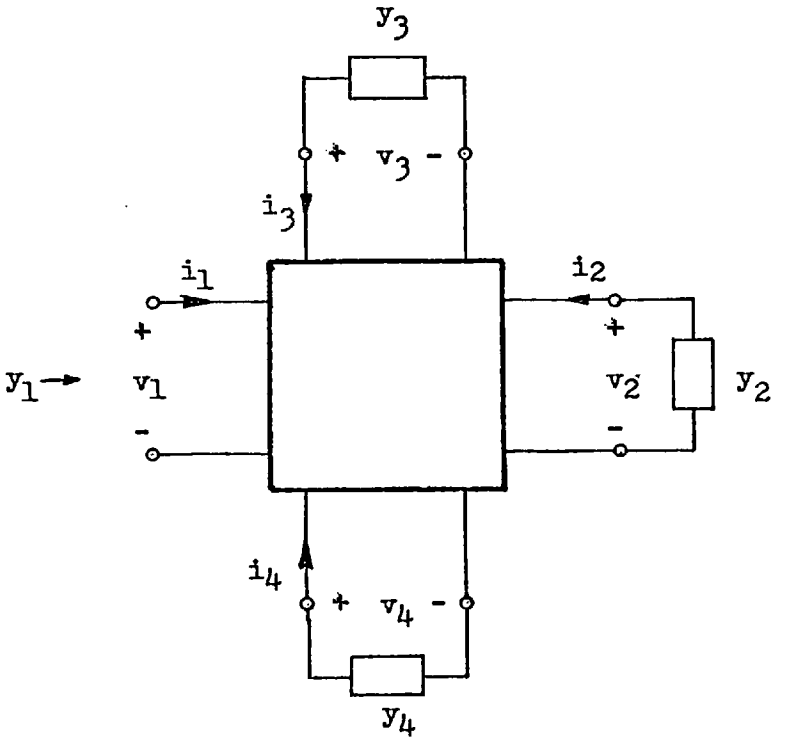
It was mentioned before (section 2.2) that different operational amplifier realizations of the same nullor circuit can differ very much in their non-ideal performance. This is the case with the two circuits in Fig. 3-14 which correspond to two different ways of pairing the nullator and norators in the PII of Fig. 3-13 to form nullors which are then replaced by operational amplifiers. It has been shown [11] that the circuit of Fig. 3-14b has better stability properties than the circuit of Fig. 3-14a.

Another useful observation concerning realizations of converters and inverters is the following: there are circuits which produce different converters and inverters corresponding to different choices of 2-terminal components which are extracted to form ports [13, 52, 55-58]. As an example, consider a 1-port network with port admittance y_1 related to the admittances y_2, y_3 and y_4 of some 2-terminal components inside the network, by the equation

$$y_1 = k \frac{y_2 y_3}{y_4} \qquad (3\text{-}11)$$

where k is independent of y_2, y_3 and y_4 [52]. If y_2 is extracted and regarded as the termination of a second port, then the resulting 2-port is a converter. If, instead of y_2, y_3 is extracted, another converter is obtained, and if y_4 is extracted the resulting 2-port is an inverter. If port 1 is terminated by an admittance y_1 and two of the other three admittances are extracted to form ports, converters are obtained by extracting y_2 and y_4 or y_3 and y_4, and an inverter will result from the extraction of y_2 and y_3. This follows from the fact that if y_2, y_3 and y_4 are extracted to form ports (Fig. 3-15), equation (3-11) leads to

$$\frac{i_1}{v_1} \frac{i_4}{v_4} = -k \frac{i_2}{v_2} \frac{i_3}{v_3}$$



$$y_1 = k \frac{y_2 y_3}{y_4}$$

$$\frac{i_1}{v_1} = k \frac{\dfrac{-i_2}{v_2} \quad \dfrac{-i_3}{v_3}}{\dfrac{-i_4}{v_4}}$$

Fig. 3-15 : A circuit that realizes various converters and inverters.

In this case, four admittances are involved in (3-11) and therefore there are $\binom{4}{2} = 6$ different combinations of two ports leading each one to a converter or inverter. It should be noted that (depending on the actual circuit involved) different combinations may lead to converters or inverters with the same circuit diagram. It should also be noted that the number of admittances appearing in an equation with the form of (3-11) can be different from 4. In particular, a circuit for which only two admittances can be related by an equation similar to (3-11) (i.e. $y_1 = k\, y_2$ or $y_1 = k\, y_2^{-1}$) realizes only one converter or only one inverter.

An example that illuatrates the above discussion is provided by the circuit in Fig. 3-11 for which equation (3-11) is applicable. It has already been pointed out that this circuit leads to the NIC's of Fig. 3-9 or to the NII of Fig. 3-10 depending on which of the conductances g_d, g_b or g_c, respectively, is considered as the termination of a second port. It can easily be verified that the other three possible 2-ports (extraction of g_b and g_c, g_d and g_c or g_b and g_d) have the same circuit diagrams as the NIC's in Fig. 3-9 or as the NII in Fig. 3-10.

3.5 - SIMULATION OF GROUNDED AND FLOATING INDUCTORS

Inductors can be simulated by a positive inverter terminated by a capacitor. This can be seen immediately from equation (3-2) applied to this case ($y_2 = sC$):

$$y_1 = k_i^y \frac{1}{sC} = \frac{1}{sL} \qquad (3\text{-}12)$$

where

$$L = \frac{C}{k_i^y}$$

is the simulated inductance. The positive inverters employed are usually gyrators.

Alternatively, an inductor can be simulated by a converter with an admittance conversion factor of the form

$$k_c^y = k\, s^{-1}$$

where k is a positive real constant. When such a converter is terminated by a resistor of conductance g, equation (3-1) yields:

$$y_1 = \frac{k}{s}\, g = \frac{1}{sL} \qquad (3\text{-}13)$$

where

$$L = \frac{1}{kg}$$

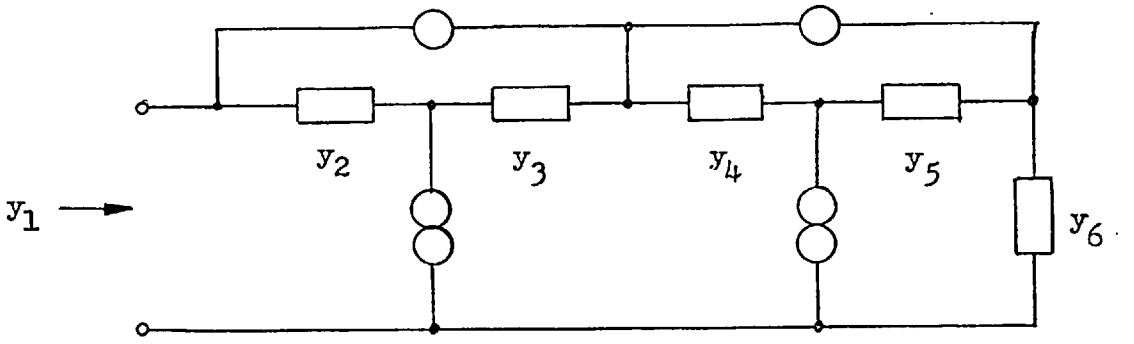
is the simulated inductance.

The simulation of inductors by terminated 2-port converters is applicable to grounded inductors since these can be regarded as 1-ports. The converters or inverters must in this case have one grounded port.

Some of the circuits that can be used to simulate inductors can be regarded either as a PII terminated by a capacitor or as a converter terminated by a resistor, depending on whether a capacitor or a resistor is considered as the termination. An example of such a circuit is shown in Fig. 3-16. This circuit can be regarded as a cascade of two of the NIC circuits of Fig. 3-9a (with the resistors replaced by general 2-terminal components) terminated by y_6. The input admittance of the circuit in Fig. 3-16 is given by

$$y_1 = \frac{y_2\, y_4\, y_6}{y_3\, y_5} \qquad (3\text{-}14)$$

This circuit has been referred to in the literature as a PIC in view of the fact that the right hand side of (3-14) is preceded by a plus sign (if $y_1 = -y_2\, y_4\, y_6/y_3\, y_5$ the circuit would be called a NIC). According



$$y_1 = \frac{y_2\, y_4\, y_6}{y_3\, y_5}$$

Fig. 3-16 : A circuit that can be used to simulate inductors or FDNR's.

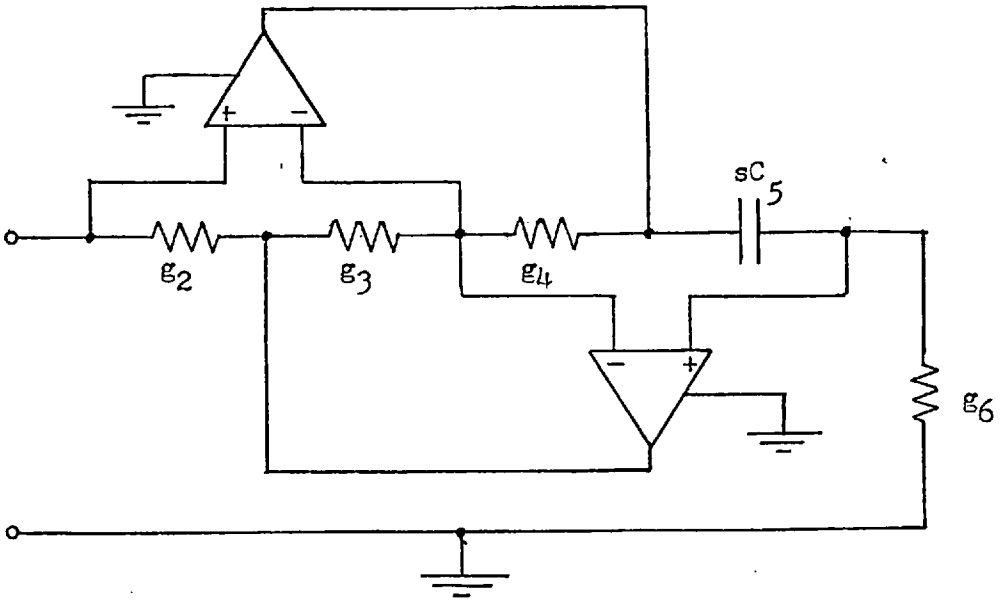


Fig. 3-17 : Inductor simulation by an operational amplifier realization of the circuit in Fig. 3-16.

to the terminology adopted in this thesis such a circuit will only be called a PIC when a converter is formed by extraction of one of the admittances in the numerator of (3-14) and the conversion factor is a positive real constant. The designation generalized impedance converter (GIC) has also been used for the circuit in Fig. 3-16.

The circuit in Fig. 3-16 can be used to simulate an inductor by using a capacitor in the place of one of the 1-ports with admittances y_3 or y_5, and resistors elsewhere. The resulting circuit can be regarded as a positive inverter terminated by the capacitor or as a converter terminated by one of the resistors whose conductances appear in the numerator of (3-14).

The circuit of Fig. 3-16 is useful in connection with the active RC simulation of doubly-terminated LC ladder filters not only when the inductor simulation method is used, but also in the case of the impedance scaling method. As discussed before, this last method requires the use of FDNR's which can be either supercapacitors, with admittances proportional to s^2 or superinductors, with admittances proportional to s^{-2}. As shown by (3-14), a supercapacitor can be obtained by using capacitors to produce two of the admittances in the numerator and resistors to realize the remaining admittances; a superinductor is obtained if y_3 and y_5 are realized as capacitors and y_2, y_4 and y_6 as resistors.

All the converters derived from the circuit of Fig. 3-16 behave as converters for any value of the admittances of the components; the same applies to the inverters. This is a desirable property, since it seems reasonable to expect a better sensitivity performance than in the cases where the components have to be related in a specified way.

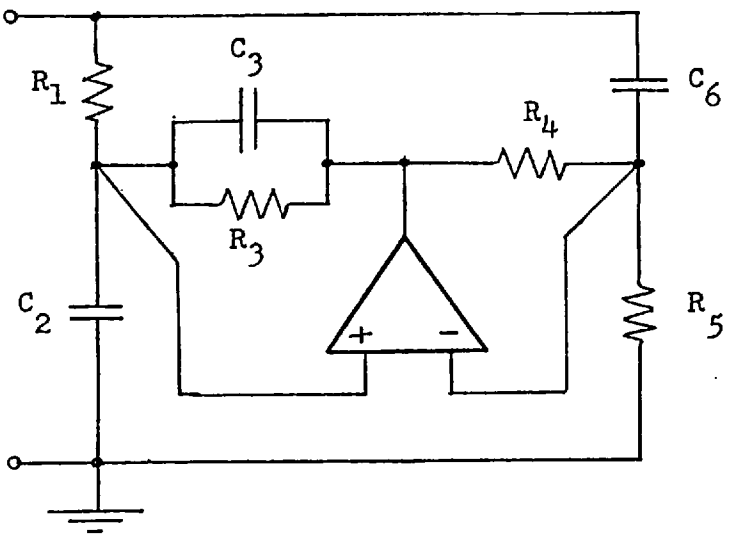
The circuit of Fig. 3-16 can be realized with two operational amplifiers (with differential input and grounded output) in many

different ways. The non-ideal performance of the different realizations has been extensively investigated [13, 34, 59-63]. It has been shown that some realizations have very good performance and these have been widely used in active filters simulating doubly-terminated ladders. This is the reason why the circuit was chosen here as an example. The inductor simulation circuit in Fig. 3-17 is a particular realization of the nullor circuit in Fig. 3-16. It has been shown that this realization possesses particularly good high-frequency performance [60].

It may be noted that the inverters obtained from Fig. 3-16 if the nullors are replaced by operational amplifiers will have only one grounded port; in the converter obtained by extraction of y_6 both ports will be grounded.

Although most of the circuits that have been used for the simulation of inductors are interpretable as terminated inverters or converters, this is not true for all inductor simulation circuits. An example of a circuit that can be used to simulate inductors but cannot be interpreted as a converter or inverter is shown in Fig. 3-18 [30, 64, 65]. This circuit only simulates an inductor if the relationships given in Fig. 3-18 involving <u>all</u> the components are satisfied. Thus it is not possible to extract one component and consider it as the termination of a converter or inverter since it is not possible to write equations in the form of (3-1) or (3-2) valid for <u>any</u> value of the terminating admittance.

Inductor simulation using converters or inverters leads to lossless inductors, assuming ideal performance of all the components involved. The same is true for the circuit of Fig. 3-18. There are, however, circuits that have been proposed for the simulation of lossy inductors; an example of such a circuit [66] is given in Fig. 3-19.



$$\frac{R_4}{R_5} = \frac{C_2}{C_3}$$

$$\frac{R_3}{R_1} = \frac{C_6}{C_3}$$

$$C_6 = C_2$$

Fig. 3-18 : Inductor simulation by a circuit which cannot be interpreted as an inverter or converter.

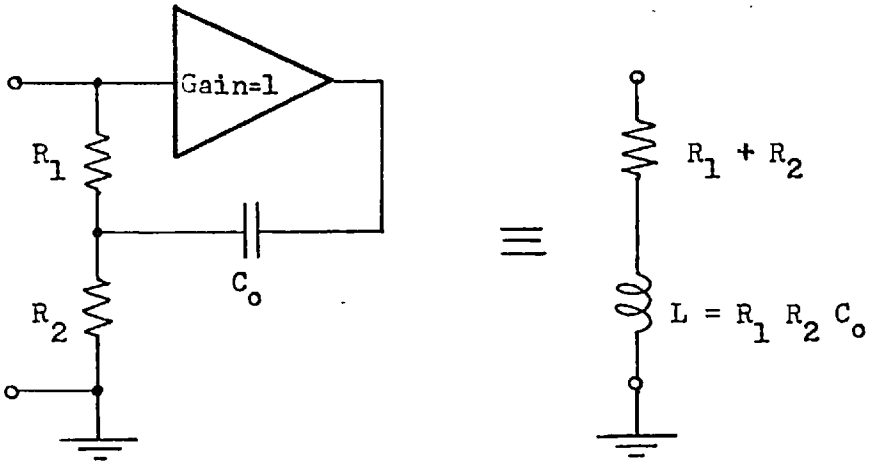


Fig. 3-19 : Simulation of a lossy inductor.

It is useful to note that a circuit that simulates a lossless inductor using only one capacitor (in addition to resistors and nullors) must be an inverter terminated by the capacitor, since the defining equation for an inverter (3-2) is necessarily satisfied for any termination.

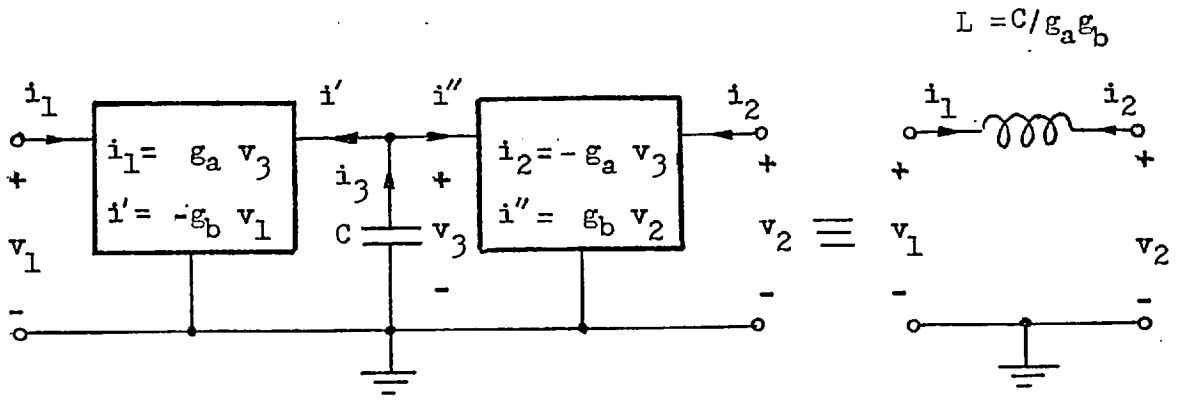
As mentioned before, an active RC circuit that simulates a floating inductor can be regarded as a 2-port (Fig. 3-4b). Later in this thesis it will be shown that most of the circuits that have been proposed for the simulation of floating inductors can be interpreted as 3-port inverters terminated by a capacitor or as 3-port converters terminated by a resistor. These 3-port inverters and converters are special cases of the multiport converters and inverters which are proposed in this thesis as a generalization of 2-port converters and inverters. Since a study of floating inductor simulation using 3-port inverters and converters is one of the main questions investigated in this thesis (chapter 6), in the present review chapter only two well known circuits, one using two grounded 2-port inverters, the other employing two grounded 2-port converters, will be mentioned.

The circuit in Fig. 3-20 uses two grounded positive inverters and one capacitor to simulate a floating inductor [67]. The circuit of Fig. 3-21 uses two grounded converters and one resistor [37, 68]; the admittance conversion factor of both converters must be

$$k_c^y = h_a h_b = k s^{-1}$$

where k is a positive real constant.

The grounded converter obtained from the circuit in Fig. 3-16 by extraction of g_b could be used to realize the circuit of Fig. 3-21. The inverters derived from the circuit of Fig. 3-16 are not grounded (it is impossible to ground both ports) and therefore cannot be used to



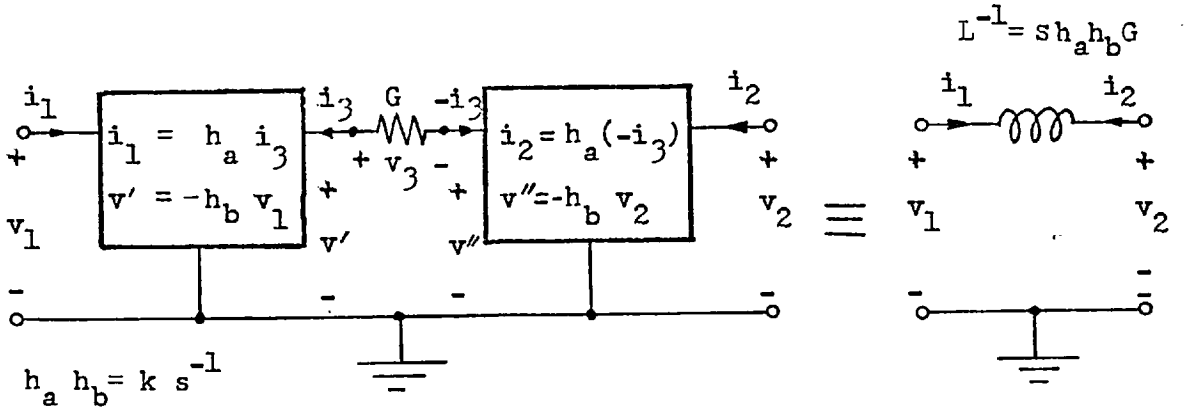
$$v_3 = -\frac{1}{sC} i_3 = -\frac{1}{sC}(i' + i'') = \frac{1}{sC}(g_b v_1 - g_b v_2)$$

$$i_1 = g_a v_3 = \frac{g_a g_b}{sC}(v_1 - v_2)$$

$$i_2 = -g_a v_3 = \frac{g_a g_b}{sC}(-v_1 + v_2)$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{1}{sL}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

Fig. 3-20 : Floating inductor simulation with two grounded inverters.



$$i_3 = -G v_3 = -G(v' - v'') = G(h_b v_1 - h_b v_2)$$

$$i_1 = h_a i_3 = h_a h_b G(v_1 - v_2)$$

$$i_2 = -h_a i_3 = h_a h_b G(-v_1 + v_2)$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{1}{sL}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

Fig. 3-21 : Floating inductor simulation with two grounded converters.

realize the circuit of Fig. 3-20; an inverter of the type shown Figs. 3-14 could be used.

3.6 - THE (ad, bc)-PLANE

It has been found useful to represent 2-ports described by real parameters as points in the (ad, bc)-plane [69-71, 32]. The symbols a, b, c and d represent the elements of the transmission matrix

$$T = \begin{bmatrix} a & b \\ c & d \end{bmatrix}$$

From the transmission description of converters and inverters (section 3.3) it follows immediately that PIC's are represented by points on the positive (ad)-axis and NIC's are represented by points on the negative (ad)-axis, as shown in Fig. 3-22. Similarly, PII's and NII's are represented by points on the positive and negative (bc)-axis, respectively (Fig. 3-22).

Reciprocal 2-ports for which

$$\det T = ad - bc = 1 \qquad (3\text{-}15)$$

are represented by points in the 'reciprocal line' shown in Fig. 3-22. The positive transformer (PT) and the negative gyrator (NG) are represented by the points of intersection of this line with the ad and bc axes, respectively (the PT and the NG were introduced in section 3.3).

Two-ports for which

$$\det T = ad - bc = -1 \qquad (3\text{-}16)$$

have been considered as anti-reciprocal [69-71] (this is suggested by the contrast with reciprocal 2-ports for which det T = ad - bc = +1). Such 2-ports are represented by points on the 'anti-reciprocal' line shown in Fig. 3-22. The positive gyrator (PG) and the negative

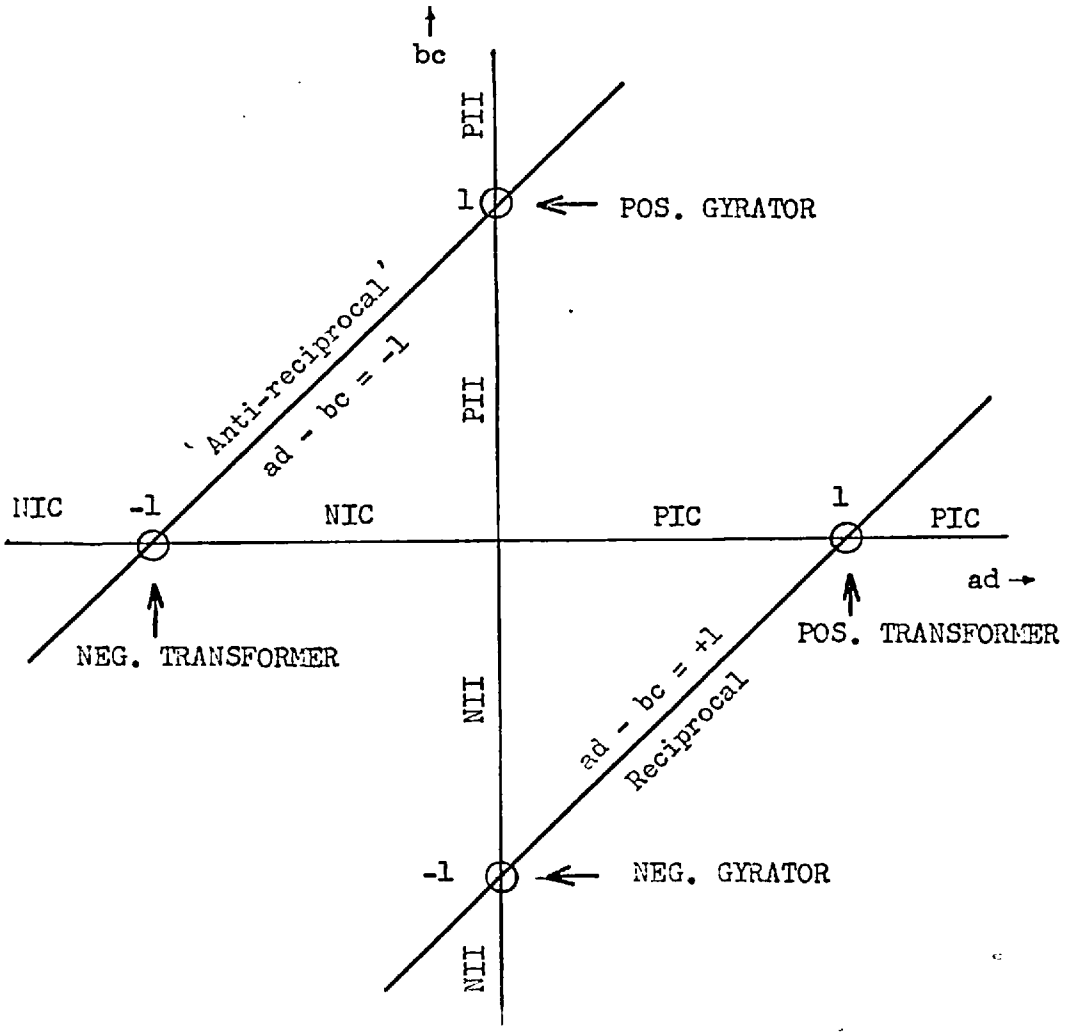


Fig. 3-22 : Converters and inverters in the (ad,bc)-plane.

transformer (NT) are represented by the points of intersection of this line with the coordinate axes (Fig. 3-22).

The four 2-ports, positive and negative transformer and positive and negative gyrator, provide very clear examples that reciprocity--non-reciprocity and activity-passivity can be combined in all possible ways:

PT: reciprocal and passive

NG: reciprocal and active

PG: non-reciprocal and passive

NT: non-reciprocal and active

There has always been a close association of converters and inverters with the concepts of reciprocity and anti-reciprocity. This is particularly true in the case of the gyrator which has been regarded since its introduction by Tellegen [72] as a prototype non-reciprocal network element. The results of an investigation of various network properties related to the concept of reciprocity and anti-reciprocity will be considered later in this thesis.

CHAPTER 4

MULTIPORT CONVERTERS AND INVERTERS

4.1 - INTRODUCTION

As discussed in the previous chapter, 2-port immittance converters and inverters are important active units used in the realization of active RC networks. A review of the definition and more salient features of 2-port converters and inverters was presented in section 3.3. It was seen that ideal transformers and gyrators are special cases of 2-port converters and inverters, respectively. Multiport versions of these special converters and inverters can be found in the literature. These are the 'multiwinding transformer' [4-6] and the 'multiterminal gyrator' [38, 39]. It is believed, however, that a full extension to multiports of the general concepts of 2-port immittance conversion and inversion has not been given in the literature.(*) Such an extension will be proposed and discussed in this chapter.

Multiport admittance and impedance converters and inverters will be defined in terms of the operation performed on the matrix description of a 'load' multiport, since it is this operation which is directly relevant to the application of these multiports. The matrix description

---

(*) There is a brief mention in [22] of 'n-port generalized converters and inverters'. This, however, has little relationship with the approach followed here (the n-port inverter is there defined as any n-port described by a non-singular admittance matrix, which leads, for n = 2, to the inclusion of many 2-ports which are not immittance inverters according to the usual definition).

of the converters and inverters is derived from the definitions. The alternative approach of giving the definitions in terms of the matrix description has the disadvantage that multiports with a different description might perform the same operations and hence be equally suited for a specific application. The approach taken here eliminates such a possibility by establishing necessary conditions for the operations of conversion or inversion to take place.

It will be shown that the proposed definitions include, as special cases, the 2-port converters and inverters, the multiwinding transformer, the multiterminal gyrator, and many of the circuits used for the simulation of floating inductors and floating negative impedances. However, it is found that they do not include the circulator (which might in some respects be regarded as a multiport version of the gyrator).

Examination of the properties of multiport converters and inverters leads to a somewhat unexpected result: it is shown that, in contrast to 2-port converters and inverters, multiport admittance converters (or inverters) are not in general simultaneously impedance converters (or inverters). This is a consequence of the definitions proposed here, which do not include the requirement of simultaneous admittance and impedance conversion (or inversion). The inclusion of such a requirement in the definitions would be unduly restrictive, since this would lead to the exclusion of several circuits which seem clearly associated with admittance or impedance conversion or inversion, for example most of the circuits used in the active RC simulation of inductive networks.

Finally, it will be shown that admittance and impedance converters and inverters can be regarded as special cases of a more general multiport, the 'hybrid converter', which is introduced and briefly discussed in the last section of this chapter.

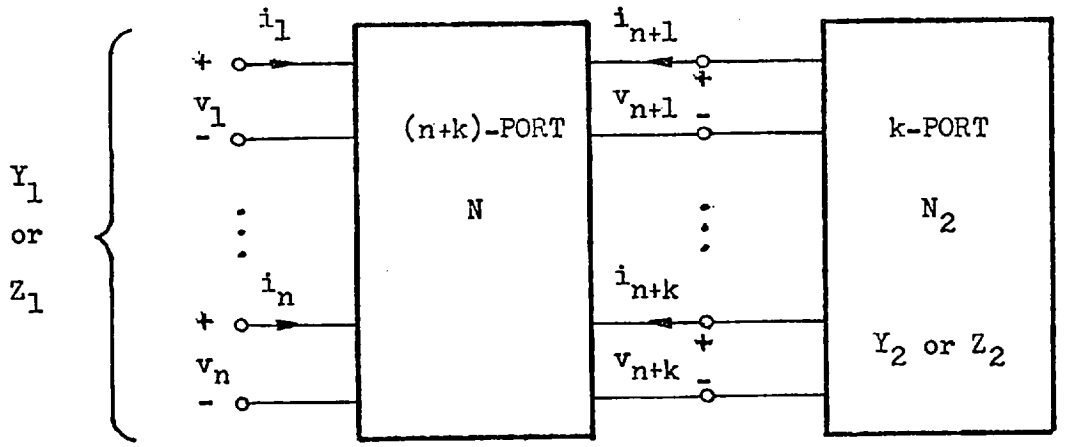
4.2 - DEFINITIONS

In order to introduce the definitions of multiport converters and inverters, consider an (n + k)-port N with n input ports and k output ports (Fig. 4-1). Assume that a 'load' k-port N_2 with an admittance matrix Y_2 or an impedance matrix Z_2 is connected to N as shown in Fig. 4-1. It is assumed that the n-port resulting from this connection of N and N_2 has an admittance matrix Y_1 or an impedance matrix Z_1.

The definition of the 2-port admittance converter involves the equation $Y_1 = k_c^y Y_2$, where k_c^y is a scalar that depends only on the converter and not on the terminating one-port. A first attempt to define a multiport admittance converter might result in the use of an expression of the form $Y_1 = K\ Y_2$ or $Y_1 = Y_2 K$ where K is a matrix that depends only on the converter. However, since matrix multiplication is not commutative, these two expressions are not equivalent. Furthermore, expressions of this form cannot be used if the square matrices Y_1 and Y_2 have different dimensions. Therefore it seems natural to use an expression of the form $Y_1 = H_{12}\ Y_2\ H_{21}$. Expressions of this form will also be used for the impedance converter and for the admittance and impedance inverters.

The following definitions are proposed: the (n + k)-port N is an Admittance Converter, Admittance Inverter, Impedance Converter or Impedance Inverter(*) if equations (4-1), (4-2), (4-3) or (4-4) respectively, are satisfied:

(*) The reason for having two types of converters (admittance and impedance) and similarly two types of inverters instead of one immittance converter and one immittance inverter will be discussed later.



$$I_1 = \begin{bmatrix} i_1 \\ \vdots \\ i_n \end{bmatrix} \qquad V_1 = \begin{bmatrix} v_1 \\ \vdots \\ v_n \end{bmatrix} \qquad I_2 = \begin{bmatrix} i_{n+1} \\ \vdots \\ i_{n+k} \end{bmatrix} \qquad V_2 = \begin{bmatrix} v_{n+1} \\ \vdots \\ v_{n+k} \end{bmatrix}$$

Fig. 4-1 : An (n+k)-port terminated by a k-port.

ADMITTANCE CONVERTER: $Y_1 = H_{12}\ Y_2\ H_{21}$ (4-1)

ADMITTANCE INVERTER: $Y_1 = G_{12}\ Z_2\ G_{21}$ (4-2)

IMPEDANCE CONVERTER: $Z_1 = K_{12}\ Z_2\ K_{21}$ (4-3)

IMPEDANCE INVERTER: $Z_1 = R_{12}\ Y_2\ R_{21}$ (4-4)

In these equations, Y_2 and Z_2 are k-square matrices, Y_1 and Z_1 are n-square, letters with subscripts 12 denote (n x k) matrices and letters with subscripts 21 denote (k x n) matrices. The matrices H_{12}, H_{21}, G_{12}, G_{21}, K_{12}, K_{21}, R_{12} and R_{21} depend only on the (n + k)-port N. The defining expressions must be valid for any load k-port N_2 that possesses an admittance description in the cases of (4-1) and (4-4) or an impedance description in the cases of (4-2) and (4-3).

The justification for the designations is obvious in the case of the converters. The choice of the name 'admittance inverter' for the multiport to which equation (4-2) applies is suggested by the fact that if N_2 has an admittance description, then $Z_2 = Y_2^{-1}$ and (4-2) becomes $Y_1 = G_{12}\ Y_2^{-1}\ G_{21}$. It should be noted, however, that it is not required in the definition of the admittance inverter that N_2 has both admittance and impedance description: it is only required that it has an impedance description and hence the appearance of Z_2, instead of Y_2^{-1}, in (4-2). Similar considerations apply to the impedance inverter.

Two-port converters in which the conversion factor is a rational function of the complex frequency variable s are often useful. In a similar way, for the multiport converters and inverters, it will be assumed that matrices H, G, K and R need not be matrices over the real field: they can, in general, be matrices over the field of rational functions of s.

Having proposed these definitions, it remains to be seen if they lead to meaningful consequences. This will be done in the next sections.

4.3 - MATRIX DESCRIPTION

The necessary and sufficient conditions, in terms of the matrix description, for the (n + k)-port N to be a converter or an inverter according to the definitions given above are presented in Table 4-1 (equations (4-5) to (4-8)). It can be seen that there is a very simple relationship between the non-zero submatrices in the matrix description and the matrices that appear in the definitions (Table 4-1). The sufficiency of the type of descriptions shown in Talbe 4-1 can easily be verified. The proof of necessity is less straightforward and will now be presented.

The admittance converter will be considered first. Since it is not known a priori which types of matrix description the converter will have, it is assumed that N is described by the general equation $MI + PV = O$ with the matrices partitioned in correspondence with the partition of the ports of N in n input and k output ports (Fig. 4-1):

$$\begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} + \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = O \qquad (4\text{-}9)$$

where

$$I_1 = \begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix} \qquad I_2 = \begin{bmatrix} i_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ i_{n+k} \end{bmatrix} \qquad V_1 = \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_n \end{bmatrix} \qquad V_2 = \begin{bmatrix} v_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ v_{n+k} \end{bmatrix}$$

and the submatrices M_{11} and P_{11} are n-square M_{22} and P_{22} are k-square, M_{12} and P_{12} are (n x k) and M_{21} and P_{21} are (k x n).

Equation (4-9) remains valid after both M and P are subjected to the same elementary row-transformations (interchange of two rows; multiplication of a row by a scalar; addition of one row multiplied

TABLE 4-1 : Definition and matrix description of multiport converters and inverters.

DESIGN.	DEFINITION	MATRIX DESCRIPTION
ADMITTANCE CONVERTER	$Y_1 = H_{12} Y_2 H_{21}$ (4-1)	$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \begin{bmatrix} 0 & \propto H_{12} \\ -\frac{1}{\propto} H_{21} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$ (4-5)
ADMITTANCE INVERTER	$Y_1 = G_{12} Z_2 G_{21}$ (4-2)	$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \begin{bmatrix} 0 & \propto G_{12} \\ -\frac{1}{\propto} G_{21} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$ (4-6)
IMPEDANCE CONVERTER	$Z_1 = K_{12} Z_2 K_{21}$ (4-3)	$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \begin{bmatrix} 0 & \propto K_{12} \\ -\frac{1}{\propto} K_{21} & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$ (4-7)
IMPEDANCE INVERTER	$Z_1 = R_{12} Y_2 R_{21}$ (4-4)	$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \begin{bmatrix} 0 & \propto R_{12} \\ -\frac{1}{\propto} R_{21} & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$ (4-8)

Note: $\propto$ is an arbitrary non-zero scalar.

by a scalar to another row). Since it is always possible to reduce a square matrix to an upper-triangular form by row-transformations, it can be assumed, without loss of generality that either M or P in (4-9) is upper-triangular. In the case of the admittance converter it is convenient to assume that M is upper-triangular and consequently $M_{21} = 0$. Taking this into account, (4-9) can be written as

$$M_{11} I_1 + M_{12} I_2 + P_{11} V_1 + P_{12} V_2 = 0 \qquad (4\text{-}10a)$$

$$M_{22} I_2 + P_{21} V_1 + P_{22} V_2 = 0 \qquad (4\text{-}10b)$$

The load k-port N_2 (Fig. 4-1) is described, in the case of the admittance converter, by

$$I_2 = -Y_2 V_2 \qquad (4\text{-}11)$$

where the (-) sign results from the choice of the reference direction for I_2 into the k output ports of N and therefore out of N_2.

Equations (4-10), in conjunction with (4-11) yield:

$$M_{11} I_1 + P_{11} V_1 + (P_{12} - M_{12} Y_2) V_2 = 0 \qquad (4\text{-}12a)$$

$$P_{21} V_1 + (P_{22} - M_{22} Y_2) V_2 = 0 \qquad (4\text{-}12b)$$

According to the definition, (4-1), Y_1 must exist for any Y_2. This means that it must be possible to terminate the (n + k)-port N by connecting any Y_2 to the output and imposing the value of V_1 at the input. With such a termination it must be possible to determine the value of all voltages and currents at the ports of N, since, if a multiport has physical meaning, all port voltages and currents can be determined when the multiport is terminated (i.e. connected to an external network which includes independent sources) in a permissible way [7]. Therefore it is required that $(P_{22} - M_{22} Y_2)$ be non-singular for any Y_2 (otherwise it would be impossible to determine V_2). One consequence of

this is that P_{22} must be non-singular, so that the case $Y_2 = 0$ is included; another consequence is that it is necessary that

$$M_{22} = 0 \tag{4-13}$$

since it can be shown (Appendix, Lemma I) that otherwise Y_2 can always be chosen such that $(P_{22} - M_{22}\ Y_2)$ is singular. Taking these results into account and noting that Y_{11} must be non-singular (otherwise the n-port resulting from the connection of N and N_2 would not have an admittance description) it follows from (4-12) that

$$Y_1 = -M_{11}^{-1}\ (P_{11} - P_{12}\ P_{22}^{-1}\ P_{21}) - M_{11}^{-1}\ M_{12}\ Y_2\ P_{22}^{-1}\ P_{21} \tag{4-14}$$

Since, for an admittance converter, Y_1 must be related to Y_2 by an equation of the form of (4-1), i.e. $Y_1 = H_{12}\ Y_2\ H_{21}$, it follows that

$$M_{11}^{-1}\ (P_{11} - P_{12}\ P_{22}^{-1}\ P_{21}) = 0 \tag{4-15}$$

and

$$-M_{11}^{-1}\ M_{12}\ Y_2\ P_{22}^{-1}\ P_{21} = H_{12}\ Y_2\ H_{21} \tag{4-16}$$

It can be shown (Appendix, Lemma II) that if (4-16) is satisfied for any Y_2, then

$$-M_{11}^{-1}\ M_{12} = \alpha\ H_{12} \tag{4-17}$$

and

$$P_{22}^{-1}\ P_{21} = \frac{1}{\alpha}\ H_{21} \tag{4-18}$$

where α is an arbitrary non-zero scalar.

From (4-10b) and (4-13) it follows that

$$V_2 = -P_{22}^{-1}\ P_{21}\ V_1 \tag{4-19}$$

or, making use of (4-18),

$$V_2 = -\frac{1}{\alpha} H_{21}\ V_1 \tag{4-20}$$

From (4-10a) and (4-19) it follows that

$$I_1 = -M_{11}^{-1} M_{12} I_2 - M_{11}^{-1} (P_{11} - P_{12} P_{22}^{-1} P_{21}) V_1$$

or, taking into account (4-15) and (4-17),

$$I_1 = \alpha H_{12} I_2 \qquad (4\text{-}21)$$

Equations (4-21) and (4-20) can be written in the form of (4-5), in Table 4-1, which is thus the description that is necessary and sufficient that a multiport possesses in order to be an admittance converter.

The proof of the necessity of (4-6) for the admittance inverter follows a similar pattern. The results for the impedance converter, (4-7) and inverter, (4-8), are then immediate, since all their equations have the same form of those applying to the admittance converter and inverter, respectively, if the V's and I's are interchanged.

4.4 - THE DIFFERENCE BETWEEN 'ADMITTANCE' AND 'IMPEDANCE' CONVERTERS AND INVERTERS

The (n + k)-port N will only be simultaneously an admittance converter and an impedance converter if it accepts both a description in the form of (4-5) and in the form of (4-7). Since these two descriptions differ by the interchange of dependent and independent variables, the matrix in (4-5)

$$H = \begin{bmatrix} 0 & \alpha H_{12} \\ -\frac{1}{\alpha} H_{21} & 0 \end{bmatrix} \begin{matrix} n \\ k \end{matrix}$$

$$\underbrace{\qquad}_{n} \quad \underbrace{\qquad}_{k}$$

must be non-singular. This means that it is necessary that the sub-

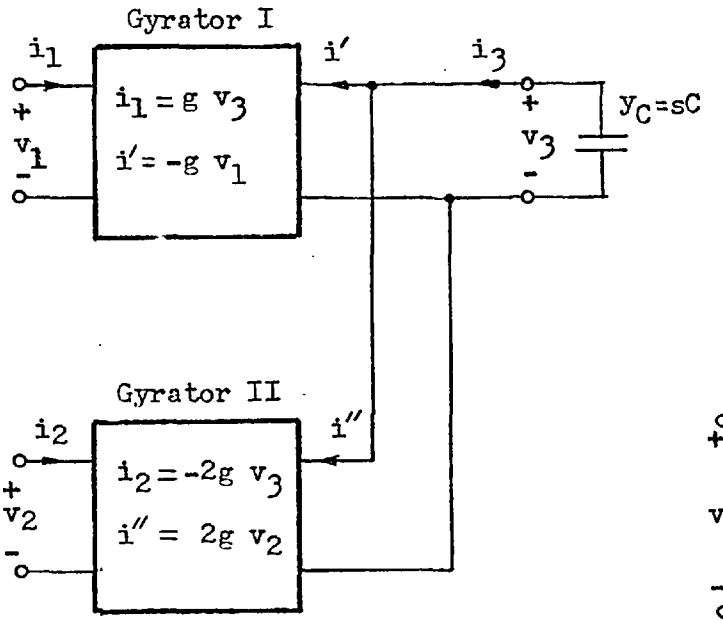
matrices H_{12} and H_{21} are square (n = k) and non-singular; otherwise det H = 0 (this follows from the expansion of the determinant using minors of order n or k, whichever is smaller). This conditions is also sufficient, since, as can be easily verified, H^{-1} has the form required by (4-7).

In a similar way it can be proved that an admittance inverter is simultaneously an impedance inverter if and only if G_{12} and G_{21} in (4-6) are square (n = k) and non-singular.

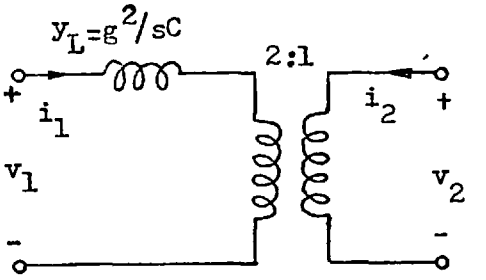
Since for 2-ports n = k = 1 and the submatrices in (4-5) and (4-6) become scalars, the conditions for simultaneous admittance and impedance conversion or inversion are automatically satisfied. In the case of multiports these conditions are not always satisfied; for instance, in a multiport with an odd number of ports, admittance and impedance conversion (or inversion) can never take place simultaneously since it is impossible to have the ports separated into two sets containing the same number of ports.

The fact that, in contrast to 2-ports, a multiport admittance converter (or inverter) may not be simultaneously an impedance converter (or inverter) will now be illustrated by means of a simple example using 3-port inverters. If two 2-port gyrators are connected as shown in Fig. 4-2a, a 3-port admittance inverter is obtained, as can be recognized from its matrix description. It could be used, when terminated by a capacitor, to simulate a network consisting of an inductor and an ideal transformer (Fig. 4-2a). This 3-port is not an impedance inverter since equation (4-4) is not satisfied (when port 3 is terminated by a 1-port, the resulting 2-port does not even have an impedance description). However, the same 2-port gyrators could be connected as shown in Fig. 4-2b in order to produce a 3-port impedance

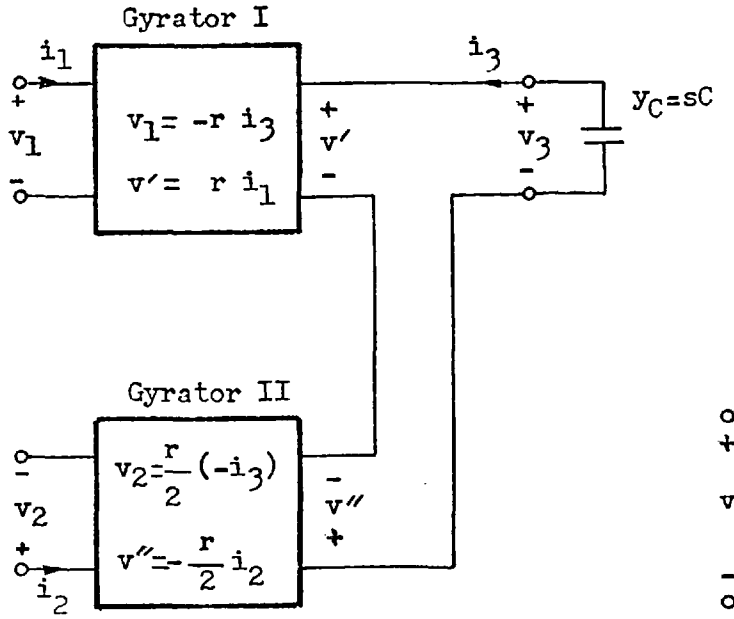
(a) 3-PORT ADMITTANCE INVERTER



$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & g \\ 0 & 0 & -2g \\ -g & 2g & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$



(b) 3-PORT IMPEDANCE INVERTER



$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & -r \\ 0 & 0 & -r/2 \\ r & r/2 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix}$$

Note: $r = g^{-1}$

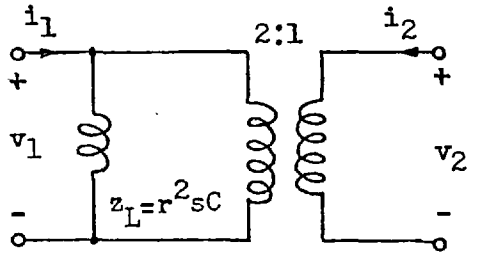


Fig. 4-2 : Example showing the difference between admittance and impedance inverters.

inverter. This 3-port could be used, when terminated by a capacitor, to simulate the inductor-transformer network shown in Fig. 4-2b.

It should be emphasised that the designation admittance converter (or inverter) is always used in this chapter to refer to all multiports satisfying (4-1)(or (4-2));it does not refer exclusively to those converters which are only of the admittance type (and not of the impedance type). A similar remark applies to the designation impedance converter (or inverter).

4.5 - SOME PROPERTIES OF MULTIPORT CONVERTERS AND INVERTERS

From the definitions and matrix descriptions in Table 4-1 it is possible to obtain several properties of multiport converters and inverters. Some of these properties will now be discussed.

Interchange of Input and Output

The definitions of multiport converters and inverters require a partition of the ports into two sets: a set of n ports labelled "input" and a set of k ports labelled "output". When the load multiport is connected at the output the result of the operations of conversion or inversion is observed at the input. The consequences of interchanging the input and output sets of ports (denoted by subscripts 1 and 2, respectively) will now be examined.

An admittance converter is described by equation (4-5),

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & \alpha H_{12} \\ -\frac{1}{\alpha} H_{21} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

which can also be written as

$$\begin{bmatrix} V_2 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{\alpha} H_{21} \\ \alpha H_{12} & 0 \end{bmatrix} \begin{bmatrix} I_2 \\ V_1 \end{bmatrix}$$

This equation, apart from an interchange of subscripts 1 and 2, has the form of (4-7) which describes an impedance converter. This shows that if the input and output sets of ports (denoted by subscripts 1 and 2, respectively) of an admittance converter are interchanged, the resulting multiport is an impedance converter; in other words, if conversion of the admittance type is possible in one direction, then conversion of the impedance type is possible in the other direction (in those converters which are of both types simultaneously the two operations are possible in both directions).

An admittance inverter is described by (4-6),

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & \alpha G_{12} \\ -\frac{1}{\alpha} G_{21} & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

and this can be written as

$$\begin{bmatrix} I_2 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{\alpha} G_{21} \\ \alpha G_{12} & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ V_1 \end{bmatrix}$$

This equation retains the form of (4-6) but subscripts 1 and 2 are interchanged. A similar result is obtained for the impedance inverter described by (4-8). This means that for inverters the interchange of input and output is not accompanied by a change of type: an inverter is of the admittance, or impedance, type in both directions.

Duality

As pointed out before, every equation involving the port variables of the admittance converter and inverter has a corresponding equation which applies to the impedance converter and inverter, respectively. These corresponding equations have the same form, but voltages and currents are interchanged. It can therefore be stated that the dual of a multiport admittance converter (or inverter) is an impedance converter (or inverter).

Interreciprocity

The description of the multiports which are interreciprocal (transpose or adjoint) of multiport converters and inverters can be found by applying the interreciprocity conditions (chapter 2, section 2.5) to the matrices in (4-5) to (4-8). By doing this, it can be shown that the interreciprocal of a converter or inverter is itself a converter or inverter, respectively, of the same type (admittance or impedance). This property, in conjunction with the interreciprocity theorem, can be used to derive new realizations of converters or inverters from existing ones.

4.6 - MULTIPORT TRANSFORMERS AND GYRATORS

If an admittance or impedance converter is non-reactive (the elements in the matrices are real constants) and described by a skew-symmetric hybrid matrix, then it is non-energic, i.e. the instantaneous power flowing into it is always zero. This is easily verified by substitution of (4-5) or (4-7) in the expression of the instantaneous power

$$P = I_1^t(t)V_1(t) + I_2^t(t)V_2(t)$$

The matrix description (4-5) of the non-energic admittance converter takes the form of

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & H_{12} \\ -H_{12}^t & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

and, similarly, for the non-energic impedance converter, (4-7) becomes

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 0 & K_{12} \\ -K_{12}^t & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Both the admittance and the impedance converter, may be called, in this special case, ideal multiport transformers. According to the discussion in the previous section, if a multiport ideal transformer is of the admittance type in one direction it will be of the impedance type in the other direction.

Similarly it can be shown that non-reactive admittance and impedance inverters are non-energic if described by skew-symmetric admittance or impedance matrices, respectively. In both cases it seems natural to use the designation multiport gyrator for these special inverters. There are thus two types of multiport gyrator: admittance multiport gyrator and impedance multiport gyrator. It is only when $n = k$ and G_{12} is non-singular that the multiport gyrator is simultaneously an admittance and an impedance gyrator. The 'multi-terminal gyrator', presented in [38, 39] is a multiport gyrator of the admittance type; it will be of both types simultaneously if these conditions are satisfied.

It may be interesting to note that the 3-port circulator [6] is not a multiport gyrator according to this definition, although it might be regarded, in some respects, as a multiport version of the gyrator: it is non-energic, is described by a skew-symmetric matrix, either admittance or impedance (but not both), and a 2-port gyrator is obtained if one of the ports is short or open-circuited. However, unlike the multiport gyrator considered above, it is not an inverter as can easily be seen by considering a 3-port circulator with an admittance description

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 0 & g & -g \\ -g & 0 & g \\ g & -g & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

which clearly cannot be written in the form of (4-6).

4.7 - FLOATING INDUCTOR SIMULATION

It has been seen in chapter 3 (section 3.2) that a floating inductor, when simulated by an active RC circuit has three terminals (including the ground terminal) and can therefore be described as a 2-port (Fig. 4-3a), with an admittance matrix

$$Y = \frac{1}{sL}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \qquad (4\text{-}22)$$

A floating inductor can be simulated by a 3-port admittance inverter terminated by a capacitor. Consider that the 3-port in Fig. 4-3b had an admittance description of the form

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & g_{13} \\ 0 & 0 & g_{23} \\ g_{31} & g_{32} & 0 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (4\text{-}23)$$

which corresponds to a 3-port admittance inverter with port 3 as the output port (as seen by comparison of (4-23) with (4-6)). It will be assumed that the 3-port in Fig. 4-3b is active R (contains only resistors and active components) and therefore the elements of the admittance matrix in (4-23) are real constants. If a capacitor is connected to port 3, $y_3 = sC$, the resulting 2-port (ports 1 and 2) will have an admittance matrix which can be obtained using (4-2):

$$Y = -\begin{bmatrix} g_{13} \\ g_{23} \end{bmatrix}\frac{1}{sC}\begin{bmatrix} g_{31} & g_{32} \end{bmatrix}$$

or

$$Y = -\frac{1}{sC}\begin{bmatrix} g_{13}\,g_{31} & g_{13}\,g_{32} \\ g_{23}\,g_{31} & g_{23}\,g_{32} \end{bmatrix} \qquad (4\text{-}24)$$

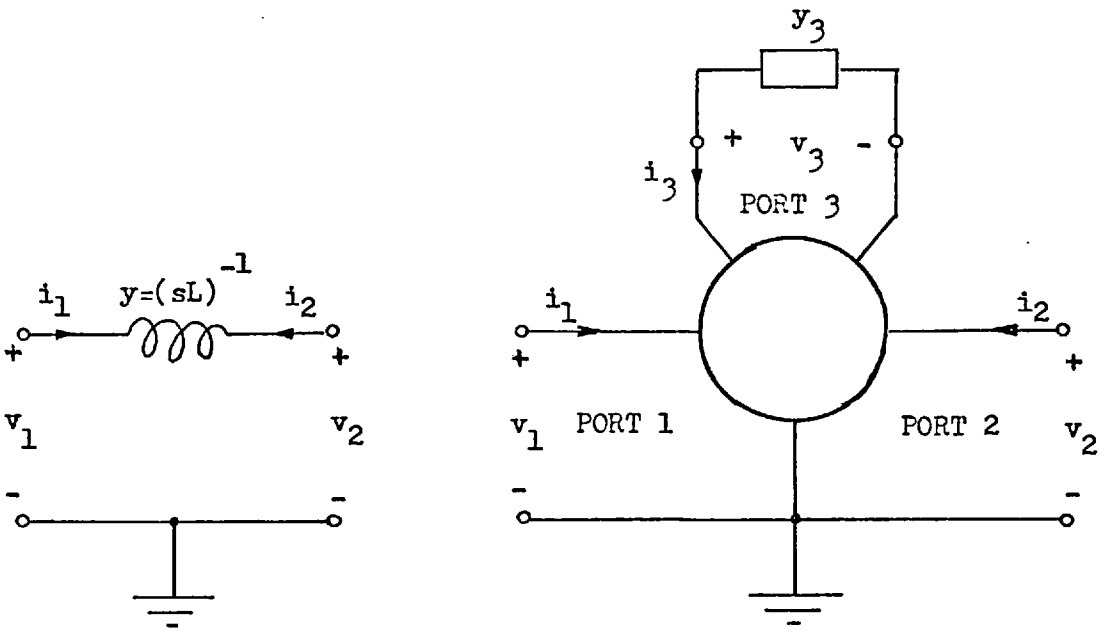


Fig. 4-3 : Floating inductor simulation.

This will be equal to the admittance matrix of a floating inductor (4-22) if and only if

$$g_{13} = -g_{23} = \overset{+}{-} g_a \qquad (g_a > 0) \tag{4-25a}$$

$$g_{31} = -g_{32} = \overset{-}{+} g_b \qquad (g_b > 0) \tag{4-25b}$$

where $\overset{+}{-} g_a$ is introduced here to denote the common value of g_{13} and $-g_{23}$, and $\overset{-}{+} g_b$ to denote the common value of g_{31} and $-g_{32}$. Substitution of (4-25) in (4-24) yields

$$Y = \frac{g_a\, g_b}{sC} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{4-26}$$

which corresponds to a floating inductor (4-22) with inductance

$$L = \frac{C}{g_a\, g_b} \tag{4-27}$$

Substituting (4-25) in (4-23) leads to

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \overset{+}{-} \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{4-28}$$

which is thus the description of a 3-port admittance inverter that will simulate a floating inductor when terminated by a capacitor.

A <u>3-port admittance converter</u> terminated by a resistor can also be used to simulate a floating inductor. The 3-port in Fig. 4-3b will be an admittance inverter with port 3 as the output port if it is described by

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_{13} \\ 0 & 0 & h_{23} \\ h_{31} & h_{32} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} \tag{4-29}$$

which is in the form of (4-5). The admittance matrix of the 2-port

obtained by termination of port 3 by a resistor, $y_3 = g$, is (from (4-1)):

$$Y = - \begin{bmatrix} h_{13} \\ h_{23} \end{bmatrix} \quad g \begin{bmatrix} h_{31} & h_{32} \end{bmatrix}$$

$$Y = -g \begin{bmatrix} h_{13} h_{31} & h_{13} h_{32} \\ h_{23} h_{31} & h_{23} h_{32} \end{bmatrix} \tag{4-30}$$

This admittance matrix will have the form of (4-22) if and only if

$$h_{13} = -h_{23} = h_a \tag{4-31a}$$

$$h_{31} = -h_{32} = -h_b \tag{4-31b}$$

where h_a and h_b are introduced simply to provide a convenient notation. Substitution of (4-31) in (4-30) leads to

$$Y = h_a h_b g \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{4-32}$$

If $h_a h_b = k s^{-1}$, where k is a positive real constant, then (4-32) represents the admittance of a floating inductor of inductance

$$L = (h_a h_b g s)^{-1} \tag{4-33}$$

Thus a floating inductor can be simulated by a 3-port admittance converter with the two input ports grounded (Fig. 4-3b), terminated by a resistor, if its description is of the form

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_a \\ 0 & 0 & -h_a \\ -h_b & h_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} \tag{4-34}$$

where

$$h_a h_b = k s^{-1} \tag{4-35}$$

and k is a positive real constant.

These 3-port admittance inverters and converters suitable for floating inductance simulation will be studied in greater detail later in this thesis. It will then be seen that almost all the circuits that have been proposed for the simulation of floating inductors can be interpreted as terminated inverters or converters.

It may be noted that the simulation of floating negative resistors or capacitors can be obtained using 3-port admittance converters or inverters terminated by a (positive) resistor or capacitor. These 3-port converters or inverters will have a matrix description in a form very similar to the description of the converters or inverters for floating inductance simulation. For instance, a converter described by (4-34) with

$$h_a\, h_b = -k \qquad (4\text{-}36)$$

where k is a positive real constant will simulate a floating negative resistor when terminated by a resistor at port 3, as shown by (4-32). A circuit that can be interpreted as such a converter was proposed in [73].

The 3-port admittance converters or inverters for floating inductor simulation cannot be simultaneously impedance converters or inverters since the total number of ports ($n + k = 3$) is odd. Since many circuits used for the simulation of grounded inductors are 2-port converters or inverters, it seems very natural to find that, as already mentioned, most of the circuits used for floating inductor simulation are 3-port converters or inverters. It would have been impossible to describe these circuits as multiport converters or inverters if the demand for simultaneous admittance and impedance conversion or inversion had been incorporated in the definitions.

4.8 - HYBRID CONVERTERS

The conversion and inversion discussed so far are operations performed by a multiport N on the admittance or impedance matrix of a load multiport N_2 (Fig. 4-1). The fact that N_2 can have other types of matrix description(e.g. hybrid, transmission, scattering) suggests the possibility of considering other types of conversion or inversion. Of these, only 'hybrid conversion' will be considered here since it will be shown that it includes, as special cases, admittance and impedance conversion and inversion, which are the main concern of this chapter. It will be shown that hybrid inverters are only a particular type of hybrid converter and therefore need not be considered separately.

The hybrid converter will be defined with reference to Fig. 4-1. It is convenient to use the notation appropriate for dealing with hybrid descriptions that was introduced before (chapter 2, section 2.1). E_1 denotes an n-vector whose components are some currents and some voltages chosen among the n currents and n voltages at the input ports of N in such a way that one variable (voltage or current) of each port is included. The n remaining port-variables, form another vector F_1 in which they are arranged with the port subscripts in the same order used in E_1 (for example: $E_1 = [i_1\ i_2\ v_3\ i_4\ v_5]^t$; $F_1 = [v_1\ v_2\ i_3\ v_4\ i_5]^t$). E_2 and F_2 are two k-vectors formed in a similar way from the k currents and k voltages at the output of N. It is assumed that the n-port resulting from the cascade-load connection of N and N_2 has a hybrid description

$$E_1 = H_1\ F_1 \tag{4-37}$$

and that N_2 has a hybrid description

$$\Delta\ E_2 = -H_2\ \Delta\ F_2 \tag{4-38}$$

where Δ is a diagonal matrix of dimension k such that the main diagonal elements are 1 if, in ΔE_2, they operate on voltages, and -1 if they operate on currents (for example, if $E_2 = [v_1\ v_2\ i_3\ i_4]^t$ then $\Delta = \text{diag.}\ (1, 1, -1, -1)$). The need for the use of Δ in (4-38) results from the choice of the reference directions of the voltages and currents in E_2 and F_2 in the usual way with respect to N and not with respect to N_2. The (n + k)-port N is a Hybrid Converter if, for any H_2,

$$H_1 = Q_{12}\ H_2\ Q_{21} \tag{4-39}$$

Since the inverse of a hybrid matrix is itself a hybrid matrix (corresponding to an interchange of dependent and independent variables) it is not necessary to consider hybrid inverters ($H_1 = P_{12}\ H_2^{-1}\ P_{21}$): these are a special case of hybrid converters.

Taking into account that $\Delta\Delta = 1$, equations (4-38) and (4-39) can be written in the form

$$E_2 = -(\ \Delta\ H_2\ \Delta\ )\ F_2 \tag{4-40}$$

$$H_1 = Q_{12}\ \Delta\ (\ \Delta\ H_2\ \Delta\ )\ \Delta\ Q_{21} \tag{4-41}$$

The matrix description that N must have in order to be a hybrid converter can very simply be obtained by noting that equations (4-37), (4-40) and (4-41) have the same form as the equations for the admittance converter: $I_1 = Y_1\ V_1$, $I_2 = -Y_2\ V_2$, and $Y_1 = H_{12}\ Y_2\ H_{21}$. Therefore the result expressed by equation (4-5) for the admittance converter shows that the hybrid converter must have a description of the form

$$\begin{bmatrix} E_1 \\ F_2 \end{bmatrix} = \begin{bmatrix} 0 & \alpha Q_{12} \Delta \\ -\frac{1}{\alpha} \Delta Q_{21} & 0 \end{bmatrix} \begin{bmatrix} F_1 \\ E_2 \end{bmatrix} \tag{4-42}$$

It is easy to see that the admittance and impedance converters and inverters discussed before are in fact special cases of hybrid converters

if the admittance and impedance description are regarded as hybrid descriptions where all the dependent variables are of one type (all currents or all voltages) and all the independent variables are of the other type. The admittance converter corresponds to the choice of variables $E_1 = I_1$, $E_2 = I_2$ (and consequently $F_1 = V_1$, $F_2 = V_2$) and the impedance converter corresponds to $E_1 = V_1$ and $E_2 = V_2$. For the admittance inverter $E_1 = I_1$, $E_2 = V_2$ and it can be regarded as an impedance-to-admittance converter. Similarly the impedance inverter is interpreted as an admittance-to-impedance converter.

It should be noted that these are limiting cases in the sense that the vector variables considered do not contain mixed voltages and currents. A 'true' hybrid converter could be, for example, one for which $E_1 = [i_1\ i_2\ v_3]^t$ and $E_2 = [v_4\ i_5]^t$. It is also possible that only one of the matrices H_1 and H_2 is a 'true' hybrid matrix: if $E_1 = [i_1\ i_2]^t$ and $E_2 = [i_3\ v_4]^t$ the hybrid converter is a 'hybrid-to-admittance' converter. The converters in these two examples do not have a 2-port counterpart since 2-port converters (and inverters) operate on a load 1-port for which a hybrid description has no meaning.

4.9 - CONCLUSIONS

The present chapter was concerned with the generalization of the concepts of imittance conversion and inversion from 2-ports to multiports. According to the generalization proposed here, admittance and impedance conversion and inversion, which are 'scalar' operations when performed by 2-ports, become 'matrix' operations when performed by multiports. One consequence of this is a distinction, which does not exist for 2-ports, between multiport admittance and impedance

converters (or inverters).

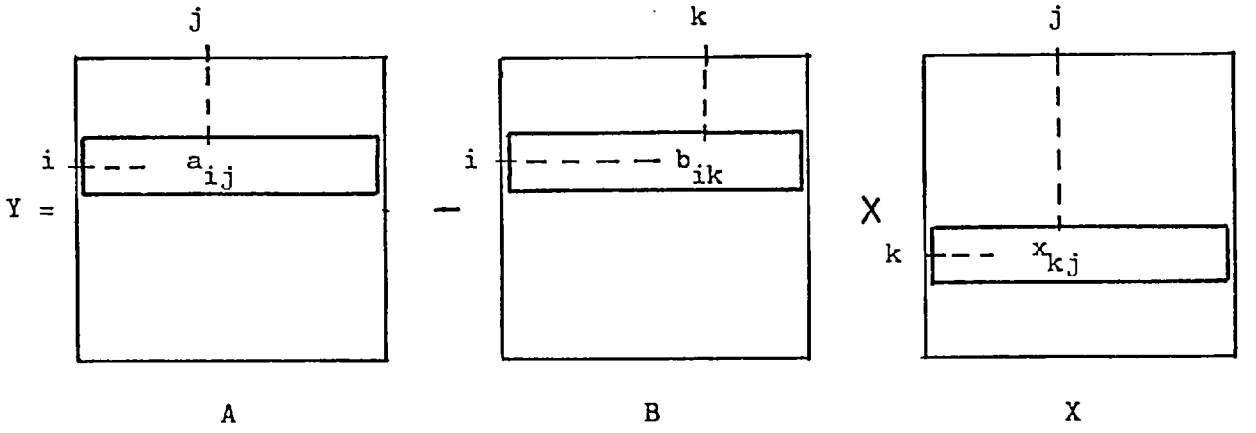
Most of the circuits that can be used for the simulation of floating inductors have been associated, in a somewhat intuitive way, with immittance inversion or conversion. In terms of the definitions proposed here these circuits can be formally described as 3-port admittance (not impedance) inverters or converters. Multiport transformers and gyrators are also special cases of multiport converters and inverters. The theory of general multiport converters and inverters proposed here provides a better understanding of these important special cases. It is believed that it is also useful as a contribution to general multiport theory.

It has also been shown in this chapter that admittance and impedance converters and inverters can be regarded as special cases of a more general concept, that of "hybrid converter". Other types of multiport converters, e.g. scattering converters, could be studied following the approach that was taken here.

APPENDIX

Lemma I. In $Y = A - BX$, where X and Y are square matrices and $B \neq O$, X can always be chosen such that Y is singular.

Proof: If $B \neq O$ it has at least one entry $b_{ik} \neq O$. If X is chosen such that all rows are O except row k and x_{kj} satisfies $a_{ij} - b_{ik} x_{kj} = O$ for all values of j, then row i in Y is a zero row-vector and hence Y is singular.



Lemma II. If $AXB = CXD \neq O$ for any X, then $A = \alpha C$ and $B = \frac{1}{\alpha} D$ where α is an arbitrary non-zero scalar.

Proof: If X is chosen such that only one entry is non-zero, $x_{ij} = 1$, then $a_{pi} b_{jk} = c_{pi} d_{jk}$. This result is true for all possible combinations of the values of the subscripts p, i, j and k. This means that $A b_{jk} = C d_{jk}$ for all j and k and hence $A = \alpha C$ ($\alpha = d_{jk}/b_{jk}$) and $B = \frac{1}{\alpha} D$.

CHAPTER 5

REALIZATION OF MULTIPORT CONVERTERS AND INVERTERS USING 2-PORT CONVERTERS AND INVERTERS

5.1 - INTRODUCTION

The formal theory of multiport converters and inverters has been presented in the previous chapter without any reference to the realization of these multiports. In the present chapter it will be shown that multiport converters or inverters can be realized by a suitable interconnection of 2-port converters or inverters, respectively. The problem of synthesising multiport converters and inverters can thus be reduced to the synthesis of the appropriate 2-port converters and inverters.

The realization using 2-port converters and inverters is straightforward and creates the possibility of using the vast amount of knowledge about the realization and performance of these 2-ports. There are however, limitations resulting from the fact that the 2-port behaviour of the converters and inverters is not necessarily guaranteed after the interconnection. Active realization requires a common ground terminal for all the 2-ports and this further restricts the configurations that can be used. These restrictions will be discussed in some detail. A number of particular configurations using 2-port converters and inverters having a grounded terminal common to both ports will be considered (these 2-port converters and inverters with a grounded terminal common to both ports are referred to, in this

thesis, by the simplified designations 'grounded converters' and 'grounded inverters').

All the realizations of multiport converters and inverters considered in this chapter are obtained from a general configuration which realizes any well-defined multiport as an interconnection of 2-ports. This configuration will be derived, in a straightforward way, from the description of a general well-defined multiport.

The realizations of multiport converters and inverters are based on the matrix descriptions that were obtained in the previous chapter and are shown there in Table 4-1. It will be assumed throughout the present chapter that the scalar α, appearing in the matrix descriptions in Table 4-1, is

$$\alpha = 1$$

since this does not affect the generality of the results obtained.

In view of the complexity of many of the diagrams considered in this chapter it has been found convenient to introduce a simplified representation. It is believed that this representation leads to diagrams which are easier to interpret. This simplified representation will be introduced in the next section.

5.2 - A SIMPLIFIED REPRESENTATION OF THE INTERCONNECTION OF MULTIPORTS

The present chapter is essentially concerned with the realization of certain multiports as an interconnection of 2-ports where it is assumed that the port behaviour is always maintained. For this situation, the usual circuit representation, in which a port is represented as a pair of terminals, is unnecessarily cumbersome and can be simplified, since it is assumed that the current flowing into one terminal is always equal to the current flowing out of the other

terminal. A simplified representation which will be extensively used in this chapter will now be introduced (this representation will not, however, be used in other chapters of the thesis).

The basic conventions associated with the simplified representation are the following:

(a) A line represents a pair of wires. The voltage between the two wires is written above or on the left-hand side of the line. The current, assumed as having the same value and opposite directions in the two wires is written below or on the right hand side of the line.

(b) A multiport is represented by a box. One of the matrices describing the multiport is given inside the box. The independent variables associated with the matrix inside the box are always shown at each port; the dependent variables, when shown, are enclosed in brackets.

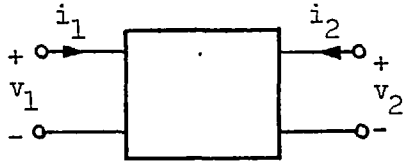
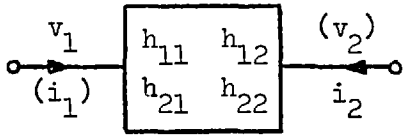
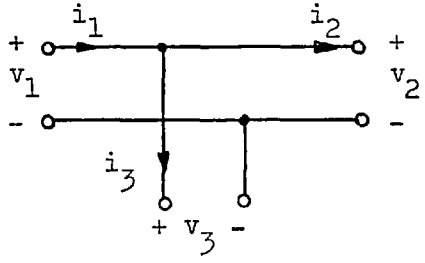
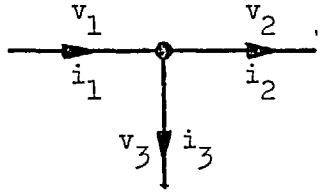
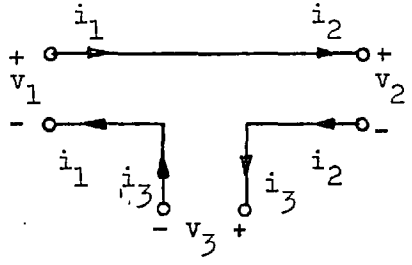
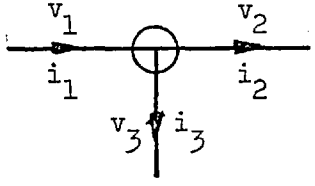
(c) Arrows may be used to denote the reference direction for the flow of energy.

(d) A dot, • , represents a parallel junction, where three ports are connected in parallel. A circle, o , represents a series junction, where three ports are connected in series.

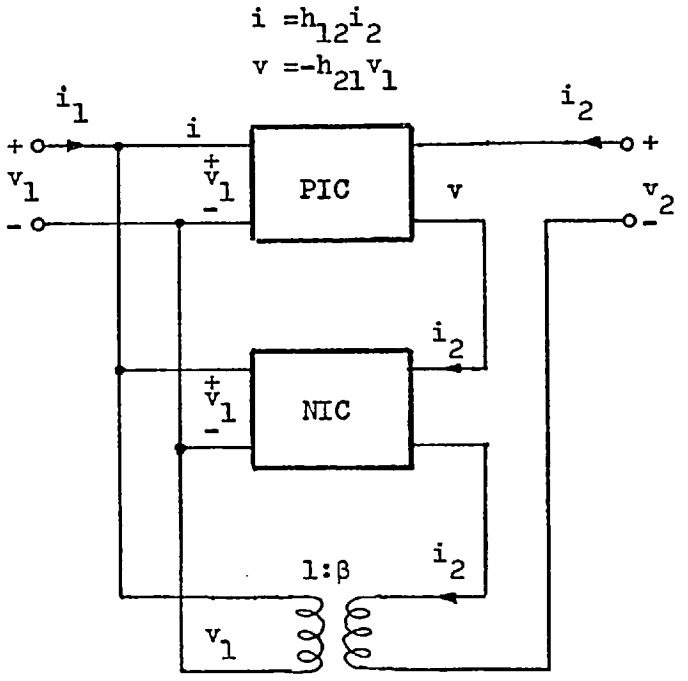
These conventions are summarized in Table 5-1. An example, showing the same network with the usual representation and with the simplified representation, is given in Fig. 5-1.

The representation of two or more wires by one line and the use of parallel junctions are very common in power systems diagrams. It may also be mentioned that the use of one line and parallel and series junctions are basic features of the 'bond graph' notation [74] with which the simplified representation used here has some similarity.

TABLE 5-1 : Simplified representation of the interconnection of multiports.

	USUAL REPRESENTATION	SIMPLIFIED REPRESENTATION	EQUATIONS
2-PORT			$\begin{bmatrix} i_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}$
PARALLEL JUNCTION			$v_1 = v_2 = v_3$ $i_1 = i_2 + i_3$
SERIES JUNCTION			$i_1 = i_2 = i_3$ $v_1 = v_2 + v_3$

(a) Usual representation



(b) Simplified representation

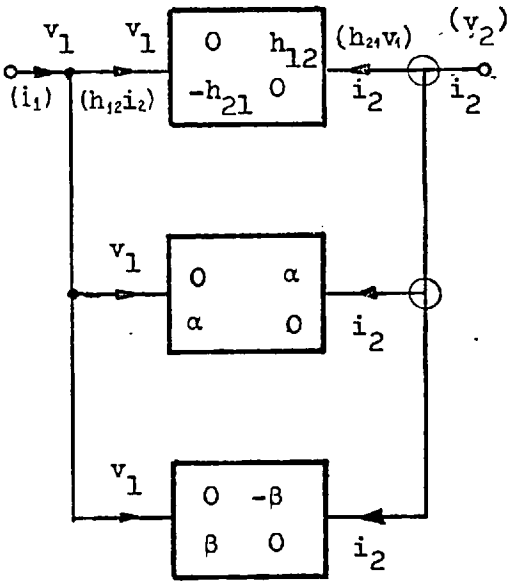


Fig. 5.1 : Example of the simplified representation.

It should be emphasized that the simplified representation leads to power-flow diagrams which must not be confused with signal-flow diagrams, such as the block-diagrams used, for instance, to represent control systems. In a power-flow diagram two variables, the product of which represents power (current and voltage in the present case), are associated with each line; in a signal-flow diagram a single information-carrying quantity is associated with each line. As a consequence, in the simplified representation, a box representing a 2-port is associated with four parameters, whereas a block in a signal-flow diagram represents a single transmission operator.

5.3 - REALIZATION OF WELL-DEFINED MULTIPORTS USING 2-PORTS

It was mentioned in chapter 2 (section 2.1) that a multiport is said to be well-defined if it has at least one type of hybrid description, the admittance and impedance descriptions being regarded as particular types of hybrid descriptions. It will now be shown how any hybrid matrix can be realized by an interconnection of 2-ports.

A multiport described by an admittance matrix can be realized by an interconnection of 2-ports as shown in Fig. 5-2, where the simplified representation described in the previous section has been used. Having in mind the meaning of the parallel junction (see Table 5-1) it is easy to see that the set of 2-ports interconnected as shown in Fig. 5-2 will have the admittance description given in the same figure. In a similar way it can be seen that a multiport with an impedance description can be realized as shown in Fig. 5-3 (the meaning of the series junctions used in this figure is explained in Table 5-1).

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} & y_{13} & \cdots & y_{1n} \\ y_{21} & y_{22} & y_{23} & \cdots & y_{2n} \\ y_{31} & y_{32} & y_{33} & \cdots & y_{3n} \\ \vdots & & & & \\ y_{n1} & y_{n2} & y_{n3} & \cdots & y_{nn} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \vdots \\ v_n \end{bmatrix}$$

$$y_{11} = \sum_{1}^{n} (y_{11})_i \qquad y_{22} = \sum_{1}^{n} (y_{22})_i \qquad y_{33} = \sum_{1}^{n} (y_{33})_i \qquad \vdots \qquad y_{nn} = \sum_{1}^{n} (y_{nn})_i$$

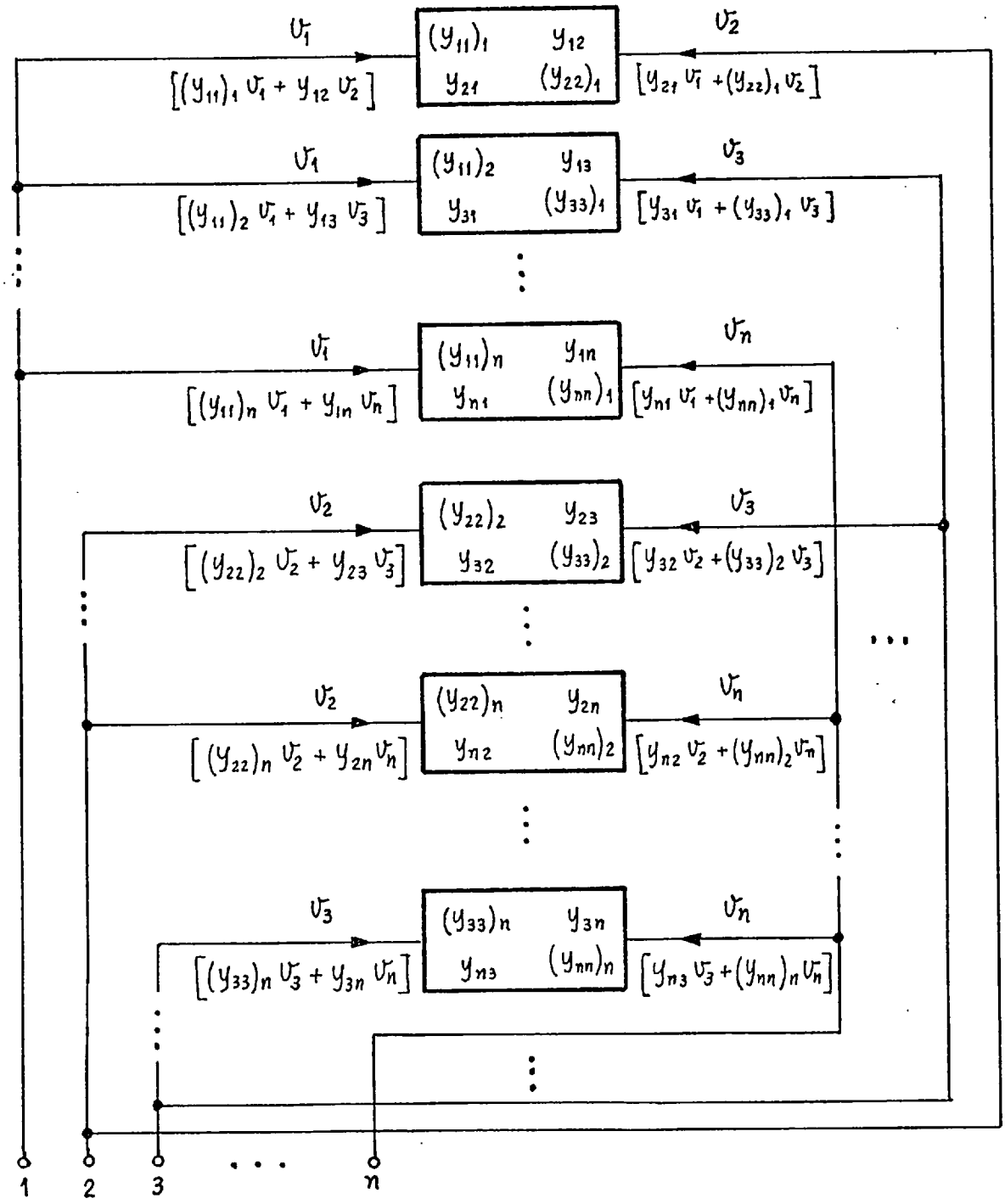


Fig. 5-2 : Realization of a multiport with an admittance description.

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} & z_{13} & \dots & z_{1n} \\ z_{21} & z_{22} & z_{23} & \dots & z_{2n} \\ z_{31} & z_{32} & z_{33} & \dots & z_{3n} \\ \vdots & & & & \\ z_{n1} & z_{n2} & z_{n3} & \dots & z_{nn} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ \vdots \\ i_n \end{bmatrix}$$

$$z_{11} = \sum_{i=1}^{n} (z_{11})_i$$
$$z_{22} = \sum_{i=1}^{n} (z_{22})_i$$
$$z_{33} = \sum_{i=1}^{n} (z_{33})_i$$
$$\vdots$$
$$z_{nn} = \sum_{i=1}^{n} (z_{nn})_i$$

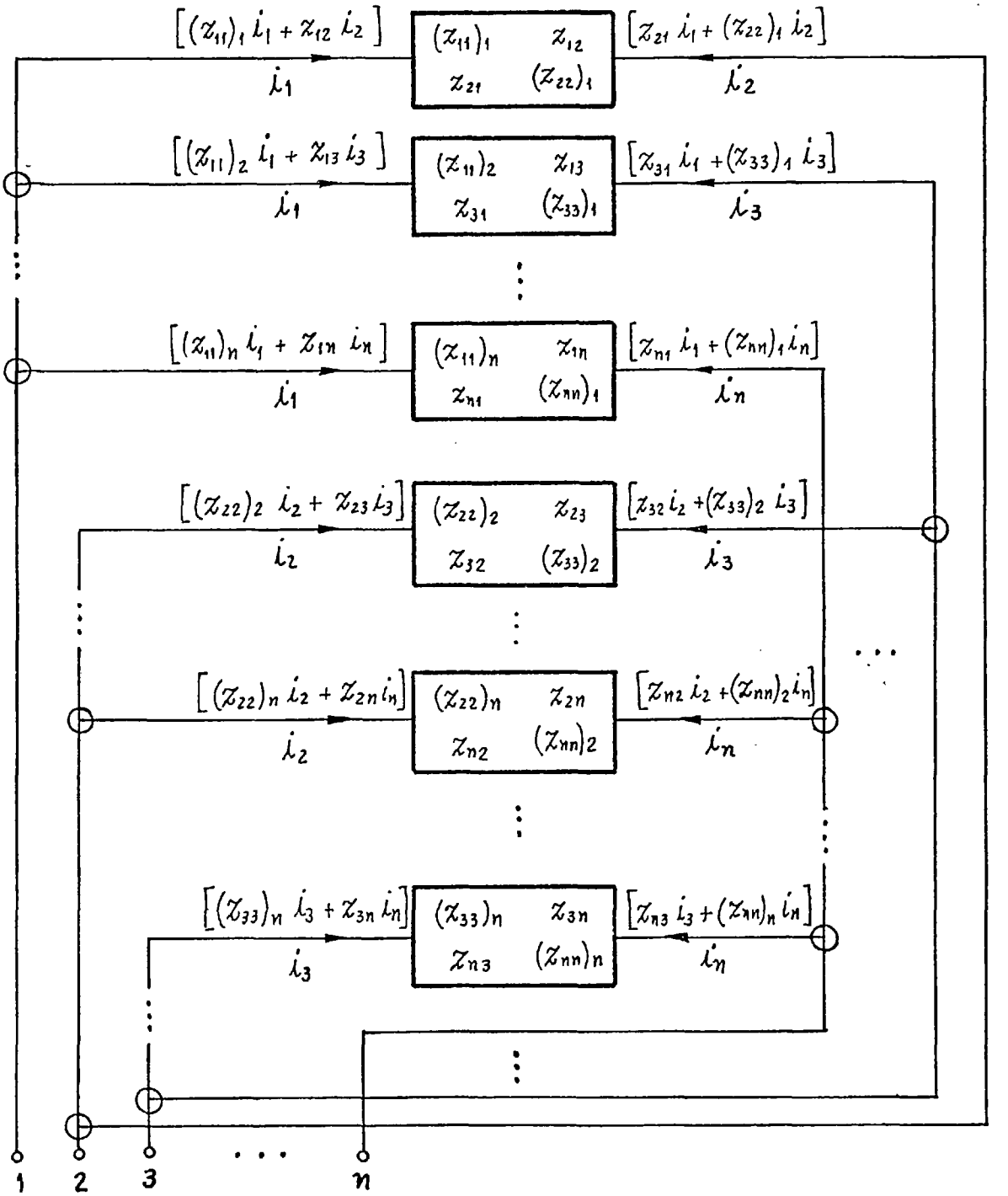


Fig. 5-3 : Realization of a multiport with an impedance description.

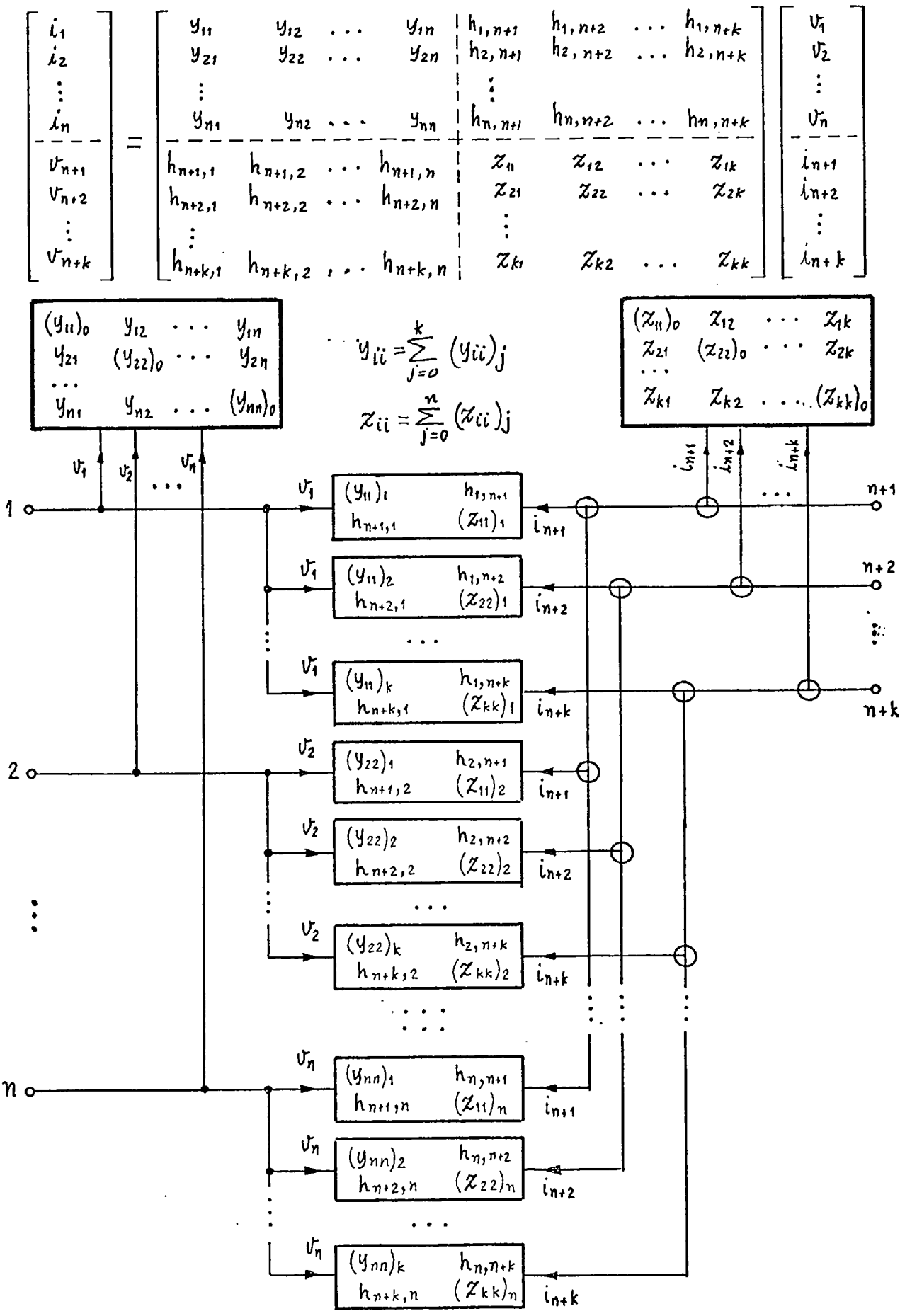


Fig. 5-4 : Realization of a multiport with a hybrid description.

A multiport with a general hybrid description can be realized as shown in Fig. 5-4. In this figure the n-port described by an admittance matrix can be realized as shown in Fig. 5-2 and the k-port described by an impedance matrix can be realized as shown in Fig. 5-3.

In all three cases (Figs. 5-2, 5-3 and 5-4) the number of 2-ports required is the number of off-diagonal elements in the matrix to one side of the diagonal. In order to realize an m-port, the number of 2-ports required is therefore

$$\tfrac{1}{2}\, m \quad (m - 1)$$

A smaller number of 2-ports may be required if the matrix contains pairs of zeros placed symmetrically with respect to the main diagonal.

It may be noted that the main-diagonal elements of an m-port matrix are the sum of the main-diagonal elements in m of the 2-ports (Figs. 5-2, 3, 4). This means that all but m 2-ports can be chosen with zero main-diagonal elements and will therefore be 2-port converters or inverters. Even those 2-ports with non-zero main-diagonal elements can be replaced by 2-port converters or inverters with 1-ports connected in parallel or in series with the ports, as shown in Fig. 5-5.

It is important to mention that the realizations given here require that for all the 2-ports the port constraints be maintained after the interconnection, so that the 2-port description applies. If this were not assumed, it would not even have been possible to use the simplified representation. It must not be forgotten that a port is a terminal pair where the current flowing into one terminal equals the current flowing out of the other; consequently the 2-port description is only a partial description of a 4-terminal network.

Although the port constraints in the 2-ports are not always guaranteed after the interconnection, there are cases where they are satisfied. One such case is when the port constraints are a consequence

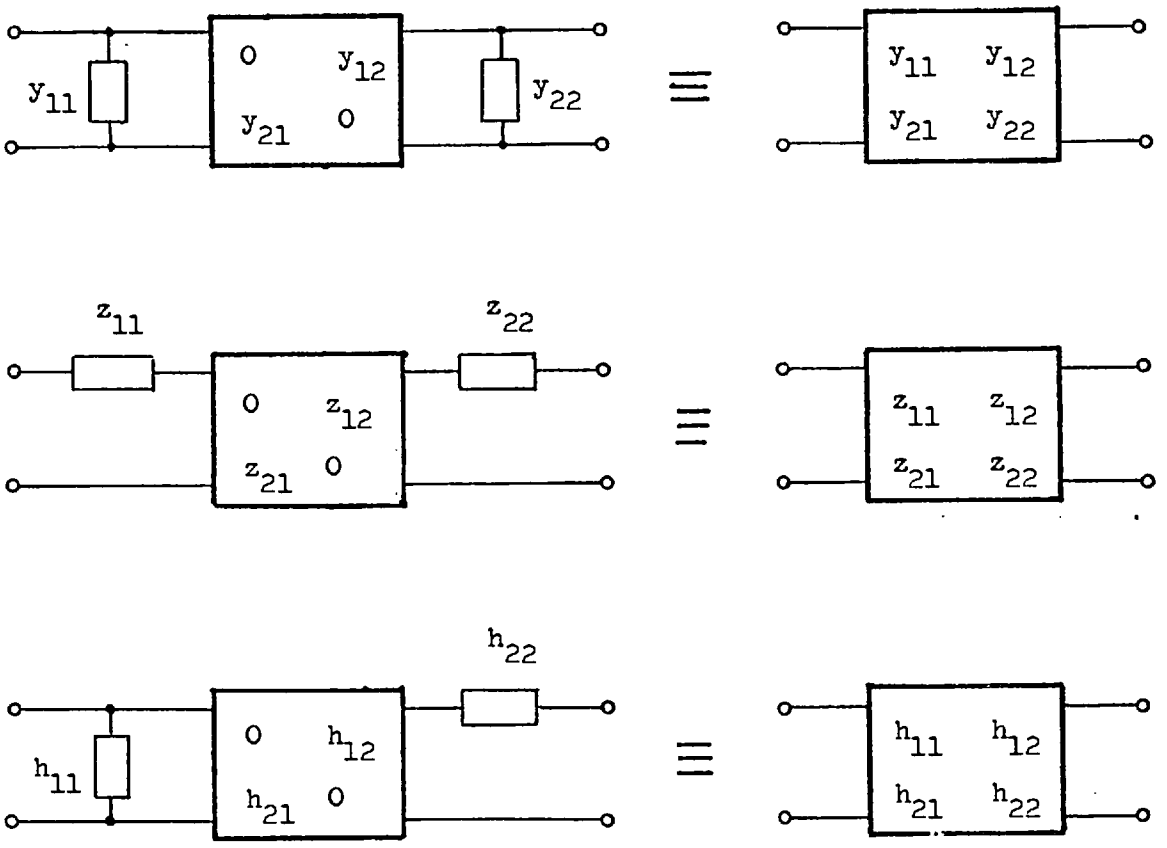


Fig. 5-5 : Realization of 2-ports using converters and inverters.

of the internal structure of the 2-ports, for instance when 'isolating' transformers are used cascaded with the ports. Another situation in which the port constraints are satisfied corresponds to the special case where *each* of the ports of every 2-port coincides, on its own, with one port of the final multiport.

If the 2-ports are actively realized, they will usually have to share a common ground terminal. This is an additional factor to be taken into account when verifying if the port constraints are maintained, since, in general, a 2-port with a ground terminal is in fact a 5-terminal network. It may be noted, however that the realization of a multiport with admittance description (Fig. 5-2) is always possible, in the general case, using grounded 2-ports (i.e. 2-ports with a grounded terminal common to both ports). Several special cases of multiports with impedance or hybrid descriptions can also be realized using grounded 2-ports (without resorting to the use of transformers). Some of these special cases will be considered in connection with the realization of multiport converters and inverters.

5.4 - REALIZATION OF MULTIPORT CONVERTERS AND INVERTERS

It was shown in the previous chapter (section 4.5) that multiport converters have the following property: an admittance converter becomes an impedance converter if the sets of input and output ports are interchanged. This means that it is not necessary to consider separately the realization of admittance and impedance converters, since a realization of an admittance converter is also a realization of an impedance converter.

Multiport inverters are, in this respect, in a different situation, since a change of type does not accompany an interchange of input and

output: the multiport resulting from the interchange of the input and the output of an admittance inverter, is also an admittance inverter and, similarly, the multiport resulting from the interchange of the input and the output of an impedance inverter is also an impedance inverter. Therefore the realization of admittance inverters has to be considered separately from that of impedance inverters.

The configurations considered in the previous section will now be particularized for the case of multiport converters and inverters. Multiport converters can be realized using solely 2-port converters connected as shown in Fig. 5-6, which is a special case of Fig. 5-4. Admittance inverters can be realized as shown in Fig. 5-7, which is a special case of Fig. 5-2, and impedance inverters as shown in Fig. 5-8 which is a special case of Fig. 5-3. Although the configurations of Figs. 5-7 and 5-8 are different, 2-port inverters are used in both cases.

It can be seen from Figs. 5-6, 5-7 and 5-8 that an (n + k)-port converter or inverter requires, in general, (n.k) 2-port converters or inverters.

It should be noted that all the comments made, in the previous section, concerning the need for the port constraints to be maintained, apply to the realizations of multiport converters and inverters considered here. If microelectronic realization of multiport converters and inverters is envisaged, the use of isolating transformers is ruled out and actively-realized 2-ports with a common ground terminal have to be considered. By using grounded 2-port inverters (inverters with both ports grounded) it is possible to realize any multiport admittance inverter (i.e. with any number of ports and without restrictions on the value of the elements in the matrix). Also several particular types of converters and of impedance inverters can be realized using

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ \hline v_{n+1} \\ v_{n+2} \\ \vdots \\ v_{n+k} \end{bmatrix} = \begin{bmatrix} \multicolumn{3}{c:}{\multirow{3}{*}{0}} & h_{1,n+1} & h_{1,n+2} & \cdots & h_{1,n+k} \\ & & & h_{2,n+1} & h_{2,n+2} & \cdots & h_{2,n+k} \\ & & & \vdots & & & \\ \multicolumn{3}{c:}{} & h_{n,n+1} & h_{n,n+2} & \cdots & h_{n,n+k} \\ \hline h_{n+1,1} & h_{n+1,2} & \cdots & \multicolumn{4}{c}{\multirow{3}{*}{0}} \\ h_{n+2,1} & h_{n+2,2} & \cdots & h_{n+2,n} & & & \\ \vdots & & & & & & \\ h_{n+k,1} & h_{n+k,2} & \cdots & & & & \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ \hline i_{n+1} \\ i_{n+2} \\ \vdots \\ i_{n+k} \end{bmatrix}$$

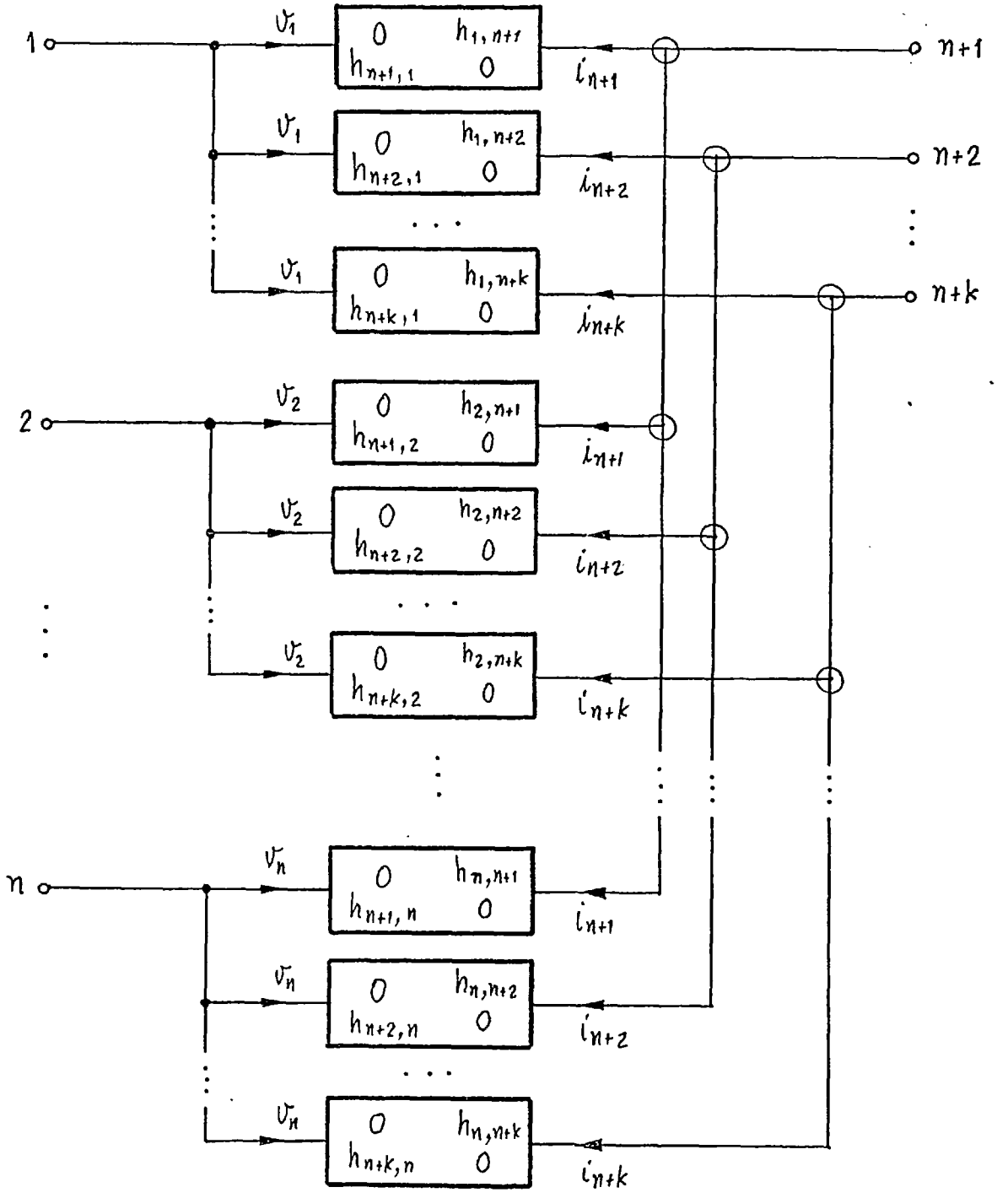


Fig. 5-6 : Multiport admittance or impedance converter.

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ \hline i_{n+1} \\ i_{n+2} \\ \vdots \\ i_{n+k} \end{bmatrix} = \left[\begin{array}{ccc|ccc} & & & y_{1,n+1} & y_{1,n+2} \cdots & y_{1,n+k} \\ & 0 & & y_{2,n+1} & y_{2,n+2} \cdots & y_{2,n+k} \\ & & & \vdots & & \\ & & & y_{n,n+1} & y_{n,n+2} \cdots & y_{n,n+k} \\ \hline y_{n+1,1} & y_{n+1,2} & \cdots y_{n+1,n} & & & \\ y_{n+2,1} & y_{n+2,2} & \cdots y_{n+2,n} & & 0 & \\ \vdots & & & & & \\ y_{n+k,1} & y_{n+k,2} & \cdots y_{n+k,n} & & & \end{array}\right] \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ \hline v_{n+1} \\ v_{n+2} \\ \vdots \\ v_{n+k} \end{bmatrix}$$

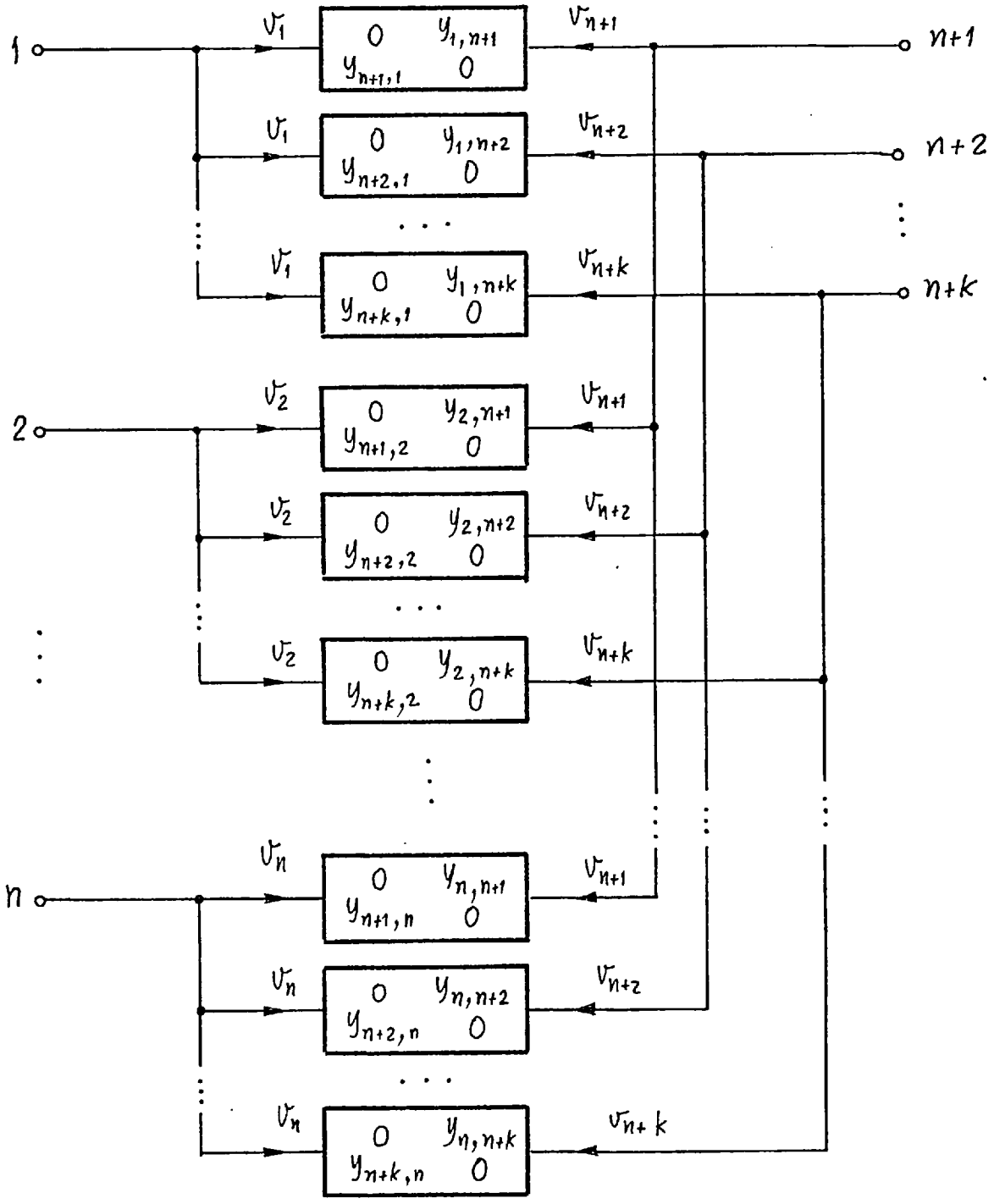


Fig. 5-7 : Multiport admittance inverter.

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ \hline v_{n+1} \\ v_{n+2} \\ \vdots \\ v_{n+k} \end{bmatrix} = \left[\begin{array}{ccc|ccc} & & & z_{1,n+1} & z_{1,n+2} & \cdots & z_{1,n+k} \\ & 0 & & z_{2,n+1} & z_{2,n+2} & \cdots & z_{2,n+k} \\ & & & \vdots & & & \\ & & & z_{n,n+1} & z_{n,n+2} & \cdots & z_{n,n+k} \\ \hline z_{n+1,1} & z_{n+1,2} & \cdots & z_{n+1,n} & & & \\ z_{n+2,1} & z_{n+2,2} & \cdots & z_{n+2,n} & & 0 & \\ \vdots & & & & & & \\ z_{n+k,1} & z_{n+k,2} & \cdots & z_{n+k,n} & & & \end{array}\right] \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ \hline i_{n+1} \\ i_{n+2} \\ \vdots \\ i_{n+k} \end{bmatrix}$$

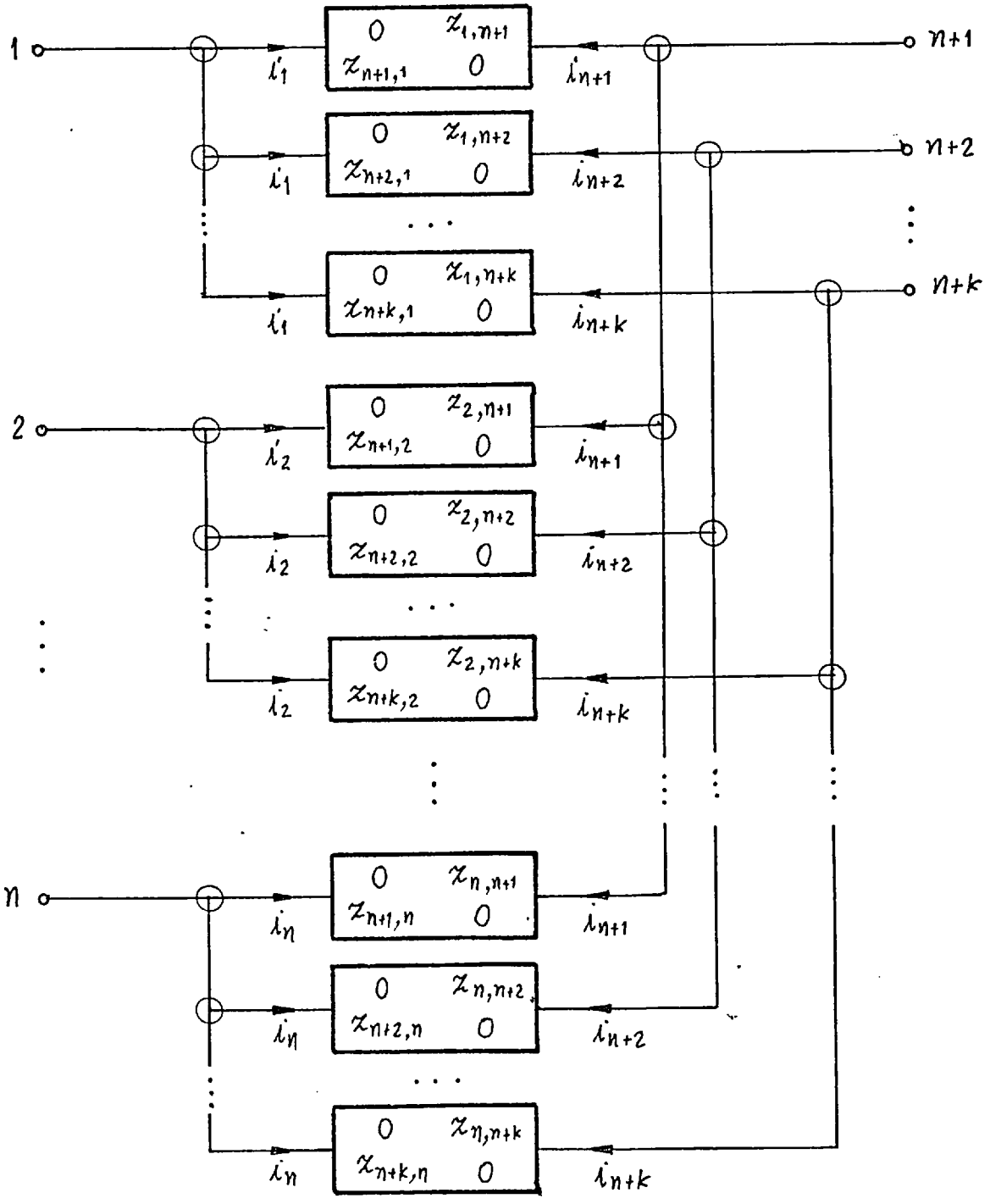


Fig. 5-8 : Multiport impedance inverter.

grounded 2-port converters and inverters, respectively. This will be considered in the next section.

5.5 - MULTIPORT CONVERTERS AND INVERTERS USING GROUNDED 2-PORT CONVERTERS AND INVERTERS

This section deals with the realization of multiport converters and inverters using 2-port converters and inverters with both ports grounded. Two-ports with only one port grounded or without any port grounded (but with a ground terminal) can be used only in very degenerate cases which will not be discussed here.

The admittance inverter is the only type of multiport converter or inverter which can be realized, with grounded 2-ports, in its most general form (without additional precautions such as the use of isolating transformers). By stating that the admittance inverter can be realized in its most general form, it is meant that the number of ports and the value of the non-zero elements in the admittance matrix are not restricted in any way. The multiport admittance inverter is therefore of particular interest concerning microelectronic realization, where the use of isolating transformers is ruled out.

The realization of the general admittance inverter is shown in Fig. 5-9 where the usual representation (as opposed to the simplified representation used in previous sections) is employed.

It may be observed that a special case of the realization in Fig. 5- 9 is the circuit for the simulation of floating inductors using two grounded inverters (usually gyrators) [67]. This circuit was discussed before (chapter 3, Fig. 3-20) and is reproduced here as Fig. 5-10.

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ \hline i_{n+1} \\ i_{n+2} \\ \vdots \\ i_{n+k} \end{bmatrix} = \left[\begin{array}{ccc|ccc} & & & y_{1,n+1} & y_{1,n+2} \cdots & y_{1,n+k} \\ & 0 & & y_{2,n+1} & y_{2,n+2} \cdots & y_{2,n+k} \\ & & & \vdots & & \\ & & & y_{n,n+1} & y_{n,n+2} \cdots & y_{n,n+k} \\ \hline y_{n+1,1} & y_{n+1,2} \cdots & y_{n+1,n} & & & \\ y_{n+2,1} & y_{n+2,2} \cdots & y_{n+2,n} & & 0 & \\ \vdots & & & & & \\ y_{n+k,1} & y_{n+k,2} \cdots & y_{n+k,n} & & & \end{array}\right] \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ \hline v_{n+1} \\ v_{n+2} \\ \vdots \\ v_{n+k} \end{bmatrix}$$

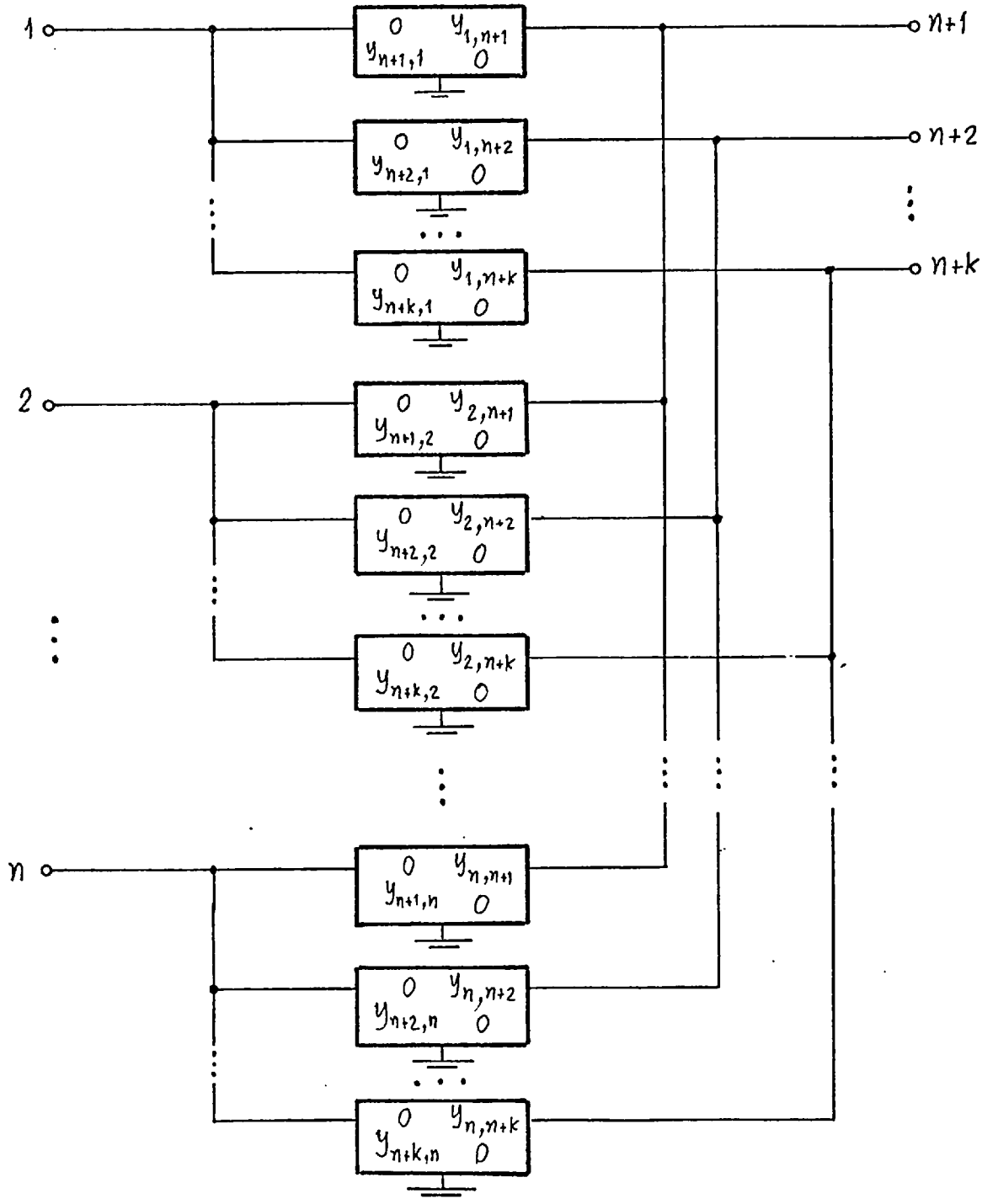
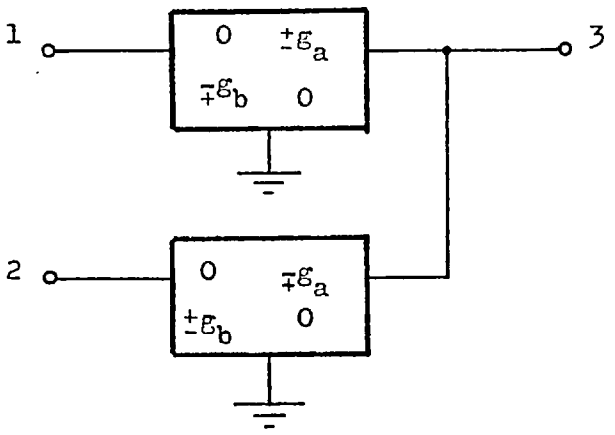


Fig. 5-9 : Admittance inverter using grounded 2-port inverters.



$g_a > 0 \qquad g_b > 0$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{matrix} + \\ - \end{matrix} \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

Fig. 5-10 : Three-port admittance inverter for floating inductor simulation.

The realization of admittance or impedance converters using grounded 2-port converters is possible only in special cases, some of which are shown in Fig. 5-11.

It may be noted that the "multi-PIC" network [37], which can be used for the simulation of inductor-networks has the configuration given in Fig. 5-11a. Special cases of the realization in Fig. 5-11c are the circuits with two grounded converters used for the simulation of floating inductors [37,68] and for the simulation of floating negative resistors [73]. These circuits were considered before (chapter 3, Fig. 3-21) and their configuration is reproduced here in Fig. 5-12.

Also in the case of multiport impedance inverters only some special types can be realized with grounded 2-port inverters. Some of these types are shown in Fig. 5-13.

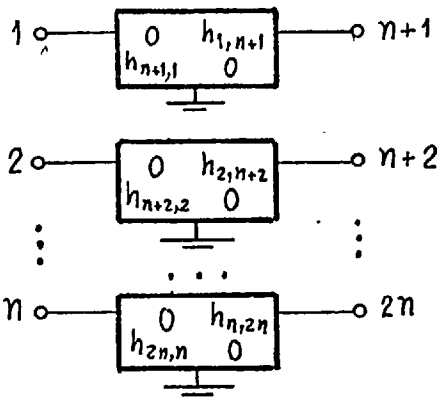
All the configurations considered in this section are potentially suitable for microelectronic realization, since the 2-ports used have a common ground terminal and since 2-port behaviour is guaranteed without any need for isolating transformers.

5.6 - CONCLUSIONS

In this chapter it is shown how any well-defined multiport can be realized using 2-ports. This method is then applied to the realization of multiport converters and inverters using only 2-port converters or inverters, respectively.

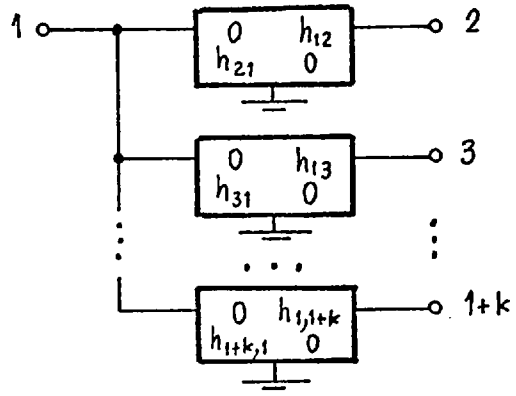
The need to ensure 2-port behaviour of the interconnected converters or inverters, and the requirement that all 2-ports share a common ground terminal, restricts the number of configurations that can be used without appropriate precautions (e.g. use of transformers to

(a)



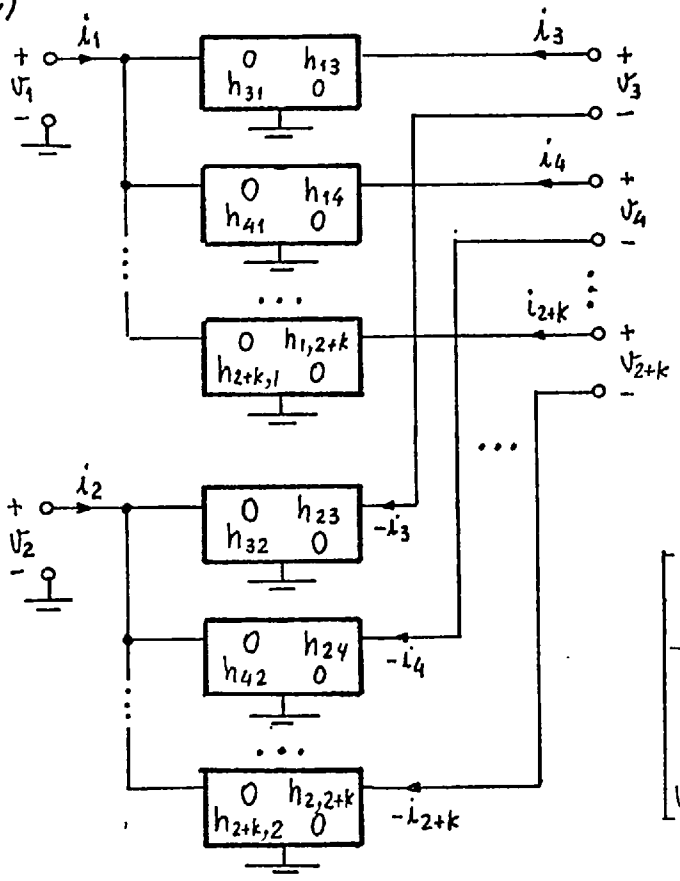
$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \\ \hline v_{n+1} \\ v_{n+2} \\ \vdots \\ v_{2n} \end{bmatrix} = \left[\begin{array}{ccc|ccc} & 0 & & h_{1,n+1} & 0 \cdots & 0 \\ & & & 0 & h_{2,n+2} \cdots & 0 \\ & & & \vdots & & \\ & & & 0 & 0 \cdots & h_{n,2n} \\ \hline h_{n+1,1} & 0 & \cdots 0 & & & \\ 0 & h_{n+2,2} & \cdots 0 & & 0 & \\ \vdots & & & & & \\ 0 & 0 & \cdots h_{2n,n} & & & \end{array}\right] \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ \hline i_{n+1} \\ i_{n+2} \\ \vdots \\ i_{2n} \end{bmatrix}$$

(b)



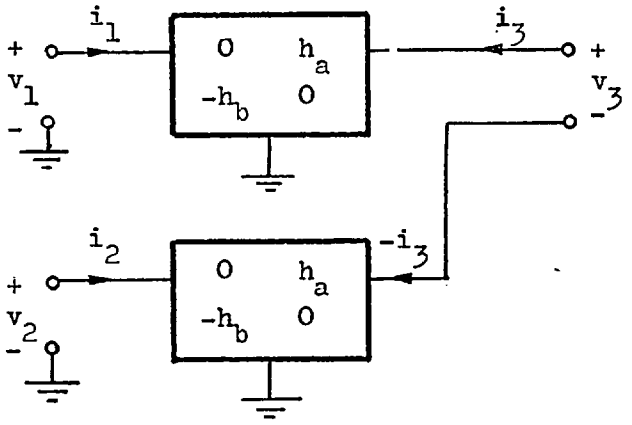
$$\begin{bmatrix} i_1 \\ \hline v_2 \\ v_3 \\ \vdots \\ v_{1+k} \end{bmatrix} = \left[\begin{array}{c|ccc} 0 & h_{12} & h_{13} \cdots & h_{1,1+k} \\ h_{21} & & & \\ h_{31} & & 0 & \\ \vdots & & & \\ h_{1+k,1} & & & \end{array}\right] \begin{bmatrix} v_1 \\ \hline i_2 \\ i_3 \\ \vdots \\ i_{1+k} \end{bmatrix}$$

(c)



$$\begin{bmatrix} i_1 \\ i_2 \\ \hline v_3 \\ v_4 \\ \vdots \\ v_{2+k} \end{bmatrix} = \left[\begin{array}{cc|ccc} & 0 & & h_{13} & h_{14} \cdots h_{1,2+k} \\ & & & -h_{23} & -h_{24} \cdots -h_{2,2+k} \\ \hline h_{31} & -h_{32} & & & \\ h_{41} & -h_{42} & & 0 & \\ \vdots & \vdots & & & \\ h_{2+k,1} & -h_{2+k,2} & & & \end{array}\right] \begin{bmatrix} v_1 \\ v_2 \\ \hline i_3 \\ i_4 \\ \vdots \\ i_{2+k} \end{bmatrix}$$

Fig. 5-11 : Some special cases of multiport converters using grounded 2-port converters.



$$h_a h_b = ks^{-1}$$

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_a \\ 0 & 0 & -h_a \\ -h_b & h_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix}$$

Fig. 5-12 : Three-port admittance converter for floating inductor simulation.

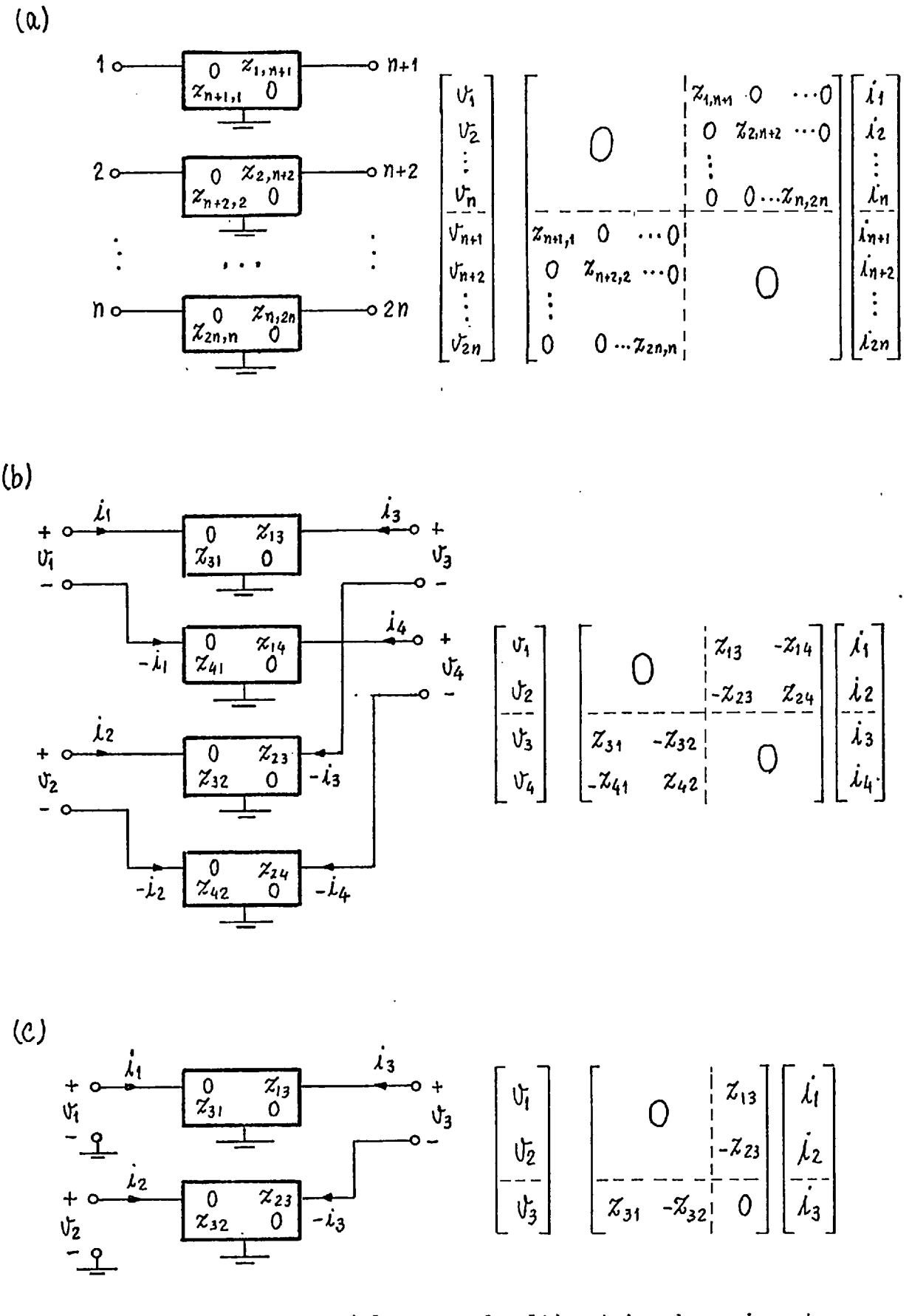


Fig. 5-13 : Some special cases of multiport impedance inverters using grounded 2-port inverters.

ensure port-behaviour). However, 2-port converters and inverters with both ports grounded can be used to realize the general multiport admittance inverter and several particular types of converters and impedance inverters.

The circuits for the simulation of floating inductors using two grounded inverters or two grounded converters are special cases of the realizations considered here (the same applies to the circuit for the simulation of floating negative resistors employing two grounded NIC's).

CHAPTER 6

A CLASSIFICATION OF 3-PORT INVERTERS AND CONVERTERS USED IN THE SIMULATION OF FLOATING INDUCTORS

6.1 - INTRODUCTION

When the simulation of grounded inductors was reviewed in chapter 3 (section 3.5) it was mentioned that most of the circuits that have been proposed in the literature are either 2-port inverters (usually gyrators) terminated by a capacitor, or 2-port converters terminated by a resistor. In some cases the same circuit can be considered either as an inverter or as a converter depending on whether a capacitor or a resistor is regarded as the termination. It has also been mentioned that not only lossy inductors but also lossless inductors can be simulated by circuits which cannot be interpreted as inverters or converters.

A similar situation is found in the case of the simulation of floating inductors. It was shown in chapter 4 (section 4.7) that a floating inductor can be simulated by a 3-port admittance inverter terminated by a capacitor or by a 3-port admittance converter terminated by a resistor. These 3-port inverters and converters are special cases of the multiport inverters and converters introduced in this thesis as a generalization of 2-port inverters and converters. Some circuits simulating a floating inductor can be interpreted either as a terminated inverter or as a terminated converter, depending on whether a capacitor or a resistor is considered as the termination (an example of this will be considered later in this chapter). It is

also possible to simulate a floating inductor by circuits which cannot be interpreted as inverters or converters. Examples of such circuits can be found in [75] and [76] (the circuits in [75] simulate a lossy inductor and the circuit in [76] simulates a lossless inductor). It should be emphasized, however, that the vast majority of circuits that have been proposed for the simulation of floating inductors are interpretable as terminated inverters or converters.

It will be assumed that the inverters used for floating inductor simulation (FIS) are realized as active R networks and are therefore described by a matrix whose elements are real constants. It was shown in chapter 4 that an inverter suitable for FIS must have a description of the form:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (6\text{-}1)$$

where g_a and g_b are positive real constants.

A converter that simulates an inductor when terminated by a resistor must contain at least one capacitor. It will therefore be an active RC network described by a matrix in which some elements are dependent on the complex frequency variable s and, as shown before (chapter 4), it must have a description of the form

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & h_a \\ 0 & 0 & -h_a \\ -h_b & h_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} \qquad (6\text{-}2)$$

where

$$h_a h_b = k s^{-1} \qquad (6\text{-}3)$$

and k is a positive real constant.

Although all inverters suitable for FIS have the same 3-port description, expressed by equation (6-1), they may have different terminal descriptions. Similarly, all converters for FIS must have the 3-port description (6-2) but different realizations may have different terminal descriptions. In this chapter a classification of 3-port inverters based on their terminal description will be established. A parellel classification will also be applied to the 3-port converters. According to this classification, circuits that belong to different classes are distinguishable by terminal measurements.

It is believed that the classification proposed here clarifies the relationships between the different realizations of inverters and converters that can be used for the realization of floating inductors. It will be made clear that whereas some realizations can be distinguished by external measurements, others cannot. It is shown that some circuits that are apparently unrelated, do in fact belong to the same class; it may be possible, if two circuits have the same terminal description, to derive one from the other. This possibility is applied to the derivation of several 3-port gyrators using three operational amplifiers from an initial circuit with two gyrators, each gyrator containing two amplifiers.

It should be noted that the inverters and converters considered here may have other applications besides their use in the simulation of floating inductors. Inverters with a description in the form of (6-1) can be used to synthesize constant resistance all-pass networks [77]. Converters described by (6-2) where

$$h_a h_b = -k \qquad (6\text{-}4)$$

and k is a positive real constant can be used to simulate floating

negative immittances [73].

6.2 - TERMINAL DESCRIPTION OF 3-PORT INVERTERS FOR FLOATING INDUCTOR SIMULATION

A 3-port admittance inverter that simulates a floating inductor when terminated by a capacitor has the general 5-terminal configuration shown in Fig. 6-1. The 3-port formed in the way indicated in Fig. 6-1 must have a description in the form of equation (6-1), i.e.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 - v_4 \end{bmatrix} \qquad (6\text{-}5)$$

where $i_3 = -i_4$ and the voltages are defined between each terminal and the ground terminal 0.

The 5-terminal network in Fig. 6-1 becomes a 3-port inverter described by (6-5) when the ports are formed as indicated in the figure. The form of the required terminal description will now be derived.

The most general description of a linear time-invariant and non-reactive 5-terminal network (terminals 0, 1, 2, 3, 4, with terminal 0 as reference) is:

$$\begin{bmatrix} m_{11} & m_{12} & m_{13} & m_{14} \\ m_{21} & m_{22} & m_{23} & m_{24} \\ m_{31} & m_{32} & m_{33} & m_{34} \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} p_{11} & p_{12} & p_{13} & p_{14} \\ p_{21} & p_{22} & p_{23} & p_{24} \\ p_{31} & p_{32} & p_{33} & p_{34} \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \qquad (6\text{-}6)$$

where all m_{ij} and all p_{ij} are real constants. If the 5-terminal

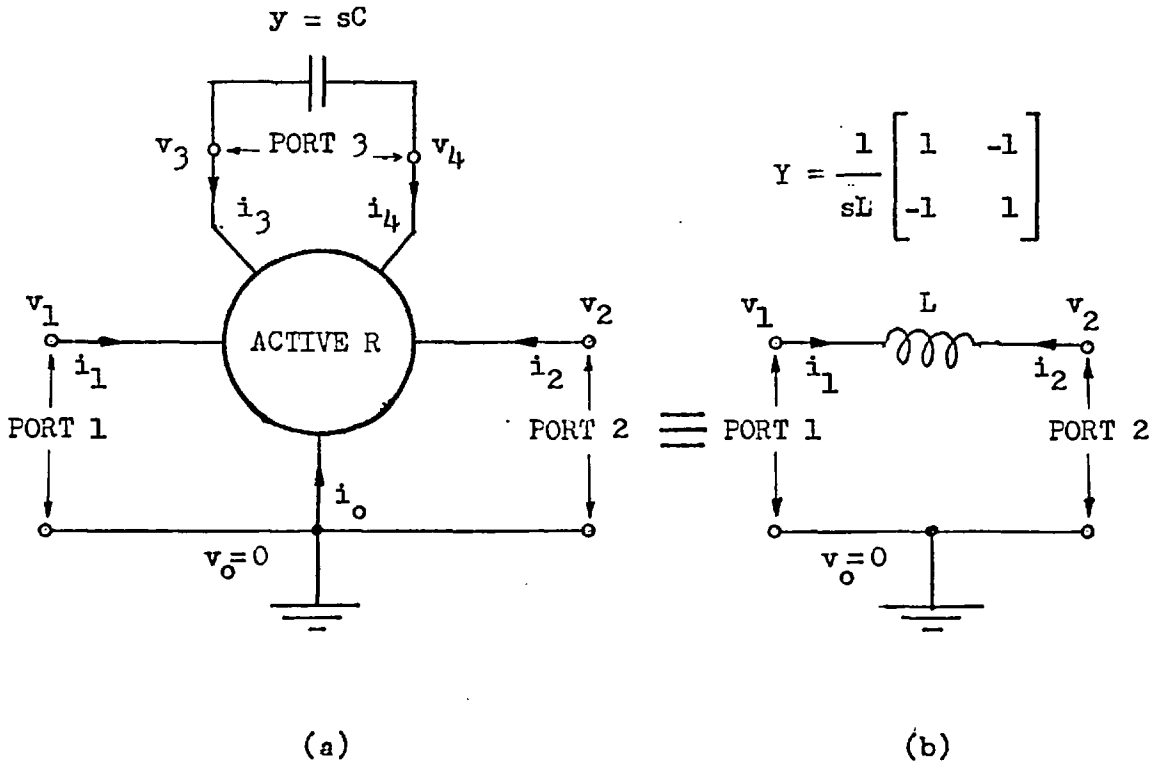


Fig. 6-1 : Floating inductor simulation by admittance inversion.

network is constrained to be a 3-port in accordance with Fig. 6-1, then

$$i_4 = -i_3 \tag{6-7}$$

With this constraint, (6-6) can be written in the form

$$\begin{bmatrix} m_{11} & m_{12} & (m_{13} - m_{14}) \\ m_{21} & m_{22} & (m_{23} - m_{24}) \\ m_{31} & m_{32} & (m_{33} - m_{34}) \\ m_{41} & m_{42} & (m_{43} - m_{44}) \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} + \begin{bmatrix} p_{11} & p_{12} & p_{13} & p_{14} \\ p_{21} & p_{22} & p_{23} & p_{24} \\ p_{31} & p_{32} & p_{33} & p_{34} \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \tag{6-8}$$

This matrix equation corresponds to four scalar equations. If the 3-port is to be a 3-port inverter described by (6-5), i.e.

$$\begin{aligned} i_1 &\mp g_a (v_3 - v_4) = 0 \\ i_2 &\pm g_a (v_3 - v_4) = 0 \\ i_3 &\pm g_b (v_1 - v_2) = 0 \end{aligned} \tag{6-9}$$

then these three equations must be obtainable from (6-8). It will be assumed that the first three equations in (6-8) have been reduced to the form of (6-9). It can be seen by comparison of (6-9) with (6-8) that (6-6) must be of the form

$$\begin{bmatrix} 1 & 0 & \alpha & \alpha \\ 0 & 1 & \delta & \delta \\ 0 & 0 & 1+\beta & \beta \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \mp \begin{bmatrix} 0 & 0 & g_a & -g_a \\ 0 & 0 & -g_a & g_a \\ -g_b & g_b & 0 & 0 \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \tag{6-10}$$

where α, β, δ, m_{4j} and p_{4j} $(j = 1, 2, 3, 4)$ are arbitrary real constants. The equations in (6-10) can be rearranged in the form

$$\begin{bmatrix} 1 & 0 & \alpha & \alpha \\ 0 & 0 & 1+\beta & \beta \\ 1 & 1 & \gamma & \gamma \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \mp \begin{bmatrix} 0 & 0 & g_a & -g_a \\ -g_b & g_b & 0 & 0 \\ 0 & 0 & 0 & 0 \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}11)$$

where the 3rd rows of the matrices in (6-11) are obtained by adding the 1st and 2nd rows of the matrices in (6-10), with $\gamma = \alpha + \delta$, and the 2nd rows of the matrices in (6-11) are the 3rd rows in (6-10).

The 5-terminal active R network in Fig. 6-1 must have a description in the form of (6-11). In equation (6-11) there are several arbitrary parameters. Each specific set of these parameters defines a specific 5-terminal network (but different sets do not necessarily denote different networks, as mentioned in 2.1). All such 5-terminal networks become the same 3-port inverter with the description given by (6-3). Some of these special cases, corresponding to different values of the arbitrary parameters in (6-11), are of particular practical and conceptual interest and will be discussed in the next sections. Three cases will be considered. The first two impose constraints on the terminal configuration of Fig. 6-1, whereas the third case imposes a constraint on the terminal currents:

Case 1: Terminal 4 (or 3) coincides with terminal 0.

Case 2: Terminal 4 (or 3) coincides with terminal 1 (or 2).

Case 3: The current i_o, entering the network through terminal 0 is zero.

For reasons which will become clear later, these cases will be discussed in the order 1, 3, 2. Realizations that do not fall into any of these special cases will also be discussed.

6.3 - FOUR-TERMINAL INVERTER

In this section, the special case where terminals 4 and 0 are coincident (Fig. 6-2) will be considered. It should be noted that the case where terminals 3 and 0 coincide differs from this only by a different numbering of the terminals.

In this case the basic 5-terminal becomes a 4-terminal network which, if a 3-port inverter with common terminal 0 is to be obtained, must have a terminal description which is identical with the 3-port description given by (6-1), i.e.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (6\text{-}12)$$

If the network in Fig. 6-2 is regarded as a 5-terminal network, then the equation

$$v_4 = 0$$

must be considered together with (6-12) leading to

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_4 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a & 0 \\ 0 & 0 & -g_a & 0 \\ -g_b & g_b & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ i_4 \end{bmatrix} \qquad (6\text{-}13)$$

This can also be written as

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \mp \begin{bmatrix} 0 & 0 & g_a & -g_a \\ -g_b & g_b & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \qquad (6\text{-}14)$$

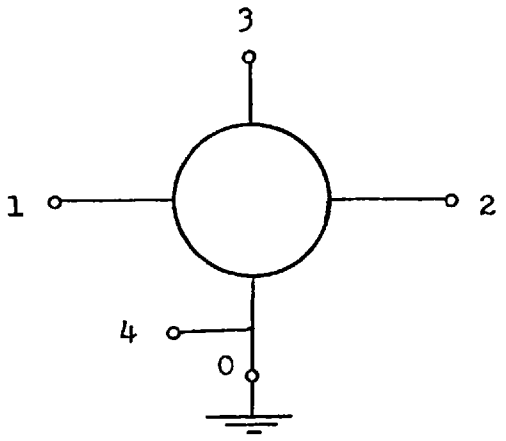
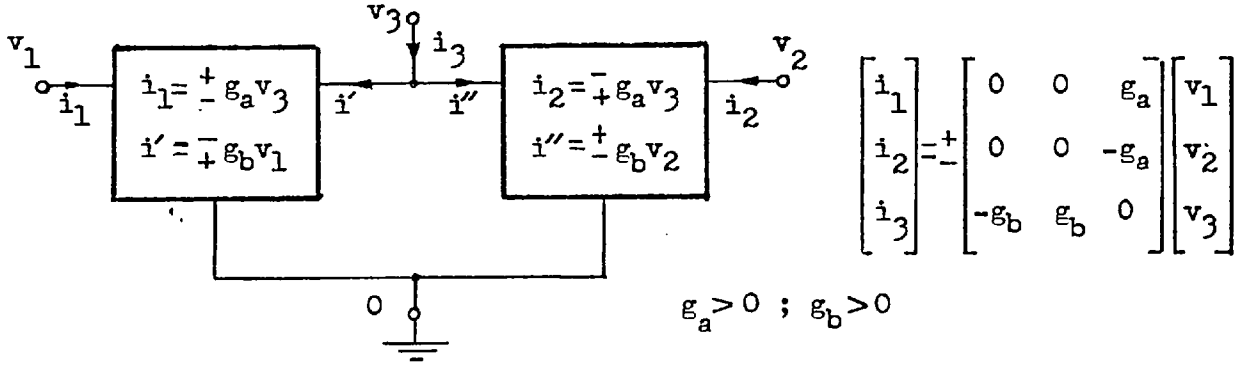


Fig. 6-2 : Special case of Fig. 6-1 where terminals 4 and 0 coincide (4-terminal inverter).



$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

Fig. 6-3 : Four-terminal inverter using two grounded inverters.

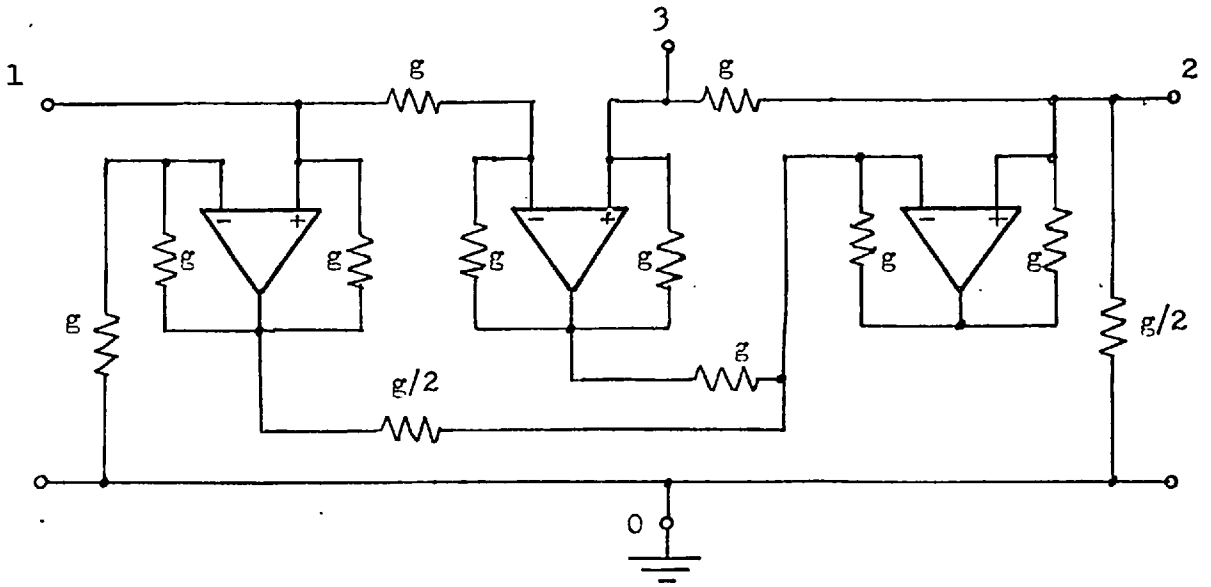


Fig. 6-4 : 4-terminal inverter with 3 operational amplifiers (Deboo's circuit).

It can be seen that (6-14) is a special case of (6-11). In this case there are no arbitrary parameters in the terminal description of the network. It is therefore impossible to distinguish between different circuits belonging to this special case (apart from the values of g_a and g_b). Since this realization of the 3-port inverter is a 4-terminal network it will be designated as a 4-terminal inverter.

Several of the circuits that have been proposed for the simulation of floating inductors are 4-terminal inverters. This is so in the case of the circuit proposed by Holt and Taylor [67] using two grounded inverters (usually gyrators); this circuit has been mentioned in previous chapters, and is reproduced here in Fig. 6-3. The circuit, using 3 operational amplifiers, published by Deboo [78] is also a 4-terminal inverter (Fig. 6-4). Likewise, the transistor circuits described in [79-82] are 4-terminal inverters. It may be noted that the designation 'semi-floating' gyrator has been used for some of these circuits (apparently in order to indicate that the capacitor is grounded but the simulated inductor is floating).

6.4 - FLOATING INVERTERS

The special case where in the 5-terminal network of Fig. 6-1

$$i_o = 0 \quad \text{or} \quad i_1 + i_2 + i_3 + i_4 = 0 \qquad (6\text{-}15)$$

will now be considered. Then the description of the 5-terminal network corresponds to (6-11) with

$$\gamma = 1$$

i.e.:

$$\begin{bmatrix} 1 & 0 & \alpha & \alpha \\ 0 & 0 & 1+\beta & \beta \\ 1 & 1 & 1 & 1 \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \mp \begin{bmatrix} 0 & 0 & g_a & -g_a \\ -g_b & g_b & 0 & 0 \\ 0 & 0 & 0 & 0 \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}16)$$

It is obvious that $\gamma = 1$ is sufficient to satisfy (6-15). To prove that $\gamma = 1$ is also necessary, assume that $\gamma \neq 1$. Then, in order to satisfy (6-15) it becomes necessary to choose the 4th rows of the matrices in (6-11) to be $[1\ 1\ 1\ 1]$ and $[0\ 0\ 0\ 0]$. If rows 3 and 4 are now interchanged a description is obtained which is a special case of (6-16).

The realizations of the 3-port inverter that belong to this special case will be designated as floating inverters. This designation is suggested by the fact that the 2-port formed by combining terminals 1 and 2 to obtain one port and terminals 3 and 4 to obtain the other port is an inverter which is 'floating' i.e., isolated from the ground terminal (in the sense that $i_o = 0$).

There are a number of obvious ways in which floating inverters can be realized:

(a) by using an ordinary 2-port inverter connected to a floating power supply, for example a battery, which is not connected to ground;

(b) by using, as in (a), an ordinary 2-port inverter but a grounded power supply and a "gyrator-floatation circuit" [83] which is inserted between inverter and power supply, simulating a high impedance;

(c) by using an ordinary 2-port inverter which contains, instead of conventional amplifiers with grounded output ports, special

amplifiers with floating output ports (and differential input ports) [84].

Two possible examples of floating inverters are shown in Fig. 6-6 in a nullator-norator representation. The circuit in Fig. 6-6a can be described by

$$i_1 = g\,(v_3 - v_4) \tag{6-17a}$$

$$-i_4 = -g\,(v_1 - v_2) \tag{6-17b}$$

$$i_1 + i_2 + i_3 + i_4 = 0 \tag{6-17c}$$

$$v_1 = v_4 \tag{6-17d}$$

and the circuit in Fig. 6-6b by

$$i_1 = g\,(v_3 - v_4) \tag{6-18a}$$

$$i_2 = -g\,(v_3 - v_4) \tag{6-18b}$$

$$i_3 = -g\,(v_1 - v_2) \tag{6-18c}$$

$$i_4 = g\,(v_1 - v_2) \tag{6-18d}$$

Equations (6-17), when written in matrix form are a special case of (6-16) and it is easy to see that (6-18) can be brought to a form which is also a special case of (6-16). However, whereas the circuit described by (6-18) has an admittance description, the circuit described by (6-17) does not have such a description, since equation (6-17d) involves voltages only and for the existence of an admittance description it is required that all voltages can be imposed independently. This shows that, although both circuits satisfy the same 3-port inverter matrix, with the same values for g_a and g_b, and belong to the same class of 3-port inverters as defined by (6-16), they can be distinguished by external terminal measurements. Thus the situation is different from that encountered in the case of the circuits in Figs. 6-3 and 6-4

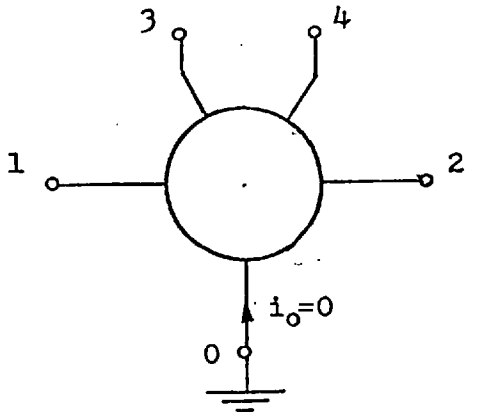
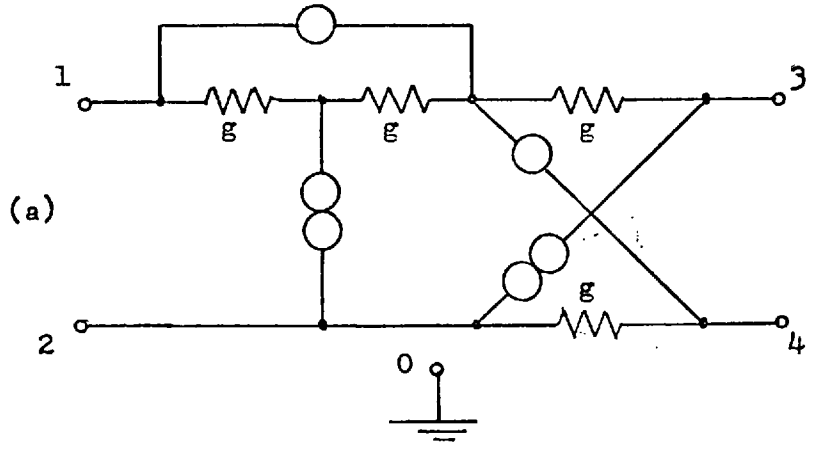
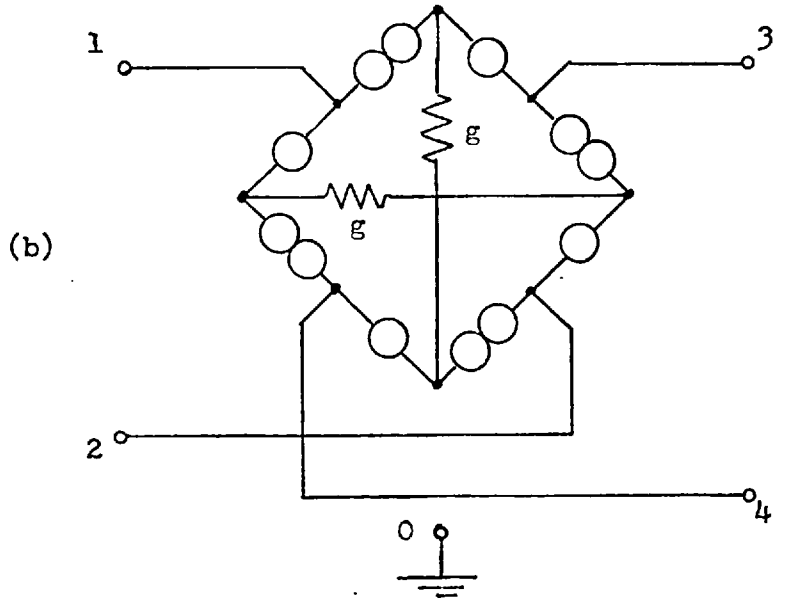


Fig. 6-5 : Special case of Fig. 6-1 where i_o=0 (Floating Inverter).



$$i_1 = g\,(v_3 - v_4)$$
$$-i_4 = -g\,(v_3 - v_4)$$
$$i_1 + i_2 + i_3 + i_4 = 0$$
$$v_1 = v_4$$



$$i_1 = g\,(v_3 - v_4)$$
$$i_2 = -g\,(v_3 - v_4)$$
$$i_3 = -g\,(v_1 - v_2)$$
$$i_4 = g\,(v_1 - v_2)$$

Fig. 6-6 : Two examples of floating inverters.

which cannot be distinguished by terminal measurements.

6.5 - FLOATING 3-TERMINAL INVERTER

The special case where terminals 4 and 1 coincide (Fig. 6-7) will now be examined. It should be noted that the four cases corresponding to terminals 4 or 3 coincident with 1 or 2 only differ from each other by the numbering of the terminals.

The terminal description (6-11) for the present case, must contain the equation

$$v_1 = v_4$$

Also, since terminals 1 and 4 are connected (Fig. 6-7) the voltages and currents must be affected in the same way by i_1 and i_4 and therefore these currents must always occur in (6-11) combined as $(i_1 + i_4)$. This means that the coefficients multiplying i_1 and i_4 must be equal, i.e.

$$m_{i1} = m_{i4} \quad \text{for } i = 1, 2, 3, 4$$

Therefore (6-11) becomes

$$\begin{bmatrix} 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \mp \begin{bmatrix} 0 & 0 & g_a & -g_a \\ -g_b & g_b & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \qquad (6\text{-}19)$$

Comparison of (6-19) and (6-16) shows that (6-19) is a special case of (6-16). Thus the case of terminals 4 and 1 coinciding is revealed - unexpectedly - as a special case of floating inverter. Since two of the terminals coincide this case will be referred to as <u>floating 3-terminal inverter</u>. One possible way of realizing it is by using any 2-port inverter which is 3-terminal and making it "float" by one

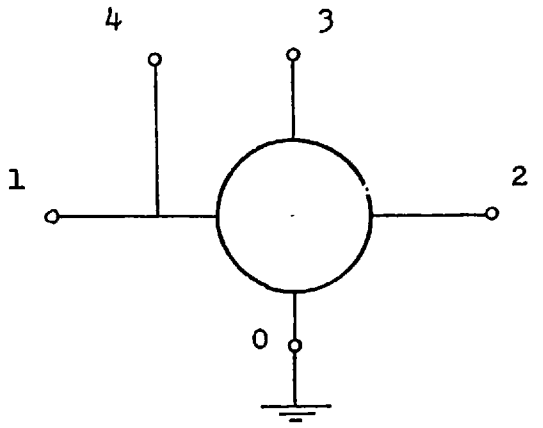


Fig. 6-7 : Special case of Fig. 6-1 where terminals 4 and 1 coincide (Floating 3-terminal inverter).

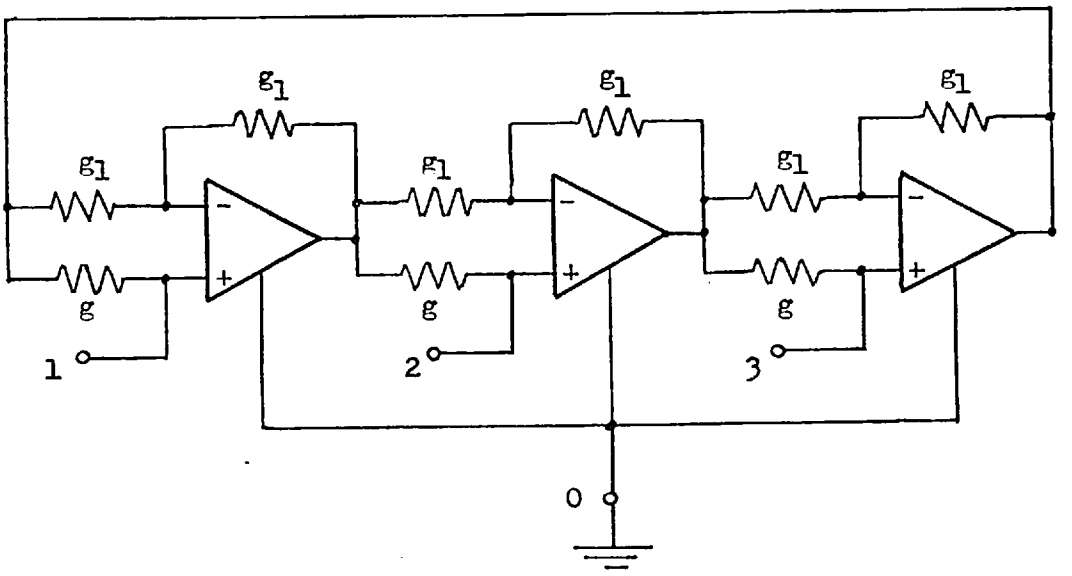


Fig. 6-8 : A 3-port circulator.

of the methods mentioned in the previous section.

If the network of Fig. 6-7 is regarded as a 4-terminal network (terminals 1 and 4 are merged) then the terminal description will be, from (6-19)

$$\begin{bmatrix} i_1 + i_4 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} g_a - g_b & -g_b & g_a \\ g_a & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (6\text{-}20)$$

If $g_a = g_b$, (6-20) becomes the description of a 3-port <u>circulator</u>:

$$\begin{bmatrix} i_1 + i_4 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & -g & g \\ g & 0 & -g \\ -g & g & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (6\text{-}21)$$

It should be noted, however, that although the same network that realizes a 3-port circulator can be used to realize a 3-port inverter, these two 3-ports are quite distinct: the ports, are formed in a different way and the port descriptions are very different.

The use of a circulator to simulate floating inductors was proposed by Rollet [85]. A circulator can be actively realized in different ways. A circuit that realizes a 3-port circulator, with all three ports grounded, and which contains 3 operational amplifiers [86, 87] is shown in Fig. 6-8.

6.6 - THE 'GENERAL' INVERTER

Most of the circuits that have been proposed for the simulation of floating inductors by admittance inversion belong to the special cases considered in the previous sections, i.e., they can be classified

either as 4-terminal inverters or as floating inverters (this includes the circuit using a circulator, which is regarded as a floating 3-terminal inverter). However, there are 3-port gyrators suitable for floating inductor simulation which do not belong to any of these special cases. An example of such a 'general' inverter ('general' means simply that the inverter does not belong to one of the special cases) appears as part of a circuit in a recent publication [49] on wave active filters, derived from doubly terminated LC ladder filters. In [49] a floating inductor is replaced by the circuit shown here in Fig. 6-9. This circuit uses only one capacitor. If the capacitor is extracted and regarded as the termination of a port, the remaining circuit is a 3-port inverter of the 'general' type, as will now be shown.

The circuit in Fig. 6-9a can be redrawn as shown in Fig. 6-9b where the operational amplifiers are replaced by nullors. Analysis of this circuit shows that it can be described by

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} - \begin{bmatrix} 0 & 0 & g/2 & -g/2 \\ -g/2 & g/2 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \qquad (6\text{-}22)$$

This equation is in the form of (6-11). However, the circuit is not a 4-terminal inverter since it is not constrained to have any voltage equal to zero. It can also be seen that i_3 does not appear in the equations describing the circuit and therefore the currents are not constrained to be $i_1 + i_2 + i_3 + i_4 = 0$ or $i_0 = 0$, which means that the circuit is not a floating inverter.

It might be asked whether it is possible to distinguish, by terminal measurements, between different 'general' realizations of the

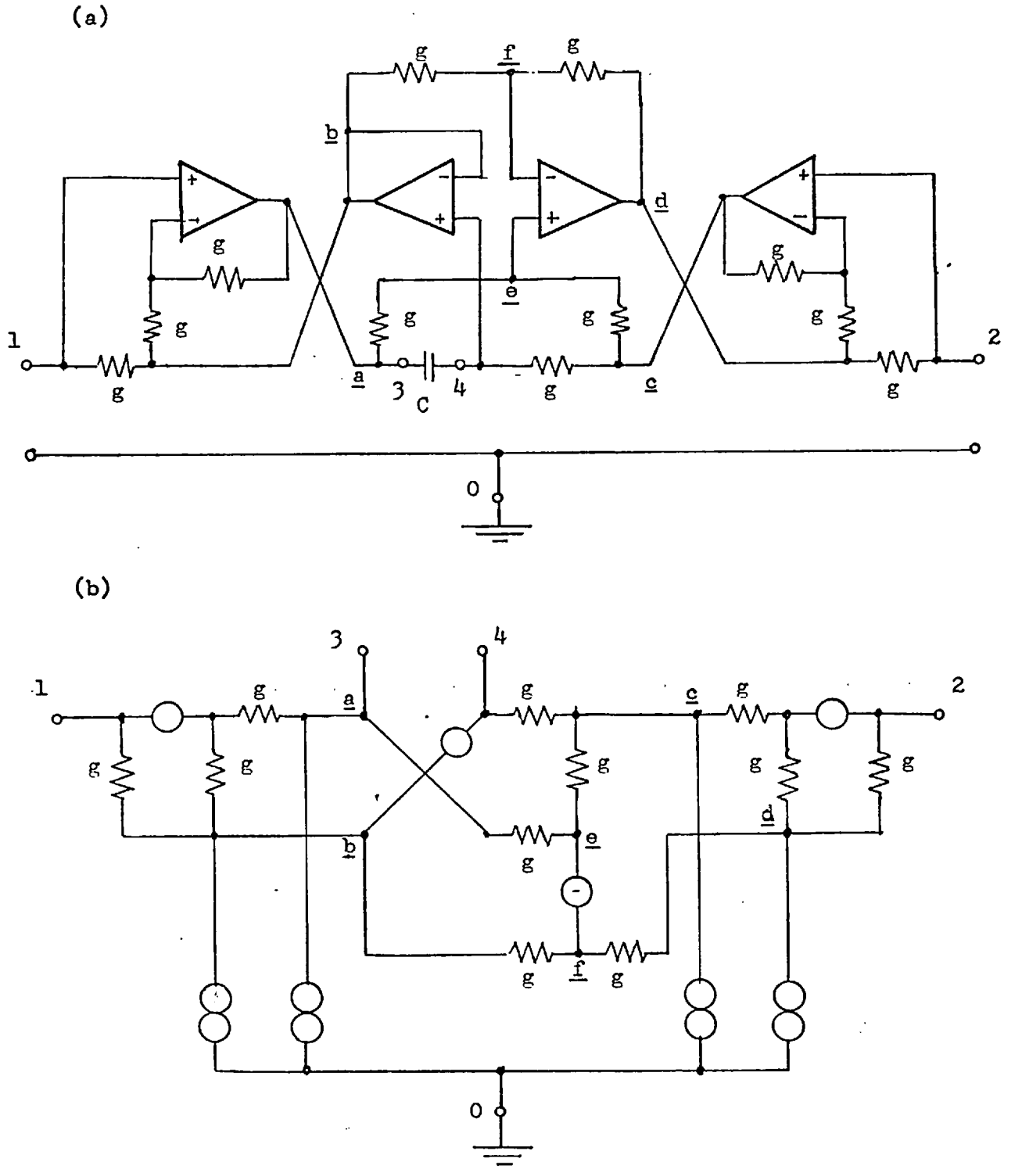


Fig. 6-9 : A 'general' inverter.

3-port inverter. This question can be answered, in the affirmative, by considering the circuit of Fig. 6-10 which is a 'general' inverter as the circuit of Fig. 6-9 but has a different terminal description. The circuit of Fig. 6-10 can be described by

$$i_1 = g_a (v_3 - v_4)$$

$$i_2 = -g_a (v_3 - v_4)$$

$$i_3 = -g_b (v_1 - v_2)$$

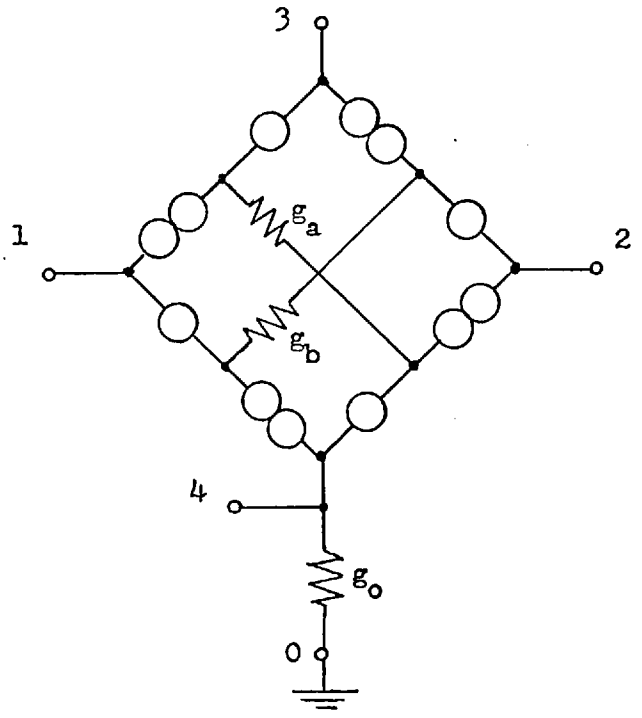
$$i_4 = g_b (v_1 - v_2) + g_o v_4$$

These equations show that the circuit is a 'general' inverter since neither any of the voltages is constrained to be zero nor does $i_o = i_1 + i_2 + i_3 + i_4 = 0$ apply. This circuit has an admittance description and can therefore be distinguished from the circuit of Fig. 6-9 which does not possess an admittance description as shown by the fact that the matrix multiplying the current-vector in (6-22) is singular (the circuit of Fig. 6-10 is presented here only to illustrate the possibility of distinguishing between different 'general' inverters; it is not claimed that this circuit is of practical interest).

An additional example of 'general' inverter is provided by a circuit that has recently been proposed for the simulation of floating inductors [88]. The circuit can be realized with 3 operational amplifiers and is shown in Fig. 6-11 in a nullator-norator representation. It is easily seen that if $g_1 = g_5 = g$ and $g_5 g_7 = g_6 g_8$ the circuit is equivalent to a floating admittance:

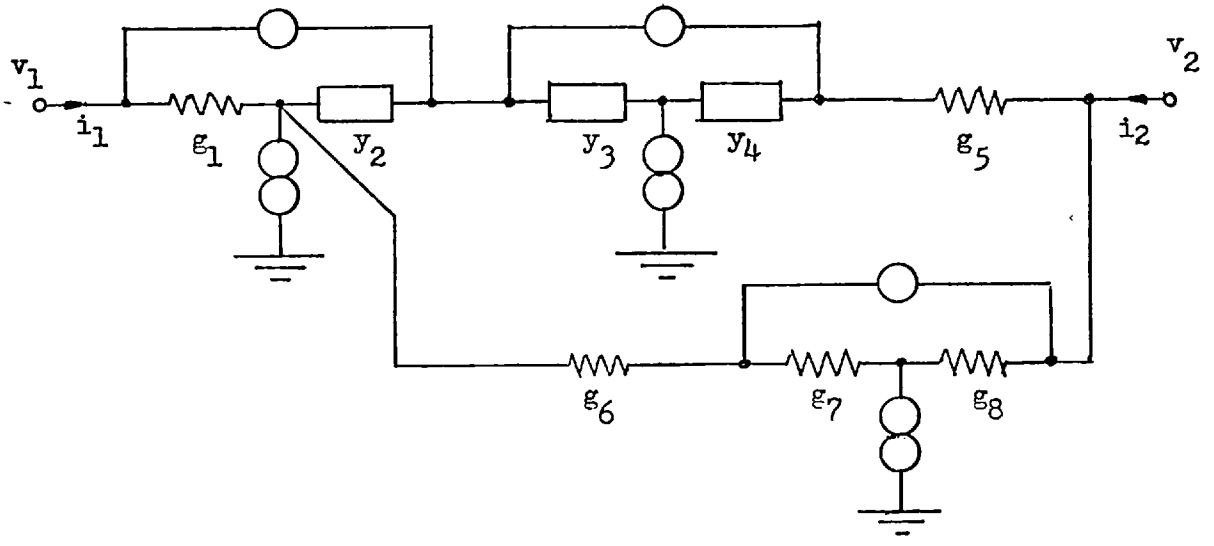
$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = g^2 \frac{y_3}{y_2 y_4} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \qquad (6\text{-}23)$$

The floating admittance will represent a floating inductor if y_2 (or y_4) is realized by a capacitor and y_3 and y_4 (or y_2) are realized by resistors.



$$i_1 = g_a (v_3 - v_4)$$
$$i_3 = -g_b (v_1 - v_2)$$
$$i_1 + i_2 = 0$$
$$i_3 + i_4 = g_o v_4$$

Fig. 6-10 : Another 'general' inverter.



$$i_1 = g_1 g_5 \frac{y_3}{y_2 y_4} (v_1 - v_2)$$

$$i_1 = -i_2 \quad \text{if } g_1 = g_5 \text{ and } g_5 g_7 = g_6 g_8$$

Fig. 6-11 : A circuit for floating inductor simulation which can be interpreted either as a converter or as an inverter.

The resulting circuit can be regarded either as a 3-port inverter terminated by the capacitor or as a 3-port converter terminated by the resistor that realizes y_3. It can be shown that the two inverter circuits obtained by extraction of y_2 or y_4 are 'general' inverters.

6.7 - THREE-PORT CONVERTERS FOR FLOATING INDUCTOR SIMULATION

The 3-port admittance converters that simulate a floating inductor when terminated by a resistor have the general 5-terminal configuration shown in Fig. 6-12. Although different realizations must have the same 3-port description, expressed by equation (6-2), they may have different terminal descriptions. Since the situation is similar to that encountered in connection with the inverters, a classification parallel to the one developed in the previous sections can be applied to the 3-port converters used for the simulation of floating inductors. Given the close similarity between the two classifications, only a brief outline of the classification of the converters will be given here.

It can be shown that the 5-terminal network of Fig. 6-12 must have a description in the form of

$$\begin{bmatrix} 1 & 0 & -h_a+\alpha & \alpha \\ 0 & 0 & \beta & \beta \\ 1 & 1 & \gamma & \gamma \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ h_b & -h_b & 1 & -1 \\ 0 & 0 & 0 & 0 \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}24)$$

The same special cases that were considered in connection with the inverters will now be examined.

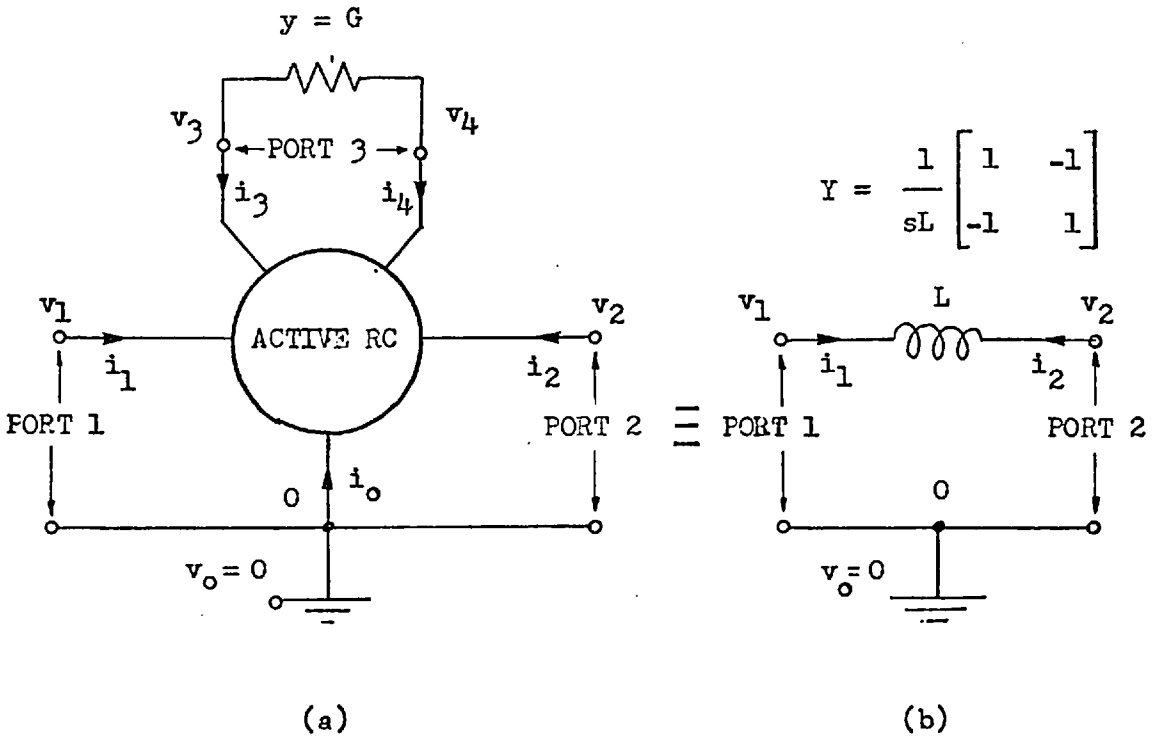


Fig. 6-12 : Floating inductor simulation

by admittance conversion

Terminals 4 and 0 coincide: 4-terminal converter

In this case the 5-terminal network of Fig. 6-12 assumes the particular configuration shown in Fig. 6-2. It is easy to show that equation (6-24) becomes:

$$\begin{bmatrix} 1 & 0 & -h_a & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ b & -b & 1 & -1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}25)$$

$i_o = 0$: floating converter

In this case $\delta = 1$ in equation (6-24):

$$\begin{bmatrix} 1 & 0 & -h_a+\alpha & \alpha \\ 0 & 0 & \beta & \beta \\ 1 & 1 & 1 & 1 \\ m_{41} & m_{42} & m_{43} & m_{44} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ h_b & -h_b & 1 & -1 \\ 0 & 0 & 0 & 0 \\ p_{41} & p_{42} & p_{43} & p_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}26)$$

A floating converter can be obtained from an ordinary 2-port converter by using one of the methods mentioned in connection with the floating inverter (section 6.4).

Terminals 4 and 1 coincide: floating 3-terminal converter

Equation (6-24) becomes

$$\begin{bmatrix} 1 & 0 & -h_a+1 & 1 \\ 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ -h_b & h_b & 1 & -1 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \quad (6\text{-}27)$$

As for the inverters, this case can be recognized as a special floating converter since (6-27) is a special case of (6-26).

If the 5-terminal network which has in this case the configuration shown in Fig. 6-7 is regarded as 4-terminal by merging terminals 1 and 4, its description can be written (from 6-27)) as

$$\begin{bmatrix} i_1+i_4 \\ i_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0 & 0 & h_a-1 \\ 0 & 0 & -h_a \\ 1-h_b & h_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \qquad (6\text{-}28)$$

In view of the correspondence between this case and the floating 3-terminal inverter, equation (6-28) corresponds to (6-20). However whereas (6-20) with $g_a = g_b$ is recognized as the description of a circulator, no way has been found of associating (6-28) with any well known 3-port.

A 3-port converter can be realized by two grounded 2-port converters. The resulting circuit has already been met in previous chapters and is reproduced here in Fig. 6-13. If the 2-port converters have the description in Fig. 6-13, then the terminal description of the 5-terminal network can be written as

$$\begin{bmatrix} 1 & 0 & -h_a & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 1 & -h_a & -h_a \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 & 0 \\ h_b & -h_b & 1 & -1 \\ 0 & 0 & 0 & 0 \\ h_b & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = 0 \qquad (6\text{-}29)$$

This equation shows that the realizations of Fig. 6-13 does not belong to any of the special cases, except if $h_a = -1$, when it becomes a floating converter.

It has already been mentioned that the circuit shown in Fig. 6-11 can be interpreted either as a converter or as an inverter. In contrast

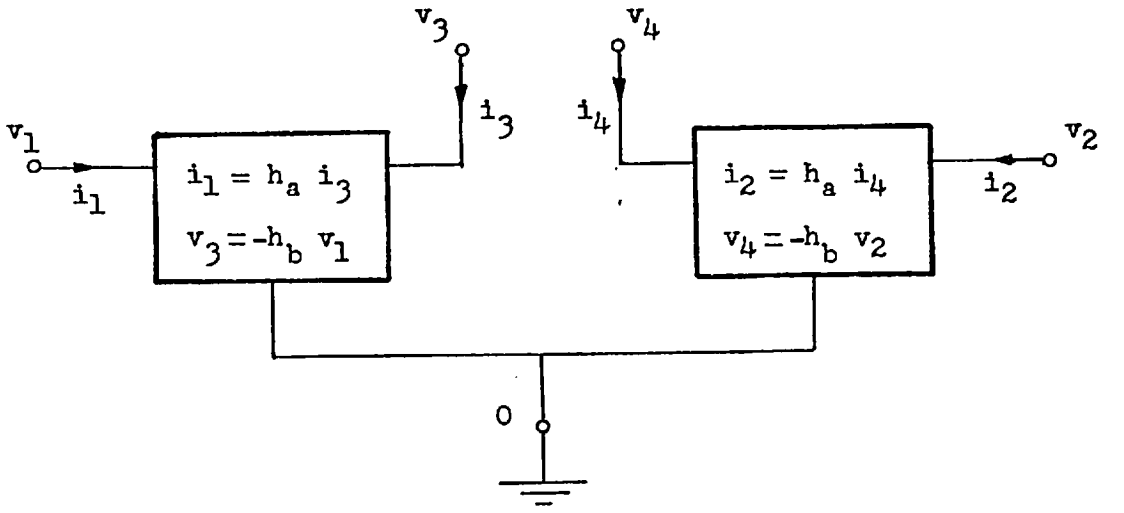


Fig. 6-13 : Three-port converter using two grounded converters.

the circuit of Fig. 6-13 can only be interpreted as a converter since it must contain more than one capacitor (both 2-port converters contain at least one capacitor).

It appears that the circuit shown in Fig. 6-13 is the only one that has been proposed so far for the simulation of floating inductors that can be interpreted as a 3-port converter but not as a 3-port inverter.

6.8 - A FAMILY OF 3-PORT INVERTERS USING 3 OPERATIONAL AMPLIFIERS

It has been mentioned before that the 3-port inverter circuit using two grounded 2-port inverters (Fig. 6-3) and the circuit published by Deboo, employing three operational amplifiers (Fig. 6-4) have the same terminal description and therefore cannot be distinguished by external measurements. In terms of the classification proposed here the two circuits belong to the same class: they are both 4-terminal inverters. However, these two circuits appear to be otherwise unrelated: one of them contains 3 operational amplifiers; the other uses 2 grounded positive inverters each of which requires at least 2 operational amplifiers (a proof that a grounded positive inverter requires at least two operational amplifiers will be presented in the next chapter). However, it will now be shown that when two specific positive inverter circuits, each containing two operational amplifiers, are connected in accordance with Fig. 6-3, one of the operational amplifiers can be made redundant; if the redundant amplifier is supressed, a 4-terminal inverter containing 3 amplifiers is obtained. In fact, the two inverters can be connected in four different ways and in each case one amplifier can be suppressed. In this way a family of four different circuit configurations which realize the 4-terminal inverter is obtained. These four circuit configurations will be given in a nullator-norator representation; each configuration contains

three nullors which can be replaced by operational amplifiers. One of the operational amplifier realizations of one of the four nullor circuits is the circuit proposed by Deboo.

The two specific positive inverter circuits to be connected in accordance with Fig. 6-3 are the two gyrator circuits of reference [78] shown here, in a nullator-norator representation, in Fig. 6-14. For convenience, the two gyrator circuits will be designated as circuit A and circuit B. These two circuits can be connected in the four possible combinations:

AA AB BA BB

Circuit AA:

When two gyrator circuits of type A are connected to form a 3-port 4-terminal inverter (Fig. 6-15a), it is very easy to see that it is possible to eliminate one nullor. In the circuit of Fig. 6-15a there is a positive resistor in parallel with a negative resistor between terminal 3 and the ground (the negative resistor is realized by the circuit of Fig. 3-11, in chapter 3). This parallel combination of two conductances g and -g is equivalent to an open-circuit and can therefore be eliminated from the circuit of Fig. 6-15a, leading to the circuit of Fig. 6-15b with only 3 nullors.

Circuit BA:

This case is shown in Fig. 6-16. Two equal resistors of conductance g can be connected between node a and the ground and between node b and the ground, as shown in Fig. 6-16a (without affecting the port behaviour). This is so because the part of the circuit between a and b is a negative imittance converter with conversion factor -1 (if the equivalence of Fig. 3-7a is applied and one of the two additional resistors is transferred

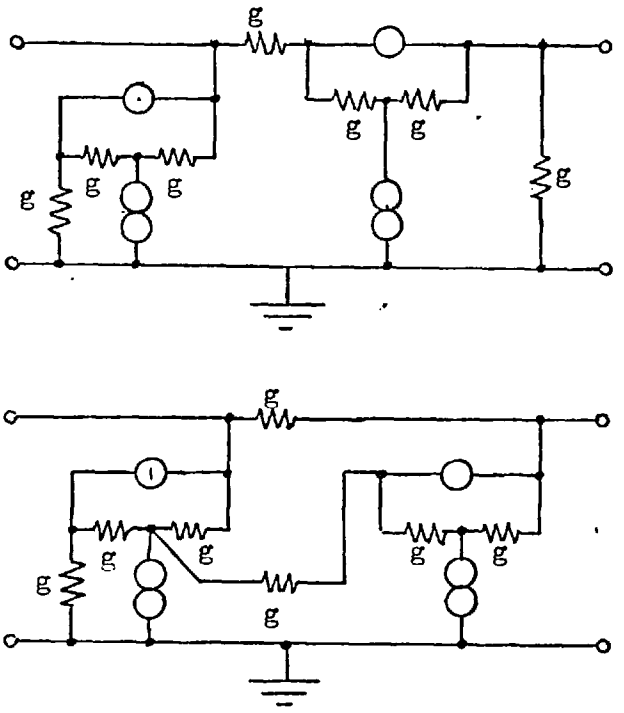


Fig. 6-14 : Two grounded gyrators.

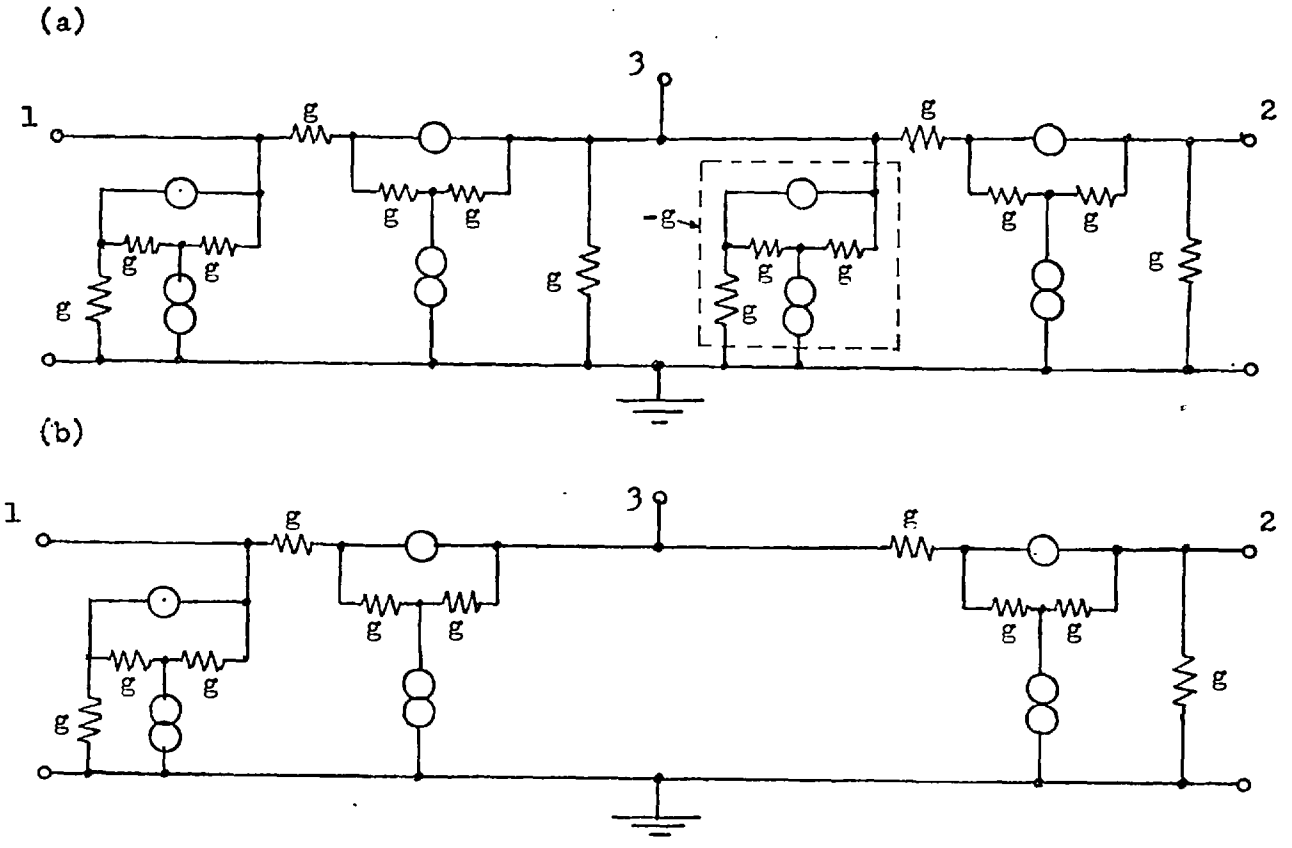


Fig. 6-15 : Circuit AA

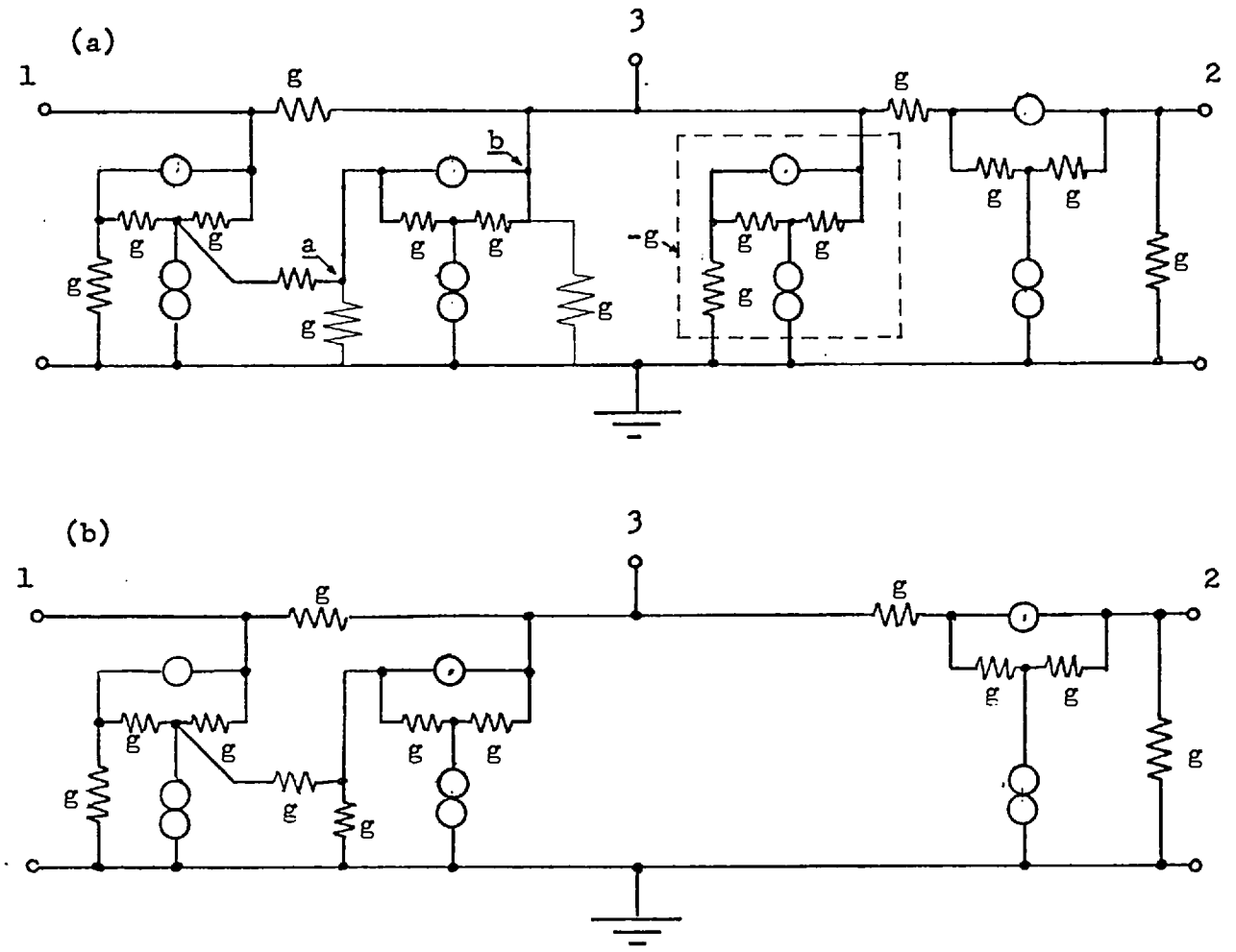


Fig. 6-16 : Circuit BA

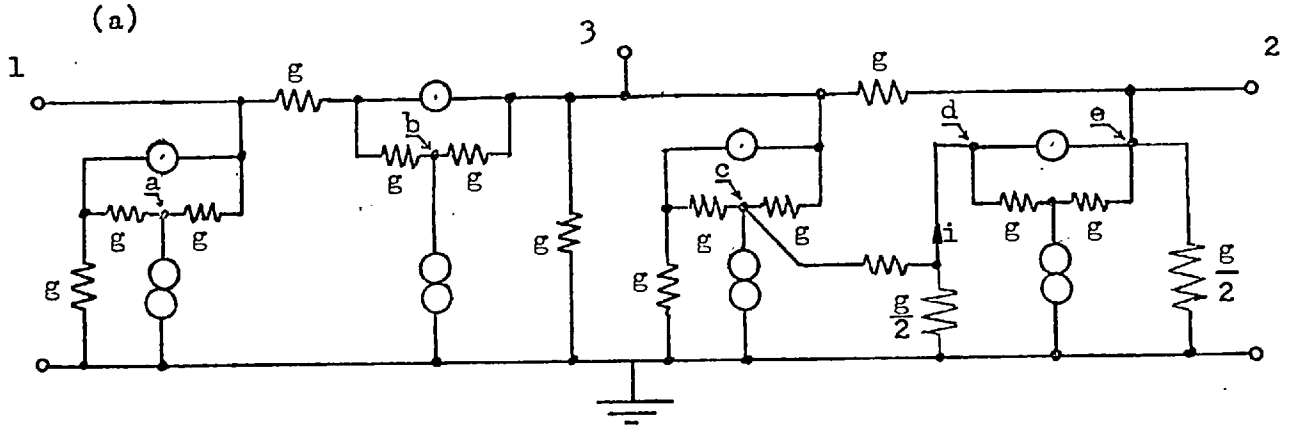
to the other side of the NIC, its conductance changes sign and cancels the other additional resistor). When the two additional resistors are inserted in the circuit a parallel combination of a positive and a negative resistor appears between terminal 3 and the ground. If this combination is eliminated, the 3-nullor circuit of Fig. 6-16b is obtained.

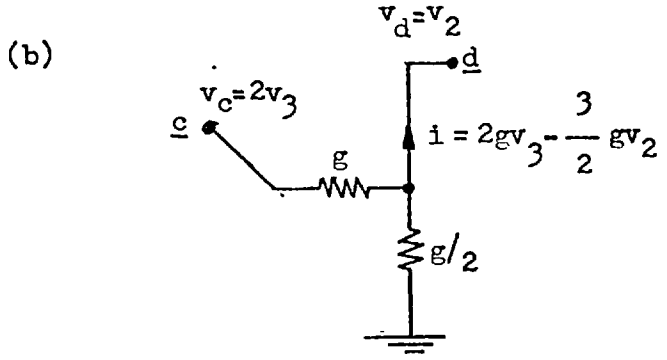
Circuit AB:

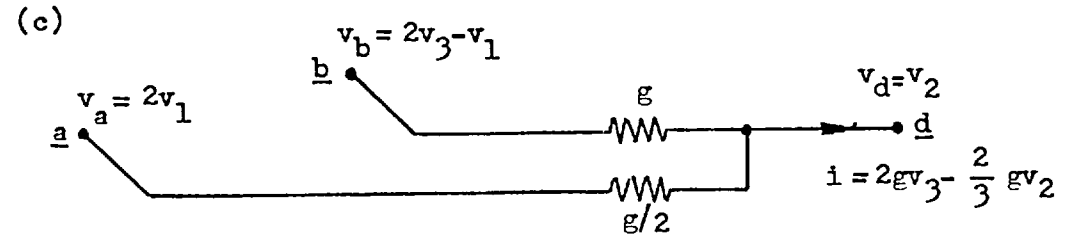
This configuration is given in Fig. 6-17. Two equal resistors of conductance g/2 can be added to the circuit between points d and e and the ground, since the part of the circuit between d and e is a NIC with conversion factor -1 (Fig. 6-17a). The voltages and currents in the circuit, with the exception of the currents in the norators, will not be altered if the part of the circuit shown in Fig. 6-17b is replaced by the circuit shown in Fig. 6-17c. If this replacement is carried out, the parallel combination of a positive and a negative resistor with conductances g and -g appears between terminal 3 and the ground. If this is eliminated, the circuit of Fig. 6-17d is obtained.

Circuit BB:

The connection of two gyrator circuits of type B is shown in Fig. 6-18a. Two equal resistors of conductance g can be connected between points b and d, and the ground. Another pair of resistors with conductance g/3 can be connected between points f and h and the ground (Fig. 6-18a). If the part of the circuit shown in Fig. 6-18b is replaced by the circuit shown in Fig. 6-18c, the voltages and currents in the remaining circuit, apart from the currents in the norators, will not be affected. When this replacement is carried out, the parallel combination of a positive and a negative resistor appears between







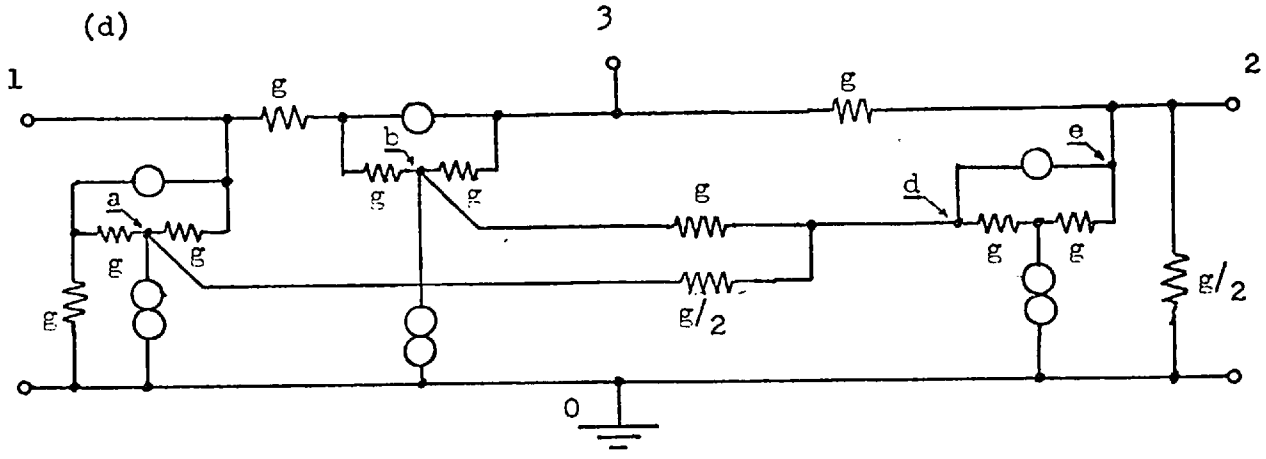


Fig. 6-17 : Circuit AB.

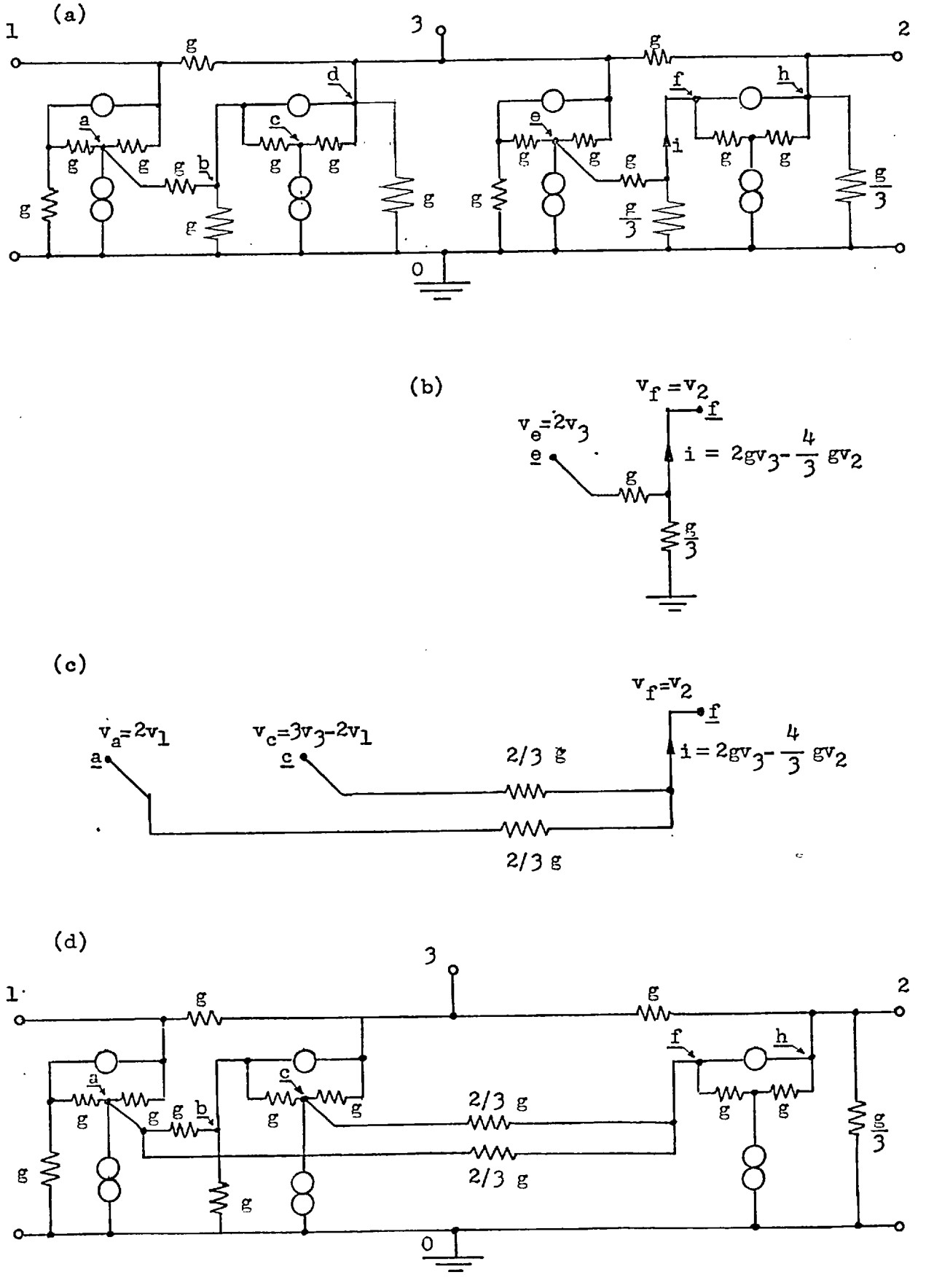


Fig. 6-18 : Circuit BB.

terminal 3 and ground. The supression of this combination leads to the circuit of Fig. 6-18d which contains 3 nullors.

It can easily be seen that the circuit in Fig. 6-17d, obtained from the configuration AB, is a nullor representation of Deboo's circuit (Fig. 6-4).

All four circuits can be realized using 3 operational amplifiers with differential input and grounded output. As mentioned before (section 2.2) a circuit with n nullators and n norators can be realized in 2^n n! different ways (there are n! different possibilities for pairing the nullators with the norators and 2^n different choices for the polarity of the inputs of the n operational amplifiers). For n = 3 there are 48 different operational amplifier realizations which have different non-ideal performance (including different stability properties).

6.9 - CONCLUSIONS

In this chapter the various methods of active RC simulation of floating inductors based on admittance inversion and conversion have been examined; in particular, the possibility of distinguishing between different circuits by external measurements was considered. All 3-port admittance inverters suitable for floating inductor simulation have the same port description (equation (6-1)) and therefore cannot be distinguished by port measurements (apart from different values of g_a and g_b); similarly all 3-port admittance converters for floating inductor simulation are described by (6-2) and cannot be distinguished by port measurements (apart from the values of h_a and h_b). However, these 3-port converters and inverters are in

general 5-terminal networks which may have different terminal descriptions. It may thus be possible to distinguish different realizations by terminal measurements.

The possibility of distinguishing different inverters by their terminal description has been used to establish a classification of inverters suitable for floating inductance simulation. In general their terminal description can be written in the form of equation (6-11) which contains several unspecified parameters. A special case is the "4-terminal inverter", described by (6-12) which includes, among others, Holt and Taylor's 2-gyrator circuit and Deboo's 3-amplifier circuit. Another special case is the "floating inverter", with a description in the form of (6-16), which includes any 2-port inverter with an individual, ungrounded power supply. A special floating inverter is the "floating 3-terminal inverter". The circuit using a circulator corresponds, in terms of the classification, to a floating 3-terminal inverter for which $g_a = g_b$.

According to the classification proposed here, circuits of different classes have different terminal descriptions, i.e. are distinguishable by terminal measurements. Whereas all 4-terminal inverters have the same terminal description, it has been shown, by means of an example, that different floating gyrators may have different terminal descriptions. All floating 3-terminal inverters, however, have the same terminal description. It has been shown that different 'general' inverters (i.e. inverters that are neither 4-terminal nor floating) can have different terminal descriptions.

A similar classification has been established for converters used in floating inductance simulation. Apart from those circuits that can be interpreted either as a terminated converter or as a terminated

inverter, the only converter circuit for floating inductor simulation referred to in the literature is apparently the circuit using two grounded 2-port converters, which belongs to the general case. This is in contrast with the situation encountered with inverters of which many realizations have been published, almost all of them belonging to the special classes.

Finally it has been shown that a family of 4-terminal inverters with 3 operational amplifiers can be derived from the circuit using two grounded gyrators, when these are replaced by two specific gyrator circuits. Although each gyrator has two amplifiers, one amplifier can be made redundant after the two gyrators are connected and can therefore be eliminated. One of the 3-amplifier circuits obtained is the circuit proposed by Deboo. It is thus shown that this circuit, which belongs to the same class as the 2-gyrator circuit, can, in addition, be derived in a simple way from a realization employing two specific gyrator circuits.

CHAPTER 7

INVERTERS WITH A MINIMUM NUMBER OF ACTIVE COMPONENTS

7.1 - INTRODUCTION

The present chapter is concerned with the realization of inverters with a minimum number of active components; in particular, 2-port positive inverters using only one active component will be considered in detail, and the possibility of grounding both ports in such inverters will be investigated. The results obtained are useful as contributions to the subject of minimal realizations of 2-port inverters, and have also direct consequences regarding the realization of multiport inverters, in general, and of 3-port inverters for floating inductance simulation, in particular. This is so because multiport admittance inverters and also some types of impedance inverters can be realized as an interconnection of grounded 2-port inverters, as discussed in chapter 5 (see Figs. 5-9 and 5-13). It should be noted that the designation 'grounded 2-port' is used in this thesis for 2-ports in which the ports have a common terminal which can be grounded.

The investigation of the minimum number of active components required to realize a network with a given description is not only of theoretical interest but is also very interesting from a practical point of view. A reduction in the number of active components in a network leads to a reduction in the d.c. power required, the heat generated, the cost, and also the volume and weight. It may be noted,

however, that there is often a trade-off between number of active components and sensitivity [89]: a reduction in the number of active components is in many instances accompanied by an increased sensitivity.

It will be assumed that the inverters to be considered here are described by real and constant parameters. It has been mentioned before (chapter 3) that a 2-port positive inverter has an admittance description of the form

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & y_{12} \\ y_{21} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

where y_{12} and y_{21} are real constants with opposite signs. If $|y_{12}| = |y_{21}|$, the positive inverter is externally passive and is called a gyrator. If $|y_{12}| \neq |y_{21}|$, the positive inverter is externally active. The designation 'active gyrator' has sometimes been used in the literature to refer to externally active positive inverters. These are referred to in this thesis simply as positive inverters, the designation 'gyrator' being restricted to externally passive inverters.

In the context of active RC networks 2-port inverters described by real and constant parameters are realized with resistors and active components (this applies also to the gyrator although it is externally passive). The active components of practical interest in the context of present technology are the transistor and the operational amplifier. The operational amplifiers commonly available have a differential input and grounded output. It will be assumed, throughout this chapter that, unless explicitly stated otherwise, the operational amplifiers have differential input and grounded output.

It is convenient to use the nullor model of transistors and operational amplifiers discussed in chapter 2, section 2.2, and shown in Figs. 2-9 and 2-10. It should be remembered that in the nullor

model of the transistor the nullator and the norator must have a common terminal; in the nullor model of an operational amplifier with differential input and grounded output the nullator and norator do not have to share a common terminal but one of the terminals of the norator must be grounded.

It is known that although the realization of gyrators ($|y_{12}| = |y_{21}|$) with nullors and resistors requires at least two nullors, it is possible to realize externally active positive inverters ($|y_{12}| \neq |y_{21}|$) with only one nullor. The main contribution in this chapter is the proof that in such one-nullor positive inverters it is not possible to ground both ports if the nullor is realized either as an ideal operational amplifier with grounded output or as an ideal transistor.

The operational amplifier realization of 2-port negative inverters and of 3-port inverters for floating inductor simulation will also be discussed.

7.2 - A REVIEW OF POSITIVE INVERTERS WITH A MINIMUM NUMBER OF ACTIVE COMPONENTS

It is well known that positive inverters can be realized by circuits containing resistors and two nullors. There are circuits in which the nullors can be replaced by operational amplifiers and circuits in which the nullors can be replaced by transistors. In both cases it may be possible for the inverter to have both ports grounded. Several examples of 2-nullor positive inverters which illustrate these statements will now be considered.

The two circuits in Figs. 7-1 and 7-2 are positive inverters (these circuits can be regarded as a cascade of the NIC of Fig. 3-9a and the NII of Fig. 3-10, in chapter 3). The circuit in Fig. 7-1 can be

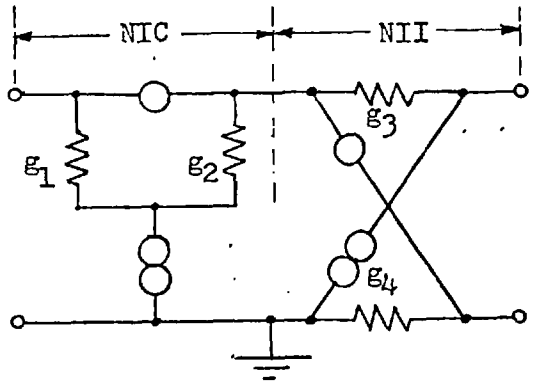


Fig. 7-1 : Gyrator realizable with 2 op. amplifiers.

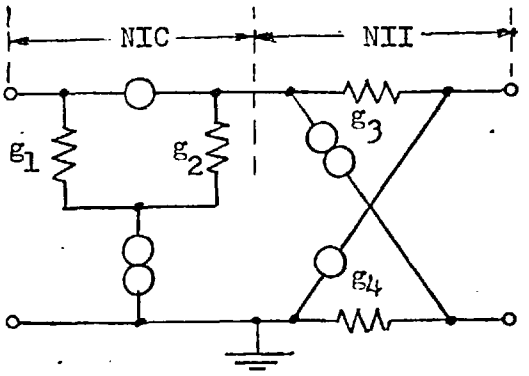


Fig. 7-2 : Gyrator realizable with 2 transistors.

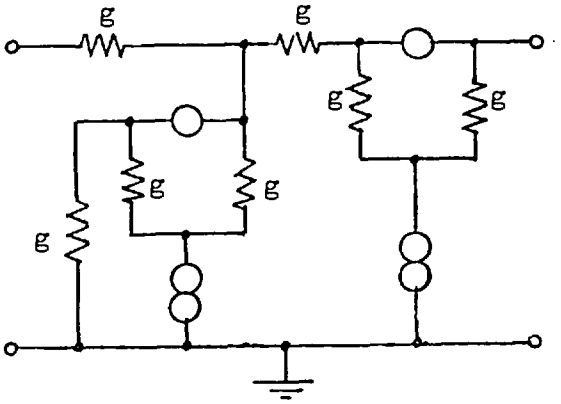


Fig. 7-3 : Grounded gyrator realizable with 2 op. amps.

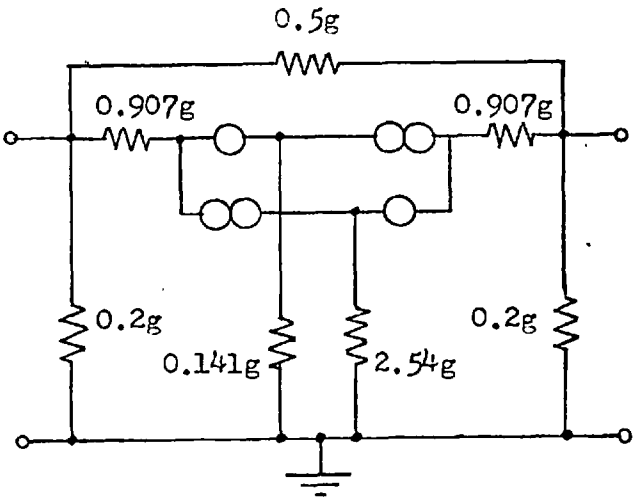


Fig. 7-4 : Grounded positive inverter realizable with 2 transistors.

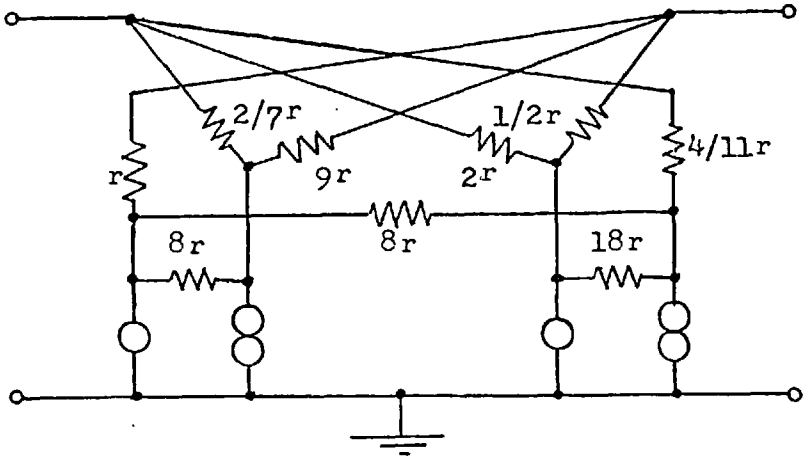


Fig. 7-5 : Grounded gyrator realizable with 2 operational amplifiers with grounded input and output.

realized with 2 operational amplifiers (with differential input and grounded output) since the norators have a common terminal. The circuit of Fig. 7-2 contains 2 nullators and 2 norators which can be paired to form nullors that can be replaced by transistors (problems associated with d.c. bias and stability of the transistor realization are not taken into account here). The two circuits in Figs. 7-1 and 7-2 behave as positive inverters for any value of the conductances; if all the conductances are equal both circuits are gyrators. Neither of these circuits can have both ports grounded.

A grounded gyrator realizable with two operational amplifiers [11] is shown in Fig. 7-3. The circuit in Fig. 7-4 [90] is a grounded positive inverter which can be realized with two transistors. In contrast to the two previous inverters (Figs. 7-1 and 7-2) the circuits of Figs. 7-3 and 7-4 only behave as inverters if the values of the conductances are suitably related (the values given in the figures are one possible set of conductance values).

The circuit in Fig. 7-5 [91] is very interesting with respect to the present discussion of inverters with a minimal number of active components: it shows that a grounded gyrator can be realized with 2 operational amplifiers with grounded input and grounded output.

The above examples show that, in addition to resistors, <u>two nullors are sufficient</u> to realize a positive inverter, in general, and a gyrator, in particular. A natural question is whether two nullors are necessary. This question will now be discussed.

It has been proved by Martinelli and Di Porto [92] that the 2-port obtained by embedding one nullor in a resistive 4-port network (Fig. 7-6) described by an admittance matrix cannot be a gyrator. Adams and Deprettere [93] have proved the same result without the restriction that the resistive 4-port must have an admittance description;

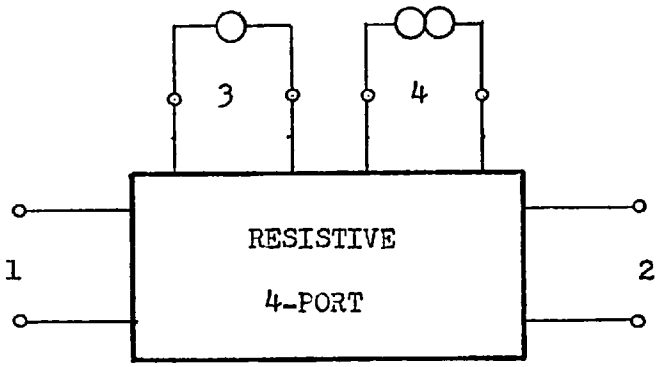


Fig. 7-6 : Connection of one nullor to a resistive 4-port.

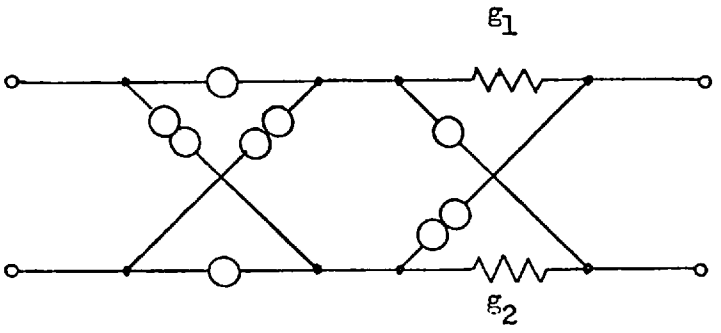


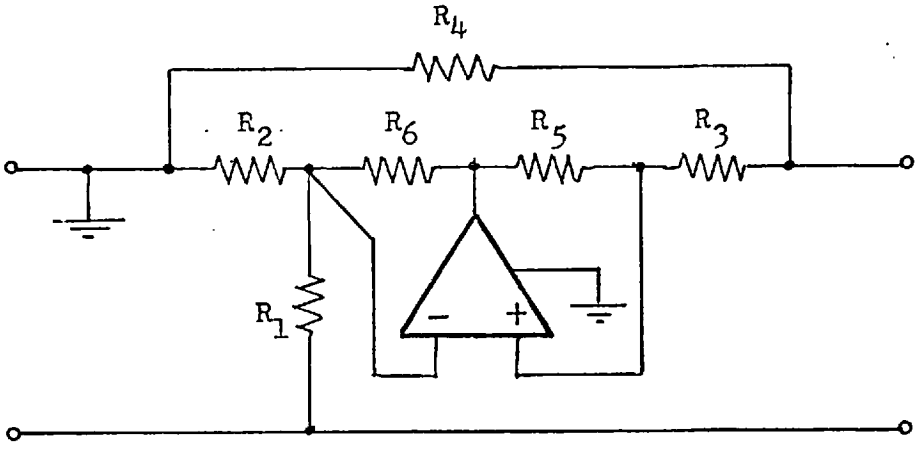
Fig. 7-7 : Gyrator with 3 nullors and only 2 resistors.

the same authors have also shown [93, 94, 95] that a gyrator requires at least 2 nullors and 4 resistors (Figs. 7-1 and 7-2) or 3 nullors and 2 resistors (Fig. 7-7). Willson and Orchard [96] have proved that it is impossible to realize a gyrator by connecting a controlled source of any kind to one of the ports of a well defined 3-port containing resistors and ideal transformers, where the controlling variable is a voltage or current inside the 3-port. This last proof is more general, not only due to the inclusion of ideal transformers, but also due to the fact that a controlled source cannot always be modelled using resistors and only one nullor. However its significance is similar to the previous proofs if consideration is restricted to realizations employing resistors and either operational amplifiers or transistors, since these can be modelled, in the ideal case, by a controlled source of infinite gain, which is equivalent to a nullor.

Until recently it was generally believed that 2 nullors would be necessary to realize a positive inverter (or, equivalently, 2 nullors would be necessary to simulate a lossless inductor using only one capacitor). However, the above proofs of the necessity of 2 nullors only apply to gyrators, i.e.,to externally passive positive inverters ($|y_{12}| = |y_{21}|$). The circuit in Fig. 7-8, due to Orchard and Willson [97] shows that, in fact, it is only the gyrator that requires 2 nullors; the circuit of Fig. 7-8 is an externally active positive inverter ($|y_{12}| \neq |y_{21}|$) and contains only one operational amplifier.

Another realization of a positive inverter using only one operational amplifier is the circuit in Fig. 7-9 [98].

It is interesting to know whether positive inverters (2-ports) with only one active component can be used to realize multiport admittance inverters (Fig. 5-9) and, in particular, 3-port inverters for floating inductance simulation (Fig. 5-10). Since these applications



$$R_2 = R_3 \qquad (1+\frac{R_1}{R_2})(1+\frac{R_3}{R_4}) = \frac{R_1R_5}{R_4R_6}$$

Fig. 7-8 : A positive inverter with only one operational amplifier (Orchard and Willson).

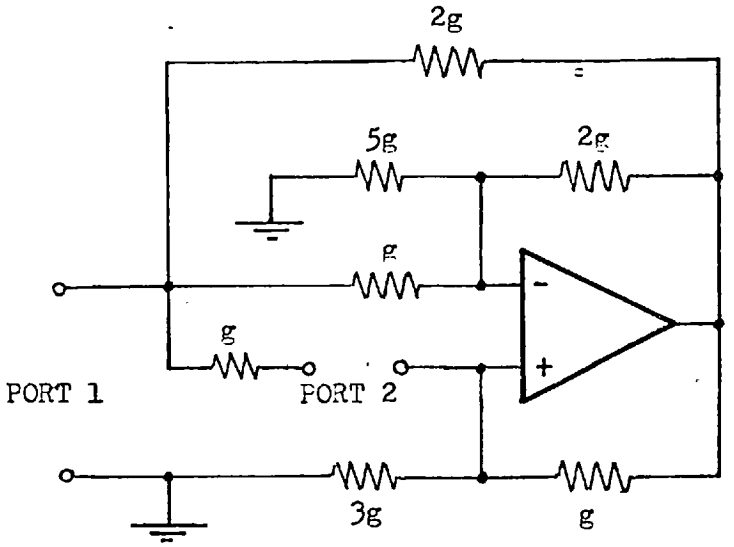


Fig. 7-9 : Another positive inverter with only one operational amplifier (Schmidt and Lee).

require 2-port inverters with both ports grounded, it is of interest to know whether it is possible to ground both ports of a positive inverter containing only one active component. The present chapter is mainly concerned with the investigation of this question. The active components to be considered are the transistor and the operational amplifier.

It may be helpful to consider the diagram in Fig. 7-10. It should be noted that when a 3-terminal network, used as a 3-port, contains one amplifier with grounded output, it may be possible to have both ports grounded, only one port grounded, or even neither port grounded, depending on the way the output of the amplifier is connected to the circuit. In the case of a transistor realization, a 3-terminal network can always be used as a 2-port with both ports grounded.

The circuit of Fig. 7-8 is an inverter of type D, in terms of the diagram of Fig. 7-10, since it is 3-terminal, and has only one port grounded. The circuit of Fig. 7-9 is of type F. The circuit inter-reciprocal with that in Fig. 7-8 (which is obtained simply by inter-changing the nullator and norator) is an inverter of type C. The possibility of realizing inverters of type E is confirmed by the circuit of Fig. 7-11. This circuit (which was obtained by the author of this thesis) is presented here solely to illustrate the existence of gyrators of type E; it is not claimed that this circuit is of any practical interest. In fact, inverters of types C and E are not of practical interest, since neither port can be grounded (when an operational amplifier with grounded output is used).

The cases A and B, in the diagram of Fig. 7-10 correspond to inverters with both ports grounded. These cases will be considered in the present chapter, and it will be proved that such inverters are impossible. The possibility of realizing non 3-terminal inverters with

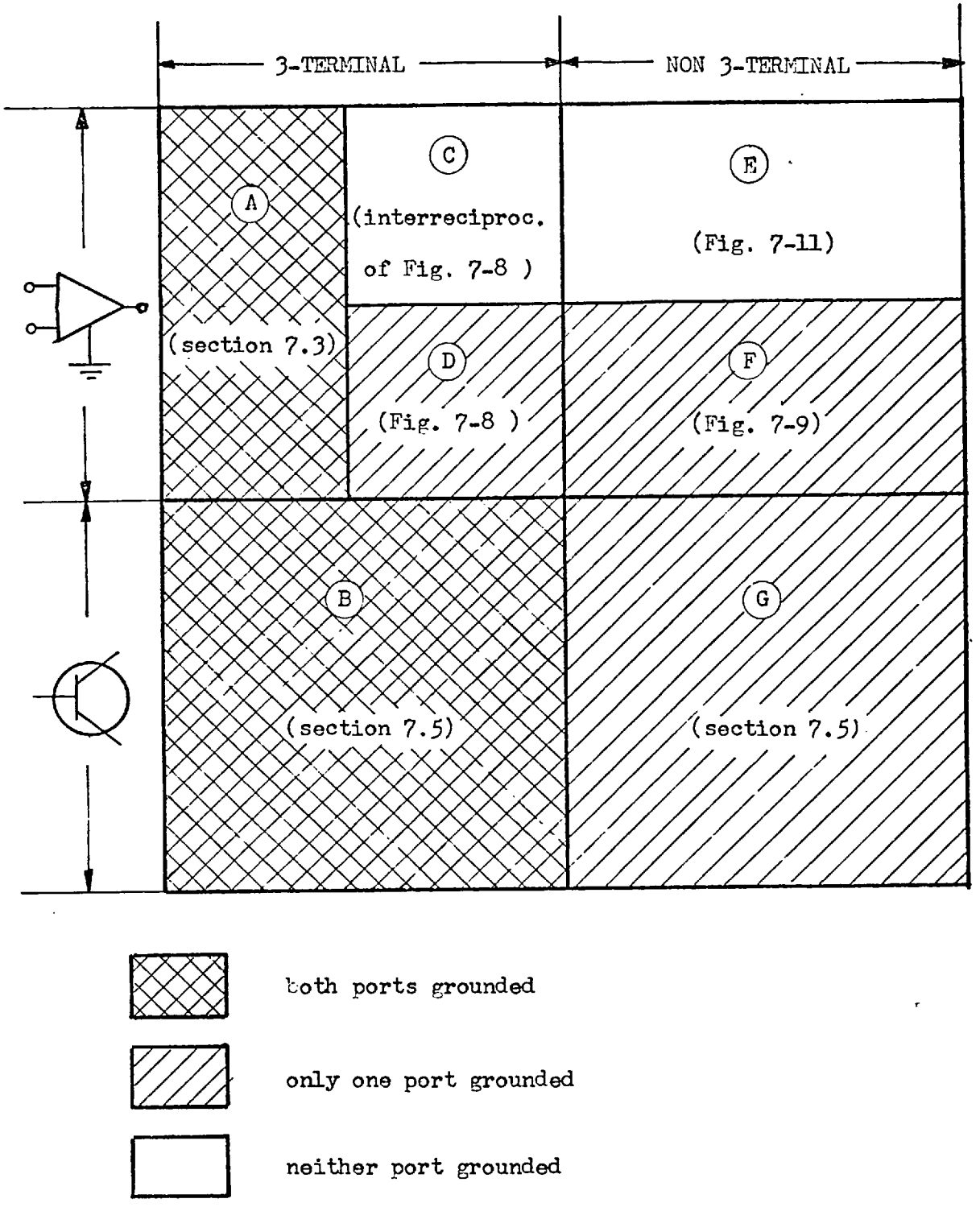


Fig. 7-10 : Different types of 1-nullor positive inverters.

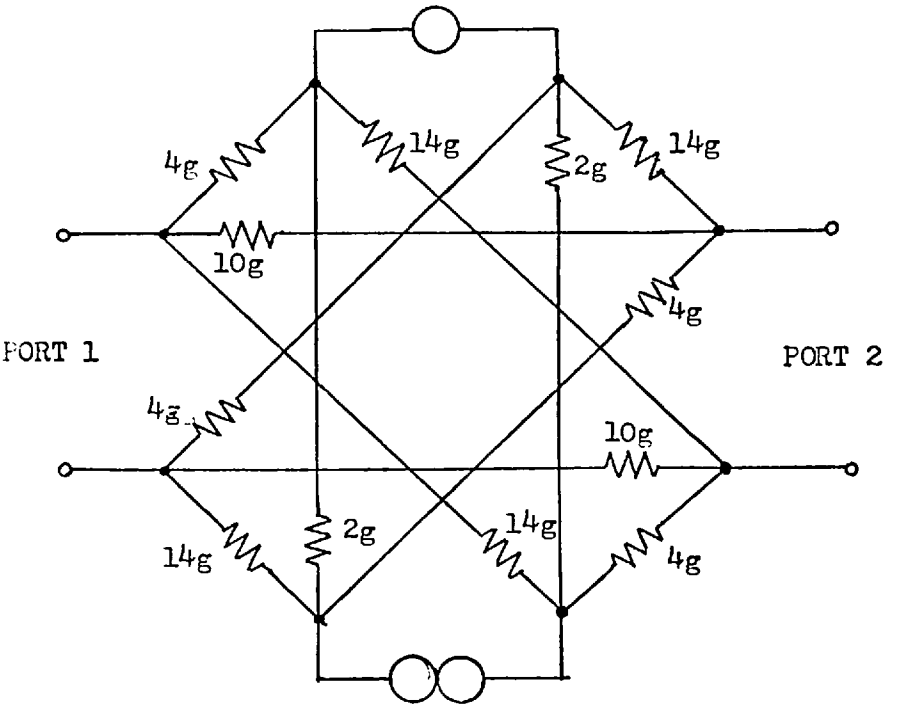


Fig. 7-11 : A positive inverter of type E.

one transistor, i.e. inverters of type E, is an interesting question which remains unsolved; however, some comments on this question will be made.

7.3 - THE ADMITTANCE PARAMETERS OF A GROUNDED 2-PORT CONTAINING RESISTORS AND ONE OPERATIONAL AMPLIFIER

In this section it will be proved that the admittance parameters of a grounded 2-port containing resistors and one operational amplifier are subject to the following constraints:

$$\text{if} \quad y_{11} = 0 \quad \text{then} \quad y_{21} \leqslant 0 \qquad (7\text{-}1a)$$

$$\text{if} \quad y_{22} = 0 \quad \text{then} \quad y_{12} \leqslant 0 \qquad (7\text{-}1b)$$

The results expressed by (7-1) have various consequences regarding the realization of inverters with operational amplifiers. These consequences will be examined in the next section.

Fig. 7-12 shows the general configuration of a 2-port consisting of resistors and one nullor, with both ports grounded and realizable with one operational amplifier with differential input and grounded output.

If the resistive 6-terminal network contains more than 6 nodes, then star-mesh transformations [99, p.131] applied to the internal nodes will transform the network into an equivalent network with only 6 nodes and positive resistors. In this equivalent network, the conductance of the resistor between nodes i and j will be denoted by g_{ij}, and the sum of the conductances of the resistors connected to node i by g_{ii}:

$$g_{ii} = \sum_{j=0}^{5} g_{ij} \qquad (i \neq j) \qquad (7\text{-}2)$$

In view of the meaning of g_{ij} it is clear that

$$g_{ij} = g_{ji}$$

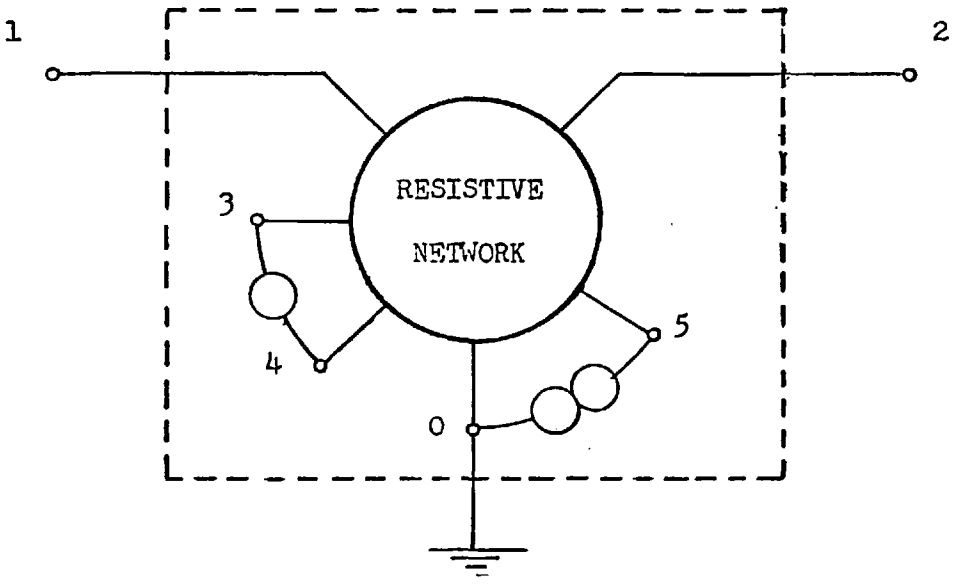


Fig. 7-12 : Grounded 2-port realizable with one operational amplifier.

and that

$$g_{ij} \geq 0$$

Since g_{34} and g_{50} refer to the resistors in parallel with the nullator and the norator, they can be assumed to be zero without loss of generality.

It should be noted that $g_{ii} \neq 0$ (for all i) since otherwise the corresponding terminal would not be connected to the resistive network (Fig. 7-12).

The indefinite admittance description of the resistive network is (assuming that $g_{34} = 0$ and $g_{50} = 0$):

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_0 \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} & -g_{13} & -g_{14} & -g_{15} & -g_{10} \\ -g_{12} & g_{22} & -g_{23} & -g_{24} & -g_{25} & -g_{20} \\ -g_{13} & -g_{23} & g_{33} & 0 & -g_{35} & -g_{30} \\ -g_{14} & -g_{24} & 0 & g_{44} & -g_{45} & -g_{40} \\ -g_{15} & -g_{25} & -g_{35} & -g_{45} & g_{55} & 0 \\ -g_{10} & -g_{20} & -g_{30} & -g_{40} & 0 & g_{00} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_0 \end{bmatrix} \qquad (7\text{-}3)$$

Taking into account the nullator and the norator

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5+i_0 \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} & -(g_{13}+g_{14}) & -g_{15} & -g_{10} \\ -g_{12} & g_{22} & -(g_{23}+g_{24}) & -g_{25} & -g_{20} \\ -g_{13} & -g_{23} & g_{33} & -g_{35} & -g_{30} \\ -g_{14} & -g_{24} & g_{44} & -g_{45} & -g_{40} \\ -(g_{15}+g_{10}) & -(g_{25}+g_{20}) & -(g_{35}+g_{45}+g_{30}+g_{40}) & g_{55} & g_{00} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_5 \\ v_0 \end{bmatrix} \qquad (7\text{-}4)$$

(the matrix in this equation is obtained from the matrix in (7-3) by adding columns 3 and 4 and by adding rows 5 and 0). Making

$i_3 = i_4 = i_5 = 0$ and taking terminal 0 as the reference, equation (7-4) yields:

$$\begin{bmatrix} i_1 \\ i_2 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} & -(g_{13}+g_{14}) & -g_{15} \\ -g_{12} & g_{22} & -(g_{23}+g_{24}) & -g_{25} \\ -g_{13} & -g_{23} & g_{33} & -g_{35} \\ -g_{14} & -g_{24} & g_{44} & -g_{45} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_5 \end{bmatrix} \qquad (7\text{-}5)$$

The admittance matrix describing the 3-terminal network (terminals 1, 2, and 0) that remains after the connection of the nullator and norator

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

can be obtained from (7-5) by elimination of v_3 and v_5:

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} \\ -g_{12} & g_{22} \end{bmatrix} - \begin{bmatrix} -(g_{13}+g_{14}) & -g_{15} \\ -(g_{23}+g_{24}) & -g_{25} \end{bmatrix} \begin{bmatrix} g_{33} & -g_{35} \\ g_{44} & -g_{45} \end{bmatrix}^{-1} \begin{bmatrix} -g_{13} & -g_{23} \\ -g_{14} & -g_{24} \end{bmatrix}$$

This leads to the following expressions for the admittance parameters of the 3-terminal network:

$$y_{11} = g_{11} - (g_{13} + g_{14}) \frac{\alpha}{\lambda} - g_{15} \frac{\beta}{\lambda} \qquad (7\text{-}6a)$$

$$y_{12} = -g_{12} - (g_{13} + g_{14}) \frac{\gamma}{\lambda} - g_{15} \frac{\delta}{\lambda} \qquad (7\text{-}6b)$$

$$y_{21} = -g_{12} - (g_{23} + g_{24}) \frac{\alpha}{\lambda} - g_{25} \frac{\beta}{\lambda} \qquad (7\text{-}6c)$$

$$y_{22} = g_{22} - (g_{23} + g_{24}) \frac{\gamma}{\lambda} - g_{25} \frac{\delta}{\lambda} \qquad (7\text{-}6d)$$

$$\lambda = g_{44}\, g_{35} - g_{33}\, g_{45}$$

$$\alpha = g_{14}\, g_{35} - g_{13}\, g_{45} \qquad \gamma = g_{24}\, g_{35} - g_{23}\, g_{45}$$

$$\beta = g_{14}\, g_{33} - g_{13}\, g_{44} \qquad \delta = g_{24}\, g_{33} - g_{23}\, g_{44}$$

It will now be shown that the admittance parameters given by (7-6) are subject to the constraints (7-1a) and (7-1b) for any choice of the values of the conductances in the network. It will first be assumed that all conductances are finite. The degenerate cases, where one or more resistors are replaced by short circuits, will be considered afterwards. The proof will be presented separately for the three cases: (1) $\lambda = 0$, (2) $\lambda > 0$, (3) $\lambda < 0$.

(1) $\lambda = 0$

It will be shown that, in this case, $y_{12} \leq 0$ and $y_{21} \leq 0$ (in this case it is not necessary to consider $y_{11} = 0$ or $y_{22} = 0$).

As $g_{33} \neq 0$ and $g_{44} \neq 0$ the last two equations in (7-5) can be written as:

$$v_3 = (g_{13}/g_{33})\, v_1 + (g_{23}/g_{33})\, v_2 + (g_{35}/g_{33})\, v_5 \qquad (7\text{-}7a)$$

$$v_3 = (g_{14}/g_{44})\, v_1 + (g_{24}/g_{44})\, v_2 + (g_{45}/g_{44})\, v_5 \qquad (7\text{-}7b)$$

For $\lambda = 0$ ($g_{35}/g_{33} = g_{45}/g_{44}$), these equations lead to

$$(g_{13}/g_{33} - g_{14}/g_{44})\, v_1 + (g_{23}/g_{33} - g_{24}/g_{44})\, v_2 = 0 \qquad (7\text{-}8)$$

Since in a 2-port with an admittance description the voltages at both ports can be freely chosen, it follows from (7-8) that $g_{13}/g_{33} - g_{14}/g_{44} = 0$ and $g_{23}/g_{33} - g_{24}/g_{44} = 0$. In this case equations (7-7) are not independent and therefore v_5 cannot be eliminated. Substituting (7-7a) in the first 2 equations of (7-5), and denoting $g_a = g_{13} + g_{14}$ and $g_b = g_{23} + g_{24}$, yields:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} g_{11} - g_a \frac{g_{13}}{g_{33}} & -g_{12} - g_a \frac{g_{23}}{g_{33}} & -g_{15} - g_a \frac{g_{35}}{g_{33}} \\ -g_{12} - g_b \frac{g_{13}}{g_{33}} & g_{22} - g_b \frac{g_{23}}{g_{33}} & -g_{25} - g_b \frac{g_{35}}{g_{33}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_5 \end{bmatrix} \qquad (7\text{-}9)$$

Since in a 2-port described by an admittance matrix i_1 and i_2 are uniquely determined by v_1 and v_2, the 3rd column in the matrix in (7-9) must be zero. The remaining elements of the matrix are the admittance parameters and it is clear that $y_{12} \leqslant 0$ and $y_{21} \leqslant 0$, since all $g_{ij} \geqslant 0$.

(2) $\lambda > 0$

It will be shown that $y_{21} > 0$ is incompatible with $y_{11} = 0$. Since y_{12} and y_{22} only differ from y_{21} and y_{11} by an interchange of the numbering of terminals 1 and 2, it follows that $y_{12} > 0$ is incompatible with $y_{22} = 0$.

Equation (7-6c) shows that, when $\lambda > 0$, in order to make y_{21} positive, either α or β must be negative. These two cases, (2a) $\alpha < 0$ and (2b) $\beta < 0$ will be examined separately.

(2a) $\alpha < 0$. Equation (7-6a) shows that, when $\lambda > 0$ and $\alpha < 0$, it is required for $y_{11} = 0$ (note that $g_{11} \neq 0$) that $\beta > 0$, i.e.,

$$g_{14} > g_{13}\, g_{44}/g_{33}$$

This inequality, in conjunction with the condition for $\alpha < 0$,

$$g_{13}\, g_{45} > g_{14}\, g_{35}$$

leads to

$$g_{13}\, g_{45} > g_{13}\, g_{35}\, g_{44}/g_{33}$$

but this is incompatible with $\lambda > 0$ ($g_{45} < g_{35}\, g_{44}/g_{33}$).

(2b) $\beta < 0$. When $\lambda > 0$ and $\beta < 0$, equation (7-6a) shows that for $y_{11} = 0$ (note that $g_{11} \geqslant g_{13} + g_{14}$ and $g_{11} \neq 0$) it is required that $\lambda \leqslant \alpha$, and, hence

$$g_{35}\,(g_{44} - g_{14}) \leqslant g_{45}\,(g_{33} - g_{13})$$

This inequality and the condition for $\lambda > 0$,

$$g_{45} < g_{35}\ g_{44}/g_{33}$$

leads to

$$g_{35}\ (g_{44} - g_{14}) < g_{35}\ (g_{44} - g_{13}\ g_{44}/g_{33})$$

which can be simplified to

$$g_{14} > g_{13}\ g_{44}/g_{33}$$

This result is incompatible with the assumption that $\beta < 0$ $(g_{14} < g_{13}\ g_{44}/g_{33})$.

(3) $\lambda < 0$

As in case (2) it will be shown that $y_{21} > 0$ is incompatible with $y_{11} = 0$. As explained before, this implies that it is also true that $y_{12} > 0$ is incompatible with $y_{22} = 0$.

It will be shown first that, in the present case ($\lambda < 0$), $y_{11} = 0$ requires that $\alpha \leq 0$. From equation (7-6a) it follows that, if $\lambda < 0$ and $\alpha > 0$, then $y_{11} = 0$ requires that $\beta < 0$, i.e.,

$$g_{13} > g_{14}\ g_{33}/g_{44}$$

This, in conjunction with the assumption that $\alpha > 0$, i.e.,

$$g_{14}\ g_{35} > g_{13}\ g_{45}$$

leads to

$$g_{14}\ g_{35} > g_{14}\ g_{33}\ g_{45}/g_{44}$$

Since this result is incompatible with the condition for $\lambda < 0$,

$$g_{35} < g_{45}\ g_{33}/g_{44}$$

it follows that the assumption $\alpha > 0$ must be rejected, i.e., $\alpha \leq 0$.

If $\alpha \leq 0$ and $\lambda < 0$, equation (7-6c) shows that $y_{21} > 0$ requires that $\beta > 0$. In order to have $y_{11} = 0$ (see equation (7-6a)) it is required that $|\lambda| \leq |\alpha|$, and hence,

$$g_{45}\ (g_{33} - g_{13}) \leq g_{35}\ (g_{44} - g_{14})$$

This, together with the condition for $\lambda < 0$,

$$g_{35} < g_{45}\ g_{33}/g_{44}$$

leads to

$$g_{45}\ (g_{33} - g_{13}) < g_{45}\ (g_{33} - g_{14}\ g_{33}/g_{44})$$

This last inequality can be simplified to

$$g_{13} > g_{14}\ g_{33}/g_{44}$$

but this is incompatible with the condition for $\beta > 0$ $(g_{13} < g_{14}\ g_{33}/g_{44})$.

Thus, it has been shown that, as long as the conductances are finite, the conditions expressed by (7-1a) and (7-1b) are satisfied by the admittance parameters of the 2-port of Fig. 7-12. The degenerate cases where one or more resistors are replaced by short circuits will now be examined. It is convenient to list the conductances of all the resistors in the network:

$$\begin{array}{ccccc} g_{12} & & & & \\ g_{13} & g_{23} & & & \\ g_{14} & g_{24} & g_{34} = 0 & & \\ g_{15} & g_{25} & g_{35} & g_{45} & \\ g_{10} & g_{20} & g_{36} & g_{40} & g_{50} = 0 \end{array}$$

If, in the network of Fig. 6-12, one of the conductances g_{12}, g_{15}, g_{10}, g_{25} and g_{20} is replaced by a short-circuit the 2-port will not have an admittance description. In the cases of g_{10} and g_{20}, one of the

ports would be short-circuited. In the case of g_{12}, the two ports would be directly connected and therefore $v_1 = v_2$. In the cases of g_{15} or g_{25}, the norator would be connected across one of the ports, and this means that the current at that port would be indeterminate.

As to the remaining conductances g_{13}, g_{14}, g_{23}, g_{24}, g_{35}, g_{30}, g_{45} and g_{40}, it is sufficient to examine the cases where g_{13}, g_{35} or g_{30} are replaced by short circuits, since all the other cases only differ from these by a different numbering of the terminals. The expressions of the admittance parameters in terms of the conductances can be obtained, in those cases that have to be examined, either by taking the limit of (7-6) when the relevant conductance tends towards infinity or, alternatively, by derivation from the admittance matrix of the resistive network (in the same way as (7-6) was derived from (7-3)). In the following only the results will be given, since the derivation using either of these methods is straightforward.

If g_{13} is replaced by a short-circuit, then y_{21} and y_{22} become

$$y_{21} = -g_{12} - g_{23} - g_{24} - g_{25}\,(g_{44} - g_{14})/g_{45}$$

and

$$y_{22} = g_{22} + g_{25}\,g_{24}/g_{45}$$

Since $g_{44} \geq g_{14}$, y_{21} cannot be positive (irrespective of the value of y_{11}). As $y_{22} = 0$ is not possible ($g_{22} > 0$) it is not necessary to examine y_{12}.

When g_{35} is replaced by a short-circuit, then

$$y_{12} = -g_{12} - g_{24}\,(g_{13} + g_{14} + g_{15})/(g_{40} + g_{14} + g_{24})$$

$$y_{21} = -g_{12} - g_{14}\,(g_{23} + g_{24} + g_{25})/(g_{40} + g_{14} + g_{24})$$

This shows that $y_{12} \leq 0$ and $y_{21} \leq 0$ (irrespective of the values of y_{11} and y_{22}).

Finally if g_{30} is replaced by a short circuit,

$$y_{11} = g_{11} + g_{15}\, g_{14}/g_{45}$$

and

$$y_{22} = g_{22} + g_{25}\, g_{24}/g_{45}$$

These equations show that $y_{11} \neq 0$ and $y_{22} \neq 0$ and therefore it is not necessary to examine y_{21} and y_{12}.

This completes the proof.

7.4 - ON THE REALIZATION OF VARIOUS TYPES OF INVERTERS USING OPERATIONAL AMPLIFIERS

An immediate consequence of the result proved in the previous section, (7-1), is that grounded positive inverters cannot be realized with only one operational amplifier (in a positive inverter $y_{11} = y_{22} = 0$ and y_{12} and y_{21} have opposite signs). Thus, positive inverters of type A (see Fig. 7-10) are not possible.

Another consequence of (7-1) concerns the realization of negative inverters with resistors and operational amplifiers. A negative inverter has an admittance description of the form

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 0 & y_{12} \\ y_{21} & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

where y_{12} and y_{21} are real constants with the same sign. The constraints (7-1) show that it is impossible to realize a grounded negative inverter with only one operational amplifier if y_{12} and y_{21} are positive. Such an inverter can be realized with two operational amplifiers, as shown by the circuit of Fig. 3-12d with the negative resistors realized

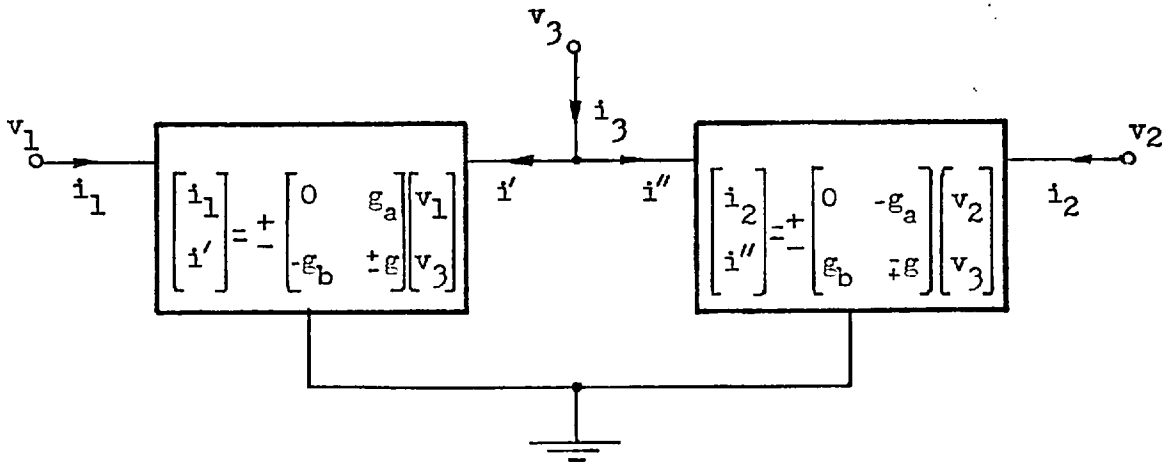
by the circuit of Fig. 3-11 (see chapter 3, section 3.4). A grounded negative inverter can be realized with one amplifier if y_{12} and y_{21} are negative; an example is the circuit of Fig. 3-12a.

The result expressed by (7-1) can also be used in connection with the realization of 3-port admittance inverters for floating inductance simulation. One way of realizing such 3-port inverters uses two grounded 2-ports connected as shown in Fig. 7-13a. Although the type of connection is the same as used in the case of the realization with two grounded inverters (Fig. 6-3), the grounded 2-ports in Fig. 7-13a do not have to be inverters: they can have the description shown in the figure. When g = 0 the 2-ports in Fig. 7-13a become inverters and the circuit in Fig. 7-13a coincides with the circuit in Fig. 6-3.

It can be seen, by inspection of the 2-port descriptions in Fig. 7-13a, that one of the 2-ports must violate the constraints expressed by (7-1) and cannot therefore be realized with only one operational amplifier. The configuration shown in Fig. 7-13a cannot thus lead to a 3-port inverter with two amplifiers. It can, however, be realized with 3 amplifiers, as shown by the circuit in Fig. 7-13b, which is one of the 3-nullor circuits derived in chapter 6 (section 6.8, Fig. 6-15b).

Whether or not a 3-port inverter for floating inductor simulation can be realized with two amplifiers is an unsolved question. The above discussion shows that a 2-amplifier realization cannot be achieved by using the configuration shown in Fig. 7-13a. It is possible, however, that some other method may lead to 3-port inverters for floating inductance simulation with only two operational amplifiers.

(a)

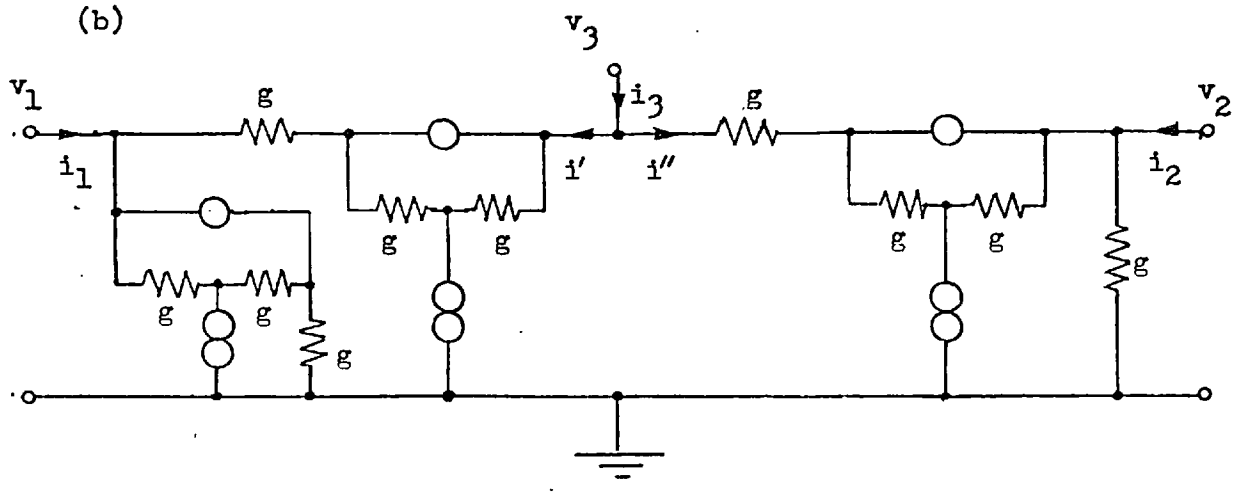


$g_a > 0 \; ; \quad g_b > 0$

$g \geq 0$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \pm \begin{bmatrix} 0 & 0 & g_a \\ 0 & 0 & -g_a \\ -g_b & g_b & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

(b)



$$\begin{bmatrix} i_1 \\ i' \end{bmatrix} = \begin{bmatrix} 0 & -g \\ g & -g \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \end{bmatrix}$$

$$\begin{bmatrix} i_2 \\ i'' \end{bmatrix} = \begin{bmatrix} 0 & g \\ -g & g \end{bmatrix} \begin{bmatrix} v_2 \\ v_3 \end{bmatrix}$$

Fig. 7-13 : Realization of a 3-port admittance inverter for floating inductor simulation.

7.5 - ON THE REALIZATION OF POSITIVE INVERTERS USING TRANSISTORS

In this section it will be shown that it is impossible to realize a grounded positive inverter using only one transistor (this is an inverter of type B, in terms of the chart in Fig. 7-10). The realizability of a positive inverter with one transistor, when the requirement of grounded ports is removed (type G in Fig. 7-10) will also be examined; however, this last question will remain unsolved.

Proof of the non-realizability of grounded positive inverters with one transistor.

A grounded 2-port, consisting of resistors and one nullor, and realizable with one transistor, must have the general configuration shown in Fig. 7-14 (note that the nullator and the norator have a terminal in common as required for a transistor realization).

The resistive network in Fig. 7-14 has an equivalent circuit with 6 nodes and positive resistors. Their conductances will be denoted by g_{ij}, as in section 7.3. As g_{35} and g_{45} are in parallel with the nullator and the norator, they will be assumed to be zero without loss of generality. As before, g_{ii} denotes the sum of the conductances of all the resistors connected to node i. It is assumed that all $g_{ii} > 0$, since $g_{ii} = 0$ would mean that node i is not connected to the resistive network.

The definite nodal admittance description of the resistive network, with terminal 0 as reference, is:

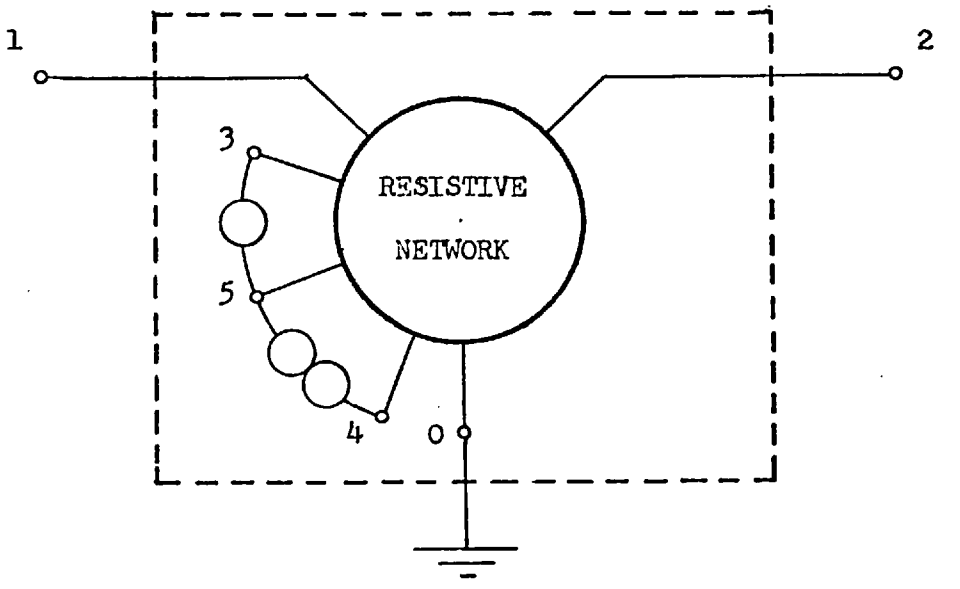


Fig. 7-14 : Grounded 2-port realizable with one ideal transistor.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} & -g_{13} & -g_{14} & -g_{15} \\ -g_{12} & g_{22} & -g_{23} & -g_{24} & -g_{25} \\ -g_{13} & -g_{23} & g_{33} & -g_{34} & 0 \\ -g_{14} & -g_{24} & -g_{34} & g_{44} & 0 \\ -g_{15} & -g_{25} & 0 & 0 & g_{55} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} \qquad (7\text{-}10)$$

By taking into account the presence of the nullator and norator, the admittance description becomes:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4+i_5 \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} & -(g_{13}+g_{15}) & -g_{14} \\ -g_{12} & g_{22} & -(g_{23}+g_{25}) & -g_{24} \\ -g_{13} & -g_{23} & g_{33} & -g_{34} \\ -(g_{14}+g_{15}) & -(g_{24}+g_{25}) & -g_{34}+g_{55} & g_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \qquad (7\text{-}11)$$

If terminals 3, 4 and 5 are rendered inaccessible ($i_3 = i_4 = i_5 = 0$) the admittance matrix of the remaining 3-terminal network can be obtained as follows:

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} & -g_{12} \\ -g_{12} & g_{22} \end{bmatrix} - \begin{bmatrix} -(g_{13}+g_{15}) & -g_{14} \\ -(g_{23}+g_{25}) & -g_{24} \end{bmatrix} \begin{bmatrix} g_{33} & -g_{34} \\ -g_{34}+g_{55} & g_{44} \end{bmatrix}^{-1} \begin{bmatrix} -g_{13} & -g_{23} \\ -(g_{14}+g_{15}) & -(g_{24}+g_{25}) \end{bmatrix}$$

The result is:

$$y_{11} = g_{11} - (g_{13} + g_{15}) \frac{\alpha'}{\lambda'} - g_{14} \frac{\beta'}{\lambda'} \qquad (7\text{-}12a)$$

$$y_{12} = -g_{12} - (g_{13} + g_{15}) \frac{\gamma'}{\lambda'} - g_{14} \frac{\delta'}{\lambda'} \qquad (7\text{-}12b)$$

$$y_{21} = -g_{21} - (g_{23} + g_{25}) \frac{\alpha'}{\lambda'} - g_{24} \frac{\beta'}{\lambda'} \qquad (7\text{-}12c)$$

$$y_{22} = g_{22} - (g_{23} + g_{25}) \frac{\gamma'}{\lambda'} - g_{24} \frac{\delta'}{\lambda'} \qquad (7\text{-}12d)$$

where

$$\lambda' = g_{33}\, g_{44} + g_{34}\,(g_{55} - g_{34})$$

$$\alpha' = g_{13}\, g_{44} + g_{34}\,(g_{14} + g_{15})$$

$$\beta' = g_{13}\, g_{34} + g_{33}\,(g_{14} + g_{15}) - g_{13}\, g_{55}$$

$$\gamma' = g_{23}\, g_{44} + g_{34}\,(g_{24} + g_{25})$$

$$\delta' = g_{23}\, g_{34} + g_{33}\,(g_{24} + g_{25}) - g_{23}\, g_{55}$$

The above equations show immediately that $\alpha' \geq 0$ and $\gamma' \geq 0$. Taking into account that

$$g_{ii} = \sum_{j=0}^{5} g_{ij} \qquad (j \neq i)$$

it is easy to verify that

$$\lambda' \geq \alpha' + \gamma' \tag{7-13}$$

and therefore $\lambda' \geq 0$. It will now be shown that λ' cannot be zero and therefore is always positive. The expression of λ' in terms of the conductances can be written as

$$\lambda' = (g_{33}\, g_{44} - g_{34}^2) + g_{34}\, g_{55}$$

Since $g_{33} \geq g_{34}$, $g_{44} \geq g_{34}$ and $g_{55} > 0$ it follows that $\lambda' = 0$ can only be obtained if $g_{34} = 0$. But even with $g_{34} = 0$, λ' cannot be zero, since $g_{34} = 0$ means that $\lambda' = g_{33}\, g_{44}$ and neither g_{33} nor g_{44} can be zero.

It will now be shown that the 2-port of Fig. 7-14 cannot be a positive inverter for any choice of the values of the conductances.

The case where all the conductances are finite will be considered first, and it will be shown that if $y_{11} = 0$ and $y_{21} > 0$ then $y_{12} = 0$. Since y_{22} and y_{21} only differ from y_{11} and y_{12} by an interchange of the numbering of terminals 1 and 2, it follows that if $y_{22} = 0$ and $y_{12} > 0$

then $y_{21} = 0$. As a consequence the 2-port of Fig. 7-14 cannot have $y_{11} = y_{22} = 0$ and y_{12} and y_{21} with opposite signs, as required by a positive inverter.

Taking into account that, as mentioned above, $\lambda' > 0$ and $\alpha' \geq 0$, equation (7-12c) shows that $y_{21} > 0$ requires $\beta' < 0$. Since $g_{11} \geq g_{13} + g_{15}$, equation (7-12a) shows that $y_{11} = 0$ requires $\alpha' \geq \lambda'$. Taking into account (7-13), i.e. $\lambda' \geq \alpha' + \gamma'$, it follows that

$$\alpha' = \lambda'$$

which means that

$$\gamma' = 0$$

Equation (7-12a) shows that with $\alpha' = \lambda'$, $y_{11} = 0$ requires $g_{11} = g_{13} + g_{15}$, which means that g_{13} and g_{15} are the only non-zero conductances connected to terminal 1, and therefore

$$g_{12} = 0 \quad \text{and} \quad g_{14} = 0$$

These last two equations, together with $\gamma' = 0$, when used in (7-12b) show that $y_{12} = 0$.

The case where one or more resistors are replaced by short-circuits will now be considered. The list of all resistors, denoted by their conductances, is:

g_{12}

g_{13} g_{23}

g_{14} g_{24} g_{34}

g_{15} g_{25} $g_{35}=0$ $g_{45}=0$

g_{10} g_{20} g_{30} g_{40} g_{50}

If one of the conductances g_{12}, g_{10} or g_{20} is replaced by a short-circuit, the 2-port does not have an admittance description.

The replacement of g_{34} by a short-circuit leads to the nullator being in parallel with the norator, and a parallel combination of a nullator and a norator is equivalent to a short-circuit.

If either g_{40} or g_{50} is short-circuited, the norator is connected to the ground terminal 0 and the resulting circuits are special cases of the circuit in Fig. 7-12, which, as proved in the previous section, cannot be a positive inverter.

As to the remaining conductances, only the cases of g_{15}, g_{13}, g_{14} and g_{30} have to be considered, since for g_{23}, g_{24} and g_{25} the circuits obtained only differ from the previous ones by the numbering of the terminals.

If g_{15} is replaced by a short-circuit, then

$$y_{22} = g_{22} + g_{23}\, g_{24}/g_{34}$$

and this shows that $y_{22} \neq 0$.

If g_{13} is replaced by a short circuit, then

$$y_{12} = -(g_{12} + g_{23}) - (g_{24} + g_{25})\,(g_{14} + g_{34})/g_{44}$$

$$y_{22} = g_{22} - (g_{24} + g_{25})\, g_{24}/g_{44}$$

Since $g_{44} \geq g_{24}$ and $g_{22} \geq g_{24} + g_{25}$, $y_{22} = 0$ requires that $g_{44} = g_{24}$ and $g_{22} = g_{24} + g_{25}$. This means that $g_{14} + g_{34} = 0$ and $g_{12} + g_{23} = 0$, and therefore $y_{12} = 0$. This argument is not invalidated by the possibility of g_{24} or g_{25} becoming infinite (in addition to g_{13}). Even when g_{24} becomes infinite $g_{24}/g_{44} = 1$; the case of g_{25} not being finite has already been rejected (if a positive inverter is not possible for infinite g_{15} it is also not possible for infinite g_{25}).

If g_{14} is replaced by a short-circuit, then

$$y_{21} = -(g_{12} + g_{24}) - (g_{23} + g_{25})(g_{13} + g_{34})/g_{33}$$

$$y_{22} = g_{22} - (g_{23} + g_{25})\, g_{23}/g_{33}$$

and an argument similar to the previous one shows that if $y_{22} = 0$, then $y_{21} = 0$.

Finally, when g_{30} is replaced by a short circuit, then

$$y_{12} = -g_{12} - g_{14}(g_{24} + g_{25})/g_{44}$$

$$y_{21} = -g_{12} - g_{24}(g_{14} + g_{15})/g_{44}$$

This shows that y_{12} and y_{21} cannot have opposite signs.

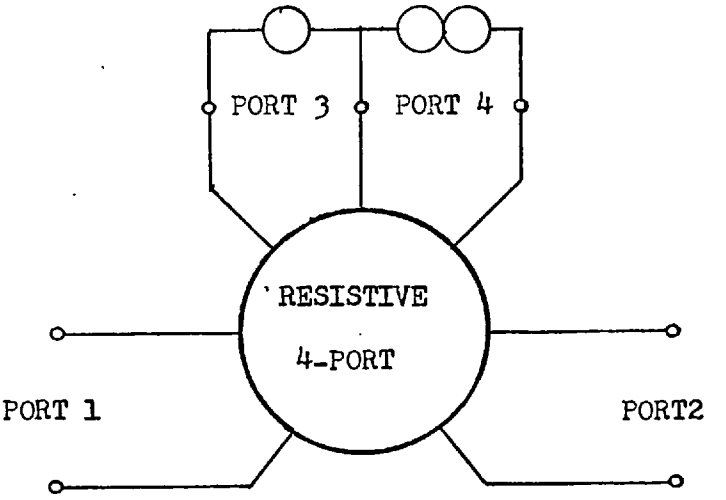
As all possible cases have been considered and rejected, the proof is now complete.

An unsolved question

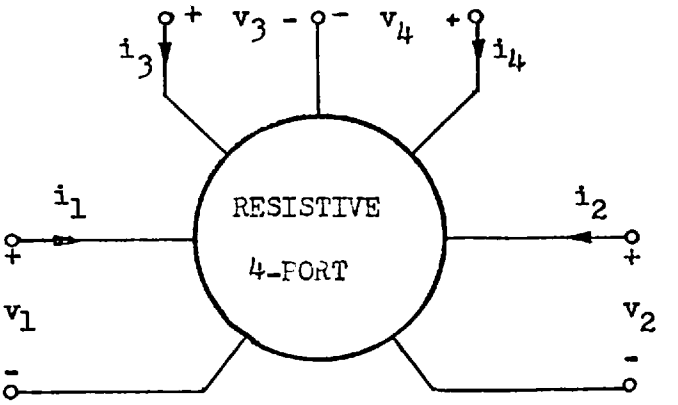
It has just been shown that a positive inverter cannot be realized with only one transistor if the two ports have a common terminal. It may be possible, however, to realize a positive inverter with only one transistor if the requirement of a common terminal for both ports is abandoned. Such a positive inverter corresponds to type G, in terms of the chart in Fig. 7-10; this is the only type in the chart for which neither an example nor a proof of impossibility have been found.

Although the investigation of the realizability of 1-transistor gyrators has not led to a conclusion, some brief comments on this question will now be presented.

A 2-port containing resistors and an ideal transistor modelled by a nullor, must have the general configuration shown in Fig. 7-15a. If the nullor is extracted, the resistor 4-port of Fig. 7-15b is obtained.



(a)



(b)

Fig. 7-15 : Connection of one ideal transistor to a resistive 4-port.

It will be assumed that this 4-port has an admittance description,

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} \\ g_{12} & g_{22} & g_{23} & g_{24} \\ g_{13} & g_{23} & g_{33} & g_{34} \\ g_{14} & g_{24} & g_{34} & g_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \qquad (7\text{-}14)$$

It should be noted that the g_{ij} $(i \neq j)$ in this matrix are not conductances of individual resistors as in sections 7.3 and 7.4; they may thus be positive or negative. Since ports 3 and 4 have a common terminal, g_{34} is negative (for the reference directions of voltages and currents in Fig. 7-15b).

The admittance parameters of the 2-port obtained by connecting a nullor to ports 3 and 4 (Fig. 7-15a) are obtained from (7-14) by taking into account the nullor constraints, $i_3 = 0$ and $v_3 = 0$. The result is

$$y_{11} = g_{11} - g_{13}\, g_{14}/g_{34} \qquad (7\text{-}15a)$$

$$y_{12} = g_{12} - g_{14}\, g_{23}/g_{34} \qquad (7\text{-}15b)$$

$$y_{21} = g_{21} - g_{13}\, g_{24}/g_{34} \qquad (7\text{-}15c)$$

$$y_{22} = g_{22} - g_{23}\, g_{24}/g_{34} \qquad (7\text{-}15d)$$

For the 2-port of Fig. 7-15a to be a positive inverter it is required that $y_{11} = 0$, $y_{22} = 0$ and that y_{12} and y_{21} have opposite signs. This can be achieved, for example, by choosing the values of g_{ij} as

$$\begin{bmatrix} 14 & -5 & 2 & -7 \\ -5 & 14 & -7 & 2 \\ 2 & -7 & 10 & -1 \\ -7 & 2 & -1 & 10 \end{bmatrix}$$

It is seen, by inspection, that this matrix is dominant; therefore it

is also paramount since any dominant matrix is paramount (the definitions of dominant and paramount matrices can be found in chapter 2, section 2.3). Since paramountcy is a necessary condition for a matrix to be realizable as the admittance matrix of a resistive multiport, it might be possible to realize the admittance matrix in the example by a resistor 4-port with the port structure shown in Fig. 7-15b. However, as far as the author knows, conditions which are both necessary and sufficient for a matrix to be realizable as the admittance matrix of a resistive 4-port with the port structure of Fig. 7-15b are not known and a synthesis procedure applicable to this case is not available.

Although this investigation remained inconclusive it is thought that the above discussion is useful since it shows that the necessary paramountcy condition can be satisfied by the matrix in equation (7-14), when the requirements for the 2-port of Fig. 7-15a to be a positive inverter are imposed.

7.7 - CONCLUSIONS

In this chapter it has been proved that in a grounded 2-port containing resistors and one operational amplifier (with differential input and grounded output) the admittance parameters are such that if $y_{11} = 0$ then $y_{21} \leqslant 0$ and if $y_{22} = 0$ then $y_{12} \leqslant 0$. This result has several consequences concerning the realization of inverters using operational amplifiers:

(a) It is not possible to realize a grounded positive inverter with only one operational amplifier (although positive inverters with one amplifier are possible if only one port is grounded).

(b) It is not possible to realize a grounded negative inverter with positive y_{12} and y_{21} using only one operational amplifier. (It is possible to employ only one amplifier if y_{12} and y_{21} are negative.)

(c) The method of realizing a 3-port admittance inverter for floating inductor simulation using two grounded 2-ports connected as shown in Fig. 7-13a (which includes, as a special case, the use of two grounded positive inverters, Fig. 6-3) requires more than two operational amplifiers.

It has also been proved that a grounded positive inverter cannot be realized with only one ideal transistor. The possibility of realizing single-transistor positive inverters without the restriction that both ports must be grounded, is an interesting question that remains unanswered.

CHAPTER 8

A SET OF NETWORK PROPERTIES RELATED TO THE CONCEPT OF RECIPROCITY

8.1 - INTRODUCTION

Immittance converters and inverters have a close association with reciprocity and non-reciprocity (i.e., the absence of reciprocity). Some types of converters and inverters are usually regarded as typical examples of non-reciprocal networks. The gyrator has played an important part in the clarification of the relationship between reciprocity-nonreciprocity and passivity-activity. Before the introduction of the gyrator concept by Tellegen [72], reciprocity was often assumed to be a necessary accompaniment of passivity. Since then it has become well known that this is not true as demonstrated by the fact that the gyrator is both passive and non-reciprocal.

Several authors have used the concept of anti-reciprocity as a kind of extreme non-reciprocity. A search of the literature reveals that two different definitions of anti-reciprocity have been in use. The only common feature of the two definitions is the fact that both include the gyrator; apart from this, they are quite distinct. Surprisingly, the incompatibility of the two definitions appears to have remained unnoticed until now.

The examination of the two definitions of anti-reciprocity shows that one of them is given for multiports and permits the establishment of an anti-reciprocity theorem which closely resembles the reciprocity theorem. However, it will be shown that, according to this definition,

there are only two types of anti-reciprocal 2-ports (these are the gyrator and the ideal transformer, if non-reactive 2-ports are considered) and all anti-reciprocal multiports are equivalent to an interconnection of these 2-ports. This severely restricts the usefulness of the anti-reciprocity theorem, since it only applies to a very limited class of networks. Furthermore it seems somewhat strange that this definition is satisfied by the transformer which is usually regarded as typically reciprocal, in contrast to the non-reciprocal gyrator.

The other definition of anti-reciprocity has been given in the literature only for 2-ports, but it applies to a larger set of 2-ports than the previous one and leads to several interesting properties regarding the cascade connection of 2-ports.

Clearly the existence of two incompatible definitions for anti-reciprocity requires clarification. This was the motivation for the investigation that led to the results reported in the present chapter.

The designation anti-reciprocity will, in this thesis, be associated with the definition given in terms of multiports. The other 'anti-reciprocity', defined in terms of 2-ports, will be renamed 'bireciprocity' (there is some justification for this choice of designations, as will be seen later).

The definition of bireciprocity, so far restricted to 2-ports, will be extended to multiports. It is believed that this extension is not a trivial one and might, to some extent, be regarded as the introduction of a new fundamental network property related to the concept of reciprocity.

A comparison of reciprocity (R), anti-reciprocity (AR) and bi-reciprocity (B) will lead to the introduction of a fourth network property, which will be named anti-bireciprocity (AB), in order to produce a 'complete pattern'. A 'complete' set, R4, of four network

properties, R4 = $\{R, B, AR, AB\}$, is thus created, in which AB is related to AR in the same way as B is related to R.

The meaning of the four properties forming the set R4 and the relationships between them will be examined in detail. Various rules concerning the interconnection of multiports which possess properties belonging to R4 will be derived.

It will be shown that the multiports that possess simultaneously two of the properties belonging to the set R4 are special cases of the multiport converters and inverters with which this thesis has been concerned in the previous chapters.

A note on the value of the determinant of the transmission matrix of (n+n)-ports possessing a property belonging to the set R4 and a reference to the relationship of the four properties with activity and passivity will also be included.

8.2 - RECIPROCITY

In this section the concept of reciprocity will be reviewed with the aim of establishing the background for the study of anti-reciprocity in the following sections.

The definition of reciprocity has already been considered in chapter 2. A linear, time invariant multiport is <u>reciprocal</u> if the currents and voltages, $\{I,V\}$ and $\{\hat{I},\hat{V}\}$, corresponding to any two possible excitations, satisfy the equation

$$I^t\hat{V} - V^t\hat{I} = 0 \qquad (8\text{-}1)$$

(I, V, $\hat{I}$ and $\hat{V}$ are the Laplace transforms of the zero-state currents and voltages, i.e., it is assumed that the initial conditions are zero).

It will be assumed here that the multiports are regarded as (n+k)-ports, as shown in Fig. 8-1. This is not required by the definition of reciprocity but is a convenient assumption, since it makes easier the comparison of later results with the results which apply in the case of reciprocity. When the multiport is regarded as an (n+k)-port, equation (8-1) can be expanded as

$$I_1^t \hat{V}_1 + I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (8\text{-}2)$$

where subscripts 1 and 2 refer to the sets of n and k ports, respectively (see Fig. 8-1).

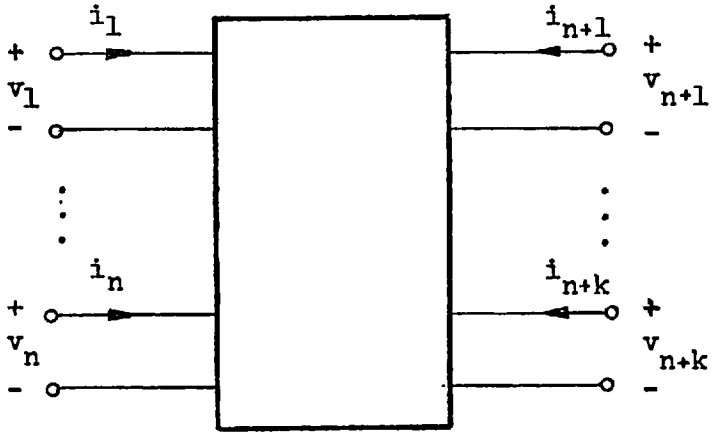
The constraints imposed by the definition of reciprocity on various matrices describing the (n+k)-port can be derived from (8-2). These constraints are shown in the first column of Table 8-1. The hybrid matrix considered is the one that corresponds to the choice of I_1 and V_2 as the dependent variables, i.e.

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \qquad (8\text{-}3)$$

The transmission matrix T, which exists only for n=k, is defined by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (8\text{-}4)$$

The reciprocity conditions in terms of the hybrid matrix were derived in chapter 2, section 2-5. The well known conditions in terms of the admittance and impedance matrices can be viewed as a special case of the conditions for the hybrid matrix. The conditions in terms of the transmission matrix appear in [100] but the derivation given there is not entirely general, since it relies on the assumption that the (n+n)-port accepts an admittance and an impedance description, in addition to having a transmission matrix; in fact the



$$I_1 = \begin{bmatrix} i_1 \\ \cdot \\ \cdot \\ \cdot \\ i_n \end{bmatrix} \qquad V_1 = \begin{bmatrix} v_1 \\ \cdot \\ \cdot \\ \cdot \\ v_n \end{bmatrix} \qquad I_2 = \begin{bmatrix} i_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ i_{n+k} \end{bmatrix} \qquad V_2 = \begin{bmatrix} v_{n+1} \\ \cdot \\ \cdot \\ \cdot \\ v_{n+k} \end{bmatrix}$$

$$I = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad V = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

Fig. 8-1 : An $(n+k)$-port.

TABLE 8.1 : Reciprocity, Anti-reciprocity, Bireciprocity and Anti-bireciprocity.

RECIPROCAL (R)	ANTI-RECIPROCAL (AR)	BIRECIPROCAL (B)	ANTI-BIRECIPROCAL (AB)
$\bar{I}^t \hat{V} - V^t \hat{I} = 0$	$I^t \hat{V} + V^t \hat{I} = 0$	$I^t \Theta \hat{V} - V^t \Theta \hat{I} = 0$	$I^t \Theta \hat{V} + V^t \Theta \hat{I} = 0$
$H_{11}=H_{11}^t$ $H_{12}=-H_{21}^t$ $H_{22}=H_{22}^t$ $(H=\Theta H^t \Theta)$	$H_{11}=-H_{11}^t$ $H_{12}=-H_{21}^t$ $H_{22}=-H_{22}^t$ $(H=-H^t)$	$H_{11}=H_{11}^t$ $H_{12}=H_{21}^t$ $H_{22}=H_{22}^t$ $(H=H^t)$	$H_{11}=-H_{11}^t$ $H_{12}=H_{21}^t$ $H_{22}=-H_{22}^t$ $(H=-\Theta H^t \Theta)$
$Y_{11}=Y_{11}^t$ $Y_{12}=Y_{21}^t$ $Y_{22}=Y_{22}^t$ $(Y=Y^t)$	$Y_{11}=-Y_{11}^t$ $Y_{12}=-Y_{21}^t$ $Y_{22}=-Y_{22}^t$ $(Y=-Y^t)$	$Y_{11}=Y_{11}^t$ $Y_{12}=-Y_{21}^t$ $Y_{22}=Y_{22}^t$ $(Y=\Theta Y^t \Theta)$	$Y_{11}=-Y_{11}^t$ $Y_{12}=Y_{21}^t$ $Y_{22}=-Y_{22}^t$ $(Y=-\Theta Y^t \Theta)$
$Z_{11}=Z_{11}^t$ $Z_{12}=Z_{21}^t$ $Z_{22}=Z_{22}^t$ $(Z=Z^t)$	$Z_{11}=-Z_{11}^t$ $Z_{12}=-Z_{21}^t$ $Z_{22}=-Z_{22}^t$ $(Z=-Z^t)$	$Z_{11}=Z_{11}^t$ $Z_{12}=-Z_{21}^t$ $Z_{22}=Z_{22}^t$ $(Z=\Theta Z^t \Theta)$	$Z_{11}=-Z_{11}^t$ $Z_{12}=Z_{21}^t$ $Z_{22}=-Z_{22}^t$ $(Z=-\Theta Z^t \Theta)$
$A^tC=C^tA$ $A^tD-C^tB=1$ $B^tD=D^tB$ $(T\Phi T^t \Phi^t=1)$	$A^tC=-C^tA$ $A^tD+C^tB=1$ $B^tD=-D^tB$ $(T\Psi T^t \Psi=1)$	$A^tC=C^tA$ $A^tD-C^tB=-1$ $B^tD=D^tB$ $(T\Phi T^t \Phi^t=-1)$	$A^tC=-C^tA$ $A^tD+C^tB=-1$ $B^tD=-D^tB$ $(T\Psi T^t \Psi=-1)$

conditions for the transmission matrix are derived in [100] from the conditions for the Y and Z matrices. A derivation from equation (8-1) will now be presented.

The transmission description, (8-4), can be used in conjunction with the definition of reciprocity, (8-2), to give

$$(V_2^t C^t - I_2^t D^t)(A\hat{V}_2 - B\hat{I}_2) + I_2^t\hat{V}_2 - (V_2^t A^t - I_2^t B^t)(C\hat{V}_2 - D\hat{I}_2) - V_2^t\hat{I}_2 = 0$$

or

$$V_2^t(C^tA - A^tC)\hat{V}_2 + V_2^t(A^tD - C^tB - 1_n)\hat{I}_2$$
$$+ I_2^t(-D^tA + B^tC + 1_n)\hat{V}_2 + I_2^t(D^tB - B^tD)\hat{I}_2 = 0 \qquad (8\text{-}5)$$

This equation must be satisfied for any I_2, V_2, $\hat{I}_2$ and $\hat{V}_2$. Chosing $I_2 = 0$ and $\hat{I}_2 = 0$ leads to

$$V_2^t\,(C^tA - A^tC)\hat{V}_2 = 0 \qquad (8\text{-}6)$$

which requires that

$$C^tA - A^tC = 0 \qquad (8\text{-}7a)$$

Similar arguments for $I_2 = 0$ and $\hat{V}_2 = 0$ (or $\hat{I}_2 = 0$ and $V_2 = 0$) and for $V_2 = 0$ and $V_2 = 0$ lead, respectively to

$$A^tD - C^tB = 1_n \qquad (8\text{-}7b)$$

and

$$B^tD - D^tB = 0 \qquad (8\text{-}7c)$$

Equations (8-7) are equivalent to

$$\begin{bmatrix} A^t & C^t \\ B^t & D^t \end{bmatrix} \begin{bmatrix} D & -C \\ -B & A \end{bmatrix} = \begin{bmatrix} 1_n & 0 \\ 0 & 1_n \end{bmatrix} \qquad (8\text{-}8)$$

By introducing a matrix Φ defined as

$$\Phi = \begin{bmatrix} 0 & 1_n \\ -1_n & 0 \end{bmatrix}$$

equation (8-8) can be written as

$$T^t \Phi T \Phi^t = 1_{2n} \tag{8-9}$$

Transposing both sides of (8-9) leads to

$$\Phi T^t \Phi^t T = 1_{2n} \tag{8-10}$$

This shows that

$$T^{-1} = \Phi T^t \Phi^t$$

and therefore the product of T and $\Phi T^t \Phi$ is commutative. Therefore equation (8-10) can also be written as:

$$T \Phi T^t \Phi^t = 1_{2n} \tag{8-11}$$

Equations (8-7) to (8-11) are equivalent ways of expressing the reciprocity conditions in terms of the transmission matrix of an (n+n)-port.

The reciprocity conditions in terms of the scattering parameters will also be considered. The basic definitions concerning the scattering description of multiports have been summarized in chapter 2. The reciprocity conditions in terms of the normalized currents and voltages, I′ and V′, the scattering variables, $\mathcal{a}$ and $\mathcal{b}$, and the scattering matrix S, are given in the first column of Table 8-2. All these results can be easily derived from equation (8-1).

A very important result concerning reciprocity is the Reciprocity Theorem: a multiport containing only reciprocal elements is itself reciprocal. As already mentioned in chapter 2, section 2.5, the reciprocity theorem is easily proved by using Tellegen's theorem in conjunction with the definition of reciprocity [2,21].

TABLE 8.2 : Reciprocity, Anti-reciprocity, Bireciprocity and Anti-bireciprocity in terms of the scattering variables.

RECIPROCAL (R)	ANTI-RECIPROCAL (AR)	BIRECIPROCAL (B)	ANTI-BIRECIPROCAL (AB)
$I'^{t}\hat{V}' - V'^{t}\hat{I}' = 0$	$I'^{t}\hat{V}' + V'^{t}\hat{I}' = 0$	$I'^{t}\Theta\hat{V}' - V'^{t}\Theta\hat{I}' = 0$	$I'^{t}\Theta\hat{V}' + V'^{t}\Theta\hat{I}' = 0$
$\mathcal{A}^{t}\hat{\mathcal{B}} - \mathcal{B}^{t}\hat{\mathcal{A}} = 0$	$\mathcal{A}^{t}\hat{\mathcal{A}} - \mathcal{B}^{t}\hat{\mathcal{B}} = 0$	$\mathcal{A}^{t}\Theta\hat{\mathcal{B}} - \mathcal{B}^{t}\Theta\hat{\mathcal{A}} = 0$	$\mathcal{A}^{t}\Theta\hat{\mathcal{A}} - \mathcal{B}^{t}\Theta\hat{\mathcal{B}} = 0$
$S = S^{t}$	$S\,S^{t} = 1$	$S = \Theta\,S^{t}\,\Theta$	$S\Theta S^{t}\Theta = 1$

8.3 - TWO TYPES OF ANTI-RECIPROCITY

A multiport that is not reciprocal is said to be non-reciprocal. It seems natural to call anti-reciprocal those multiports that have properties which are, in some sense, the opposite of the properties exhibited by reciprocal multiports.

A definition of anti-reciprocal multiports which has been proposed by several authors [20,2,21] is obtained from the definition of reciprocity given above by replacing the (-) sign in (8-1) by a (+) sign:

$$I^t \hat{V} + V^t \hat{I} = 0 \qquad (8\text{-}12)$$

The constraints imposed by anti-reciprocity on various matrices describing an (n+k)-port can be obtained from (8-12) through derivations similar to those used in connection with reciprocity. These constraints are shown in the second column of Table 8-1 (the anti-reciprocity conditions in terms of the scattering parameters can be found in Table 8-2).

Using Tellegen's theorem it is easy to prove the anti-reciprocity theorem [2,21] : A multiport containing only anti-reciprocal elements is itself anti-reciprocal.

Another definition of anti-reciprocity, in terms of 2-ports, has been proposed by several authors (see, for example [69,70,71]). In contrast with reciprocal 2-ports, for which

$$y_{12} = y_{21} \qquad (8\text{-}13a)$$

$$z_{12} = z_{21} \qquad (8\text{-}13b)$$

$$h_{12} = -h_{21} \qquad (8\text{-}13c)$$

$$\det T = ad - bc = 1 \qquad (8\text{-}13d)$$

'anti-reciprocal' 2-ports are defined by the following conditions

$$y_{12} = -y_{21} \tag{8-14a}$$

$$z_{12} = -z_{21} \tag{8-14b}$$

$$h_{12} = h_{21} \tag{8-14c}$$

$$\det T = ad - bc = -1 \tag{8-14d}$$

These conditions are equivalent in the sense that the condition in terms of one type of parameters implies the conditions in terms of the other types of parameters (if they exist).

The conditions expressed by equations (8-14) are not special cases of the anti-reciprocity conditions in Table 8-1. For instance, for the admittance matrix, the anti-reciprocity conditions in Table 8-1 require that

$$Y = -Y^t$$

which means that

$$y_{11} = 0 \; ; \qquad y_{22} = 0 \; ; \qquad y_{12} = -y_{21}$$

This is a much stronger condition than the one expressed by equation (8-14a), which only requires that

$$y_{12} = -y_{21}$$

In view of the fact that the two existing definitions of anti-reciprocity do not coincide, it seems appropriate to compare in some detail the consequences of the two definitions. This will now be done.

It is desirable to use different designations for the network properties associated with the two different definitions. The designation anti-reciprocity will be maintained for the property defined by (8-12). The designation bireciprocity will be applied to the property defined by (8-14). This designation, bireciprocity, is not entirely satisfactory, since it does not suggest the "anti-reciprocal"

nature of the property; however, as will be pointed out later, there is some justification for this choice of nomenclature.

Using the anti-reciprocity conditions for the transmission matrix (Table 8-1) it will be shown that there are only two types of anti-reciprocal 2-ports. If the conditions for the transmission matrix are particularized for 2-ports, the following equations are obtained:

$$ac = 0 \tag{8-15a}$$

$$db = 0 \tag{8-15b}$$

$$ad + bc = 1 \tag{8-15c}$$

If the parameters a, b, c and d are chosen in such a way that (8-15a) and (8-15b) are satisfied, the following table is obtained:

a	b	c	d	ad + bc
0	0	$\neq 0$	$\neq 0$	0
0	$\neq 0$	$\neq 0$	0	bc
$\neq 0$	0	0	$\neq 0$	ad
$\neq 0$	$\neq 0$	0	0	0

This table and the remaining condition (8-15c) show that there are only two possibilities

1. $a = 0 \quad , \quad d = 0 \quad , \quad bc = 1$ (8-16)

or

2. $b = 0 \quad , \quad c = 0 \quad , \quad ad = 1$ (8-17)

The first case corresponds to a 2-port with a description in the form of

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \tag{8-18}$$

and the second case corresponds to a 2-port with a transmission description of the form

$$\begin{bmatrix} i_1 \\ v_1 \end{bmatrix} = \begin{bmatrix} \gamma^{-1} & 0 \\ 0 & \gamma \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \qquad (8\text{-}19)$$

If in (8-18) the parameter g is a real constant the 2-port is a positive gyrator, and if γ in (8-19) is a real constant the 2-port is a positive transformer (the positive transformer and positive gyrator have been introduced in chapter 3, section 3.3). Although the 2-port described by (8-18) is only a gyrator if g is real and constant, it is convenient, in this chapter, to extend the designation positive gyrator to the case where g may be a function of s (a more rigorous designation, such as 'generalized positive gyrator', is not used here because it would be too cumbersome). Similarly, the designations positive transformer, negative transformer and negative gyrator will, in the present chapter be applied to 2-ports described by parameters which are allowed to be functions of s.

Thus, the only anti-reciprocal 2-ports possessing a transmission description are the positive gyrator and the positive transformer.

Anti-reciprocal multiports will now be considered. These are described by a skew-symmetric hybrid matrix (Table 8-1). This applies to well-defined multiports since these always possess some hybrid description. By using the realization method discussed in chapter 5, section 5.3, it is easy to see that only 2-port positive transformers and positive gyrators are required when the hybrid matrix is skew-symmetric. This means that any well-defined(*) multiport which is anti-reciprocal is equivalent to an interconnection of positive gyrators and positive transformers. This shows that the set of all anti-

(*) Although the author has not found any example of an anti-reciprocal multiport that is not well-defined, it has not been proved that any anti-reciprocal multiport must be well-defined has not been proved.

reciprocal multiports is relatively 'empty' and therefore the usefulness of the anti-reciprocity theorem is very restricted.

The definition of bireciprocity does not lead to a theorem similar to the reciprocity or anti-reciprocity theorems, since a multiport containing only bireciprocal components is not necessarily bireciprocal itself. However, the following statements apply to the cascade of 2-ports (they are a consequence of det T = 1 for reciprocal 2-ports, and det T = -1 for bireciprocal 2-ports):

(a) The 2-port resulting from the cascade connection of a reciprocal and a bireciprocal 2-port is birecpirocal.

(b) The 2-port resulting from the cascade connection of two bireciprocal 2-ports is reciprocal.

These statements are less general than the anti-reciprocity theorem, since the type of connection involved (cascade) is specified. However they apply to a much wider class of 2-ports.

The two statements (a) and (b) establish a means of effecting a transformation from the universe of reciprocal 2-ports to the "anti-universe" of bireciprocal 2-ports, and vice versa, via the cascading with any bireciprocal 2-port, e.g., a gyrator. This indicates that the set of all bireciprocal 2-ports is as "dense" as the set of all reciprocal 2-ports. This is in contrast with the relative "emptiness" of the set of all anti-reciprocal 2-ports which, as seen before, contains only the positive gyrator and the positive transformer.

This discussion of the two definitions can be illustrated (for non-reactive 2-ports, i.e., 2-ports described by constant and real parameters) by using the(ad,bc)-plane. As shown in Fig.8-2, reciprocal and bireciprocal 2-ports are represented by two parallel lines. In contrast with this, anti-reciprocal 2-ports are represented by two

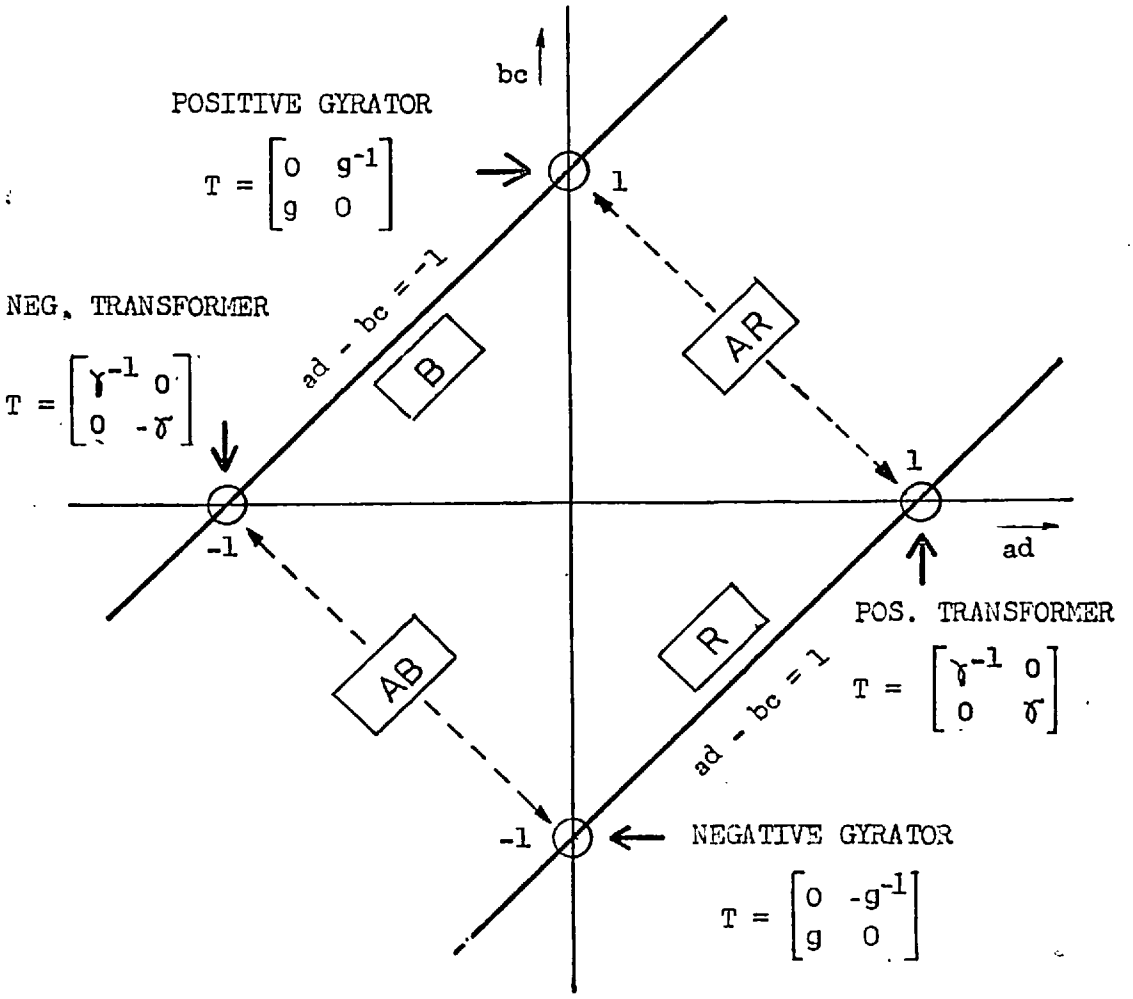


Fig. 8-2 : The (ad,bc)-plane.

points only, one on the reciprocal line (positive transformer) and the other on the bireciprocal line (positive gyrator).

The foregoing discussion shows that, whereas the definition of anti-reciprocity, by equation (8-12), is valid for multiports and leads to the anti-reciprocity theorem, the definition of bireciprocity, by equations (8-14), is restricted to 2-ports, but leads to some very interesting consequences. This suggests that it would be desirable to extend to multiports the definition of bireciprocity so far restricted to 2-ports.

Apparently the extension of (8-14a) and (8-14b) to multiports would be

$$y_{ij} = -y_{ji} \qquad (i \neq j) \tag{8-20a}$$

and

$$z_{ij} = -z_{ji} \qquad (i \neq j) \tag{8-20b}$$

However, whereas equations (8-20a) and (8-20b) are equivalent in the case of 2-ports, for n-ports with $n>2$ these two equations are no longer equivalent as shown by the following example.

A 3-port described by the admittance matrix

$$Y = \begin{bmatrix} 1 & 1 & -1 \\ -1 & 1 & 1 \\ 1 & -1 & 1 \end{bmatrix}$$

which satisfies (8-20a), can, equivalently, be described by the impedance matrix

$$Z = Y^{-1} = \tfrac{1}{2} \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$$

which does not satisfy (8-20b)

This shows that the extension to n-ports of equations (8-14), which are valid for 2-ports, is not straightforward. However it will

be shown in the next section that,by interpreting 2-ports as (1+1)-ports, an extension of (8-14) to (n+k)-ports is possible.

8.4 - BIRECIPROCITY

The fact that, for 2-ports, the definition of bireciprocity,

$$ad - bc = -1 \tag{8-21}$$

differs from the reciprocity condition,

$$ad - bc = +1 \tag{8-22}$$

by a change in sign, suggests that the generalization of bireciprocity for (n+n)-ports might be obtained from the reciprocity conditions in terms of the transmission matrix,

$$A^t D - C^t B = 1_{2n} \tag{8-23a}$$

$$A^t C = C^t A \tag{8-23b}$$

$$B^t D = D^t B \tag{8-23c}$$

by changing $+1_{2n}$ to -1_{2n} in (8-23a), since this is the equation that for 2-ports leads to (8-22). Thus bireciprocity might be defined by

$$A^t D - C^t B = -1_{2n} \tag{8-24a}$$

$$A^t C = C^t A \tag{8-24b}$$

$$B^t D = D^t B \tag{8-24c}$$

A preliminary investigation of the consequences of (8-24) shows that some of the interesting features of bireciprocity are maintained, but a complete generalization has not yet been achieved, since (8-24) only applies to (n+n)-ports and only to those which have a transmission description. However this limitation can be avoided. It can be shown that (8-24) can be obtained from an equation similar to (8-2):

$$I_1^t \hat{V}_1 - I_2^t \hat{V}_2 - V_1^t \hat{I}_1 + V_2^t \hat{I}_2 = 0 \tag{8-25}$$

(the derivation of (8-24) from (8-25) is entirely parallel to the derivation of (8-23) from (8-2) given in section 8.2).

Equation (8-25) will now be regarded as the general definition of bireciprocity. It implies that the ports are partitioned into two sets, associated with subscripts 1 and 2, but these sets do not have to contain the same number of ports, i.e., the multiport is regarded as an (n+k)-port.

By using the auxiliary matrix

$$\Theta = \begin{bmatrix} 1_n & 0 \\ 0 & -1_k \end{bmatrix}$$

equation (8-25) can be written in the more compact form

$$I^t \Theta \hat{V} - V^t \Theta \hat{I} = 0 \qquad (8\text{-}26)$$

The bireciprocity conditions in terms of various matrices can be obtained from (8-25) and are given in the third column of Table 8.1. It should be noted that the specific hybrid matrix considered is the one that corresponds to the choice of variables

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix} \qquad (8\text{-}27)$$

where subscripts 1 and 2 are associated with the sets of n and k ports into which the ports have been partitioned as required by the definition of bireciprocity. In fact, in the case of the hybrid matrix two different partitions of the ports are involved: one associated with the definition of bireciprocity, and the other with the choice of variables for the hybrid description. Although these two partitions do not have to coincide, in this chapter only the particular H matrix is considered for which the two partitions coincide.

Similar considerations apply to the transmission matrix chosen:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (8\text{-}28)$$

This particular choice of variables for the hybrid and transmission matrices leads to simpler equations which provide more insight.

The bireciprocity conditions in terms of the scattering parameters can be easily derived from (8-26) and are given in Table 8-2.

It is apparent that the results in Table 8-1 (3rd column) lead to conditions (8-14) for 2-ports. This confirms that a generalization of the original definition (8-14) of bireciprocal 2-ports has been achieved.

8.5 - ANTI-BIRECIPROCITY

If equations (8-1), (8-12) and (8-26) are compared (first row of Table 8.1), it becomes apparent that a 'complete pattern' will be obtained if a fourth equation is considered:

$$I^t \ominus \hat{V} + V^t \ominus \hat{I} = 0 \qquad (8\text{-}29)$$

This equation will be taken as the definition of a new network property which will be designated as anti-bireciprocity. As for bireciprocity, a partition of the ports into two sets is implied by the definition of anti-bireciprocity. Equation (8-29) can be expanded as

$$I_1^t \hat{V}_1 - I_2^t \hat{V}_2 + V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (8\text{-}30)$$

From (8-30) it is possible to derive the anti-bireciprocity conditions for various matrices (Table 8.1); the conditions in terms of the scattering parameters are also given (Table 8.2). The particular hybrid and transmission matrices considered correspond to the same choice of variables as in the case of bireciprocity.

With Table 8.1 now complete, a comparison of the conditions imposed on the various matrices by reciprocity (R), anti-reciprocity (AR), bireciprocity (B) and anti-bireciprocity (AB) confirms that a complete pattern can only be obtained if anti-bireciprocity is included. The set of these four network properties related to the concept of reciprocity will be referred to as R4:

$$R4 = \{R, AR, B, AB\}$$

The abbreviation R will be used both for the noun reciprocity and for the adjective reciprocal; the abbreviations AR, B and AB will be used in a similar way. It is convenient to refer to a multiport possessing one of the four network properties forming the set R4 as a multiport 'belonging to R4'.

From the conditions in Table 8.1 it can easily be seen that the only AB 2-ports are the negative transformer, which has a description of the form

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} \gamma^{-1} & 0 \\ 0 & -\gamma \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \qquad (8\text{-}31)$$

and the negative gyrator, which is described by

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 0 & -g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} v_2 \\ -i_2 \end{bmatrix} \qquad (8\text{-}32)$$

In the (ad,bc)-plane, AB 2-ports are represented by two points, as shown in Fig. 8-2. It is seen that AB, when added to R, AR and B completes a pattern in the (ad,bc)-plane.

The 'completeness' of the set R4 = {R, AR, B, AB} will now be examined from a different point of view.

The equations defining the four properties in R4, (8-1), (8-12), (8-26) and (8-29) can be expanded as the algebraic sum of the four terms

$$I_1^t \hat{V}_1, \quad I_2^t \hat{V}_2, \quad V_1^t \hat{I}_1, \quad V_2^t \hat{I}_2$$

equal to zero. The four equations only differ in the signs assigned to the four terms. The consequences, in terms of the admittance matrix, of equations with all possible sign patterns are given in the table on the next page.

It suffices to consider only the sign patterns which start with a (+) sign, since the patterns starting with a (-) sign do not lead to different equations (an equation corresponding to a pattern with a leading (-) sign coincides with an equation with a leading (+) sign multiplied by -1).

It can be seen from the table that all sign patterns that lead to equations different from the four already considered, correspond to degenerate multiports without interaction between the ports in different sets, i.e.

$$Y_{12} = 0 \quad \text{and} \quad Y_{21} = 0$$

This shows that the 4 properties considered so far form a 'complete' set in the sense that they are the only interesting properties defined by equations of the type considered above.

8.6 - THE MEANING OF BIRECIPROCITY AND ANTI-BIRECIPROCITY

The definitions of both B and AB imply a partition of the ports into two sets. Therefore the concepts of B and AB are not applicable to 1-ports. This contrasts with R and AR which have a meaning for 1-ports: all 1-ports are R, and there are two (and only two) 1-ports which are also AR, the short-circuit and the open-circuit (the nullator and the norator are not considered here, since they must always occur as nullator-norator pairs (nullors), i.e., as part of 2-ports).

SIGN PATTERN	ADMITTANCE MATRIX			COMMENTS
+ - - -	$Y_{11}=Y_{11}^t$	$Y_{22}=-Y_{22}^t$	$Y_{12}=Y_{21}=0$	————
+ - - +	$Y_{11}=Y_{11}^t$	$Y_{22}=Y_{22}^t$	$Y_{12}=-Y_{21}^t$	BIRECIPROCITY
+ - + -	$Y_{11}=-Y_{11}^t$	$Y_{22}=-Y_{22}^t$	$Y_{12}=Y_{21}^t$	ANTI-BIRECIPROCITY
+ - + +	$Y_{11}=-Y_{11}^t$	$Y_{22}=Y_{22}^t$	$Y_{12}=Y_{21}=0$	————
+ + - -	$Y_{11}=Y_{11}^t$	$Y_{22}=Y_{22}^t$	$Y_{12}=Y_{21}^t$	RECIPROCITY
+ + - +	$Y_{11}=Y_{11}^t$	$Y_{22}=-Y_{22}^t$	$Y_{12}=Y_{21}=0$	————
+ + + -	$Y_{11}=-Y_{11}^t$	$Y_{22}=Y_{22}^t$	$Y_{12}=Y_{21}=0$	————
+ + + +	$Y_{11}=-Y_{11}^t$	$Y_{22}=-Y_{22}^t$	$Y_{12}=-Y_{21}^t$	ANTI-RECIPROCITY

So far B and AB have been formally defined in terms of equations (8-26) and (8-29). Further insight into the meaning of B and AB can be obtained by considering separately relationships between 'ports of the same set' and relationships between 'ports of different sets'. In this discussion, considering initially B multiports, only two ports of a B multiport will be selected for consideration; all the remaining ports will be either short-circuited or open-circuited. This is done in accordance with the assignment of zero value to either voltages or currents as independent variables in a hybrid description (which is always possible for a well-defined multiport). Examination of (8-25) and (8-1) leads immediately to the following conclusion:

- In a B multiport, any number of ports of the same set form an R multiport, and any two ports of different sets form a B 2-port.

In a similar way, it can be seen from (8-30) and (8-12) that:

- In an AB multiport, any number of ports of the same set form an AR multiport, and any two ports of different sets form an AB 2-port. In other words, if a multiport is AB, any two ports of the same set behave as a positive transformer or as a positive gyrator, and any two ports of different sets as a negative transformer or negative gyrator .

The reason for the choice of the designation <u>bireciprocal</u> can now be appreciated: there is a partition of the ports into <u>two</u> sets and the ports of each set are <u>reciprocal</u>. Similarly, in the case of anti-bireciprocity, there is a partition of the ports into two sets and the ports of each set are anti-reciprocal.

8.7 CASCADE CONNECTION OF VARIOUS TYPES OF MULTIPORTS

Several rules can be established concerning the character of an (n+k)-port N formed by the cascade connection of an (n+q)-port N_1 with an (q+k)-port N_2 (see Fig. 8-3) if N_1 and N_2 belong to the set R4. If n = k then additional rules can be derived which require that only one of N_1 or N_2 belong to R4.

If N_1 and N_2 are both R, N is also R as a consequence of the reciprocity theorem. Similarly, it follows from the anti-reciprocity theorem that if N_1 and N_2 are both AR, then N is also AR. These two rules are well known. However, when, in addition to R and AR, also B and AB are considered, several new rules can be obtained.

One of these new rules is that if N_1 is R and N_2 is B then N is B. This is easily proved by applying the defining equations (8-2) and (8-25) to N_1 and N_2 (Fig. 8-3):

$$I_1^t \hat{V}_1 + I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (8\text{-}33)$$

and

$$-I_2^t \hat{V}_2 - I_3^t \hat{V}_3 + V_2^t \hat{I}_2 + V_3^t \hat{I}_3 = 0 \qquad (8\text{-}34)$$

Elimination of the terms with subscript 2, leads to

$$I_1^t \hat{V}_1 - I_3^t \hat{V}_3 - V_1^t \hat{I}_1 + V_3^t \hat{I}_3 = 0 \qquad (8\text{-}35)$$

and this shows that N is B.

Following a similar procedure several other rules can be obtained. These combination rules are summarized in Tables 8-3a and 8-3b. The rules in Table 8-3a, involving R and B are isomorphic to those in Table 8-3b, involving AR and AB.

It can easily be shown, by means of counter-examples, that similar rules cannot be established concerning other combinations of two

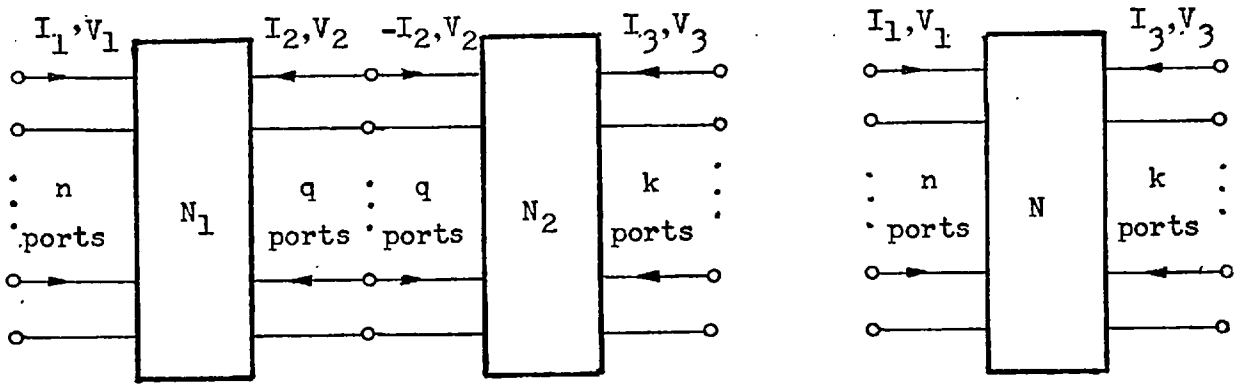


Fig. 8-3 : Cascade connection of 2 multiports.

TABLE 8-3 : Rules concerning the cascade connection of an (n+q)-port and a (q+k)-port.

(a)

N_2 \ N_1	R	B
R	R	B
B	B	R

(b)

N_2 \ N_1	AR	AB
AR	AR	AB
AB	AB	AR

TABLE 8-4 : Rules concerning the cascade of two (n+n)-ports.

N_1	N_2	N
L_ϕ	R	L_ϕ
L_ϕ	B	$-L_\phi$
L_ψ	AR	L_ψ
L_ψ	AB	$-L_\psi$
R	M_ϕ	M_ϕ
B	M_ϕ	$-M_\phi$
AR	M_ψ	M_ψ
AB	M_ψ	$-M_\psi$

properties. For instance, if N_1 is R and N_2 is AR, N may or may not possess a property belonging to the set R4.

For the special case where N_1 and N_2 are both (n+n)-ports possessing transmission matrices, quantitative results regarding N can be established. In this case only one of the sub-networks N_1 and N_2 is required to belong to the set R4. The various rules are expressed in terms of four matrices which are related to the transmission matrix as follows:

$$L_\phi = T\,\Phi\,T^t\,\Phi^t \tag{8-36}$$

$$L_\psi = T\,\Psi\,T^t\,\Psi \tag{8-37}$$

$$M_\phi = \Phi\,T^t\,\Phi^t\,T \tag{8-38}$$

$$M_\psi = \Psi\,T^t\Psi\;\;T \tag{8-39}$$

where Φ and Ψ are auxiliary matrices that have been used before:

$$\Phi = \begin{bmatrix} 0 & 1_n \\ -1_n & 0 \end{bmatrix} \qquad \Psi = \begin{bmatrix} 0 & 1_n \\ 1_n & 0 \end{bmatrix}$$

The various rules are given in Table 8-4. A proof will only be given for the case where N_1 is arbitrary and N_2 is either R or B. The proofs for the other cases are very similar .

For the multiport N, with $T = T_1\,T_2$, L_ϕ is, by definition

$$(L_\phi)_N = T_1\,T_2\,\Phi\,T_2^t\,T_1^t\,\Phi^t \tag{8-40}$$

or, taking into account that $\Phi\,\Phi^t = 1_{2n}$

$$(L_\phi)_N = T_1(T_2\,\Phi\,T_2^t\;\Phi^t)\,\Phi\,T_1^t\;\Phi^t \tag{8-41}$$

If N_2 is R, then $T_2\,\Phi\,T_2^t\;\Phi^t = 1_{2n}$ and therefore

$$(L_\phi)_N = T_1\,\Phi\,T_1^t\;\Phi^t$$

or

$$(L_\phi)_N = (L_\phi)_{N_1} \tag{8-42}$$

If N_2 is B, then $T_2 \Phi T_2^t \Phi^t = -1_{2n}$, and consequently

$$(L_\Phi)_N = -(L_\Phi)_{N_1} \qquad (8\text{-}43)$$

8.8 - MULTIPORT TRANSFORMERS AND GYRATORS

It has already been mentioned that the only AR 2-ports are the positive transformer, which is also reciprocal, and the positive gyrator, which is also bireciprocal; it has also been mentioned that the only AB 2-ports are the negative transformer, which is also bireciprocal, and the negative gyrator, which is also reciprocal. This is clearly illustrated (for 2-ports described by real, constant parameters) by the representation of these 2-ports on the (ad,bc)-plane (Fig. 8-2). There are thus four 2-ports which possess simultaneously two properties of the set R4 = { R, AR, B, AB } :

Positive Transformer	(PT)	:	R and AR
Negative Transformer	(NT)	:	B and AB
Positive Gyrator	(PG)	:	AR and B
Negative Gyrator	(NG)	:	R and AB

The present section is concerned with multiports that possess simultaneously two properties belonging to the set R4. A systematic search for these multiports can easily be conducted using the results in Table 8.1. In this search (n-k)-ports described by an admittance, impedance, or hybrid description will be considered. The hybrid matrix used is the one considered in Table 8.1 (which is discussed in section 8.4). The results of the search are given in the table on the next page.

It can be seen that if the degenerate multiports without interaction between the two sets of ports are discarded, only six (n+k)-ports are left. These can be regarded as a generalization of the 2-ports

	Y	Z	H
R + AR	$Y_{11}=0$ $Y_{22}=0$ $Y_{12}=Y_{21}=0$	$Z_{11}=0$ $Z_{22}=0$ $Z_{12}=Z_{21}=0$	$H_{11}=0$ $H_{22}=0$ $H_{12}=-H_{21}^t$ POS. TRANSF.
R + B	$Y_{11}=Y_{11}^t$ $Y_{22}=Y_{22}^t$ $Y_{12}=Y_{21}=0$	$Z_{11}=Z_{11}^t$ $Z_{22}=Z_{22}^t$ $Z_{12}=Z_{21}=0$	$H_{11}=H_{11}^t$ $H_{22}=H_{22}^t$ $H_{12}=H_{21}=0$
R + AB	$Y_{11}=0$ $Y_{22}=0$ $Y_{12}=Y_{21}^t$ NEG. GYRATOR	$Z_{11}=0$ $Z_{22}=0$ $Z_{12}=Z_{21}^t$ NEG. GYRATOR	$H_{11}=0$ $H_{22}=0$ $H_{12}=H_{21}=0$
AR + B	$Y_{11}=0$ $Y_{22}=0$ $Y_{12}=-Y_{21}^t$ POS. GYRATOR	$Z_{11}=0$ $Z_{22}=0$ $Z_{12}=-Z_{21}^t$ POS. GYRATOR	$H_{11}=0$ $H_{22}=0$ $H_{12}=H_{21}=0$
AR + AB	$Y_{11}=-Y_{11}^t$ $Y_{22}=-Y_{22}^t$ $Y_{12}=Y_{21}=0$	$Z_{11}=-Z_{11}^t$ $Z_{22}=-Z_{22}^t$ $Z_{12}=Z_{21}=0$	$H_{11}=-H_{11}^t$ $H_{22}=-H_{22}^t$ $H_{12}=H_{21}=0$
B + AB	$Y_{11}=0$ $Y_{22}=0$ $Y_{12}=Y_{21}=0$	$Z_{11}=0$ $Z_{22}=0$ $Z_{12}=Z_{21}=0$	$H_{11}=0$ $H_{22}=0$ $H_{12}=H_{21}^t$ NEG. TRANSF.

TABLE 8.5 : Multiport Transformers and Gyrators

DESIGNATION		MATRIX DESCRIPTION				PROPERTIES		
		H	Y	Z	T (n=k)	RECIPROCITY	ACTIVITY	IMMITTANCE TRANSF.on
POSITIVE TRANSFORMER		$\begin{matrix} 0 & K \\ -K^t & 0 \end{matrix}$	——	——	$\begin{matrix} -(K^t)^{-1} & 0 \\ 0 & -K \end{matrix}$	R and AR	non-energic if K real	admittance converter in one direction and inpedance converter in other direction (**)
NEGATIVE TRANSFORMER		$\begin{matrix} 0 & K \\ K^t & 0 \end{matrix}$	——	——	$\begin{matrix} (K^t)^{-1} & 0 \\ 0 & -K \end{matrix}$	B and AB	active if K real	
POSITIVE GYRATOR	Admittance Gyrator	——	$\begin{matrix} 0 & G \\ -G^t & 0 \end{matrix}$	only exists if n=k and $\lvert G\rvert \neq 0$ (*)	$\begin{matrix} 0 & (G^t)^{-1} \\ G & 0 \end{matrix}$	B and AR	non-energic if G, R real	admittance inverter in both directions
	Impedance Gyrator	——	only exists if n=k and $\lvert R\rvert \neq 0$ (*)	$\begin{matrix} 0 & R \\ -R^t & 0 \end{matrix}$	$\begin{matrix} 0 & -R \\ -(R^t)^{-1} & 0 \end{matrix}$			impedance inverter in both directions
NEGATIVE GYRATOR	Admittance Gyrator	——	$\begin{matrix} 0 & G \\ G^t & 0 \end{matrix}$	only exists if n=k and $\lvert G\rvert \neq 0$ (*)	$\begin{matrix} 0 & -(G^t)^{-1} \\ G & 0 \end{matrix}$	R and AB	active if G, R real	admittance inverter in both directions
	Impedance Gyrator	——	only exists if n=k and $\lvert R\rvert \neq 0$ (*)	$\begin{matrix} 0 & R \\ R^t & 0 \end{matrix}$	$\begin{matrix} 0 & -R \\ (R^t)^{-1} & 0 \end{matrix}$			impedance inverter in both directions

(*) If these conditions are satisfied, the (n+k)-port is simultaneously an admittance and an impedance inverter (in both directions.

(**) If n=k and det $K \neq 0$ the transformer is simultaneously an admittance and an impedance converter in both directions.

discussed above and will be referred to by the same designations as the corresponding 2-ports. The matrix description and more significant properties of these multiports are given in Table 8-5. It can be seen that all the multiports in Table 8-5 are special cases of the multiport admittance and impedance converters and inverters discussed before in this thesis.

8.9 - THE DETERMINANT OF THE TRANSMISSION MATRIX

For 2-ports the determinant of the transmission matrix is +1 if the 2-port is R, -1 if it is B, and has two possible values, ± 1, both for AR and AB 2-ports.

For a reciprocal (n+n)-port

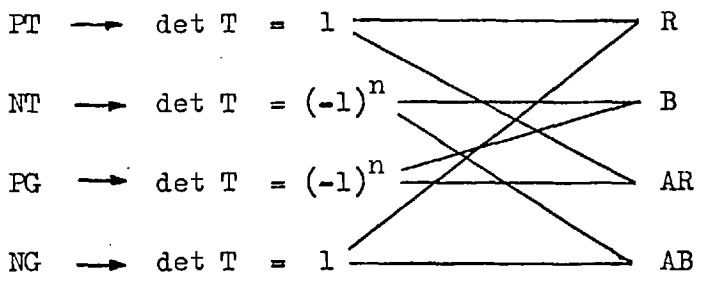
$$T \Phi T^t \Phi^t = 1_{2n}$$

(see Table 8.1). Taking the determinant of both sides and taking into account that $(\det \Phi)^2 = 1$ it follows that

$$(\det T)^2 = 1 \qquad (8\text{-}44)$$

This result is also obtained for AR, B and AB (n+n)-ports. Thus for (n+n)-ports belonging to the set R4, det T can only be +1 or -1. It is of interest to know whether there are cases where it can be decided whether det T is +1 or -1. Although the author has not found an answer to this question, a conjecture will be proposed.

The multiport transformers and gyrators with n=k are examples of (n+n)-ports belonging to the set R4. Their transmission matrices are given in Table 8-5. The value of det T can be determined by making use of the Laplace expansion using minors of order n. The following results are obtained:



Thus the value of det T for these particular (n+n)-ports follows the pattern

	R	AR	B	AB
n odd	1	$\pm$ 1	-1	$\pm$1
n even	1	1	1	1

It is conjectured that these results are valid in general, since no counter-example was found to disprove this.

It should be mentioned that it is proved in [101] that det T = 1 for reciprocal (n+n)-ports which have a transmission matrix in which the submatrix C is non-singular.

8.10 - RELATIONSHIPS WITH PASSIVITY AND ACTIVITY

In this section some relationships between the four properties in R4 = {R, AR, B, AB} and passivity-activity will be considered.

Concerning R and B, simple relationships with activity and passivity are not apparent. Both R and B multiports can be passive or active.

The only AR 2-ports are the positive transformer and the positive gyrator which have been assumed in this chapter, to be, in general, described by parameters which can be functions of s. When both these two ports are non-reactive, i.e., described by real and constant parameters, they are non-energic (this is well known; a proof has

been presented as part of the survey in chapter 3). Since, as mentioned before, any AR multiport that is well-defined is equivalent to an interconnection of positive transformers and positive gyrators, it follows that:

- Any well-defined AR multiport described by real and constant parameters is non-energic.

The only AB 2-ports are the negative transformer and the negative gyrator. When these 2-ports are non-reactive, they are active (among all converters and inverters described by real and constant parameters only the positive transformer and positive gyrator are not active, as shown in 3.3). Since, as shown in section 8.6 an AB 2-port is obtained by taking 2-ports of different sets and open or short-circuiting the remaining ports, it follows that:

- Any AB multiport described by real and constant parameters is active.

8.11 - CONCLUSIONS

It has been shown that the concept of anti-reciprocity has, until now, been covered by two conflicting definitions. An investigation with the aim of clarifying this conflict, has led to the generalization of one of these definitions, which so far had been given for 2-ports only, to multiports. The examination of the meaning of this generalized definition has suggested that this type of 'anti-reciprocity' might be designated as bireciprocity (B); the designation anti-reciprocity (AR) has been retained for the other definition (a different nomenclature has been used in [105]).

Comparison of the definitions of reciprocity (R), anti-reciprocity (AR) and bireciprocity (B) has led to the introduction of a new network property in order to obtain a 'complete pattern'. This new

property has been designated as anti-bireciprocity (AB). A set of four network properties related to the concept of reciprocity, R4 = {R, AR, B, AB} , is thus created and it is shown that in many respects B is related to R in the same way as AB is related to AR.

The meaning and the consequences of B and AB have been examined in detail. The conditions in terms of various types of matrices describing B and AB multiports have been derived. Various rules have been established concerning the cascade connection of two multiports if one of them, and if both of them, possess one of the four network properties contained in the set R4.

It has been shown that multiport transformers and gyrators, which are special cases of the multiport converters and inverters considered in previous chapters, possess simultaneously two of the four network properties in the set R4.

It has also been shown that the determinant of the transmission matrix of (n+n)-ports possessing all of the four properties can only be +1 or -1.

Finally, it has been pointed out that, in the case of well-defined multiports described by real and constant parameters, all AR multiports are non-energic and all AB multiports are active.

It is believed that the results given in this chapter, not only clarify the conflict between the two existing definitions of anti-reciprocity, but can also be helpful in the treatment of various problems concerning non-reciprocal networks.

CHAPTER 9

A GENERALIZATION OF RECIPROCITY AND ANTI-RECIPROCITY

9.1 - INTRODUCTION

A previous chapter was concerned with a set of four network properties: reciprocity (R), anti-reciprocity (AR), bireciprocity (B) and anti-bireciprocity (AB). In the present chapter a generalization of these properties will be proposed. The generalization consists in the introduction of the concepts of generalized reciprocity, $R(\alpha)$, and generalized anti-reciprocity, $AR(\alpha)$, which are defined in terms of a parameter α.

It will be shown that the usual concept of reciprocity corresponds to $R(1)$, i.e., to generalized reciprocity with $\alpha = 1$; bireciprocity is interpreted as $R(-1)$. This is represented symbolically as

$$R = R(1) \qquad \text{and} \qquad B = R(-1)$$

It will also be shown that

$$AR = AR(1) \qquad \text{and} \qquad AB = AR(-1)$$

Various results established before in terms of R, AR, B and AB can be expressed in a considerably more general form in terms of $R(\alpha)$ and $AR(\alpha)$. These results include various rules concerning the cascade connection of multiports. Other consequences of the definitions of $R(\alpha)$ and $AR(\alpha)$ will be considered and the meaning of the two generalizations will be discussed in some detail.

9.2 GENERALIZED RECIPROCITY

It has been seen before that in the case of an (n+k)-port (Fig. 8.1) the equation defining reciprocity

$$I^t \hat{V} - V^t \hat{I} = 0 \qquad (9\text{-}1)$$

can be expanded as

$$I_1^t \hat{V}_1 + I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (9\text{-}2)$$

where subscripts 1 and 2 are associated with the sets of n and k ports, respectively.

The definition of generalized reciprocity is obtained from (9-2) by multiplying the terms associated with one of the two sets of ports by a scalar α which can, in general, be a rational function of the complex frequency variable s. If $\alpha \neq \pm 1$ it is necessary to specify whether α multiplies the terms associated with the set of n ports (subscript 1) or with the set of k ports (subscript 2). In the first case generalized reciprocity (also generalized reciprocal) will be denoted by $\overleftarrow{R}(\alpha)$, and in the second case by $\overrightarrow{R}(\alpha)$.(*) Both cases will be referred to collectively as $R(\alpha)$.

The defining equation for $\overrightarrow{R}(\alpha)$ is thus:

$$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - \alpha V_2^t \hat{I}_2 = 0 \qquad (9\text{-}3)$$

Dividing (9-3) by α

$$\frac{1}{\alpha} I_1^t \hat{V}_1 + I_2^t \hat{V}_2 - \frac{1}{\alpha} V_1^t \hat{I}_1 - V_2^t \hat{I}_2 = 0 \qquad (9\text{-}4)$$

and this shows that if a (n+k) port is $\overrightarrow{R}(\alpha)$ it is also $\overleftarrow{R}(\frac{1}{\alpha})$. This result will be represented symbolically by:

(*) If it is imagined that the set of n ports is on the left hand side and the set of k ports on the right hand side, then the arrow points towards the set of ports associated with the terms multiplied by α.

$$\vec{R}(\alpha) = \overleftarrow{R}(\tfrac{1}{\alpha}) \qquad (9\text{-}5)$$

The following discussion of $R(\alpha)$ will be done in terms of $\vec{R}(\alpha)$ only, since any result valid for $\vec{R}(\alpha)$ can immediately be translated into a similar result in terms of $\overleftarrow{R}(\alpha)$, by means of (9-5).

Equation (9-3), defining $R(\alpha)$, can be written in the more compact form

$$I^t \Theta_\alpha \hat{V} - V^t \Theta_\alpha \hat{I} = 0 \qquad (9\text{-}6)$$

where

$$\Theta_\alpha = \left[1_n \dot{+} \alpha 1_k \right]$$

i.e.,

$$\Theta_\alpha = \text{diag} \left(\underbrace{1,1,\ldots 1}_{n}, \underbrace{\alpha,\alpha,\ldots\alpha}_{k} \right)$$

$R(\alpha)$ contains as special cases the usual reciprocity (R), which corresponds to $\alpha = 1$, and also bireciprocity (B), which corresponds to $\alpha = -1$. This will be represented symbolically as

$$R = \vec{R}(1) = \overleftarrow{R}(1) \qquad (9\text{-}7)$$

$$B = \vec{R}(-1) = \overleftarrow{R}(-1) \qquad (9\text{-}8)$$

The constraints imposed by $\vec{R}(\alpha)$ on the hybrid matrix of an (n+k)-port will now be derived. It is convenient to use the notation appropriate for dealing with hybrid descriptions that was introduced in chapter 2.

E denotes an (n+k)-vector whose components are some currents and some voltages chosen among the (n+k)-currents and (n+k)-voltages at the ports of the (n+k)-port, in such a way that one (and only one) variable (voltage or current) of each port is included. The (n+k) remaining port variables form another vector F in which they are arranged with the port subscripts in the same order as in E (for example, if

$E = [\, i_1\ v_2\ v_3\ i_4\ v_5\ i_6 \,]^t$, then $F = [\, v_1\ i_2\ i_3\ v_4\ i_5\ v_6 \,]^t$). Any hybrid description will be of the form

$$E = H\,F \tag{9-9}$$

Equation (9-6) which defines $\vec{R}(\alpha)$ can be written, in terms of E and F, in the form of

$$E^t \Lambda \hat{F} - F^t \Lambda \hat{E} = 0 \tag{9-10}$$

where Λ is a diagonal matrix of dimension (n+k) whose elements Λ_{jj} are chosen in accordance with the nature of the elements e_j of E as indicated by the following rules:

(a) $e_j = i_p$, $p \leq n$ (i_p is a component of I_1) : $\Lambda_{jj} = 1$

(b) $e_j = i_p$, $p > n$ (i_p is a component of I_2) : $\Lambda_{jj} = \alpha$

(c) $e_j = v_p$, $p \leq n$ (v_p is a component of V_1) : $\Lambda_{jj} = -1$

(d) $e_j = v_p$, $p > n$ (v_p is a component of V_2) : $\Lambda_{jj} = -\alpha$

It is easy to see that in all four cases the contribution to the left hand side of equation (9-10) is in accordance with equation (9-3):

(a) $e_j\hat{f}_j - f_j\hat{e}_j = i_p\hat{v}_p - v_p\hat{i}_p \qquad (p \leq n)$

(b) $\alpha\, e_j\hat{f}_j - \alpha\, f_j\hat{e}_j = \alpha\, i_p\hat{v}_p - \alpha\, v_p\hat{i}_p \quad (p > n)$

(c) $-e_j\hat{f}_j + f_j\hat{e}_j = -v_p\hat{i}_p + i_p\hat{v}_p \qquad (p \leq n)$

(d) $-\alpha\, e_j\hat{f}_j + \alpha\, f_j\hat{e}_j = -\alpha\, v_p\hat{i}_p + \alpha\, i_p\hat{v}_p \quad (p > n)$

The $\vec{R}(\alpha)$ conditions in terms of a hybrid matrix H can be obtained by substituting (9-9) in (9-10):

$$F^t(H^t \Lambda - \Lambda H)\,\hat{F} = 0 \tag{9-11}$$

Since this equation must be valid for any F and $\hat{F}$, it follows that

$$\Lambda H = H^t \Lambda \tag{9-12}$$

which means, since $\Lambda = \Lambda^t$ that ΛH is a symmetric matrix.

Equation (9-12) can be written as

$$H = \Lambda^{-1} H^t \Lambda \tag{9-13}$$

For the special case where the hybrid matrix corresponds to $E = [I_1, V_2]^t$ (and, consequently $F = [V_1, I_2]^t$)

$$\Lambda = \begin{bmatrix} 1_n & 0 \\ 0 & -\alpha 1_k \end{bmatrix}$$

and (9-13) leads to:

$$H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} = \begin{bmatrix} 1_n & 0 \\ 0 & -\frac{1}{\alpha}1_k \end{bmatrix} \begin{bmatrix} H_{11}^t & H_{21}^t \\ H_{12}^t & H_{22}^t \end{bmatrix} \begin{bmatrix} 1_n & 0 \\ 0 & -\alpha 1_k \end{bmatrix}$$

$$= \begin{bmatrix} H_{11}^t & -\alpha H_{21}^t \\ -\frac{1}{\alpha}H_{12}^t & H_{22}^t \end{bmatrix}$$

This shows that

$$H_{11} = H_{11}^t \; ; \; H_{22} = H_{22}^t \; ; \; H_{12} = -\alpha H_{21}^t \tag{9-14}$$

The admittance matrix can be regarded as a special case of hybrid matrix, corresponding to $E = [I_1 \; I_2]^t$. In this case $\Lambda = \Theta_\alpha$ and it follows from (9-13) that

$$Y = \Theta_\alpha^{-1} \; Y^t \; \Theta_\alpha \tag{9-15}$$

or

$$Y_{11} = Y_{11}^t \; ; \quad Y_{22} = Y_{22}^t \; ; \quad Y_{12} = \alpha Y_{21}^t \tag{9-16}$$

Similarly, the impedance matrix can be regarded as the special case of hybrid matrix corresponding to $E = [V_1 \; V_2]^t$ and thus $\Lambda = -\Theta_\alpha$. From (9-13) it follows that

$$Z = \Theta_\alpha^{-1} \; Z^t \; \Theta_\alpha \tag{9-17}$$

or

$$Z_{11} = Z_{11}^{t} \quad ; \quad Z_{22} = Z_{22}^{t} \quad ; \quad Z_{12} = \alpha Z_{21}^{t} \tag{9-18}$$

The definition of $\vec{R}(\alpha)$ in terms of the scattering variables can easily be obtained. The current and voltage vectors, I and V, are expressed in terms of the normalized current and voltage vectors I' and V' by

$$I = R_o^{-\frac{1}{2}} I' \quad \text{and} \quad V = R_o^{\frac{1}{2}} V' \tag{9-19}$$

where

$$R_o^{\frac{1}{2}} = \text{diag}\,(r_{o1}^{\frac{1}{2}}, r_{o2}^{\frac{1}{2}} \ldots.)$$

and

$$R_o^{-\frac{1}{2}} = \text{diag}\,(r_{o1}^{-\frac{1}{2}}, r_{o2}^{-\frac{1}{2}} \ldots.)$$

Substitution of (9-19) in (9-6) leads to

$$I'^{t}\, \Theta_\alpha\, \hat{V}' - V'^{t}\, \Theta_\alpha\, \hat{I}' \tag{9-20}$$

The scattering variables $\mathcal{a}$ and $\mathcal{b}$ are related to I' and V' by

$$I' = \mathcal{a} - \mathcal{b} \quad \text{and} \quad V' = \mathcal{a} + \mathcal{b} \tag{9-21}$$

Substitution of (9-21) in (9-20) yields the defining equation of $\vec{R}(\alpha)$ in terms of the scattering variables

$$\mathcal{a}^{t}\, \Theta_\alpha\, \hat{\mathcal{b}} - \mathcal{b}^{t}\, \Theta_\alpha\, \hat{\mathcal{a}} = 0 \tag{9-22}$$

The scattering matrix is defined by

$$\mathcal{b} = S\, \mathcal{a} \tag{9-23}$$

The $\vec{R}(\alpha)$ conditions in terms of the scattering matrix are obtained by substitution of (9-23) in (9-22). This leads to

$$S = \Theta_\alpha^{-1}\, S^{t}\, \Theta_\alpha \tag{9-24}$$

The rules obtained in the previous chapter concerning the nature of an (n+k)-port N resulting from the cascade connection of an (n+q)-port N_1 with a (q+k)-port N_2 (Fig. 8-3), when N_1 and N_2 are R or B in the 4 possible combinations (Table 8-3a) can be generalized by making use of the new concept of $R(\alpha)$.

If (Fig. 8-3) N_1 is $\vec{R}(\alpha)$ and N_2 is $\vec{R}(\beta)$, then

$$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - \alpha V_2^t \hat{I}_2 = 0 \qquad (9\text{-}25)$$

$$- I_2^t \hat{V}_2 + \beta I_3^t \hat{V}_3 + V_2^t \hat{I}_2 - \beta V_3^t \hat{I}_3 = 0 \qquad (9\text{-}26)$$

Multiplication of (9-26) by $-\alpha$ leads to

$$\alpha I_2^t V_2 - \alpha V_2^t \hat{I}_2 = \alpha \beta I_3^t \hat{V}_3 - \alpha \beta V_3^t \hat{I}_3 \qquad (9\text{-}27)$$

and substitution of (9-27) in (9-25) yields

$$I_1^t \hat{V}_1 + \alpha\beta I_3^t \hat{V}_3 - V_1^t \hat{I}_1 - \alpha \beta V_3^t \hat{I}_3 = 0 \qquad (9\text{-}28)$$

which shows that N is $\vec{R}(\alpha\beta)$. This result will be expressed by the symbolic equation

$$\vec{R}(\alpha) + \vec{R}(\beta) \longrightarrow \vec{R}(\alpha\beta) \qquad (9\text{-}29)$$

The rules in Table 8-3a are obtained from (9-29) by making $\alpha = \pm 1$ and $\beta = \pm 1$.

Another result concerning the interconnection of multiports is the following: if an $\vec{R}(\alpha)$ (n+k)-port is connected to a reciprocal (R) k-port as shown in Fig. 9-1, the resulting n-port is reciprocal. This follows immediately from the definition of R, equation (9-1), and the definition of $\vec{R}(\alpha)$, equation (9-3). This result is applicable to those multiport converters and inverters which are $R(\alpha)$ since converters and inverters are associated with the type of multiport interconnection shown in Fig. 9-1.

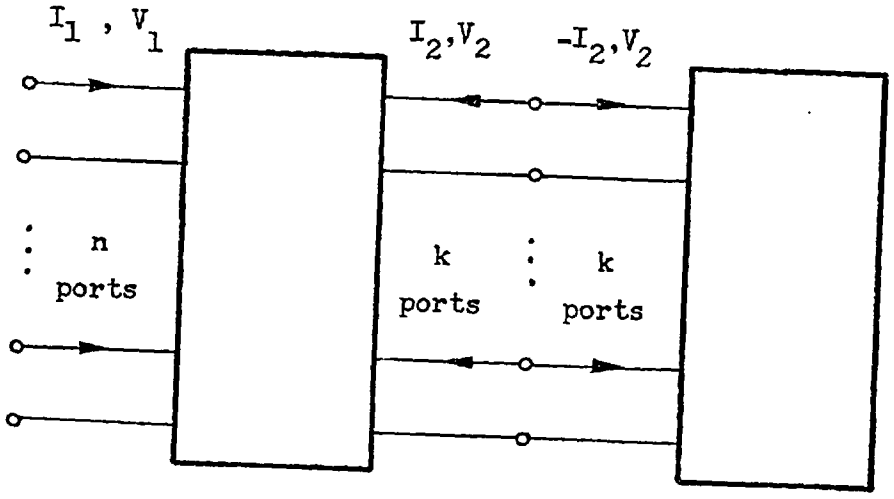


Fig. 9-1 : An (n+k)-port terminated by a k-port.

9.3 - GENERALIZED ANTI-RECIPROCITY

The equation defining anti-reciprocity is obtained from (9-1) by replacing the (-) sign by a (+) sign, leading to

$$I^t \hat{V} + V^t \hat{I} = 0 \qquad (9\text{-}30)$$

or, in an expanded form, for (n+k)-ports:

$$I_1^t \hat{V}_1 + I_2^t \hat{V}_2 + V_1^t \hat{I}_1 + V_2^t \hat{I}_2 = 0 \qquad (9\text{-}31)$$

The definition of generalized anti-reciprocity is obtained from (9-31) in the same way as the definition of generalized reciprocity was obtained from (9-2): the terms associated with one of the two sets of ports are multiplied by a scalar α. As for generalized reciprocity, there are two possibilities, represented by $\vec{AR}(\alpha)$ and $\overleftarrow{AR}(\alpha)$. These will be referred to collectively by $AR(\alpha)$.

The defining equation for $\vec{AR}(\alpha)$ is

$$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 + V_1^t \hat{I}_1 + \alpha V_2^t \hat{I}_2 = 0 \qquad (9\text{-}32)$$

Division of (9-32) by α, yields

$$\frac{1}{\alpha} I_1^t \hat{V}_1 + I_2^t \hat{V}_2 + \frac{1}{\alpha} V_1^t \hat{I}_1 + V_2^t \hat{I}_2 = 0 \qquad (9\text{-}33)$$

which shows that if a multiport is $\vec{AR}(\alpha)$ it is also $\overleftarrow{AR}(\frac{1}{\alpha})$. This is represented symbolically by

$$\vec{AR}(\alpha) = \overleftarrow{AR}(\frac{1}{\alpha}) \qquad (9\text{-}34)$$

A more compact version of (9-32) is obtained by making use of the matrix Θ_α defined before

$$I^t \Theta_\alpha \hat{V} + V^t \Theta_\alpha \hat{I} = 0 \qquad (9\text{-}35)$$

$AR(\alpha)$ includes, as special cases, anti-reciprocity (AR), which corresponds to $\alpha = 1$ and anti-bireciprocity (AB), which corresponds to $\alpha = -1$:

$$AR = \overrightarrow{AR}(1) = \overleftarrow{AR}(1) \tag{9-36}$$

$$AB = \overrightarrow{AR}(-1) = \overleftarrow{AR}(-1) \tag{9-37}$$

The $\overrightarrow{AR}(\alpha)$ conditions in terms of the hybrid matrices will now be derived.

Equation (9-35), which defines $\overrightarrow{AR}(\alpha)$, can be written, in terms of the hybrid variables E and F,

$$E^t \Gamma \hat{F} + F^t \Gamma \hat{E} = 0 \tag{9-38}$$

where Γ is a diagonal matrix of dimension (n+k) whose elements Γ_{jj} are 1 or α according to the following rule: both for $e_j = i_p$ and $e_j = v_p$,

$$\text{if } p \leq n \quad \text{then} \quad \Gamma_{jj} = 1$$

$$\text{if } p > n \quad \text{then} \quad \Gamma_{jj} = \alpha$$

The $\overrightarrow{AR}(\alpha)$ conditions in terms of a hybrid matrix H can be obtained after substitution of $E = HF$ in (9-38). The result is:

$$\Gamma H = - H^t \Gamma \tag{9-39}$$

or, equivalently,

$$H = - \Gamma^{-1} H^t \Gamma \tag{9-40}$$

For the hybrid matrix which corresponds to $E = \left[I_1 \; V_2 \right]^t$, $\Gamma = \Theta_\alpha$ and (9-40) becomes

$$H = - \Theta_\alpha^{-1} H^t \Theta_\alpha \tag{9-41}$$

or

$$H_{11} = - H_{11}^t \; ; \quad H_{22} = - H_{22}^t \; ; \quad H_{12} = - \alpha H_{21}^t \tag{9-42}$$

For both the admittance and impedance matrices, regarded as special hybrid matrices, $\Gamma = \Theta_\alpha$. The AR(α) conditions for the admittance matrix are, from (9-40),

$$Y = - \Theta_\alpha^{-1} Y^t \Theta_\alpha \tag{9-43}$$

or

$$Y_{11} = - Y_{11}^t ; \quad Y_{22} = - Y_{22}^t ; \quad Y_{12} = - \alpha Y_{21}^t \tag{9-44}$$

The conditions for the impedance matrix Z have the same form.

The definition of $\vec{AR}(\alpha)$ in terms of the normalized currents and voltages, obtained by substitution of (9-19) in (9-35) is:

$$I'^t \Theta_\alpha \hat{V}' + V'^t \Theta_\alpha \hat{I}' = 0 \tag{9-45}$$

Substitution of (9-21) in (9-45) leads to the definition of $\vec{AR}(\alpha)$ in terms of the scattering variables

$$\mathcal{a}^t \Theta_\alpha \hat{\mathcal{a}} - \mathcal{b}^t \Theta_\alpha \hat{\mathcal{b}} = 0 \tag{9-46}$$

From (9-46) the $\vec{AR}(\alpha)$ conditions in terms of the scattering matrix S are easily obtained as

$$\Theta_\alpha = S^t \Theta_\alpha S \tag{9-47}$$

which can also be written in the form of

$$S \Theta_\alpha^{-1} S^t \Theta_\alpha = 1 \tag{9-48}$$

The rules obtained in the previous chapter (Table 8-3b) concerning the cascade connection (Fig. 8-3) of AR and AB multiports can be generalized by using AR(α). It is easily shown that if an (n+q)-port N_1 is $\vec{AR}(\alpha)$ and a (q+k)-port N_2 is $\vec{AR}(\beta)$, then the (n-k)-port N resulting from the cascade connection of N_1 and N_2 (Fig. 8-3) is $\vec{AR}(\alpha\beta)$. This will be represented as:

$$\vec{AR}(\alpha) + \vec{AR}(\beta) = \vec{AR}(\alpha\beta) \tag{9-49}$$

This rule is analogous to the one that applies to the cascade of $\vec{R}(\alpha)$ multiports (9-29) and is proved in a similar way.

The rules in Table 8-3b are special cases of (9-49) for $\alpha = \pm 1$ and $\beta = \pm 1$.

Another result concerns the interconnection of multiports shown in Fig. 9-1. If an (n+k)-port which is $\vec{AR}(\alpha)$ is connected to an anti-reciprocal (AR) k-port, the resulting n-port is anti-reciprocal. This is very easy to see from the definitions of AR (equation (9-30)) and $\vec{AR}(\alpha)$ (equation (9-32)).

9.4 - THE SPECIAL CASE OF (n+n)-PORTS

An (n+n)-port can be described by a transmission matrix T defined by

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \qquad (9\text{-}50)$$

The $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ conditions in terms of the transmission matrix can be obtained after substitution of (9-50) in the defining equations (9-3) and (9-32). The derivation is very similar to that given in the previous chapter for the case of normal reciprocity (section 8.2). The results for $\vec{R}(\alpha)$ are

$$A^t C = C^t A \quad ; \quad B^t D = D^t B \quad ; \quad A^t D - C^t B = \alpha\, 1_n \qquad (9\text{-}51)$$

or

$$T\, \Phi\, T^t\, \Phi^t = \alpha\, 1_{2n} \qquad (9\text{-}52)$$

and for $\vec{AR}(\alpha)$

$$A^t C = -C^t A \quad ; \quad B^t D = -D^t B \quad ; \quad A^t D + C^t B = \alpha\, 1_n \qquad (9\text{-}53)$$

or

$$T\, \Psi\, T^t\, \Psi = \alpha\, 1_{2n} \qquad (9\text{-}54)$$

The auxiliary matrices Φ and Ψ have been used before; they

are defined as

$$\Phi = \begin{bmatrix} 0 & 1_n \\ -1_n & 0 \end{bmatrix} \quad \text{and} \quad \Psi = \begin{bmatrix} 0 & 1_n \\ 1_n & 0 \end{bmatrix}$$

For both $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ (n+n)-ports the value of the determinant of the transmission matrix is

$$\det T = \pm \alpha^n \qquad (9\text{-}55)$$

This result is easily obtained by taking the determinant of both sides of (9-52) and (9-54)

The rules (9-29) and (9-49) obtained in sections 9.2 and 9.3 apply to the cascade connection of an (n+q)-port with a (q+k)-port (Fig. 8-3) where n, q and k can be different. If n = q = k several other rules can be obtained which are a generalization of the rules obtained in the previous chapter and given in Table 8.4. The generalized rules are also given in terms of four matrices related to the transmission matrix T:

$$L_\Phi = T\,\Phi\,T^t\,\Phi^t \qquad M_\Phi = \Phi\,T^t\,\Phi^t\,T$$
$$L_\Psi = T\,\Psi\,T^t\,\Psi \qquad M_\Psi = \Psi\,T^t\,\Psi\,T$$

The rules are given in the following table (with reference to Fig. 8-3 with n = q = k):

N_1	N_2	N
L_ϕ	$\vec{R}(\alpha)$	α L_ϕ
L_ψ	$\vec{AR}(\alpha)$	α L_ψ
$\vec{R}(\alpha)$	M_ϕ	α M_ϕ
$\vec{AR}(\alpha)$	M_ψ	α M_ψ

The proof of these rules is entirely similar to the proof of the corresponding rules in the previous chapter (section 8.7).

9.5 - MISCELLANEOUS COMMENTS

Partition of ports into two sets

The definitions of both R(α) and AR(α) are, in general, associated with a partition of the ports into two sets. It is only for the case α = 1 that the variables associated with the ports in different sets are treated equally and therefore a partition is not necessary.

Equations (9-3) and (9-1) show that if in an $\vec{R}(\alpha)$ (n+k)-port all ports of one of the two sets are either open or short-circuited, the reduced multiport obtained is reciprocal (R); if two ports, one of each set, are selected for consideration, and all the other ports are rendered inaccessible by open or short-circuit terminations, the 2-port obtained is $\vec{R}(\alpha)$.

In a similar way, equations (9-32) and (9-30) show that, in an $\vec{AR}(\alpha)$ multiport, ports of the same set form an anti-reciprocal (AR) reduced multiport and any two ports of different set form an $\vec{AR}(\alpha)$ 2-port.

The meaning of α

The $\vec{R}(\alpha)$ conditions in terms of the various matrices show that any 2-port is $\vec{R}(\alpha)$ with

$$\alpha = \frac{y_{12}}{y_{21}} = \frac{z_{12}}{z_{21}} = -\frac{h_{12}}{h_{21}} = ad - bc \qquad (9\text{-}56)$$

The $\vec{AR}(\alpha)$ conditions show that an $\vec{AR}(\alpha)$ 2-port must satisfy one of the following equivalent conditions

$$y_{11} = y_{22} = 0 \;;\; z_{11} = z_{22} = 0 \;;\; h_{11} = h_{22} = 0 \;;\; ac = bd = 0 \qquad (9\text{-}57)$$

If these conditions are satisfied the 2-port is $\vec{AR}(\alpha)$ with

$$\alpha = -\frac{y_{12}}{y_{21}} = -\frac{z_{12}}{z_{21}} = -\frac{h_{12}}{h_{21}} = ad + bc \qquad (9\text{-}58)$$

In contrast with 2-ports, not all (n+k)-ports are R(α). An (n+k)-port with $n > 1$ or $k > 1$ is R(α) only if the relevant conditions are satisfied.

The parameter α will now be examined in the context of the modelling of 2-ports by the cascade connection of a reciprocal with a non-reciprocal 2-port. One such model, first proposed in [102], and also discussed in [2], is obtained by noting that the admittance description of a 2-port

$$i_1 = y_{11} v_1 + y_{12} v_2 \qquad (9\text{-}59a)$$

$$i_2 = y_{21} v_1 + y_{22} v_2 \qquad (9\text{-}59b)$$

can, equivalently, be written in the form

$$i_1 = y_{11}v_1 + (y_{12}y_{21})^{\frac{1}{2}} \left(\frac{y_{12}}{y_{21}}\right)^{\frac{1}{2}} v_2 \qquad (9\text{-}60a)$$

$$i_2 = (y_{21}y_{12})^{\frac{1}{2}} \left(\frac{y_{21}}{y_{12}}\right)^{\frac{1}{2}} v_1 + y_{22}\, v_2 \qquad (9\text{-}60b)$$

These equations can be interpreted as describing the cascade connection of a reciprocal 2-port, described by

$$i_1 = y_{11}v_1 + (y_{12}y_{21})^{\frac{1}{2}}\, v' \qquad (9\text{-}61a)$$

$$i' = (y_{12}y_{21})^{\frac{1}{2}}\, v_1 + y_{22}\, v' \qquad (9\text{-}61b)$$

with a non-reciprocal 2-port described by

$$v' = \left(\frac{y_{12}}{y_{21}}\right)^{\frac{1}{2}} v_2 \qquad (9\text{-}62a)$$

$$i_2 = \left(\frac{y_{21}}{y_{12}}\right)^{\frac{1}{2}} i' \qquad (9\text{-}62b)$$

as shown in Fig. 9-2.

The description of the non-reciprocal 2-port, (9-62), written in the form of

$$v' = \alpha^{\frac{1}{2}}\, v_2 \qquad (9\text{-}63a)$$

$$i' = \alpha^{\frac{1}{2}}\, i_2 \qquad (9\text{-}63b)$$

where

$$\alpha = (y_{12}/y_{21})^{\frac{1}{2}} \qquad (9\text{-}64)$$

shows that it is a power amplifier with a power gain α, in the reverse direction, if the original two port is $\vec{R}(\alpha)$. It can also be observed, from the hybrid description of the non-reciprocal 2-port

$$\begin{bmatrix} -i' \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 & -\alpha^{\frac{1}{2}} \\ \alpha^{-\frac{1}{2}} & 0 \end{bmatrix} \begin{bmatrix} v' \\ i_2 \end{bmatrix} \qquad (9\text{-}65)$$

that it is $\vec{R}(\alpha)$ (this is not surprising in view of the combination rule (9-29)). This non-reciprocal 2-port has been designated "anti-

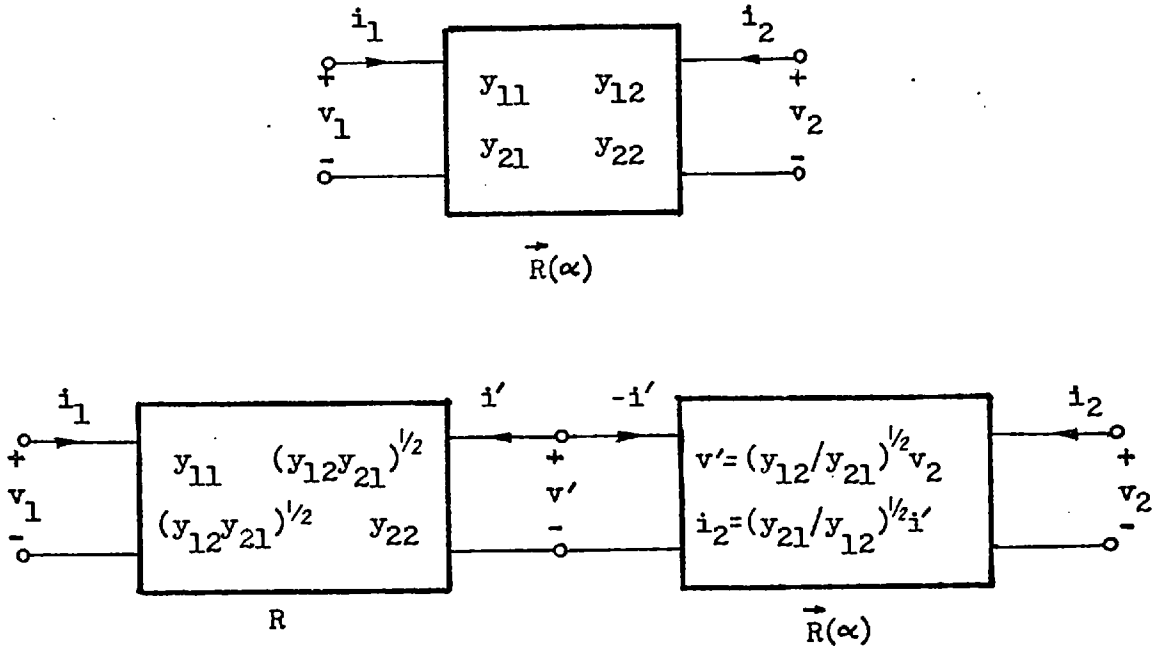


Fig. 9-2 : Model of a non-reciprocal 2-port using an 'anti-reciprocal transition'.

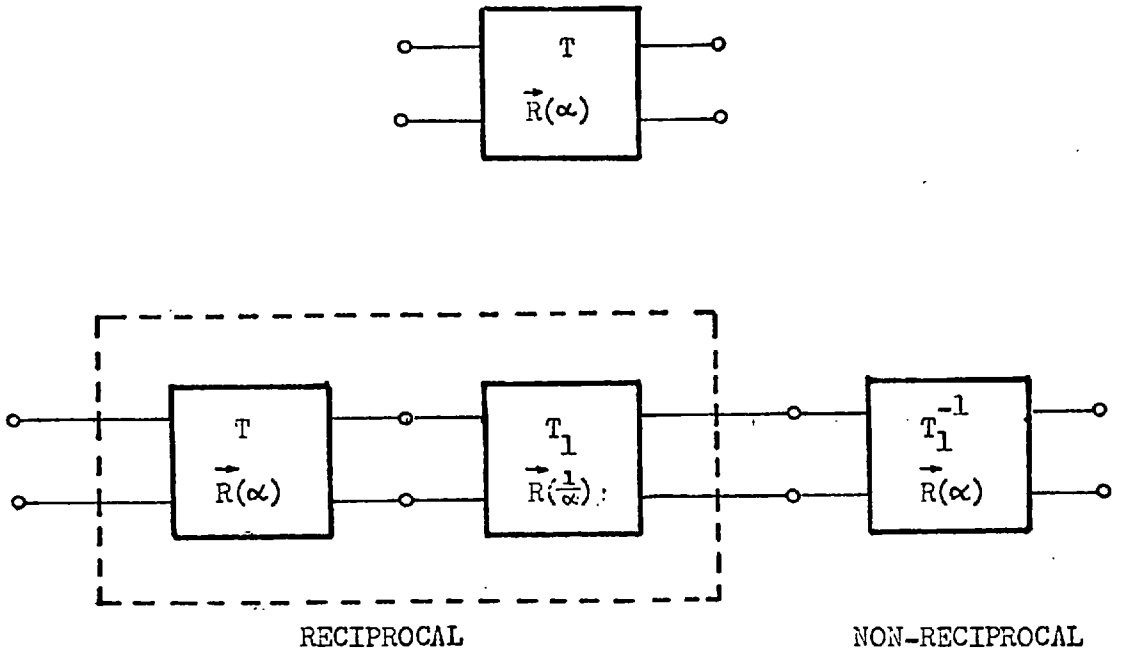


Fig. 9-3 : Model of a non-reciprocal 2-port.

reciprocal transition". It is interesting to note that it is not anti-reciprocal in the sense of any of the two definitions existing in the literature (AR and B restricted for 2-ports, as discussed in the previous chapter). It is, however, anti-reciprocal in the sense of the generalized definition proposed here: it is $\vec{AR}(\alpha)$ with $\alpha = (y_{12}/y_{21})^{\frac{1}{2}}$, as shown by the hybrid matrix in (9-65) (in fact this 2-port is both $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$, with α given by (9-64)).

It may be of interest to note that the decomposition in Fig. 9-2 is not unique if the only requirement is that one of the two ports in the model be reciprocal. A 2-port (with a transmission matrix T) is not affected by the cascade with two others (Fig. 9-3) if their transmission matrices are T_1 and T_1^{-1}. If the original 2-port is $\vec{R}(\alpha)$ and if T_1 is chosen in such a way that the corresponding 2-port is $\vec{R}(1/\alpha)$, i.e., $a_1d_1 - b_1c_1 = 1/\alpha$, then, in view of the combination rule (9-29) the 2-port resulting from the cascade of T and T_1 is reciprocal and can thus be taken as the reciprocal part in the model (see Fig. 9-3).

Unilateral (n+k)-ports

Unilateral 2-ports are defined by the following equivalent conditions

$$y_{12} = 0 \quad , \quad z_{12} = 0 \quad , \quad h_{12} = 0 \tag{9-66}$$

The $\vec{R}(\alpha)$ conditions (9-56) show that any unilateral 2-port is $\vec{R}(0)$ and vice versa.

If unilateral (n+k)-ports are defined by the matrix version of equations (9-66)

$$Y_{12} = 0 \quad , \quad Z_{12} = 0 \quad , \quad H_{12} = 0 \tag{9-67}$$

then it can be stated that any (n+k)-port is unilateral if it is $\vec{R}(0)$, since the $\vec{R}(\alpha)$ conditions for $\alpha = 0$ include (9-67). It should be noted, however that, apart from 2-ports, unilateral (n+k)-ports are not necessarily $\vec{R}(0)$.

Similarly it can be seen that all $\vec{AR}(0)$ multiports are unilateral, but unilateral multiports (including 2-ports) are not necessarily $\vec{AR}(0)$.

Multiport Converters and Inverters

It will now be shown that some multiport converters are simultaneously $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ and that some multiport inverters are simultaneously $\vec{R}(\alpha)$ and $\vec{AR}(-\alpha)$ (for the same value of α).

Equations (9-16) and (9-44) show that a multiport with admittance description can only be both $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ if the admittance matrix is zero. A similar conclusion can be reached with respect to the impedance matrix. However, if a multiport has the hybrid description for which (9-14) and (9-42) were derived, it will be both $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ if

$$H_{11} = 0 \quad ; \quad H_{22} = 0 \quad : \quad H_{12} = -\alpha H_{21}^{t} \qquad (9\text{-}68)$$

Such a multiport is a special case of multiport converter; if $\alpha = 1$ it is a positive transformer and if $\alpha = -1$ it is a negative transformer (multiport positive and negative transformers have been discussed in the previous chapter, section 8.8).

Equations (9-14) and (9-42) show that the requirement of simultaneous $\vec{R}(\alpha)$ and $\vec{AR}(-\alpha)$ leads to a zero hybrid matrix (the hybrid matrix considered is the one for which (9-14) and (9-42) are valid). If the multiport possesses an admittance matrix, equations (9-16) and (9-44) show that it is both $\vec{R}(\alpha)$ and $\vec{AR}(-\alpha)$ if

$$Y_{11} = 0 \quad ; \quad Y_{22} = 0 \quad ; \quad Y_{12} = \alpha Y_{21}^{t} \tag{9-69}$$

A similar result is obtained if the impedance matrix is considered:

$$Z_{11} = 0 \quad ; \quad Z_{22} = 0 \quad ; \quad Z_{12} = \alpha Z_{21}^{t} \tag{9-70}$$

The multiports described by (9-69) or (9-70) are special cases of multiport inverters. If $\alpha = -1$ they are positive gyrators, and if $\alpha = +1$ they are negative gyrators (multiport positive and negative gyrators have been considered in section 8.8 of the previous chapter).

On the possibility of a further generalization

The definition of $R(\alpha)$ was obtained from the definition of R by multiplying two of the terms in (9-2) by a scalar α. It seems reasonable to investigate the possibility of a further generalization, which might be obtained by multiplying each term in (9-2) by a different scalar coefficient (one term can always be assumed to have coefficient 1):

$$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 + \beta V_1^t \hat{I}_1 + \gamma V_2^t \hat{I}_2 = 0 \tag{9-71}$$

The constraints imposed by (9-71) on the admittance matrix are

$$Y_{11}^{t} = \beta Y_{11} \tag{9-72a}$$

$$\alpha Y_{22}^{t} = \gamma Y_{22} \tag{9-72b}$$

$$Y_{12}^{t} = \gamma Y_{21} \tag{9-72c}$$

$$\alpha Y_{21}^{t} = \beta Y_{12} \tag{9-72d}$$

If equation (9-72d) is written in the form of

$$Y_{12}^{t} = \frac{\alpha}{\beta} Y_{21}$$

and compared with (9-72c) it is seen that either

$$\gamma = \frac{\alpha}{\beta} \tag{9-73}$$

or

$$Y_{12} = Y_{21}^{t} = 0 \tag{9-74}$$

Since (9-74) means absence of transmission between the two sets of ports, it will be assumed that the three coefficients are related according to (9-73).

For networks with a hybrid description

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

the constraints imposed by (9-71) are

$$H_{11}^{t} = \beta H_{11} \tag{9-75a}$$

$$\alpha H_{22} = \gamma H_{22}^{t} \tag{9-75b}$$

$$H_{12}^{t} = -\alpha H_{21} \tag{9-75c}$$

$$\beta H_{12} = -\gamma H_{21}^{t} \tag{9-75d}$$

If (9-75d) is written in the form of

$$H_{12}^{t} = -\frac{\gamma}{\beta} H_{21}$$

and compared with (9-75c) it is seen that either

$$\gamma = \alpha \beta \tag{9-76}$$

or

$$H_{12} = H_{21}^{t} = 0 \tag{9-77}$$

Since (9-77) means that there is no transmission between ports of different sets, it will be assumed that (9-76) applies.

Equations (9-73) and (9-76) must be accepted together if it is postulated that (9-71) must be applicable to (n+k)-ports with trans-

mission between the two sets of ports, both when the multiports possess an admittance description, and when they possess a hybrid description. From (9-73) and (9-76) it follows that $\beta = \pm 1$. If $\beta = 1$ then $\gamma = \alpha$ and (9-71) coincides with (9-32) which is the defining equation of $\vec{AR}(\alpha)$. If $\beta = -1$, then $\gamma = -\alpha$ and (9-71) is reduced to the form of (9-3) which defines $\vec{R}(\alpha)$. This means that the two cases discussed in this chapter, $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$, are the only interesting cases contained in an equation of the form (9-71).

9.6 CONCLUSIONS

It has been shown that the definitions of reciprocity (R) and anti-reciprocity (AR) can be generalized in such a way that the two network properties introduced in the previous chapter, bireciprocity (B) and anti-bireciprocity (AB), become special cases of generalized reciprocity, $R(\alpha)$, and generalized anti-reciprocity, $AR(\alpha)$, respectively. The various rules concerning the cascade connection of multiports can be expressed in terms of $R(\alpha)$ and $AR(\alpha)$; the class of multiports to which these rules apply has thus been significantly extended. The basic results concerning $R(\alpha)$ and $AR(\alpha)$ are summarized in Table 9-1.

Various questions have been examined, which provide a better insight into the meaning of the generalization proposed here. It has been pointed out that some multiport converters are both $\vec{R}(\alpha)$ and $\vec{AR}(\alpha)$ and that some multiport inverters are simultaneously $\vec{R}(\alpha)$ and $\vec{AR}(-\alpha)$, for the same value of α.

Finally, it has been shown that $R(\alpha)$ and $AR(\alpha)$ are the most general network properties with interesting consequences which can

TABLE 9.1 : Generalized Reciprocity and Generalized Anti-reciprocity.

	GENERALIZED RECIPROCITY $\vec{R}(\alpha) = \overleftarrow{R}(\alpha^{-1})$	GENER. ANTI-RECIPROCITY $\vec{AR}(\alpha) = \overleftarrow{AR}(\alpha^{-1})$
DEFINITION	$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 - V_1^t \hat{I}_1 - \alpha V_2^t \hat{I}_2 = 0$	$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 + V_1^t \hat{I}_1 + \alpha V_2^t \hat{I}_2 = 0$
SPECIAL CASES	$\vec{R}(1) = R$; $\vec{R}(-1) = B$	$\vec{AR}(1) = AR$; $\vec{AR}(-1) = AB$
ADMITTANCE MATRIX	$Y_{11}=Y_{11}^t$; $Y_{22}=Y_{22}^t$; $Y_{12}=\alpha Y_{21}^t$	$Y_{11}=-Y_{11}^t$; $Y_{22}=-Y_{22}^t$; $Y_{12}=-\alpha Y_{21}^t$
HYBRID MATRIX	$H_{11}=H_{11}^t$; $H_{22}=H_{22}^t$; $H_{12}=-\alpha H_{21}^t$	$H_{11}=-H_{11}^t$; $H_{22}=-H_{22}^t$; $H_{12}=-\alpha H_{21}^t$
TRANSMISSION MATRIX (n = k)	$A^tC=C^tA$; $B^tD=D^tB$; $A^tD-C^tB=\alpha 1_n$	$A^tC=-C^tA$; $B^tD=-D^tB$; $A^tD+C^tB=\alpha 1_n$
CASCADE (Fig. 8.3) $(n+q) + (q+k) \rightarrow (n+k)$	$\vec{R}(\alpha) + \vec{R}(\beta) \rightarrow \vec{R}(\alpha\beta)$	$\vec{AR}(\alpha) + \vec{AR}(\beta) \rightarrow \vec{AR}(\alpha\beta)$
CASCADE $(n+n) + (n+n) \rightarrow (n+n)$	$L_\phi + \vec{R}(\alpha) \rightarrow \alpha L_\phi$	$L_\psi + \vec{AR}(\alpha) \rightarrow \alpha L_\psi$
	$\vec{R}(\alpha) + M_\phi \rightarrow \alpha M_\phi$	$\vec{AR}(\alpha) + M_\psi \rightarrow \alpha M_\psi$

be defined by an equation of the form:

$$I_1^t \hat{V}_1 + \alpha I_2^t \hat{V}_2 + \beta V_1^t \hat{I}_1 + \delta V_2^t \hat{I}_2 = 0$$

where α, β and δ are scalar coefficients.

CHAPTER 10

CONCLUSIONS

10.1 - SUMMARY OF THE MAIN RESULTS

The conclusions of the research reported in this thesis have already been presented in the last sections of each chapter. The main results will now be reviewed.

A generalization to multiports of the concepts of 2-port immittance conversion and inversion has been proposed. The conditions which the matrix description of multiport converters and inverters must satisfy have been derived from the proposed definitions. It is pointed out that whereas 2-port admittance converters or inverters are also impedance converters or inverters, and vice versa, this is not generally true for the multiport converters and inverters proposed here. However, the inclusion in the definitions of the requirement for simultaneous admittance and impedance conversion or inversion would be undesirably restrictive.

A further generalization has also been suggested: the concept of multiport 'hybrid converter' is introduced and it is shown that it includes, as special cases, both converters and inverters (and both the admittance and the impedance types).

Most of the circuits proposed for the simulation of floating inductors can be interpreted as 3-port admittance (and not impedance) converters and inverters. Multiport transformers and gyrators are also special cases of multiport converters and inverters. It is believed that the theory of multiport conversion and inversion that has been

developed here not only provides a better understanding of these important special cases but is also useful as a contribution to general multiport theory.

It has been shown how any well-defined multiport can be realized as an interconnection of 2-ports. This is applied to the realization of multiport converters and inverters. The limitations arising from (a) the need to guarantee that after the 2-ports are interconnected all terminal-pairs still behave as ports, and (b) the existence of a ground terminal in all the 2-ports, in the case of active realization, are discussed. The possibility of using 2-port converters and inverters in which the ports have a common terminal that can be grounded is investigated.

A comparative study of various realizations of 3-port converters and inverters suitable for the simulation of floating inductors has been carried out. Although all 3-port inverters have the same port description, different realizations may have different terminal descriptions. A classification of 3-port inverters for floating inductor simulation based on their terminal description is presented. A parallel classification is also applied to the 3-port converters. It is shown that some circuits that are apparently unrelated belong to the same class. It is believed that the proposed classification is useful in providing greater insight into various methods of floating inductor simulation.

A well known method of floating inductor simulation uses two grounded gyrators. The resulting circuit can be interpreted as a 4-terminal, 3-port admittance inverter. It is shown that when two specific gyrator circuits, each with two operational amplifiers, are used, one of the operational amplifiers becomes redundant and can

be suppressed, thus leading to a 3-port inverter with three operational amplifiers. There are four ways of associating the two gyrators and, in each case, one amplifier can be suppressed. Thus, a family of four different circuits is obtained. One of these circuits is known; the other three are believed to be novel.

The realization of some types of inverters using a minimum number of active components has been investigated. In particular, minimal realizations of the 2-port positive inverter are discussed in detail. It is proved that for a grounded 2-port (i.e. a 2-port where both ports are grounded) containing resistors and one operational amplifier, the admittance parameters are subject to the following constraints: (a) if $y_{11} = 0$ then $y_{21} \leq 0$, and (b) if $y_{22} = 0$ then $y_{12} \leq 0$. This result has various consequences regarding the realization of different types of inverters; one of these consequences is that it is not possible to realize a grounded positive inverter with only one operational amplifier (although it is possible to realize single-amplifier positive inverters with only one grounded port). It has also been proved that it is not possible to realize a grounded positive inverter with only one ideal transistor (it is not known whether it is possible to realize a single-transistor positive inverter with only one grounded port). These conclusions are not only useful by themselves as results concerning the minimal realization of 2-port positive inverters but have also consequences regarding 3-port inverters: they show that the method of floating inductor simulation using two grounded positive inverters requires more than two active components (operational amplifiers or transistors).

Converters and inverters have often been associated with the discussion of reciprocity and non-reciprocity (the absence of reciprocity). The gyrator, in particular, has always been regarded as possessing a kind of extreme non-reciprocity or anti-reciprocity. Two different definitions of anti-reciprocity can be found in the literature. Surprisingly, the incompatibility of these two definitions does not seem to have been noticed before. An investigation started with the aim of clarifying this situation led to various new results. One of the definitions, so far restricted to 2-ports, is generalized for multiports. This generalized version, together with the other definition of anti-reciprocity and the definition of reciprocity, suggests the introduction of a fourth network property related to the concept of reciprocity in order to obtain a 'complete pattern'. The set of four properties is referred to as R4. The meaning of the new definitions is examined in some detail. Various rules concerning the cascade connection of two multiports, where one or both of them possess one of the four properties, are presented. It is shown that the only 'non-degenerate' multiports possessing simultaneously two properties belonging to the set R4 are special cases of multiport converters or inverters.

It has also been shown that, although in some respects the set of four properties is 'complete', a further extension is possible. Both reciprocity and one of the types of anti-reciprocity are given a generalized definition in terms of a scalar parameter α. The two generalized properties, designated as $R(\alpha)$ and $AR(\alpha)$, contain as notable special cases the four properties forming the set R4. The rules, mentioned above, concerning the cascade connection of two multiports become special cases of more general rules in terms of $R(\alpha)$ and $AR(\alpha)$.

10.2 - SUGGESTIONS FOR FURTHER WORK

A number of unsolved problems related to the subject of this thesis will now be mentioned.

It is believed that the theory of multiport admittance and impedance converters and inverters (and also the concept of hybrid converter) presented in this thesis may be useful in connection with multiport synthesis. Since various methods of multiport synthesis that can be found in the literature are given in terms of scattering parameters, it might be useful to develop a theory of multiport converters and inverters in terms of the scattering variables.

Most of the realizations of multiport converters and inverters considered in this thesis are based on the use of 2-port converters or inverters (other methods have only been considered in the case of 3-port admittance converters and inverters for floating inductance simulation). It might be of interest to investigate other types of realization of multiport converters and inverters, for instance using nullors or using controlled sources.

The classification of 3-port converters and inverters for floating inductor simulation proposed in this thesis was established under the assumption that the converters and inverters have ideal performance. It is possible that circuits belonging to the same class have also common features concerning their non-ideal behaviour. It is believed that this question deserves further investigation.

A comparison between converter and inverter methods of floating inductor simulation, taking into account the non-ideal performance, appears to be another interesting problem. For this comparison, 3-port inverters and converters realized with two grounded 2-port inverters and with two grounded 2-port converters, respectively, might be considered.

There is a number of questions concerning minimal realizations of converters and inverters which remain unanswered. Two such questions have already been pointed out in chapter 7. One of these concerns the realization of positive inverters with resistors and one ideal transistor; the other refers to the realization of 3-port inverters for floating inductor simulation with two operational amplifiers. Another unsolved question, concerning converters (rather than inverters) with a minimum number of active components will now be mentioned.

In connection with the method of simulation of LC ladder filters by impedance scaling (see chapter 3, section 3.2) one-ports with admittance proportional to s^2 (super-capacitors) or proportional to s^{-2} (super-inductors) are required. Converters with a conversion factor proportional to s^{-2} or to s^{-1} terminated by a resistor or terminated by a capacitor, respectively, can be used to realize super-capacitors; the first type of converters can also be used to realize super-inductors. In some versions of the impedance scaling method, converters with a conversion factor proportional to s^{-1} or s^{-2} are indispensable for impedance matching different sections of a filter. Such converters can be realized with 2 operational amplifiers, for instance using the circuit of Fig. 3-16, in chapter 3. It would be of interest to know whether realizations with only one amplifier are possible.(*)

(*) It may be noted that it has recently been shown [98] that super-capacitors and super-inductors can be realized with only one operational amplifier and the minimum number of capacitors required, wich is 2 (earlier circuits with one amplifier and more than two capacitors had been proposed in [89]); the circuits in [98] and [89], however, are not interpretable as converters.

Finally, in connection with the investigation of anti-reciprocity, an unsolved question concerns the value of the determinant of the transmission matrix T of (n+n)-ports which possess one of the four properties considered in chapter 8; it would be of interest to prove or disprove the conjecture presented in section 8.7. This question can be formulated in a more general form by considering the det T of (n+n)-ports that possess generalized reciprocity, $R(\alpha)$, or generalized anti-reciprocity, $AR(\alpha)$.

REFERENCES

[1] N. BALABANIAN, T. A. BICKART, Electrical Network Theory, Wiley, 1969.

[2] R. SPENCE, Linear Active Networks, Wiley 1970.

[3] W. KLEIN, Grundlagen der Theorie Elektricher Schaltungen, Teil 1: Mehrtortheorie, Akademie Verlag, Berlin, 1970.

[4] R. W. NEWCOMB, Linear Multiport Synthesis, Mc Graw-Hill, 1966.

[5] V. BELEVITCH, Classical Network Theory, Holden-Day, 1968.

[6] H. J. CARLIN, A. B. GIORDANO, Network Theory, Prentice-Hall, 1964.

[7] B. D. H. TELLEGEN, On Nullators and Norators, IEEE Trans. Circuit Theory, vol. CT-13, pp. 466-468, Dec. 1966.

[8] H. J. CARLIN, Singular Network Elements, IEEE Trans. Circuit Theory, vol. CT-11, pp. 67-72, Mar. 1964.

[9] H. J. CARLIN, D. C. YOULA, Network Synthesis with Negative Resistors, Proc. IRE, vol. 49, pp. 907-920, May 1961.

[10] A. ANTONIOU, New Gyrator Circuits Obtained by Using Nullors, Electron. Letters, vol. 4, pp. 87-88, Mar. 1968.

[11] A. ANTONIOU , Three-Terminal Gyrator Circuits Using Operational Amplifiers, Electron. Letters, vol. 4, pp. 591-592, Dec. 1968.

[12] A. ANTONIOU, Realization of Gyrators Using Operatinal Amplifiers and Their Use in RC-Active Network Synthesis, Proc. IEE, vol. 116, pp. 1838-1850, Nov. 1969.

[13] L. T. BRUTON, A Study of Circuit Techniques for Use in Microelectronic Communication and Control Systems, Ph. D. Thesis, Univ. of Newcastle Upon Tyne, 1969.

[14] J. BENDIK, Equivalent Gyrator Networks with Nullators and Norators, IEEE Trans. Circuit Theory, vol. CT.-14,p. 98, Mar. 1967.

[15] A. C. DAVIES, Nullator-Norator Equivalent Networks for Controlled Sources, Proc. IEEE, vol. 55, pp. 772-773, May 1967.

[16] A. C. DAVIES, Matrix Analysis of Networks Containing Nullators and Norators, Elect. Letters, vol. 2, pp. 48-49, Feb. 1966.

[17] E. A. GUILLEMIN, On the Analysis and Synthesis of Single-Element-Kind Networks, IRE Trans. Circuit Theory, vol. CT-7, pp. 303-312, Sep. 1960.

[18] E. A. GUILLEMIN, On the Realization of an n^{th} Order G Matrix, IRE Trans. Circuit Theory, vol. CT-8, pp. 318-323, Sep. 1961.

[19] L. WEINBERG, Network Analysis and Synthesis, Mc Graw-Hill, 1962.

[20] E. S. KUH, R. A. ROHRER, Theory of Linear Active Networks, Holden-Day, 1967.

[21] P. PENFIELD, R. SPENCE, S. DUINKER, Tellegen's Theorem and Electrical Networks, MIT Press, 1970.

[22] W.E. HEINLEIN, W.H.HOLMES, Active Filters for Integrated Circuits, Prentice-Hall, 1974.

[23] W. SARAGA ,Frequency-Selective Networks Suitable for Microelectronic Realization, Jour. Science and Technology, vol. 38, pp. 128-138. 1971.

[24] E. A. GUILLEMIN, Synthesis of RC-Networks, J. Math. and Phys., vol. 28, pp. 22-42, 1949.

[25] K. L. SU, B. J. DASHER, A Solution to the Approximation Problem for RC Lowpass Filters, Proc. IRE, vol.44, pp. 914-920, July 1956.

[26] K. L. SU, Synthesis of RC Bandpass Filters, IEEE Trans. Circuit Theory, vol. CT-14, pp. 140-148, June 1967.

[27] C. F. KURTH, Analog and Digital Filtering in Multiplex Communication Systems, IEEE Trans. Circuit Theory, vol. CT-20, pp. 408-415, July 1973.

[28] J. G. LINVILL, RC Active Filters, Proc. IRE, vol. 42, pp.555-564,

Mar. 1954.

[29] I.W. SANDBERG, Synthesis of Driving Point Impedance with Active RC Networks, Bell Syst. Tech. Jour., vol.39, pp. 947-962, July 1960.

[30] W. SARAGA, A Contribution to Active RC Network Synthesis, in Recent Developments in Network Theory (ed. S. R. Deards), Pergamom Press, 1963.

[31] R. P. SALLEN, E.L. KEY, A Practical Method of Designing RC Active Filters, IRE Trans. Circuit Theory, vol. CT-2, pp. 78-85, Mar 1955.

[32] S. K. MITRA, Analysis and Synthesis of Linear Active Networks, Wiley, 1969.

[33] H. J. ORCHARD, Inductorless Filters, Electron. Letters, vol. 2, pp. 224-225, Sep. 1966.

[34] H. J. ORCHARD, D. F. SHEAHAN, Inductorless Bandpass Filters, IEEE Jour. Solid State Circuits, vol. SC-5, pp. 108-118, June 1970.

[35] W.H. HOLMES, W. E. HEINLEIN, S. GRÜTZMANN, Sharp-Cutoff Low-Pass Filters Using Floating Gyrators, IEEE Jour. Solid State Circuits, vol. SC-4, pp. 38-50, Feb. 1969.

[36] J. VALIHORA, J. T. LIM, L. T. BRUTON, The Feasibility of Active Filtering in Frequency Division Multiplex Systems, Proc. IEEE Int. Symp. Circuits and Systems, pp. 121-125, San Francisco, 1974.

[37] J. GORSKI-POPIEL, RC-Active Synthesis Using Positive-Immittance Converters, Electron. Letters, vol. 3, pp. 381-382,Aug.1967.

[38] A. G. J. HOLT, R. LINGGARD,The Multiterminal Gyrator, Proc. IEEE, vol. 56, pp. 1354-1355, Aug. 1967.

[39] A. G. J. HOLT,R. L. LINGGARD, Multiterminal Gyrator, Proc. IEE, vol. 117, pp. 1591-1598, Aug. 1970.

[40] L. T. BRUTON, Network Transfer Functions Using the Concept of Frequency-Dependent Negative Resistence, IEEE Trans. Circuit Theory, vol. CT-16, pp. 406-408, Aug. 1969.

[41] R. JEFFERS, D. HAIGH, Active RC Lowpass Filters for F. D. M. and P.C. M. Systems, Proc. IEE, vol. 120, pp.945-953, Sep. 1973.

[42] D.G. HAIGH, W. SARAGA, Practical LC Filter Simulation Techniques for the Design of Active RC Band-Pass Filters, Proc. 1st European Conf. Circ. Theory and Design, pp. 336-341, London, July 1974.

[43] W. SARAGA, D. G. HAIGH, R. G. BARKER, Microelectronic Active RC Channel Band-Pass Filters for FDM SSB Telephone Systems, Proc.European Conf. Circ. Theory and Design, Genoa, Sep.1976.

[44] F. E. J. GIRLING, E. F. GOOD, The Leap Frog Feedback Filter, Royal Radar Establishment Memorandum 1176, Sep. 1955.

[45] K. R. LAKER, M. S. GHAUSI, A Comparison of Active Multiple-Loop Feedback Techniques for Realizing High-Order Bandpass Filters,IEEE Trans. Circuits and Systems, vol. CAS-21, pp.774-783, Nov. 1974.

[46] K. R. LAKER, M. S. GHAUSI, J. J. KELLY, Minimum Sensitivity Active (Leapfrog) and Passive Ladder Bandpass Filters, IEEE Trans. Circuits and Systems, vol. CAS-22, pp. 670-677, Aug. 1975.

[47] P. O. BRACKET, A. S. SEDRA, Direct SGF Simulation of LC Ladder Networks with Applications to Active Filter Design, IEEE Trans.Circuits and Systems, vol. CAS-23, pp. 61-67, Feb. 1976.

[48] D. J. PERRY, Multifarious Multifeedback Filters, IEE Colloquium Digest no. 1976/33, May 1976.

[49] A. G. CONSTANTINIDES, G. HARITANTIS, Wave Active Filters, Electron. Letters, vol. 11, pp. 254-256, June 1975.

[50] H. WUPPER, K. MEERKÖTTER, New Active Filter Synthesis Based on Scattering Parameters, IEEE Trans. Circuits and Systems, vol. CAS-22, pp. 594-602, July 1975.

[51] A. G. CONSTANTINIDES, H. G. DIMOPOULOS, Active RC Filters Derivable from LC Ladder Filters via Linear Transformations, IEE Jour. Electronic Circuits and Systems, vol. 1, no. 1, Sep. 1976.

[52] W. H. HOLMES, On Inverters and Converters, IEEE Trans. Circuit Theory, vol. CT-18, pp. 723-726, Nov. 1971.

[53] A. C. DAVIES, The Gyrator as an Impedance-Transforming Two-Port, IEE Colloquium Digest no.1968/12, Apr. 1968.

[54] P. S. ALEXANDROFF, An Introduction to the Theory of Groups, Blackie & Son, 1959.

[55] R. W. DANIELS, Gyrators, Negative Impedance Converters, and Related Circuits, IEEE Trans. Circuit Theory, vol. CT-16, pp.261-262, May 1969.

[56] R. W. DANIELS, The Synthesis of Fundamental Gyrators, IEEE Trans. Circuit Theory, vol. CT-16, pp. 543-544, Nov. 1969.

[57] R. W. DANIELS, A Method for Generating Some Active Circuits, IEEE Trans. Circuit Theory, vol. CT-18, pp. 397-399, May 1971.

[58] V. M. PAUKER, Equivalent Networks with Nullors for Positive Immittance Inverters, IEEE Trans. Circuit Theory, vol. CT-17, pp.642-644, Nov. 1970.

[59] L. T. BRUTON, Nonideal Performance of Two-Amplifier Positive Impedance Converters, IEEE Trans. Circuit Theory, vol. CT-17, pp. 541-549, Nov. 1970.

[60] L.T. BRUTON, J. T. LIM, High- Frequency Comparison of GIC-Simulated Inductance Circuits, Int. Jour. Circ. Theory and Appl., vol.2, pp. 401-404, Apr. 1974.

[61] A. ANTONIOU, K. S. NAIDU, Modeling of a Gyrator Circuit, IEEE Trans. Circuit Theory, vol. CT-20, pp. 533-540, Sep. 1973.

[62] A. ANTONIOU, K. S. NAIDU, A Compensation Technique for a Gyrator and its Use in the Design of a Channel-Bank Filter, IEEE Trans. Circuits and Systems, vol. CAS-22, pp. 316-323, Apr. 1975.

[63] D. G. HAIGH, On the Simulation of LC Filters by Active RC Networks, Ph. D. Thesis, University of London, 1976.

[64] S. K. MITRA, A Unique Synthesis Method of Transformerless Active RC Networks, J. Franklin Inst., vol. 274, pp. 115-129, Aug. 1962.

[65] A. W. KEEN, J. L. PETERS, Inductance Simulation with a Single Differential-Input Operational Amplifier, Electron. Letters, vol. 3, pp. 136-137, Apr. 1967.

[66] A. J. PRESCOTT, Loss-Compensated Active Gyrator Using Differential-input Operational Amplifiers, Electron. Letters, vol. 2, pp. 283-284, July 1966.

[67] A. G. HOLT, J. TAYLOR, Method of Replacing Ungrounded Inductors by Grounded Gyrators, Electron. Letters, vol. 1, p. 105, June 1965.

[68] R. H. S. RIORDAN, Simulated Inductors Using Differential Amplifiers, Electron. Letters, vol. 3, pp. 50-51, Feb. 1967.

[69] M. KAWAKAMI, Some Fundamental Considerations on Active Four-Terminal Linear Networks, IRE Trans. Circuit Theory, vol. CT-5, pp. 115-121, June 1958.

[70] A. W. KEEN, Active and Nonreciprocal Networks, in Network and Switching Theory (ed. G. Biorci), Academic Press, 1968.

[71] J. GLOVER, Basic T Matrix Patterns for 2-port Linear Transformation Networks in the Real Domain, Electron. Letters, vol. 10, pp. 495-497, Nov. 1974.

[72] B. D. H. TELLEGEN, The Gyrator, a New Electric Network Element, Philips Research Report, vol. 3, pp. 81-101, Apr. 1948.

[73] A. ANTONIOU, Floating Negative-Impedance Converters, IEEE Trans. Circuit Theory, vol. CT-19, pp. 209-212, Mar. 1972.

[74] D. C. KARNOPP, R. ROSENBERG, System Dynamics: A Unified Approach, Wiley, 1975.

[75] D. R. WISE, Active Simulation of Floating Lossy Inductances, Proc. IEE, vol. 121, pp. 85-87, Feb. 1974.

[76] S. C. DUTTA-ROY, V. NAGARAJAN, Active RC Synthesis of a Floating Immitance Using Operational Amplifiers, proc. IEEE Int. Symp. Circuit Theory, pp. 304-307, Toronto, Apr. 1973.

[77] T. YANAGISAWA, I. KANEMITU, Y. SHYOJI, Constant Resistance Network Using a 3-Port Gyrator, Proc. IEEE, vol. 58, pp. 836-837, May 1970.

[78] G. J. DEBOO, Application of a Gyrator-Type Circuit to Realize Ungrounded Inductors, IEEE Trans. Circuit Theory, vol. CT-14, pp. 101-102, Mar. 1967.

[79] W. H. HOLMES, An Improved Version of a Floating Gyrator, IEEE Jour. Solid state Circuits, vol. SC-4, pp. 162-163, June 1969.

[80] T. YANAGISAWA, I. KANEMITU, Y. SHYOJI, Three-Port Gyrators, Electron. and Commun. in Japan, vol. 54-A, pp. 1-8,1971.

[81] J. H. W. MÜLLER, Hybrid Integrated Gyrator in Dual-in-Line Package for Universal Application, IEEE Trans. Circuit Theory, vol. CT-18, pp. 726-728, Nov. 1971.

[82] H. O. VOORMAN, A. BIESHEUVEL, An Electronic Gyrator, IEEE Jour.Solid State Circuits, vol. SC-7, pp. 469-474, Dec. 1972.

[83] D. E. SHEAHAN, Gyrator Floatation Circuit, Electron. Letters, vol.3, pp. 39-40, Jan. 1967.

[84] H.R. TRIMMEL, W. E. HEINLEIN, Fully Floating Chain-Type Gyrator Circuit Using Operational Transconductance Amplifiers, IEEE Trans. Circuit Thery, vol. CT-18, pp. 719-721, Nov. 1971.

[85] J. M. ROLLETT, Circulator-Capacitor Networks, Electron. Letters, vol. 4, pp. 599-601, Dec. 1968.

[86] J. M. ROLLETT, P. E. GREENAWAY, Directly Coupled Active Circulators, Electron. Letters, vol. 4, pp. 579-580, Dec. 1968.

[87] A. W. KEEN, J. L. GLOVER, R. J. HARRIS, Realization of the Circulator Concept Using Differential-Input Operational Amplifiers, Electron. Letters, vol. 4, pp. 389-391, Sep. 1968.

[88] M. A.REDDY, Some New Operational Amplifier Circuits for the Realization of the Lossless Floating Inductance, IEEE Trans. Circuits and Systems, vol. CAS-23, pp. 171-173, Mar. 1976.

[89] W. SARAGA, A Contribution to the Design of Low Sensitivity Active RC Networks, Proc. IEEE Int. Symp. on Circuits and Systems, pp. 191-195, San Francisco, Apr. 1974.

[90] T. YANAGISAWA, Y. KAWASHIMA, Active Gyrator, Electron. Letters, vol. 3, pp. 105-107, Mar. 1967.

[91] W. JOST, Die Realisierung des Idealen Gyrators mit zwei Operationsverstaerkern, Arch. Elekt. Übertragung, vol. 21, pp. 152-157,1967.

[92] G. MARTINELLI, P. G. DI PORTO, Minimal Number of Nullors for Realizing Active Gyrators, Electron. Letters, vol. 4, pp. 273-274, June 1968.

[93] K. M. ADAMS, E. DEPRETTERE, On the Realization of Gyrators by Nullors and Resistors, Int. Jour. Circ. Theory and Appl. , vol. 2, pp. 287-290, Sep. 1974.

[94] E. DEPRETTERE, On the Minimal Realization of the Gyrator by means of Nullors and Resistors - I, Int. Jour. Circ. Theory and Appl., vol. 3, pp. 383-390, Dec. 1975.

[95] E. DEPRETTERE, On the Minimal Realization of the Gyrator by means of Nullors and Resistors -II, Int. Jour. Circ. Theory and Appl., vol. 4, pp. 285-297, July 1976.

[96] A. N. WILLSON, H. J. ORCHARD, Realization of Ideal Gyrators, IEEE Trans. Circuits and Systems, vol. CAS-21, pp. 729-732, Nov. 1974.

[97] H. J. ORCHARD, A. N. WILLSON, New Active-Gyrator Circuit, Electron. Letters, vol. 10, pp. 261-262, June 1974.

[98] C. E. SCHMIDT, M. S. LEE, Multipurpose Simulation Network with a Single Amplifier, Electron. Letters, vol. 11, pp. 9-10, Jan. 1975.

[99] E. A. GUILLEMIN, Introductory Circuit Theory, Wiley, 1953.

[100] J. SHEKEL, Matrix Analysis of Multiterminal Transducers, Proc. IRE, vol. 42, pp. 840-847, May 1954.

[101] H. EDELMANN, Zur Kettendeterminante Portzahlsymmetrischer Netze Mehrerer Klemmenpaare, Arch. Elekt. Übertragung, vol. 16, pp. 419-421, 1962.

[102] G. C. AUREL , Some Tools for the Analysis and Representation of Linear Two-Port Networks, IEEE Trans. Circuit Theory, vol. CT-12, pp. 18-21, Jan. 1965.

[103] M. M. SILVA, On the Realization of One-Nullor Gyrators, Proc. IEEE Int. Symp. Circuits and Systems, pp. 273-276, Boston, Apr. 1975.

[104] M. M. SILVA, W. SARAGA, On the Classification of Active RC Circuits Simulating Floating Inductors, Proc. 3rd. Int. Symp. on Network Theory, pp. 489-496, Split, Yugoslavia, Sep. 1975.

[105] W. SARAGA, M. M. SILVA,Three Different Types of Antireciprocity, Proc. Europ. Conf. Circuit Theory and Design, Genoa, Sep. 1976.