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DC/DC CONVERTERS FOR HIGH VOLTAGE DIRECT CURRENT TRANSMISSION

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The work presented in this thesis has been conducted by the author. All other work has been referenced and acknowledged where appropriate.

Abstract

High Voltage Direct Current (HVDC) transmission has to date mostly been used for point-to-point projects, with only a few select projects being designed from the outset to incorporate multiple terminals. Any future HVDC network is therefore likely to evolve out of this pool of HVDC connections. As technology improves, the voltage rating, at the point of commission, of the these connections increases. Interconnection therefore requires the DC equivalent of the transformer, to bridge the voltage levels and create a multi-terminal network.

This thesis investigates new potential DC/DC converter topologies, which may be used for a range of HVDC applications. Simple interconnections of new and legacy HVDC links is unlikely to require a large voltage-step, but will be required to transfer a large amount of power. As the HVDC network develops it may become feasible for wind-farms and load-centres to directly connect to the DC network, rather than requiring new and dedicated links. Such a connection is called an HVDC tap and is typically rated at only a small fraction of the link's peak capacity (around 10%). Such taps would connect a distribution voltage level to the HVDC network. DC/DC converters suitable for large-step ratios (>5:1) may find their application here.

In this work DC/DC converters for both small and large step-ratios are investigated. Two approaches are taken to design such converters: first, an approach utilising existing converter topologies is investigated. As each project comes with a huge price-tag, their reliability is paramount. Naturally, technology that has already proven itself in the field can be modified more readily and quickly for deployment. Using two modular multilevel converters in a front-to-front arrangement has been found to work efficiently for large power transfers and low step-ratios. Such a system can be operated at higher than 50 Hz frequencies to reduce the volume of a number of passive components, making the set-up suitable for compact off-shore applications. This does however incur a significant penalty in losses reducing the overall converter efficiency.

In the second approach DC/DC converter designs are presented, that are more exper-

imental and would require significantly more development work before deployment. Such designs do not look to adapt existing converter topologies but rather are designed from scratch, purely for DC/DC applications. An evolution of the front-to-front arrangement is investigated in further detail. This circuit utilises medium frequency (>50 Hz) square current and voltage waveforms. The DC/DC step-ratio is achieved through a combination of the stacks of cells and a transformer. This split approach allows for high-step ratios to be achieved at similar system efficiencies as for the front-to-front arrangement. The topology has been found to be much more suitable for higher than 50 Hz operation from a losses perspective, allowing for a compact and efficient design.

Acknowledgements

In my time at Imperial College, so many people have guided and provided me with invaluable advice, that it would be impossible to list them all here. There are, however, some who deserve a special mention. First and foremost I must thank my supervisor Tim Green for his patience through my blunders and the trust that at least some of his advice would eventually stick. He has provided me with fantastic opportunities, for which I am grateful.

From amongst my friends and colleagues at Imperial, special thanks is deserved by Michael Merlin, for he has diligently and repeatedly made time to explain aspects of control and power converters to me. I am also grateful to Adria and Richard for insightful discussions about all things related to transformers.

I also wish to thank the people I met from Alstom Grid for numerous helpful discussions and providing me with an industrial point-of-view on the work.

Finally, a big thank you to my family: my mum and dad have been an immense support through out all my time at Imperial and it simply would not have been possible without them. Last, I want to thank my fiancé Yazhini, who has been a bottomless source of motivation and encouragement, particularly during my writing of this thesis. Without her, it may never have come to an end.

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Symbols

Converter quantities for Chapters 3 to 5

$V_{d1,d2}$	DC link voltages
V_{AC}	AC voltage
V_{ϕ}	Converter AC voltage
V_{st}, V_{sb}	Voltage across top (t) or bottom (b) stack of cells
V_{dt}, V_{db}	Voltage across top (t) or bottom (b) director-switch
V_c	Nominal Cell voltage
$\hat{V}_{xx}$	Voltage magnitude
$\Delta V_c^{+,-}$	Voltage deviation above (+) or below (-) nominal cell voltage
U_t, U_b	Terminal voltage of inductive network relative to ground
I_{ϕ}	Converter AC current
$I_{t,b}$	Top (t) or bottom (b) arm current
I_{d1}, I_{d2}	DC link current
I_v	Vertical energy balancing current
$I_{\Re}$	Real part of complex current I
$I_{\Im}$	Imaginary part of complex current I
E_{st}, E_{sb}	Energy drift of top (t) or bottom (b) stack over one cycle
E_{stx}	Energy drift in top stack due to current x over one cycle
E_{cell}	Energy stored in cell capacitor
E_{s0}	Nominal energy stored in stack of cells
$\Delta E_s^{+,-}$	Energy deviation in stack above (+) or below (-) E_{s0}

$\hat{E}_s$	Maximum stored energy in stack
$\check{E}_s$	Minimum stored energy in stack
C_c	Cell capacitance
$\hat{C}_c$	Minimum cell capacitance to ensure $gamma_c$ for $\hat{E}_s$
$\check{C}_c$	Minimum cell capacitance to ensure $gamma_c$ for $\check{E}_s$
$L_{t,b}$	Top (t) or bottom (b) arm inductance
$R_{t,b}$	Effective resistance of arm inductance
N_c	Number of cells
N_d	Number of director-switches
P_{AC}	Active AC power
Q_{AC}	Reactive AC power
S_ϕ	Apparent power rating on converter AC side
f_{AC}	AC frequency
α	Phase angle difference between I_ϕ and V_{AC}
δ	Phase angle difference between V_ϕ and V_{AC}
ω_0	Natural frequency
ϵ	overlap period
γ_c	Voltage deviation margin relative to nominal cell voltage

Converter quantities for Chapters 6 to 8

$V_{a,b}^{+,-}, V_{o,i}^{+,-}, V_{t,b}$	Top (+ or t) and bottom (- or b) stack voltages for different stacks
V_e	AC balancing voltage
$V_L^{+,-}$	Terminal voltages of inductive network
V_{tv}, V_{bv}	Stack voltage required to generate AC voltage
V_{tc}, V_{bc}	Stack voltage available to control current
$U^{+,-}$	Voltage between terminals of inductve network
$I_{a,b}^{+,-}, I_{o,i}^{+,-}, I_{t,b}$	Top (+ or t) and bottom (- or b) stack current for different stacks
$I^{+,-}$	Loop currents
I_e	Circulating Ac balancing current
$E_{a,b}^{+,-}, E_{o,i}^{+,-}, E_{t,b}$	Top (+ or t) and bottom (- or b) stack energy drifts for different stacks
E_Σ	Sum of absolute stack energy drifts
$E^{+,-}, E_{a,b}$	Energy drift due to loop currents
E_{01}	Energy drawn from HV1 link per cycle
E_{oi}^{+}, E_{oi}^{-}	Top (+) and bottom (-) stack energy mismatch
E_c	Nominal energy in DC link capacitor
E_{s0}	Nominal energy stored in stack
$\Delta E_{t,b}^{+,-}$	Minimum (-) and maximum (+) energy deviation away from E_{s0}
P_1	power from HV1 link
$S_{a,b}^{+,-}, S_{o,i}^{+,-}, S_{t,b}$	Apparent power rating of stack
S_Σ	Total apparent power rating of all stacks in converter
$L_{a,b}^{+,-}, L_{o,i}^{+,-}, L_{t,b}$	Arm inductance
R_f, L_f, C_1	Passive DC filter components
Q	Quality factor of filter
f_n	Corner frequency of filter
f_{AC}	AC frequency
α, β	Loop current scalars
ϵ	Energy balancing current scalar

λ	Duty cycle of V_e
κ	Converter step-ratio
κ_s	Transformation-ratio of stacks
κ_t	Step-ratio of transformer
ζ_{cm}	Voltage control margin
$\gamma_{1,2}$	Voltage rippled of DC side capacitors
γ_c	Voltage rippled of cell capacitors

Controller quantities

A, B, M_u, M_L	State-space matrices
A_d, B_d	Discretised state-space matrices
J	Cost function of LQR
Q, R	Cost matrices of LQR
Q_{50}, Q_0	Quality factors of second-order filters
T_s	Simulation time-step
f_{cs}	Controller sampling frequency
k_{50}, k_0	Gains for second-order filters

Transformer quantities

$V_{p,s}$	Primary or secondary voltage
V_m	Magnetising voltage
U_ℓ	Voltage across leakage inductance
$I_{p,s}$	Primary or secondary current
I_m	Magnetising current
I', V'	Referred current or voltage
L_m	Magnetising inductance
$L_{1-2,1-2}$	Mutual inductance terms
L_ℓ	Leakage inductance
Z	Complex impedance
B	Flux density
Φ	Flux
A_c	Cross-sectional area of core
P_t	Active power rating of transformer
$P_{core,windings}$	Losses in core or windings
$n_{1,2}, n_{p,s}$	Number of turns in (primary or secondary) windings
n_e	Ratio of winding turns
k_t	Coupling factor
w_h	Winding height
ℓ_m	Mean magnetic path length
μ	Permeability
η_t	transformer efficiency
v_t	Transformer volume
$\tilde{v}_t$	Normalised transformer volume

Chapter 1

Introduction

Electricty is the most refined and valuable form of energy in today's world. To allow widespread access to electricity, a transmission network on an awesome scale has been built over the last century. At the beginning this network was fed by a fleet of mainly coal, later also oil and gas fired generators (referred to as conventional generation). These forms of electricity generation dominate the mix to this day.

In a move to wean ourselves off the raw materials that feed this conventional generation and reduce our carbon dioxide emissions, nuclear and renewable energy sources (RES) have been developed. The potential of some RES has been exploited for a long time, as is the case, for example, with hydro power. Large dam projects, such as the Three Gorges Dam, with a combined generating capacity of 22.4 GW [2], can take phenomenal scales. Some countries, like Norway and Brazil, generate most of their electricity demand using hydro power alone.

This option is, however, not feasible for the majority of countries. Thus alternative RES have been developed, particularly solar and wind. The scale of wind farms in the North Sea has been steadily rising over the last few years, as larger and more numerous turbines are erected further off-shore. The development of off-shore wind generation in the North Sea is estimated to reach 40 GW by 2020 and 150 GW by 2030 [3]. As more wind-farms are commissioned, they move ever further away from the shore. Today, projects like BorWin1, are a distance of 125 km away from the shore line [4].

This illustrates the big difference between conventional generation and RES: conventional generators could be placed near the load centres and the fuel be brought to them. This is not the case with RES. They are inherently inflexible and not only require to be built where the resources are, but can also be intermittent in generating.

As the RES content of the European, and indeed world-wide, electricity mix increases,

the transmission system will have to be upgraded as well. Today the network is designed to efficiently transport electricity from the power plants to the load centres. As this has mainly been conventional generation, this tended to be a uni-directional, or trickle-down, system. A more interconnected system, capable of connecting distant RES and allowing more flexible power flows has to be build to accommodate the the new form of generation and ensure supply security.

Regional powers have recognised this and have promoted plans such as the European supergrid [5]. Transmission technology called High Voltage Direct Current (HVDC) transmission, is being advocated to reinforce the existing AC interconnected grid, as well as create new long distance interconnections, such as NorNed, the Norway - Netherlands interconnector [6].

HVDC technology has been around for over 50 years, but its development has recently experienced a surge. New HVDC technologies allow the construction and operation of large multi-terminal DC networks [7]. This does not however mean that all components of a potential future DC network are presently commercially available or even fully developed. One crucial component which, if the the development of AC networks is anything to go by, will play an important role, is the DC/DC converter - or the DC equivalent of the transformer.

1.1 Problem Statement and Thesis Outline

This thesis investigates potential DC/DC converters, using the latest HVDC technology, suitable for a range of applications. In particular two approaches to the design of a DC/DC converter are taken: first, an approach which utilises existing and reliable technologies to achieve the required goal. This may be advantageous if a DC/DC converter is to be commissioned in the next ten years, as research and development times have in the past run into several years for similar HVDC DC/AC converters. The second approach takes a longer view: it investigates purpose designed DC/DC circuits, which will take longer to gain viability and commercial acceptance.

The work focuses on better understanding the design parameters of a number of different DC/DC converters. The losses and the converter volume tend to be the most important features of a converter, as they affect the lifetime and initial capital costs. Typically, when designing a converter, internal parameters can be varied to achieve trade-offs to affect the losses or volume.

In particular the chapters of this work cover the following work:

Chapter 2

This chapter introduces the basics of HVDC technology. It also provides a review of the existing literature on DC/DC converters and their suitability for HVDC applications.

Chapter 3

A front-to-front (F2F) arrangement of two DC/AC converters, connected through a common AC voltage, is presented. Important background information to the method of operation of the two Voltage Source Converters (VSCs) considered for such a circuit topology is provided. A circuit description of, as well as control mechanism for the direct-coupled F2F topology is presented. As both converters share a common AC voltage, but connect to different DC potentials, the choice of AC voltage magnitude has a big impact on the performance of each converter. The effects of this on the overall system efficiency and volume are explored in detail.

Chapter 4

The F2F arrangement can be supplemented with galvanic isolation on the internal AC connection. This allows each converter to operate with a different AC voltage, which can potentially improve the system performance. This chapter presents the modified circuit and the relevant changes to the controller of the direct-coupled system. It also investigates how the system performance is affected by the transformer.

Chapter 5

Both F2F topologies presented can utilise higher than 50 Hz frequencies in their AC link. The operation and effect on the direct-, as well as the transformer-coupled systems, are investigated at 500 Hz operation.

Chapter 6

Two fundamental operating methods for purpose designed cell based DC/DC converters are presented. Two circuits for each method have also been explored in some detail. The power capacity ratio has been used to compare all four converters with each other. This measure indicates the ratio of the installed power rating of the power electronics relative to the transferred power.

Chapter 7

One of the four converters presented in chapter six, the shunt connected primary

converter, is analysed in more detail and control mechanisms are presented. Crucial operational design parameters are investigated, such as the number of cells required.

Chapter 8

The design trade-offs of the individual components of the shunt connected primary converter are investigated. The focus in this chapter is on the means to optimise the converter for either losses or volume.

1.2 Author's Publications based on this Work

Based on Chapter 3

T. Lüth, M. M. C. Merlin, T. C. Green, C. D. Barker, F. Hassan, R. W. Critchley, R. W. Crookes, K. Dyke, *"Performance of a DC/AC/DC VSC System to Interconnect HVDC Systems"*, 10th IET International Conference on AC and DC Power Transmission, pp.1-6, 2012.

Based on Chapter 3

T. Lüth, M. M. C. Merlin, T. C. Green, C. D. Barker, F. Hassan, R. W. Critchley, R. W. Crookes, D. Trainer, K. Dyke, *"Choice of AC Operating Voltage in HV DC/AC/DC System"*, IEEE Power and Energy Society General Meeting (PES), pp.1-5, 2013.

Based on Chapters 3 to 5

T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, C. D. Barker, *"High-Frequency Operation of a DC/AC/DC System for HVDC Applications"*, IEEE Transactions on Power Electronics, Volume:29, Issue: 8, pp.4107-4115, 2014.

Based on Chapter 6

T. Lüth, M. M. C. Merlin, T. C. Green, *"Modular Multilevel DC/DC Converter Architectures for HVDC Taps"*, 6th Conference on Power Electronics and Applications, EPE'14-ECCE Europe, pp.1-10, 2014.

Based on Chapter 7

T. Lüth, M. M. C. Merlin, T. C. Green, *"A DC/DC Converter Suitable for HVDC Applications with Large Step-ratios"*, IEEE Energy Conversion Congress and Exposition (ECCE), pp.1-8, 2014.

Chapter 2

Background to HVDC transmission and the role of DC/DC converters within it

In this chapter the basic technologies relevant to this thesis are introduced. This is done with the intention of enabling the work presented in the following chapters, to be understood and compared to other work within the field. Whilst the background information provided aims for enough breadth to be comprehensive in nature, it does not provide thoroughly detailed information. These can be found in the reference texts cited. A basic understanding of electricity is assumed.

2.1 High Voltage Direct Current Transmission Technology

The first ever cable laid to transmit power and supply the customers of Pearl Street, New York, in 1882 used direct current (DC) [8]. It was the fruit of the labour of Thomas Edison and in today's terms was more of a distribution, rather than a transmission line: it operated at 110 V and was supplied by a single 100 kW generator [9], supplying electricity to within a few blocks of the generator. Paltry as it may seem today, it was revolutionary at the time.

The system however suffered from a major drawback: Edison was not able to utilise a higher voltage, thereby limiting the transmission distance to a few hundred meters, due to the resistive losses in the cables. This meant that only a larger number of small scale generators would allow a large portion of New York to be supplied with electricity, severely limiting the profitability of the undertaking.

Alternating current had been envisaged for use in supplying electricity to homes and factories by the likes of Sebastian Ziani de Ferranti, Nikola Tesla and George Westinghouse [10, 11, 12, 13, 14]. The demonstration of the closed iron-core transformer by Déri, Bláthy and Zipernowsky in 1884 [15] gave the championed AC distribution and transmission systems the edge over the DC ones: it allowed the voltages and currents to be stepped up and down as required, allowing large central power stations to supply the systems. Stations like the Deptford central electric light station were built able to generate 1000 kW at 10 000 V [10]. The lack of efficient means to step voltages in DC, eventually meant that AC became the prevalent method of transmission and distribution, leading to the vast three-phase AC power systems spanning entire nations and connecting continents we know today.

However, by 1954 DC had made a comeback in the form of the Gotland 1 transmission corridor [16]. The prohibitive transmission losses Edison had to battle with were overcome in this project by raising its transmission voltage to 110 000 V at 200 A [17]. It was the first High Voltage Direct Current (HVDC) transmission line in commercial operation.

2.1.1 Reasons for Using HVDC

AC transmission is by far the most widely used transmission technology on the planet. However an increasing number of new transmission projects utilise HVDC, not AC. The most common reason for this is the length of the transmission line.

Renewable generation is often not found near load centres, but rather in remote regions, such as the hydro-plants in Brazil, China, India or Norway [18]. For the Belo Monte project in Brazil for example, a 3000 MW bipole arrangement at $\pm$800 kV has been proposed covering a distance of 2300 km. Utilising AC transmission technology for such distances and power ratings would be extremely costly as the AC line has to be supplied with reactive current to energise it every half-cycle; a DC system does not require to be re-energised as its voltage remains fixed.

As a line is only rated for a certain current magnitude, the higher the reactive power demand, the lower the current "head-room" for the active power. The reactive power demand of the line also increases with distance and voltage rating. To counteract these effects shunt or series compensation can be installed along the transmission line, which is however very costly and requires bulky passive components or converter stations.

For these reasons, at a certain distance HVDC transmission becomes more economical, as it does not require reactive compensation or energising currents. Compared to AC, it does however come with a higher initial cost, as specially build DC/AC converter stations

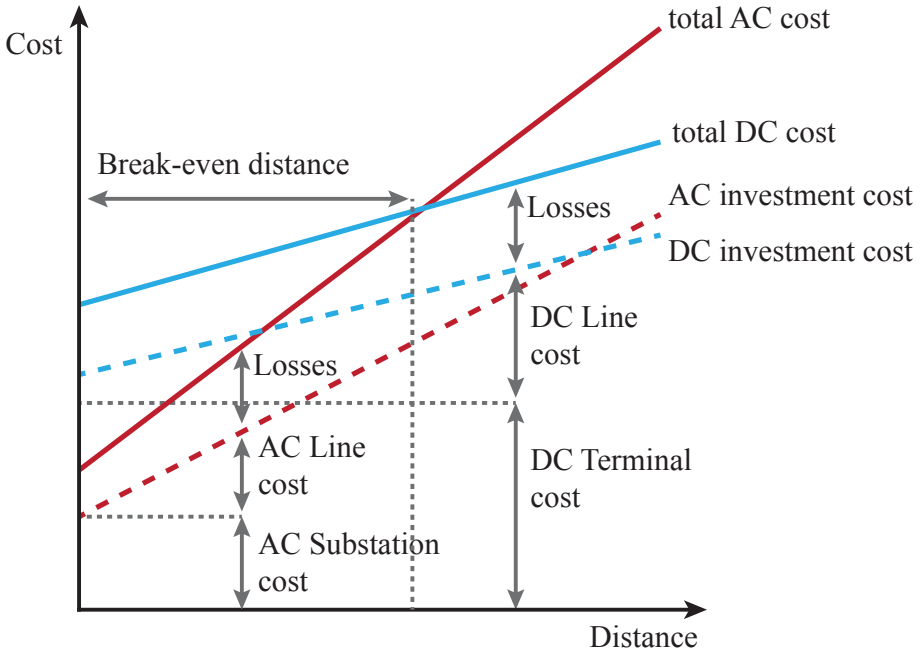

Figure 2.1: Relative cost of AC vs. DC transmission against distance.

are required to interface the existing AC grid with the DC transmission line. Figure 2.1 illustrates the relative costs of DC and AC transmission against the transmission distance [16, 7, 19].

The break-even distance is the point at which HVDC transmission becomes cheaper than the AC alternatives. This distance depends on a number of factors such as the technologies considered and whether the line utilises overhead (OH) lines or cables. As cables contain a grounded sheath close to the cable, their capacitance per unit length tends to be significantly higher than that of OH lines. Consequently the break-even distance of cable projects is significantly shorter at between 40 and 80 km [7, 19] compared to between 500 to 800 km for OH lines [16, 20]. The use of cables is set to become more prevalent in new transmission projects due to a number of off-shore wind projects in the North Sea and on the US coast which are being developed, for which HVDC connections are used due to their distance from shore [21, 22].

HVDC has further application areas: because its RMS currents tend to be higher than those of AC for the same conductor cross-sectional area, the power density of HVDC transmission is higher. In [23] an 800 kV HVDC transmission corridor carrying 18 GW has been estimated to require only a third of the footprint of a 800 kV AC transmission corridor. As the foot-print for transmission corridors has been constrained in Europe for

many years, this allows a capacity upgrade without the need for additional space.

For this reason, HVDC projects have been commissioned and planned to be embedded within a larger AC grid and ease the congestion on the existing transmission corridors. Prominent projects include the Eastern and Western interconnectors in the UK and new HVDC north-south transmission corridors in Germany [24]. Interconnections between countries and entire regions have also been commissioned and the prospect of a grid to facilitate a free energy market across Europe is envisaged to utilise HVDC [5, 7].

2.1.2 HVDC Technology

Although an HVDC system utilises a number of components the most important two are the cables and OH lines as well as the converter stations. The former will not be discussed here in any detail. Suffice it to say that OH lines can presently support higher voltages and currents than cables, although the latest cable technology, as published in [25], allows for ±525 kV operation at 2.6 GW. These power levels are getting close to the in-feed limitations in most countries which will limit the power rating of any one line.

As this thesis deals with DC/DC converters a brief overview of the DC/AC converter technologies relevant to HVDC applications is presented in the next sections.

Current Source Converter Technology

The older of the two, Current Source Converter (CSC) technology has been around since the 1950s but still has some advantages that make it a best seller with most HVDC companies today. It uses series connected thyristors, most commonly arranged in a six-pulse bridge, as shown in figure 2.2. The name derives from the six commutations per cycle that the converter goes through, which produces a characteristic 6^{th} harmonic ripple on the DC voltage. To improve the harmonic content of the DC side two six-pulse bridges can be operated in series with each other, which is referred to as a 12-pole arrangement and used in most modern HVDC CSCs [20]. The AC connections of the two converters require a 30° phase shift relative to each other, resulting in a complex transformer arrangement.

Because this topology uses thyristors, it is also referred to as a line commutated converter (LCC), as the thyristor cannot actively be switched off but has to wait for a zero-current crossing to do so. This makes the controller relatively simple, as only a short firing command has to be supplied to each device at the point of turn-on. It also however means that a CSC requires a strong AC grid to connect to, to ensure that the AC currents commutate at the required times. Due to the operating method the CSC always provides a lagging power factor, i.e. it always appears as a reactive load. A typical reactive power

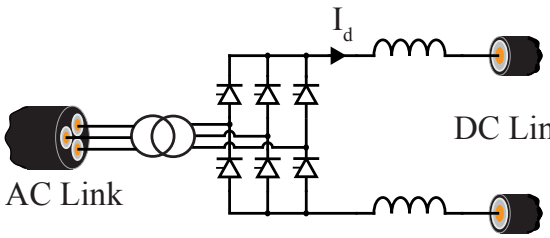

Figure 2.2: Six-pulse Current Source Converter.

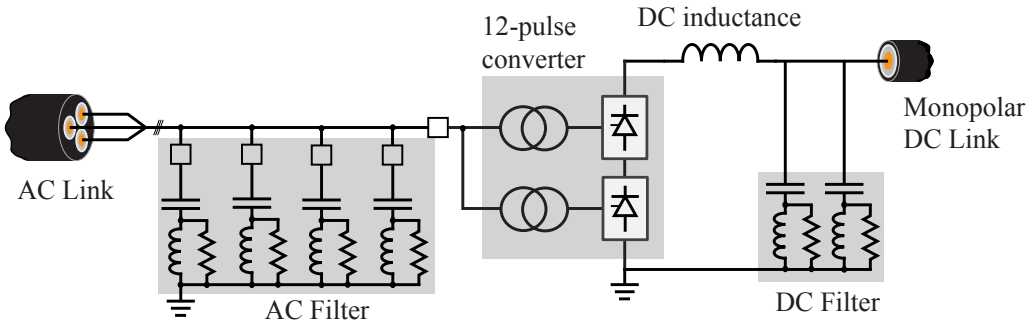

Figure 2.3: High level circuit diagram of Current Source Converter and required passive components [1].

demand for such a converter is around 55% of the power rating. Although over 60% of this is typically supplied by the AC side filters, this still leaves a significant reactive power demand to be supplied by the AC grid. More could be supplied by the filters, but in general this solution would b too costly as they require significant amount of space.

The general diagram of a CSC is shown in figure 2.3. It's operation assumes a fixed DC current, hence it requires a large DC side inductor (DC Smoothing inductors used in ±500 kV, 3000 MW Three Gorges transmission project are 290 mH each [18]). Even when operated in a 12-pulse arrangement, a CSC requires significant passive filter banks, as can be seen from the high level circuit diagram. These are costly, as they require a significant amount of space, which due to land-ownership rights can be difficult to acquire. The current direction is fixed in a CSC. So, to reverse the power-flow through a line the DC voltage polarity is reversed. For this reason CSC technology is less suitable for multi-terminal applications [7].

A big advantage of the CSC technology is its extremely high current and voltage ratings. It is relatively easy to connect individual thyristors in series and package them compactly, including their snubber circuitry, as shown in figure 2.4. Due to the high current ratings, thyristors can be supplied at, CSC schemes can operate at extremely

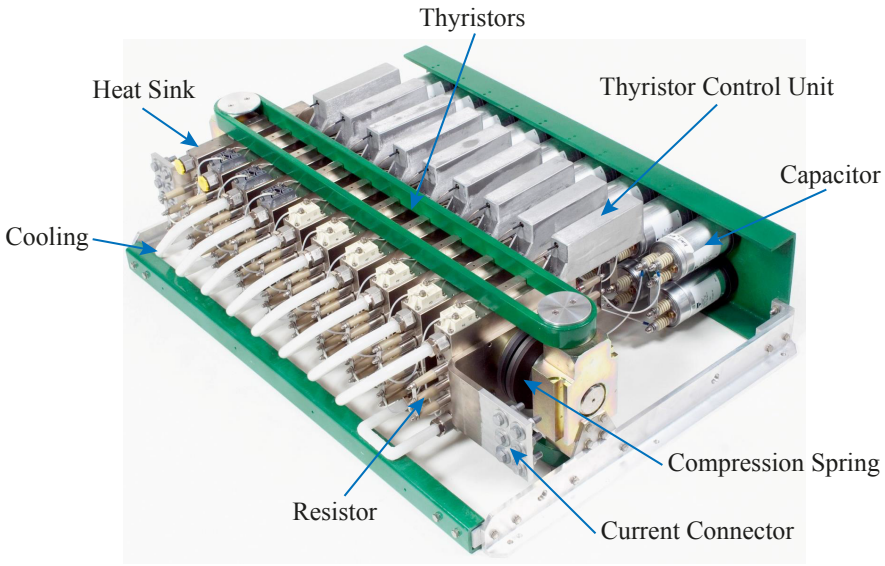

Figure 2.4: Thyristor module for HVDC applications built by ABB[1].

high power levels: the most powerful transmission line at the time was commissioned in 2013 in China, running from Jinping to Sunan, a distance of 2090 km and it has a rated capacity of 7200 MW at ±800 kV [26]. Finally due to the low switching losses involved in utilising thyristors CSCs can operate with high efficiencies. Typically the converter losses are stated as between 0.6 and 0.8% of rated power [1].

Voltage Source Converter Technology

Since the late 1990s an alternative HVDC technology, the Voltage Sourced Converter (VSC), has been commercially available [1]. The first generation of VSCs looked a lot like the CSC six-pulse bridge but utilising Insulated-Gate Bipolar Transistors (IGBTs) or Gate Turn-Off thyristors (GTOs), as shown in figure 2.5, which can be actively switched off, interrupting the current path in the arms. The name of these converters stems from their operating methodology: a VSC assumes a fixed DC voltage and controls the current to vary and reverse the power flow. This makes them inherently suitable for multi-terminal applications [7].

In the three-phase bridge VSC, commonly referred to as a three-level converter, the AC side waveforms are created using PWM switching, as illustrated in figure 2.5. This implies that the arm devices are hard-switched, typically at a frequency significantly higher than

[1]image courtesy: [27]

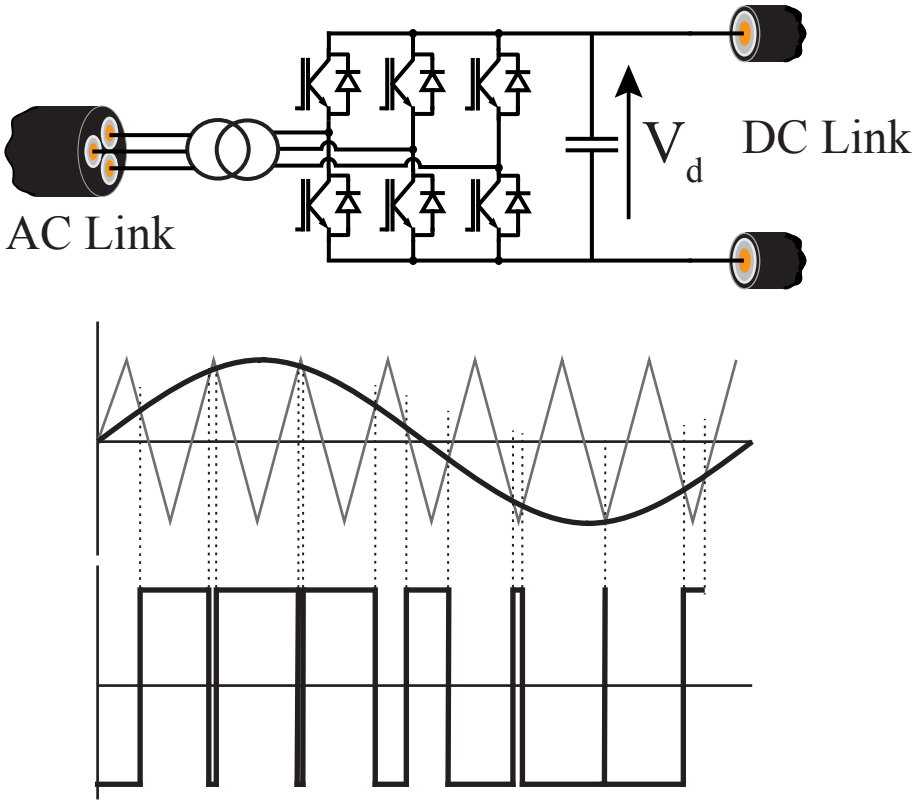

Figure 2.5: Two level voltage source converter.

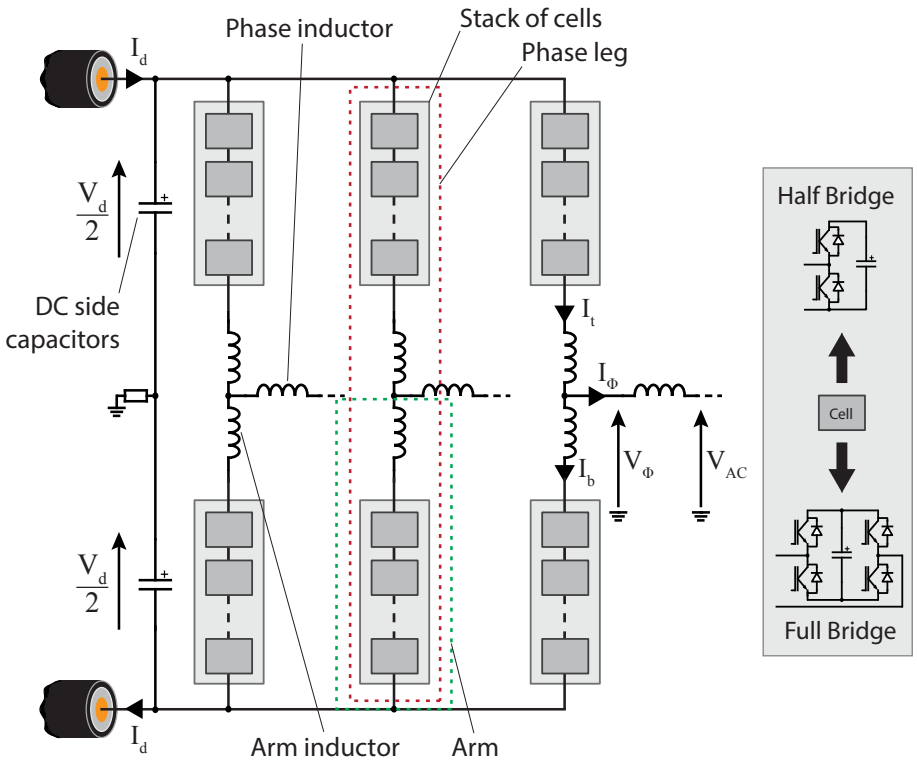

Figure 2.6: Three phase VSC modular cell based VSC.

50 Hz. Consequently the losses of a three-level type VSC are considerably higher than those of a CSC at about 1.7% [28].

To reduce the harmonic content and lower the switching frequency of individual devices, more levels were introduced, spawning a family of voltage-source multi-level converters [29]. The problem with most of the proposed designs is an exponentially increasing device count as the number of levels is increased which leads to significantly higher circuit complexities. This problem was ultimately overcome by a modular multi-level design, often referred to as the MMC [30, 31], as shown in figure 2.6. A number of other modular multi-level converter topologies have been proposed since [32, 33, 34].

The modular design has allowed the component count to be linear with the number of levels and simplified the voltage grading of the IGBTs, which can be problematic [35, 36]. Thus a HVDC MMC will today provide in excess of 200 levels, resulting in a virtually harmonic free AC voltage and current waveform. Consequently the filter requirements have been drastically reduced, particularly compared with CSCs, as illustrated in figure 2.7, showing a high-level circuit diagram of a VSC and the required passive components.

Furthermore the losses have been significantly reduced with the latest generation of

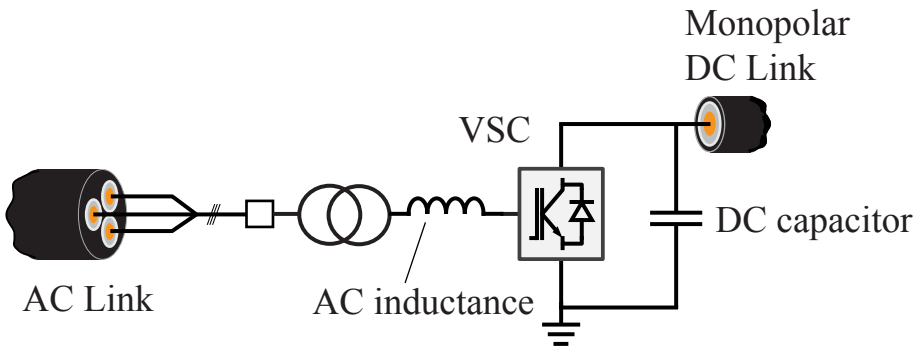

Figure 2.7: High level circuit diagram of Voltage Source Converter and required passive components [1].

modular VSCs: losses of only 1% of the rated power have been reported [28, 1]. Industry insiders expect this figure to be decreased further still with the development of new modular topologies over the next few years, bringing it in line with CSC efficiency ratings.

The VSC technology furthermore allows for a so called black-start, which implies that it can connect to weak grids such as wind-farms. Its low filter requirements allow for a compact station design of as little as 58% relative to a CSC station (which includes the filters) with similar voltage level and power rating [37]. These aspects make VSC technology particularly appealing as an off-shore alternative, where platform space comes at a premium.

Other advantages of VSCs include a much shorter response time than CSCs where the line-commutation imposes a limit on the minimum response time. Furthermore a VSC does not inherently require reactive power and can operate in current leading as well as lagging mode, making it possible to offer ancillary services to the AC grid in the form of voltage support.

2.2 DC/DC Converters for HVDC Networks

The early DC network, built by Edison, in part failed because at the time a crucial component was missing: the DC counterpart to the transformer, the DC/DC converter. As HVDC is being used more widely and with the recent innovations in VSC technology, a HVDC grid has once again become a plausible next step [29, 38, 39, 40, 41]. Such an interconnected grid is expected to span entire countries and in particular in Europe, is expected to facilitate a free energy market [42, 43, 5].

To enable such a grid being constructed, DC/DC converters are expected to have their

role to play. A number of possible application areas have been envisaged, as illustrated in figure 2.8. A DC grid is not expected to be commissioned in one project; rather it is expected to grow out of interconnections of existing point-to-point transmission corridors. As such links may have been built utilising different cable technologies, their DC voltage may be slightly different. To interconnect such lines DC/DC converters with a low step-ratio (less than 5:1) would be required.

It is also conceivable that an existing CSC link is to be integrated into a VSC dominated grid. A specialised DC/DC converter might thus not necessarily provide a step-ratio but rather the interface between two differing technologies, to allow an unimpeded bi-directional power flow. This can be problematic due to the different mechanisms by which CSC and VSC lines achieve a power flow reversal.

Furthermore as DC grids develop and encompass larger areas, great care must be taken to ensure that DC faults do not cause the entire system to shut down. Whilst DC breakers [39] will almost certainly play their role, DC/DC converters can also provide DC fault propagation prevention measures. This can be done through galvanic isolation of the two interconnected DC links or by means of fault blocking circuit arrangements (such as used in a full-bridge MMC [44, 45, 46] or the AAC [34]).

Finally it may also be of interest to connect a remote load, such as a town or factory, or a generator, such as a wind-farm or solar plant, to a nearby HVDC transmission corridor. In such instances the power rating of the connection may only be a fraction of the total HVDC link capacity; in such cases we talk of a HVDC tap. Due to their lower power rating, such taps typically connect straight to low- or medium-voltage level feeders. This implies that they must also be able to cope with a large step-ratio between the HVDC link voltage, which will be in the hundreds of kV, and a distribution voltage of maybe tens of kV.

Following the resurgence of HVDC utilising the CSC technology, a number of publications discussed the possibility and technical considerations of tapping CSC HVDC lines [47, 48, 49]. Due to the prevalence of CSC links today, tapping them is still a much discussed topic, evidenced by [50, 51, 52, 53, 54].

Two different high level tap topologies have been discussed in the literature [47]: the parallel and series tap, as illustrated in figure 2.9. The series tap is directly integrated into the transmission line and must therefore be able to carry the entire link current but only needs to with-stand a fraction of the voltage. It needs to be noted, however, that a series tap has to be fully insulated to the line voltage, which will require a significant amount of insulation and space. Relative to ground a series tap will also require a large voltage insulation, typically across a transformer such as described in [53]. Furthermore,

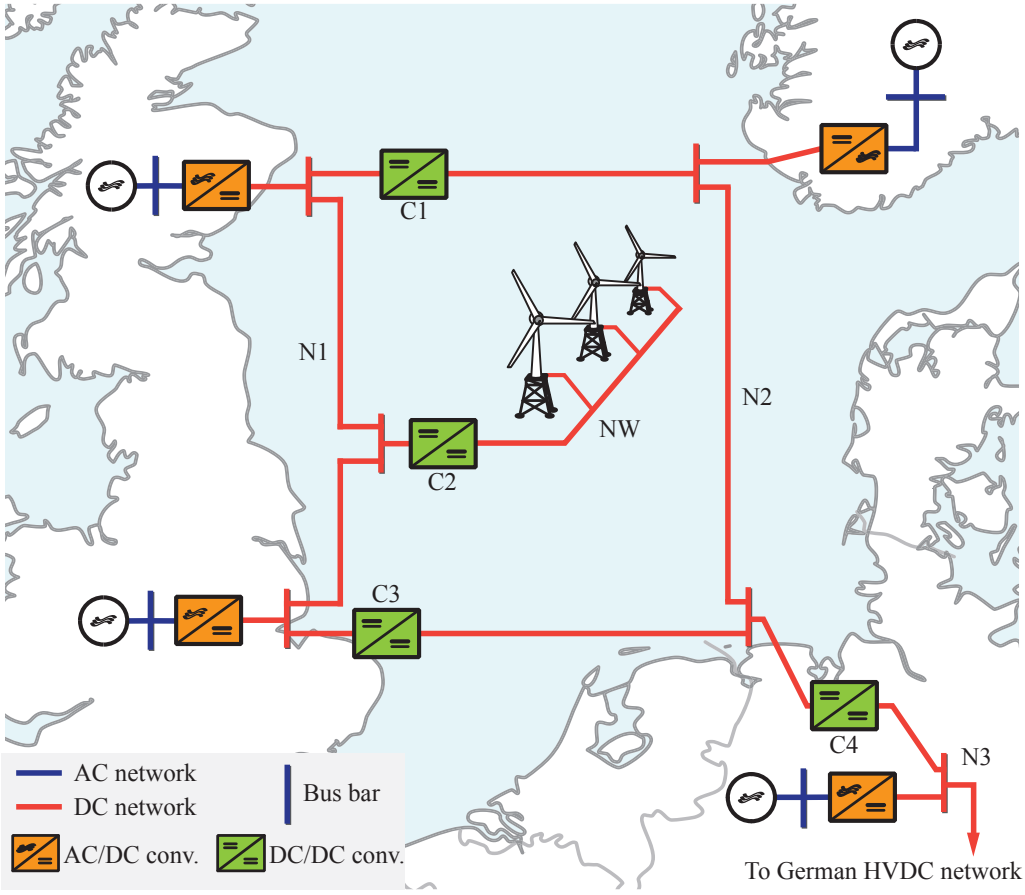

Figure 2.8: Possible application areas of DC/DC converters in HVDC network.

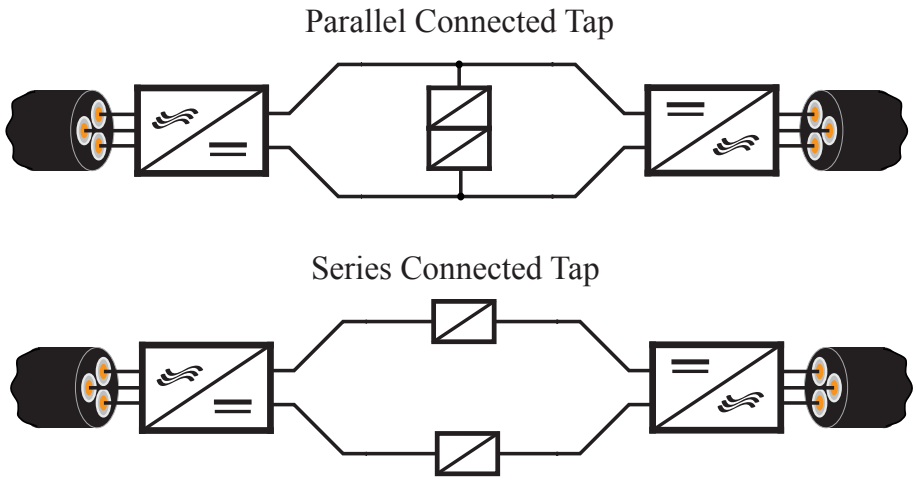

Figure 2.9: Series and parallel tap design in a HVDC network.

in order to maintain the availability of the rest of the line, in case of an open circuit fault in the tap converter, an additional bypass circuit has to be installed.

A parallel tap on the other hand has to be able to withstand the entire link voltage but only a fraction of the link's current magnitude [51, 50, 54, 55]. This reduces the additional insulation requirements. To prevent the converter from propagating a DC fault to the rest of the network, it would need to be designed to be able to support the link voltage during fault conditions or contain DC breakers which can disconnect the converter from the network. Parallel taps are inherently more suitable to VSC rather than CSC transmission links, as they are not suited for voltage polarity reversal and require additional connectors to rearrange their circuit [51].

A tap could consist of a conventional DC/AC converter followed by a transformer, as illustrated in figure 2.10. Such an arrangement may however not provide the best utilisation of the semiconductors and also contains a bulky 50 Hz transformer. An alternative tap layout is shown in figure 2.11 which uses a DC/DC converter to achieve the step-ratio. Furthermore DC collection grids have been proposed for off-shore wind farms [56, 57, 58, 59]. To connect such a medium voltage (MV) grid to the HVDC link, a DC/DC tap would be required.

2.2.1 Switched Mode Power Supplies

Switched Mode Power Supplies (SMPS) have been studied extensively and find numerous applications in the low power range (up to a few kilo watts) [60]. One of the most well known SMPS is the buck/boost converter, as shown in figure 2.12. It can be used to

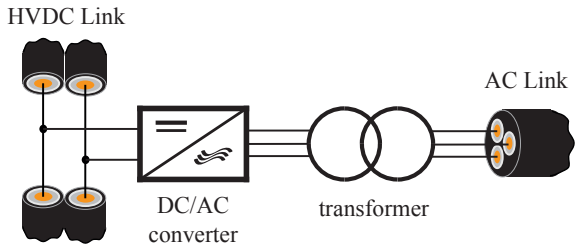

Figure 2.10: HVDC rap consisting of conventional DC/AC converter and transformer.

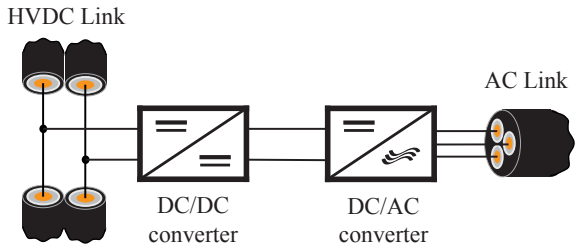

Figure 2.11: HVDC tap using a DC/DC and a low voltage DC/AC converter.

provide a voltage step between V_{d1} and V_{d2}. SMPS draw pulses of current from the V_{d1} connection, which can require significant filtering effort on the DC side, to ensure that the current ripple is kept within tolerable limits (typically 3%) [61].

Furthermore the semiconductors have to be able to withstand the difference in voltage between the two DC links, which significantly increases as the step-ratio increases. As the switch has to be able to hard-switch, an active device, like an IGBT, is required which implies that a number of such devices have to be connected in series to achieve the required blocking voltage. This can be problematic due to significant snubber and gate-driving requirements [35, 36].

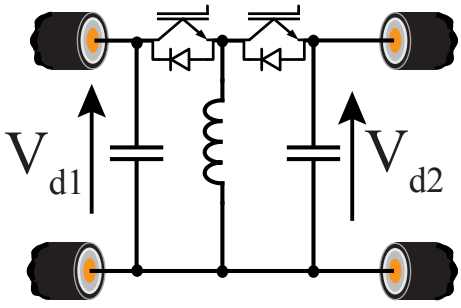

Figure 2.12: Buck-boost circuit.

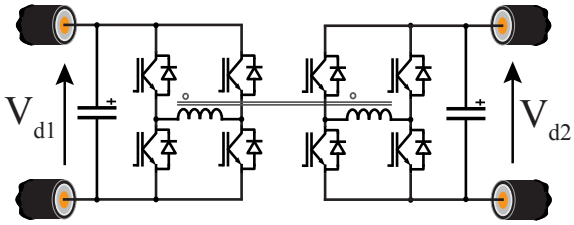

Figure 2.13: Circuit of a Dual Active Bridge (DAB) converter.

In HVDC applications the losses play an important role in the feasibility of any converter design, as the lifetime of such converters is expected to be at least 20 years. Therefore losses significantly contribute to the lifetime cost. To reduce the filter requirements of the SMPS, a higher switching frequency can be employed. This however significantly increase the switching losses incurred and thus its lifetime cost.

The step-ratio of conventional SMPS topologies is usually limited to about 1:4 [62] for practical reasons, although alternative designs have been proposed which utilise internally coupled inductances to achieve higher step-ratios [63, 64]. Although these circuits perform well at low power levels, they do not lend themselves very well for scaling up to HVDC voltage and power levels, due to a large component count and complex circuit arrangements.

A modular design utilising SMPS modules has been proposed in [65] to overcome some of these challenges. By series or parallel connection of SMPS modules, large step-ratios can be achieved. The presented circuit, however, operated with 5% of losses relative to its power rating, which is large enough to make the circuit unfeasible for HVDC applications.

2.2.2 Dual Active Bridge Type Converter

The concept of a DC/AC/DC conversion process is used in a large family of converters: the Dual Active Bridge (DAB) arrangements. The circuit, as illustrated in figure 2.13 and first published in [66, 67], utilises simple active H-bridges on each DC link, which are interfaced through a transformer. Each H-bridge acts as a two level converter generating square-waves across the windings of the transformer. The phase-shift of the AC waveforms relative to each other, is used to control the power flow through the converter, as described in [66]. The transformer provides the step-ratio as well as galvanic isolation between the DC connections.

When designed carefully, this circuit can be operated such that the devices in both bridges are zero voltage switched (ZVS), significantly reducing the switching losses [68, 69, 70]. This makes a high-frequency operation in excess of 10 kHz feasible, allowing for

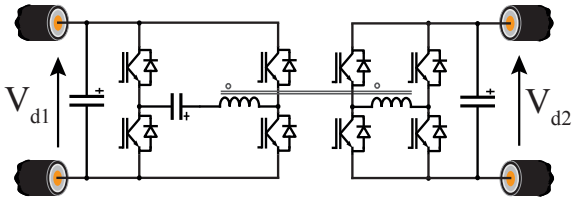

Figure 2.14: Circuit of a Series Resonant Converter.

a compact transformer design.

As the bridges require active switching devices, this topology can be highly effective for low to medium voltage applications, where the entire DC link voltage can be blocked by a single device. For HVDC, and other high voltage, applications a string of series connected IGBTs would be required which can be problematic due to the snubber requirements to ensure equal voltage balancing across the switches as well as synchronous switching of the devices within an arm [35, 36].

Resonant Converters

The Series Resonant Converter (SRC) shares a similar circuit layout to the DAB, as shown in figure 2.14. Variations of this circuit have been proposed and discussed in [71, 69, 72, 73, 74, 75]. Other resonant converters utilising a DAB like converter architecture have been proposed in [76, 62, 77, 78] The topology benefits from virtually no switching losses, due to the soft-switching of the transistors. As these topologies however also require a resonant tank and continue to operate at high switching frequencies in the tens of kHz, the resonant sink's passive components add significant conduction losses [79].

Apart from [76, 62], the SCR converters use IGBTs, which means that they are also susceptible to the problems associated with series connected IGBTs at high DC voltages. The topology discussed in [76, 62] however utilises thyristors instead, which have been used extensively in series connections in CSCs. As confirmed by an industrial source, the building of such thyristor valves requires less volume than one using IGBTs would and can be done with extremely high reliability. As discussed in [80, 81] this topology is very efficient at low step-ratios, with estimated losses of 1.5% at a step-ratio of 5:3 and a power rating of 300 MW. As the step-ratio is increased, an increase in the losses has been reported up to between 5% for a step-ratio of 20:1 [62] (at 80:4 kV and 5 MW) and as high as 21.8% for 60:1 [81] (at 5:300 kV and 5 MW).

The size of the passive components is a function of the AC frequency used in the resonant tank. Some topologies like [74, 69, 75, 77, 78] lend themselves to higher frequencies, as

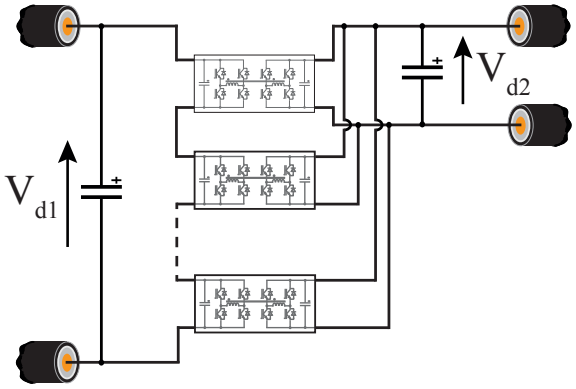

Figure 2.15: Illustration of a modular DAB converter.

they use active switches (such as IGBTs or MOSFETs). The resonant converter discussed in [62, 81] uses thyristors, which have a more limited turn-off time, thus limiting the AC frequency to about 1 kHz [76] and making for comparably larger passive components. The voltage stress across the capacitor in [76, 81] has to be considered also, as the peak capacitor voltage is equal to the lower plus higher DC link voltage. Considering the anecdotal problems of large high voltage DC link capacitors, told by industrial sources at Alstom, Siemens and ABB, this high voltage stress may be problematic for HVDC applications.

Modular DAB Type Converter

The problem of series connected IGBTs in HVDC DAB like converters can be overcome by using DAB modules as have been proposed in [82, 83, 79, 84]. In such topologies the higher voltage DC side sees a number of DAB modules connected in series. On the lower voltage DC side the same modules are connected in parallel to achieve a very high voltage step. This arrangement has been illustrated in figure 2.15.

Different DAB type modules, such as SRC or Dual Half Bridge (DHB) types, have been suggested. All of which operate with a mutually coupled inductance to implement part of the step-ratio. As the modules are however connected in series on one side and in parallel on the other, the transformers windings have to be rated to different DC voltages, depending on the position of the module within the circuit. This means that either all transformers have to be rated to the highest blocking voltage or require different designs. The former alternative implies unnecessary winding insulation, which causes extra losses in the insulation dielectric and larger transformers.

The latter alternative implies different leakage inductances for each transformer unless the winding arrangements are varied, which would make the transformer designs even

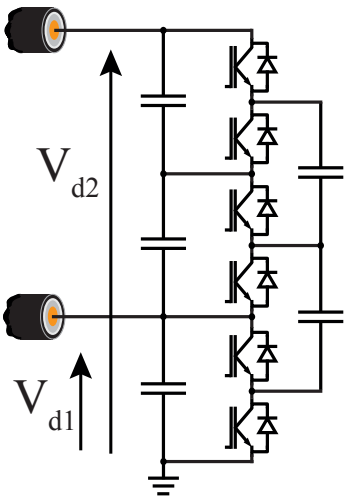

Figure 2.16: Circuit diagram of a switched capacitor converter.

more complex. Especially the SCR types modules require the leakage inductance for the resonant circuit. Varying leakage inductances therefore would imply that each module has to be especially tuned and sized for its position in the converter. Standard DAB modules also use the leakage inductance to control the power flow. This is done by adjusting the phase angle across it. In this case varying leakage inductances will require each cell to operate with a different range of phase angles, making the controller more complex.

In either case, although the converters are referred to as modular, each module will require to be different from the others in some aspect. It can be argued that this defeats the objective of a modular design, which is to simplify the manufacturing process and to ensure high reliability of individual components by manufacturing all of them to the same specifications.

2.2.3 Switched Capacitor Type Converter

The switched capacitor converter, also referred to as the flying capacitor converter or voltage multiplier, has been used to generate a DC voltage step in a number of proposed circuits: [85, 86, 87, 88]. The general principle is illustrated in figure 2.16 and is based on the principle of passing charge from one capacitor to the next.

Since the switches are typically IGBTs or MOSFETs, they can be switched at a very high frequency, typically in the hundreds of kilo Hertz, allowing for relatively small capacitors and a compact converter design. The voltage stressing of the switches can however be problematic, as in [89], as in each level of the converter, the switches have to be able

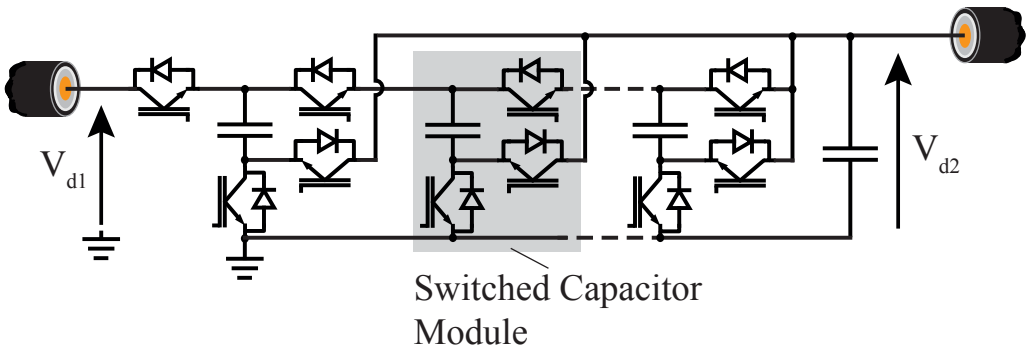

Figure 2.17: Illustration of a modular switched capacitor converter.

to block a different voltage. This topology also suffers from voltage balancing problems of the capacitors as they are of different size [89].

In [90] a modular topology has been proposed to allow for better voltage regulation of the capacitors and a simplified switching mechanism. It is conceivable that this topology allows for easy scaling up to HVDC voltage levels, using a large number of modules, such as shown in figure 2.17. A topology with similar modules but a different switching mechanism has indeed been proposed for such an application in [91]. Both switched capacitor topologies suffer from a large number of switching devices as the number of levels is increased. Furthermore, [91] requires that the lower voltage side DC voltage is equal to the module voltage, which makes it particularly suitable for very large step-ratios, but less so for low ones, as a different switching arrangement or different module design with series connected IGBTs may be required. In its present format both modular designs achieve high efficiency ratings of between 98.75% and 99.1%, although only [91] has been investigated for a high power application of 1 MW.

2.2.4 Modular Cell Based Converters

Some work, particularly over the last two years, has proposed the use of modular cells as can be found in the MMC, of either half- or full-bridge design, in DC/DC converters. Such cells have been shown to be used in DC/AC converters to great effect and efficiency and it is hoped the same can be done in DC/DC converters also.

A front-to-front arrangement of conventional DC/AC converters, utilising cells, has been proposed in [61] to facilitate a DC step by members of Alstom Grid. Such a topology is shown in figure 2.18 and utilises an internal AC connection. This work was used in part for the motivation for a joint project between the author of this work and Alstom grid on front-to-front connected circuit topologies.

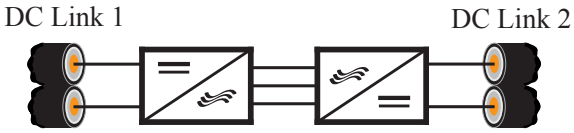

Figure 2.18: Illustration of a front-to-front converter arrangement.

A similar topology has also been investigated in operation similar to that of the DAB converter in [92, 93, 19]. Such topologies operate with high frequency square-waves which make better use of the installed silicon but will require a special transformer design at HVDC power levels. This makes this particular design more experimental, which is fine if there exists no immediate need for a DC/DC converter. For a DC/DC topology based solely on conventional and proven, and thus more reliable, technology, conventional sinusoidal operation of the AC link might be more appropriate.

Recently other DC/DC circuit designs have been proposed in [94, 95, 96, 97, 98] without galvanic isolation. Indeed similar converter topologies had been looked at by the author before these works were published in [99], in an internal technical report. The relevant publications will be referenced in chapter six when the topologies are discussed in more detail.

Chapter 3

Principles and operation of the direct coupled front-to-front converter arrangement

The interconnection of new and legacy HVDC links, i.e. utilising older technology, is one of the more probable uses for HVDC DC/DC inter-connectors. The voltage level of state of the art HDVC links is increasing in line with better cable and overhead line technology. Connecting a new and a legacy link together therefore is likely to require a DC/DC converter to bridge the difference in operating voltage of the two. Considering two typical HVDC voltages, $\pm 320kV$ and $\pm 500kV$ for example, it can be noted that the step-ratio for such an interconnecting DC/DC converter will be relatively low, i.e., less than $5:1$.

Furthermore, considering the rate of new HVDC developments, particularly around Europe and China, such DC inter-connectors may well be required within the next 10 years. To simplify the design process and ensure the reliability of such converters a sensible point to start at, would be to utilise existing HVDC technology, rather than new and untested designs. This could be done by forming a front-to-front (F2F) arrangement of two DC/AC converters, as illustrated in figure 3.1.

Such an arrangement would use commercially available DC/AC converters to build upon the experience gathered with them in other HVDC projects. As Voltage Source Converter (VSC) technology is generally regarded as the most suitable for forming multi-terminal HVDC networks [7], this technology will also be considered for the F2F topology. The following section will introduce the basic operational principle behind two VSCs used in this work. Following this the principles of operation of the F2F topology using the

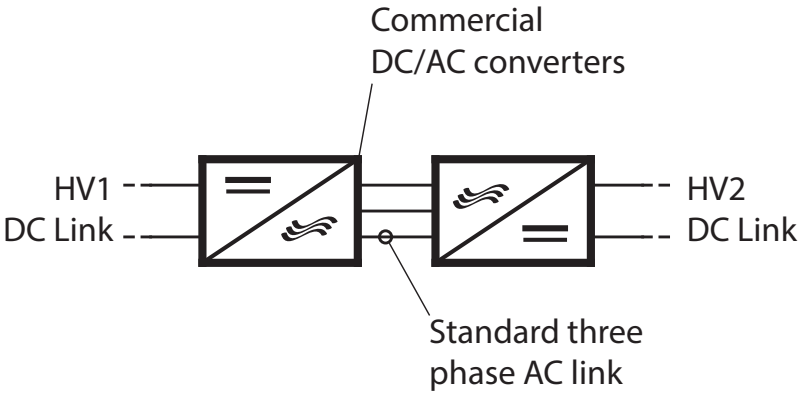

Figure 3.1: Front-to-front arrangement utilising DC/AC converters.

VSCs will be explained. Finally an investigation into the most suitable AC voltage of the internal AC link is presented for a simulated test system.

In the literature review in chapter two some forms of the front-to-front arrangements have already been explored in the literature, and presently still are, using VSCs [92, 93, 19]. This work has however focused on operating the converters in new ways. In this work the idea of utilising a F2F system is to use existing and proven technology, including operating principles, to ensure reliability.

3.1 Converters Considered for F2F Topology

Two different VSCs are considered in this work for the F2F: first, the technically proven and commercially available Modular Multilevel Converter (MMC) [31]. Second, the Alternate Arm Converter (AAC) [34], which is a converter that has been proven in scaled down laboratory work and is expected to become commercially available in the next few years. Both converters use modular cell technology in a similar arrangement. They will be briefly introduced in this section. As this work is not about the optimisation of the individual DC/AC converters, only a basic variety will be explained and used here.

Both converters have a similar structure and therefore a number of common parameters. Figure 3.2 shows the general arrangement of a modular VSC with parallel AC phase connections. Each phase leg consists of two arms. In each arm a stack of cells generates the AC voltage at the mid-point of the phase leg and controls the currents across the inductive network. The latter consist of the arm and phase inductors.

The stack of cells (or cell stack) can be thought of as a controlled voltage source. It consists of a number of series connected cells, typically either of the full- or half-bridge

variety. Other specialised cell types exist but are not the subject of discussion in this work [100]. As the cell voltage is typically small relative to the DC and AC voltages the stacks generate, the converter can operate with a large number of voltage levels. In a full scale converter several hundred cells per stack are not uncommon.

Due to this large number of voltage levels the AC current and voltage waveforms are very clean, i.e., have very little harmonic content. This has been a problem with previous generations of multilevel VSCs, which operated with two or three levels and a PWM switching scheme. This meant significant harmonic content which required comparatively large passive filters.

The AC phase voltage (V_{AC}) definition can be used for all VSCs discussed in this work, as given in (3.1). As each converter is designed for a three-phase arrangement, each phase is shifted by 120° relative to the other two. The term k in the voltage and current definitions denotes the phase number. The AC phase current (I_ϕ) is defined as per (3.2) with a phase delay relative to the AC voltage (α). The converter voltage (V_ϕ) is defined before the phase inductance and therefore has a phase shift relative to the AC voltage, δ, as shown in (3.3).

$$V_{AC}(t) = \hat{V}_{AC} \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3}\right) \tag{3.1}$$

$$I_\phi(t) = \hat{I}_\phi \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \alpha\right) \tag{3.2}$$

$$V_\phi(t) = \hat{V}_\phi \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \delta\right) \tag{3.3}$$

$$\therefore \omega_0 = 2\pi f_{AC} \tag{3.4}$$

3.1.1 Modular Multilevel Converter

The MMC has been commercialised by a number of HVDC equipment manufacturers. Each arm in a converter phase leg conducts half of the AC current continuously throughout the cycle, as illustrated in figure 3.3. The DC current drawn from the HVDC link is split equally between the three phases and flows continuously through each phase leg. Thus the arm current can be expressed as the sum of half the AC and a third of the DC current as per (3.5) and (3.6).

$$I_{tk}(t) = \frac{\hat{I}_{AC}}{2} \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \alpha\right) + \frac{I_d}{3} \tag{3.5}$$

$$I_{bk}(t) = \frac{-\hat{I}_{AC}}{2} \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \alpha\right) + \frac{I_d}{3} \tag{3.6}$$

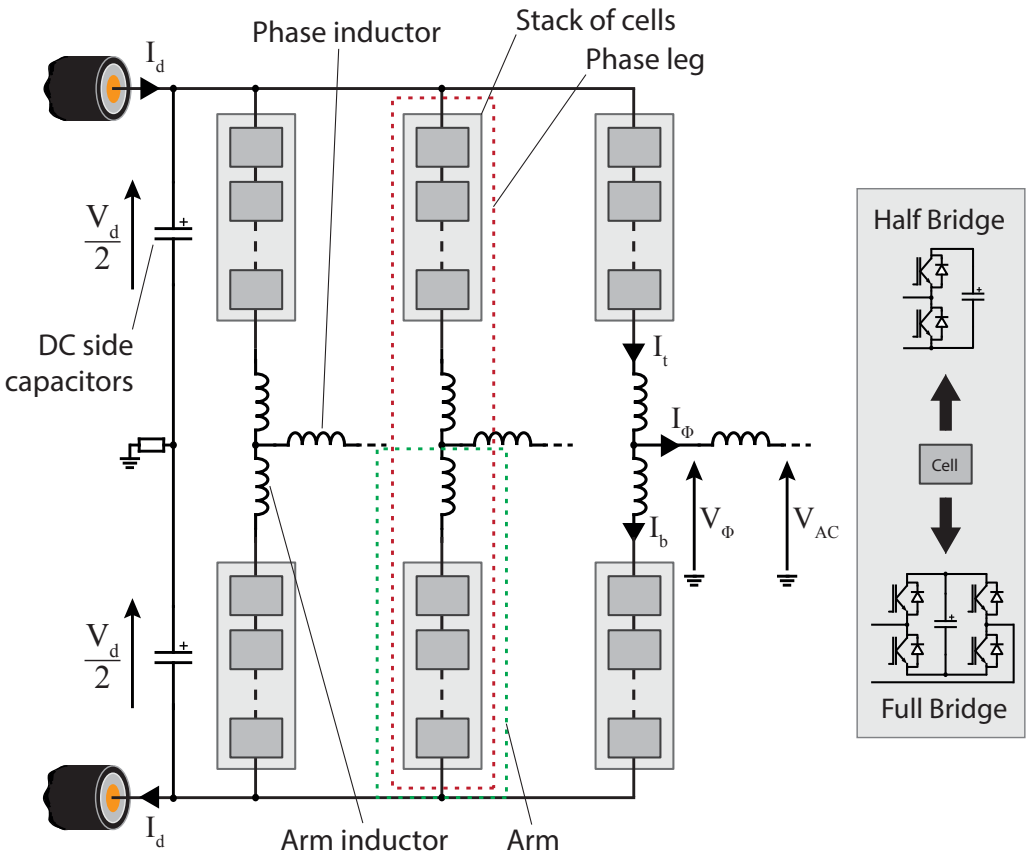

Figure 3.2: General modular VSC circuit.

The stacks of cells have to be able to generate the AC voltage and control the currents across the inductive network. As the currents are sinusoidal and thus have a very gradual change, no extra voltage capability is required to achieve this. Therefore the dominant aspects, when it comes to scaling the required voltage capability in the stacks are the DC and AC voltage magnitudes. From the voltage profile of the stacks shown in figure 3.3 it can be noted that at most a stack has to generate the DC terminal voltage plus the AC magnitude. The voltage across the stack can be expressed as per (3.7) and (3.8) and the peak voltage capability of each stack can thus be found as per (3.9). These equations assume that the voltage phase shift across the arm inductances is negligibly small.

$$V_{stk}(t) = \frac{V_d}{2} - \hat{V}_\phi \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \delta\right) \tag{3.7}$$

$$V_{sbk}(t) = \frac{V_d}{2} + \hat{V}_\phi \sin\left(\omega_0 t - \frac{2\pi(k-1)}{3} + \delta\right) \tag{3.8}$$

$$\hat{V}_{stk,sbk} = \frac{V_d}{2} + \hat{V}_\phi \tag{3.9}$$

Typically the AC voltage is chosen to be of the same magnitude as the DC terminal voltage (i.e., $\hat{V}_\phi = \frac{V_d}{2}$). This is the largest voltage magnitude possible where the stacks can be built using half-bridge cells only which implies fewer devices in the conduction path than full-bridge cells. Raising the AC magnitude above this value means that the stacks have to over-modulate, i.e., add to the DC terminal voltage to generate the AC waveform. This requires full-bridge cells. As the control algorithms are not assumed to be able to handle stacks containing both types of cells, the entire stack has to contain full-bridge cells, no matter the amount of over-modulation required. In terms of terminology, an AC magnitude of less than the DC terminal voltage requires the stack to under-modulate. The concepts of over- and under-modulation are illustrated in figure 3.4.

Third harmonic injection can be used to flatten the peak of the AC voltage generated by the stacks, as explained in [101]. This has not been considered in this work, as it is a modification of the standard operation of the MMC and therefore outside the scope of this work.

Energy Balancing Mechanism

The cells contain capacitors which are switched in and out of the conduction path to generate the required voltage across the stack. This means that the arm current will at times flow through the capacitor and either charge or discharge it, depending on its

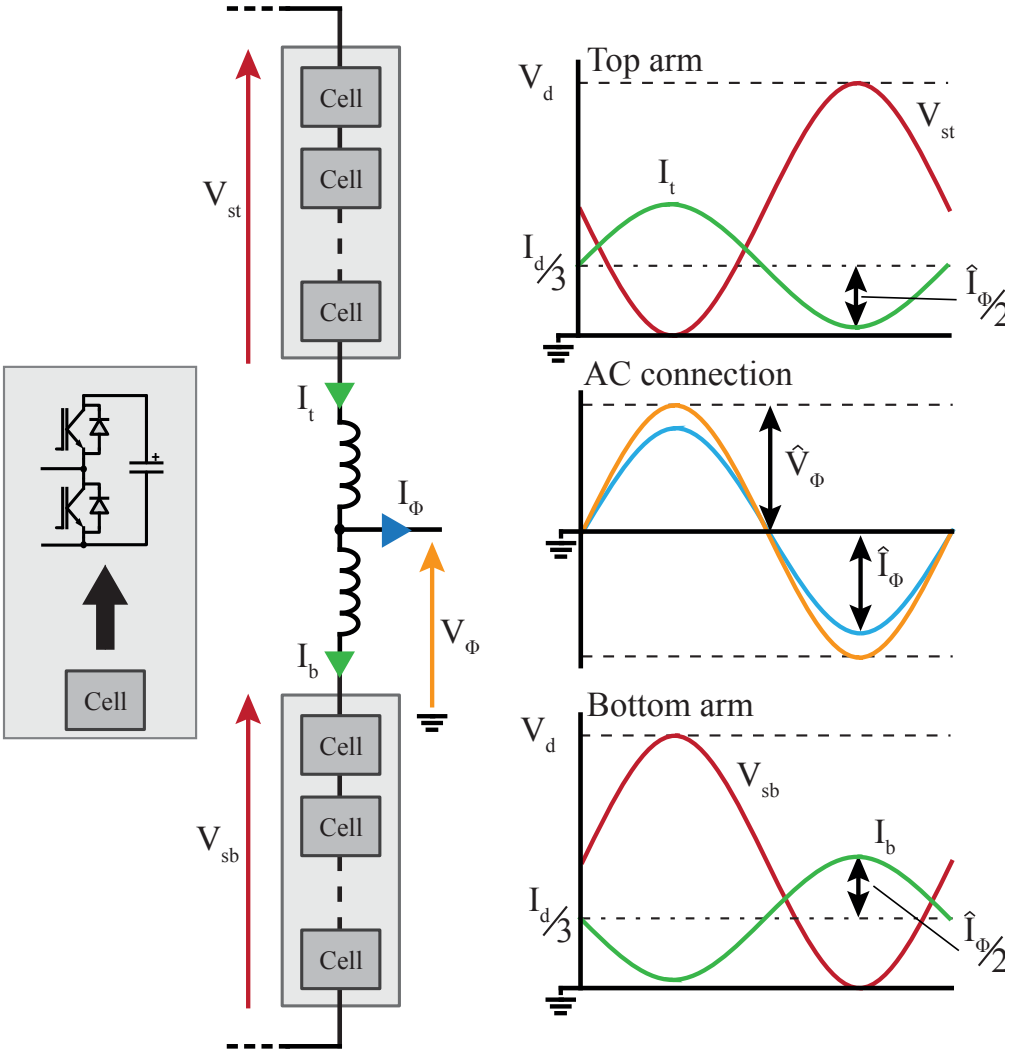

Figure 3.3: Currents and voltages during normal operation of the MMC.

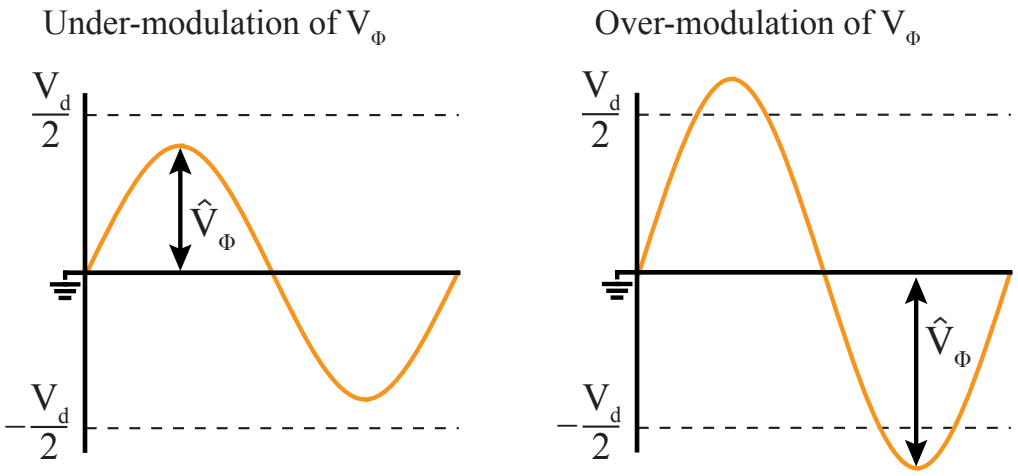

Figure 3.4: Over- and under-modulation of converter voltage definitions.

direction. To ensure that any modular converter is capable of continuous operation, its cells and therefore its stacks of cells have to be energy balanced, to prevent excessive over- or under-charging of the capacitors.

To determine the energy drift, which gradually over- or under-charges the cell capacitors, of the cell stack, we can look at power flowing through the stack integrated over one AC cycle. The energy equations for the top and bottom stack for one phase, $k = 1$, are shown in (3.10) and (3.11). As the currents and voltages are assumed to be shifted by the same phase angle for the other two phases, the energy equations will be the same for them. Phase imbalances are not considered here, as the AC link in the front-to-front topology will be internal to the system, which would make it unlikely for a phase unbalance to occur.

$$\begin{aligned} E_{st} &= \int_0^{\frac{2\pi}{\omega_0}} V_{st}(t) I_{st}(t) \mathrm{d}t \\ &= \frac{\pi}{\omega_0} \left(\frac{V_d I_d}{3} - \frac{\hat{V}_\phi \hat{I}_\phi}{2} \cos(\delta - \alpha) \right) \end{aligned} \tag{3.10}$$

$$\begin{aligned} E_{sb} &= \int_0^{\frac{2\pi}{\omega_0}} V_{sb}(t) I_{sb}(t) \mathrm{d}t \\ &= \frac{\pi}{\omega_0} \left(\frac{V_d I_d}{3} - \frac{\hat{V}_\phi \hat{I}_\phi}{2} \cos(\delta - \alpha) \right) \end{aligned} \tag{3.11}$$

The energy equations show that by adjusting the DC current component, flowing through the arm, the power drawn from the AC side can be matched, such that the

stack's energy drift equates to zero. This can be done for any value of delta and alpha. Therefore the MMC does not require any further energy balancing mechanisms to avoid energy drift.

For transient energy drifts, which require energy to be moved between the top and bottom stacks, an additional vertical balancing current can be introduced, called $I_v(t)$. This current can simply be defined as a square-wave at the same frequency as the AC wave-form, as defined in (3.12). The effect of this vertical balancing current on the stacks' energy is derived in (3.13) and (3.14). From the equations it can be noted that an equal and opposite energy drift is achieved in the top and bottom stacks, which effectively moves energy from one to the other. By adjusting the sign and the value of $\hat{I}_v$ the amount of energy and direction, can be varied by the controller.

The energy that can be exchanged between the stacks is limited by the phase angle delay δ. As this is due to the impedance of the phase inductance, it can reasonably be expected to be small and well below the value of $\frac{\pi}{2}$, which would disable the vertical balancing.

$$I_v(t) = \hat{I}_v \cdot \mathrm{sqw}\left(\omega_0 t\right) \tag{3.12}$$
$$\therefore\ \mathrm{sqw}\left(\omega_0 t\right) = \begin{cases} 1 & \text{if } 0 \leq t < \frac{\pi}{\omega_0}, \\ -1 & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0}. \end{cases}$$

$$\begin{aligned} E_{stv} &= \int_0^{\frac{2\pi}{\omega_0}} V_{st}(t) I_v(t) \mathrm{d}t \\ &= -4\cos(\delta)\frac{\hat{V}_\phi \hat{I}_\phi}{\omega_0} \end{aligned} \tag{3.13}$$

$$\begin{aligned} E_{sbv} &= \int_0^{\frac{2\pi}{\omega_0}} V_{sb}(t) I_v(t) \mathrm{d}t \\ &= +4\cos(\delta)\frac{\hat{V}_\phi \hat{I}_\phi}{\omega_0} \end{aligned} \tag{3.14}$$

$$\tag{3.15}$$

As the energy mismatch between the stacks during steady-state operation is expected to be very small, the magnitude of the vertical balancing current is expected to be small also. As this an AC current which is controlled to flow through the arms and not into the AC connection, it will circulate through the DC side capacitors. As the current magnitude is small however, the voltage ripple due to this current is also kept small. Furthermore since the square-wave can be kept symmetrical for the entire cycle, the DC side capacitors

will not experience any energy drift due to it. An alternative balancing method using sinusoidal wave-forms has also been proposed in [102].

3.1.2 Alternate Arm Converter

The Alternate Arm Converter (AAC) is a recent modification of the MMC. As this converter is presently being readied for commercialisation and presently is the only direct contender to the MMC, which has already been commercialised, it is a sensible second choice to use in the F2F system analysis.

The AAC, as just mentioned, is a modification of the MMC: it also consists of three phase legs connected in parallel to the DC link. Each phase leg consists of two stacks. The modification is the way the AC current is directed through the converter arms, as illustrated in figure 3.5: Each arm conducts the AC current for half of the AC cycle. Whilst the arm conducts the cells in the stack generate the AC voltage at the midpoint of the phase leg - just as in the MMC.

As each arm conducts the full AC current for half a cycle at a time, the other arm's current path can be interrupted through the use of simple switches in series with the cells. These are called the directors switches. These director switches replace some of the cells, which in the MMC would generate the AC voltage. Therefore each director switch is typically a number of series connected IGBTs to ensure that the entire director switch can withstand the required voltage imposed across it.

The arm currents can be defined as per (3.16) and (3.17).

$$I_t(t) = \begin{cases} I_\phi(t) & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ 0 & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.16}$$

$$I_b(t) = \begin{cases} 0 & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ I_\phi(t) & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.17}$$

The voltage generated by the stacks of cells can be expressed as shown in (3.18) and (3.19). Similarly the voltage across the director switches can be defined as per (3.20) and (3.21).

$$V_{st}(t) = \begin{cases} \frac{V_d}{2} - V_\phi & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ \frac{V_d}{2} & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.18}$$

$$V_{sb}(t) = \begin{cases} \frac{V_d}{2} & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ \frac{V_d}{2} - V_\phi & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.19}$$

$$V_{dt}(t) = \begin{cases} 0 & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ -V_\phi & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.20}$$

$$V_{db}(t) = \begin{cases} -V_\phi & \text{if } 0 \leq t < \frac{\pi}{\omega_0} \\ 0 & \text{if } \frac{\pi}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.21}$$

Energy Balancing Mechanism

The energy drift of the stacks can be found by integrating the current flowing through the arm and the voltage it generates, as shown in (3.22) and (3.23).

$$\begin{aligned} E_{st} &= \int_0^{\frac{2\pi}{\omega_0}} V_{st}(t) I_t(t) \mathrm{d}t \\ &= \frac{V_d \hat{I}_\phi}{\omega_0} \cos(\alpha) - \frac{\hat{V}_\phi \hat{I}_\phi \pi}{2\omega_0} \cos(\alpha - \delta) \end{aligned} \tag{3.22}$$

$$\begin{aligned} E_{sb} &= \int_0^{\frac{2\pi}{\omega_0}} V_{sb}(t) I_b(t) \mathrm{d}t \\ &= \frac{V_d \hat{I}_\phi}{\omega_0} \cos(\alpha) - \frac{\hat{V}_\phi \hat{I}_\phi \pi}{2\omega_0} \cos(\alpha - \delta) \end{aligned} \tag{3.23}$$

Using the energy drift equations ((3.22) and (3.23)), the conditions required for the drift to be zero can be found as per (3.24). The AC converter voltage magnitude for which the energy drift in the cell stacks is zero, given a certain DC voltage magnitude, is called the sweet-spot.

$$E_{st} = 0 \tag{3.24}$$

$$\therefore \hat{V}_\phi = \frac{2V_d}{\pi} \frac{\cos(\alpha - \delta)}{\cos(\alpha)} \tag{3.25}$$

If the AAC is however not operated at the sweet-spot, a rebalancing mechanism is required to counteract the energy drift. This is done by introducing an overlap period, during which both arms are in conduction, i.e., both director switches are closed. The overlap period per half cycle can be expressed as an angle, ϵ. During the overlap period a DC current can flow through both stacks to counter-act the energy drift. This concept is illustrated in figure 3.6.

The overlap period affects the voltage capabilities of the stacks: as the arms have to stay in conduction for longer, they require more cells to support the additional voltage to generate the AC voltage further into the other half-cycle. For similar reasons fewer director switch devices are required as they are replaced by cells. The equations for the

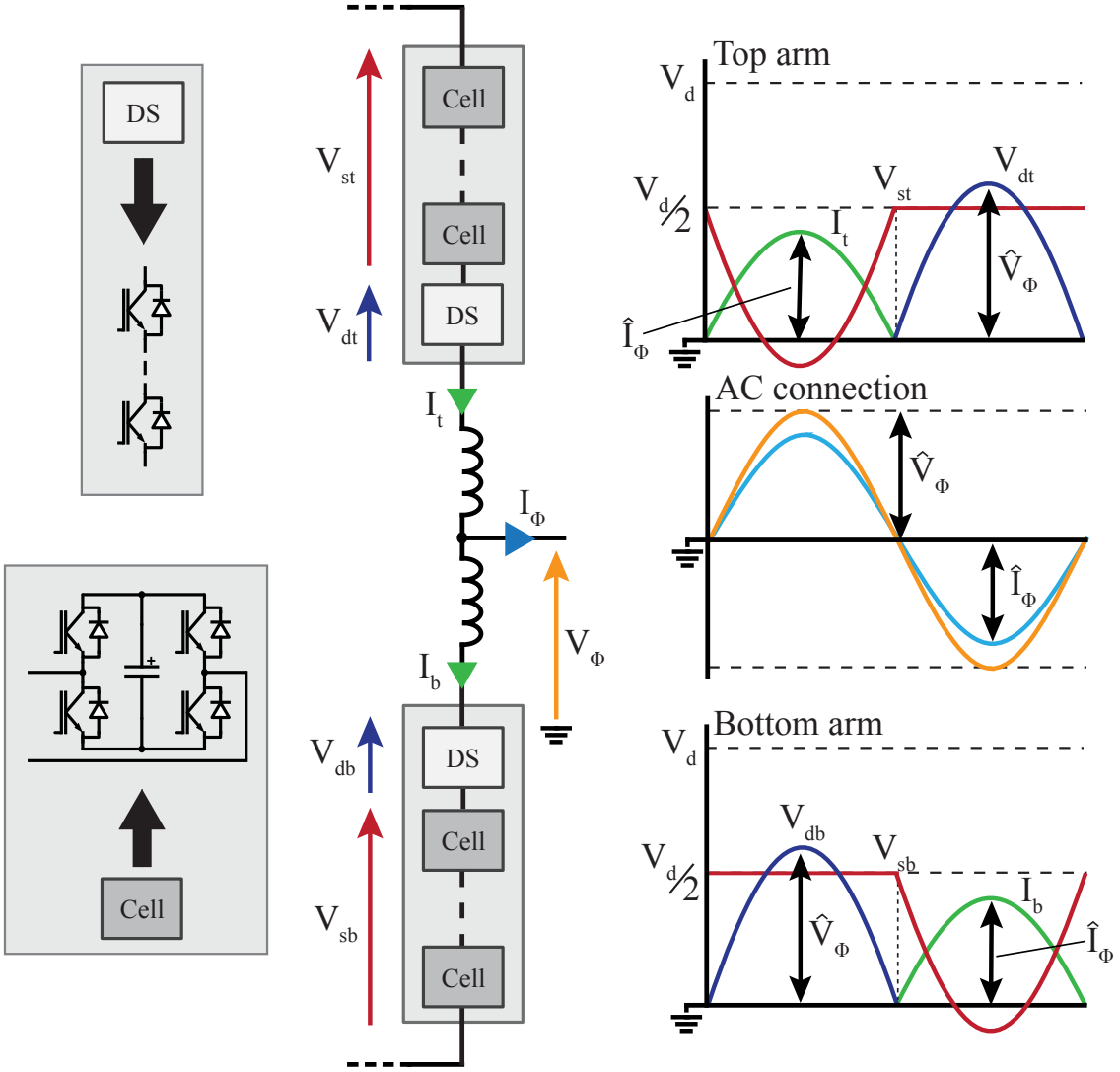

Figure 3.5: Currents and voltages during normal operation of the AAC.

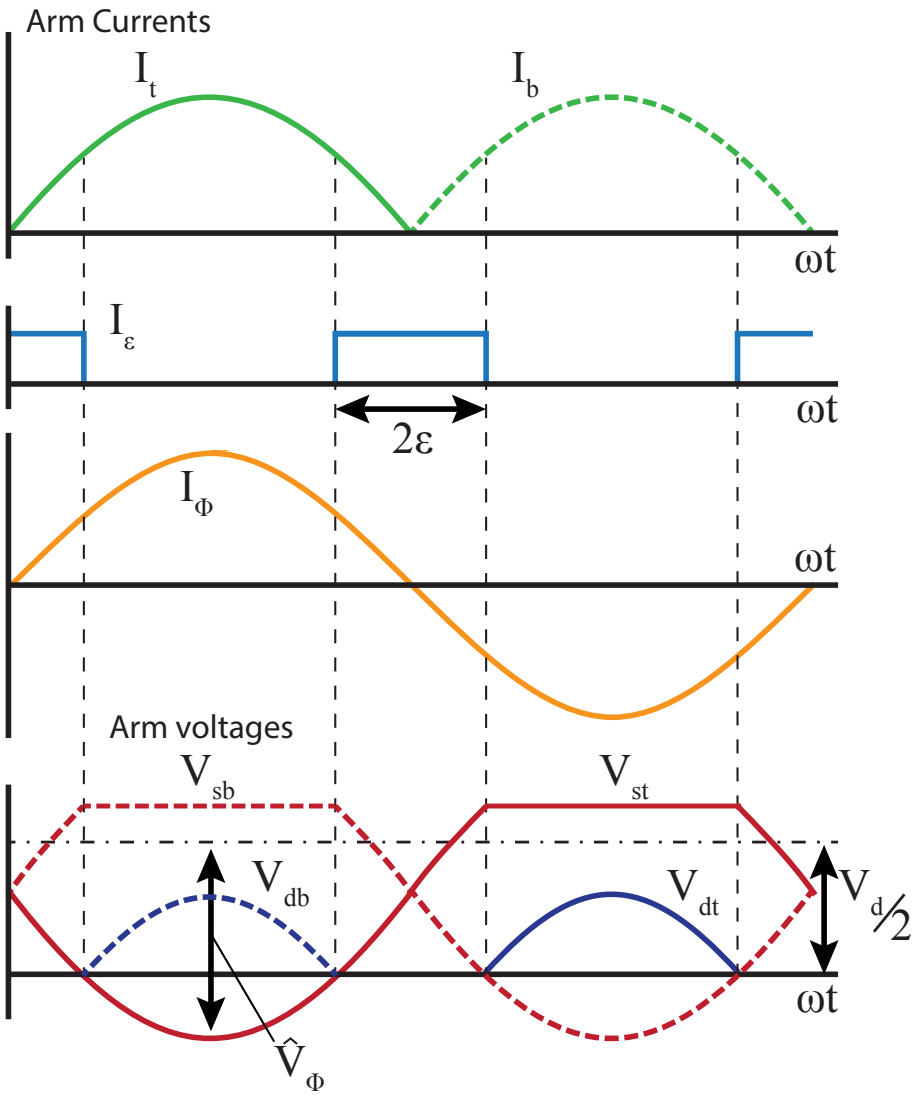

Figure 3.6: Arm currents and stack voltages with overlap period.

voltages generated by the stacks and director switches, taking the overlap period into account, are shown in (3.26) to (3.29).

$$V_{st}(t) = \begin{cases} \frac{V_d}{2} - V_\phi(t) & \text{if } 0 \leq t < \frac{\pi+\epsilon}{\omega_0} \\ 0 & \text{if } \frac{\pi+\epsilon}{\omega_0} \leq t < \frac{2\pi-\epsilon}{\omega_0} \end{cases} \tag{3.26}$$

$$V_{sb}(t) = \begin{cases} 0 & \text{if } 0 \leq t < \frac{\pi+\epsilon}{\omega_0} \\ \frac{V_d}{2} - V_\phi(t) & \text{if } \frac{\pi+\epsilon}{\omega_0} \leq t < \frac{2\pi-\epsilon}{\omega_0} \end{cases} \tag{3.27}$$

$$V_{dt}(t) = \begin{cases} 0 & \text{if } 0 \leq t < \frac{\pi+\epsilon}{\omega_0} \\ V_\phi(t) & \text{if } \frac{\pi+\epsilon}{\omega_0} \leq t < \frac{2\pi-\epsilon}{\omega_0} \end{cases} \tag{3.28}$$

$$V_{db}(t) = \begin{cases} V_\phi(t) & \text{if } 0 \leq t < \frac{\pi+\epsilon}{\omega_0} \\ 0 & \text{if } \frac{\pi+\epsilon}{\omega_0} \leq t < \frac{2\pi-\epsilon}{\omega_0} \end{cases} \tag{3.29}$$

The effect of the overlap current (I_ϵ) on the stacks' energy is illustrated in (3.30) and (3.31). From the equations it can be noted that the overlap current has an equal effect on both stacks in a phase leg. Furthermore the energy transferred can be adjusted by varying the length of the overlap period (ϵ) and the magnitude of the overlap current ($\hat{I}_\epsilon$). The value of $\hat{I}_\epsilon$ can be adjusted dynamically by the energy controller during operation. The overlap length however determines the number of cells and is therefore fixed by the designer.

$$\begin{aligned} E_{st\epsilon} &= \int_0^{\frac{2\pi}{\omega_0}} V_{st}(t)\hat{I}_\epsilon \mathrm{d}t \\ &= \frac{2\hat{I}_\epsilon V_d \epsilon}{\omega_0} \end{aligned} \tag{3.30}$$

$$\begin{aligned} E_{sb\epsilon} &= \int_0^{\frac{2\pi}{\omega_0}} V_{sb}(t)\hat{I}_\epsilon \mathrm{d}t \\ &= \frac{2\hat{I}_\epsilon V_d \epsilon}{\omega_0} \end{aligned} \tag{3.31}$$

As the overlap balancing method has an equal effect on both stacks a separate balancing mechanism has to be employed to shift energy vertically between stacks inside the same phase leg. A similar method to the one used in the MMC can be used: by running a square-wave during the overlap period this can be achieved. The principle of operation for this vertical balancing is illustrated in figure 3.7. It should be noted that to achieve the same effect during the two overlap periods per cycle, the square-wave has to be inverted

for one of them. The vertical balancing current can thus be defined as per (3.32).

$$I_v = \begin{cases} \hat{I}_v & \text{if} \quad 0 \leq t < \frac{\epsilon}{\omega_0} \\ \hat{I}_v & \text{if} \quad \frac{\pi-\epsilon}{\omega_0} \leq t < \frac{\pi}{\omega_0} \\ -\hat{I}_v & \text{if} \quad \frac{\pi}{\omega_0} \leq t < \frac{\pi+\epsilon}{\omega_0} \\ -\hat{I}_v & \text{if} \quad \frac{2\pi-\epsilon}{\omega_0} \leq t < \frac{2\pi}{\omega_0} \end{cases} \tag{3.32}$$

The effect of the vertical balancing on the energy of the stacks is shown in (3.33) and (3.34). From the equations it can be noted that this energy balancing mechanism has an equal and opposite effect on the top and bottom stacks. An increase in overlap length requires a smaller vertical balancing current magnitude to cause the same effect (assuming $\epsilon < \frac{\pi}{2}$).

$$\begin{aligned} E_{stv} &= \int_0^{\frac{2\pi}{\omega_0}} V_{st}(t) I_v \mathrm{d}t \\ &= -\frac{4\hat{V}_\phi \hat{I}_v}{\omega_0} \sin(\epsilon) \end{aligned} \tag{3.33}$$

$$\begin{aligned} E_{sbv} &= \int_0^{\frac{2\pi}{\omega_0}} V_{sb}(t) I_v \mathrm{d}t \\ &= \frac{4\hat{V}_\phi \hat{I}_v}{\omega_0} \sin(\epsilon) \end{aligned} \tag{3.34}$$

Even when the converter is operated at its sweet-spot, the capability to provide some vertical balancing is essential to ensure a stable operation. Therefore even when the converter doesn't need an overlap period to rebalance a steady-state energy drift some overlap-period should be built into the converter to allow for vertical balancing.

3.2 F2F System Description

To connect two DC links operating at slightly different DC voltages, two DC/AC converters can be used in a front-to-front arrangement, as illustrated in figure 3.8. The converters are linked via an internal AC connection. In this chapter this connection is assumed to only consist of a phase inductance, making it a so called directly coupled system. This implies that the two converters share a common AC voltage. This section provides voltage and current descriptions of the system and introduces the control system developed for it.

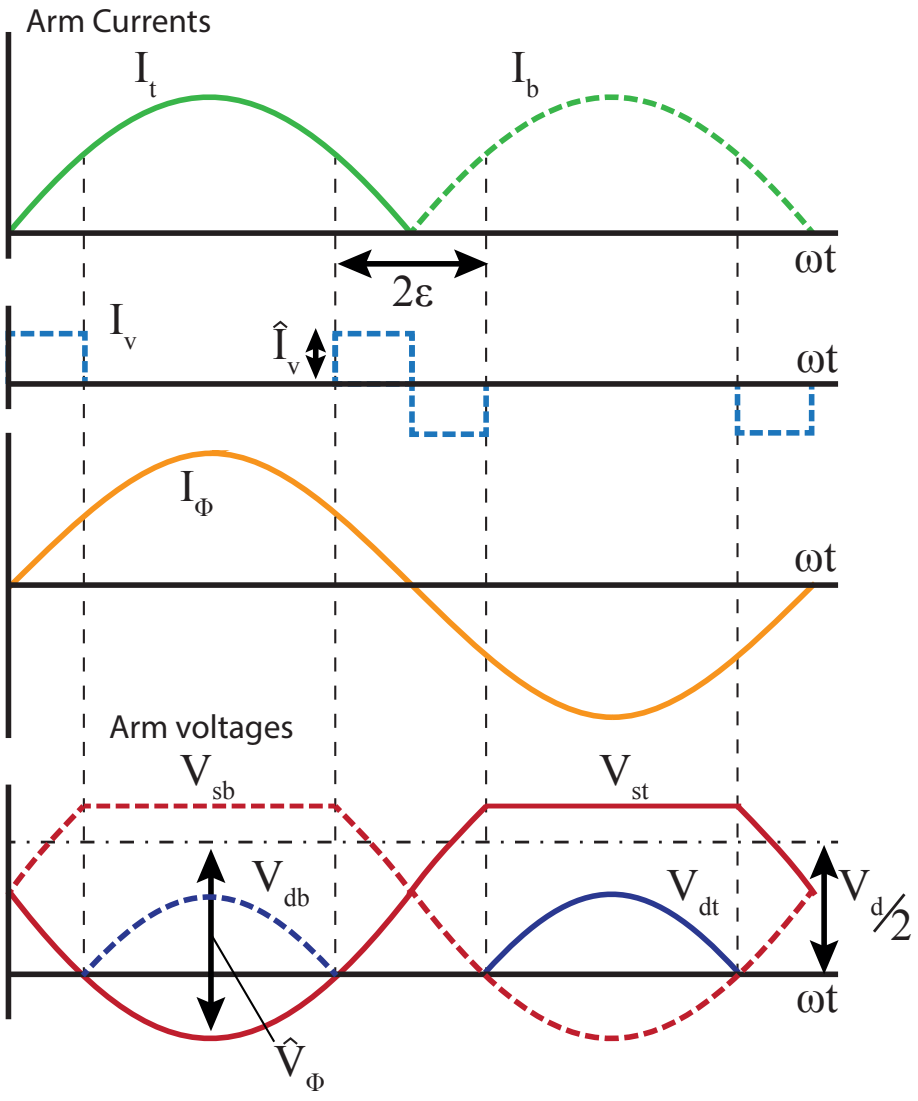

Figure 3.7: Arm currents and stack voltages with vertical balancing.

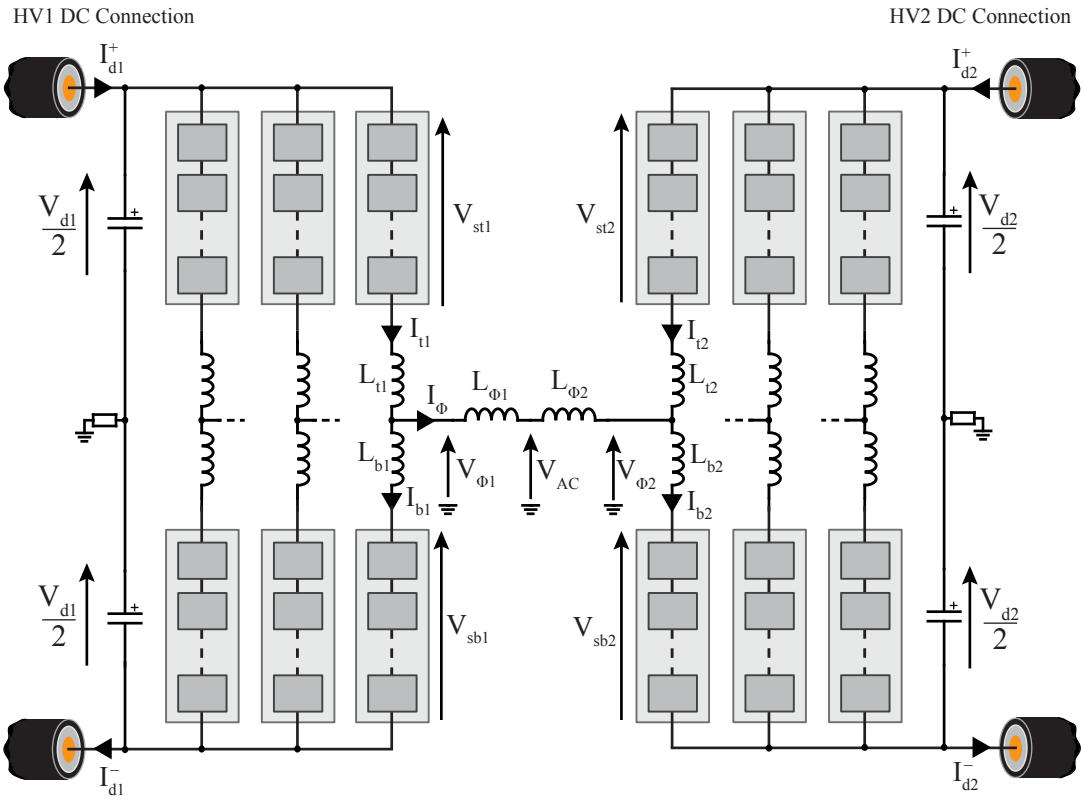

Figure 3.8: Front-to-front direct coupled arrangement with two VSCs.

3.2.1 Coupling Description

The converters considered here use a standard three-phase arrangement. As such each phase is a duplicate of the other two but operated with a 120° phase shift. Therefore for the purpose of the voltage and current definitions as well as the controller, only one phase will be analysed here, as the same definitions apply to the other two.

Using the same notation as for the voltage and current definitions for the VSCs, the AC voltage (V_{AC}) at the midpoint of the phase inductance (shown as a split inductance $L_{\phi 1,\phi 2}$) can be defined as per (3.1) and the phase AC current (I_ϕ) as per (3.2). In the F2F system two converter voltages exist, as defined in (3.35) for the HV1 side converter and in (3.36) for the HV2 side converter.

$$V_{\phi 1} = \hat{V}_{\phi 1} \sin\left(\omega_0 t + \delta_1\right) \tag{3.35}$$

$$V_{\phi 2} = \hat{V}_{\phi 2} \sin\left(\omega_0 t + \delta_2\right) \tag{3.36}$$

The arm current definitions depend on the type of converter used and have been presented in sections 3.1.1 and 3.1.2.

When considering the power flows across the direct-coupled AC connection a positive power transfer refers to a power flow from the HV1 side to the HV2 side. The voltage V_{AC} can be thought of as the common mode voltage of the AC link. Thus the converter voltages $V_{\phi 1,\phi 2}$ can be expressed in terms of V_{AC} and a voltage vector ($u_{\phi 1,\phi 2}$) perpendicular to the phase current I_ϕ as per (3.37). The AC voltages and currents can be visualised in a phasor diagram as shown in figure 3.9.

$$\begin{aligned} V_{\phi 1,\phi 2} &= V_{AC} + u_{\phi 1,\phi 2} \\ &: \; u_{\phi 1} = \hat{u}_{\phi 1} \cos(\omega_0 t + \alpha) \\ &: \; u_{\phi 2} = -\hat{u}_{\phi 2} \cos(\omega_0 t + \alpha) \end{aligned} \tag{3.37}$$

The apparent power definitions using the converter voltages can thus be expressed as per (3.38) and (3.39). These definitions assumes that a power transfer reference is defined for the common-mode voltage and show the power flowing through each phase. The phase angle delay of the phase current, α, is thus determined by the power transfer reference. If no reactive power is transferred between the converters, $\alpha = 0$. The reactive power demanded by the phase inductances, $L_{\phi 1,\phi 2}$, is satisfied by adding the voltages $u_{\phi 1,\phi 2}$ to the common mode voltage, V_{AC}. The phasor diagram illustrates how the addition of this

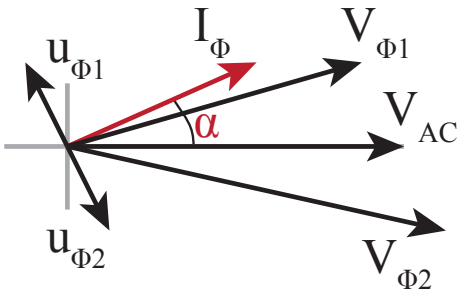

Figure 3.9: Phasor diagram of F2F Ac voltages and current.

voltage can significantly affect the magnitude of the converter voltages (relative to V_{AC}). To avoid having to add additional cells to the cell stacks to generate a higher converter voltage the reactive power demand of the phase inductance should be minimised.

$$\begin{aligned} S_{\phi 1} &= V_{\phi 1} I_{\phi}^{*} \\ &= V_{AC} I_{\phi}^{*} + u_{\phi 1} I_{\phi}^{*} \\ &= P_{AC} + j\left(Q_{AC} + Q_{L\phi 1}\right) \end{aligned} \tag{3.38}$$

$$\begin{aligned} S_{\phi 2} &= V_{\phi 2} I_{\phi}^{*} \\ &= -V_{AC} I_{\phi}^{*} - u_{\phi 2} I_{\phi}^{*} \\ &= -P_{AC} + j\left(-Q_{AC} + Q_{L\phi 2}\right) \end{aligned} \tag{3.39}$$

In a DC/AC application the phase inductance is part of the AC side filter to ensure that the AC waveforms remain within tolerable limits. As the AC link of the F2F arrangement is fully internal to the system no such limitations apply. Thus the best way to minimise the reactive power demand of the phase inductance is to not include it in the circuit, effectively setting $L_{\phi 1,\phi 2} = 0$.

3.2.2 System Controller

To ensure that the set power transfer reference is tracked correctly by the F2F system, a closed loop control system has been designed and implemented. The controller is based upon controllers designed for the AAC in [102]. It consists of three general stages, as illustrated in figure 3.10: first, the generation of time domain current references; second, the conversion of the current references into required stack voltages; and third, the translation of the stack voltages into cell level commands. Each phase of the F2F system is controlled separately.

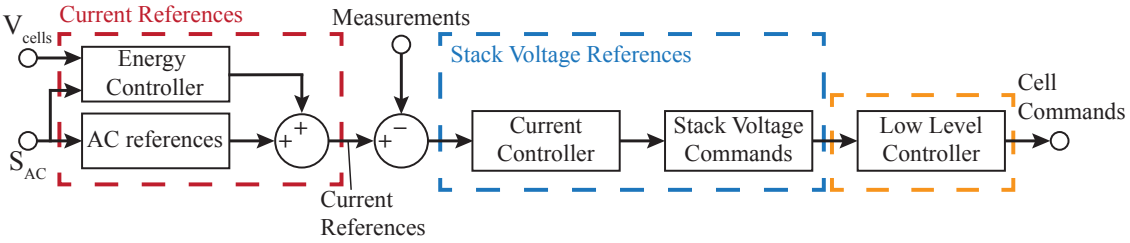

Figure 3.10: F2F controller overview.

AC References

The F2F system takes a single apparent power reference as an input (P and Q reference). One third of the power reference is transferred by each phase. Knowing the power transfer definition, a positive power transfer flows from the HV1 side to the HV2 side, the power reference per phase is used to determine the AC current magnitude and phase angle relative to V_{AC} using (3.40), where S_{AC} denotes the apparent power transferred between the converters per phase. The control mechanism is illustrated in figure 3.11.

$$S_{AC} = V_{AC} I_{\phi}^{*} \tag{3.40}$$

Depending on the type of VSC used, the AC current reference is translated into the AC component of the arm current references, as described in the arm current equations in sections 3.1.1 and 3.1.2. This results in a time domain reference of the AC current component for the phase current as well as the arm current for both converters.

Energy Controller

The energy controller monitors the cells in each stack and converts their voltage into the energy contained within the stack using K_e, as per (3.41). In the equation C_c refers to the cell capacitance and V_c to the cell voltage. Figure 3.12 illustrates the energy control circuit used for each phase-leg per converter. The controller outputs the magnitude of the vertical balancing using the difference error in the energy of the top and bottom stacks in each phase leg. The DC current reference is found by adding a feed-forward term to a feed-back term. The latter is found from the absolute energy mismatch found in the stacks.

This set up is used as shown for the MMC implementation. For the AAC, the feed-forward term is taken out and the overlap balancing current magnitude, $\hat{I}_{\epsilon}$, is set by the feed-back term only. The reference is also set to zero when $\omega_0 t$ is outside the overlap

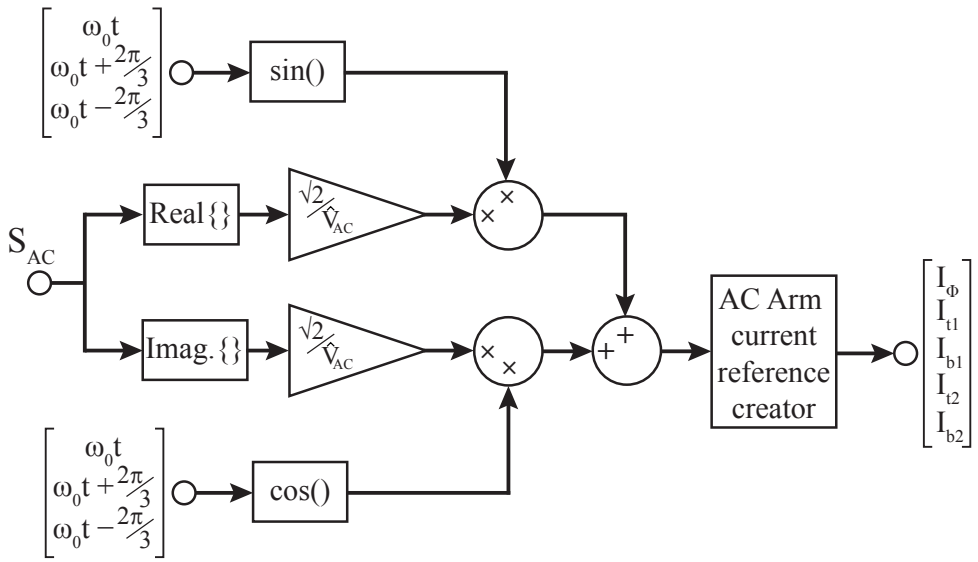

Figure 3.11: AC reference current builder for F2F system.

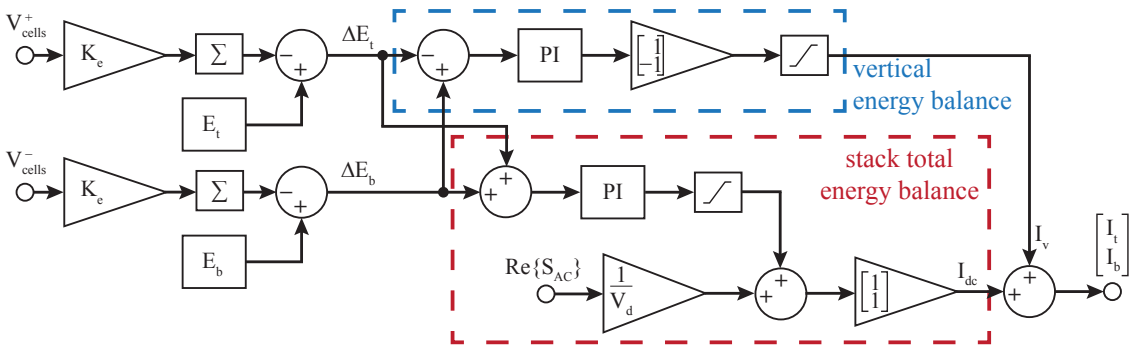

Figure 3.12: F2F Energy controller per converter phase-leg.

period. Similarly the magnitude of the vertical balancing reference has to be inverted at the appropriate times, as explained in section 3.1.2.

$$E_{cell} = \frac{1}{2} C_c V_c^2 \tag{3.41}$$

$$\therefore K_e = \frac{C_c}{2} \tag{3.42}$$

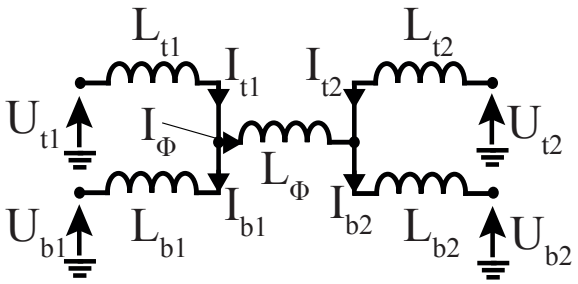

Figure 3.13: F2F equivalent inductive network.

Current Controller

After the AC and DC (or overlap) current references are combined and the measured currents have been subtracted, the resulting error signal is passed to the current controller. A real controller would be implemented on a digital system, such as an FPGA or a CPU, and therefore have a limited sampling frequency. Realistically a sampling frequency of tens of kilo Hertz is used. To emulate this fact in the simulation the current control block is only executed at the sampling frequency.

The current controller works on the following principle: the arm and phase inductances in each phase of the F2F system form an inductive network, as shown in figure 3.13. The stacks of cells can be viewed as controllable voltage sources. This means that the terminal voltages of this inductive network can directly be generated by the cell stacks. Using the basic VI relationship for an inductor ($V = L\frac{dI}{dt}$), the currents flowing through the network can be controlled by generating the required terminal voltages.

The state-space of the inductive network can be reduced to three currents as shown in (3.43).

$$\begin{bmatrix} 0 & 1 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} U_{t1} \\ U_{b1} \\ U_{t2} \\ U_{b2} \end{bmatrix} = \begin{bmatrix} L_\phi + L_{b1} & -L_{b1} & L_{b2} \\ -L_{b1} & L_{t1} + L_{b1} & 0 \\ L_{t2} & 0 & L_{t2} + L_{b2} \end{bmatrix} \begin{bmatrix} \dot{I}_\phi \\ \dot{I}_{t1} \\ \dot{I}_{b2} \end{bmatrix} \tag{3.43}$$

$$\therefore M_u u = M_L \dot{x} \tag{3.44}$$

The state-space can be expressed in the standard form $\dot{x} = Ax + Bu$ as shown in (3.45).

$$\dot{x} = \underbrace{\mathbf{0}_{3,3}}_{A} x + \underbrace{(M_u \backslash M_L)}_{B} u \tag{3.45}$$

To improve the tracking of the sinusoidal current reference and avoid steady-state errors, the state-space has been extended by standard second-order filters. In the AAC this state-space expansion has only been applied to the phase current reference as the arm currents only include piece-wise sinusoidal waveforms.

A 50 Hz band-pass filter, as described in (3.46), was used to expand the state-space as shown in (3.48). The variables Q_{50} and k_{50} denote the quality factor and the gain of the filter function. A high quality factor of 10 and moderate gain value of 1 have been found to work best.

$$H_{50}(s) = \frac{\mathrm{s}k_{50}\omega_{50}}{\mathrm{s}^2 Q_{50} + \mathrm{s}\omega_{50} + Q_{50}\omega_{50}^2} \tag{3.46}$$

$$= \frac{R_{50}}{x} \tag{3.47}$$

$$\begin{bmatrix} \dot{x} \\ \dot{R}_{50} \\ \ddot{R}_{50} \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & 0 & 1 \\ \frac{k_{50}\omega_{50}}{Q_{50}} A & -\omega_{50}^2 & -\frac{\omega_{50}}{Q_{50}} \end{bmatrix} \begin{bmatrix} x \\ R_{50} \\ \dot{R}_{50} \end{bmatrix} + \begin{bmatrix} B \\ 0 \\ \frac{k_{50}\omega_{50}}{Q_{50}} B \end{bmatrix} u \tag{3.48}$$

To include an integrator action, a low-pass filter with the general form, as per (3.49), has also been included. It's state-space expansion has been illustrated in (3.51). For this filter a quality factor of 1 and a gain of 1 have been found to work best. The corner frequency used is 1 Hz.

$$H_0(s) = \frac{k_0 Q_0 \omega_0^2}{\mathrm{s}^2 Q_0 + \mathrm{s}\omega_0 + Q_0\omega_0^2} \tag{3.49}$$

$$= \frac{R_0}{x} \tag{3.50}$$

$$\begin{bmatrix} \dot{x} \\ \dot{R}_{50} \\ \ddot{R}_{50} \end{bmatrix} = \begin{bmatrix} A & 0 & 0 \\ 0 & 0 & 1 \\ k_0\omega_0 & -\omega_0^2 & -\frac{\omega_0}{Q_0} \end{bmatrix} \begin{bmatrix} x \\ R_0 \\ \dot{R}_0 \end{bmatrix} + \begin{bmatrix} B \\ 0 \\ 0 \end{bmatrix} u \tag{3.51}$$

The expanded state-space can thus be written in standard form as shown in (3.52). This state-space is still however defined in continuous time. To take the fact that the current controller is sampled at a frequency f_{cs} into account, the state-space has to be discretised as shown in (3.53). The discretised state matrices are labelled A_d and B_d. I

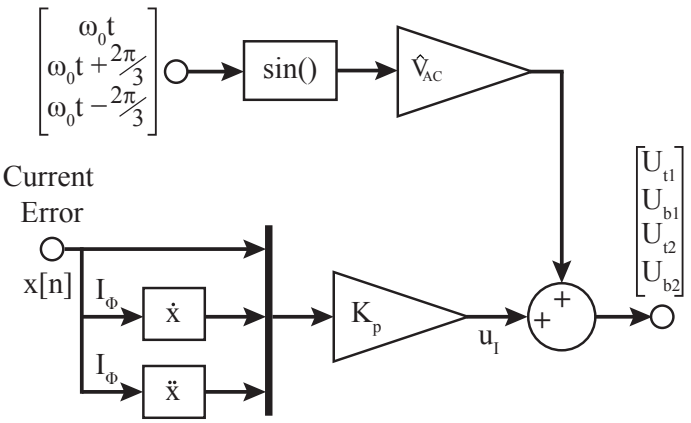

Figure 3.14: F2F curret controller.

denotes the identity matrix.

$$\dot{x_e} = A_e x_e + B_e u_e \tag{3.52}$$

$$e^{\begin{bmatrix} A_e & B_e \\ 0 & 0 \end{bmatrix} \cdot T_{cs}} = \begin{bmatrix} A_d & B_d \\ 0 & I \end{bmatrix} \tag{3.53}$$

The current controller is shown in figure 3.14. The discretised current error can be seen to be extended by it first and second derivatives for the two filters included in the extended state-space. The gain matrix K_p can be found using Linear Quadratic Regulator (LQR) theory. An existing function in Matlab (function: *dlqr()*) can be used, which minimises the cost function, J (as per (3.54)) over an infinite time horizon.

$$J = \sum_{k=0}^{\infty} \left(\underbrace{\Delta x[k]^T Q \Delta x[k]}_{J_x} + \underbrace{\Delta u[k]^T R \Delta u[k]}_{J_u} \right) \tag{3.54}$$

As there are a total of five currents in the inductive network (i.e., per phase), J_x can be expressed as shown in (3.55). The variables $q_{t1,t2,b1,b2}$ are the costs associated with the corresponding current errors. Since only three currents are required to control the system,

J_x can be reduced as shown in (3.56).

$$J_x = q_\phi \Delta I_\phi^2 + q_{t1} \Delta I_{t1}^2 + + q_{b1} \Delta I_{b1}^2 + q_{t2} \Delta I_{t2}^2 + q_{b2} \Delta I_{b2}^2 \tag{3.55}$$

$$\begin{aligned} &= (q_\phi + q_{b1} + q_{t2}) \Delta I_\phi^2 + (q_{t1} + q_{b1}) \Delta I_{t1}^2 + (q_{b2} + q_{t2}) \Delta I_{b2}^2 \\ &\quad -2q_{b1} \Delta I_\phi^2 \Delta I_{t1}^2 - 2q_{t2} \Delta I_\phi^2 \Delta I_{b2}^2 \end{aligned} \tag{3.56}$$

The cost matrix Q can thus be defined as shown in (3.57).

$$Q = \begin{bmatrix} q_\phi + q_{b1} + q_{t2} & -q_{b1} & -q_{t2} \\ -q_{b1} & q_{t1} + q_{b1} & 0 \\ -q_{t2} & 0 & q_{b2} + q_{t2} \end{bmatrix} \tag{3.57}$$

By varying the difference in cost on two particular current errors (using $q_{t,b,p}$) the errors can be ranked. A more highly ranked current (i.e. a higher cost than others) will result in a greater response magnitude. Changing the difference in magnitude between the cost matrices R and Q will either amplify or attenuate the response to a certain error. The cost for the stack voltages can be equal for both converters in the matrix R, as shown in (3.58). The variable k_r is used to tune the control response with a value of 10^{-3} having been found to work best.

$$R = k_r \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.58}$$

The output of the control matrix K_p is a set of four terminal voltages which will generate the required currents flowing through the inductive network. To achieve the correct power flow a voltage reference for the AC voltage magnitude must be added on top of these references. This is the common-mode AC voltage and therefore the same for all four terminals (within the same phase). For this reason it can be seen intuitively that it will not induce any currents and only serves to set the AC link voltage.

Stack Voltage Commands

The final output from the current controller is a set of terminal voltages which are to be applied to the inductive network. These voltage references have to be converted into the

relevant stack voltages using (3.59) to (3.62).

$$V_{st1} = \frac{V_{d1}}{2} - U_{t1} \tag{3.59}$$

$$V_{sb1} = \frac{V_{d1}}{2} + U_{b1} \tag{3.60}$$

$$V_{st2} = \frac{V_{d2}}{2} - U_{t2} \tag{3.61}$$

$$V_{sb2} = \frac{V_{d2}}{2} + U_{b2} \tag{3.62}$$

Low Level Controller

The low level controller fulfils two roles: first, the requested stack voltage is discretised and as a result all cells are allocated a certain state (i.e., apply capacitor voltage across terminal or short circuit) which is translated into the gate signals of the individual IGBTs in the cells. Which cell is chosen to be switched into which state depends on the rank of the cell. If n cells are required to apply their capacitor's voltage at their terminals, then the top n cells in the ranking will be chosen to do so.

At the same time the cell duty has to be rotated. Whenever a cell's capacitor is switched into the conduction path, it will either be charged or discharged depending on the current direction. This discharge causes the voltage of the capacitor to fluctuate. To spread this fluctuation across all the cells within a stack relatively equally, the cells rank is rotated depending on the cells' voltages. By lowering the frequency of this ranking, the cells' voltages can be allowed to stray further way from the mean cell voltage of the stack. As a ranking can cause cells to switch states, it is associated with a certain amount of switching losses. To limit these losses, the rotation (or ranking) frequency is typically limited.

An overview of the low level controller used per cell stack, has been shown in figure 3.15. The cell voltages for a particular stack are taken as an input. These voltages are then ranked. The frequency of this is dictated by the rotational frequency, f_{rot}, which is typically expressed as a multiple of the AC frequency. A value of $8.2 \cdot f_{AC}$ has been found to work well.

At the controller's sampling frequency, the stack voltage to be generated (V_s) is discretised into an integer number of cell voltages. This output is combined with the cell ranking to determine which cells inside a stack should be switched into which state. The state and type of the cell determines the gate signals of the IGBTs.

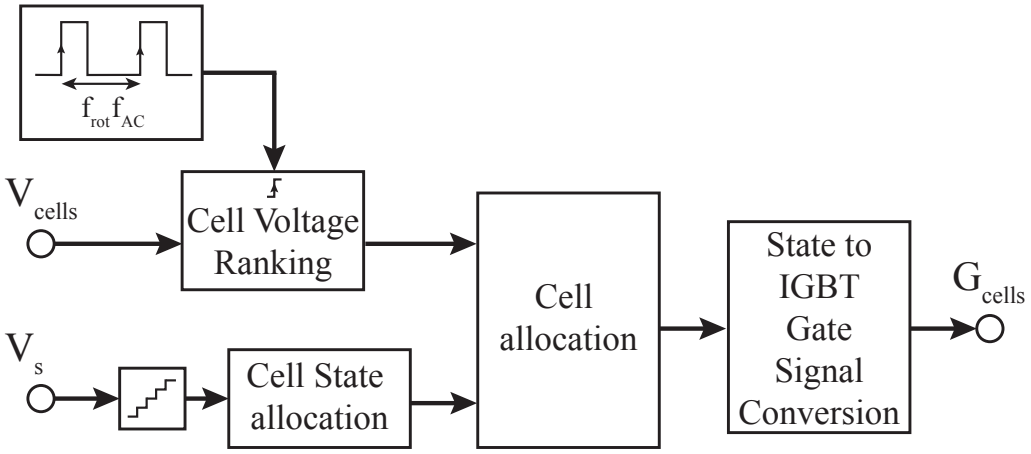

Figure 3.15: Low level controller overview.

3.3 Choice of Internal AC Operating Voltage

In the F2F topology the AC link is fully internal to the system. As such its operating AC voltage is a design choice. This section investigates the effects of an increasing AC voltage on each DC side converter and on the system as a whole. This is done for both converter types.

To facilitate the comparison between the AC voltages and the different converter types, the comparisons, where relevant, are done for a test system. This has been described in detail in table 3.2. The voltages of it have been scaled down from HVDC voltage levels to ±25 kV for the HV1 DC side and ±15 kV for the HV2 DC side. An overall step-ratio of 5:3 is modelled by the system. Reduced voltages were chosen to reduce the computational complexity of the Simulink simulation which models the system at the device level. However a large enough voltage was chosen to allow for the use of realistic cell voltages and allow for a large enough number of cells per arm to enable a smooth current control.

The cell voltage was kept at a realistic 1.8 kV, limited by the IGBT's blocking voltage (device used: Mitsubishi CM1200HA-66H). This means that fewer cells are modelled in the converters than a full scale HVDC converter would use, which has an adverse affect on the accuracy of the current tracking. As such the design criteria for the DC side filters will not be covered. As the converters were chosen in the first place for being commercially available products, their normal DC side filters are assumed to be sufficient for this application. Furthermore as both converters are multilevel converters little difference is to be expected in the DC filter design between the two.

Table 3.1: AC voltages of particular interest in test system.

$\hat{V}_{AC}$	Reason
15.0 kV	$\frac{V_{d2}}{2}$
19.1 kV	HV2 AAC sweet-spot AC voltage
25.0 kV	$\frac{V_{d1}}{2}$
31.8 kV	HV1 AAC sweet-spot AC voltage

The power transfer level was chosen to be 30 MW from the HV1 to the HV2 DC side. This implies 10 MW per phase and results in realistic current magnitudes in the arms, similar to those in a full voltage system.

Four AC voltage magnitudes in particular have been chosen for more detailed analysis (an overview is provided in table 3.1): the first two are the standard AC magnitudes at which a MMC might be operated at, i.e., the DC terminal voltage ($\frac{V_d}{2}$). As the system links to two DC links, both voltages are investigated further. The other two choices are the AC voltage magnitudes at which the energy drift of the AAC is naturally zero and the converter is said to operate at its sweet-spot.

Table 3.2: F2F direct coupled test system parameters.

System Parameter	Variable	Value
Voltage and Power ratings		
HV1 link voltage	V_{d1}	50 kV
HV2 link voltage	V_{d2}	30 kV
Power rating	P_1	30 MW
HV1 DC current	I_{d1}	600 A
HV2 DC current	I_{d2}	1000 A
MMC Converter Parameters		
Nominal cell voltage	V_c^{nom}	1800 V
Arm inductance	$L_{t,b}$	800 μH
Square-wave frequency	f_{AC}	50 Hz
Cell rotation frequency	f_{cr}	$8.2f_{AC}$ Hz
Simulation Parameters		
Simulation time step	T_s	1 μs
Controller sampling frequency	f_{cs}	50 kHz

3.3.1 Passive Component Sizing

The converters contain a large number of cell capacitors which can take up a significant fraction of the volume of each cell, as illustrated in the photograph shown in figure 3.16. The image shows a full-bridge cell manufactured by Alstom Grid[1]. The blue component is a 7 mF capacitor and can be noted to clearly dominate the device in terms of volume.

Therefore sizing the cell capacitors is important to minimise the volume the system requires. This section provides the background methodology for this and presents the analysis for the direct-coupled F2F system. Furthermore a brief comment about the arm inductors will be made.

[1]Soon to be GE.
[2]image courtesy: www.alstom.com/grid

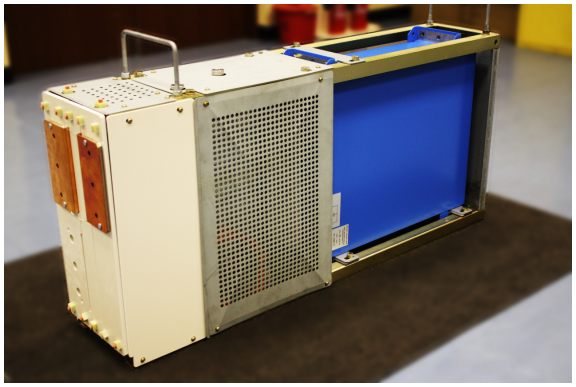

Figure 3.16: Full bridge cell manufactured by Alstom[2].

Cell Capacitors

The cell capacitors are sized to be able to handle a certain voltage ripple, or voltage deviation, every cycle. The current flowing through and the voltage generated by the stack of cells, causes the energy to deviate in the cell stack, from its nominal energy, as defined in (3.63). In the equation C_c refers to the cell capacitance, N_c to the number of cells in the stack and V_c to the nominal cell voltage.

$$E_{s0} = \frac{1}{2} C_c N_c V_c^2 \tag{3.63}$$

Assuming that the cells all experience an equal portion of the energy deviation, the basic capacitor equation linking energy and voltage, can be used to find the required cell capacitance to limit the voltage deviation. By solving the integral of the power flowing through the stack over one cycle, the intra-cycle energy profile of the stack can be found. Equation (3.64) shows the basic form of the integral. The arm currents and voltages used have been outlined in sections 3.1.1 and 3.1.2. The results can be used to find the peak absolute energy deviations away from the nominal energy, as defined in figure 3.17. The solutions to the integral over one cycle are shown in figure 3.18.

$$\Delta E_{st,sb}(t) = \int_0^{\frac{2\pi}{\omega_0}} V_{sb,st}(t) I_{t,b}(t) \mathrm{d}t \tag{3.64}$$

Graphs a) and b) show the intra cycle energy deviation for the four chosen AC voltage magnitudes and a power transfer of 30 MW (from HV1 side to HV2 side) for the F2F system utilising MMCs. Similarly graphs c) and d) show the intra cycle energy deviation for the F2F system utilising AACs and an overlap period of $\epsilon = 60°$. The results shown

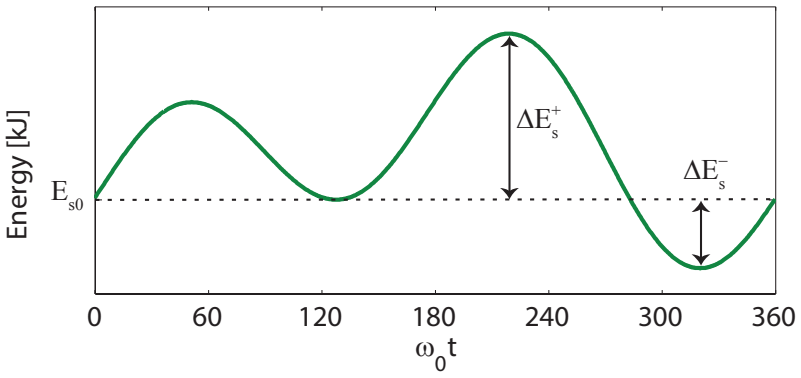

Figure 3.17: Definition of absolute energy deviations.

are all normalised such that the nominal energy level (E_{s0}) is set to zero.

The results show that as the AC voltage magnitude is increased the peak absolute energy deviation decreases for the HV1 converters (regardless of type). On the HV2 side the lowest peak absolute energy deviation is achieved at 19.1 kV. The results on both DC sides indicate that the AAC tends to have a lower peak energy deviation than the MMC for the same AC voltage magnitude.

The minimum and maximum energies of a cell stack can be defined as the sum of the nominal energy and the peak energy deviation as shown in (3.65) and (3.67). The equations introduce a measure for the voltage ripple, called the voltage deviation margin

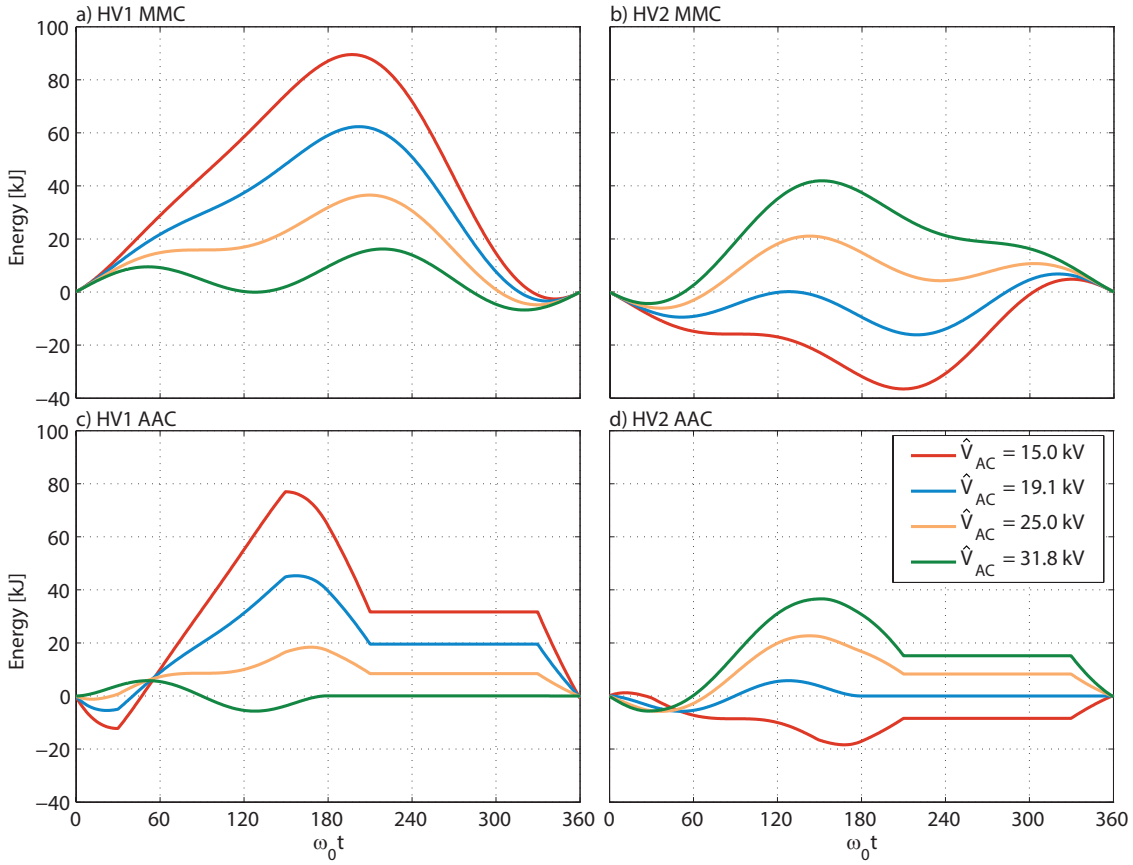

Figure 3.18: Normalised intra cycle energy deviation of top cell stack in all converter varieties over one AC cycle.

γ_c. This variable describes the voltage limits for the capacitor voltage.

$$\begin{aligned}
\hat{E}_s &= E_{s0} + \Delta E_s^+ && (3.65)\\
&= \frac{1}{2} N_c C_c \hat{V}_c^2 \\
&= \frac{1}{2} N_c C_c V_c^2 (1+\gamma_c)^2 \\
&= \underbrace{\frac{1}{2} N_c C_c V_c^2}_{=E_{s0}} + \underbrace{\frac{1}{2} N_c C_c V_c^2 \left(\gamma_c^2 + 2\gamma_c\right)}_{=\Delta E_s^+} && (3.66)\\
&: \hat{V}_c = V_c(1+\gamma_c) \\
\check{E}_s &= E_{s0} - \Delta E_s^- && (3.67)\\
&= \frac{1}{2} N_c C_c \check{V}_c^2 \\
&= \frac{1}{2} N_c C_c V_c^2 (1-\gamma_c)^2 \\
&= \underbrace{\frac{1}{2} N_c C_c V_c^2}_{=E_{s0}} - \underbrace{\frac{1}{2} N_c C_c V_c^2 \left(\gamma_c^2 - 2\gamma_c\right)}_{=\Delta E_s^-} && (3.68)\\
&: \check{V}_c = V_c(1-\gamma_c)
\end{aligned}$$

Using the equations for $\Delta E_s^{+,-}$ in (3.66) and (3.68), expressions for the cell capacitance can be found, as shown in (3.69) and (3.70). The values of $\Delta E_s^{+,-}$ can be found as explained above by using (3.64). Thus the cell capacitance can be found for a range of γ_c as shown in figure 3.19 for the HV1 MMC as way of illustration. Per voltage margin two cell capacitances can be calculated: one using ΔE_s^+ and one using ΔE_s^-. The larger of the two values is the worst case scenario and is required to keep the voltage ripple within the specified margin. Thus the results shown in figure 3.19 only show the larger value of the two.

$$\hat{C}_c = \frac{2\Delta E_s^+}{N_c V_c^2 \left(\gamma_c^2 + 2\gamma_c\right)} \tag{3.69}$$

$$\check{C}_c = \frac{2\Delta E_s^-}{N_c V_c^2 \left(\gamma_c^2 - 2\gamma_c\right)} \tag{3.70}$$

Figure 3.19 shows that for any AC voltage magnitude the cell capacitance quickly increases as the voltage margin is reduced. Depending on the magnitude of the peak energy deviation, as illustrated in graph a) in figure 3.18, the cell capacitance increases (for a fixed γ_c) as the energy deviation increases, and in this case as the AC voltage magnitude decreases.

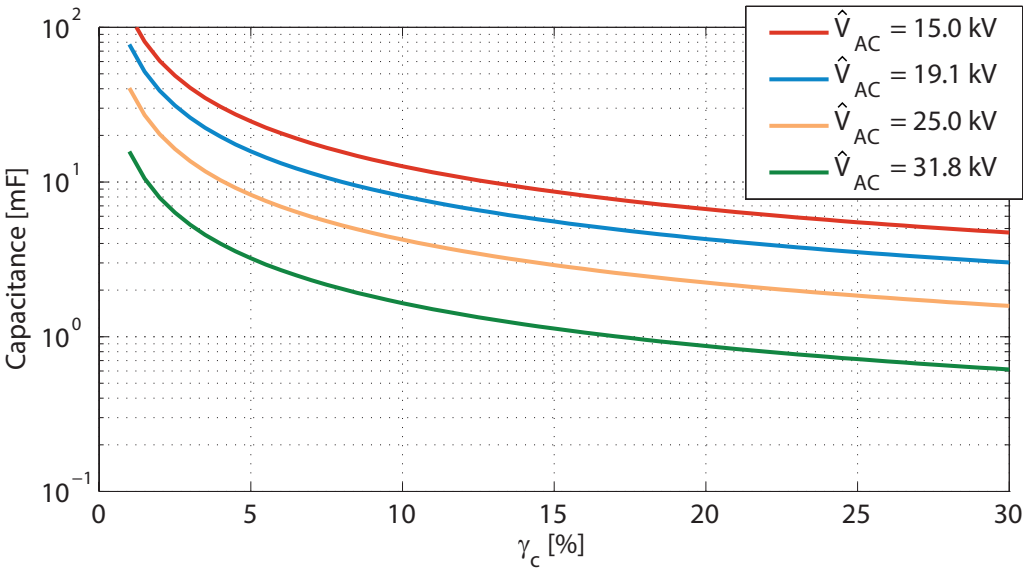

Figure 3.19: Cell capacitance with respect to voltage deviation margin γ_c for different AC voltage magnitudes for HV1 MMC.

Figures 3.20 and 3.21 show the cell capacitance for a range of AC voltage magnitudes for a fixed $\gamma_c = 15\%$, for both converter types. The results show that the cell capacitance scales differently with AC voltage between the HV1 and HV2 converter. This is to be expected, as the energy deviations (figure 3.18) scales differently also. The AACs can be noted to achieve a lower possible cell capacitance in the region of their respective AC sweet-spot voltages, compared to the MMCs. Their cell capacitance does however rise more sharply beyond these points than that of the MMCs.

For a better measure of the relative volume taken up by the cell capacitors the number of cells has to be taken into account also. Figures 3.22 and 3.23 shows the capacitance required per converter phase leg and the sum of the two for a system wide measure. The results show that the F2F system utilising MMCs has a larger minimum system capacitance of 370 mF per phase than the AAC system, with 250 mF per phase. The MMC system does however offer a wide range of AC voltages above 21 kV which provide a similar capacitance, whereas the AAC's capacitance rises quickly above an AC voltage of 29 kV but is still lower than the MMC's at 19 kV, whereafter it again rises sharply.

It should be noted that the resulting cell capacitance measures are absolute minima and assume that the energy deviation is spread equally among all the cells. As not all the cells' capacitors are always switched into the conduction path, this essentially assumes an infinite rotation frequency which is of course unrealistic. As a result the actual voltage

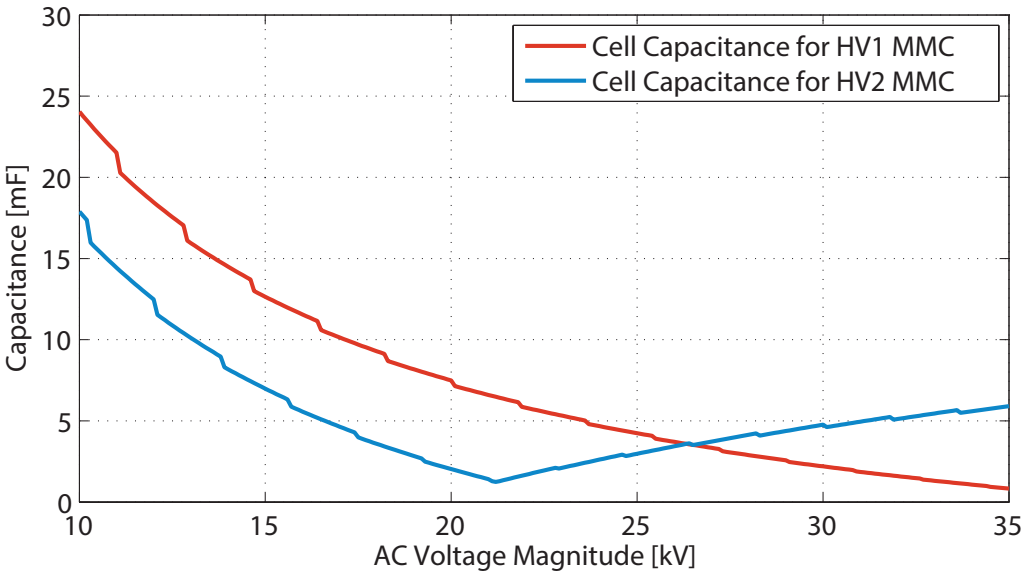

Figure 3.20: Cell capacitance with respect to AC voltage magnitudes for both MMCs and $\gamma_c = 10\%$.

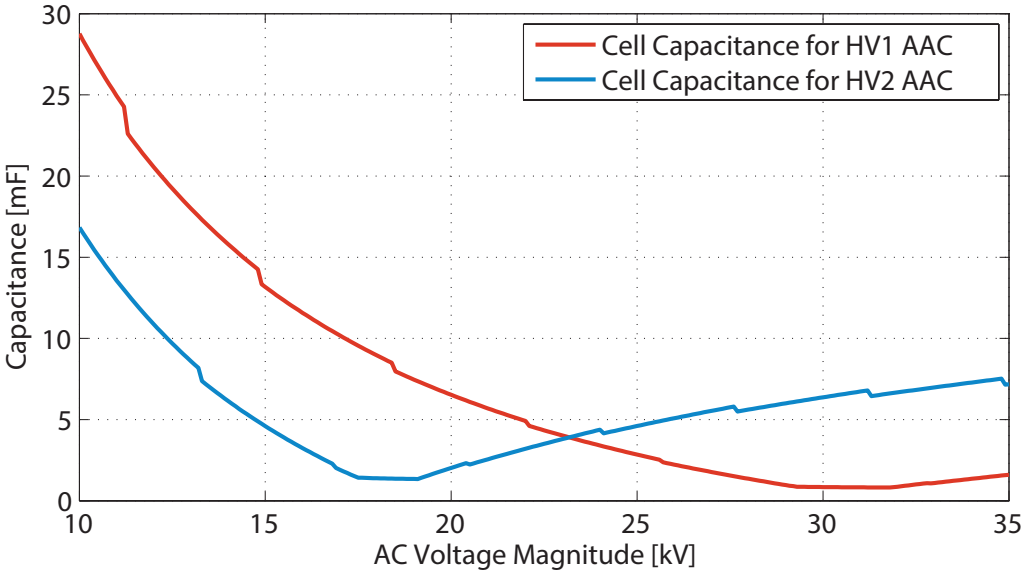

Figure 3.21: Cell capacitance with respect to AC voltage magnitudes for both AACs and $\gamma_c = 10\%$.

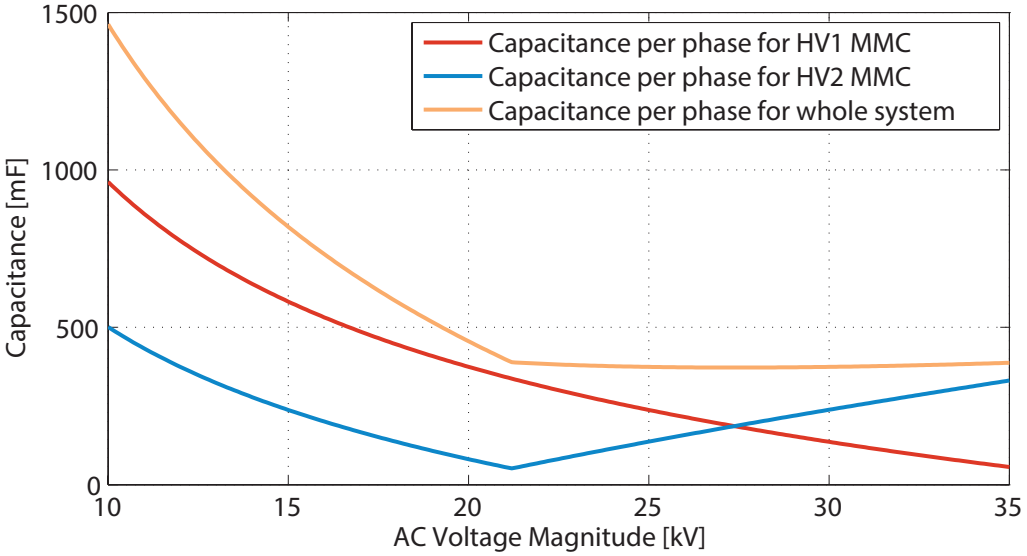

Figure 3.22: Capacitance per phase with respect to AC voltage magnitudes for both MMCs and system wide, for $\gamma_c = 10\%$.

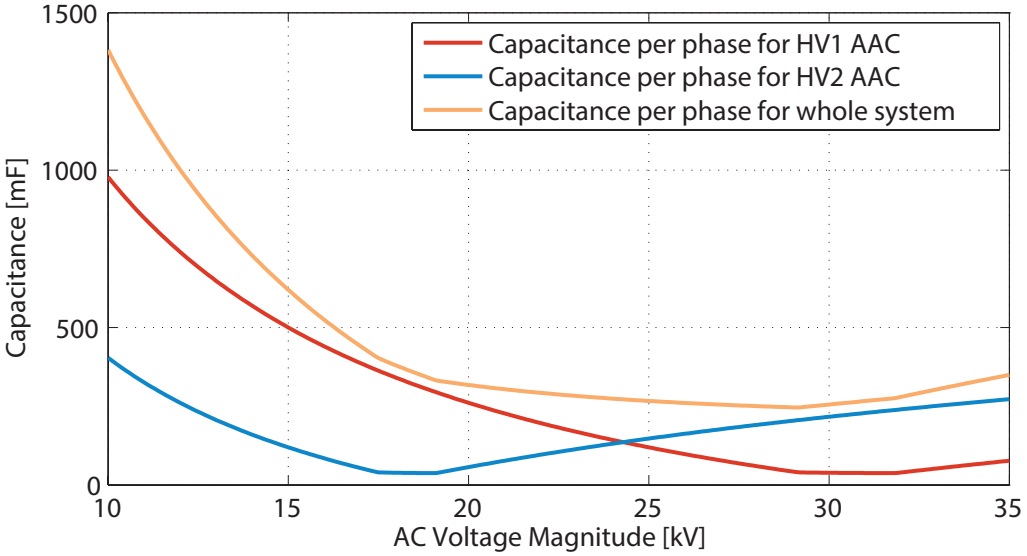

Figure 3.23: Capacitance per phase with respect to AC voltage magnitudes for both AACs and system wide, for $\gamma_c = 10\%$.

Table 3.3: Cell capacitances used in simulations for different AC voltages for $\gamma_c = 10\%$.

$\hat{V}_{AC}$ [kV]	HV1 MMC [mF]	HV2 MMC [mF]	HV1 AAC [mF]	HV2 AAC [mF]
15.0	13.2	4.6	12.7	7.0
19.1	7.4	1.4	8.1	2.8
25.0	2.9	4.6	4.3	3.0
31.8	0.9	6.6	1.7	5.3

deviation of any individual cell can be above or below the mean voltage deviation.

To test the accuracy of the voltage deviation predictions the system was simulated at different AC voltage magnitudes using the corresponding cell capacitances (found from figures 3.20 and 3.21) for $\gamma_c = 10\%$, as summarised in table 3.3. The mean cell voltage, measured from the simulation, at each of the four AC voltage magnitudes was used to find the positive and negative voltage deviation ($\Delta V_c^{+,-}$), as defined in figure 3.24, and therefore the positive and negative voltage margins. These measurements are shown in tables 3.4 and 3.5.

The results show that in most cases the voltage ripple was kept below 10%, in one instance by as much as 4.5%. The positive and negative voltage deviation measured is not the same. Thus the larger of the two is used to find the error in tables 3.6 and 3.7. On average the voltage deviations were 30 and 25% lower than expected for the MMC F2F and AAC F2F systems respectively. In the estimation smooth and ideal current and voltage waveforms are assumed. As can be seen in the next section, the stacks' voltages have a distinctive step like pattern to it due to the discrete voltage levels of the cells. This may lead to unaccounted for variations in the intra-cycle energy deviation. Furthermore any phase angle difference due to the reactive power demanded by the arm inductances has not been taken into account, as the this is expected to be small.

Since the cells cannot share the energy deviation equally due to a limited cell rotation frequency, another important factor that has not been taken into account in the cell sizing so far is the fact that individual cells' voltages will deviate above or below the mean cell voltage. This is illustrated in figure 3.25 which shows the mean cell voltage in an MMC as well as the minimum and maximum voltage any cell has at any point in time. Results are shown for two different rotating frequencies. It can be noted that at a rotating frequency of only $8.2 \cdot f_{AC}$ the minimum cell voltage can deviate significantly more from the mean. By increasing the cell rotation frequency the maximum and minimum cell voltages can be brought closer to the mean however. A higher rotational frequency will however incur

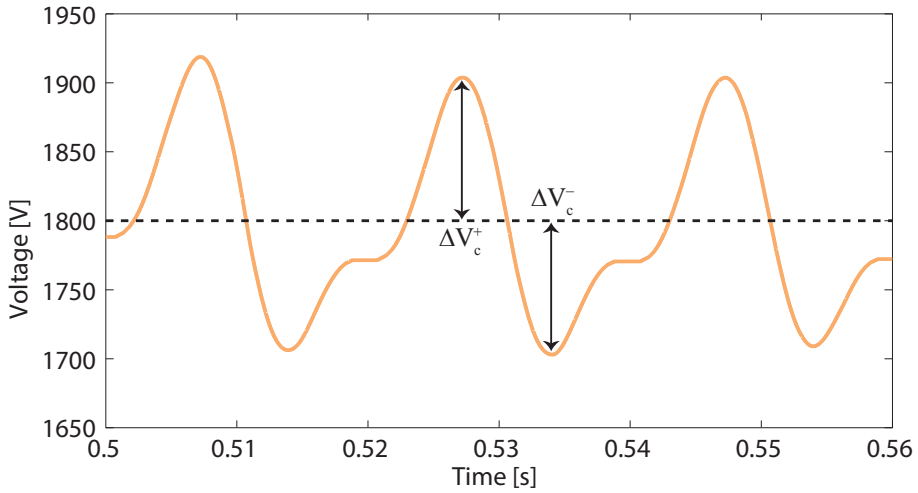

Figure 3.24: Typical cell voltage deviation from the mean.

Table 3.4: Voltage deviation of mean cell voltage for F2F using MMCs.

	HV1 MMC		HV2 MMC	
$\hat{V}_{AC}$ [kV]	γ_c^+ [%]	γ_c^- [%]	γ_c^+ [%]	γ_c^- [%]
15.0	5.5	4.5	5.1	6.0
19.1	6.0	4.8	7.1	8.0
25.0	5.2	6.9	5.7	7.8
31.8	8.1	10.1	5.4	5.8

Table 3.5: Voltage deviation of mean cell voltage for F2F using AACs.

	HV1 AAC		HV2 AAC	
$\hat{V}_{AC}$ [kV]	γ_c^+ [%]	γ_c^- [%]	γ_c^+ [%]	γ_c^- [%]
15.0	6.1	5.6	4.5	7.6
19.1	6.0	5.4	8.2	16.6
25.0	6.3	5.1	5.7	6.7
31.8	11.3	21.6	6.6	5.7

Table 3.6: Error between measured and designed for cell voltage deviation in F2F using MMCs.

	HV1 MMC		HV2 MMC	
$\hat{V}_{AC}$ [kV]	$\hat{\gamma}_c$ [%]	error [%]	$\hat{\gamma}_c$ [%]	error [%]
15.0	5.5	-45	6	-40
19.1	6.0	-40	8	-20
25.0	6.9	-31	7.8	-22
31.8	10.1	1	5.8	-42
Mean error		-30%		

Table 3.7: Error between measured and designed for cell voltage deviation in F2F using AACs.

	HV1 MMC		HV2 MMC	
$\hat{V}_{AC}$ [kV]	$\hat{\gamma}_c$ [%]	error [%]	$\hat{\gamma}_c$ [%]	error [%]
15.0	6.1	-39	7.6	-24
19.1	6.0	-40	16.6	66
25.0	6.3	-37	6.7	-33
31.8	21.6	116	6.6	-34
Mean error		-25%		

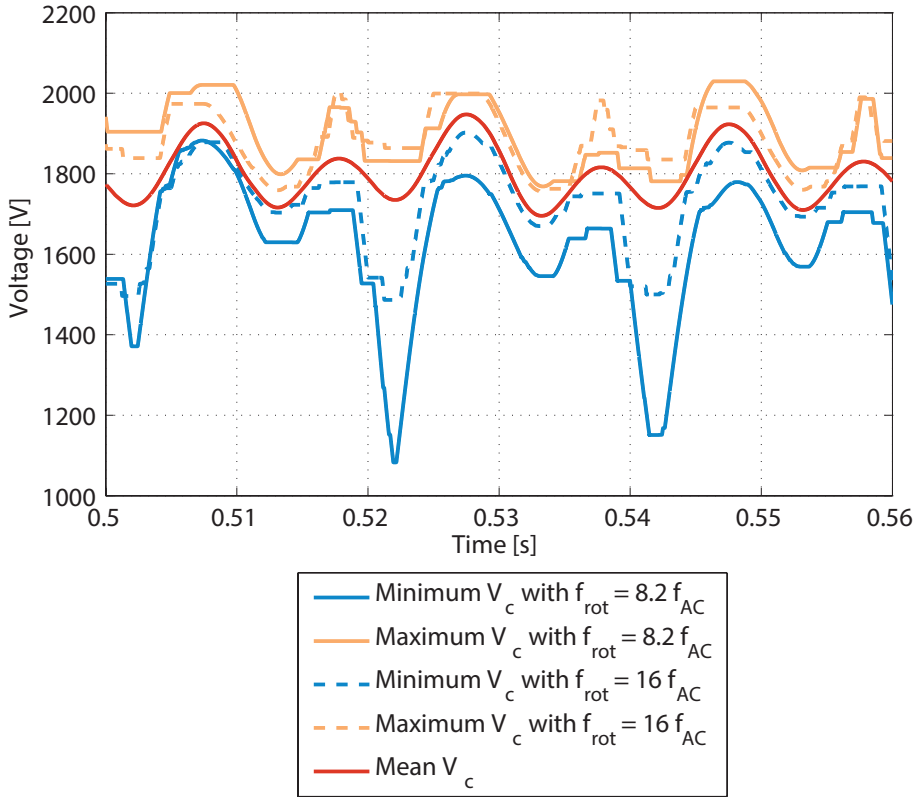

Figure 3.25: Cell voltage range for top stack in HV1 side MMC at $\hat{V}_{AC} = 31.8$ kV for different cell rotation frequencies.

higher switching losses, making its choice a trade-off between the voltage deviation, and by extension the cell capacitance, and the converter's losses.

Arm Inductors

The arm inductances in the converter are required to control the converter currents, as has been described in section 3.2.2. Typically the arm inductance in the MMC is larger than that in the AAC to aid with the control of the DC current flowing through the MMC's arms throughout the entire cycle. As the different phases amount to parallel connected voltage sources, small voltage mismatches across them can cause significant circulating currents through the arms. These are kept in check by switching additional cells in and out of the conduction path.

Thus a reduction in arm inductance causes more switching as the currents ramp more quickly. This in turn causes additional switching losses. As a DC current path exists for the entire cycle in the MMC, a larger arm inductance is typical for this converter. In the

AAC however a DC current path only exists during the overlap period. As such there exists a trade-off for the AAC, which allows a smaller arm inductance, provided slightly higher switching losses are acceptable during the overlap period. As the overlap period only lasts for a fraction of the cycle, this typically means smaller arm inductances are used than in the MMC.

Specific to the front-to-front arrangement, a smaller arm inductance in the AAC is in fact required under certain conditions. The direct-coupled system shares an AC voltage magnitude between both converters. Thus at certain AC magnitudes significant overlap balancing currents have to be run through the arms to ensure zero energy drift in the stacks, at AC voltages away from the sweet-spot. As these balancing currents are defined as square-waves they require quick current transitions. A small arm inductance helps to achieve these, particularly if the balancing current magnitude is relatively large. Throughout the analysis the arm inductance has been kept constant for each converter type, at 10 mH for the MMC and 2 mH for the AAC at 50 Hz.

3.3.2 System Currents

Figures 3.26 and 3.27 show the estimated system current magnitudes as the AC magnitude is increased for a system using MMCs and AACs respectively. As the AC magnitude is raised the AC current magnitude falls accordingly. In the MMC the DC current flowing through each arm is constant with respect to the AC voltage magnitude. Thus they have a significant impact on the arm current. In the AAC however the DC overlap current magnitude depends on the AC voltage magnitude. Below 20 kV they can be noted to quickly rise. Both overlap currents can however be zero if the converter is operated at the sweet-spot. As the two sweet-spots (19.1 and 31.8 kV) are far apart, both converters cannot be operated with zero balancing currents simultaneously. A trade-off AC voltage in between the two sweet-spots may be suitable as it spreads the overlap current burden between both converters.

The arm currents as as well as the corresponding stack voltages from the simulations are shown in figure 3.28 for the HV1 side MMC and in figure 3.29 for the HV2 side MMC. The arm currents can be noted to be continuous. The stack voltage has a distinctive step-like nature, due to the discrete voltage levels of the cells. Near the peaks in the HV1 MMC and near the troughs of the HV2 MMC, a slope can be noticed on the stack voltage. This is due to the cell discharging and can cause slight current waveform distortions. In a DC/AC system larger capacitors would need to be used to reduce this distortion as the harmonic content of the AC waveforms has strict limitations. As the AC link is fully

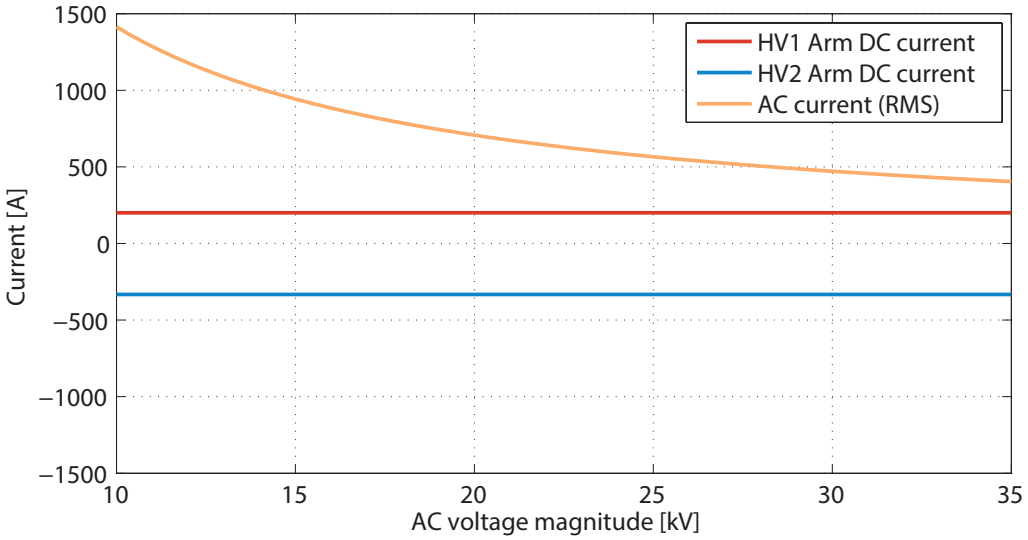

Figure 3.26: System currents in F2F system with MMCs at full power rating.

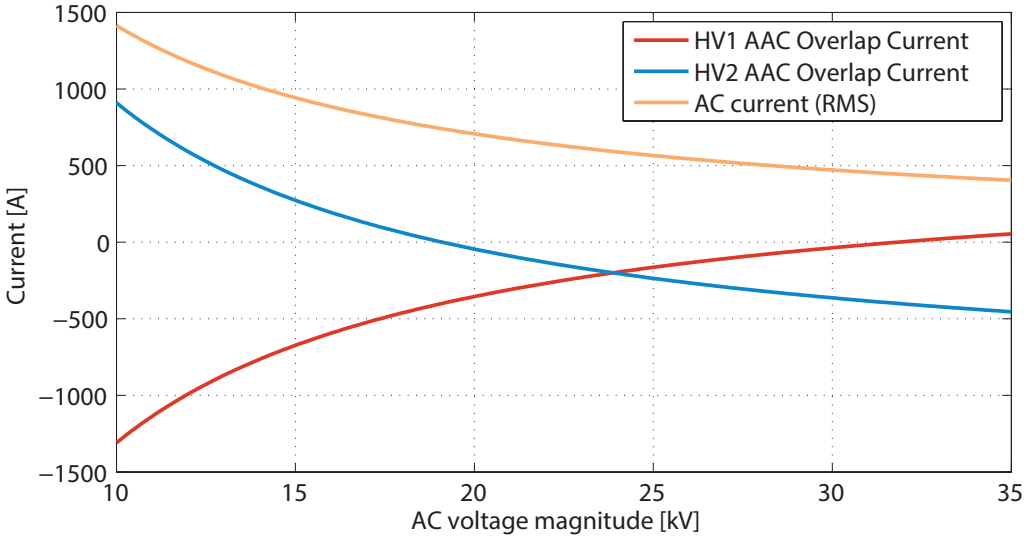

Figure 3.27: System currents in F2F system with AACs at full power rating.

internal to the F2F system however, such aspects are not as important.

The arm currents in the AACs, shown in figures 3.30 and 3.31, illustrate the discontinuous operational nature of the AAC. As the AC voltage decreases from 31.8 kV the overlap currents, needed to ensure zero energy drift, can clearly be seen to increase. When the overlap period starts and finishes, spikes can be observed in the stack voltage profile. These are the voltages that are applied across the arm inductance to ramp up the overlap current. Particularly at an AC voltage of 15 kV it can be seen that these voltage spikes require several cells. A larger arm inductance would require even more cells or limit the current's ramp rate. As supposed to the MMC, the arms can be noted to carry the full AC current, when they are in conduction.

The stack voltage can be seen to contain a plateau at the same time as the arm no longer carries any current. This is when the director switches are open and provide some voltage blocking capability to the stack. One reason for achieving a quick current ramp rate in the AAC is the opening of the director switches. The controller aims to reduce the arm current to zero before the director switches are opened to avoid hard switching them which can be very lossy. As the time the controller can wait for the arm current to be driven to zero is limited, as the cells have to generate a rising voltage in the meantime, a hard-switch may become unavoidable if the arm current is not transitioned quickly enough due to an oversized arm inductance.

3.3.3 Number of Cells in the stacks

Another important aspect of the system is the number of cells. More cells will add extra volume due to the space required for the IGBTs and their driving circuitry, particularly as the capacitance is minimised to take up less volume. The number of cells (N_c) is calculated from the peak voltage the stack has to be able to generate, as shown in (3.71). In sections 3.1.1 and 3.1.2 it has been shown that the stack voltage is a function of the AC voltage magnitude. Thus the number of cells varies with AC voltage, as illustrated in figures 3.32 and 3.33.

The number of cells required per phase leg in the MMCs can be noted to be significantly higher than for the AACs. The latter however also require director switches, the number of which has been calculated as per (3.72). Since the peak voltage the direct switches have to be able to block is a function of the AC magnitude and the overlap period, both of which are common to both converters, the same number of switches is required for both the HV1 and HV2 side AACs.

For both converter types it can be noted that the number of cells significantly increases

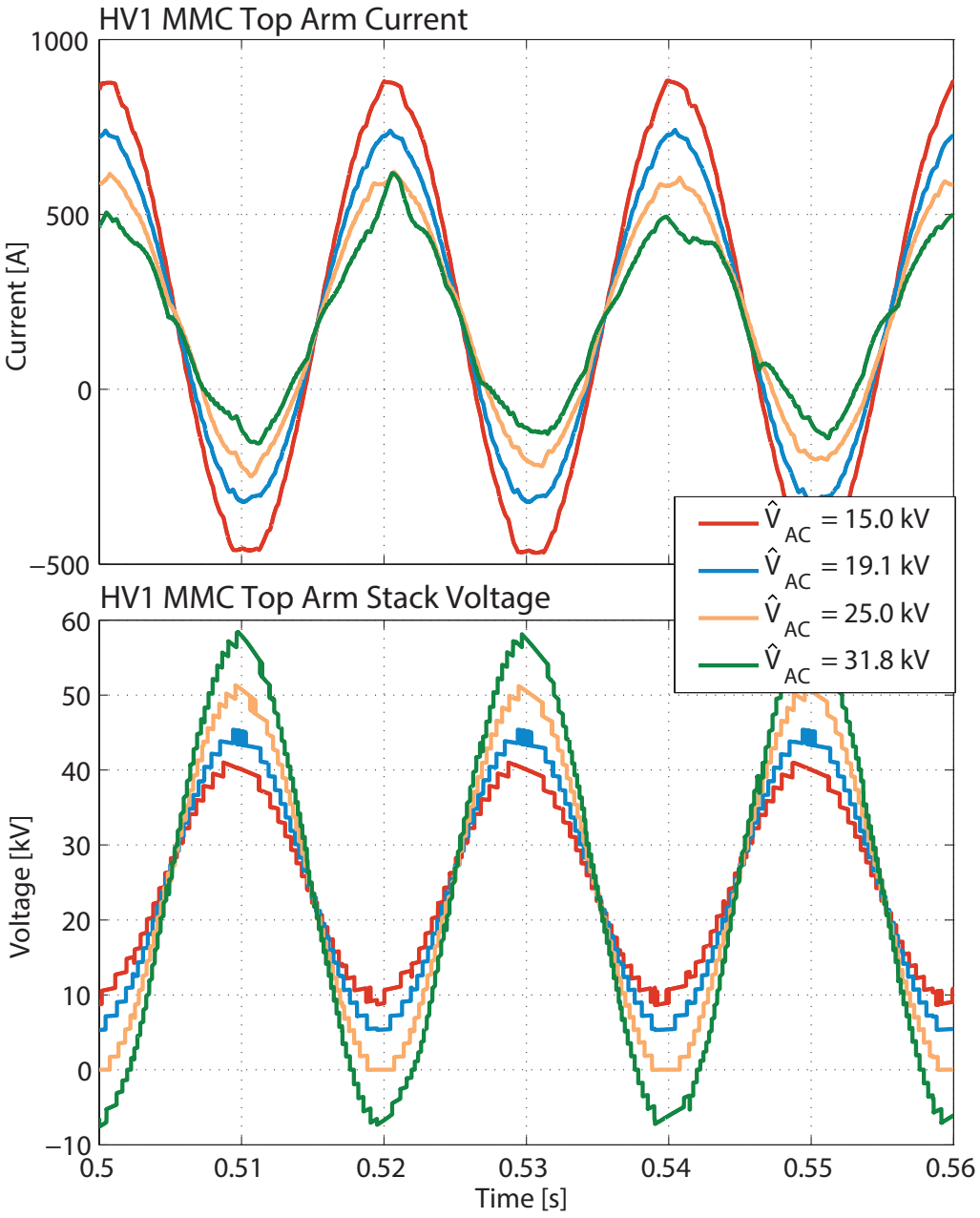

Figure 3.28: Top arm current and stack voltages of HV1 MMC for varying AC voltage magnitude.

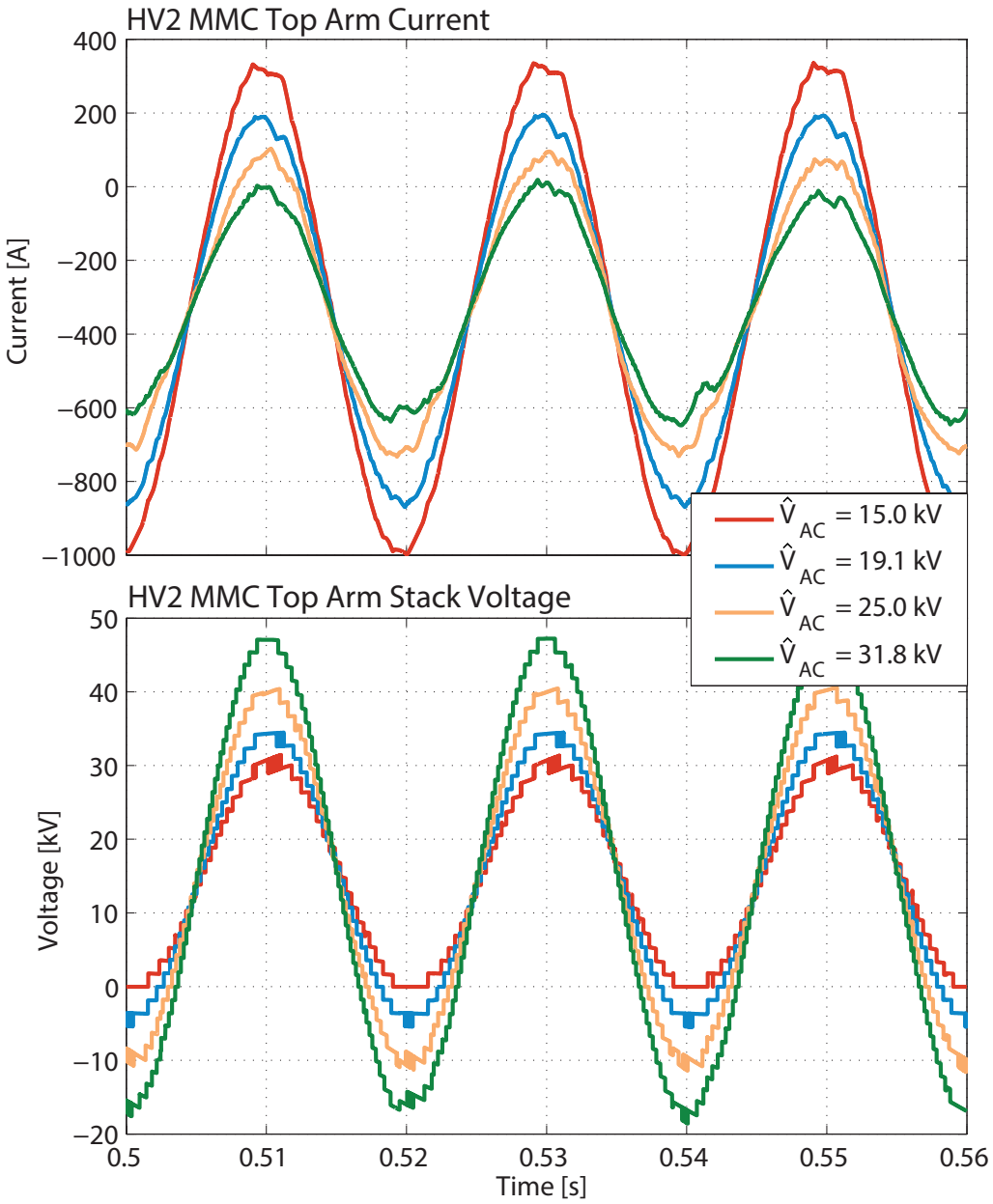

Figure 3.29: Top arm current and stack voltages of HV2 MMC for varying AC voltage magnitude.

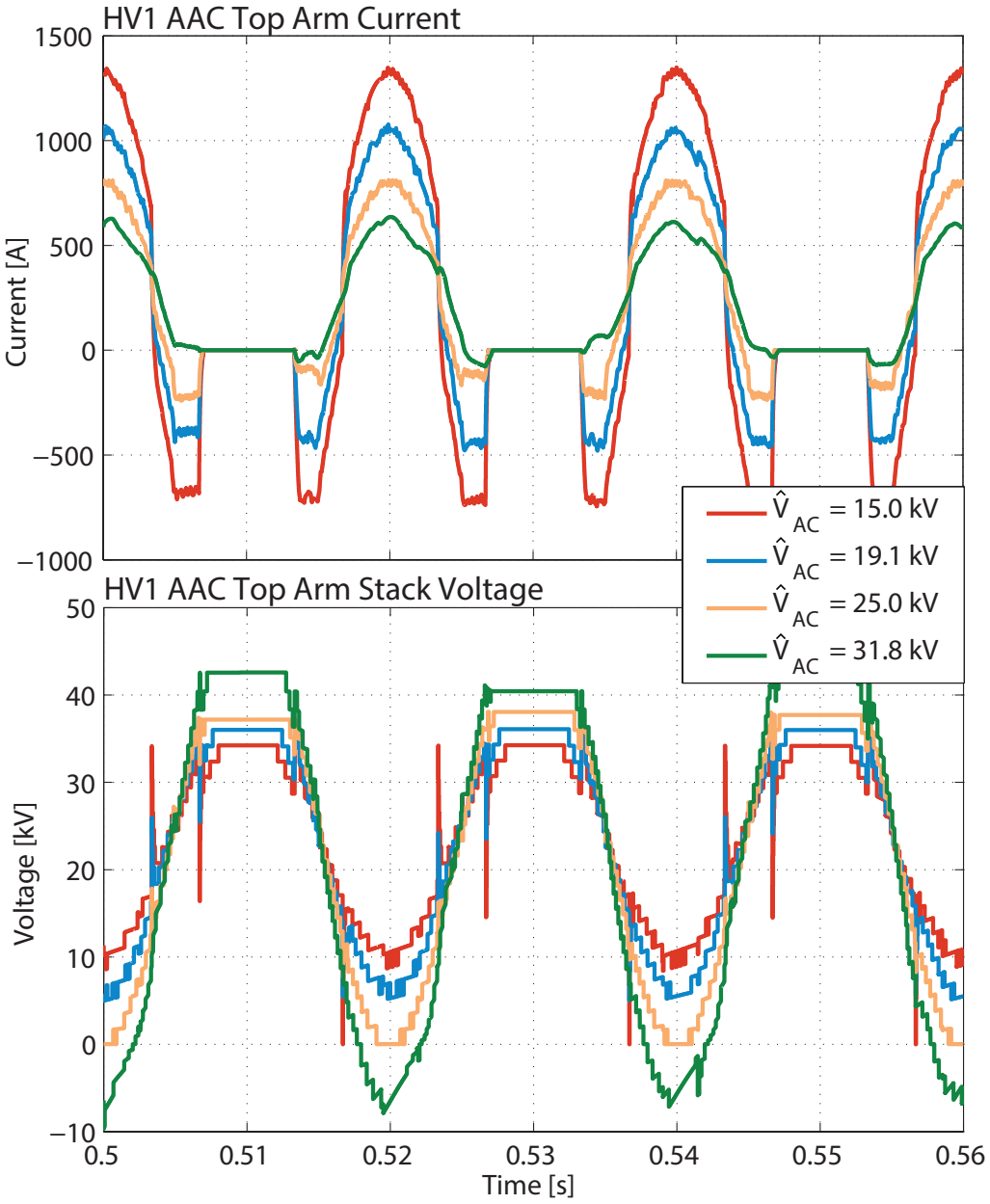

Figure 3.30: Top arm current and stack voltages of HV1 AAC for varying AC voltage magnitude.

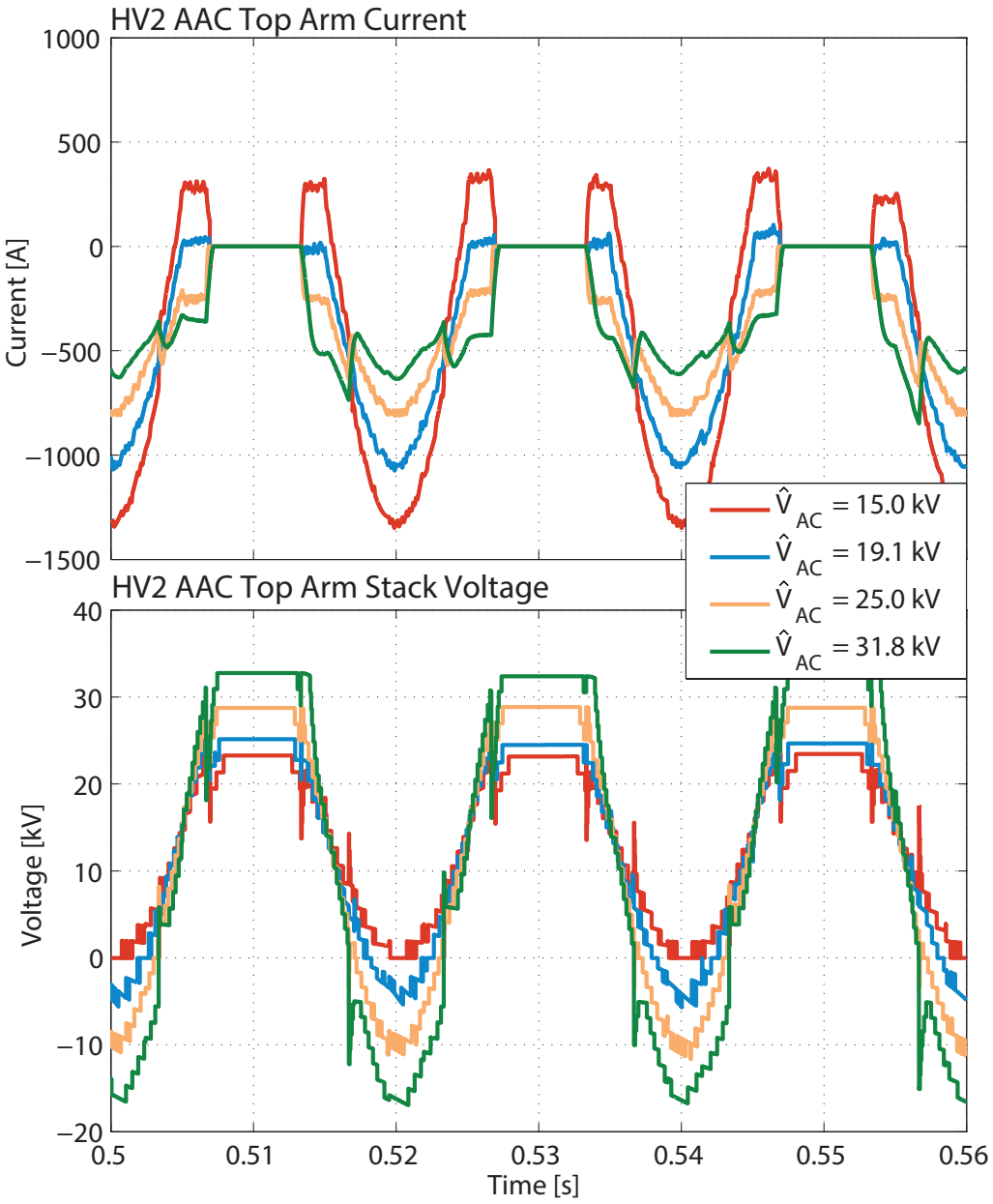

Figure 3.31: Top arm current and stack voltages of HV2 AAC for varying AC voltage magnitude.

as the AC voltage magnitude increases. An increase in the number of cells does not however require additional space. It also implies that there are more switching devices in the conduction path. As each device suffers a conduction and switching loss, a higher number of devices in the conduction path implies higher losses. The number of switching devices (including the director switches) in the conduction path, per phase, are shown in figures 3.34 and 3.35.

From the results it can be seen that the number of devices increases as the number of cells increases. There is also a prominent step-up in the number of devices for each converter at a certain AC voltage. AC voltages above this point are higher than the terminal voltage of the DC link of the associated converter (i.e., $\hat{V}_{AC} > \frac{V_d}{2}$). This means that the stacks have to over-modulate, which requires reverse voltage capability in the stacks. This in turn requires full-bridge cells. Assuming that the cell rotation and energy balancing algorithms cannot deal with mixed cell-type stacks, all of the cells have to become full-bridges. The jump in the number of devices is due to the fact that a full-bridge has two switches in the conduction path at all times, whereas a half-bridge only has one.

Comparing the sums of the number of devices in the conduction path per phase of the HV1 and HV2 side converters, it can be noted that the F2F system utilising MMCs has a higher number of devices, than the system using the AACs, for AC voltages above 15 kV. Below this voltage the MMC system has in fact fewer devices in the conduction path. This may allow the MMC F2F system to operate with lower losses at this AC voltage.

$$N_c = \left\lceil \frac{\hat{V}_{st,sb}}{V_c} \right\rceil \tag{3.71}$$

$$N_d = \left\lceil \frac{\hat{V}_{sd,sd}}{V_c} \right\rceil \tag{3.72}$$

3.3.4 Power Losses

The efficiency of any converter is hugely important. Due to the large power rating of HVDC converters, it is doubly so for HVDC applications, as every MW lost adds to the lifetime cost of the converter. To get a more accurate idea of the system efficiency, the main source of the looses has been considered here: the semiconductors. In the Simulink simulation each transistor was modelled using loss curves taken from the data-sheet for

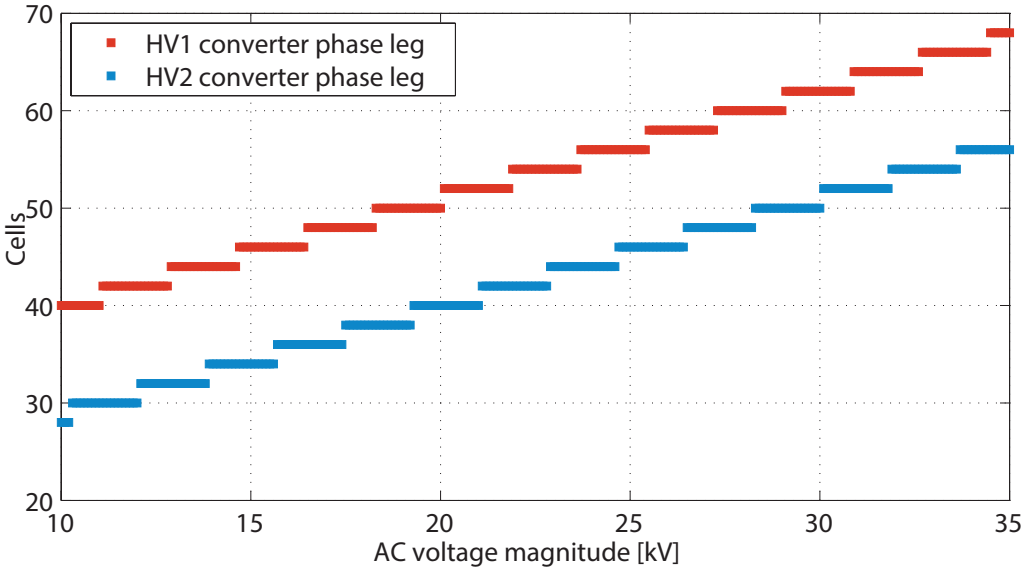

Figure 3.32: Number of cells per phase leg in MMC F2F system with respect to AC voltage magnitude.

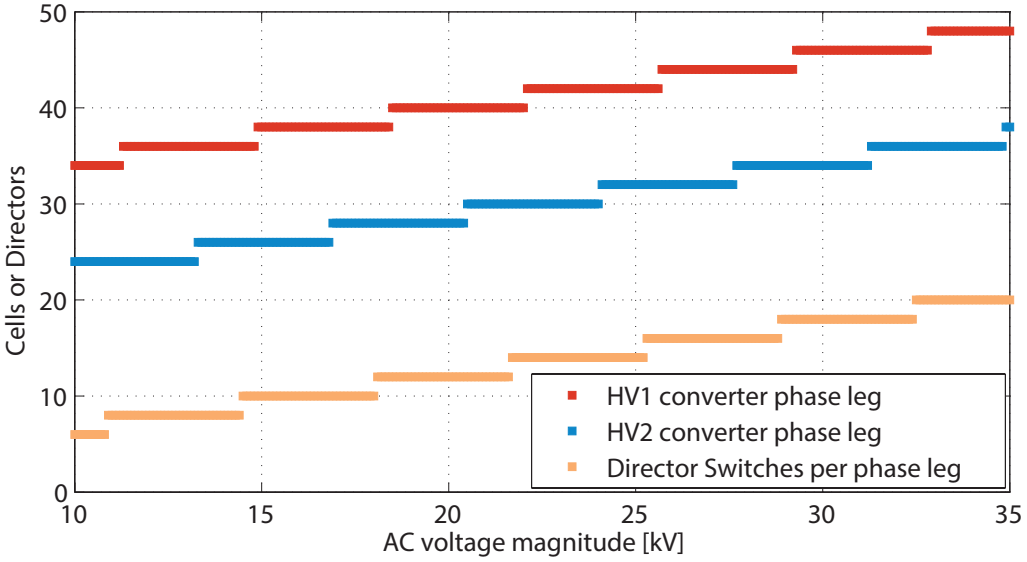

Figure 3.33: Number of cells and director switches per phase leg in AAC F2F system with respect to AC voltage magnitude.

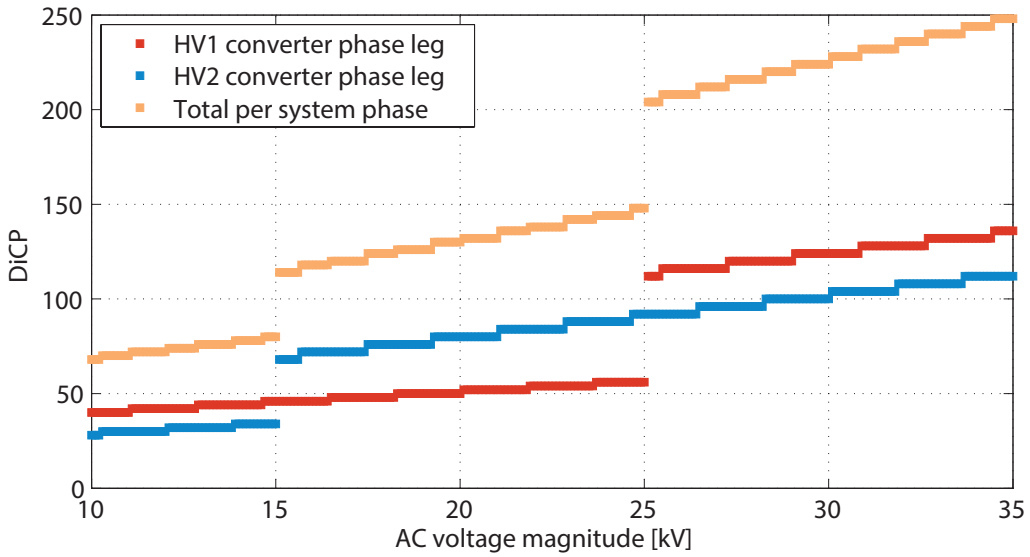

Figure 3.34: Number of devices in the conduction path (DiCP) per phase in MMC F2F system.

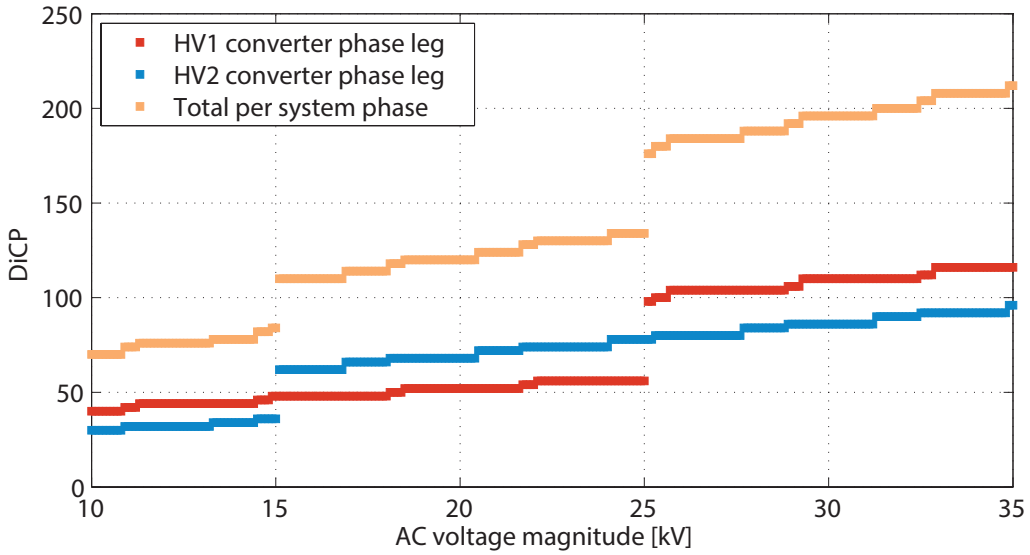

Figure 3.35: Number of devices in the conduction path (DiCP) per phase in AAC F2F system.

the conduction and switching losses and applied to the measured simulation currents and voltages. The detailed methodology of the loss modelling can be found in Appendix B.

The results for the F2F system utilising MMCs are shown in figure 3.36 for a range of AC voltages. For each AC voltage the losses incurred in each converter as well as the total of the two is shown. The results show that the least lossy AC voltage choice is 15 kV. This is the highest voltage magnitude at which both converters contain only half-bridges.

As the AC voltage is increased, the AC current magnitude falls, and therefore also the RMS current in the arms. Even though the number of cells increases with rising AC voltage, the overall losses fall due to the falling arm current magnitude. This can be observed in the losses of the HV1 MMC, which has steadily falling losses until the cells have to become full-bridges at 31.8 kV. At this point the converter's losses increase by 60% compared to the losses at 25 kV. A similar jump in losses can be seen for the HV2 converter between 15 and 19.1 kV.

For this reason it can therefore be argued that 15 kV for the AC voltage, forms the best trade-off between AC current magnitude and the number of devices in the conduction path for the MMC F2F system.

In comparison, the losses for the F2F system utilising AACs are illustrated in figure 3.37. The losses incurred in each converter can be noted to follow a similar pattern as the MMCs: they decrease as the AC current magnitude falls until the converter has to utilise full-bridge cells, which results in a notable increase. The losses in the AAC however can be seen to be significantly higher at 15 kV than those of the MMC. This is because of the difference in operation: the AAC arms experience the full AC current magnitude, as well as a significant overlap current for half the cycle. Not only are the losses a non-linear function of the current magnitude, but the F2F system also has more devices in the conduction path at 15 kV.

As well as the cell conduction and switching losses, the AAC also incurs losses in the director switches. As the currents are controlled such that the director switches are soft-switched, they incur negligible switching losses. Their conduction losses however can be seen to be significant, making up around 20% of the converter's losses.

In section 3.3.2 the arm current could be seen to be heavily affected by the overlap currents. As the AC voltage is raised, the HV1 AAC operates closer to its sweet-spot voltage resulting in a significant decrease in the overlap current magnitude. This combined with the falling AC current magnitude explains why the losses incurred in the HV1 AAC fall more quickly than those of the HV1 MMC do with rising AC voltage.

The most efficient AC voltage for the AAC F2F system is found to be at 25 kV, between the two sweet-spot voltages. Similar to the MMC F2F system, this voltage allows for the

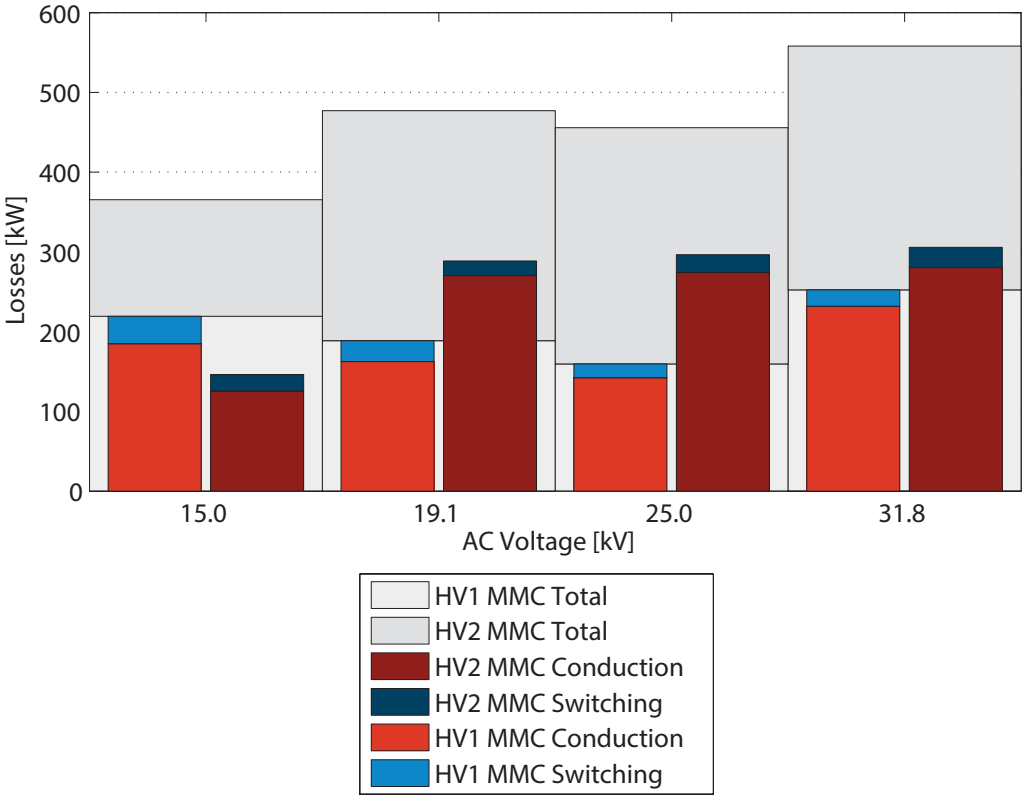

Figure 3.36: Losses in the stacks for MMC F2F system for a range of operating voltages.

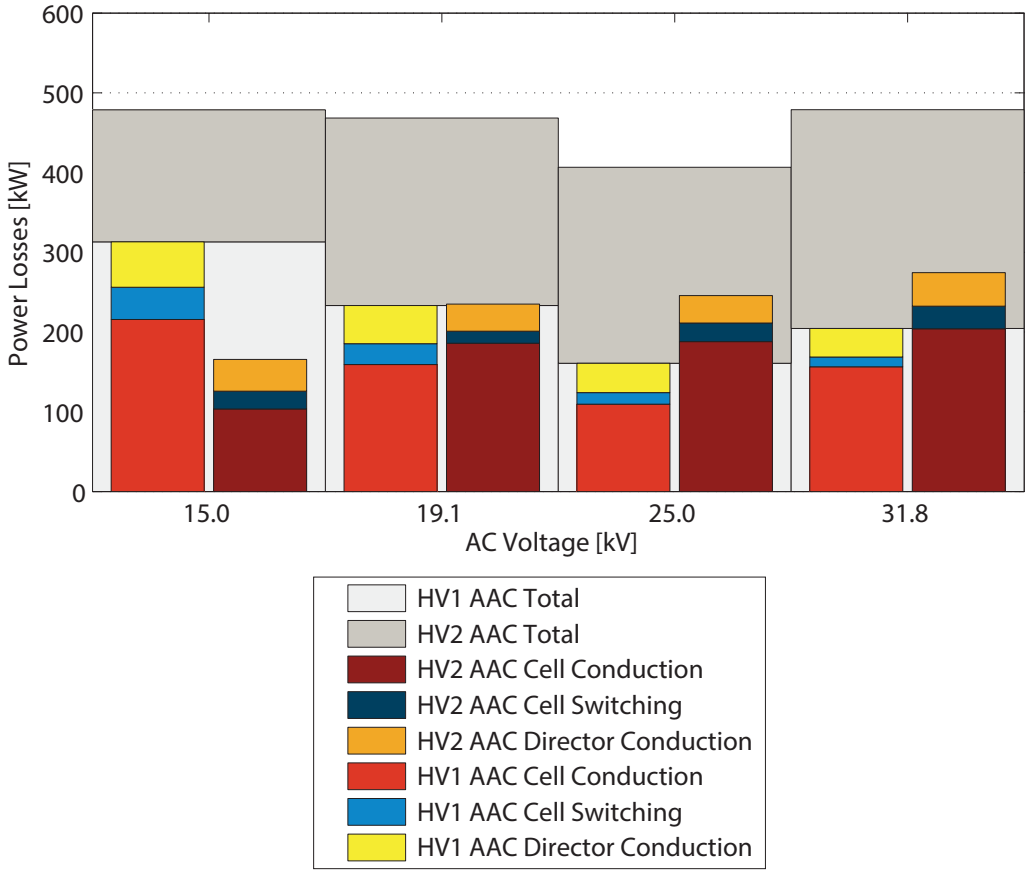

Figure 3.37: Losses in the stacks for AAC F2F system for a range of operating voltages.

best trade-off between the number of cells and the arm current magnitudes, when using AACs. The system incurs semiconductor losses of 407 kW at 25 kV compared to 365 kW at 15 kV in the MMC F2F system.

AC Sweet-Spot Voltage Operation with reduced Overlap Period

At the sweet-spot AC voltage the AACs have been shown to require only very small overlap balancing currents to rebalance minor energy drifts. This means that the overlap period can be made shorted than 60°. This implies that the stacks have a lower peak voltage and require fewer cells. At the same time more director switches are required. The effect of operating one of the converters with a reduced overlap period on the total number of devices in the conduction path is summarised in tables 3.8 and 3.9.

As the cells have to be full-bridges when the AAC operates at its sweet-spot AC voltage magnitude, reducing the number of cells per phase and replacing them with director

Table 3.8: Number of devices in HV2 AAC at an AC voltage of 19.1 kV for different overlap periods.

	HV2 AAC		HV1 AAC
	$\epsilon = 60°$	$\epsilon = 20°$	$\epsilon = 60°$
N_d per phase	12	18	12
N_c per phase	28	22	40
Cell Type	FB	FB	HB
DiCP per phase	68	62	52
DiCP per phase for whole system	120	114	

Table 3.9: Number of devices in HV1 AAC at an AC voltage of 31.8 kV for different overlap periods..

	HV1 AAC		HV2 AAC
	$\epsilon = 60°$	$\epsilon = 20°$	$\epsilon = 60°$
N_d per phase	18	30	18
N_c per phase	46	34	36
Cell Type	FB	FB	FB
DiCP per phase	110	98	90
DiCP per phase for whole system	200	188	

switches (the effect of reducing the overlap period) causes a drop in the number of switching devices in the conduction path, as can be seen from the tables. Overall a reduction of 9.5 and 9.4% in the number of devices across the F2F system can be achieved.

As the arm currents are not significantly affected by the change in overlap period, the reduction in switching devices causes a reduction in losses, as shown in figure 3.38. The system's semiconductor losses were reduced by 5.5% from 472 to 446 kW at an AC voltage magnitude of 19.1 kV and by 4.0% from 479 to 460 kW at 31.8 kV. Whilst these are significant reductions, they do not lower the system losses below the achieved best for the F2F AAC system of 407 kW at 25 kV.

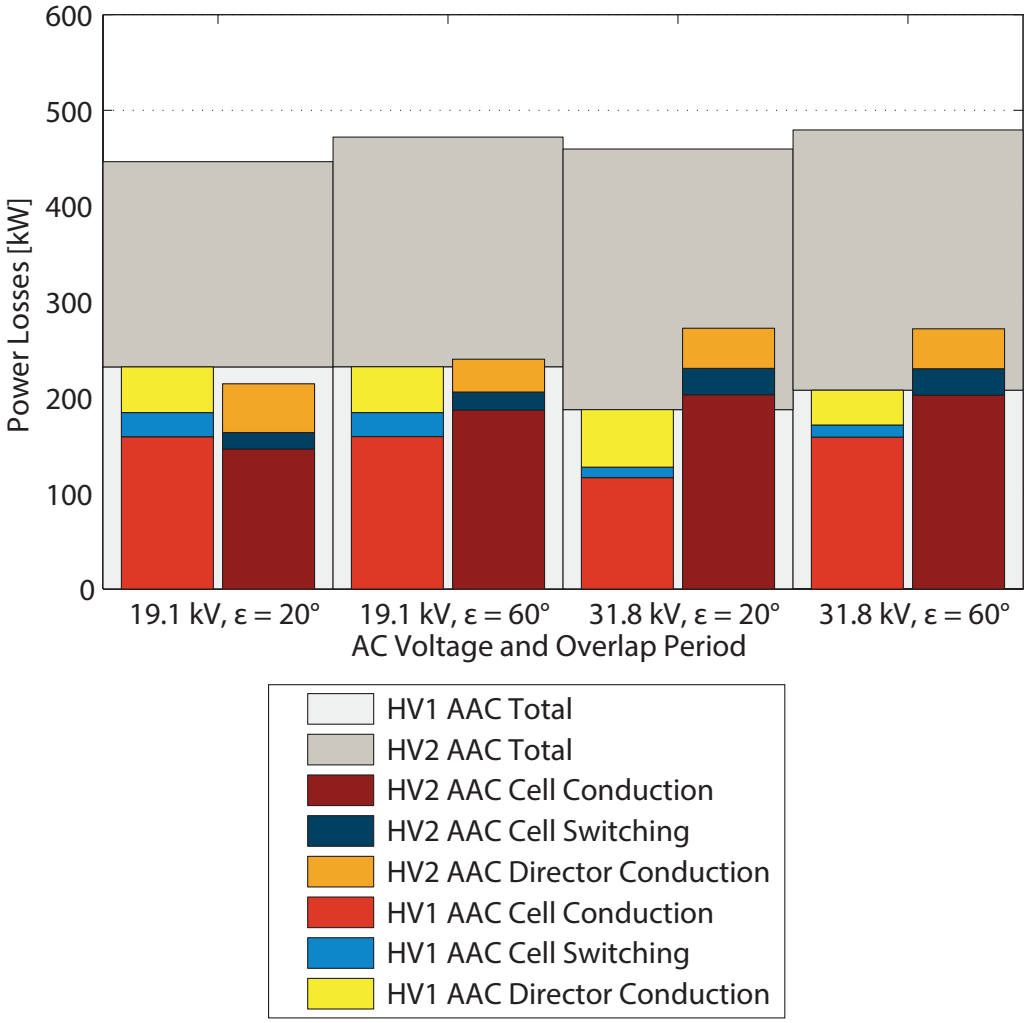

Figure 3.38: Losses in the stacks for AAC F2F system for sweet-spot operation with reduced overlap period.

Arm Inductors

As the size of the arm inductors varies significantly between the MMC and the AAC, its losses and volume have also been modelled. The inductors have all been modelled as air-cored brooks coils with a fixed current density in the turns of 1 MA m^{-2}. A detailed description of the modelling methodology used can be found in Appendix C.

Even though the current density has been kept constant, the number of turns and radius of the coil, change with an increasing AC voltage magnitude, as the cross-sectional area per turn decreases[3]. This causes the resistance of the inductance to increase, as shown in tables 3.10 and 3.11. Since the RMS arm current however drops with an increasing AC voltage and the losses scale to the square of the RMS arm current, the overall conduction losses incurred in the inductors falls with increasing AC voltage. This is shown for the MMC F2F system ($L_{t,b} = 10$ mH) in figure 3.39 and the AAC F2F system ($L_{t,b} = 2$ mH) in figure 3.40.

Although the arm inductance in the AAC is only 20% of that in the MMC, its losses, at 24.5 kW at 15 kV AC voltage magnitude, are only 63% of those in the MMC at 38.8 kW. Because the conduction losses scale to the square of the current and the AAC arm currents have a significantly higher peak value. For all AC voltages, the AAC's arm inductance losses are about half of those incurred in the MMC, making up between 3 and 10% of the converter losses. This makes them relatively insignificant.

The smaller inductance value of the AAC's arm inductances does however cause a comparative reduction in volume required fro the coils, as shown in figure 3.41. It should however be noted that the volume of the coil is likely to be insignificant compared with the insulation required for it.

3.4 Note About DC Fault Propagation Prevention

Both the MMC an AAC are capable of generating an AC wave-form in case of a DC side fault, provided that their stacks contain enough full-bridge cells. When only half-bridge cells are used this is not possible as there exists no reverse voltage capability in the stacks. In the F2F system the AC link is internal to the system and fault-management is not about maintain a clean AC wave-from but rather about preventing a DC fault on one line to affect the other.

This is still possible in the F2F system even when only half-bridge cells are used. As soon as a DC fault is detected the cells are switched into their 0V state, taking all

[3]For details please refer to Appendix C.

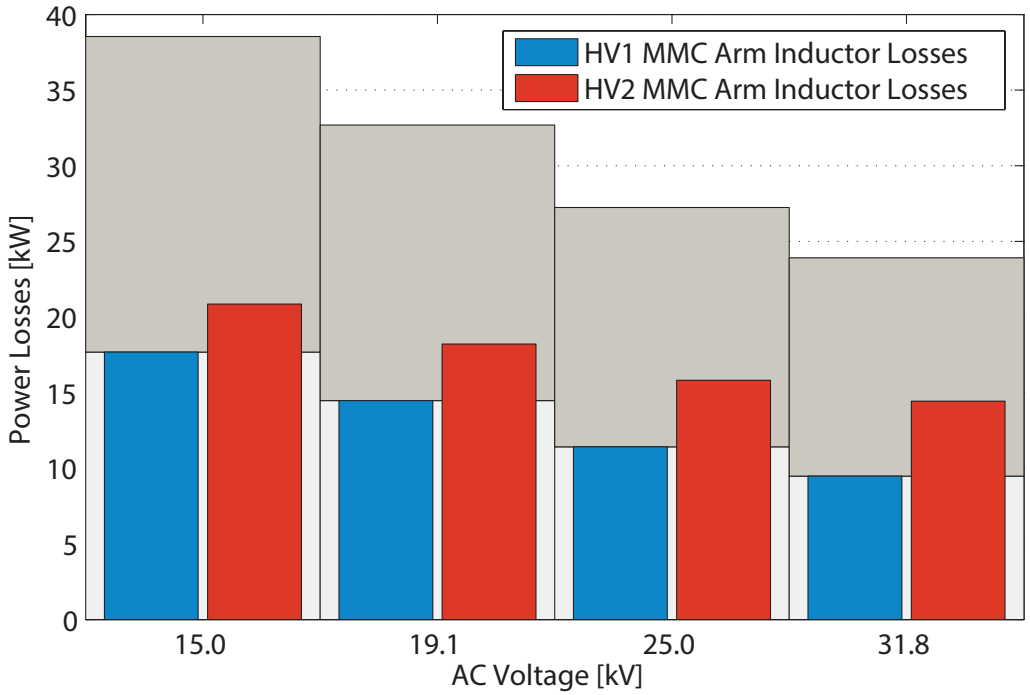

Figure 3.39: Losses incurred in the arm inductors of the MMCs for different AC voltage magnitudes.

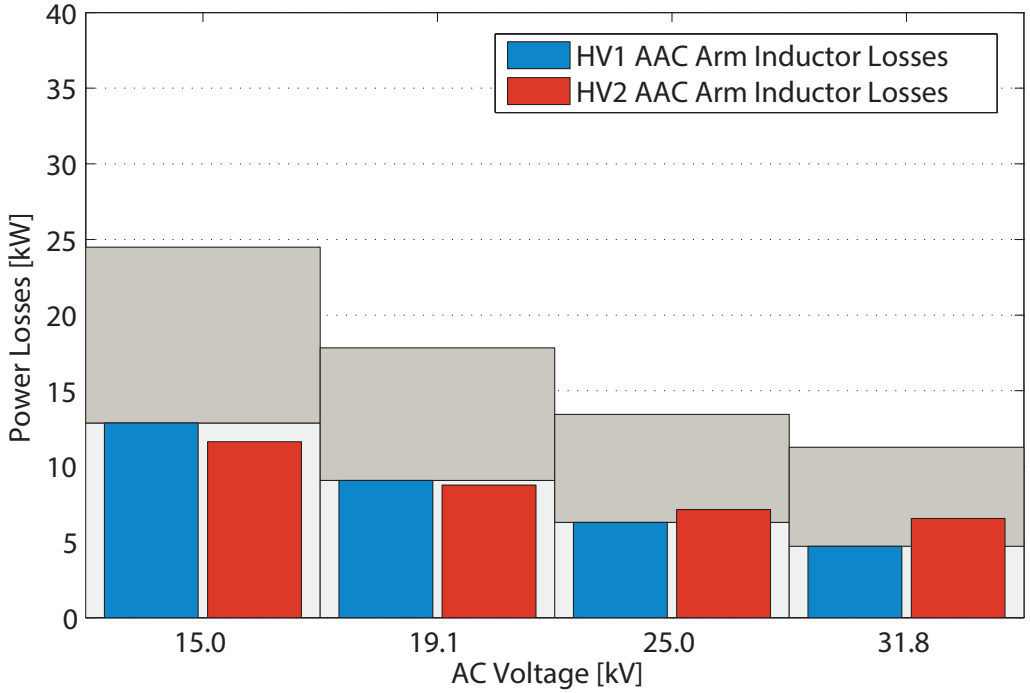

Figure 3.40: Losses incurred in the arm inductors of the AACs for different AC voltage magnitudes.

Table 3.10: Effective series resistance of arm inductors in MMCs.

$\hat{V}_{AC}$ [kV]	$R_{t,b}$ in HV1 MMC [mΩ]	$R_{t,b}$ in HV2 MMC [mΩ]
15.0	11.1	10.5
19.1	13.2	12.2
25.0	15.9	14.0
31.8	18.4	15.6

Table 3.11: Effective series resistance of arm inductors in AACs.

$\hat{V}_{AC}$ [kV]	$R_{t,b}$ in HV1 AAC [mΩ]	$R_{t,b}$ in HV2 AAC [mΩ]
15.0	10.8	11.6
19.1	13.7	14.0
25.0	17.4	16.0
31.8	21.1	17.0

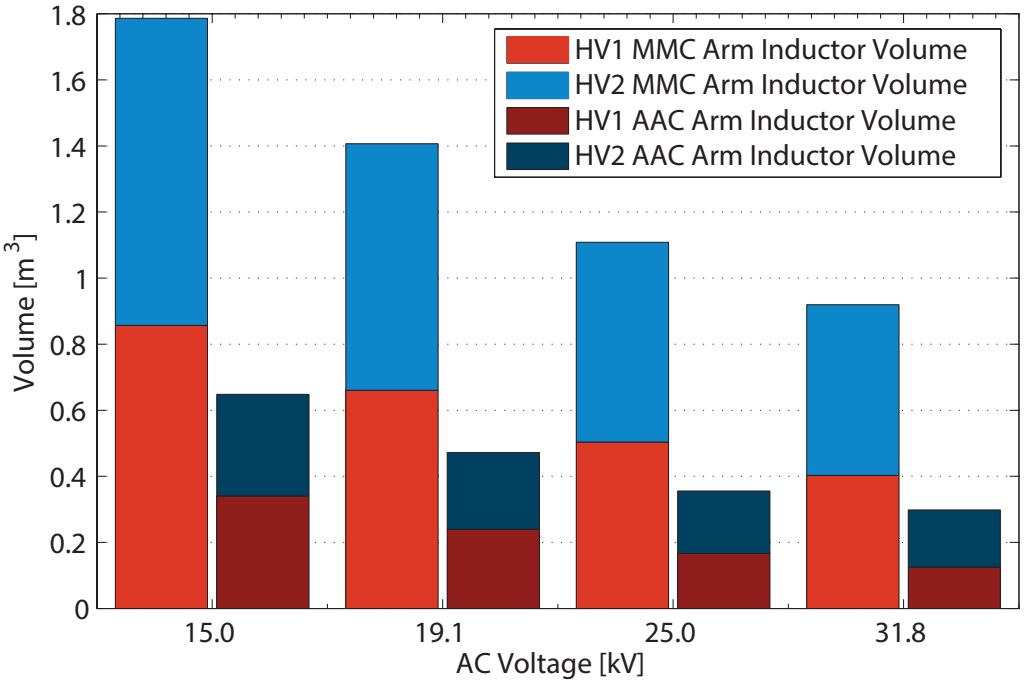

Figure 3.41: Volume of the arm inductors for both MMCs and AACs with varying AC voltage.

capacitors out of the conduction path and effectively grounding the AC link through the anti-parallel diodes in the cells. At the same time the other converter is controlled to simply generate the required DC terminal voltage across each stack and control its arm currents to zero. This will quickly induce a zero current crossing on the AC side which allows a conventional AC breaker to disconnect both AC links electrically.

3.5 Chapter Summary: Direct-coupled F2F system performance

This chapter has introduced the concept of forming a DC/DC converter through a front-to-front arrangement of two conventional DC/AC converters. Such a system using a direct-coupling on the AC side was analysed for use with two different modular VSCs: the MMC and AAC.

Due to the direct-coupling, both converters share a common AC voltage. The background to the design principles of the MMC and AAC showed that the ratio of the DC to AC voltage has a big impact on the converter design. It affects the number of devices in the conduction path, which is a proxy measure for the losses, and the capacitance required in each cell. As a large cell capacitance can significantly increase the converter's overall volume, it can be used as proxy measure for the converter's size.

Using a scaled down test system, which implements a 5:3 step-ratio, it has been demonstrated that an AC voltage cannot be chosen such that both volume and losses are minimised. Tables 3.12 and 3.13 summarise the results for both converter types and a range of voltages. It can be noted that the most efficient system utilises MMCs operated at a voltage of 15 kV, the HV2 DC terminal voltage, and operates with only 1.35% of losses. At this voltage both converter utilise half-bridge cells only. It can however also be noted that at this voltage the MMC F2F requires the largest total capacitance in its cells: 819 mF per phase.

The best AAC F2F system operates with slightly higher losses, 1.4%, at 25 kW (the HV1 terminal voltage) but requires only 267 mF in cell capacitance per phase. This set up therefore can be said to be the best trade-off which provides relatively low losses but also allows the system to operate near the minimum volume.

Table 3.12: Summary of the MMC F2F direct-coupled system performance measures.

$\hat{V}_{AC}$ [kV]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Total	$\frac{P_{loss}}{P_{transferred}}$
15.0	819 mF	*365 kW*	*39 kW*	404 kW	1.35%
19.1	510 mF	*477 kW*	*33 kW*	510 kW	1.70%
25.0	374 mF	*456 kW*	*27 kW*	483 kW	1.61%
31.8	379 mF	*558 kW*	*24 kW*	582 kW	1.94%

Table 3.13: Summary of the AAC F2F direct-coupled system performance measures.

$\hat{V}_{AC}$ [kV]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Total	$\frac{P_{loss}}{P_{transferred}}$
15.0	620 mF	*479 kW*	*25 kW*	504 kW	1.68%
19.1	332 mF	*468 kW*	*18 kW*	486 kW	1.62%
25.0	267 mF	*407 kW*	*13 kW*	420 kW	1.40%
31.8	278 mF	*479 kW*	*11 kW*	490 kW	1.63%

Chapter 4

Transformer-coupled variation of the F2F arrangement

The previous chapter introduced the direct coupled front-to-front (F2F) topology. In this two modular DC/AC converters shared a common internal AC voltage. Two modular voltage source converter types have been introduced and discussed as potential options for the F2F topology. An AC voltage which minimises the overall system wide losses or volume has been found for both converter types. It is however noteworthy, that these AC voltage magnitudes were essentially trade-offs: the losses of the individual converters were not necessarily minimised.

This is an essential limitation of the direct-coupled F2F system, which forces a common AC voltage magnitude upon both converters. By introducing a transformer into the AC link, the primary and secondary AC voltages can be chosen independently of each other to optimise for either losses or volume. The transformer will however also incur a loss and require additional space, which may mean that the overall system performance may not be improved.

A transformer also potentially allows different step-ratios to be implemented whilst the converters remain optimised for losses or volume. To be able to compare the introduction of a transformer into a F2F system, the same step-ratio as in the direct-coupled F2F has been investigated here.

This chapter investigates how the system description has changed through the introduction of the three single phase transformers into the system and how introduces the modified controller descriptions. Furthermore the implications in the converter sizing as well as the system's losses is discussed. To allow a balanced comparison with the direct-coupled F2F topology the transformer losses and volume have also been modelled.

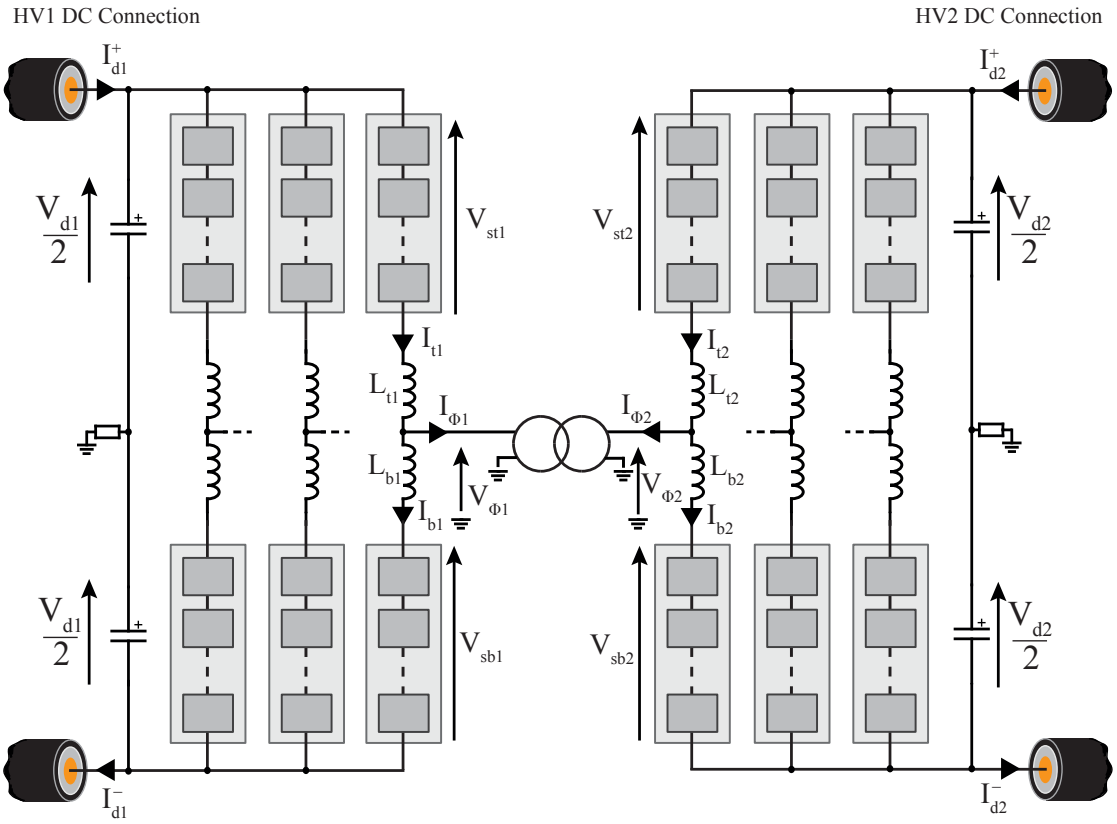

Figure 4.1: Circuit diagram of the transformer-coupled F2F topology using two VSCs.

4.1 Transformer Coupled F2F System Description

The transformer-coupled F2F topology has been investigated using the same modular VSCs as discussed in the previous chapter in sections 3.1.1 and 3.1.2. The introduction of a transformer allows the two converter voltages to be different, compared to the direct-coupled topology. Each phase has been coupled using a single phase transformer. Thus the system can still be analysed on a per-phase basis. The circuit diagram for the transformer-coupled is shown in figure 4.1 along with the notation used to describe the voltages and currents in the coupling.

4.1.1 Coupling Description

Similarly as for the direct-coupled F2F topology, the system consist of three phases, each of which phase shifted by 120° to each other. Electrically the phases are only connected to each other at the DC side. This means that the AC coupling can be described for one

phase only and be expected to be the same for the others, taking the phase shift into account.

The converter voltages $V_{\phi1,\phi2}$ form the primary and secondary voltages of the transformer. The definitions remain unchanged as per (3.35) and (3.36). Differently to the direct-coupled version however, two AC currents have to be defined, as per (4.1) and (4.2).

$$I_{\phi1} = \hat{I}_{\phi1} \sin(\omega_0 t + \alpha_1) \tag{4.1}$$

$$I_{\phi2} = \hat{I}_{\phi2} \sin(\omega_0 t + \alpha_2) \tag{4.2}$$

The transformer can be represented by an equivalent circuit as shown in figure 4.2. This model describes the transformer with an ideal mutual coupling to implement the voltage and current step-ratio, as well as leakage inductances ($L_{\ell1,\ell2}$) on either side. The primary voltage of the ideal transformer (or V_m) is generated across the magnetising inductance L_m using (4.3). Since $V_{\phi1}$ is sinusoidal, the required magnetising current can be expressed as per (4.4).

$$I_m = \frac{1}{L_m} \int V_m(t) \mathrm{d}t \tag{4.3}$$

$$I_m = -\frac{\hat{V}_{\phi1} \cos(\omega_0 t)}{\omega_0 L_m} \tag{4.4}$$

The primary and secondary voltages and currents are linked to each other through the mutual induction model as described in (4.5). The mutual inductance matrix terms are linked to the equivalent model inductances as described in (4.6) to (4.8), where the number of turns in the windings of the ideal transformer are denoted by $n_{1,2}$ [103].

$$\begin{bmatrix} V_{\phi1}(t) \\ V_{\phi2}(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \begin{bmatrix} \dot{I}_{\phi1}(t) \\ \dot{I}_{\phi2}(t) \end{bmatrix} \tag{4.5}$$

$$\begin{aligned} L_{12} &= \frac{n_2}{n_1} L_m \\ &= L_{21} \end{aligned} \tag{4.6}$$

$$L_{11} = L_{\ell1} + \frac{n_1}{n_2} L_{12} \tag{4.7}$$

$$L_{22} = L_{\ell2} + \frac{n_2}{n_1} L_{12} \tag{4.8}$$

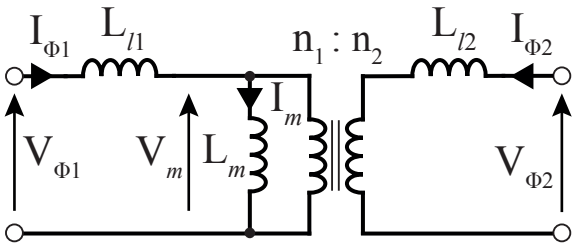

Figure 4.2: Equivalent inductance model of single phase transformer.

Ignoring any voltage drops across the leakage inductances the effective step-ratio of the transformer (n_e) can be described as per (4.9).

$$n_e = \frac{\hat{V}_{\phi 2}}{\hat{V}_{\phi 1}} \tag{4.9}$$

$$= \frac{n_2}{n_1} \tag{4.10}$$

The mutual coupling coefficient, k_t, is used to describe the leakage inductance in terms of the magnetising inductance. It can be viewed as a measure of how much flux escapes and doesn't couple with the other winding and can be expressed in terms of the mutual inductances as per (4.11).

$$k_t = \frac{L_{12}}{\sqrt{L_{11} L_{22}}} \tag{4.11}$$

4.1.2 Voltage Drop Across Leakage Inductance

It has been asserted that the voltage drop across the leakage inductance is small enough to be ignored when calculating the step-ratio required of the transformer. This section illustrates this claim by way of an example calculation.

First, the transformer's equivalent circuit can be re-defined as shown in figure 4.3, which maps the secondary side onto the primary side, such that one no longer has to consider the ideal transformer. Assuming that n_e refers to the effective step-ratio across the ideal transformer in the previous model, the referred secondary current and voltage can be expressed as per (4.12) and (4.13).

$$I'_{\phi 2} = I_{\phi 2} n_e \tag{4.12}$$

$$V'_{\phi 2} = \frac{V_{\phi 2}}{n_e} \tag{4.13}$$

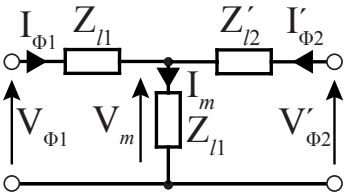

Figure 4.3: Equivalent transformer circuit with referred secondary.

The inductances in the equivalent circuit can be expressed as generic impedances. Using (4.12) and (4.13) the referred secondary leakage impedance can be expressed as per (4.14).

$$Z'_{\ell 2} = \frac{Z_{\ell 2}}{n_e^2} \tag{4.14}$$

The referred transformer equivalent circuit allows the use of standard current analysis using Kirchoff's laws to express the magnetising current using the primary and secondary currents as per (4.15).

$$I_m = I_{\phi 1} + I'_{\phi 2} \tag{4.15}$$

The transformer currents can each be expressed as a sum of its orthogonal components as shown in (4.16) to (4.18).

$$I_{\phi 1} = I_{\Re \phi 1} + jI_{\Im \phi 1} \tag{4.16}$$

$$I'_{\phi 2} = I'_{\Re \phi 2} + jI'_{\Im \phi 2} \tag{4.17}$$

$$I_m = I_{\Re m} + jI_{\Im m} \tag{4.18}$$

Similarly the transformer's impedances can be expressed as a sum of real and imaginary components as per (4.19) to (4.21).

$$Z_{\ell 1} = R_{\ell 1} + jX_{\ell 1} \tag{4.19}$$

$$Z'_{\ell 2} = R'_{\ell 2} + jX'_{\ell 2} \tag{4.20}$$

$$Z_m = R_m + jX_m \tag{4.21}$$

The primary and referred secondary voltages can thus be defined in terms of the magnetising voltage and the voltage drop across the leakage impedances as per (4.22) and

(4.23).

$$\begin{aligned} V_{\phi 1} &= V_m + U_{\ell 1} \\ &= I_m Z_m + I_{\phi 1} Z_{\phi 1} \qquad (4.22) \\ V_{\phi 2} &= V_m + U_{\ell 2} \\ &= I_m Z_m + I_{\phi 2} Z_{\phi 2} \qquad (4.23) \end{aligned}$$

To simplify these expressions a number of assumptions can be made: first, that the magnetising current is purely imaginary and negative in magnitude as per (4.4). Second, no reactive power is supplied to the transformer from the secondary side, therefore the imaginary component of the referred secondary current is zero. Third, the only reactive power, supplied from the primary side is the magnetising current component. Thus the imaginary component of the primary current is equal to the magnetising current. And finally, the active power flowing from the primary side into the transformer is equal to the active power flowing from the transformer into the secondary side. Theses assumptions are summarised in (4.24) to (4.26).

$$I_m = -jI_{\Im m} \qquad (4.24)$$

$$I_{\phi 1} = I_{\Re \phi 1} + I_m \qquad (4.25)$$

$$I'_{\phi 2} = -I_{\Re \phi 1} \qquad (4.26)$$

Assuming that the transformer's impedances are dominated by their inductive components, the expressions describing the primary and secondary voltages ((4.22) and (4.23)) can be simplified as shown in (4.27) and (4.28). The phasor diagram shown in figure 4.4 illustrates theses equations using the current definitions provided in (4.27) and (4.28).

$$V_{\phi 1} = I_{\Im m} \left(X_m + X_{\phi 1} \right) + jI_{\Re \phi 1} X_{\phi 1} \qquad (4.27)$$

$$V'_{\phi 2} = I_{\Im m} X_m - jI_{\Re \phi 1} X'_{\phi 2} \qquad (4.28)$$

The magnitude of the primary and referred secondary voltages for a given ideal step-ratio can thus be calculated as per (4.29) and (4.30).

$$|V_{\phi 1}| = \sqrt{\left(I_{\Im m} \left(X_m + X_{\phi 1} \right) \right)^2 + \left(I_{\Re \phi 1} X_{\phi 1} \right)^2} \qquad (4.29)$$

$$|V_{\phi 2}| = n_e \sqrt{\left(I_{\Im m} X_m \right)^2 + \left(I_{\Re \phi 1} X'_{\phi 2} \right)^2} \qquad (4.30)$$

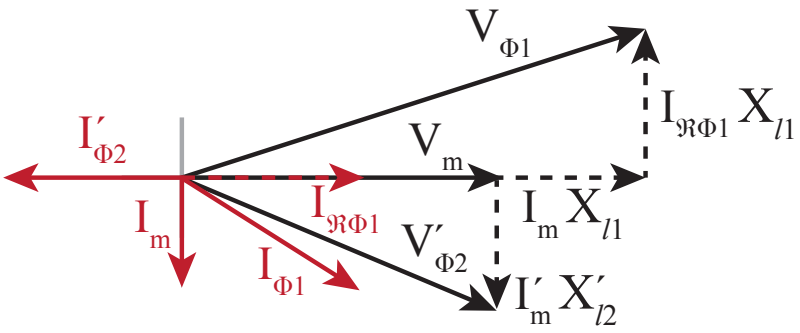

Figure 4.4: Phasor diagram illustrating transformer voltages and currents.

To illustrate the effect of the voltage drops across the leakage inductances one can use some assumed but realistic values for the transformer and its currents (using the test system as introduced in chapter three as an example): let the active power rating of the transformer be 10 MW with assumed primary and secondary voltage magnitudes of 25 and 15 kV respectively. This results in a real primary current RMS magnitude of 566 A. Further assume the magnetising current magnitude to be 5% that of the secondary current magnitude, coming to 47 A RMS in this example.

To generate a primary voltage of 25 kV at 50 Hz the magnetising inductance is thus required to be 1.19 H in size. Assuming a coupling factor of 0.995 the primary and secondary (actual, not referred) leakage inductances come to 6.0 and 2.2 mH respectively. Therefore using (4.29) and (4.30) the actual primary and secondary voltages can be found to be 25.23 and 14.93 kV respectively. Since the cells provide a resolution of 1.8 kV only, it is unlikely that the primary and secondary voltages will have an error margin that is larger than the difference between the assumed and actual transformer voltages. Furthermore it should be considered that as the coupling factor is increased the leakage inductance decreases, reducing this difference further still. Thus when sizing the step ratio for the transformer it is a reasonable simplification to use the ideal winding voltages. Additional voltage capability in the stacks is also not required as the difference in voltage is relatively small and falls within the margin of error.

4.1.3 System Controller

Due to the introduction of the transformer, the inductive network has changed, resulting in a change in the current controller. The methodology however remains the same: by applying voltages at the terminals of the inductive network, the currents flowing through it can be controlled to track certain references, as outlined in section 3.2.2.

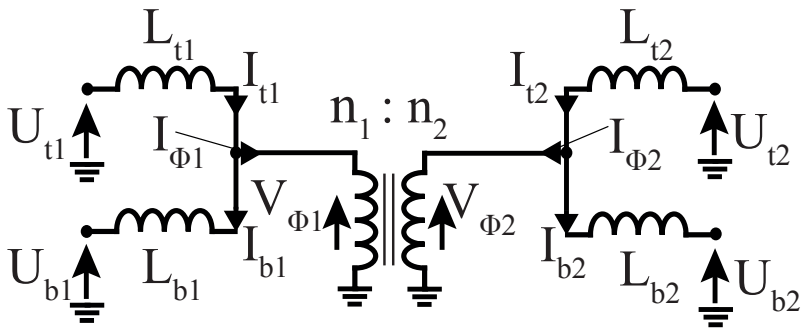

Figure 4.5: Inductive network per phase of transformer-coupled F2F system.

Not only are there extra inductive elements in the network, but also an additional current: I_m. Using the current equations in (4.12) and (4.15), the mutual inductance model of the transformer as well as considering the voltage drops across the inductors, the state-space of the inductive network in each phase can be expressed with four currents as shown in (4.31) and (4.32).

$$\begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} U_{t1} \\ U_{b1} \\ U_{t2} \\ U_{b2} \end{bmatrix} =$$

$$\begin{bmatrix} L_{t1}+L_{b1} & 0 & L_{t1} & n_e L_{t1} \\ 0 & L_{t2}+L_{b2} & 0 & L_{t2} \\ -L_{b1} & L_{b2} & L_{11}-L_{21} & L_{12}-L_{22}+n_e\left(L_{11}-L_{21}\right) \\ 0 & -L_{b2} & L_{21} & L_{22}+n_e L_{21} \\ -L_{b1} & 0 & L_{11} & L_{12}+n_e L_{11} \end{bmatrix} \begin{bmatrix} \dot{I}_{b1} \\ \dot{I}_{b2} \\ \dot{I}_m \\ \dot{I}_{\phi 2} \end{bmatrix} \tag{4.31}$$

$$\therefore M_u u = M_L \dot{x} \tag{4.32}$$

The state-space can be expressed in the standard form $\dot{x} = Ax + Bu$ as shown in (4.33).

$$\dot{x} = \underbrace{\mathbf{0}_{5,4}}_{A} x + \underbrace{\left(M_u \backslash M_L\right)}_{B} u \tag{4.33}$$

It can also be extended to include second-order filters as described in 3.2.2. The discretisation and the formation of a gain matrix using LQR theory also remains unchanged.

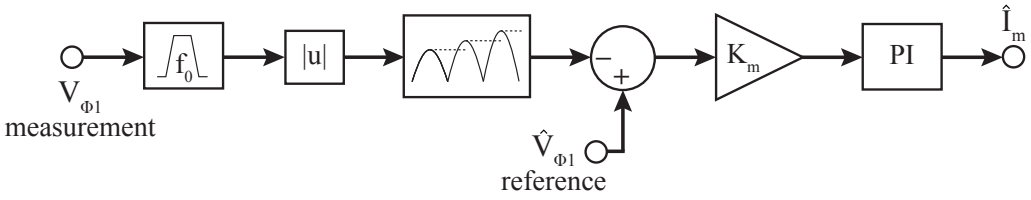

Figure 4.6: Magnetising current magnitude controller used to ensure that the correct AC voltages are generated.

As different currents are used the cost matrix Q is slightly different as shown in (4.34).

$$Q = \begin{bmatrix} q_{t1} + q_{b1} & 0 & q_{t1} & -q_{t1} \\ 0 & q_{t2} + q_{b2} & 0 & q_{t2} \\ q_{t1} & 0 & q_{t1} + q_m + q_{\phi 1} & -q_{t1} - q_{\phi 1} \\ -q_{t1} & q_{t2} & -q_{t1} - q_{\phi 1} & q_{t1} + q_{t2} + q_{\phi 1} + q_{\phi 2} \end{bmatrix} \tag{4.34}$$

In the direct-coupled system controller, the AC voltage magnitude was set using a common-mode term. In the transformer-coupled system, the equivalent to the common-mode voltage, is the voltage across the magnetising inductance (V_m). Thus by controlling the magnetising current the AC voltage magnitudes on both sides of the transformer are also controlled. This means that no common-mode signal needs to be added to the stack voltage commands. Instead an additional control block tasked to monitor the AC voltage magnitude directly, can be added to the current reference stage, which provides the magnetising current magnitude, as shown in figure 4.6.

This controller uses the primary voltage ($V_{\phi 1}$) measurement to find the magnitude of the presently generated primary voltage. An error signal is formed from this and a reference magnitude of $V_{\phi 1}$. The gain K_m, as defined in (4.35), is used to convert the voltage error signal into a current signal which is then fed into a PI controller. It can be noted that the gain K_m can also be incorporated into the PI stage.

$$K_m = \frac{1}{2\pi f_{AC} L_m} \tag{4.35}$$

The current controller for the transformer-coupled system is shown in figure 4.7. The gain matrix K_p is found using LQR theory as explained in section 3.2.2.

As the magnetising current cannot be measured directly, (4.15) can be used to find its time domain signal using measurements of the primary and secondary currents, as shown

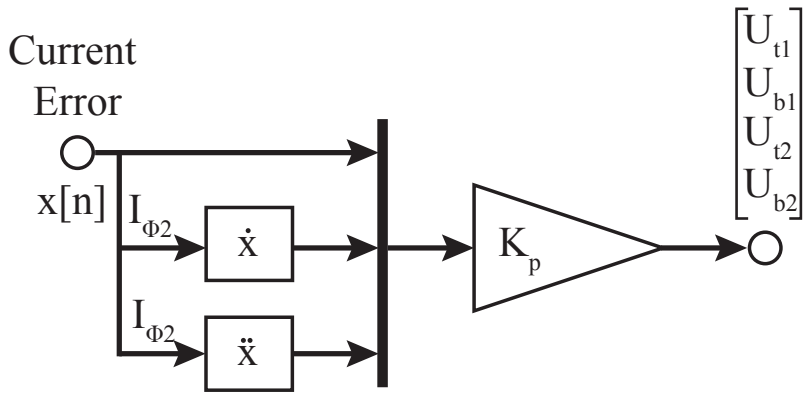

Figure 4.7: Current controller in transformer-coupled F2F system.

in (4.36).

$$I_m = I_{\phi 1} + n_e I_{\phi 2} \tag{4.36}$$

4.2 System Operation

The transformer-coupling allows the AC voltages to be set at their optimal value to minimise the losses and the volume or the converter. This section presents the converter specifications for the relevant AC voltage magnitudes and the resulting power losses. As the transformer forms an additional component to the system, its looses and volume have also been investigated.

4.2.1 Converter Specifications

The operational results from the direct-coupled system arrangement (section 3.3.4) showed that both types of converters have the lowest losses when operated with an AC voltage magnitude equal to their respective terminal voltage (i.e., 25 and 15 kV for HV1 and HV2 respectively). In so far as the capacitance required per converter is an indicator for the converter volume, these AC voltage magnitudes do not represent the best operating points to minimise the converters' volume. Figure 4.8 illustrates the capacitance required per converter phase with respect to AC voltage magnitude.

The graph shows that the AC voltages each MMC has its minimum phase capacitance, lie significantly above the respective terminal voltages at 35.3 and 21.2 kV for the HV1 and HV2 side respectively. The AACs also have a lower phase capacitance at near sweet-spot voltages (31.8 and 19.1 kV as shown in figure 3.23).

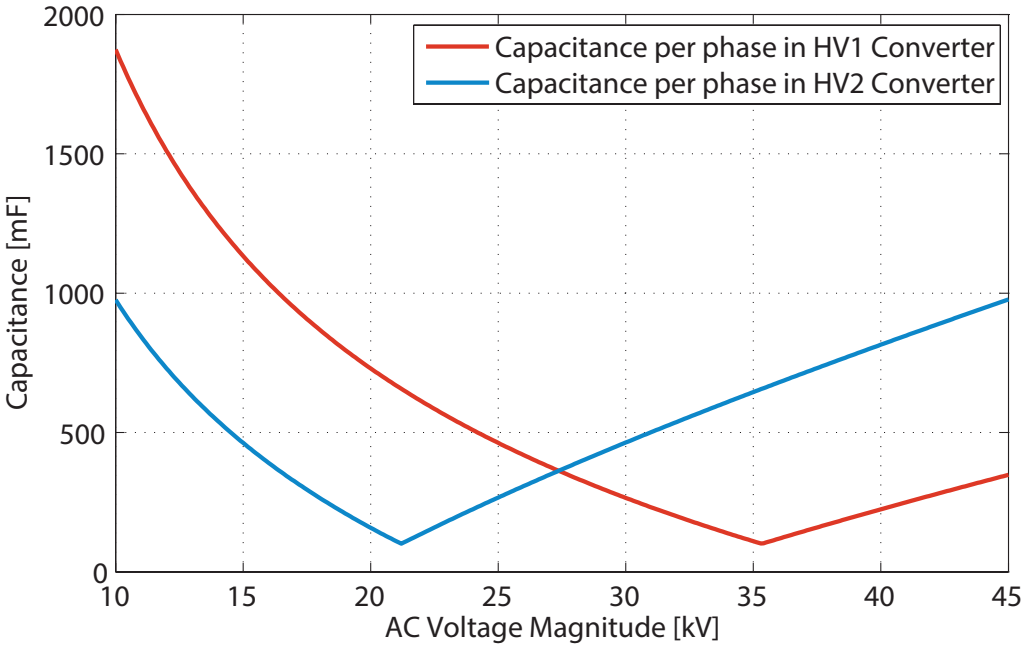

Figure 4.8: Capacitance per phase in F2F MMC system for varying AC voltage.

Depending on the AC voltage, different number of cells and cell types are used in the stacks. Table 4.1 summarises the converter specifications for the four relevant system variants: two per converter type with AC voltages either set to minimise the losses or the phase capacitance (i.e. volume).

From the data in the table it can be noted that the system wide capacitance per phase, for the MMC F2Fs, is more than four times larger for variants one and two than for three and four, which are for the AAC F2Fs. At the same time the number of devices in the conduction path, an indicator for the losses, is about half. Therefore whilst system variants two and four are expected to be smaller in volume than the other two, the losses are expected to be significantly higher. It is worth to take note of the fact that the system capacitance required in the AAC system tends to be significantly smaller than that in the MMCs F2F systems.

Table 4.1: F2F transformer-coupled system variants to minimise losses or phase capacitance.

Converter	$\hat{V}_\phi$ [kV]	C_c [mF]	N_c per phase	Cell Type	N_d per phase
Variant 1: MMCs with minimal losses					
MMC1	25.0	8.3	58	HB	-
MMC2	15.0	13.6	36	HB	-
Total number of devices in the conduction path per phase					94
System wide phase capacitance					971 mF
Variant 2: MMCs with minimal phase capacitance					
MMC1	35.3	1.6	70	FB	-
MMC2	21.2	2.5	44	FB	-
Total number of devices in the conduction path per phase					228
System wide phase capacitance					222 mF
Variant 3: AACs with minimal minimal losses					
AAC1	25.0	5.5	44	HB	16
AAC2	15.0	9.0	28	HB	10
Total number of devices in the conduction path per phase					98
System wide phase capacitance					494 mF
Variant 4: AACs with minimal phase capacitance					
AAC1	31.8	1.6	36	FB	30
AAC2	19.1	2.6	24	FB	18
Total number of devices in the conduction path per phase					168
System wide phase capacitances					120 mF

4.2.2 Power Losses

The system losses mainly consist of three components: the semiconductor losses, the transformer losses and the arm inductor losses. The latter have already been investigated in the previous chapter in section 3.3.4. Not only have they been identifier to have limited impact on the total system losses, but similar inductors are used in the transformer coupled system as in the direct-coupled system, such that these results will not be reproduced here.

As the transformer to be used is of a typical 50 Hz design for sinusoidal wave-forms, it can be expected to be highly efficient. Its losses are investigated further in the following section. It also implies that the semiconductor losses will have the biggest impact on the overall system efficiency. The losses incurred in the semiconductors in all four system variants, introduced in table 4.1, are summarised in figure 4.9.

The losses of the MMC system operated at 25:15 kV can be noted to be the lowest of all the variants presented, with a total of 361 kW. The AAC F2F system operated at the same voltages incurred slightly higher losses at 416 kW. Both the MMC and the AAC variant of the F2F system with higher AC voltages, but minimal phase capacitances, can be noted to incur significantly higher losses at 540 and 504 kW respectively.

Referring back to the converter losses in the direct-coupled system (figure 3.36), the loss-results from the transformer-coupled system can be noted to be slightly higher than the losses of the individual converters of the direct-coupled system. This is mainly due to slightly increased switching losses and the fact that an additional cell per stack was used in the transformer-coupled system, thereby incurring higher conduction losses.

The transformer-coupled system has been found to be more sensitive to cell-capacitance under voltage. The cell voltages have been shown to deviate during a cycle due to the arm currents. This effectively reduces the voltage capability at points of the cycle. Since the current control is dependent on sufficiently high voltages being applied at the terminals of the internal inductive network, these voltage deviations can cause the system to loose control over the currents.

To prevent this from happening an additional cell was inserted into each stack providing extra voltage capability, but also adding extra switching devices into the conduction path. By increasing the cell rotation frequency individual cells have in the previous chapter in section 3.3.1, been shown to exhibit less extreme voltage deviations away from the mean cell voltage across the stack. Thus the transformer-coupled systems have been simulated using a higher cell rotation frequency than the direct-coupled system, at 16 rotations per cycle. As this implies more switching events the switching losses will be slightly higher also.

Transformer Losses

In the simulation model the transformer is modelled by its mutual inductance model. To investigate the losses and estimate the volume of the transformer a separate model of a shell-type transformer has been built, as described in detail in Appendix A on page 299. This model designs the core dimensions such that the material specific flux density is not

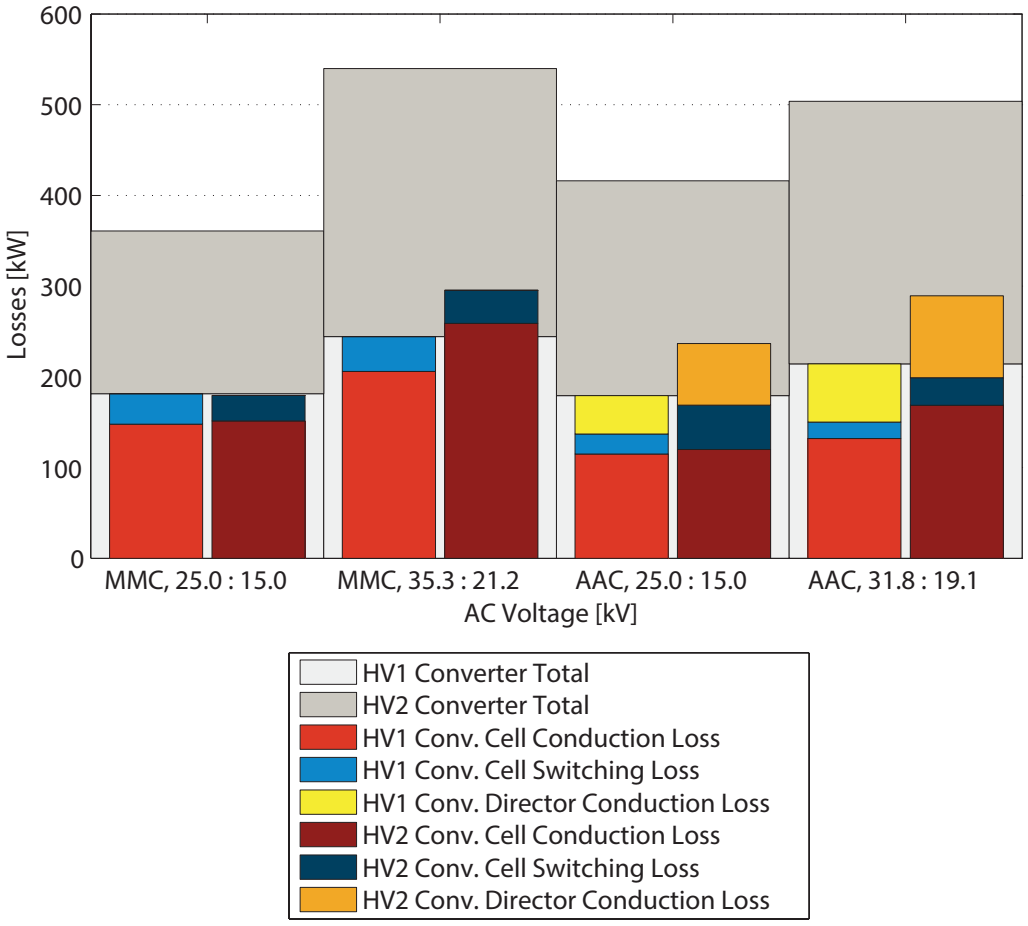

Figure 4.9: Converter losses of transformer coupled F2F system for a range of AC voltages.

exceeded and a designer set magnetising current magnitude can be used (which limits the magnetising inductance of the transformer). Furthermore, the model designs the windings such that the winding losses are minimised, using a variable number of strands of litz-wire. It should be noted that the model does not take thermal effects into account. For further details about the design algorithm and its limitations please refer to the Appendix on page 299.

A range of transformers with different winding voltages, as detailed in table 4.2, have been modelled such that the magnetising current of each was kept constant at 1% of the secondary's magnitude. The core material used is standard electrical steel. The algorithm modelling the transformer was used to sweep a range of input parameters, such as the number of turns and the height of the windings (w_h), to find the most efficient design.

From the results in table 4.2 it can be noted that the efficiency for all three winding voltage pairs, is estimated to be 99.6%, or around 40 kW. Even though the model makes a number of simplifying assumptions, this is a realistic result, as typical 50 Hz transformers have been designed to very high efficiency ratings [103]. Although the step-ratio remains unchanged, the number of turns can be seen to significantly increase as the magnitude of the winding voltages increases. This is because the secondary current's magnitude, and therefore the magnetising current magnitude, drops which requires the magnetising inductance (L_m) of the transformer to be increased. As the magnetising inductance is proportional to the square of the number of turns, this causes n_p and n_s to increase, maintaining the step-ratio.

Whilst the height of the windings also increase with increasing winding's voltage magnitude, the overall transformer volume does not significantly change. Although the number of turns increases, the winding currents drop in magnitude allowing each turn to be thinner, whilst maintaining the same current density.

The magnetising current delivers purely reactive power to the magnetising inductance. As such it will be out of phase with the current transferring active power across the internal AC link. Keeping the magnetising current small relative to this current therefore not only reduces the effects on the converter voltage, but also reduces the impact it has on the losses incurred in the switching devices of the converter supplying it. As can be seen from table 4.3, such a reduction in magnetising current causes the losses of the transformer to rise.

As the magnetising current is reduced in magnitude, the magnetising inductance of the transformer must be increased to generate the same winding voltages. As explained in (A.8), this requires the number of turns to be increased. This in turn causes higher losses in the windings as the effective winding resistance increases. Since the magnetising

current at 1% of $\hat{I}_{\phi 2}$ is already small enough to be considered to have negligible impact on the converter losses, a further reduction in magnetising current would therefore only increase the overall system losses.

Table 4.2: Transformer losses and dimensions for $\hat{I}_m = 0.01\hat{I}_{\phi 2}$.

$V_{\phi 1} : V_{\phi 2}$ [kV]	Losses [kW]	Efficiency [%]	$n_p : n_s$ [turns]	w_h [m]	Volume [m^3]
25.0 : 15.0	40.3	99.6	275:165	1.45	6.38
31.8 : 19.1	40.3	99.6	366:220	1.65	6.32
35.3 : 21.2	46.6	99.6	416:250	1.75	6.35

Table 4.3: Transformer losses and dimensions for $\hat{I}_m = 0.005\hat{I}_{\phi 2}$.

$V_{\phi 1} : V_{\phi 2}$ [kV]	Losses [kW]	Efficiency [%]	$n_p : n_s$ [turns]	w_h [m]	Volume [m^3]
25.0 : 15.0	70.3	99.3	583:350	1.85	6.40
31.8 : 19.1	70.8	99.3	741:445	1.85	6.30
35.3 : 21.2	71.0	99.3	849:510	1.95	6.71

4.3 Chapter Summary: System performance of F2F topology with galvanic isolation

In this chapter the possibility of adding a transformer into the internal Ac link of a front-to-front topology has been explored. This will not only provide galvanic isolation between the links, but also allow each converter to operate at a different AC voltage, chosen independently of the other. Doing so allows each converter to be operated with minimal losses or volume capacitance, as different AC voltages achieve this.

Tables 4.4 and 4.5 summarise the operating voltages investigated and the resulting system performance. The lowest efficiency for either the MMC F2F or the AAC F2F system can be seen to require the largest cell capacitances. Although the converter losses can be minimised by operating the system with AC voltages equal to the respective terminal DC voltages (which reduces the number of devices in the conduction path as only half-bridge cells are required), the transformers add significantly to the total system loss, making up about 20% of the total losses. Thus even the lowest losses do not beat the direct-coupled

Table 4.4: Summary of the MMC F2F transformer-coupled system performance measures.

$\hat{V}_{AC}$ [kV]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Trans.	Total	$\frac{P_{loss}}{P_{transferred}}$
25.0:15.0	971 mF	*361 kW*	*32 kW*	*121 kW*	514 kW	1.71%
35.5:21.2	222 mF	*540 kW*	*18 kW*	*140 kW*	698 kW	2.33%

Table 4.5: Summary of the AAC F2F transformer-coupled system performance measures.

$\hat{V}_{AC}$ [kV]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Trans.	Total	$\frac{P_{loss}}{P_{transferred}}$
25.0:15.0	494 mF	*416 kW*	*18 kW*	*121 kW*	555 kW	1.85%
31.8:19.1	120 mF	*504 kW*	*14 kW*	*121 kW*	638 kW	2.13%

topology variant.

The AAC F2F system does however achieve a significantly lower capacitance than all other alternatives. At 120 mF per phase it is only 45% of the lowest value of the direct-coupled variants presented (AAC F2F at 25 kV, 267 mF). This does however come at a price: this system configuration incurs 638 kW of losses, or 2.13% of the transferred power. Considering that this topology also requires transformer, which, without cooling equipment, have been estimated to require slightly over $6m^3$ of volume each, as well as the associated bushings, the volume advantage may not be as much as initially thought.

Chapter 5

High frequency operation of F2F topologies

The fact that the AC link in the front-to-front topology is fully internal to the system allows the freedom to choose its voltage magnitude. This can be used to optimise the design of the converters for losses and volume. It also potentially allows the frequency to be higher or lower than 50 Hz.

The rational for a higher operating frequency is to reduce the volume of the passive components. Particularly the cell capacitors and the transformer can be reduced in size as the frequency is raised, allowing some of the largest components to be shrunk down in size. This can potentially allow for a much more compact converter, an aspect of particular importance for offshore applications, where space comes at a premium.

The downside to an increased frequency are higher losses, particularly in the converters: the number of switching events is proportional to the frequency and each switching event is also a potential loss. As the current and voltage magnitudes remain unchanged, higher switching losses can be expected.

This argument also points to why lower than 50 Hz frequencies are of less interest and not covered in this analysis. At 50 Hz, the switching losses have been shown in previous chapters to account for only a small fraction of the total converter losses, which are dominated by the conduction losses. Whilst reducing the frequency will reduce these losses it should be noted that the increase in volume required for the passive components and the transformer makes for a poor trade-off, since a reduction in the switching losses (from 50 Hz levels) only provides a marginal improvement in efficiency.

Thus this chapter focuses on the effects of an increase in frequency on the passive components and the associated converter losses, at an increased frequency of 500 Hz. This

frequency is an order of magnitude higher than typical 50 Hz operation but not so high as to warrant a revolutionary design. A case in point here is the fact that electrical steel in transformers can be used up to about 700 Hz for transformer cores. Using the results from the previous two chapters the most efficient AC voltages for the direct- and transformer-coupled systems were chosen for investigation. Table 5.1 lists the system voltages used.

Table 5.1: AC voltages used in F2F system investigated at 500 Hz operation.

Coupling Type	VSC type	$V_{\phi 1}$	$V_{\phi 2}$
Direct	MMC	15.0 kV	15.0 kV
Direct	AAC	25.0 kV	25.0 kV
Transformer	MMC	25.0 kV	15.0 kV
Transformer	AAC	25.0 kV	15.0 kV

5.1 Effect of AC Frequency on Passive Components

The cell capacitors, arm inductors and the transformer are all affected by the AC frequency and will be briefly discussed here with regards to this aspect.

5.1.1 Arm Inductors

To maintain a fixed impedance in the arm inductors, their value should be adjusted as the frequency is changed. As the inductor's impedance is proportional to the frequency, the arm inductors have been scaled accordingly: for an increase in frequency from 50 to 500 Hz, the MMC's 10 mH become 1 mH and the AAC's 2 mH become 0.2 mH.

It is also important to consider the arm inductor size from a current control perspective: the arm currents are controlled by applying appropriate voltages at the terminals of the inductive network formed by the arm inductors. The terminal voltages set the voltage applied across the inductances to induce a change in the current. Considering the expression for the arm current in the case of the MMC, as per (3.5), and the standard VI expression for an inductance, as illustrated in (5.1), it can be noted that the voltage required across the inductance is proportional to the AC frequency. Thus if the frequency is raised and the arm inductances remained the same, a significantly larger voltage would

need to be applied at the terminals to induce the same sinusoidal currents.

$$\begin{aligned} V &= L\frac{\mathrm{d}}{\mathrm{d}t}\left(\hat{I}\sin(\omega t)\right) \\ &= L\hat{I}\omega\cos(\omega t) \end{aligned} \tag{5.1}$$

Considering a peak AC arm current of 400A, at 50 Hz with an arm inductance of 10 mH, a peak voltage of 1.26 kV is required to induce the current, which rises to 12.6 kV as the frequency is increased to 500 Hz. In this example a frequency increase to 500 Hz could be supported by the stacks, which ultimately have to generate the terminal voltages. If a higher arm inductance were used however, the stacks would soon require additional voltage capability to be able to generate the required voltages. Especially in the transformer-coupled system, care needs to be taken when sizing the arm inductors, as the leakage inductance will further add to the total inductance in the network.

In chapter two, it has been explained that using smaller arm inductors in a 50 Hz system increases the number of switching events and thereby the switching losses, as the current's rate of change has a higher limit. In essence, the system becomes more "twitchy". As the switching frequency increases as the AC frequency is raised in any case, a reduced arm inductance, scaled with a constant impedance, can be used. It should be noted that this implies a higher sampling rate of the discrete controller. In the simulations, used in this chapter, the sampling frequency was therefore raised from 50 to 500 kHz for a 500 Hz operation, to allow the systems to operate with reduced arm inductances.

In section 3.3.1 the difference in arm inductance between the MMC and the AAC has been shown to yield smaller power losses and inductor volumes for the smaller inductance, provided the design parameters were kept the same. Similarly, another argument for reducing the arm inductance as the frequency is increased, is the potential reduction in the losses and volume. It should be noted however that the impact of this on the system efficiency will be limited, as the arm inductors only contribute a small portion to the total system losses at 50 Hz already.

Using the same inductor sizing algorithm as explained in Appendix C, the inductors have been designed as air-cored Brooks coils and their losses estimated accordingly. The results are shown in figures 5.1 and 5.2 for the direct- and transformer-coupled systems respectively for operation at both 50 and 500 Hz. From the results it can be noted that reducing the inductance by a factor of 10 has caused a reduction in losses of between 73 and 76% for all system variants. The lowest losses have been estimated at 3.36 kW for the direct-coupled F2F system utilising AACs, operating at 25 kV. The main reason for the reduction in losses is the reduction in the coil's series resistance as the radius and the

number of turns is reduced.

The reduction in the number of turns also causes a significant reduction in the volume of the coil required, as illustrated in figure 5.3. The coil's volume in the direct-coupled systems has been reduced by about 62% for both VSC types. An even greater reduction has been achieved in the transformer-coupled system, where the average reduction is 74% for both converter types. The smallest volume per pair of inductors has been estimated at 0.135 m^3 for the arm inductors in the AACs, indicating a direct relationship between the inductance and the coil's volume.

5.1.2 Cell Capacitors

In section 3.3.1 the cell capacitance required for a certain voltage ripple has been shown to be proportional to the intra-cycle energy deviation. In (3.64) this in turn has been shown to be inversely proportional to frequency. It thus follows that to achieve the same voltage ripple at higher frequencies, the cell capacitance can be reduced. This effect is demonstrated in figure 5.4 which shows the voltage ripple of the mean cell voltage of the same stack in the HV2 AAC for two different frequencies and cell capacitances.

5.1.3 High Frequency Transformer

Even though 500 Hz is not a particularly high frequency compared with frequencies used in other applications where transformers are used [103], the design and losses of the transformer will be affected. Raising the AC frequency will in particular impact the size of the cross-sectional area of the core.

The transformer is typically designed to a specific flux-density (this is also the case with the algorithm used in this work and described in Appendix A). According to Faraday's law the voltage induced in a winding is proportional to the derivative of the flux passing through it, as per (5.2). Accordingly, the integral of the winding's voltage, which in the case of the transformer remains fixed, yields an expression for the flux, which in (5.3) can be noted to be inversely proportional to frequency. As shown in (5.4), a reduction in the flux due to an increase in the frequency, will therefore yield a smaller cross-sectional area (A_c) of the core, assuming the flux-density (B) remains constant.

$$v(t) = \frac{\mathrm{d}\Phi(t)}{\mathrm{d}t} \tag{5.2}$$

$$\therefore \Phi = -\frac{\hat{V}_{\phi 1}\cos(\omega_0 t)}{\omega_0} \tag{5.3}$$

$$\Phi = BA_c \tag{5.4}$$

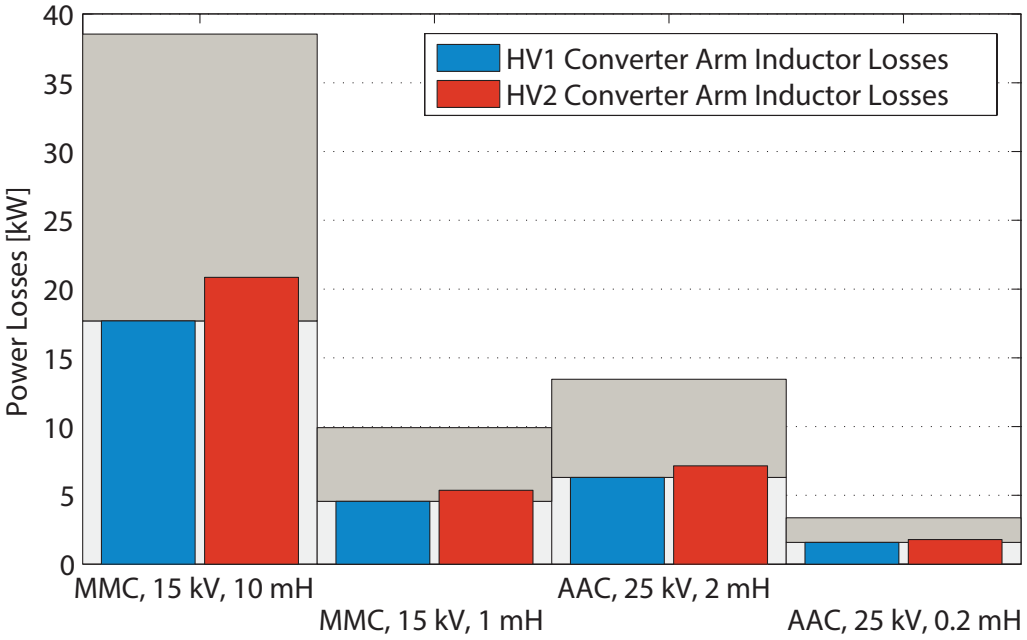

Figure 5.1: Arm inductor losses for direct-coupled F2F systems using both MMCs and AACs for 50 and 500 Hz.

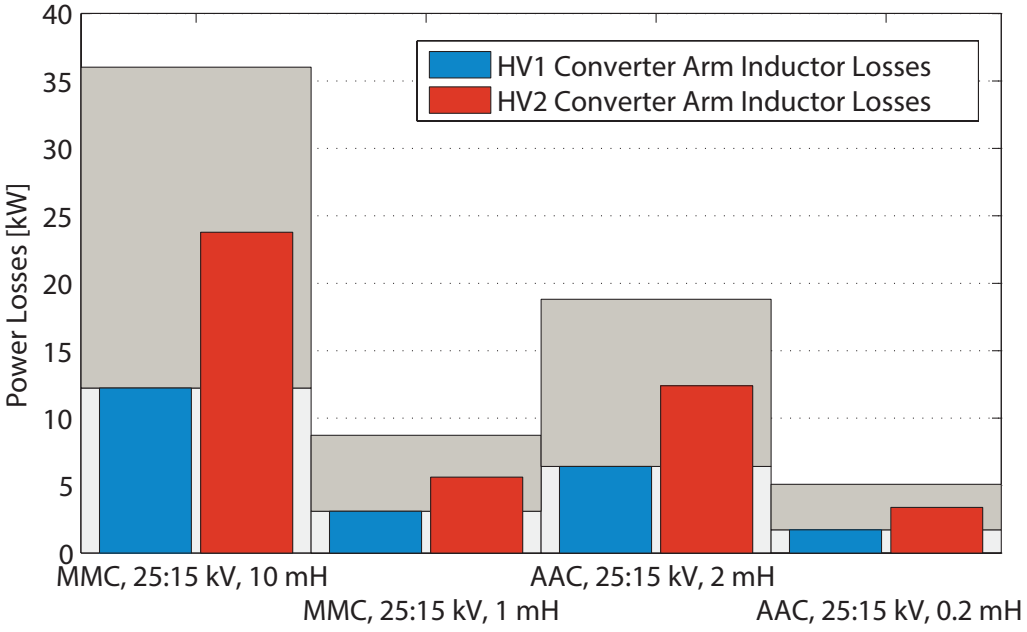

Figure 5.2: Arm inductor losses for transformer-coupled F2F systems using both MMCs and AACs for 50 and 500 Hz.

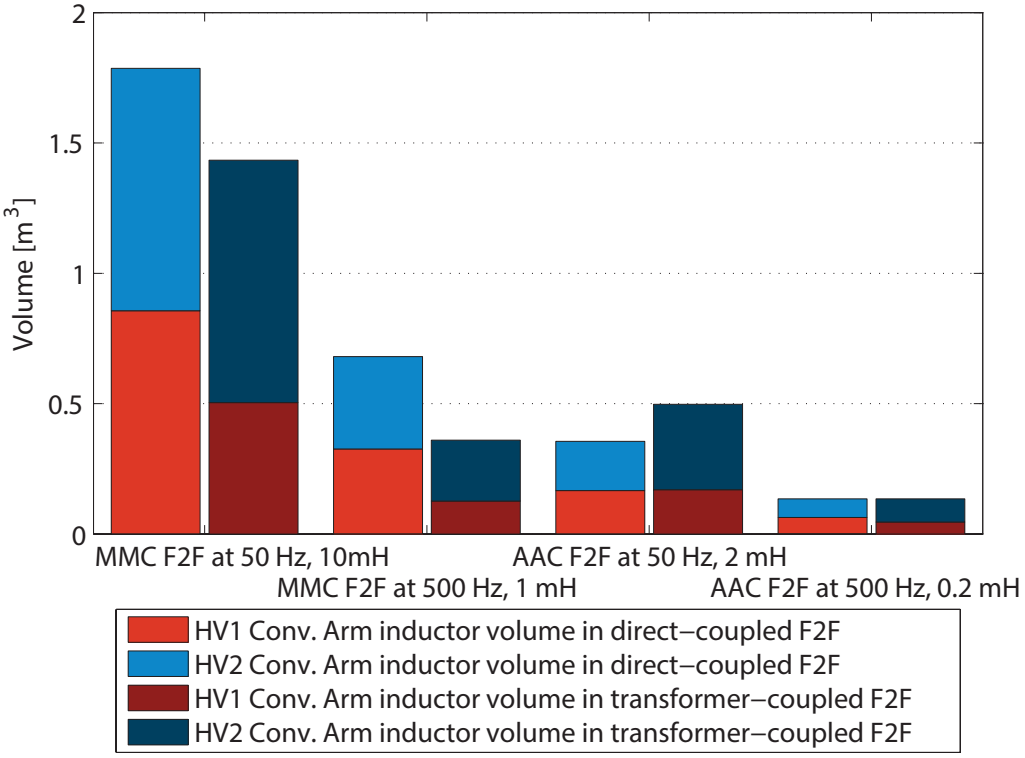

Figure 5.3: Volume per arm inductor in direct- and transformer-coupled F2F systems for 50 and 500 Hz.

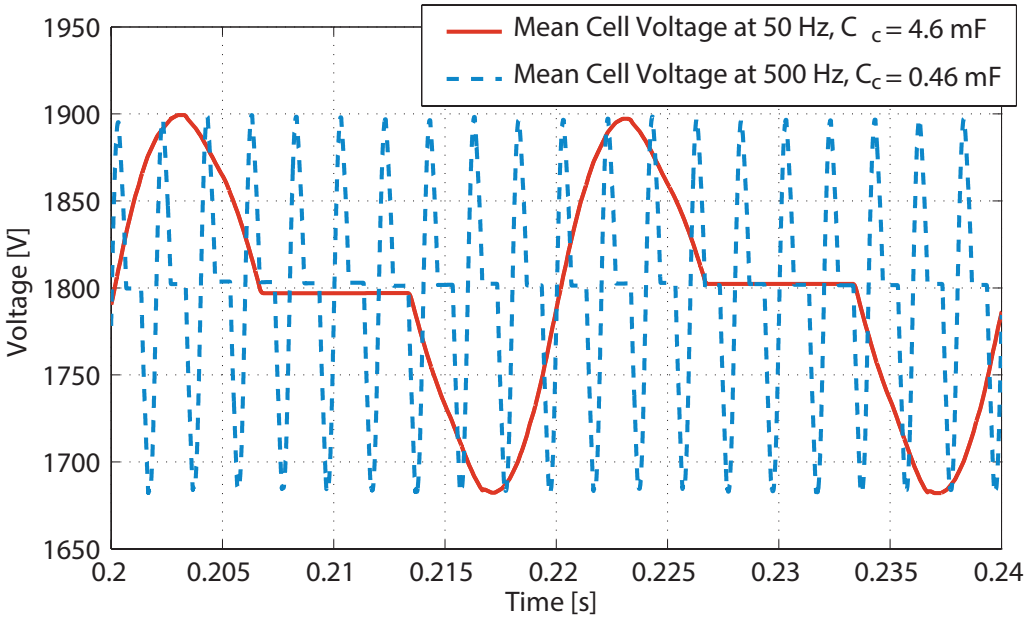

Figure 5.4: Mean cell voltage deviation in top stack of HV2 AAC in direct-coupled F2F system at 50 and 500 Hz.

According to the modified Steinmetz equation [104, 105], power losses in the core are, among others, a function of two aspects: the frequency of the flux (i.e. the AC voltage frequency) and the total mass of the core. Table 5.2 presents the design parameters and the estimated core and winding losses of two transformers, designed with different magnetising currents, for 50 and 500 Hz operation, to explore this trade-off in core losses. The results presented are the most efficient designs across a range of secondary turns (n_s) and winding heights (w_h).

For both magnetising current magnitudes it can be noted that a ten fold increase in frequency causes a four fold increase in core losses, a three fold reduction in winding losses and an about six fold reduction in volume. The reduction in winding losses is due to the reduced number of turns required to achieve the required magnetising inductance. It can be noted that for the smaller magnetising current (and therefore larger magnetising inductance) the winding losses were significantly higher then the core losses. Thus the reduction of the winding losses with an increase in frequency was greater than the increase in core losses, causing the overall transformer efficiency to increase. At 500 Hz both transformer have been estimated to incur about 50 kW of losses, which although significant, only constitutes about 10% of the converter losses.

Table 5.2: Transformer characteristics at 50 and 500 Hz using electrical steel as core material for winding voltages of 25:15 kV.

Magnetising Current constant	1%		0.5%	
AC frequency [Hz]	50	500	50	500
n_p	275	159	583	350
n_s	165	95	350	210
Volume [m^3]	6.38	1.12	6.40	1.46
w_h [m]	1.45	0.95	1.85	1.15
Core Loss [kW]	10.3	41.2	5.3	21.2
Winding Loss [kW]	30.0	10.2	64.9	26.9
Efficiency [%]	99.6	99.5	99.3	99.5

5.2 Converter Losses

The losses incurred in switching devices in the converters have been estimated as described in Appendix B. The losses for the direct-coupled system at 50 and 500 Hz have been summarised in figure 5.5.

The results show a significant increase in losses when the system are operated at 500 Hz. This is due to a 13 fold increase in switching losses. As in the AAC a number of cells have effectively been replaced by direct-switches, this system uses fewer switches in its cells than the MMC F2F system. As a result the switching losses start from a smaller base, at 50 Hz, and consequently do not grow in magnitude as much as in the MMC system. As the conduction losses remain unaffected by the AC frequency, the overall system losses of the AAC F2F are lower, at 852 kW, than those of the MMC F2F, at 979 kW, at 500 Hz. At 50 Hz it is the other way around.

The effect of an increase in frequency on the converter in the transformer coupled system can be seen in figure 5.6. The switching losses incurred in the cells again cause a large increase in converter losses when the system are operated at 500 Hz. The MMC F2F system can be noted to operate with 941 kW and the AAC with 1050 kW of losses.

In the previous chapter it was explained that the transformer-coupled system was found to require a higher cell rotation frequency at $16 \cdot f_{AC}$ compared with $8.2 \cdot f_{AC}$ for the direct-coupled system. The transformer-coupled system also contains an extra cell in each cell stack to provide additional voltage capability. For these reasons the losses

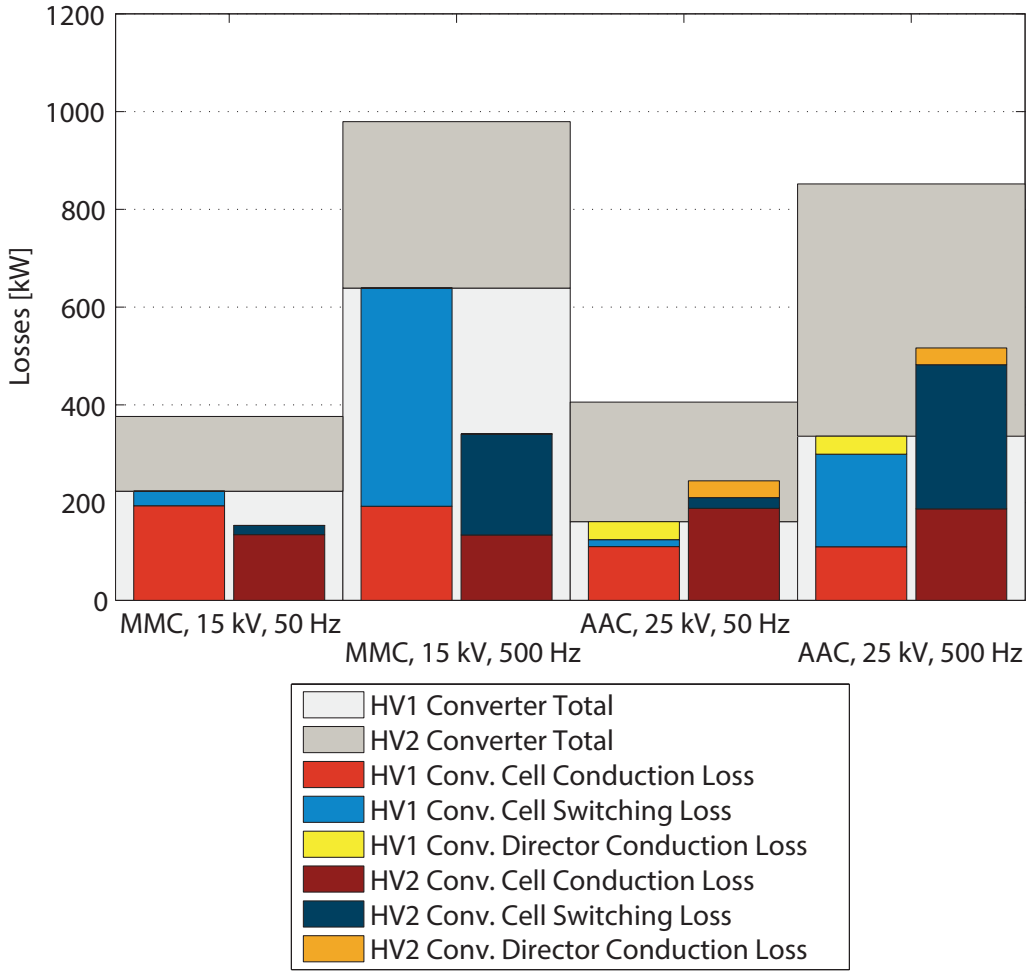

Figure 5.5: Converter losses for direct-coupled F2F systems using both MMCs and AACs for 50 and 500 Hz.

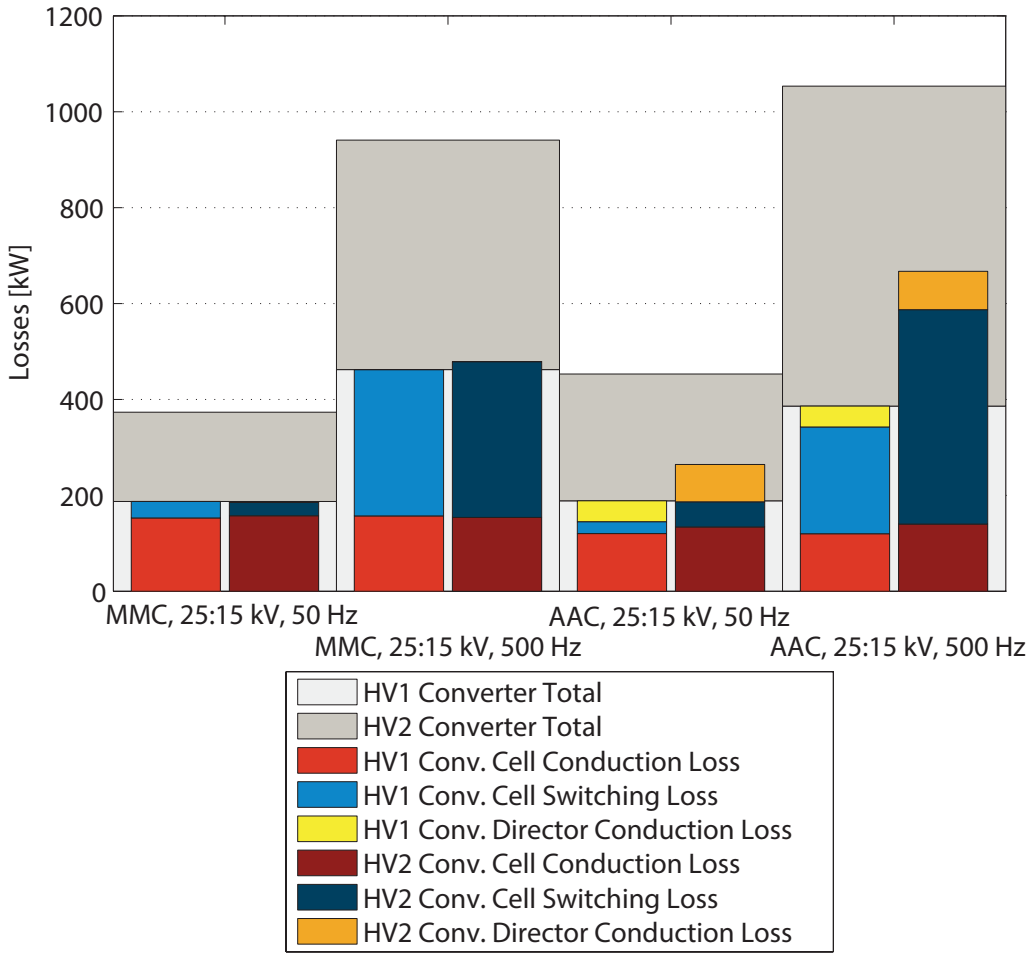

Figure 5.6: Converter losses for transformer-coupled F2F systems using both MMCs and AACs for 50 and 500 Hz.

incurred in the HV2 MMCs for example are slightly different between the direct- and transformer-coupled systems, even though the converter voltage in both cases is 15 kV. Since these conditions were found to be required for stable operation in the transformer-coupled system, a like-for-like comparison is still possible.

The difference in rotation frequency can also be used to illustrate its effects on the losses (ignoring the fact that an extra cell is included in the transformer-coupled system): a doubling of the rotation frequency causes and increase in the switching losses in the HV2 MMC, operated at 15 kV, from 19 to 29 kW at 50 Hz and from 207 to 325 kW at 500 Hz. This equates to an increase by a factor of about 1.5 in both cases. A similar ratio can be found when looking at the switching losses of the HV1 AAC, which is operated at 25 kV in both scenarios.

5.3 Chapter Summary: Raising the AC frequency in the F2F topologies

This chapter explored the effects on the system performance, measured by the systems' losses and its volume, from raising the AC frequency from 50 to 500 Hz. This increase is possible as the AC links is fully internal to the system and therefore not limited by normal AC grid codes. Such an increase in frequency can significantly reduce the cell capacitance and therefore the associated volume. Thus the most efficient AC voltage may be chosen for the F2F system and then the frequency raised until the required volume reduction is achieved.

Tables 5.3 and 5.4 shows the results for an increase in frequency for the most efficient MMC and AAC direct-coupled F2F variants. Similarly tables 5.5 and 5.6 show the results for the most efficient transformer-coupled system variants.

Since the cell capacitance has been confirmed to scale inversely with respect to frequency, the cell capacitance can be noted to fall significantly, especially for the AAC direct-coupled F2F system (27 mF per phase). For the same system variant the losses also significantly increase, due to a higher rate of switching in the cells, from 1.39 to 2.85% of the transferred power. In this regard the AAC fares significantly better than the MMC, which contains significantly more cells.

Due to the extra losses in the transformer, all transformer-variants incur significantly higher losses and require a higher capacitance. Thus, unless galvanic isolations is absolutely essential, a transformer does not appear to be feasible for such low step-ratios as explored with the test system.

The direct-coupled system achieves a reasonably good system performance. Whist the operation at 500 Hz significantly increases the losses, it can be used as a guide for the system designer. by first choosing an AC voltage purely based on losses, the AC frequency can then be raised to reduce the volume of the cell capacitance, keeping the extra switching losses incurred because of it in mind.

Table 5.3: Summary of the MMC F2F direct-coupled system performance measures at $\hat{V}_{AC} = 15$ kV.

f_{AC} [Hz]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Total	$\frac{P_{loss}}{P_{transferred}}$
50	819 mF	*376 kW*	*39 kW*	404 kW	1.35%
500	82 mF	*979 kW*	*10 kW*	989 kW	3.30%

Table 5.4: Summary of the AAC F2F direct-coupled system performance measures at $\hat{V}_{AC} = 25$ kV.

f_{AC} [Hz]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Total	$\frac{P_{loss}}{P_{transferred}}$
50	267 mF	*405 kW*	*13 kW*	420 kW	1.40%
500	27 mF	*852 kW*	*3 kW*	855 kW	2.85%

Table 5.5: Summary of the MMC F2F transformer-coupled system performance measures at winding voltages of 25 : 15 kV.

f_{AC} [Hz]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Trans.	Total	$\frac{P_{loss}}{P_{transferred}}$
50	971 mF	*373 kW*	*36 kW*	*121 kW*	530 kW	1.77%
500	97 mF	*941 kW*	*9 kW*	*154 kW*	1104 kW	3.68%

Table 5.6: Summary of the AAC F2F transformer-coupled system performance measures at winding voltages of 25 : 15 kV.

f_{AC} [Hz]	Cap. per phase	*Conv. losses*	*Ind. Losses*	Trans.	Total	$\frac{P_{loss}}{P_{transferred}}$
50	494 mF	*453 kW*	*19 kW*	*121 kW*	593 kW	1.98%
500	49 mF	*1050 kW*	*5 kW*	*154 kW*	1209 kW	4.03%

Chapter 6

Alternative Waveforms and Converter Formats

Previous chapters explored how a DC to DC conversion for HVDC applications could be achieved effectively, using technology and, in particular, circuit topologies that are already well-studied. Such circuits have their advantages, particularly if it comes to reducing the time taken for a DC/DC converter to progress from design to commissioning. Transmission system operators are by nature cautious customers of new equipment, especially when it comes to equipment worth several millions of pounds sterling. From this viewpoint, utilising well understood circuit topologies and technologies makes sense for the system operator, as they will have greater faith in proven components' reliability.

If one were given a free hand at designing new circuit topologies and formats then one might arrive at some alternative designs to the front-to-front-arrangement presented previously. This chapter presents four such designs, which still utilise modular cell technology, but are not necessarily arranged in accustomed three-phase designs nor use sinusoidal waveforms.

In the previous DC/AC/DC system format the DC to DC conversion was achieved with an intermediate AC step. Alternatively a DC/DC converter could be designed to allow for a direct conversion, without such an AC step. In this chapter two designs for such direct DC/DC converter are presented along with two alternative designs for DC/AC/DC converters. The latter however were designed with non-conventional AC waveforms in mind from the outset.

6.1 Direct DC/DC Conversion Circuit Topologies

Since a stack of cells can be thought of as a controlled voltage source, it can be used to generate a DC voltage, thereby effectively applying a DC step. The direct conversion circuit topologies use this idea to provide a DC to DC conversion using only cell stacks. There are no intermediate AC conversion steps to provide this conversion nor are there any transformers included in any of the circuits.

6.1.1 Parallel Output Pole Topology

The first direct conversion architecture is shown in figure 6.1. A similar circuit has been presented in [98]. This circuit can be thought of as the DC version of the MMC. It utilises two phase legs, consisting of two stacks of cells each, which generate a DC voltage at their midpoint ($V_{d2}/2$). Each cell stack is connected in series with an arm inductance (labelled $L_{a,b}^{+,-}$) to provide additional inductance in the current paths to limit their respective rates of change ($\frac{dI}{dt}$). By controlling the voltages across these inductances, the cell stacks can control the converter's currents.

Voltage and Current equations

The voltages ($V_{d1,d2}$) and currents ($I_{d1,d2}$) of two DC links are related through the converter step-ratio (κ) as per equations (6.1) and (6.2), such that V_{d2} is the lower of the two voltages.

$$V_{d2} = \kappa \cdot V_{d1} \tag{6.1}$$

$$I_{d2} = \frac{I_{d1}}{\kappa} \tag{6.2}$$

$$\therefore \kappa = (0, 1] \tag{6.3}$$

The stacks have to provide DC voltages as per equations (6.4) to (6.7). From them it can be seen that as the step-ratio increases ($\kappa \to 0$) the stack voltages in a phase leg change to accommodate the lower output (HV2) voltage. The total voltage capability per

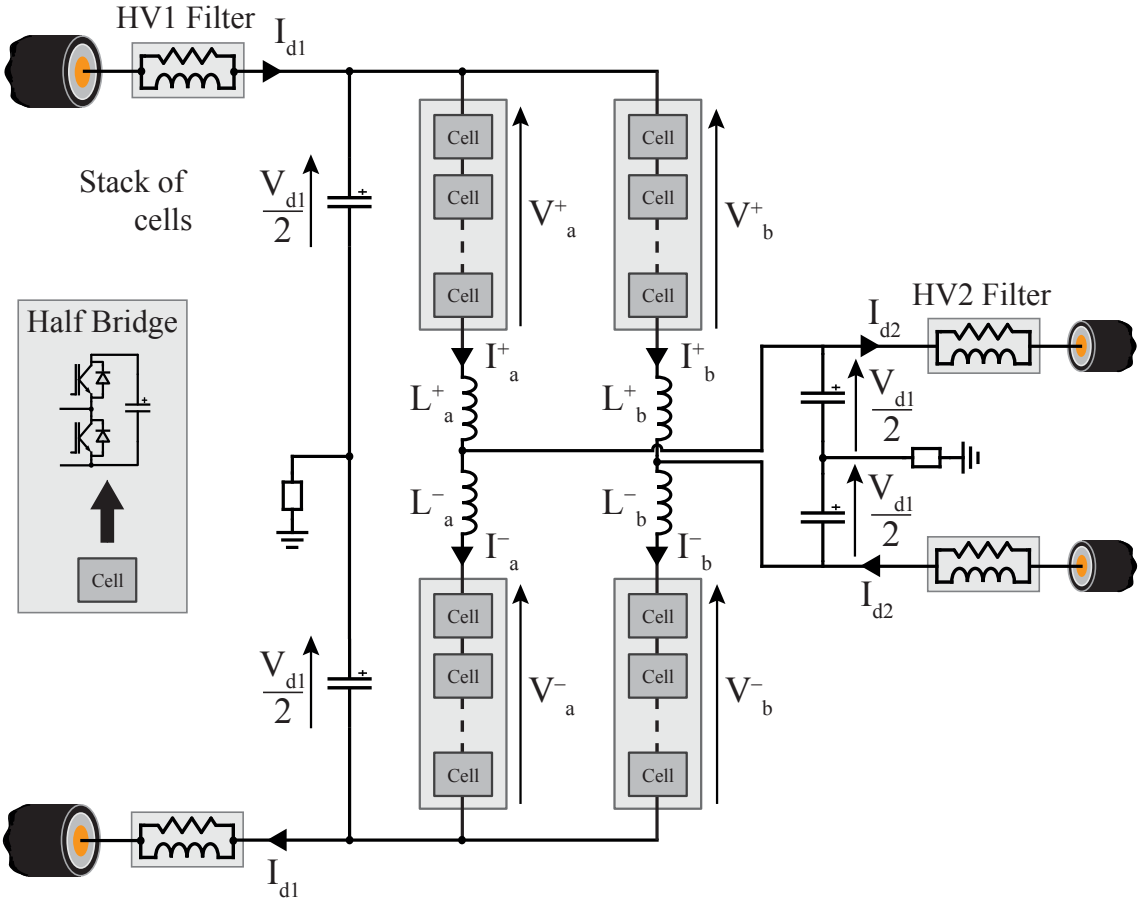

Figure 6.1: Parallel output pole, direct conversion DC/DC circuit

stack pair in a phase leg (i.e. $V_a^{+,-}$) remains unchanged.

$$\begin{aligned} V_a^+ &= \frac{V_{d1}}{2} - \frac{V_{d2}}{2} \\ &= \frac{V_{d1}}{2}(1-\kappa) \end{aligned} \tag{6.4}$$

$$\begin{aligned} V_a^- &= \frac{V_{d1}}{2} + \frac{V_{d2}}{2} \\ &= \frac{V_{d1}}{2}(1+\kappa) \end{aligned} \tag{6.5}$$

$$\begin{aligned} V_b^+ &= \frac{V_{d1}}{2} + \frac{V_{d2}}{2} \\ &= \frac{V_{d1}}{2}(1+\kappa) \end{aligned} \tag{6.6}$$

$$\begin{aligned} V_b^- &= \frac{V_{d1}}{2} - \frac{V_{d2}}{2} \\ &= \frac{V_{d1}}{2}(1-\kappa) \end{aligned} \tag{6.7}$$

Assuming that the current I_{d1} splits equally between phase legs a and b and that the current I_{d2} splits similarly equally between the top and bottom stacks, the arm currents can be found as per (6.8) to (6.11). As the DC power on the HV1 and HV2 sides must be equal (ignoring losses), the current magnitude in the HV2 DC link increases linearly as the HV2 voltage drops, i.e., the step-ratio increases (assuming a constant power transfer magnitude). Consequently the arm currents are a function of the step-ratio.

$$\begin{aligned} I_a^+ &= \frac{I_{d1}}{2} + \frac{I_{d2}}{2} \\ &= \frac{I_{d1}}{2}\left(1 + \frac{1}{\kappa}\right) \end{aligned} \tag{6.8}$$

$$\begin{aligned} I_a^- &= \frac{I_{d1}}{2} - \frac{I_{d2}}{2} \\ &= \frac{I_{d1}}{2}\left(1 - \frac{1}{\kappa}\right) \end{aligned} \tag{6.9}$$

$$\begin{aligned} I_b^+ &= \frac{I_{d1}}{2} + \frac{I_{d2}}{2} \\ &= \frac{I_{d1}}{2}\left(1 - \frac{1}{\kappa}\right) \end{aligned} \tag{6.10}$$

$$\begin{aligned} I_b^- &= \frac{I_{d1}}{2} - \frac{I_{d2}}{2} \\ &= \frac{I_{d1}}{2}\left(1 + \frac{1}{\kappa}\right) \end{aligned} \tag{6.11}$$

Cell stack energy balancing mechanism

As with all circuits that utilise cells and other capacitors it is vital to ensure that during normal operation the cell capacitors do not get fully discharged, as this would prevent normal operation of the circuit. Since low level control algorithms will ensure that individual cell capacitors inside a stack of cells are balanced, we can at this point focus solely on the energy of the stack as a whole. To investigate this we need to look at the energy equations of the stacks, as shown in (6.12) to (6.15). Since this circuit has no natural frequency as all currents and voltages are DC, the time window for the integration (T_0) can be of any value.[1]

$$\begin{aligned} E_a^+ &= \int_0^{T_0} V_a^+ I_a^+ \mathrm{d}t \\ &= \frac{1}{4} T_0 V_{d1} I_{d1} (1-\kappa) \left(1 + \frac{1}{\kappa}\right) \\ &= T_0 V_{d1} I_{d1} \left(\frac{1-\kappa^2}{4\kappa}\right) \\ &= E_{01} \left(\frac{1-\kappa^2}{4\kappa}\right) \\ &\therefore\ E_{01} = T_0 V_{d1} I_{d1} \end{aligned} \tag{6.12}$$

$$\begin{aligned} E_a^- &= \int_0^{T_0} V_a^- I_a^- \mathrm{d}t \\ &= \frac{1}{4} T_0 V_{d1} I_{d1} (1+\kappa) \left(1 - \frac{1}{\kappa}\right) \\ &= E_{01} \left(\frac{\kappa^2-1}{4\kappa}\right) \end{aligned} \tag{6.13}$$

$$\begin{aligned} E_b^+ &= \int_0^{T_0} V_b^+ I_b^+ \mathrm{d}t \\ &= \frac{1}{4} T_0 V_{d1} I_{d1} (1+\kappa) \left(1 - \frac{1}{\kappa}\right) \\ &= E_{01} \left(\frac{\kappa^2-1}{4\kappa}\right) \end{aligned} \tag{6.14}$$

[1] The only reason for expressing the equations in terms of energy rather than power are purely for continuity and so as not to have to talk about energy and power balancing in the same vein.

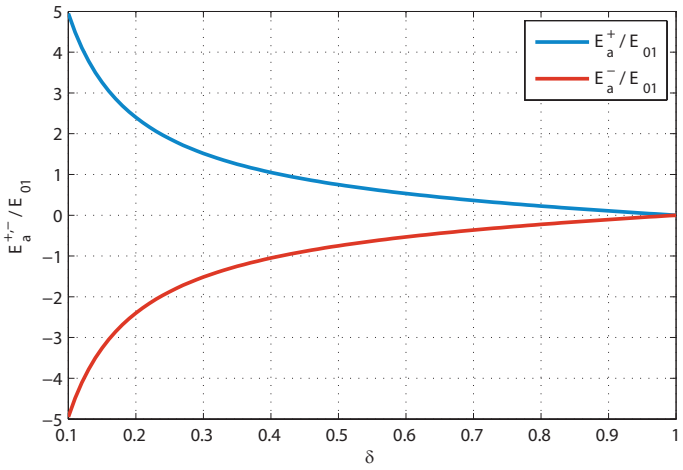

Figure 6.2: Energy drift in parallel pole DC/DC converter with respect to step-ratio.

$$\begin{aligned} E_b^- &= \int_0^{T_0} V_b^- I_b^- \mathrm{d}t \\ &= \frac{1}{4} T_0 V_{d1} I_{d1} (1-\kappa) \left(1 + \frac{1}{\kappa}\right) \\ &= E_{01} \left(\frac{1-\kappa^2}{4\kappa}\right) \end{aligned} \tag{6.15}$$

The energy equations, (6.12) to (6.15), show that the energy of the stacks is non-zero after a time T_0. The stacks are therefore not energy balanced and suffer from energy drift. It can furthermore be noticed that the energy drift $E_a^+ = E_b^-$ and similarly $E_a^- = E_b^+$. This is not a surprising result as the voltage, (6.7) to (6.8), and current equations, (6.11) to (6.12), show a similar symmetry.

Furthermore it can be noted that the energy drift is proportional to the input power: $\frac{E_{01}}{T_0}$. The relationship between the energy drift and the step ratio is non-linear and has been illustrated in figure 6.2. From the graph it can be noticed that energy drift for a step-ration of 10:1 ($\kappa = 0.1$) is 6.6 times larger than for a step-ratio of 2:1 ($\kappa = 0.5$).

To derive the energy equations in (6.12) to (6.15) we assumed that the currents from the DC links (I_{d1} and I_{d2}) split equally between both phases as well as the top and bottom phases (see (6.8) to (6.11)). This assumption is not however necessarily true as the link currents could be split arbitrarily as long as the equations in (6.16) and (6.17) remain true. The definition of the currents $I_{a,b}$ and $I^{+,-}$ can be seen in figure 6.3.

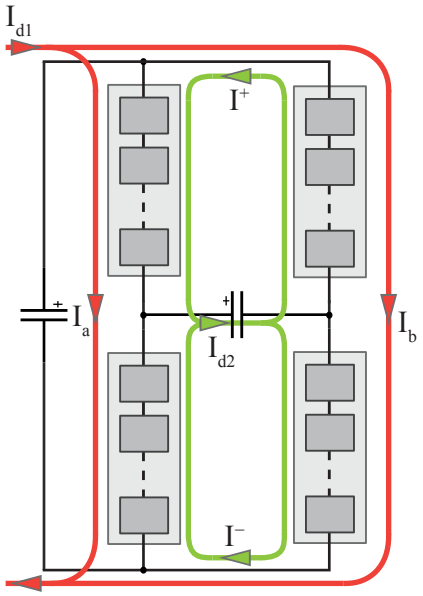

Figure 6.3: Split of DC links currents in parallel output pole DC/DC circuit.

$$I_{d1} = I_a + I_b \tag{6.16}$$

$$I_{d2} = I^+ + I^- \tag{6.17}$$

We can define the the loop currents $I_{a,b}$ and $I^{+,-}$ in terms of the DC link currents as shown in (6.18) and (6.19).

$$\begin{aligned} I_a &= \alpha I_{d1} \\ I_b &= (1-\alpha) I_{d1} \\ &: \alpha = [0,1] \end{aligned} \tag{6.18}$$

$$\begin{aligned} I^+ &= \beta I_{d2} \\ I^- &= (1-\beta) I_{d2} \\ &: \beta = [0,1] \end{aligned} \tag{6.19}$$

The arm current definitions in terms of α, β and I_{d1} then become (6.20) to (6.23).

$$\begin{aligned} I_a^+ &= I_a + I^+ \\ &= I_{d1}\left(\alpha + \frac{\beta}{\kappa}\right) \end{aligned} \tag{6.20}$$

$$\begin{aligned} I_a^- &= I_a - I^- \\ &= I_{d1}\left(\alpha - \frac{1-\beta}{\kappa}\right) \end{aligned} \tag{6.21}$$

$$\begin{aligned} I_b^+ &= I_b - I^+ \\ &= I_{d1}\left(1 - \alpha - \frac{\beta}{\kappa}\right) \end{aligned} \tag{6.22}$$

$$\begin{aligned} I_b^- &= I_b + I^- \\ &= I_{d1}\left(1 - \alpha + \frac{1-\beta}{\kappa}\right) \end{aligned} \tag{6.23}$$

The energy equations of the cell stacks using the current definitions given in (6.20) to (6.23) are derived in (6.24) to (6.27).

$$\begin{aligned} E_a^+ &= \int_0^{T_0} V_a^+ I_a^+ \mathrm{d}t \\ &= \frac{1}{2} E_{01}\left(\alpha + \frac{\beta}{\kappa}\right)(1-\kappa) \end{aligned} \tag{6.24}$$

$$\begin{aligned} E_a^- &= \int_0^{T_0} V_a^- I_a^- \mathrm{d}t \\ &= \frac{1}{2} E_{01}\left(\alpha - \frac{1-\beta}{\kappa}\right)(1+\kappa) \end{aligned} \tag{6.25}$$

$$\begin{aligned} E_b^+ &= \int_0^{T_0} V_b^+ I_b^+ \mathrm{d}t \\ &= \frac{1}{2} E_{01}\left(1 - \alpha - \frac{\beta}{\kappa}\right)(1+\kappa) \end{aligned} \tag{6.26}$$

$$\begin{aligned} E_b^- &= \int_0^{T_0} V_b^- I_b^- \mathrm{d}t \\ &= \frac{1}{2} E_{01}\left(1 - \alpha + \frac{1-\beta}{\kappa}\right)(1-\kappa) \end{aligned} \tag{6.27}$$

To find the best value of α and β that minimises the absolute energy drift of the converter (E_Σ) we must consider the sum of the absolute energy drifts of all the cell stacks as described in (6.28).

$$E_\Sigma = \left|E_a^+\right| + \left|E_a^-\right| + \left|E_b^+\right| + \left|E_b^-\right| \tag{6.28}$$

We can now simply consider how the ratio $\frac{E_\Sigma}{E_{01}}$ scales with respect to the loop current variables α and β for a range of step-ratios (κ). Figure 6.4 shows the results from which we can notice two trends: first, that there exists a region where E_Σ is minimised for any particular κ. This region increases as κ approaches 0. Second, and more importantly, we can see that the minimum absolute energy drift of the converter dramatically increases as κ tends to 0.

Although we must conclude that varying the split of the loop currents $I_{a,b}$ and $I^{+,-}$ does not automatically balance the overall energy drift in the converter, a modulation of these currents may still be useful to counteract temporary energy imbalances. Due to power ramps or other transient events it may become necessary to shift energy from one cell stack to another.

We can group the four stacks into vertical and horizontal pairs. The total energy contained in each horizontal pair is derived in (6.29) and (6.30), and in each vertical pair in (6.31) and (6.32).

$$\begin{aligned} E_a &= E_a^+ + E_a^- \\ &= E_{01}\left((\alpha+\beta) - \frac{1}{2}\left(1+\frac{1}{\kappa}\right)\right) \end{aligned} \tag{6.29}$$

$$\begin{aligned} E_b &= E_b^+ + E_b^- \\ &= E_{01}\left(\frac{1}{2}\left(1+\frac{1}{\kappa}\right) - \left(\alpha+\frac{\beta}{\kappa}\right)\right) \end{aligned} \tag{6.30}$$

$$\begin{aligned} E^+ &= E_a^+ + E_b^+ \\ &= E_{01}\left(\frac{1}{2}(1+\kappa) - (\alpha\kappa+\beta)\right) \end{aligned} \tag{6.31}$$

$$\begin{aligned} E^- &= E_a^- + E_b^- \\ &= E_{01}\left((\alpha\kappa+\beta) - \frac{1}{2}(1+\kappa)\right) \end{aligned} \tag{6.32}$$

The equations derived in (6.33) and (6.34) show the expressions for the difference in energy in the horizontal and vertical pair of cell stacks respectively. Both loop current modulation indices (α and β) can be noted to affect the balance. When all stacks are equally balanced the expressions will equate to zero. Should there be mismatch then the

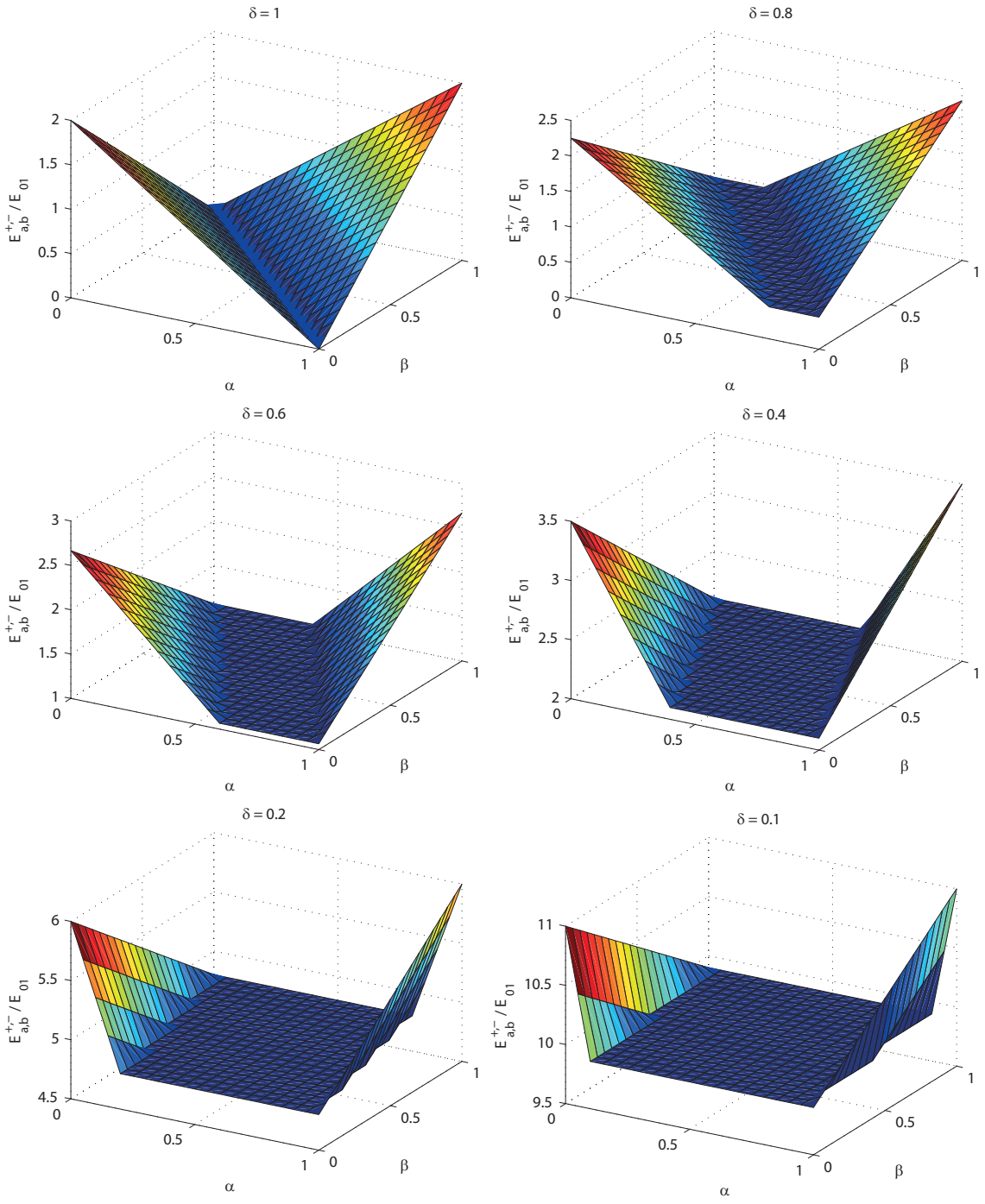

Figure 6.4: Scaling of energy drift ratio ($\frac{E_\Sigma}{E_{01}}$) for range of step-ratios with respect to different $I^{+,-}$ and $I_{a,b}$ splits.

loop currents can be modulated so as to counteract this imbalance.

$$\begin{aligned} E_{ab} &= E_a - E_b \\ &= E_{01}\left(2\left(\alpha + \frac{\beta}{\kappa}\right) - \left(1 + \frac{1}{\kappa}\right)\right) \end{aligned} \tag{6.33}$$

$$\begin{aligned} E^{+-} &= E^{+} - E^{-} \\ &= E_{01}\left(1\left(\kappa + 1\right) - 2\left(\alpha\kappa + \beta\right)\right) \end{aligned} \tag{6.34}$$

Figure 6.5 shows how the energies E_{ab} and E^{+-} can be affected by α and β. The top two graphs show the energy drifts for $\kappa = 1$. Both E_{ab} and E^{+-} can be seen to be equal and opposite with respect to α and β. Importantly there exist a range of solutions for any particular energy drift as the planes are notably diagonal with respect to the axes. This makes it easier to find suitable values for α and β simultaneously to allow for efficient energy rebalancing.

As the step-ratio is increased ($\kappa = 0.1$) the planes become more aligned with the axes, as shown in the bottom two graphs in figure 6.5. Furthermore a significant difference in peak values between the horizontal and vertical energy drifts can be noted. These two factors make it increasingly difficult to utilise these modulated loop currents to completely rebalance the cell stacks vertically as well as horizontally, as the step-ratio increases.

An energy controller utilising modulated loop currents for energy balancing purposes would also need to take the limitations placed on α and β into account. From figure 6.4 it was concluded that there exists a region for each step-ratio where the absolute energy drift is kept to a minimum. Therefore the values of the α and β should be chosen so as to maintain converter operation within that region. Furthermore the crucial limitation of possible values for α and β as described in (6.18) and (6.19) also need to be taken into account.

The energy drift experienced in the cell stacks due to steady-state operation remains an issue. As the existing currents in the converter have been shown to be inadequate in rebalancing this energy drift, an additional current and voltage need to be introduced to the system. A circulating AC current (I_e), as shown in figure 6.6, combined with an AC voltage (V_e) applied at both phase leg mid-points can be used to rebalance the cell stacks. The AC voltages are applied such that the voltage across the HV2 DC link capacitor remains the desired DC voltage, as illustrated in figure 6.7, without any AC component.

Square-waves were chosen for the AC component to allow the magnitude of the AC

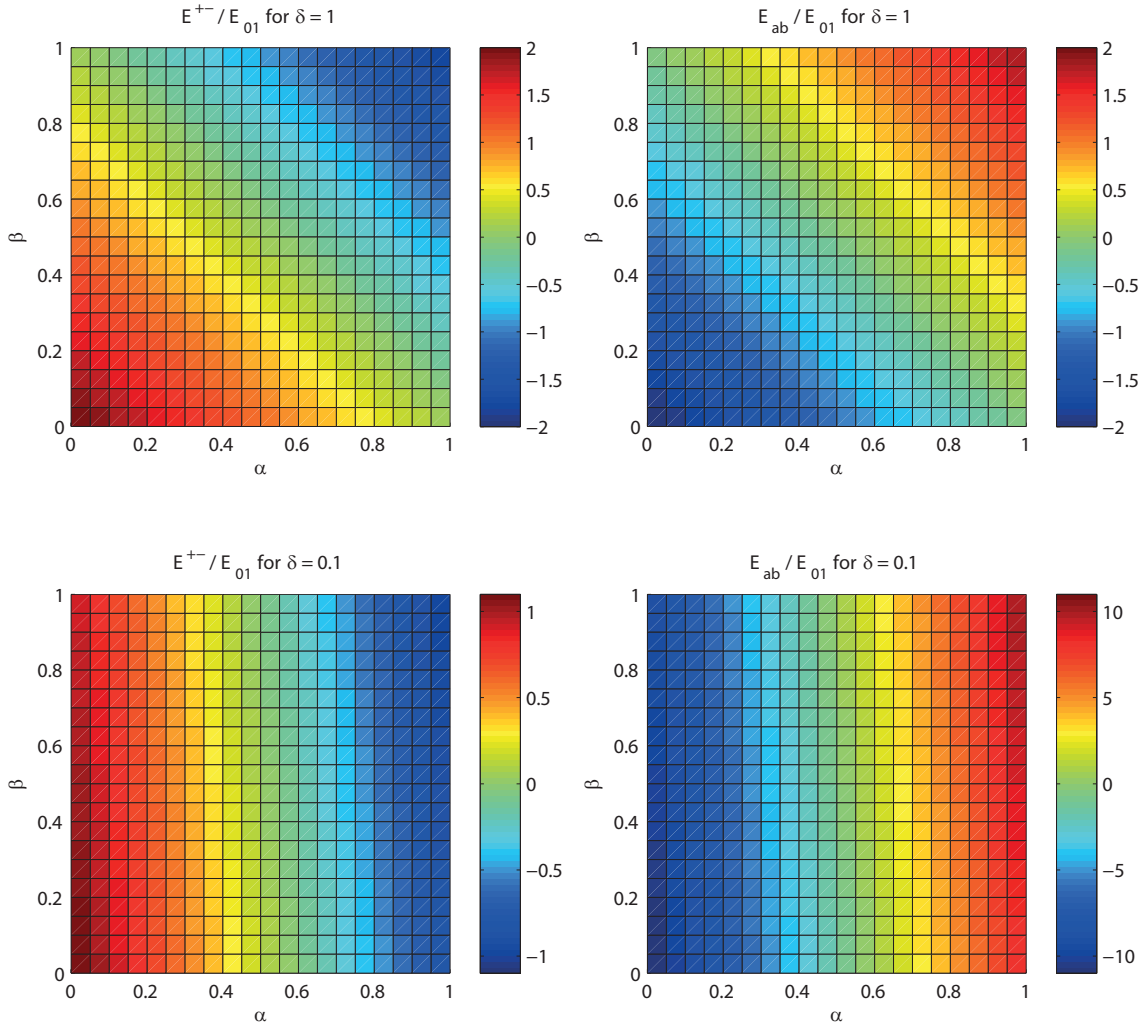

Figure 6.5: Vertical (E^{+-}) and horizontal (E_{ab}) energy drift with respect to α an β for $\kappa = 1$ and $\kappa = 0.1$.

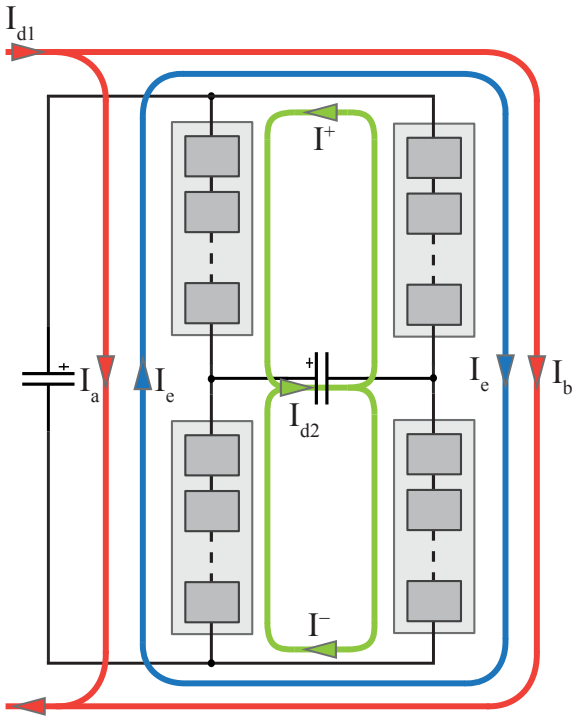

Figure 6.6: Circulating AC balancing current overlay on top of DC currents in parallel output pole DC/DC circuit.

voltage to be an integer number of coll voltages. This minimises the switching losses associated with the generation of the AC component.

The modified cell stack energy equations taking the AC balancing voltage and current into account are shown in (6.35) to (6.38). These equations assume balanced DC loop currents ($\alpha = \beta = \frac{1}{2}$).

$$\begin{aligned} E_a^+ &= \int_0^{T_0} V_a^+ I_a^+ \mathrm{d}t \\ &= \left[t \left(\frac{V_{d1}}{2}(1-\kappa) - \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 + \frac{1}{\kappa} \right) + \hat{I}_e \right) \right]_0^{\lambda T_0} \\ &\quad + \left[t \left(\frac{V_{d1}}{2}(1-\kappa) + \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 + \frac{1}{\kappa} \right) - \hat{I}_e \right) \right]_{\lambda T_0}^{T_0} \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{4} (1-\kappa) \left(1 + \frac{1}{\kappa} \right) - \frac{V_e \hat{I}_e}{2} \right) \\ &\quad + T_0 (1-2\lambda) \left(\frac{V_e I_{d1}}{4} \left(1 + \frac{1}{\kappa} \right) - \frac{V_{d1} \hat{I}_e}{2} (1-\kappa) \right) \end{aligned} \tag{6.35}$$

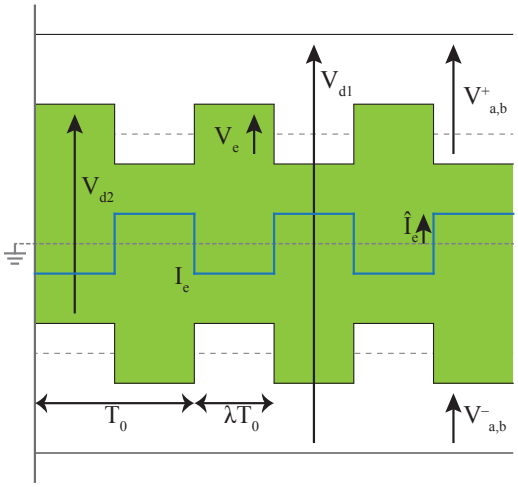

Figure 6.7: Illustration of proposed balancing circulating current and AC voltage in parallel output pole DC/DC circuit.

$$
\begin{aligned}
E_a^- &= \int_0^{T_0} V_a^- I_a^- \,\mathrm{d}t \\
&= \left[t \left(\frac{V_{d1}}{2}(1+\kappa) + \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 - \frac{1}{\kappa} \right) + \hat{I}_e \right) \right]_0^{\lambda T_0} \\
&\quad + \left[t \left(v(1+\kappa) - \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 - \frac{1}{\kappa} \right) - \hat{I}_e \right) \right]_{\lambda T_0}^{T_0} \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{4} (1+\kappa) \left(1 - \frac{1}{\kappa} \right) + \frac{V_e \hat{I}_e}{2} \right) \\
&\quad - T_0(1-2\lambda) \left(\frac{V_e I_{d1}}{4} \left(1 - \frac{1}{\kappa} \right) + \frac{V_{d1} \hat{I}_e}{2} (1+\kappa) \right)
\end{aligned} \tag{6.36}
$$

$$
\begin{aligned}
E_b^+ &= \int_0^{T_0} V_b^+ I_b^+ \,\mathrm{d}t \\
&= \left[t \left(\frac{V_{d1}}{2}(1+\kappa) - \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 - \frac{1}{\kappa} \right) - \hat{I}_e \right) \right]_0^{\lambda T_0} \\
&\quad + \left[t \left(\frac{V_{d1}}{2}(1+\kappa) + \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 - \frac{1}{\kappa} \right) + \hat{I}_e \right) \right]_{\lambda T_0}^{T_0} \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{4} (1+\kappa) \left(1 - \frac{1}{\kappa} \right) + \frac{V_e \hat{I}_e}{2} \right) \\
&\quad + T_0(1-2\lambda) \left(\frac{V_e I_{d1}}{4} \left(1 - \frac{1}{\kappa} \right) + \frac{V_{d1} \hat{I}_e}{2} (1+\kappa) \right)
\end{aligned} \tag{6.37}
$$

$$
\begin{aligned}
E_b^- &= \int_0^{T_0} V_b^- I_b^- \,\mathrm{d}t \\
&= \left[t \left(\frac{V_{d1}}{2}(1-\kappa) + \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 + \frac{1}{\kappa} \right) - \hat{I}_e \right) \right]_0^{\lambda T_0} \\
&\quad + \left[t \left(\frac{V_{d1}}{2}(1-\kappa) - \frac{V_e}{2} \right) \left(\frac{I_{d1}}{2} \left(1 + \frac{1}{\kappa} \right) + \hat{I}_e \right) \right]_{\lambda T_0}^{T_0} \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{4} (1-\kappa) \left(1 + \frac{1}{\kappa} \right) - \frac{V_e \hat{I}_e}{2} \right) \\
&\quad - T_0 (1-2\lambda) \left(\frac{V_e I_{d1}}{4} \left(1 + \frac{1}{\kappa} \right) - \frac{V_{d1} \hat{I}_e}{2} (1-\kappa) \right)
\end{aligned} \tag{6.38}
$$

Setting duty-cycle of the AC waveforms (λ) equal to $\frac{1}{2}$ allows the steady-state energy drift of the stacks to be rebalanced using the circulating current (I_e) and the AC voltage offset (V_e). Furthermore modulating λ allows us to rebalance horizontal or vertical energy imbalances as well. Using the equations shown in (6.35) to (6.38) we can redefine the vertical ((6.39) to (6.40)) and horizontal ((6.41) to (6.42)) stack pair energies.

$$
\begin{aligned}
E_a &= E_a^+ + E_a^- \\
&= T_0 \left(1 - 2\lambda \right) \left(\frac{V_e I_{d1}}{2\kappa} - V_{d1} \hat{I}_e \right)
\end{aligned} \tag{6.39}
$$

$$
\begin{aligned}
E_b &= E_b^+ + E_b^- \\
&= -T_0 \left(1 - 2\lambda \right) \left(\frac{V_e I_{d1}}{2\kappa} - V_{d1} \hat{I}_e \right)
\end{aligned} \tag{6.40}
$$

$$
\begin{aligned}
E^+ &= E_a^+ + E_b^+ \\
&= T_0 \left(1 - 2\lambda \right) \left(\frac{V_e I_{d1}}{2} + \kappa V_{d1} \hat{I}_e \right)
\end{aligned} \tag{6.41}
$$

$$
\begin{aligned}
E_b &= E_b^+ + E_b^- \\
&= -T_0 \left(1 - 2\lambda \right) \left(\frac{V_e I_{d1}}{2} + \kappa V_{d1} \hat{I}_e \right)
\end{aligned} \tag{6.42}
$$

The horizontal (E_{ab}) and vertical (E^{+-}) energy drift can be expressed in terms of λ as shown in (6.43) and (6.44). From these equations it can be seen that modulating λ will affect both the vertical and horizontal energy balances. Thus the most effective

solution for the energy controller to employ may well be a combination of modulating the loop currents using α and β as well as λ. Since figure 6.5 illustrated that the horizontal energy exchange becomes more sensitive to small changes in α as the step-ratio increases, the horizontal energy balance should be done with the loop currents, as only a small modulation will be required, therefore affecting the vertical balance less. This leaves the modulation of λ to address any vertical energy imbalances.

$$\begin{aligned} E_{ab} &= E_a - E_b \\ &= 2T_0\,(1-2\lambda)\left(\frac{V_e I_{d1}}{2\kappa} - V_{d1}\hat{I}_e\right) \end{aligned} \tag{6.43}$$

$$\begin{aligned} E^{+-} &= E^{+} - E^{-} \\ &= 2T_0\,(1-2\lambda)\left(\frac{V_e I_{d1}}{2} + \kappa V_{d1}\hat{I}_e\right) \end{aligned} \tag{6.44}$$

The disadvantages of the additional AC voltage and circulating current is the fact that whilst the voltage across the HV2 capacitor remains unaffected, the terminal voltage relative to ground however is no longer purely DC. This may make the grounding arrangement, should one be required on this side, more difficult.

The AC voltage generated by the stacks means that the peak voltage capability of the stacks increases as $|V_e|$ increases. This means more cells and higher losses. The circulating AC current may also slightly raise losses as the conduction losses partly scale to the square of the current magnitude. Choosing the AC frequency will also require a trade-off: a higher frequency will require the cells to switch at a higher frequency, raising the switching losses. It may however also reduce the peak energy deviation experienced by the cells during each cycle. This would allow for smaller capacitances to be used in the cells, significantly decreasing the cells' volume. Further detailed studies of this circuit will be required to make a more detailed assessment of the trade-offs involved and confirm the effectiveness of the proposed balancing mechanisms.

6.1.2 Series Output Pole Topology

An alternative to the parallel output pole topology presented previously, is shown in figure 6.8, consequently referred to as the series output pole topology. A similar circuit has been presented in [95]. It consists of a single phase leg which supports the difference in output voltage ($V_o^{+,-}$) with two outer cell stacks connected between the corresponding DC terminals and two inner cell stacks bridging the HV2 voltage ($V_i^{+,-}$). The mid-point of the

two inner cell stacks is connected to the mid-point of the HV1 split cell capacitors forming a neutral connection which allows two energy balancing currents to be run, as explained in the following sections. To allow the cell stacks to control the currents through the current loops, each stack is series connected with an arm inductor ($L_{o,i}^{+,-}$).

Voltage and Current equations

The voltages ($V_{d1,d2}$) and currents ($I_{d1,d2}$) of the two DC links are related through the converter step-ratio (κ) as per equations (6.45) and (6.46), such that V_{d2} is the lower of the two voltages. This definition has been kept the same as for the previous circuit topology.

$$V_{d2} = \kappa \cdot V_{d1} \tag{6.45}$$

$$I_{d2} = \frac{I_{d1}}{\kappa} \tag{6.46}$$

$$\therefore \ \kappa = (0, 1] \tag{6.47}$$

The description of the cell stack voltages can be seen in (6.48) to (6.49). The voltage of top and bottom stacks ($V_{t,b}$) will increase as the step-ratio increases ($\kappa \to 0$). At the same time the voltage of the middle stack (V_m) will decrease with an increasing step-ratio. Ignoring any voltage capability required of the cell stacks for energy balancing purposes, this means that the total voltage capability of all four stacks, as described here, will not vary with step-ratio and is proportional to the HV1 voltage V_{d1}.

$$\begin{aligned} V_o^+ &= \frac{V_{d1}}{2} - \frac{V_{d2}}{2} \\ &= \frac{V_{d1}}{2}(1 - \kappa) \\ &= V_o^- \end{aligned} \tag{6.48}$$

$$\begin{aligned} V_i^+ &= \frac{V_{d2}}{2} \\ &= \frac{\kappa V_{d1}}{2} \\ &= V_i^- \end{aligned} \tag{6.49}$$

The arm currents are described in (6.50) and (6.51). The outer stacks can be noted to carry the full HV1 link current (I_{d1}). Since HV1 is of a higher voltage than HV2 this is the lower of the two link currents (assuming that input power must match the output

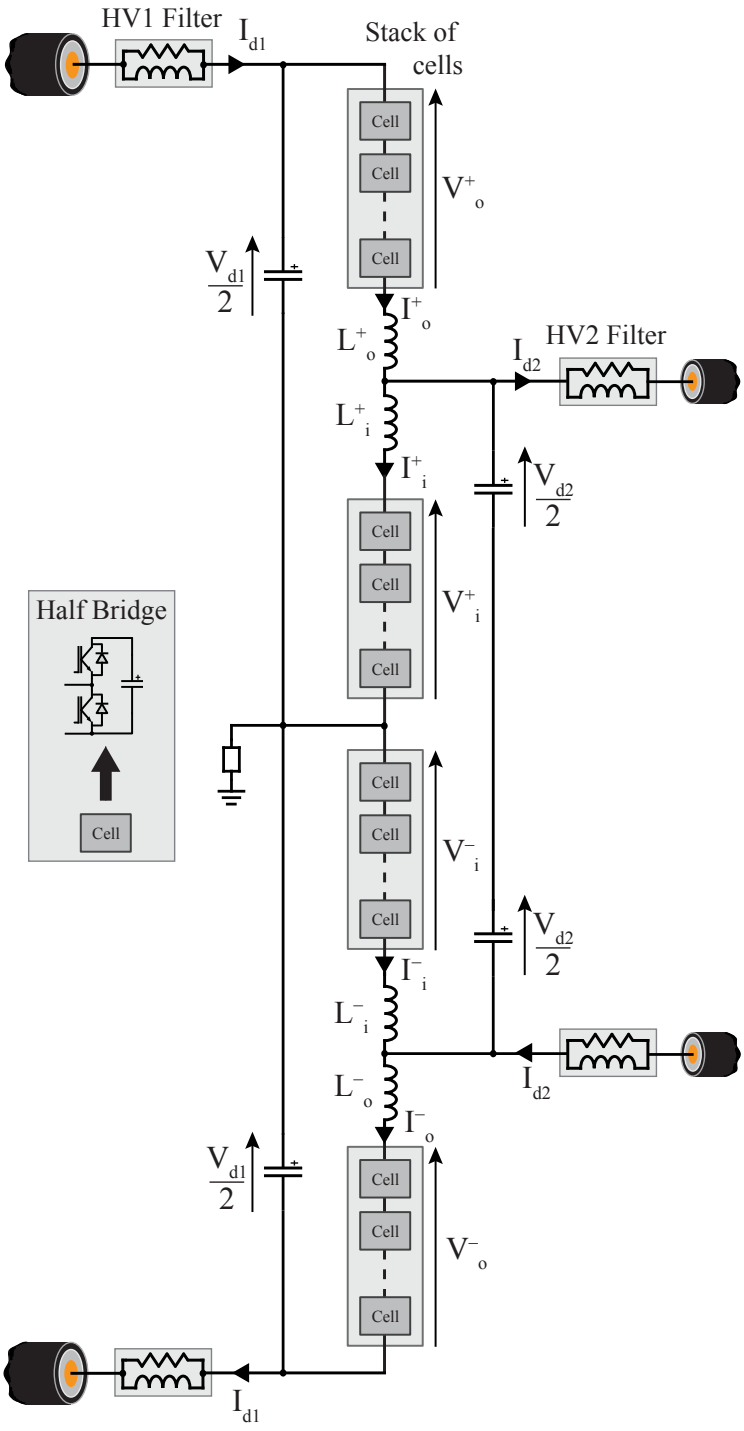

Figure 6.8: Series output pole, direct conversion DC/DC circuit

power). The middle stacks carry the difference between the two link currents. Thus as the step-ratio increases ($\kappa \to 0$) this current increases whilst the current in the outer stacks remains unchanged.

$$\begin{aligned} I_o^+ &= I_{d1} \\ &= I_o^- \end{aligned} \tag{6.50}$$

$$\begin{aligned} I_i^+ &= I_{d1} - I_{d2} \\ &= I_{d1}\left(1 - \frac{1}{\kappa}\right) \\ &= I_i^- \end{aligned} \tag{6.51}$$

Cell stack energy balancing mechanism

To assess the energy balancing requirements of the cell stacks during steady-state operation we must consider the energy equations of each stack as per the equations (6.52) to (6.55).

The energy equations show that all four stacks incur an energy drift which is proportional to the input power ($\frac{E_{01}}{T_0}$). The energy drift of the outer and inner stacks are of equal and opposite magnitude. This is true for the upper ($E_{o,i}^+$) and lower ($E_{o,i}^-$) pair of stacks. As the step-ratio increases ($\kappa \to 0$) the absolute energy drift increases as the energy state of each stack pair moves further apart. This is illustrated in figure 6.9 which shows how the energy drift is related to a changing step-ratio.

These equations only take the DC currents into account and serve to verify the existence of energy drift in the stacks. This emphasises the necessity for additional balancing mechanisms to be introduced to the circuit.

$$\begin{aligned} E_o^+ &= \int_0^{T_0} V_o^+ I_o^+ \mathrm{d}t \\ &= \frac{1}{2} T_0 V_{d1} I_{d1} (1 - \kappa) \\ &= E_{01}\left(\frac{1-\kappa}{2}\right) \\ &\therefore\ E_{01} = T_0 V_{d1} I_{d1} \end{aligned} \tag{6.52}$$

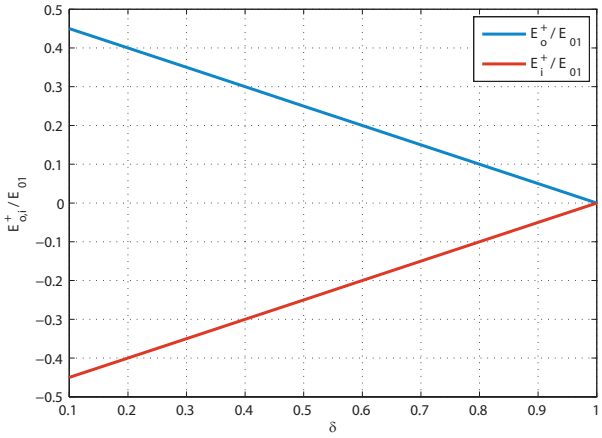

Figure 6.9: Energy drift in top inner and outer cell stacks of series output pole DC/DC circuit.

$$\begin{aligned} E_i^+ &= \int_0^{T_0} V_i^+ I_o^+ \mathrm{d}t \\ &= E_{01}\left(\frac{\kappa - 1}{2}\right) \end{aligned} \tag{6.53}$$

$$\begin{aligned} E_i^- &= \int_0^{T_0} V_i^- I_o^- \mathrm{d}t \\ &= E_{01}\left(\frac{\kappa - 1}{2}\right) \end{aligned} \tag{6.54}$$

$$\begin{aligned} E_i^- &= \int_0^{T_0} V_i^- I_o^- \mathrm{d}t \\ &= E_{01}\left(\frac{1 - \kappa}{2}\right) \end{aligned} \tag{6.55}$$

The series output pole DC/DC circuit only has a single current path for each link current. This means that there exists no way to modulate the link currents like in the parallel output pole circuit to provide a mechanism to exchange energy between the stacks. Therefore three additional circulating currents have to be set up to allow for the energy drift to be rebalanced as illustrated in figure 6.10. To enable energy to be exchanged with the cell stacks we must also add an AC voltage offset to the stack voltages as described in

figure 6.11. From this figure it can be seen that despite a square-wave offset on all stack voltages, the HV2 pole-to-pole voltage remains constant, provided the AC waveforms are kept in phase with one an other.

The energy equation for each stack can be rewritten taking the balancing currents and voltages into account as detailed in (6.56) to (6.59).

$$\begin{aligned} E_o^+ &= \int_0^{T_0} V_o^+ I_o^+ \mathrm{d}t \\ &= \left[t \left(\frac{V_{d1}}{2}(1-\kappa) - V_e \right) (I_{d1} + I_e^+ + I_L) \right]_0^{\lambda T_0} \\ &\quad + \left[t \left(\frac{V_{d1}}{2}(1-\kappa) + V_e \right) (I_{d1} - I_e^+ - I_L) \right]_{\lambda T_0}^{T_0} \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2}(1-\kappa) - V_e(I_e^+ + I_L) \right) \\ &\quad + T_0(1-2\lambda) \left(V_e I_{d1} - \frac{V_{d1}}{2}(I_e^+ + I_L)(1-\kappa) \right) \end{aligned} \tag{6.56}$$

$$\begin{aligned} E_i^+ &= \int_0^{T_0} V_i^+ I_i^+ \mathrm{d}t \\ &= \left[t \left(\frac{\kappa V_{d1}}{2} + V_e \right) (I_{d1} \left(1 - \frac{1}{\kappa} \right) + I_e^+ + I_L) \right]_0^{\lambda T_0} \\ &\quad + \left[t \left(\frac{\kappa V_{d1}}{2} - V_e \right) (I_{d1} \left(1 - \frac{1}{\kappa} \right) - I_e^+ - I_L) \right]_{\lambda T_0}^{T_0} \\ &= T_0 \left(-\frac{V_{d1} I_{d1}}{2}(1-\kappa) + V_e(I_e^+ + I_L) \right) \\ &\quad - T_0(1-2\lambda) \left(V_e I_{d1} \left(1 - \frac{1}{\kappa} \right) + \frac{\kappa V_{d1}}{2}(I_e^+ + I_L) \right) \end{aligned} \tag{6.57}$$

$$\begin{aligned} E_i^- &= \int_0^{T_0} V_i^- I_i^- \mathrm{d}t \\ &= \left[t \left(\frac{\kappa V_{d1}}{2} - V_e \right) (I_{d1} \left(1 - \frac{1}{\kappa} \right) - I_e^- + I_L) \right]_0^{\lambda T_0} \\ &\quad + \left[t \left(\frac{\kappa V_{d1}}{2} + V_e \right) (I_{d1} \left(1 - \frac{1}{\kappa} \right) + I_e^- - I_L) \right]_{\lambda T_0}^{T_0} \\ &= T_0 \left(-\frac{V_{d1} I_{d1}}{2}(1-\kappa) + V_e(I_e^- - I_L) \right) \\ &\quad + T_0(1-2\lambda) \left(V_e I_{d1} \left(1 - \frac{1}{\kappa} \right) + \frac{\kappa V_{d1}}{2}(I_e^- - I_L) \right) \end{aligned} \tag{6.58}$$

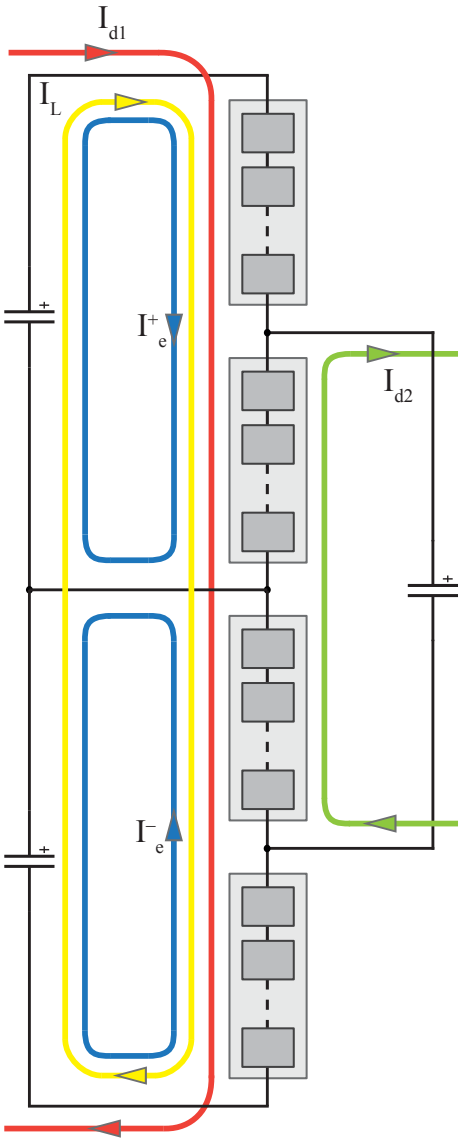

Figure 6.10: DC and AC balancing current loops in series output pole DC/DC circuit.

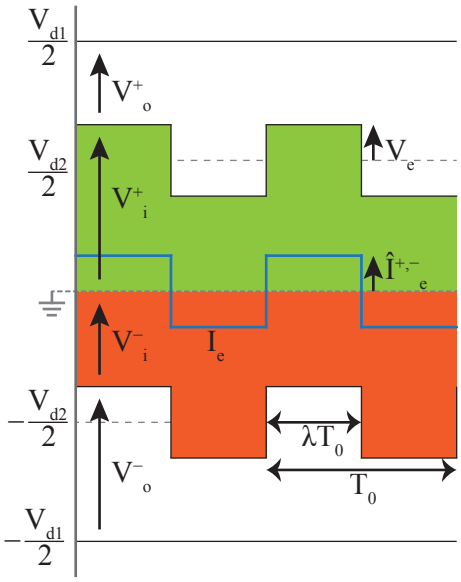

Figure 6.11: Stack voltages with AC energy balancing modulation voltage.

$$\begin{aligned} E_o^- &= \int_0^{T_0} V_o^- I_o^- \,\mathrm{d}t \\ &= \left[t \left(\frac{V_{d1}}{2}(1-\kappa) + V_e \right) (I_{d1} - I_e^- + I_L) \right]_0^{\lambda T_0} \\ &\quad + \left[t \left(\frac{V_{d1}}{2}(1-\kappa) - V_e \right) (I_{d1} + I_e^- - I_L) \right]_{\lambda T_0}^{T_0} \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2}(1-\kappa) - V_e(I_e^- - I_L) \right) \\ &\quad + T_0(1-2\lambda) \left(-V_e I_{d1} + \frac{V_{d1}}{2}(I_e^- - I_L)(1-\kappa) \right) \end{aligned} \tag{6.59}$$

The stack energy equations have now become significantly more complex. We can however split the energy balancing problem into two: in the previous energy drift equations ((6.52) to (6.55)) it was found that a positive energy drift in the outer stacks was matched by a negative energy drift of equal magnitude in the inner stacks. We can therefore begin by considering the rebalancing of the top (E_{oi}^+) and bottom (E_{oi}^-) energy mismatches between the stacks. The equations for these mismatches are provided in (6.60) and (6.61).

The nominal operating point for the square-wave is with a duty-cycle equal to one half ($\lambda = \frac{1}{2}$), which is to say the square-wave is symmetric. At this operating point the equations simplify significantly and the top and bottom energy mismatches can be rebalanced by controlling the loop currents $I_e^{+,-}$ and the magnitude of the AC waveform (V_e). The loop current I_L will also affect the energy rebalancing. This current however is

primarily to be used to rebalance the second aspect of the energy balancing problem, as a change in I_L will affect both stack pairs equally.

$$\begin{aligned} E_{oi}^{+} &= E_{o}^{+} - E_{i}^{+} \\ &= T_0 \left(V_{d1} I_{d1} (1-\kappa) - 2V_e (I_e^{+} + I_L) \right) \\ &\quad + T_0 (1-2\lambda) \left(V_e I_{d1} \left(2 - \frac{1}{\kappa} \right) + \frac{V_{d1}}{2} (I_e^{+} + I_L)(2\kappa - 1) \right) \end{aligned} \tag{6.60}$$

$$\begin{aligned} E_{oi}^{-} &= E_{o}^{-} - E_{i}^{-} \\ &= T_0 \left(V_{d1} I_{d1} (1-\kappa) - 2V_e (I_e^{-} + I_L) \right) \\ &\quad + T_0 (1-2\lambda) \left(-V_e I_{d1} \left(2 - \frac{1}{\kappa} \right) - \frac{V_{d1}}{2} (I_e^{-} - I_L)(2\kappa - 1) \right) \end{aligned} \tag{6.61}$$

The second aspect of the energy problem is the necessity to ensure that the total energy in each stack pair is the same. Such an energy mismatch could typically occur due to transient events and may not be a problem during steady-state operation. Nonetheless an effective rebalancing mechanism for such a case is important.

The first step in defining the stack pair energy mismatch is to define the total energy in each stack pair as described in (6.62) and (6.63). From these equations it can be noted that the total energy of each stack pair can only be changed by varying λ away from its nominal value of $\frac{1}{2}$. The stack pair energy mismatch (E^{+-}) can then be defined as the difference between the total stack pair energies as shown in (6.64).

This equation illustrates that both the AC voltage magnitude (V_e) and the loop current magnitude I_L could be used to shift energy between the stack pairs. The difference in loop currents $I_e^{+} - I_e^{-}$ will affect the energy mismatch. Nominally this difference will be zero however and therefore will have little effect.

The energy balancing mechanisms described in this section are relatively complex with three balancing currents and one voltage magnitude to be controlled. Furthermore the duty cycle for the AC waveform (λ) has to also be regulated to affect the stack pair-to-pair balancing. All variables will inadvertently affect the cell stack energy balances but do so in a linear fashion. This means that despite the large number of control variables available a linear controller can be used, which makes the controller significantly simpler than a non-linear one.

$$\begin{aligned} E^{+} &= E_{o}^{+} + E_{i}^{+} \\ &= T_0 (1-2\lambda) \left(\frac{V_e I_{d1}}{\kappa} - \frac{V_{d1}}{2} \left(I_e^{+} + I_L \right) \right) \end{aligned} \tag{6.62}$$

$$
\begin{aligned}
E^{-} &= E_o^{-} + E_i^{-} \\
&= T_0(1-2\lambda)\left(-\frac{V_e I_{d1}}{\kappa} + \frac{V_{d1}}{2}\left(I_e^{-} - I_L\right)\right)
\end{aligned} \tag{6.63}
$$

$$
\begin{aligned}
E^{+-} &= E^{+} - E^{-} \\
&= T_0(1-2\lambda)\left(\frac{2V_e I_{d1}}{\kappa} - \frac{V_{d1}}{2}\left(I_e^{+} - I_e^{-}\right) - V_{d1} I_L\right)
\end{aligned} \tag{6.64}
$$

6.2 Alternative DC/DC Circuit Topologies With Intermediate AC Step

Previous chapters explored to some extend the use of an intermediate AC conversion step to generate an overall DC/DC voltage step. Incorporating such an intermediate step allows the use of transformers to contribute to the overall step-ratio. As transformers can typically be built with very high efficiencies such circuit topologies may be more efficient than direct conversion alternatives. Furthermore the galvanic isolation provided by the magnetic circuit also means that the two DC networks connected together through the DC/DC converter can be decoupled from each other. This can simplify the fault propagation prevention measures of a converter.

As the AC step is completely internal to the converter we can also move away from the "typical" AC waveforms used in high power systems. Both the wave-shape and the frequency can be chosen based on engineering trade-offs rather than grid-codes. Consequently we introduce two circuit topologies in this section, both of which incorporate such an intermediate square-wave AC step and utilise a transformer.

6.2.1 Shunt Connected Primary

In this circuit topology we utilise two stacks of cells to form a phase leg connected between the HV1 DC terminals, as shown in figure 6.12. The stacks are used to generate an AC square-wave at the mid-point between the stacks. The primary winding of a single-phase transformer is connected between the mid-point of the stacks and the mid-point of the split HV1 DC side capacitors (effectively neutral). On the secondary side of the transformer a rectifier converts the square-wave into DC again.

The use of square-waves allows this circuit to be of a single phase design (as opposed to the typical three phase DC/AC converter design) whilst keeping the HV2 filter requirements to a minimum.

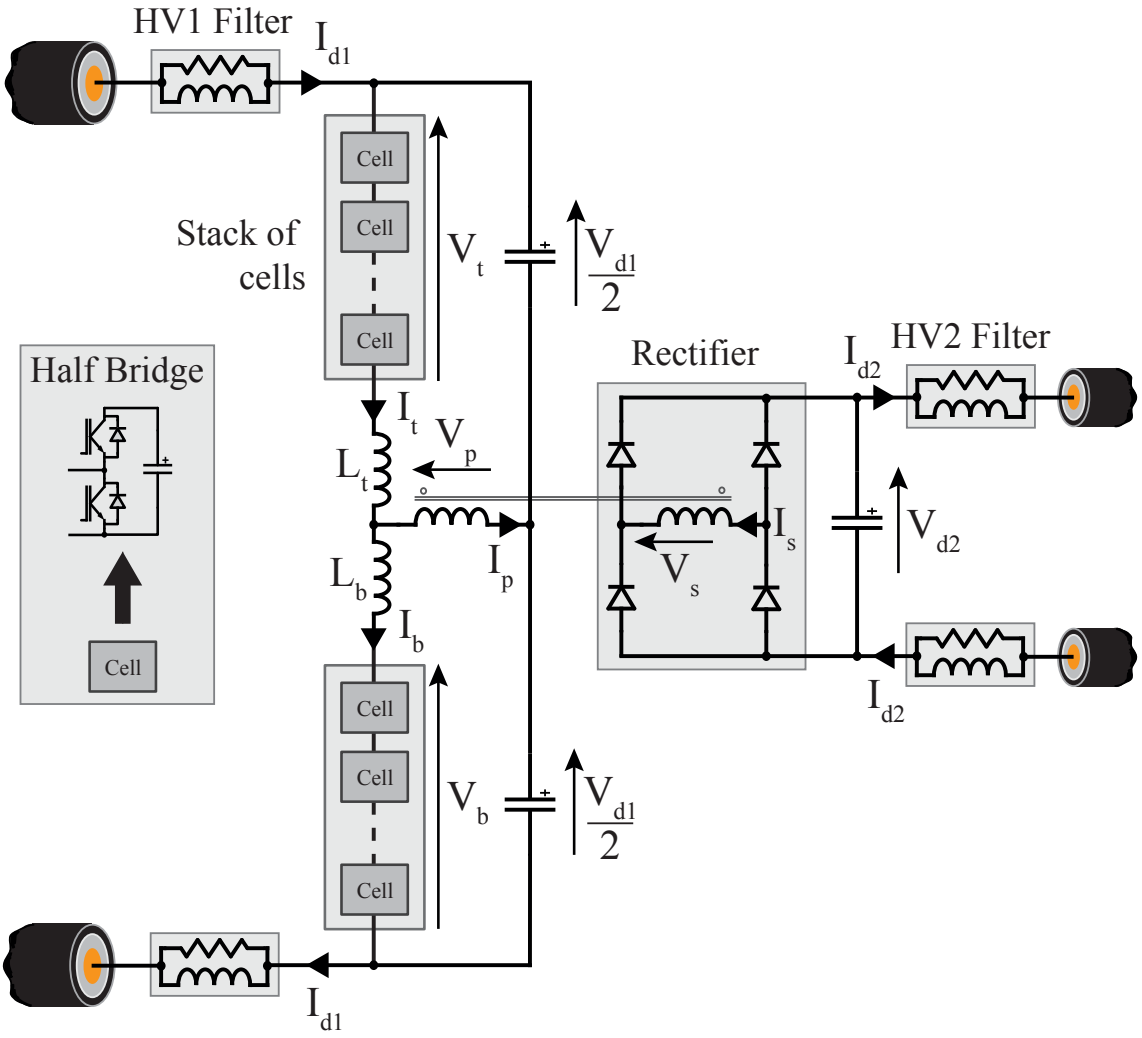

Figure 6.12: DC/AC/DC circuit with galvanic isolation and a shunt connected primary

The arm inductors $L_{t,b}$ are used to limit the rate of change of the arm currents ($I_{t,b}$) and enable the cell stacks to control them.

Voltage and Current equations

Describing the voltages and currents in the system we start by defining the AC waveform applied across the primary as per (6.65) and (6.66).

$$V_p(t) = \hat{V}_p \cdot \text{sqw}\left(\frac{t}{T_0}\right) \tag{6.65}$$

$$I_p(t) = \hat{I}_p \cdot \text{sqw}\left(\frac{t}{T_0}\right) \tag{6.66}$$

$$\therefore \text{ sqw}\left(\frac{t}{T_0}\right) = \begin{cases} 1 & \text{if } 0 \leq t < \frac{T_0}{2}, \\ -1 & \text{if } \frac{T_0}{2} \leq t < T_0. \end{cases}$$

The voltages across the cell stacks can thus be defined as shown in (6.67). While the total voltage across both stacks never exceeds the HV1 DC link voltage, the total voltage capability of the stacks has to be larger to support the peak AC voltage magnitude as well as half of the HV1 link's voltage.

$$\begin{aligned} V_t(t) &= \frac{V_{d1}}{2} - V_p(t) \\ V_b(t) &= \frac{V_{d1}}{2} + V_p(t) \end{aligned} \tag{6.67}$$

The primary current as defined in (6.66) is split equally between both arms and circulates back through the DC link capacitors. Furthermore, to draw power from the HV1 link a DC current flows through both cell stacks. The equations for the arm currents are shown in (6.68) and (6.68).

$$\begin{aligned} I_t(t) &= I_{d1} + \frac{I_p(t)}{2} \\ I_b(t) &= I_{d1} - \frac{I_p(t)}{2} \end{aligned} \tag{6.68}$$

By generating an AC voltage waveform (as per (6.67)) with a magnitude less than $\frac{V_{d1}}{2}$ the cell stacks can provide an effective DC voltage step (κ_s), as defined in (6.69) and (6.70). The transformer step ratio (κ_t) links the primary and secondary voltages and currents as per (6.71) and (6.72). The rectifier will convert the AC secondary voltage and current into DC as defined by (6.73) and (6.74). We can therefore define an overall converter step-ratio using the individual step-ratios of the stacks and the transformer as written in (6.74) and

(6.75).

$$\hat{V}_p = \kappa_s V_{d1} \tag{6.69}$$
$$\hat{I}_p = \frac{I_{d1}}{\kappa_s} \tag{6.70}$$

$$\hat{V}_s = \kappa_t \hat{V}_p \tag{6.71}$$
$$\hat{I}_s = \frac{\hat{I}_p}{\kappa_t} \tag{6.72}$$

$$V_{d2} = \hat{V}_s \tag{6.73}$$
$$I_{d2} = \hat{I}_s$$

$$V_{d2} = \kappa_t \kappa_s V_{d1} \tag{6.74}$$
$$I_{d2} = \frac{I_{d1}}{\kappa_t \kappa_s} \tag{6.75}$$

Cell stack energy balancing mechanism

The energy equations of the two cell stacks are shown in (6.76) and (6.77) . The equations take the AC component of the arm currents into account already as they form an integral part of the circuit operating mechanism to transfer power across from one DC link to the other.

Using the voltage and current definitions in (6.69) and (6.69), it can be noted that the stacks experience no energy drift under nominal conditions. This implies that during steady-state conditions the cell stacks are "self-balancing". To be able to cope with transient energy imbalances in the stacks the circuit does however require a mechanism to shift

energy from one cell stack to the other.

$$\begin{aligned}
E_t &= \int_0^{T_0} V_t(t) I_t(t) \mathrm{d}t \\
&= \left[t \left(\frac{V_{d1}}{2} - \hat{V}_p \right) \left(I_{d1} + \frac{\hat{I}_p}{2} \right) \right]_0^{\frac{T_0}{2}} \\
&\quad + \left[t \left(\frac{V_{d1}}{2} + \hat{V}_p \right) \left(I_{d1} - \frac{\hat{I}_p}{2} \right) \right]_{\frac{T_0}{2}}^{T_0} \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} \right) \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\kappa_s V_{d1} I_{d1}}{2\kappa_s} \right) \\
&= 0
\end{aligned} \tag{6.76}$$

$$\begin{aligned}
E_b &= \int_0^{T_0} V_b(t) I_b(t) \mathrm{d}t \\
&= \left[t \left(\frac{V_{d1}}{2} + \hat{V}_p \right) \left(I_{d1} - \frac{\hat{I}_p}{2} \right) \right]_0^{\frac{T_0}{2}} \\
&\quad + \left[t \left(\frac{V_{d1}}{2} - \hat{V}_p \right) \left(I_{d1} + \frac{\hat{I}_p}{2} \right) \right]_{\frac{T_0}{2}}^{T_0} \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} \right) \\
&= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\kappa_s V_{d1} I_{d1}}{2\kappa_s} \right) \\
&= 0
\end{aligned} \tag{6.77}$$

Such a vertical energy exchange could be achieved by modulating how the primary current is split between the top and bottom arm current paths. The primary current can be split into two components $I_p^{+,-}$ which combine at the mid-point between the cell stacks, which is illustrated in figure 6.13. As long as (6.78) holds true the way I_p is split between the top and bottom arm can be modulated around the nominal value of $\frac{1}{2}$ using the modulation variable α. The resulting equations for the stack energies are summarised in (6.79) and (6.80). Varying α away from its nominal value will induce an equal and

opposite energy drift in the cell stacks proportional to the HV1 power ($P_{d1} = V_{d1}I_{d1}$).

$$\begin{aligned} I_p(t) &= I_p^+(t) + I_p^-(t) \\ &: \; I_p^+(t) = \alpha I_p(t) \\ &: \; I_p^-(t) = (1-\alpha) I_p(t) \end{aligned} \tag{6.78}$$

$$\begin{aligned} E_t &= T_0 \left(\frac{V_{d1}I_{d1}}{2} - \alpha \hat{V}_p \hat{I}_p \right) \\ &= T_0 \left(\frac{V_{d1}I_{d1}}{2} - \alpha V_{d1} I_{d1} \right) \\ &= T_0 V_{d1} I_{d1} \left(\frac{1}{2} - \alpha \right) \end{aligned} \tag{6.79}$$

$$\begin{aligned} E_b &= T_0 \left(\frac{V_{d1}I_{d1}}{2} - (1-\alpha) \hat{V}_p \hat{I}_p \right) \\ &= T_0 \left(\frac{V_{d1}I_{d1}}{2} - \alpha V_{d1} I_{d1} \right) \\ &= T_0 V_{d1} I_{d1} \left(\alpha - \frac{1}{2} \right) \end{aligned} \tag{6.80}$$

Relative to the energy balancing mechanisms discussed in the direct conversion DC/DC circuits, the shunt connected primary DC/DC topology has a relatively straight forward balancing arrangement. For one this is because the intermediate step is already an integral part of the circuit design and therefore it already includes two energy transfers from each stack. Also there are only two series connected cell stacks which limits the number of necessary stack-to-stack energy exchanges required for stable operation.

6.2.2 Series Connected Primary

This circuit topology is a variation of the previous shunt connected primary DC/DC circuit. It also consists of two cell stacks connected between the HV1 DC terminals and a transformer connected to a rectifier on the secondary side, as illustrated in figure 6.14. The main difference in this circuit is that the primary is now connected between the two stacks which means that the primary voltage is now completely floating with no direct neutral connection.

The cell stacks are used to generate a square-wave voltage across and a square-wave current through the primary. In the circuit diagram the arm inductors $L_{t,b}$ are shown in series with the primary. Considering that the transformer will contain a certain amount

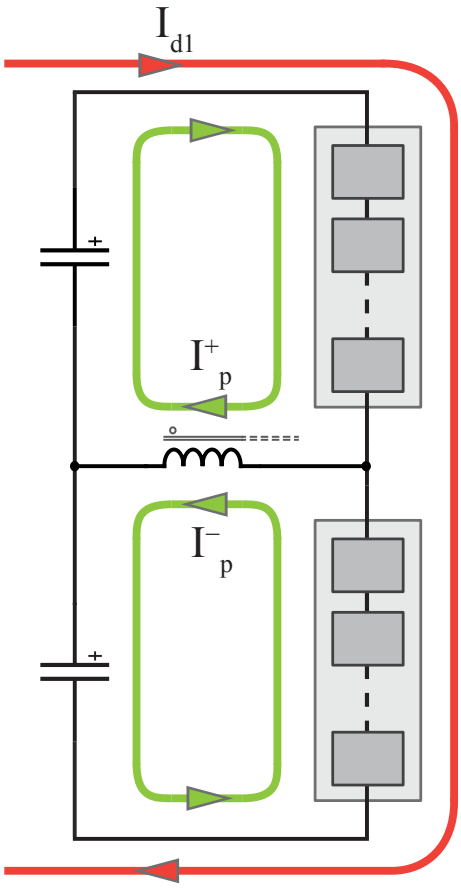

Figure 6.13: Current loops in shunt connected primary DC/AC/DC converter.

of leakage inductance, including separate arm inductors may prove unnecessary. Only the absolute inductance in the current-path is important, aso as to limit the rise time of the current and allow the cell stacks to control the arm currents effectively.

Voltage and Current equations

Figure 6.15 illustrates the operating principle of the stacks and which voltages they need to generate. The voltage expressions for the stacks can be seen in (6.81) and (6.82) along with a definition of the primary voltage in (6.83).

$$V_t(t) = \frac{V_{d1}}{2} - \frac{V_p(t)}{2} \tag{6.81}$$

$$\begin{aligned} V_b(t) &= \frac{V_{d1}}{2} - \frac{V_p(t)}{2} \\ &= V_t(t) \end{aligned} \tag{6.82}$$

$$\begin{aligned} V_p(t) &= \hat{V}_p \,\mathrm{sqw}\left(\frac{t}{T_0}\right) \\ &\therefore \mathrm{sqw}\left(\frac{t}{T_0}\right) = \begin{cases} 1 & \text{if } 0 \le t < \frac{T_0}{2}, \\ -1 & \text{if } \frac{T_0}{2} \le t < T_0. \end{cases} \end{aligned} \tag{6.83}$$

As the primary current flows through both stacks we need only define it and no other arm currents as per (6.84).

$$I_p(t) = I_{d1} + \hat{I}_p \,\mathrm{sqw}\left(\frac{t}{T_0}\right) \tag{6.84}$$

If the primary voltage magnitude ($\hat{V}_p$) is smaller than $\frac{V_{d1}}{2}$ the cell stacks effectively generate a step-ratio (κ_s). We can thus define the primary voltage in terms of κ_s and the HV1 voltage and current (V_{d1} and I_{d1}) as per (6.85) and (6.86). The transformer can also provide a step-ratio (κ_t) linking the primary and secondary voltages ((6.87)) and currents ((6.88)). The rectifier will generate the HV2 voltage and current as per (6.89) and (6.90). We can therefore define HV2 in terms of HV1 and the step-ratios ((6.91) and (6.92)).

$$\hat{V}_p = \kappa_s V_{d1} \tag{6.85}$$

$$\hat{I}_p = \frac{I_{d1}}{\kappa_s} \tag{6.86}$$

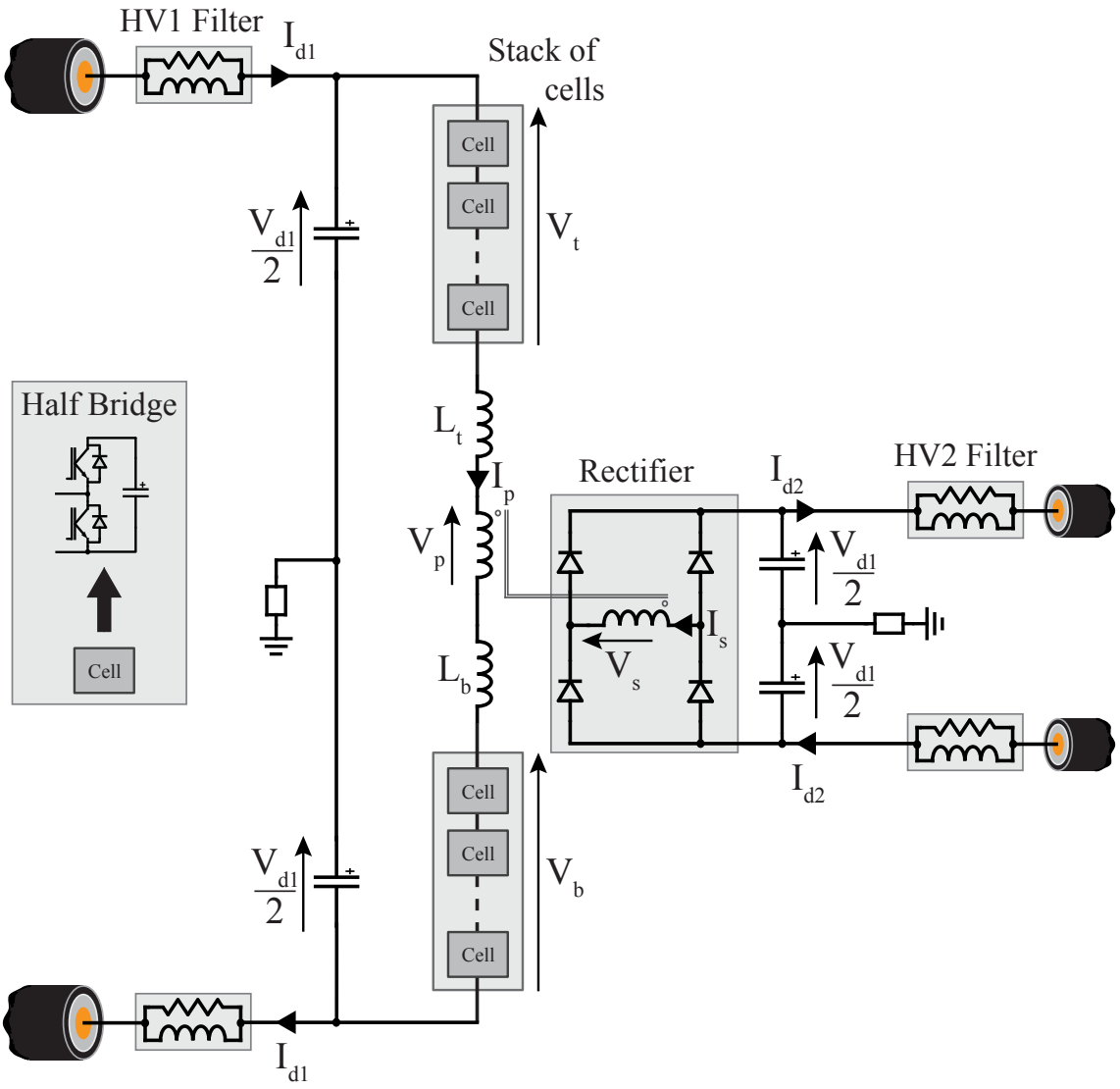

Figure 6.14: DC/AC/DC circuit with galvanic isolation and a series connected primary.

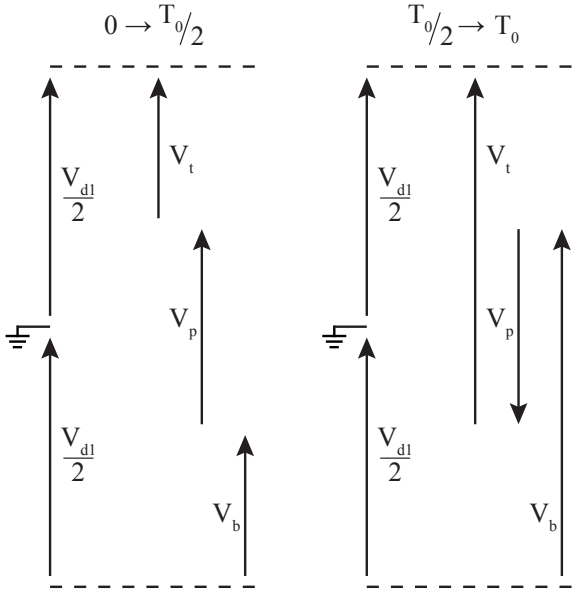

Figure 6.15: Diagram illustrating how the primary voltage is generated by the cell stacks in the series connected primary DC/AC/DC converter.

$$\hat{V}_s = \kappa_t \hat{V}_p \tag{6.87}$$

$$\hat{I}_s = \frac{\hat{I}_p}{\kappa_t} \tag{6.88}$$

$$V_{d2} = \hat{V}_s \tag{6.89}$$

$$I_{d2} = \hat{I}_s \tag{6.90}$$

$$V_{d2} = \kappa_s \kappa_t V_{d1} \tag{6.91}$$

$$I_{d2} = \frac{I_{d1}}{\kappa_s \kappa_t} \tag{6.92}$$

Cell stack energy balancing mechanism

The energy equations for both cell stacks are shown in (6.93) and (6.94). As before, the AC current is an integral component of the power conversion mechanism in the converter and is therefore included in the most basic energy equation. Using the voltage and current definitions in (6.85) and (6.86) the energy balances can be simplified and can be noted to equal zero. This implies that during steady-state operation we can expect the stacks to

remain energy balanced regardless of the step-ratio.

$$\begin{aligned} E_t &= \int_0^{T_0} V_t(t) I_p(t) \mathrm{d}t \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} \right) \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\kappa_s V_{d1} I_{d1}}{2\kappa_s} \right) \\ &= 0 \end{aligned} \tag{6.93}$$

$$\begin{aligned} E_b &= \int_0^{T_0} V_b(t) I_p(t) \mathrm{d}t \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} \right) \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\kappa_s V_{d1} I_{d1}}{2\kappa_s} \right) \\ &= 0 \end{aligned} \tag{6.94}$$

To deal with energy imbalances caused by transient events we must however also be able to shift energy from stack to stack. This is presently not possible ($E_t - E_b = 0$) as there are no variables that can be used to affect a change in the difference between the energy of the top and bottom stack.

In previous circuits we introduced an additional circulating current to exchange energy between different stacks. In this circuit a modulated current (effectively an AC current) would also affect the secondary current of the transformer as it would pass through the primary winding. This makes such an option unsuitable for the series primary DC/DC converter.

Instead we can add a DC voltage offset to the stack voltages (V_e) and modulate its magnitude and polarity to effectively exchange energy between the stacks. Conceptually this will cause a slight DC voltage offset in the primary voltage relative to ground, as illustrated in figure 6.16. Since the primary is however floating, adding the same offset to both stacks will ensure that the voltage across the primary remains unchanged. Thus the operation remains unchanged also but the transformer may require a slightly increased DC insulating capability. This can be kept relatively small however as this energy balancing mechanism is only expected to correct slight energy drifts due to transient events, which keeps the value of V_e possibly as small as the voltage across a single cell. This in turn minimises the switching losses associated with the generation of the balancing voltage.

The stack equations with the balancing voltage offset are shown in (6.95) and (6.96). The resulting stack energy equations are summarised in (6.97) and (6.98). Equation (6.99) illustrates the difference between the stack energies can be corrected by proportionally modulating the offset voltage V_e.

$$V_t(t) = \frac{V_{d1}}{2} - \frac{V_p(t)}{2} + V_e \tag{6.95}$$

$$V_b(t) = \frac{V_{d1}}{2} - \frac{V_p(t)}{2} - V_e \tag{6.96}$$

$$\begin{aligned} E_t &= \int_0^{T_0} V_t(t) V_p(t) \mathrm{d}t \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} + V_e I_{d1} \right) \end{aligned} \tag{6.97}$$

$$\begin{aligned} E_t &= \int_0^{T_0} V_t(t) V_p(t) \mathrm{d}t \\ &= T_0 \left(\frac{V_{d1} I_{d1}}{2} - \frac{\hat{V}_p \hat{I}_p}{2} - V_e I_{d1} \right) \end{aligned} \tag{6.98}$$

$$\begin{aligned} E_{tb} &= E_t - E_b \\ &= 2 T_0 V_e I_{d1} \end{aligned} \tag{6.99}$$

6.3 Discussion of Alternative DC/DC circuits

The previous two section introduced four different DC/DC circuits and explained how they may be made to work. What remains is to find some common denominators of all four topologies and use those to compare them against each other. The power rating of the cell stacks can be used to gauge how the circuits compare to one and other in size. The cell stacks form a significant portion of the total converter volume and cost. A smaller apparent power rating therefore indicates a more cost effective converter where the silicon of the semiconductors has a higher utilisation.

Depending on the application, the possibility of the converter to block DC faults from propagating may also be of importance. This section will take an initial qualitative look at the plausible fault responses of the circuits. Using all of this information we will finally look at which applications the circuits might be best suited for.

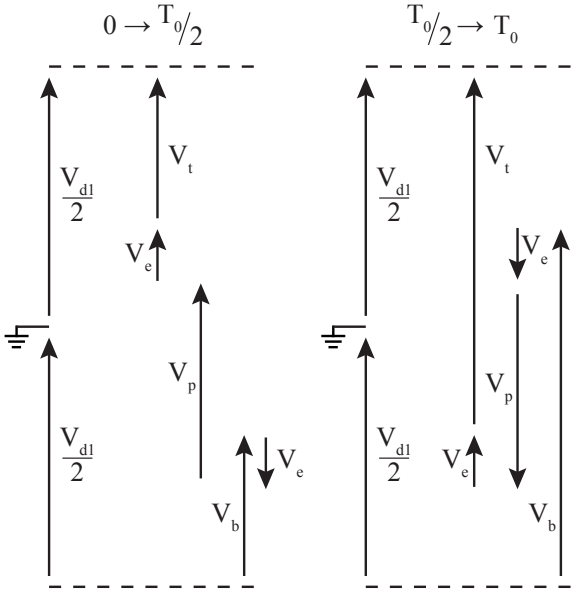

Figure 6.16: Diagram illustrating how the balancing voltage is used in the series connected primary DC/AC/DC converter.

6.3.1 Total Apparent Power Rating

The cell stacks in the converters will need to be rated for a certain voltage and current. In turn the semiconductor devices need to be rated for at least the peak value of each. The apparent power rating (S) of the cell stack can thus be defined the product of the peak voltage and current. By summing the absolute apparent power ratings of all cell stacks in any one circuit we can find expressions for the converter's apparent power rating (S_Σ).

In the following sets of equations the apparent power ratings for the four circuits presented in this chapter are laid in detail. From the previous voltage and current definitions of the circuits we know that the voltage and current equations tend to be symmetrical. It is therefore not necessary to calculate the apparent power rating of each stack.

Both of the direct conversion circuits were shown to require energy balancing AC voltages and currents (V_e and I_e). Since these are required to rebalance a significant energy drift incurred in all stacks, they will be of significant magnitude and are therefore included in the peak ratings used below. As they may be sized differently for different circuits their variables are annotated with a subscript cn where the n denotes the circuit number. The latter is derived from the order in which the circuits were presented in this chapter, starting with the direct conversion circuits.

The first set of equations ((6.100) to (6.106)) describe the apparent power required in

the top and bottom cell stacks of phase A in the parallel output pole direct conversion DC/DC (circuit 1). Equation (6.100) can be simplified using the definitions in (6.103) and (6.104) to yield the expression shown in (6.101). The equation (6.104) can be found from the energy equations in the previous section. The balancing current magnitude ($\hat{I}_e$) can be chosen freely provided that (6.104) is satisfied. By defining the balancing current's magnitude in terms of the HV1 DC current (I_{d1}), as per (6.105), we can simplify the stack's apparent power equation to (6.102).

Using the same definitions for the bottom stack, its apparent power rating can be found as per (6.106). As the voltage and current definitions were found to be symmetric we can use the same expressions for phase B as for phase A. The equations for both the stacks can be combined to find the total apparent power rating of the converter as shown in (6.107). This equation illustrates that the total installed power rating of the semiconductors is heavily influenced by the magnitude of the balancing current as well as the step-ratio of the converter.

$$
\begin{aligned}
S_a^+ &= \left|V_a^+\right|\left|I_a^+\right| \\
&= \left(\frac{V_{d1}}{2}(1-\kappa) + \frac{(V_e)_{c1}}{2}\right)\left(\frac{I_{d1}}{2}\left(1+\frac{1}{\kappa}\right) + \left(\hat{I}_e\right)_{c1}\right) \\
&= \frac{P_1}{2}\left(\frac{\kappa}{2}\left(\frac{1}{\kappa^2}-1\right) + \frac{\left(\hat{I}_e\right)_{c1}}{I_{d1}}(1-\kappa) + \frac{(V_e)_{c1}}{2V_{d1}}\left(1+\frac{1}{\kappa}\right) + \frac{(V_e)_{c1}\left(\hat{I}_e\right)_{c1}}{2}\right) && (6.100) \\
&= \frac{P_1}{2}\left(\kappa\left(\frac{1}{\kappa^2}-1\right) + \frac{\left(\hat{I}_e\right)_{c1}}{I_{d1}}(1-\kappa) + \frac{I_{d1}}{4\left(\hat{I}_e\right)_{c1}}(1-\kappa)\left(1+\frac{1}{\kappa}\right)^2\right) && (6.101) \\
&= \frac{P_1}{2}\left(\kappa\left(\frac{1}{\kappa^2}-1\right) + \epsilon(1-\kappa) + \frac{1}{4\epsilon}(1-\kappa)\left(1+\frac{1}{\kappa}\right)^2\right) && (6.102)
\end{aligned}
$$

$$
\begin{aligned}
&: P_1 = V_{d1}I_{d1} && (6.103) \\
&: \frac{(V_e)_{c1}\left(\hat{I}_e\right)_{c1}}{2} = \frac{P_1}{4}(1-\kappa)\left(1+\frac{1}{\kappa}\right) && (6.104) \\
&: \left(\hat{I}_e\right)_{c1} = \epsilon I_{d1}, \epsilon = (0,1] && (6.105)
\end{aligned}
$$

$$
\begin{aligned}
S_a^- &= \left|V_a^-\right| \left|I_a^-\right| \\
&= \left(\frac{V_{d1}}{2}(1+\kappa) + \frac{(V_e)_{c1}}{2}\right)\left(\left|\frac{I_{d1}}{2}\left(1-\frac{1}{\kappa}\right)\right| + \left(\hat{I}_e\right)_{c1}\right) \\
&= \frac{P_1}{2}\left(\left|\frac{\kappa}{2}\left(1-\frac{1}{\kappa^2}\right)\right| + \frac{\left(\hat{I}_e\right)_{c1}}{I_{d1}}(1+\kappa) + \left|\frac{(V_e)_{c1}}{2V_{d1}}\left(1-\frac{1}{\kappa}\right)\right| + \frac{(V_e)_{c1}\left(\hat{I}_e\right)_{c1}}{2}\right) \\
&= \frac{P_1}{2}\left(\kappa\left(\frac{1}{\kappa^2}-1\right) + \epsilon(1+\kappa) + \frac{1}{4\epsilon}(1-\kappa)\left(\frac{1}{\kappa}-1\right)\left(1+\frac{1}{\kappa}\right)\right) \qquad (6.106)
\end{aligned}
$$

$$
\begin{aligned}
(S_\Sigma)_{c1} &= S_a^+ + S_a^- + S_b^+ + S_b^- \\
&= 2\left(S_a^+ + S_a^-\right) \\
&= P_1\left(\left(\frac{1}{\kappa^2}-1\right)\left(2\kappa + \frac{1}{2\epsilon}\right) + 2\epsilon\right) \qquad (6.107)
\end{aligned}
$$

The apparent power equations for the cell stacks of the second direct conversion circuit, the series output pole DC/DC, can be derived in much the same way as for the first, as illustrated in (6.108) to (6.115). The general formula as expressed in 6.108 can be simplified using (6.111) to (6.114). The balancing mechanism of this circuit includes two currents: $I_e^{+,-}$ and I_L. As they are both used for energy balancing purposes we can group both variables into one as per (6.114). The simplified form equation is shown in (6.110).

Similarly the apparent power rating for the top inner stack (S_i^+) can be calculated as in (6.115) using the same definitions as for S_o^+. The total converter apparent power rating can then be calculated as per (6.116). The power equations for the bottom stacks ($S_{o,i}^-$) are the same as for the top two stacks assuming that the energy balancing current I_e^- is of the same magnitude as I_e^+, which under steady-state operation is the case.

The total apparent power rating can be seen to be dependent on the magnitude of the balancing current and the converter's step-ratio, similar to the parallel output's apparent power rating. In order to better judge how the two circuits compare to one and other the installed apparent power capacity per unit of converter power rating (as defined by P_1) is plotted in figure 6.17 for both circuits. This measure is also referred to as the power

capacity ratio.

$$\begin{aligned}
S_o^+ &= \left|V_o^+\right|\left|I_o^+\right| \\
&= \left(\frac{V_{d1}}{2}(1-\kappa) + (V_e)_{c2}\right)\left(I_{d1} + (I_e)_{c2}\right) \\
&= \frac{P_1}{2}(1-\kappa) + \frac{V_{d1}\left(\hat{I}_e\right)_{c2}}{2}(1-\kappa) + (V_e)_{c2}\, I_{d1} + (V_e)_{c2}\left(\hat{I}_e\right)_{c2} && (6.108) \\
&= \frac{P_1}{2}\left(2(1-\kappa) + \frac{\left(\hat{I}_e\right)_{c2}}{I_{d1}}(1-\kappa) + \frac{I_{d1}}{\left(\hat{I}_e\right)_{c2}}(1-\kappa)\right) && (6.109) \\
&= \frac{P_1}{2}\left(2(1-\kappa) + \epsilon(1-\kappa) + \frac{1}{\epsilon}(1-\kappa)\right) && (6.110)
\end{aligned}$$

$$\begin{aligned}
&: P_1 = V_{d1} I_{d1} && (6.111) \\
&: (V_e)_{c2}\left(\hat{I}_e\right)_{c2} = \frac{P_1}{2}(1-\kappa) && (6.112) \\
&: \left(\hat{I}_e\right)_{c2} = \epsilon I_{d1}, \epsilon = (0,1] && (6.113) \\
&: \left(\hat{I}_e\right)_{c2} = \left(\hat{I}_e^+ + I_L\right)_{c2} && (6.114)
\end{aligned}$$

$$\begin{aligned}
S_i^+ &= \left|V_i^+\right|\left|I_i^+\right| \\
&= \left(\frac{\kappa V_{d1}}{2} + (V_e)_{c2}\right)\left(\left|I_{d1}\left(1 - \frac{1}{\kappa}\right)\right| + (I_e)_{c2}\right) \\
&= \frac{P_1}{2}\left((1-\kappa) + \frac{\left(\hat{I}_e\right)_{c2}}{I_{d1}}\kappa + \frac{I_{d1}}{\left(\hat{I}_e\right)_{c2}}\left(\frac{1}{\kappa} - 1\right)(1-\kappa) + (1-\kappa)\right) \\
&= \frac{P_1}{2}\left(2(1-\kappa) + \epsilon\kappa + \frac{1}{\epsilon}(1-\kappa)\left(\frac{1}{\kappa} - 1\right)\right) && (6.115)
\end{aligned}$$

$$\begin{aligned}
(S_\Sigma)_{c2} &= S_o^+ + S_i^+ + S_i^- + S_o^- \\
&= 2\left(S_o^+ + S_i^-\right) \\
&= P_1\left(\epsilon + (1-\kappa)\left(4 + \frac{1}{\epsilon\kappa}\right)\right) && (6.116)
\end{aligned}$$

The diagrams (figure 6.17) show the power capacity ratio of both circuits relative to the converter's step ratio (κ) and the magnitude of the balancing current relative to I_{d1} (ϵ). The parallel output pole appears to suffer from a particularity large power capacity ratio as the step-ratio increases ($\kappa \to 0$). Reducing the balancing current's magnitude increases

this further. For the series connected output pole circuit (shown in bottom diagram) the power capacity ratio also increases with respect to an increasing step-ratio. A larger ϵ will in this case also lead to a lower power capacity ratio, indicating that a larger balancing current magnitude yields a better semiconductor utilisation.

At lower step ratios ($\kappa \to 1$) both direct conversion circuits tend towards a power capacity ratio of 0. As the step ratio approaches 1:1, stacks that carry the DC current tend towards a zero voltage whilst at the same time the stacks that generate the link voltage tend towards zero DC current. This trend is shown in figure 6.18 for $\epsilon = 1$ which has been seen to minimise the power capacity ratio for larger step ratios.

The apparent power ratings for the cell stacks of the DC/AC/DC circuit with shunt primary connection are shown in equations (6.117) to (6.118). The equations as presented in (6.117) can be simplified using (6.119) and (6.120) into the expression shown in (6.118). As there are only two stacks with the same peak voltage and current ratings in this circuit topology the total apparent power rating can be expressed as shown in (6.121). As the total converter step-ratio of this topology is split into the step-ratio applied by the cell stacks and the transformer step-ratio, only the former is present in the expressions. Varying the transformer step-ratio will have no impact on the apparent power rating of the cell stacks.

The equation for the apparent power rating of the top cell stack in the DC/AC/DC with series primary connection, as seen in (6.122), was also derived by using the definitions in (6.119) and (6.120). Similarly to the shunt connected DC/AC/DC circuit the cell stacks share the same peak voltages and currents which allows the expression for the total apparent power rating to be expressed as shown in (6.123). The voltage relevant for the mechanism which allows energy to be exchanged between the cell stacks, has been omitted from these expressions to simplify the comparison between the circuits. The energy that has to be rebalanced in this manner is typically small. This implies that the additional voltage capability required of the cell stacks will also be small relative to the size of the

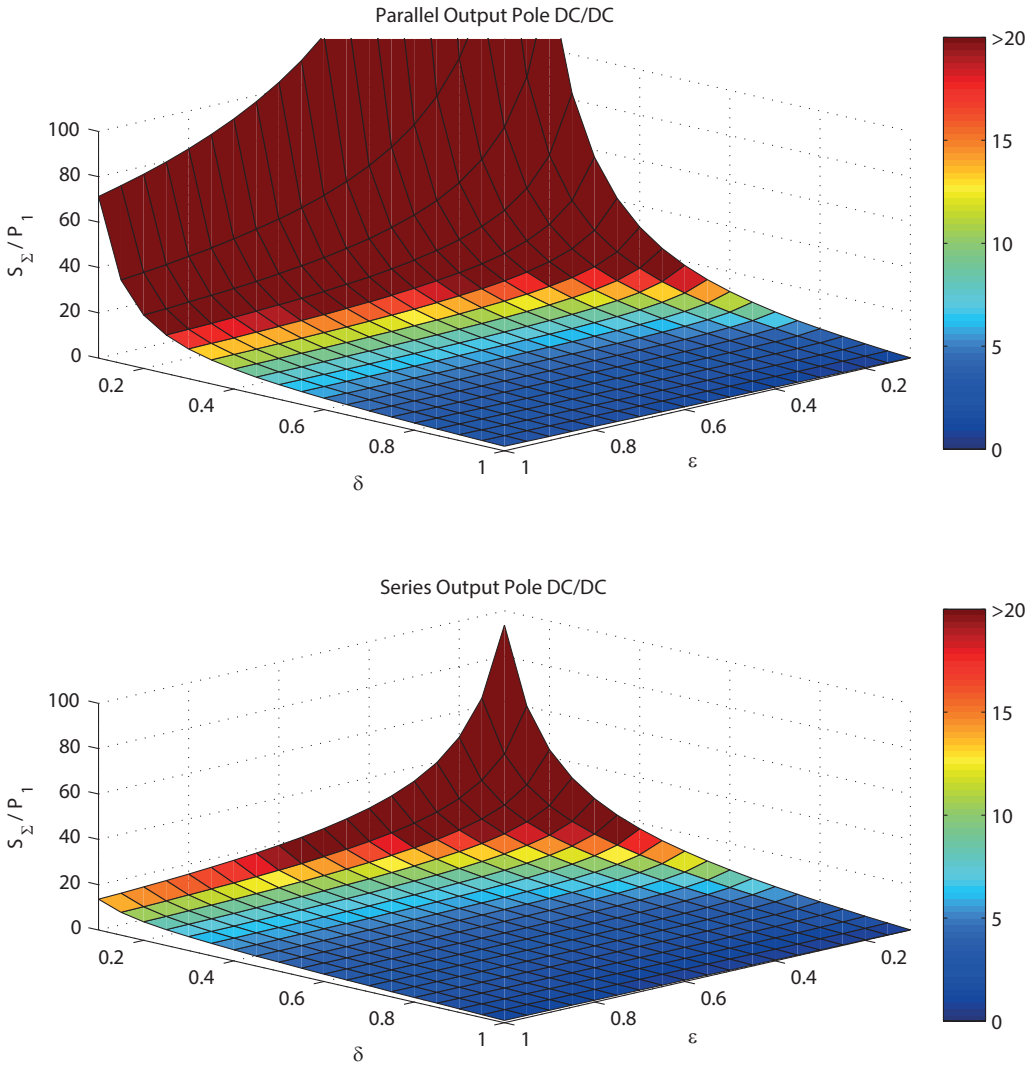

Figure 6.17: Capacity ratio of direct conversion DC/DC converters.

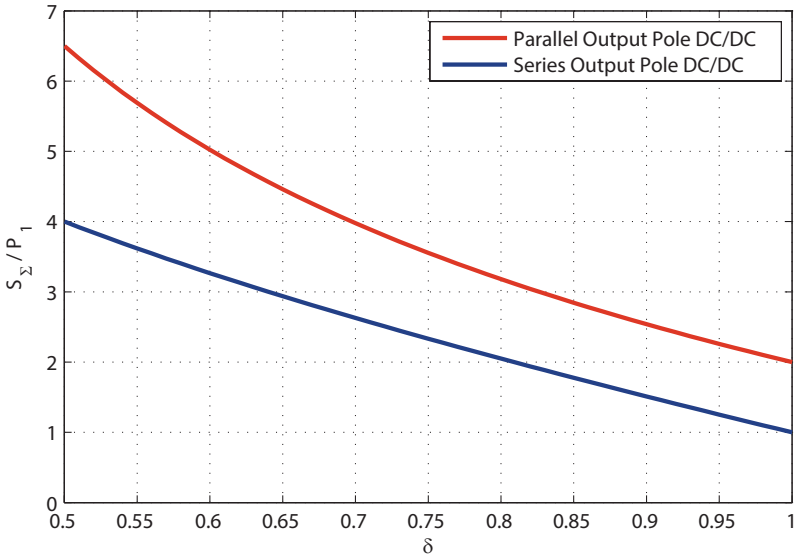

Figure 6.18: Capacity ratio of direct conversion DC/DC converters with $\epsilon = 1$, focused around low step-ratios.

peak cell stack voltage and will thus not greatly impact the power capacity ratio.

$$\begin{aligned} S_t &= \left|\hat{V}_t\right| \left|\hat{I}_t\right| \\ &= \left(\frac{V_{d1}}{2} + \kappa_s V_{d1}\right)\left(I_{d1} + \frac{\hat{I}_p}{2}\right) \qquad (6.117) \\ &= V_{d1} I_{d1} \left(\frac{1}{2} + \kappa_s\right)\left(1 + \frac{1}{2\kappa_s}\right) \\ &= P_1 \left(1 + \kappa_s + \frac{1}{4\kappa_s}\right) \qquad (6.118) \end{aligned}$$

$$\therefore \hat{I}_p = \frac{I_{d1}}{\kappa_s} \qquad (6.119)$$

$$\therefore P_1 = V_{d1} I_{d1} \qquad (6.120)$$

$$\begin{aligned} (S_\Sigma)_{c3} &= S_t + S_b \\ &= 2S_t \\ &= 2P_1 \left(1 + \kappa_s + \frac{1}{4\kappa_s}\right) \qquad (6.121) \end{aligned}$$

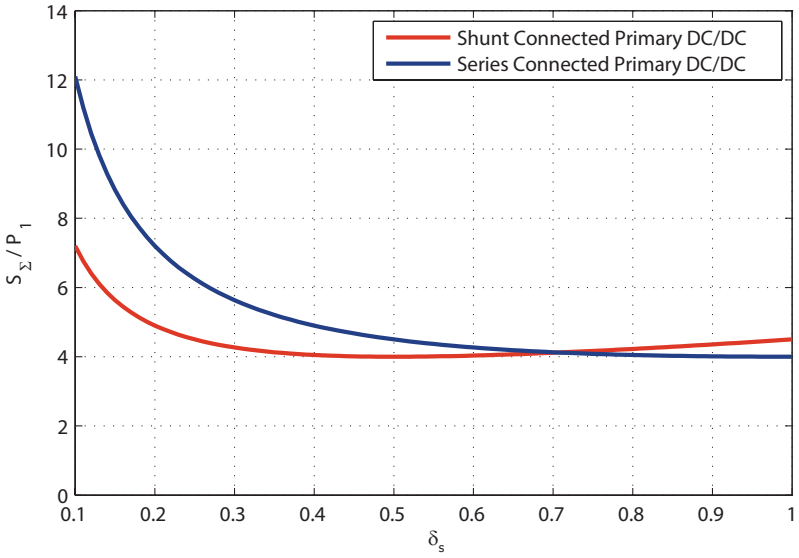

Figure 6.19: Capacity ratio of DC/DC converters with intermediate AC step.

$$\begin{aligned} S_t &= \left|\hat{V}_t\right| \left|\hat{I}_t\right| \\ &= \left(\frac{V_{d1}}{2} + \frac{\kappa_s V_{d1}}{2}\right)\left(I_{d1} + \hat{I}_p\right) \\ &= \frac{P_1}{2}\left(2 + \kappa_s + \frac{1}{\kappa_s}\right) \end{aligned} \tag{6.122}$$

$$\begin{aligned} (S_\Sigma)_{c4} &= S_t + S_b \\ &= 2S_t \\ &= P_1\left(1 + \kappa_s + \frac{1}{4\kappa_s}\right) \end{aligned} \tag{6.123}$$

The expressions for the total apparent power rating for both DC/AC/DC circuits presented in this chapter can be used to display the power capacity ratio for a range of cell stack step-ratios, as illustrated in figure 6.19. From the diagram it can be noted that the shunt connected primary circuit has a lower power capacity ratio at step ratios above $10:7$ ($\kappa_s < 0.7$) and has a minimum at $\kappa_s = \frac{1}{2}$. The series connected DC/AC/DC performs worse at cell stack step-ratios $\kappa_s < 0.7$ and slightly better at lower ones.

As the transformer can also apply a significant step ratio in the DC/AC/DC topologies, these circuits could be operated at their optimal power capacity ratio and still achieve an

overall high step-ratio. Thus from a power capacity ratio point of view these circuits appear more suitable at high step-ratios ($\kappa \to 0$) than the direct conversion ones. Even when the stacks provide a step-ratio the shunt connected primary DC/AC/DC has the lowest power capacity ratio for high step-ratios. Both the series connected primary DC/AC/DC and the series output pole DC/DC have a similar performance whilst the parallel output DC/DC has the highest power capacity ratio of all four circuits.

For small step-ratios however the direct conversion circuits and in particular the series output pole DC/DC, perform significantly better. For step ratios less than $2:1$ ($\kappa > 0.5$) it consistently has a lower power capacity ratio than either DC/AC/DC topology.

6.3.2 DC Fault Tolerance

The ability of converters to help out in case of DC side faults, is very valuable as it may allow the converter to provide ancillary services or significantly reduce the need and therefore the cost of additional protection equipment. In this initial review of the circuits under fault conditions, we will consider only one scenario in which both DC lines on either side are faulted to ground.

In case of a fault on the HV1 side in the parallel output pole DC/DC circuit, the converter could not block fault currents from flowing into the fault, as illustrated in figure 6.20. This is because there are only half-bridge cells in the converter's cell stacks, making it impossible for the stacks labelled a^+ and b^- to generate the required voltage. Due to the anti-parallel diodes in the cells, this means that there exists an uncontrolled current path through which the fault current can pass.

To be able to reverse the polarity of the stack and prevent the fault current from flowing through it, they would need to contain full-bridge cells, which would double the devices in the conduction path and significantly increase the converter's power capacity ratio and losses. The changing voltage requirements for the stacks in case of faults is illustrated in figure 6.21. In the diagrams presented, only stacks for phase a are considered. As the converter is symmetrical, however, the same aspects apply to phase b.

From the diagram on the left (showing a fault on the HV1 side) it can be seen that stack a^- requires no voltage polarity change and would only need to generate a smaller voltage than during normal operation. The diagram on the right illustrates the voltage requirements for the stacks during a fault on the HV2 side: No stack has to generate voltage in the opposite direction but it can be noticed that stack a^+ needs to be able to generate a larger voltage than during normal operation. If it is equipped to do so then a HV2 side fault can be prevented from affecting the HV1 DC side. Such extra capacity

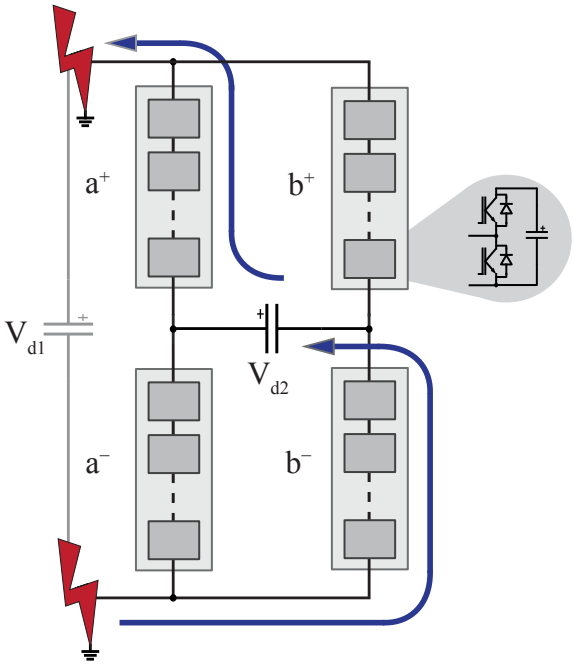

Figure 6.20: Possible fault current paths in parallel output pole DC/DC circuit in case of line-to-ground faults on HV1 side.

implies additional cells and a higher power capacity ratio as well as losses in the converter. This could be particularly noticeable at lower step-ratios ($\kappa \cong 1$) as $\hat{V}_a^+$ would typically be small and therefore require significantly more additional voltage capability.

If it does not however have this extra voltage capability, then an uncontrollable fault current would develop flowing through the stack and into the fault. As such a current would flow through the top anti-parallel diode of the half-bridge cell and start to charge up the cell capacitor. Whilst this would increase the total voltage across the stack and counteract the rise in fault current magnitude, it could quickly cause the capacitor to charge above and beyond its safe operating limit. Therefore a quick fail-safe disconnect mechanism for the cells would be required to short out the cells, protecting the cells but leaving the fault current uncontrolled.

In the case of faults on either DC side for the series output pole DC/DC converter, the required stack voltages are shown in figure 6.22. In case of a fault in the HV1 side (left diagram) the outer stacks (marked as o^+ in figure 6.23) have to be able to reverse the polarity of the voltage they generate and possibly provide a larger voltage magnitude (similar to the fault scenario discussed in the previous circuit). This implies upgrading the cells in those particular stacks to full-bridge cells, with the same negative results as

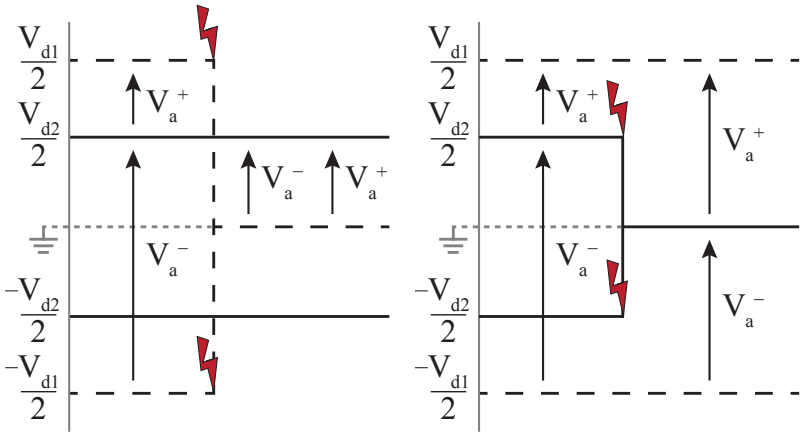

Figure 6.21: Stack voltage requirements for phase leg of parallel pole DC/DC circuit in case of faults line-to-ground faults in HV1 (left-hand side diagram) and HV2 side (right-hand side diagram).

for the previous circuit. The inner stacks (V_i^+ for instance) are not affected.

Figure 6.23 illustrates the fault current path in case the outer stacks cannot provide the required fault blocking voltages. In this case the anti-parallel diode of the bottom switch in the cells provides a path for the fault current.

On the right-hand side the diagram in figure 6.22 illustrates the increase in voltage magnitude required of the outer stacks. Under normal operation these stacks are rated for the voltage difference between the HV1 and HV2 pole voltages. At higher step-ratios ($\kappa \to 0$) this difference approaches the required voltage capability to block HV2 side faults. Thus, upgrading the voltage capability of the outer stacks to be able to cope with HV2 faults is more economical at high step-ratios, as fewer additional cells have to be added.

From this first look at the fault scenarios, it has become clear the neither direct conversion circuit topology can block a DC fault on either side, without some upgrading of the voltage capability of some of their cell stacks. As such an upgrade increases the power capacity ratio and consequently the cost and losses of the converter, it would not be trivial. Being able to prevent DC faults which occur on the higher voltage (HV1) side from propagating to the lower voltage (HV2) side appears to be the least economically feasible, as it requires an increased voltage capability as well as full-bridge cells. Blocking faults occurring on the HV2 side however seems more plausible, particularly for larger step-ratios.

The other two DC/DC topologies contain an intermediate AC link. A fault on the HV1 side will ground the primary in both circuits. The diodes on the HV2 side will prevent

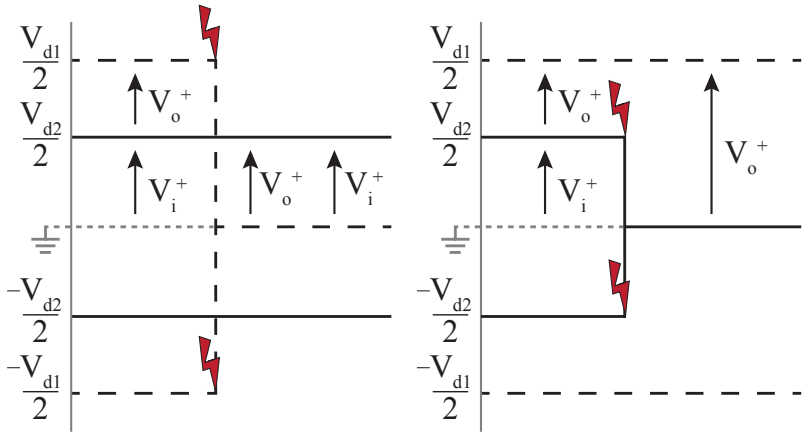

Figure 6.22: Stack voltage requirements for phase leg of series pole DC/DC circuit in case of faults line-to-ground faults in HV1 (left-hand side diagram) and HV2 side (right-hand side diagram).

any fault current from flowing from the HV2 link into the fault. In case of a fault on the HV2 side the cell stacks remain in full control of the currents as they have sufficient voltage rating to support the HV1 voltage when the transformer's secondary is grounded and therefore no voltage appears across the primary. As such the DC/AC/DC circuits seem to be ideally suited to provide protection from DC fault propagation as no upgrades to the circuit are required.

6.3.3 Suitable areas of application

Areas of application for DC/DC converters in general have been discussed early on in this work, in chapter 2. Here we consider these areas and weight up which of the presented alternative DC/DC circuits may be the most suitable for each. We begin by looking at the area of interconnecting a legacy and new DC link. For this, two particular applications for DC/DC converters are of interest.

Firstly the interconnection of VSC lines with slightly different voltage levels. Particularly as cable technology progresses the voltage level of the DC poles tends to increase. Therefore an interconnection between for example a legacy $\pm 320kV$ line and a new $\pm 500kV$ line are plausible and would require a step-ratio somewhere in between $1 \geq \kappa \geq 0.64$. The series output pole direct conversion architecture has been shown to have the lowest power capacity ration for $\kappa \geq 0.5$ and would seem the most suitable for such an application.

A significant number of the legacy links are however not of VSC but CSC technology.

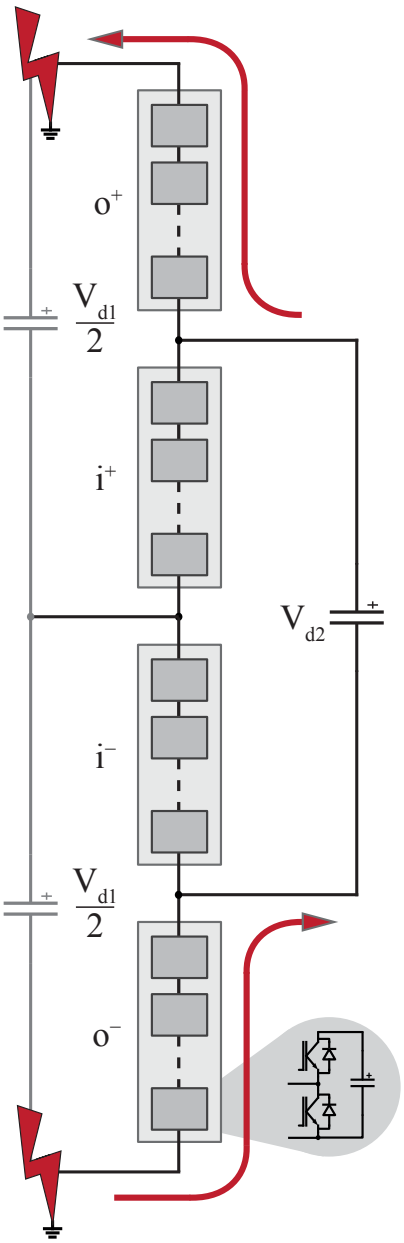

Figure 6.23: Possible fault current paths in parallel series pole DC/DC circuit in case of line-to-ground faults on HV1 side.

Since VSC technology may be favoured in the future for its suitability for multi-terminal DC networks, it may become economically feasible to interconnect some old CSC lines with newer VSC ones. Since the two technologies rely on different mechanisms to reverse a power flow, such interconnection is not trivial: a VSC retains the same voltage polarity across the line and reverses the current flow direction. CSC technology on the other hand reverses voltage polarity and maintains the same current flow direction to achieve the same effect. If one would want to achieve such a voltage polarity reversal with extensive switching equipment to reconnect the CSC poles to the converter, then the parallel output pole direct conversion circuit may be suitably modified. Since it doesn't matter whether a positive or negative voltage pole is connected to either phase leg of the circuit, a CSC connection could be made on the HV2 side, provided that its voltage is greater in magnitude than that of the HV1 side. This would however require additional voltage capability in the stacks to allow either phase to support either a positive or a negative output voltage (relative to ground).

If the DC/DC converter in these applications is to protect against DC fault propagation, then the direct conversion circuits would need to be upgraded in terms of voltage capability. It has been discussed that this may increase their power capacity ratio significantly. As the DC/AC/DC circuits presented in this chapter are already equipped to deal with faults on either DC side they may become more appealing for these applications.

For the high step-ratio ($\kappa \leq 0.5$) application area also, the circuits with an intermediate AC stage have a significantly better power capacity ratio than the direct conversion alternatives. Tapping HVDC lines to connect an en-route DC wind-farm collector grid or an AC load centre can be done more effectively using DC/DC converters, than a DC/AC stage followed by a transformer. The DC/AC/DC circuits presented in this chapter are only capable of a uni-directional power flow from the HV1 to the HV2 side. A wind-farm would require a power flow from the low- to the high-voltage side. These circuit would therefore need to be capable of bi-directional power flow. This could be achieved by using a an active rectifier for example.

6.4 Chapter Summary: New modular DC/DC converter designs

The previous three chapters have explored the use of tried and tested modular VSC technology to build a DC/DC converter. In this chapter new circuit designs are presented, which use the same modular cell technology, but new circuits to achieve a DC/DC step.

Two different types of modular converter are introduced: the direct conversion and the intermediate AC step topologies.

Two direct-conversion variants are presented, one based on a parallel arrangement on the higher voltage side, the other based on a series one. These circuits operate such that the entire transferred power is not transformed into AC. Rather an internal AC loop is used to rebalance the cells, which is means it operates at only a fraction of the transferred power rating. In these circuits the transformation ratio is achieved without the use of any magnetically coupled components.

Furthermore, two circuit variants utilising an internal AC link, like the F2F topology, have been introduced. These circuits have been designed with square voltage waveforms in mind and are intended for a higher than 50 Hz frequency operation. In some ways, they form the next evolutionary step in the F2F arrangement. A transformer provides additional capability to achieve higher step-ratios and provides galvanic isolation.

By using the power capacity ratio, a measure which indicates the total power rating of the installed power electronics normalised with the power rating of the converter, all four circuit topologies were compared against each other. The direct-conversion topologies are most suitable for relatively low step-ratios, less than 2:1. In particular the series-output pole topology provides very low capacity ratios, approaching one as the step-ratio approaches one.

The transformer-coupled variants can be optimised to a minimum power capacity-ratio of four, which equates to a transformation ratio of 2:1. The transformer then perform the rest of the stepping action. If an overall step-ratio of less than 2:1 should be required, a step-up transformer would be needed. Thus these topologies are less suitable for such step-ratios.

Finally the possibility of modifying the individual variants to provide fault propagation prevention capabilities has been discussed. In the case of the direct conversion topologies this would lead to significant increases in the power capacity ratio as additional cells would be required in the stacks. The transformer-coupled topologies seem more suitable as the DC networks can be disconnected on the internal AC link.

As the F2F topologies previously investigated, have been analysed for a low step ratio of 5:3, a topology suitable for larger step-ratios has been identified for further investigation. Since the shunt-connected transformer-coupled topology, presented in this chapter, has the better power capacity-ratio of the two, it has been chosen and will be presented in greater detail in the next two chapters.

Chapter 7

Principles of operation of square-wave modular DC/DC converter

The previous chapter compared four new circuit topologies with each other. It identified the square-wave DC/AC/DC circuit with a shunt primary connection as the most suitable converter topology for high step-ratios ($\kappa \leq 0.5$). This circuit not only achieves the lowest power-capacity ratio at high step-ratios but also contains galvanic isolation. The internal AC connection can be used to prevent DC faults from propagating across the converter to affect the other DC connection. As it utilises square-waves it lends itself for a compact, single phase design, making it particularly attractive for HVDC tapping applications.

This chapter investigates this converter topology further by introducing the control algorithm taking a look at the steady-state operation of the converter. The aim of this chapter is to provide insights into the control algorithm and operational parameters of the square-wave shunt connected primary DC/DC converter. The basic system equations were derived in section 6.2.1 and will not be reviewed again here.

7.1 Converter Controller

To be able to simulate the converter effectively a closed-loop control system is required. Such a system contains three distinct components as illustrated in figure 7.1. Since the stacks form, what can essentially be thought of as, controllable voltage sources we can use them and the inductive network they are connected to, to regulate the currents flowing

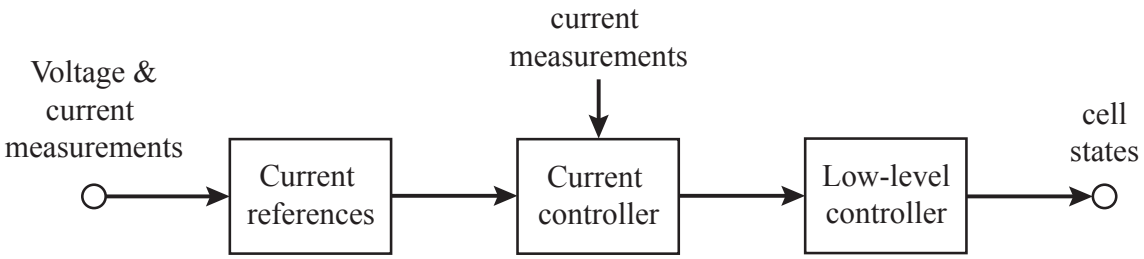

Figure 7.1: General overview of controller for square-wave modular DC/DC converter.

through the converter. The first step therefore is to create the current references we wish to track. Using these references and the current measurements from the converter, we can create references which stipulate the voltage required of each cell stack to track the currents. Lastly these signals then get translated into individual cell states which determine the output voltage across each cell, by the low level controller.

7.1.1 Current Controller

Although the current controller is the central piece of the overall control system, it determines what comes before and after it. Thus it makes sense to look at it first. The general idea behind this controller is to use the inductive network, made up of the arm inductors and the transformer, to regulate the currents flowing through the converter. This can be achieved by controlling the terminal voltages of the inductive network using the cell stacks.

We start by considering a simplified view of the inductive network as illustrated in figure 7.2. Using the current and voltage definitions outlined in (7.1) and (7.3), the state-space representation of this inductive network can be written as in (7.4).

$$U^+ = V_L^+ - V_p \tag{7.1}$$

$$U^- = V_L^- - V_p \tag{7.2}$$

$$I_p = I_t - I_b \tag{7.3}$$

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} U^+ \\ U^- \end{bmatrix} = \begin{bmatrix} L_t + L_p & -L_p \\ L_p & -L_b - L_p \end{bmatrix} \begin{bmatrix} \dot{I}_t \\ \dot{I}_b \end{bmatrix} \tag{7.4}$$

The circuit doesn't contain a separate component L_p (primary winding) but instead uses the leakage inductances of the transformer. Using the equivalent model of a single

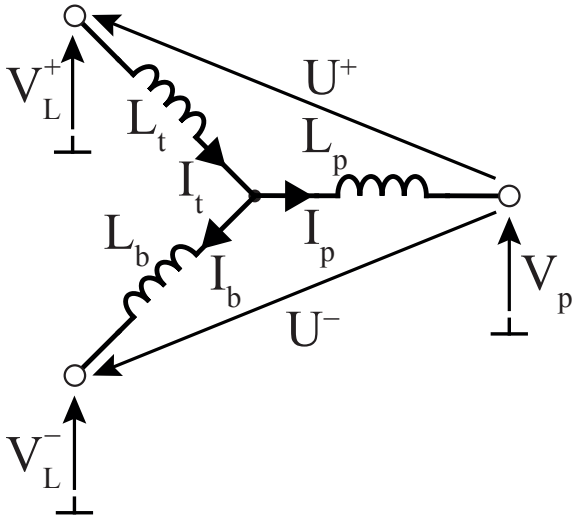

Figure 7.2: Equivalent inductive network view of square-wave modular DC/DC with shunt connected primary.

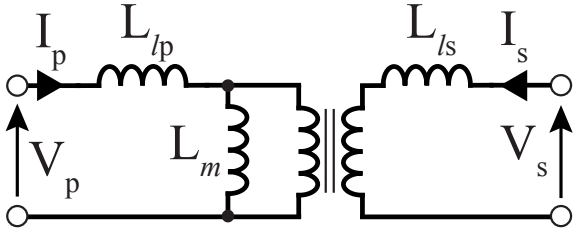

Figure 7.3: Equivalent inductive circuit for a single phase transformer.

phase transformer, as shown in figure 7.3, L_p can be replaced with expression (7.5).

$$L_p = L_{lp} + \kappa_t^2 L_{ls} \tag{7.5}$$

The state-space representation can be written in the form of a continuous linear time-invariant system ($\dot{x} = Ax + Bu$) as shown in (7.6) to (7.7).

$$\begin{bmatrix} \dot{I}_t \\ \dot{I}_b \end{bmatrix} = \mathbf{0}_{2,2} \begin{bmatrix} I_t \\ I_b \end{bmatrix} + \begin{bmatrix} L_t + L_{lp} + \kappa_t^2 L_{ls} & -L_{lp} - \kappa_t^2 L_{ls} \\ L_{lp} + \kappa_t^2 L_{ls} & -L_b - L_{lp} - \kappa_t^2 L_{ls} \end{bmatrix}^{-1} \begin{bmatrix} U^+ \\ U^- \end{bmatrix} \tag{7.6}$$

In a realistic system the controller would not operate in real time. Measurement acquisition and computational delays will mean that a realistic sampling frequency the control system would be less than 100 kHz. Therefore a discrete version of the state space

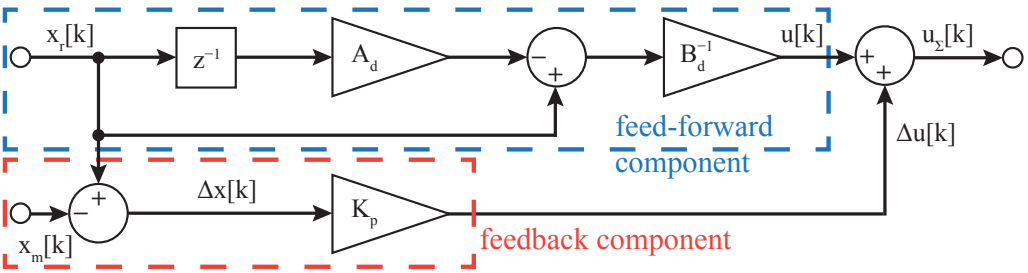

Figure 7.4: Current controller for square-wave modular DC/DC converter.

model will be more appropriate to use than a continuous time one. Using the property as described in (7.7) the state space matrices A and B can be discretised (into A_d and B_d). The variable T_{cs} denotes the sampling period of the controller.

$$e^{\begin{bmatrix} A & B \\ 0 & 0 \end{bmatrix} \cdot T_{cs}} = \begin{bmatrix} A_d & B_d \\ 0 & I \end{bmatrix} \tag{7.7}$$

The current controller itself consists of two components: a feed-forward and feedback term, as illustrated in figure 7.4. The feed-forward component uses the current references ($x_r[k]$) and the discrete system description to estimate the required voltages ($u[k]$). The feed-back component uses the current measurements ($x_m[k]$) to create an error signal ($\Delta x[k]$). Only two current measurements are required. For this work the two arm currents were chosen. The error signal in turn is fed into a Multiple-In-Multiple-Out (MIMO) proportional gain (K_p). Its output is then added to the feed-forward output. The feed-back component ensures that the current controller operates in closed-loop. It should be noted that the final outputs from the current controller ($u_\Sigma[k]$) are not stack voltages to be applied but is a vector containing the voltages $U^{+,-}$.

Linear Quadratic Regulator (LQR) theory can be used to find the gains in K_p. The gains can be found using an existing function in Matlab suitable for the computation of discrete LQR problems (function: *dlqr()*) such that the cost function (J), as per (7.8), is minimised over an infinite time horizon.

$$J = \sum_{k=0}^{\infty} \left(\underbrace{\Delta x[k]^T Q \Delta x[k]}_{J_x} + \underbrace{\Delta u[k]^T R \Delta u[k]}_{J_u} \right) \tag{7.8}$$

As there are three currents in the inductive network the cost component dependent on the currents, J_x, can be expressed as per (7.9), where $q_{t,b,p}$ refer to the costs placed on

the corresponding current errors. Using (7.3) this J_x can be expressed in terms of the arm currents as per (7.10).

$$J_x = q_t \Delta I_t^2 + q_b \Delta I_b^2 + q_p \Delta I_p^2 \tag{7.9}$$

$$= (q_t + q_p)\, \Delta I_t^2 + (q_b + q_p)\, \Delta I_b^2 + (-2q_p)\, \Delta I_t \Delta I_b \tag{7.10}$$

The cost matrix Q can thus be defined as per (7.11).

$$Q = \begin{bmatrix} qt + q_p & -q_p \\ -q_p & q_b + q_p \end{bmatrix} \tag{7.11}$$

By varying the difference in cost on two particular current errors (using $q_{t,b,p}$) the errors can be ranked. A more highly ranked current (i.e. a higher cost than others) will result in a greater response magnitude. Similarly by changing the difference in magnitude between the cost matrices R and Q will either amplify or attenuate the response to a certain error. There are only two voltages relevant to the inductive network ($U^{+,-}$) and since neither one should be preferred over the other as they will both be translated into stack voltages, the cost matrix R is simply a scaling factor (k_r) multiplied by the identity matrix, as shown in (7.12). The scaling factor can be used to tune the controller. A value of 10^{-3} has been found to work well for this converter.

$$R = k_r \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{7.12}$$

Reference Converter

The output of the current controller is a vector ($u_\Sigma[k]$) containing two voltage references ($U^{+,-}$) to be applied across the inductive network. These voltages are defined in the context of the cell stacks and the HV1 link capacitor in figure 7.5. Since we can only directly influence the voltages across the stacks ($V_{t,b}$) the voltage references from the current controller have to be converted using the equations (7.13) and (7.14).

$$V_t(t) = \frac{V_{d1}}{2} - V_p(t) - U^+(t) \tag{7.13}$$

$$V_b(t) = \frac{V_{d1}}{2} + V_p(t) + U^-(t) \tag{7.14}$$

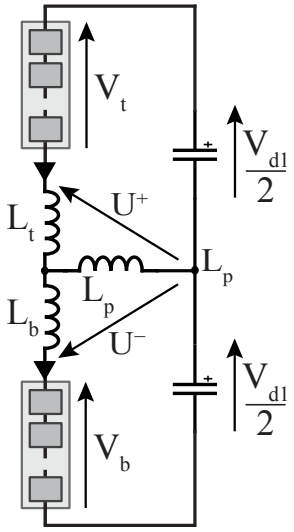

Figure 7.5: Voltages on HV1 side of square-wave DC/DC converter with shunt connected primary.

7.1.2 Current References

The current references used in the current controller are formed from a range of lower level controllers as illustrated in figure 7.6:

- The *energy balancing* block monitors the cell and HV1 link capacitors and generates the relevant currents to ensure their energy remains balanced.
- The *power controller* ensures that the measured power output at the HV2 side matches up with the power transfer reference.
- The *magnetising controller* provides the required magnetising current for the transformer such that it is completely energised from the primary side.
- Finally, the *Secondary current controller* ensures that no unwanted DC currents develop in the secondary.

A number of the block's outputs are then combined to form the AC arm reference currents in the wave-shape generator.

Energy Balancing

The theory of the energy balancing mechanism has been discussed in some detail in the previous chapter in section 6.2.1 on page 166. The control loops used to energy balance

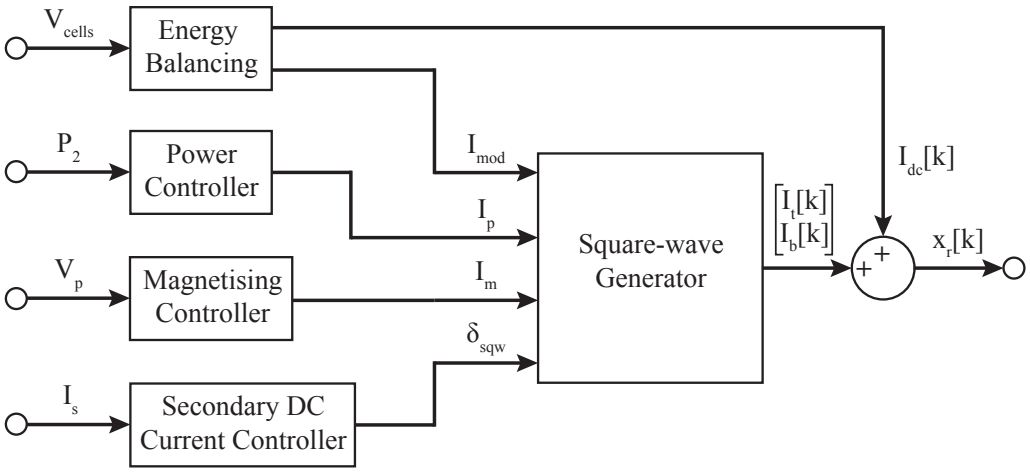

Figure 7.6: Layout of the current reference building block of the control system for the square-wave modular DC/DC converter.

the DC/DC converter are shown in figure 7.7. The energy balancing controller monitors the average energy of the stacks and creates an error signal for each ($\Delta E_{a,b}$). These are used to estimated the total energy imbalance and the difference in energy between the two stacks. The latter can be corrected by modulating the share of the primary current that each stack carries (nominally 50% each). This is achieved by introducing a modulating current vector (I_{mod}) which has an equal and opposite effect on both arm currents.

The total energy imbalance in the stacks can be addressed by a DC current flowing through both stacks (I^s_{dc}). The formation of this reference is split into a feed-forward and feedback term as illustrated. The feed-forward term is estimated from the power reference and the nominal HV1 voltage.

As the HV1 DC side capacitors serve as the return path for the primary current they may be subject to temporary energy imbalances due to slightly asymmetric currents. By modulating the DC current component that flows through the top and bottom arms a small DC current can be induced to flow through either DC side capacitor which can be used to charge or discharge it slowly. This current is kept small compared to the magnitude of the primary's square-wave. It will therefore not require significant additional current capabilities in the transformer's windings. The DC modulating component is combined with the DC current reference to flow through the cell stacks.

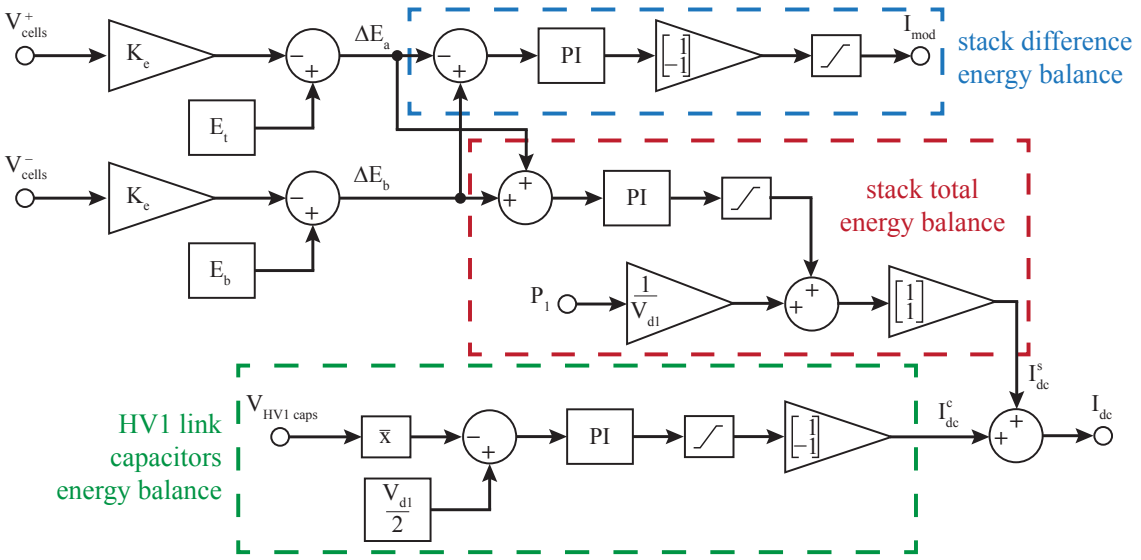

Figure 7.7: Energy balance controller for square-wave modular DC/DC converter.

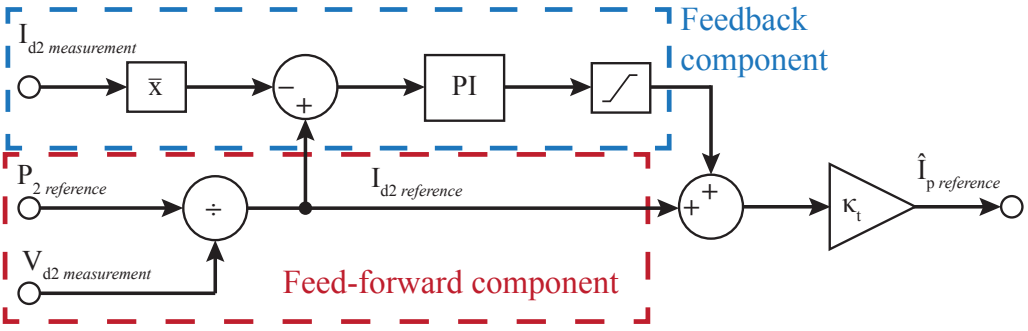

Figure 7.8: Power controller for square-wave DC/DC.

Power Controller

The power to be transferred from one HV connection to the other is set by a power transfer reference signal. The power controller measures the power on the HV2 side and calculates a reference for value for the HV2 link current I_{d2}. This is then used directly as a feed-forward term, which is combined with a feed-back term. The latter is calculated from the error signal of the reference and measured I_{d2} as illustrated in figure 7.8. The step-ratio of the transformer (κ_t) is finally used to crate a reference for the primary current's magnitude.

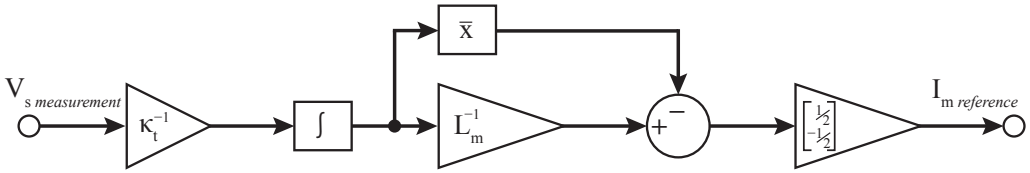

Figure 7.9: Magnetising controller for square-wave DC/DC.

Magnetising Controller

A transformer's voltages are set up across the magnetising inductance L_m which is typically placed on the primary side in transformer equivalent models. Physically however a transformer can be magnetised from either winding or a combination of the two. Since it is advantageous to make the secondary currents appear as close to an ideal square-wave as possible, in order to minimise the size of the HV2 filters, all of the magnetisation current should be supplied through the primary side in the shunt connected primary DC/DC. Creating an appropriate reference for this current is handled by the magnetising controller, as illustrated in figure 7.9.

The magnetising current for a transformer is given by (7.15). This equation is also used to estimate the magnetising current magnitude required for the transformer. The voltage across the primary is generated by the cell stacks. As the stacks are also in charge of controlling the currents, the primary voltage will typically not be a clean primary waveform. The voltage on the secondary on the other hand is dictated by the current: depending on its direction it will clamp the secondary across the HV2 link capacitor one direction or the other. For this reason, to estimate the required magnetising current, the secondary voltage is measured and scaled up using the transformer's step-ratio. To ensure that the signal is centred around zero a running average is deducted.

$$I_m(t) = \frac{1}{L_m} \int V_p(t) \mathrm{d}t \tag{7.15}$$

Transformer Secondary DC Current Controller

The current on the secondary side of the transformer is not directly controlled by the cell stacks. Whilst we can control its AC component that passes through the transformer by controlling the AC currents on the primary, the same cannot be done for the DC component in the secondary. To ensure that the mean secondary current remains zero, the duty cycle of the square-wave can be used, as illustrated in figure 7.10.

By varying the duty-cycle of the square-wave around its nominal value of 0.5, the

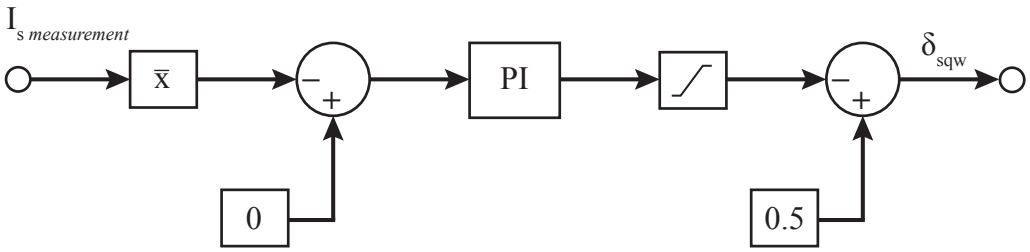

Figure 7.10: Secondary DC current controller.

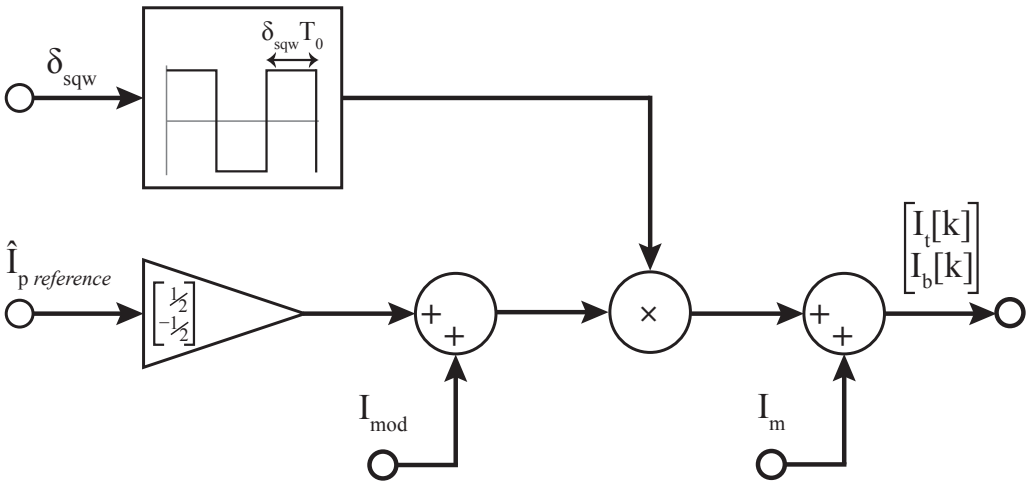

Figure 7.11: Square-wave generation block in square-wave DC/DC converter.

secondary side current can be ramped up or down. Any DC current component developing on the primary side is counteracted by the current controller.

Square-wave generator

The previously mentioned blocks, which are part of the current reference builder, generate current magnitudes and a duty-cycle for the arm currents but not time domain signals. This is the job of the square-wave generator. Here, as illustrated in figure 7.11, the duty cycle (δ_{sqw}) is used to generate a simple square-wave centred around zero. The primary current magnitude and the modulating current (I_{mod}) are combined to form the magnitude of the square-wave component for each arm current. Finally the magnetising current component is added on top of that, forming the current reference for the AC component of the arm currents.

7.1.3 Cell-Level Controller

The cell-level controller for the square-wave DC/DC converter works in the same way as for the front-to-front arrangements, or indeed for any modular converter. Its job is to convert the voltage reference, supplied by the current controller, for the cell stacks and turn it into commands for the individual cells. These commands dictate the cell's state and thereby which switches are turned on and which off. The actual controller used in this work is the same as for the F2F simulations and further details can be found in a previous chapter in section 3.2.2.

7.1.4 Enabling bi-directional power transfer

The circuit as has been presented in the previous chapter on page 163, only allows for a unidirectional power transfer from the HV1 to the HV2 side, because the rectifier used in the system only operates as desired for one current direction. As the rectifier only utilises diodes, the direction of the secondary current will determine which HV2 terminal is clamped to which terminal of the secondary winding.

To reverse the power flow the secondary current has to be inverted without changing the secondary's voltage profile. This in effect equates to shifting the current square-wave by 180° relative to the voltage wave-form. In a passive rectifier (i.e. consisting only of diodes) shifting the current waveform will cause the diodes to enter forward conduction at different times. Since these however form the only connection path between the winding and DC terminals, the voltage waveform will shift along with the current waveform. This prevents a bidirectional power flow using a passive rectifier.

Using an active rectifier, as illustrated in figure 7.12, allows the current waveform to be shifted relative to the voltage waveform. The active switches clamp the DC terminal voltages to the secondary and allow current to flow in the opposite direction to their anti-parallel diodes at the same time. The switches will typically be high powered IGBTs or GTOs, as they have to be able to withstand the secondary current magnitudes.

As the rectifier now contains active devices they require switching signals. The switching pattern will have to take the square-wave duty-cycle into account and ensure that two series connected devices are not switched on at the same time, to prevent shorting the DC side. The switching signal generator is shown in figure 7.13.

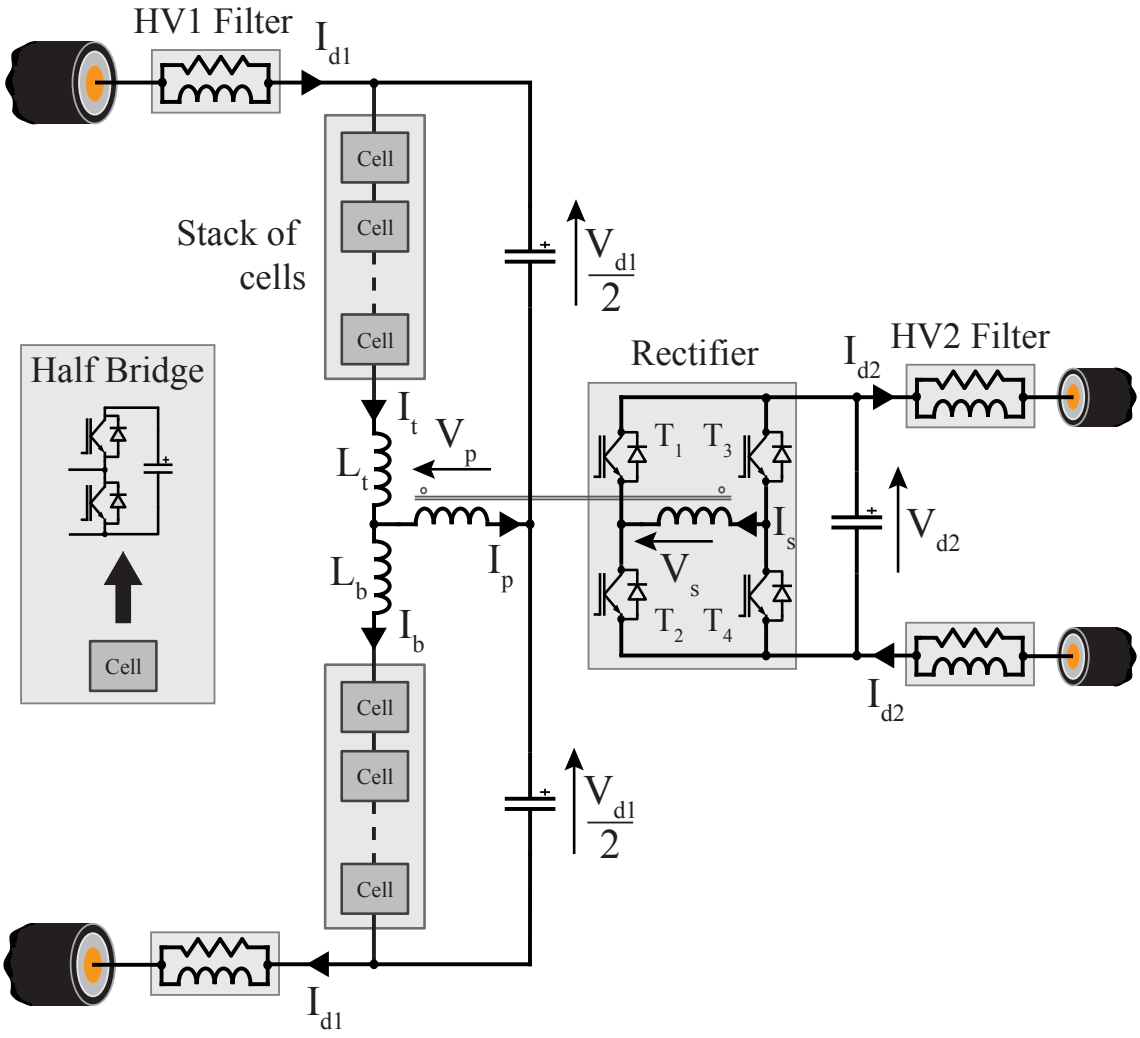

Figure 7.12: Circuit diagram for shunt connected primary DC/AC/DC converter with active rectification.

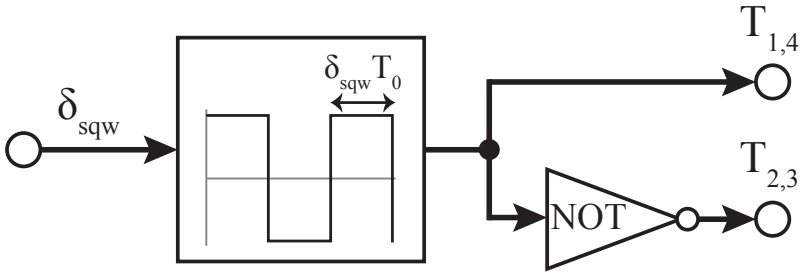

Figure 7.13: Switching signal generator for rectifier switches.

7.2 Basic Steady-State Operation

Following the theory of the shunt connected primary DC/DC converter, this section will explore its basic operation via a simulation model. To reduce the computational complexity of the model a scaled-down version has been used. It was scaled so as to maintain current magnitudes in the thousands of ampere on the lower voltage side, as would be the case in a full scale converter. The model parameters are listed in table 7.1. Unless stated otherwise in the following sections, the parameters listed remain unchanged and a positive power flow, that is a power transfer from HV1 to HV2, is assumed.

7.2.1 Operation of Stacks of Cells

The arm currents flowing through the cell stacks are the two system currents which are actively controlled by the cell stacks. Any errors in the tracking of these currents will affect the converter operation and the resulting DC currents. We therefore start by looking at these arm currents and the corresponding stack voltages for a range of transformation-ratios. Figure 7.14 shows simulation results for the voltages and currents for the top cell stack and figure 7.15 the same for the bottom stack.

As the cell stack transformation variable (κ_s) is decreased, which effectively increases the voltage step generated by the stacks, the current magnitudes increase to maintain power level parity. The arm currents contain a DC offset which is due to the DC current drawn from the HV1 link which exchanges energy between the DC side and the cell stacks. The AC component of the currents in the top and bottom arm, which are measured as shown in figure 7.12, are 180° out of phase relative to each other, as they combine at the mid-point of the stacks to form the primary current.

An ideal square-wave has an infinite rate-of-change (or ramp-rate) when it transitions between its maximum and minimum values and vice versa. Realistically this is of course unachievable: the inductance in the arm's current path combined with the limited voltage capability of the cell stacks severely limits the possible current ramp-rate, as dictated by the general VI relationship of inductors as described in (7.16). This means that the transition time (being a rise or fall time) is finite and non-zero, and can be significant, as is illustrated in figure 7.16.

$$V = L\frac{\mathrm{d}I}{\mathrm{d}t} \tag{7.16}$$

From the bottom graph in figure 7.16, showing the stack's voltage, it can be noted that

Table 7.1: System parameters used in Simulation of square-wave modular DC/DC test system.

System Parameter	Variable	Value
Voltage and Power ratings		
HV1 link voltage	V_{d1}	100 kV
HV2 link voltage	V_{d2}	10 kV
Power rating	P_1	20 MW
HV1 DC current	I_{d1}	200 A
HV2 DC current	I_{d2}	2000 A
Converter Parameters		
Stack transformation-ratio	κ_s	0.3
Stack voltage control margin	ζ_{cm}	10 %
Peak stack voltage capability	$\hat{V}_t$	88 kV
Number of cells per stack	N_c	49
Nominal cell voltage	V_c^{nom}	1800 V
Cell capacitance	C_c	4 mF
Arm inductance	$L_{t,b}$	800 μH
Square-wave frequency	f_{AC}	500 Hz
Cell rotation frequency	f_{cr}	$8.2f_{AC}$ Hz
Transformer Parameters		
Transformer step ratio	κ_t	0.33
Peak primary voltage	$\hat{V}_p$	30 kV
Peak secondary voltage	$\hat{V}_s$	10 kV
Coupling factor	k_t	0.9998
Primary leakage inductance	L_{lp}	0.51 mH
Secondary leakage inductance	L_{ls}	0.06 mH
Magnetising inductance (primary side)	L_m	2.53 H
Filter Parameters		
HV1 filter resistance	R_{f1}	5 Ω
HV1 filter inductor	L_{f1}	6 mH
HV1 link capacitor	C_1	100 μF
HV1 filter resistance	R_{f2}	5 Ω
HV1 filter inductor	L_{f2}	2 mH
HV1 link capacitor	C_2	500 μF
Simulation Parameters		
Simulation time step	T_s	1 μs
Controller sampling frequency	f_{cs}	100 kHz

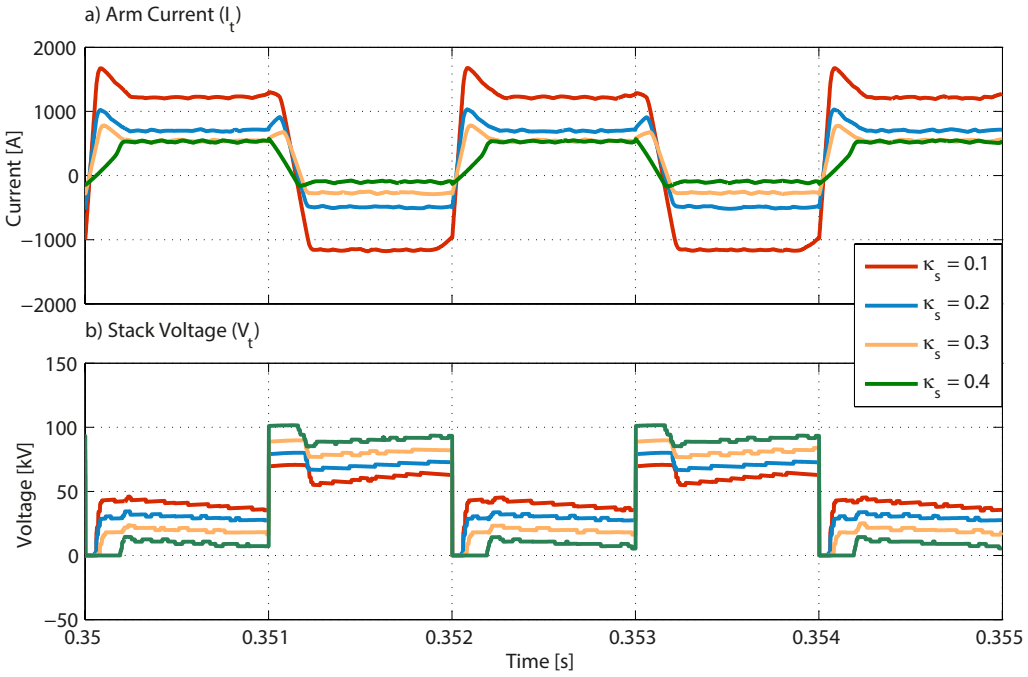

Figure 7.14: Arm currents and corresponding stack voltages for top arm for a range of stack transformation-ratios.

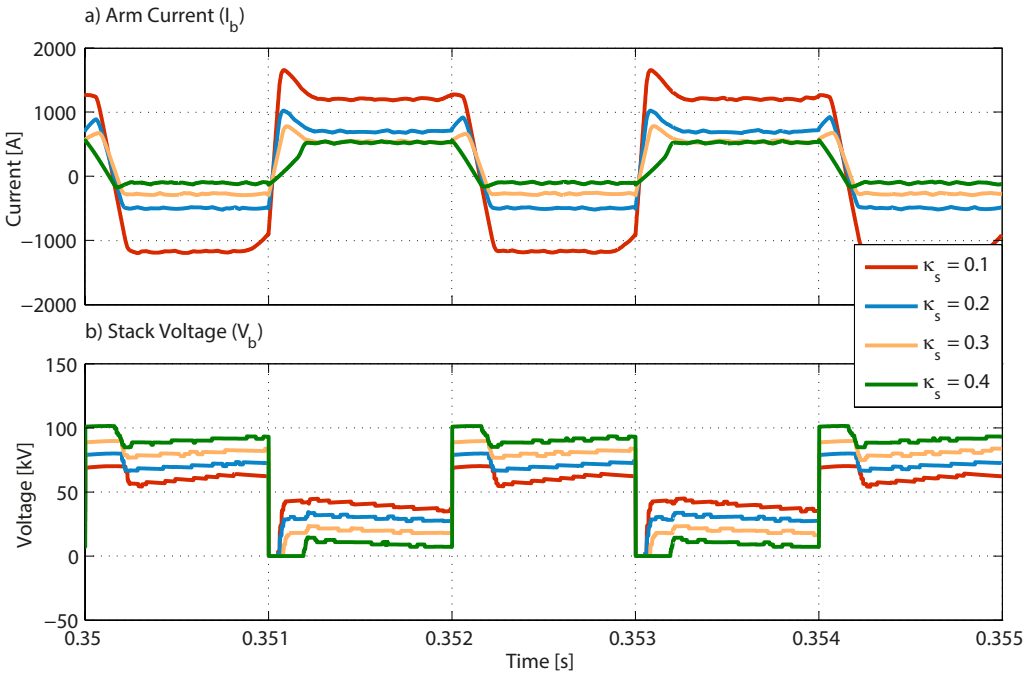

Figure 7.15: Arm currents and corresponding stack voltages for bottom arm for a range of stack transformation-ratios.

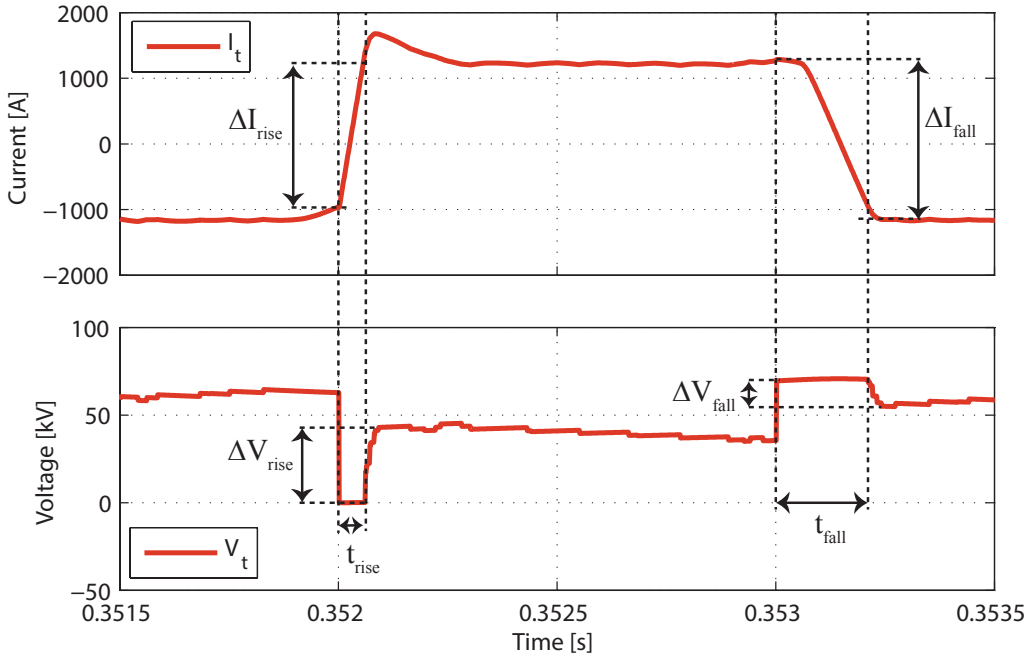

Figure 7.16: Stack current and voltage illustrating transition times for $\kappa_s = 0.1$.

the voltages the stacks generate fall to zero during a rising current transition and peak during a falling current transition. This is the result of the control action being applied across the inductive network to track the current references. On top of this the stacks also generate the square-wave voltage of the primary. In between edges a slight slope can be noticed. This is the result of supplying a triangular magnetising current to the primary.

Rectification of an ideal square-wave results in a clean DC signal. As the transition times increase the rectified current will contain an increasing amount of harmonic content. As a stable HV2 DC voltage and a clean DC current may be required, the filter will inadvertently become larger and costlier. Minimising the transition times will therefore reduce the burden on the filters but may come at an additional cost. To better understand this trade-off we must look at what affects the transition times of the square-wave in the converter using (7.16). We start by looking at the voltage across the inductive network used to control the currents.

Voltage applied across inductive network

The current-controller generates voltage requests for the stacks to implement. As it is a discretised controller, these voltages, if generated by the stacks, would lead to the desired change in current in one time-step of the controller (T_{cs}). The requested voltages are

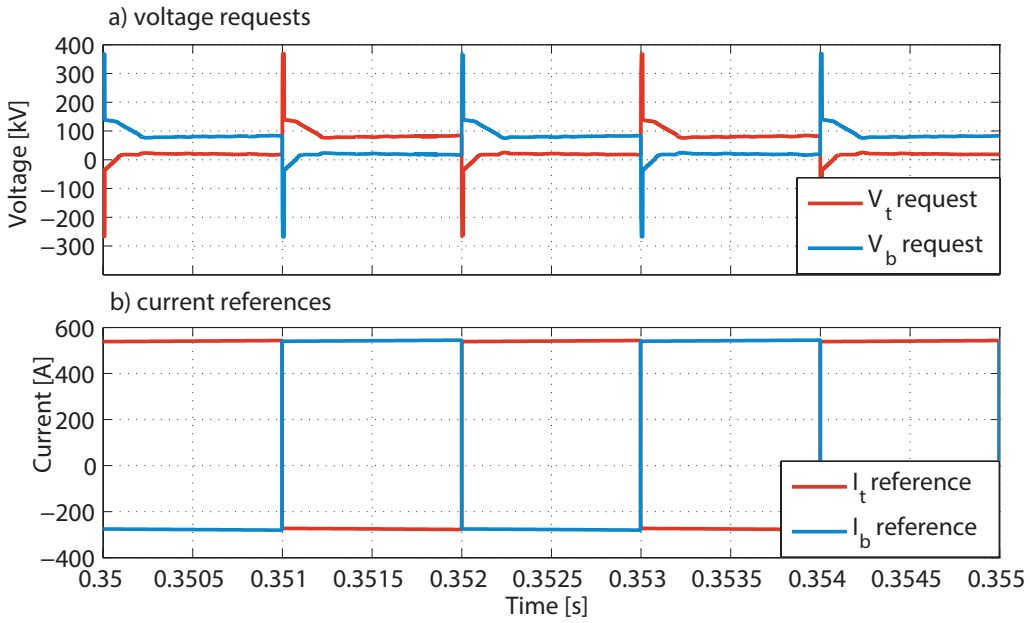

Figure 7.17: Requests for stack voltages from the current controller (top) and current references to be tracked (bottom).

relatively large compared with the peak voltage capability of the stack, as can be seen from figure 7.17. The graphs show the requested stack voltages, from the current controller, for the test system long with the arm current references that are to be tracked. The requested voltages in combination with limited voltage capability of the stacks lead to a stack voltage profile as previously shown in figure 7.16.

It therefore stands to reason that if more voltage capability in the stacks were available, the current transitions would take less time. The basic voltage capability of the stacks is calculated using only the DC and AC voltage magnitudes (see section 6.2.1). To enable the controller to regulate the currents in the arms a voltage control margin (ζ_{cm}) is used to supplement the peak voltage capability of the stacks, as per (7.17).

$$\hat{V}_{t,b} = V_{d1}\left(\frac{1}{2} + \kappa_s\right)(1 + \zeta_{cm}) \tag{7.17}$$

Knowing that the converter uses half-bridge cells in its stacks, the maximum voltage capability of each stack is limited to V_{d1}. Any more and reverse polarity voltage capability would be required, which cannot be generated using half-bridge cells alone. Using this limit we can therefore define the largest transformation-ratio (κ_s) the stacks are capable of, using half-bridge cells only, for varying ζ_{cm}, as illustrated in (7.18) and displayed in

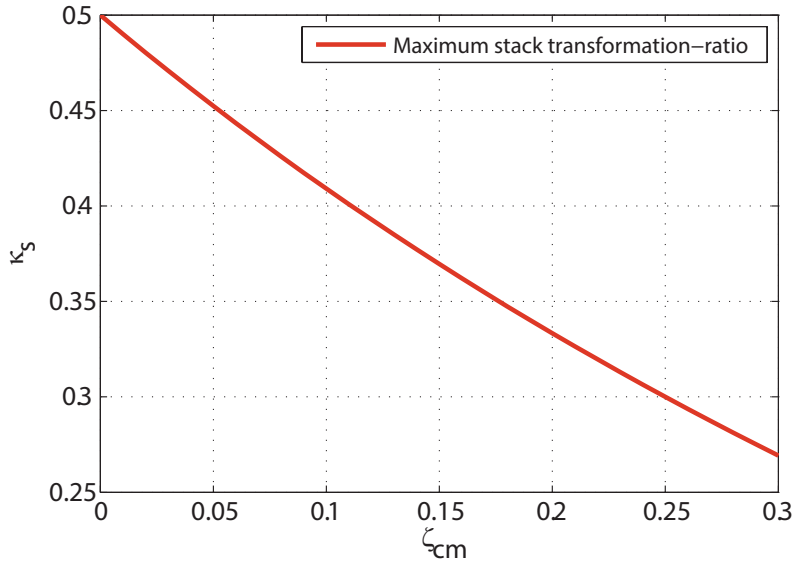

Figure 7.18: Maximum stack transformation-ratio possible for varying control voltage margin (ζ_{cm}), utilising half-bridge cells only.

figure 7.18. From the graph it can be seen that for a voltage control margin of 10% the peak transformation-ratio possible is just over 0.4 (5:2).[1]

$$\begin{aligned} \kappa_s = = & \frac{1}{1+\zeta_{cm}} - \frac{1}{2} \\ : & \ max\left(\hat{V}_{t,b}\right) = V_{d1} \end{aligned} \tag{7.18}$$

Figure 7.19 shows the arm current of the top stack of cells along with the stack's generated voltage for a range of ζ_{cm}. As the voltage available to transition the arm current increases (i.e., an increasing ζ_{cm}) the transition times decrease. It can also be noted that the rise and fall times are different and that this difference is amplified as the control margin is increased. This is because the voltage that can be applied across the inductive network, as generated by the stacks of cells, is not symmetrical which allows currents to be ramped more quickly in one direction than the other.

Let the stack voltage ($V_{t,b}$) consist of two components: first, the component V_{tv} which is the voltage required across the stack to generate the primary voltage V_p, as per (7.19) and (7.20). Second, we can define a voltage which the current controller requires the stacks

[1]Incidentally, this is the reason why the peak transformation-ration presented in figures 7.14 and 7.15 was 0.4.

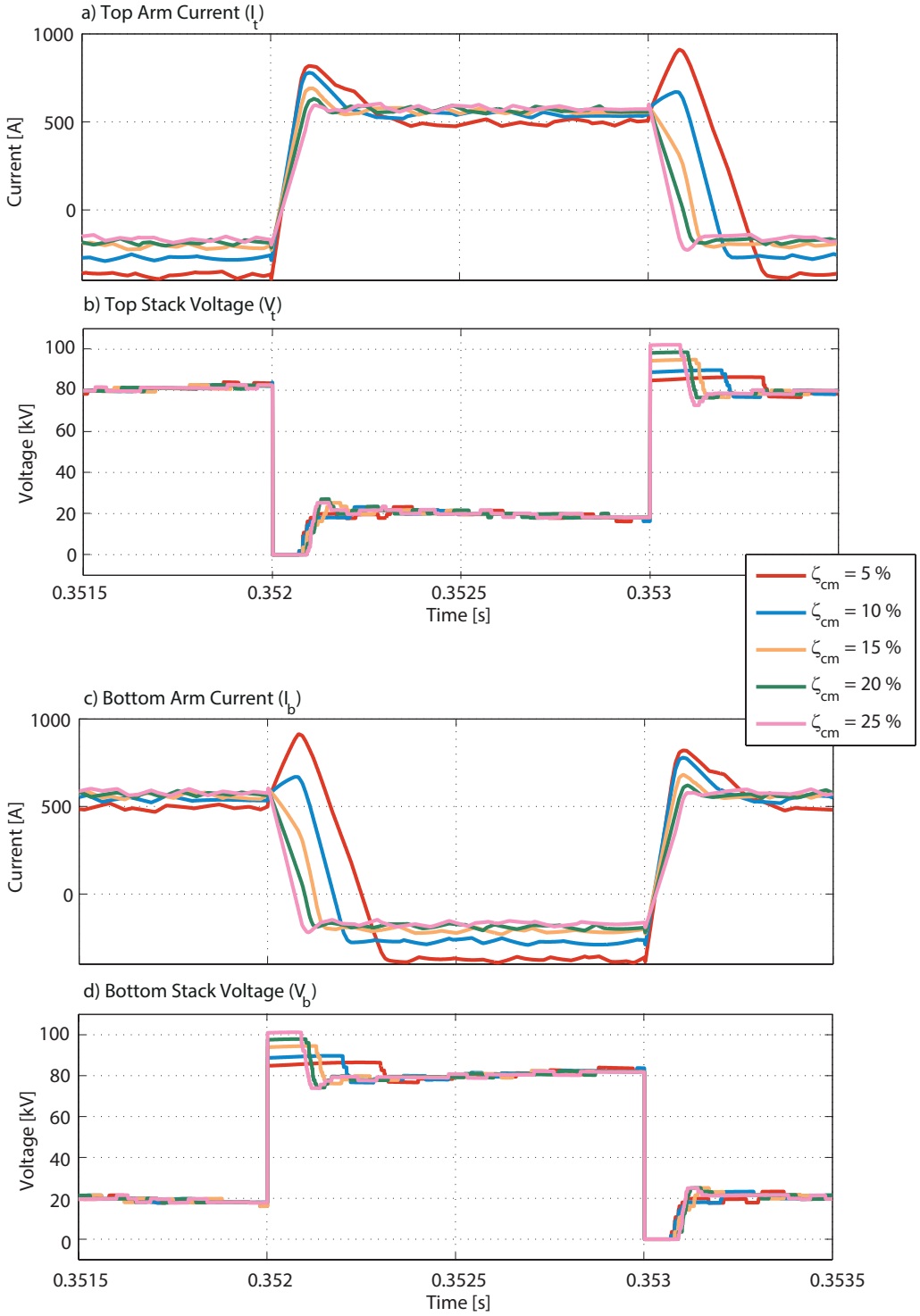

Figure 7.19: Arm currents and stack voltages for top and bottom arm with varying ζ_{cm} for $\kappa_s = 0.3$.

to generate to apply a certain voltage, $U^{+,-}$, across the inductive network to control the currents. Both components make up the stack voltages as described in (7.21) and (7.22). Let the variable $\hat{V}_{t,b}$ denote the maximum voltage a stack can generate, dependent on the voltage control margin as per (7.17).

$$V_{tv}(t) = \frac{V_{d1}}{2} - V_p(t) \tag{7.19}$$

$$V_{bv}(t) = \frac{V_{d1}}{2} + V_p(t) \tag{7.20}$$

$$\therefore\ V_p(t) = \hat{V}_p \cdot \mathrm{sqw}\left(\frac{t}{T_0}\right)$$

$$\therefore\ \mathrm{sqw}\left(\frac{t}{T_0}\right) = \begin{cases} 1 & \text{if } 0 \leq t < \frac{T_0}{2}, \\ -1 & \text{if } \frac{T_0}{2} \leq t < T_0. \end{cases}$$

$$V_t(t) = V_{tv}(t) + V_{tc}(t) \tag{7.21}$$

$$V_b(t) = V_{bv}(t) + V_{bc}(t) \tag{7.22}$$

Since the stacks consist of half-bridge cells, the stack voltages are limited as per (7.23).

$$V_{t,b} = [0, \hat{V}_{t,b}] \tag{7.23}$$

Knowing this and considering the equations (7.19) to (7.22), we can define the limits for V_{tc} and V_{bc} as per (7.24) and (7.25).

$$\begin{aligned} V_{tc} &= [-V_{tv}, \hat{V}_t - V_{tv}] \\ &= [\check{V}_{tc}, \hat{V}_{tc}] \end{aligned} \tag{7.24}$$

$$\begin{aligned} V_{bc} &= [-V_{bv}, \hat{V}_b - V_{bv}] \\ &= [\check{V}_{bc}, \hat{V}_{bc}] \end{aligned} \tag{7.25}$$

To ramp up the current in the primary (rising edge transition, or from now on referred to as a rising transition) we need to ramp the current up in the top arm and down in the bottom one (as per the current definitions in figure 7.12). A rising transition requires a positive voltage across the inductive network (as per figure 7.17), $U^{+,-}$. To effect a rising transition in the primary current the top stack therefore has to raise its associated terminal voltage of the inductive network above the primary voltage. As the current reference requests an instantaneous transition the stack will operate at its lower V_{tc} limit ($\check{V}_{tc}$) such that the stacks voltage is reduced to $V_t(t) = 0kV$, as can be seen in graph b) in

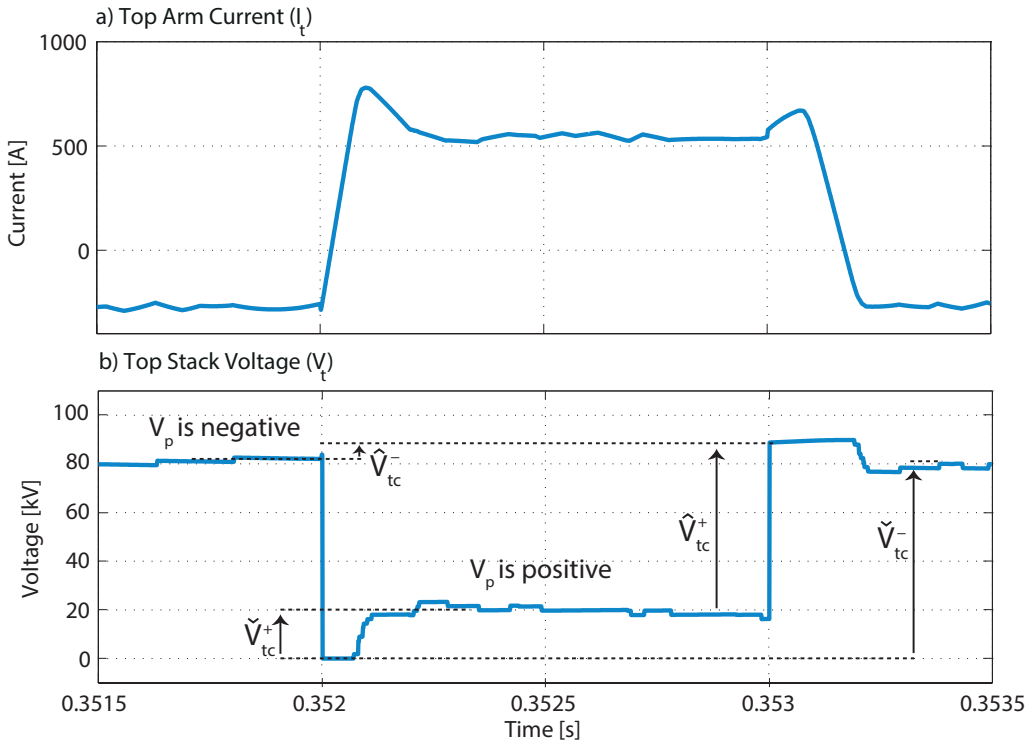

Figure 7.20: Arm current and stack voltage to illustrate $\check{V}_{tc}$ and $\hat{V}_{tc}$, for $\kappa_s = 0.3$ and $\zeta_{cm} = 0.1$.

figure 7.19. It should be noted that during this time the primary voltage is positive and at a magnitude of V_p.

At the same time the lower stack has to implement a falling transition (falling current edge) in its arm current. It does so as quickly as possible by raising its terminal voltage above the primary voltage. In so doing it operates at its peak V_{bc} such that the stacks voltage is limited by its peak capability, $\hat{V}_t$. This can be observed in graph d) in figure 7.19.

Similarly to implement a falling current transition the top stack will operate at its $\hat{V}_{tc}$ and the bottom stack at its $\check{V}_{tc}$. Figure 7.20 illustrates what $\check{V}_{tc}^{+,-}$ and $\hat{V}_{tc}^{+,-}$ mean in relation to the voltage across the stacks as explained here. The figure shows an example for the top stack of cells only. The table 7.2 summarises which voltage limits are relevant to which primary current transitions.

Now that the actions taken by the stacks for a current transition are understood, we can note that the actions taken by each stack are subject to different voltage limits. Thus if the current controlling components of the stack voltage, V_{tc} and V_{bc}, are not of equal

Table 7.2: Voltage limits relevant for current transitions depending on primary voltage.

I_p transition	$V_p > 0$	$V_p < 0$
Rising edge	$\check{V}_{tc}^{+}, \hat{V}_{bc}^{+}$	$\hat{V}_{tc}^{-}, \check{V}_{bc}^{-}$
Falling edge	$\hat{V}_{tc}^{+}, \check{V}_{bc}^{+}$	$\check{V}_{tc}^{-}, \hat{V}_{bc}^{-}$

and opposite magnitude then the voltages across the inductive network, $U^{+,-}$, are not symmetrical. This leads to the arm current ramping its arm current up more quickly than the bottom arm current is ramped down, causing not only a difference in the transition times but also a voltage across the arm inductors. This in turn results in the observed current overshoots, which get larger as the difference in $U^{+,-}$ increases.

To explain the connection between the transformation-ratio κ_s and voltage control margin ζ_{cm}, and the difference in transition time we can rewrite (7.24) and (7.25), using (7.17) and (6.69), as shown in (7.26) to (7.29). The minimum voltages, $\check{V}_{tc}$ and $\check{V}_{bc}$, are independent of the control margin and form the difference between the DC terminal and the primary voltage. Because of this there exist two different values for the minimum voltage components depending on the polarity of the primary voltage when a transition occurs.

$$\check{V}_{tc} = -V_{d1}\left(\frac{1}{2} - \mathrm{sqw}\left(\frac{t}{T_0}\right)\kappa_s\right) \tag{7.26}$$

$$\hat{V}_{tc} = V_{d1}\left(\left(\frac{1}{2} + \kappa_s\right)(1+\zeta_{cm}) - \left(\frac{1}{2} - \mathrm{sqw}\left(\frac{t}{T_0}\right)\kappa_s\right)\right) \tag{7.27}$$

$$\check{V}_{bc} = -V_{d1}\left(\frac{1}{2} + \mathrm{sqw}\left(\frac{t}{T_0}\right)\kappa_s\right) \tag{7.28}$$

$$\hat{V}_{bc} = V_{d1}\left(\left(\frac{1}{2} + \kappa_s\right)(1+\zeta_{cm}) - \left(\frac{1}{2} + \mathrm{sqw}\left(\frac{t}{T_0}\right)\kappa_s\right)\right) \tag{7.29}$$

The voltages, normalised with respect to V_{d1}, for both cases are shown in figure 7.21. Graph a) (top) shows the results for a positive primary voltage (where the primary voltage, V_p, is defined as in figure 7.12 and graph b) (bottom) for a negative V_p, for a constant transformation-ratio of $\kappa_s = 0.3$. In a), $\check{V}_{tc}$ is constant at a ratio of 0.2, which agrees with the simulation results shown in figure 7.20 where 20% of 100 kV are used to bring about the rising edge current transition. Similarly when the primary voltage is negative $\hat{V}_{tc}$ should be about 8 kV according to graph b) which is again confirmed by figure 7.20 during a falling edge transition of the arm current.

During a rising edge transition of the primary current both stacks of cells act in concert but are limited by different voltage limits: e.g., when the primary voltage is positive the

limits $\check{V}_{tc}$ and $\hat{V}_{bc}$ are relevant. Similarly for a falling edge transition in the primary current when the primary voltage is negative, the voltage limits $\hat{V}_{tc}$ and $\check{V}_{bc}$ are of interest. From figure 7.21 it can be noted that the relevant voltage limits for all transitions cross at $\zeta_{cm} = 0.25$. For a control margin of this value, for $\kappa_s = 0.3$, the voltages available for the current transitions in the top and bottom stacks are the same. Therefore the transition time for a falling edge is the same as for a rising one, which is confirmed by the simulation results in figure 7.19.

We can thus define the relationship between the transformation-ratio (κ_s) and the control margin (ζ_{cm}) for which the transition times will be equal, as shown in (7.30). This relationship turns out to be the same (just rearranged) as for the maximum ζ_{cm} for a certain κ_s, as calculated in (7.18) and shown in figure 7.18. Therefore the maximum allowed control margin (assuming half-bridge cells) for any κ_s is also the control margin for which the transition times will be equal and minimising the overshoot observed in the arm currents.

Whether this control-margin should indeed be chosen is another question however and one that is best assessed by looking at the engineering trade-offs involved. This will be done in the next section.

$$\zeta_{cm} = \frac{1}{\frac{1}{2} + \kappa_s} - 1 \quad \text{as } \left|\check{V}_{tc}\right| = \left|\hat{V}_{bc}\right| \tag{7.30}$$

Another interesting observation that can be made from the graphs in figure 7.21, is the fact that we have so far only considered two pairs of voltage limits even though there are four in total. The other two, such as $\hat{V}_ac$ and $\check{V}_{bc}$ when V_p is positive, are relevant when the primary current and voltage are out of phase, i.e., when the power flow is reversed to transfer energy between HV2 and HV1.

In this case the AC components of the arm currents are inverted, as shown in figure 7.22 for a range of control margins and a fixed transformation-ratio of 0.3. Compared to the arm currents in case of a power transfer from HV1 to HV2, it can be noted that the transition times are much shorter for both rising and falling current transitions. This is due to the larger voltages available to ramp the currents (V_{tc} and V_{bc}) as can be seen from figure 7.21. It can be noted that increasing the current control margin ζ_{cm} has virtually no effect on the falling current transitions. The current overshoot at the rising current transitions can be seen to be shortened in duration, but not magnitude, due to an increasing control margin.

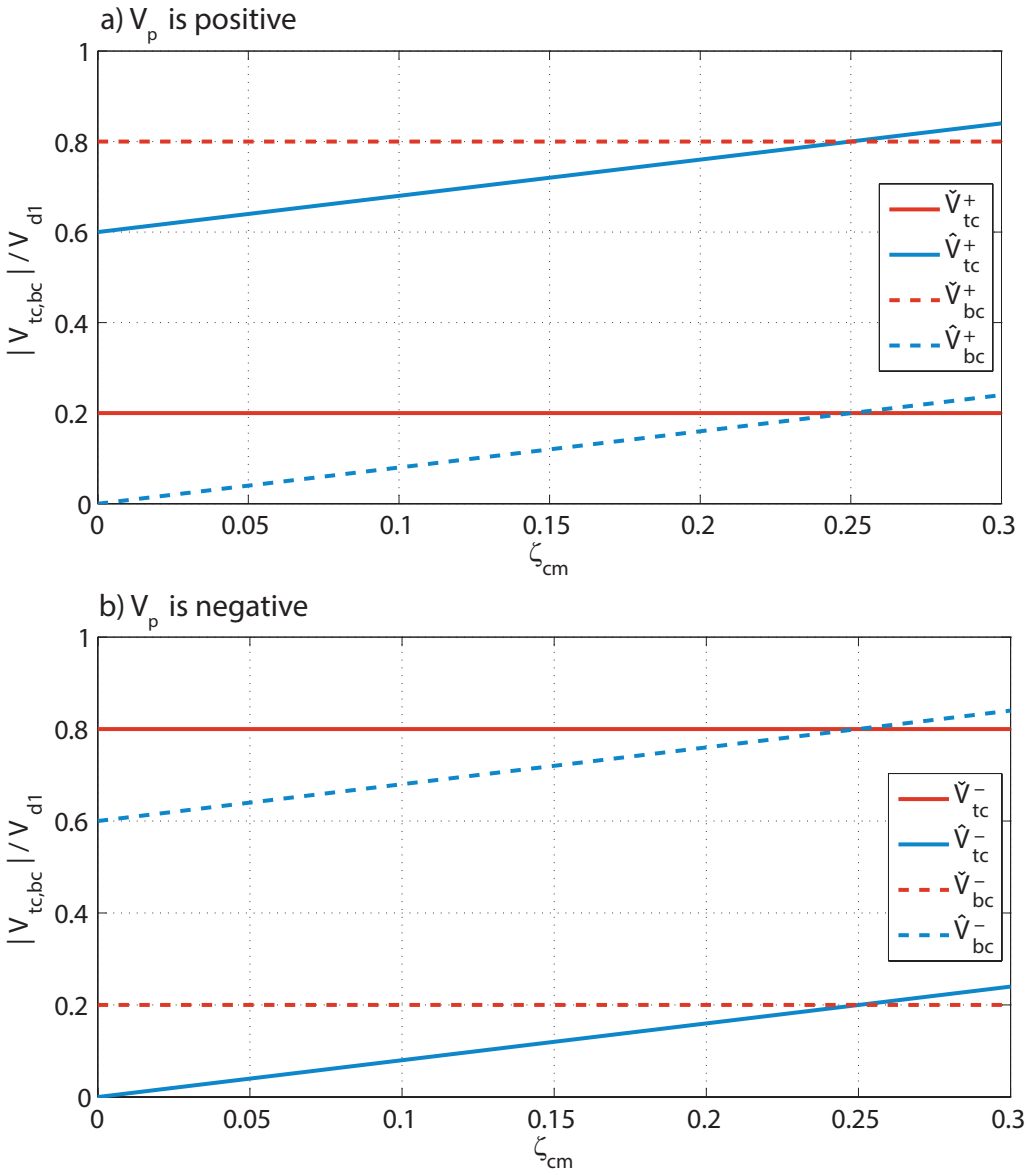

Figure 7.21: Normalised maximum and minimum voltage component available in stacks of cells to control currents, for $\kappa_s = 0.3$.

When it comes to choosing the control margin for the converter, the application should therefore be taken into careful consideration: If the DC/DC converter is only required to feed power into the higher voltage link (HV1), then a small (such as 5%) control margin will suffice. For a power transfer in the opposite direction a significantly larger control margin may prove more suitable. It should be noted that a larger control margin would evidently not hamper a power transfer from HV2 to HV1, but will add extra cells to the stacks and therefore increase the losses (something that will be explored in more detail in the next chapter).

The current overshoots observed in the arm currents in figures 7.22 as well as 7.19 are also also in part due to the fact that the controller has a finite sampling frequency. This means that in between samples the current may deviate from the reference unhindered. To reduce this deviation one can increase the sampling frequency of the controller. The effect of this on the overshoot in the arm currents is illustrated in figure 7.23 which shows the top arm current transitions, for a power transfer from HV2 to HV1, for a range of sampling frequencies. These results clearly indicate that an increase in sampling frequency reduces the overshoot as stipulated. The benefits of increasing it do however diminish with little visible improvement at 400 kHz compared to 200 kHz.

Practically it would be challenging to achieve sampling frequencies of 100 kHz or more due to the significant delays between measurement and acquisition. DC/AC VSC installations have been said to use around 10 to 50 kHz which for a 50 Hz AC wave-form has been more than enough. Since the converter is operational at the higher end of those sampling frequencies it my not pose too much of a problem. Similarly it operates with a significantly higher AC frequency and therefore may be justified to operate with a higher sampling frequency also.

Inductance in the current path

Other than applying a larger voltage across the inductive network to reduce the time taken to ramp the current up or down, we can instead explore reducing the total inductance in the current path. A lower inductance will lead to a faster transition in the arm current for the same voltage applied across it. The inductive network consist of the arm inductors and the leakage inductance of the transformer, as previously described in figure 7.2.

Figure 7.24 illustrates the effect of an increasing arm inductance on the top arm current. As the voltage capabilities of the stacks remain unchanged across all scenarios, the transition time increases as the arm inductance increases, because the rate of change of the current is smaller. Since the arm inductances form the series inductance for the DC current

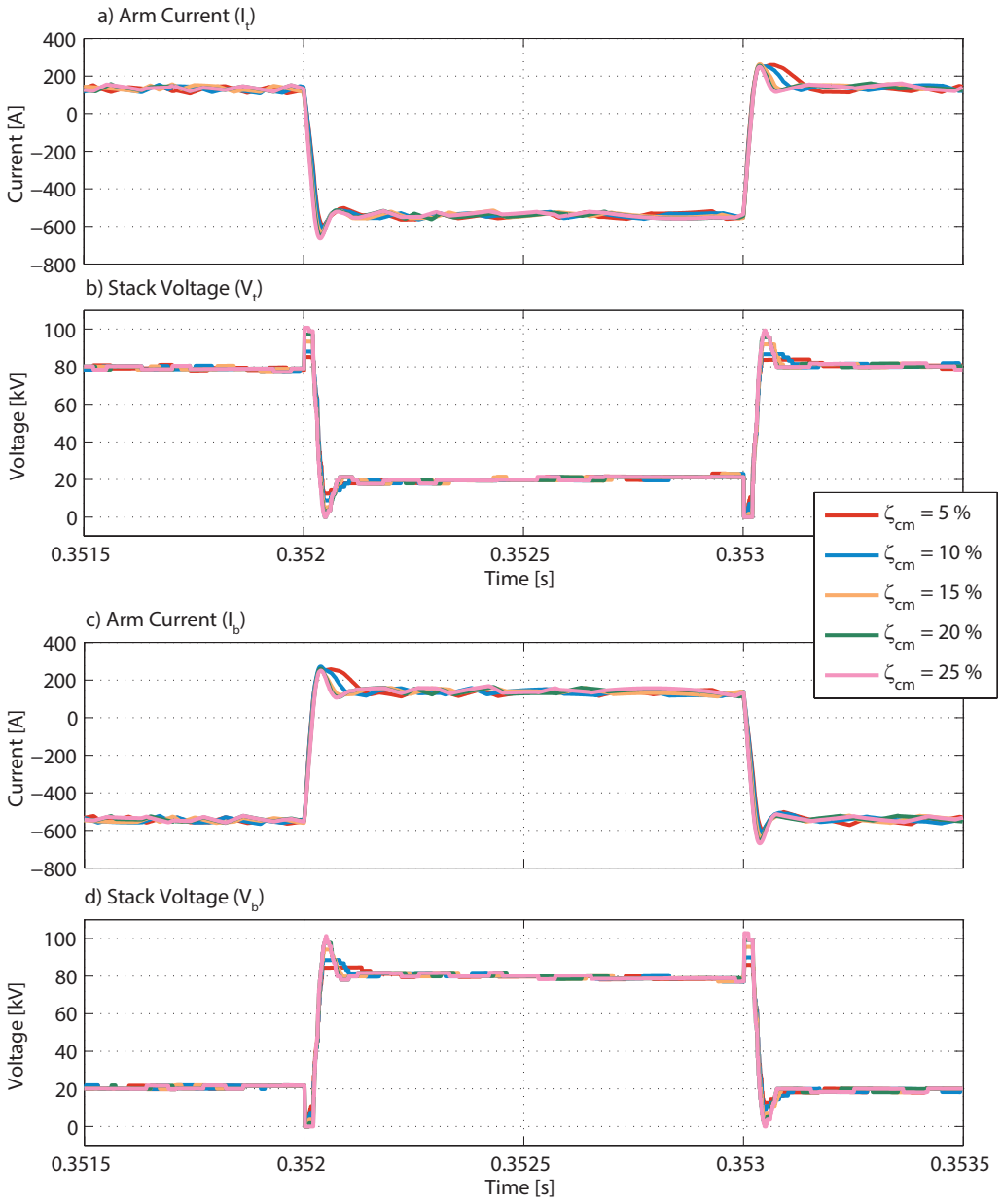

Figure 7.22: Arm currents and stack voltages for power transfer from HV2 to HV1 for a range of control margins, for $\kappa_s = 0.3$.

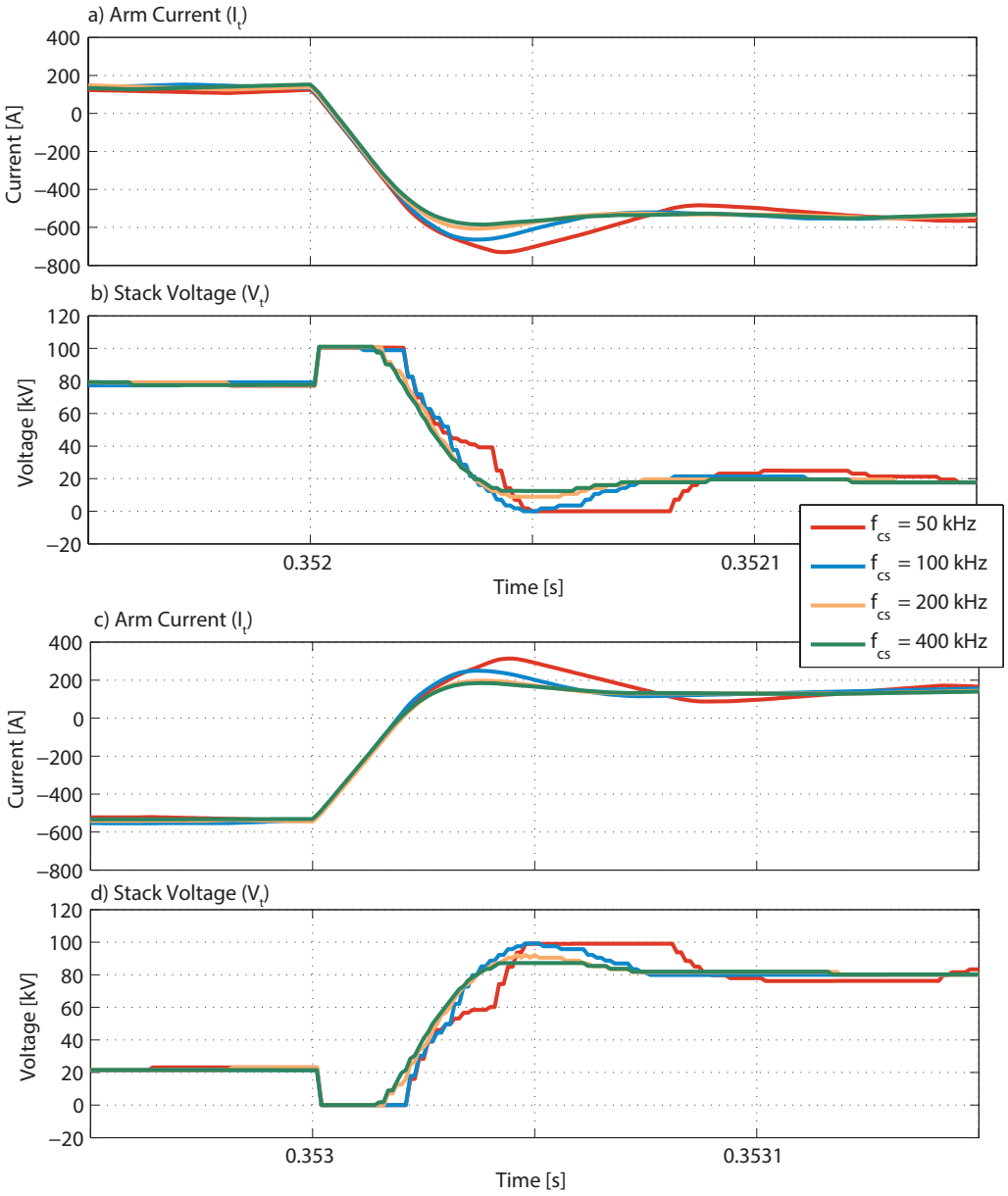

Figure 7.23: Current transitions in top arm along with stack voltages for range of controller sampling frequencies, for a power transfer from HV2 to HV1 and also $\kappa_s = 0.3$ and $\zeta_{cm} = 0.25$.

path, the current overshoot can be observed to be smaller for larger arm inductances.

Earlier it has been established that the overshoot can be counteracted with a higher sampling frequency. Since this current overshoot is significantly longer than a single sampling period of the controller (even at 100 kHz), the sampling frequency cannot be the only factor affecting it, particular for a significantly longer transition period as is the case for the results shown (power transfer from HV1 to HV2 instead of the reverse, which benefits from quicker transition periods).

As the stacks can be seen to reach their voltage capability limits for both transitions, as shown in figure 7.24, it is also plausible that the stacks start to loose control of the DC current component during the transition period. This is supported by the simulation results which show that both arm currents experience similar overshoot currents at the same time (as can be seen from graphs a) and c)).

Increasing the leakage inductance will also increase the overall inductance in the AC current path, not however in the DC current path. The transition time will therefore increase whilst the overshoot will not decrease. This is supported by the simulation results as shown in figure 7.25, which also show that the overshoot current increases as the leakage current increases. Since the larger inductance in the AC current path requires the stacks to operate at their voltage capability limits for longer the, the DC current component remains uncontrolled for longer allowing the overshoot current to rise for a longer period of time.

From these results it can be concluded that ideally the leakage inductance should be reduced as much as possible as an increase in its value has only negative effects. The choice of arm inductance depends on two factors: first, the voltage control margin of the cell stacks. A smaller control margin means that stacks will need to operate at their voltage capability limits for longer to achieve the required AC current transition. During this time the DC component can become uncontrolled and a larger arm inductance would be beneficial to limit its rate of change and therefore reduce the overshoot's magnitude.

Second, since the stacks of cells operate with discrete voltage levels, a perfect match for the voltage as requested by the current controller cannot be guaranteed. Therefore in between sampling steps of the current controller the arm current may fluctuate as a single cell is switched in and out of conduction. A smaller inductance will allow this current to deviate further in between sampling steps. The arm inductance in this sense also becomes a function of the discrete voltage level step size in the stacks and the sampling frequency of the controller.

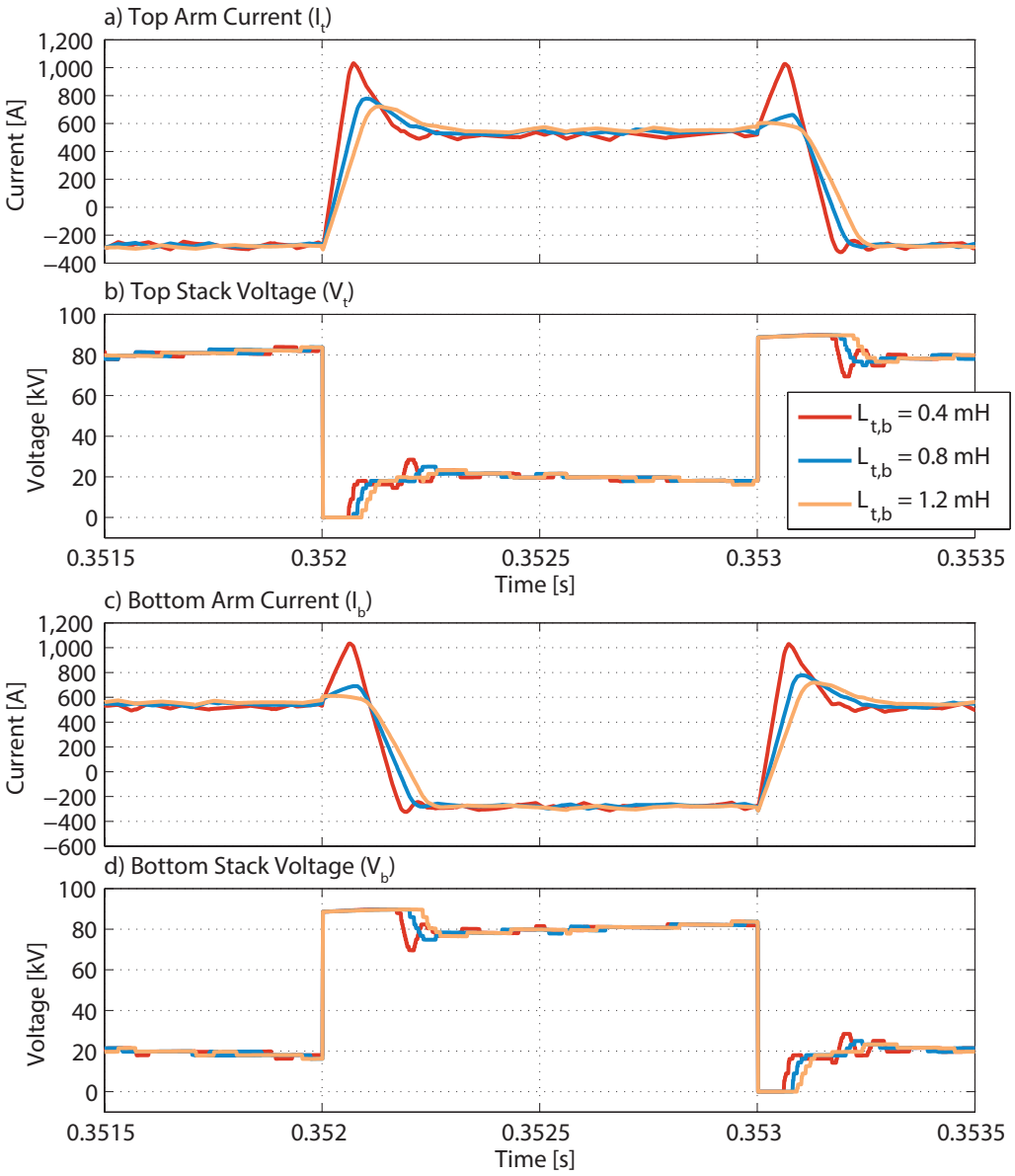

Figure 7.24: Arm currents and stack voltages for range of arm inductances, for $\kappa_s = 0.3$, $\zeta_{cm} = 0.1$ and $L_{lp} = 1mH$.

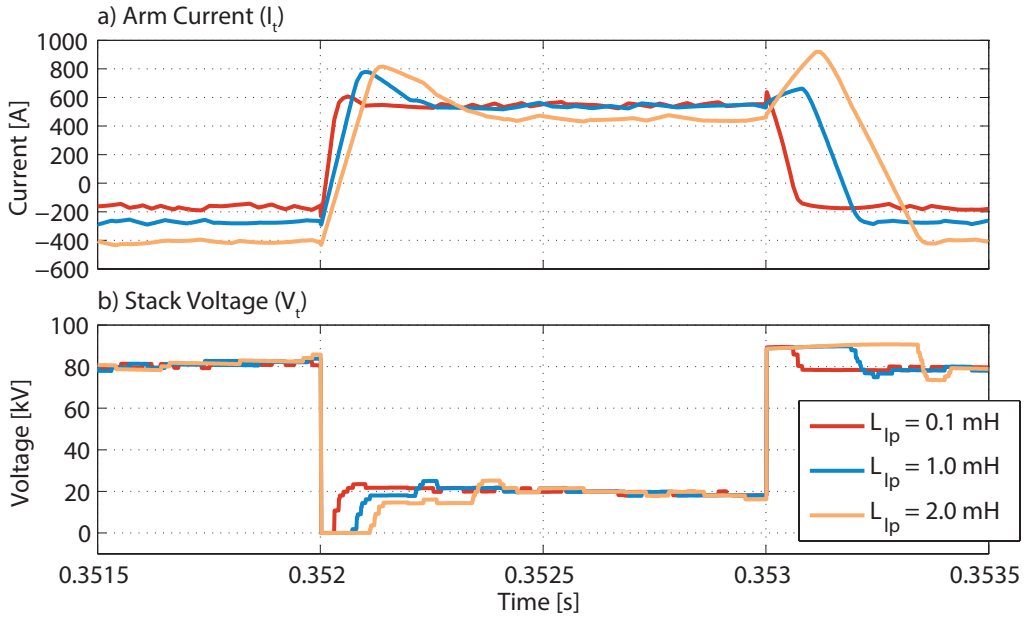

Figure 7.25: Top arm current and stack voltage for range of transformer leakage inductances, for $\kappa_s = 0.3$, $L_{t,b} = 0.8mH$ and $\zeta_{cm} = 0.1$.

Peak-to-peak current magnitude

Finally, the time taken for the arm current transitions also depends on the magnitude of the AC current, i.e., the ΔI. By reducing the transformation-ratio of the stacks ($\kappa_s \rightarrow 0.5$) the AC current magnitude is reduced, as the power level is kept constant, because the primary voltage is raised.

As the transformation-ratio is reduced, the voltage available to the stacks to control the current transitions decreases, as shown in figure 7.26. Here the results for (7.26) to (7.29) are shown with respect to κ_s for a fixed control margin of 10%. The arm current transitions for a power transfer from HV1 to HV2 will be the slowest as the voltages available for these transitions ($\check{V}_{tc}^{+}$, $\hat{V}_{bc}^{+}$, $\hat{V}_{tc}^{-}$ and $\check{V}_{bc}^{-}$) are the smallest in magnitude. As the transformation-ratio is reduced, the magnitude of $\check{V}_{tc}^{+}$ and $\check{V}_{bc}^{-}$ significantly decreases, thereby reducing the voltage that can be applied across the inductive network. Therefore the ramp-rate of the arm current will be lower. This can be observed in figure 7.14 where it could be noticed that the rate of change of the arm current is significantly lower at $\kappa_s = 0.3$ than at higher transformation-ratios. Simply operating the converter with a lower transformation-ratio will therefore not yield quicker arm transitions.

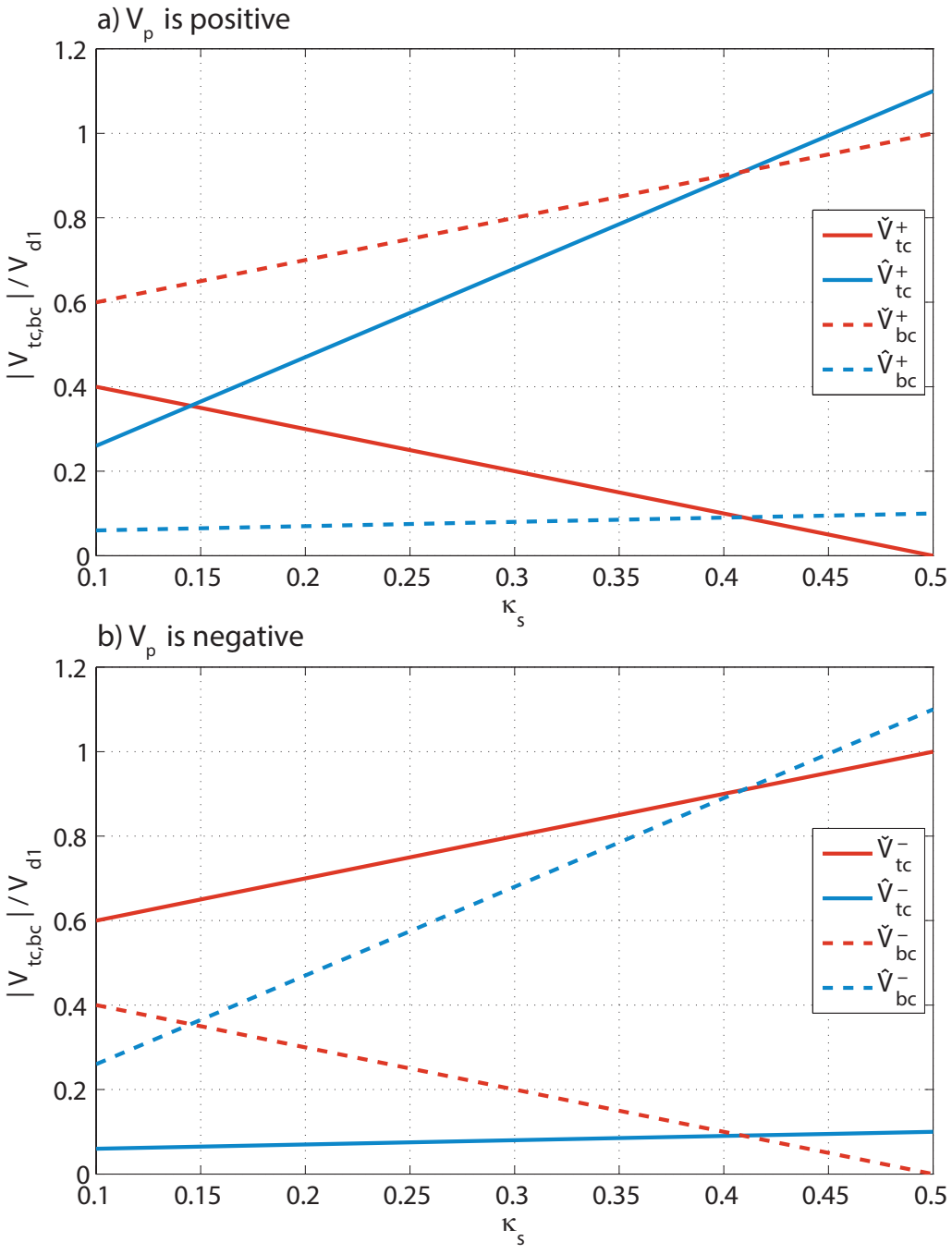

Figure 7.26: Voltage limits relevant for current transitions with respect to transformation-ratio (κ_s), for $\zeta_{cm} = 0.1$.

7.2.2 Filter Requirements

The previous section explored the operation of the stacks of cells and the resulting arm currents. As this converter is intended as a single phase design, the use of square-waves to minimise the filter requirements on the HV2 side have been advocated. As the stacks have a limited voltage capability, the AC current component has a finite rise and fall time. The length of these transition times will also affect the currents flowing into the DC links and therefore directly affect the filter requirements.

Figure 7.27 shows the DC currents for both DC connections without any DC side filter (i.e., without any DC inductance and resistance). The DC side capacitors were included as they are critical to the operation of the converter. A DC cable was not modelled in this scenario, but it would mainly add additional line capacitance, thereby improving the result. From this point of view the results shown here is the "worst-case scenario".

The results shown are for $\kappa_s = 0.3$ and two different control-margins (ζ_{cm}): 25% presents the control margin at which the transition times are equal and the overshoot of the arm currents is minimal. At $\zeta_{cm} = 10\%$ significant overshoots occur combined with a lengthy transition period, the effect of which can clearly be seen in graph a): the DC current is characterised by large spikes every half cycle (for 500 Hz that is 0.001 s). The increased transition times for the lower control-margin can also be noted in the HV2 DC current in graph b), which shows longer troughs in the current.

Such currents are clearly in need of filtering to meet strict limitations placed on the current and voltage ripple being fed into the DC link. There are no general numbers for tolerable limits for the DC side published by the ENTSO-E or the BSI as of yet, but we can make some educated assumptions about them, for the purpose of designing the DC filters. The design procedure starts with sizing the DC side capacitor, which forms part of the DC filter, followed by the remaining passive components.

DC side capacitors

The DC side capacitors can be sized independent of the filtering requirements. By way of an example, the HV1 side capacitors form part of the return path for the AC component of the arm currents. This means that, although they will not suffer from an energy drift, that would charge or discharge them, they will endure an energy deviation. This can be estimated by integrating the instantaneous power of the capacitor as per (7.31), where V_c represents the voltage across the capacitor and I_c the current flowing through it. The energy deviation will cause the voltage across the capacitor to deviate, creating a voltage ripple. The capacitance should be chosen so as to keep this voltage ripple within tolerable

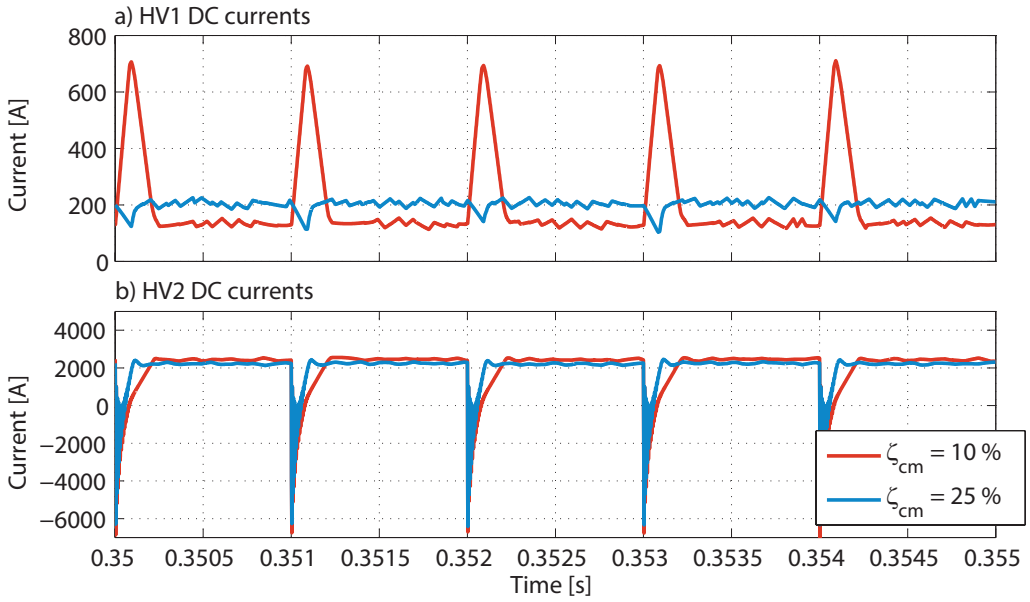

Figure 7.27: DC currents for HV1 and HV2 for two control-margins at a transformation-ratio of 0.3, for a power transfer from HV1 to HV2.

limits.

$$E_c(t) = \int_0^{T_0} V_c(t) I_c(t) \mathrm{d}t \tag{7.31}$$

The nominal energy in the HV1 capacitors (E_c) can be defined as per (7.32). Similarly the maximum and minimum energies can be defined in terms of the voltage deviation for HV1 (γ_1) from the nominal capacitor voltage (V_{c1}) as per (7.33) and (7.34). The capacitance C_1 should then be calculated such that the instantaneous capacitor energy (E_{c1}) neither pass $\hat{E}_{c1}$ nor fall below $\check{E}_{c1}$.

$$E_{c1} = \frac{1}{2} C_1 V_{c1}^2 \tag{7.32}$$

$$\begin{aligned} \hat{E}_{c1} &= \frac{1}{2} C_1 \hat{V}_{c1}^2 \\ &= \frac{1}{2} C_1 V_{c1}^2 \left(1 + \gamma_1\right)^2 \end{aligned} \tag{7.33}$$

$$\begin{aligned} \check{E}_{c1} &= \frac{1}{2} C_1 \check{V}_{c1}^2 \\ &= \frac{1}{2} C_1 V_{c1}^2 \left(1 - \gamma_1\right)^2 \end{aligned} \tag{7.34}$$

As the current flowing through the capacitor is a symmetrical square-wave and the nominal voltage across it is the DC terminal voltage, we can define $I_{c1}(t)$ and $V_{c1}(t)$ as per (7.34) and (7.35) respectively.

$$\begin{aligned} I_{c1} &= \frac{I_p(t)}{2} \\ &= \frac{I_{d1}}{2\kappa_s} \end{aligned} \tag{7.35}$$

$$V_{c1} = \frac{V_{d1}}{2} \tag{7.36}$$

Using (7.32) with (7.34) and (7.35) we can find expressions that estimate $\hat{E}_{c1}$ and $\check{E}_{c1}$ as shown in (7.37) and (7.38) respectively.

$$\begin{aligned} \hat{E}_{c1} &= E_{c1} + \int_0^{\frac{T_0}{4}} \frac{P_1}{2\kappa_s} \mathrm{d}t \\ &= E_{c1} + \frac{P_1}{4f\kappa_s} \\ &\because f = \frac{1}{T_0} \end{aligned} \tag{7.37}$$

$$\begin{aligned} \check{E}_{c1} &= E_{c1} - \int_0^{\frac{T_0}{4}} \frac{P_1}{2\kappa_s} \mathrm{d}t \\ &= E_{c1} - \frac{P_1}{4f\kappa_s} \end{aligned} \tag{7.38}$$

The equations (7.37) and (7.38) can be used along with the expression for E_{c1} given in (7.32) to calculate the expressions for the capacitance, as shown in (7.39) and (7.40). From the expressions it can be noted that the capacitance due to $\check{E}_{c1}$ ($\check{C}_1$) will be marginally larger to maintain the voltage ripple limitations, as its denominator will be slightly smaller. Equation (7.38) can therefore be used to provide a value for the DC side capacitance. The results for the sample system for a range of γ_1 and various transformation-ratios are shown in figure 7.28. The required capacitance can be seen to rise quickly as the tolerable ripple magnitude is reduced. Increasing the transformation-ratio of the stacks ($\kappa_s \to 0$) further increases the required capacitance as the magnitude of the AC current flowing through the capacitors increases.

$$\hat{C}_1 = \frac{P_1}{4f\kappa_s V_c^2 \left(2\gamma_1 + \gamma_1^2\right)} \tag{7.39}$$

$$\check{C}_1 = \frac{P_1}{4f\kappa_s V_c^2 \left(2\gamma_1 - \gamma_1^2\right)} \tag{7.40}$$

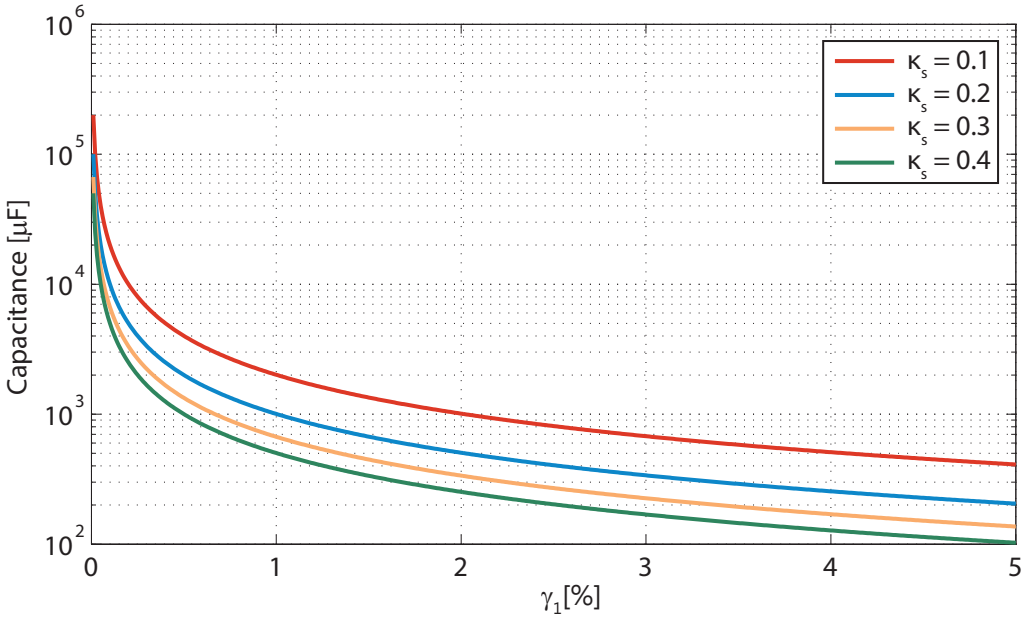

Figure 7.28: HV1 DC capacitance as a function of tolerable voltage deviation (γ_1).

The filter on the HV2 side can be sized in a similar manner, starting with the DC capacitor. The difference to the HV1 side is in the method of determining the current flowing through the DC capacitor. On the HV1 side the current could be estimated as it is the return path for the arm current. On the HV2 side it solely depends on the AC component due to the imperfect AC current transitions. This can be found from simulation results by subtracting the mean value from the measurement.

These current measurements can then be used, along with (7.31), to find the maximum ($\hat{\epsilon}$) and minimum ($\check{\epsilon}$) energy deviation of the capacitor. Using (7.41) and (7.42) the capacitance for a particular voltage ripple (γ_2) can be found for both energy deviation values. Figure 7.29 shows the results for the test system, using control-margins of both 10 and 25%, for a range of γ_2. It can be noted that in this case the energy rise ($\hat{\epsilon}$) requires the larger capacitance and therefore should be considered as the minimum possible HV2 DC capacitance.

$$\hat{C}_2 = \frac{2\hat{\epsilon}}{V_{d2}^2\left((1+\gamma_2)^2 - 1\right)} \tag{7.41}$$

$$\check{C}_2 = \frac{2\check{\epsilon}}{V_{d2}^2\left((1-\gamma_2)^2 - 1\right)} \tag{7.42}$$

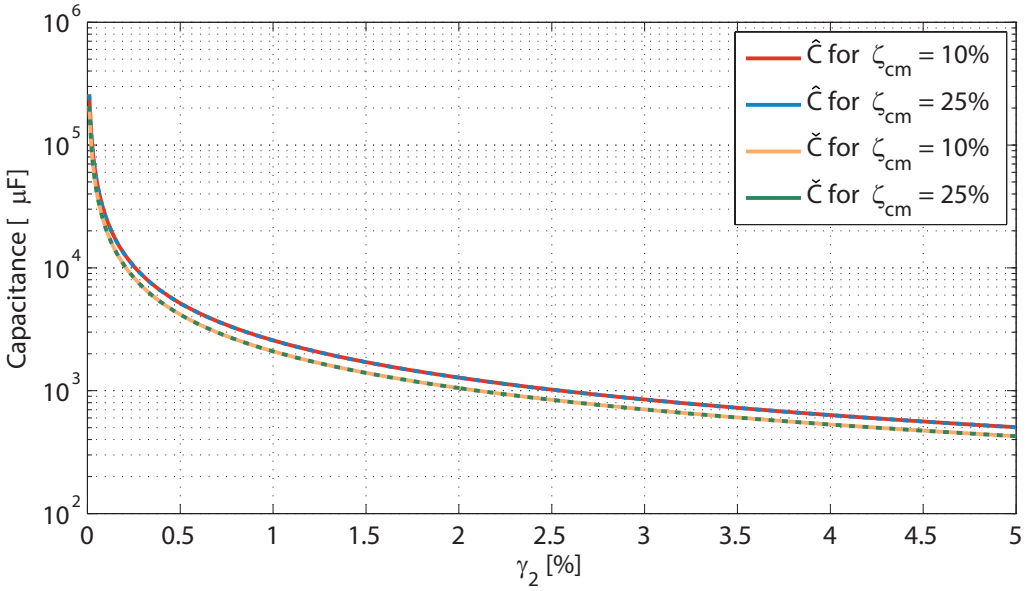

Figure 7.29: HV2 DC capacitor size for varying ripple margins (γ_2), for system operating with ζ_{cm} of 10 and 25%.

DC Filter Inductance and Resistance

The selection of the DC inductance and resistance depends on the type of filter which is to be implemented. The parallel arrangement, as shown in figure 7.30, forms a low-pass filter. For DC/AC applications notch filters are often considered. These contain a series RL arrangement, which means that the entire DC current will flow through the filter's resistance, making it more lossy than the low-pass filter arrangement: in this the resistor is in parallel to the resistor and therefore conducts significantly less current.

Since this section is aimed to illustrate the trade-offs associated with the filter design, we will focus on the low-pass filter arrangement. It is however acknowledged that this may not be the best DC filter, but will be shown to be more than adequate for this converter. The transfer function of the low-pass filter is shown in (7.43) along with the expressions

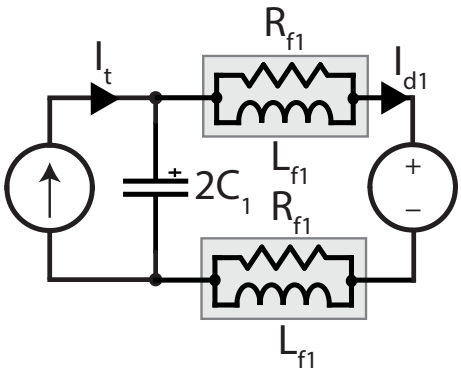

Figure 7.30: Low pass filter used on HV1 DC side.

for its corner-frequency (f_n) in (7.44) and quality factor (Q) in (7.45).

$$\begin{aligned} H(s) &= \frac{I_{d1}}{I_t} \\ &= \frac{s\frac{L_f}{R_f} + 1}{s^2 L_f C + s\frac{L_f}{R_f} + 1} \end{aligned} \tag{7.43}$$

$$: f_n = \frac{1}{2\pi\sqrt{L_f C}} \tag{7.44}$$

$$: Q = \frac{R_f}{2\pi f_n L_f} \tag{7.45}$$

The capacitor will already have been chosen based on the permissible voltage deviation across it. By setting a suitable corner-frequency, (7.44) can be used to find the required filter inductance. The corner-frequency has to be chosen based on the harmonic content of the current, which is illustrated in figure 7.31. Graph a) (top) shows the frequency content of the HV1 DC current and graph b) (bottom) shows the same for HV2, for the control-margin settings for which the currents have been introduced earlier (figure 7.27). The harmonics are placed at regular intervals of 1000 Hz for both currents. For a control-margin of 10% the harmonic content can be seen to be substantial for both currents, peaking at 63.5% at 1000 Hz in the case of I_{d1}. When the control-margin is increased to 25% the harmonic content drops significantly in the HV1 DC, down to a peak of 5.5% at 1000 Hz, but less so for the HV2 DC current.

This is because the harmonic content on the HV1 side is mainly due to a DC current component which is common to both stacks during the transition periods. The AC current is fully internal to the cell stacks and the and the DC side capacitors and will therefore not directly affect the harmonic content. The DC current on the HV2 side however is the

rectified version of the AC current flowing through the transformer and is thus affected by the imperfect current transitions. These are improved with an increasing control-margin but still exist.

From the FFT results it can be concluded that a corner-frequency of less than 1000 Hz is required to sufficiently attenuate the harmonics. Using (7.44) a range of results for the filter inductance are presented in figure 7.32 for different DC side capacitors. As the corner frequency is moved closer to 0 Hz the inductance required quickly rises. The DC capacitor size chosen also significantly affects the inductance value, with a larger capacitance allowing for a smaller inductor to be used. Trading-off the size of the inductor by allowing for a larger capacitor may be beneficial as the conduction losses tend to be smaller in a capacitor than those in an inductor. At the same time a smaller voltage-ripple is achieved as well. Even with a relatively small DC side capacitor (100 μF) the required filter inductance can be kept to within a few milli-Henries.

The effect of choosing a smaller corner-frequency can be seen in figures 7.33 and 7.34. Both graphs show the effect of the filter with varying corner-frequencies on the DC current. The first (figure 7.33) does this for a converter operating with a control-margin of just 10%. It shows that because of the significant harmonic content, the corner frequency ought to be as low as under 100 Hz to maintain a sufficiently small current ripple. Figure 7.34 shows the filtered DC current for a system using $\zeta_{cm} = 0.25$. As the harmonic content is significantly smaller in magnitude, the corner-frequency of the filter can be larger, whilst keeping the current-ripple to within acceptable limits. Therefore a larger control-margin allows the use of a higher corner-frequency which in turn reduces the size of the DC filter inductance.

Once a corner-frequency has been chosen the filter's resistance can be calculated using (7.45), depending on the quality-factor of the filter. The quality-factor stipulates the attenuation (or magnification as may be) of the corner-frequency. As such, if $Q > 1$, care should be taken not to select a corner-frequency which has a significant magnitude in the frequency-spectrum of the DC link current. A larger quality-factor will lead to a larger resistor, increasing the resistive losses incurred in it, as shown in figure 7.35. An increasing corner-frequency significantly reduces the size of the required resistance for a constant quality-factor.

The effect of different quality-factors on the filtered current can be seen in figures 7.36 and 7.37. The first displays result for a system with $\zeta_{cm} = 10\%$ and the latter for one with $\zeta_{cm} = 25\%$. The current of the system with a relatively small control-margin can be seen to require a relatively large quality-factor to be smoothed out to within tolerable limits. Whilst this will lead to a small resistance, it means that some frequencies will be

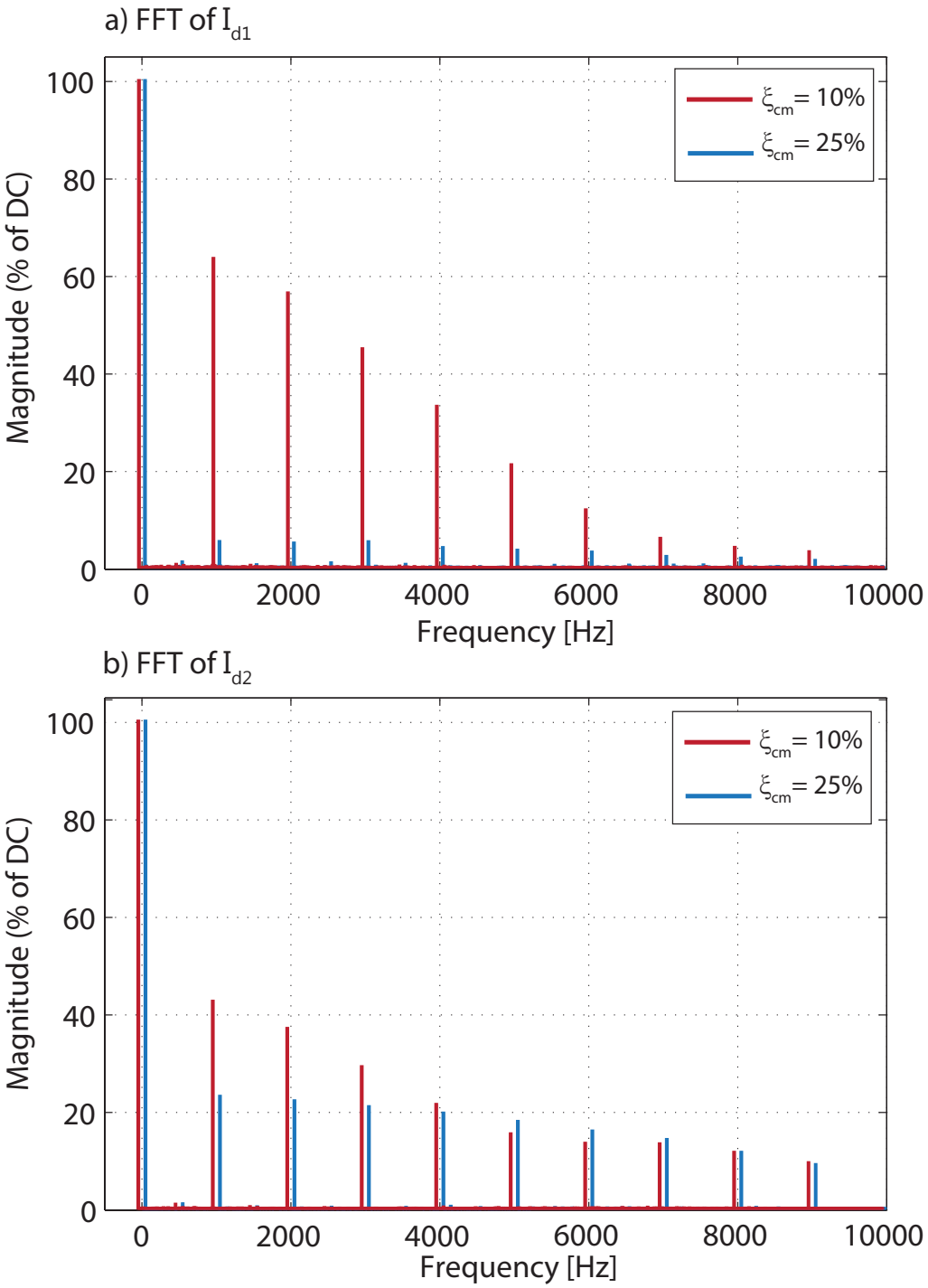

Figure 7.31: Magnitude of harmonics in unfiltered DC side currents for operation with different control-margins.

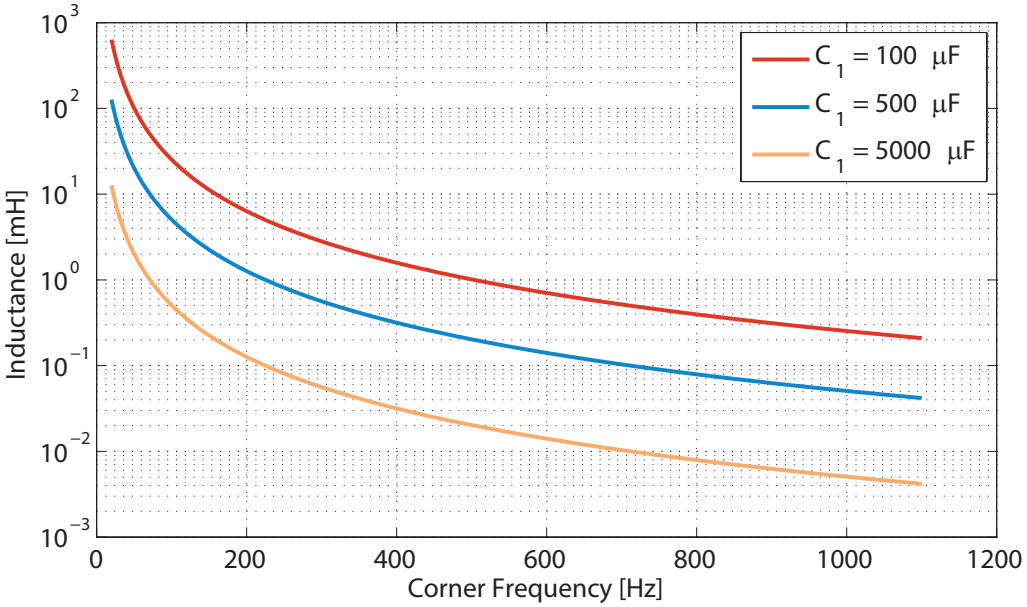

Figure 7.32: Required HV1 DC filter inductor size with respect to filter's corner frequency, for different DC capacitor sizes.

amplified by the filter. The current of the system with a control-margin of 25% could be operated with a $Q < 1$, avoiding this danger.

We can thus summarise the design process of the DC side low-pass filter with the following trade-offs:

- Smaller f_n leads to a larger L_f and R_f.
- Larger C_1 reduces required size of L_f.
- Larger Q reduces R_f but with danger of amplifying some frequencies if $Q > 1$.

An increasing inductor size cannot only become cumbersome in terms of its physical dimensions, due to its magnetic core, but also tends to become more lossy. The losses incurred in capacitors tend to scale more favourably than those incurred in inductors. Therefore when it is possible to reduce the size of an inductor by increasing a capacitor, it should be regarded as a favourable trade-off.

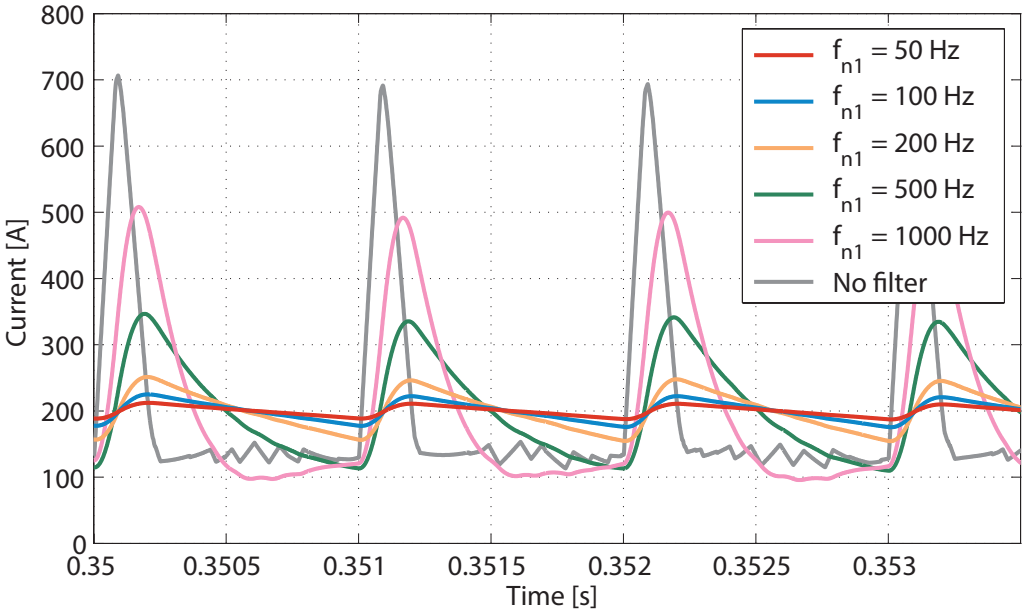

Figure 7.33: Effect of filter on HV1 DC current, where $\zeta_{cm} = 0.1$, for varying corner-frequencies, for a filter with $Q = 0.707$ and $C_1 = 100\mu F$.

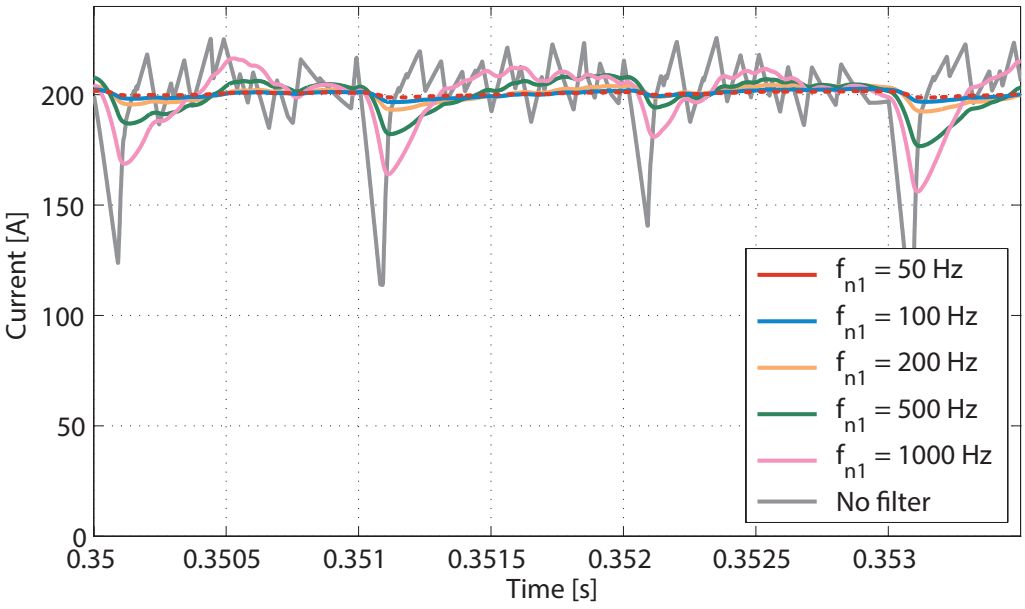

Figure 7.34: Effect of filter on HV1 DC current, where $\zeta_{cm} = 0.25$, for varying corner-frequencies, for a filter with $Q = 0.707$ and $C_1 = 100\mu F$.

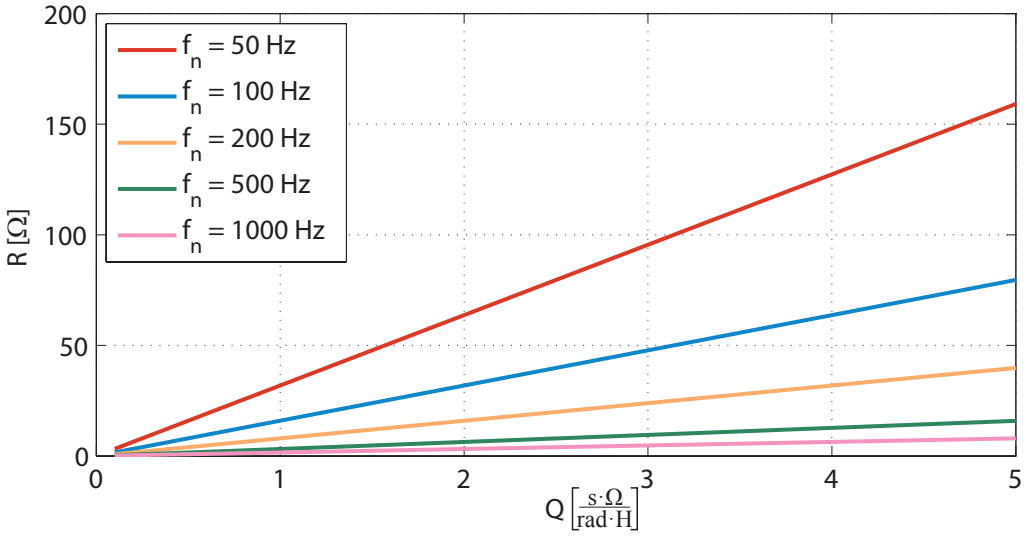

Figure 7.35: Filter resistor size for different corner-frequencies with respect to the quality-factor (Q), for $C_1 = 100\mu F$.

7.3 Chapter Summary: Design considerations for square-wave modular DC/DC

The DC/DC converter discussed in this chapter is of a single phase design. As such square-waves have been proposed to be used for the internal AC connection as they can be rectified back into DC relatively easily. Ideal square-waves would thus need no significant output filter. This is only the case however if the AC arm current component is transitioned from it positive to its negative peak instantaneously (and vice versa from its negative to its positive peak).

Realistically this is not possible as the rate of change of the arm current is limited by the series inductance and the voltage capability of the cell stacks. This limitation means that the slower the transition occurs the higher the filter requirements are. The system can be modified in two ways to deal with this problem: first, the voltage capability in the stacks can be raised using the control-margin variable (ζ_{cm}). Second, the series inductance can be reduced.

The inductance in the AC current path consists of two main component, stray inductances aside: the arm and the transformer's leakage inductances. It has been shown to be counter productive to lower the former: although the rise time is increased the arm current also suffer from a significantly increased current overshoot after the transition. This is because during the transition the cell stacks have to ramp their respective arm

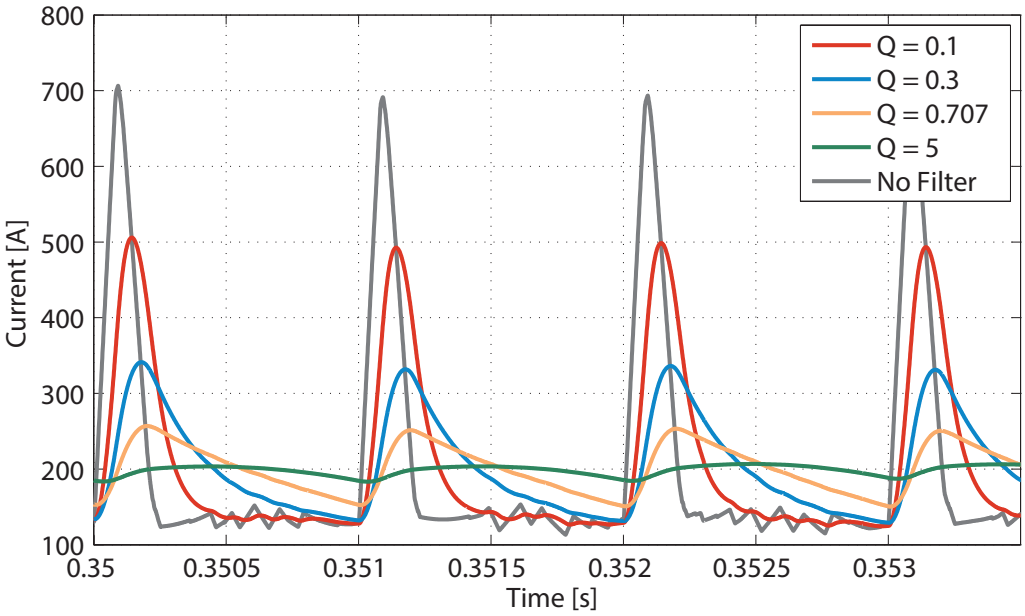

Figure 7.36: Effect of filter on HV1 DC current, where $\zeta_{cm} = 0.1$, for different quality-factors (Q) with a constant corner-frequency of 220 Hz.

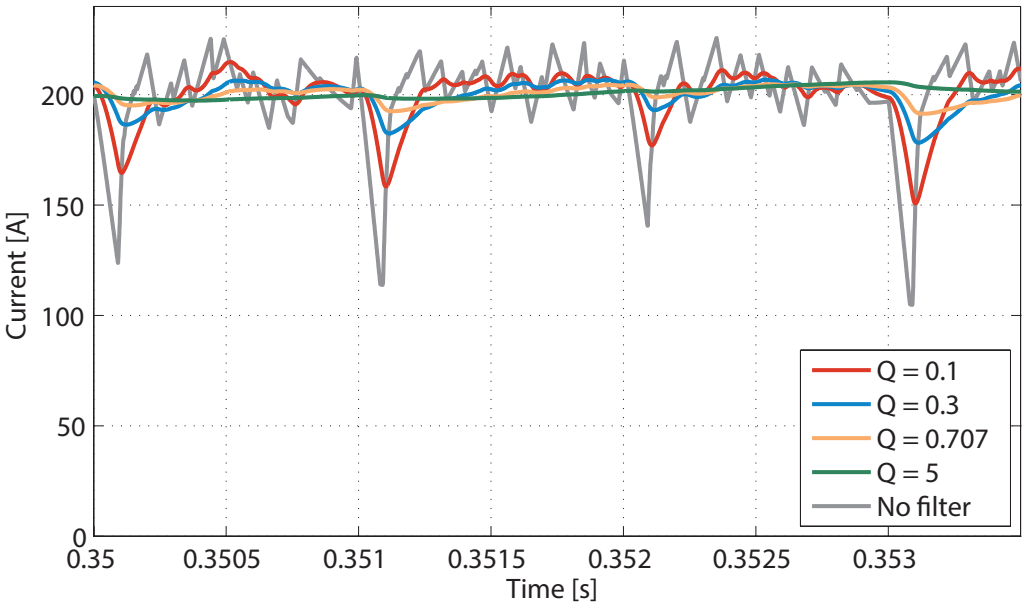

Figure 7.37: Effect of filter on HV1 DC current, where $\zeta_{cm} = 0.25$, for different quality-factors (Q) with a constant corner-frequency of 220 Hz.

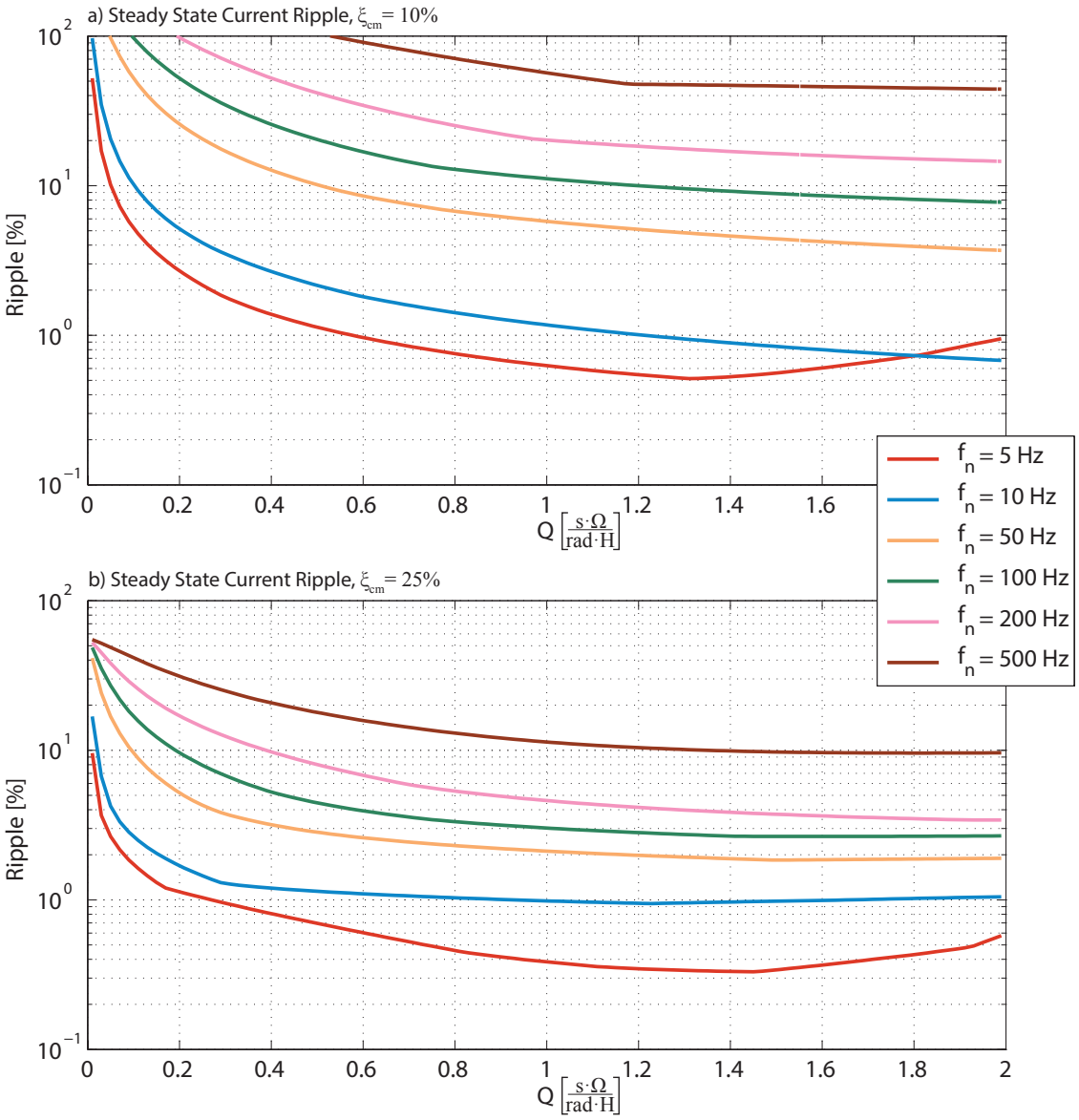

Figure 7.38: Graphs showing the steady state ripple of the filtered HV1 DC current for $\zeta_{cm} = 10\%$, graph a), and 25%, graph b) ($C_1 = 500\mu F$).

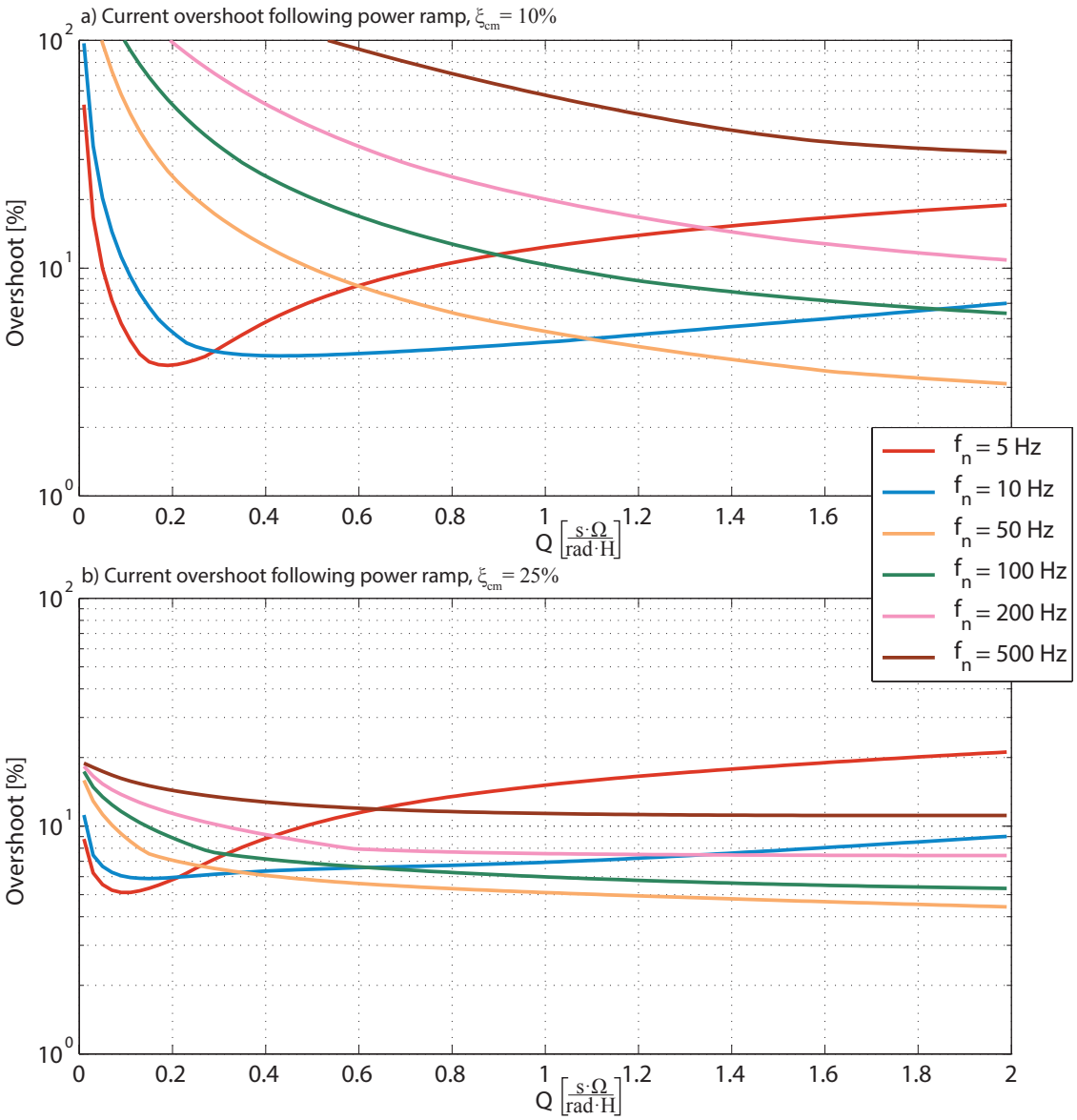

Figure 7.39: Graphs showing the overshoot following a power ramp of the filtered HV1 DC current for $\zeta_{cm} = 10\%$, graph a), and 25%, graph b) ($C_1 = 500\mu F$).

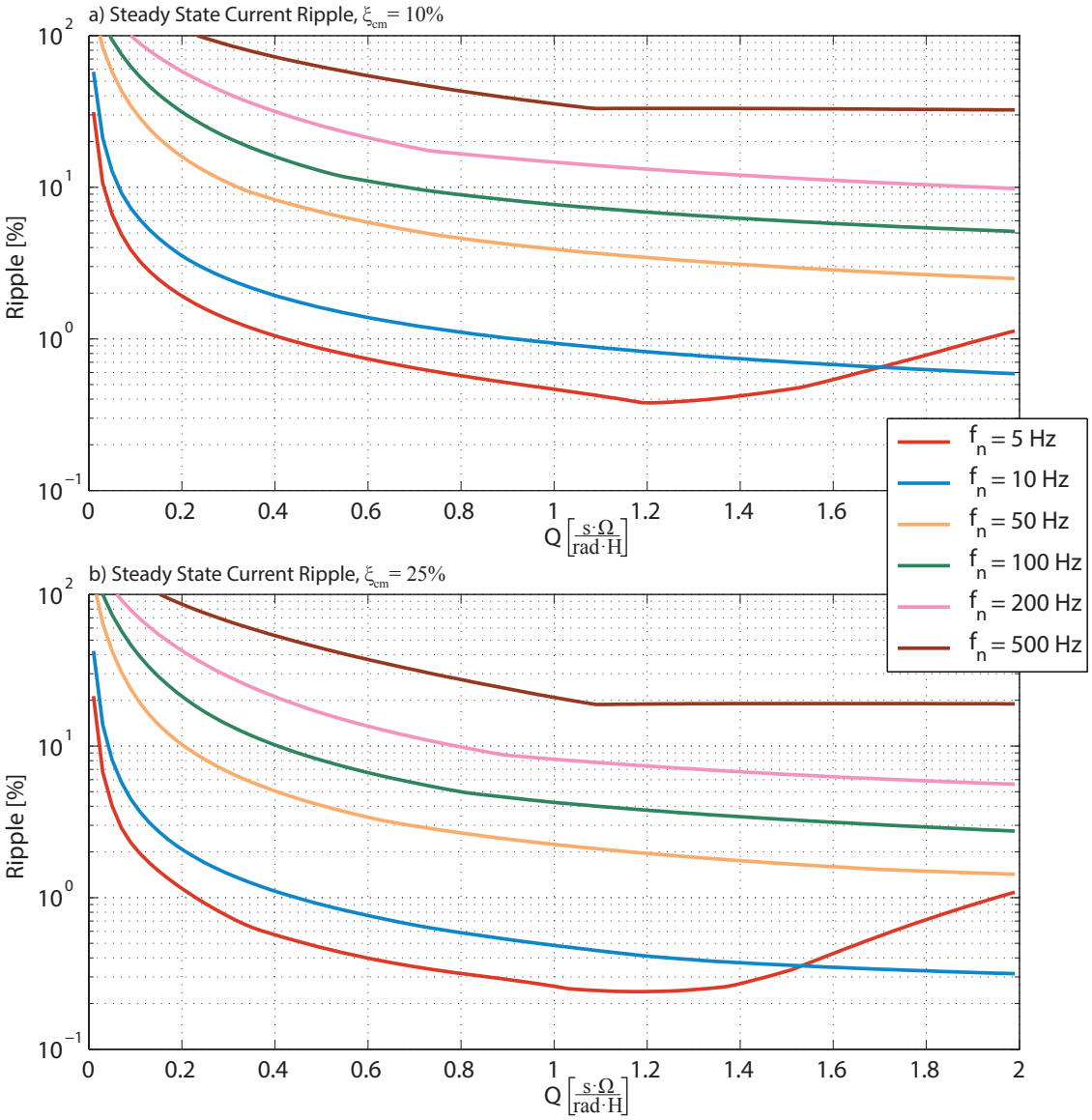

Figure 7.40: Graphs showing the steady state ripple of the filtered HV2 DC current for $\zeta_{cm} = 10\%$, graph a), and 25%, graph b) ($C_2 = 500\mu F$).

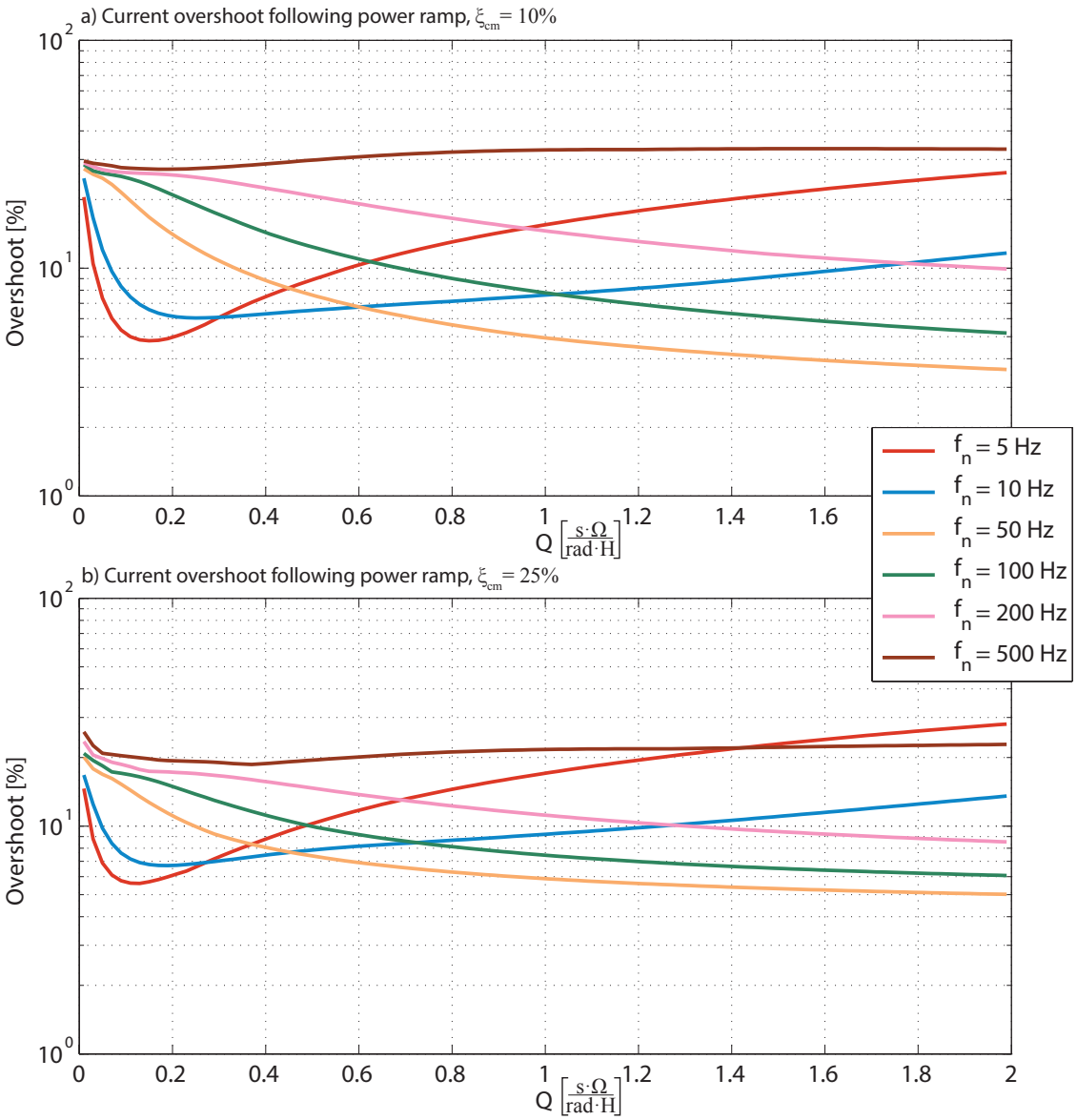

Figure 7.41: Graphs showing the overshoot following a power ramp of the filtered HV2 DC current for $\zeta_{cm} = 10\%$, graph a), and 25%, graph b) ($C_2 = 500\mu F$).

currents in opposite directions (because the primary current is split equally between both arms). During the transition time therefore there exists a voltage potential across the arm inductors which causes a current common to both arms to flow. As the arm inductors are the only inductance in the path of this current, lowering their impedance also increases the rate of rise of this undesired arm current.

Alternatively the leakage inductance could be reduced as much as possible. This has been shown to yield very good results. High power (i.e., mega Watts range) transformers tend to be relatively large in size making it more likely for them to have larger leakage inductances. Design efforts for this power range have to date not tried to reduce the leakage inductance as mush as possible, although similar efforts have been made in low power applications. It remains to be investigated to what extend a high power transformer can be designed to reduce the leakage inductance as, although temperature limits inside the transformer as well as packing factors and high voltage insulation distances are sure to limit these efforts.

Increasing the voltage capability of the cell stacks is therefore the most feasible solution, as this can be done relatively easily by adding more cells. The control-margin ζ_{cm} measures the added voltage capability. Depending on the transformation-ratio of the stack, a certain control-margin has been recommended which ensures that the rise and fall times of the AC current are the same. This has been shown to significantly reduce the filter requirements, due to the imperfect current transitions.

Chapter 8

Circuit component variations in SW-M DC/DC

The worth of a power converter is hugely affected by two important aspects: its efficiency and its physical size. Usually there are aspects of the converter which can be manipulated to trade one of those two aspects against the other. In this chapter we will look at such loss-volume trade-offs and offer some numbers with respect to the overall system performance of the shunt connected primary DC/DC converter, introduced previously.

Any results presented in this chapter are for the test system presented in chapter 7, table 7.1. Individual parameters may be changed but this will be noted in the text.

8.1 Passive Component Sizing

This section will present the effects the size and capacity of the passive components in the converter have on its performance. In the previous chapter the arm inductors and to some extent the transformer, as well as the DC side filter components, have been discussed. Those discussions focused on the components' effects on the basic operation of the circuit. They will be briefly revisited here to investigate how those changes can also affect the performance of the converter. Furthermore to this the sizing of the cell capacitors will be investigated here.

8.1.1 Cell Capacitors

The cell capacitors can make up a significant portion of the total volume of the cell, as has been illustrated in 3.3.1. The sizing method used is similar to that used in the

front-to-front topologies: the cell capacitor experiences an energy deviation during a cycle which results in a voltage deviation across it. The minimum capacitance is limited by the maximum voltage deviation that is allowed to occur.

Using the basic formula, as illustrated before in (7.31), the energy deviation of the stacks can be found by integrating their respective arm current with the stacks' generated voltage. The voltages generated by the top and bottom stacks are independent of the power flow direction and are re-illustrated in (8.1) and (8.2).

$$V_t(t) = V_{d1}\left(\frac{1}{2} + \kappa_s \,\mathrm{sqw}\left(\frac{t}{T_0}\right)\right) \tag{8.1}$$

$$V_b(t) = V_{d1}\left(\frac{1}{2} - \kappa_s \,\mathrm{sqw}\left(\frac{t}{T_0}\right)\right) \tag{8.2}$$

$$\therefore \ \mathrm{sqw}\left(\frac{t}{T_0}\right) = \begin{cases} 1 & \text{if } 0 \leq t < \frac{T_0}{2}, \\ -1 & \text{if } \frac{T_0}{2} \leq t < T_0. \end{cases}$$

The arm currents can be similarly defined, but depend also on the direction of the power flow, as illustrated in (8.3) and (8.4).

$$I_t(t) = \mathrm{sgn}(P_1)\, I_{d1}\left(1 + \frac{1}{2\kappa_s}\,\mathrm{sqw}\left(\frac{t}{T_0}\right)\right) \tag{8.3}$$

$$I_b(t) = \mathrm{sgn}(P_1)\, I_{d1}\left(1 - \frac{1}{2\kappa_s}\,\mathrm{sqw}\left(\frac{t}{T_0}\right)\right) \tag{8.4}$$

$$\therefore \ \mathrm{sgn}(P_1) = \begin{cases} 1 & \text{if power transferred from HV1 to HV2,} \\ -1 & \text{if power transferred from HV2 to HV1} \end{cases}$$

Since the energy of the stack is stored across all the stacks' cells, the nominal (steady-state) energy of a stack can be defined, as shown in (8.5), as the product of the energy contained within each cell. The voltage V_c denotes the nominal cell voltage.

$$E_{s0} = \frac{1}{2} C_c N_c V_c^2 \tag{8.5}$$

As both the current and the voltage experienced by each stack are square-waves, the energy-deviation will take the form of a triangle-wave. The energy controller will ensure that the average value of this triangle-wave will be centred around the nominal stack energy (i.e., $\frac{E_{s0}}{N_c}$), as illustrated in figure 8.1. The figure also illustrates the definitions of the energy deviations $\Delta E_s^{+,-}$ as being the maximum and minimum value above and below the nominal stack energy level.

As the currents and voltages are symmetrical for the top and bottom stack, we need only look at one of them, to find the energy deviations experienced by both stacks. The

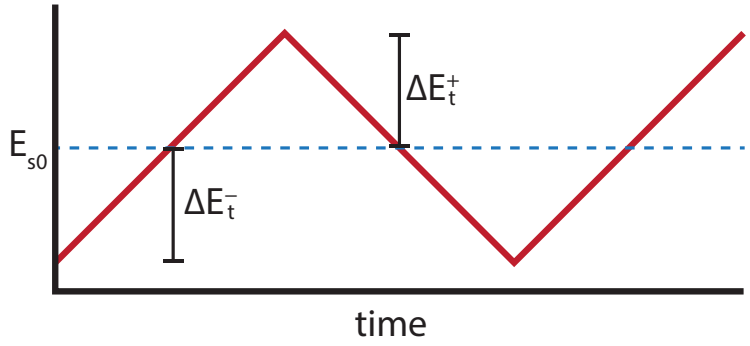

Figure 8.1: Illustration of typical energy deviation in the cell stacks.

energy deviations for the top stack of cells have been derived in (8.6) and (8.7). From the equations it can be noted that they are inversely proportional to the square-wave's frequency and proportional to the power magnitude. As the stack's transformation-ratio increases (i.e., $\kappa_S \to 0$) the energy deviation will quickly increase. It can also be noted that ΔE_t^+ and ΔE_t^- are of equal and opposite value, which is as expected, since the energy-deviation should not contain any energy-drift as explained in section 6.2.1.

$$\begin{aligned}
\Delta E_t^+ &= \int_{\frac{T_0}{4}}^{\frac{T_0}{2}} V_t(t) I_t(t) \mathrm{d}t \\
&= \frac{P_1}{4 f_{AC}} \left(\frac{1}{4\kappa_s} - \kappa_s \right) \qquad (8.6) \\
\Delta E_t^- &= \int_{\frac{3T_0}{4}}^{T_0} V_t(t) I_t(t) \mathrm{d}t \\
&= \frac{P_1}{4 f_{AC}} \left(\kappa_s - \frac{1}{4\kappa_s} \right) \qquad (8.7) \\
&\because f_{AC} = \frac{1}{T_0} \\
&\because P_1 = V_{d1} I_{d1}
\end{aligned}$$

The maximum and minimum energies of the stack can be defined, as shown in (8.9)

and (8.11). These equations make use of the allowed voltage ripple (γ_c) for each cell.

$$\begin{aligned}
\hat{E}_t &= E_{s0} + \Delta E_t^+ && (8.8)\\
&= \frac{1}{2} N_c C_c \hat{V}_c^2 \\
&= \frac{1}{2} N_c C_c V_c^2 (1+\gamma_c)^2 && (8.9)\\
&\therefore \hat{V}_c = V_c(1+\gamma_c) \\
\check{E}_t &= E_{s0} + \Delta E_t^- && (8.10)\\
&= \frac{1}{2} N_c C_c \check{V}_c^2 \\
&= \frac{1}{2} N_c C_c V_c^2 (1-\gamma_c)^2 && (8.11)\\
&\therefore \check{V}_c = V_c(1-\gamma_c)
\end{aligned}$$

The expressions (8.8) and (8.10) can be rearranged to find the minimum capacitances required, to deal with the minimum and maximum energy deviations, as shown in (8.12) and (8.13). The minimum capacitance that should be used is the larger one of either $\hat{C}_c$ or $\check{C}_c$. It should be noted that these values calculate the minimum capacitance and should be used as a guiding figure. They assume a perfect distribution of the energy deviation across all cells. This in effect assumes an infinite cell rotation frequency. Realistically of course this cannot be achieved and therefore some cells will stray above or below the voltage deviation and should therefore be taken into account. The following subsection discuss the effects of varying a number of the parameters of these expressions.

$$\hat{C}_c = \frac{|P_1| \left(\frac{1}{4\kappa_s} - \kappa_s\right)}{2 f_{AC} N_c V_c^2 \left(\gamma_c^2 + 2\gamma_c\right)} \tag{8.12}$$

$$\check{C}_c = \frac{|P_1| \left(\kappa_s - \frac{1}{4\kappa_s}\right)}{2 f_{AC} N_c V_c^2 \left(\gamma_c^2 - 2\gamma_c\right)} \tag{8.13}$$

Effect of voltage deviation margin, γ_c

The cell capacitances required follow an inverse quadratic relationship with respect to the voltage deviation margin. The capacitance estimations using (8.12) and (8.13) for the test system, are shown in figure 8.2. The graph shows the exponentially increasing cell capacitance required for decreasing voltage deviation margin. Using capacitors, which allow a larger voltage ripple, can therefore significantly reduce the cell's capacitance and its volume.

By varying the cell capacitance in the simulation model we can confirm the accuracy

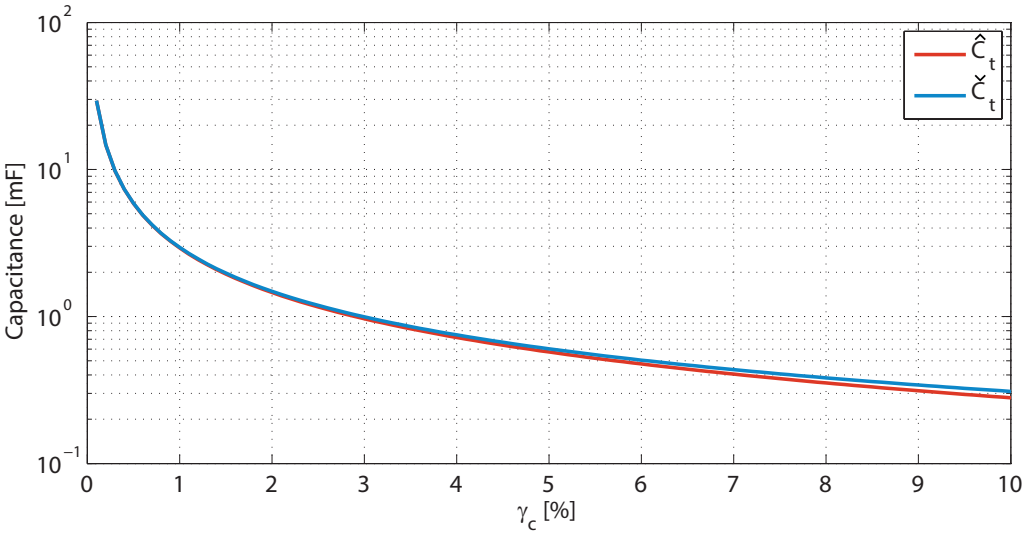

Figure 8.2: Minimum cell capacitance required with varying voltage deviation margin for test system.

of (8.12) and (8.13). Figure 8.3 shows the mean voltage across the capacitor, of all cells in the top stack, for each simulation time-step and different cell capacitance values. Some imperfections around the peaks and troughs can be noted. These are due to the imperfect current transitions of the arm currents. An increasing cell capacitance can be noted to significantly reduce the voltage deviation above and below the nominal cell voltage of 1800 V. Table 8.1 summarises the measurements taken from figure 8.3 and the predicted voltage deviations, as read from figure 8.2. Whilst the trend is confirmed, there exists an error margin between the measurements and the predicted values, with the measured values lying above the predicted ones. This can be attributed to the fact that the actual rotation frequency is limited to $8.2 f_{AC}$, which allows the cells to drift further away from the predicted mean value. The choice of rotation frequency is further discussed in 8.1.1. Furthermore, the imperfect current transition of the square-wave introduces unaccounted for energy deviations. In light of these imperfections in the simulation, the capacitance estimation model can be considered accurate enough, to predict the theoretical minimum cell capacitance.

Effect of stack transformation-ratio, κ_s

The cell stacks' transformation-ratio can be seen to play a significant role in the cell capacitance equations. Figure 8.4 depicts the results for the total stack capacitance, rather than the cell capacitance. As the transformation-ratio changes, so does the voltage

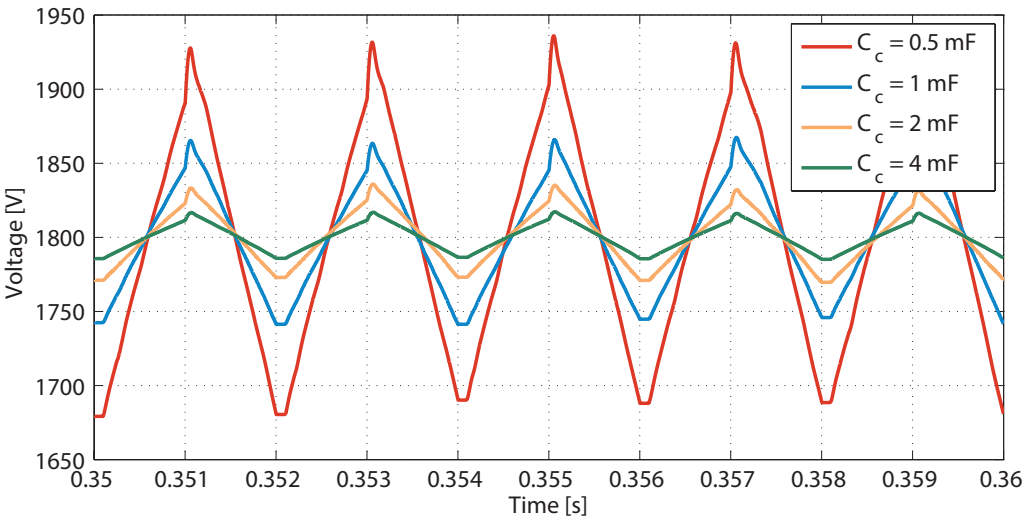

Figure 8.3: Mean cell voltages across all cells in the top stack for different cell capacitances (system's $\zeta_{cm} = 25\%$).

Table 8.1: Voltage deviations of cells for different cell capacitances.

	Measurements				*Predicted*	
$C_c[mF]$	$\Delta V_c^+[V]$	$\Delta V_c^-[V]$	$\gamma_c^+[\%]$	$\gamma_c^-[\%]$	$\gamma_c^+[\%]$	$\gamma_c^-[\%]$
0.5	140	122	7.8	6.8	5.7	6.0
1	69	59	3.9	3.3	2.9	3.0
2	36	30	2.0	1.2	1.5	1.5
4	17	15	1.0	0.8	0.7	0.7

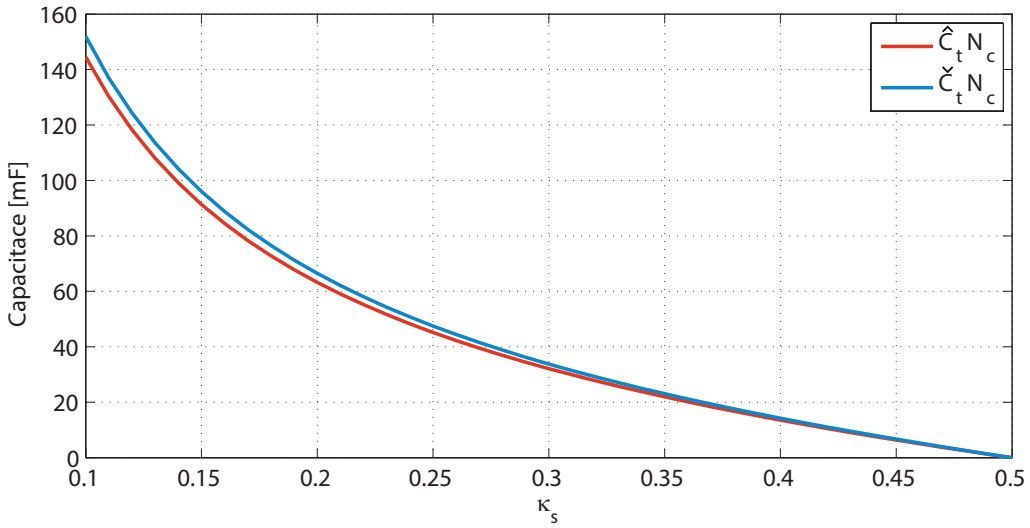

Figure 8.4: Minimum possible stack capacitance for varying transformation-ratio ($\gamma_c = 5\%$).

capability required of the stacks. For a constant nominal cell voltage, this implies that the number of cells will vary also. As the capacitance is an indicator of volume, the whole stack capacitance is considered here.

From the graph it can be seen that as κ_s tends towards zero, the stacks' capacitance tends towards zero also, since the primary voltage at this point has a peak voltage equivalent to the HV1 terminal voltage ($\frac{V_{d1}}{2}$). Therefore the arm current never flows through the capacitors as they are never switched into the conduction path.

Even though a transformation-ratio of 0.5 is technically infeasible with half-bridge cells only, as no voltage capacity would be left to control the currents, the trend indicates that a lower transformation-ratio (i.e., $\kappa_s \to 0.5$) will result in overall smaller capacitors, irrespective of the other system parameters. This equates to a lower volume in the cell stacks due to their capacitance. Conversely it can be noted from the graph that the minimum capacitance increases sharply as the transformation-ratio is increased (i.e., $\kappa_s \to 0$), causing more voluminous stacks of cells.

Effect of square-wave frequency, f_{AC}

The minimum cell capacitance is inversely proportional to the frequency of the square-wave. This intuitively makes sense, since as the frequency increases the time available for the energy to deviate above or below the nominal energy level decreases. The effect of this on the cell capacitance of the test system, and therefore on the volume of the stacks, is

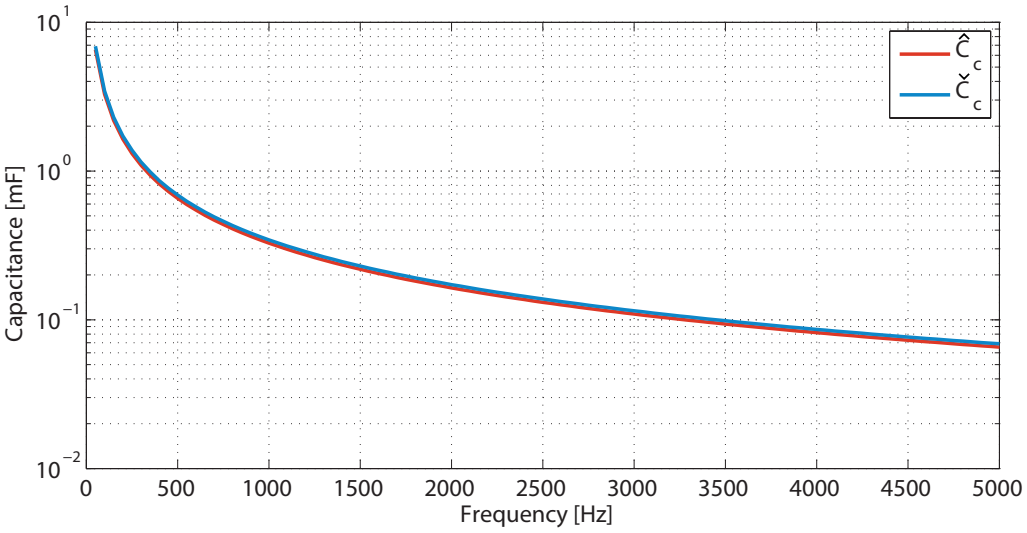

Figure 8.5: Minimum possible cell capacitance for varying square-wave frequency ($\gamma_c = 5\%$).

illustrated in figure 8.5. By increasing the frequency from 500 to 2000 Hz, the minimum cell capacitance is decreased from 689 to 172 μF.

Effect of nominal cell voltage, V_c

The energy stored inside a capacitor scales to the square of the nominal capacitor voltage (i.e., V_c). Assuming that the permissible voltage ripple remains a fixed fraction of the capacitor's voltage, then the minimum cell capacitance scales to the inverse of the square of the cell voltage. This leads to significant reduction in the size of not only the individual cell capacitors, as illustrated in figure 8.6, but also to a marked reduction in total stack capacitance with increasing cell voltage, as shown in figure 8.7. Whether this also leads to a reduction in volume of the cell capacitance depends on how the volume of the capacitor scales with respect to operating voltage, i.e., the energy density of the capacitor.

For the test system it can be noted that whilst increasing the cell voltage beyond 6000 V will yield little decrease in the size of the cell capacitor, the fact that the total number of cells continues to decrease, significantly reductions the total stack capacitance, and therefore its volume. The discontinuous appearance of the results shown, is caused by the step-like increase in the number of cells with respect to a decreasing cell voltage, as the number of cells is always rounded up.

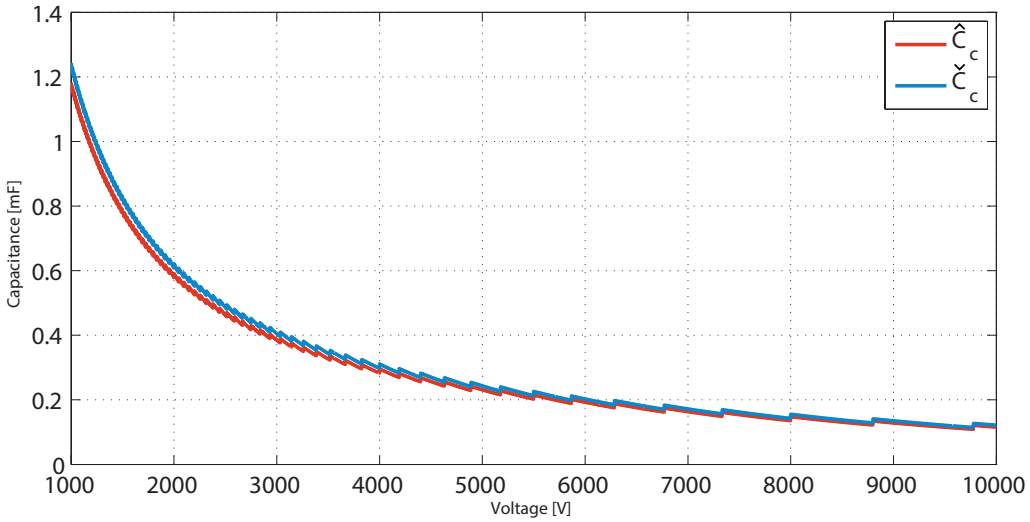

Figure 8.6: Minimum possible cell capacitance for varying nominal cell voltage ($\gamma_c = 5\%$).

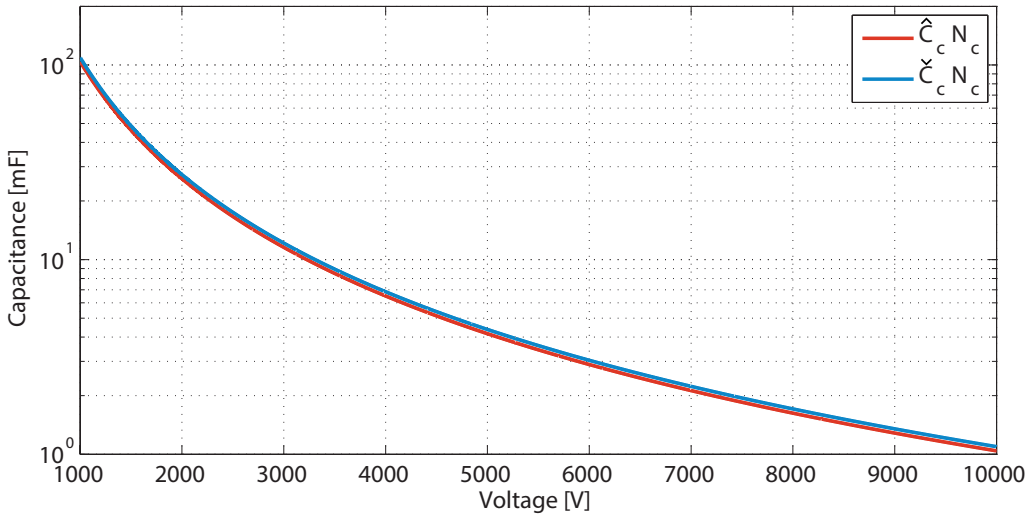

Figure 8.7: Minimum possible total stack capacitance for varying nominal cell voltage ($\gamma_c = 5\%$).

Effect of rotational frequency, f_{cr}

The cell level controller rotates the cells within a stack in and out of conduction throughout the cycle, whilst ensuring at all times that the the required number of cells remain in conduction, to generate the requested voltage across the stack. This is done to spread the energy deviation as evenly as possible across all the cells, ensuring that no one cell significantly over- or under-charges away from the nominal cell voltage.

The number of times the controller rotates the cells is referred to as the cell rotation frequency, denoted f_{cr}, and is expressed in Hertz as a multiple of the AC frequency (f_{AC}. Thus a rotation frequency of $8f_{AC}$ rotates the cell duties eight times per AC cycle. As typically a relatively low multiple of f_{AC} is chosen, from experience, a non integer value tends to work best. This is because over a number of cycles it gradually shifts the time slots when the rotation occurs throughout the cycle.

The minimum cell capacitance equations assume that the rotational frequency is effectively infinite, such that the energy deviation is split equally amongst all cells in a stack, at any point throughout the cycle. The effect of a realistic rotation frequency can be seen in figure 8.8, which illustrates that, whilst the mean cell voltage deviation is as it should be, individual cells deviate further away from the mean. It can be seen that with an increasing rotational frequency the minimum and maximum voltage of any one cell within a stack move closer to the mean across all the cells. An increase in rotational frequency will, however, cause more switching events in the cells, thereby increasing their losses. This is investigated further in the section about the active switching devices in this chapter.

8.1.2 Arm Inductors

The arm inductors are necessary to increase the inductance in the current-paths of the DC current, flowing through both stacks and the AC component flowing through the primary winding. In section 7.2.1 the operational trade-offs involved with varying the size of the arm inductance have been explored: A reduction in the size of the inductance allows for a faster AC current transition, which lowers the required filter size. At the same time, the rate of change of the current increase. To prevent the arm currents from deviating too far from the set reference current, the cell stacks will have to switch cells in and out of the conduction path more often.

Each switching event is also a loss event. Thus as the arm inductance is lowered the switching losses increase also, as illustrated in figure 8.9. In the graph the switching loss is split into its two components, namely the switching losses incurred due to a cell rotation

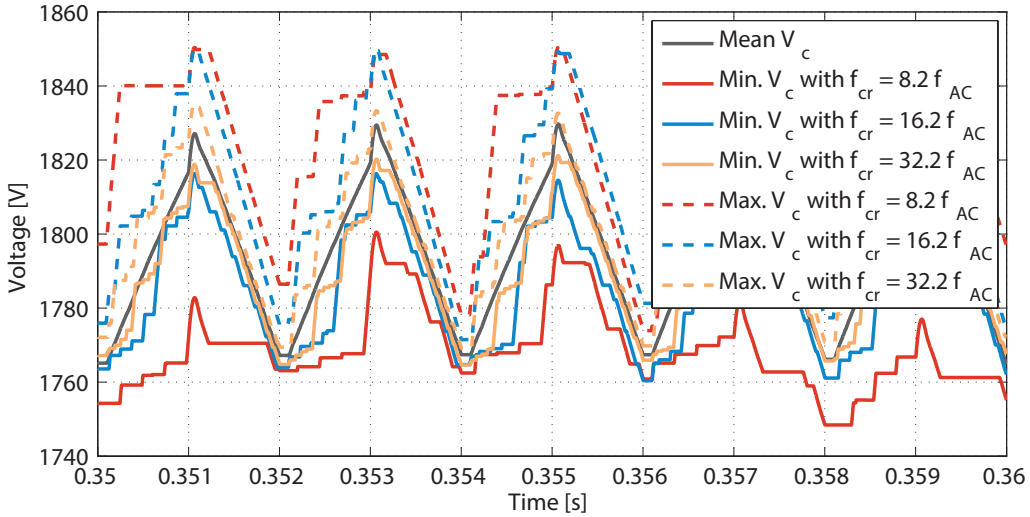

Figure 8.8: Maximum and minimum voltage of any one cell within top stack for different cell rotation frequencies.

event and the losses incurred, because the voltages the stacks are requested to generate have changed. The latter is also referred to as a voltage generation switching loss. The results show that most of the increase in losses is due to an increase in the switching losses incurred due to voltage generation. An increase in arm inductance from 0.8 to 1.2 mH appears to have little effect on the switching losses however.

The reduction in switching losses with increasing inductance have to be weighed against the increase in losses incurred in the inductor. The inductor can be modelled as a Brooks coil (see Appendix C for details of a Brooks coil). To make the results comparable with each other the current density is kept constant for all inductance values. In essence this means the same wire thickness is used. Table 8.2 shows the results for the arm inductors assuming a constant current density of 1 MAm^{-2} in the turns and a packing factor of 50%.

As the inductance is increased the volume of the coil increases as the number of turns increases. This in turn, also causes the losses incurred in the inductor to increase. From the results table it can, however, be noted that relative to the total losses in the cell stack, the inductor contributes only a very small fraction. A size of 0.8 mH for the test system therefore seems like a suitable choice, as it reduces the switching losses, whilst allowing for a small enough inductance to achieve a fast current transition.

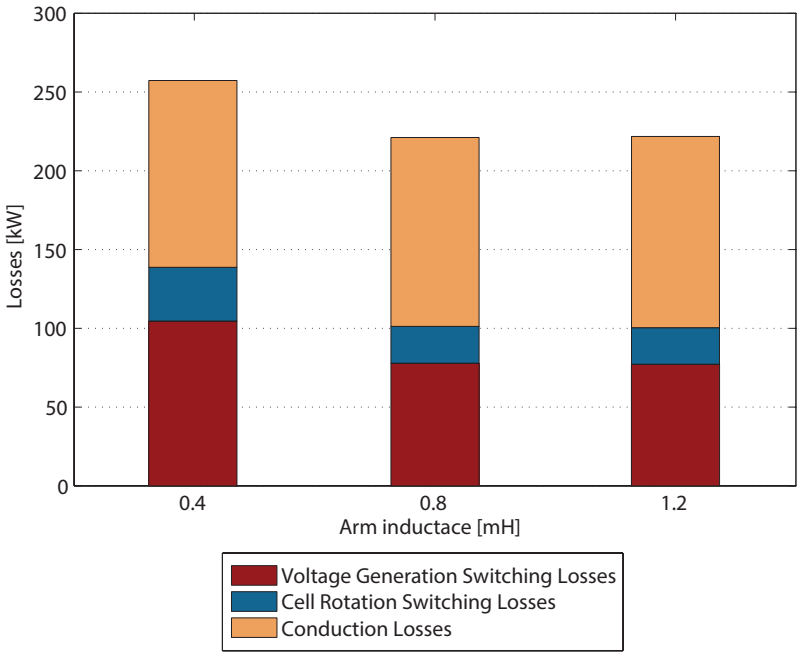

Figure 8.9: Losses incurred in cell stacks with varying arm inductance and control margin ($\kappa_s = 0.3$ and $\zeta_{cm} = 25\%$).

Table 8.2: Arm inductor sizes and losses.

Inductance $[mH]$	Volume $[m^3]$	Losses $[W]$	Fraction of total arm losses
0.4	0.059	450	0.35%
0.8	0.089	690	0.62%
1.2	0.113	894	0.81%

8.1.3 DC Filter

Section 7.3 in chapter 7 provided details for HV1 and HV2 DC filters, for a maximum DC current ripple of 5%. The values for the inductor, resistor and capacitor calculated are used here to illustrate the volume of and losses incurred by the DC filters.

The inductors were designed as Brooks coils, as described in Appendix C. The losses incurred in the capacitor have not been modelled, as they are expected to be comparatively small. To allow for a level comparison between the filters, a common current density in the inductor turns has been chosen at 1 MAm^{-2} which implies a reasonable utilisation of the copper without stressing it too much. The results are summarised in table 8.3 and are per HV filter circuit. The volume of the resistor has not been estimated. The volume of the inductor only includes the volume of the coil, but not that of the insulation clearance required. It could be assumed that the entire inductor and resistor of the filter will be mounted on an insulated platform, as they operate at the DC terminal voltage. As the clearance required for this is fixed, the only aspect that could be optimised is the size of the platform to be insulated, which is indicated by the volume of the inductor.

In the previous chapter the importance of the control margin on the converter's operation has been discussed. It has been shown that by increasing the control margin the size of the filter components can be reduced. The results shown, quantise this reduction in terms of volume of the inductor and the filter's losses. It can be seen that the volume and losses for the HV1 filter are small compared with the losses in the HV2 filter. Whilst the increase in control margin reduces the volume for both filters, the most significant effect in terms of absolute losses, can be noted for the HV2 side, as its losses are reduced by 43 and its volume by 46%. Although the losses on the HV1 side were reduced by 92%, they only constitute 12% of the sum of the HV1 and HV2 losses to begin with.

The reason for the large difference in losses and volume between the HV1 and HV2 sides, are the different RMS currents that each filter experiences: the DC current on the HV1 side is 10 times smaller than that on the HV2 side. This implies that the current density of the inductors on each side should be different. The effect of dropping the current density is illustrated in table 8.4 which shows the results for volume and losses, for the inductors at a current density of 0.5 MAm^{-2}. From the change relative to a current density of 1 MAm^{-2}, it can be noted that the losses drop more slowly than the volume increase.

Table 8.3: Filter sizes and losses.

HV1 Filter, $\zeta_{cm} = 10\%$			
Component	Size	Volume	Loss
Inductor	56.3 mH	0.54 m^3	3.42 kW
Resistor	7.5 Ω	-	0.22 kW
		Total	3.44 kW
HV1 Filter, $\zeta_{cm} = 25\%$			
Inductor	0.56 mH	0.03 m^3	0.22 kW
Resistor	0.75 Ω	-	0.04 kW
		Total	0.26 kW
HV2 Filter, $\zeta_{cm} = 10\%$			
Inductor	14.1 mH	3.74 m^3	23.54 kW
Resistor	3.75 Ω	-	5.89 kW
		Total	29.43 kW
HV2 Filter, $\zeta_{cm} = 25\%$			
Inductor	5.10 mH	2.03 m^3	12.79 kW
Resistor	2.25 Ω	-	3.89 kW
		Total	16.68 kW

Table 8.4: Inductor sizes and losses, current density (d_{It}) of 0.5 MAm^{-2}.

HV1 Filter				
Inductance	Volume	relative change	Loss	relative change
56.3 mH	1.24 m^3	+130%	1.97 kW	-42%
0.56 mH	0.08 m^3	+160%	0.12 kW	-45%
HV2 Filter				
14.1 mH	8.58 m^3	+129%	13.5 kW	-43%
5.1 mH	4.66 m^3	+130%	7.35 kW	-43%

8.2 Transformer

The transformer has been modelled by a separate Matlab algorithm, as described in detail in Appendix A on page 299. The design of a transformer takes a number of parameters as inputs. They can be split into two categories: first, the operational parameters. The specific the primary and secondary voltages, the power rating and the AC frequency. Second, there are a number of design parameters. These do not affect the operational parameters, but concern how the transformer's core and windings are designed. The transformer sizing algorithm, written as part of this work, takes four such design parameters as inputs: the number of secondary turns, height of the winding window, magnetising inductance and the type of core material.

This section investigates the effects on the transformer's losses and volume as both types of input parameters are varied. The effect of the operational parameters is relevant as the transformer forms part of a larger system, i.e., the DC/DC converter. The design parameters can be used to truly customise and therefore optimise the transformer for an particular set of operating parameter inputs.

8.2.1 Design Input Parameters

This section presents the effects of the three design input parameters on the transformer's performance: number of secondary (LV winding) turns, height of the windings window and the magnetising inductance. The standard parameters of the test transformer for the results presented here are summarised in table 8.5 and apply unless stated otherwise. The algorithm automatically assigns a value of [NaN] to solutions which yield an unfeasible transformer design. Conditions for this are explained in Appendix D. Whenever magnetising inductance is discussed, it is done so from the primary point of view (i.e. L_m is always referred to the primary). The reader is encouraged to familiarise themselves with this Appendix first as it introduces the relevant terminology.

Number of Secondary Turns

The number of turns on the secondary (n_s) can be chosen freely. Increasing them causes the number of turns on the primary to increase as well to maintain a constant step-ratio. Figure 8.10 shows the efficiency of a transformer with a fixed winding window height (w_h) of 1 m and a magnetising inductance (L_m) of 0.95 H. The core is made of laminations of standard electrical steel[1]. The efficiency can be seen to peak at about 99.55 % for 40

[1] AK electrical steel, Lite Carlite, M-2

Table 8.5: Test transformer input parameters.

Parameter	Symbol	Value
Primary Voltage Magnitude	$\hat{V}_p$	30 kV
Secondary Voltage Magnitude	$\hat{V}_s$	10 kV
Transformer Step-ratio	κ_t	$0.\dot{3}$
Power Rating	P_t	20 MW
AC Frequency	f_{AC}	500 Hz

secondary turns. Increasing n_s above 40 turns causes the efficiency to drop. At 100 turns it is still above 99.3 % however. No results below 36 turns yielded feasible transformer designs.

The trend of the efficiency can be see to coincide with the trend of the core losses as a percentage of the total losses. Figure 8.11 shows the losses incurred in the core and the windings with respect to n_s. It can be noticed that with an increasing number of turns the core losses increase only very slightly, whilst the winding losses have a clear minimum at 40 turns. The magnetising inductance is fixed, therefore, according to (8.14), as the number of turns increases the mean magnetic path length (ℓ_m) has to increase as well. For a fixed winding window height (w_h) this implies that the yokes have to increase in length, thereby increasing the total volume of the core. As the core losses are a function of the core's volume, this causes the core losses to increase.

Similarly the total area available for the windings increases, thereby increasing the mean turn length for primary and secondary. The AC resistance is a function of the mean turn length. At the same time changing the number of turns causes the current density in each turn to change. These two factors cause the trade-off in n_s to minimise the winding losses, as seen in figure 8.11.

$$L_m = \frac{\mu n_p^2 A_{fl}}{\ell_m} \tag{8.14}$$

Windings Window Height

The height of the winding window is an input, that to an extent, can be chosen freely. Increasing the height allows the turns to be wound more closely around the central full leg,

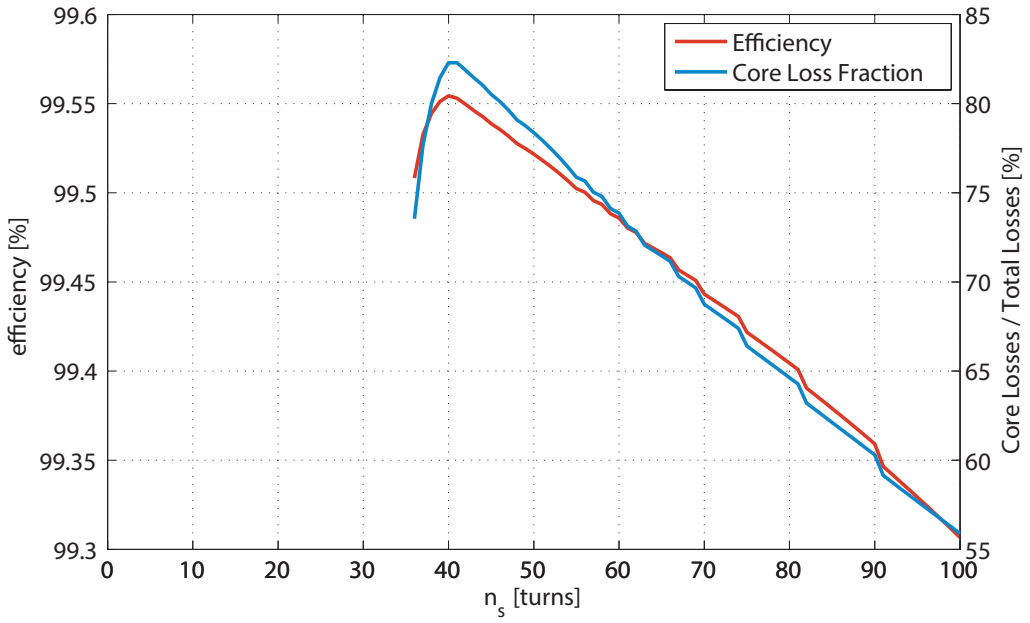

Figure 8.10: Transformer efficiency and percentage core losses of total losses with respect to n_s for $w_h = 1m$ and $L_m = 0.95$ H.

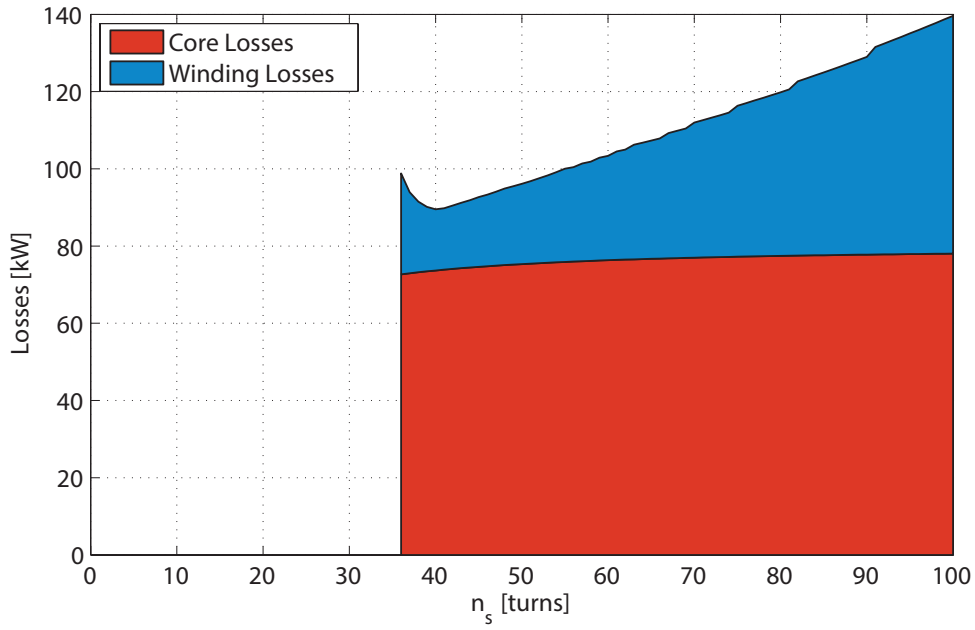

Figure 8.11: Core and winding losses with respect to n_s for $w_h = 1m$ and $L_m = 0.95$ H.

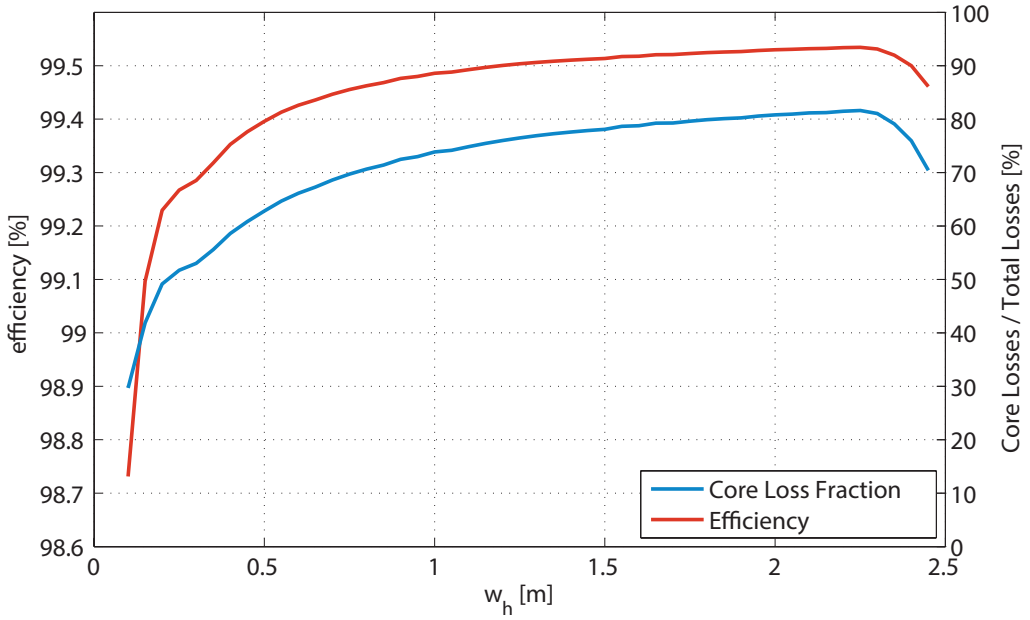

Figure 8.12: Transformer efficiency and percentage core losses of total losses with respect to w_h for $n_s = 60$ and $L_m = 0.95H$.

reducing their mean turn length. This lowers winding losses and increase the efficiency, as illustrated in figures 8.12 and 8.13. The former shows the transformer's efficiency with varying window height for a test transformer with 60 turns on the secondary side. Below 0.1 m no valid answer was found. A steep improvement in the efficiency as the height is increased can be noticed, plateauing at an efficiency of about 99.6 % at a height of 2.3 m. After the peak the efficiency begins to drop as the losses in the windings increases again, as can be seen in figure 8.13.

A change in the window height can also be observed to make no difference to the core losses as the core volume remains unchanged. The mean magnetic path length is kept constant. Thus increasing the height means the yokes become shorter, in effect moving everything more closely to the central leg. As the cross-sectional areas of the core's components remain unchanged, the total volume is constant.

The winding window height and the number of secondary turns are the two most flexible design input parameters. To optimise their values, the transformer's performance indices can be calculated against a range for both and presented in heat-maps. This section considers three main performance indices: first, the efficiency. Second, the total volume of the transformer, as measured by its tank dimensions. This uses the the maximum height, width and depth of the transformer, but ignores any cooling equipment that may

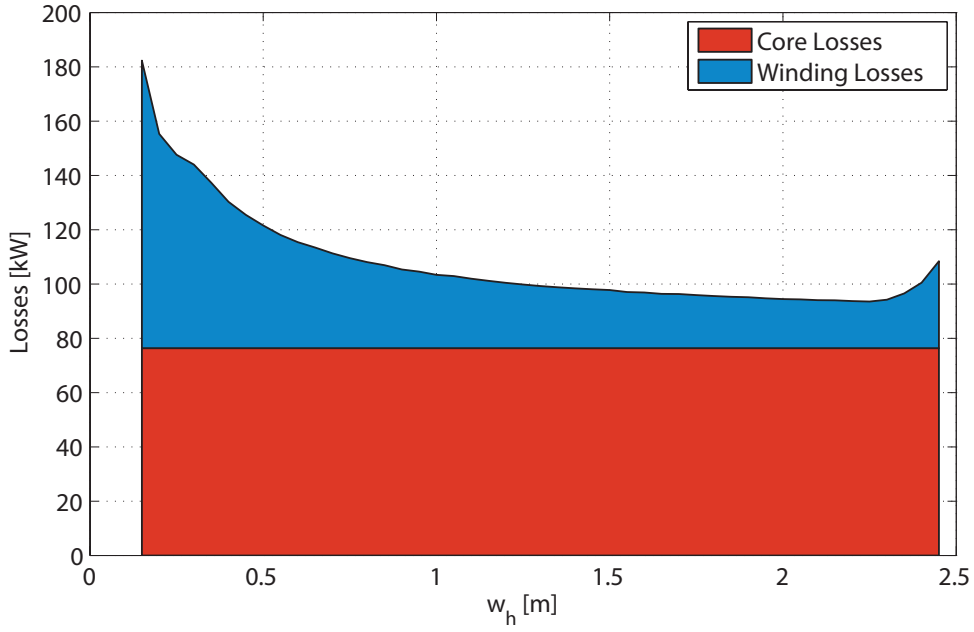

Figure 8.13: Core and winding losses with respect to w_h for $n_s = 60$ and $L_m = 0.95$ H.

be required. Third, the coupling factor, and by extension the leakage inductance. The previous chapter stressed the importance of reducing the inductance in the current path for the DC/DC converter to allow for a quick transition. To achieve this very high coupling factors are required.

Figure 8.14 shows the transformer efficiency, as calculated using (8.15), against a range of w_h and n_s. Results below 99 % are only noted with a blank rectangle, to allow for a better colour diversification of the rest of the results. Unfeasible designs resulted in no result. From the graph it can be noted that a transformer efficiency above 99.5 % is achievable. The best results were obtained around 40 turns on the secondary and a window height of about 1 m.

$$\eta_t = \frac{P_t}{P_t + P_{core} + P_{windings}} \tag{8.15}$$

To allow for a better trade-off between the volume and the efficiency, a normalised volume ($\tilde{v}_t$) is presented in this work, as defined by (8.16). Figure 8.15 shows the normalised volume results for the test transformer. The best trade-offs can be seen to lie along the diagonal stretch, just before the design inputs result in an unfeasible transformer design.

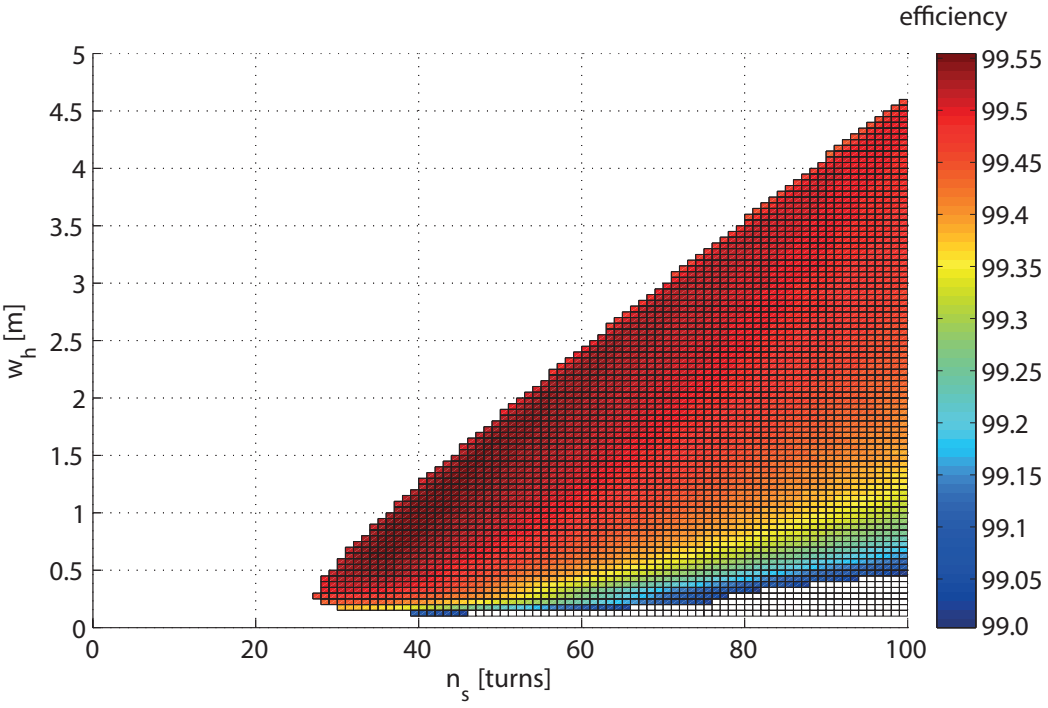

Figure 8.14: Transformer efficiency with respect to w_h and n_s for $L_m = 0.95$ H.

Some of the lowest volumes coincide with the highest efficiency results.

$$\tilde{v}_t = \frac{v_t}{\eta_t} \tag{8.16}$$

The coupling factor for the test transformer has been calculated for a range of n_s and w_h, as shown in figure 8.16. As a high coupling factor is essential for this application, only results above 0.999 are shown. Again, the best results are achieved along the upper diagonal region of results just before the design become unfeasible. This is the region where the window height has been increased enough to minimise the number of layers in the windings[2] This minimises the sum of the gaps between adjacent layers, which is proportional to the leakage inductance. The results also indicate that some of the highest coupling factors are achieved when the transformer is the most efficient.

[2]Please refer to Appendix A for a complete definition of the term "layer".

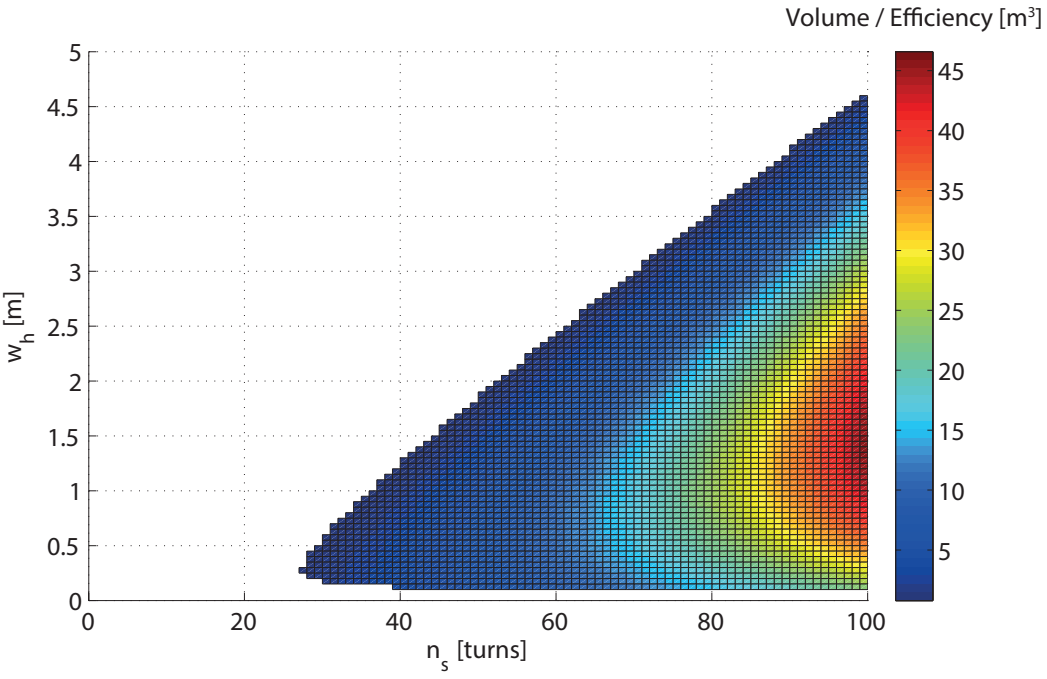

Figure 8.15: Normalised transformer volume with respect to w_h and n_s for $L_m = 0.95$ H.

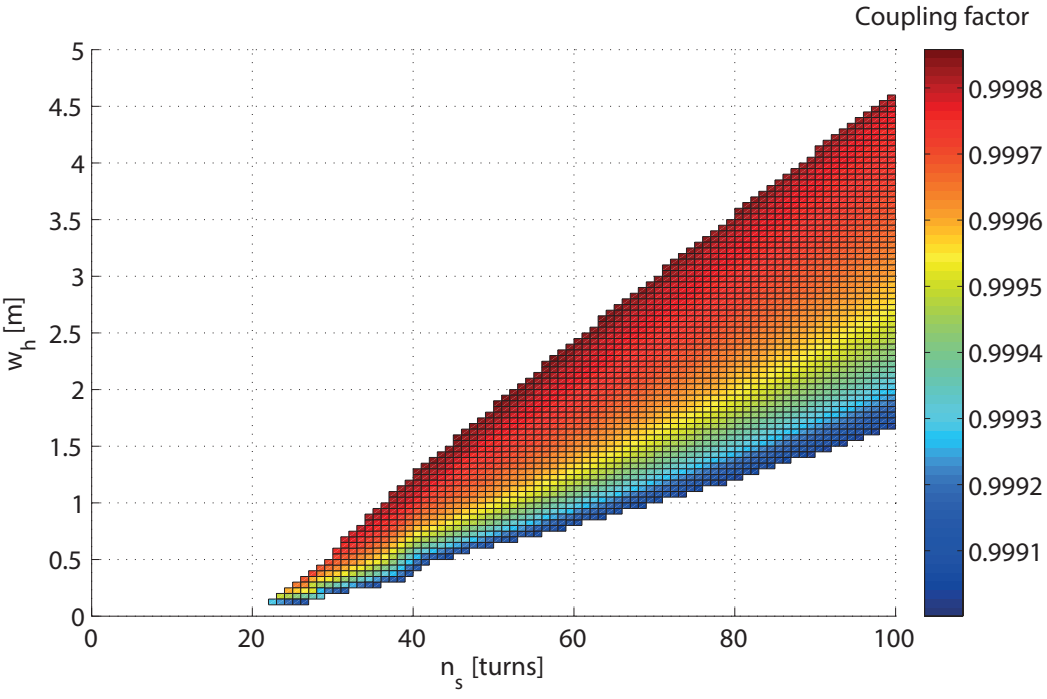

Figure 8.16: Coupling factor with respect to w_h and n_s for $L_m = 0.95$ H.

Magnetising Inductance

The magnetising inductance is the last design input: increasing it implies that the magnetising current is decreased in magnitude. As this current is fed from the cell stack side of the DC/DC converter, a reduction in magnitude reduces the losses incurred in the semiconductors due to it. A larger magnetising inductance also allows for a smaller transformer volume, as the mean magnetic path length can be shorter as the number of turns increases. On the other-hand if the magnetising inductance is reduced and the coupling factor is maintained at a very high level, the leakage inductance is reduced.

Figure 8.17 shows the transformer's efficiency for a range of w_h and n_s for a transformer with half of teh previously used magnetising inductance, i.e. $L_m = 0.48H$. As this lower inductance slightly lower efficiencies can be achieved, but still above 99.2 %. This is because: to lower the magnetising inductance, assuming all other factors, including the number of turns, remain constant, the mean magnetic pathway has to increase. This can only be done by increasing the length of the yokes, as the height is fixed by w_h. Thus the core volume and by extension the core losses increase, lowering the overall efficiency. The number of feasible solutions can however be seen to have increase, giving greater flexibility to the design process. The best efficiencies are achieved in the region of 20 turns with a winding height around 0.5 to 1 m.

From figure 8.18 the volume normalised with the efficiency is shown for the lower magnetising inductance transformer designs. Results above 100 m^3 have been shown colourless to make the lower and more interesting results, more distinguishable. It can be noted that the lowest volumes are achieved near the maximum feasible w_h for any n_s. The volume is of similar magnitude as for the transformer with a larger magnetising inductance. For these previous designs, none was feasible below about 30 turns on the secondary. The lower magnetising inductance allows designs with s few as 16 turns on the secondary, which are also the results with the lowest volumes. This indicates that although the core volume increased, this was offset by the reduction in volume taken up by additional turns.

Finally a marginally higher coupling factor can be achieved with a lower magnetising inductance, as shown in figure 8.19. This means however that the absolute leakage inductance is significantly smaller.

Core Material

The last possible design variable is the core material. All results so far have been shown for laminated electrical steel but specialised materials exist, such as Metglas 2605SA1.

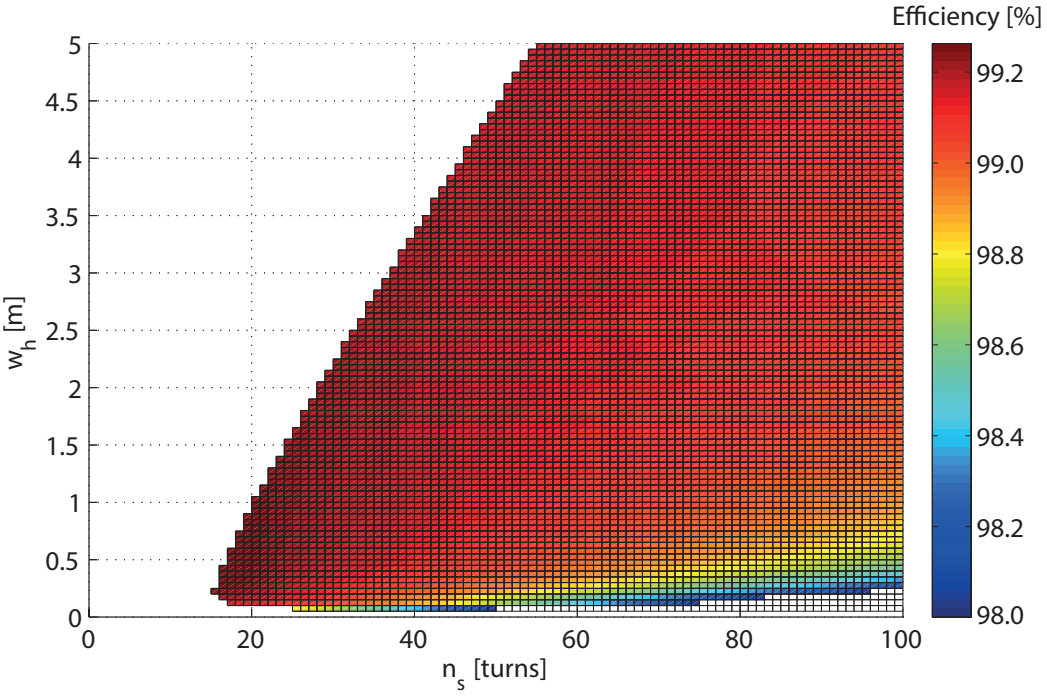

Figure 8.17: Transformer efficiency with respect to w_h and n_s for $L_m = 0.48$ H.

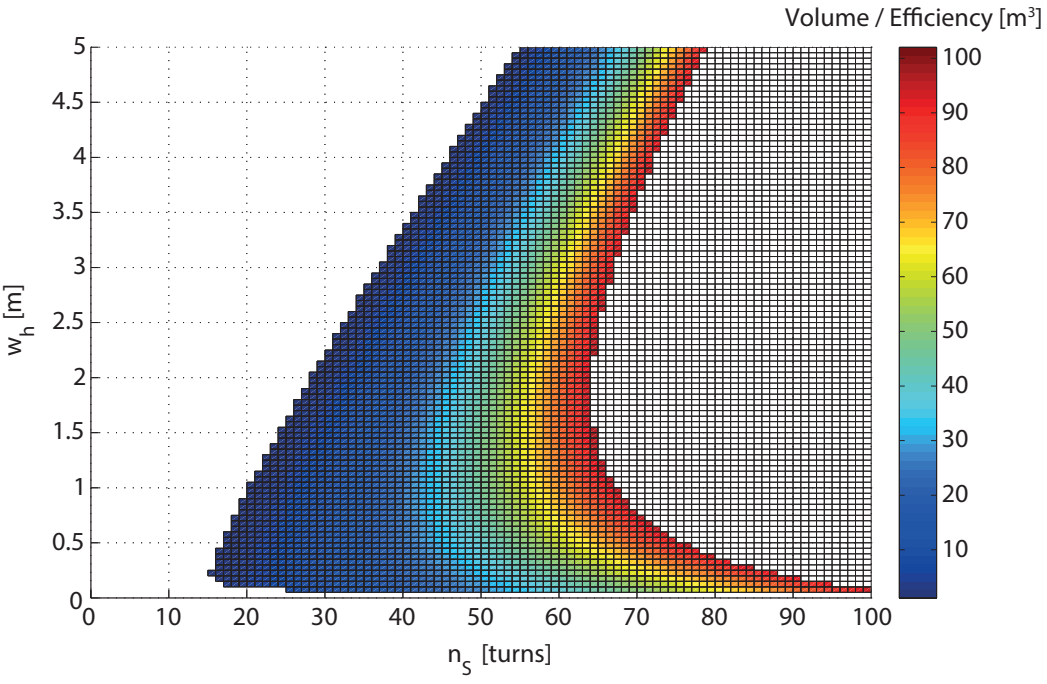

Figure 8.18: Transformer normalised volume with respect to w_h and n_s for $L_m = 0.48$ H.

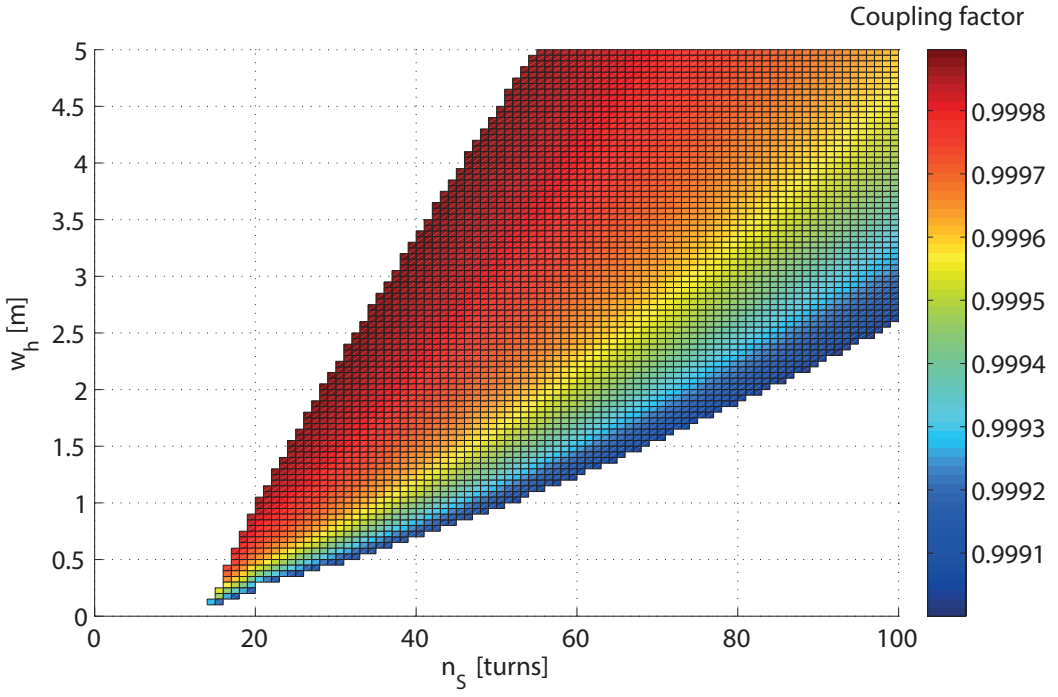

Figure 8.19: Transformer coupling factor with respect to w_h and n_s for $L_m = 0.48$ H.

This material exhibits lower specific core losses, but can only operate at a lower peak flux density and has a significantly higher permeability.

The standard electrical steel used previously has a permeability of 1.89 mH m^{-1}. Metglas 2605SA1 on the other hand has a permeability of 16.88 mH m^{-1}, almost ten times higher. This means that this core material is particularly suitable for very high magnetising inductances. The efficiency results for $L_m = 4.78$ H are shown in figure 8.20. Compared to a steel core with $L_m = 0.95$ H, there are significantly more feasible solutions. The Metglas core also achieves a higher peak efficiency: 99.7 compared with 99.6 %.

The normalised volume, as illustrated in figure 8.21, is similar to a steel core (with $L_m = 0.95$ H). The lowest volumes coincide with the highest efficiencies, as the best trade-off between winding height and number of turns is reached. Volumes above 50 m^3 are shown as black boxes without colour-code.

Crucially the coupling factor of the Metglas core transformer can be designed to be higher than that of the steel core (with $L_m = 0.95$ H), as shown in figure 8.22. Coinciding with the lowest volumes and highest efficiencies, coupling factors above 0.9999 have been calculated. This indicates that the most efficient n_s to w_h trade-offs not only result in the most compact designs but also minimise the number of winding layers, to allow for high

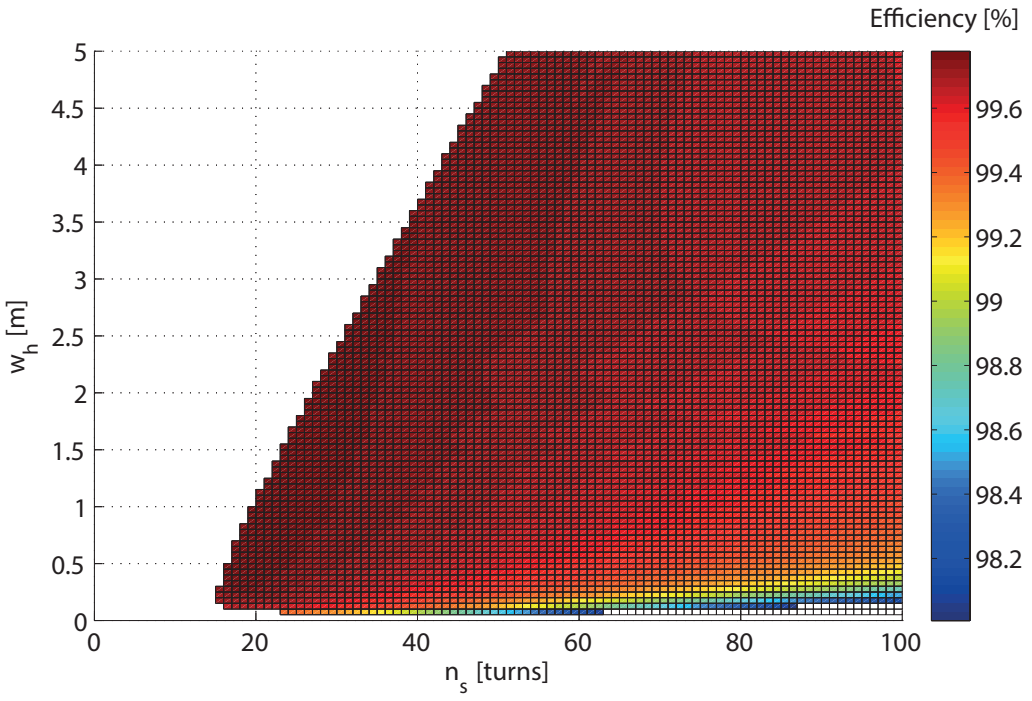

Figure 8.20: Transformer efficiency with respect to w_h and n_s for $L_m = 4.78$ H and core material M.2605SA1.

coupling factors. A coupling factor of 0.9999 and a magnetising inductance of 4.78 H still results in a significant primary leakage inductance of 0.5 mH.

8.2.2 Operational Input Parameters

This section presents the transformer's performance as the operational parameters, such as frequency and step-ratio, are changed. These changes have knock-on effects on the operation and performance of other converter components and therefore subject to system wide trade-offs. A range of different operating parameters have been modelled. For each setting a range of design parameters have been used, namely a range of secondary turns and winding window heights have been simulated. The results presented are for the most efficient design.

Step-ratio

The step-ratio of the transformer (κ_t) describes the difference in voltage between the primary and secondary side. As the secondary voltage is fixed, an increase in the step-ratio (i.e., $\kappa_t \to 0$) therefore implies an increase in the primary voltage. The magnetising

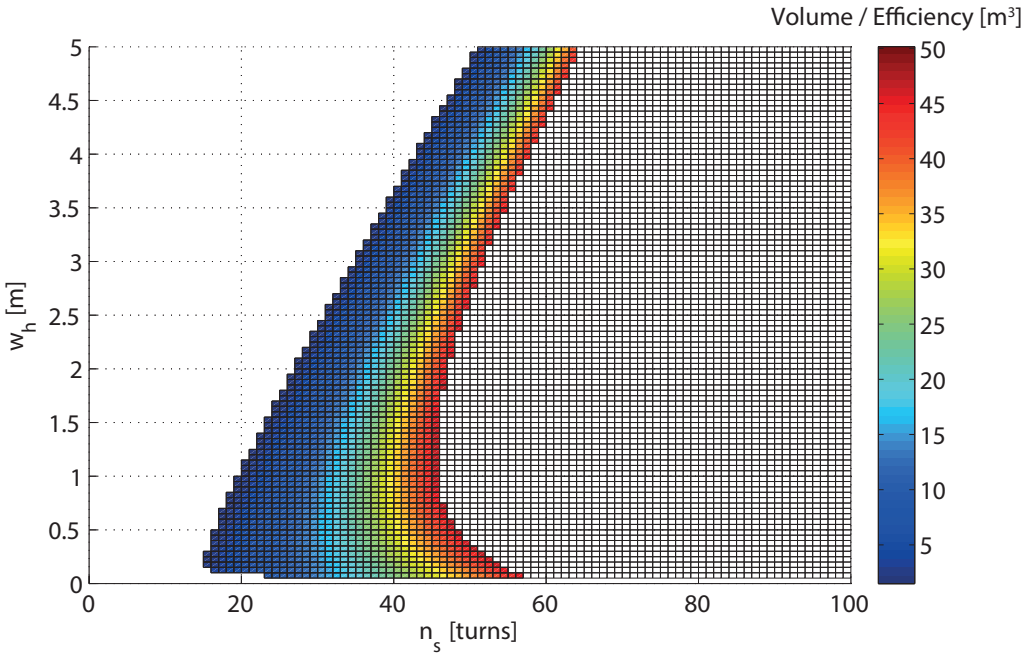

Figure 8.21: Transformer normalised volume with respect to w_h and n_s for $L_m = 4.78$ H and core material M.2605SA1.

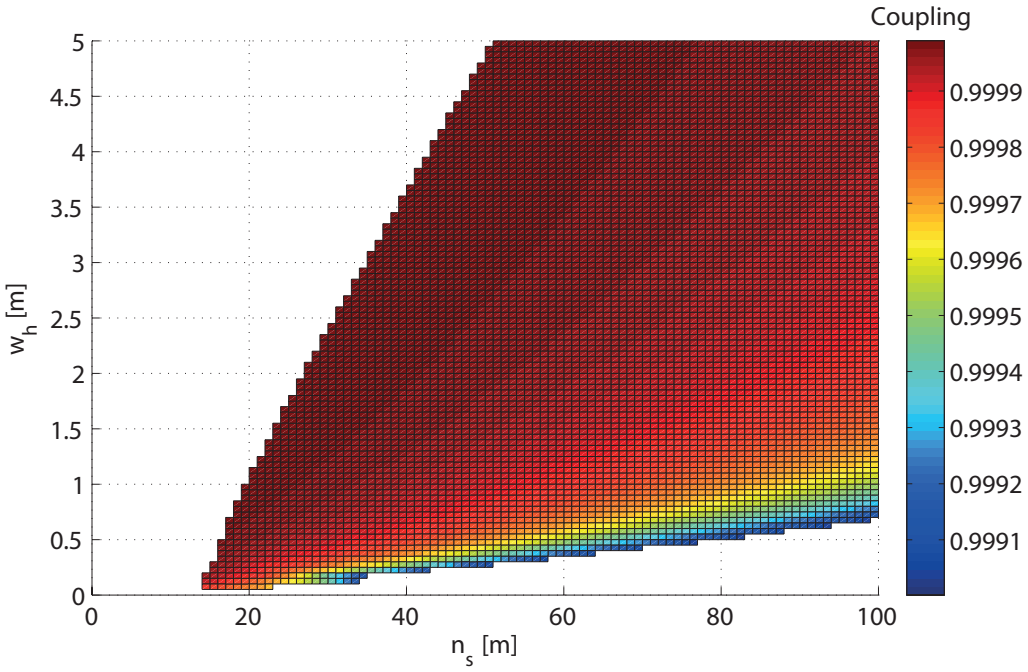

Figure 8.22: Transformer coupling factor with respect to w_h and n_s for $L_m = 4.78$ H and core material M.2605SA1.

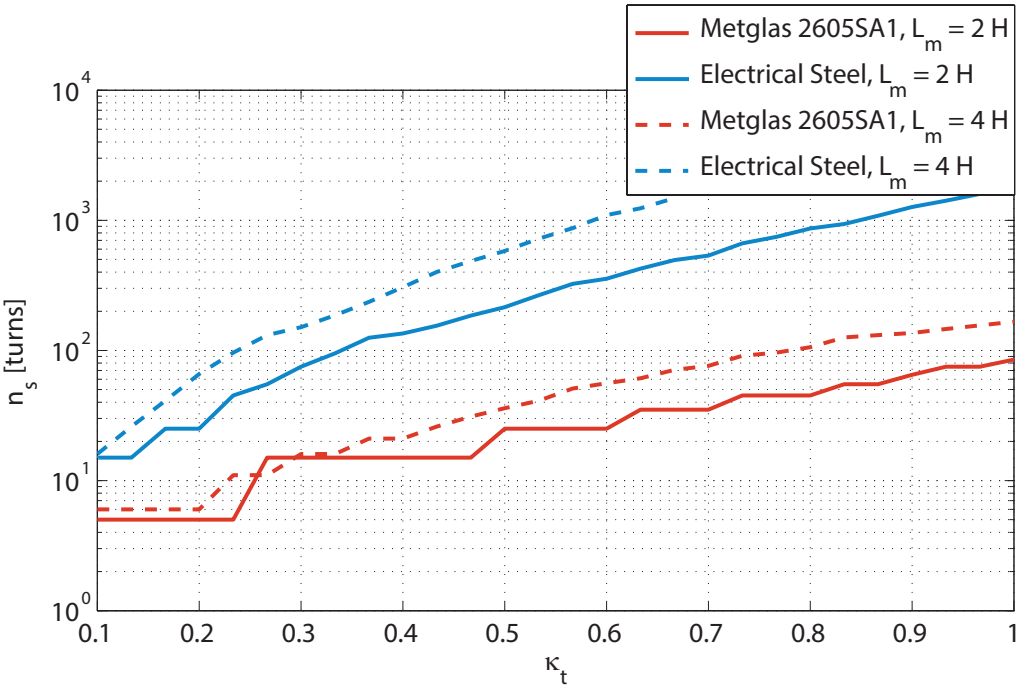

Figure 8.23: Number of turns on the secondary for most efficient transformer designs with varying step-ratio.

inductance is defined from the primary side, thus as κ_t tends towards zero the number of turns on the secondary decreases as the number of primary turns remains fixed. This is illustrated in figure 8.23 which shows the number of secondary turns with respect to the step-ratio for different magnetising inductances and core materials. Due to its higher permeability the Metglas core material requires fewer turns as the magnetising inductance is increased, than the steel core.

The leakage inductance illustrated in figure 8.24 can be noted to increase as κ_t tends towards one. This coincides with the number of turns increasing as this increase causes the number of layers in the windings to increase, which in turns increases the leakage flux.

The best efficiencies are summarised in figure 8.25. The steel core can be see to have a narrow range of step-ratios towards the lower end, at which the efficiency is above 99 %. Increasing the magnetising inductance increases this band slightly, but does not prevent the efficiency to drop off quickly for a κ_t above 0.5. The peak in efficiency is caused by the opposite trends of the winding and core losses with respect to the step-ratio.

The losses in the core increase as κ_t tends towards zero, as shown in figure 8.26. This is

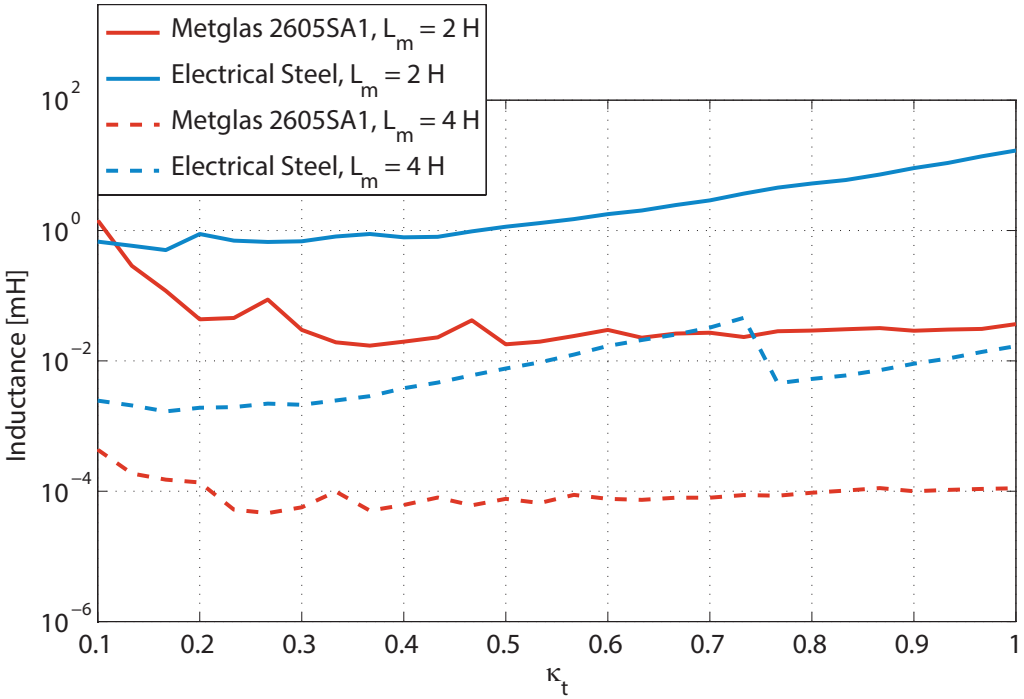

Figure 8.24: Leakage inductance referred to primary for most efficient transformer designs with varying step-ratio.

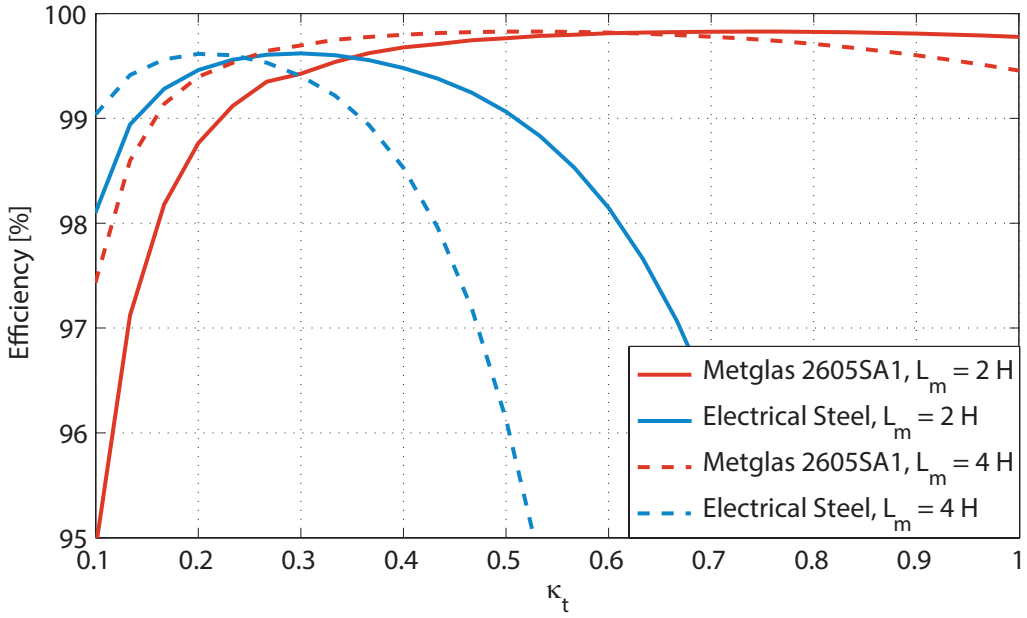

Figure 8.25: Efficiencies for transformer designs with varying step-ratio.

because the primary voltage increases causing the peak flux to increase too. To maintain a constant flux density in the core the core's cross-sectional area has to increase, thereby increasing the core's volume and losses. It can be noted that the lower peak flux density of the Metglas core cause its losses to be consistently higher than those of the electrical steel.

The winding losses on the other hand increase as κ_t tends towards one. This is because the number of turns and therefore the series resistance in the windings increases. As the Metglas core has a higher permeability its number of turns is consistently lower then those of the steel-cored transformer designs. As a result its winding losses are significantly lower. This allows the Metglas cored transformers to maintain a high efficiency (above 99.5 %) for a much larger step-ratio range than the steel cored ones.

The steel cored transformer designs can be noted to be more suitable for higher step-ratios ($\kappa_t \to 0$) where the core losses dominate. The Metglas cored transformers on the hand are more suitable for low step-ratios as they minimise the number of turns required.

These trends can also be noticed with regards to the transformer volume, as shown in figure 8.27. The volume of the steel-cored transformers is lowest for the highest step-ratios. The Metglas cored transformers follow the opposite trend. Both core materials result in a minimum volume of about 2 m^3.

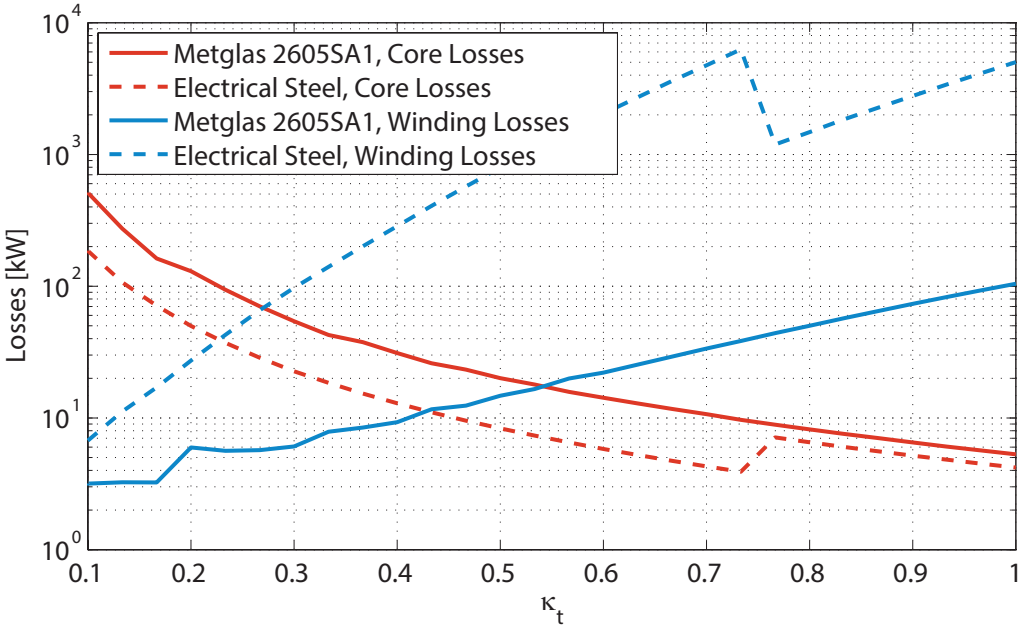

Figure 8.26: Losses for transformer designs with varying step-ratio for $L_m = 4H$.

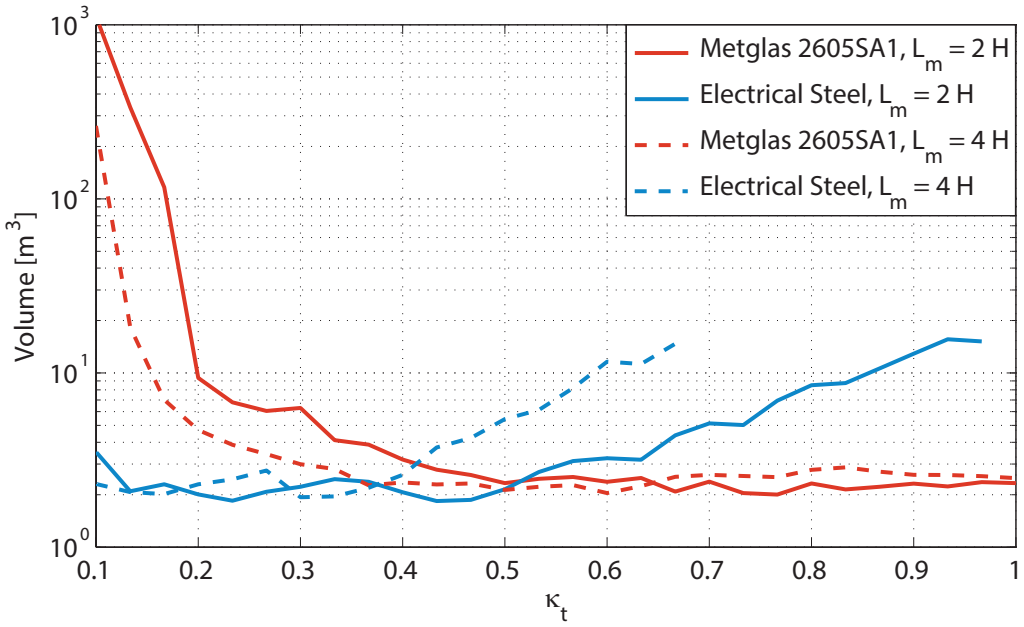

Figure 8.27: Transformer volume for most efficient transformer designs with varying step-ratio.

AC Frequency

Increasing the AC frequency allows the cross-sectional area of the core to decrease as the peak flux during a cycle decreases. Whilst the core volume therefore decreases (assuming a constant L_m), the hysteresis losses per unit volume of the core increase. In the windings the effective resistance changes with frequency as the skin and proximity effects become more dominant.

To illustrate the effects of a changing AC frequency on the transformer's performance, the test transformer was designed for a range of n_s and w_h. For each frequency the result with the highest efficiency was selected. The magnetising inductance was sized such that the frequency dependent magnetising impedance (Z_m) is kept constant. As Z_m is a function of frequency, which implies that the value of L_m decreases with respect to frequency, as illustrated in (8.17). This sizing method ensures that the leakage inductance decreases as the frequency increases.

$$L_m = \frac{V_p}{2\pi f_{AC} I_m} \tag{8.17}$$

Figure 8.28 shows the magnetising inductance with respect to frequency for the two different magnetising impedances used in the results for this sub-section. At lower frequencies the inductance is significantly higher than at high frequencies, which leads to significantly more turns. Figure 8.29 supports this. It shows the number of turns on the secondary, for the most efficient designs, for both impedances and both core materials. Due to the higher permeability the Metglas core can be noted to require significantly fewer turns for all frequencies.

The leakage inductance can be seen to decrease as the number of turns decreases, as shown in figure 8.30. As the number of turns increases for both core types with an increasing magnetising inductance, the leakage inductance also increases. This is because more turns implies that there are more layers and therefore more gaps between the layers, increasing the flux leakage.

The efficiency results for the two magnetising impedances, are shown in figure 8.31, for both core types. The transformer with the higher magnetising impedance can be noted to achieve the best efficiency for all frequencies. As the frequency increases the efficiency drops significantly: for a steel core with $Z_m = 3$ kΩ from 99.55 % at 500 Hz to 98.57 % at 5000 Hz. The Metglas core consistently under-performs compared with the steel core, being about 0.3 % less efficient for $Z_m = 3$ kΩ. The lower magnetising impedance produces significantly lower efficiencies which also drop off more quickly with respect to frequency.

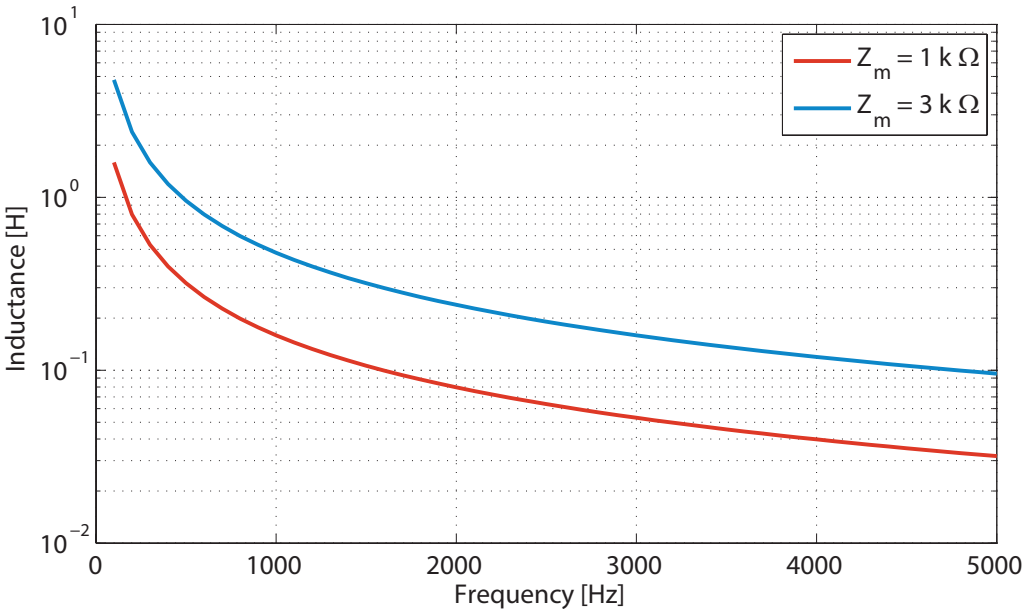

Figure 8.28: Magnetising inductance for best efficiency with respect to frequency for constant magnetising impedance.

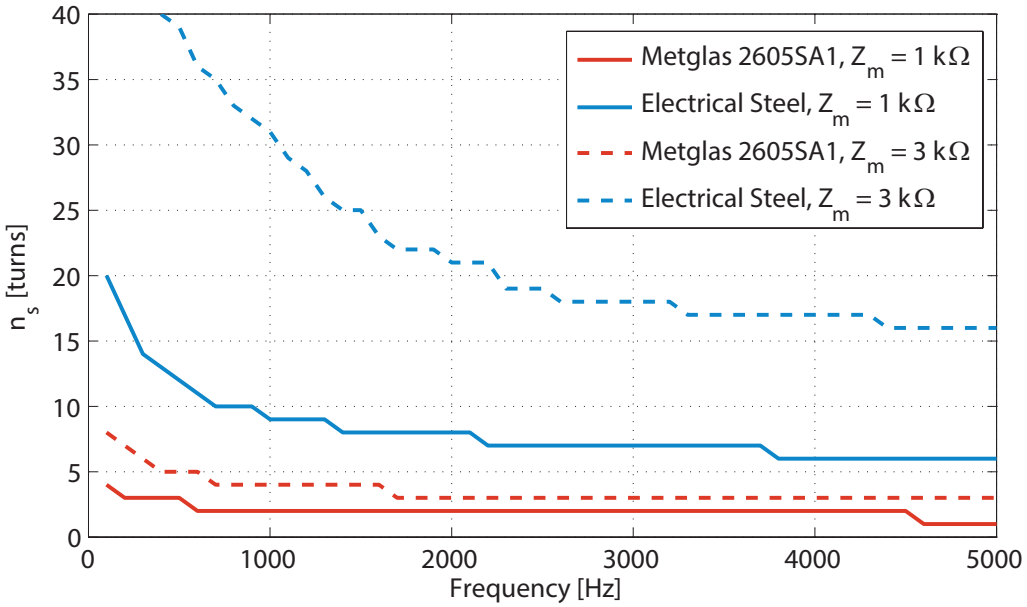

Figure 8.29: Number of turns on the secondary for best efficiency with respect to frequency for constant magnetising impedance.

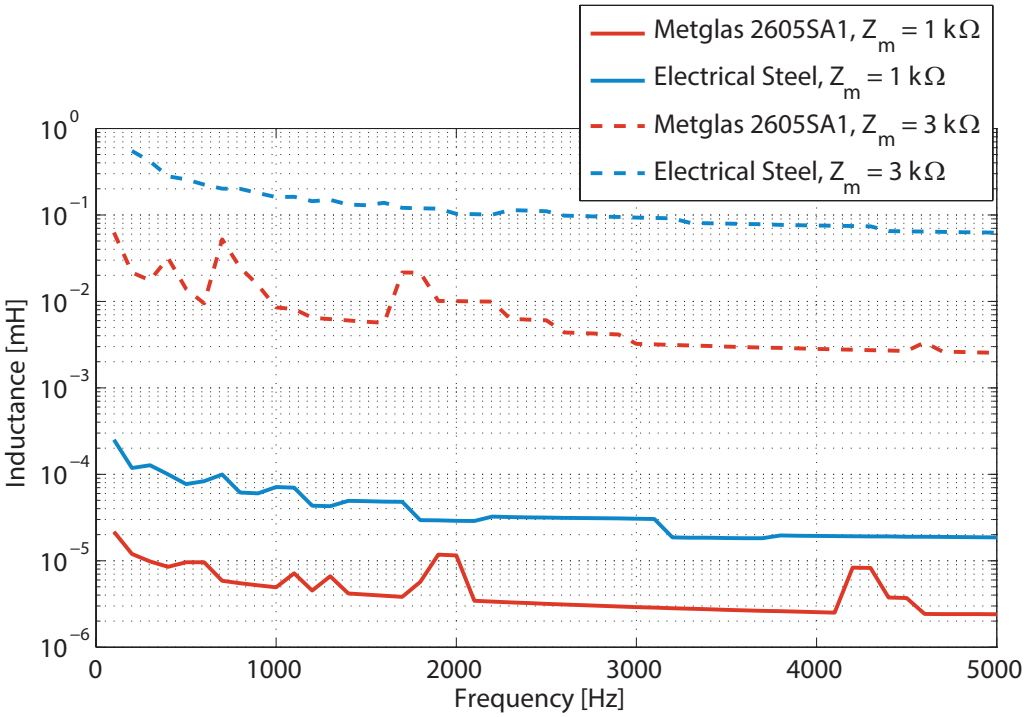

Figure 8.30: Leakage inductance referred to primary for best efficiency with respect to frequency for constant magnetising impedance.

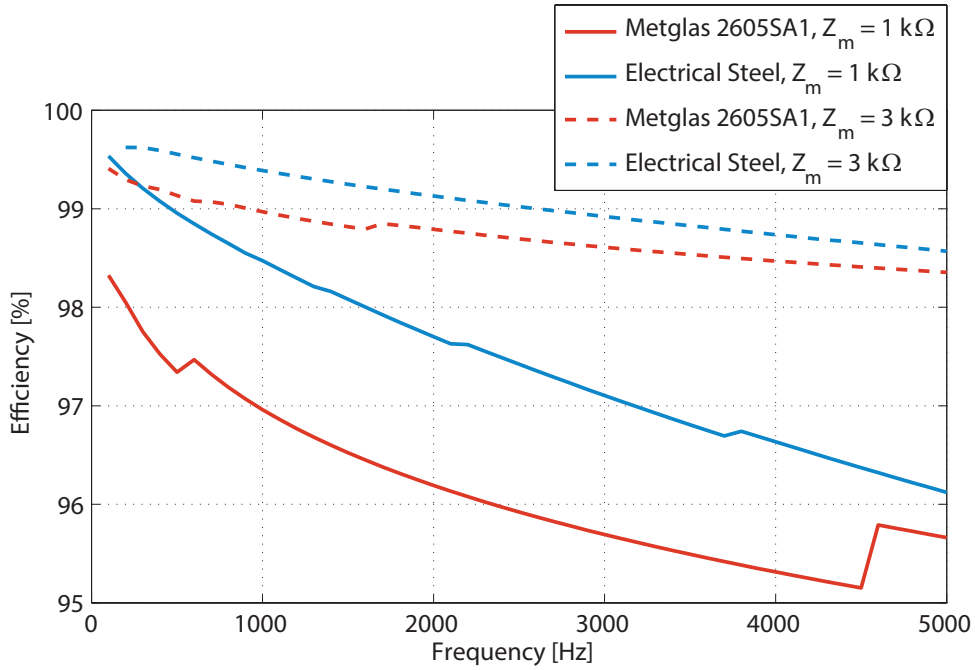

Figure 8.31: Best transformer efficiency with respect to frequency for constant magnetising impedance.

The volume of the transformer, as the results in figure 8.32 show, is decreased by an increase in magnetising inductance. This is because the length of the yokes can be shorter as the magnetising inductance is larger. The volume of the transformer drops significantly as the frequency increases, as the the core's cross sectional area decreases. This reduced the width and height of the transformer. The higher operating flux density of the steel core allows the steel-cored transformers to have a lower volume than the Metglas-cored ones. Again this is due to a decreased cross-sectional area in the steel cores, relative to the Metglas cores.

The trend of the volume for the steel cored transformers shows that the transformer volume is roughly inversely proportional to frequency. For $Z_m = 3$ kΩ the volume drops from 2 m^{-3} at 500 Hz to 0.17 m^{-3} at 5000 Hz. It should be noted at this point however that the transformer model does not take temperature limits and the required cooling equipment into account. As the transformer losses increase with respect to frequency and the volume drops we can assume the temperature and therefore the volume of the cooling equipment to increase with frequency. Thus a more realistic transformer volume would decrease more slowly than the rate at which the frequency rises.

The results indicate that even with a significant increase in AC frequency a highly

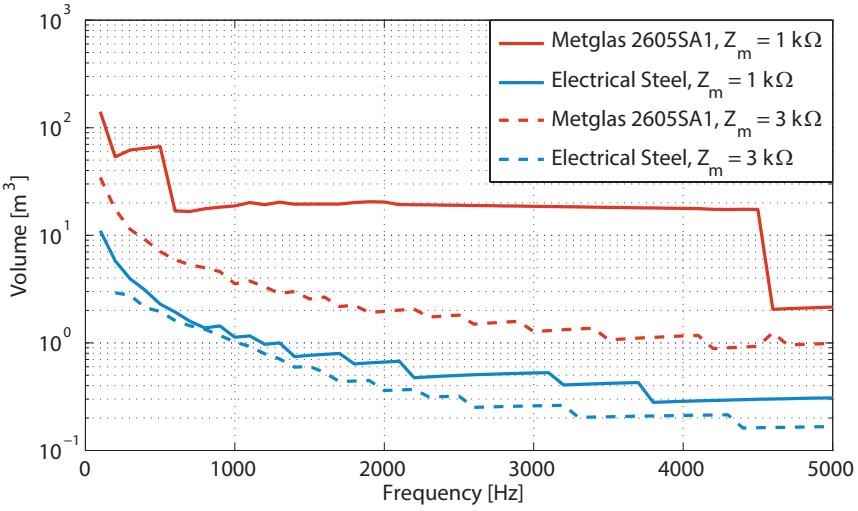

Figure 8.32: Transformer volume for best efficiency with respect to frequency for constant magnetising impedance.

efficient transformer can be designed. To achieve the best results a magnetising impedance should be chosen, as this yielded the best efficiencies and the smallest transformers. A significant increase in the leakage inductance needs to be weighed up against this though. The use of a specialised high permeability core material such as Metglas 2605SA1, allows for a trade-off: the high permeability allows for high magnetising inductances with a low number of turns, thereby reducing the leakage inductance. At the same time however the lower peak flux density capability of the material means that the core volume and losses will be larger than those of electrical steel.

8.3 Cell Stacks

Although the cell capacitance has already been discussed earlier in this chapter, there are a number of other stack operating parameters which can be changed. This section investigates the effects of varying them and explores how best to chose the optimal value. The semiconductor losses have been estimated as explained in Appendix B.

8.3.1 Cell Voltage

In section 8.1.1 it was found that by increasing the nominal cell voltage the cell capacitance could be reduced. By using different switching devices the cell design can be kept as it is (i.e., no series connected switches inside the cell). From the manufacturer's website,

Table 8.6: Switching devices used for different cell voltages.

V_c [V]	Switching Module	Rated V_{ce} [V]	Rated I_{ce} [A]
1000	Mitsubishi CM1200HA-66H	3300	1200
1800	Mitsubishi CM1200HA-66H	3300	1200
3000	Mitsubishi CM1200HG-90R	4500	1200
5000	Mitsubishi CM750HG-130R	6500	750

Table 8.7: Cell capacitances and voltages.

V_c [V]	N_c	C_c [mF]	E_{stack} [kJ]
1000	100	3.63	181
1800	56	2.0	181
3000	34	1.19	182
5000	20	0.73	183

data for a range of Mitsubishi IGBTs have been used to simulate a range of nominal cell voltages, as shown in table 8.6. A safety voltage margin of at least 1500 V was used. The 5000 V cell has a more limited current capability, which makes this device unsuitable for κ_s below 0.3.

As the cell voltage is increased the number of cells required per stack is decreased, as illustrated in figure 8.33 for the test system. The cell capacitance has been scaled such that at a nominal cell voltage of 1800 V a 2 mF capacitance is used. The resulting cell capacitances and the total stack voltage capability are summarised in table 8.7. The total stored energy in the stack can be calculated as per (8.18). Assuming that the energy density of the capacitors remains constant across all cell voltages, the stored energy in the stack can be used as an indicator of volume: since the results indicate that the total stored energy remains constant, we can expect the volume due to the capacitance to remain constant as well.

$$E_{stack} = \frac{1}{2} N_c C_c V_c^2 \tag{8.18}$$

Scaling the cell capacitances this way assumes a constant voltage deviation fraction (γ_c). As this was defined as a fraction of the cell voltage the voltage deviation magnitude

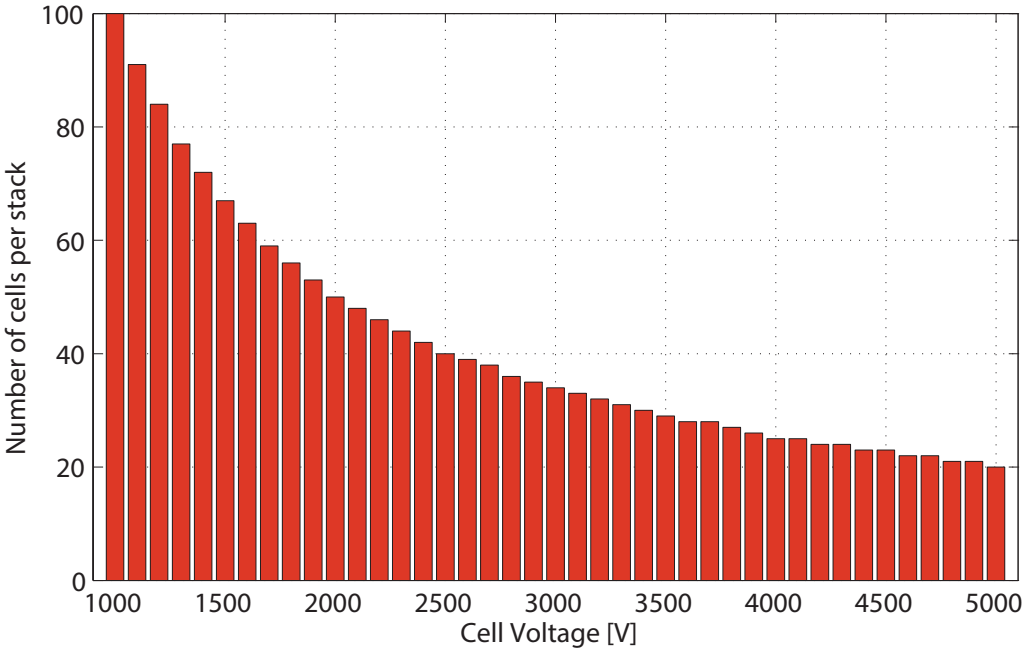

Figure 8.33: Number of cells per stack for varying cell voltage, for $\kappa_s = 0.3$ and $\zeta_{cm} = 25\%$.

in fact increases with cell voltage as shown graph a) in figure 8.34. The graph shows the mean cell voltage deviation centred around 0 (i.e., mean voltage minus the nominal cell voltage). To confirm the theory of the capacitor scaling and the original sizing algorithm, the normalised cell voltage deviation is shown in graph b). It can be noted that when the voltage magnitude is normalised with respect to the nominal cell voltage, the deviation is constant across all cell voltage and peaks at around the predicted value of 1.5% (as calculated in section 8.1.1.

The effect off using different switching devices and cell voltages on the losses can be seen in figure 8.35. The results show that the device CM1200HA-66H at a nominal cell voltage of 1800 V produces the most efficient design. The IGBT modules used for nominal cell voltages of three and five kilo-Volts suffer from particularly high switching losses but have lower conduction losses. Thus they may be more suitable for designs with lower AC frequencies, where the conduction losses dominate in the cell stacks.

8.3.2 Stack Transformation-ratio

The stack's transformation-ratio dictates the magnitude of the primary voltage. Assuming a constant power transfer, increasing this ratio ($\kappa_s \to 0$) therefore causes the magnitude of the primary current to rise as its voltage falls, as illustrated in figure 8.36. The current is

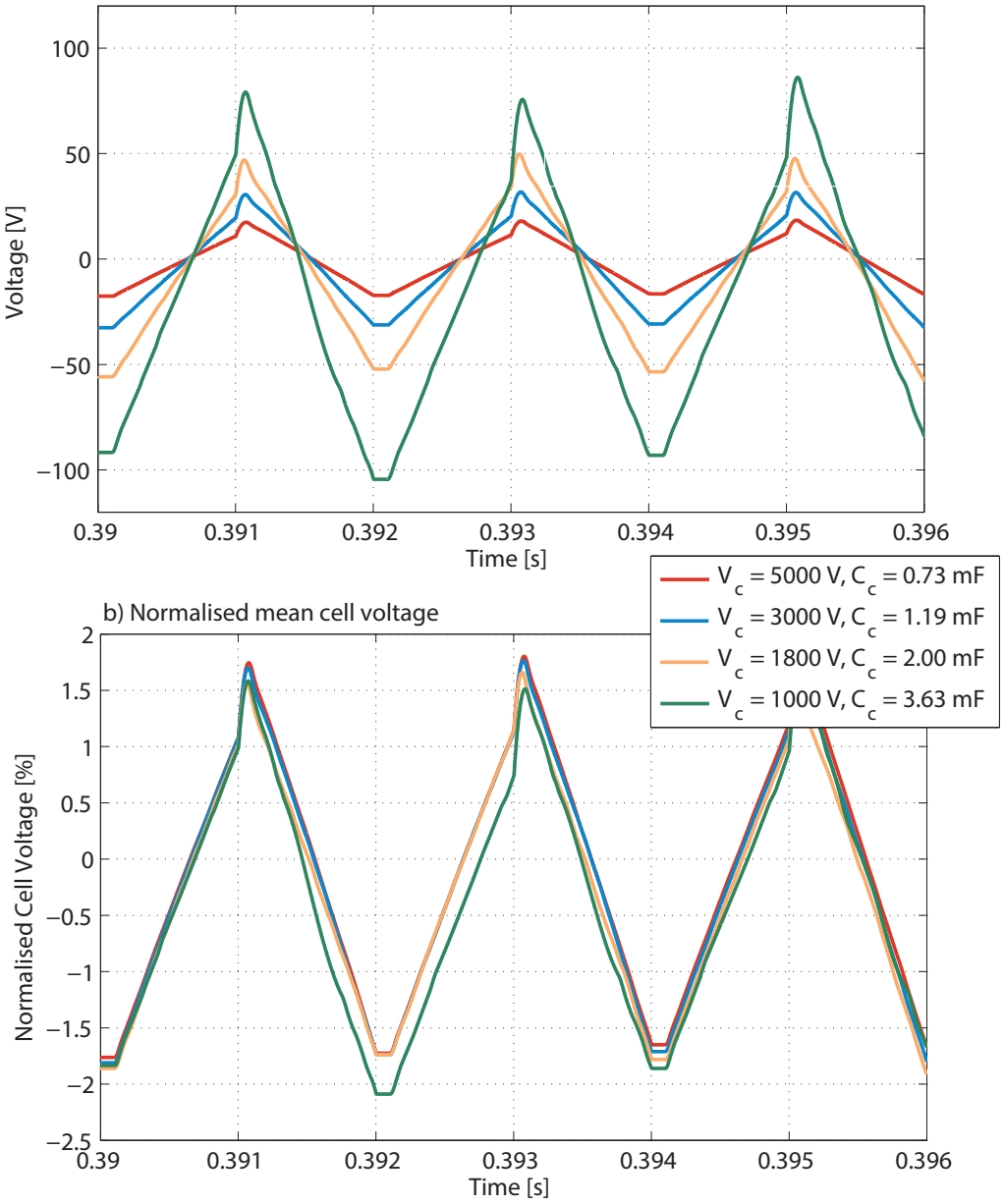

Figure 8.34: Mean cell voltage across all cells in top stack for different cell voltages, for $\kappa_s = 0.3$ and $\zeta_{cm} = 25\%$.

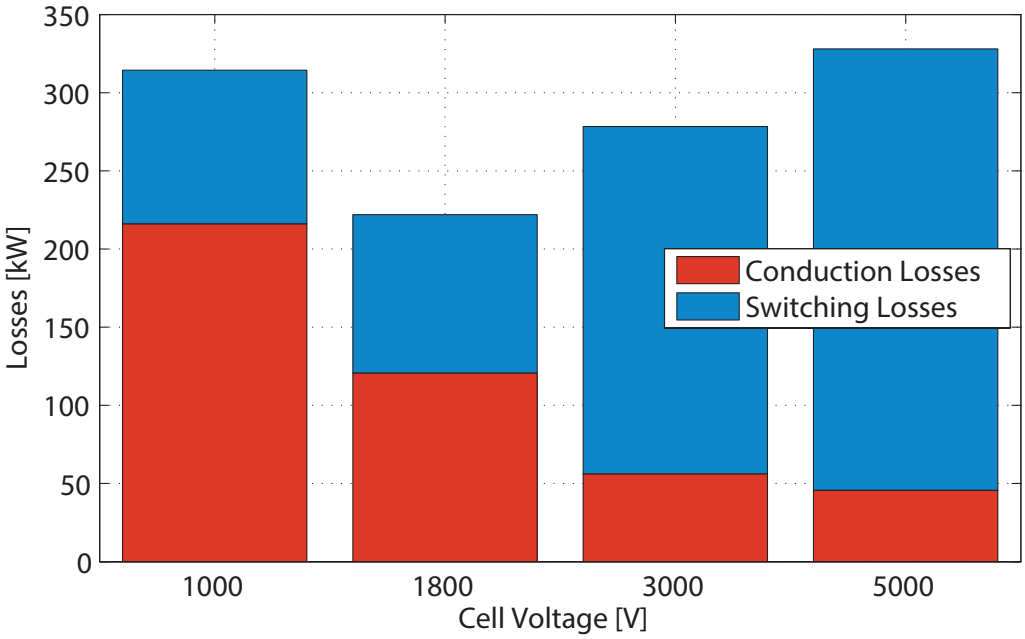

Figure 8.35: Stack losses for different cell voltages, for $\kappa_s = 0.3$ and $\zeta_{cm} = 25\%$.

inversely proportional to κ_s and can be seen to rise sharply as κ_s is reduced. The primary voltage on the other hand is proportional and therefore linearly increasing with κ_s.

An increase in the primary current implies an increase in the RMS arm current as it is split equally between both arms. The semiconductor losses are a function of current magnitude and will therefore increase as a result, as $\kappa_s \to 0$. An increase in the primary voltage on the other hand reduces the voltage capability in each stack and therefore the number of cells in it (assuming a constant nominal cell voltage), as shown in figure 8.37. The graph shows a 33% reduction in the number of cells when κ_s is reduced from 0.4 to 0.1. This also reduces the number of semiconductors in the conduction path and thereby decreases the overall losses.

Therefore there exist two opposing trends with a varying transformation-ratio. From the loss results shown in figure 8.38 it can be seen that the total semiconductor losses significantly decrease as κ_s is increases. Therefore the decrease in current magnitude is more dominant than the increase in the number of switching devices. Overall there is a decrease of 72% in the losses as κ_s is increased from 0.1 to 0.4. The reduction in losses as κ_s increases diminishes, with a difference reduction in losses of only 24% between κ_s of 0.3 and 0.4. The split of the conduction and switching losses can be seen to remain constant.

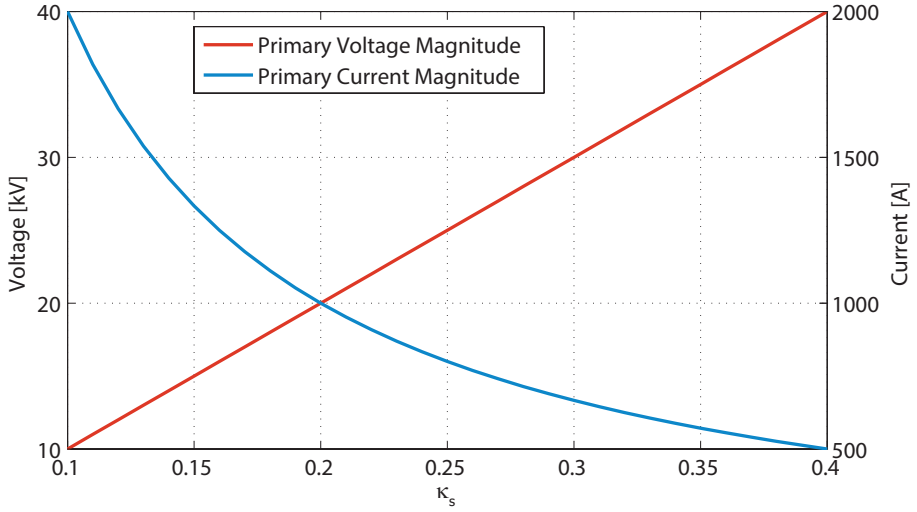

Figure 8.36: Primary current and voltages for a range of transformation-ratios (κ_s).

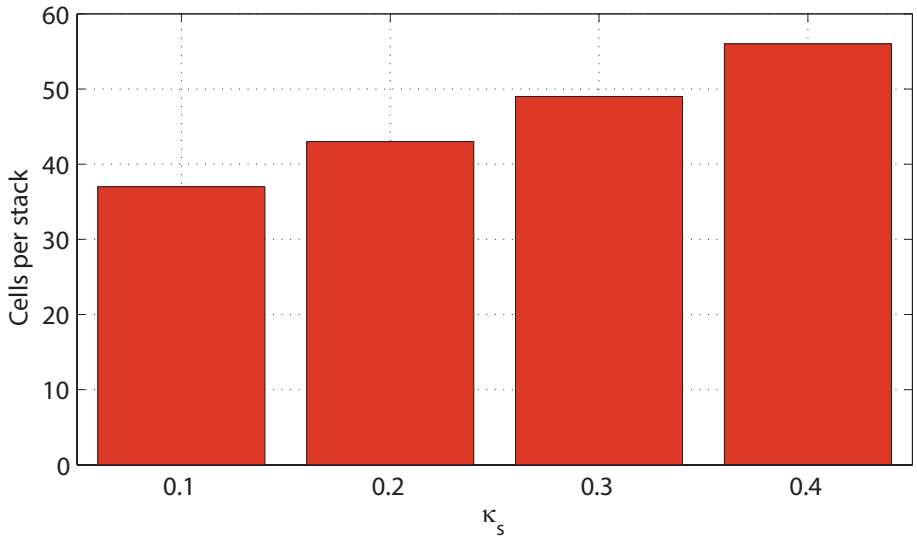

Figure 8.37: Number of cells per stack for a cell voltage of 1800 V and $\zeta_{cm} = 10\%$ for a range of transformation-ratios (κ_s).

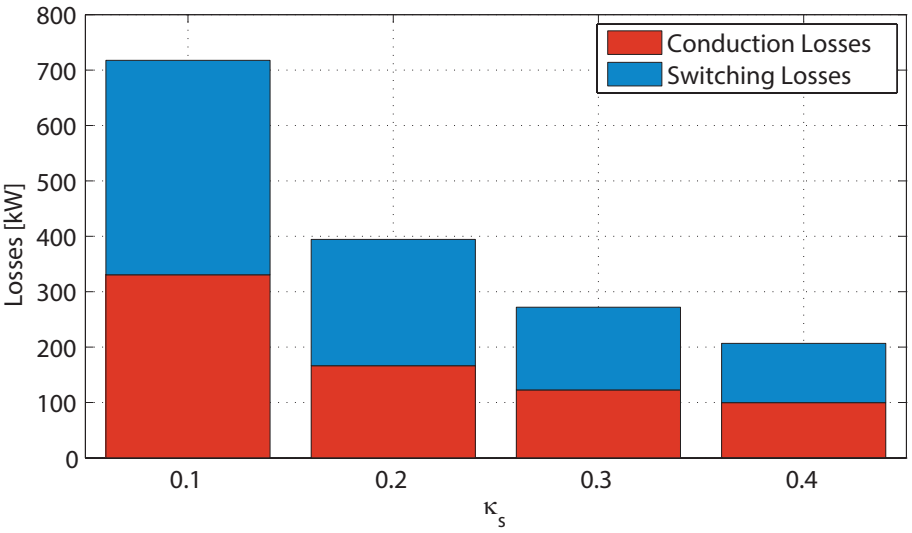

Figure 8.38: Losses incurred in the cell stacks for a range of transformation-ratios (κ_s).

8.3.3 Voltage Capability of Stacks

Increasing the voltage capability of the stacks beyond the minimal voltage requirements for the primary voltage using the control margin ζ_{cm} has been introduced in section 7.2.1. Higher control margins have been shown to significantly improve the arm current waveforms and allow for quicker AC transitions, which reduces the filter requirements. A higher margin means more cells though and therefore more semiconductors in the conduction path, resulting in higher conduction losses. At the same time previous analysis has shown the AC transitions to be much more controlled as the control margin is increased, resulting in significantly smaller overshoots. As can be seen from figure 8.39 it is the reduction in this overshoot which is the more dominant trend, lowering the conduction losses slightly.

At the same time the switching losses increase. This is due to rising cell rotation switching losses, as shown in figure 8.40. As the control margin increases more cells are not required to be in use for most the AC cycle (other than for AC current transition periods). They are therefore more likely to be switched into the conduction path as part of the cell rotation rotation. As this involves changing the states of two cells a switching loss is incurred.

Overall the lowest total loss can be noted to occur for $\zeta_{cm} = 10\%$. Increasing this to 25% only caused an increase in losses of 4% however, which is small enough to make it feasible.

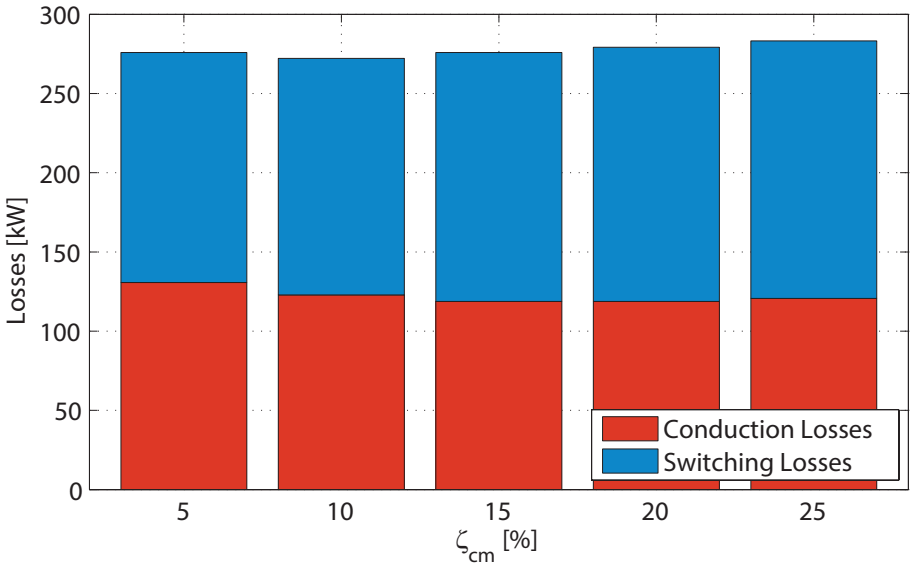

Figure 8.39: Losses incurred in cell stacks with varying ζ_{cm} for $\kappa_s = 0.3$.

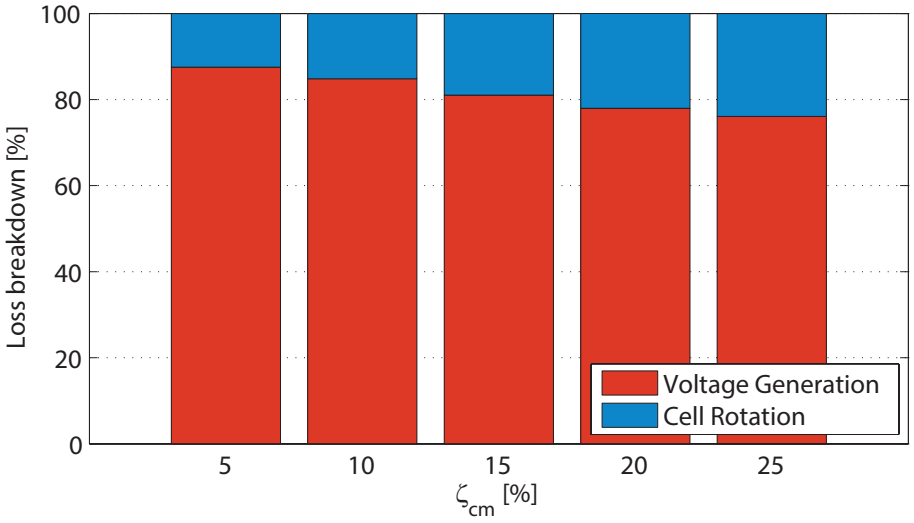

Figure 8.40: Switching loss breakdown with varying ζ_{cm} for $\kappa_s = 0.3$.

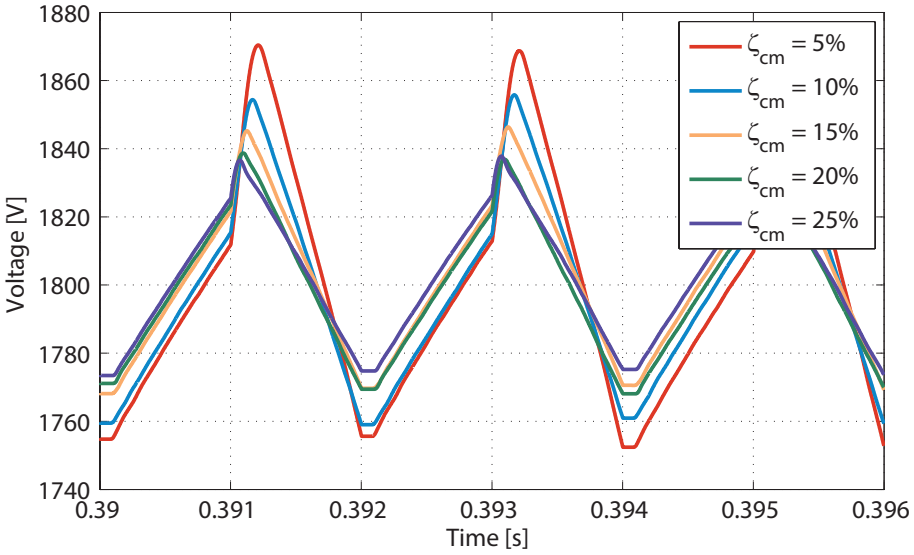

Figure 8.41: Mean cell voltage with varying ζ_{cm} for $\kappa_s = 0.3$.

Increasing the control margin does not just affect the losses but actually also lowers the cell capacitance requirement. Figure 8.41 shows the mean cell voltage of the top stack during normal operation for a range of ζ_{cm}. It has been discussed before that the overshoot current can be significant for small control margins. The direct result of this is the a larger energy, and by extension voltage, deviation in the cells. From the graph a the peak deviation for $\zeta_{cm} = 25\%$ can be seen to be 36 V. In contrast for $\zeta_{cm} = 10\%$ it is almost twice as much at 70 V. Thus to keep the cell voltage deviation within fixed limits a larger capacitor is required for smaller ζ_{cm} than for larger ones.

8.3.4 AC Frequency

An increase in the AC frequency has been shown to allow the reduction in volume of the transformer and the cell capacitance. It does however also cause an increase in the switching losses incurred in the cells, which can make very AC frequencies unfeasible. Figure 8.42 shows the losses for a range of frequencies from 50 to 5000 Hz. The cell capacitance was scaled inversely to AC frequency, such that at 500 Hz the test value of 2 mF was used.

The loss results clearly show a steep increase in the switching losses with respect to frequency, whilst conduction losses stayed constant. Above 50 Hz the losses scale nearly linearly with respect to frequencies, as shown in table 8.8. As the cell rotation frequency is a fixed number of rotations per AC cycle, the associated switching losses remain constant

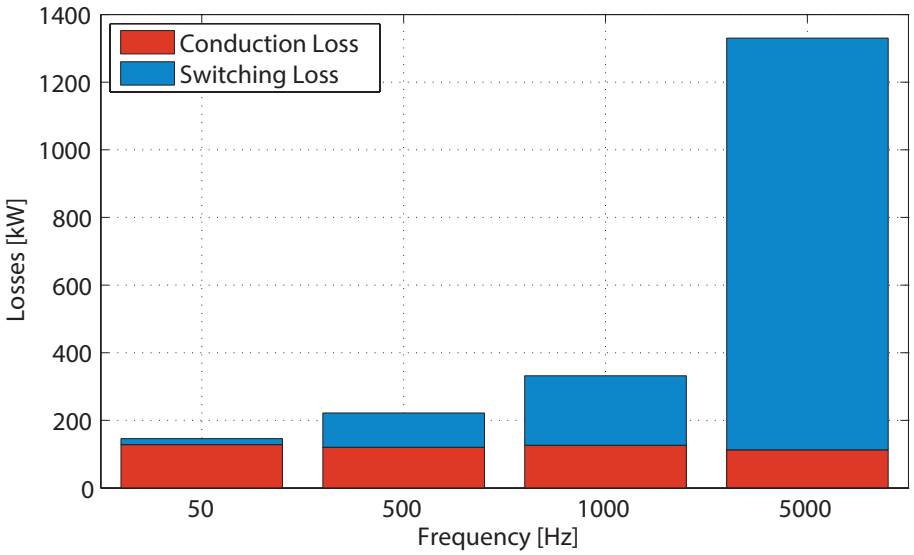

Figure 8.42: Losses incurred in the cell stacks for a range of AC frequencies.

Table 8.8: Switching losses with respect to frequency.

f_{AC} [Hz]	Switching Loss [kW]	Multiplier
50	17.4	-
500	101	5.8
1000	202	2.0
5000	1220	6.0

for all AC frequencies. This is supported by the switching loss breakdown as presented in figure 8.43 which shows the split between cell rotation and voltage generation related switching losses to be approximately the same across the tested frequencies.

8.3.5 Cell Rotation Frequency

The cell rotation frequency is defined in the number of rotations per AC cycle. Each rotation implies that the cells are ranked according to cell voltage and used in descending order or rank. This ensures that the cells which suffer from for instance the highest voltage above the nominal cell voltage get used first when the arm current is positive and last when it is negative.

Each rotation event is therefore a re-ranking event and may cause a cell to be switched into or out of the set of active cells, depending on whether its rank changes. If this happens

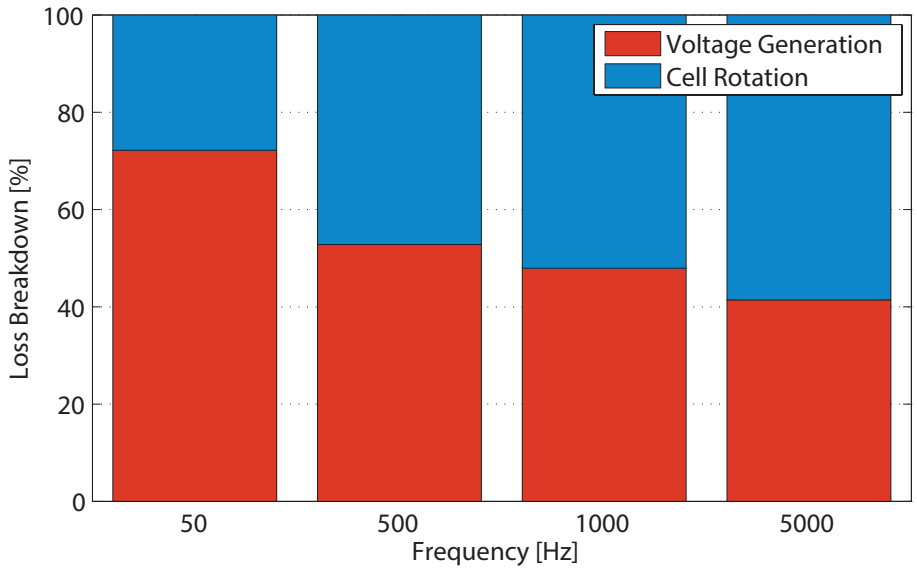

Figure 8.43: Split of switching losses in the cell stacks for a range of AC frequencies.

than this can be called a rotation loss. Ranking the cells more often per cycle ensures that that the maximum and minimum cell voltage outliers are closer to the cell voltage mean. This is illustrated in figure 8.44 which shows the maximum, minimum and mean cell voltage for the top stack for two extreme cell rotation frequencies. Rotating below 5.2 times per cycle does not provide stable cell voltages. This means that a single cell may "run" away with its voltage. Rotating a non-integer number of times per cycle ensures that the instance of rotation varies across a number of AC cycles. This limits the effect of "run" away cells.

The maximum and minimum instantaneous cell voltages are important as they have to be taken into account when sizing the cell capacitors to limit the voltage ripple. Raising the cell rotation frequency can therefore reduce the required cell capacitance. Rotating at a higher frequency does however increase the switching losses, as illustrated in figure 8.45. Although the increase in rotation frequency does not translate into a proportional increase in switching losses, the increase is significant enough to make high (i.e. 32.2 rotations per cycle) significantly less feasible. From figure 8.46 it can be seen that already at 16.2 rotations per cycle the losses associated with the cell rotation dominate the switching losses, making up 70% of the total switching losses.

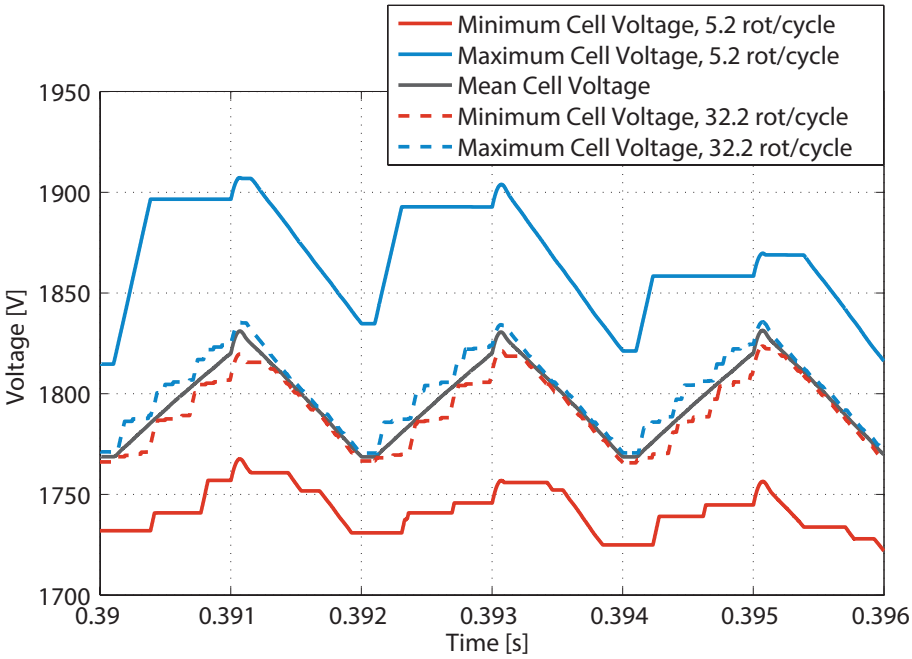

Figure 8.44: Cell stack losses for different cell rotation frequencies.

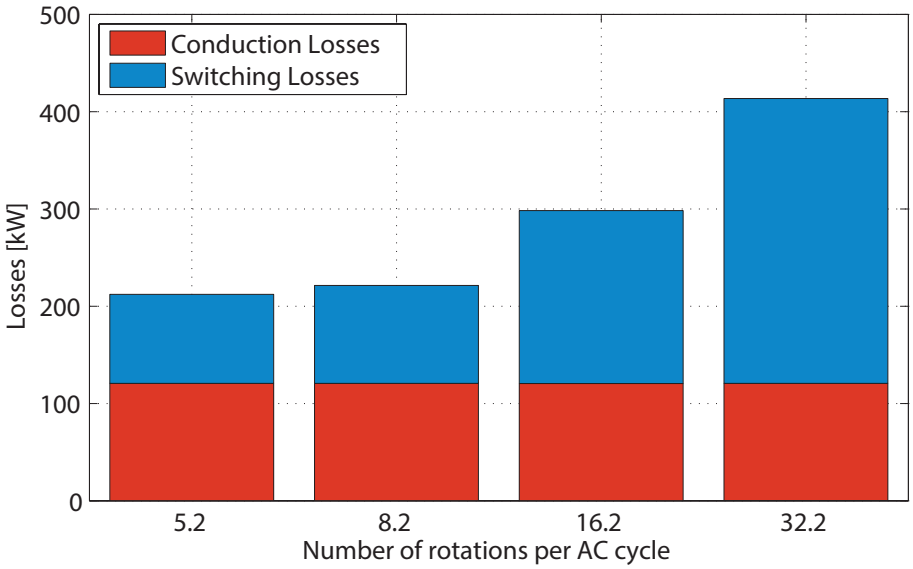

Figure 8.45: Cell stack losses for different cell rotation frequencies.

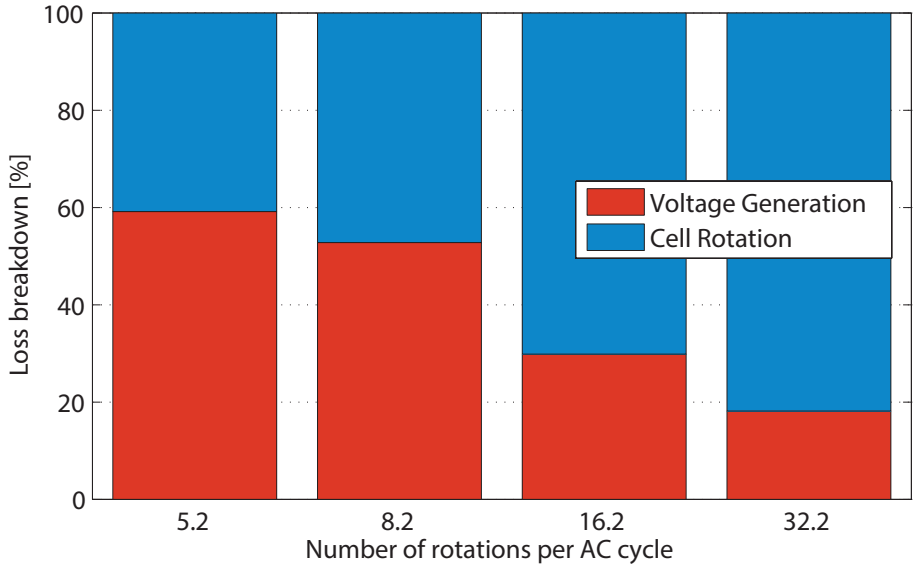

Figure 8.46: Loss breakdown for different cell rotation frequencies.

8.4 Rectifier

The rectifier converts the AC square-wave back into DC on the secondary side of the transformer. As such it typically carries a significantly higher current than the cell stacks but has to support a smaller voltage. The converter as presented in chapter 7 contains a simple passive diode rectifier. This limits the power transfer from the HV1 to the HV2 side though. To allow bi-directional power transfer, an active rectifier could be used.

8.4.1 Active versus Passive Rectifier

The passive rectifier consists of four arms containing only diodes. Each arm has to be able to withstand the HV2 DC voltage of 10 kV and carry the full HV2 DC current of 2000 A. For the simulation of the test system the Mitsubishi device FD3000AU-120DA has been used which can withstand 6000 V of repetitive reverse voltage and carry up to 3000 A in average forward current. Two such devices in series per arm are required to meet the voltage and current criteria for the rectifier of the test system.

The active rectifier utilises IGBT modules with anti-parallel diodes, like the cells. For the simulation a series and parallel arrangement per rectifier arm has been chosen to allow for the large current. The devices used is the Mitsubishi CM1200HG-90R with a collector DC current rating of 1200 A and a blocking voltage rating of 4500 V. As in the cells each IGBT is operated for a nominal V_{ce} of 3000 V only (1500 V safety margin and overshoot

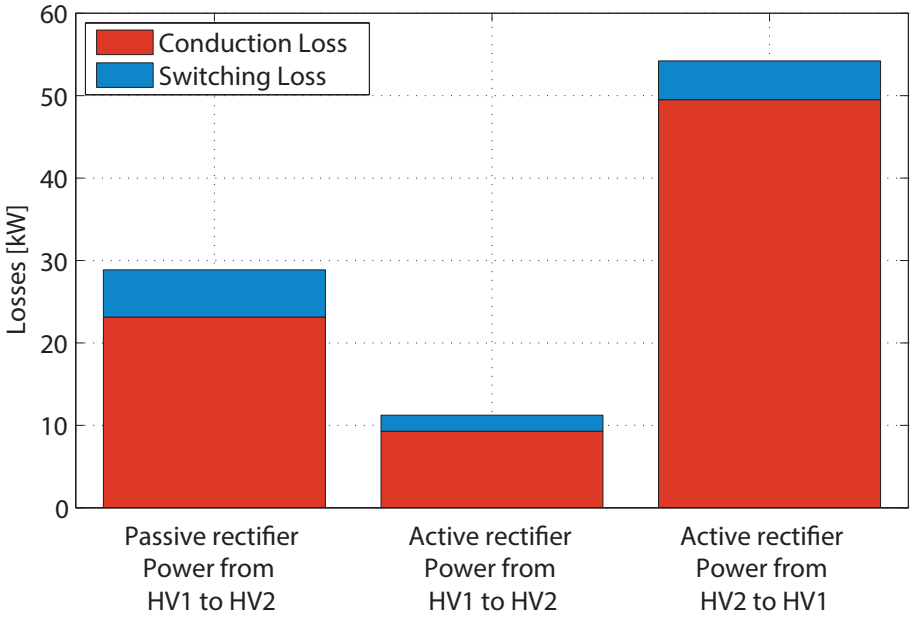

Figure 8.47: Rectifier losses for passive and active (for latter in both power flow directions).

capability). Therefore each rectifier arm contains eight devices, two in parallel and four in series. The grading circuit is modelled with a very large impedance and is therefore not considered in the losses.

The losses for both the passive and the active rectifier are summarised in figure 8.47. The losses of the active rectifier (11 kW) can be noted to be smaller than those of the passive one (39 kW) for a power flow from the HV1 to the HV2 side. This is because diodes used in the passive rectifier have a slightly larger forward voltage drop. Furthermore each device carries a higher current than the anti-parallel diodes in the active one as there are no parallel connected devices.

When the power flow is reversed the active rectifier suffers significantly higher losses, increasing to 54 kW. This is mainly due to the increased conduction losses as the current now flows through the IGBT. The switching losses, despite the rectifier having to hard-switch during turn-off, are comparatively small relative to the conduction losses.

AC Frequency

The rectifier has been seen to incur switching losses, due to reverse recovery losses of the diodes and switch-off losses incurred in the IGBT. Figure 8.48 shows how the losses increase as the AC frequency is increased, for the active bridge with a power flow from the HV2 to the HV1 side. They are indicative of the behaviour of the switching losses for

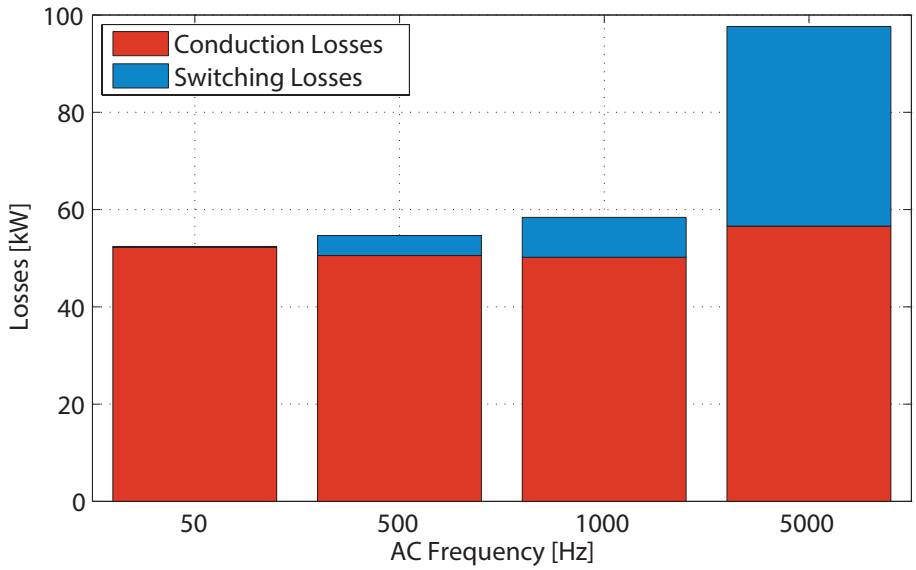

Figure 8.48: Rectifier losses with respect to AC frequency.

a power flow from HV1 to HV2 for either an active or passive rectifier.

The results show that at a very high frequency (5000 Hz) the switching losses have increased significantly, to 41 kW from 4 kW at 500 Hz. They appear scale linearly with respect to frequency, which makes sense as the current magnitudes flowing through the rectifier remain unchanged but the more switching events occur per unit time at higher frequencies. The conduction losses can be seen to remain similar (between 51 and 57 kW) for all frequencies.

8.5 Chapter summary: Performance trade-offs in modular square-wave DC/DC converter

This chapter has looked in detail at the design choices and possible trade-offs of the components of the modular square-wave DC/DC converter, with shunt connected primary. Aside from reliability, the most important aspects of a converter designed for HVDC applications are its losses and its size. The losses contribute significantly to its lifetime costs and should therefore be minimised as much as possible. The size can be an issue if a converter is to be built offshore, where all components have to be mounted on an off-shore platform, which puts a premium on space. Thus reducing the volume can significantly reduce the capital cost of a converter.

The cell capacitance is a component which can take up a significant amount of space,

as has been illustrated in earlier chapters. It can thus be used as a indication for the converter volume. A number of parameters affect the size of the capacitance required per phase; these can be split into two categories: those design parameters and the operational parameters. Of course, the operational parameters can be chosen to achieve a certain overall design goal, but in this context a design parameter refers to a variable which is adjusted to meet outside criteria, such as grid-codes.

As such there is one design parameter for the cell capacitance: the allowed voltage ripple. This is usually limited by the type of capacitor and is assumed to be something the manufacturer will know of before the design process starts. Allowing a greater voltage deviation in the cells means that the cell capacitance can be kept smaller.

A number of operational parameters also affect the phase capacitance: first and foremost is the transformation-ratio of the stacks. As $\kappa_s \to 0.5$, the required capacitance tends towards zero. It has however been established that an operation at this transformation-ratio is not feasible with this converter design due to the required voltage control margin (ζ_{cm}). Previously a control-margin of 25% has been identified as the most suitable. At this control-margin the largest κ_s possible is 0.3.

As the capacitance is inversely proportional to the AC frequency, it is very effective to reduce the capacitance significantly further. As the AC frequency is raised the switching losses in the stacks and the transformer losses increase as well. The switching losses have been found to increase exponentially: moving from 50 to 500 Hz increased the switching losses by a factor of 6; moving from 50 to 5000 Hz by a factor of 70. This makes an operation at frequencies above 1000 Hz unfeasible in most situations.

As mentioned, the transformer losses are also affected by the AC frequency. An increase in frequency causes a general drop in efficiency. The effect of this can be mitigated through the use of internal design parameters of the transformers by increasing the magnetising impedance, the efficiency at a particular frequency can be raised. It should, however, also be noted that a larger magnetising impedance causes a significant increase in leakage inductance. A large leakage inductance is undesirable as it requires additional voltage capabilities in the stacks to generate quick current transitions in the square-waves.

Two different core materials have been investigated and shown to result in more efficient transformer designs depending on the transformer's step-ratio: electric steel has been shown to yield the best results for high step ratios, such as $\kappa_t = 0.1$, whereas the high permeability core material Metglas 2605SA1 has provided the best efficiencies for the lower step-ratio spectrum. Through a careful design a transformer efficiency above 99% has been achieved for step-ratios between $\kappa_t = 0.1 : 1$.

The lowest losses in the stacks, at $\kappa_s = 0.3$, have been found with a control-margin

Table 8.9: Summary of the losses in the modular square-wave DC/DC operated at 500 Hz, $\zeta_{cm} = 25\%$ and step-ratio of 10:1.

Stack losses for $\kappa_s = 0.3$	222 kW
Transformer losses	80 kW
Inductor losses (0.8 mH)	1.4 kW
Rectifier (active)	11 kW
Total	315 kW
Loss fraction	1.57%
Capacitance in both stacks ($\gamma_c = 5\%$)	68 mF

of 10%. Increasing this further to 25% minimises the filter requirements, reducing their losses and volume significantly, but also causes an increase of 4% in the converter losses. As the reduction in the losses in the filters is of similar magnitude as the gain in losses in the stacks, this seems like a favourable trade-off as the volume of the filters has also been reduced.

The total converter losses and stack capacitance, for operation at 500 Hz, have been summarised in table 8.9. From the results it can be seen that the transformer, although operating at a high efficiency, contributes a quarter of the total converter losses. As the system utilises very small arm inductors, their losses are insignificantly small (<0.5%). The active rectifier losses will increase if the power flow is reversed to 57 kW. The DC filters have been omitted from the table as they will depend on the requirements of the DC links. Since a control-margin of 25% is used in the stacks however, the DC filtering requirements have been minimised as much as possible. With losses of 1.57% of the transferred power rating (20 MW), this converter still suffers significant losses compared, but performs well compared to the previously presented front-to-front topologies and at a much higher step-ratio.

This chapter has illustrated a number of potential trade-offs which need to be considered when designing the converter. This however also makes it difficult to present a single best solution. Thus this chapter should be taken as a guide which indicates important trends. It will ultimately be up to the designer and the devices available to him or her, to finalise the converter specifications.

Chapter 9

Technical and academic conclusions

This final chapter is comprised of three sections: first, the main conclusions and insights from across this work are brought together to compare the different DC/DC topologies that have been presented. Second, the specific contributions of the author are listed. Finally, possible avenues for further research, based on the presented work, are explored.

9.1 Technical conclusions: modular cell based DC/DC converter topologies for different step-ratios for HVDC applications

For the developing HVDC grid, the equivalent to the AC transformer, a DC/DC converter, has yet to be built at scale for a real use case. It may however prove to be an integral part of any future DC grid in, for example, making a connection between old and new lines that operate at different voltage levels or allowing the integration of new wind-farms into an off-shore transmission grid without an HVAC transformer.

Some designs have been proposed in the literature, but most have inherent problems when the voltage and power level are scaled up to HVDC ratings. The latest DC/AC Voltage Source Converters (VSCs) use modular cell-based technology which could be used to solve these problems. This work investigated how this technology can be used and the performance of some circuit topologies, in two sections: first, the re-purposing of tested and therefore reliable, DC/AC circuits has been investigated in a front-to-front (F2F)

arrangement. The scale and low number of projects in the field of HVDC means, that commissioning bodies of converters tend to be extremely cautious. Thus if a DC/DC converter would be required within the next five to ten years, a circuit that shares many component parts and controls in common with a proven design concept is more likely to be preferred to an entirely new concept.

The second part of the work looked at the other side of this argument: in the more distant future, the advantages of purpose-designed and optimised DC/DC converters may be needed and the designs may have had enough time to be properly developed and demonstrated. To this end, various classes of such modular cell-based DC/DC converters are proposed and investigated. One in particular has been chosen for a detailed study, in the last two chapters.

9.1.1 Front-to-front topology

The most straightforward F2F topology includes two three-phase DC/AC converters which are connected directly with each other on the AC side - hence it is called a direct-coupled F2F topology. Such a topology has been introduced and two different modular DC/AC Voltage Source Converters (VSCs) have been presented as potential candidates in such a circuit: the Modular Multilevel Converter (MMC) and the Alternate Arm Converter (AAC). The MMC has, at the time of writing, already been commissioned and built in north-sea off-shore projects. The AAC on the other hand is slightly newer and less extensively studied. Its operation has however been demonstrated on a scaled-down laboratory converter and industry sources claim it to be ready for sale in the next couple of years. As we are considering a time frame of about ten years for the F2F topology, the AAC is a sensible second choice to be able to compare and contrast with the MMC.

The main use of a F2F topology has been envisaged as an inter-connector between two lines that operate at slightly different voltages. As such, a system with a relatively low step ratio of 5:3 has been analysed using a scaled-down test system. Two of the most important aspects of any HVDC converter are its efficiency and volume. The lower the efficiency, the higher the cost of its losses. Since these converters are intended for applications rated at hundreds of MWs and an operational lifetime of at least 20 years, the lifetime costs associated with the power losses can be significant. The volume can be of a particular issue for offshore applications where the entire converter has to be mounted on an off-shore platform, where space comes at a premium.

The fact that the AC link is fully internal to the system allows its parameters to be adjusted. Since the AC link has a significant effect on the converter parameters, the

AC side can be chosen so as to optimise the system for its losses and volume. The first parameter considered was the stored energy in the cell capacitors. The intra-cycle energy deviation of the cell capacitors leads to a voltage ripple and the cell capacitor is typically chosen to limit this ripple to around 10% of the nominal operating voltage of the cell. The minimum capacitance required within a stack is therefore a function of the chosen AC voltage magnitude at which the system operates and this function has been derived as an aid to designers. Since the cell capacitor is a large fraction of the cell volume and the IGBT's size is not a strong function of operating point, the cell capacitor volume is taken as an indicator of total cell volume.

In the direct-coupled system the two converters operate with a shared AC voltage magnitude but different DC voltages. Thus an AC voltage which provides the lowest system wide capacitance, does not necessarily minimise the individual converter capacitances as much as possible.

The losses of the semiconductors (Appendix A), inductors (Appendix C) and, where applicable, transformers (Appendix B) have been modelled. This allows the system losses to be estimated for a 30 MW test system operating at DC voltages of ± 25 and ± 15 kV. For the direct-coupled test system, the best efficiency has been achieved using MMCs (1.35% of losses) and an AC voltage equal to the terminal voltage of the lower DC side. At this voltage both converters can utilise half-bridge cells, which significantly reduces the number of devices in the conduction path and minimises the system-wide losses. At this operating point, the system requires a particularly large total cell capacitance (relative to the other AC voltages tested) of 819 mF (or 133 kJ/MVA) per phase for the test system. By using AACs instead of MMCs, the volume of the system can be significantly reduced for a small increase in losses. Operating at the higher DC terminal voltage, the capacitance of the system has been reduced by 67% (to 267 mF per phase, or 43 kJ/MVA) but the losses raised to 1.40% of the maximum transferred power (chapter 3).

By introducing a transformer into the AC link, a large step-ratio becomes possible and the two converters can be operated at different AC voltages. This allows both converters to be operated at their highest efficiencies or lowest capacitance operating points. However, the transformer also introduces additional losses to the system and volume (although quantifying the transformer volume relative to capacitance volume is not straightforward and subject to various assumptions). In chapter 4, it has been found that even when each converter is operated at its most efficient AC voltage, the additional losses of the transformer cause an overall increase in the system losses: the transformer-coupled MMC F2F test system incurs at least 1.71% and a AAC F2F system at least 1.85% of losses. Although the transformer can reduce the capacitance of the AAC F2F system by a further

55% (to 120 mF per phase, or 19 kJ/MVA) relative to the previously presented direct-coupled AAC F2F, the losses rise to 2.13%, making most transformer-coupled systems less appealing than the direct-coupled alternatives for moderate step-ratios.

If a reduction in volume is required, then it is the AC frequency rather than AC voltage that is the most effective parameter to vary. The results discussed so far were for standard 50 Hz operation. In chapter 5 the effects of operating at 500 Hz have been investigated. The intra-cycle energy deviation is inversely proportional to the AC frequency which allows the system capacitance to be significantly reduced using a higher frequency. For example, the capacitance in the direct-coupled AAC F2F system discussed earlier, operated at 500 rather than 50 Hz, sees its capacitance reduced by a factor of ten from 267 mF per phase (or 43 kJ/MVA) to 27 mF (or 4 kJ/MVA).

This also, however, affects the switching losses of the IGBTs in the cells: raising the AC frequency to 500 Hz causes the most efficient direct-coupled MMC F2F to incur losses of 3.30% (up from 1.35%) and the most efficient direct-coupled AAC F2F 2.85% of losses (up from 1.40%). It can thus be noted that the increase in switching losses is less severe in the AACs than in the MMCs. This is because the AAC utilises fewer cells in each phase and is operated differently, using discontinuous currents in its arms. This allows the director-switches, which replace some of the cells, to be soft-switched, thereby incurring no switching losses, no matter the AC frequency.

As the system capacitance scales inversely with frequency the following three-step design procedure for a F2F system is proposed:

1. Unless galvanic isolation or a large step-ratio is absolutely required, operate without a transformer, and preferably with AACs, as they provide the best trade-off between losses and volume. If the absolutely best efficiency is required, use MMCs instead, but note that this incurs a penalty in volume.

2. Scale the converters for the most efficient AC operating voltage typical at 50 Hz. This is most likely going to be a terminal voltage of one DC link or the other.

3. Knowing the limit of the acceptable losses of your system, increase the AC operating frequency to minimise the cell capacitance and thereby reduce the total converter volume.

A frequency above 500 Hz is unlikely to be chosen, due to the steeply increasing switching losses and the diminishing returns of reducing the cell capacitor size (since the cell capacitor ceases to be a significant fraction of the total volume). It can therefore be argued that this frequency change is modest modification to already tested components

and not a large technological risk. Even if a transformer is required, the frequency is not raised so far as to make the design of a high-power transformer drastically different to a 50 Hz equivalent.

9.1.2 Alternative DC/DC converter topologies for HVDC applications

Assuming a free-hand at designing a modular cell based DC/DC converter, two different fundamental circuit ideas are introduced in chapter 6: first, the direct-conversion method and second, modified DC/AC/DC designs.

The direct-conversion method's guiding design principle is that, unlike in DC/AC/DC topologies, the transferred power is not fully converted into AC before being rectified again. Instead the DC links connect directly into the converter and the cells are used to bridge the DC voltage potential between them. To prevent the cells from discharging during normal operation of the converter, internal balancing currents and voltages are generated and circulated through the converter. To prevent them from interacting with the DC sides and allow an energy exchange with the cells, they tend to consist of AC waveforms.

Two direct-conversion circuits have been introduced, illustrated in figure 9.1, both of which are suitable for symmetric monopole connections. The first forms a parallel arrangement on the higher voltage side and is hence called the parallel output pole converter. The second converter contains a series arrangement of the stacks to form the lower DC output poles; it is called the series output pole converter. Both converters are capable of bi-directional power flow and have been found to be most suitable for relatively small step-ratios, of less than 2:1, for two main reasons: first, their power capacity ratio, a measure which calculates the power rating of the cell stacks that is required per unit of transferred power, rises quickly above such step-ratios. This makes them less feasible than the other modified DC/AC/DC converters, above ratios of 2:1, but more so below that ratio. Second, as the step-ratio rises, so does the energy drift that the AC balancing currents have to address. These currents can become very large, relative to the DC currents and is expected to lead to significant semiconductor losses.

Two modified DC/AC/DC circuits are also presented, which are shown in figure 9.2. These are each intended to be of the most basic design, so only a single phase has been studied in this work. The first converter consist of an MMC-like phase-leg arrangement and two DC-side capacitors. Between the midpoints of the stacks in the phase-leg and the DC-side capacitors a transformer winding is connected. Across this a square-wave voltage and current waveform is applied. The secondary winding is connected between

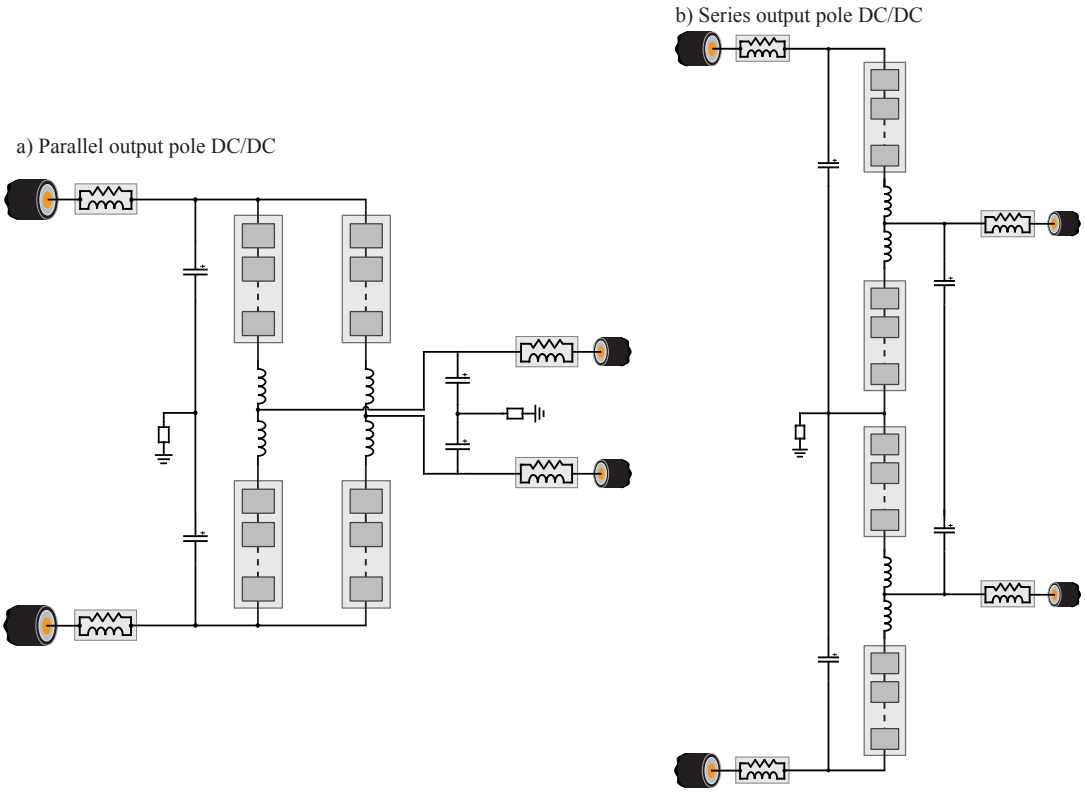

Figure 9.1: Direct-coupled DC/DC converter circuits presented.

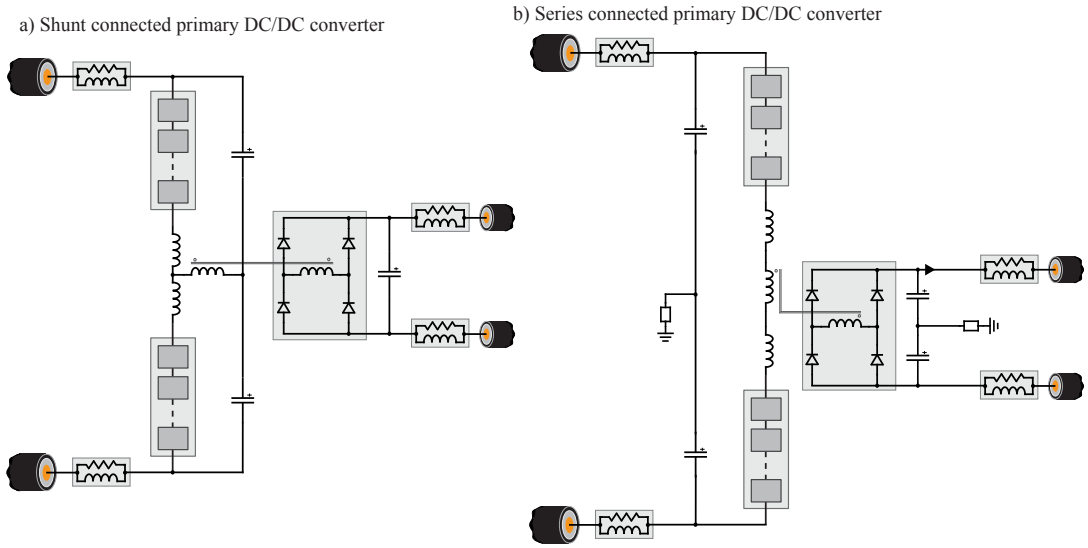

Figure 9.2: Transformer-coupled DC/DC converter circuits presented.

the midpoints of an H-bridge, either active or passive, which rectifies the square-waveforms into DC and connects to the lower voltage DC link. A passive rectifier will limit the power flow from the higher voltage to the lower voltage side, whereas an active bridge allows bi-directional power transfer. As the primary of this converter is effectively connected in parallel to the phase leg, it is also referred to as the square-wave modular DC/DC with shunt connected primary.

The second circuit presented consist of a similar phase leg arrangement, but with the primary winding connected between each stack; it is referred to as the series connected square-wave modular DC/DC converter. The secondary side and rectifier are arranged in the same manner.

The combination of the stacks' transformation-ratio as well as the transformer's step-ratio, allows both of these converters to be operated with a high overall step-ratio. This makes them suitable for HVDC tap applications. Furthermore, the transformer also allows the transformation-ratio of the stacks to be optimised to achieve the lowest possible power capacity ratio. The transformer's step-ratio can then be adjusted to achieve the desired overall step-ratio.

To minimise the losses incurred in the stacks, all four circuits (two direct and two modified DC/AC/DC) only utilise half-bridge cells. To allow the direct-coupled converter topologies to prevent DC-fault propagation, the stacks require extra cells and may have to be of the full-bridge variety. The square-wave DC/AC/DC converters are expected to

be able to cope with DC faults without further cell stack upgrades as the internal AC link can be used to electrically disconnect the two DC sides from each other.

The shunt-connected primary DC/AC/DC converter has been chosen for further study, as it provides the best power capacity ratio and is capable of high step-ratios (it also forms an evolution of the previously investigated front-to-front arrangement). In chapter 7 its controller and its method of operation have been explained in detail.

The use of square-waves means that the DC side filters can be kept particularly small, provided that the square-wave currents can be transitioned quickly between the extremes. To this end these circuits utilise very small arm inductances: a test system for the shunt connected primary converter operated at 20 MW and 100 kV on the high voltage DC link, uses 0.8 mH per arm inductor. In particular, the rate at which these transitions can be achieved depends on the voltage available in the stacks for this control purpose. A control-margin, a measure of the number of additional cells in each stack to implement the current control (i.e. the current transitions) has been investigated in detail. The optimal control-margin has been found to also be the maximum possible one, depending on the transformation-ratio of the stacks, provided only half-bridge cells are used.

This can mean adding a significant number of additional cells, such as 25% for a transformation-ratio of 33:10, relative to the minimum required to generate the AC voltage. It has, however, been shown that such a significant increase does not add significantly to the losses. This is because, for low control margins, the arm current can suffer from a significant overshoot after the transition period, which adds to the losses and the extra cells reduces this at the expense of additional conduction power loss throughout. A quick current transition also allows the DC filters to be particularly small (possibly even redundant, depending on the DC link ripple specification). This converter also requires a careful transformer design because the leakage inductance is in the AC current path and has to be kept very small to allow a quick current transition.

The design trade-offs, which affect the shunt connected converter's efficiency and its volume, have been investigated in detail in chapter 8. The higher the transformation-ratio of the stacks, the higher the losses, which are incurred by them, despite the fact that the number of cells per stack decreases. As the control-margin essentially prevents the operation of the lowest possible transformation ratio (2:1) a compromise can be struck which reduces the losses but allows for enough voltage capability (using half-bridge cells only) to allow for quick current transitions. A transformation-ratio of 33:10 has been identified as a suitable value.

For a 20 MW test system, operated with a step-ratio of 100:10 kV DC and an AC frequency of 500 Hz, the total losses in the stacks, transformer, arm inductors and the

rectifier have been estimated to add up to 315 kW, or 1.57% of rated power. The total capacitance required in the cell stacks is 68 mF, or 6 kJ/MVA. Whilst a like-for-like comparison with the F2F arrangement is difficult (because the step-ratios applied are so very different) each phase in the F2F carried 10 MW and was connected to a 50 kV DC link, which means that the arm currents are of similar magnitude. It can thus be noticed that the shunt connected primary DC/DC operates with a relatively low capacitance (or stored energy per unit rated power) compared with the front-to-front arrangement, in part because it operates at 500 Hz. Compared with the F2F operation at 500 Hz its losses are however significantly lower, implying that this topology is more suited for high frequency operation. The losses could be reduced by lowering the AC frequency but this would significantly increase the total capacitance required.

9.2 Academic contributions by the author

The use of a front-to-front arrangement utilising VSCs had been proposed in the literature by industry but not analysed in any detail. A thorough analysis into the choice of operational parameters for two different VSCs in a F2F arrangement has been performed in chapters three through five. As a result of the findings a design guide for a F2F arrangement has been proposed. In particular, chapter 3 identified the effects of the choice of AC operating voltage on system capacitance and efficiency for a direct-coupled system. Chapter 4 analysed the effect of the introduction of galvanic isolation into the system which creates an additional degree of freedom in form of the transformer ratio. It was identified that this allows each converter to be operated at its optimal point. To support this choice, the effect of choice of AC voltage of each converter on total cell capacitance or losses was analysed. Chapter 5 investigated the effects of raising the AC frequency. The effects on the capacitance and losses in both the semiconductors and the transformer were identified. Circuit-level simulations were used to support and verify the analysis.

In chapter 6 alternative modular cell-based DC/DC converters were proposed. In particular, the modified DC/AC/DC converters had not been presented in the literature. Basic energy balancing mechanisms have been proposed for the four proposed DC/DC converter circuits, as well as strategies on how to upgrade the converters to provide fault propagation prevention capabilities.

The shunt connected primary square-wave converter was selected for more detailed study in chapters 7 and 8. A controller was proposed and verified which controls the converter currents as well as the DC current in the secondary winding and maintains the nominal voltage of the DC side capacitors. Detailed analysis of the voltage capability re-

quired in the stacks to control square-wave currents has been presented and optimal values have been found for a range of transformation-ratios. Design trade-offs were identified that can be made to affect the converter's performance in terms of the cell capacitor size, DC filter size, number of cells, cell rotation frequency, transformer design and choice of switching devices. Identification of these trade-offs is crucial to tailoring the converter design to a particular application with a particular combination of pressures on cost, volume and efficiency.

9.3 Further Work on cell based HVDC DC/DC converters

The direct-coupled converter topologies suffer from two particular problems in their presented arrangement: first, the balancing voltages cause an AC ripple on the lower voltage DC terminals relative to ground. This makes their grounding problematic and may pose a problem when cables are used, as their outer sheath tends to be grounded. Second, the AC balancing currents impose a large current burden on the cells as the step-ratio is increased. Modifications to the circuits could be explored to alleviate both the output ripple and reduce the current burden.

The series-connected primary DC/AC/DC topology has not been studied in great detail yet and may provide advantages over the shunt-connected arrangement in terms of efficiency and cell volume. Furthermore, both it and the shunt-connected topology should be investigated for parallel operation because by utilising more than one phase it may be possible to eliminate the DC-side capacitors. Altering the AC waveforms may also allow for small DC filters, particularly on the low DC voltage side, as was the case with square-wave operation, but with the advantage of a reduced number of cells. This could be achieved by utilising trapezoidal wave-forms which do not require as quick a transition as square-waves do, allowing the converter to operate with a smaller control-margin. This in turn should lower the losses incurred in the cells.

It has been suggested that the parallel output pole direct-coupled converter might be suitable for interconnection of a CSC and VSC link. Due to the large number of CSC point-to-point connections in existence today, this may well prove to be a useful capability and warrants further investigation. Such a converter could be contrasted with a more conventional front-to-front arrangement of a DC/AC VSC and CSC.

So far these converter topologies have been suggested for HVDC applications but with recent advances in silicon carbide and gallium nitride transistor technology, their efficiency may be improved. They also open up the possibility for applications on distribution level voltages. Such converter could also be used in off-shore wind-farm DC collector grids.

Appendix A

Transformer Modelling

In the design of a transformer a number of parameters come together, that all influence the performance measures. Due to this complexity and unavailability of common models, a transformer model, using existing research, was built for this work. This Appendix explains this model and provides the background information to the results relating to transformers presented in the work.

The goal for this model was to have a relatively simple tool with which it is possible to evaluate some basic performance measures of the transformers and explore them as basic operational parameters, like AC frequency, are varied. As with many other aspects of this work the goal was to explore how the volume and losses of the transformer would develop. As mentioned, this was to be a simplified model, which will likely never be complete. As such what is presented here is a snapshot of the state of the model at the time of writing.

The model has not yet been verified against experimental results as a whole. All design equations and methods have however been chosen from peer-review sources, which have themselves verified their work. The model was constructed in Matlab to be able to quickly iterate through a large number of core geometries without having to build specific finite element models.

A.1 Design Procedure

As the dimensions of the transformer greatly influence the losses and volume, the first step is to design a basic transformer given some basic input parameters. Some aspects of the design are optimised to minimise the losses. The flow chart shown in illustrates the basic steps of the algorithm and will be discussed in further detail in this section. Table A.1 provides an overview of the variables used along with a brief description. Figure A.1

illustrates the steps of the design algorithm, which are discussed in more detail in the following sections.

Table A.1: List of variables for design of transformer.

Variable	Units	Explanation
Input parameters		
$V_{p,s}$	V	Primary and secondary voltage profiles
f	Hz	Fundamental frequency of $V_{p,s}$
P	W	Active power rating
n_s	turns	Number of secondary (LV) turns
L_m	H	Magnetising inductance, referred to primary
h_w	m	Height of winding window
Material parameters		
$\hat{B}_m$	T	Peak flux density
D_m	kg m^{-3}	Density
μ_m	H m^{-1}	Permeability
K_m		
α_m		Core loss coefficients
β_m		
Constants		
$\hat{n}_{sc}$	-	Maximum allowed number of strands in cable
$\hat{J}_i$	A m^{-2}	Maximum current density limit
$\check{J}_i$	A m^{-2}	Minimum current density limit

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Table A.1: List of variables for design of transformer.

Variable	Units	Explanation
k_B	-	Flux density safety margin
k_{pT}	-	Packing factor of turns in winding
k_{pS}	-	Packing factor of strands in turn
V_{BDV}	V m^{-1}	Breakdown voltage of transformer oil
k_{BDV}	-	Safety margin of breakdown voltage
μ_0	H m^{-1}	Permeability of free space
μ_{Cu}	H m^{-1}	Permeability of copper (Cu)
ρ_{Cu}	Ωm	Resistivity of copper (Cu)
D_{Cu}	kg m^{-3}	Density of Cu
Core Design		
w_w	m	Width of winding window
r_{fl}	m	Radius of central core leg
r_{hl}	m	Radius of half-leg
r_y	m	Radius of yoke
A_{fl}	m^2	Cross-sectional area of central core leg
A_{hl}	m^2	Cross-sectional area of half-leg
A_y	m^2	Cross-sectional area of yoke
ℓ_m	m	Mean-magnetic path length
P_{cv}	W kg^-1	Specific core loss
P_{core}	W	Core loss

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Table A.1: List of variables for design of transformer.

Variable	Units	Explanation
Winding Design		
d_{icwA}	m	Insulation distance between core and winding A
d_{icwB}	m	Insulation distance between core and winding B
d_{iww}	m	Insulation distance between winding A and winding B
$h_{A,B}$	m	Height of winding A or B
w_w	m	Combined width of windings A and B
$w_{A,B}$	m	Windings widths
$A_{A,B}$	m^2	Area for winding A or B
$A_{tA,tB}$	m^2	Area per turn in winding A or B
$A_{cA,cB}$	m^2	Area of wire in each turn in winding A or B
$A_{CuA,CuB}$	m^2	Area of copper in each turn
$n_{tlA,tlB}$	-	Number of turns per layer
$n_{lA,lB}$	-	Number of layers in winding
$n_{scA,scB}$	-	Number of strands per turn
$r_{cA,cB}$	m	Radius of wire
$D_{sA,sB}$	m	Diameter of strand
$J_{iA,iB}$	A m^{-2}	Current density in winding A or B
$\ell_{A,B}$	m	Mean turn length of winding
$K_{dA,dB}$	-	Normalising factor of winding resistance
$P_{wA,wB}$	W	Power loss if windings

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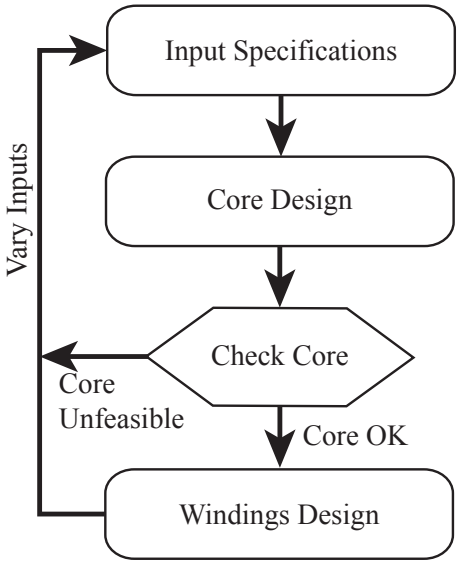

Figure A.1: Flowchart illustrating transformer design algorithm.

Table A.1: List of variables for design of transformer.

Variable	Units	Explanation
$R_{DCwA,DCwB}$	Ω	DC resistance of winding
$R_{ACwA,ACwB}$	Ω	Normalised AC resistance of winding
δ	m	Skin depth
$\bar{d}_{cA,cB}$	m	Mean distance between cables in turns adjacent turns
$L_{\ell A,\ell B}$	H	Leakage inductance in winding
$L_{\ell g}$	H	Leakage inductance in winding-winding gap
k_t	-	Coupling factor

A.1.1 Input specifications

The design of a transformer is influenced by a great number of parameters. Therefore narrowing down the number of variables chosen by the designer is important to limit the scope of the scope of the design algorithm. As this algorithm is used to model transformers for different applications, essential system parameters such as: frequency, power rating and primary and secondary voltages were chosen as inputs. These are the transformer ratings.

Furthermore a number of design parameters have to be specified. The core material can be chosen freely, to allow for a direct comparison of the core losses and dimensions between different materials. Each material is defined by a range of properties, as outlines in table A.1. This data can be obtained from the material's datasheet.

The magnetisation of the core requires a current, which does not contribute the power transfer across the transformer. As this current is supplied by the converter and therefore flows through the semiconductor devices on the cells, limiting this current can lower the losses in the cell stacks. As the magnetising current's magnitude and the magnetising inductance of the transformer are inversely proportional, as per (A.1), either can be chosen as an input parameter.

$$L_m = \frac{\hat{V}_p}{2\pi f I_m} \tag{A.1}$$

: I_m is the RMS value of the magnetising current

Finally the number of secondary turns (throughout the algorithm the secondary is always considered the LV winding) and the internal height of the winding window are required to be specified to allow the algorithm to design the rest of the transformer. During the design stage a sensitivity analysis varying these input parameter can allow their optimisation.

The constants defined in table A.1 remained unchanged throughout all simulations presented in this work. Their values are summarised in table A.2.

A.1.2 Core Design

The core dimensions are computed for a standard shell-type core. Figure A.2 illustrates the core design and dimensions.

The number of turns required in the primary winding to achieve the transformer's step-ratio can be found as per (A.2).

$$n_p = n_s \frac{\hat{V}_p}{\hat{V}_s} \tag{A.2}$$

Table A.2: List of values used for constants.

Variable	Value
$\hat{n}_{sc}$	500
$\hat{D}_i$	$4 \cdot 10^6$
$\check{D}_i$	$1 \cdot 10^6$
k_B	0.1
k_{pT}	0.5
k_{pS}	0.7
V_{BDV}	$12 \cdot 10^3$
k_{BDV}	1

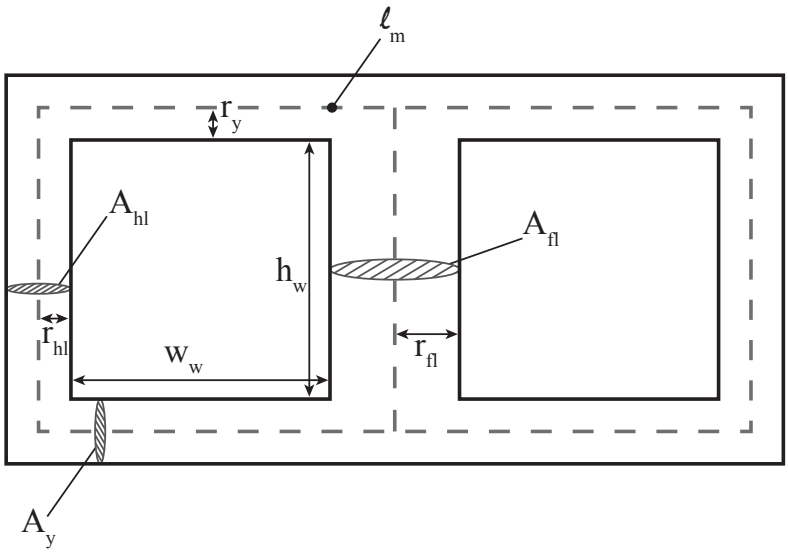

Figure A.2: Shell core design and dimension as used in core design algorithm.

The maximum flux density at which the transformer is to be operated at depends on the flux density safety margin and the core's peak flux-density capability, as described in (A.3).

$$\hat{B}_o = \hat{B}_m \left(1 - k_B\right) \tag{A.3}$$

Using n_p and $\hat{B}_o$ the cross-sectional area of the central full-leg can be calculated using (A.4) [**?**].

$$A_{fl} = \frac{\hat{V}_p}{2 f n_p \hat{B}_o} \tag{A.4}$$

Assuming that the core leg is round, it radius can be found as per (A.5).

$$r_{fl} = \sqrt{\frac{A_{fl}}{\pi}} \tag{A.5}$$

The half-legs and yokes of the core each carry half of the flux flowing though the central full-leg. Therefore to maintain the same flux-density in theses components, their cross-sectional area has to be equal to half that of the central leg. Their cross-sectional area and radius are defined as per (A.6) and (A.7).

$$\begin{aligned} A_{hl} &= \frac{A_{fl}}{2} \\ &= A_y \end{aligned} \tag{A.6}$$

$$\begin{aligned} r_{hl} &= \sqrt{\frac{A_{hl}}{\pi}} \\ &= r_y \end{aligned} \tag{A.7}$$

Using A_{fl} and L_m we can determine the required mean magnetic path length (ℓ_m) to achieve the magnetising inductance L_m, as per (A.8).

$$\ell_m = \frac{\mu_m n_p^2 A_{fl}}{L_m} \tag{A.8}$$

The length of the yoke can thus be found to achieve the required ℓ_m. The width of the inner winding window can therefore be calculated as shown in (A.9).

$$w_w = \ell_m - 2\left(h_w + 2r_y + r_{hl} + r_{fl}\right) \tag{A.9}$$

Knowing this, all core dimensions have been specified. This means that the total core

volume v_c can be found, as per (A.10).

$$\begin{aligned} v_c &= v_{fl} + 2v_{hl} + 4v_y \\ &: v_{fl} = A_{fl} w_h \\ &: v_{hl} = A_{hl} w_h \\ &: v_y = A_y \left(w_w + r_{fl} + 2r_{hl} \right) \end{aligned} \tag{A.10}$$

Using the material specific loss coefficients the specific core loss (P_{cv}) can be calculated using the Modified Steinmetz Equation, as per (A.11), which has has been shown to be highly accurate [106, 105].

$$P_{cv} = \left(\frac{8}{\pi^2} \right)^{\alpha_m - 1} K_m f^{\alpha_m} \hat{B}_o^{\beta_m} 1^{\beta_m - \alpha_m + 1} \tag{A.11}$$

Using the core volume and the specific core loss the total core loss can be calculated as per (A.12).

$$P_{core} = P_{cv} v_c D_m \tag{A.12}$$

A.1.3 Winding Design

Following the design of the core, the size of the internal windows into which the windings have to fit, is known. Figure A.3 illustrates how the windings are arranged on top of each other and figure A.4 denotes the winding's dimensions.

The windings design algorithm is an iterative algorithm which sweeps through a range of different winding sizes to find the solution which generates the lowest total windings losses. First, the maximum possible height of each winding is calculated, as per (A.14), taking the required insulation distances, calculated in (A.13), into account.

$$\begin{aligned} d_{icwA} &= \frac{\hat{V}_p}{V_{BDV}} \left(1 + k_{BDV} \right) \\ d_{icwB} &= \frac{\hat{V}_s}{V_{BDV}} \left(1 + k_{BDV} \right) \\ d_{iww} &= \frac{\hat{V}_p + \hat{V}_s}{V_{BDV}} \left(1 + k_{BDV} \right) \end{aligned} \tag{A.13}$$

$$\begin{aligned} h_A &= w_h - 2d_{icwA} \\ h_B &= w_h - 2d_{icwB} \end{aligned} \tag{A.14}$$

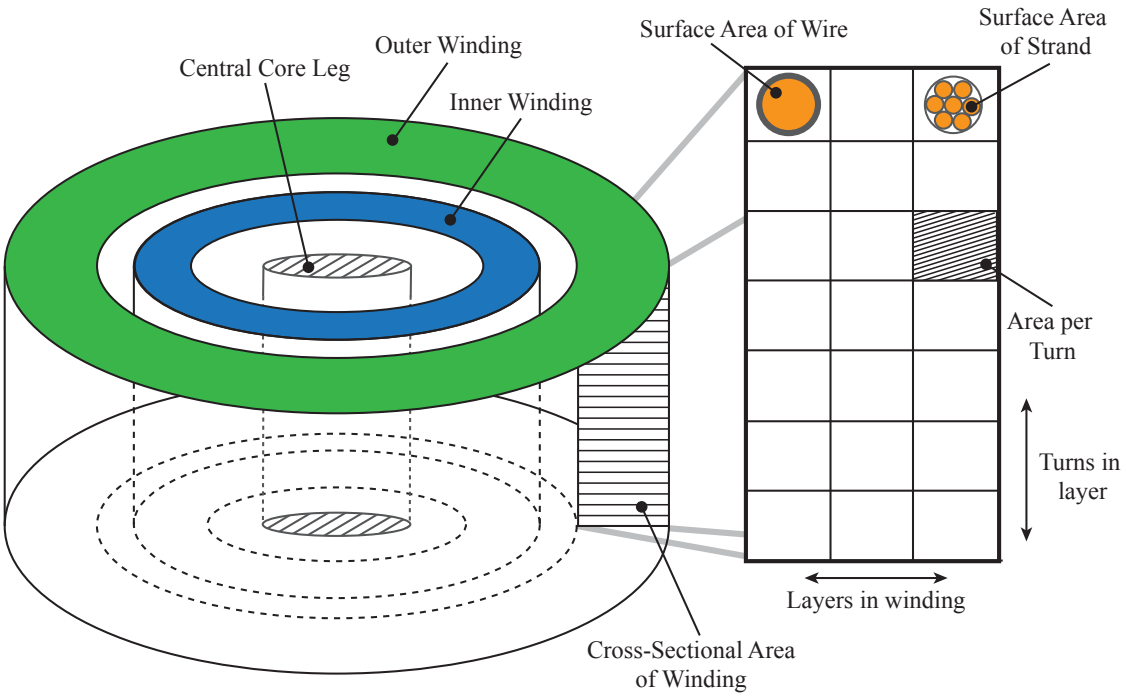

Figure A.3: Illustration of the winding arrangement.

The width of the window available to both windings combined can be found using (A.15).

$$w_{ww} = w_w - d_{icwA} - d_{icwB} - d_{iww} \tag{A.15}$$

To calculate the thickness of the turns, this width has to be split between the two windings. A range of possible width allocations are tried and the resulting winding losses calculated the algorithm then chooses the lowest loss scenario as the best solution. The next few steps illustrate the calculation done for each winding width allocation. First, the winding widths are calculated as per (A.16), such that they sum to w_{ww}.

$$\begin{aligned} w_A &= x w_{ww} \\ w_B &= (1-x) w_{ww} \\ &: \; x = (0, 1) \end{aligned} \tag{A.16}$$

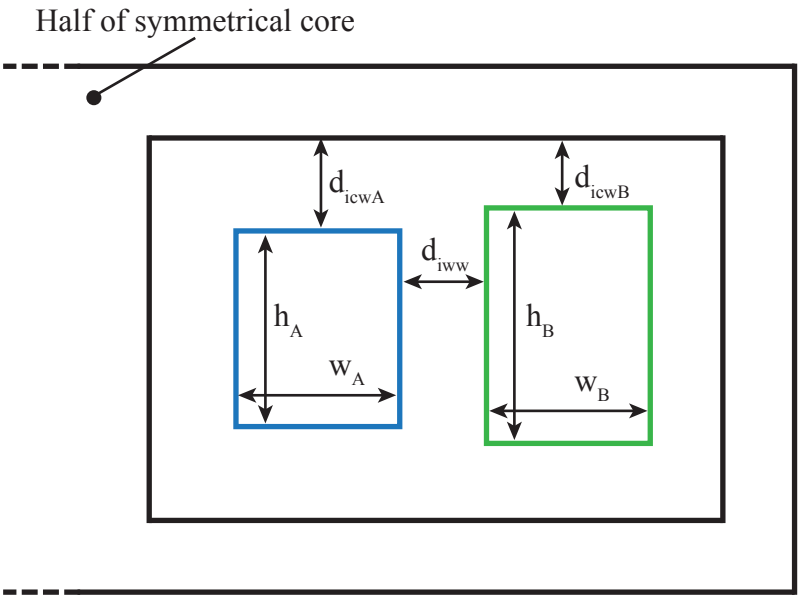

Figure A.4: Winding dimensions.

The allocated area for each winding can thus be found using (A.17).

$$A_A = w_A h_A \tag{A.17}$$
$$A_B = w_B h_B$$

Into the winding's area the required number of turns have to fit. Each turn is modelled to take up a square area as illustrated in figure A.3. This area can be found as per (A.18).

$$A_{tA} = \frac{A_A}{n_p} \tag{A.18}$$
$$A_{tB} = \frac{A_B}{n_s}$$

The number of turns per layer is defined in (A.19) and the resulting number of layers can be calculated as shown in (A.20).

$$n_{tlA} = \left\lfloor \frac{h_A}{\sqrt{A_{tA}}} \right\rfloor \tag{A.19}$$
$$n_{tlB} = \left\lfloor \frac{h_B}{\sqrt{A_{tB}}} \right\rfloor$$

$$n_{lA} = \frac{n_p}{n_{tlA}} \qquad (A.20)$$
$$n_{lB} = \frac{n_s}{n_{tlB}}$$

Each turn is wound using a round cable which takes up a portion of the area allocated per turn. The fact that insulation and turns packing means that not all of the available area is taken up by the cable is modelled by the packing factor k_{pT}. The area available for the cable can thus be found as shown in (A.21) and its radius is defined in (A.22).

$$A_{cA} = A_{tA} k_{pT} \qquad (A.21)$$
$$A_{cB} = A_{tB} k_{pT}$$

$$r_{cA} = \sqrt{\frac{A_{cA}}{\pi}} \qquad (A.22)$$
$$r_{cB} = \sqrt{\frac{A_{cB}}{\pi}}$$

The cable in this algorithm is modelled as Litz wire with n_{sc} round strands. The actual area of copper is therefore limited further due to the packing of the strands by the packing factor k_{pS}, shown in (A.23).

$$A_{CuA} = A_{cA} k_{pS} \qquad (A.23)$$
$$A_{CuB} = A_{cB} k_{pS}$$

Using (A.23) and the RMS value of the winding currents the current density of the turns can be calculated, as per (A.24). The current density of each winding is checked against the minimum and maximum current densities allowed. If the density is below the minimum, the area allocated to the copper in each turn is reduced until the minimum current density is achieved. If the maximum density is exceeded this particular winding widths allocation results in a infeasible solution and the algorithm moves on to the next winding widths split.

$$J_{iA} = \frac{A_{CuA}}{I_p} \qquad (A.24)$$
$$J_{iB} = \frac{A_{CuB}}{I_s}$$

The diameter of the strands can be optimised to minimise the effective AC resistance

of the winding, as described in [107]. The relevant equations for both windings are given in (A.25). The skin depth (δ) used in (A.25) can be calculated using (A.26).

$$\begin{aligned} D_{sA} &= \sqrt{\frac{-a+\sqrt{a^2+12\delta^4}}{2}} \\ D_{sB} &= \sqrt{\frac{-b+\sqrt{b^2+12\delta^4}}{2}} \\ &: a = \frac{(2\pi k_{pS} r_{cA})^2}{4}\left(16n_{lA}^2 - 1 + \frac{24}{\pi^2}\right) \\ &: b = \frac{(2\pi k_{pS} r_{cB})^2}{4}\left(16n_{lB}^2 - 1 + \frac{24}{\pi^2}\right) \end{aligned} \tag{A.25}$$

$$\delta = \sqrt{\frac{\rho_{Cu}}{\pi f \mu_0 \mu_{Cu}}} \tag{A.26}$$

Using the optimal strand diameter the number of strands in the Litz wire can be calculated using (A.27). If the optimal number of strands exceeds the maximum limit, the number strands is lowered to the maximum number and the resulting strand diameter recalculated.

$$\begin{aligned} n_{scA} &= \frac{4r_{cA}^2 k_{pS}}{D_{sA}} \\ n_{scB} &= \frac{4r_{cB}^2 k_{pS}}{D_{sB}} \end{aligned} \tag{A.27}$$

The mean turn length, as calculated in (A.28), is required to calculate the DC resistance of the windings as per (A.29).

$$\begin{aligned} \ell_A &= 2\pi\left(r_{fl} + d_{icwA} + \frac{w_A}{2}\right) \\ \ell_B &= 2\pi\left(r_{fl} + d_{icwA} + w_A + d_{iww} + \frac{w_B}{2}\right) \end{aligned} \tag{A.28}$$

$$\begin{aligned} R_{DCwA} &= \frac{4\rho_{Cu} n_p \ell_A}{\pi n_{scA} D_{sA}^2} \\ R_{DCwB} &= \frac{4\rho_{Cu} n_p \ell_B}{\pi n_{scB} D_{sB}^2} \end{aligned} \tag{A.29}$$

The strand diameter can be used to calculate a normalising factor, K_d, which can be used to calculate the AC resistance of the winding from its DC resistance, as described

in [107]. The equations to calculate K_d relevant for this transformer design are shown in (A.30). Using (A.29) the AC resistance can be calculated as per (A.31).

$$\begin{aligned}
K_{dA} &= \frac{\zeta_A}{\sqrt{2}}\left(\Phi_{1A} - \frac{\pi^2 n_{scA} k_{pS} \Phi_{2A}}{24}\left(16n_{lA}^2 - 1 + \frac{24}{\pi^2}\right)\right) \\
K_{dB} &= \frac{\zeta_B}{\sqrt{2}}\left(\Phi_{1B} - \frac{\pi^2 n_{scB} k_{pS} \Phi_{2A}}{24}\left(16n_{lB}^2 - 1 + \frac{24}{\pi^2}\right)\right) \\
&: \zeta_A = \frac{D_{sA}}{\delta} \\
&: \zeta_B = \frac{D_{sB}}{\delta} \\
&: \Phi_{1A,1B} = 2\sqrt{2}\left(\frac{1}{\zeta_{A,B}} + \frac{\zeta_{A,B}^3}{3 \cdot 2^8} - \frac{\zeta_{A,B}^5}{3 \cdot 2^{14}}\right) \\
&: \Phi_{2A,2B} = \frac{1}{\sqrt{2}}\left(\frac{-\zeta_{A,B}^3}{2^5} + \frac{\zeta_{A,B}^7}{2^{12}}\right)
\end{aligned} \tag{A.30}$$

$$\begin{aligned}
R_{ACwA} &= K_{dA} R_{DCwA} \\
R_{ACwB} &= K_{dB} R_{DCwB}
\end{aligned} \tag{A.31}$$

The AC resistance can thus be used to estimate the winding losses using the RMS winding current as shown in (A.32). For each winding width split the total winding loss $P_{windings}$ is calculated. The split which produces the lowest total winding loss is chosen as the best solution for those particular core dimensions and transformer ratings.

$$\begin{aligned}
P_{wA} &= I_p^2 R_{ACwA} \\
P_{wB} &= I_s^2 R_{ACwB} \\
P_{windings} &= P_{wA} + P_{wB}
\end{aligned} \tag{A.32}$$

As the exact arrangement of the turns and windings has been calculated, the leakage inductance can be found for each winding using the method described in [108]. In his method Dowell calculated the leakage inductance based on the energy stored within the windings and the insulation gap between them. The leakage inductance due to the insulation gap between the windings is described as per (A.33).

$$L_{\ell g} = \frac{\mu_0 \ell_A d_{iww} n_p^2}{h_w} \tag{A.33}$$

The leakage inductance of the windings depends on the mean distance between turns

on the windings, due to the packing factor. As each conductor is modelled as a round wire, the mean distance between two wires can be estimated using (A.34). Using this, the leakage inductance of both windings can be found as described in (A.35).

$$\begin{aligned} \bar{d}_{cA} &= \sqrt{A_{cA}} - \frac{\pi r_{cA}}{2} \\ \bar{d}_{cB} &= \sqrt{A_{cB}} - \frac{\pi r_{cB}}{2} \end{aligned} \tag{A.34}$$

$$\begin{aligned} L_{\ell A} &= \frac{\mu_0 \ell_A d_{iww} n_p^2 d_{cA}(n_{lA}-1)}{3h_w}\left(1 - \frac{1}{2n_{lA}}\right) \\ L_{\ell A} &= \frac{\mu_0 \ell_A d_{iww} n_s^2 d_{cB}(n_{lB}-1)}{3h_w}\left(1 - \frac{1}{2n_{lB}}\right) \end{aligned} \tag{A.35}$$

In [108] the leakage inductance calculated in for the gap between the windings is referred to the primary side. Therefore the primary and secondary leakage inductances can be calculated as per (A.36).

$$\begin{aligned} L_{\ell p} &= L_{\ell A} + L_{\ell g} \\ L_{\ell s} &= L_{\ell B} \end{aligned} \tag{A.36}$$

The coupling factor is an easy to use measure of the leakage inductance relative to the magnetising inductance. It can be calculated using the magnetising and leakage inductances as shown in (A.37) [103].

$$k_t = \frac{L_m}{L_m + L_{\ell p}} \tag{A.37}$$

A.2 Model Limitations

At present the transformer model does not take temperature into account. This has two main drawbacks: first the losses in reality are a function of temperature as the material coefficients change significantly with temperature. As the operating temperature of the core and windings is typically at around 80°C this can have a significant impact on the losses, which are modelled at 25°C. Second, the cooling required to keep the core at a sensible operating temperature, to prevent it from melting for instance, may require larger distances between the windings and the core to allow sufficient oil to flow and take the heat out of the components. This in turn will affect the leakage inductance calculations as well as overall volume of the transformer. more significant on the total volume though,

may be the volume required for the heat-exchanger on the outside of the transformer case.

Appendix B

Analytically Estimating Losses in Semiconductors

From the literature it is known that the semiconductors constitute a large portion of the total converter losses. To judge the converter efficiency a method of modelling the losses is required. The method presented here is based on initial work done by Dr. P. Mitcheson. More general details on semiconductor losses can be found in [109].

B.1 Analytical Semiconductor Loss Estimation

The losses in a switching device, like an IGBT, are incurred, can be split into two categories: the conduction and the switching losses. The conduction losses are incurred due to a voltage drop across the device, when it is active and a current is flowing through it. The switching losses are incurred when the device changes state, i.e. turn-on and turn-off, and are due to the fact that the current through the device nor the voltage across it change instantaneously. Instead Instead a certain delay is incurred as illustrated in figure B.1.

The losses in this work are estimated from a Simulink simulation model. The switching devices used in this simulation do not model the realistic current and voltage behaviour of a switch. To nonetheless accurately estimate the losses incurred in each device the following methodology was used: First, a device was selected and its loss characteristic curves, with respect to its collector current (I_C), were extracted. Data sheets provide on-state voltage drops as a function of the collector current, as shown in figure B.2. The switching losses are typically measured for a certain collector-emitter voltage (V_{CE}). As the switching losses can be seen to be a function of I_C as well as V_{CE} the switching-loss data is normalised with the indicated test V_{CE}. This results in a function of switching

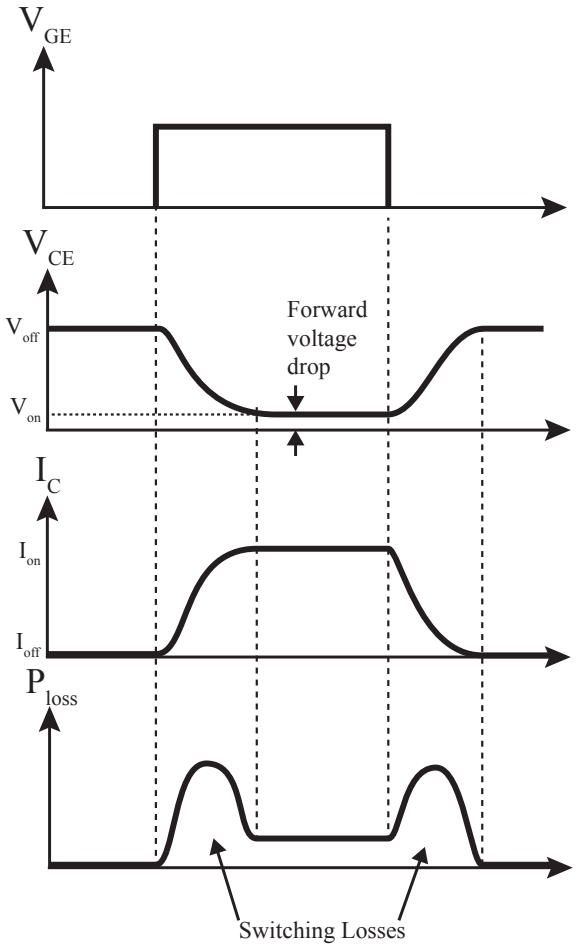

Figure B.1: Realistic current and voltage behaviour in a switching device.

energy loss with respect to I_C as shown in figure B.3.

In the simulation the I_C, V_{CE} and the gate signals are measured and used to determine the semiconductor losses for each switch individually. The conduction loss function uses the gate signal to determine from which time-step onwards the device is active and feeds the measured I_C through a function block which implements the device specific forward voltage drop and the resulting loss, using (B.1).

$$P_c = f_{Vce}(I_C[k])I_C[k] \tag{B.1}$$

The switching losses use time-delayed measurements to take the trailing effect of both the voltage and current during a change of state into account. Taking a turn-on loss as an example: the value of V_{CE} one time-step before the gate signal indicates a change in state is used in conjunction with the present current measurement. The normalised switching loss is scaled using the measurement of V_{CE} as per (B.2) to (B.4).

$$P_{on} = f_{E-on}(I_C[k])V_{CE}[k-1] \tag{B.2}$$

$$P_{off} = f_{E-off}(I_C[k-1])V_{CE}[k] \tag{B.3}$$

$$P_{erec} = f_{E-erec}(|I_C[k-1]|)V_{CE}[k] \tag{B.4}$$

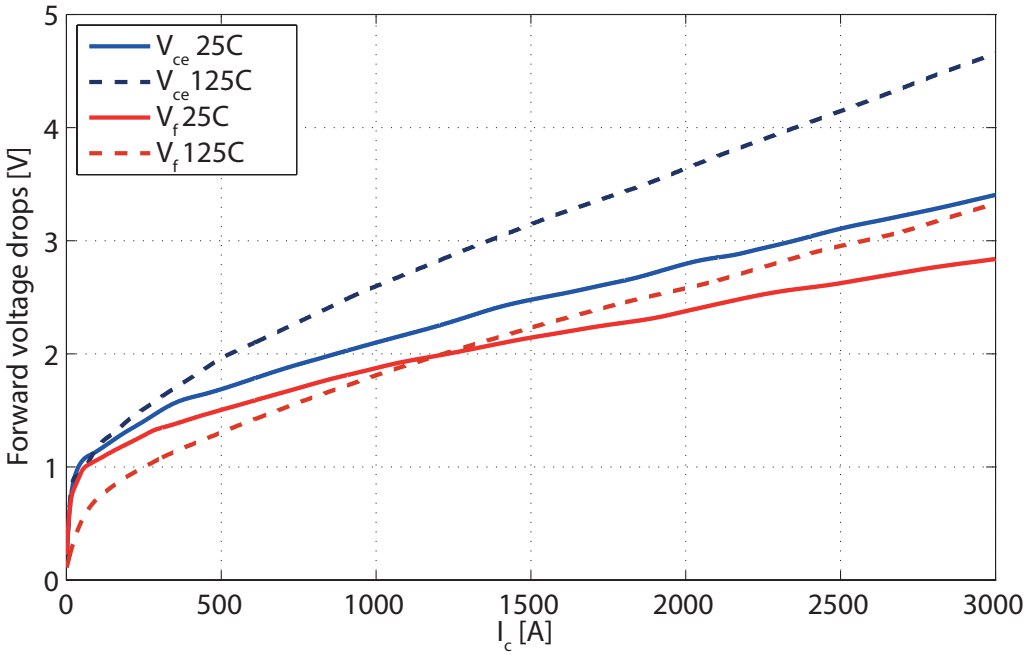

Figure B.2: Forward voltage drops of IGBT and anti-parallel diode for Mitsubishi CM1500HG66R device.

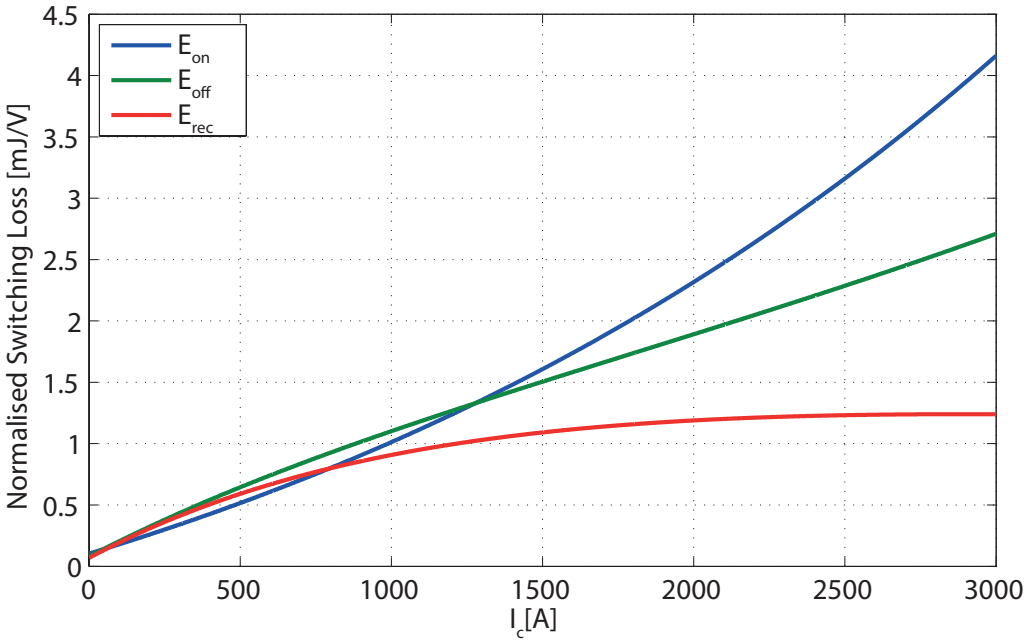

Figure B.3: Switching energy loss of IGBT and anti-parallel diode Mitsubishi CM1500HG66R device.

Appendix C

Inductor Modelling

The Brooks coils utilises an air core and the ideal ratio of the radius of the coil to its thickness to minimise the losses, as described in [110]. In this appendix the methodology of the inductor losses calculation is described.

C.1 Brooks Coil Inductor Calculations

The dimensions of a Brooks coil are illustrated in figure C.1. From the definitions of the brooks coils, as described in the diagram, the cross-sectional area of each conductor, A_c, can be found as per (C.1). The variable k_B is the packing factor, and a typical value of 0.5 is used for the results and n refers to the number of turns on the coil.

$$A_c = \frac{k_B c^2}{n} \tag{C.1}$$

By definition of the Brooks coil, the inductance can be found as per (C.2).

$$\begin{aligned} L &= k_L \mu_0 c n^2 \\ &\therefore\ k_L = 2.02845 \end{aligned} \tag{C.2}$$

When the inductor is designed, only its inductance is known. Equations (C.1) and (C.2) can be combined to find an expression for c, as showing in (C.3).

$$\begin{aligned} A_c &= \frac{k_B c^2 \sqrt{k_L \mu_0 c}}{\sqrt{L}} \\ \therefore c &= \left(\frac{A_c \sqrt{L}}{k_B \sqrt{k_L \mu_0}} \right)^{\frac{2}{5}} \end{aligned} \tag{C.3}$$

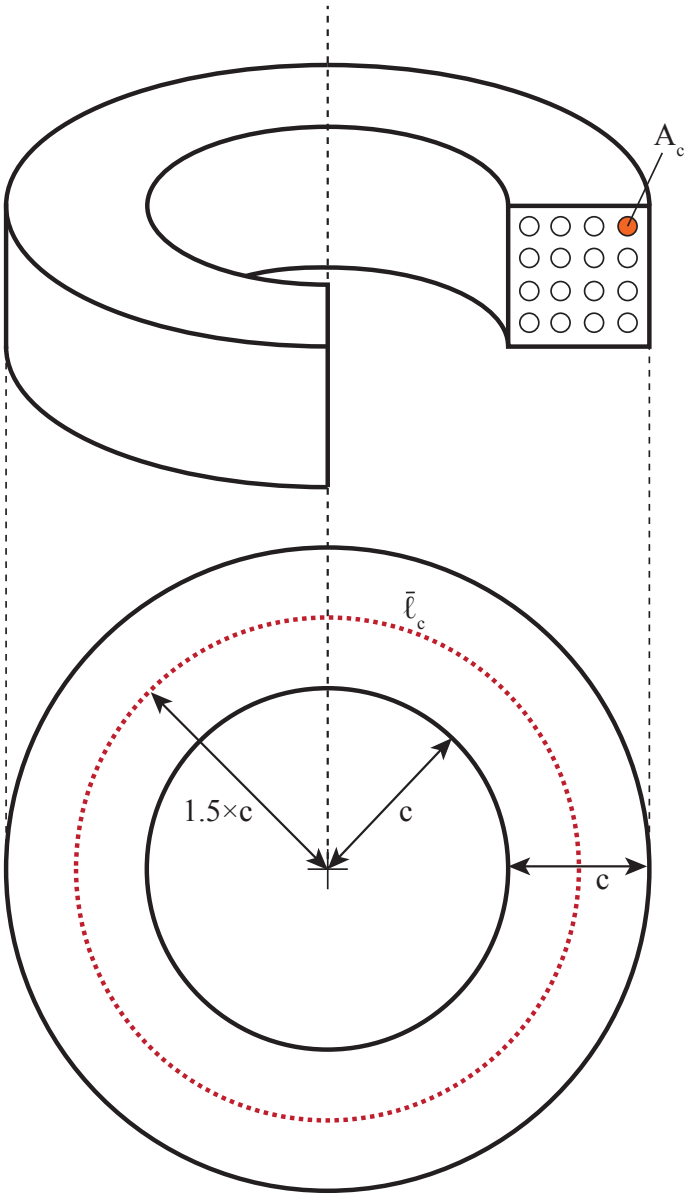

Figure C.1: Brooks coild dimensions and labels.

To solve equation (C.3) the cross-sectional area of each conductor needs to be known. A common design practise is to fix a certain current density for the turns, in this case $10^6 Am^{-2}$. As the RMS current through the arms can be found through simulation or analytically, the cross-sectional area required to achieve the desired current density can be found.

Once c has been found for a desired inductance, L, the mean length per turn can be found using (C.4).

$$\bar{l}_c = 3\pi c \tag{C.4}$$

Thus the resistance in the coil can be found to estimate the conduction losses in the coil as per (C.5). The variable ρ_{Cu} refers to the resistivity of copper.

$$R_L = \frac{n\bar{l}_c\rho_{Cu}}{A_c} \tag{C.5}$$

Appendix D

Terms and labels used in this document explained

Transformer refers to the passive, magnetic variety in this thesis always.

***Converter* Arm** refers to a fraction of a converter leg, consisting of a group of series connected devices. An arm typically contains a stack of cells and an arm inductance.

***Converter* Leg** consists of a number of arms, typically two. It represents the series components which are connected in shunt between two DC poles.

***Cell* stack** denotes a group of series connected cells.

Cell in the context of this thesis refers to either half- or full-bridge arrangement which applies the voltage of a capacitor across the terminals of the cell. In the wider context a cell can also refer to other arrangements which fulfil a similar purpose but may contain more switches and/or other energy storage devices.

***Energy* deviation** denotes the reoccurring difference between the instantaneous energy and the nominal (or average) energy, typically referred to in the context of a capacitor or cell stack. Integrating the energy deviation over a full cycle equals to zero.

***Energy* drift** denotes the difference in energy at the beginning and end of a full cycle.

MMC refers to the Modular Multilevel Converter used for AC/DC conversion. Also see VSC.

AAC refers to the Alternate Arm Converter which is a modification on the MMC. Also see VSC.

VSC refers to a Voltage Source Converter. In a VSC HVDC link a power flow reversal is achieved by reversing the current flow.

CSC refers to a Current Source Converter. In a CSC HVDC link a power flow reversal is achieved by reversing the voltage polarity.

HVDC refers to High Voltage Direct Current. It is a term commonly used when referring to DC connections used for transmission purposes.

Power Capacity Ratio describes the ratio of the installed apparent power capacity relative to the power rating of a cell stack or a converter.

MIMO stands for Multiple-In-Multiple-Out and is often used in the context of control or signal processing.

over- or under modulation describes whether the AC voltage generated by a converter has a magnitude larger than (over-modulated) or less (under-modulated) than the DC terminal voltage

DC terminal refers to the connection made between a converter and a DC cable or over-head line

F2F is an abbreviation for Front-to-front and refers to the arrangement of two DC/AC converter connected via their AC sides

DiCP is an abbreviation for Devices in the Conduction Path and is used as an indicator to the converter efficiency

LQR is an abbreviation for Linear Quadratic Regulator, which refers to a method of calculating controller gains based on minimising a cost function

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