Patterning methods for organic electronics

A thesis submitted in partial satisfaction for the degree of Doctor of Philosophy

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This thesis describes the work carried out between October 2010 and October 2013 in the ‘Nanostructured Materials and Devices’ group of Imperial College London, under the supervision of Professors John de Mello and Thomas Anthopoulos.

The material in this thesis has not been previously submitted for a degree at any university and, except where explicitly stated, is the product of my own work.

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Abstract

Organic electronics is an exciting new avenue for low cost electronics. The unique properties of organic semiconductors may enable a new generation of electronic devices to be fabricated into flexible, large area, and even transparent consumer products. However, for this to become a reality, many challenges must first be overcome. As the performance of these materials continues to improve, it is now necessary to look to new manufacturing methods and materials that can fully exploit the advantages of organic materials.

The work presented in this thesis is focused on the development of new and high resolution fabrication methods which are compatible with organic electronic materials. The findings presented in the first half of this thesis are based on the idea that fundamentally new forms of manufacturing are required to match the unique properties of organic materials. Initially the adhesion properties of several materials are analysed with a focus on how they interact at the nano-scale. Further work then outlines how adhesion forces can be manipulated and used to produce highly aligned nano-scale electronic devices, something that until now has required high cost and specialist equipment.

The second part of this thesis describes how existing fabrication methods can be modified to produce high performance organic devices. By creating self-aligned organic transistors, higher frequency device operation and enhanced performance may be possible. New materials such as graphene and low voltage nano-scale dielectrics are tested in this configuration and compared with similar devices reported in the literature.

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Contents *Page*

1.0 Introduction 7
1.1 Background 7
1.2 Thesis outline 9

2 Literature review 12
2.1 Organic field effect transistors 13
2.1.1 Physical attributes of OFETs 15
2.1.2 OFET architecture 17
2.1.3 Operating principles of OFETs 19
2.1.4 Current-voltage regime 20
2.1.5 OFET parameter extraction 22
2.2 Fabrication techniques 25
2.2.1 Photolithography 27
2.2.2 Electron beam lithography 29
2.2.3 Printing 30
2.2.4 Nano-transfer printing 31
2.2.5 Metal transfer printing 33
2.2.6 Cold welding 35
2.2.7 Hot lift-off 36
2.2.8 Controlled cracking 37
2.2.9 Chemical lithography 39
2.2.10 Thermo-chemical AFM 40
2.3 Conclusion 42

3 Experimental 48
3.1 Peel testing 48
3.2 Atomic and scanning electron microscopy 50
3.2.1 Atomic force microscopy 50
3.2.2 Scanning electron microscopy 53
3.3 Contact angle measurements 56
3.4 Metal deposition 58
3.5 Self-assembly monolayer deposition 60
3.6 Sample fabrication 61
3.6.1 Adhesion lithography sample fabrication 61
3.6.2 Self-aligned gate sample fabrication 65
3.7 Electrical measurements 66
3.7.1 Current-voltage measurements 66
3.7.2 Photodiode measurements 67

4 Adhesion lithography 69
4.1 Adhesion measurements 70
4.1.1 Glass adhesion properties 74

4.1.2 Al adhesion properties 76
4.1.3 Au adhesion properties 78
4.1.4 Benzocylobutene adhesion properties 80
4.1.5 Summary of adhesion properties 82
4.2 Adhesive patterning 83
4.2.1 Peel testing 85
4.2.2 Advanced peel testing 89
4.3 Adhesive fracture mechanics 101
4.4 High-resolution adhesive patterning 109
4.4.1 Adhesion lithography nano-devices 116
4.4.2 Alternative configurations 119
4.5 Conclusion 120

5 Self-aligned transistors 125
5.1 SU8 photoresist 126
5.1.1 SU8 processing parameters 127
5.2 Self-aligned gate fabrication process 131
5.2.1 Fabrication and optimisation of self-aligned gate devices 133
5.2.2 Self-aligned gate development 139
5.3 Self-aligned gate devices 150
5.3.1 High voltage self-aligned gate devices 151
5.3.2 Low voltage self-aligned gate devices 153
5.4 Nano-scale self-aligned gate structures 157
5.5 Conclusion 165

6 Conclusion and further work 170
6.1 Conclusion 170
6.2 Further work 176

Appendix 178

1

Introduction

1.1 Background

Electrical devices, which utilise organic materials such as conjugated polymers and small molecules, are being actively developed for use in commercial devices [1-3]. Unlike their inorganic counterparts, many organic materials can be solution processed into thin films at room temperature [4, 5]. This not only offers the prospect of reducing the price of the manufactured product, but also the amount of energy required for the production of electronic devices.

The principal building block of any complex electrical circuit is the transistor, which can be likened to an electronic switch [6]. When integrated into a large array of other transistors, useful computational tasks can be performed in fast succession. While silicon transistors are by far the most commonly used form of transistor, organic field-effect transistors (OFETs) offer attractive new opportunities in many emerging fields [7, 8]. Unfortunately the charge carrier motilities seen in most OFETs are not yet high enough to make commercial implementation of these devices viable at the present time [9-11]. However the ability to engineer new organic semiconductors through standard organic chemistry has led to a steady improvement in material properties.

An example of an electrophoretic display using flexible OFETs as the drive circuitry is shown in **Figure 1**. While this concept is technically feasible, with demonstrations devices produced by at least one company [12], the current generation of organic devices do not possess the required performance or stability for retail products [13, 14]. One challenge facing organic materials is that they lend themselves to solution processed manufacture techniques which are incompatible with most inorganic fabrication methods [15, 16]. This has resulted in the need to develop new and novel fabrication systems specifically for OFETs and related devices [17]. Without the development of new fabrication methods, products based on organic materials will most likely not be possible.

Figure 1: Photograph of a flexible electrophoretic display manufactured using OFETs by Plastic Logic.

1.2 Thesis outline

This thesis describes research conducted to further advance the fabrication of OFETs and related organic electronics devices. New fabrication methods have been researched that may enable the future development of organic electronic based devices. The aim of the work described here is to develop new ways to fabricate organic devices in a scalable manner with optimum performance. Some of the specific issues addressed by this work include:

- Downscaling of organic transistors to an extent that they can operate at the high frequencies required for modern display panels and communication devices.
- Reduction of the operating voltage used in organic devices to enable their use in portable applications.
- An assessment of the role adhesion plays when fabricating devices, and how it can be controlled to enable high resolution patterning.
- Characterisation of the adhesion properties of various materials and their interactions with each other during fabrication.
- Modification of the adhesion properties of materials, using various surface coatings and heat treatments.

The research presented here is divided into two main experimental chapters. The first chapter discusses work related to the adhesion properties of various materials and new adhesion fabrication techniques. A number of characterisation techniques are used in this section, including peel testing and nano-scale adhesion testing using an atomic force microscope (AFM). The understanding gained throughout these measurements is used to fabricate nano-scale photo-diodes using a new technique we call “adhesion lithography”. We show how the technique can be used to fabricate discrete working

electrical devices, offering the prospect for more complex integrated circuits in the future.

The second chapter reports methods for fabricating self-aligned OFETs (in which the gate electrode is precisely positioned in the channel region above the source and drain electrode) without the use of highly complex or expensive equipment. Results indicate that it is possible to use a simple back illumination technique combined with optimum thermal crosslinking to fabricate working self-aligned transistors. The concept is demonstrated using several semiconductors and low voltage dielectrics. Additional work is also presented to show how the techniques could be further downscaled using a combination of lithography and ink-jet printing.

Finally a short conclusion is presented where a summary of the work and future outlook for the techniques developed is presented.

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2 Organic electronics literature review

There is significant research and commercial interest in the use of organic semiconductor based materials for electrical applications [1]. The beneficial properties of these materials include large area processing [2], solution deposition [3], low-temperature deposition [4], transparency [5] and flexibility [6]. OFETs have already been demonstrated in applications like radio frequency identification tags [7], sensors [8], memory devices [9] and flexible displays [10]. Researchers have made great progress in developing new polymers with increased performance and also in understanding how they operation [11]. This chapter will review current research trends in organic electronics with a major focusing on new fabrication methods which are currently under investigation. A brief outline of their physical properties and operating principles is also included.

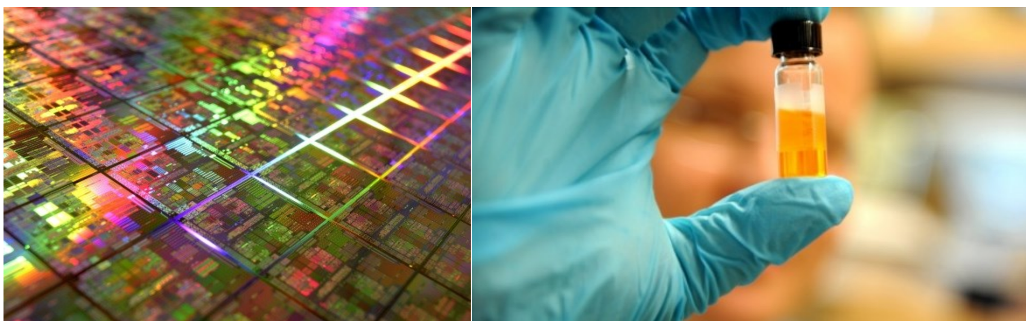

Figure 1: Left: Photograph of an integrated circuit fabricated using traditional materials such as Silicon. Right: Photograph of a vile of a semiconducting polymer ink, a new type of semiconductor material.

2.1 Organic Field Effect Transistors

Organic semiconductors are an emerging class of materials with the potential to replace silicon as the active material in field effect transistors (FETs) [12] for selected applications. Organic field effect transistors (OFETs) do not require expensive high temperature processing and those based on polymeric and soluble small molecule semiconductors can be deposited from solution below 120°C. Broadly speaking there are three types of organic semiconductor materials: polymers, solution processed small molecules and vacuum processed small molecules [13].

Figure 2 shows differences of the field effect mobility of various organic seminconductors based on their solubility. Recently OFETs have shown they can perform at a similar level to some of their inorganic counterparts, such as amorphous silicon paving the way for their future use in electrical devices [14].

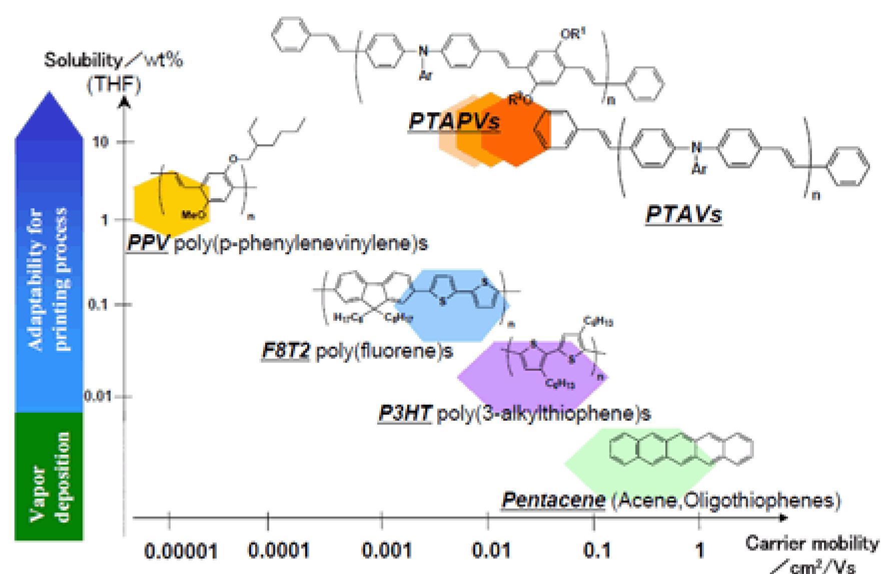

Figure 2: Relation between carrier mobility and solubility of organic semiconductors when dissolved in tetrahydrofuran (THF) or deposited by thermal evaporation. Image reproduced from [15].

The ability of organic materials to transport electronic charge arises from their conjugation. Covalently bound carbon atoms are present in the form of single and double alternating bonds; in the case of hydrocarbons, conjugation along the molecular chain causes delocalisation of one of the four valence carbon electrons allowing charge transport to occur [16]. A detailed description of the origins of charge transport in organic materials is outside the scope of this work, but many authors have presented accounts of such systems, notably in references [17-19].

Of importance for OFET performance is the ability of a thin film of organic material to organise into an ordered film where weak Van der Waals intermolecular bonds can facilitate charge transport through the film. The electronic wave function is either localised to individual molecules or to small groups of molecules along the carbon chain rather than the entire film. The ability of organic semiconductors to transport charge is, therefore, largely determined by intermolecular hopping through the organic material and is affected by the presence of trap states as well as chemical purity and crystallinity [17]. Solution processed amorphous molecular systems can be modelled using variable range hopping theory (VHR) [20]. This model assumes that a hopping event (between two localised electronic states) occurs by quantum mechanical tunnelling through internal energy barriers created along the molecular chain. Hopping is a thermally activated process and therefore mobility increases with temperature. The activation energy for hopping in a molecular system is determined by the distance to the next site. Short hopping events have small activation energies while large hopping events will have larger energies. As will be discussed later in this chapter, an applied gate voltage will induce the filling of lower energy states within the OFET channel, reducing the activation energy and increasing mobility. The degree of electronic

overlap between wave functions on the molecular chain and the number of available hopping sites have a critical influence on device performance [16].

Small molecules organic semiconductors are typically deposited using traditional semiconductor fabrication methods, such as thermal evaporation. Such films have a tendency to form larger, more ordered polycrystalline films where the overlap of the molecular orbit is greater than that of solution processed polymers [21, 22]. As such VRH theory may not be sufficient to describe such a system (since hopping occurs over shorter distances). Instead the multiple trapping and release model (MTR) has been applied, [23] where it is assumed that charge carriers are localised within chemical defects which act as localised trap states. Carriers are then promoted to a short-lived energy band above the trap states where they are available for transport. Transport is now limited by the offset in energy levels between the trap level and 'extended-state' band [24, 25]. There is much debate within the scientific community about the exact mechanisms of charge transport within organic materials, but the two models presented above have been most widely used.

2.1.1 Physical attributes of OFETs

Polythiothene has been extensively researched for used as a semiconductor in OFETs [26, 27]. Although insoluble, which would prohibit its use as a solution processable material, wet synthesis methods have been developed to attach alkyl chains along the molecular backbone, inducing solubility [28]. The molecular design of such materials is of critical importance to the performance of organic devices. For example, by designing polymers to self-organise into crystalline lamellas, the intermolecular orbital overlap can increase charge transport. An early report was presented in ref [29], where the performance of regioregular poly(3-hexylthiophene-2,5-diyl) (rr-P3HT)

OFETs (a polymer which has strong intermolecular interactions between repeating alkyl side chains) was found to depend on the molecular weight, degree of regioregularity and deposition conditions. In turn these factors heavily influenced the orientation of the polymer lamella structure. It was believed the π-π stacking of the P3HT molecules was improved through the introduction of ordered lamellae, with charge transport enhanced in the direction perpendicular to the lamella. In addition the mobility of rr-P3HT was initially found to depend on the domain size and the degree of interconnection between lamellae. For example, large molecular weights resulted in smaller domains but a greater degree of interconnection [30]. The high degree of conjugation in such films results in a reduction of the polymer's ionisation potential and increased vulnerability to oxidation, making air-stable operation challenging without encapsulation [31].

Another example of a high-mobility semi-crystalline organic semiconductor is poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (pBTTT) which has a reported mobility as high as 1.1 $cm^2 V^{-1} s^{-1}$ [31]. In such polymers charge transport occurs in the plane of the film along the interface of the OFET where the motion of charges is not impeded by the presence of insulating side chains. The performance of pBTTT can be increased by inducing the formation of more semi-crystalline regimes. In one such report pBTTT was deposited onto a hydrophobic substrate, resulting in a reduction in surface nucleation sites and improved long range order and device performance in terms of mobility (**Figure 3**) [32].

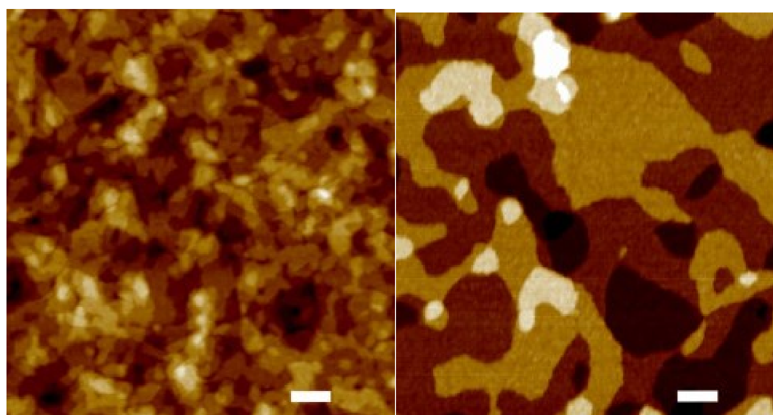

Figure 3: Left: non-surface-modified substrate results in disorder and lower charge transport. Right: A hydrophobic substrate (modified with a self-assembled monolayer) promoted the formation of crystalline regions and improves molecular order resulting in enhanced OFET mobility. Image reproduced from [32].

More recently high performance donor-acceptor copolymer such as naphthalenediimide and bithiophene (PNDI2OD-T2) have been reported with electron mobilities of 0.8 $cm^2 V^{-1} s^{-1}$ [33]. While a dip coated copolymer of cyclopentadithiophene and benzothiadiazole (CDT-BTZ) was found to have a mobility of 3.5 $cm^2 V^{-1} s^{-1}$ [34]. Both polymers were first thought to be amorphous, but reported to be semi-crystalline with NDI-T2 adopting a face-on π-stacking structure while CDT-BTZ was found to form a semi-crystalline, edge-on, lamellar structure [35]. Additionally low-bandgap copolymers based on diketopyrrolopyrrole (DPP) have received increasing attention with mobilities of up to 10 $cm^2 V^{-1} s^{-1}$ reported for a DPP copolymer with thienothiophene-based acceptor units [36]. These copolymers do not appear to follow the same trend as highly semi-crystalline polymers such as P3HT or pBTTT, but, perhaps surprisingly they have higher mobilities - the origin of which required require further research to establish.

2.1.2 OFET Architecture

OFETs are composed of an organic semiconducting material through which current flows in a *channel* which connects other parts of the device such that it functions in a similar way to a switch. Two electrodes, the *source* and *drain*, are at opposite sides of the channel (**Figure 4**). In a bottom gate bottom contact TFT a third electrode, the *gate*, is positioned under the organic semiconductor and is used to control the transport of charge occurring through the channel by applying an external voltage [37, 38]. The conductance of the device depends on how much of the channel material is open to the current flowing through it. Small variations in the gate voltage induce large changes in the current flowing in the channel material. Modulation of the gate voltage occurs via a dielectric layer which separates the channel from the gates, preventing the device from shorting [38].

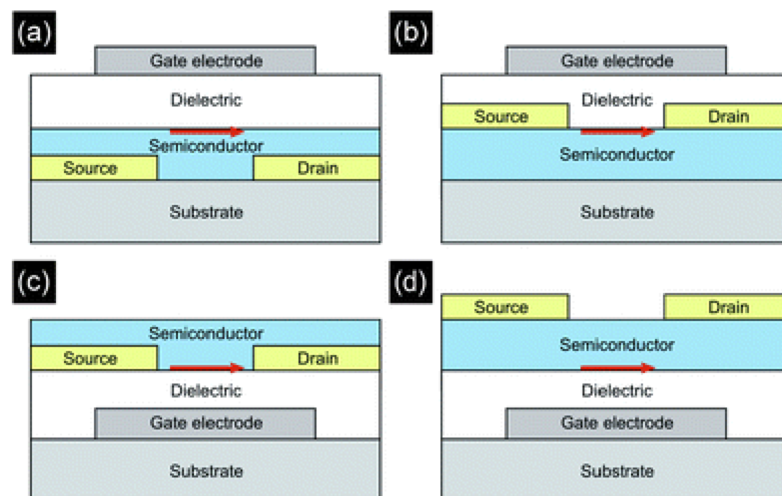

Figure 4: Schematic of four different configurations of OFETs. (a) top-gate bottom-contact, (b) top-gate top-contact, (c) bottom-gate bottom-contact, and (d) bottom-gate top-contact. The arrow shows the charge conduction interface. Image reproduced from [39].

Thus the main elements of an organic transistor are three contacts (*source*, *drain* and *gate*), a semiconducting material and a dielectric layer (**Figure 4**). Organic

transistors differ from inorganic TFTs in that they are intrinsic semiconductors and do not operate in an inversion mode, but rather in accumulation model where charge carriers are accumulated in the semiconductor-dielectric interface [37].

Different combinations of these elements are possible, for example *bottom gate - bottom contact* where the drain and source electrodes are positioned directly on the dielectric film; *bottom gate - top contact* where the source and drain electrodes are grown on the organic semiconductor; and *top gate - bottom contact* in which the dielectric film is deposited on the organic semiconductor and the gate contact is placed on top of it. These configurations can alter the performance and stability of the device; specifically, it is important to consider the effect on the delicate organic semiconductor of depositing metal electrodes on top since the deposition of metals can damage the underlying film. For this reason *bottom gate - bottom contact* OFETs tend to be more widely used as the semiconductor is deposited after the electrodes.

It is common to refer to the voltage applied between drain and source as V_{DS}, while the voltage applied to the gate (more accurately between the source and gate electrodes) is labelled as V_G. By convention, the source is generally grounded and a voltage is applied to the drain contact. The current flowing through the channel is referred to as I_{DS} and it is a strong function of V_G. Similarly the physical dimensions of the channel are described by the channel length (L) and the channel width (W) [40, 41].

The dielectric is sandwiched between the gate electrode and the organic semiconductor. Together they work as two plates of a capacitor. On applying V_G either positive or negative mobile charges accumulate at the interface of the gate/dielectric and dielectric/semiconductor interfaces depending on the applied bias. The accumulated

mobile charges in the semiconductor move in response to the applied V_{DS}. As such the device is *off* when no V_G is applied no free charge carriers are able to flow, while the device is *on* when V_G is applied [37, 40]. The important aspect of the device is the gate induced *field-effect*.

2.1.3 Operating Principles of OFETs

When no electric field is applied to an OFET the organic semiconductor has a completely filled highest occupied molecular orbital (HOMO) and completely empty lowest occupied molecular orbital (LUMO), resulting in an insulating channel between the source and drain electrodes. When a voltage is applied to the gate (V_G) and drain (V_D) electrodes (while keeping the source at ground (V_S = 0)), charges of the opposite sign are attracted to the semiconductor-dielectric interface from the source and occupy available states in the semiconductor channel. The carriers that flow in a semiconductor depend on the energies of the HOMO and LUMO levels with respect to the work function of the source and drain electrodes. For low voltage operation the electrode-semiconductor interface requires good Ohmic contact and the work function of the injecting electrode being close to the HOMO or LUMO level of the semiconductor to avoid the formation of a large potential barrier at this interface. For a *p-type* transistor, when a negative voltage is applied to the gate, holes will be attracted from the source electrode and occupy HOMO states in the semiconductor. Similarly, for an *n-type* transistor, when a positive voltage is applied to the gate, electrons will be attracted from the source electrode and occupy available LUMO states.

For high current flow within the active layer, it is beneficial to have a large number of mobile charges. In most devices however there are usually a high number of charge traps, either within the dielectric or semiconductor. These traps must be filled

before charges can move; as such a minimum gate voltage has to be applied to obtain a free electron density within the channel, which is known as the *threshold voltage* (V_T) [38, 41]. The number of accumulated charges at the semiconductor-dielectric interface is proportional to both the applied gate voltage and the capacitance of the gate dielectric. Once V_T is overcome the free electrons are able to move under the influence of the external field such that current flows from the source to drain electrodes, this is referred to as the *drain current* (I_D).

2.1.4 Current-voltage regime

When no voltage is applied across the source and drain electrodes ($V_D = 0$) and a voltage greater than the V_T is applied to the gate electrode ($V_G > V_T$) a uniform density of charge will accumulate in the channel (**Figure 5 A**). The area number density of induced mobile charge carriers Q_{mob}, at the semiconductor-dielectric interface is given by equation 1. Here C_i is the capacitance per unit area of the gate dielectric [40, 42].

$$Q_{mob} = C_i(V_G - V_T) \quad (1)$$

On the application of a small source-drain voltage ($V_D < V_G - V_T$) carriers within the channel are attracted to the drain. A current will flow while carriers are still being injected from the source, resulting in a linear variation in charge density across the channel (**Figure 5 B**). Under these circumstances the channel resistance at the semiconductor-dielectric interface remains unchanged as the drain voltage is varied. At this point, the transistor is said to be operating in the *linear regime*. As V_D is increased, the spatial distribution of charge carriers becomes nonlinear causing a variation in I_D and V_D as the resistance of the channel increases. The transistor will be “pinched off” when $V_D \geq V_G - V_T$ (**Figure 5 C**), the resistance of the channel is now very high and a depletion region will form next to the drain electrode with no mobile charge carriers

present. The high electric field induced from the depleted region forces carriers to move away from the drain, thereby increasing the pinch-off point further as well. Once "pinch-off" is met, the current is saturated even though the number of accumulated charges only decreases slightly. This occurs as the width of the channel is much larger than the width of the depleted region [37, 42]. The voltage drop between the source electrode and the pinch-off point will remain constant at $V(x) = V_G - V_T$ as the source-drain voltage is increased, and hence the current will remain constant. The device is now operating in the *saturated regime* [41].

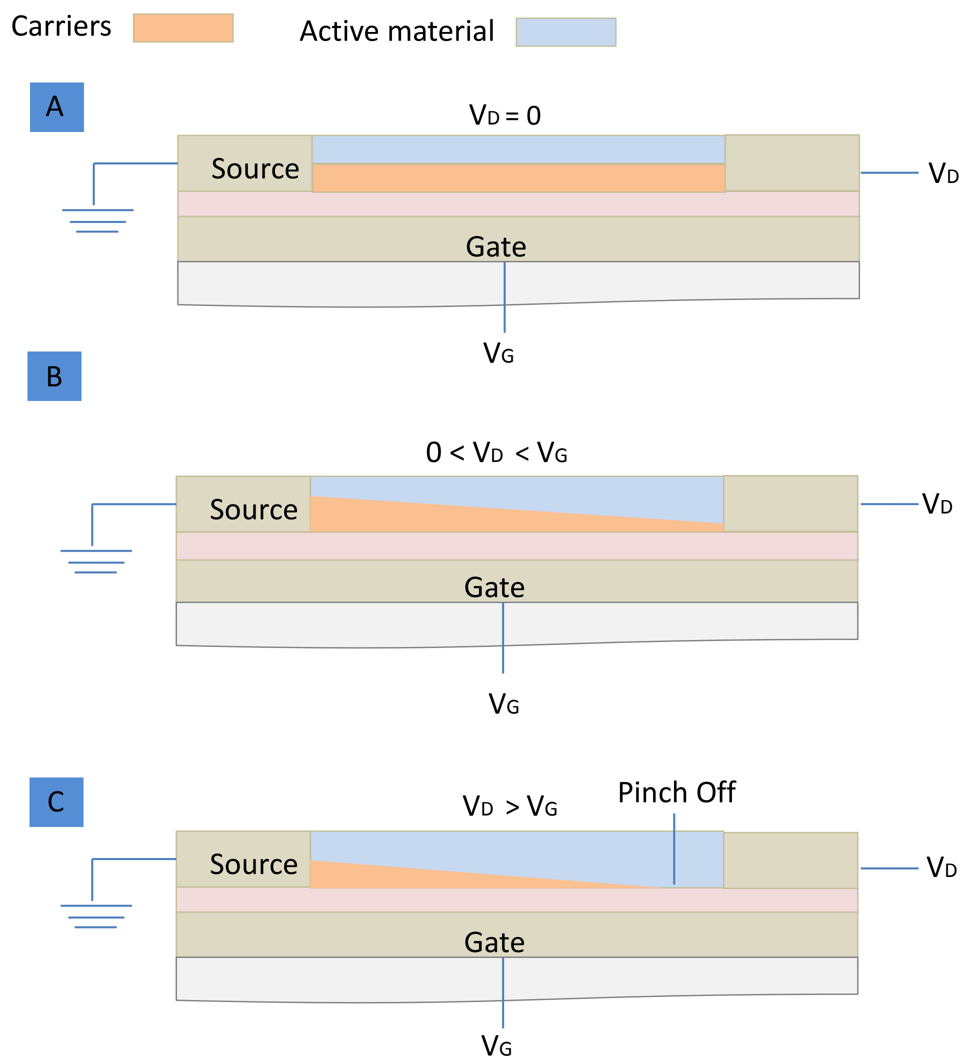

Figure 5: Schematic representation of the charge carrier concentration (orange) as a function of distance from source electrode (x). (a) When there is no drain current and $V_G > V_T$, the carrier concentration is uniform. (b) When $V_D < V_G - V_T$ there is a linear variation in carrier density with x. (c) When $V_D \geq V_G - V_T$, the channel is pinched-off and a depletion region will form adjacent to the drain electrode.

It is possible to extract and quantify a number performance metrics commonly used for the assessment and comparison of OTFTs from experimentally acquired transfer (**Figure 6 A**) and output curves (**Figure 6 B**). The most commonly used values are discussed in more detail in the following section.

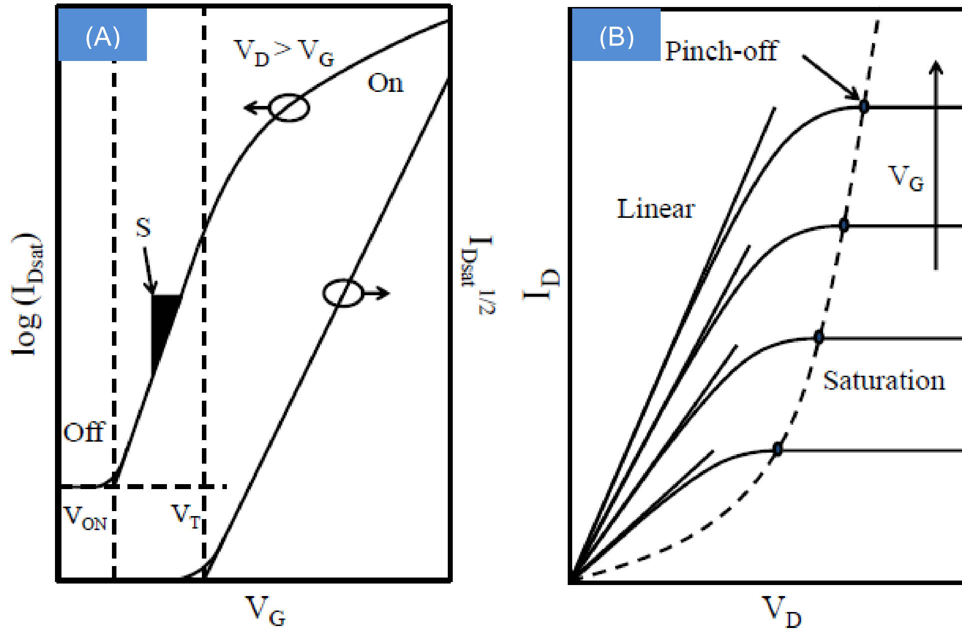

Figure 6: Ideal TFT measurement data showing (A) transfer characteristic for device in saturation and the output characteristics (B). The device is working in the linear and saturation regimes. The intercept of the dashed line represents the channel current reaching pinch off. Image reproduced from [39].

2.1.5 OFET Parameter Extraction

The most frequently cited figure of merit for semiconductors is mobility (μ, expressed in cm^2/Vs), determines a transistor's ability to drive an external load and operate at higher frequencies [41]. To extract the mobility and other useful quantities from an OFET the *gradual channel approximation* is used. A derivation is produced below.

The density of accumulated charges at the semiconductor/dielectric interface can be described using the relationship $Q = C\ \ V$. By considering this, along with equation

1, the relationship between the charge density at a distance *x* from the source electrode can be expressed as:

$$Q(x) = C_i[V_G - V_T - V(x)] \tag{2}$$

where *V(x)* is the channel bias and *Q(x)* is the charge density both at position *x*. When I_D is given by the product of the charge density (*Q*), channel width (*W*), charge carrier mobility (μ) and the electric field strength (*F*):

$$I_{D(x)} = W\mu Q_{(X)} F_{(X)} \tag{3}$$

Substituting equation 2 and 3 and assuming the field strength at *x* is given by $F_{(x)} = \frac{\mathrm{d}V_{(x)}}{d_x}$ we obtain:

$$I_{D(x)} = W\mu C_i[V_G - V_T - V_{(x)}]\frac{dV_{(x)}}{d_x} \tag{4}$$

By integrating along the channel length *L*, using the boundary conditions $V_{(0)} = 0$, $V_{(L)} = V_D$ we can solve equation 4 for $I_{D(X)}$:

$$\int_0^L I_D dx = W\mu \int_0^{V_D} C_i[V_G - V_T - V_{(x)}]dV_{(x)} \tag{5}$$

We obtain:

$$I_D = \frac{W\mu C_i}{L}\left[V_G - V_T V_D - \frac{V_D^2}{2}\right] \tag{6}$$

This is the general form of the equation describing the drain current in an OFET as a function of the applied gate and drain voltages. It is from this equation that most relevant parameters are extracted. Assuming the device is operating in the linear regime where I_D is proportional to V_D, such that charges are evenly distributed across the channel, we can simplify the above equation in the linear regime to yield.

$$I_{Dlin} = \frac{W}{L}\mu_{lin} C_i (V_G - V_T)V_D \tag{7}$$

In the saturation regime increasing V_D beyond $V_G - V_T$ has little effect on the measured drain current hence the drain current is approximately equal to that obtained when $V_D = V_G - V_T$. By again substituting into equation 6 we can gain an approximation for I_D in the saturated regime:

$$I_{Dsat} = \frac{W}{2L}\mu_{sat}C_i(V_G - V_T)^2 \tag{8}$$

To determine the mobility in the linear regime, we can take the first derivative of the drain current with respect to the gate voltage of equation 7, such that the mobility can be expressed as:

$$\mu_{lin} = \frac{L}{WC_iV_D}\frac{d^2I_D}{V_G^2} \tag{9}$$

The saturation regime can either be evaluated from the second derivative of I_D with respect to V_G, or the square-root of the first derivative:

$$\mu_{lin} = \frac{L}{WC_i}\frac{d^2I_D}{V_G^2} \tag{10}$$

$$\mu_{lin} = \frac{L}{WC_i}\left(\frac{d^2\sqrt{I_D}}{V_G^2}\right)^2 \tag{11}$$

2.2 Fabrication techniques

Research into the next generation of fabricating techniques is central to the evolution of nano-scale electronics. As a result of smaller, faster circuitry electronics has advanced to a point where technology has become increasingly integrated and accessible with the advent of smartphones and wearable devices [43]. In a typical electronic chip billions of discrete structures are patterned and then connected to other components. The development of new fabrication techniques is therefore critical to improving performance and driving down cost.

Figure 7 shows the evolution of one of the most common types of electrical component, the transistor, from its conception in 1954 through to its modern day equivalent in 2011, as an example of how far fabrication technologies have evolved.

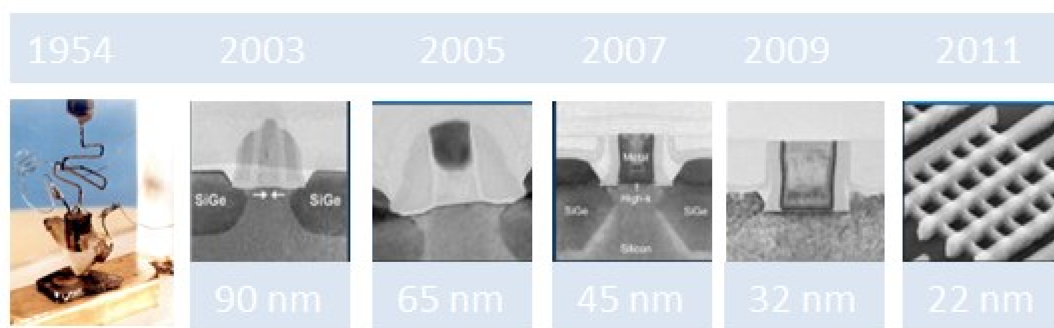

Figure 7: Photographs of various types of transistor architecture as they have evolved since 1954. Left to right: The first transistor made in Bell Labs in 1954 used simple parts. This is in stark contrast to more modern designs which have shrunk dramatically in size over the past 20 years. Between 2003 and 2011 the gate size of a transistor has been reduced from 90 nm to just 22, allowing more transistors per unit area thereby increasing performance and reducing power usage. Image reproduced from [44].

The ability to pattern materials at submicron and nanometre length scales is crucial in many areas of nanotechnology. A number of top-down patterning methods

have been developed to meet this challenge. They can be broadly grouped into four main categories: photolithography [45], direct-write methods [46], stamping techniques [47] and methods based on a scanning probe [48]. In established photolithography techniques, optical masks are used to transfer patterns to a photoresist using light. The smallest feature which can be patterned is limited by diffraction at best a quarter of the wavelength of the light used [49]. The demand for smaller feature sizes has prompted the use of shorter wavelength sources such as deep ultraviolet (around 200 nm), extreme ultraviolet (10–13 nm) [50], and X-rays (around 1 nm) [51]. Semiconductor companies are also turning to liquid immersion, optical interference and other techniques to extend resolution into the 20–50 nm range [52]. However these new variations of photolithography suffered from significant yield problems, leading to increased costs[53]. Direct-write methods such as electron-beam and ion-beam lithography [54] use focused beams of particles to achieve higher resolution compared to photolithography. These methods avoid the use of masks and light sources, but have lower throughput. Nano-scale stamping techniques have perhaps generated the most interest out of all the aforementioned techniques due to their simplicity and low cost. Generally a pre-patterned stamp is used to deposit or remove a thin film onto a surface using chemical [55] or physical [56] forces. Probe-based nano-patterning methods rely on the local interactions between a tip and the surface of a film to alter the surface by mechanical, chemical, thermal or fluidic means as the tip is scanned over the surface. The below sections detail some of the more prominent nano-patterning methods.

2.2.1 Photolithography

Photolithography is now the primary method used to fabricate electrical-circuitry. Photolithography comes in various forms, but in general ultra-violet light (UV light) is exposed through a photomask mask upon the surface of a light-sensitive material (called a photoresist), selectively blocking parts of the UV light from interacting with the photoresist [57]. Photoresists undergo an induced chemical change when exposed to specific wavelengths of light. When the photoresist is exposed to UV light it either cross-links (negative photoresist) or degrades (positive photoresist) such that these parts of the resist become insoluble or soluble respectively (**Figure 8**) [58]. By either rinsing the photoresist in a developer solution or placing it in an etching machine, the insoluble parts of the resist are removed, leaving a pattern on selected areas of the resist [59]. To further harden the resist or remove any residue of the developer, the wafer frequently undergoes a post-bake process. During this process, the resist temperature can be controlled to cause a plastic flow of the resist which can be desirable for tailoring sidewall angles [57].

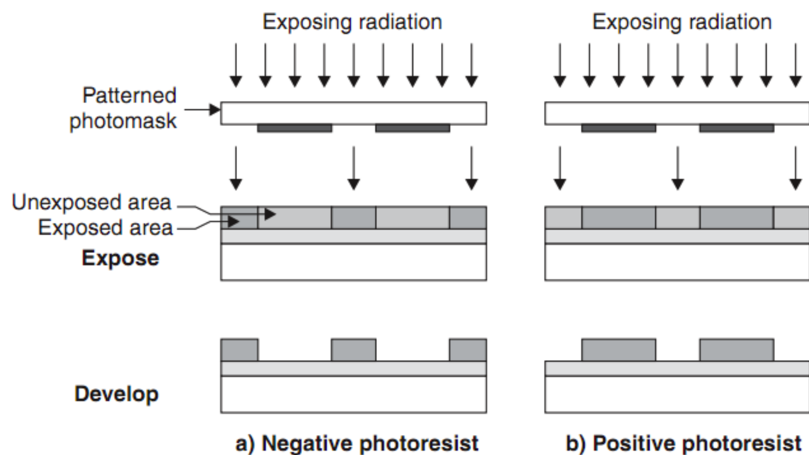

Figure 8: Schematic of negative and positive tone photoresists under development. The negative tone resists crosslinks when it is exposed to light becoming insoluble, while the positive tone resist is degraded when exposed such that the opposite pattern of the photomask is formed in the resist. Image reproduced from [59].

The major advantage of photolithography is its ability to produce exact copies from a master at a high speed, while also allowing fast switching of shadow masks when a new layout is required. There are also disadvantages to photolithography such as the difficulty of projecting a clear image of the mask onto the photoresist without edge distortion [60]. This is a critical factor and can be affected by the quality of the resist, type of optics used, strength of the light source and most importantly the wavelength of the light and the ability of the focusing optics to illuminate the mask effectively [61]. The type of photolithography system used plays a large part in determining the quality of the features and the smallest dimension which can be patterned. There are three major types of photolithography contact, proximity and projection (**Figure 9)**.

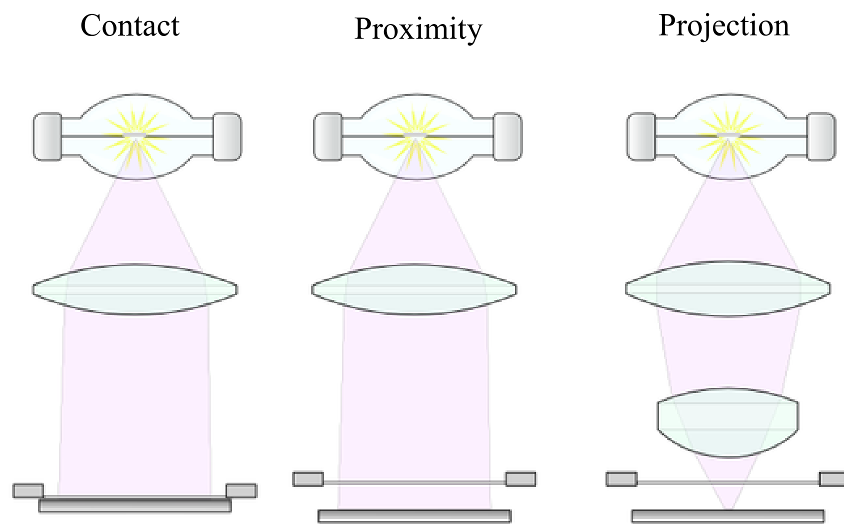

Figure 9: Schematic of three types of photolithography: Contact and proximity based lithography systems are the simplest forms of photolithography as they do not use multiple optical lenses and therefore replicate a 1:1 pattern from the photomask. A contact based system will place the substrate in direct contact with the photomask while in a proximity based system there is a small gap between the two, reducing wear on the mask. Projection based lithography uses multiple lenses to reduce the size of the feature being imprinted, the reduction system can use several different layers and requires precise control and alignment to achieve accurate results. This is the system commonly used for smaller dimensions. Image reproduced from [61].

Typically contact and proximity lithography operate at either 365 or 414 nm and does not use reduction lenses [62]. Projection-based lithography incorporates various types of reduction optics to focus the mask on the resist, allowing smaller dimensions to

be fabricated. Current state-of-the-art projection photolithography uses deep ultraviolet (DUV) light from excimer lasers with wavelengths of 248 and 193 nm, allowing minimum feature sizes down to 14 nm [63]. Further downscaling of photolithography is expected to bring significant challenges due to optical diffraction limitations and the difficulties of producing high power light sources below 10 nm.

2.2.2 Electron beam lithography

In addition to photolithography, direct write fabrication methods exist such as scanning electron beam lithography (EBL) [64, 65]. Direct write methods are slower than the parallel approach of photolithography as only one area of a substrate can be patterned at a given time. However the achievable resolution is typically greater than photolithography as the spot size of the beam is the dominant factor limiting the feature size. Reports exist of EBL being used to pattern features as small as 5 nm for example [66]. During EBL a pattern is carved out over a resist material line-by-line, using a high-energy beam of electrons. In the process the resist is either depolymerised or polymerised, allowing it to be used as a template for later etching steps. The resolution of electron beam lithography is limited by high-energy secondary electrons which are scattered from the primary beam, causing them to penetrate the resist [64]. Increased accelerating voltages produce fewer secondary electrons in the resist, but edge roughness limits the reproducible patterning of resists to features around 10 nm in most cases. Unlike photolithography a photomask is not required. However the method is relatively quick and cheap for producing one off designs once the initial equipment has been purchased [67].

2.2.3 Printing

Printing is an emerging direct-write fabrication method, which involves a fluid being controllably deposited upon a substrate in a similar fashion to a typical desktop printer. Electrically conductive or semiconducting 'ink' is used in place of vacuum deposited metals and semiconductors. Recently much attention has been paid to using larger scale printing apparatus such as gravure printing systems [68] which are more commonly used to print newspapers. Inkjet printing can be reasonably accurate over a macro scale (±10 µm), but it is also slow (compared to contact printing methods) as the print head is required to move continuously across the substrate. Features as small as 500 nm have been printed using self-aligned inkjet printing methods [69], but the majority of published research related to feature sizes greater than 10 µm [70]. The feature size achievable using gravure printing are typically no smaller than 100 µm, but it is far quicker than inkjet printing as a roller imprints a pattern as a substrate is passed over it at several meters/min [71]. As such a trade-off exists between the two methods in terms of speed and resolution of the printing method.

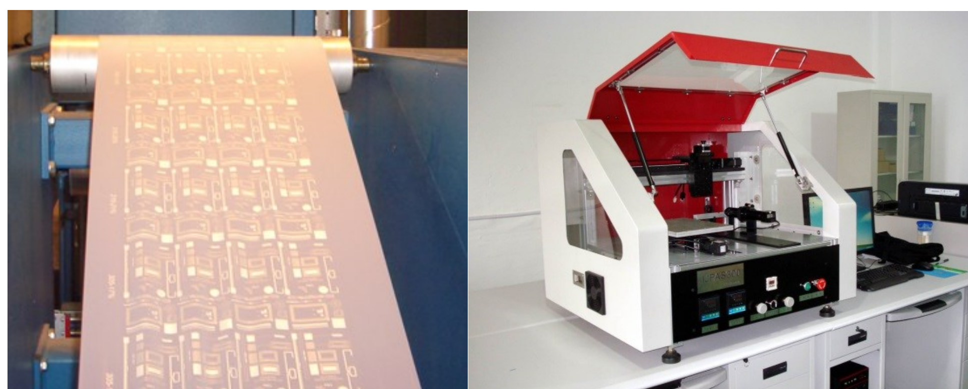

Figure 10: (A) Photograph of a gravure printing press, image reproduced from [68]. (B) An ink-jet printer which is specifically used for printing organic electronics, image reproduced from [72].

2.2.4 Nanotransfer printing

Nanotransfer printing (nTP) has been used to print both micro and nano-scale features as small as 10 nm [73]. In the nTP process, varying levels of surface adhesion are used to transfer a pattern to a substrate. nTP can be carried out in ambient conditions and allows direct printing of features over several layers in large areas. Typically metal layers are printed and the technique has been demonstrated on both rigid and flexible substrates [74], however rigid masks are required for smaller features as they deform less.

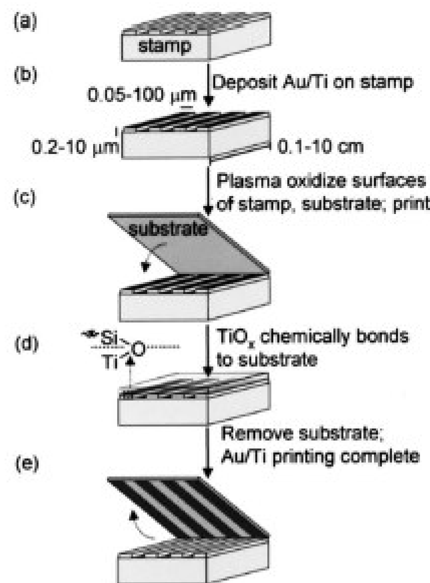

Figure 11: Schematic of the nTP process. (a and b) A PDMS stamp is coated with a metal film via thermal evaporation. (c) The stamp is placed upon a cleaned silicone substrate which has been chemically activated with reactive –OH groups. (d) The –OH groups react with the metal forming a chemical bond such that the two surfaces become adhered (e) The PDMS stamp is removed from the substrate resulting in the Au on the raised sections of the stamp to become detached as the Au is chemically bonded to the substrate in (d). Image reproduced from [55].

The nTP process can be seen in **Figure 11**. Initially a thin film of metal (in this case Ti) is deposited on the raised and recessed regions of a stamp by vacuum

deposition (**A**). The surface of the stamp is now covered with Ti and is exposed with an oxygen plasma to create reactive –OH groups (**B**). The stamp is then carefully placed upon the substrate to which the pattern is to be transferred. When the stamp is in contact with the substrate a condensation reactions occur between the Ti and the silicone substrate. This results in permanent covalent bonds of Ti–O–Si that produce strong adhesion between the two surfaces (**C**/**D**). Removing the stamp from the substrate transfers the metal film from the raised regions of the stamp to the substrate. While micron-scale features can be patterned by hand, finer nano scale features need the stamp to be placed and removed using a jig to ensure stability of the stamping process [75]. The resolution of the printed patterns is limited only by the resolution of the stamp itself, and the edge resolution is limited by the grain size of the evaporated metals. Additionally for repeat use of the stamp, it is necessary to remove any regions which have not transferred fully [76]. This process can damage the structure of some stamp materials meaning each stamp has a limited life span [77]. nTP is limited to systems in which covalent interactions assist the transfer of the solid materials from the surfaces of the stamps to the substrates. Many different systems have been successfully printed using nTP, including self-assembled monolayers, metals, polymers and biological compounds. Examples of printed patterned formed using nTP are shown in **Figure 12**.

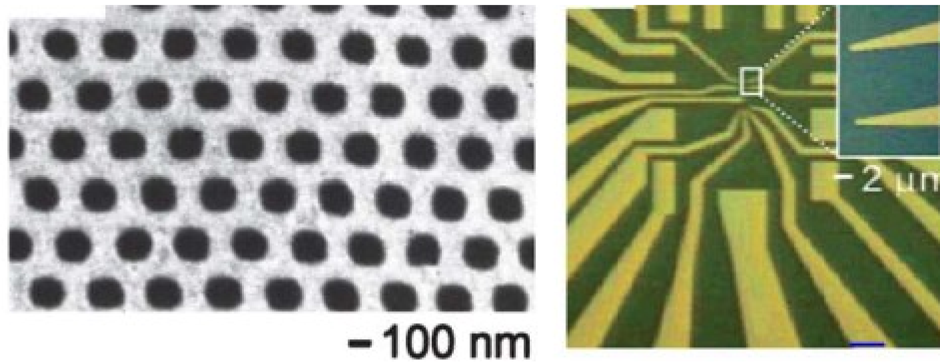

Figure 12: SEM images of Au/Ti patterns generated by nTP printing. (a) 500 nm Au/Ti lines and spaces were printed with a GaAs stamp onto a PDMS/PET substrate. (b) Au on a thiol-terminated SAM modified silicon wafer. Image reproduced from [78].

2.2.5 Metal transfer printing

Metal transfer printing (MTP) has been widely used to apply metal top contact electrodes to electrical devices, including OFETs [79]. MTP can be both additive and subtractive. MTP is similar to nTP, however it differs as a thermally induced adhesion change is used to imprint a pattern onto a substrate rather than the condensation reactions seen in uTP. A schematic of the MTP process is shown in **Figure 13**. Initially a polymer film is coated upon a substrate. The substrate is then heated below its melting temperature (T_m) but above its glass transition temperature (T_g), inducing the formation of a semi-crystalline polymer. At this stage the polymer is soft and "tacky" with strong adhesion. A patterned PDMS film is then coated with a thin metal layer before being placed upon the polymer surface. After applying pressure (to induce adhesion), the metal on the raised portions of the stamp is transferred. When heated above T_g, the adhesion ability of the polymer film surfaces increase, and a permanent contact is formed between the metal layer and the polymer.

MTP uses mechanical interlocking of the metal film and the polymer and as such a wide a wider variety of metal/polymer combinations can be used for printing

than is the case for the chemical adhesion process of uTP [80]. However the resolution limit of MTP is far lower at around 1 μm. This is because the metal layer is applied to a soft tacky film, which will undergo some degree of deformation when applying the PDMS stamp [81]. MTP does not require significant plastic deformation of the metal films to achieve transfer. As such MTP requires very little force to be exerted on the polymer during transfer [82].

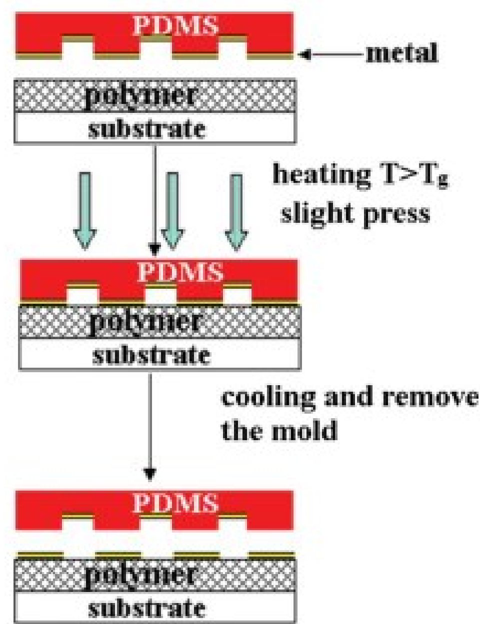

Figure 13: Schematic of the MPT process. (a) A patterned PDMS stamp with a metal thin film thermally evaporated on its surface is placed in contact with a substrate with a polymer film coated on top. (b) A small amount of pressure is applied to the stamp to ensure good contact and thermal transfer. The substrate and stamp are then heated past the T_g of the polymer such that the metal on the raised sections of the stamp become adhered to the polymer film. (c) When the stamp is removed, the metal film on the raised sections of the stamp is left adhered to the substrate, forming the desired pattern on top of the polymer film. Image reproduced from [79].

Recently MTP has been integrated into large-area “roll-to-roll” manufacturing equipment, with good reproducibility and speed reported [83]. The MTP process may be more suited to large-area manufacturing than uTP as it does not rely on chemical interactions to transfer material (which has typically resulted in poor yields). As shown

in **Figure 14 C** MTP can also be used to fabricate multilayer structures which are necessary for applications in microelectronics.

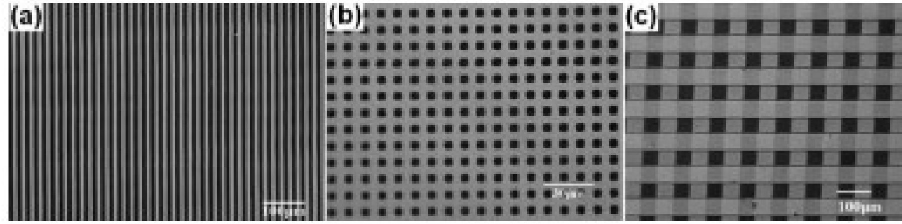

Figure 14: (a and b) Single layer MPT film patterned in Au (c) multilayer film showing a two layer Au structure fabricated on a PS/Si substrate. Image reproduced from [79].

2.2.6 Cold welding

Cold welding is mainly used to pattern electrodes for top-contact OFETs by forming metallic bonds between clean (unoxidized) metal surfaces with a mutual solubility surface. The bonds form when the metals are brought into contact, normally with an applied pressure [84] (**Figure 15**).

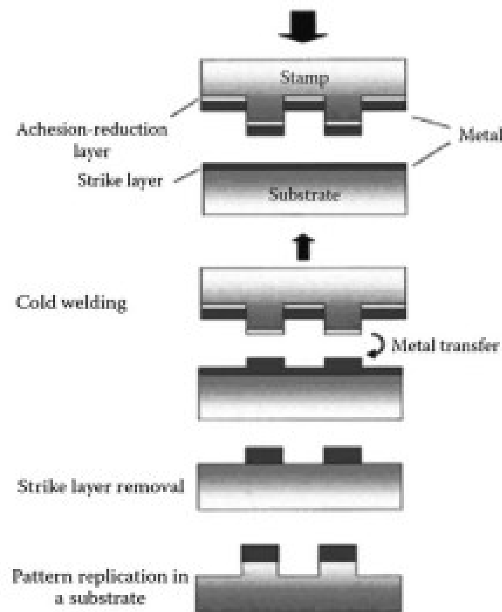

Figure 15: Schematic of the cold welding process. (a) A rigid stamp is fabricated with a metal thin film deposited on top of an "adhesion reduction layer". A substrate is similarly coated with a "strike layer" and a metal thin film. (b) The stamp is placed in contact with the substrate with high pressure (>150 MPa) such that the metal deposited on the raised regions of the "adhesion reduction layer" bonds with the metal on the substrate. (c) On the removal of the stamp, the desired pattern is transferred. The "strike layer" is now removed, typically by etching, and the final patterned film is now in place. Image reproduced from [85].

The specific process of forming a patterned film using cold welding involves fabricating a rigid master stamp which is then coated with an "adhesion reduction layer" upon which a metal is deposited. The substrate is then coated with a sacrificial layer ("strike layer") onto which Au is deposited. When the rigid stamp is pressed into contact with the substrate using high pressure (>150 MPa), the Au film in the raised regions of the stamp are transferred onto the substrate such that the two metals are forced together and metallic bonding occurs between them [86]. The "strike layer" is then etched away, leaving the pattern imprinted on the substrate. Although the use of PDMS stamps in place of rigid moulds has been reported [87] the majority of reports of cold welding have used rigid stamps as the stamps are more durable and last longer. However, more flexible stamps allow for a reduced pressure on the substrate, allowing a wider variety of materials to be patterned. Feature sizes vary from hundreds of nano-meters to millimetres depending on the pressure being applied to the stamp.

2.2.7 Hot lift-off

Hot lift-off is a subtractive technique mainly used to pattern organic materials [88]. The process uses a heated-patterned epoxy stamp to selectively remove material when placed into contact with a substrate. High pressure is first applied to the stamp to ensure the organic film adequately delaminates from the substrate; the pressure is then reduced before heat is applied to the stamp with the aim to further cure the epoxy and associated organic material on the substrate. If heating of the stamp does not occur the organic material will not detach from the substrate as the adhesion between the stamp and organic film too weak [89]. Separation of the stamp from the substrate results in the removal of unwanted regions of the organic film, leaving a pattern imprinted on the substrate (**Figure 16**). Hot lift-off works assuming the organic film fractures along the edges of the stamp. This can be problematic when large grains have formed in the

organic film as the grains need to be fractured before delamination can occur. Additionally the thermal bond formed between the stamp and organic film during heating must be greater than the bond between the substrate and organic film for successful patterning.

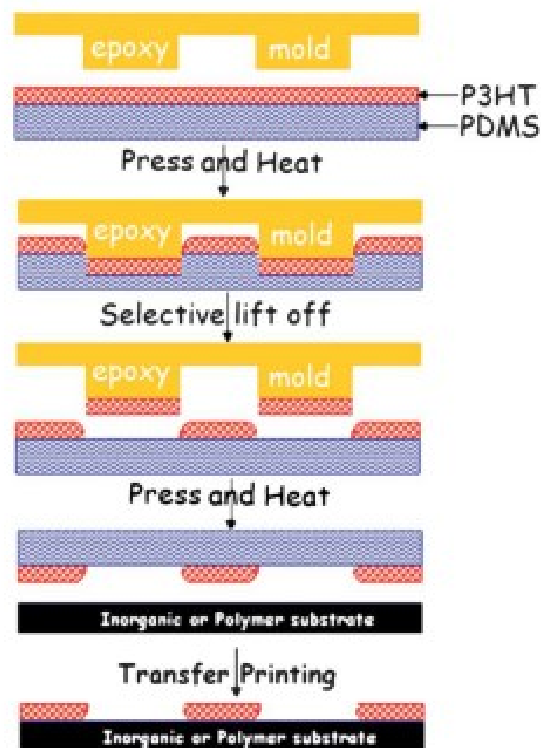

Figure 16: Schematic of the hot lift-off process. (a) an epoxy stamp is patterned with the desired features and placed on top of a polymer film which is typically deposited onto a PDMS substrate. (b) On application of heat and pressure to the epoxy stamp, raised portions of the stamp become attached to the mould (c). When removed the PDMS stamp is now imprinted with the desired pattern and can be transferred in a similar process to MTP onto a substrate using heat and pressure. Image reproduced from [90].

2.2.8 Controlled cracking

It has recently been found that nano-scale gaps can be formed using a process referred to as controlled cracking [91]. By defining “micro-notches” in an inorganic film, cracking is initiated in a highly controllable manner such that control over the

uniformity and shape of the cracks can be accomplished. The crack occurs on the thin inorganic film during deposition as a result of stress arising between different layers of inorganic material deposited under highly optimised conditions. The geometric characteristics of the cracks are influenced by the adjacent stress field, which is determined by the value of the film stress at the time of cracking. To achieve successful cracking a "micro-notch" designed with an optimal tip angle is required to reduce stress during deposition. It was reported that the characteristics of the notch determines when the crack starts to form during deposition. Crack formation can also be controlled through processing conditions and system parameters, and by ensuring an optimum lattice mismatch within different layers of the film [91].

Unlike stamping methods, which are typically limited to small areas, controlled cracking can be undertaken using tools more typically used in semiconductor fabrication and as such may represent a simple approach for high-resolution, arbitrary nano-patterning. However no electrical devices have yet been demonstrated with this technique and the cracking method proposed has not been demonstrated to be able to fabricate more complex multi-layered features, which are typically required for fabricating integrated electrical components.

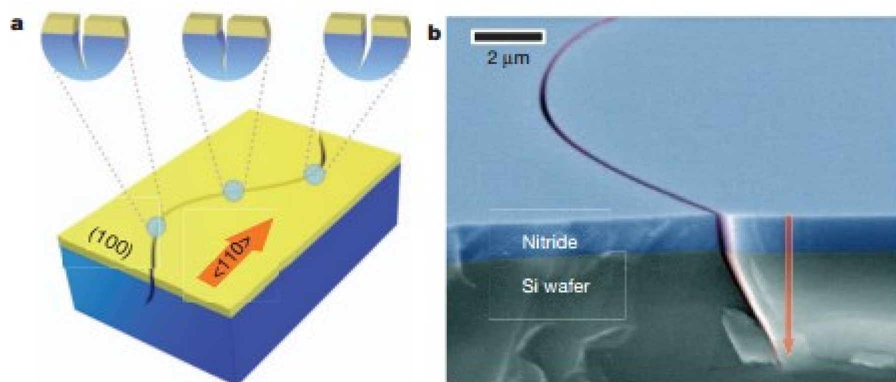

Figure 17: (a) Schematic and (b) SEM of the controlled cracking process. Image reproduced from [91].

2.2.9 Chemical lithography

Chemical lithography is a subtractive patterning method which uses a combination of contact printing and self-assembled monolayers (SAMs) to lift off a chemical resist through bonding of the SAM and a metal film [92]. In the chemical lithography process, a PDMS stamp is first activated using oxygen plasma treatment. This yields a strongly hydrophilic and reactive surface. A metal thin film is then deposited onto a substrate and chemically modified using a SAM. The SAM is selected to ensure its head group will undergo bonding with the activated –OH surface of the PDMS stamp.

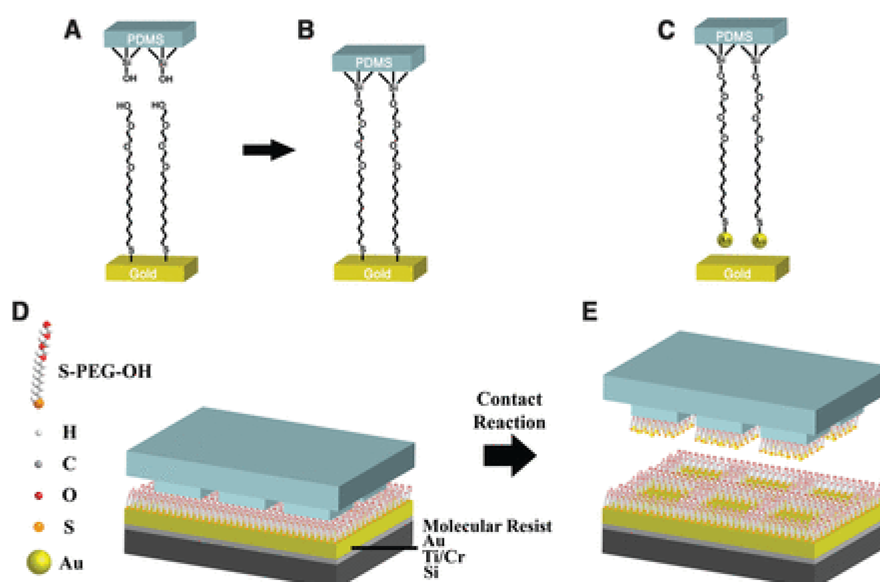

Figure 18: Schematic of the chemical lithography process. (a and b) A Au substrate coated with a SAM is brought into contact with a –OH activated PDMS stamp. (c) The SAM bonds with the –OH group on the PDMS stamp such that the two become attached. When the stamp and substrate are separated the SAM is removed from the Au film along with the Au which they are attached to suggesting the Au-Au bond is ruptured rather than the Au-SAM bond. (d and e) When used with a patterned PDMS stamp the SAM on the Au can be selectively patterned against the raised areas of the PDMS stamp. The SAM can then be used as an etching mask resulting in a patterned Au film. Image reproduced from [92].

The stamp and SAM-modified substrate are brought into conformal contact, and bonding between the raised patterned sections of the PDMS stamp and SAM coated Au

surface then occurs. When the stamp is peeled away from the substrate, the SAM is selectively removed the raised sections of the activated PDMS stamp. Hence the SAM is left patterned on the surface of the Au. The SAM is then used as a chemical etching mask such that nano-scale features can be defined in two relatively simple steps [92]. After the chemical lithographical process, a thin layer of Au is present on the surface of the PDMS stamp suggesting that the SAM-Au bond has not been ruptured but rather the Au-Au bond at the surface of the Au film has been broken instead. The time required for the contact-induced chemical reaction at the stamp-substrate interface has been determined to be as low as 1 minute, suggesting this technique could be used for the rapid fabrication of nano-scale features. Chemical lithography has been reported to enable fabrication some of the smallest features ever reporter for stamping techniques at between 30 and 40 nm. Hence with further refinement, the technique may be able to approach smaller dimensions which are typically achievable seen with more advanced photo-lithographical techniques [92].

2.2.10 Thermo-chemical AFM

Thermo-chemical lithography is a probe-based fabrication technique involving a heated wire on a scanning probe. When the probe is brought into contact with a substrate coated with a specific polymer, a chemical reaction occurs (due the heated probe) and localised patterning can take place in the area around the probe tip (**Figure 19**). Although the wire used for patterning is over 5 μm in diameter, the contact area between a hemispherical tip and a flat surface is much smaller than the radius of the tip as such only a small region of the surface is hot enough for the thermochemical reaction to proceed [93].

Thermochemical lithography is capable of patterning features as small as 28 nm on demand (i.e. without the use of any masks), using a wide range of materials [94]. The resolution is determined by the spatial extent of the tip–sample interaction and the thermal conductivity of the material being patterned [95]. The main factor affecting the success of patterning is the requirement to use thin films as the tip can only modify the surface of the film (this can result in incomplete conversion in the entire depth of the film) [96]. Due to small temperature fluctuations in the heated wire, line edge roughness also limits the ultimate resolution of thermochemical lithography. Although the technique is versatile, in common with other probe based techniques, its throughput is low and this method is unlikely to be able to compete with optical methods and stamping methods in this regard [97].

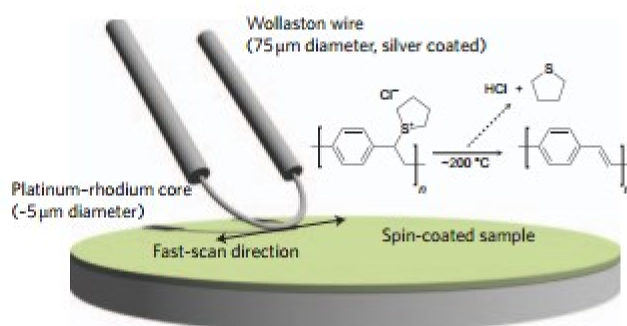

Figure 19: Schematic of the thermochemical AFM nano-patterning process. A resistively heated wire probe is mounted on an AFM. The probe is scanned in contact with a precursor polymer at a constant temperature inducing conversion of the precursor into a polymer thin film. In the above example conversion of the precursor polymer poly(p-xylene tetrahydrothiophenium chloride) (PXT) to fully conjugated polyphenylene vinylene (PPV) occurs optimally at 200°C. Image reproduced from [93].

2.3 Conclusion

The above discussion focused on recent developments in organic electronics and nano- and micro- scale manufacturing. Although organic electrical devices are not yet at a point where they can compete with their inorganic counterparts in terms of performance they are making fast progress. New manufacturing methods will be critical to developing commercially successfully product in particular those involving flexible devices on large area substrates.

While some of the fabrication methods discussed above are only suited for research use over small areas, variations of these methods have shown they can be integrated onto "roll-to-roll" printing equipment [98] (**Figure 20**). Development of all the fabrication methods discussed above into high speed processes is critical if they are to meet to the requirements of speed and reproducibility needed for industrial scale use.

Figure 20: A "roll-to-roll" printing press equipped with a PDMS roller to imprints a pattern at high speeds onto a substrate. Fabricated by Industrial Technology Research Institute, Korea.

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3 Experimental

This chapter outlines the experimental methods and techniques used for the work presented in this thesis, including the techniques used to characterise materials and fabricate devices.

3.1 Peel Testing

Peel testing was employed to investigate the adhesion between adjacent metal layers. Peel testing is commonly used to evaluate the adhesive strength of tape, adhesives and flexible substrates [1]. It has been successfully used to determine the adhesion of many materials such as rubber, biomaterials, dental materials, medical packaging and consumables, but it is most commonly used to test adhesive glues [2]. Typical tests involve peeling two bonded flexible adhered materials from each other, with one material being fixed to a moving stage. Peel tests are usually conducted at a constant rate of separation at various angles, with 90° being the most common. Parameters such as peak peel load and average peel strength can be used to characterise the peeling process. For all the measurements reported here, peel tests were carried out using the 90° peel test apparatus (**Figure 1**).

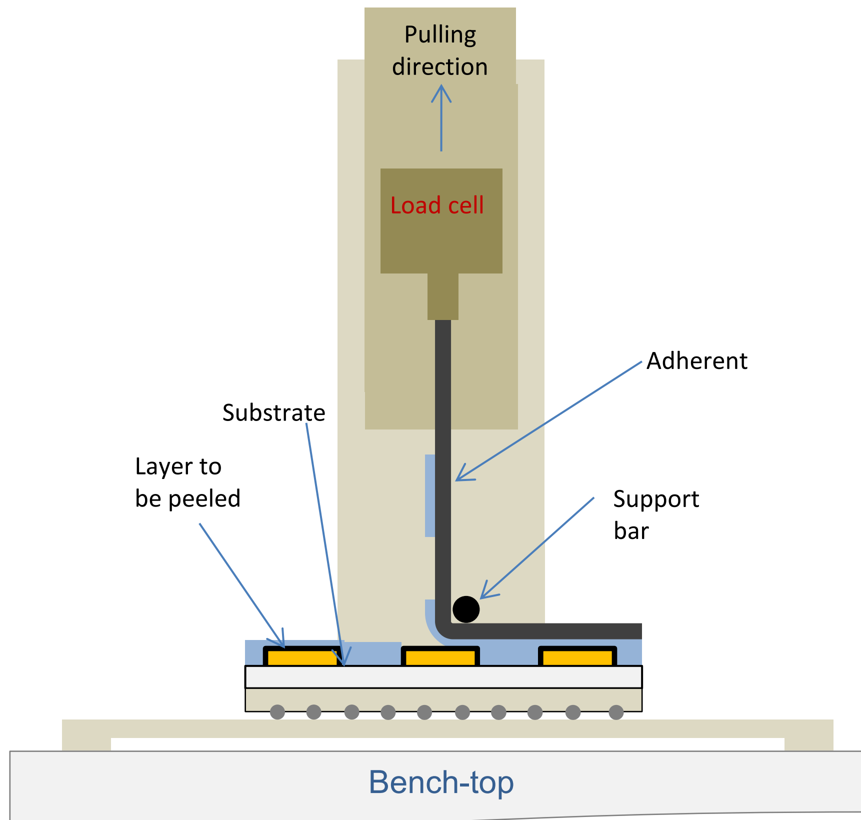


Figure 1: Schematic illustrating the geometry of a 90º peel test, using a ribbon of adhesive tape as a flexible adherent. The substrate is firmly attached to a light weight, low friction travelling stage that moves horizontally as the adhesive tape is pulled vertically from the substrate at a constant speed. The 90º geometry is maintained by means of a narrow horizontal bar oriented along the inner bend of the adhesive tape. The vertical force is recorded as a function of time using a strain gauge, and converted to a force versus displacement "peel-curve" on the basis of the constant velocity.

The substrate was firmly mounted on a light weight, low friction horizontal stage. Polyvinyl chloride backed (PVC) insulation tape (AT7 PVC Insulation Tape, Advanced Tapes) and adhesive glue (First Contact Red, Photonic Cleaning Technologies) were both measured to determine their peeling effect on various surfaces. When the PVC tape was tested a short strip (~0.5 cm) was firmly attached to the surface of the film being investigated. In the case of the adhesive glue, the as-received solution was applied to the surface of the material to be peeled using the provided applicator brush and allowed to dry. To allow the glue to be peeled effectively a strip of PVC tape

was applied to its surface, when the tape when then peeled back the adhesive glue was removed in one strip and stayed adhered to the PVC tape. To record the peeling force, the other end of the PVC tape was connected to a vertical stage via a digital force gauge (ELC-09S Tensile Load Cell, Xiamen Elane Electronics). The adhesive tape was pulled vertically from the substrate at a constant speed, with the 90º geometry being maintained by means of a narrow horizontal bar oriented along the inner bend of the adhesive tape. The vertical force was recorded as a function of time using the strain gauge, and converted to a force *versus* displacement "peel-curve" on the basis of the constant velocity.

3.2 Atomic and scanning electron microscopy

3.2.1 Atomic force microscopy

Atomic force microscopy (AFM) can be used to examine surface topography of samples on the sub-micron length scale. A cantilever is raster-scanned across the surface of the sample. The force between the tip of the cantilever and the sample gives rise to a deflection of the cantilever. This deflection is measured using a laser beam, which is reflected off the back of the cantilever. The height of the cantilever is then adjusted using a feedback mechanism to maintain a constant distance between the sample surface and the cantilever tip. The vertical height of the sample can then be plotted as a function of lateral position **Figure 2**.

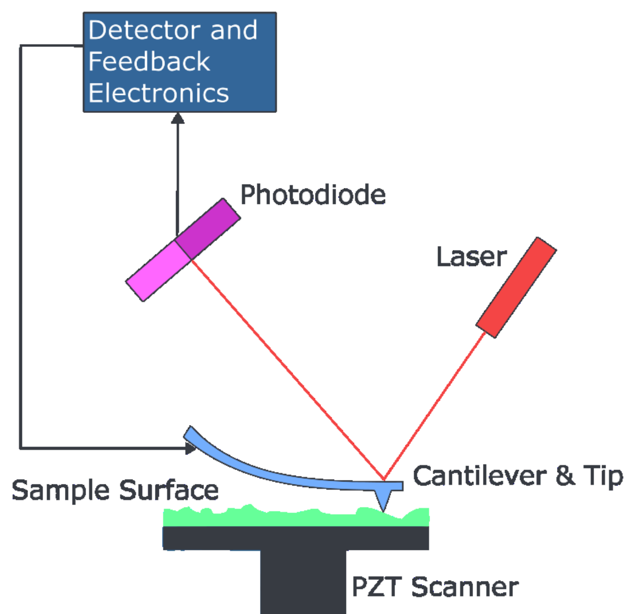


Figure 2: Schematic of the operating principles of an AFM. A sample is first placed upon a scanning stage which can move along three axes (X,Y,Z). A cantilever is moved into close contact with the surface of a sample such that it deflects from its equilibrium position. A laser diode, which has been aligned with the end of the cantilever, records this deflection with the aid of a photo detector. When the cantilever is moved across the surface (typically in “tapping mode”) a 3D image of the samples surface is recorded with nano-scale precision.

The most common form of AFM is tapping mode. In this mode the cantilever oscillates near to its resonant frequency. Tapping mode AFM reduces damage to the sample surface compared to other scan modes where the tip is held in constant contact with the surface. It also avoids problems with short-range forces causing the tip to stick to the sample surface. Throughout this work AFM was carried out in tapping mode using an Agilent 5500 atomic force microscope in ambient-pressure air. The approximate resonance frequency of the silicon cantilever was 150 kHz with a force constant was 5 N/m. AFM tips were purchased form Budget Sensors (model number Tap150-G).

AFM force spectroscopy was used to measure the adhesion forces of various surfaces to the tip of an AFM cantilever through the acquisition of a force curve, which depicts the deflection of the cantilever as a function of distance from the sample surface. If the spring constant of the cantilever is known and the sample is held at a fixed distance from the cantilever, the displacement of the cantilever can be directly related to surface forces (such as adhesion) acting at the tip-sample interface. The force curve is determined at a particular tip-sample interaction point on the sample. The force curve is related to the material property of the tip as well as its shape and as such the technique is instrument specific and does not directly measure the adhesion of the sample but rather the tip/sample interaction.

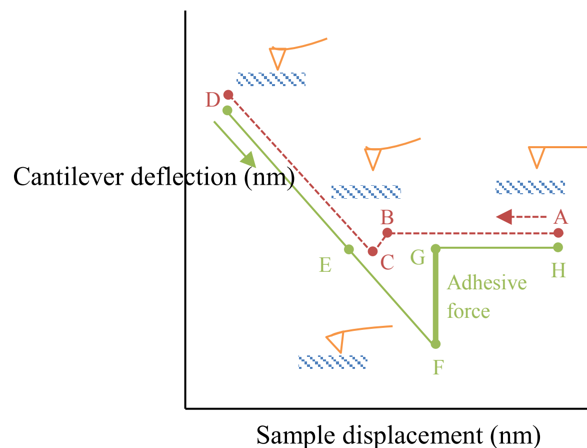


Figure 3: Schematic of the AFM force spectroscopy measurement. When the force gradient exceeds the stiffness of the cantilever jump-to-contact occurs (A → C). Between points C and D the tip comes into contact with the sample's surface. The AFM then attempts to withdraw the tip at point (D → F). The adhesion force can be determined by the recorded pulling force differential between F and G.

At the start of the adhesion measurement, a large distance separates the tip and sample and there is negligible interaction between them (**Figure 3**, **A**). The tip is moved towards the sample until it reaches a point close to the sample surface (**B**). As the

sample moves towards the tip, various attractive long- and short-range forces pull on the tip determined by the strength of the attraction between the tip and sample surface. Once the total force gradient acting on the tip exceeds the stiffness of the cantilever (typically a few nN), jump-to-contact occurs and the tip is in contact with the sample (**A** → **C**). At point **D**, the tip and sample are in contact and deflection is dominated by mutual electronic repulsions between the tip and sample (just a few pN). Between points (**E** → **F**) the tip is withdrawn. The time the tip and sample are in contact (**D** → **G**) can be controlled to increase their interaction time and the potential for chemical interaction. During withdrawal (**D**→ **H**) adhesion bonds formed during contact with the surface, cause the tip to adhere to the sample up to some distance beyond the initial contact point (**D**). Eventually the stiffness of the cantilever overcomes the adhesion forces causing it to pull off sharply, springing upwards to its noncontact position (**F** → **G**). Force curves were recorded using NanoSensors PointProbe Plus FM-AFM cantilevers in a nitrogen controlled chamber (<20ppm) to reduce the effects of relative humidity using a scan speed of 1 μ/s. The force constant of the silicon cantiliver was 0.2 N/m and the resident frequency was 25 kHz.

3.2.2 Scanning Electron Microscope

The observation and characterisation of organic and inorganic materials on a micro and nano scale can be achieved using a scanning electron microscope (SEM). The SEM uses a finely focused electron beam to analyse a selected area of a sample. The beam scans the surface in a raster pattern. Interaction of the beam and surface results in the production of signals, due to backscattered and secondary electrons striking a detector. These emissions along with x-rays and photons, which are also generated, allow the examination of the sample including surface topography,

crystallography and composition. Normally the signals of greatest interest are the secondary and backscattered electrons as any variation in these signals recorded by the SEM is the result of differences in surface topography. The SEM produces images of a three dimensional appearance due to the large depth of field of the beam and the shadowing effect of the secondary and backscattered electron [3].

The two major components of the SEM are the electron column and control console (**Figure 4**). The column is formed from an electron gun and various lenses which are used to alter and control the path of the electron beam as it travels down towards the evacuated sample chamber. The electron gun generates and accelerates electrons in the range of 0.1 to 30 keV. The spot size formed by SEMs can be less than 10 nm, and contains sufficient probe current to generate clear images. Specimens are loaded onto a stage directly under the electron beam. The stage is able to rotate 360° so multiple samples can be loaded and positioned under the beam without the need to release the vacuum. The stage is biased and samples are attached to a 'stub' using conductive silver paint. Typically samples are around 5 mm^2 but the area examined is far smaller at only a few microns square. The purpose of the vacuum is to remove contaminates from the chamber, oil, water and other carbon contaminates can interfere with the detection and path of electrons. [4]

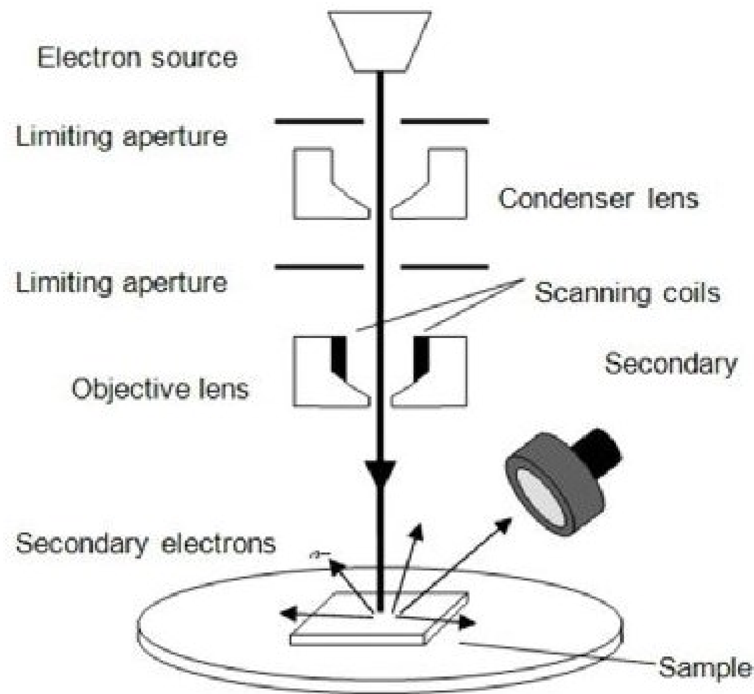


Figure 4: Schematic diagram of a SEM depicting the various lenses through which an electron beam flows before interacting with a sample. Reproduced from [5]

Topographic contrast arises due to the number and trajectories of backscattered electrons and the number of secondary electrons depending on the angle of the incidence beam and specimen. An Everhart – Thornley (E –T) detector can be used to collect both secondary and backscattered electrons, but dedicated backscattered detectors can also be used to improve detection rates [4, 6]. The E –T detector is located on one side of the specimen, limiting it to an anisotropic view and placed at a high angle relative to the beam (

Figure 5). If only a backscattered electron signal is detected, the image will comprise by bright regions of high signal and dark regions from low signal area, and the resulting image would have a harsh contrast. Although the entire surface is still excited, backscattered electrons which face the detectors are able to reflect their electrons towards the detector more effectively resulting in a higher contrast image being

recorded. The SEM used during this work as a Gemini 1525 FEGSEM using a working voltage of 5 keV.

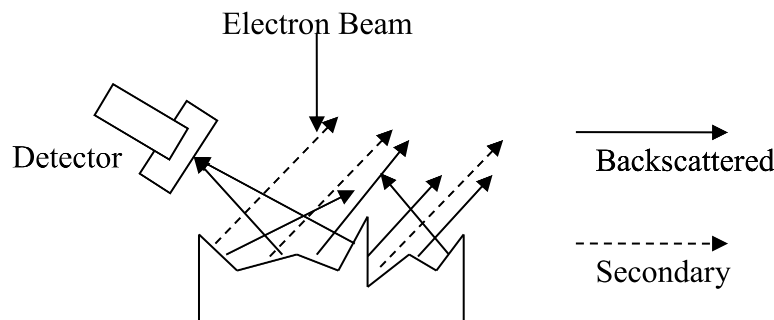


Figure 5: Schematic depicting the formation of both backscattered and secondary electrons after the interaction of the main electron beam has occurred with the samples surface.

A variant of SEM is cross-sectional SEM, in this operating mode a focused ion beam is used to mill into a samples surface cutting out a section in a desired pattern or shape. Once cut the cross section of the sample can be imaged which a high degree of accuracy allowing for inspection of different layers of the material. The major consideration when performing this operation is the damage which can occur to the sample during milling, removed material can easily accumulate on the sample resulting in damage and contamination of the sample. Cross-sectional SEM was performed using a Helios NanoLab 600 at a working voltage of 10 keV.

3.3 Contact angle measurements

When a water drop is placed onto a solid surface, its behaviour depends on the adhesive forces between the liquid and the surface. If the adhesive forces are attractive,

the liquid drop is pulled toward the surface and spreads along the surface. This type of surface is referred to as hydrophilic. If the adhesive forces are repellent, the liquid drop minimizes its contact with the surface and the surface is said to be hydrophobic. To determine if a surface is hydrophobic or hydrophilic, contact angle measurements can be undertaken by dispensing a static drop of fluid upon a sample and recording the contact angle with the surface. This can be used to determine if a SAM is present on a surface, or to investigate the wetting characteristics of different molecules.

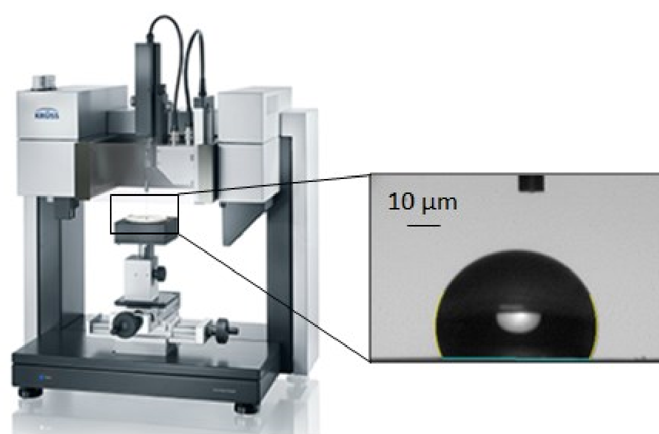


Figure 6: Photograph of a static contact angle measurement machine (Kruss DSA100) along with an enlarged photograph of a static drop being analysed.

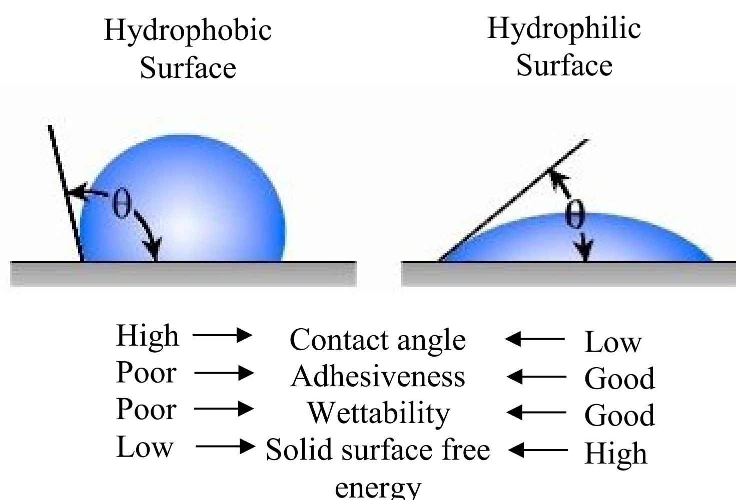


Figure 7: Schematic of a hydrophobic and hydrophilic surface along with properties associated with each type of surface including contact angle, adhesion, wettability and surface free energy.

Both cohesive and adhesive forces act on a liquid when it comes into contact with a surface and together determine the liquid's shape and form. Cohesive forces are intermolecular (i.e. hydrogen bonds and Van der Waals forces) and encourage molecules of the same type to stay together in tight formation, effectively causing the liquid to resist separation. Adhesion forces by contrast cause the attraction of unlike molecules to come together through mechanical forces (interlocking) or electrostatic forces. Adhesion will cause a liquid to "cling" to a surface and effectively separate over the surface.

The contact angle is determined by the interaction between forces in the gas, liquid and solid phase. In general when the cohesive forces are weaker than adhesive forces (i.e. molecules of the liquid tend to interact more with solid molecules than liquid molecules) the contact angle is larger and the surface is hydrophilic. Similarly when the cohesive forces are stronger than the adhesive forces (i.e. molecules of the liquid tend to interact more with each other than with the solid molecules) the contact angle is smaller and surface is hydrophilic . The contact angle measuring machine used in this work was a Kruss DSA100 which was operated in a climate controlled clean room using a static drop volume of 10 µl.

3.4 Metal Deposition

Vacuum-deposition is commonly used for the deposition of metals and small organic materials. Vacuum-deposition was performed in a deposition system housed in a N_2 glovebox to reduce the risk of oxidation of organic materials and some metals. To perform vacuum-deposition, samples were first loaded into a metal substrate holder and

placed within the deposition chamber; the material to be deposited was loaded into a crucible directly under the sample at the bottom of the chamber. To deposit patterned firms a stencil was placed in front of the sample substrate. Prior to evaporation, the chamber was evacuated and the pressure was reduced to approximately 10^{-6} mbar. Once the sublimation temperature of the material had been reached, deposition of the material commences at the set deposition rate. In this work, a deposition rate of 1 Ås^{-1} was used for metals and 0.5 Ås^{-1} for organic materials; a lower rate was used for organic materials to allow for the formation of larger crystals during deposition.

The quality of films formed by shadow mask evaporation can be increased by using bi-layer masks, which reduce shadowing of the deposited electrode. However over time the masks become worn and as such the dimensional stability of shadow masking is not high. Further reduction of shadowing was achieved by designing mask holders which support the stencil reducing the tendency of the thin stencil to sag during development (**Figure 8**).

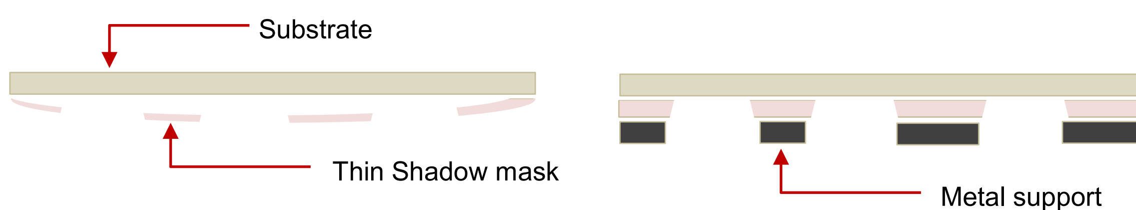


Figure 8: Schematic depicting the sagging effect which can be encountered when using shadow masking to define features through a thin metal stencil. In this case a second thicker metal support was added under the shadow mask to support it, thereby reducing the sagging effect.

The purity of evaporated organic materials is more important than the deposition of metals as organic materials forms an active semiconductor layer. As such highly pure 99.99% organic molecules were purchased used and the material purity was further

improved by pre-heating the organic materials at a temperature just below their sublimation temperature for 1-2 hours before deposition.

3.5 SAM deposition

Self-assembled monolayers (SAMs) are typically deposited by drop-casting, dip-coating or from the vapour phase, although other methods have been suggested such as deposition via spin casting [7-9]. The formation of a well-defined monolayer is challenging owing to the tendency of SAMs to attach to impurities and undergo localised changes in topography when attaching to surfaces [10]. When applying a SAM molecule, which only attached to an oxidised surface (such as octadecylphosphonic acid (ODPA) or phosphonododecyl-phosphonic acid (PHDA), a well-defined oxide layer must first be formed. For SAMs which attach to native metal surfaces like Au (such as octadecanethiol (ODT) or mercaptohexadecanoic acid (MHA)) the formation of an oxide layer is not required. Ensuring the film is clean is then the main criteria for successful SAM deposition. For the work presented in thesis, SAM deposition was accomplished by placing a substrate on a hotplate at 300°C and spraying it with deionised water for a period of 10 minutes to clean the upper surface and in the case of oxidising films induce the formation of a well-defined oxide layer. The substrates were then cleaned in an oxygen plasma (100 W, O_2 flow-rate: 3 mL/min) for ten minutes, and then immersed in a 5 mM solution of ODPA in isopropanol (IPA) for 48 hours. The films were then thermally annealed at 120 °C for one hour in N_2, before rinsing lightly in isopropyl alcohol to remove unbound/residual SAM molecules.

3.6 Sample fabrication

The following section presents fabrication methods used for this work in this thesis, including, thin film deposition, annealing conditions and SAM deposition. Further details, which are specific to individual experiments, are presented within the experimental chapters. The relevance of the structures described below is also fully discussed within the experimental chapters.

3.6.1 Adhesion lithography sample fabrication

Procedure A. For the fabrication of structures with a uniform layer of Al (M1) covered by a uniform layer of Au (M2), with or without a SAM, the following procedure was followed:

Thermally cross-linkable benzocyclobutene (BCB) polymer was deposited onto clean 2 cm × 2 cm glass substrates by spin-casting the as-received material (Cyclotene 3022 – 46, Dow Chemicals) at 2000 rpm for 30 s in nitrogen. The films were pre-annealed on a hot plate in a nitrogen atmosphere (<10 ppm O_2) at 170 °C for 60 min to partially cross-link the BCB.

To prepare structures without octadecylphosphonic acid (ODPA), the substrates were loaded into a high vacuum (10^{-6} mbar) thermal evaporator and 40 nm layers of Al were sequentially deposited at 1 $Ås^{-1}$. To prepare structures with ODPA, the substrates were removed from the thermal evaporator after deposition of the Al layer, cleaned in an oxygen plasma (100 W, O_2 flow-rate: 3 mL/min) for ten minutes, and then immersed in a 5 mM solution of ODPA in isopropanol for 48 hours. The films were then thermally

annealed at 120 °C for one hour in N_2, before rinsing lightly in isopropanol to remove unbound/residual SAM molecules. The substrates were then returned to the thermal evaporator for deposition of the Au layer (40 nm, 1 $Ås^{-1}$). Finally, all substrates were post-annealed for 4 hours at 200 °C in N_2 to complete the cross-linking of the BCB (**Figure 9**).

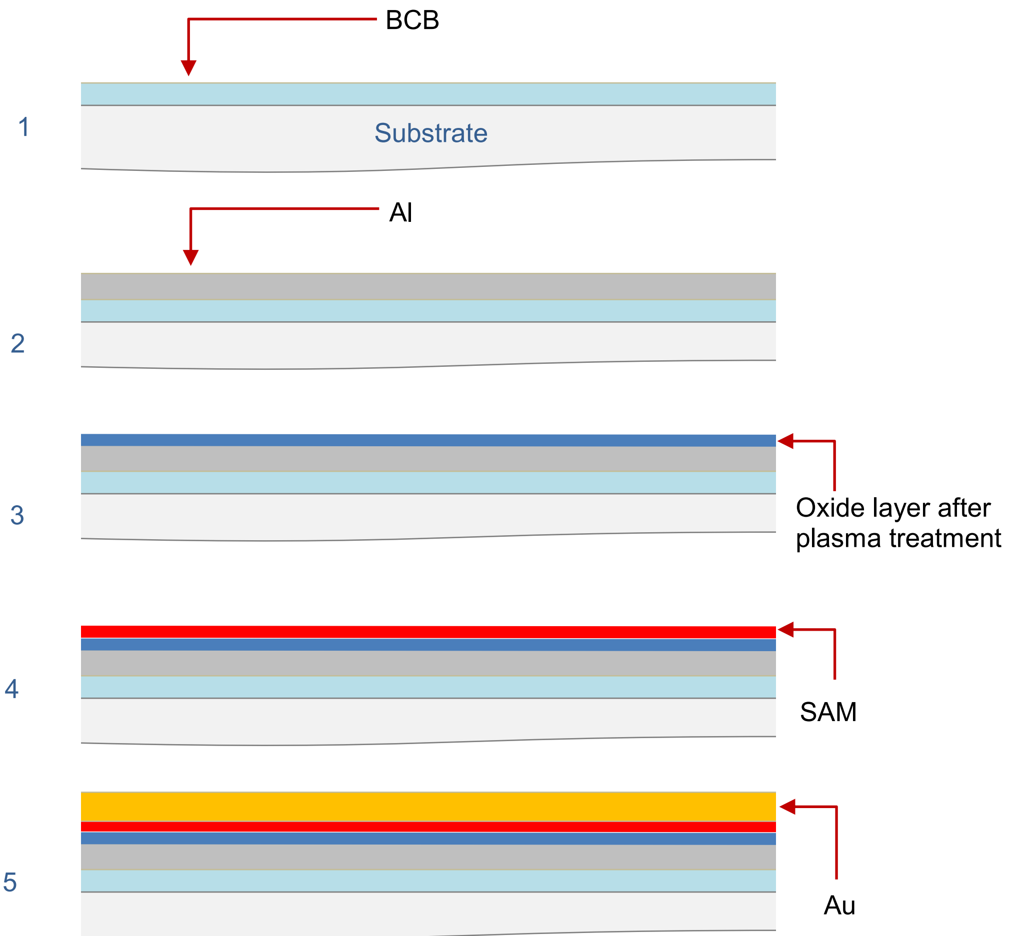


Figure 9: Schematic depicting the fabrication of structures where Al is used as M1. Initially partially cured BCB is deposited onto a glass slide via spin coating (1). Al is then thermally evaporated on top (2). An oxide layer is grown on the Al in a plasma chamber (3). A SAM (ODPA) is then deposited on the surface of the oxide by immersing the substrate in a solution of the molecules. Finally a layer of Au is evaporated on top of the SAM, forming a 5 layer structure.

Procedure B. For the fabrication of structures with a uniform layer of Au (M1) covered by a uniform layer of Al (M2), with or without a SAM, the following procedure was followed:

To prepare structures without octadecanethiol (ODT), clean 2 cm × 2 cm glass substrates were loaded into a high vacuum (10^{-6} mbar) thermal evaporator, and a thin (5-10 nm) layer of thermally evaporated Cr was deposited onto the glass at 1 Ås^{-1}. 40 nm layers of Au and Al were then sequentially deposited at 1 Ås^{-1}. To prepare structures with ODT, the substrates were removed from the thermal evaporator after deposition of the Au layer, cleaned in an oxygen plasma (100 W, O_2 flow-rate: 3 mL/min) for ten minutes, and then immersed in a 5 mM solution of ODT in IPA for 48 hours. The films were then rinsed lightly in isopropanol to remove unbound/residual SAM molecules, before returning the substrates to the thermal evaporator for deposition of the Al layer (40 nm, 1 Ås^{-1}) (**Figure 10**).

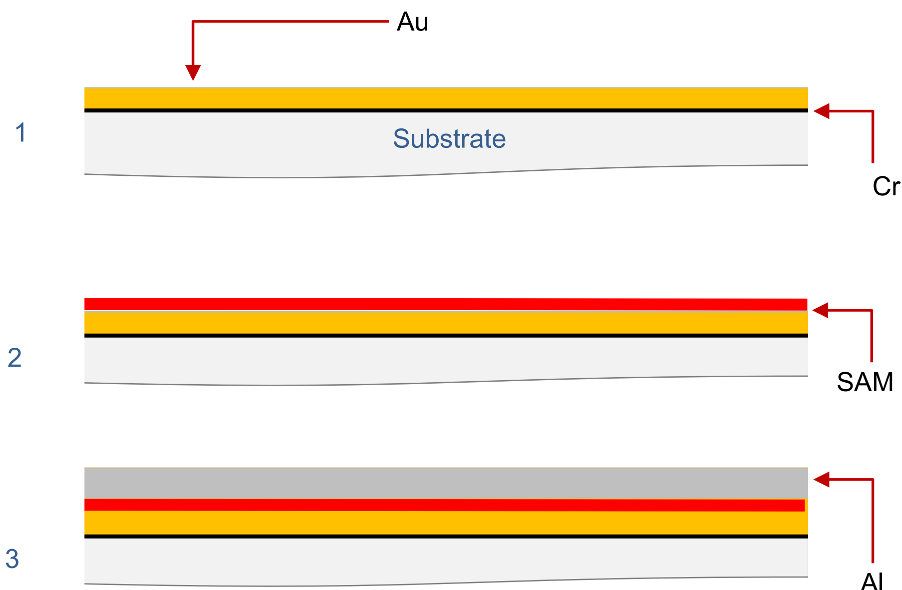


Figure 10: Schematic depicting the fabrication of structures where Au is used as M1. Initially a thin (< 5 nm) layer of Cr is deposited via thermally evaporation to aid adhesion of Au, which is subsequently deposited. A SAM (ODT) is then deposited on

the surface of the Au by immersing the substrate in a solution of the molecules for 24 hours. Finally a layer of Al is evaporated on top of the SAM forming a 3 layer structure.

Procedure C. For the fabrication of SAM-coated line arrays of M1 covered by a uniform layer of M2, the following procedure was used:

Fabrication was carried out using the same procedures described in A and B (with the SAM present, except the line array pattern was defined by evaporating M1 though a shadow mask (**Figure 11**). The spacing, widths and lengths of the line arrays were 4, 1.2 and 20 mm, respectively.

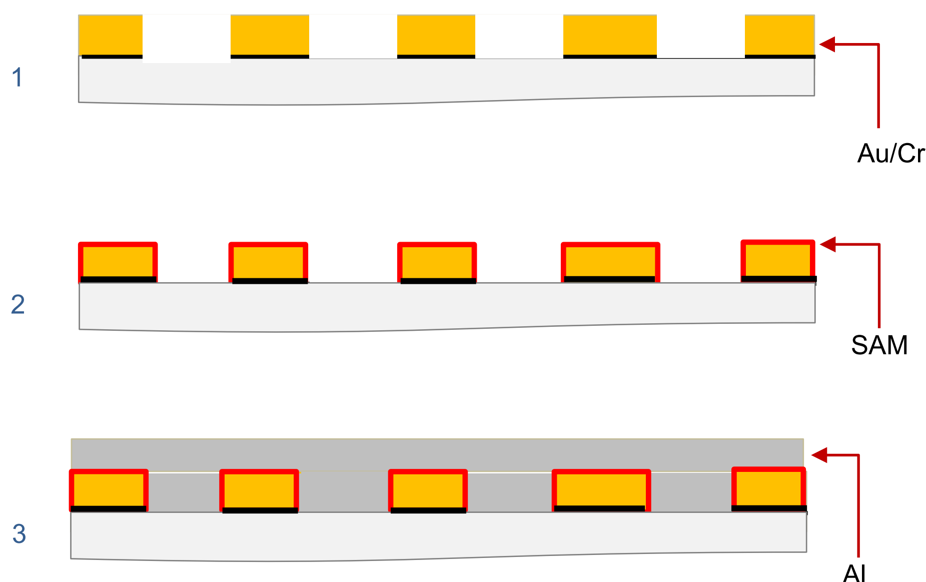


Figure 11: Schematic depicting the fabrication of structures used for peeling line patterns. Either Al or Au is first deposited using thermal evaporation through a shadow masking forming a line array (1) the SAM is deposited (2) and then a second dissimilar metal is deposited on top (3)

Procedure D. For the fabrication of concentric square electrodes with a central Au square, the following method was employed:

Fabrication was carried out using the same general procedure described in A (with ODPA present), except the Al layer (M1) was patterned photolithographically in a concentric "square-ring in square-ring" geometry (see Chapter 4 Figure 28) as follows: (1) AZ 1805 positive photoresist (AZ Electronic Materials) was deposited on top of the Al by spin-coating the as-received solution at 3000 rpm for 40 s; (2) the resist was soft baked at 100 °C for 60 s; (3) it was then selectively exposed at 365 nm for 6 s (10 mJ) via a chrome-plated quartz shadow mask, using a mask aligner (Karl Suss MA3); (4) the resist was post-exposure baked at 100 °C for 60 s; (5) the substrate was immersed in MA-319 developer (AZ electronic materials) for 90 s, rinsed and dried; (6) the resist was hard-baked at 120 °C for 60 s; (7) The Al was then etched by immersion in Al etchant (ANPE 80/5/5/10, Microchemicals GmbH) at 40 °C for ~30 s; (8) finally, the photoresist was removed by rinsing repeatedly in acetone and IPA.

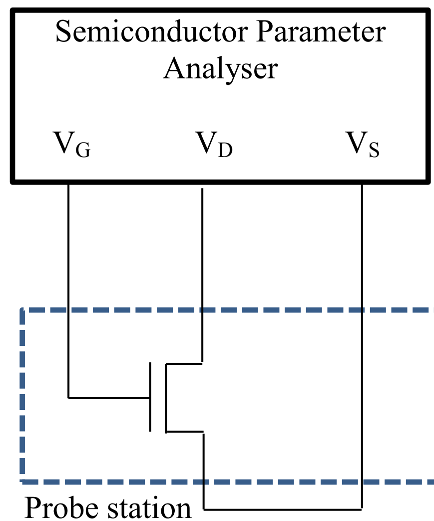
3.6.2 Self-aligned gate sample fabrication

SU8 was deposited onto clean 2 cm × 2 cm glass substrates by spin-casting the as-received material at between 500 and 3000 rpm for 30 s. The films were annealed on a hot plate at between 90 and 100 °C for up to 60 s resulting in the SU8 becoming partially cross-linked. The substrate when then transferred onto a mask aligned (Karl Suss MJB 3) and exposed for between 10 and 30 seconds. The substrate was then annealed on a hot plate at between 90 and 150 °C to induce photo-acid diffusion within the film. To remove undeveloped areas of the film, the SU8 was developed in 2-methoxy-1-methylethyl acetate (PGMA). Further details are presented for the fabrication of the self-aligned gate devices in Chapter 4.

3.7 Electrical measurements

3.7.1 Current-voltage measurements

OFET device performance was evaluated by current-voltage measurements. Useful information about the device performance such as the mobility of the semiconductor can be evaluated from the data gained during testing and was discussed within Chapter 2. For this work a Keithley 4200-SCS semiconductor parameter analyser (SPA) was used in combination with a probe station in a N_2 filled glove box (**Figure 12**).



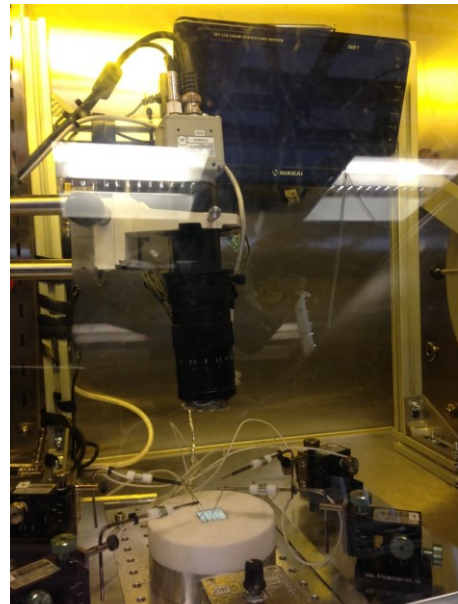


Figure 12: Left: Schematic representation of the experimental setup for carrying out electrical characterisation of OFETs. Right: Photograph showing a video probe station in a N2 filled glove box used for testing OFET device performance.

The probe station is used in an N_2 environment to reduce the effects of oxygen and water molecules on the semiconductor, which can reduce the performance on the device [11]. The device under test is placed on a plastic chuck and contact is made by moving “micro-probes” onto the source, drain and gate contacts.

3.7.2 Photodiode measurements

Photo-detector characterisation was conducted in a similar way to the current-voltage measurements described above. Device characteristics were measured in the dark and under illumination from a high power LED at various drive voltages. Specifically, transient current measurements were performed under pulsed illumination using an ultra-bright 660 nm LED driven by a wave function generator (TTI TG 4001) with pulse durations ranging from 50 to 500 ns. The output current for the photo-detector was amplified (Stanford Research SR570, 10 μA/V) and recorded on an oscilloscope (Tektronix TPS 2024). The output of a fast response time Si photodiode (DET100A, ThorLabs) was simultaneously recorded along with that of the device. Sequential current-voltage sweeps from -1 to +1 V were performed with the resulting current recorded in a nitrogen controlled atmosphere using a Keithley 4200 SPA.

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4 Adhesion lithography

New fabrication methods are frequently proposed to develop smaller and more efficient electrical devices [1, 2]. Many methods are however, variations on previous fabrication techniques which usually involve stamping [3], etching [4] or otherwise imprinting [5] patterns upon a surface. One approach which has received relatively little attention as a patterning technique is the use of adhesion forces. The lack of attention adhesive based patterning has received is perhaps surprising given the pivotal role it plays in many fabrication techniques. In photolithography, for example, strong adhesion of the photoresist to both metals and semiconductors is required to facilitate later processing [6]. If the photoresist detaches due to poor adhesion to the underlying layer, patterning will be unsuccessful [7]. Failure of photoresist normally involves premature detachment from the underlying material, most likely as a cause of improper development conditions [8]. Similarly, when fabricating complex electrical components which can form many interconnected layers, bonding agents are typically used to prevent detachment, demonstrating the importance of adhesion to successful manufacturing. One reason for the reduced cost of fabricating electrical components is the higher achievable yield now possible, partly thanks to better understanding of the adhesion mechanisms occurring during fabrication and throughout their lifetime [9].

Many newer fabrication techniques rely on some form of adhesive bonding to define micro- and nano- scale features. Take polydimethylsiloxane (PDMS) stamping, for instance, where to imprint a pattern upon a surface it is first required to release the pattern from the stamp [10, 11]. Stamping requires a difference between the adhesion of the patterned material to the stamp and surface with the latter needing to be stronger to

enable transfer. Similarly, self-aligned printing uses self-assembly monolayers (SAMs) to provide an adhesive (or wetting) barrier which induce a “roll-off” effect when a liquid is deposited [12, 13]. While these examples demonstrate adhesion is relevant to many fabrication techniques, this chapter describes a new technique that uses adhesive bonding as a fabrication methodology.

4.1 Adhesion measurements

The surfaces of four material systems (glass, Au, Al and Benzocyclobutene (BCB)) were initially examined to gain an understanding of their adhesive characteristics. Their adhesion properties were characterised based on their surface energies and ‘pull-off’ forces, using contact angle measurements, friction force-AFM and peel testing. Both their native surface properties and their properties after the attachment of SAMs were investigated, with a view to better understanding how SAMs could be used to alter the adhesion properties of each material.

Glass, Au and Al were treated with four different of SAMs (**Figure 1**), which from the literature were expected to alter the surface adhesion properties of the film. It has previously been shown that SAMs can form a nano-scale barrier upon the surface of these material [14, 15] such that their native adhesion properties are altered to more closely match that the functional group of the SAM monolayer [16]. It is possible to attach phosphoric acid based SAMs to oxidised surfaces such as Al [17], while thiol SAMs are widely deposited onto non-oxidising metallic surfaces such as Au [18]. These

are the most commonly studied type of SAM and have been discussed extensively in the literature.

SAMs with two different functional end-groups were investigated, as shown in **Figure 1**. These SAMs were both alkane and carboxyl terminated SAMs and were expected to show differing adhesion properties based on their functional groups.

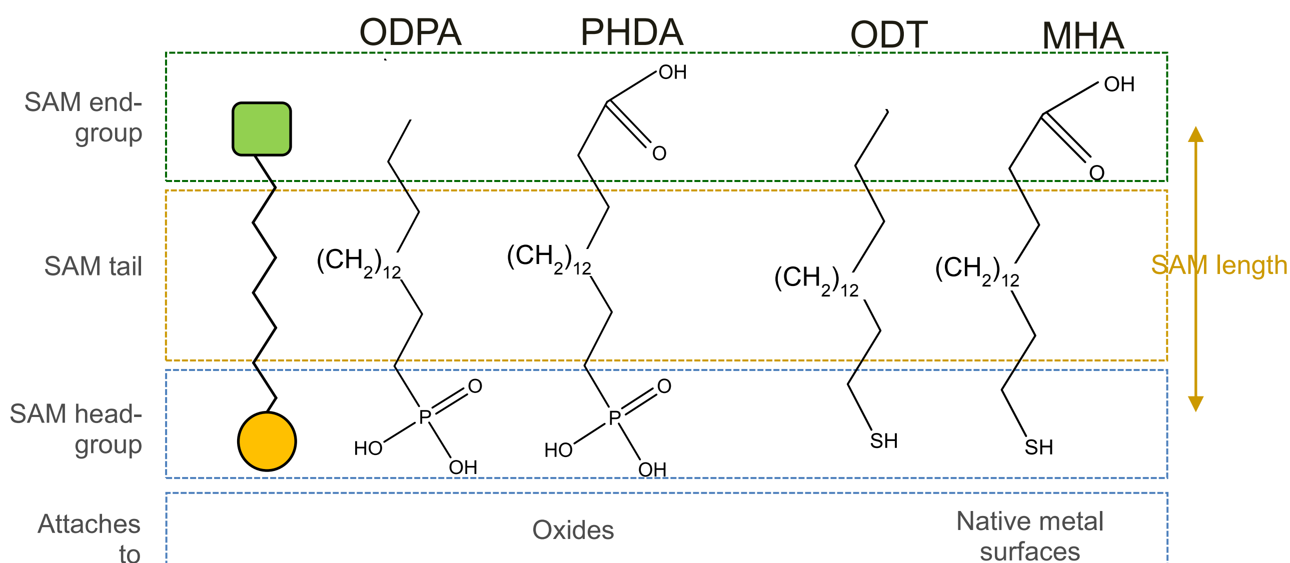

Figure 1: The chemical structures of four different SAMs from right to left octadecylphosphonic acid (ODPA) and phosphonododecyl-phosphonic acid (PHDA) for attachment to Al and glass and octadecanethiol (ODT) and mercaptohexadecanoic acid (MHA) for attachment to Au.

By using the same terminal group on SAMs across different material systems (glass, Al, Au and BCB), it was hoped an understanding of how the SAMs are capable of altering the adhesion properties of the materials they are attached to could be gained. Au and Al were selected due to their prevalence in electronic and opto-electronic devises, while BCB is widely used in the electronics industry due to its ease of processing, good planarization, and its ability to act as a 'spin-on' dielectric material and adhesion promoter. BCB is cured via thermal activation at temperatures above

200°C, the extent of curing increasing with time [19]. Although it is not possible to attach a SAM to BCB due to an absence of suitable bonding sites its adhesion properties were investigated at various stages during curing.

For each material system, contour plots were produced by making contact angle measurements (Kruss G10) at multiple positions across surfaces. The drop-volume was kept constant at 10 μl and all measurements were performed in a climate-controlled clean room. In the case of the non-SAM treated films, surfaces were first cleaned in an O_2 plasma for 30 seconds with a plasma rating of 100 watts and O_2 flow rate of 10 mbar. SAM deposition was performed by thoroughly cleaning the substrate in acetone and isopropyl alcohol (IPA) using an ultrasonic bath before placing the substrates into an O_2 plasma for 20 minutes to remove organic contaminants and in the case of Al induce the formation of a surface oxide layer. The substrates were then placed in a Petri dish containing the dissolved SAM molecule (5 mm) where they were left covered for 24 hours to allow SAM attachment before being removed and finally lightly rinsed and dried in a stream of N_2.

While contact angle measurements give a good indication of the surface energy, coverage and wettability of a surface, they do so in a macroscopic way owing to the droplet area being on the order of a few mm^2. Friction force-AFM, however, allows for a nanoscale probe of the local adhesion forces present at the sample's surface via the interaction of a special, low resonant frequency, AFM tip with the sample's surface. The peak detachment force is directly related to the properties of the AFM tip and sample's surface as outlined in Chapter 3. As the interaction of the sample and tip only occurs

over 10 – 20 nm (the diameter of the AFM tip) the measurement gives a powerful insight to the local surface properties of the film.

The friction force-atomic force microscope used in this study was an Aglient 5500 AFM with NanoSensors PointProbe Plus tips. To reduce the effects of relative humidity, which can strongly alter the tip-sample interaction [20], measurement were performed in an inert atmosphere with a constant flow of dry nitrogen. A single friction force-AFM scan is subject to environmental instability due to the small forces being measured; as such 10 scans were taken at 5 second intervals in 3 different positions across the sample. In addition to investigating a single tap of the AFM tip (which is only in contact with the sample for a short, undetermined, amount of time), the AFM tip was also held in contact with the sample surface for 1, 5 and 10 seconds at each position to determine whether the interaction of the tip changed with time.

A typical friction force-AFM scan curve is shown in **Figure 2**. Only the re-trace of the scan is shown, corresponding to the withdrawal of the AFM tip and the withdrawn from the sample surface (as discussed in the experimental chapter). The retrace describes the cantilever's actions after it has made contact with the sample's surface, this demonstrates the adhesive "pull-off" force used by the cantilever to overcome the short-range interaction forces present near the sample's surface.

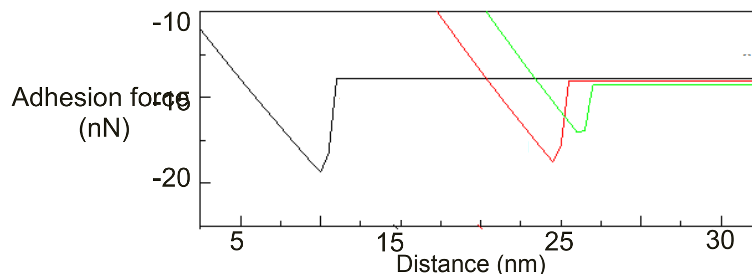

Figure 2: Three different adhesion force scan points recorded on a bare Al surface showing the 'pull-off' force encountered by the AFM tip at each point.

4.1.1 Glass adhesion properties

Owing to its low coefficient of thermal expansion (~3 × 10^{-6} /°C at 20°C), glass containing borosilicate is commonly used in the electronics industry. The major components of borosilicate glass are silica and boron oxide. It has previously been reported that phosphonic acid SAMs can be attached to silica [21]. But to the author's knowledge, the deposition of phosphonic acid SAMs onto borosilicate glass has not been reported previously.

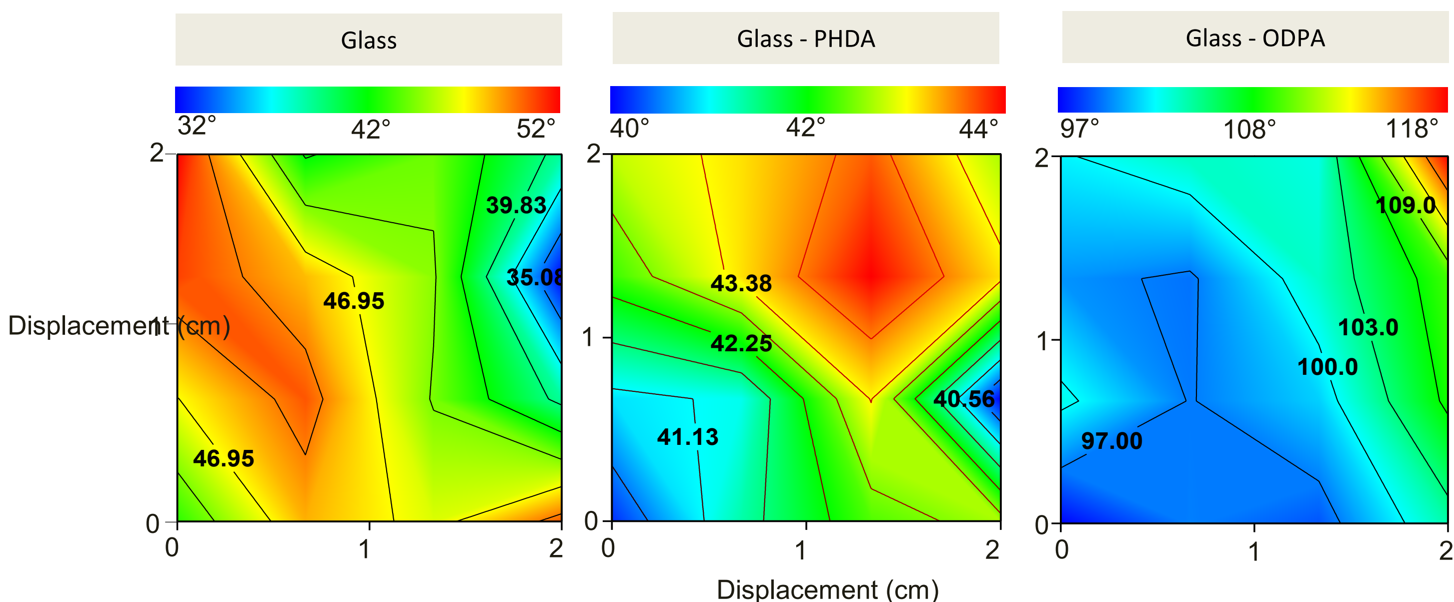

Figure 3: Static angle contour plots for 2 x 2 cm glass substrates with different surface treatments. The bare glass film shows an average contact angle of 44 ±6.4°, decreasing to 42 ±5° for PHDA and sharply increasing to 105 ±3.5°when ODPA is applied.

Static contact angle contour plots for borosilicate glass slides treated with PHDA, ODPA and an untreated film are displayed in **Figure 3.** As can be seen, the contact angle reduces slightly when PHDA is due to the surface becoming more hydrophilic. When coated with ODPA, however, the contact angle sharply increases due to an increase in hydrophobicity. The difference in contact angle for two SAM-coated surfaces shows the SAM has a dramatic effect on the surface properties of the glass

film, either preventing or inducing wetting depending on the SAM functional group. Further evidence can be seen in the friction force-AFM data of **Figure 4**.

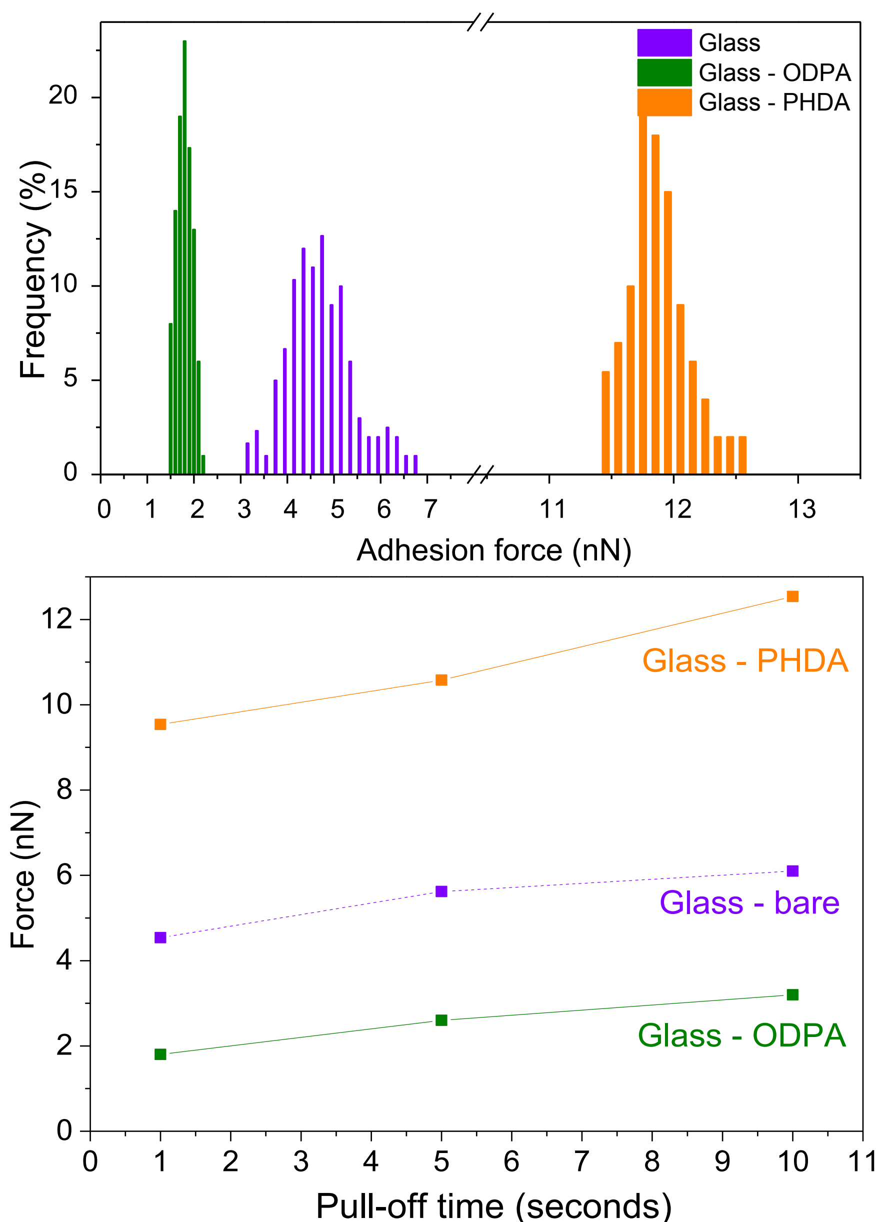

Figure 4: Top: Histogram showing the required AFM cantiliever 'pull-off' force in nN for glass slides coated with ODPA (1.8 ± 0.3 nN) and PHDA (11.6 ± 0.5 nN), along with a bare glass film (5.1 ± 0.4 nN). Bottom: averge 'pull-off' force for the same films when the AFM cantiliever is held on the surface for between 1 and 10 seconds.

The PHDA-coated glass slide with its O_2-rich SAM functional group records the highest adhesion force of 11.6 ± 0.5 nN compared to 1.8 ± 0.3 nN for the hydrophilic ODPA-coated slide and 5.1 ± 0.4 nN for the native glass surface conforming the SAM can modify the surface of borosilicate glass.

4.1.2 Al adhesion properties

Phosphonic acid SAMs have been widely used as ultra-thin dielectrics in organic thin film transistors where Al is commonly used as a gate electrode [22]. Applying the SAM to the electrode modifies the surface energy of the Al, making it either more hydrophobic or hydrophilic, depending on the nature of the SAM applied [23]. Many reports have been published describing ways to optimise and control the deposition of SAMs [17] on metal surfaces. However their influence on surface adhesion has been largely overlooked, and warrants further investigation. **Figure 5** and **Figure 6** show static contact angle measurements contour plots and friction force-AFM adhesion measurements of bare Al, Al-PHDA and Al-ODPA respectively.

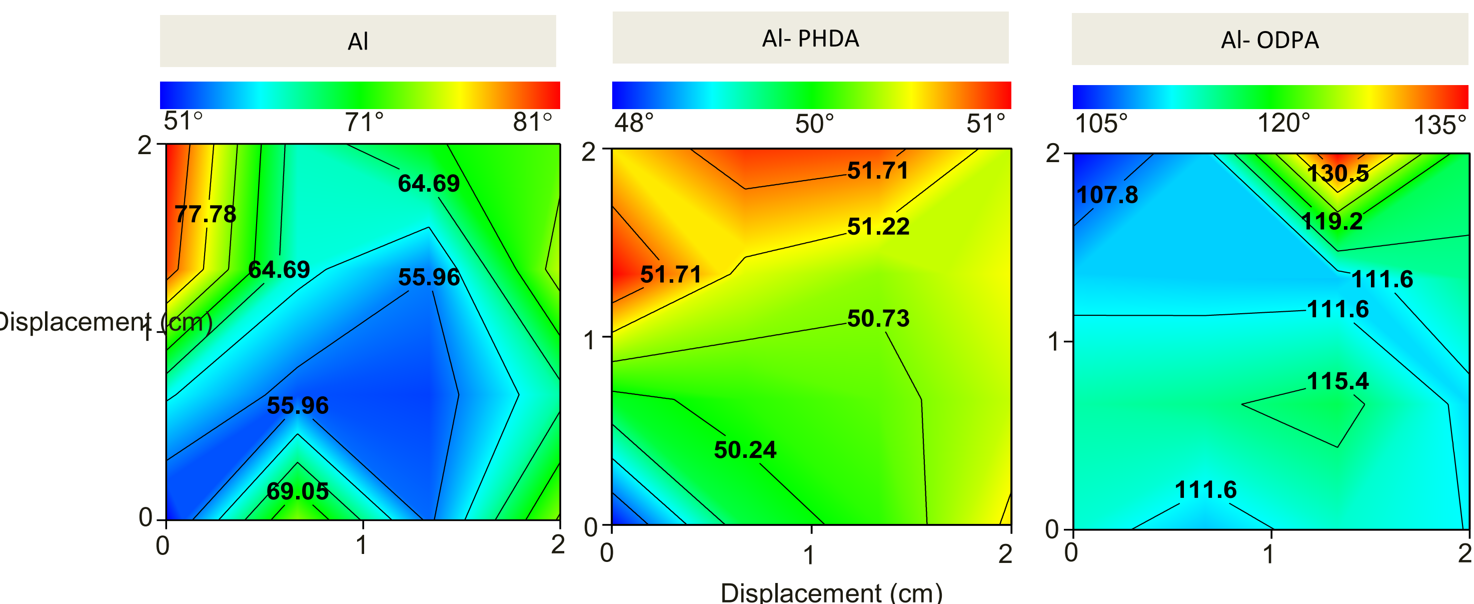

Figure 5: Static angle contour plots for 2 x 2 cm Al coated glass substrates with different surface treatments. The bare Al film shows an average contact angle of 66 ± 4°, decreasing to 51 ± 6° for PHDA, sharply increasing to 116 ± 2° for ODPA.

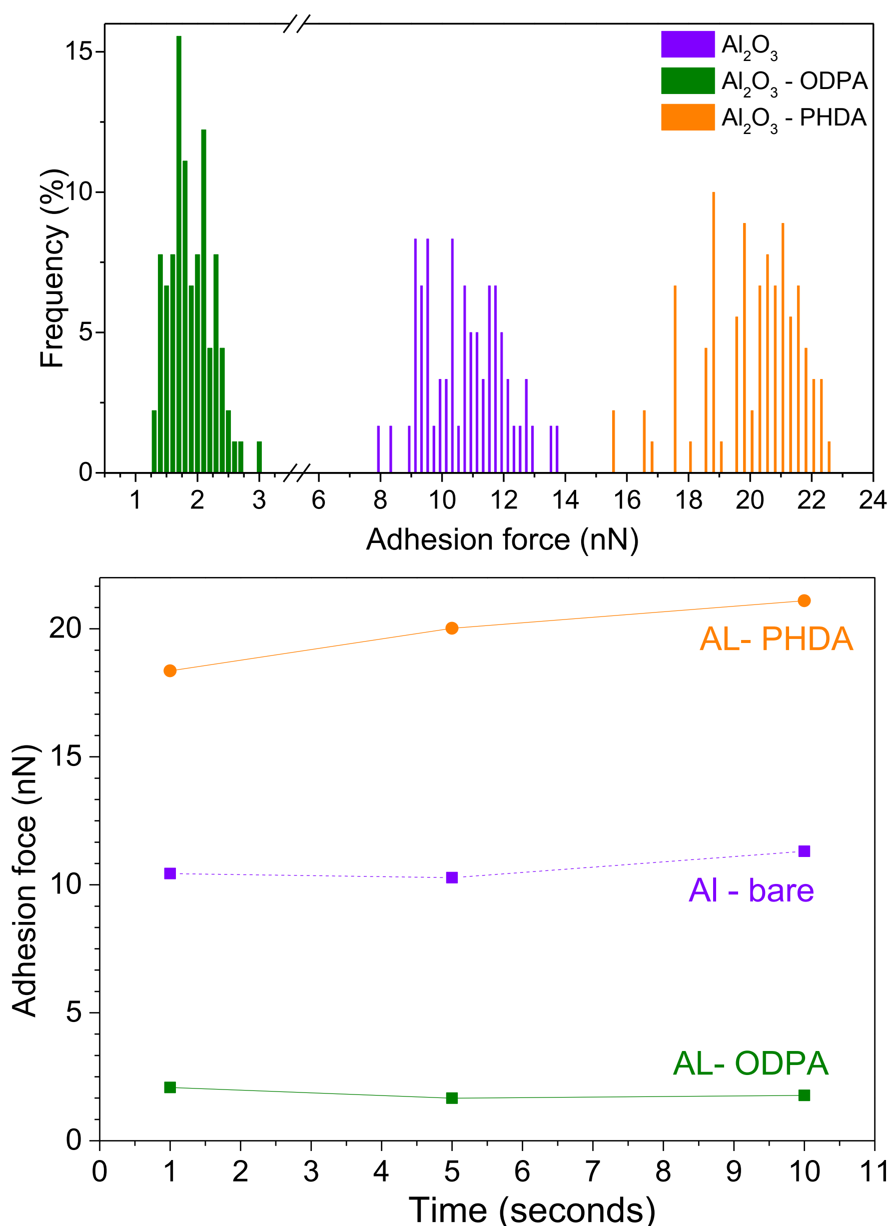

Figure 6: Top: Histogram showing the required AFM cantilever 'pull-off' force for Al-coated glass slides coated with ODPA(1.8 ± 0.3 nN), PHDA (22.4 ± 0.5 nN) and bare Al film (10.7 ± 0.4 nN) when the cantilever was held in contact with the substrate for 1 second. Bottom: average 'pull-off' force for the same films when the AFM cantilever is held on the surface for between 1 and 10 seconds.

The native contact angle of the Al is 66 ± 4° falling to 51 ± 6° for PHDA and rising to over 116 ± 2° for ODPA. For bare Al an adhesion force of 10.7 ± 0.4 nN was recorded by friction force-AFM. Using the hydrophobic SAM monolayer ODPA reduced the adhesion to 1.8 ± 0.3 nN (compared to 1.8 ± 0.3 nN for the ODPA-coated

glass slide). Using PHDA, the adhesion force increased to 22.4 ± 0.5 nN compared to 11.6 ± 0.5 nN for the ODPA-coated glass slide.

4.1.3 Au adhesion properties

Thiols are used in a wide range of fields including molecular biology, inorganic chemistry, surface science and materials science [24]. It has been shown that the thiol-Au bond is stronger than other functional group metal combinations, giving rise to a very stable surface coating [25, 26]. As shown in **Figure 7** coating Au with a SAM induces similar wetting changes to Al and glass. The film becomes either more hydrophilic or hydrophobic depending on the chemical composition of the SAMs tail group.

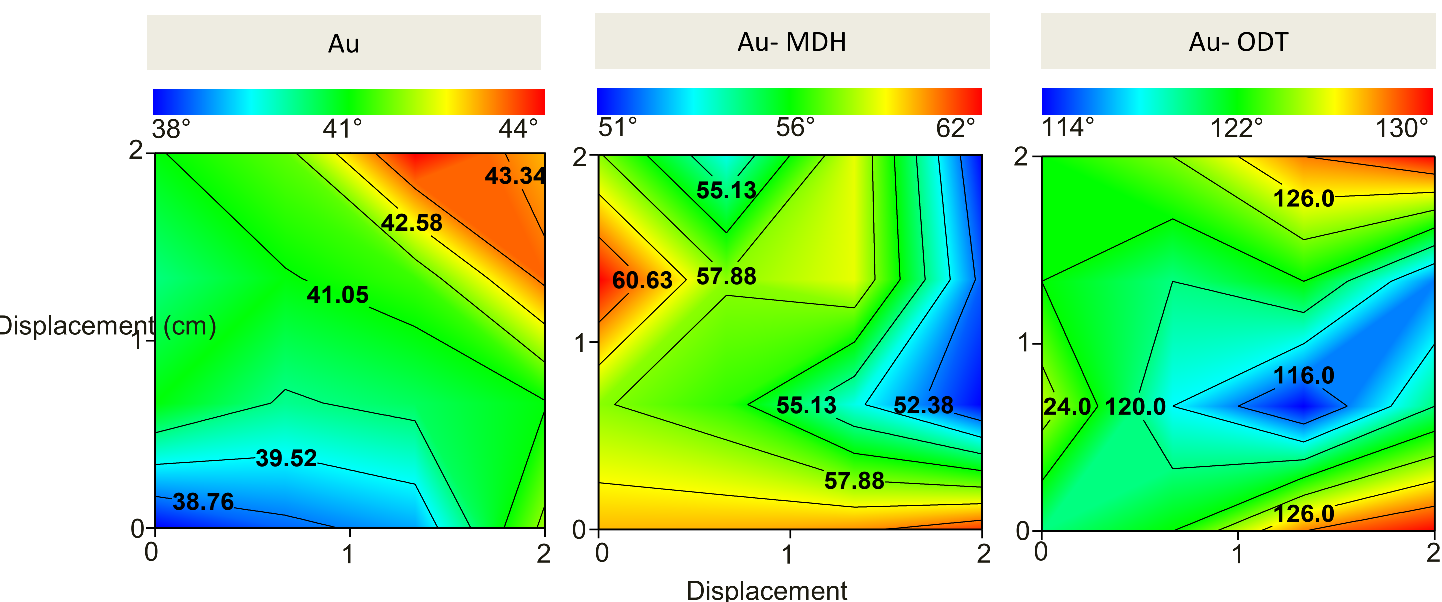

Figure 7: Static angle contour plots for 2 x 2 cm Au-coated glass substrates with different surface treatments. The bare Au film shows an average contact angle of 41 ± 6°, increasing to 55 ± 2° for MHA and, similar to the Al-ODPA, sharply increasing to 119 ± 1 ° for the ODT film.

Friction force-AFM adhesion measurements for the Au-coated SAM film showed the same trend seen for the glass and Al films, with higher adhesion values

recorded for the hydrophilic Au-MHA film and lower values for the hydrophobic Au-ODA film. As the thiol and phosphoric acid SAMs show similar results irrespective of the underlying layer and head group, the tail group surface chemistry appears to be the dominant factor in the deciding the adhesion strength (**Figure 8**).

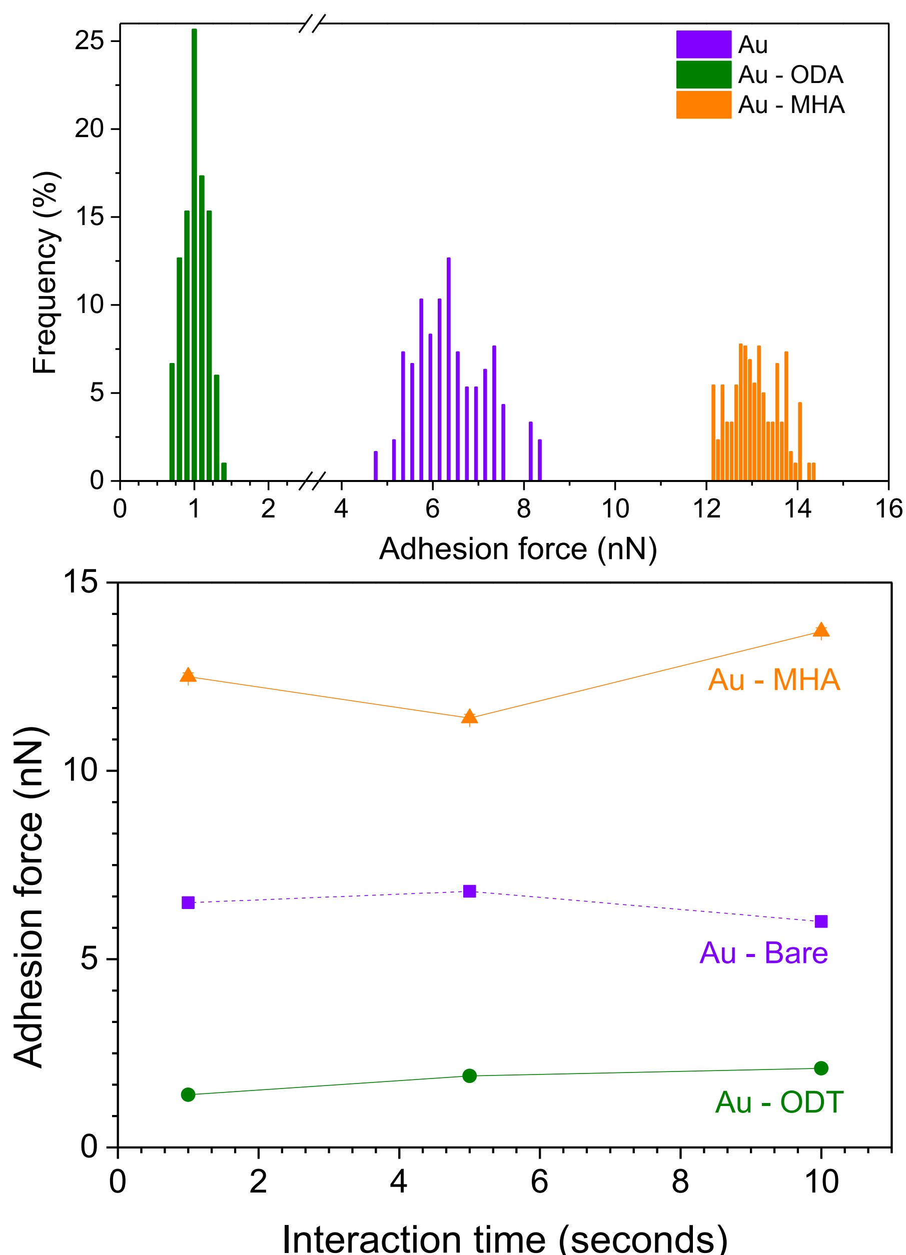

Figure 8: Top: Frequency distribution diagram representing the required AFM cantilever pull-off force in nN for Au slides coated with ODT (1.2 ± 0.3 nN) and MHA (13.4 ± 0.4 nN) along with a bare Au film (6.4 ± 0.4 nN) when the cantilever was held in contact with the substrate for 1 second. Bottom: average pull off force for the same films when the AFM cantilever was held on the surface for between 1 and 10 seconds.

4.1.4 Benzocyclobutene adhesion properties

Benzocyclobutene (BCB) is a heat curable polymer supplied in a liquid pre-cursor form consisting of a partially polymerised polymer in an organic solvent. After deposition onto a substrate (typically by spin coating) and evaporation of the solvent, BCB can then be polymerised via heat curing. The degree of polymerisation is generally controlled by how long and at what temperature the film is cured. Partly polymerised layers typically have better adhesion to the following layer than fully cured ones [27, 28]. To more closely study the effect of polymerisation on the adhesive properties of BCB, as-deposited BCB, soft-baked BCB (partially cured) and hard-baked BCB (fully cured) films were investigated. As-deposited BCB was lightly annealed at 100°C for 20 minutes to remove solvent and form a semi-stable film; soft baked BCB was annealed at 150-170°C for 2 hours and fully cured BCB was annealed for 6 hours at 250°C as per the manufacturers' recommendations.

Owing to the instability of BCB in its as-deposited form, it was not possible to carry out static contact angle measurements of the BCB film even with an initial 100°C annealing step as the film was too soft. **Figure 9** depicts the results for the soft- and hard- baked films which were stable enough to measure. As can be seen from **Figure 9**, the average contact angle for the soft-baked film was 57 ± 5° compared to 71 ± 7° for the hard-baked film. Hard-baking therefore makes the film slightly more hydrophobic but does not prohibit wetting to the extent of ODPA or ODA.

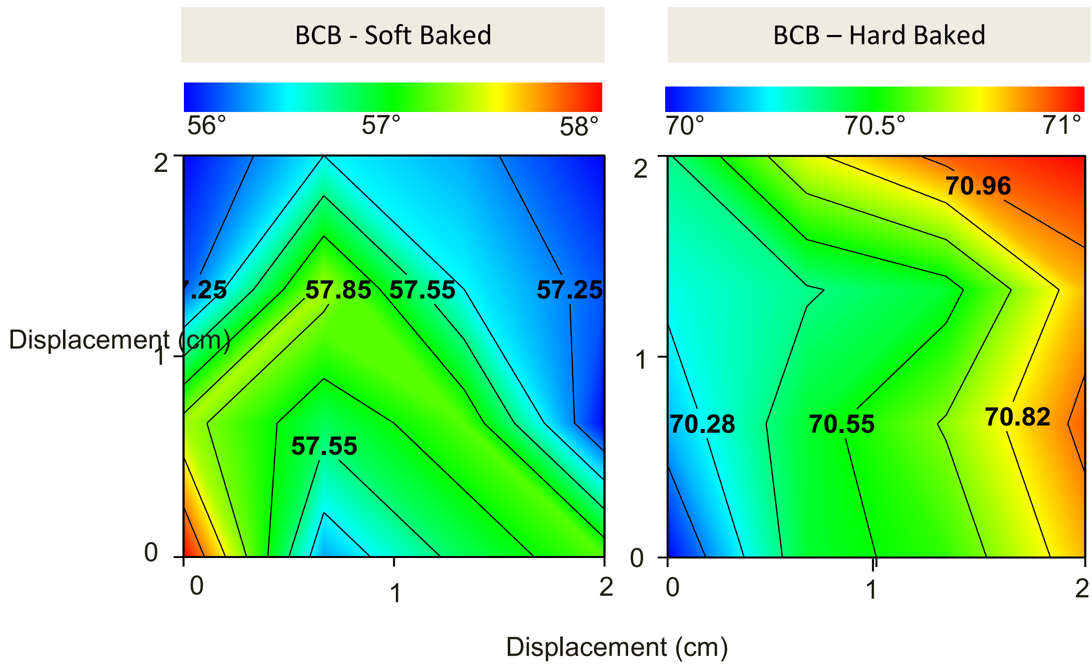

Figure 9: Static angle contour plots for 2 x 2 cm BCB-coated glass substrates under different curing conditions. The soft baked BCB film showed an average contact angle of 57 ± 5°, compared to 70 ± 7° for the hard-baked film.

The friction force AFM data in **Figure 10** shows the soft-baked film recording an adhesion force of 10.6 ± 0.4 nN compared to 2.3 ± 0.3 nN for the hard-baked film suggesting a significant decrease in adhesion occurs on annealing as the BCB undergoes crosslinking.

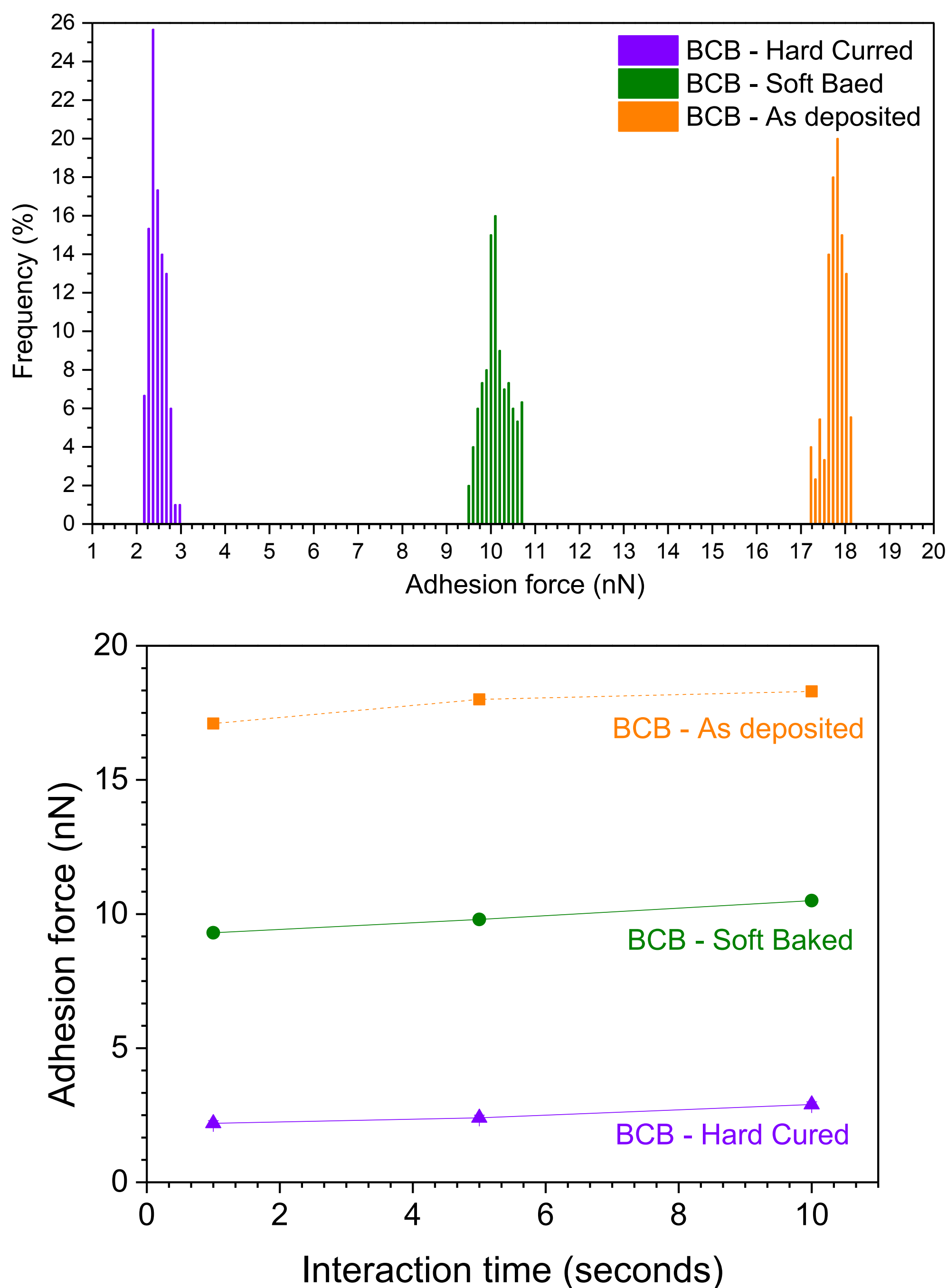

Figure 10: Top: frequency distribution diagram representing the required AFM cantilever pull-off force in nN for BCB coated slides after undergoing different curing treatments, namely soft baking (10.6 ± 0.4 nN), hard baking (2.3 ± 0.3 nN) and light annealing at 100°C (17.9 ± 0.3 nN) when the cantilever was held in contact with the substrate for 1 second. Bottom: average pull-off force for the same films when the AFM cantilever was held on the surface for between 1 and 10 seconds.

4.1.5 Summary of adhesion properties

The adhesion measurements reported in the first half of this chapter show how the adhesion forces of various materials differ based on their surface properties and treatment methods. As is clear from **Figure 11**, by modifying the native adhesion of glass, Al, Au and BCB with SAMs or heat treatments, it was possible to either enhance or reduce the adhesion of the underlying material. The greatest difference was achieved by applying hydrophobic SAMs such as ODPA and ODT to the metallic films or hard baking the BCB substrate. In all cases this resulted in a large reduction in the adhesion properties of each film (applying more hydrophilic SAMs such as PHDA and MHA resulted in a small increase in adhesion for the metallic films).

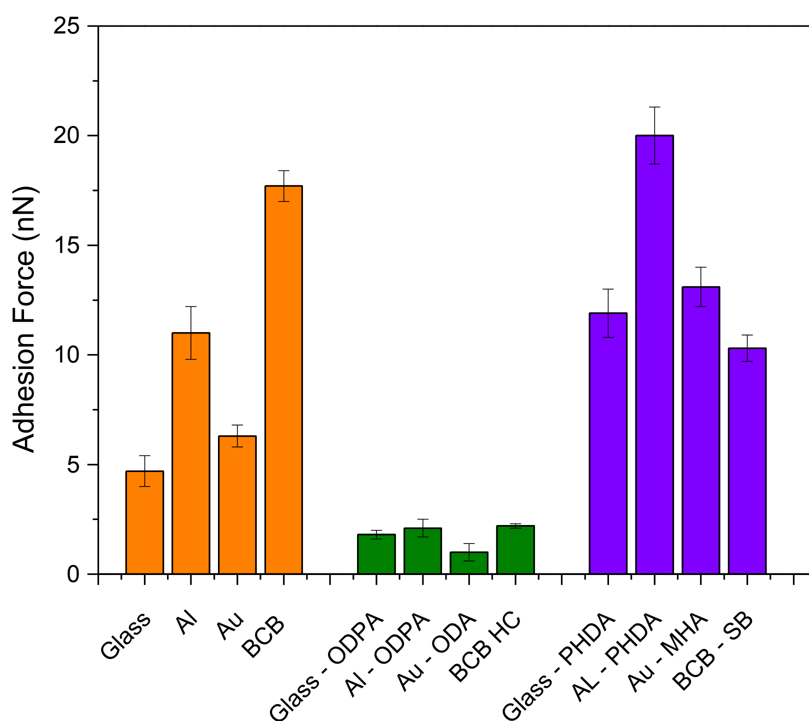

Figure 11: Comparison of the measured nano-scale adhesion forces of glass, Al, Au and BCB substrates. The lowest recorded adhesion forces were observed when low adhesion SAMs such as ODPA and ODT were coated on glass, Al and Au. Increased curing of the BCB film lead to reduced adhesion due to further crosslinking occurring within the film.

4.2 Adhesive patterning

On the basis of the understanding gained in the previous section, I sought to develop an adhesion-based method for pattering thin films. I show that patterning of metal films can be carried out by removing one metal from another using only adhesion forces such that, in the final configuration, the two metals sit side by side in a coplanar configuration isolated from each other. For patterning to succeed it is imperative to ensure the adhesion of the metal to the substrate is sufficient to withstand the peeling force being applied (i.e. the metal must not delaminate from the substrate during peeling. This can be investigated by using adhesion tape to strip away a deposited material). Three types of household adhesive tape were selected to compare their adhesion and physical properties (**Figure 12**) aluminium tape, PVC-backed electrical insulation tape and scotch tape. The adhesion of tape is normally specified in terms of their adhesion to steel, this ranges from 1.8 N /mm for PVC-baked tape to 2.2 N /mm for scotch tape and to 3.4 N /mm for aluminium tape. Another important property is the elasticity of the tape when it is peeled from a surface, which may affect the uniformity of the applied strain the metal film is subjected to during peeling. The elasticity varies from 25% for the rigid aluminium backed tape to 150% for the scotch tape and to 350% for the PVC backed electrical insulation tape.

For the patterning process described below, weak peeling forces were required to minimise the risk of the metal detaching from the substrate. Initial visual peeling tests of the three tapes on plain glass substrates demonstrated that the electrical insulation tape, which has the weakest level of adhesion, left the least amount of residue (which could be easily removed by rinsing the substrate in solvents). As such electrical

insulation tape was chosen to undertake initial experimentation on the peeling properties of the various metal films.

Figure 12: Three types of tape (A) aluminium tape, (B) PVC-backed tape and (C) common household Scotch tape.

4.2.1 Peel testing

To determine the effects of the electrical insulation tape in peeling metal films, 40 nm of Au and Al were evaporated onto glass slides via shadow masking forming 30 5 x 5 mm squares in a pattern similar to that used for the international standard governing adhesion testing, American Society for Testing and Materials (ASTM) D3359 - 09e2, which is commonly used to compare adhesive films [29] (see **Figure 20**). While ASTM D3359 - 09e2 specifies the use of 50 10 x 10 mm squares this pattern would be too large to fit onto the substrates used in this experiment, as such the pattern was modified to make use of fewer smaller squares. The pattern allows for a visual inspection of the amount of metal removed after peeling has occurred by examining both the substrate and the back side of the tape (where any removed metal will remain). In addition to glass substrates, to which the adhesion of metal was expected to be low, BCB-coated glass slides were also tested. To investigate the effect of curing on the peeling behaviour, tests were made after BCB had been soft-baked (e.g. BCB deposition – soft-bake – metal deposition), hard-baked (e.g. BCB deposition – hard-bake –metal

deposition), and both soft- and hard-baked with the metal deposition occurring before the hard-bake (i.e. BCB deposition – soft-bake – metal deposition – hard-bake).

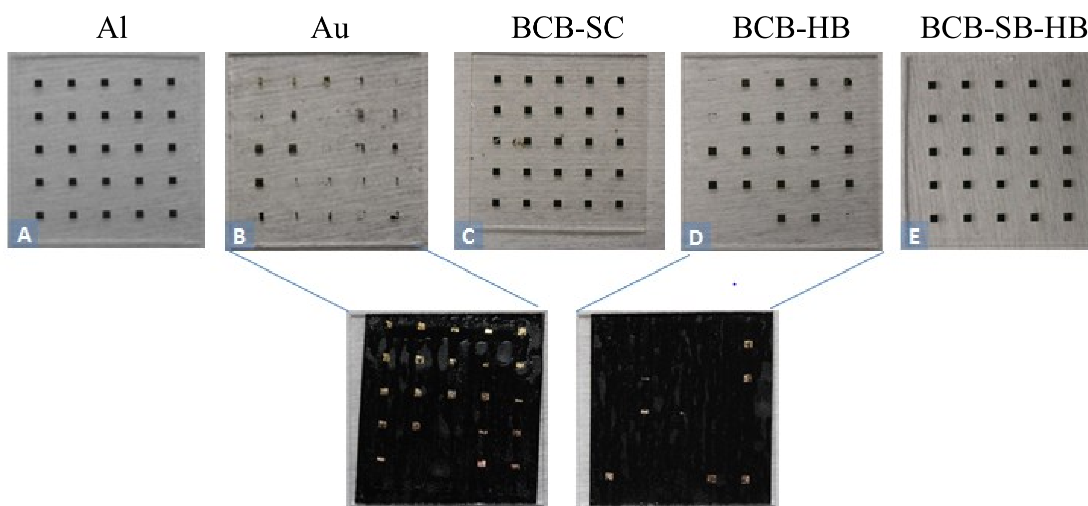

Figure 13: Top row: photographs of various metals deposited onto glass microscope slides after being peeled using electrical insulation tape. (A) Al, remains fully attached to the substrate (B) Au is largely removed by the peeling force of the tape (C) BCB coated slide which has been soft baked before having Au deposited on top and then peeled. The Au remains on the surface of the BCB (D) BCB-coated slide with Au deposited after hard baking, showing detachment of the Au. (E) BCB-coated slide with Au deposited after soft baking and before hard baking to a fully cured state. Similar to (C) the Au remains fully attached to the film.

Both Al and Au were initially deposited onto glass slides. As can be seen from **Figure 13**, the Al squares stayed attached to the glass substrate after being peeled using the electrical insulation tape (**A**), in contrast much of the Au was removed by the tape (**B**)**.** To see whether BCB could enhance the adhesion of the Au, the three curing treatments described above were carried out. When Au was deposited onto hard-baked BCB, the Au film detached (**D**). However when deposited on soft-baked BCB, Au remain attached, with or without a final hard baking step as shown in **E**.

The adhesion of metals to BCB is affected by the degree of crosslinking within the polymer film [30]. When BCB is first deposited it has a tacky consistency. When

soft-baked the film hardens to a point where it is possible to evaporate a uniform film on top of it. As was previously discussed the adhesion of Au to the soft baked film was 10.6 ± 0.4 nN, nearly twice the adhesion of glass (5.1 ± 0.4 nN). Thus when the Au is deposited at this stage it adheres to the partially cross-linked surface of the BCB moreover as **Figure 13 E** demonstrates it remains adhered even after the final hard-bake.

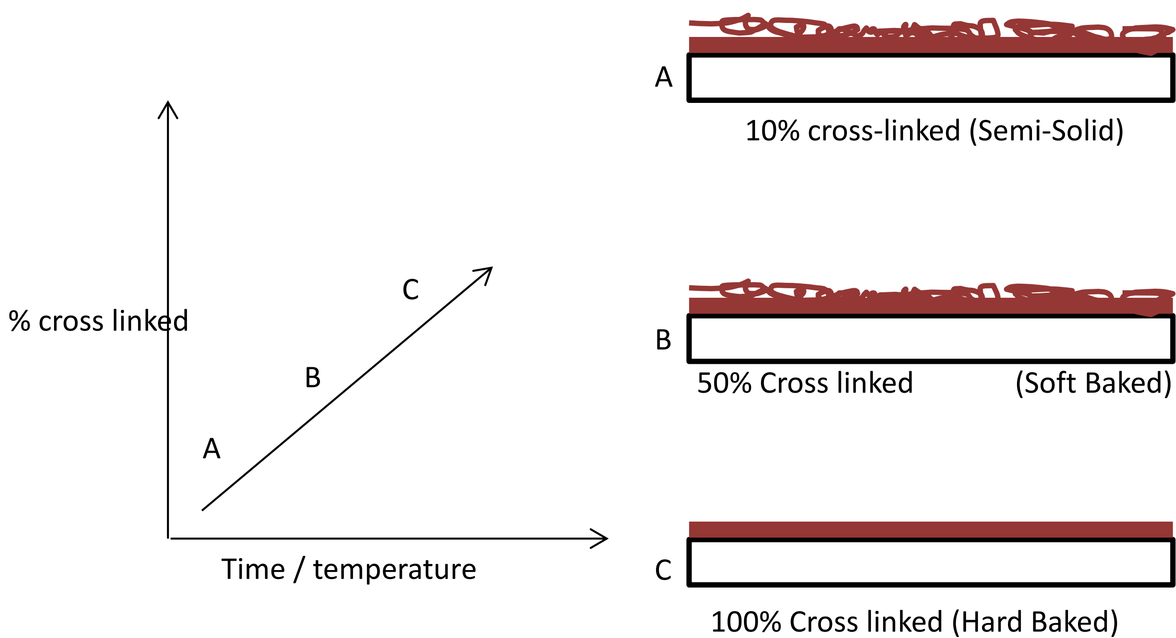

Figure 14: Diagram depicting the three stages of the BCB curing cycle in reference to its adhesion properties. The initially deposited film is a semi-solid and required annealing before it is suitable for device fabrication. In this state the film is very sticky.

The differences in the adhesion properties of BCB during its various stages of crosslinking are summarised in **Figure 14**. When first deposited BCB is highly adhesive as non-cross-linked polymer chains are present on the surface of the film. However the film is also too unstable (i.e. if a metal is thermally evaporated as this stage the metal will be wrinkly in appearance upon the as-deposited BCB) to deposit further material as it has not yet been cross-linked (**A**). Upon annealing, approximately 50% of the film is

cross-linked [30], at this stage non cross-linked chains remain on the surface of the BCB film, ensuring good adhesion (**B**). When fully cross-linked by further annealing the film, the BCB is converted into a highly stable and chemically inert solid body with weak adhesive properties (**C**). At this point, any bonding which has previously occurred during the soft bake remains and as such any material adhered during the soft bake remains on the BCB after the hard bake has been completed.

As an alternative adhesion layer to thermally cured adhesives, it is common to use an evaporated adhesion layer such as Cr or Ti. In this approach a thin adhesion layer is deposited and Au is then deposited upon this film. In this configuration, the Au forms a bond not with the glass slide but the adhesion layer which has better native adhesion to glass. To determine if this configuration could provide adequate adhesion of Au to withstand the peeling force of the adhesive tape, ~5 nm of Al or Cr were deposited on glass microscope slides. As **Figure 15** shows, the inclusion of 5 nm of either Al or Cr before deposition of the Au results in an enhanced adhesion effect such that the Au could not now be removed by the applied peeling force.

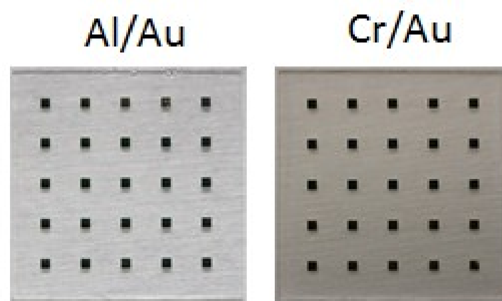

Figure 15: Photographs of Au deposited onto a glass microscope slide coated with a 5 nm layer of Al or Cr after repeatedly peeling with PVC tape. The Au remained adhered to the glass, even after repetitive peeling attempts.

To summarise, both Al and Au can withstand adhesive peeling on glass slides. However, Au requires the use of an adhesion layer or polymer coating to ensure it stays adhered, adding to the complexity of using Au for patterning. For an adhesive bond to

form, the metal must react chemically with the surface. In the case of Au, a noble metal, bond-formation is weak and thus poor adhesion occurs. However Al is able to react chemically with the glass surface (assuming it's clean) where it forms a strongly adhered interface. The adhesion of Au may be enhanced using BCB. Inter-diffusion and mechanical interlocking of the two materials occurs when BCB is cross-linked, resulting in the formation of a strong adhesive bond capable of preventing detachment during peeling by adhesive tape.

4.2.2 Advanced peel testing

To further evaluate the adhesion properties of both Al and Au, an adhesion tester was used to determine the pull-off force for various combinations of each metallic film. Further details of the peel testing procedure are given in Chapter 3. The initial metal film, M1, (either Al or Au) was first deposited uniformly onto a glass microscope slide. When Au was used for M1 a 5 nm layer of Cr or Al was used as an adhesion layer (discussed above). A second, metal film, M2, can then be deposited on top of M1 to form a two layer structure. M1 and M2 were not deposited in immediate succession. Instead the vacuum within the evaporation chamber was broken before the deposition of M2. M1 was cleaned and subjected to a light oxygen plasma ash before deposition of M2. This is necessary as if this structure were to be used for patterning the vacuum would also be broken and the film subjected to cleaning. In the case of Al plasma ashing would induce the formation of a thin oxide layer on the surface of the film (**Figure 16**).

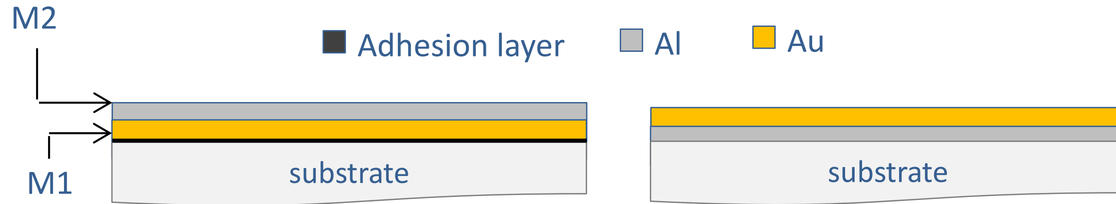

Figure 16: Structure of the initial peel test samples using Al on the AU (left) and Au on the Al (right). In this configuration both films are in contact with each other, for adhesion to occur between M1 and M2 physical interlocking, inter-diffusion or chemical bonding between each surface must occur. It would be expected that both films will adhere to each such that it will not be possible to separate the two films.

For complete peeling of the tape from the surface of M2 (without the removal of M2) the adhesion between the adhesive tape and M2 must be weaker than the adhesion between M2 and M1, which can be ensured by judicious selection of the adhesive tape and ensuring strong adhesion of M2 to M1 occurs. The adhesion between M1 and M2 can, however, be altered by the deposition of a physical barrier between the two films which would act to reduce the chemical reactions which normally take place during evaporation of M2 upon M1. Barrier metals and metal oxides such as cobalt, indium oxide or tantalum are commonly used to chemically isolate semiconductors from their metal interconnects during integrated circuit manufacture [31]. Typically such barriers have electrical conductivity to facilitate electrical connections between different layers in the circuit. The barrier, therefore, acts to chemically isolate materials within the circuit which may otherwise inter-diffuse, limiting their performance. Too thin a barrier and the coating will not be effective; too thick and it may interfere with the normal operation of the circuit. Typically such coatings are deposited and etched in much the same way as the other parts of the circuit. Thus if a barrier material were deposited between M1 and M2 it may be possible to remove the two films from each other by peeling M2 from M1 using tape this may enable patterning to occur if M1 or M2 is patterned.

It has already been established in the last chapter that the presence of a SAM can reduce the surface adhesion of a metallic film by up to 90%. The benefit of applying a SAM over traditional barrier materials is that they can self-assemble into well aligned and continuous 'films' as well as potentially providing electrical insulation. The basis of the pattering procedure described here is that the SAM selectively attaches onto the profile of M1 where it inhibits adhesion of M2. To investigate the effects of attaching a SAM to M1, the same configuration described before was used (**Figure 16**) except a low adhesion SAM was deposited on M1: ODPA onto Al and ODT onto Au. As shown in **Figure 17**, this results in a sandwich configuration where the SAM sits between M1 and M2.

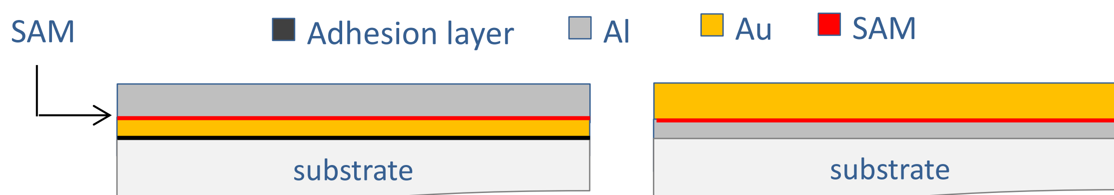

Figure 17: Structure of the SAM-treated films used for peel testing. The SAM was deposited on top of M1 before the deposition of M2 such that it was sandwiched between the two films in the final configuration.

For whole-film peeling, i.e. where the SAM is not in contact with the glass slide, SAM attachment should only occur on the metallic parts of the film (M1). However if part of the glass slide is exposed through voids in M1 phosphoric acid based SAMs, such as ODPA, would attach to the glass through these voids (i.e. the SAM will both attach to the glass slide and M1). As such the adhesion profile between M1 and the glass will be similar and controllable patterning may not be possible (**Figure 18 A**). To avoid this, a substrate to which ODPA will not attach is required, such as an appropriately selected polymer. By coating the surface of the glass with that polymer before depositing M1, the SAM will only attach to the metallic patterned electrode,

resulting in the desired adhesion profile forming between the two surfaces (**Figure 18 C**).

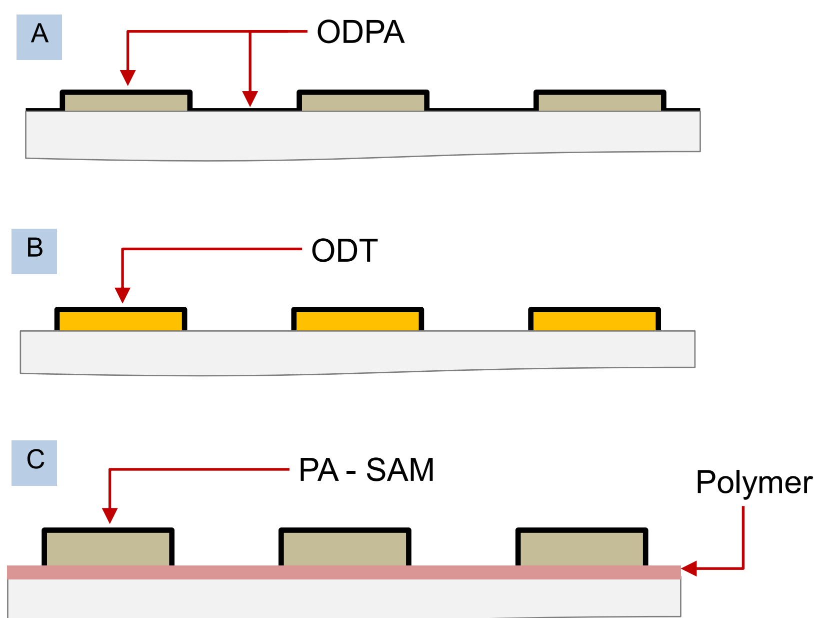

Figure 18: Schematic of SAM-treated patterned films. (A) When ODPA is applied to glass it adheres to both M1 and the glass such that no adhesion profile is created. (B) ODT, however, does not attach to glass and only forms on the Au film. (C) To prevent ODPA from attaching to the glass slide, a polymer buffer layer can be used to which ODPA does not attach.

BCB was chosen as a buffer layer as its adhesion properties had already been investigated. For films where Al was used as M1, glass slides were first coated with a 2 µm thick soft-cured BCB buffer layer (**Figure 19 A-B**). Al was deposited on top of the BCB, and ODPA was then allowed to self-assemble onto the Al surface by immersion in a solution of the SAM (**Figure 19 C**). At this stage, the surface of the BCB was still not fully cured, allowing M2 to be deposited and form a well-adhered film. The BCB was then fully heat cured to ensure that both M1 and M2 were strongly adhered to the substrate (If M2 is Au this also negates the need for an adhesion layer such as Cr since Au is strongly adhered to the BCB substrate during the curing cycle (**Figure 19 D**)).

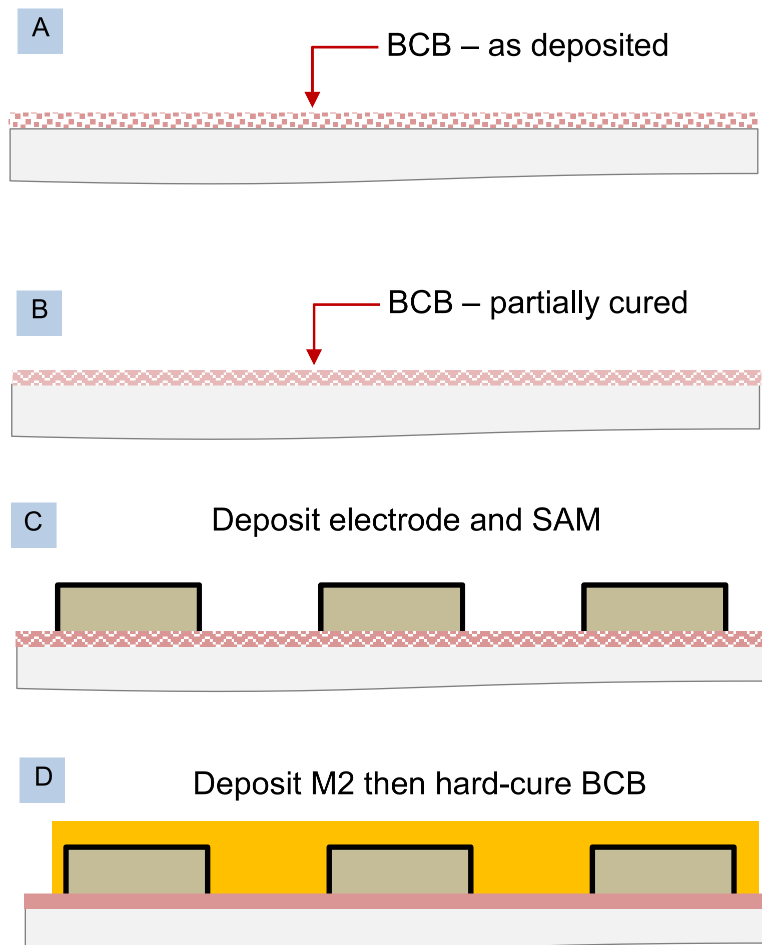

Figure 19: Schematic depicting the polymer buffer deposition method: (A) BCB is deposited on a glass microscope slide (B) BCB is partially cured to make it robust enough for further processing (C) Al is deposited and ODPA self assembles only onto the Al (D) M2 is deposited and the film is hard cured.

To initiate peeling a peel tester was used to controllably peel the tape and record the associated peeling forces. Electrical insulation tape was applied evenly across the surface of M2 and peeled back at a constant rate of 10 mm/s, 90° relative to the surface (**Figure 20**). The peeling force was then recorded as a function of distance travelled along the substrate

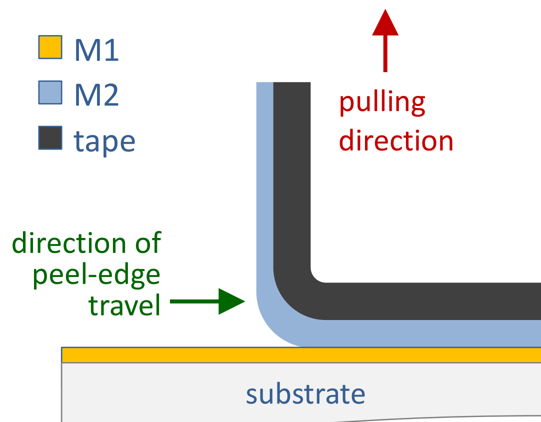

Figure 20: Peel testing of two different metals using PVC tape. The second metal (M2) is peeled off the first by applying an high adhesive tape to the surface of M2 and vertically peeling the tape away from the substrate. The substrate travels horizontally on a linear stage as the tape is pulled vertically by a linear actuator.

Figure 21 B shows peel curves of Au (M2) being detached from Al (M1) with and without a SAM barrier layer. With the SAM in place, the Au can be cleanly peeled from the ODPA coated Al, but without the SAM the Au cannot be peeled and remains in place. The forces recorded by the strain gauge show that the SAM is capable of reducing the adhesion between the two films, with the peak peeling force being reduced ten-fold from ~1.6 N without the ODPA monolayer to ~0.16 N with. Equivalent measurements using Al (M2) on top of Au (M1) yielded broadly similar results, with the peak peeling force being reduced from ~1.6 N without the ODT monolayer to ~0.35 N with (**Figure 22 B**), again demonstrating the effectiveness of the SAM in reducing adhesion between the films.

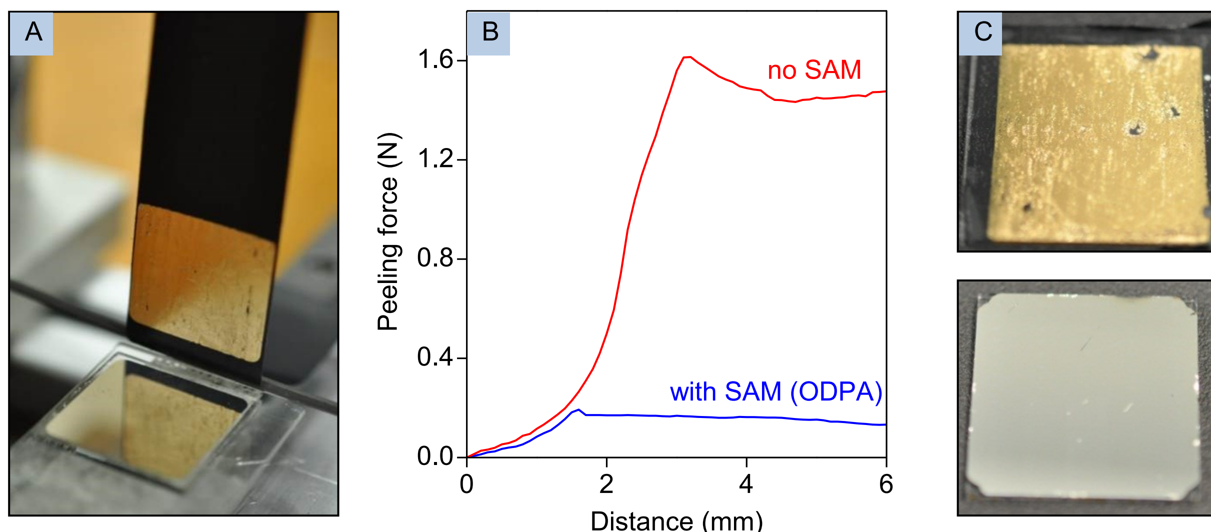

Figure 21: (A) Photograph showing Au being peeled from the surface of an ODPA coated Al glass slide. (B) Peel-curves for a layer of Au on top of a uniform layer of Al, with and without an intervening SAM layer of ODPA. The initial shallow response at low displacements corresponds to elimination of slack in the system, and is followed by a substantial increase in gradient as the tape stretches and its tension increases. Without ODPA the applied force peaks at a high value of ~1.6 N as peeling commences, before decreasing to a slightly lower steady-state value of ~1.4 N. With ODPA the applied force peaks at a much lower value of ~ 0.2 N when peeling commences before falling to a steady state value of ~ 0.15 N. (The slight overshoot in peeling force in each case indicates that the force required to propagate peeling is slightly lower than that required to initiate peeling). (C) Photograph showing the reverse side of the PVC tape after peeling (top) and the Al film after peeling has occurred (bottom).

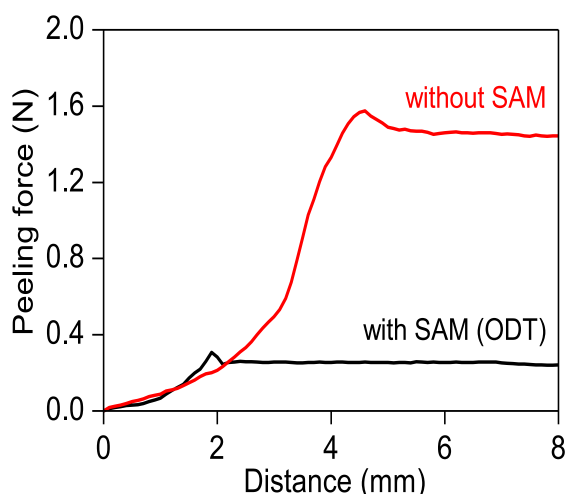

Figure 22: Peel-curves for a layer of Al on top of a uniform layer of Au, with and without an intervening SAM layer of ODT. The initial shallow response at low displacements corresponds to elimination of slack in the system, and is followed by a substantial increase in gradient as the tape stretches and its tension increases. Without ODT the applied force peaks at a high value of ~1.6 N as peeling commences, before decreasing to a slightly lower steady-state value of ~1.5 N. With ODT the applied force peaks at a much lower value of ~ 0.35 N when peeling commences before falling to a steady state value of ~ 0.2 N.

In practice the insulation tape cannot make truly conformal contact with the *entire* underlying surface, and consequently it is not always possible to completely remove the unwanted parts of M2 in a single peeling step. In these circumstances a second (or occasionally third) peeling step is required to remove the residual material. It is likely that imperfect SAM coverage, changes of surface topography of M1, or poor contact with the adhesive all combine to result in incomplete peeling. As such for further peeling experiments a solution-deposited glue was used in place of the tape (First Contact, Photonic Cleaning Technologies [32]). On drying the glue, forms a thin-film polymeric coating in intimate contact with the underlying surface (**Figure 23**). For the purpose of the peeling test the glue was applied uniformly to the surface of the M2 and allowed to dry before being peeled away.

Figure 23: Left: First Contact cleaning solution. Right, first contact being peeled from a glass slide. Images reproduced from [32].

For initial low resolution patterning tests, line patterns of M1 were deposited onto glass slides by shadow masking (**Figure 24),** the relevant low adhesion SAM was applied, and a uniform layer of M2 was deposited across the full area of the substrate. Adhesive tape or glue was applied uniformly to the surface of M2 and then pulled away from the substrate at 90° using the peel tester (V = 10 mm/s), with the peel-edge travelling in a direction perpendicular to the M1 lines.

The effect of switching from the adhesive tape to the solution-deposited glue is shown in **Figure 25**. When tape was used for peeling (blue line **Figure 25**) and when Al was used as M1, the strain gauge registered a low value of 0.2 N for the applied force whenever the peel-edge was located directly above one of the SAM-coated lines of Al.

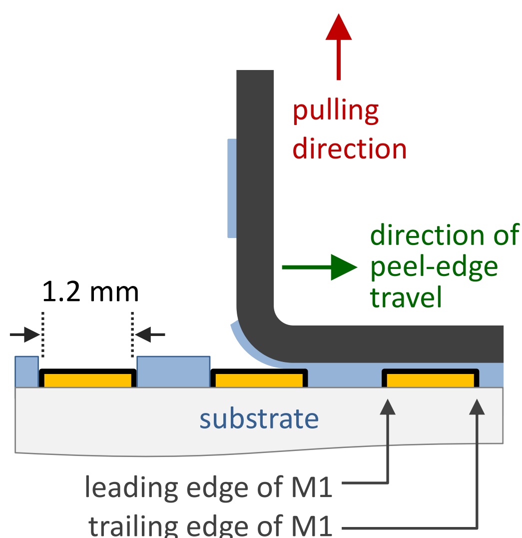

Figure 24: Peel testing of two different metals where the first metal (M1) is a simple line pattern. The second metal (M2) is peeled off the first by placing an adhesive tape or film on the surface of M2 and vertically peeling it away from the surface. The substrate travels horizontally on a linear stage as the tape is pulled vertically using a linear actuator.

A steady linear increase to ~1 N was recorded whenever the peel-edge passed into the region between the lines of M1, before falling back to ~0.2 N when the peel-edge reached the next SAM coated Al line (blue line **Figure 25**). When peeling occurred using the solution-coated glue (red line **Figure 25**) a similar peeling force value of 0.16 N was recorded when the peel edge was located above the Al lines. However, the behaviour in the region between lines was notably different, with the peeling force stabilising rapidly to ~0.35 N compared to the ~1 N value for the tape.

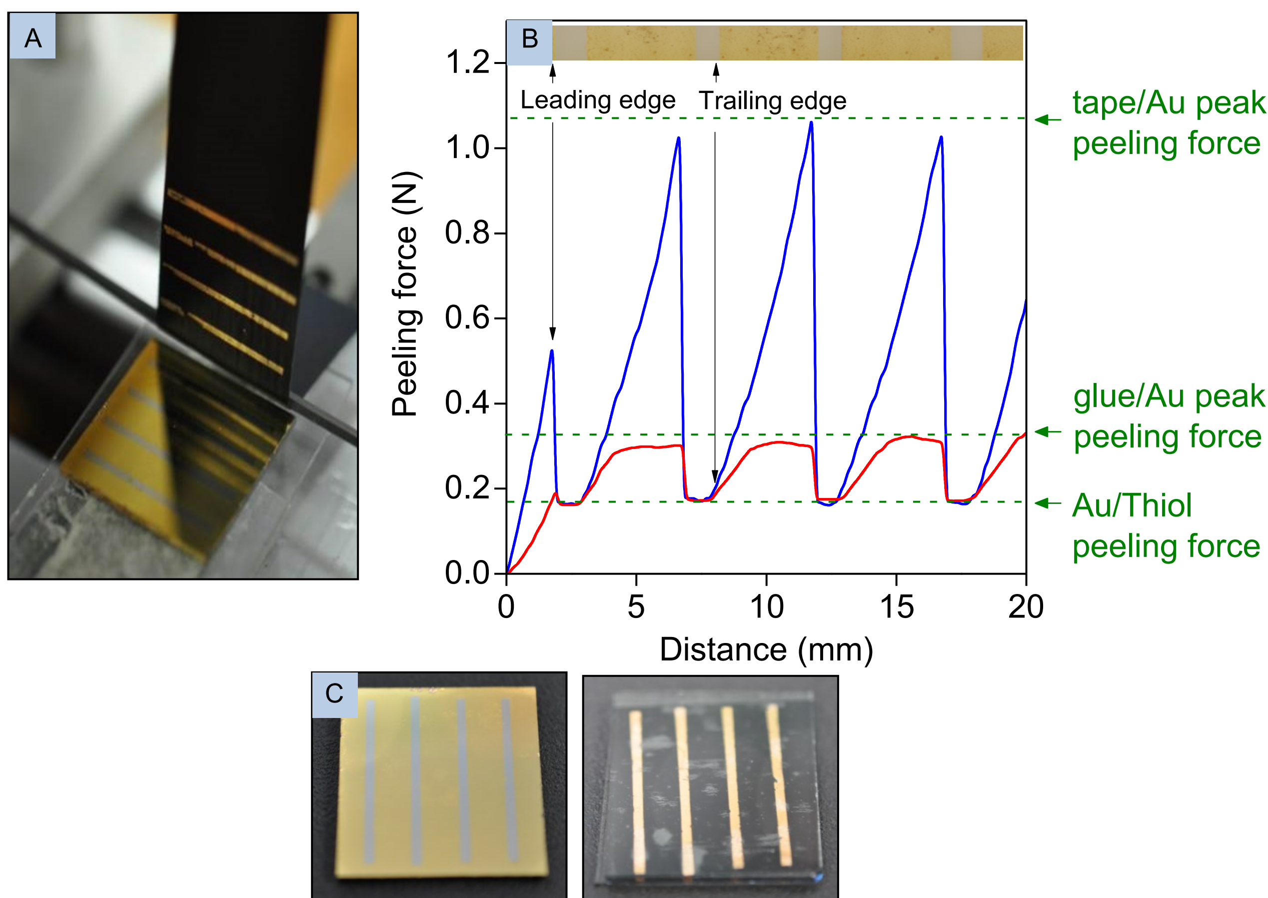

Figure 25: (A) Photograph showing the tape after peeling Au from an Al line array using the peel tester, with removed Au visible on the tape. (B) Peel curves for Au films on top of ODPA-coated Al line arrays, using insulation tape (blue line) or solution-coated glue (red line) as the adhesive layer. In the case of insulation tape a linear increase in the peeling force from ~0.2 N to ~1 N is observed as the peel-edge passes across the (Al-free) regions between lines due to simultaneous peeling and stiffening of the tape, followed by a rapid decrease back to ~0.16 N as the peel-edge passes onto the ODPA-coated Al. In the case of solution-coated glue, a similar (~0.16 N) value of the peeling force is observed when the peel edge is located above the Al lines but the behaviour in the region between lines is notably different, with the peeling force stabilising rapidly to ~0.35 N. The smaller peeling force differential between the Al and Al-free regions is beneficial for achieving controlled peeling. (C) A photograph of the final patterned structure along with the reversed side of the peeling tape (stuck to a glass slide).

The maximum peel force of the tape (~1 N) was 5 times higher than that for the solution processed glue. This lower peeling force will result in a lower peeling being exerted on M2 when peeling which may reducing the fracturing force at the interface of M1 and M2, such that at the interface between the two metals fracturing will occur more

favourably with less premature fracturing. Reversing the structure (Au as M1, and Al as the top layer of metal M2) yielded broadly similar results, with the strain gauge registering a low value of ~0.25 N for both the PVC tape and solution deposited glue rising to ~1 N for the PVC tape and ~0.35 N solution processed glue (**Figure 26**).

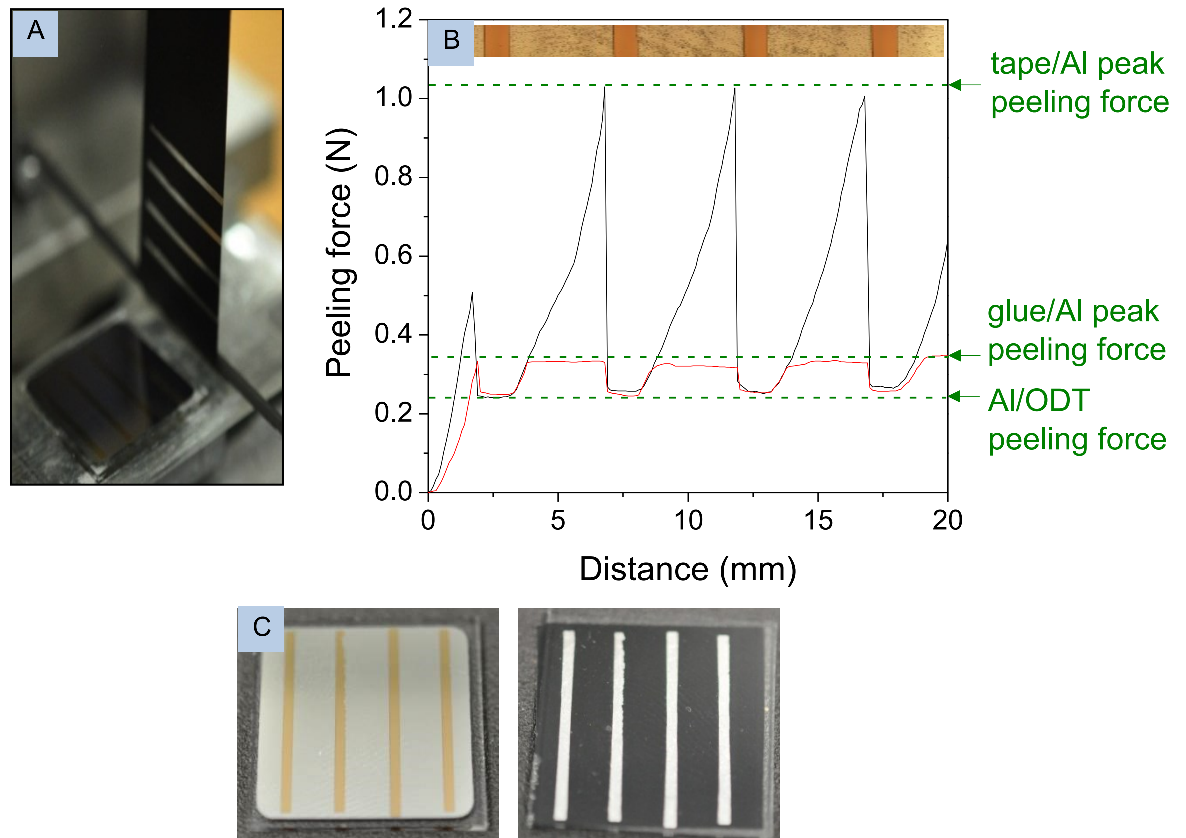

Figure 26: (A) Photograph showing the tape after peeling Al from an Au line array on the peel tester, with the removed Al visible on the tape. (B) Peel curves for Al films on top of ODT-coated Au line arrays, using insulation tape (black line) or solution-coated glue (red line) as the adhesive layer. In the case of insulation tape a linear increase in the peeling force from ~0.25 N to ~1 N is observed as the peel-edge passes across the (Au-free) regions between lines due to simultaneous peeling and stiffening of the tape, followed by a rapid decrease back to ~0.25 N as the peel-edge passes onto the ODT-coated Au. In the case of solution-coated glue a similar value of the peeling force is observed when the peel edge is located above the Au lines, but the behaviour in the region between lines is notably different, with the peeling force stabilising rapidly to ~0.35 N. The smaller peeling force differential between the Au and Au-free regions obtained using the glue is beneficial for achieving controlled peeling. (C) A photograph of the final patterned structure along with the reversed side of the peeling tape (stuck to a glass slide).

In both cases the behaviour is consistent with peeling of M2 occurring at the weakly adhered SAM/M2 interface whenever the tape was located above M1 and no peeling occurring at the strongly adhered M2/substrate interface. This interpretation was confirmed visually by inspecting the underside of the tape after peeling, which showed lines of peeled M2 that mirrored the original line pattern of M1 (**Figure 25 D)**.

High resolution microscope images of a peeled line scan where M1 is Au and M2 is Al are shown in **Figure 27** after peeling has occurred using tape. It is clear that the Al has been almost completely peeled from the ODT coated line pattern such that the M1 and M2 sit side by side. In addition the residue adhesive on the tape can be clearly seen on the Al, but not the Au confirming peeling has taken place.

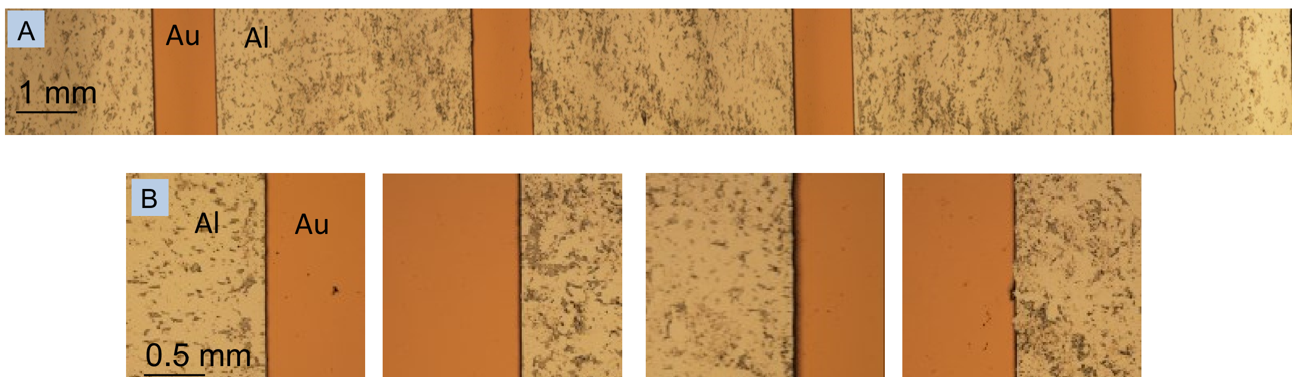

Figure 27: High resolution microscope images of the peeled pattern seen in **Figure 26** after being peeled using tape. The Al regions have residue glue from the tape on its surface, while the Au shows that the Al has completely been detached from its surface. The two metals sit side by side with some regions on the edge of the Au line not fully peeled.

The fidelity of the peeling process depends on several factors including: the topographies of M1 and M2; the relative adhesive forces between the various layers; the direction of peeling; and the tackiness and elasticity of the adhesive layer. For complete and accurate patterning M2, must fracture sharply at the leading edge (see **Figure 25 A**

for location of leading and trailing edge) of M1 (allowing M2 to detach from the SAM), peel in a continuous strip until the trailing edge of M1 is reached, and then fracture sharply again (allowing M2 to remain attached to the substrate). As such the forces generated at the leading and trailing edges of the line pattern – which in general can differ significantly – have a strong influence on the patterning resolution. In particular, excessively strong peeling forces on approach to the leading edge of M1 can cause premature fracturing of M2 on the substrate, while excessively weak peeling forces on leaving the trailing edge can cause delayed or failed fracturing of M2 on the tape – both cases resulting in deterioration of the patterning resolution. While the glue and adhesive tape provided similar forces of ~0.25 N on leaving the trailing edge, the glue provided a much smaller force on approaching the leading edge of ~0.35 N (compared with ~1 N for the adhesive tape), making it the more appropriate choice when high resolution patterning is required.

4.3 Adhesive fracture mechanics

Having obtained an understanding of the peeling parameters which govern adhesive patterning, more complex and closely packed patterning was attempted to demonstrate the viability of adhesion lithography. Alternating concentric patterns of dissimilar metals (Au and Al) were fabricated, with the objective of achieving nano-scale separations between the two metals – a challenging task that is difficult to achieve using conventional patterning methods [33]. The pattern design, shown in **Figure 28** compromised 50 concentric squares per 2 x 2 cm glass substrate.

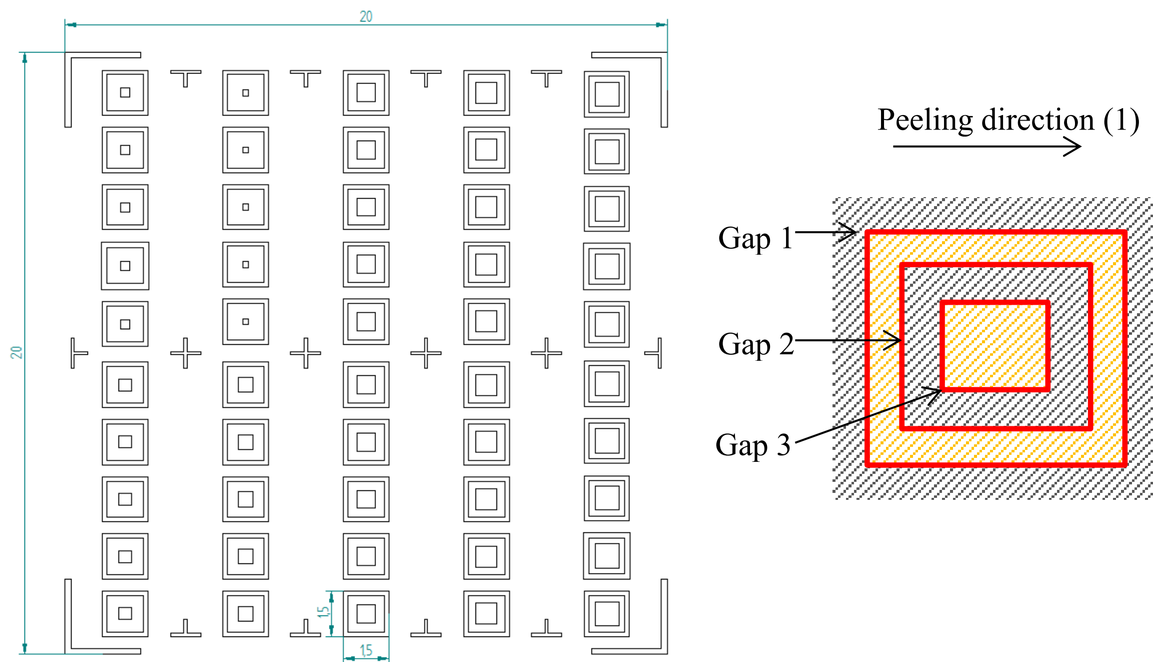

Figure 28: Computer aided design model of fifty concentric squares on a 2 x 2 cm substrate. Each square is produced in a range of sizes allowing different outer perimeters of M1 and M2. The design is capable of working in either a positive or negative configuration.

Each square was patterned using photolithography rather than shadow masking to ensure a good quality edge profile, along which peeling could occur (**Figure 29**).

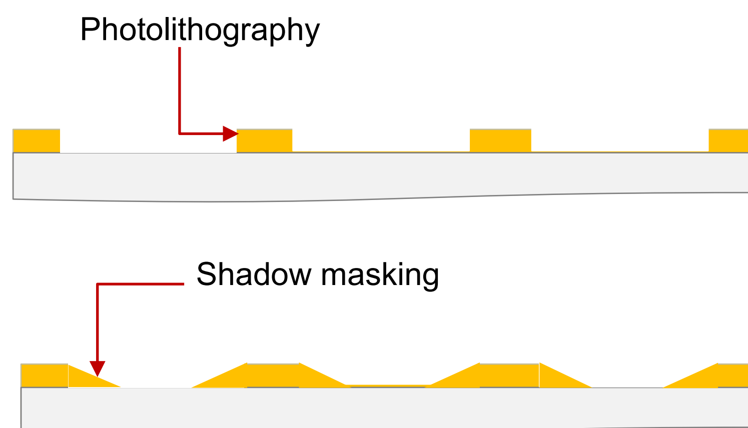

Figure 29: When a feature is defined using photolithography the edge profile is typically vertically with respects to the substrate, resulting in a well-defined edge along which peeling can occur. In contrast shadow masking tends to produce a sloped edge resulting in poorly defined and uneven electrode.

The general procedure to prepare structures is depicted in **Figure 30**. Initially a uniform layer of M1 is deposited (in this case Al was used as M1) on a glass slide, and then defining a concentric “square-ring in square-ring” pattern using either lift-off or etching methods (**A**) (See photo in **Figure 31** for this configuration). Next, a monolayer of ODPA was applied to M1 by immersing the substrate in a solution of the relevant SAM for 24 hours, before a uniform layer of M2 (in this case Au) was deposited across the full area of the substrate (**B**). Either tape or glue was then applied on top of M2 such that it covered the entire film (**C**) before being peeled away and in the process removing the low adhesion areas of the film which do not remain adhered to the substrate (**D**). Since Al was used as M1 the glass slide was first coated with a 2 µm layer of BCB.

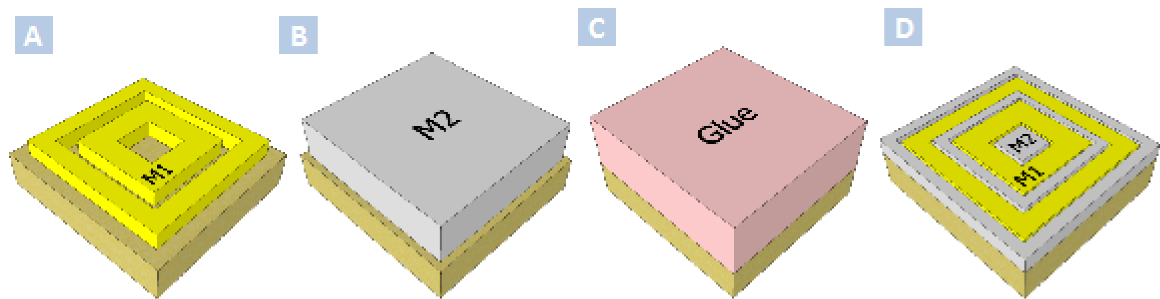

Figure 30: Schematic illustrating the procedure for the fabricating aligned concentric squares of Al with a central square of Au, involving: (A) deposition of Al (M1) in a “square-ring in square-ring” geometry, followed by treatment with ODPA; (B) deposition of a uniform layer of Au (M2) on top of the patterned Al and the exposed substrate; (C) application of solution-deposited glue across the entire surface of the Au; (D) removal of the glue to peel away the unwanted parts of Au (i.e. those lying above Al), leaving behind an in-plane concentric arrangement of Al and Au

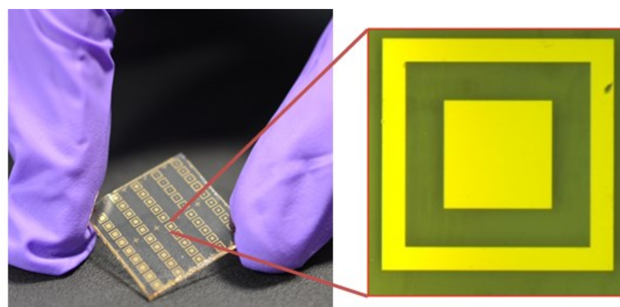

Figure 31: Photograph of a 2 x 2 cm glass slide after M1 has been patterned; enlarged region shows a microscope image of the final pattern. The dimensions of each square differ across the substrate providing different perimeter ratios of the final configuration of M1 and M2. The outer dimensions of the square shown are 0.5 x 0.5 cm.

Initial patterning with PVC did not result in the formation of closely aligned concentric squares for the reasons discussed previously. The critical factor to successfully removing M2 from M1 is correctly matching the peeling and adhesion forces acting on M1 and M2 together with forming a well-defined SAM adhesion barrier on the surface of M1. When these two factors were only partially met it was possible to remove M2 from M1, but in the process M2 was also removed from the BCB-coated substrate on areas of the substrate where it should have remained had patterning been completed fully. The importance of correctly annealing BCB after Au deposition is critical to the ADL process: without annealing Au is easily removed from the BCB, but with adequate annealing of the BCB, the Au remained attached to the BCB after the peeling procedure. This is demonstrated in **Figure 32** where temperature ramping of the BCB film after deposition of M2 was found to improve the peeling process. When curing of the BCB film occurred before deposition of M2 peeling largely failed, with large proportions of M2 becoming detached from the BCB –coated substrate (**Figure 32 Right**).

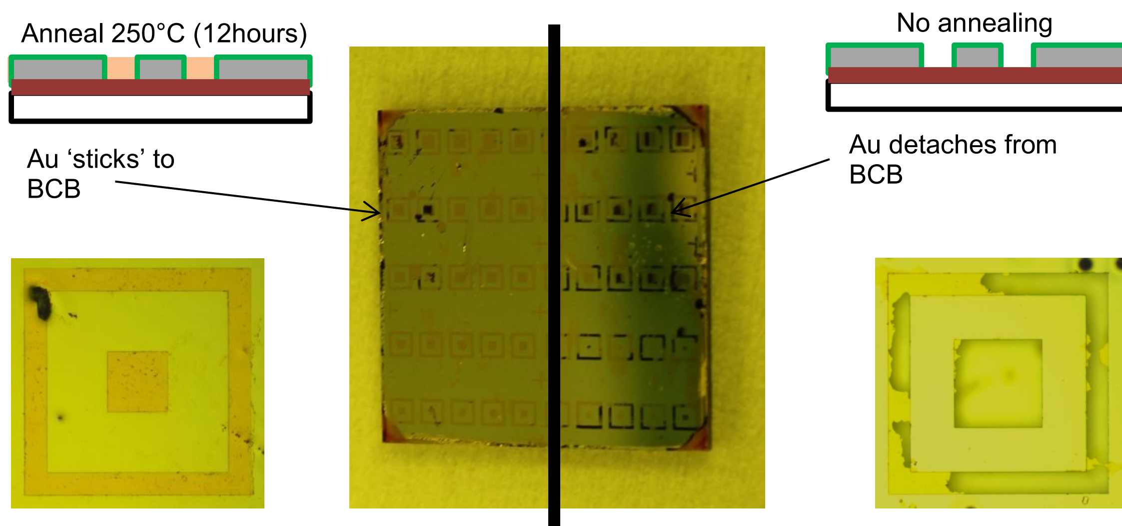

Figure 32: Right: when the BCB is not annealed, or annealed insufficiently, the Au detaches easily from the substrate during peeling leaving sparse regions of Au attached to the substrate. Left: When correctly annealed, specifically with a temperature ramp over several hours the adhesion of the Au to the substrate is greatly enhanced such that success patterning occurs.

When annealing occurred after deposition of M2 peeling is successful and M2 remains adhered to the BCB-coated substrate (**Figure 32 Left**). On the improperly cured BCB substrate it is clear that M2 was removed in relation to the peeling direction (**Figure 33**). In this case M2 fractures at the trailing edge of M1 where it becomes detached from the BCB-coated substrate. For M2 to successfully peel it must fracture at the leading edge of M1 which requires the fracture force of M2 to be less than the adhesion of M2 to the BCB-coated substrate. By annealing the BCB film after deposition of M2, the adhesion of M2 to the BCB is increased beyond the fracture toughness M2 and successful peeling is possible.

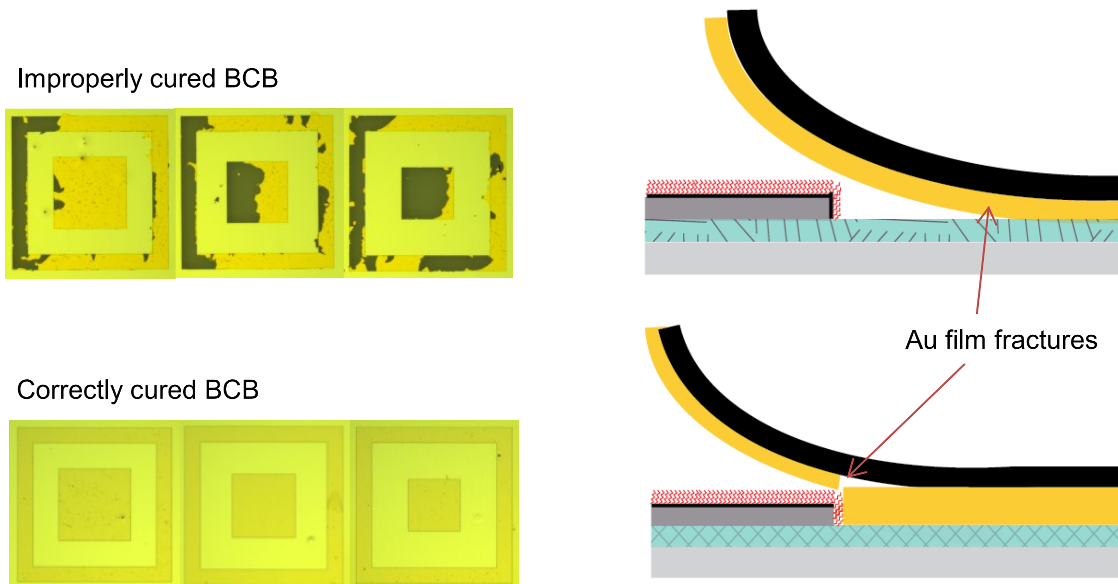

Figure 33: Left: microscope images of patterned electrode on partially and fully cured BCB. Right: Schematic representing how the adhesion force of the tape initially overcomes the adhesion force of the low adhesion substrate (top) before the Au film eventually fractures and breaks, resulting in poor patterning resolution. The "pull-off" effect changes with the tape peeling direction against the low adhesion SAM. When the substrate adhesion is in excess of the peeling force, M2 is peeled from M1 at the interface of the SAM.

Following successful patterning, an alternating concentric arrangement of the two metals was obtained comprising an inner square of Au and an outer square of Al on the BCB-coated glass substrate in exact alignment. Micrographs at each stage in the

fabrication procedure are shown in **Figure 34 A - C**. The removed Au can be seen on the reverse side of the tape in **D**. As was the case for the line patterns (**Figure 27**) adhesive can be seen on the surface of M2, confirming the tape was in contact with all areas of M2 during peeling and that M2, was able to withstand the peeling force of the tape. In the final configuration three discrete gaps are formed between M1 and M2, allowing multiple electronic devices to be fabricated within a single structure. The final configuration of the patterned films comprised three nano-gaps (G1, G2 and G3) with each gap enabling the fabrication of an independent isolated electronic device.

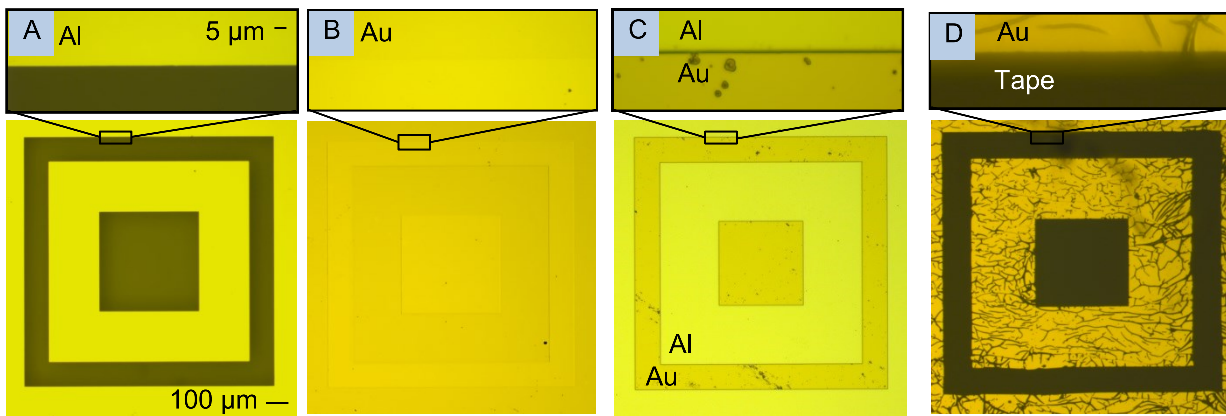

Figure 34: Micrographs of the three stages of fabrication of the ADL process, with the reverse side of the peeling tape show in the final image. (A) Patterned Al features are defined on a partially cured BCB film using standard photo-lithography. A low adhesion SAM, ODPA, is deposited onto the Al. (B) Au is thermally evaporated over the entire film. The adhesion of the Au is then selectively enhanced on the substrate by completely curing the BCB via thermal annealing. An adhesive tape is placed on top of the non-patterned Au film and peeled back (C). Providing the adhesion of the sticky tape / glue is greater than the adhesion of the Au-SAM and also lower than the adhesion between the Au and BCB, the Au is selectively removed from above the SAM - as shown in (D).

To evaluate the size of the gap between M1 and M2, AFM images were recorded at the interface between the two metals. **Figure 35** shows that the two metals are tightly meshed at the interface. The two metals can be clearly distinguished by their differing granular structures. To determine the separation of the two films, profile line scans of both the phase and topography images were recorded and are presented

alongside the AFM micrographs. The separation of the two metals is evident as a change in height can be seen. The topography scan shows a more gradual "fall-off" of at the edge of the interface, while the phase, (which represents the "stickiness" of a material) shows a more pronounced drop. The FWHMs of the topography scans are 59 and 62 nm respectively, but due to the nature of how AFM images are recorded and the difficulty of resolving a sharp change in topography a poor estimate of the gap width is inevitably obtained. Imaging using an SEM is a better method of determining gap size on the nanoscale.

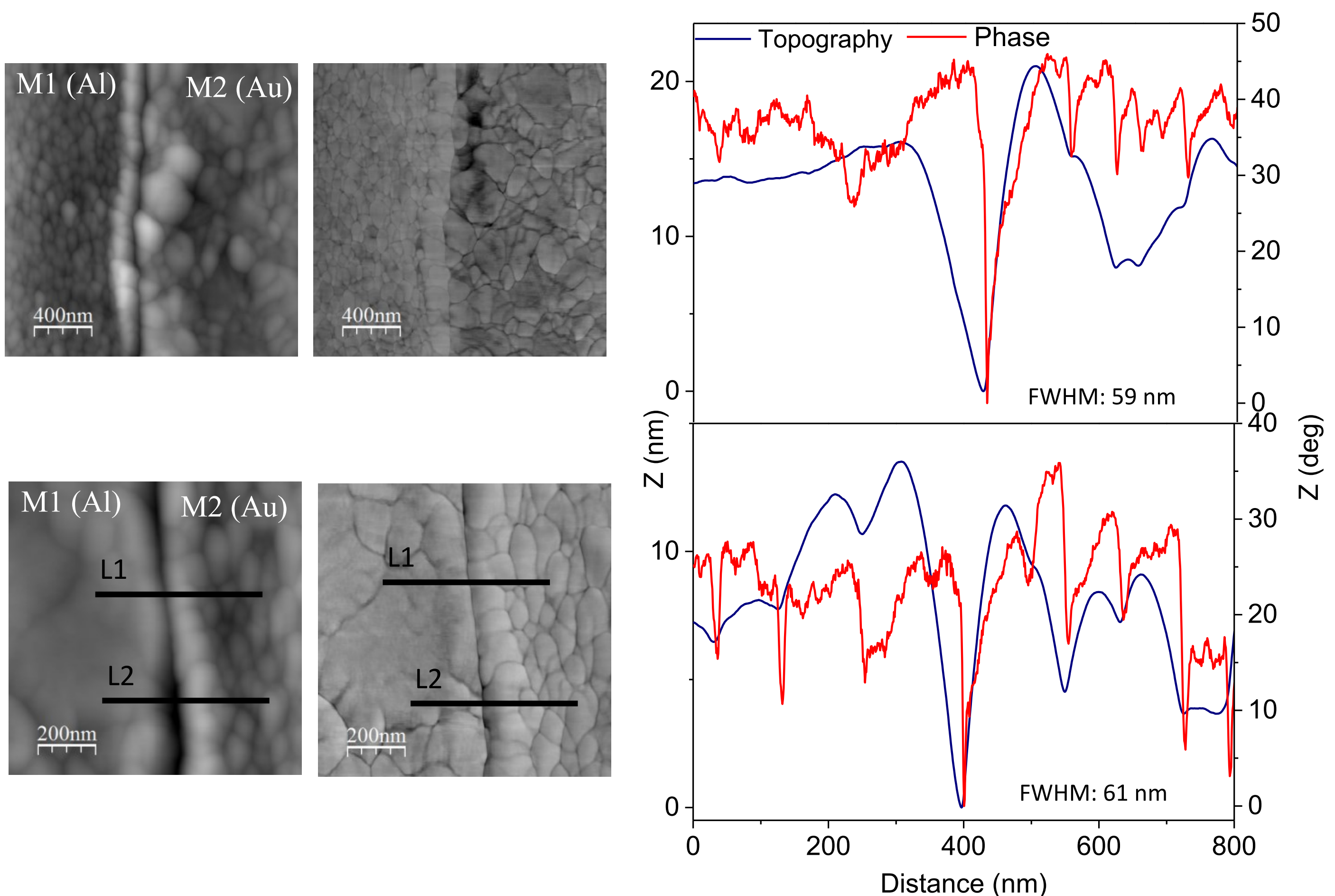

Figure 35: Left: AFM topography and phase images of the gap between M1 and M2. The presence of two different materials can be clearly seen from the different grain structures. The two materials mesh closely at the interface resulting in a nano-scale separation between the films. Right: topographical line scans of two lines (L1 and L2) on the AFM phase and topography images. The gap between the two films is represented by a "fall-off" on the Z scale of each scan. The FWHMs are 61 and 59 nm respectively.

Cross sectional SEM (CS SEM) micrographs taken at the interface between M1 and M2 using the same configuration of M1 and M2 described above are displayed in **Figure 36**. The CS SEM clearly shows two separate metals (M1 and M2), in close alignment as expected. While the AFM scans suggested a ~60 nm gap, the SEM suggests a larger gap around 150 nm.

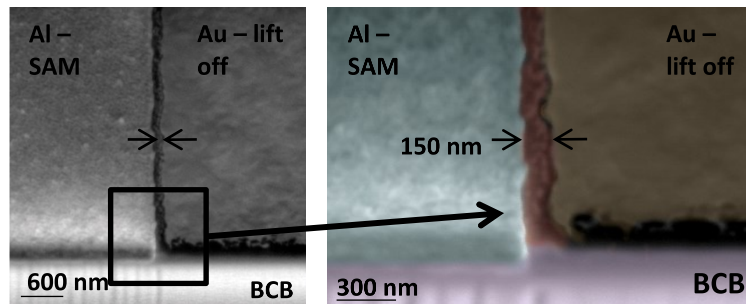

Figure 36: CS SEM cross section images of the gap of the same electrode showing a sub 150 nm gap between the two electrodes. The cross section was taken at the interface between M1 and M2 by iron milling into the film.

SEM is a more reliable method to determine nanoscale gap widths compared to AFM as it does not suffer from variations in tip shape and feedback errors which are commonly associated with AFM imaging. In reality, to correctly determine the gap size, a much larger area from AFM would need to be investigated as localised sections may be subject to differing adhesion forces (resulting in alternative fracturing geometries throughout over the edge profile). However these images give a good indication that the two electrodes are separated on the ~100 nm length scale.

Control samples were fabricated with no SAM interlayer to confirm patterning was a consequence of the inclusion of the low adhesion SAM between M1 and M2. Without the SAM, peeling would either fail or result in uncontrolled removal of M1

from the substrate depending on the number of times the peeling action was performed (**Figure 37**).

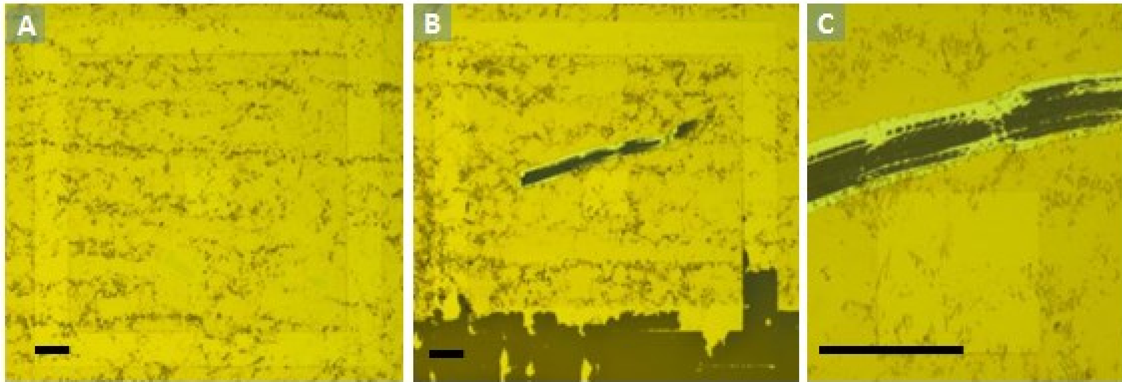

Figure 37: (A) Failed peeling using PVC tape. (B) Occasionally M1 became detached from the substrate. (C) Magnification of a scratch on (B). Both M1 and M2 are clearly visible in the scratch area confirming both metals are deposited and do not normally peel apart. Scale bar 100 µm.

4.4 High-resolution adhesive patterning

As discussed earlier in this chapter, low adhesion solution processed glue lowers the adhesion forces present during peeling compared to PVC tape. To further develop the ADL method, low adhesion glue was used for patterning. The fabrication process was similar to that using the PVC tape except the glue was peeled off the substrate using tweezers after it had dried.

Figure 38 shows photographs outlining the process of fabricating the final ADL structure using adhesive glue. The glue is applied to the substrate using a brush (an outline of M1 can be seen under M2 owing to the semi-transparent nature of the thin

film of M2). As the glue is peeled off, the concentric pattern of the two electrodes is clearly visible. Using the adhesive glue allows for more controllable peeling owing to the closer matched adhesion forces of the glue compared to the adhesive tape at the SAM-M2 interface.

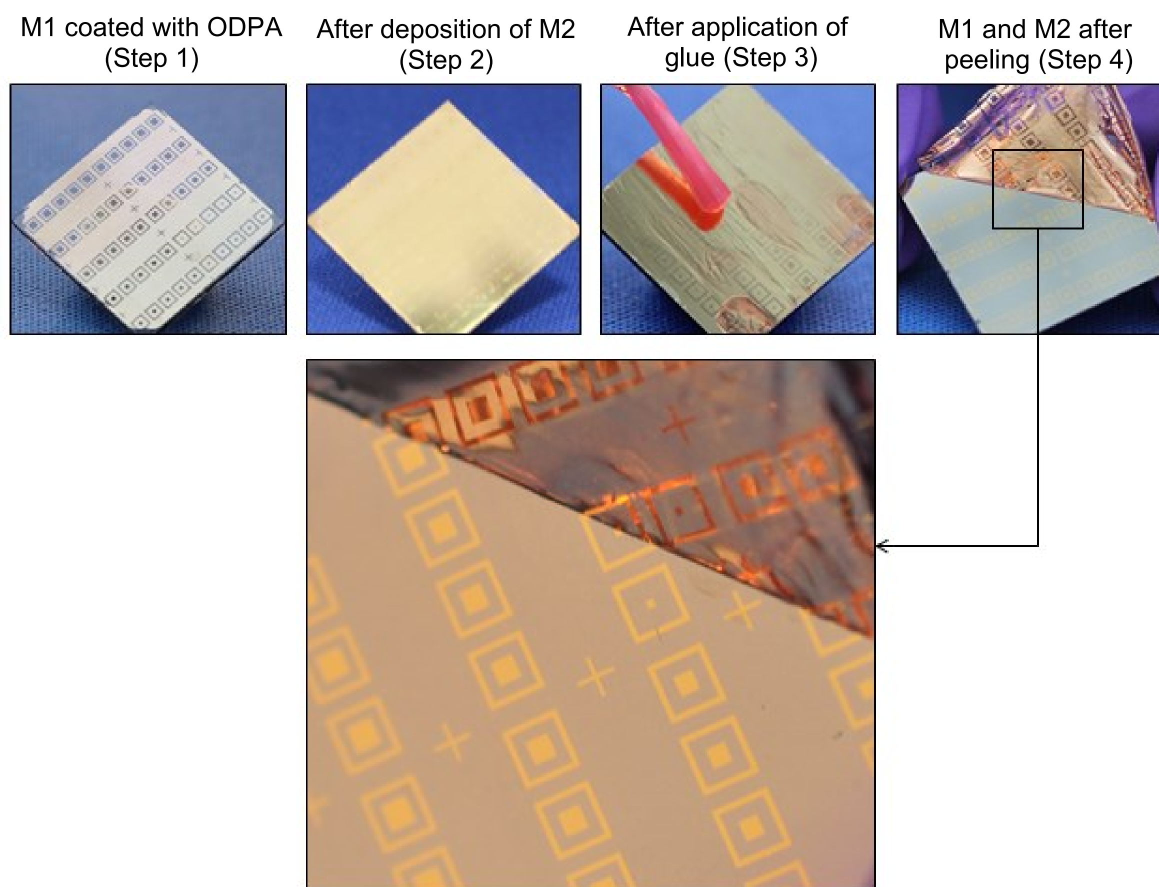

Figure 38: Photographs of the same four processing steps outlined in **Figure 30**, with adhesive glue being applied to the surface of M2 and peeled off to reveal the patterned structure.

The final configuration of the pattern along with the reverse side of the glue (with the low adhesion areas of M2 attached) is shown in **Figure 39**. On close visual inspection, the definition of the concentric squares appears excellent with no visible voids or gaps at any point along the perimeter of the pattern. Unlike the PVC tape no residue was left on the surface and typically only one peeling action was required due to the intimate contact the glue makes with the substrate as it dries.

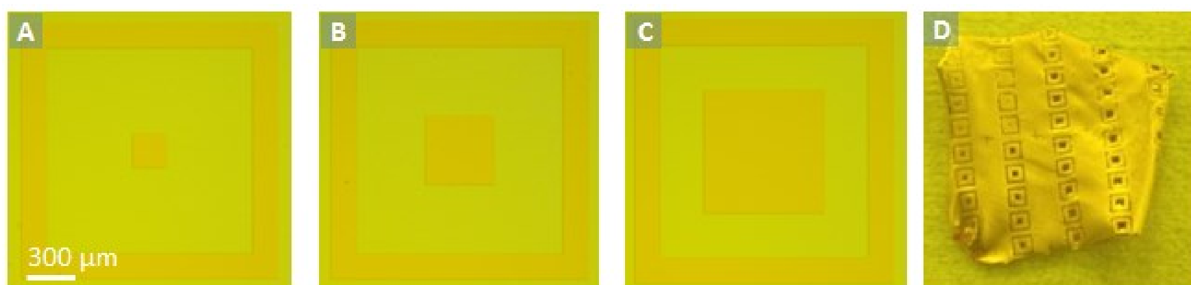

Figure 39: (A,B,C) examples of the concentric pattern produced using adhesion lithography where M1 is Al and M2 is Au. (D) The reverse side of the adhesive tape after peeling. The low adhesion areas of M2 transfer to the glue, producing a negative of the original patterned film.

Further AFM imaging performed after deposition of M2 on several areas of the film revealed a highly oriented macroscopically continuous grain boundary within M2 directly above the edge of M1 in both the topography and phase images (**Figure 40**). This pre-formed boundary (crack) is a consequence of the differing surface energies of the hydrophilic substrate and hydrophobic SAM-coated surface of M1. During peeling fracture occurs along the inter-granular interface between the two metals, with M2 fracturing close to the interface of the SAM. It is the presence of this pre-formed crack that enables the fabrication of highly aligned discrete features. The fracturing forces at the inter-granular boundary are weak compared to the bulk film, resulting in a highly controllable process capable of yielding a much sharper tear than fracturing of a randomly polycrystalline film. In the absence of a macroscopically continuous grain boundary, tearing would instead need to occur via the formation of numerous intergranular and transgranular micro-cracks in the region of the applied stress close to the interface of M1 and M2. The final tear would occur when the cracks were sufficient in number and size to coalesce into a contiguous fracture boundary. Owing to the distributed nature of the constituent micro-cracks, the result would be a much rougher break that would not follow the boundaries of M1 as closely.

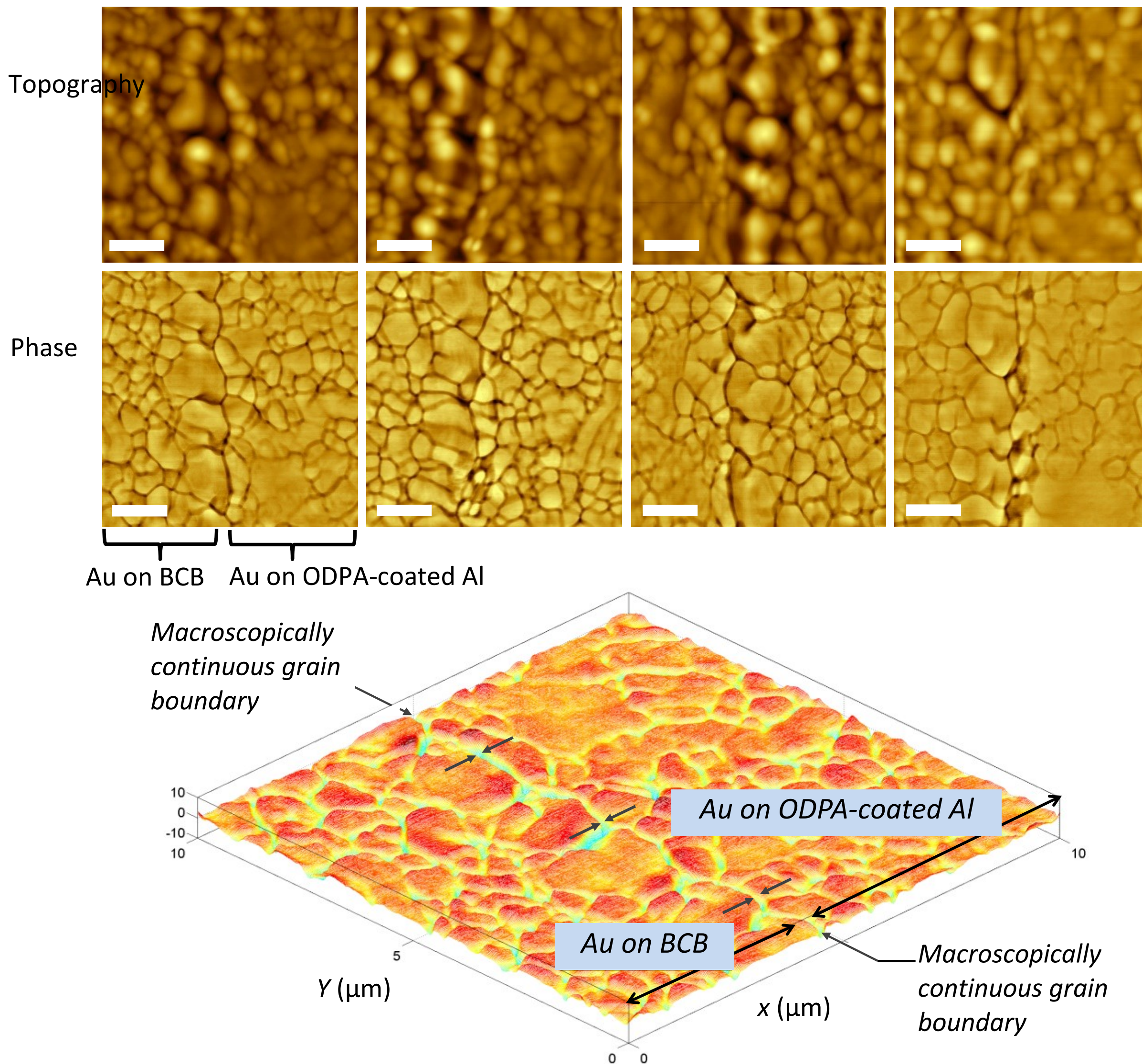

Figure 40: Top: Topography and phase AFM images of the interface between M1 and M2 at 4 different positions across the substrate - scale bar represents 100 nm. Bottom: Three dimensional surface plot of an AFM phase image, representing the area between M1 and M2. The macroscopically continuous grain boundary in the Au surface is clearly visible at x ≈ 5 μm.

The granular growth and fracture of M2 is essential for the controllable fracture of M2. The resolution and uniformity of the fractured edge between M1 and M2 is, in part, governed by the granular growth and thus the method by which M2 is deposited. It may be possible to induce further granular growth along the boundaries of M2 via more controllable deposition techniques such as e-beam evaporation [34, 35]. Assuming other aspects of the peeling action are optimised (such as the adhesion of M2 to the substrate

and the formation of a well-defined peel edge), the final 'resolution' between the two films could be the spacing between the grains of M2 which are fractured during peeling. This could in principle be as small as just a few nanometres.

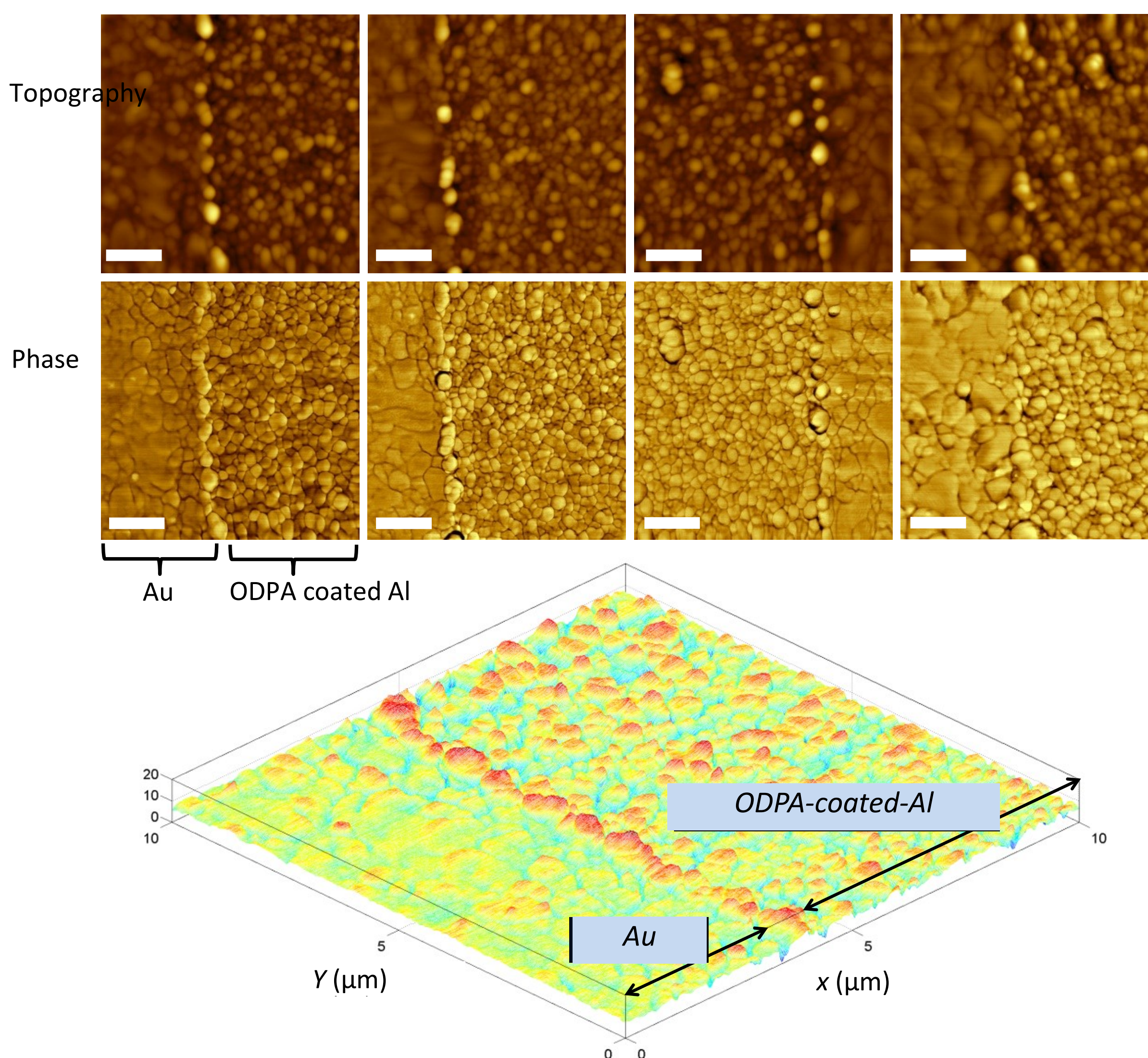

Figure 41: Top: Topography and phase AFM images of the interface between M1 and M2 at 4 different positions across the substrate - scale bar represents 100 nm. Bottom: three dimensional surface plot of the AFM phase image. M1 and M2 can be seen sitting in close proximity side-by-side on the substrate after peeling.

AFM images obtained after the peeling step (**Figure 41**) confirm the formation of a sharp interface between M1 and M2 with no obvious voids or gaps. As the size of the gap between M1 and M2 was not apparent from the above AFM data high resolution

scanning electron micrographs imaging (HR-SEM) was again used to determine the separation of the films (**Figure 42**). It is apparent from this data that the two films are not connected and peeling of M2 has occurred at the interface of M1. The images reveal a grain-like structure of the two metals and the formation of a tight intergranular boundary between them, along which the Au (M2) fractured during peeling. To evaluate the size of the gap between the two films analysis of ~2 μm section along the interface of M1 and M2 was performed indicated separations of 33 ± 7 nm at the leading edge of the Al (M1) and 12 ± 5 nm at the trailing edge (**Figure 43**).

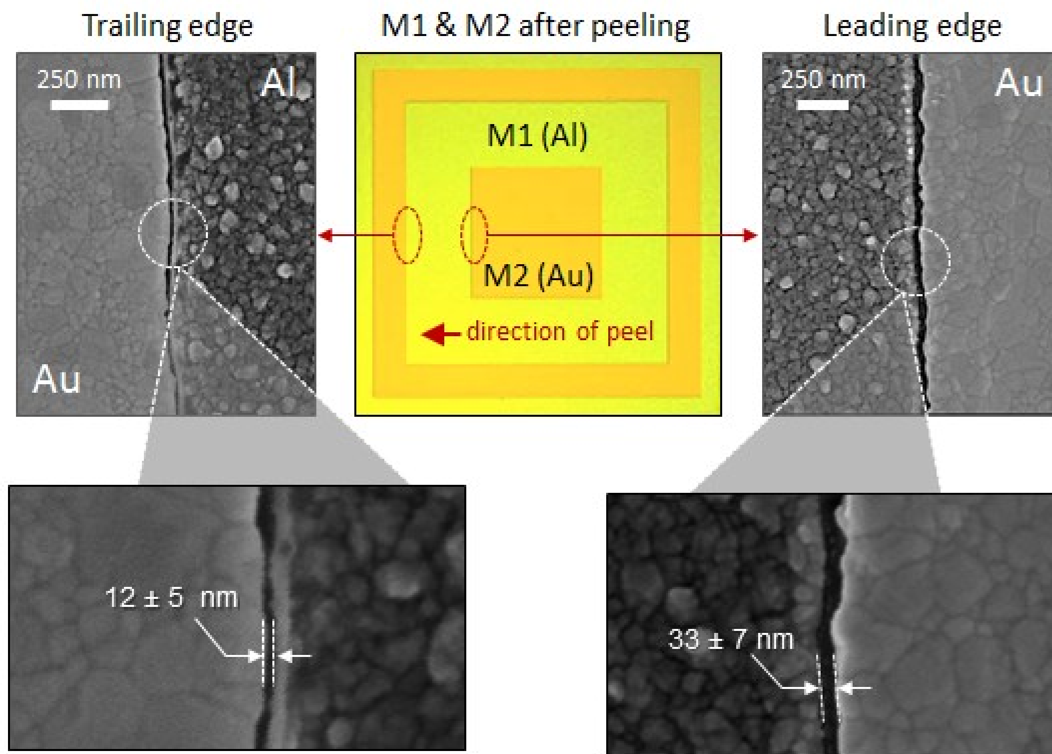

Figure 42: Micrograph of the concentric square electrode (where M1 is Al and M2 is Au) with associated SEM images of the Al/Au interface at the leading (right) and trailing (left) edges in relation to the direction of peeling.

By fabricating M1 using basic wet etching techniques, as opposed to dry etching or e-beam lithography, the peeling action occurs on a non-uniform edge profile; as such these values do not represent the ultimate resolution limit of ADL. Additionally, on

close examination of the trailing edge histogram includes a number of gap spacing's in the sub-4-nm range, indicating that the narrowest regions of the trailing edge nanogap are comparable in size to the SAM length.

The difference in gap widths at the leading and trailing edge is consistent with the previously discussed difference in peeling forces at the leading (0.35 N) and trailing edge (0.16 N). The higher the peeling force the greater the risk that, in addition to sharp cracking along the SAM-induced nanogap, diffuse cracking will also take place through the formation of intergranular and transgranular microcracks in the region of the applied stress. Owing to the inherently distributed nature of such microcracks, a broadening of the final electrode spacing is expected to result unless the peeling forces are more closely matched.

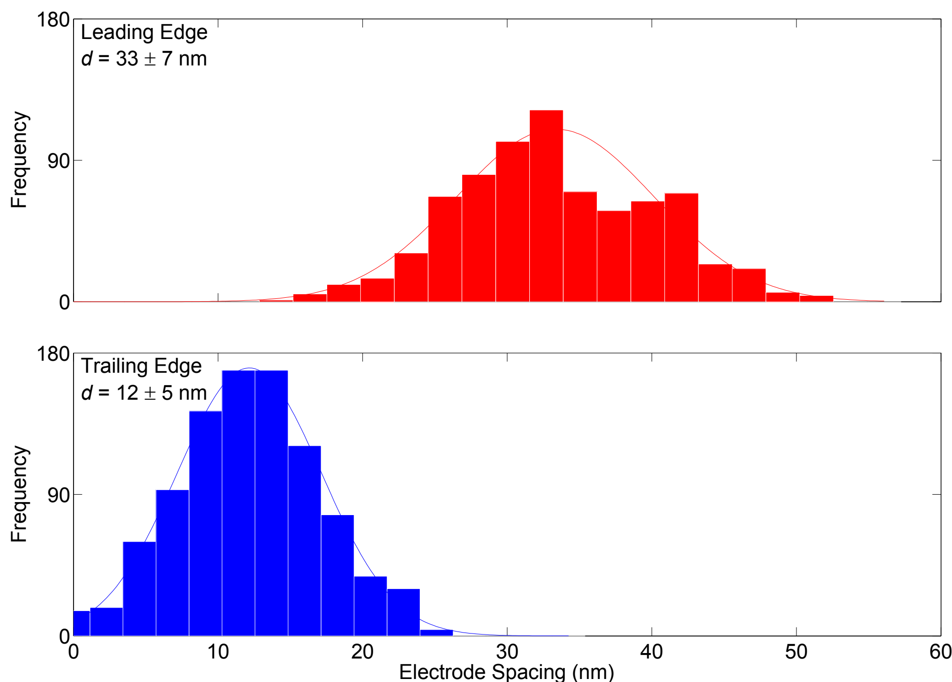

Figure 43: Histograms of measured nanogap spacing for concentric square Al/Au electrodes. Data was obtained at ~2.3 nm intervals along a ~2 μm measurement line at the leading- and trailing- edges. When peeling at the leading edge (a) gap spacing of 33 ± 7 nm is recorded, while peeling at the trailing edge (b) yields tighter spacing of 12 ± 5 nm.

The nanogap ADL pattern has an aspect ratio on the order of ~100,000 (10^{-3} m / 10^{-8} m) with small sub 15 nm separation of the two electrodes. This is smaller than many recent reports of more complex fabrication techniques, such as chemical lithography and controlled cracking which yield gap sizes of between 30 and 100 nm [36, 37]. It is striking that nano-scale alignment can be achieved even with coarsely patterned electrodes, thereby avoiding the need for high resolution e-beam or optical lithography at any point in the fabrication procedure.

4.4.1 ADL nano-devices

To confirm the suitability of ADL patterned electrodes for electronic devices, the SAM layer was removed by oxygen plasma leaving both M1 and M2 uncoated (ensuring the SAM does not act to insulate M1 from M2). By making electrical contact across G1, G2 and G3, sequential current-voltage sweeps from -1 to +1 V were performed with the resulting current recorded in a nitrogen controlled atmosphere using a Keithley 4200 semiconductor parameter analyser (SPA).

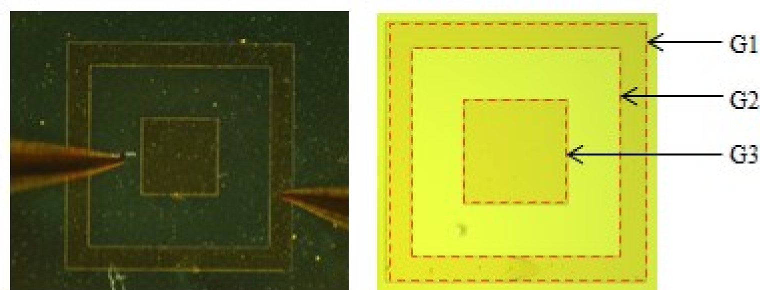

Figure 44: Left: Video camera microscope image of an ADL device under test. Right: Microscope showing the location of the three gaps formed by the ADL process.

For each junction tested, no current was recorded above the detection limit of the associated instrumentation (~10 pA), thus confirming the electrical isolation of the

electrodes around the complete perimeter of the square. After confirming the isolation of the electrodes, coplanar organic photodiodes were fabricated by depositing a donor/acceptor blend of poly(3-hexylthiophene) (P3HT) and C_{61}-butyric acid methyl ester (PCBM) [38] (in a blend ratio of 1:1) upon the substrate via spin coating. Before electrical contact was made across junctions G1, G2 and G3 with the resulting current-voltage characteristics recorded using a SPA (where forward bias corresponded to Au being biased positively with respect to Al). To facilitate charge generation, the substrate was illuminated using white light. Despite the non-optimised architectures, a clear photovoltaic response under white light illumination was recorded from all three nano-junction across several devices tested (**Figure 45**). In addition, as the perimeter of the active nano-junction increased in length from 1.5 to 3 to 4 mm, a corresponding increase in the magnitude of the photocurrent was recorded. This simple device represents one of the few successfully reported examples of a coplanar nano-scale device fabricated using non-traditional fabrication techniques [39-41].

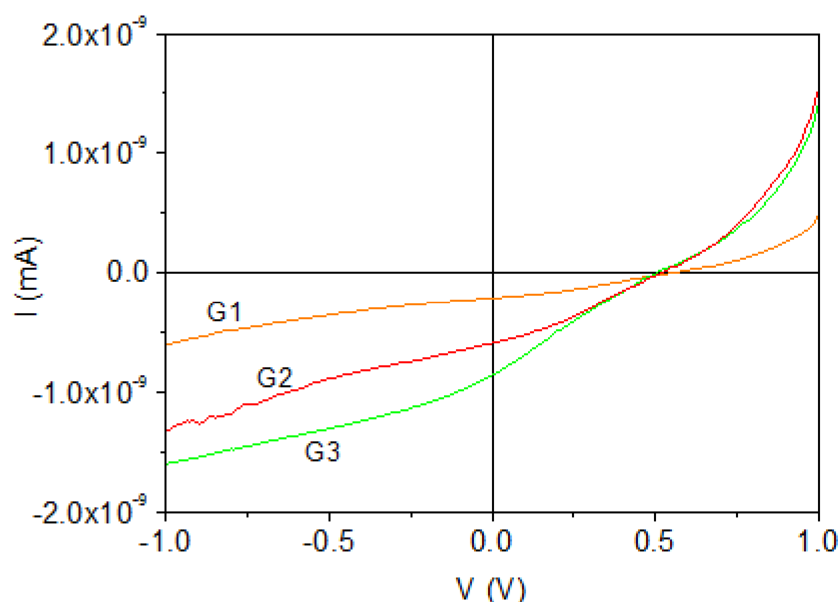

Figure 45: Current-Voltage (*I*-*V*) curves for photovoltaic devices fabricated using the ADL process (Al/P3HT:PCBM/Au). *I*-*V* measurements were recorded across three different Al/Au interfaces by making electrical contact at the positions denoted by G1, G2 and G3; forward bias corresponds to Au being biased positively with respect to Al.

Further transient current measurements performed under pulsed illumination using an ultra-bright 660 nm LED driven with a 50 ns pulse width by a wave function generator (TTI TG 4001), are presented in **Figure 46**. To ensure adequate current readings, the output current signal was amplified (Stanford Research SR570, 10 μA/V) with the associated current reading recorded on an oscilloscope (Tektronix TPS 2024). The output of a fast response time Si photodiode (DET100A, ThorLabs) was simultaneously recorded along with that of the ADL device. A clear photoresponse was recorded by the ADL photodiode with a maximum photocurrent rise time of ~ 300 ns for a 50 ns pulse, compared to ~ 40 ns for the fast Si photodiode (**Figure 46**). Further improvements in device performance should be expected upon incorporation of higher mobility photoactive semiconductors and through device architecture optimisation. However these results represent an important first demonstration of using ADL to fabricate functional nanoscale electrical devices.

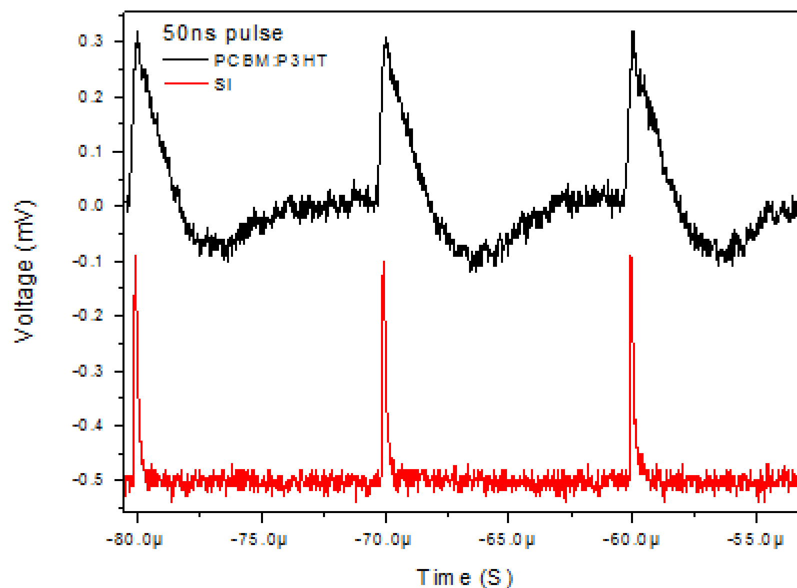

Figure 46: Black line: transient photocurrent of a PCBM:P3HT photodiode under ~1.2 mW/cm^2 pulsed excitation at 660 nm and an applied bias of – 2 V. The red line shows the simultaneous response from a Si photodiode.

4.4.2 Alternative configurations

The ADL technique may be applied to other combinations of SAMs and metal electrodes. In addition to using ODPA as an adhesion modifier, it has also been possible to fabricate structures using different metals and SAM combinations such as using Au for M1 and ODT as the adhesion modifier. For example, **Figure 47** shows the patterning of devices structures fabricated using Au as M1, Al as M2 and ODT as the low adhesion SAM. In this configuration M1 was negatively patterned, resulting in an inner concentric square formed from M1 and the outer square formed from M2.

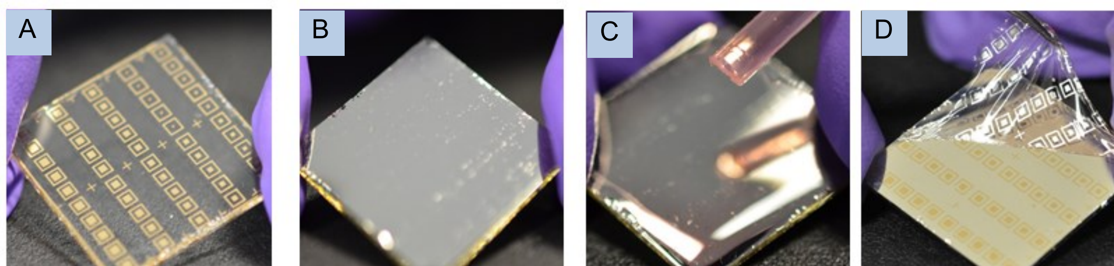

Figure 47: Photographs illustrating the procedure for the fabrication of aligned concentric squares of Al with a central square of Au where Au is M1, involving: (A) deposition of Cr-Au (M1) in a "square-ring in square-ring" geometry, followed by treatment with ODT; (B) deposition of a uniform layer of Al (M2) on top of the patterned Au and the exposed substrate; (C) application of solution-deposited glue across the entire surface of the Al; (D) removal of the glue to peel away unwanted parts of Al (i.e. those lying above Au), leaving behind an in-plane concentric arrangement of Al and Au.

4.5 Conclusion

The initial work in this chapter outlines the adhesion properties of several material systems and how applying different surface coatings and heat treatments can strongly affect how they behave. It was found the adhesion of a material can be strongly changed using simple surface modifications. In the case of a metal, this was accomplished using SAMs which were either hydrophobic or hydrophilic, while for polymers, such as BCB, heat treatment was found to alter the degree of cross-linking in the film, making the surface harder and less adhesive.

The work in the first half of this chapter was used to guide the procedure developed in the second half for the fabrication of highly aligned electrodes using adhesive forces. Unlike traditional methods of nano fabrication, which tend to be slow and expensive, the adhesion lithography method is quick and cheap to implement. The process works by controlling the underlying adhesion of two metal films such that the removal of one is possible with respects of the other when an adhesion modifier is applied between them. The gap, which was found to form between the films in the final configuration, was recorded to be as low as 12 ± 5 nm. Theoretically the gap could be reduced to as small as the height of the adhesion modifier applied – in this case just a few nanometers. Many factors were found to influence the success of the ADL process, including the substrate adhesion and leading and trailing edges of the peeled film. Peel testing confirmed the difference in peel forces can cause a localised difference in the size of the gap on either side of the initially patterned electrode. By more closely matching the peeling forces generated at interface of M1 and M2 using low adhesion solution deposited glue, highly controllable peeling was possible such that photodiodes

with nanoscale electrode spacing were fabricated using organic semiconductors confirming the method can produce working devices.

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5 Self-aligned transistors

For organic electronics to see widespread use improved fabrication methods are needed [1, 2]. Current solution processed organic semiconductors have been found to possess equivalent performance to their amorphous silicon counterparts in certain metrics such as mobility [3, 4]. In addition graphene has been shown to have an extremely high carrier mobility, far outweighing that of crystalline silicon [5, 6]. The theoretical advantageous manufacturing properties of organic semiconductors and graphene are not however enough to secure their use in future generations of electronics [7]. Before such technologies will see widespread adoption, greater progress will need to be made in fabrication technologies can make large-area electronics cost effective to produce [8, 9]. Such technologies must be capable of integration into existing fabrication facilities with minimum process change, while retaining the requirements for low-cost, large-area, flexible electronics manufacturing [10-12]. Previous attempts to develop new manufacturing techniques for large area electronics have often failed to match the need to retain compatibility with existing tools and techniques used to produce electronic components [1, 10, 13].

This section is focused on developing organic field effect transistors (OFETs) fabrication techniques capable of producing large area electronics, while also being compatible with traditional fabrication technologies such as photolithography. For this, study the negative-tone photoresist SU8 was investigated with the aim of developing

highly aligned transistors using a back illumination fabrication technique [14]. Additionally, to confirm the ability of the fabricated structures to be used in devices, the organic semiconductor C_{60} was tested using the newly fabricated architecture along with the high mobility semiconductor graphene.

5.1 SU8

SU8 is a negative-tone photoresist most commonly used for the manufacture of high aspect ratio MEMS devices [15]. Based on an epoxy, Epon SU-8, sold by Shell Chemicals, the use of SU8 as a photoresist was developed and patented at the IBM-Watson Research Centre using a triarylsulfonium hexafluorantimonium salt photo-acid generator (PAG) to induce strong photo-crosslinking via exposure to UV light (US Patent No.4882245) [16].

During exposure to ultraviolet light, the PAG decomposes resulting in the formation of hexafluoroantimonic acid which diffuses towards the SU8 monomer and subsequently opens the epoxy rings, resulting in cationic polymerisation wherever the acid is present [17]. The high number of epoxy rings per carbon chain results in the formation of covalent bonds once the photo-acid initiates crosslinking. The slow diffusion of the photo-acid within the film is the rate-limiting step when attempting to crosslink SU8 into dense films. As such the diffusion of the photo-acid to the nearby monomer is accelerated using a post-exposure bake (PEB) at a temperature above the polymer glass transition temperature (T_g=55°C) [18].

5.1.1 SU8 Processing parameters

General processing guidelines for SU8 are similar to most negative photoresists. SU8 adheres well to most substrates and forms stable and chemically inert films [19]. **Figure 1** depicts the typical processing steps undertaken when working with SU8 films.

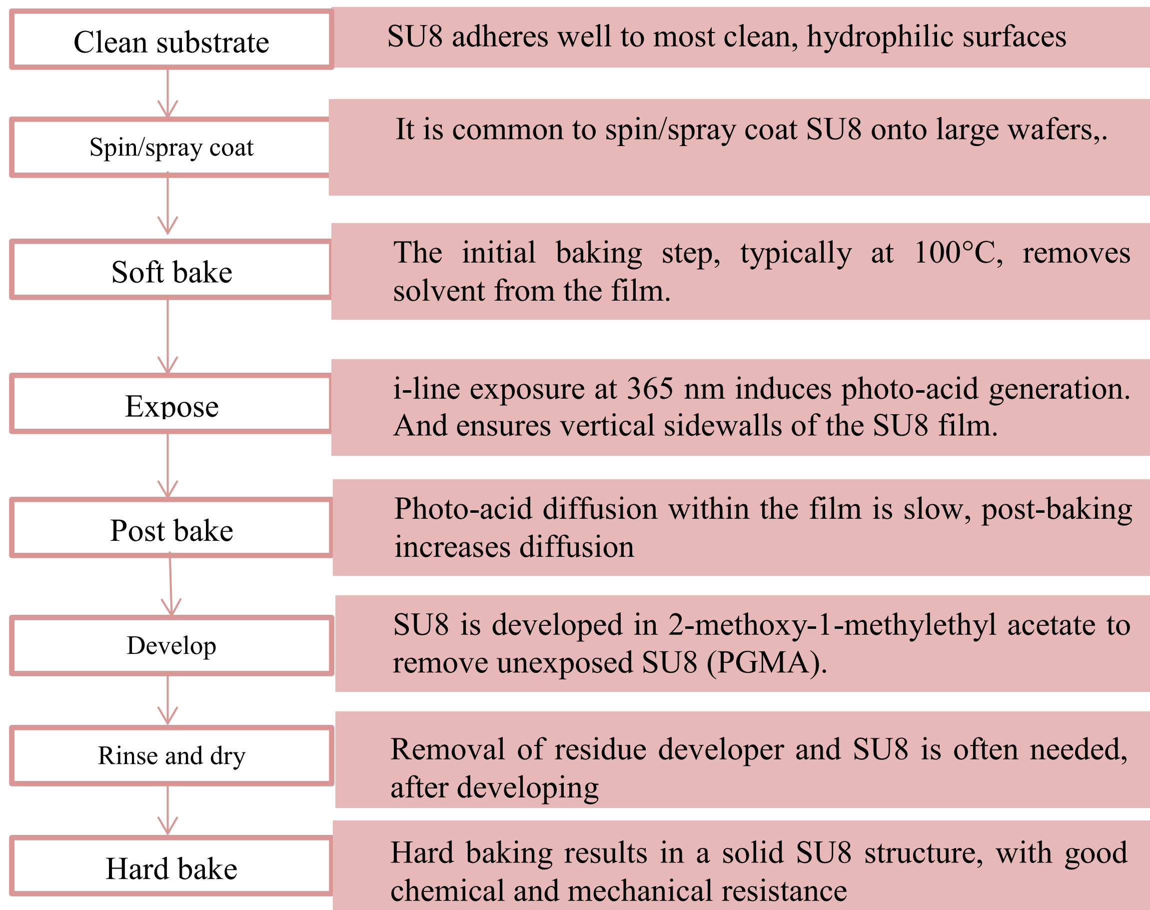


Figure 1: Outline of the SU8 fabrication process.

Spin coated SU8 solutions ranging from 2 μm to over 100 μm in thickness are used for a variety of micro-mechanical applications [20]. The thickness of the SU8 film is dependent on several factors including the viscosity of the resist and the spin speed/acceleration. An organic solvent, gamma-butyrolacton (or cyclopentanone for newer grades of SU8 [17]) is used to disperse SU8. The solvent not only influences the

solution viscosity but also the rate at which the photo acid diffuses within the film once exposed to UV light. The solid content of SU8 varies from around 70% for thick variants to less than 10% for thinner grades [21, 22].

The exact requirements for processing SU8 films are determined based on film thickness, solids content, exposure dose and feature size. The most commonly used SU8 formulations typically yield film thickness greater than 2 μm, the associated processing parameters for which are well documented [20, 23]. The preparation of films less than 1 μm thick has only recently been explored for use as dielectric layers or thinner mechanical structures [24]. Greater care needs to be undertaken when processing thinner films as the reduced solid contents can lead to film cracking and delamination. When processing thinner sheets of SU8, the exposure dose and pre-exposure bake (PEB) must be reduced to lower the thermal stress within the film, which would otherwise cause damage [25] (the processing conditions for SU8 used in this study are discussed in the experimental chapter).

The exposure of SU8 results in photo-acid generation which occurs most favourably at a wavelength of 365 nm. While SU8 absorbs more strongly at shorter wavelengths, it becomes difficult to control exposure and produce well defined features. For this reason filters are commonly used to filter out lower wavelength light [26, 27]. Longer wavelengths, on the other hand, induce insufficient photo-acid generation for realistic exposure times. For example, the transmission of SU8 increases from 6% at λ = 365 nm to about 58% at 405 nm. As well as the exposure wavelength, exposure dose must also be considered. A higher exposure dose for shorter periods does not necessarily result in greater resolution as photo-acid is generated too quickly, causing

further diffusion into the film which reduces resolution. Excessively low exposure doses on the other hand can lead to insufficient crosslinking and film failure during development. Over-development, where development occurs beyond the edges of the lithography mask, is most likely to occur when higher exposure doses are used. Close contact between the mask and substrate is beneficial for reducing the risk of over-development as less shadowing occurs, but care must be taken not to "stick" the SU8 film onto the shadow mask with excessive force. The optimum exposure dose of SU8 ranges from 800 mJ/cm^2 for thick films, to around 100 mJ/cm^2 for sub-1μm-thick films (**Figure 2**).

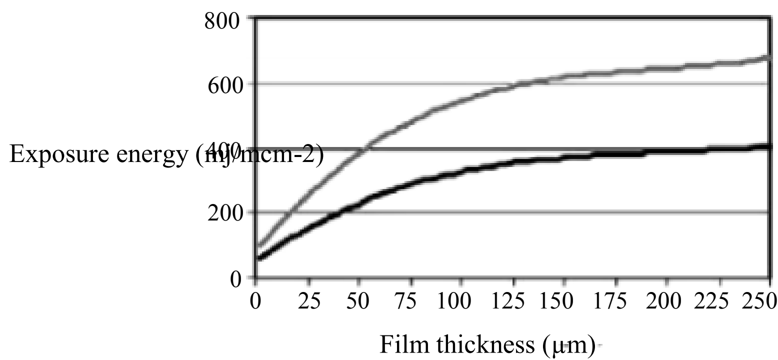


Figure 2: Required exposure dose for various thickness of SU8. Reproduced from [18].

Diffusion of the photo-acid within SU8 is an important factor in determining the resolution of the exposed feature. Extended post-exposure bake (PEB) times and temperatures result in greater diffusion of the photo-acid within the film - i.e. diffusion away from the areas defined during the exposure of the film - such that over-development occurs even if the exposure dose is fully optimised. The pre-bake temperature and exposure time also influence the degree to which diffusion can occur at later development stages as they affect the residual concentration of the organic solvent remaining in SU8; residual solvent in the film facilitates diffusion of the photo-acid. Low solvent content reduces diffusion of the photo-acid after exposure as well as

reducing the mobility of the epoxy chains; the latter also causes increased film stress as the molecular chains within the photoresist are unable to relax [18].

During the PEB, internal stresses are created within the film such that the film undergoes shrinkage, with a corresponding increase in density. One further factor which can cause film damage during the PEB is any mismatch in the coefficient of thermal expansion of the substrate and film. Figure 3 shows two ~250 nm layers of SU8 which have undergone deformation as a result of internal stress within the film. **Figure 3 A** shows stress cracks on exposed areas of the film, while **Figure 3 B** image show delamination of cross-linked areas. Typically, the PEB is performed on a hotplate at a temperature of around 95°C for a period of 1 to 5 minutes. One method for eliminating, or at least reducing, the thermal shock effect of the PEB is via temperature ramping, which provides the polymer chains more time to relax and realign. After cross-linking is complete the reaction will slow down and eventually stop, at which point the PEB temperature can be ramped downwards to room temperature.

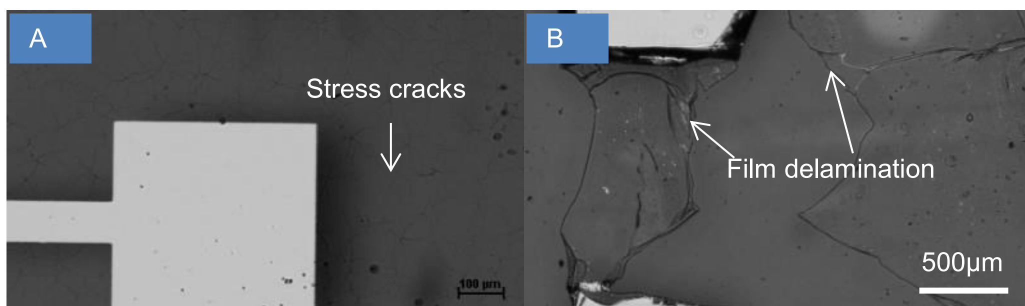


Figure 3: (A) Micrograph showing a thin ~250 nm layer of SU8 which has undergone cracking as a result of thermal stress. (B) An SU8 film of the same thickness which has undergone delamination on a glass substrate.

5.2 SAG fabrication process

Recently an interlayer lithographical process has been developed at Imperial College for the rapid fabrication of electrical devices. The process limits the requirmnet for the use of multiple shadow masks and enables patterning of complex devices such as OFETs and OLEDs. The work presented in this chapter expands on this previous research to develop the interlayer lithography method to develop self-aligned gate devices.

Unlike traditional OFETs, where the source drain and gate electrodes overlap (see **Figure 6**), self-aligned gate OFETs are typically more challenging to manufacture as close alignment of source drain and gate is required [14, 28, 29]. This alignment typically involves using optical photolithography masks and mask aligners, a time consuming and expensive process. As depicted in **Figure 4** and **Figure 5** by using the interlayer technique it may be possible to eliminate the use of lithography masks and instead use the gate electrode to fulfil this function, thereby enabling the rapid fabrication of self-aligned OFETs as no alignment procedures would be required. The method proceeds as follows. The gate electrode is first deposited on a glass substrate, and a thin film of SU8 is then spin coated onto the gate electrode and glass slide (**Figure 4 A/B**). The SU8 is soft-baked but processed no further at this stage. After soft-baking, the SU8 is “tacky” but robust enough to undergo further processing. A continuous Au cross-shaped electrode is then deposited on the soft-baked SU8. The left half of the cross will later become the source electrode and the right half will later become the drain electrode. The cross-shaped electrode is separated vertically from the gate by the SU8 (**Figure 4 C**).

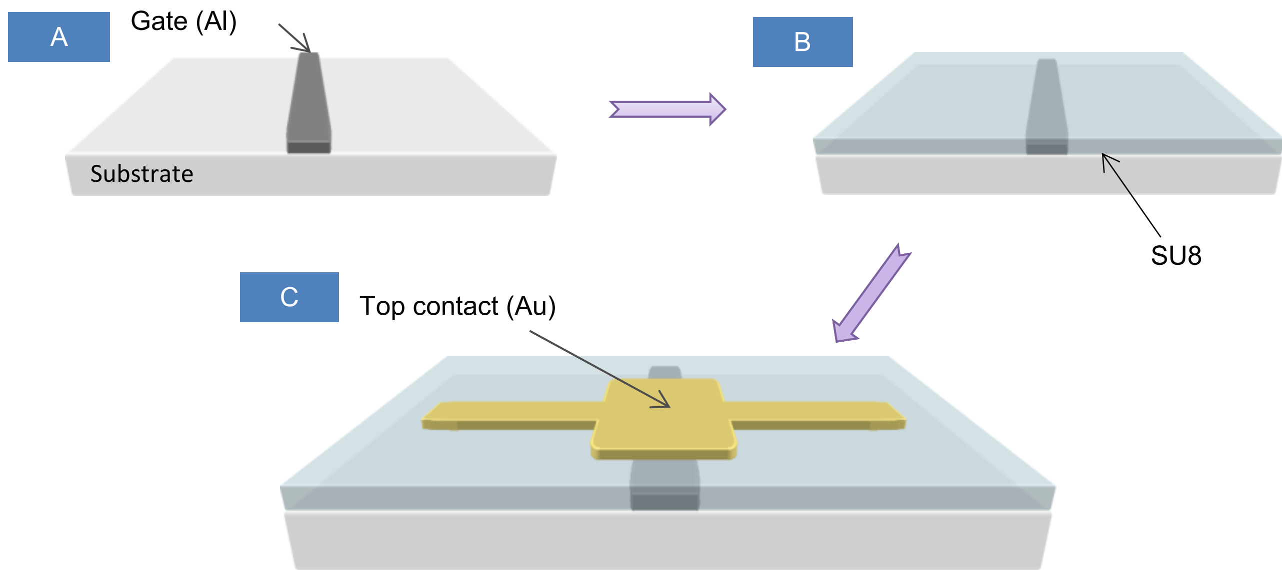


Figure 4: Schematic of the initial back illumination self-aligned gate fabrication process. (A) An Al gate is first deposited by shadow masking using thermal evaporation. (B) SU8 is then deposited on top of the entire film and soft baked. (C) A layer of Au is later deposited as the source and drain electrode on top of the SU8 interlayer.

The substrate is then back exposed using UV light (**Figure 5 A**). The gate electrode effectively acts as a shadow mask, preventing the SU8 directly behind it from being cross-linked. After exposure the substrate is baked on a hotplate, causing the exposed SU8 to become insoluble, while leaving the un-exposed SU8 behind the gate soluble. The entire film is then developed in the SU8 developer (PGMA) to remove the soluble SU8 and in the process remove the Au electrode directly above the gate. Following development, the cross-shape is split in two providing closely spaced source and drain electrodes to the left and right of the gate. The final configuration of the film was such that the deposited top contacts are self-aligned on either side of the gate electrode as shown in **Figure 5 B**.

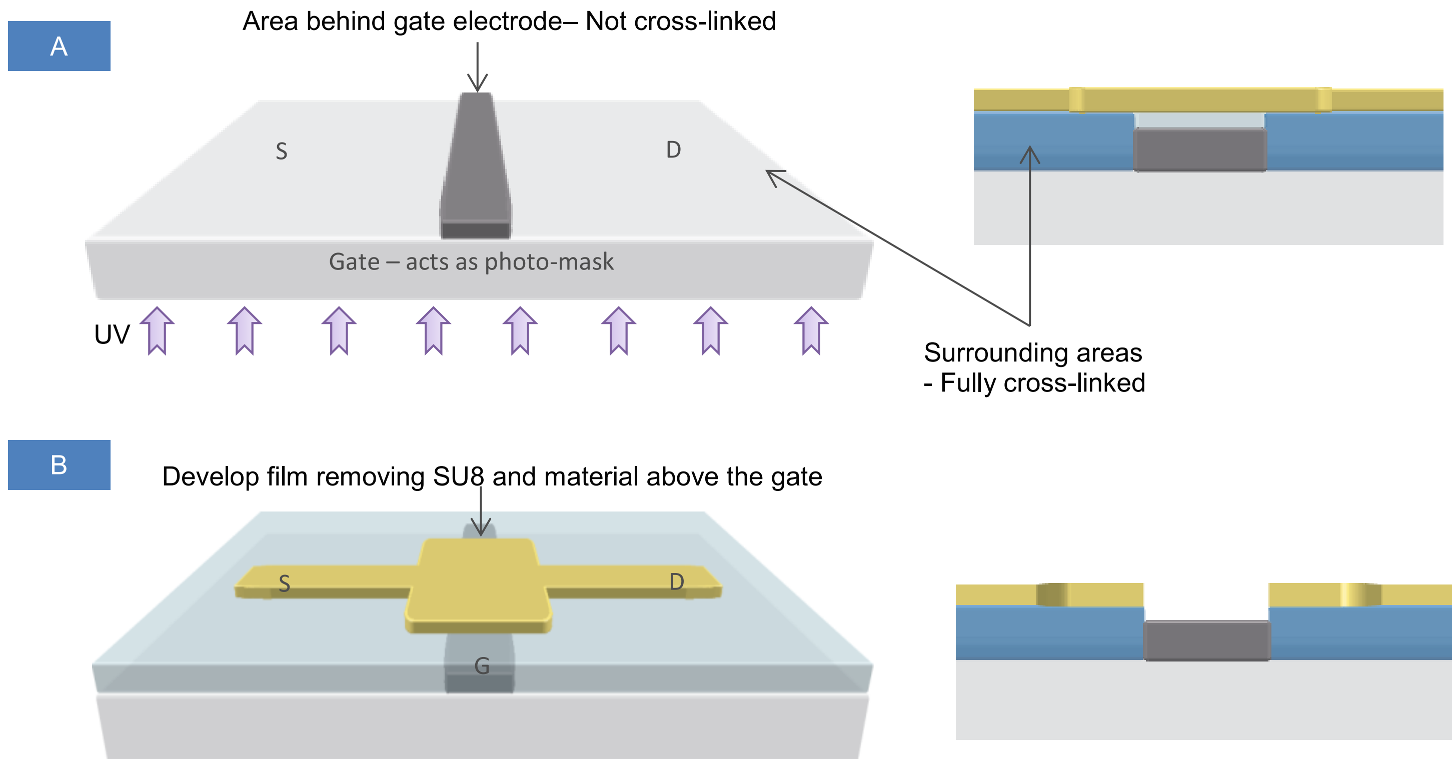


Figure 5: Schematic of the final development of the back-illumination self-aligned gate fabrication process. (A) The entire film is back-exposed using UV light (365 nm) and subjected to a PEB. The SU8 above the gate electrode remains soluble while the SU8 surrounding it, which supports the subsequently formed source and drain electrodes, becomes insoluble. (B) In the process of development, the SU8 above the gate is removed, along with the overlying Au. Thus, in the final configuration the source, drain and gate electrodes are isolated with the source and drain self-aligned against the gate electrode.

5.2.1 SAG fabrication and optimisation

Self-aligned transistors are attractive due to their potential for high frequency operation. However, one challenge is achieving efficient charge injection into the semiconductor. If there is no spatial overlap the performance of the device will be limited as charge injection cannot efficiently occur across a non-conducting gap [30, 31] (**Figure 6 B**). As such aligned inorganic TFTs have some degree of overlap [32-34], while this overlap may increase the capacitance of the device it ensures the device, operates efficiently. These difficulties faced when developing aligned transistors is

perhaps why the majority of the published research on OFETs relates to the traditional overlap designs despite their unfavourably high capacitances.

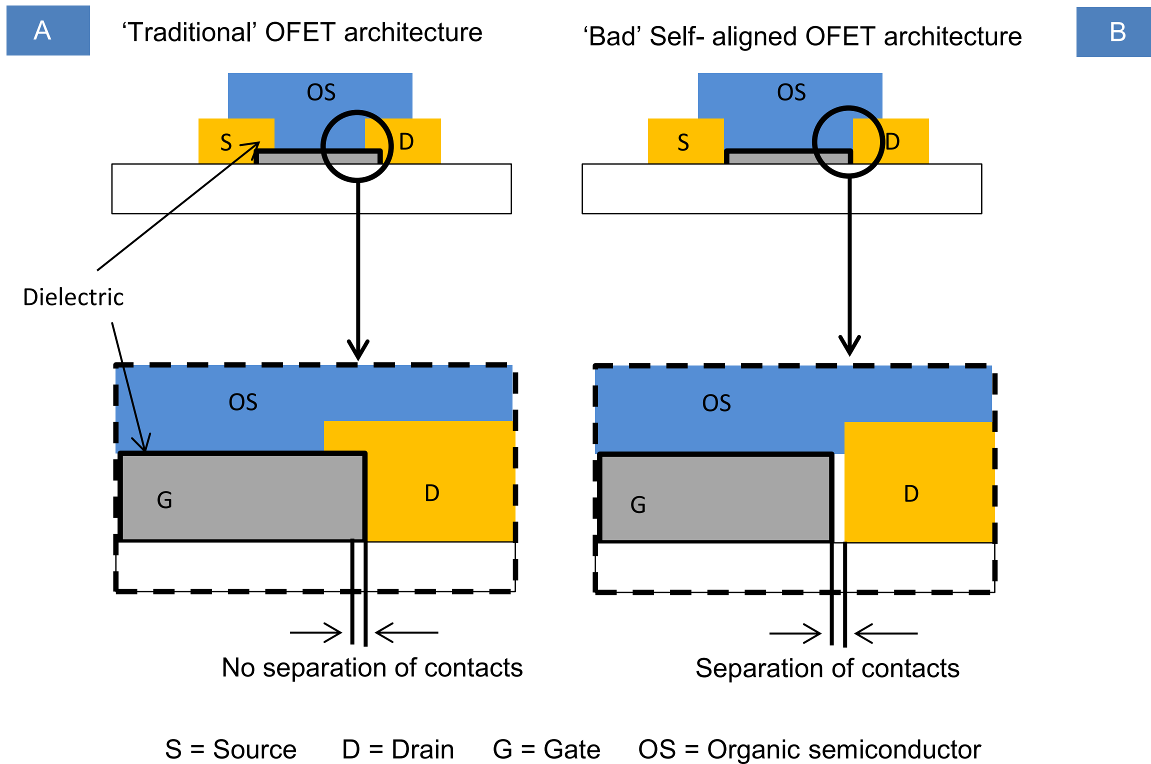


Figure 6: Schematic of self-aligned gate OFET architectures, showing (A) a small amount of overlap between the source, drain and gate, and (B) no overlap between the contacts with a small separation of the contacts.

For traditional fabrication systems, a mask aligner is programmed to precisely position photo-masks at different stages of the fabrication process. In this case the amount of overlap between the source, drain and gate is related to the achievable tolerance of the mask aligner and its alignment optics. The back illumination technique proposed above does not require the use of traditional alignment techniques. The self-aligned method described above will theoretically result in no overlap of the contacts, provided development of the photoresist is sufficiently controlled. However if the development is not fully controlled some degree of “spread” over the gate may occur e.g. as a result of photo-acid diffusion. This spread is one of the controlling factors

governing the performance of the resultant devices, some small amount of spread being necessary for efficient operation.

It is possible it will take longer to develop the SU8 photoresist under the source and drain electrode as the SU8 developer will not absorb into the SU8 at equal rates in areas where it is covered with metal contacts. This will result in over development of uncoated areas of the film with the coated areas left under developed. With prolonged development times, shrinkage of the SU8 film can be expected to occur with a loss of 10-20% of the SU8 volume being common. This may further separate the contacts as the source and drain are drawn away from the gate.

It takes longer to develop the SU8 photoresist under the source and drain electrodes as the SU8 developer does not absorb into the SU8 at equal rates in areas where it is covered with metal contacts. This can result in over development of uncoated areas of the film, while coated areas may still be underdeveloped. With prolonger development times shrinkage of the SU8 film can be expected to occur, with a loss of 10-20% of the SU8 volume being common. This may further separate the contacts as the source and drain are drawn away from the gate.

If the SU8 is under exposed, it may developed around the outside boundary of the gate electrode with a small gap between the edge of the SU8 and side of the gate electrode. This may result in poor contact with the source and drain electrode as these are defined by the development of the SU8 film (**Figure 7 A**). To reduce the likelihood of the source, drain and gate becoming separated, the exposure conditions were chosen to ensure the SU8 was overexposed, which results in greater photo-acid diffusion within

the SU8 and causes areas of the SU8 lying outside the area of the gate electrode to become cross-linked, reducing the separation of the three electrodes (**Figure 7 B**). Over exposure can be achieved using a higher dosage of UV light, or exposing the film for a longer time period than recommended by the standard processing protocol.

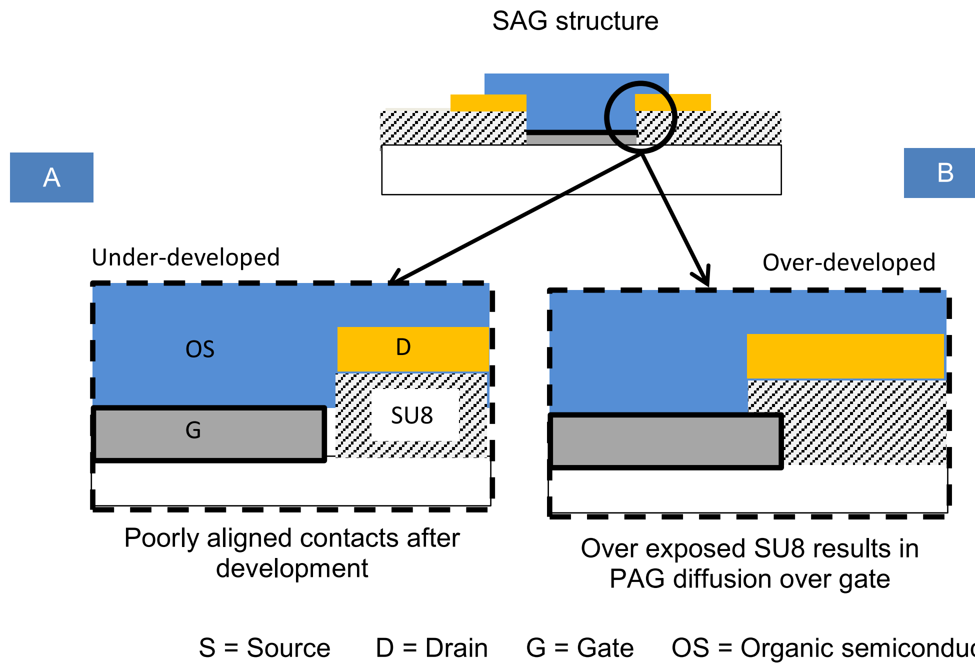


Figure 7: Schematic of the self-aligned gate structure, showing the possible alignments of the source, drain and gate contacts after development of the non-cross-linked SU8 resist. (A) Separation of the source drain and gate electrodes when under development of the SU8 occurs. (B) A small overlap of the electrodes is possible when the SU8 is over developed such that SU8 was cross linked over the gate.

The proposed design of the self-aligned gate architecture generates a further challenge in addition to the horizontal separation of the contacts described above. The SU8 interlayer raises the source and drain above the gate electrode, separating the contacts and further reducing the efficiency of charge injection as depicted in **Figure 8**. To limit this effect, the SU8 interlayer must be kept thin. It was not possible to completely eliminate the vertical separation as the photoresist must cover the gate electrode to allow the top contact to be removed during development. If the photoresist

was thinner than the gate electrode it would not completely cover the gate, preventing the removal of the central strip from the cross-shaped electrode during development.

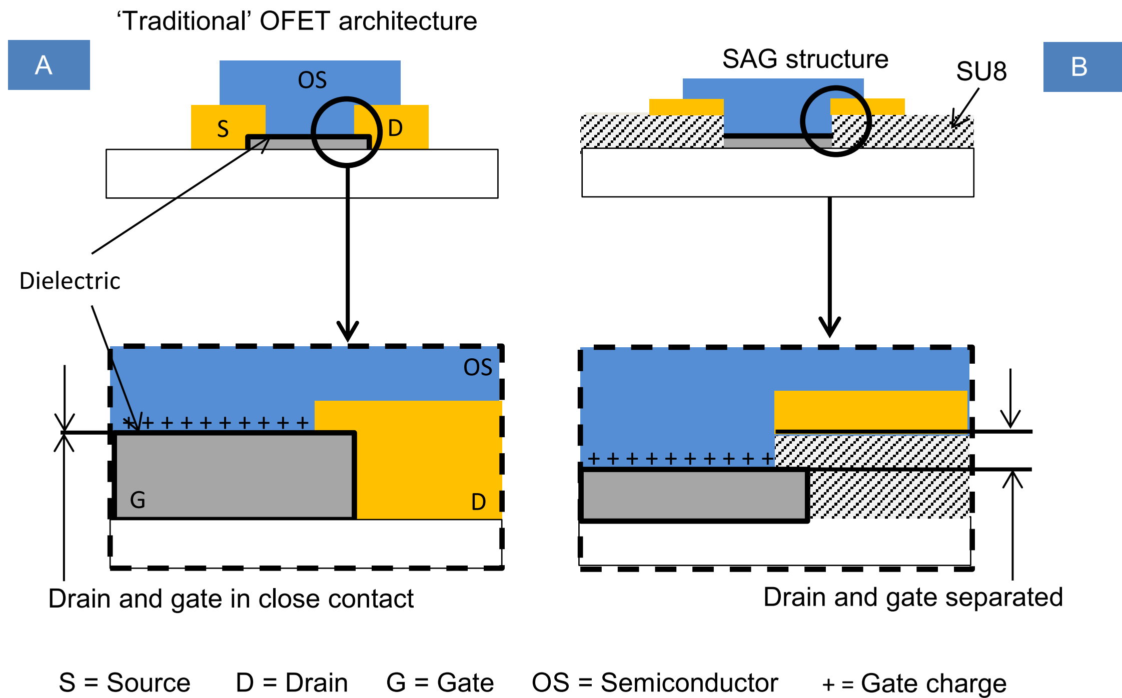


Figure 8: (A) Schematic of a traditional – non-aligned – OFET where the drain and gate are in close contact. (B) The proposed back illumination self-aligned gate structure where vertical separation was present between the top of the gate and bottom of the source/drain electrode. In this configuration charge injection is offset from the top of the gate where the SU8 has raised the source and drain electrodes.

The thinnest SU8 formula available from the manufacture is SU8 2000.5 which forms films as thin as 500 nm. The gate electrode was typically 50 nm thick, resulting in a 450 nm height differential between the source/drain and gate electrodes. To reduce this offset the SU8 2000.5 formula was diluted using SU8 thinner to allow the deposition of thinner SU8 layers. As shown in **Figure 9**, by reducing the solid content of SU8 2000.5 formula to 75 wt%, the thickness of the film was reduced to 400 ± 30 nm. This fell to 250 ± 40 nm when diluted to 50 wt%, and just 125 ± 25 nm when diluted to 25wt% solid contents, representing a ~4 fold reduction from the initial value of 500 nm. Further dilution of the SU8 resulted in poor quality patchy film across the

substrate that could not be used for reliable high resolution patterning. The thinnest value of the SU8 film fabricated above was 125 ± 25 nm thick for the 25 wt% film, subtracting the thickness of this film from the thickness of the gate electrode (75 nm) implies a vertical offset of around 50 nm, while the SU8 film diluted by 50 wt% results in a vertical offset of 200 nm. There was a concern that the offset of the 25 wt% film might be too small to allow the photoresist to cover the gate electrode and allow for effective development of the self-aligned structure. Therefore both the 50 wt% and 25 wt% formulations were investigated.

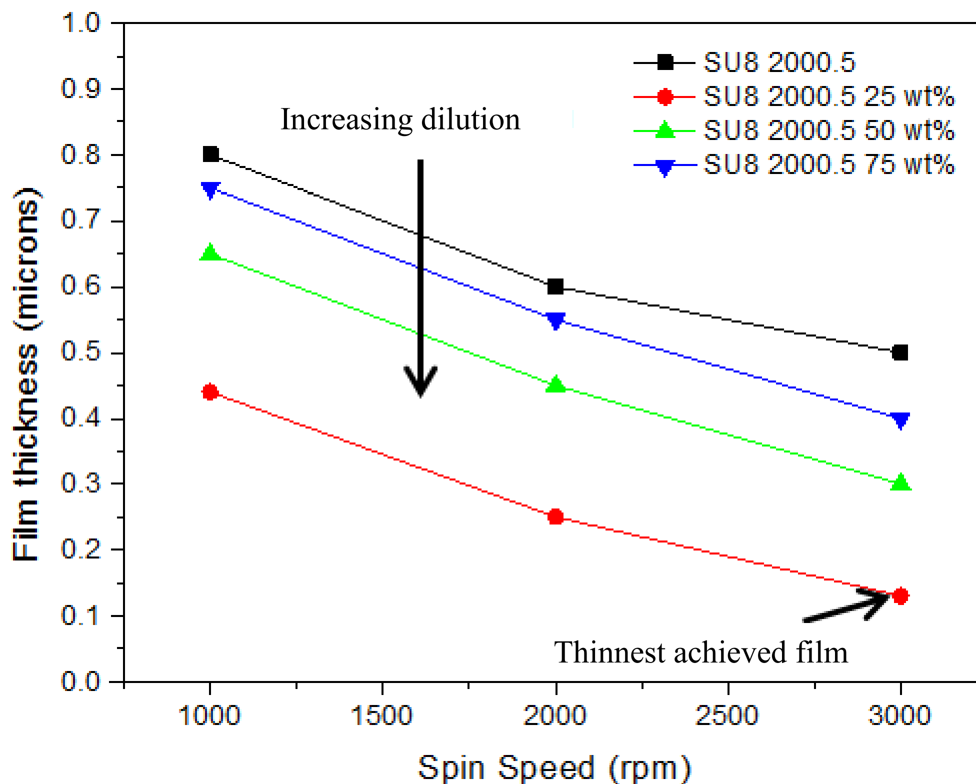


Figure 9: Thickness of SU8 films formed by spin coating at speeds ranging from 1000 to 3000 rpm from solutions of various concentrations. The minimum thickness achievable without sacrificing film quality was 125 ± 25 nm, representing a 75% decrease from the undiluted SU8 2000 solution. (wt% represents the concentration of the solution relative to its initial concentration)

5.2.2 SAG development

Films were fabricated on 20 x 20 mm glass microscope slides which had previously been cleaned by immersion in acetone, Decon 90 and isopropyl alcohol for 5 minutes each. As outlined above, the first part of the fabrication process involved deposition of a gate electrode by thermal evaporation - this was done before deposition of the SU8 interlayer via spin casting. Deposition of the top contacts was also carried out by thermal evaporation through a shadow mask. The computer aided design drawing of the associated shadow masks are shown in **Figure 10**.

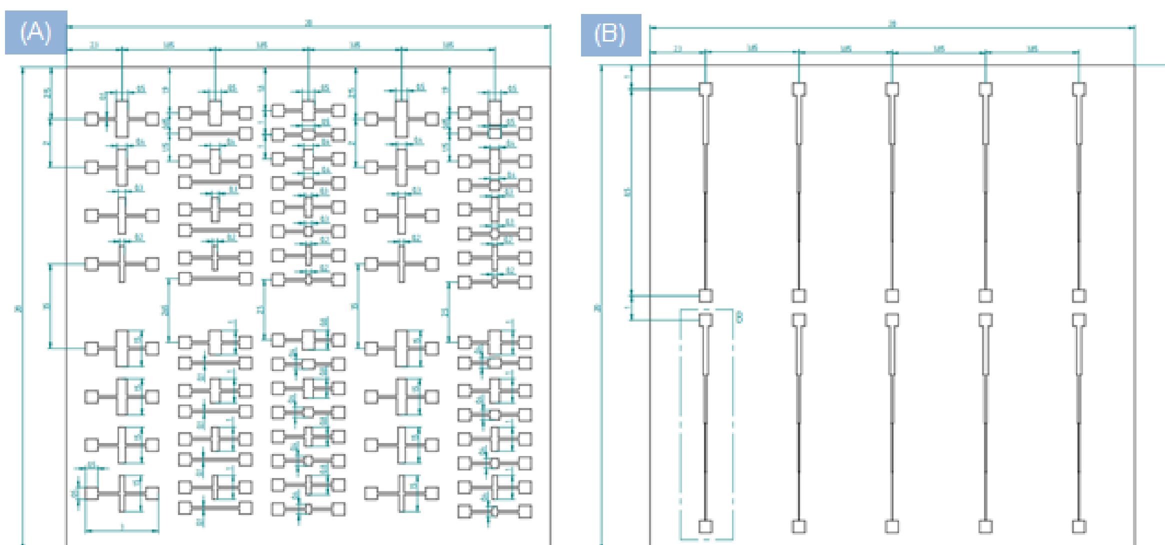


Figure 10: Computer aided design drawings of the (A) source and drain and (B) shadow masks.

All stages of fabrication were carried out in a climate-controlled clean room, except the deposition of the metallic contacts, which was performed in a thermal evaporator located within a glove box with an inert nitrogen atmosphere (O_2 levels below 10 ppm). All evaporations were carried out at a pressure < 10^{-6} mBar. **Figure 11** shows photographs of 50 wt% and 25 wt% SU8 interlayers after the top contacts were applied. To aid removal of the top contacts, the thickness of the top cross-shaped Au

electrode was just 25 nm - thinner than the 50 nm electrodes typically used for OFETs. The deposition rate was held constant at 0.1 Å/s to avoid damage to the thin SU8 film underneath as it has been reported that high rates of deposition can damage adjacent layers [35].

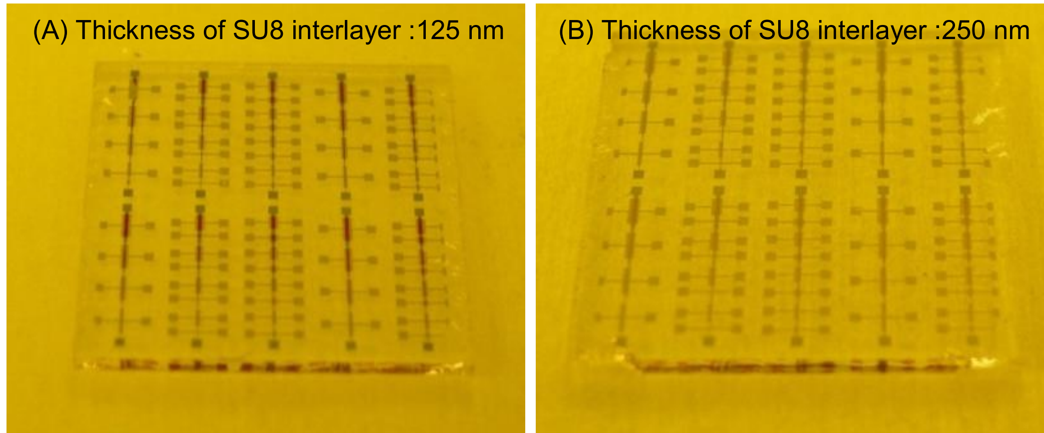


Figure 11: Photographs of fabricated devices before exposure and development of the SU8 interlayer, using 25wt% SU8 (A) and 50wt% SU8 (B).

As the gate electrode acts as the photo-mask in the patterning procedure the substrate was placed upside down on a metal plate and exposed at 365 nm using a Kaul Swiss mask aligner. This differs from the normal approach where the film is placed face up and a photo-mask positioned above the substrate and subsequently exposed (If the substrate was not placed upside down it would be completely exposed as the evaporated electrode is on the top surface of the glass). Several exposures development conditions were evaluated in an attempt to optimise the exposure time and baking conditions of the SU8 film. For the thinner 125 nm film, the substrate was exposed for between 5 and 20 seconds, while the thicker 250 nm film was exposed for between 10 and 20 seconds. The exposure dose was kept constant at 10 mJ/cm^2 for each film. It was found that an exposure time of 10 seconds was sufficient for the thinner 125 nm film, along with a post exposure bake of 30 seconds. Under these conditions, the SU8 photoresist was slightly overexposed against the gate electrode. By overexposing it was ensured that

during later development the source and drain electrodes would not be withdrawn from the edge of the gate as would be the case if the SU8 was aligned more closely to the perimeter of the gate electrode (**Figure 12 A**). When the exposure time and post exposure bake were increased too much excessive over-development occurred, with the SU8 photoresist cross-linking over the entire gate electrode (**Figure 12 B**). An increased exposure time of 15 seconds and a 45 second post exposure bake was used for the thicker 200 nm SU8 film.

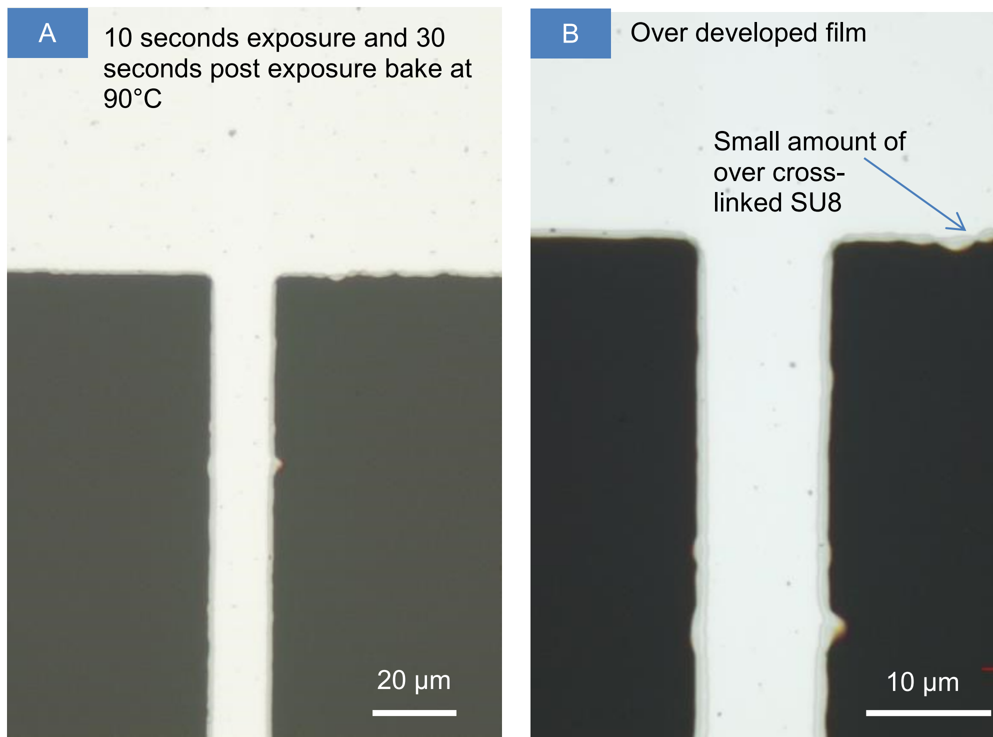


Figure 12: (A): Micrograph of over-developed SU8 film obtained from a 25 wt% solution showing a small amount of over development on the gate electrode. The degree of over development can be changed by controlling the time the film exposure time. (B) Micrograph of a heavily developed film in which unexposed regions have cross-linked.

After the SU8 film was exposed and subjected to a post exposure bake it was developed. Sonicating SU8 during development is standard procedure as it aids the removal of non-cross-linked areas [36]. Several additional factors influence the success of development at this stage, including: the manner in which the substrate is supported

during development; the "freshness" of the developer; the placement of the substrate within the sonic bath; and the power of the sonic bath. Initially it was observed that the top contacts were too delicate to be placed in a beaker containing the developer even for short periods as the contacts were completely removed by the harsh vibrations caused by the sonic bath. This was a consequence of the poor adhesion of the Au contacts and the inability of the thin SU8 film to adhere adequately to the substrate. The vibrations of the sonic bath were found to be worsened when the substrate made direct contact with the glass beaker as the vibrations of the beaker which were transmitted through the glass substrate with no damping occurring. To reduce electrode damage, the substrate was placed in a PTFE basket, in order to avoid direct glass on glass contact (**Figure 13**).

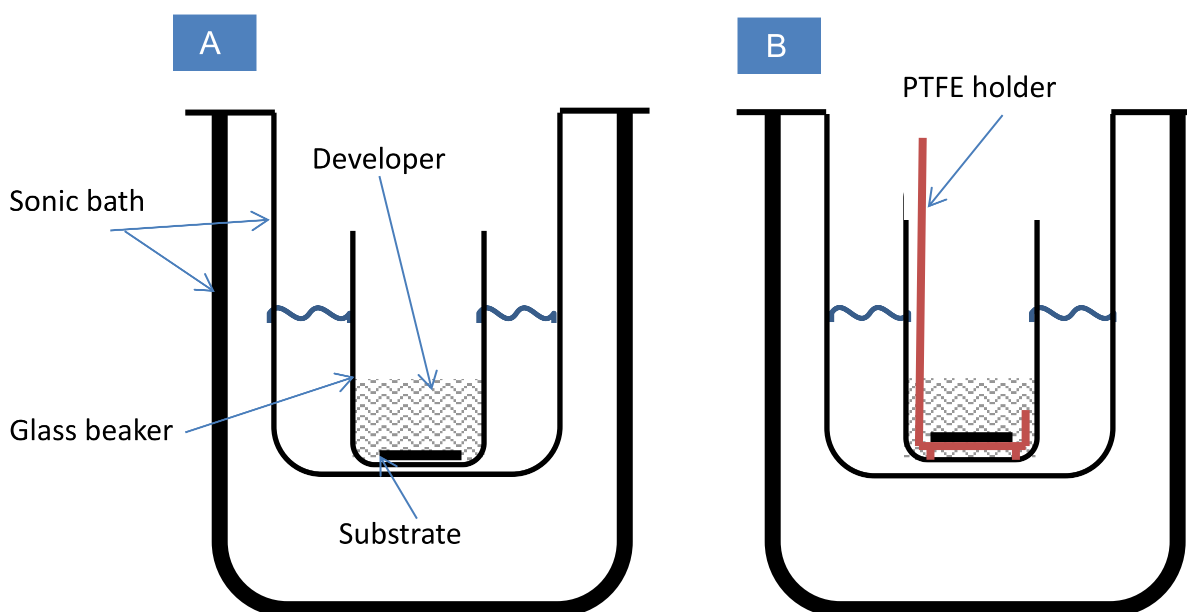


Figure 13: Schematic depicting the placement of the substrate in the sonic bath (A) Initially the substrate was placed in a glass beaker in a solution of SU8 developer. This was found to cause excessive damage to the film when vibrations from the glass beaker were transferred to the glass substrate. (B) By placing the film in a PTFE holder the glass on glass contact was avoided and the film were less prone to delamination.

Holding the substrate in the manner shown in **Figure 13** reduced the delamination of the Au allowing preliminary results to be obtained. While it was possible to develop both the 50 wt% and 25 wt% SU8 films, neither could be reliably

developed with large parts of the films being removed uncontrollably. Over 500 films were made and, in general, the thinner SU8 would detach over areas of the film such that the source, drain and gate were never aligned or useable as devices. For both concentrations of SU8, the contacts would frequently be removed along with surrounding SU8 as shown in **Figure 14**. Using thicker SU8 reduced this problem somewhat but it then became difficult to remove the Au film from above the gate, resulting in incomplete development.

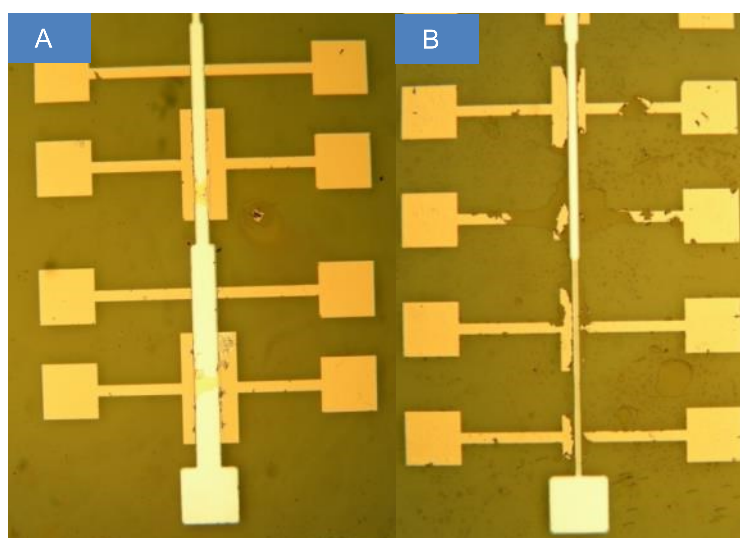


Figure 14: Micrographs of the self-aligned gate OFET prepared by back illumination using the procedure described above. Thicker films prepared from 50 wt% SU8 (A) were somewhat easier to develop with less of the Au film detaching from the substrate compared to thinner films prepared from 25 wt% SU8 (B). In addition to the Au delamination, large areas of SU8 also became detached for the 25 wt% film.

To overcome this, the substrate was sonicated for a longer period of 20 minutes in an attempt to remove the Au which was still loosely attached above the gate. As shown in **Figure 15**, this resulted in excessive damage on both sides of the electrode. Two main problems were encountered: the Au would either flake off in larger chunks or slowly break off from the top and bottom of the contact against the gate.

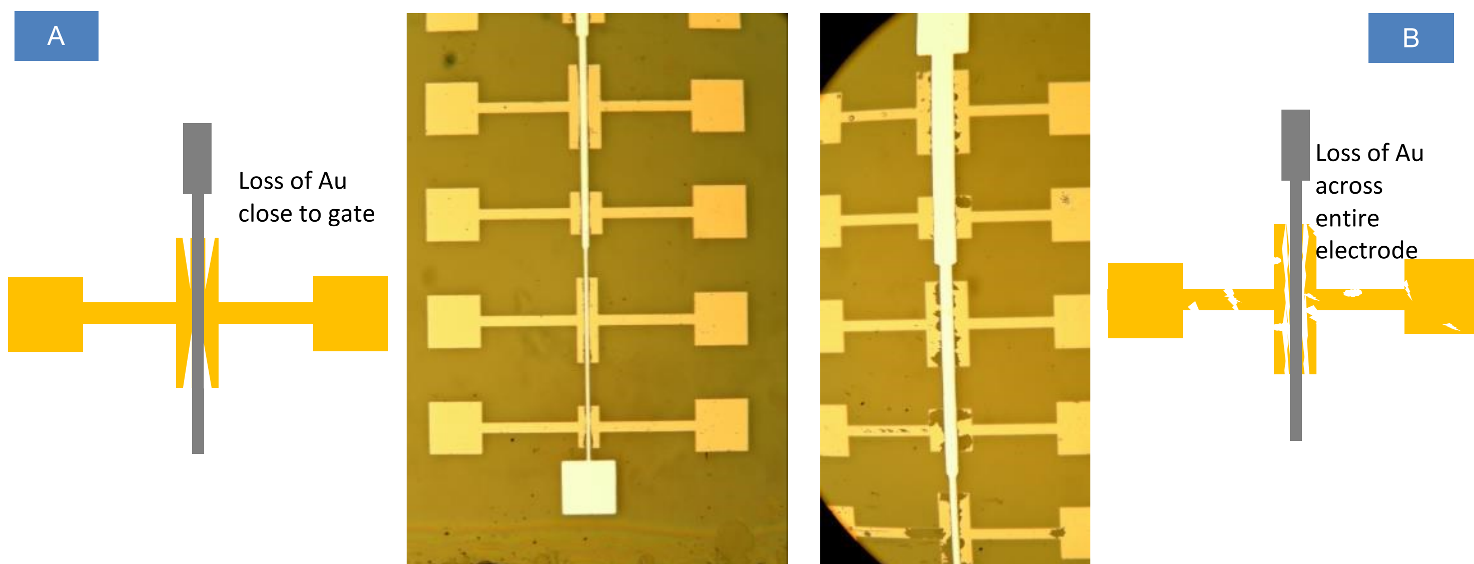


Figure 15: Schematic and micrographs depicting the effects of prolonged sonication on the 50 wt% SU8 film. The Au typically either started to break off around the gate electrode (A) or broke off in larger areas on the entire electrode (B) .

To understand the steps occurring during development, films prepared from 50 wt% thickness SU8 were developed by placing the substrate in the SU8 developer solution with no sonication until the SU8 under the Au had dissolved. **Figure 16** shows the Au electrode after the centre section had "sunk" down on top of the gate. When the substrate was later subjected to sonication, the Au film fractured and it detached from the top of the gate against the edge of the cross-linked SU8 film (**Figure 16 B**).

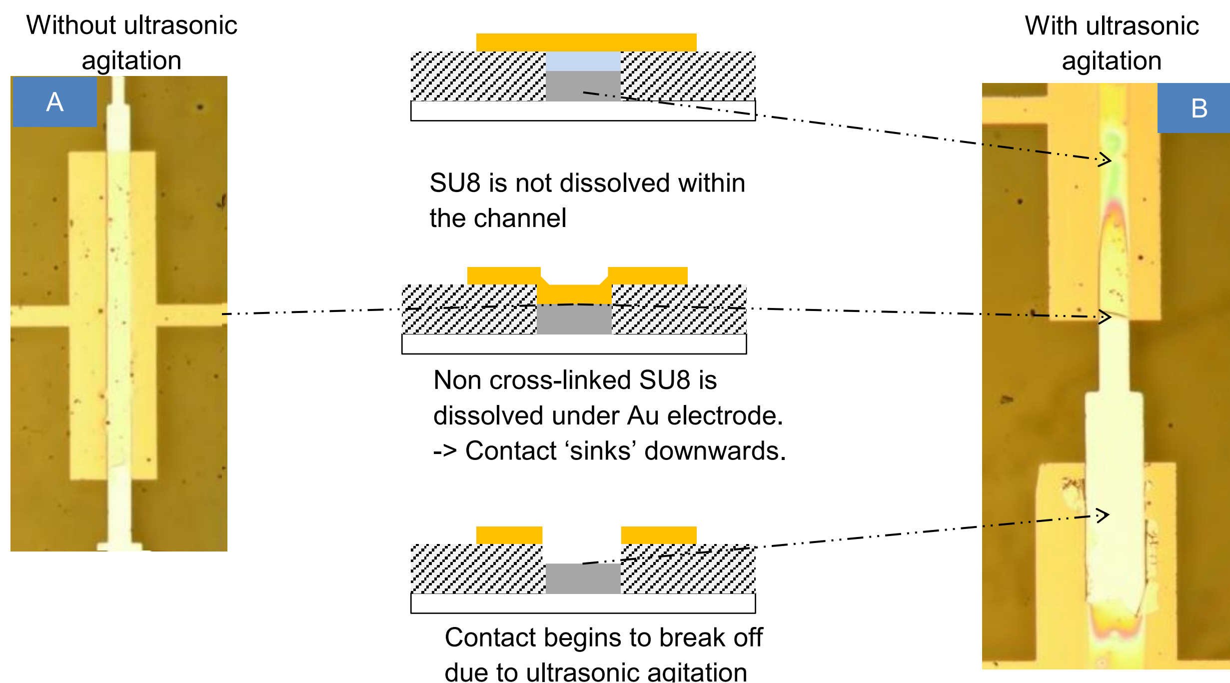


Figure 16: Micrographs and schematic showing the different stages of the self-aligned gate development process. (A) When the film was left in a solution of the developer solution for over an hour, the SU8 above the gate is dissolved causing the overlying Au to 'sink' into the gate channel. When the film is then sonicated (B) the Au breaks off over the gate electrode.

The development time was also found to differ depending on the location of the electrode. Devices in the corner of the substrate were observed to develop more rapidly (**Figure 17 A**), than those in the centre (**Figure 17 B**). Further sonication to fully develop the central devices caused the definition of the edge devices to degrade severely. The differing development times across the substrate were due to the wide range of dimensions being developed (from 10 μm to 1 mm). Devices with smaller features developed most quickly as they required less material to be removed. A trade off exists between developing larger and smaller features: larger dimensions require longer development times but damage smaller features. Taking this into account it was found that the best results were gained by only attempting to develop a sub section of devices on the substrate which had similar sizes.

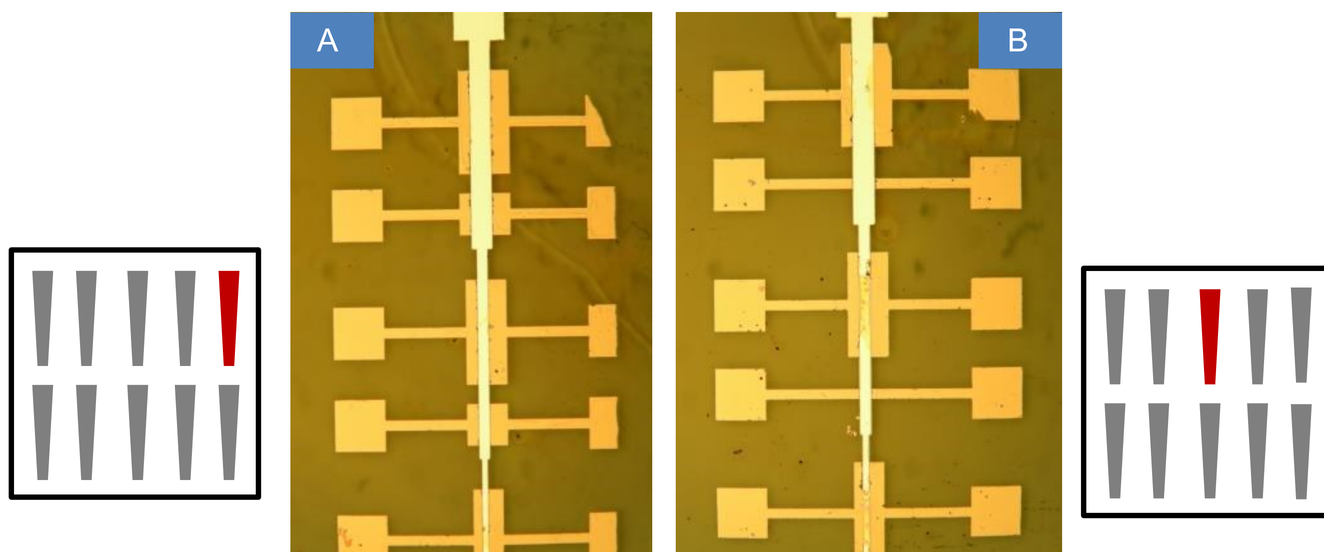


Figure 17: Schematic and micrograph of the differing development conditions across the substrate. (A) An entire row of devices located in the corner of the substrate showing complete development. (B) A different row of devices in the centre of the same substrate after being developed under the same conditions. Smaller devices in the corner are well developed while larger central devices are still partly undeveloped.

Over aggressive sonication during development was found to be responsible for the poor development achieved. As can be seen in **Figure 16,** sonication is needed to remove Au from above the gate electrode, and thus this step in the fabrication process cannot be omitted. In an attempt to reduce the damage caused by sonication and obtain functional devices, the position in which the substrate was held during developing was modified. As shown in **Figure 18**, instead of securing the substrate in a PTFE holder (which may still transmit high energy vibrations through to the substrate), the substrate was instead held from above in the developer solution such that the substrate was not in contact with the glass beaker. In addition, the glass slide was also held face down, so that the Au film was inclined to drop off the gate electrode, assisting detachment from the substrate (**Figure 18 C**).

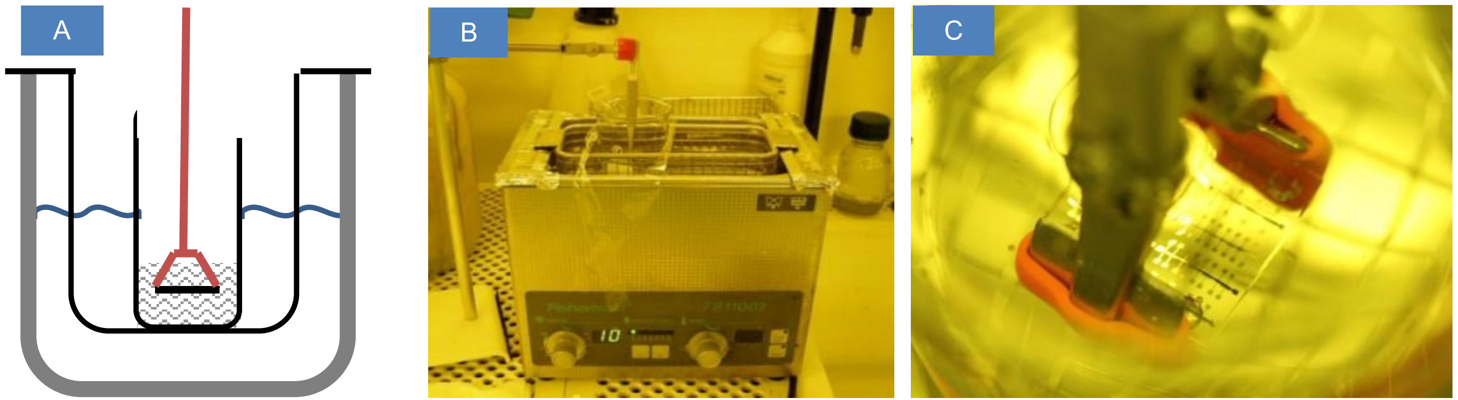


Figure 18: (A) Schematic of the substrate being developed within the sonic bath using an improved configuration. The Substrate is held within the developer with no contact with the glass beaker. (B) Photograph of the development setup where the substrate is being held with the aid of a clamp stand. (C) Close-up photograph of the substrate during development, the substrate can be seen held upside down with rubber pads eliminating glass on metal contact with the metal holder used to secure the substrate.

Using this modified development method, the previously observed delamination of SU8 and the associated damage to the electrode was reduced substantially. **Figure 19** shows micrographs of fully developed devices fabricated with the thinner 25 wt% interlayer. A range of device geometries are shown from different parts of the substrate, confirming that, by eliminating high energy vibrations, the reliability of the development procedure can be dramatically improved. Successful development was possible with features as small as 20 µm, the smallest feature size achieved by shadow masking without inducing shadowing of the electrodes.

Some problems remained with the development process: specifically the SU8 had a tendency to form pin-holes during the baking process. The formation of the pin-holes is likely a consequence of the SU8 shrinking during cross-linking. The very thin layers of SU8 are unable to flow and reform into a complete sheet as would normally be the case for thicker films [23].

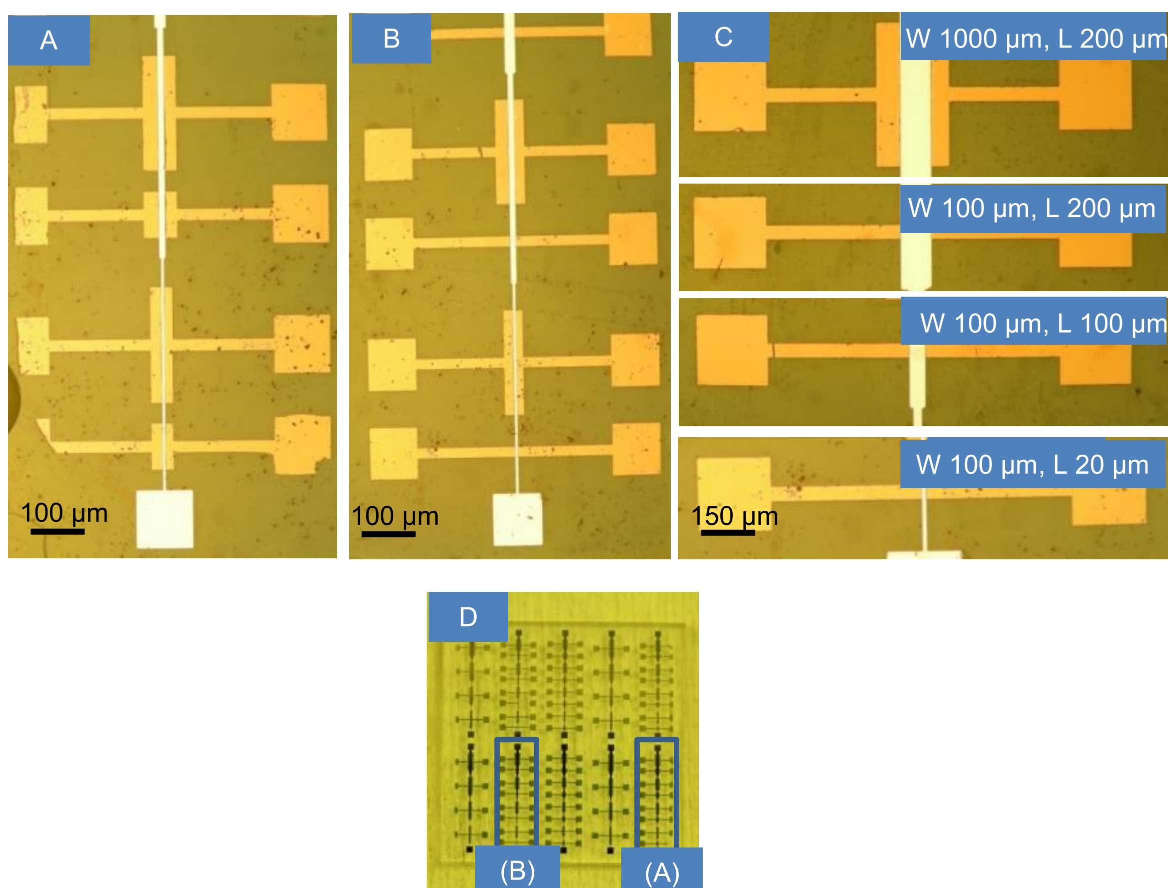


Figure 19: (A, B) Micrographs of a row of successfully developed devices fabricated using 25 wt% SU8 on a single substrate. Pin holes can be seen on the substrate as a consequence of the very thin layers of SU8 used in the fabrication process. Higher magnification micrographs are displayed in (C) where the channel formation can be seen to be well defined compared to previous attempts. (D) Photograph of the final developed film with the two rows shown in (A) and (B) highlighted.

As previously discussed, when the source and drain electrodes are physically separated from the gate, charge injection is difficult to operate, so it is common to have a small overlap of both the source and drain electrodes with the gate on self-aligned devices. Using the back illumination method, this can be accomplished by over developing the SU8 to make the photo acid in the SU8 diffuse over the side of the gate electrode during development. This effect can be seen in **Figure 20** where high resolution micrographs of the final electrode are shown. The sides of the source and drain overhang the gate electrode by < 1 µm, partially obscuring the gate electrode underneath. The three electrodes are still separated vertically as the SU8 is cross-linked

under them, and in the final device configuration a layer of dielectric will be present above the gate electrode providing further electrical isolation.

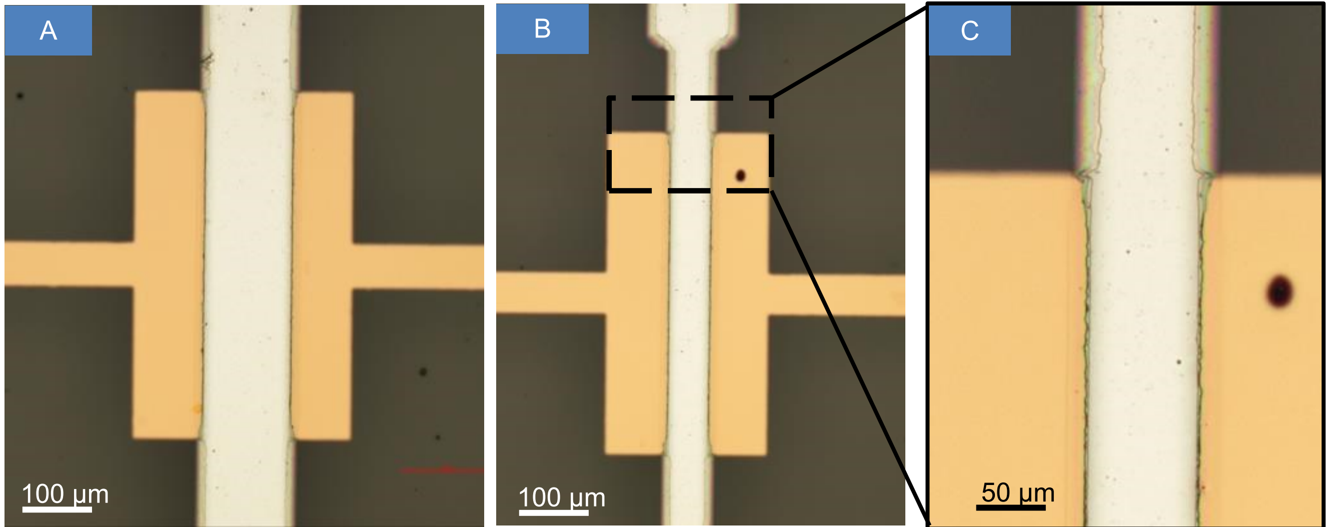


Figure 20: (A, B, C) Micrographs showing the small overlap of the source and drain electrode against the gate. The overlap is necessary to ensure efficient charge injection into the semiconductor. The overlap is measured to be < 1 µm. (C) Shows an enlarged section of (B).

The above discussion describes the principal difficulties encountered when fabricating the self-aligned gate transistors, and the manner in which each stage of the fabrication process was carefully considered and optimised. Once these issues had been addressed, the patterning fidelity was improved, and at this point initial devices were tested to determine if they could function as working transistors.

5.3 SAG devices

Self-aligned gate transistors have previously been reported using both SU8 (**Figure 21 A**) and SAM dielectrics (**Figure 21 B**). The main focus of current research with such devices is on achieving low leakage current, and high capacitances to enable low-voltage OFET operation with high performance [37].

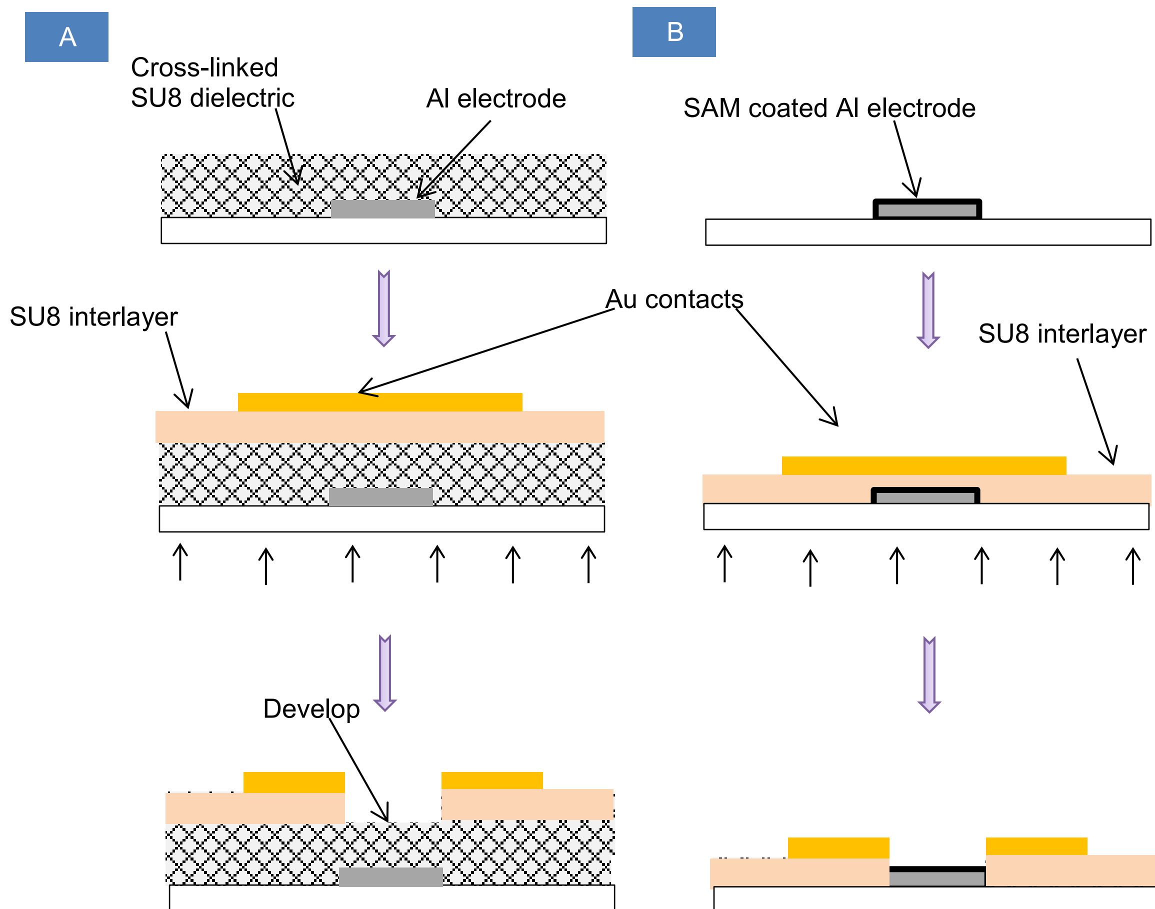


Figure 21: Schematic of the fabrication process for the two types of dielectrics use in this work. (A) 2 μm thick cross-linked dielectric formed from SU8. To fabricate this structure SU8 was first deposited over the gate electrode and cross-linked before depositing a second layer of SU8. (B) For the SAM dielectric ODPA or PHDA was applied before the SU8 interlayer was deposited. The remainder of the fabrication process was the same as described in the previous section.

Common dielectric materials for low-voltage devices include ultrathin polymer films [38], polyelectrolytes [39], and hybrid organic/inorganic dielectrics [40]. SAMs

have proven to be some of the most promising candidates for low gate-voltage dielectrics owing to their advantageous self-assembly properties. The SAM effectively suppress tunnelling through the device by virtue of their highly ordered aliphatic chains even though they are only a few nano-meters in thickness [41]. For the work reported here, low-voltage graphene-based devices employing ODPA as the gate dielectric and evaporated C60 as the organic semiconductor were fabricated. Devices were also fabricated using a layer of crosslinked SU8 as the dielectric. Testing of the self-aligned gate OTFTs was carried out with the assistance of Dr Cecilia Mattevi, Dr Florian Coll´eaux, Dr John Labrum and Yen-Hung Lin at Imperial College London.

5.3.1 High voltage SAG gate devices

The SU8 dielectric based devices were fabricated by thermally evaporating an Au gate electrode onto a glass slide, and then spin coating a 2 µm layer of SU8 on top. The SU8 film was then fully cross-linked and cured. To reduce the density of mobile charge traps, the SU8 film was baked in a nitrogen chamber for 12 hours [23, 42]. As the SU8 dielectric layer is optically transparent, back illumination can still be used to fabricated the transistors using the self-aligned method described above. Using SU8 as both a dielectric and photoresist has the advantage that all processing is performed on a material with the same coefficient of thermal expansion. This may reduce cracking of the very thin SU8 interlayer as well as allowing for better adhesion during development. Assuming a dielectric constant of 4.1 [43] the geometric capacitance of a 2 µm thick film of SU8 is 3.7 nF/cm^2.

C60 was used for the organic semiconductor by thermally depositing 30 nm of C60 at a rate of 1 Å/s in an ultra-high vacuum. OTFT characterisation was carried out

using a Keithley 4200 series Semiconductor Parameter Analyser in a nitrogen environment. The transfer and output curves for a typical device are shown in **Figure 22**. Field effect mobilities were extracted using equation (9) in the linear regime (see chapter 2) and yielded a value of 0.45 $cm^2\ V^{-1}s^{-1}$ for the self-aligned gate device. This value compares well to reports of PHDA-C_{60} based devices which are not self-aligned and range from 0.30 to 0.27 $cm^2\ V^{-1}s^{-1}$ [44] suggesting the lack of overlap capacitance between the source, drain and gate may offers improved device performance now self-aligned.

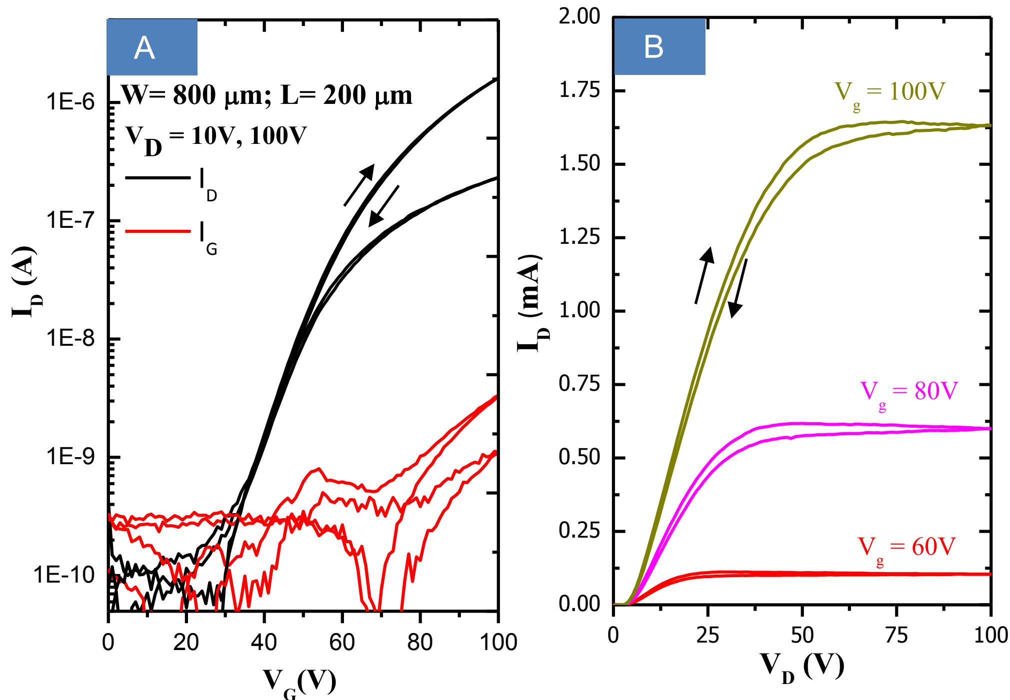


Figure 22: Electrical characteristics of a typical n-type C_{60}-based OTFT using SU8 as a dielectric. (A) Transfer and (B) Output characteristics of a PHDA-C_{60} based transistor using the self-aligned device architecture

5.3.2 Low voltage SAG devices

The above C_{60} based devices operate at high gate voltages (i.e. >50 V) which are unsuited for most applications due to the low power efficiency. SAM-based dielectrics using PHDA monolayers were also investigated in the self-aligned gate architecture with a view to reducing operating voltages. (Note: PHDA is the same monolayer investigated as adhesion modifier in Chapter 4). The use of SAMs for low voltage dielectric interfaces has been well documented [41, 45, 46]. To avoid leakage currents, a well-defined and continuous monolayer must be formed over the gate electrode and the monolayer must be as uniform as possible [41]. The reported geometric capacitance for PHDA is reported to vary from 350 nF/cm^2 [47] to over 1 μF/cm^2 [44]. This wide variation in measured values is due to the difficulties in achieving well-defined SAM monolayers. The geometric capacitance is much higher than that attainable with polymer dielectrics such as SU8 due to the short length of the SAM, and allows for the fabrication of OFETs with lower operating voltages is below 2V [48].

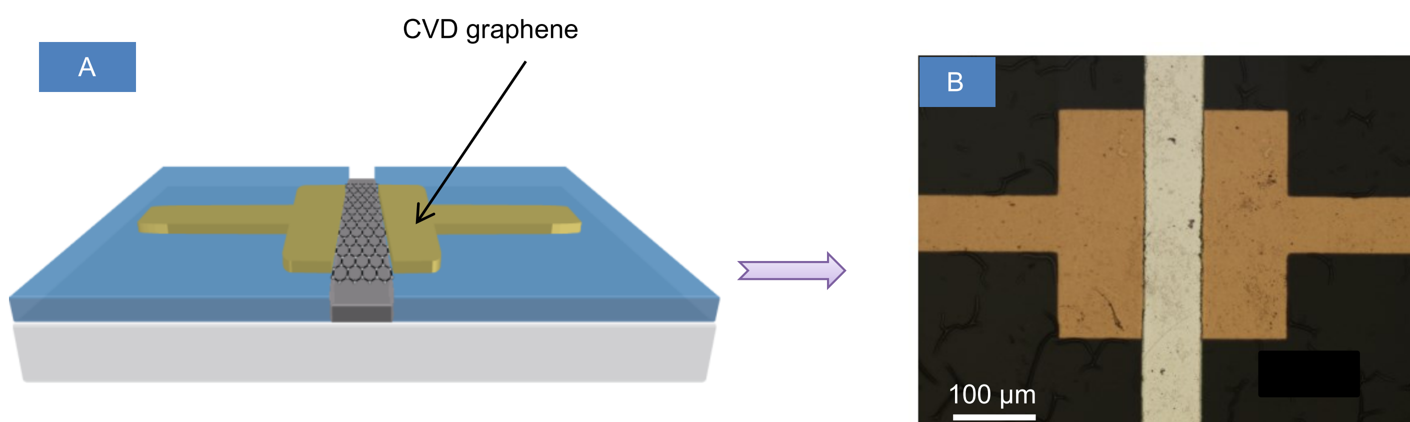


Figure 23: (A) Schematic of the CVD grown graphene after transfer onto the self-aligned structure. (B) Micrograph of a self-aligned-gate device covered with graphene.

Initial results for SAM dielectric devices were gained using graphene as the active semiconductor layer owing to previous reports of high mobility devices

fabricated using graphene and SAMs [49]. CVD graphene was grown on copper substrates and transferred to the self-aligned gate structure by Dr Cecilia Mattevi using the procedure outlined in [50]. A micrograph of a graphene-covered self-aligned device is shown in **Figure 23**; a sheet of graphene is distributed on top of the SAG device the channel width was 20 µm and its length 100 µm.

The transfer characteristics for the graphene device are shown in **Figure 24**, assuming the geometric capacitance of the SAM to be 450 nF/cm^2, the carrier mobility was determined to be 220 cm^2/Vs. The mobility is lower than values typically reported for pristine graphene-based transistors which can be > 100-times higher than the value reported here [51]. Many factors influence the low recorded mobility; in this case the large dimension of the channel was likely the limiting factor. Additionally a continuous defect-free monolayer of graphene is difficult to fabricate and position across the entire width of the channel. Graphene-based devices with similar channel dimensions to those reported here have carrier mobility of ~330 cm^2/Vs [49], suggesting a similar performance level to the devices tested here.

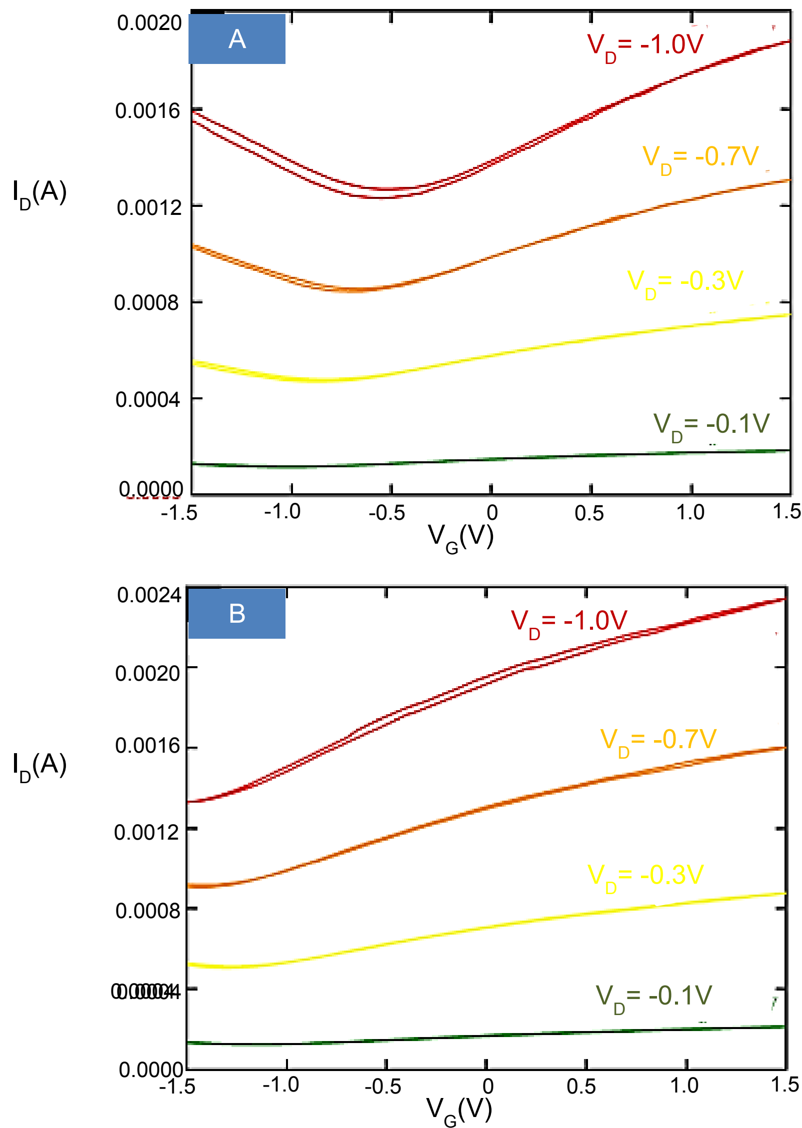


Figure 24: Transfer characteristics of the SAG TFT based on a PHDA SAM dielectric with CVD-grown graphene as the active layer - (A) Positive drain voltage (B) Negative drain voltage.

The poor performance of the graphene devices tested thus far was attributed to the presence of residual water molecules on the surface of the graphene which were introduced during the transfer process of the graphene onto the self-aligned device architecture [52]. In an attempt to remove any impurities from the device, they were annealed at 150°C for 24 hours on a hot plate in a nitrogen environment, and the device characteristics were re-measured after the device cooled down to room temperature. The

transfer curves for different positive and negative drain voltages are shown in (**Figure 25**). One of the most significant changes is the carrier mobility, which nearly doubles to 377 cm^2 /Vs, along with a 1.5x increase in drain current. These values more closely match those reported for similar micron-sized device architectures and demonstrate the viability of the self-aligned gate structure for graphene based devices.

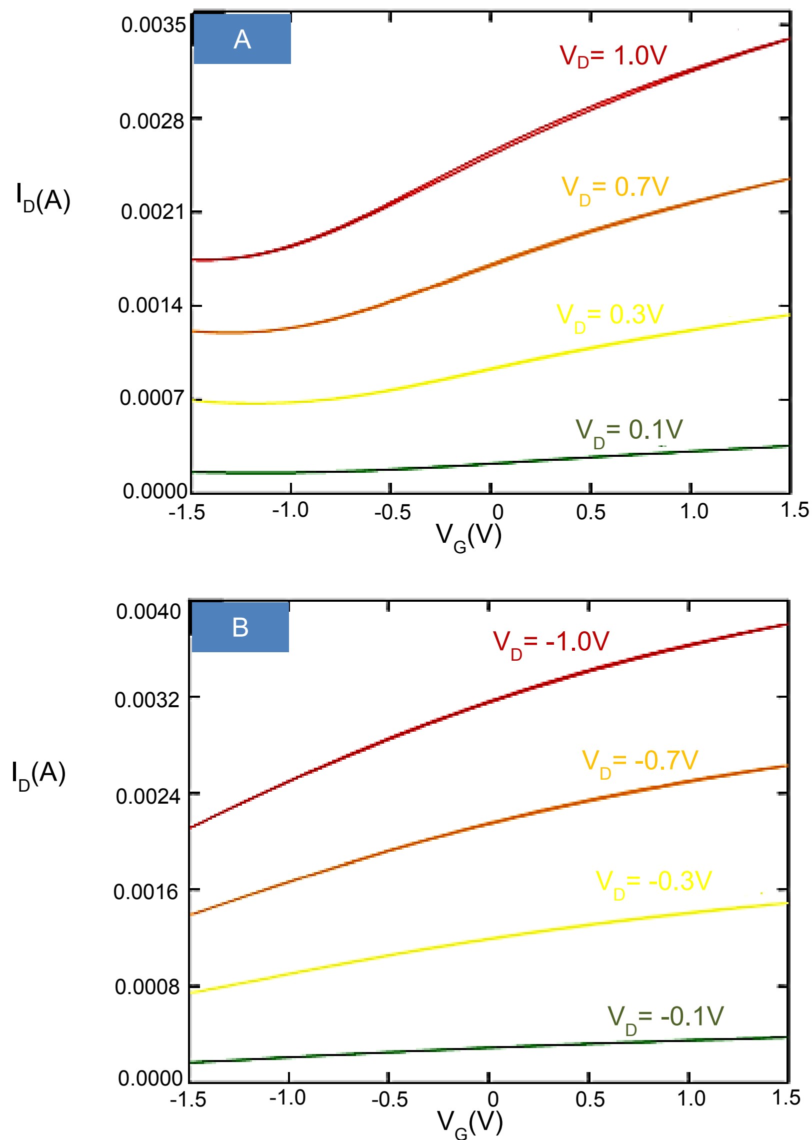


Figure 25: Transfer characteristics of the SAG TFT based on a PHDA SAM dielectric with CVD-grown graphene as the active layer after thermal annealing at 150°C (A) Positive drain voltage (B) Negative drain voltage.

These initial results outline the possibility of fabricating working devices using the self-aligned gate architecture using a variety of different dielectrics and semiconductors. Further work is required to assess the efficiency of the devices and to determine the performance benefit of the reduced source, drain and gate overlap. The results presented above are intended to show the developed architecture is capable of producing operating devices, rather than be an exhaustive characterisation of the tested devices.

5.4 Nano-scale SAG structures

OFETs with channel dimensions less than 500 nm have been reported for applications where high frequency (> 100 MHz) operation is required [53]. The formation of sub-micron channels is challenging and for large area devices has typically been accomplished using either self-aligned inkjet printing [53], electron beam lithography [54] or stamping techniques [55]. Short channel effects, such as increased contact resistance can dominate at such dimensions, meaning channel scaling, dielectric thickness and contact alignment must be considered during fabrication to insure devices operate correctly. The self-aligned lithography method as specified above was limited to channels widths of 20 μm since the contacts were deposited by shadow masking which suffers from shadowing. Based on an adaptation of self-aligned inkjet printing [16] we report here a method for fabricating simple photo-lithographic masks with short channel dimensions ranging from 1 μm to 200 nm. The masks serve as a low cost alternative to expensive high resolution photo masks which are supplied by specialist manufacturers. Moreover, as they are fabricated by inkjet printing, in principle, there is no limit to the size of the mask that can be produced. The following work was undertaken within Professors Peter Ho's group at the National University of Singapore.

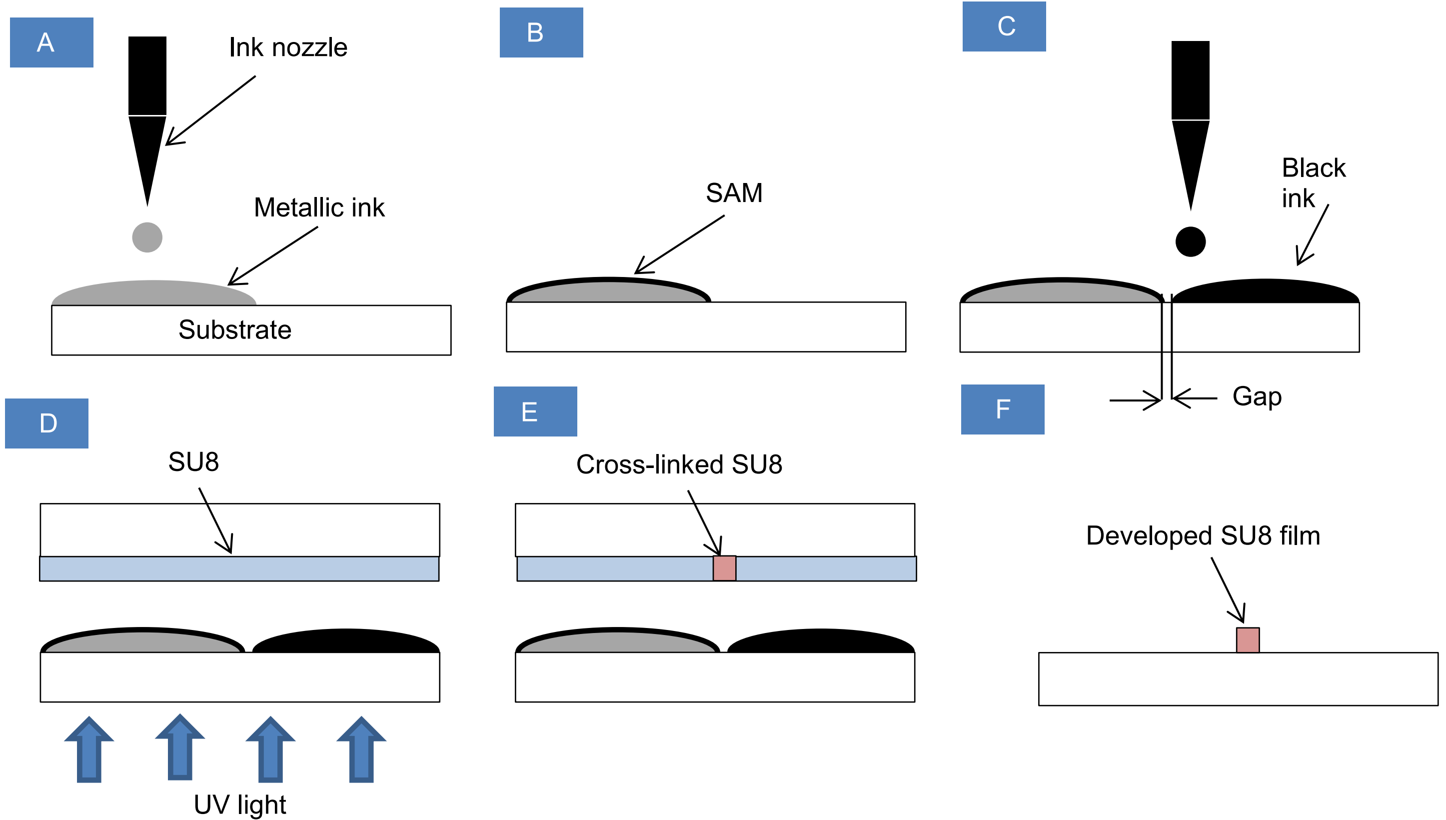
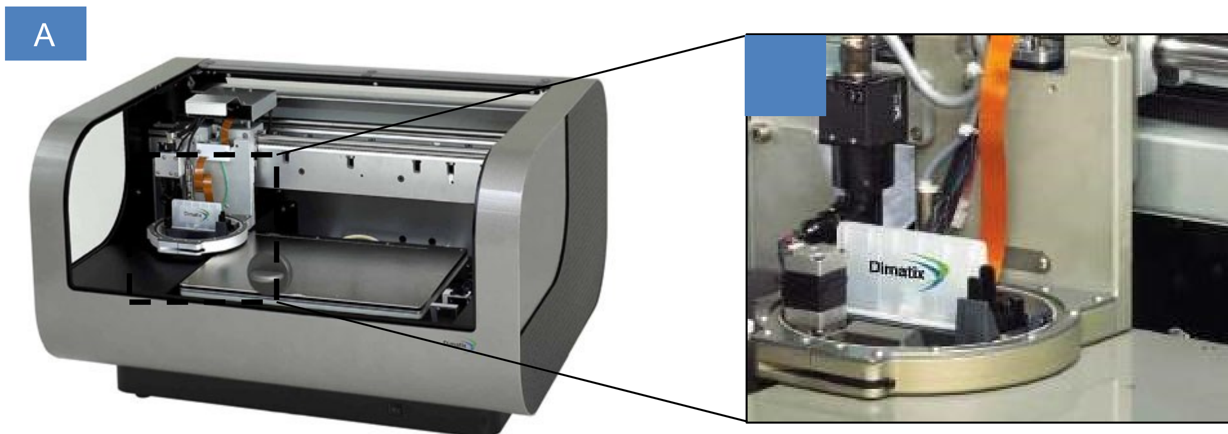


Figure 26: Schematic of the fabrication process for the nano-scale self-aligned lithography mask. (A) First a metallic ink is deposited using inkjet printing in the desired pattern. (B) A SAM is then applied to the metallic ink resulting in a difference in surface energy between the substrate and ink. (C) A black ink is printed over the top of the silver ink such that it rolls-off the edge of the silver ink, forming a small gap between the two. (D) After drying dried the substrate can be used as a photo mask. In this configuration a SU8 film is placed above the mask and exposed with UV light. (E) SU8 is cross-linked through the gap in the two ink droplets such that in the final step (F) the SU8 can be developed into a free-standing structure a few hundred nm in width.

The method, depicted in **Figure 26**, uses a printed metal line to which a hydrophobic SAM is applied. A second opaque ink is printed over the top of the initial metal line and due to the presence of the hydrophobic SAM the second ink drop "rolls-off" the metal line. When the ink has fully dried, it is separated from the metal line by a narrow gap between the first and second printed line that can be used for photolithographic patterning. The width of the gap depends on the composition of the ink and the type of SAM used, but, previous reports for silver ink have shown typical separations of between 100 nm and 500 nm [30].



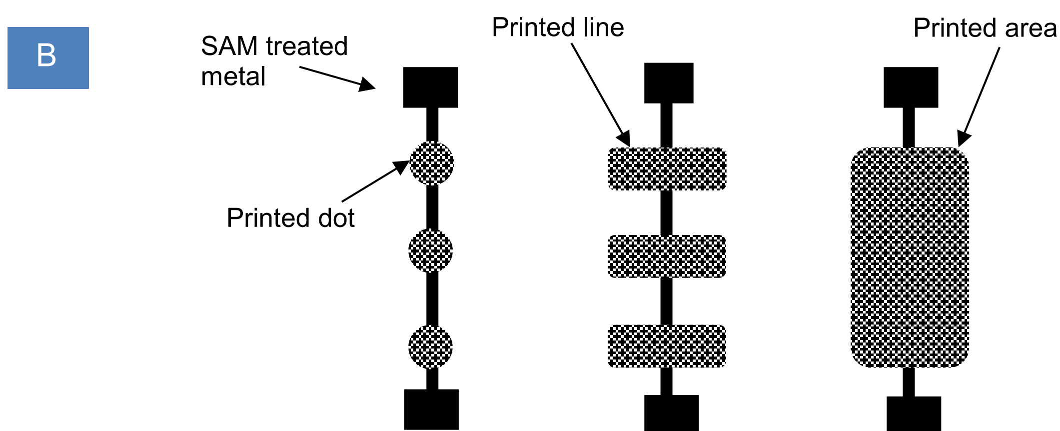


Figure 27: (A) Photograph of a Dimatix DMP-2800 digital inkjet printer typically used for printing high resolution patterns. (B) An enlarged view of the print head and ink cartridge used for printing. (C) Schematic of the three different patterns which were printed over the SAM-coated electrode. The first pattern printed was an array of single droplets printed over a thermally evaporated metal electrode; the second pattern was an array of lines a few centimetres long printed over the thermally evaporated metal electrode (the 'line' is a series of droplets printed in close concession) and the final pattern was a continuous area of ink printed over the entire metal electrode.

Using aqueous ink and a "drop-on-demand" inkjet printer (Dimatix DMP-2800 – **Figure 27**), it is possible to print patterns with a high dimensional accuracy (± 10 µm). In initial testing the metal line was deposited by thermal evaporation to ensure the roll-off effect described above was possible. Black ink purchased from Hitachi IPL was used for printing [56]. The ink is specially formulated for printing on glass surfaces and is heat resistant up to 1300 °C when fully dry.

To ensure the ink was sufficiently opaque for use as a photo-mask, a glass substrate was first coated uniformly with the ink, allowed to dry and placed over a SU8 coated glass slide. The substrate was then exposed using a mask aligner. The SU8 underneath did not cross-link under standard mask aligner exposure conditions [23], and was completely removed when placed in the SU8 developer confirming the black ink could be used as a photo-mask as it effectively blocks UV light. **Figure 28** shows the results of printing black ink over thermally evaporated Al and Au electrodes when no SAM monolayer is present. The similarities in wetting between the substrate and electrode cause the black ink droplet to form a continuous line in direct contact with the metal. This is expected since gap formation with the metal can occur only after wetting of either the substrate or metal electrode has been modified [30].

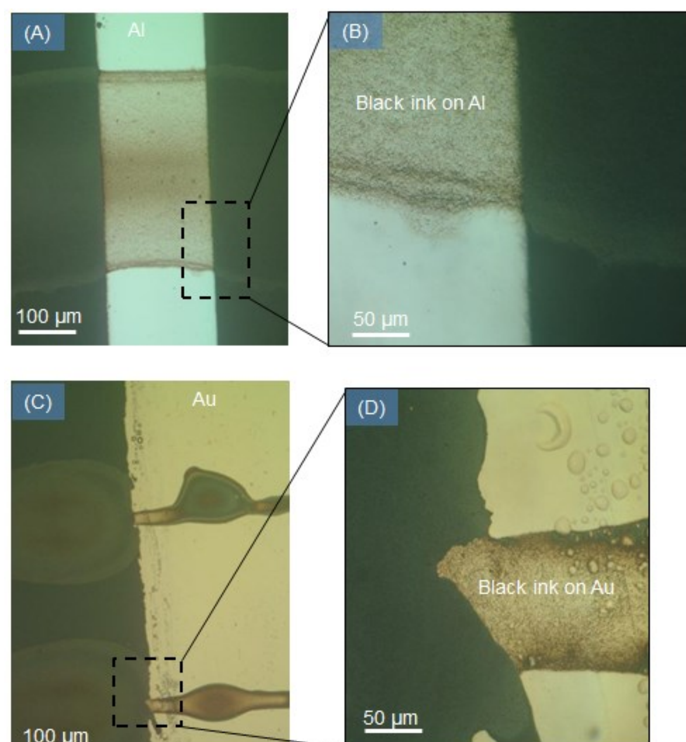


Figure 28: Micrographs of black ink printed onto (A) Al and (C) Au when no SAM has been applied, (B) and (D) show enlarged areas of the Al and Au respectively. The micrographs demonstrate no gap is formed when the ink is printed over the initial electrode.

To modify the surface energy of the Al electrode, ODPA was applied to the Al electrode using the technique described in Chapter 4. The formation of the SAM monolayer was confirmed by visually contact angle measurements where the surface became increasingly hydrophobic. Initially the black ink was printed over the Al line pattern using discrete droplets of approximate diameter 5 µm, to determine if the ink would roll off the line pattern (**Figure 29 A**). The ink clearly rolled off the SAM coated electrode and dried in close proximity to (but not touching) the edge of the Al (**Figure 29 B,C**). Several drops were printed and this effect was consistently observed. The average separation of the metal and ink was determined to be 6 ± 0.7 µm. This is higher than the sub-micron values previously reported and is most likely due to the SAM attaching to the glass substrate.

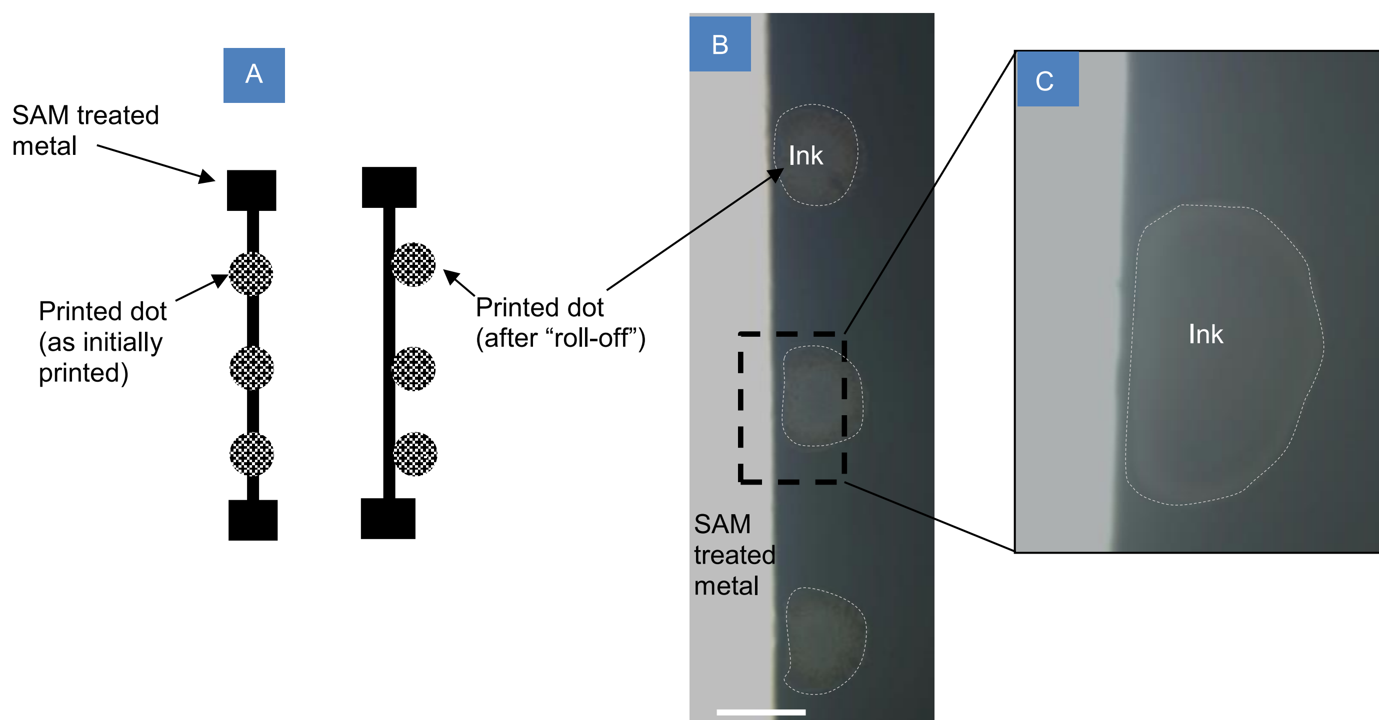


Figure 29: (A) Schematic depicting closely spaced ink drops which are printed on the substrate adjacent to the SAM-coated electrode. (B) Micrograph of three printed ink droplets which have successfully rolled off the edge of the electrode along with an enlarged section of one of the drops after the electrode was coated with ODPA (C). The ink has been highlighted to aid visual inspection in (B) and (C).

To further evaluate the technique, elongated line patterns of approximate dimensions 1 x 2 cm were printed over both ODPA coated Al and ODT coated Au. The SAMs induced a roll off effect of the black ink for both the Al and Au line patterns. The separation of the ink against the Al electrode was reduced to 3 ± 0.4 μm (**Figure 30**), while it was not possible to record a value for the Au electrode using an optical microscope as the gap was too small.

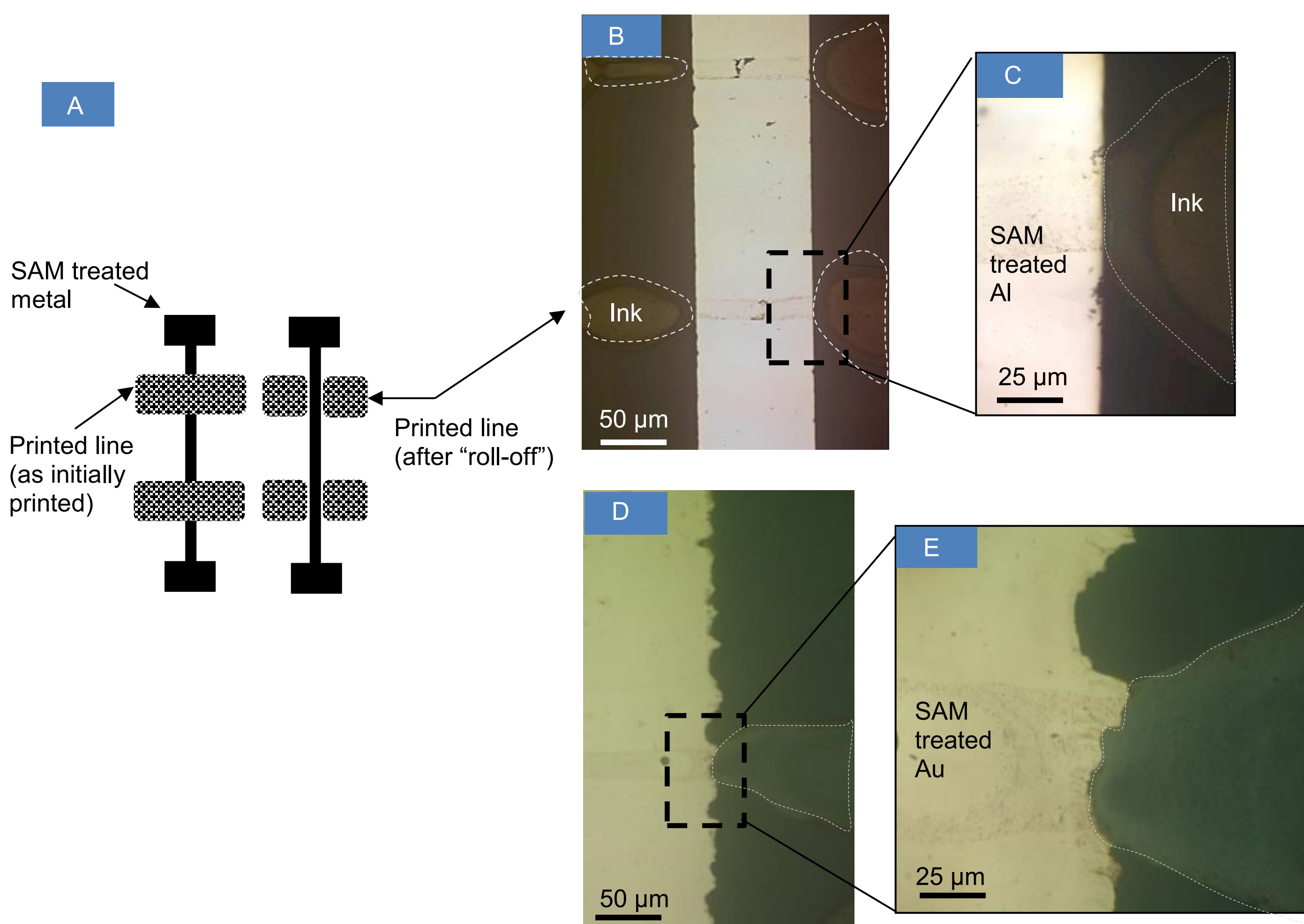


Figure 30: (A) Schematic depicting deposition of lines of black ink on the SAM-treated metal electrode. (B) Micrograph of an ODPA treated Al electrode after deposition and drying of the black ink; the ink can be seen to have rolled off the metal and formed two droplets on either side of the line; an enlarged area is show in (C). Micrograph of an ODT-treated Au electrode after deposition and drying of the black ink. The Au line was formed by masking areas of a substrate with tape and hence the line is rougher then the Al line which was deposited via shadow masking. Despite the rough edge, the ink rolls off the SAM coated metal and is tightly aligned against its edge, as can be seen in the enlarged image (E). The ink has been highlighted to aid visual inspection in (B) and (C).

As can be seen in the highlighted areas of **Figure 30**, the ink dried in close alignment to the jagged edges of the metal. The Al image in **Figure 29** and **Figure 30** show that it is preferable to print a line over a dot. While the dot quickly rolls off the metal, the line takes longer to re-align and in the process dries closer to the edge of the metal. The smaller gap width in the case of the Au is due to the thiol SAM not attaching to the glass substrate. As such when the ink droplet "rolls-off" the electrode the low surface energy of the substrate does not encourage further "roll-off" of the ink but is rather more likely to encourage the ink to dry next to the Au electrode.

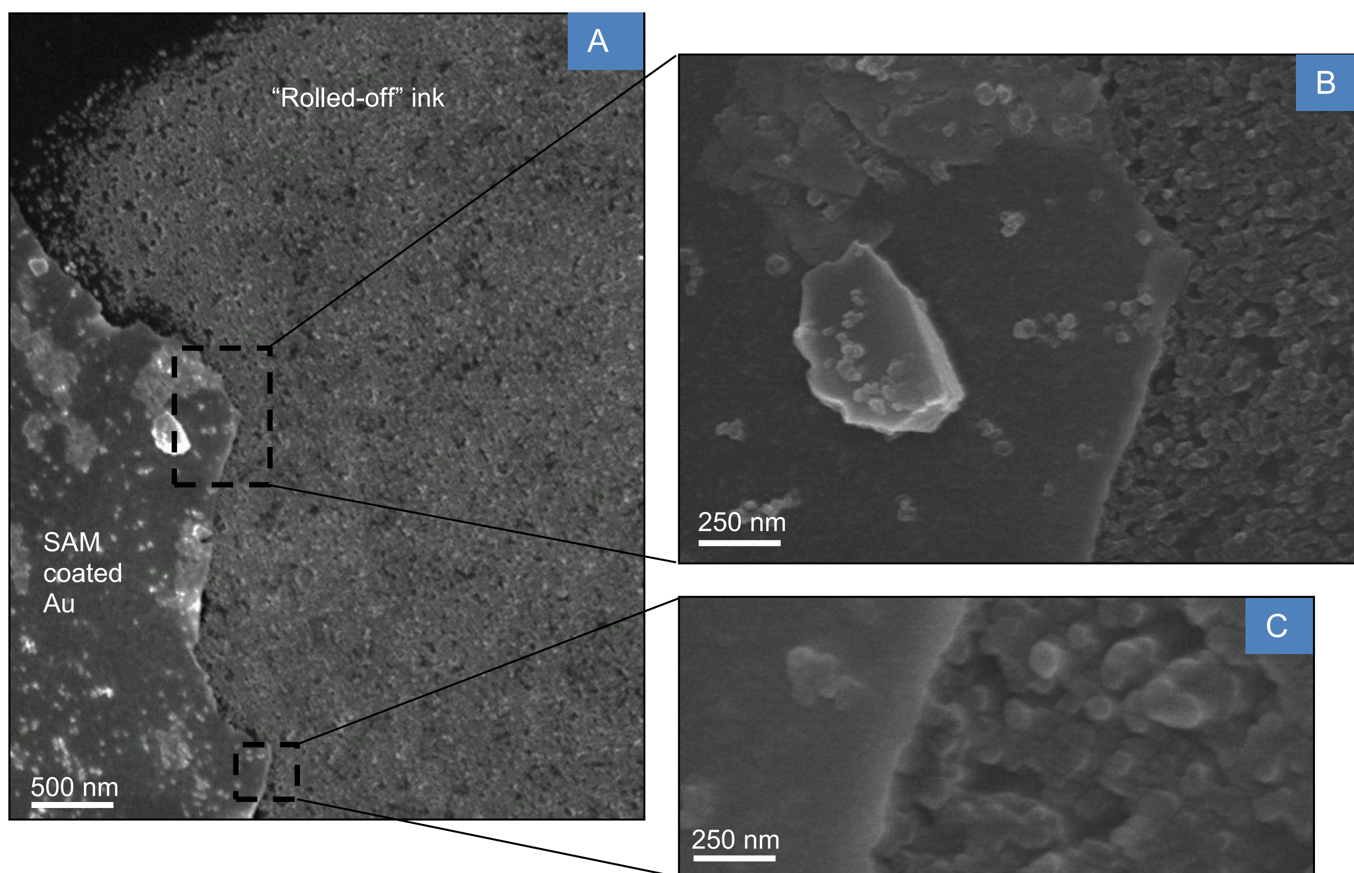


Figure 31: (A) SEM micrograph of the Au substrate seen in **Figure 30**. The SEM shows the interface of the ink droplet and the Au electrode .The separation of the two materials is less than 100 nm, as can be seen by the enlarged areas highlighted in (B) and (C).

To evaluate the separation achieved for the Au electrode high magnification SEM micrographs were recorded, the results for which are shown in **Figure 31**. The separation of the metal and ink was smallest at the centre of the droplet, where the majority of the ink accumulated during drying. As can be seen in **Figure 31 B** and **C** the separation is not apparent even at close magnification. The results are promising, and suggest self-aligned inkjet printing could be a viable way to produce sub 100 nm masks.

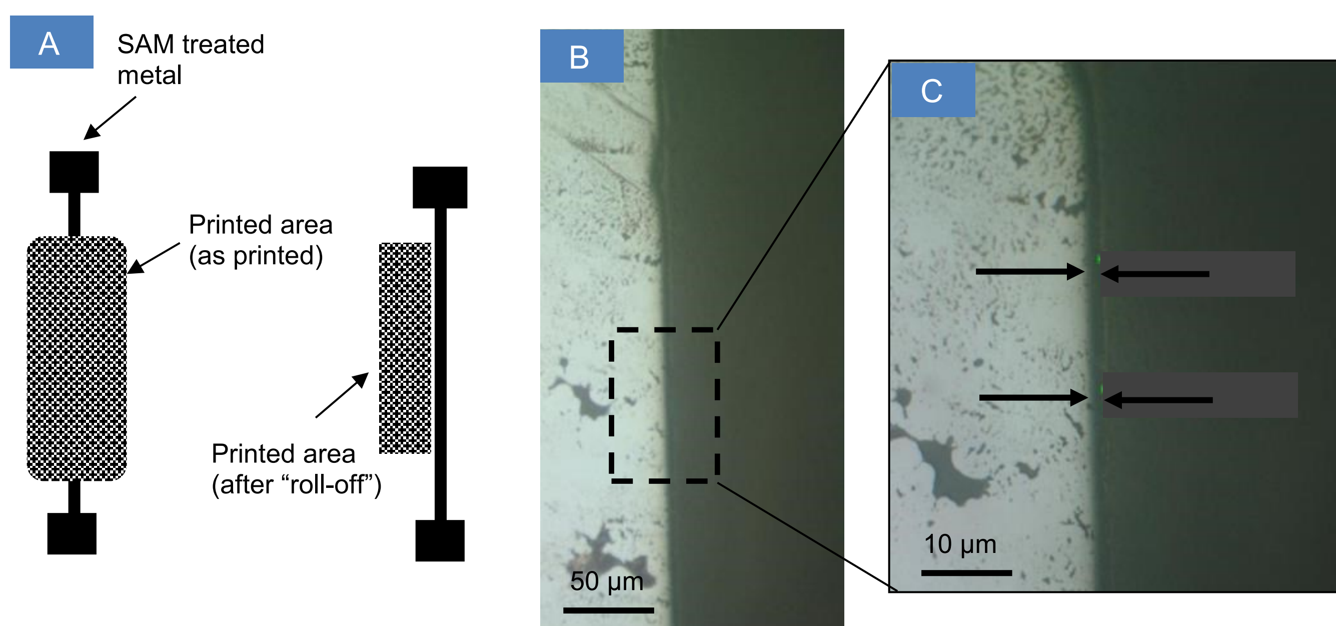


Figure 32: (A) Schematic depicting the large area ink pattern to be printed. The pattern was formed by passing the print head over the electrode multiple times. (B) Micrograph of an ODPA coated Al line pattern after printing has occurred. The separation of the electrode and ink is apparent and can be seen in the enlarged area of (C). The arrows on (C) indicate the location of the gap between the two materials.

The final printing pattern investigated was a large-area continuous sheet. This was formed by rastering of the printer backwards and forwards over the electrode. This pattern is the most useful to study as larger areas must be printed to obtain usable lithography masks rather than the small areas demonstrated above. The 1.3 ± 0.3 μm gap seen in for this pattern is smaller than was previously recorded using the line pattern for the ink (**Figure 32**). While the gap was still limited by the presence of some residue

ODPA on the glass slide, the gap appears uniform and well defined. This configuration could be used to produce masks with channel dimensions ~1 µm representing a good medium between more expensive methods of defining lithography masks and the ability to produce on demand templates and line patterns.

5.5 Conclusion

By using negative tone photoresists combined with back illumination of an evaporated gate electrode, it was possible to produce self-aligned devices with channel dimensions as small as 20 µm. The success of the patterning procedure was found to be highly dependent on the way the substrate was developed as over sonication easily damaged the OFET structure. It was demonstrated that over-developing the photoresist resulted in a small overlap of the source and drain electrode that lead to more efficient charge injection . Working devices were tested using C_{60}, graphene semiconductors and SAM and SU8-based dielectrics, with initial results suggesting these devices had on par-performance with similar non-aligned devices. By fabricating working organic devices using proven organic semiconductors and dielectrics, the technique was validated as a viable method for the fabrication of self-aligned transistors without the need for high precision alignment.

Additionally work was undertaken to investigate methods to downscale the back illumination technique using high resolution printed shadow masks fabricated by ink-jet printing. Preliminary results indicate inks can be used to aid the formation of nano-scale shadow masks using SAMs to induce a 'roll-off' effect of the ink. The resulting gap between the SAM and the ink can later be used to fabricate nano-scale shadow masks

without the use of electron beams or complex lithographical steps. Initial results suggest it may be possible to control the gap formed by the roll-off effect such that a variety of sizes can be formed.

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6 Conclusion and further work

This thesis describes advances in the fabrication of organic electronic devices. Research was undertaken on methods to downscale devices using techniques that are well suited to the large area fabrication of organic devices on rigid and flexible substrates. The emphasis throughout was on developing innovative methods which do not require expensive equipment and are compatible with existing fabrication technologies. The following section summarises the findings presented in this thesis and offers new avenues for further work which can be conducted.

6.1 Conclusion

The first experimental chapter outlined the effects of self-assembled monolayers (SAMs) coatings and heat treatments on the adhesive properties of polymers and metallic thin films. After studying the reaction of metallic films which had been treated with various SAMs, it was determined the coatings could significantly alter the adhesion and wetting properties of the underlying metallic film. It was also found that, by controlling the curing conditions of a polymer (BCB), the adhesion properties could be changed. Contact angle measurements were used to gain a macroscopic understanding of the wetting properties of the films, while friction force AFM was used to investigate adhesion forces at the nano-scale. Although friction force AFM is not commonly used in this manner; it was possible to measure differences in the surface

adhesion of the various films on the pico-Newton level. The above experiments indicated that hydrophobic SAMs such as ODPA and ODT lower the adhesion properties of the metallic films to which they are attached, while hydrophilic SAMs do the opposite owing to differences in the chemical composition of the SAM's tail group. Similarly, by controlling the degree of crosslinking in a polymer film (BCB), the adhesion to metal films may be varied. The uniformity of the wetting profile of the polymer film indicated the heat treatment acts uniformly across the film, making it well suited to large area fabrication. With SAM-coated films it can be difficult to achieve uniform coverage as has previously been documented [1]. However recent progress has been made to increase coverage through the use of co-solvent mixtures, which stabilise the SAM tail when deposited [2]. Such deposition techniques may offer interesting avenues for further investigations to improve fabrication yield by improving the uniformity of the surface adhesion profile.

Based on the understanding gained of the adhesive properties of various materials in the first half of the chapter, it was determined these adhesion properties could be used for patterning nano-scale features, using a technique that we call "adhesion lithography". It was found that, by coating one metal with a low adhesion SAM, it was possible to selectively remove a second thermally deposited metal deposited on top of the SAM-coated metal by placing a higher adhesive interface (such as tape or glue) upon the second metal and peeling back. Critically (after the peeling process occurred) the second metal remained in areas where no SAM had been deposited. After peeling, the two metals sit side-by-side separated by a small nano-scale gap. To develop this technique, several variations were explored. Initially simple patterned features were fabricated using thermally evaporated line patterns several

millimetres wide on glass substrates. It was not initially possible to achieve high fidelity patterning on this configuration, as the substrate adhesion was found to be too low to allow successful peeling to occur, resulting in the removal of the entire film. To understand the forces involved during peeling, and so ultimately be able to fabricate working devices, peel testing was used to measure the peeling forces. While peel testing is more commonly used to evaluate surface coatings and adhesive tapes for the much larger forces typically found in industrial applications, for this work a custom-built peel tester was fabricated using a specialist low-loading force gauge and precision linear stage. Using this equipment, it was possible to determine the nano-scale adhesion forces acting along the patterned films. Based on these measurements, it was possible to identify a low adhesion glue, which more closely matched the peeling forces present when peeling occurred. This, in addition to enhancing the surface adhesion of the glass substrate, enabled successful patterning to occur.

In initial attempts, I was unable to form a nano-scale gap as the first metal was deposited via shadow masking, which produces sloped and poorly defined sidewalls. By using photolithography, higher resolution patterning could be achieved as fracturing of the two metallic films could then occur against a well-defined edge profile. The formation of an inter-granular fatigue point at the interface of the low adhesion SAM-coated metal electrode (M1) and the second metallic film (M2) was confirmed using AFM. Fracture was preferential at this interface during peeling, as the film already had a pre-defined 'weak-point' between the films. When the initial electrode was deposited via photolithography, the gap between M1 and M2 was recorded using SEM to be as small as 12 nm. Previous reports of such small asymmetrically aligned electrodes have typically involved the use of much more complex and expensive fabrication equipment

such as electron beam lithography. In the case of more scalable techniques such as chemical lithography [3] or controlled cracking [4] nano-gaps have only been demonstrated on smaller areas with poor reproducibility. Using adhesion lithography aspect ratios in excess of 100,000 were achieved, demonstrating the possibility to use the technique over large areas. The versatility of the technique was further demonstrated by using different combination of SAMs and metals for M1 and M2. It was found that, through judicious selection of the SAM and metals, the adhesion lithography method could be applied to a variety of material combinations.

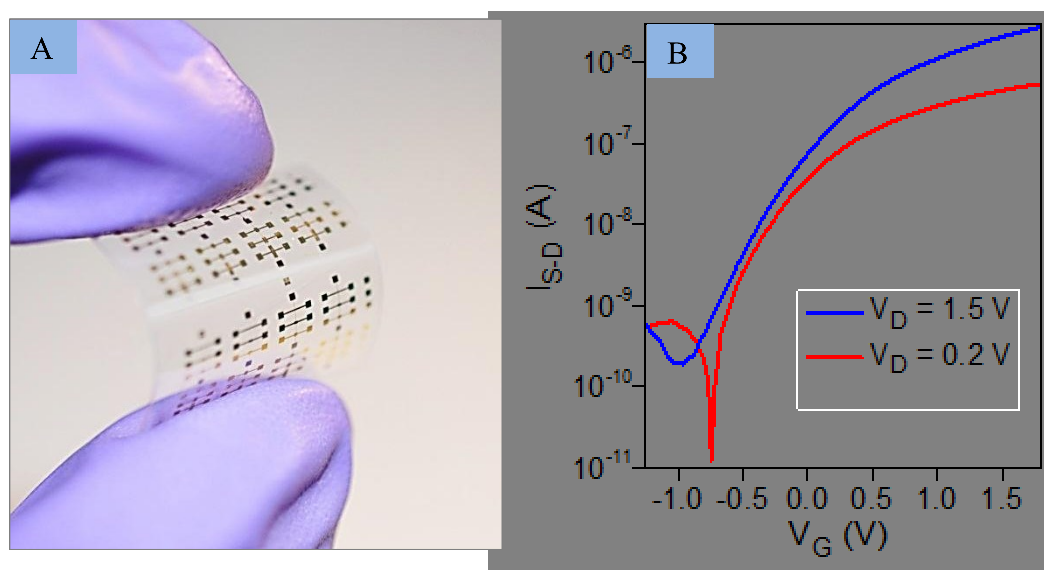

Figure 1: (A) Photograph of a self-aligned OFET fabricated using the adhesion lithography process on a flexible substrate. (B) The associated transfer characteristics measured for an In_2O_3 transistor. The device channel width and length are 400 µm and 30 µm, respectively. The device shows good current on/off ratio (>10^3) with maximum electron mobility values exceeding 2 cm^2/Vs.

Once well-aligned nano-scale electrodes were fabricated, the ability of the structures to be used in working devices was investigated. Photodiodes were fabricated using PCBM:P3HT as the active layer. As shown in the latter half of Chapter 4 a clear photodiode response was recorded proving the adhesion lithography technique can be

successfully used to fabricate working devices. Since this work was completed, further research has been undertaken by James Sempel at Imperial College London to develop organic electronic devices using the adhesion lithography technique. Using the methods developed in this work, it has been possible to fabricate working self-aligned OFETs with nano-scale alignment (**Figure 1**).

The second experimental chapter outlined methods to produce aligned OFETs by fabrication methods which are compatible with large area processing techniques. Typically the equipment used to fabricate nano-scale electronics is poorly suited to the fabrication of large area as they require high precision alignment which is difficult to control over large areas. The method demonstrated in this work does not use such equipment to produce self-aligned OFETs and could pave the way for low-cost, large-area devices.

The proposed fabrication method for the self-aligned device used negative tone photoresists combined with back illumination of an evaporated gate electrode to develop highly aligned devices. The proposed structure resulted in separation of the source, drain and gate. It was realised that this may not be sufficient to allow charge injection in the device. As such the method was modified to use thinner layers of photoresist to reduce the vertical offset. In addition the interlayer was deliberately overdeveloped to ensure the source and drain were overlapped with the gate. While the latter effect may reduce the speed of the device, as some degree of overlap is present within the OFET structure increasing the capacitance, it ensures the three electrodes are connected and able to inject charges more directly as outlined in ref [4] and [5]. Additionally, if fabricated on flexible substrates, the overdevelopment will ensure the

structure will stay in contact when the substrate if flexed. If the contacts are only just touching when the substrate is flat then when the substrate is flexed the source and drain may become separated during bending.

The success of the patterning process was found to be highly dependent on the way the substrate was developed as over-sonication easily damaged the OFET structure. By modifying the development process to reduce harsh vibrations on the substrate, the development could be better controlled, and it was possible to produce self-aligned devices with channel dimensions as small as 20 μm. Several working devices were fabricated and tested using C_{60} or graphene for the semiconductors and a SAM or SU8for the dielectrics. Initial results showed these devices had on par-performance with similar non-aligned devices. Work has since been undertaken by Minho Yoon at Imperial College to further develop this technique using similar methods.

Finally attempts to downscale the back illumination technique using high resolution printed shadow masks were conducted using ink-jet printing. Preliminary results indicate inks can be used to aid the formation of nano-scale shadow masks, using SAMs to induce a ‘roll-off’ effect of the ink. The resulting gap between the SAM and the ink was later used to fabricate nano-scale shadow masks without the use of electron beams or complex lithographical steps. Initial results suggest it may be possible to control the gap formed by the roll-off, enabling smaller channel lengths to be fabricated over large areas.

6.2 Further work

Both adhesion lithography and the self-aligned gate architecture have been shown to be viable methods to fabricate various electrical devices on the micro and nano-scale. Further work in both areas is already underway at Imperial College, as outlined above.

Issues which need to be addressed for adhesion lithography are further improvements in the size and uniformity of the nano-gap, along with greater control of the gap length between M1 and M2. This is needed as modern nano-electronics has a high requirement for reproducibility. Additionally greater attention needs to be given to control of the adhesion forces acting between the substrate, M1, M2 and the SAM during deposition as it is likely that small differences in the deposition conditions between the various layers can reduce device yield during peeling. By focusing on greater process control and reproducibility it may be possible to further reduce gap size between M1 and M2, possibly to the length of the SAM which is just a few nano-meters.

Devices produced using the self-aligned gate technique may enable fast, larger area electronics to be produced using simple processing equipment on "roll-to-roll" equipment. However, further work should be undertaken to determine how much "over-crosslinking" is needed to ensure good contact is formed between the source, drain and gate. Additionally the technique needs to be tested using more semiconductors and dielectrics.

If these issues are addressed it is likely that both adhesion lithography and the self-aligned gate technique could find widespread use in both research and industrial applications.

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Appendix

Journal articles

Beesley, D. J. *et al.* Sub-15-nm patterning of asymmetric metal electrodes and devices by adhesion lithography. *Nat. Commun.* 5:3933 doi: 10.1038/ncomms4933 (2014).

Awards

Beesley, D. J*,* Adhesion lithography for nano-scale electronics, overall winner, EPSRC UKICT pioneers (2013).

Conference proceedings

Beesley, D. J. *et al.* High performance large area electronics using self-aligned gate OFETs (oral), at Materials Research Society (MRS) Fall Meeting, Boston, USA, 2011.

Beesley, D. J. *et al.* Adhesive patterning for nano-scale electronics (poster), at Materials Research Society (MRS) Spring Meeting, San Francisco, USA, 2013.