"GAIN SENSITIVITY OF LINEAR ACTIVE NETWORKS"

by

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a Thesis submitted for the Degree of

DOCTOR OF PHILOSOPHY

of the

UNIVERSITY OF LONDON

Department of Electrical Engineering,

Imperial College of Science & Technology,

August 1966.

"How can you explain the fact that our men use the same materials to build identical cars yet some are faster than others? I am convinced that each one of our cars has its own individuality - a soul."

Enzo Ferrari.

ABSTRACT

In this thesis, the two-port tuned amplifier is analysed both in the conjugately matched and the mis-matched modes, with the aim of obtaining a set of conditions for the optimum gain-sensitivity performance of the amplifier.

The analysis is carried out in a three-dimensional space whose axes are the real and imaginary parts of the inverse of the measure of non-reciprocity and the inverse of the unilateral power gain. The actual power gain of the two-port is represented by a series of surfaces on each of which power gain remains constant.

Spreads in a batch of active two-ports are expressed in terms of departures of a point from the surface representing the power gain of the average two-port in directions parallel to the axes. Conditions are derived which express the maximum initial departure from the initial average power gain in terms of the initial spreads and the required average power gain. Thus it is possible to test at the very outset whether a batch of two-port active networks (transistors) can be used to build amplifiers given the gain-sensitivity condition as $G \pm \Delta G$, where G is the required average power gain and ΔG is the maximum tolerable deviation.

Two basic types of feedback are suggested and their performance vis-a-vis gain-sensitivity for various types of spread

in the four-dimensional space are compared.

Geometrical models are used to illustrate the concepts involved in the employment of the three-dimensional space and the movement of a point which represents a particular active two-port network in the space with feedback. Statistical methods are used in processing data collected from a batch of transistors and finally, the theoretical results are verified by measurement.

ACKNOWLEDGEMENTS

The author wishes to express his deep gratitude to his supervisor Dr. R. Spence of the Electrical Engineering Department, Imperial College, London, for his encouragement and guidance during the course of this work. He also wishes to thank his colleagues in the Circuit Theory Laboratory in particular E.J. Purslow, H.Y. Chow, V. Arandjelovic and B.Y. Ozal and also J.W. Bandler of the Microwave Laboratory for many hours of interesting discussion on the philosophy of circuit theory and other unrelated topics.

Financial support provided by the Ministry of Aviation (Royal Aircraft Establishment) in the form of a research contract is gratefully acknowledged.

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LIST OF PRINCIPAL SYMBOLS

Symbol or Abbreviation	Definition	First used on Page
h	hybrid two-port matrix parameters	19
g	hybrid two-port matrix parameters	19
Z	impedance, two-port matrix parameters	19
Y	admittance, two-port matrix parameters	19
p	general two-port matrix parameters	19
L	magnitude of $p_{12}p_{21}$	20
M	real part of $p_{12}p_{21}$	20
N	imaginary part of $p_{12}p_{21}$	21
k_i	Stern's stability factor	20
S_i	invariant stability factor	21
η_i	inherent stability factor	21
ϕ_i	invariant stability figure	21
U	unilateral power gain	22
$\underline{\lambda}$	complex measure of inverse of non-reciprocity	24
G	power gain (conjugate matched)	3
ΔG	change in gain	3
IGS	inverse gain space	34
$\Delta\lambda_R$	spread in the real part of $\underline{\lambda}$	37
$\Delta\lambda_I$	spread in the imaginary part of $\underline{\lambda}$	37
$\Delta(1/U)$	spread in 1/U	37
μ	sensitivity of gain	39

S	fractional change of gain	41
X	degree of mismatch	56
R	real part of 'Z'	20
X	imaginary part of 'Z'	20
ρ	real part of 'Y'	19
σ	imaginary part of 'Y'	19
a	magnitude of V_1/V_2	71
α	angle of V_1/V_2	71
Re(p)	real part of p	56
ρ_1	$\rho_s + \rho_{11}$, real part of immittance of port 1	20
ρ_2	$\rho_L + \rho_{22}$, real part of immittance of port 2	20

LIST OF PRINCIPAL SUBSCRIPTS

Symbol	Subscripts Refer to	First used on Page
i,k,l	points on average gain surface	37
j	point not on average gain surface	37
av	average	47
lo	lower	47
up	upper	48
I	imaginary part of	24
R	real part of	24
s	source	19
L	load	19
t	transducer	19
n	negative	74

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Chapter 1

INTRODUCTORY BACKGROUND

1.1 INTRODUCTION

In order to study the behaviour of active networks, many electrically equivalent circuits have been developed to illustrate how they work.[1,2] Relatively simple forms exist for specific applications but to make these at all realistic over a frequency band or for general purposes, it has to be quite complicated. The usefulness of equivalent circuits is limited in so far as it makes relatively simple calculations of say gain of an amplifier in which the active device will be used, an extremely lengthy operation.

An alternative way of dealing with active devices is to treat them as 'black boxes', that is to determine their electrical properties in terms of applied voltages and currents at its terminals at a particular frequency thus avoiding involvement in the inner workings of the device.[3-6] The electrical properties are usually defined in the form of open-circuit impedances (z-parameters), short-circuit admittances (y-parameters), or a mixture of the two which is generally described as hybrid parameters. Other characterizations exist for special purposes such as a- and b-parameters for cascade connection.[7]

A two-port network, as the name implies, is an electrical network which has two 'ports' or terminal pairs. One port is described as the input port and the other as the output port. A port is any pair of leads in the network through which current, voltage or power can be fed or extracted. Normally, the signal obtained from the output port is a transformation of what goes into the input port. A large number of electrical networks fall under this classification, for example, transmission lines, filters, amplifiers and attenuators.

A large number of two-ports have only three terminals. Thus the input and output ports have to share a common lead which is normally, but not necessarily, connected to ground. The transistor is one example of this group. The mathematical techniques for dealing with these three-terminal two-ports include the use of matrix algebra.[8] The device can be represented by a 3 x 3 matrix which does not indicate which of the three terminals is the common terminal. To obtain a particular configuration of the two-port, the row and column representing the appropriate common terminal is removed and what is left describes the two-port completely.[9]

1.1.1 Sensitivity

Sensitivity problems arised in every field of engineering.

It is impossible to manufacture identical parts to be used in any system and therefore the designer must take into account the ultimate effect of the imperfections of the elements which make up the system. For example, the designer cannot afford to design an amplifier and then discover that when a batch of these are built in the factory, some of them give a gain of, say, 30 db, others give only, say, 10 db and worse still others become unstable and oscillate, just because the elements used have tolerances on their nominal values. The problem of sensitivity is therefore a problem of the cumulative effects of tolerances on the response of the system as a whole.

1.2 CHOICE OF THE TRANSISTOR

In this thesis, the two-port active network is taken to be a junction transistor operating under conditions of small signal and therefore in a linear fashion. Biasing is accordingly arranged.

Quite apart from the ordinary advantages of using transistors as active devices such as small physical size and low power consumption, the transistor has a finite input impedance and even at low frequencies it is non-unilateral.[10-13] These two properties of the transistor make it a good choice for a general study of

two-ports as the conclusions reached can be made applicable to other two-ports by setting the appropriate parameters to zero or infinity.

1.3 HISTORICAL BACKGROUND

In 1929, Strecker and Feldtkeller[5] published a paper in which they analysed two-ports by means of matrix algebra. Three years later, Baerwald[6] carried the work of the two gentlemen further by showing its application to various passive bilateral networks. The next significant work was published by Guillemin[3] in his book on communication networks in which he dealt with among other things the inter-connection of two-ports. Seven years passed before Peterson[14] extended the matrix algebra technique to active non-bilateral two-ports.

The name 'two-port' was first used by Wheeler and Dettinger[15] in connection with a superhetrodyne convertor but has come to be accepted as adequate description for a large number of circuit units and elements.

Early attempts to use the transistor for amplification were hampered by the non-unilateral nature of the device i.e. the existence of internal feedback in the transistor. With some values of internal feedback, passive terminations at the ports can make the two-port oscillate. Further, the internal feedback

made the input impedance a function of the output impedance thus complicating the problems involved in cascading amplifiers since the tuning of the previous stages affected the tuning of subsequent stages. Many workers therefore attempted to unilateralise the transistor before using it in amplifier circuits.[10-13] But unilateralisation was not easy to achieve and among other things required an ideal transformer.[16] Several workers have since shown that unilateralisation is unnecessary for stable operation of a two-port amplifier.[13,16,17]

In 1946, Roberts[18] derived an expression for the transducer gain of the conjugately matched, as well as the arbitrarily terminated two-port. In 1961, Venkateswaran and Boothroyd[19] showed that the power gain expression for the arbitrarily terminated and the conjugately matched two-port amplifier maintains the same form in all matrix configurations. Thus the transducer gain

$$G_t = \frac{4 \rho_S \rho_L |p_{21}|^2}{\left|(p_{11} + p_S)(p_{22} + p_L) - p_{12}p_{21}\right|^2}$$

where $p = \rho + j\sigma$ and p can be in the form of Y-, Z-, h-, or g-parameters. Lathi[20] and Rollett[21] later derived the same expression.

The problem of stability which was mentioned above will now be discussed in a little more detail. In 1933, Gewertz[37] published the results of his work on reciprocal two-port networks in which he derived a condition for stability of the form,

$$R_{11}R_{22} - R_{12}^2 > 0$$

where the matrix of the two-port is of the form,

$$\begin{bmatrix} R_{11} + jX_{11} & R_{12} + jX_{12} \\ R_{21} + jX_{21} & R_{22} + jX_{22} \end{bmatrix}$$

In 1952, Llewellyn[22] extended Gewertz's condition to cover non-reciprocal networks. Llewellyn's conditions were:

$$R_{11} > 0 \ ,$$

$$R_{22} > 0$$

and

$$4(R_{11}R_{22} + X_{12}X_{21})(R_{11}R_{22} - R_{12}R_{21}) - (R_{12}X_{21} - R_{21}X_{12})^2 > 0$$

In 1956, Bahrs[36] derived an expression for the margin between the point of operation of a potentially unstable element, in a stable mode, and instability, which he called ρ. When ρ was greater than unity the device was stable. This was one of the first attempts to attach a numerical value to how far a device is from instability.

In the following year, Stern[26] derived the same condition but in a slightly different form. This has come to be known as 'Stern's stability criterion' and it is generally written in the form,

$$k_i = \frac{2\rho_1\rho_2}{L + M} > 1 \quad \text{for stability}$$

where $\rho_1 = \rho_{11} + \rho_s$ and $\rho_2 = \rho_{22} + \rho_L$

and

$$L = |M + jN| = |p_{12}p_{21}|$$

In 1961, Venkateswaran derived what he described as the 'invariant stability factor' S_i where,

$$S_i = \eta_i + \sqrt{\eta_i^2 - 1}$$

and

$$\eta_i = \frac{2\rho_{11}\rho_{22} - M}{L}$$

As before, when η_i is greater than unity, the two-port is said to be <u>inherently stable</u>, that is, no pair of passive terminations can be found which will make the two-port oscillate. When η_i is less than unity, the two-port is said to be <u>potentially unstable</u> and a pair of passive terminations can be found which will make it oscillate. This stability factor appeared in the work of several authors as different symbols. For example Lathi[20] called it the 'invariant stability figure' and used the symbol ϕ_i. Aurell[24] gave it the symbol k, and Linvill and Schimpf[25] called the reciprocal of η_i the 'critical factor', C.

In order to ensure that the two-port will not oscillate under all conditions of passive termination, although the two-port itself might be potentially unstable, Venkateswaran[23], Singleton and Scanlan[27] have shown that the value of η_i can be increased by the addition of

resistive elements at the input or output or both parts of the device. The device together with the 'pads' as they are generally called, can then be treated as a new device which is inherently stable.

An alternative way of dealing with the problem of using potentially unstable devices to produce useful and stable gain is to choose the resistive parts of the source and load such that Stern's stability criterion is satisfied. Venkateswaran and Boothroyd[19] using this technique derived an expression for power gain incorporating a 'performance factor' n. Later, Lathi[20] and a little later Spence[28] independently introduced the concept of 'skew factor' as a measure of the departure of the resistive part of the termination from the optimum determined by the choice of the performance factor n.

In order to discuss later developments, it is convenient to leave the design aspect for the moment and to introduce some achievements in the more theoretical aspects of the active network.

For a two-port to provide useful power gain, it must be 'active'. Mason[29] has shown that the unilateral power gain (U) of a device must be greater than unity if it is active. Mason also showed that the numerical value of U remained the same even with the change of the common terminal and that if the device is embedded in a lossless environment, U remained unchaged. Mason's U has been widely used in connection with two-port amplifiers and oscillators. Meadows and Dasher[30] have extended the concept of U for application to n-port networks.

Shekel[31] developed the idea of gyrators from the ideas of

Tellegen[32]. Since a two-port active network is only partly unilateral, Shekel[31] separated the unilateral part of the device, which is the gyrator, from the bi-lateral part which represents the reciprocal part of the device. In its admittance form, it consists of a delta of passive bi-lateral admittances whose nodes are connected to the three terminals of the gyrator.

As it is not possible to manufacture exactly identical components by the same industrial process, nominally identical devices have differing responses to the same stimulus. The study of sensitivity is aimed at reducing the differences between the responses of the individual devices of the same batch. Passive elements are relatively easy to manufacture to a close tolerance. For example, in the manufacture of capacitors, the two most important parameters which have to be controlled are the areas of the plates and the thickness of the di-electric and these are not very difficult to control. Active elements, however, are usually influenced by a large number of parameters some of which are not readily controllable in the manufacturing processes. For example, the response of a transistor depends on a large number of parameters of which the doping level in the emitter, base and collector, the areas of the junctions, the thickness of the base are but a few.

Linvill and Gibbons[33] approached the problem of sensitivity by considering changes in the values of the matrix elements. The hybrid parameter h_{21}, which they assumed to be real, and which exhibited the largest spread, was used to estimate the spreads in the three other

h-parameters. Quite apart from the assumption that the hybrid parameters were real, Singhakowinta[34] has shown that this approach is unsatisfactory as it involves lengthy calculations which have little or no relationship to reality. Lathi's[20] work on sensitivity was done from the point of view of variation in the values of the physical equivalent circuit of the transistor and he reached a number of empirical conclusions that gain-sensitivity performance can be improved by reducing the impedance of the input mesh, increasing the impedance of the output mesh or by adding an impedance in series with the common lead. (In the common emitter configuration, this is called emitter degeneration).

In 1964, Singhakowinta and Boothroyd[35] derived an expression which related the power gain of an active two-port to its non-reciprocity (Y_{21}/Y_{12}) and its unilateral power gain (U),

$$\text{where} \quad U = \frac{|Y_{21} - Y_{12}|^2}{4\left[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})\right]} \; .$$

The importance of this contribution lies in the fact that it became possible to reduce the number of parameters to be considered in the design of conjugately matched amplifiers to three, namely, the real and imaginary parts of the reciprocal of the measure of non-reciprocity (λ_R and λ_I) and the reciprocal of the unilateral power gain (1/U). Due to the simplicity of the approach, Singhakowinta[34] was able to make a three-dimensional model which displayed the three parameters mentioned above on the axes and a series of surfaces each of which

represented a constant value of conjugate matched power gain.

Singhakowinta[34] represented the spread in the parameters of a batch of transistors by a group of points in the three-dimensional space, and by enclosing them firstly in a cylinder and then in a sphere, he was able to indicate on a normalized chart, areas in which improved sensitivity performance could be obtained.

In order to achieve the improved sensitivity performance, it is necessary to move the points of operation of the batch of transistors from one area to another and this is done by embedding. On a normalised chart, lossless as well as lossy embedding moves the points in a straight line. In terms of the space model, lossless embedding moves the points of operation in such a way that the values of 1/U remains unchanged. Port-padding on the other hand leaves λ_R and λ_I unchanged while altering the value of 1/U.

As Singhakowinta's work immediately preceeded the present work, it is often referred to in this thesis.

1.4 FORMULATION OF THE PROBLEM

There are several defects in the work of Singhakowinta[34] which need to be rectified. His assumption that the spread in the 'inverse gain space' can be enclosed in some arbitrary geometrical volume and the use he made of normalized charts tended to confuse rather than elucidate the advantages of this new approach to sensitivity, and there

is a need to replace it by simpler concepts and techniques.

Secondly, it has been known that when negative feedback is applied to a batch of devices, such as transistors, which exhibit spread in gain, then the result is to reduce the spread in gain. It is also common knowledge that the reduction of the spread in gain is paid for by the loss of average gain. What is not known is the precise relationship which exists between the improvement in sensitivity performance and the loss of average gain. A knowledge of this relationship should give an indication of the methods to be used in the synthesis of embedding networks which will optimise the gain-sensitivity performance of the devices.

Thirdly, several stability factors have been mentioned above which purport to measure how far or how near a device is to instability,[27] i.e. the generation of oscillations. The implication here is that say, a transistor which has an S_i value equal to 4 is twice as stable as one with an S_i equal to 2, or indeed that the former is more stable than the latter. Stability factors as measures of stability need to be carefully examined.

Mason's U has over the years come to be associated, and in some cases become synonymous, with activity. There is need to show how far Mason's condition for activity, namely, that U must be greater than unity, is valid especially with reference to the manner in which U is connected to the theory of conjugately matched amplifiers.

1.5 PRESENT WORK

In the present work, gain-sensitivity performance of linear active devices is made the main theme. The emphasis is on being able to predict, from a knowledge of the positions of the points of operation of a batch of transistors in the inverse gain space whether a specified gain-sensitivity performance can be achieved and what kind of embedding can be used to achieve it.

The problems outlined in Section 1.4 are discussed and solutions are suggested.

A new concept of the 'average transistor' is used in the design of embedding networks and in the choice of source and load impedances. Given a batch of transistors, there can be no guarantee that one of the batch will exhibit average properties all round: one might be found which will have average gain but with non-average input or output impedance, for example. This problem is solved by the application of statistical techniques.

Digital computers are used as aids to the design of embedding networks, to perform various types of calculations and also in the analysis of statistical data collected from the transistors used in this work. Apart from speed and accuracy, computer techniques offer the advantage of using the programs developed during the course of this work for a wide range of applications. Some of these programs will be discussed in detail later.

As general design guides, experimental results are presented

which relate the effects of the spread in the passive embedding elements to changes in gain-sensitivity performance. The changes in response due to changes in emitter current and collector voltages are also given.

This work does not deal with gain-sensitivity due to changes in temperature, mechanical vibration and stresses, radiation or ageing.

1.6 ORIGINALITY

Except where references have been made to the work of others, the work presented in this thesis was carried out independently by the author and, to his best knowledge, the conclusions recorded in the last chapter are original.

Chapter 2

GAIN - SENSITIVITY RELATIONSHIP

2.1 INTRODUCTION

When a batch of transistors of the same type are used to build nominally identical amplifiers, it is highly improbable that the amplifiers will give identical gain. This is because each element used in the construction departs slightly from its nominal value. In general, the departure in passive elements such as capacitors, inductors and resistors are slight and the factors which affect their values are relatively simple to analyse and control. For example, the capacitance of a capacitor is basically controlled by the thickness and permittivity of its dielectric and the area of its plates. Therefore, spreads in passive elements used in an amplifier circuit are unlikely to affect the performance of an amplifier adversely. This suggests that the differences in the gains of the amplifiers are due largely to the differences in the transistors.

In order to study the effect of the changes in transistors on the gain of the amplifiers, it is necessary to eliminate the changes in gain due to changes in the passive elements in the circuit. To do this it is necessary to design an amplifier such that the transistors can be changed easily. Since it is assumed that all the transistors in the batch will be conjugately matched, it is necessary to make the

resistive as well as the reactive parts of the terminations tunable. For a batch of 20 p-n-p planar silicon transistors the results of measurements are shown in Fig. 2.1a.

When negative feedback is applied equally to all the transistors in the batch, it is well known that the differences in gain will tend to diminish and also that the average gain of the whole batch will decrease. Fig. 2.1b shows a typical effect of connecting a single resistor between emitter and collector (Y-feedback) of the common-base amplifier.

2.2 DESIGN REQUIREMENTS

When a designer is presented with a batch of transistors and asked to build a set of amplifiers which satisfy the gain condition given in the form $G \pm \Delta G$ db, he should be able to determine on the basis of the scatter of the small signal parameters:

a) whether it is possible to satisfy the conditions

b) what type or types of embedding are necessary to achieve the requirements.

In making his choice of embedding he must take into consideration the following important points,

i) The design procedure should be as simple and accurate as possible.

ii) the resulting gain-sensitivity performance should be as close to the optimum as possible (i.e. maximum possible average gain with

minimum possible gain spread).

iii) the number of embedding elements should be the minimum possible thus reducing the cost of manufacture and increasing reliability.

The answer to question (a) must be obtained before starting the design. In order to clarify the position further, the problem will be put in numerical terms. Supposing that we have a batch of transistors which give a natural average gain of 25 db with a spread of $\pm$ 3 db and that for our purposes $\pm$ 3 db spread is more than we can tolerate and further that an average gain of 23 db and a spread of $\pm$ 1 db will satisfy our requirement. The question is, if we use negative feedback to reduce the spread from $\pm$ 3 db to $\pm$ 1 db will the average gain then be greater or less than the required 23 db? If the answer is: greater than 23 db, then we can proceed with the design. If the answer is less than 23 db, we either have to relax the requirements or, failing that, to reject those of the transistors which give extreme values of gain.

2.3 CONJUGATE MATCHED GAIN OF TWO-PORT

For a two-port which is inherently stable or made so by embedding, Singhakowinta and Boothroyd[35] have shown that the following equation holds:

$$\sqrt{\frac{U}{G}} = \frac{|\underline{A} - 1|}{|\underline{A} - G|} \quad . \qquad (2.1)$$

This equation expresses the conjugate matched gain G in precisely three terms, namely, the complex measure of non-reciprocity $\underline{A}$ (i.e. Y_{21}/Y_{12}) and the unilateral power gain U.

2.3.1 $\underline{\lambda}$ - 1/U Space (Inverse Gain Space)

Because equation (2.1) involves four parameters, Singhakowinta[34] was able to construct a three dimensional space model to represent it. He chose to use the inverse of the complex measure of non-reciprocity (i.e. $Y_{12}/Y_{21} = \underline{\lambda}$) and the inverse of the unilateral power gain 1/U as the axes. Thus he obtained a family of surfaces each representing a particular value of gain.

Equation (2.1) can be written in the form,

$$\frac{U}{G} = \frac{\left| 1 - \underline{\lambda} \right|^2}{\left| 1 - G\underline{\lambda} \right|^2} \quad . \tag{2.2}$$

It can be shown that if $U \gg 1$ and $1 \gg \left| \underline{\lambda} \right|$, then,

$$\lambda_I^2 + (\lambda_R - 1/G)^2 - 1/GU = 0. \tag{2.3}$$

The assumptions that $U \gg 1$ and $1 \gg \left| \underline{\lambda} \right|$ are valid as typical values are about 100 and 0.003 respectively.

From equation (2.3) it can be shown that a plane of constant 1/U cuts the constant gain surfaces in circles, as shown in Fig. 2.2a, and that a plane of constant λ_R cuts the constant gain surfaces in hyperbolae as shown in Fig. 2.2b.

Since we are interested in the conjugate matched gain, it should

be possible to incorporate one of the stability conditions and then confine our attention to the inherently stable region of the four-dimensional model.

It can be shown that when $S_i = 1$ (which is the same condition as $k_i = 1$),

$$\lambda_I^2 - (1/2U)^2 - \lambda_R/U = 0 \qquad (2.4)$$

Equation (2.4) represents a surface which separates the inverse gain space (IGS) into regions of inherent stability and potential instability. This surface cuts a plane of constant 1/U in a parabola and a plane of constant λ_R in a hyperbola represented by:

$$\lambda_I^2 - (1/2U)^2 - k/U = 0. \qquad (2.5)$$

where k is a constant. When k = 0, the hyperbola degenerates into two straight lines given by:

$$\lambda_I = \pm (1/2U). \qquad (2.6)$$

The boundary is shown in Figs. 2.2a and 2.2b. Fig. 2.3 is a model illustrating the stability surface broken to show three constant gain surfaces.

From now on, we shall confine our attention to the stable region of the inverse gain space and unless otherwise stated, conjugate matched gain will be referred to simply as gain.

2.3.2 Embedding in the Inverse Gain Space (IGS)

One of the advantages of working in the IGS is that when the transistor is embedded (i.e. feedback is applied to it), the resulting change can be represented approximately by a movement of the point of operation in a straight line to a new position. The direction and distance moved depends on the type of embedding used, the nature of the embedding element and the value of the element. These will be explained in detail.

Considering only lossless embedding for the moment, there are two types of simple embedding, namely 'Y' mode embedding or feedback and 'Z' mode embedding. These two types of embedding are shown in Fig. 2.4 and their corresponding matrices are given. The third possibility of connecting a reactive element across the input or output port has not been considered as it is assumed that the reactive part of the port immitances will be tuned out (i.e. conjugately matched).

Since the quantity U is invariant to lossless reciprocal embedding, the effect of such embedding can be considered as a movement in a plane of constant 1/U. Fig. 2.5 shows such a section. If the point of operation of the transistor is originally at a point such as M, then Y-mode embedding might move the point of operation along a line NML. The direction of motion depends on whether the element used is a capacitance or an inductor; an inductance moves it in the direction of N and a capacitance moves it in the direction of L. The distance moved in the directions shown depends on the value of the inductance or capacitance used. The distance moved is

linearly related to the value of susceptance or reactance of the element, (i.e. if 50 pF moves it a distance of 2 cms then 100 pF will move it 4 cms.). Z-mode embedding moves the point of operation along a line PMK. A capacitance will move it in the direction of P and an inductance will move it the direction of K.

A combination of Y- and Z-modes of embedding can, in general, be used to move the point of operation to any point on the plane of constant 1/U, such as Q.

The use of lossy elements (i.e. resistive elements) in embedding circuits have the common effect of changing the value of 1/U. In addition to the two types of embedding already considered, a third, namely, port-padding can be used. These are illustrated in Fig. 2.6 with the appropriate matrices. Y-mode resistive embedding might move a point of operation such as M in the direction of P. It should be noted that this movement is not in the plane of constant λ_R as shown in Fig. 2.7, in which the locus of motion is projected onto the constant λ_R plane for simplicity. As before, the distance moved is linearly related to the value of the resistance used. Z-mode embedding might move the point of operation from M in the direction of N. Again this movement is not in the plane of constant λ_R. It should be noted that the value of 1/U is decreasing as the point of operation moves from M to N. This type of movement is subject to a number of conditions which will be discussed in detail in Chapter 3. Port padding has the interesting property of altering the value of 1/U while leaving λ_R and λ_I unchanged. Thus the motion is in the plane of the paper

and parallel to the 1/U axis. There are two types of port padding namely, Y-mode padding in which the resistive element(s) is connected across the input and/or output port(s) and Z-mode padding in which the resistive element(s) is connected in series with the lead(s).

2.4 SPREAD IN THE INVERSE GAIN SPACE

Supposing we measured the gains of a batch of transistors and found that they were all of the same value, we can draw one of two conclusions, namely that all the transistors operated at the same point in the IGS or that they operated at different points in the IGS but on the same gain surface. The first case is most improbable and can be dismissed. The second while being highly unlikely illustrates one point and that is, when the points of operation of the transistors have been plotted in the IGS, it is possible to 'see' an apparent spread in the points when in fact no spread in gain exists. In terms of equation (2.3) the three parameters, λ_R, λ_I and 1/U can be altered while 1/G is kept constant.

In general, if we measure a batch of transistors and compute the values of λ_R, λ_I and 1/U and proceed to plot them in the IGS, we shall find that there will be considerable spread in the values of the co-ordinates of the points. Fig. 2.8 show typical spreads projected on to planes of constant 1/U and λ_R respectively. Now, if we compute the average gain of the batch of transistors and locate the constant gain surface which corresponds to it, we should find that the surface goes

through the points separating those of higher-than-average gain from those of lower-than-average gain. Those with average gain will naturally sit on the surface. The higher-than-average transistors will be on the convex side of the constant gain surface and those with lower-than-average gain will be on the concave side.

2.4.1 Definition of spread in the Inverse Gain Space

The transistor with the minimum gain in a batch operates at a point such as j, as shown in Fig. 2.9, and has a value of gain equal to G_j. If lines are drawn parallel to the axes from j to the surface representing the value of the average gain and these meet it in the points i, k, and l then, because i, k, and l are on a constant gain surface, $G_i = G_k = G_l$. It is clear that if we had transistors operating at i, k and l, although there will be considerable spread in λ_R, λ_I and 1/U, there will be no spread in gain between them. The reason G_j is different from G_i, G_k, G_l is that it 'sits' on a constant gain surface which has a different value. Thus as we move from say l to j, we would go through constant gain surfaces representing gains of values lying between G_l and G_j. We can now define spreads in the inverse gain space as:

$$\Delta\lambda_R = \lambda_{R_j} - \lambda_{R_k} \tag{2.7}$$

$$\Delta\lambda_I = \lambda_{I_l} - \lambda_{I_j} \tag{2.8}$$

$$\Delta(1/U) = (1/U)_j - (1/U)_i \tag{2.9}$$

where the suffices of λ_R, λ_I and $1/U$ refer to the values of these parameters at the points. From (2.3)

$$\lambda_{I_i}^2 + (\lambda_{R_i} - 1/G_i)^2 - 1/G_i U_i = 0 \qquad (2.10)$$

$$\therefore \quad 1/U_i = \frac{\lambda_{I_i}^2 + (\lambda_{R_i} - 1/G_i)^2}{1/G_i} \qquad (2.11)$$

Now, from (2.9)

$$\Delta(1/U) = 1/U_j - \frac{\lambda_{I_i}^2 + (\lambda_{R_i} - 1/G_i)^2}{1/G_i}$$

$$= \frac{1/G_i U_j - \lambda_{I_i}^2 - (\lambda_{R_i} - 1/G_i)^2}{1/G_i} \qquad (2.12)$$

But $\lambda_{R_i} = \lambda_{R_j} = \lambda_R$ and $\lambda_{I_i} = \lambda_{I_j} = \lambda_I$.

Therefore, in general,

$$\Delta\lambda_R = \frac{1/G_i U_j - \lambda_I^2 - (\lambda_R - 1/G_i)^2}{2(1/G_i - \lambda_R)} \qquad (2.13)$$

Similarly,

$$\Delta\lambda_I = \frac{1/G_i U_j - \lambda_I^2 - (\lambda_R - 1/G_i)^2}{2\lambda_I} \qquad (2.14)$$

and

$$\Delta(1/U) = \frac{1/G_i U_j - \lambda_I^2 - (\lambda_R - 1/G_i)^2}{1/G_i} \qquad (2.15)$$

The above parameters will be referred to as the spreads in the co-ordinates of the point of operation of the transistor. Fig. 2.9 shows a physical representation of the spreads in a three-dimensional model.

2.4.2 Sensitivity factors in the Inverse Gain Space

The definition used by Hakimi and Cruz[38] in a study of the effect on the response of a multi-parameter system of a variation Δp in the parameter p was $\frac{\Delta R/R}{\Delta p}$, ΔR being the change in response resulting from Δp.

Using this definition and starting from (2.3), it can be shown that,

$$\lambda_I^2 = \lambda_R/U + (1/2U)^2 - (1/\mu_R)^2 \qquad (2.16)$$

$$(\lambda_R + 1/2U)^2 = \frac{(\lambda_R^2 + \lambda_I^2 + \lambda_I/\mu_I)^2}{(\lambda_R^2 + \lambda_I^2 + 2\lambda_I/\mu_I)} \qquad (2.17)$$

$$\lambda_I^2 = \lambda_R/U + (1/2U)^2 - (1/2\,\mu_{(1/U)})^2 \qquad (2.18)$$

where $$\mu_I = \frac{\partial G/G}{\partial \lambda_I} , \qquad (2.19)$$

$$\mu_R = \frac{\partial G/G}{\partial \lambda_R} \quad \text{and} \qquad (2.20)$$

$$\mu_{(1/U)} = \frac{\partial G/G}{\partial (1/U)} \qquad (2.21)$$

are the sensitivities to gain (or sensitivity factors) in directions parallel to λ_I, λ_R and 1/U respectively.

It can be seen from (2.16) that for constant values of μ_R, a family of surfaces can be drawn in the IGS. This is also true of μ_I and $\mu_{(1/U)}$ in (2.17) and (2.18). By inspecting (2.16) and (2.18), it can be seen that gain is twice as sensitive to changes in λ_R as in 1/U. Further, when μ_R, μ_I and $\mu_{(1/U)}$ are equal to infinity, (2.16), (2.17) and (2.18) reduce to,

$$\lambda_I^2 = \lambda_R/U + (1/2U)^2 \qquad (2.22)$$

which is the same as (2.4) and therefore the condition that $S_i = k_i = 1$ is identical to equating the sensitivity factors to infinity. The relationship between sensitivity and stability will be discussed in detail later.

The above suggests that a three-dimensional approach in which spread in gain due separately to λ_R, λ_I and 1/U is considered offers distinct advantages over Singhakowinta's method[34] of treating the spread in $\underline{\lambda}$ as a circular spread and then dealing with the spread in 1/U separately.

2.4.3 Changes in Gain

In section 2.4.1 we obtained expressions for the spreads in directions parallel to the coordinate axes. In section 2.4.2, sensitivity factors in directions parallel to the axes were derived. We can now combine the two in order to obtain expressions for the changes of gain which occur as a result of movement in the inverse gain space parallel to each axis in turn.

Sensitivity factor was defined as $\frac{\Delta G/G}{\Delta p}$. To a first order of approximation,

$$\Delta G/G = \frac{\Delta G/G}{\Delta p} \cdot \Delta p \qquad (2.23)$$

Therefore,

$$\Delta\lambda_R\mu_R\Big|_k = \frac{\Delta G}{G}\Big|_{\text{due to } \lambda_R} = S_R$$

$$S_R = \frac{1/G_iU_j - \lambda_{I_j}^2 - (\lambda_{R_j} - 1/G_i)^2 \cdot 1/G_i}{(1/G_i - \lambda_{R_j})(2\lambda_{R_k}^2 + 2\lambda_{I_j}^2 - 1/G_iU_j - 2\lambda_{R_k}/G_i)} \qquad (2.24)$$

and

$$\Delta\lambda_I\mu_I\Big|_l = \frac{\Delta G}{G}\Big|_{\text{due to } \lambda_I} = S_I$$

$$S_I = -\frac{\lambda_{I_l}\ 1/G_iU_j - \lambda_{I_j}^2 - (\lambda_{R_j} - 1/G_i)^2}{2\lambda_{I_j}\ (\lambda_{R_j}^2 + \lambda_{I_l}^2) - \lambda_{R_j}/G_i - 1/2\ G_iU_j} \qquad (2.25)$$

and

$$\Delta(1/U)\mu_{(1/U)}\Big|_i = \frac{\Delta G}{G}\Big|_{\text{due to } (1/U)} = S_{(1/U)}$$

$$S_{(1/U)} = \frac{1/G_iU_j - \lambda_{I_j}^2 - (\lambda_{R_j} - 1/G_i)^2}{2\ \lambda_{R_j}^2 + \lambda_{I_j}^2 - \lambda_{R_j}/G_i - 1/2G_iU_j} \qquad (2.26)$$

From Fig. 2.9 it can be seen that movement from i to j should result in

the same change in gain as movement from 1 to j or k to j. This means that the change in gain resulting from movement from the average gain surface to j is independent of the path taken. Thus

$$\Delta G = \int_j^k \mu_R d(\lambda_R) = \int_j^l \mu_I d(\lambda_I) = \int_j^i \mu_{(1/U)} d(1/U) \tag{2.27}$$

If we calculate the partial differential $\partial S_p/\partial p$ where p is consecutively λ_R, λ_I and $1/U$, and equate the result to zero, it should be possible to locate any turning points which might exist in the directions parallel to the axes of the IGS.

$$\frac{\partial S_R}{\partial \lambda_R} = 0 \quad \text{gives a turning point when } \lambda_R = \infty \ , \tag{2.28}$$

$$\frac{\partial S_I}{\partial \lambda_I} = 0 \quad \text{gives a turning point when } \lambda_I = 0 \quad \text{and} \tag{2.29}$$

$$\frac{\partial S_{(1/U)}}{\partial (1/U)} = 0 \quad \text{gives a turning point when } 1/U = 0. \tag{2.30}$$

The result of (2.28) is not interesting since a turning point at infinity cannot have much practical value. Equation (2.29) however shows that a turning point exists on the plane of symmetry of the inverse gain space. A second partial differential shows that S_I has a minimum turning point at $\lambda_I = 0$. This means that the change in gain resulting from small movement in a direction parallel to the λ_I axis is a minimum when λ_I is equal to zero. Equation (2.30) like (2.28) does not give any interesting result since U has to have an

infinite value in order to obtain the turning point.

The same conclusions can be drawn from Figs. 2.2a and 2.2b. From Fig. 2.2a, it can be seen that the constant gain lines cross the λ_R axis at right angles since they are circles and their centres are on the λ_R axis. Therefore a small movement from the λ_I axis at right angles to it will produce virtually no change in gain. This is not the case if λ_I is not equal to zero in the first place. Since the axis is a line of symmetry, a turning point must exist on it and this turning point must be a minimum. Therefore one of the conditions for optimum gain-sensitivity performance is that $\lambda_I = 0$. This result was arrived at by Singhakowinta using a different method. From Fig. 2.10 it can be seen that the lines of constant gain have no turning points on them in the directions parallel to the axes. However, movement in directions parallel to the λ_R and 1/U axes which result in improved gain-sensitivity will be discussed when embedding networks are considered.

2.5 CHANGE IN AVERAGE GAIN - CHANGE IN GAIN SPREAD

The dependence of change in gain spread on change in average gain was mentioned briefly in section 2.2. We shall now discuss this dependence in some detail.

In Section 2.4.3, it was concluded that the change in gain resulting from movement in the inverse gain space from the average gain surface to another point in the space was independent of the path

taken. Bearing in mind Fig. 2.9, we can write, to a first order of approximation,

$$\left.\frac{\partial(1/G)}{\partial\lambda_R}\right|_k \cdot \Delta\lambda_R = \left.\frac{\partial(1/G)}{\partial\lambda_I}\right|_l \cdot \Delta\lambda_I = \left.\frac{\partial(1/G)}{\partial(1/U)}\right|_i \cdot \Delta(1/U) \qquad (2.31)$$

The above equation is similar to (2.23) but instead of taking the partial differentials of gain with respect to λ_R, λ_I and $1/U$, the partial differentials of inverse gain have been taken. This is more convenient as the basic relationship between gain and the parameters of the inverse gain space given by equation (2.3) involves $1/G$ rather than G. The value of the differentials are evaluated at the points k, l and i since these give average values for the whole batch of transistors.

Since $G_i = G_k = G_l$ and $G_i > G_j$ to a first order of approximation,

$$\frac{1}{G_i} = \frac{1}{G_j} - \left.\frac{\partial(1/G)}{\partial\lambda_R}\right|_k \cdot \Delta\lambda_R \qquad (2.32)$$

$$\frac{1}{G_i} = \frac{1}{G_j} - \left.\frac{\partial(1/G)}{\partial\lambda_I}\right|_l \cdot \Delta\lambda_I \qquad (2.33)$$

$$\frac{1}{G_i} = \frac{1}{G_j} - \left.\frac{\partial(1/G)}{\partial(1/U)}\right|_i \cdot \Delta(1/U) \qquad (2.34)$$

Rearranging (2.34),

$$\left.\frac{\partial(1/G)}{\partial(1/U)}\right|_i \cdot \Delta(1/U) = \frac{1}{G_j} - \frac{1}{G_i}$$ which we define as $\Delta(1/G)$. (i.e. change in inverse gain between points i and j).

From (2.3) we obtain the partial differential

$$\frac{\partial(1/G)}{\partial(1/U)} = \frac{1/G}{2/G - 2\lambda_R - 1/U} \tag{2.35}$$

Therefore,

$$\left.\frac{\partial(1/G)}{\partial(1/U)}\right|_i = \frac{1/G_i}{2/G_i - 2\lambda_R - 1/U_i} \tag{2.36}$$

Substituting in (2.34) and recalling (2.15), we get

$$\Delta(1/G) = \frac{1/G_i U_j - \lambda_I^2 - (\lambda_R - 1/G_i)^2}{2/G_i - 2\lambda_R - 1/U_i} \tag{2.37}$$

From Fig. 2.9,

$$\begin{aligned} 1/U_j &= 1/U_i + \Delta(1/U) \\ &= \frac{\lambda_I^2 + (\lambda_R - 1/G_i)^2 + \Delta(1/U)/G_i}{1/G_i} \end{aligned} \tag{2.38}$$

Substituting in (2.37) and leaving out the suffices where they refer to the point j, and at the same time recalling (2.11), we get

$$\Delta(1/G) = \frac{\Delta(1/U)/G_i^2}{1/G_i^2 - (\lambda_R^2 + \lambda_I^2)} \tag{2.39}$$

We have now obtained an expression for the inverse gain spread, $\Delta(1/G)$, in terms of λ_R, λ_I, the average natural gain, G_i, and the spread in $1/U$, $\Delta(1/U)$.

Starting with (2.32), an expression can be derived connecting the spread in inverse gain, $\Delta(1/G)$, with the spread in λ_R, $\Delta\lambda_R$, and the natural average gain G_k. This relationship can be shown to be:

$$\Delta(1/G) = \frac{2\Delta\lambda_R/G_k}{1/G_k + \lambda_R - \Delta\lambda_R} \qquad (2.40)$$

Equation (2.33) can be used to relate $\Delta(1/G)$ to λ_I, but then there appears to be little point in doing this since one of the conditions for optimum gain-sensitivity operation is that λ_I should be equal to zero and further it has been pointed out in Section 2.4.3 that the sensitivity of gain to changes in λ_I in the vicinity of the $\lambda_I = 0$ plane is very low.

So far we have not considered any particular type of embedding network which will make equations (2.39) and (2.40) realisable. We shall now consider possible embedding networks that can be used in the amplifier circuit.

2.5.1 Lossless Embedding

Lossless embedding has the property of leaving the value of U unchanged. From Fig. 2.11, therefore, if we have one transistor operating at i_1 and another at j_1 and we use lossless embedding to change their value of λ_I to zero, since their values of 1/U remain constant, the spread $\Delta(1/U)$ remains constant and the transistors which operated at i_1 and j_1 will now operate at i_2 and j_2 respectively.

Assuming we wish to operate the transistors at $\lambda_I = 0$ (which is a condition for optimum gain-sensitivity operation) then we can now move the point i_1 along a line parallel to the λ_R axis on the $\lambda_I = 0$ plane until it intersects the line of constant gain which has the same

value as the desired average gain. If then the value of λ_R is X, the required average gain is G_{av} and the specified minimum gain is G_{lo}, (2.39) then becomes:

$$\Delta(1/G) = \frac{\Delta(1/U)/G_{av}^2}{1/G_{av}^2 - X^2} \qquad (2.41)$$

Now from (2.3) when $\lambda_I = 0$,

$$X^2 = \frac{1}{G_{av}^2} - \frac{2}{G_{av}\sqrt{G_{av}U_i}} + \frac{1}{G_{av}U_i} \qquad (2.42)$$

Substituting in (2.41) we get

$$\Delta(1/G) = \frac{\Delta(1/U)/G_{av}}{2/\sqrt{G_{av}U_i} - 1/U_i} \qquad (2.43)$$

If $1/G_{lo} - 1/G_{av} \geqslant \Delta(1/G)$, the design specifications can be satisfied using lossless embedding. Therefore,

$$\frac{1}{G_{lo}} - \frac{1}{G_{av}} \geqslant \frac{\Delta(1/U)/G_{av}}{2/\sqrt{G_{av}U_i} - 1/U_i}$$

and

$$\frac{1}{G_{lo}} \geqslant \frac{1}{G_{av}}\left[\frac{\Delta(1/U)}{2/\sqrt{G_{av}U_i} - 1/U_i} + 1\right] \qquad (2.44)$$

We have therefore obtained a condition which relates the required average and minimum gain to the original spread in 1/U and the 1/U of the 'average transistor'. Since these quantities are known before the design is commenced, it is possible to apply the condition given in (2.44) to test whether the specifications can be met.

If instead of using the transistor with the lowest gain, we use that with the highest gain, G_{up}, it can be shown that

$$\frac{1}{G_{av}}\left[\frac{\Delta(1/U)}{2/\sqrt{G_{av}U_i} - 1/U_i} + 1\right] \geqslant \frac{1}{G_{up}} . \qquad (2.45)$$

A few tests based on practical considerations are necessary to confirm the condition given in (2.44). As $G_{av} > G_{lo}$, the part inside the square brackets has to be greater than unity. That is,

$$\frac{\Delta(1/U)}{2/\sqrt{G_{av}U_i} - 1/U_i} > 0 \qquad (2.46)$$

$\Delta(1/U)$ is positive by definition and therefore the only way in which (2.46) can possibly not be satisfied is when the denominator becomes negative i.e. when

$$\frac{1}{U_i} > \frac{2}{\sqrt{G_{av}U_i}} \qquad \text{which gives}$$

$$G_{av} > 4U_i . \qquad (2.47)$$

It can be shown that in the stable region of the IGS, gain cannot be greater than 4U. Since we are here dealing with conjugate matched gain, (2.46) always holds.

There are two ways in which G_{lo} can approach G_{av}. The first is when $\Delta(1/U)$ approaches zero and the second is when both G_{lo} and G_{av} approach zero (i.e. when the average gain is zero and therefore the spread is also zero). Both these conditions are satisfied by

(2.44). The above tests are equally applicable to (2.45).

2.5.2 Lossy Embedding (Port Padding)

The effect of port padding, is easy to analyse since it only changes the value of 1/U and leaves both λ_R, and λ_I unchanged. From Fig. 2.11, therefore, transistors operating at i_1, j_1, l_1, and k_1 will operate at i_3, j_3, l_3 and k_3 respectively. From (2.40), we obtain the expression

$$\frac{1}{G_{lo}} \geqslant \frac{1}{G_{av}} \left[\frac{2\Delta\lambda_R}{1/G_{av} + \lambda_R - \Delta\lambda_R} + 1 \right] \quad (2.48)$$

using similar steps to those shown in equations (2.41) to (2.44). The counterpart of (2.48) is

$$\frac{1}{G_{av}} \left[\frac{2\Delta\lambda_R}{1/G_{av} + \lambda_R - \Delta\lambda_R} + 1 \right] \geqslant \frac{1}{G_{up}} . \quad (2.49)$$

As before, $G_{av} > G_{lo}$ therefore the part inside the square brackets in (2.48) has to be greater than unity. That is,

$$\frac{2\Delta\lambda_R}{1/G_{av} + \lambda_R - \Delta\lambda_R} > 0$$

The quantity $\Delta\lambda_R$, by definition, is positive and therefore the denominator must be positive i.e. $1/G_{av} + \lambda_R \geqslant \Delta\lambda_R$. It can be shown from (2.3) that λ_R lies between $3/G_{av}$ and $-1/G_{av}$, assuming that $\lambda_I = 0$. In the case when $\lambda_R = -1/G_{av}$, the point of operation of the transistor is on the stability surface of the inverse gain space and (2.48) breaks down. It must be noted however, that resistive port-

padding cannot, in general, be used to cause the transistor to become unstable.

As $\Delta\lambda_R$ approaches zero, G_{lo} approaches G_{av} (the point k, in Fig. 2.9, coincides with j). Alternatively, as both G_{av} and G_{lo} approach zero, the spread in gain will approach zero. The above conditions are satisfied by both (2.48) and (2.49).

2.5.3 Y-mode Lossy Embedding

As was mentioned in section (2.3.2), Y-mode lossy embedding changes the value of 1/U as well as that of $\underline{\lambda}$. This makes it rather difficult to analyse the performance of an amplifier in which this type of embedding has been employed. A further disadvantage arises because the condition for optimum gain-sensitivity operation, namely $\lambda_I = 0$, cannot, in general, be satisfied by using Y-mode lossy embedding alone. This means that some other type of embedding has to be employed in addition to this. Such a circuit would not only be expensive but unreliable as well. There are also a number of practical objections to the use of Y-mode lossy embedding which will be discussed in Chapter 4. For the rest of this work, lossy embedding will be restricted to resistive port-padding.

2.5.4 Resistive-Capacitive Embedding

The use of capacitance and resistance only in the embedding circuit will not be considered in detail here, as it is a special case

which will limit the original point of operation of the two-port to areas above the λ_R axis. (i.e. positive values of λ_I). It can be seen from Fig. 2.5 that the $\lambda_I = 0$ can be satisfied only if the transistor has a positive value of λ_I.

2.6 LOSSLESS VERSUS LOSSY EMBEDDING

2.6.1 'Ideal' Spreads

In order to study the advantages and disadvantages of lossless and lossy embedding vis-a-vis gain sensitivity performance, we can consider three transistors located at the points A, B, and C as shown in Fig. 2.10, such that the gains of transistors B and C are equal, the values of λ_R for transistors A and C are equal and the values of 1/U for transistors A and B are equal. Thus the difference in gain between transistors A and B is due exclusively to the spread $\triangle\lambda_R$ and that between A and C to the spread $\triangle(1/U)$. This is a case of 'ideal' spread and it will be referred to as such.

Assuming that the spreads remain constant when the devices are embedded to move through small distances about their present location, then the point A moves to A', B will move to B' and C to C' such that AA' = BB' = CC'. If instead, A is moved to A'' such that the gain at A' is equal to the gain at A'', B will then move to B'' and C to C'' such that AA'' = BB'' = CC''. Since movement of the point A to A' can be accomplished by using lossless embedding and the movement from A to A'' by lossy embedding (port-padding) the problem of comparing the gain-

sensitivity performance of the two types of embedding is reduced to examining the gains at the points B', B", C' and C".

It is assumed that λ_I is equal to zero for all the three transistors before and after embedding.

2.6.2 Conditions Governing Choice of Embedding

Recalling (2.3) with $\lambda_I = 0$, we have

$$(\lambda_R - 1/G)^2 = 1/GU \qquad (2.50)$$

This is the equation of a parabola for which positive finite values of 1/U will be considered. From (2.50), the slope of the constant gain lines is given by

$$\frac{\partial(1/U)}{\partial\lambda_R} = \frac{2(\lambda_R - 1/G)}{1/G} \qquad (2.51)$$

Assuming a straight line approximation for the constant gain line through A'A" we can write:

$$\text{Slope of A'A"} \simeq \frac{2(\lambda_{R_{A'}} - 1/G_{A'})}{1/G_{A'}} \simeq \text{Slope of B'B"}$$

The slope of the constant gain line through B' is given approximately by

$$\frac{2(\lambda_{R_{B'}} - 1/G_{B'})}{1/G_{B'}} .$$

For $\Delta\lambda_R$, if

$$\frac{2(\lambda_{R_{A'}} - 1/G_{A'})}{1/G_{A'}} > \frac{2(\lambda_{R_{B'}} - 1/G_{B'})}{1/G_{B'}} , \qquad (2.52)$$

it follows from Fig. 2.10 that $G_{B'} > G_{B''}$. Therefore movement in a direction parallel to the λ_R axis leads to improved gain-sensitivity operation over movement in a direction parallel to the 1/U axis, that is, lossless embedding will result in a greater reduction in the gain spread than lossy embedding. The inequality (2.52) simplifies to,

$$G_{A'} \lambda_{R_{A'}} > G_{B'} \lambda_{R_{B'}} . \tag{2.53}$$

Similarly, for $\Delta(1/U)$, if $G_{C''} > G_{C'}$

$$G_{A'} \lambda_{R_{A'}} > G_{C'} \lambda_{R_{C'}} \tag{2.54}$$

movement in a direction parallel to the 1/U axis results in a greater reduction of gain spread than movement in a direction parallel to the λ_R axis, that is, port-padding will lead to a superior gain-sensitivity performance.

2.6.3 Distribution of Points of Operation and Choice of Embedding

In the preceeding section, we derived conditions which govern the choice of the type of embedding to be employed for reducing the spread in gain arising from spreads in λ_R and 1/U. In general, a typical batch of transistors will display both types of spread. We therefore have to decide in the light of the distribution of the points of operation which of the two types of embedding is predominant i.e. what type of embedding will reduce the gain spread of the maximum number of transistors by the maximum amount with the highest average gain possible.

In order to determine which of the two types of ideal spread

predominates in causing the spread in gain, we can sum the moduli of the distances of the points of operation from the average gain surface. Thus we obtain two quantities $\sum\Delta(1/U)$ and $\sum\Delta\lambda_R$. From section (2.4.2), it will be recalled that the gain of the device is twice as sensitive to changes in λ_R as in 1/U. Therefore, the spread in gain is caused by spread in 1/U if $\sum\Delta(1/U) > 2\sum\Delta\lambda_R$ and the appropriate type of embedding can then be chosen.

2.6.4 Port-Padding

As already stated, port-padding is the simplest way of reducing the value of U without affecting those of λ_R and λ_I. We have a choice of padding either the input and/or the output ports. We shall now consider the advantages and disadvantages of the three possible combinations of port-padding in both the Y-mode and Z-mode.

Considering the two modes of padding, it is obvious that the use of both input and output pads has no real advantages. Firstly, the introduction of two resistors in to circuit will increase the cost of the amplifier and lower its reliability. Secondly, there is no criterion to help the designer to decide the relative values of the resistors at the input and output in order to obtain the required value of U.

Non-linearity in the transistor amplifier arises mainly because of the non-linear nature of the input characteristics of the transistor. One technique of improving this is to swamp it with an external resistance (such as the source resistance i.e. mismatching). For Z-mode port-

padding therefore, the input seems to be the place to put it.

Amplifiers are quite often used in a cascaded chain and if losses due to mismatch are to be avoided, the transformers have to be designed to couple them together. Since coupling transformers are easier to design and wind when the admittance ratio is close to unity, it is desirable that Y-mode port-padding should be applied in such a way as to increase the lower of the two admittances. For example, for a common emitter transistor amplifier, the input admittance is about ten orders higher than the output admittance. In a cascade chain therefore, Y-mode output port-padding has obvious advantages over Y-mode input port-padding.

2.7 MISMATCHED AMPLIFIER

2.7.1 Mismatch using a Potentially Unstable Two-Port

A potentially unstable two-port will oscillate at some point as the terminations are varied over an infinite range. However, useful gain can be obtained from it by a judicious choice of terminations so as to avoid instability. A popular[36, 20, 26, 28] way of solving the problem has been the use of source and load terminations which give mismatch conditions at the ports. The actual choice of terminations depends largely on how much loss of gain the designer is willing to exchange for "increased stability". Thus the choice depends on the 'experience' of the designer and design to specified limits is too complex to consider.

2.7.2 Mismatch using an Inherently Stable Two-port

Although for an inherently stable device, the argument put forward for using mismatch terminations does not apply, there are equally compelling reasons to investigate the performance of the mismatched inherently stable two-port.

In transistors, non-linearity arises mainly because the input impedance which is generally low, is non-linear. The linearity of the transistor amplifier can be improved considerably if it is fed from a source impedance (presumed linear) which is higher than the input impedance. The effect of this is to 'swamp' the non-linearity.

Given a source and load impedance to be used in conjunction with an inherently stable two-port amplifier, tremendous advantages can be obtained by avoiding the use of matching transformers at the output and/or input provided that this does not lead to a serious loss of gain.

The degree of the mismatch must be chosen with care as the noise performance of the amplifier tends to deteriorate as the source and input or the load and output impedances diverge[41,42].

2.7.3 Transducer Gain with 'Degree of Mismatch' - X

The transducer gain of a two-port is given by

$$G_t = \frac{4\left|p_{21}\right|^2 \mathrm{Re}(p_s)\mathrm{Re}(p_L)}{\left|(p_{11}+p_s)(p_{22}+p_L)-p_{12}p_{21}\right|^2} \qquad (2.55)$$

Assuming that the two-port is inherently stable, values of source and

load immittances can be found which will match the two-port. Supposing we designate the symbols $\hat{\rho}_s$ and $\hat{\rho}_L$ to these parameters. Then,

$$\hat{\rho}_s = R\,\rho_{11} \qquad \text{and} \qquad \hat{\rho}_L = R\,\rho_{22} \tag{2.56}$$

where

$$R = \sqrt{1 - M/\rho_{11}\rho_{22} - N^2/4\,\rho_{11}^2\rho_{22}^2} \tag{2.57}$$

and

$$M + jN = p_{12}p_{21} \tag{2.58}$$

We can define the source and load imittances as

$$\rho_s = \hat{\rho}_s(1 \pm X) \qquad \text{and} \qquad \rho_L = \hat{\rho}_L(1 \mp X). \tag{2.59}$$

Since the reactive parts of the immittances have to be tuned out,

$$\sigma_s \triangleq -\sigma_{11} + N/2\,\rho_{22} \qquad \text{and} \qquad \sigma_L \triangleq -\sigma_{22} + N/2\,\rho_{11} \tag{2.60}$$

Substituting the above in the transducer gain expression (2.55), it can be shown after considerable simplification that the gain for degree of mismatch X is:

$$G_x \triangleq \frac{4|p_{21}|^2\,\rho_{11}\rho_{22}(1 - X^2)}{4\,\rho_{11}^2\rho_{22}^2\left[R(1 - X^2) + 1\right]^2 + N^2} \tag{2.61}$$

One advantage offered by (2.61) is the absence of $\pm$ X which means that we are free to choose to make ρ_s greater or less than $\hat{\rho}_s$. Secondly, we have lost one degree of freedom in the choice of terminations since ρ_s and ρ_L are related to each other by the degree of mismatch X.

When X = 0, the gain is equal to the conjugate-matched gain which

is;

$$G_c = \frac{4\left|p_{21}\right|^2 \rho_{11}\rho_{22}}{4\,\rho_{11}^2\rho_{22}^2\,(R+1)^2 + N^2} \qquad (2.62)$$

Fig. 2.12 is a plot of gain against mismatch factor X and it can be seen that the gain is symmetrical about X = 0 and it is fairly flat over a wide range of values of mismatch factor reaching 3 db when $X = \pm 0.825$.

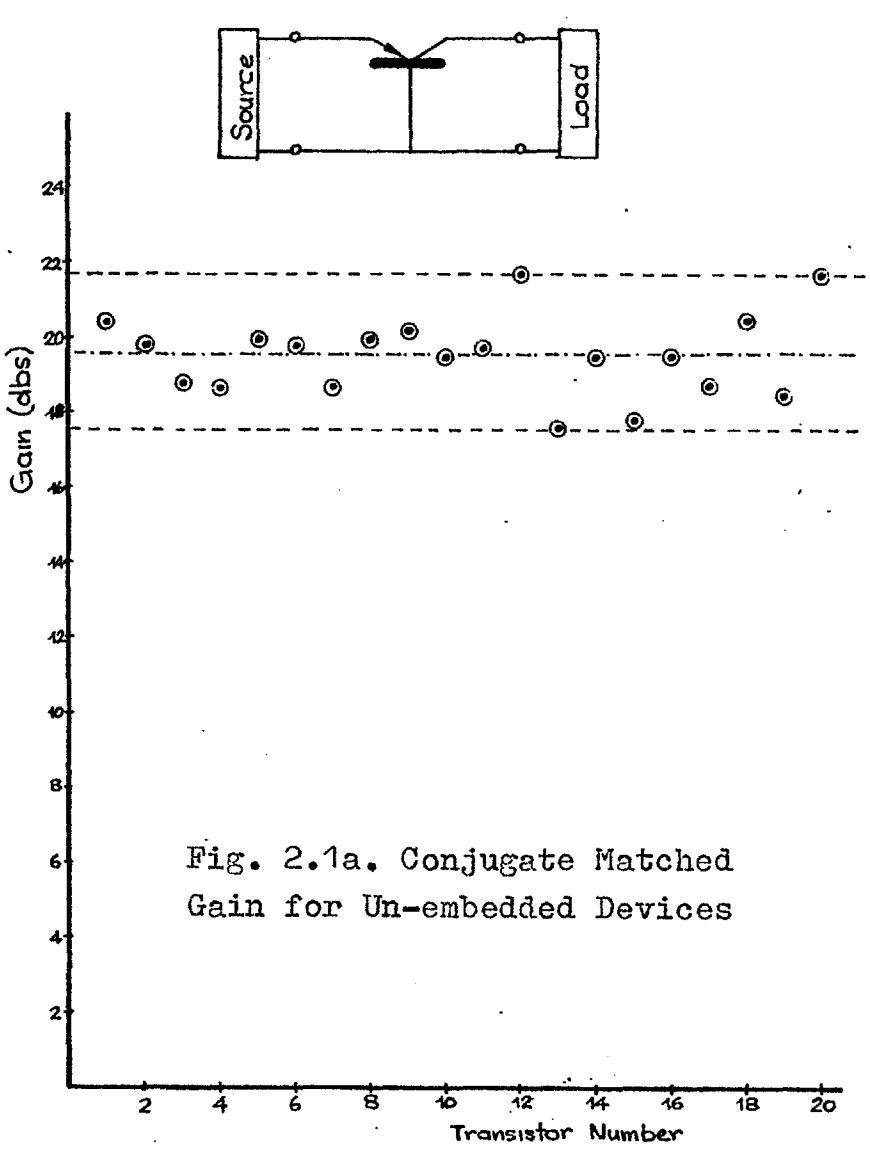


Fig. 2.1a. Conjugate Matched Gain for Un-embedded Devices

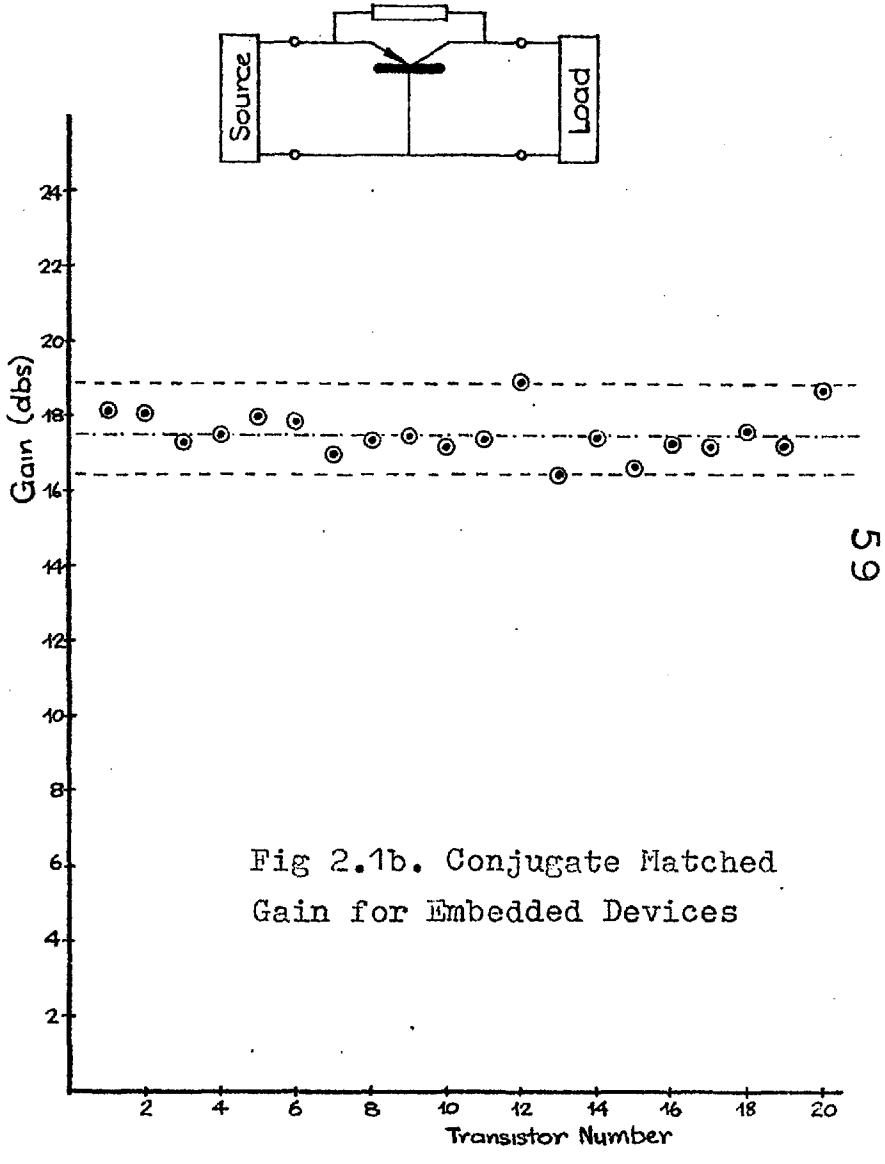


Fig 2.1b. Conjugate Matched Gain for Embedded Devices

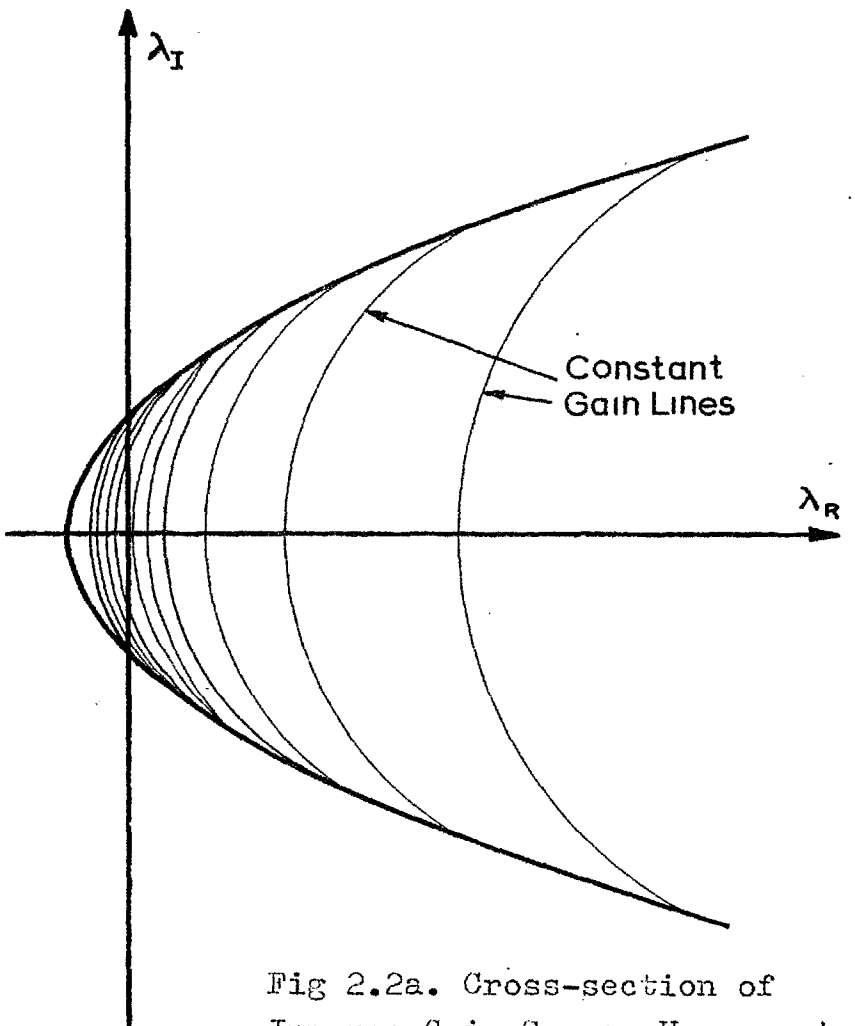


Fig 2.2a. Cross-section of Inverse Gain Space. U = const.

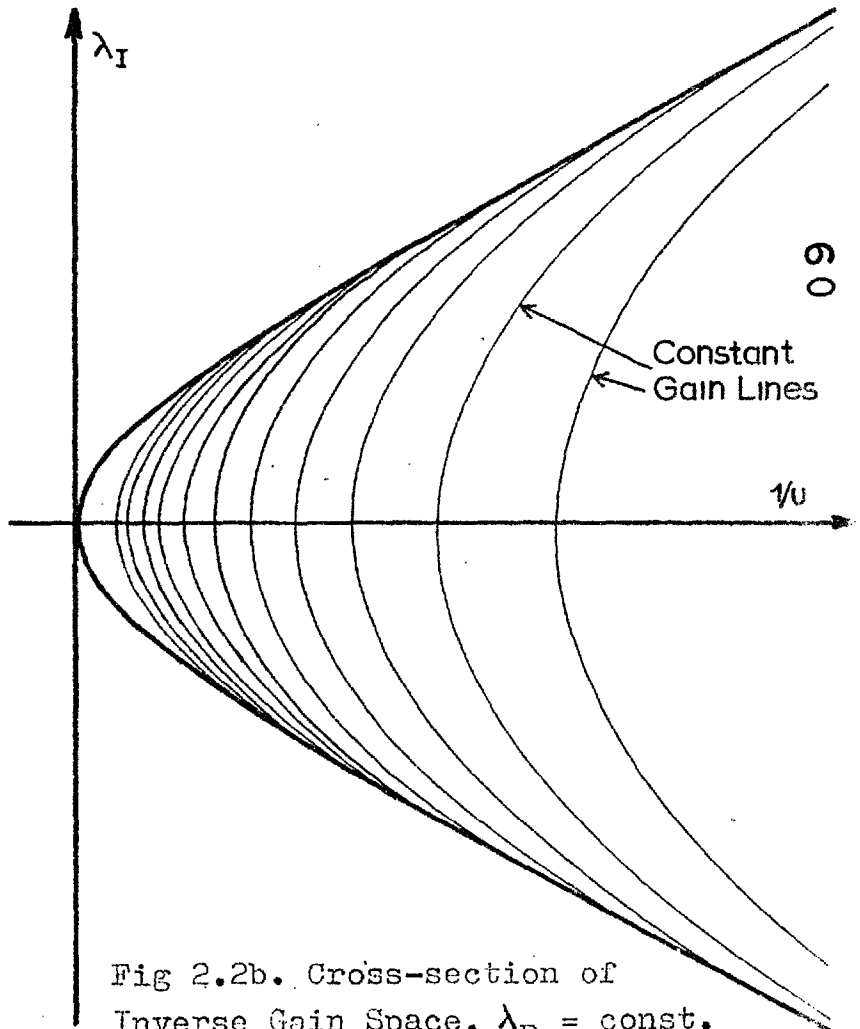


Fig 2.2b. Cross-section of Inverse Gain Space. λ_R = const.

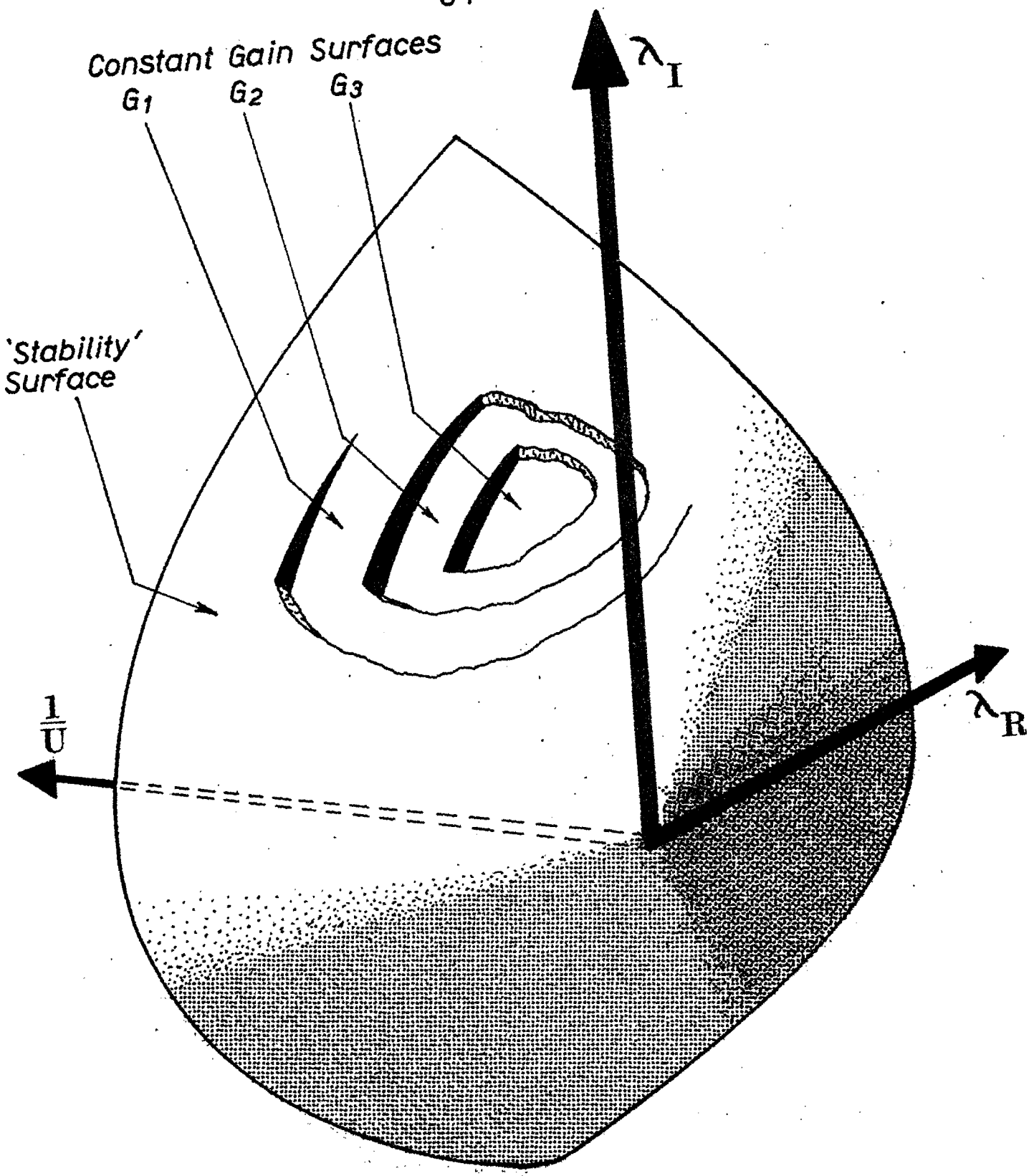
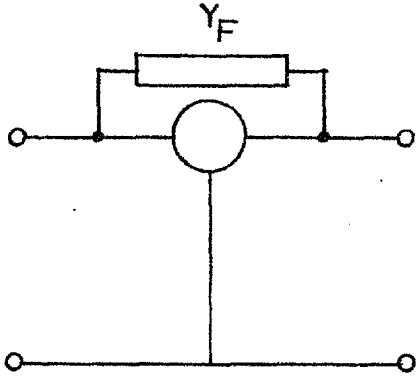
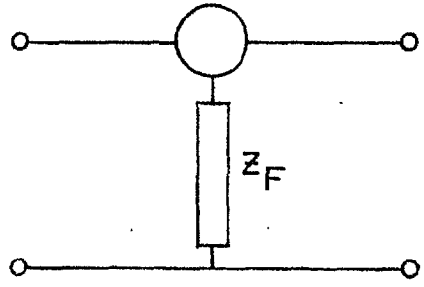


Fig 2.3. Model of the Inverse Gain Space.



Y-feedback

$$\begin{bmatrix} Y_{11}+Y_F & Y_{12}-Y_F \\ Y_{21}-Y_F & Y_{22}+Y_F \end{bmatrix}$$



Z-feedback

$$\begin{bmatrix} Z_{11}+Z_F & Z_{12}+Z_F \\ Z_{21}+Z_F & Z_{22}+Z_F \end{bmatrix}$$

Fig 2.4. Y and Z mode Embedding or Feedback.

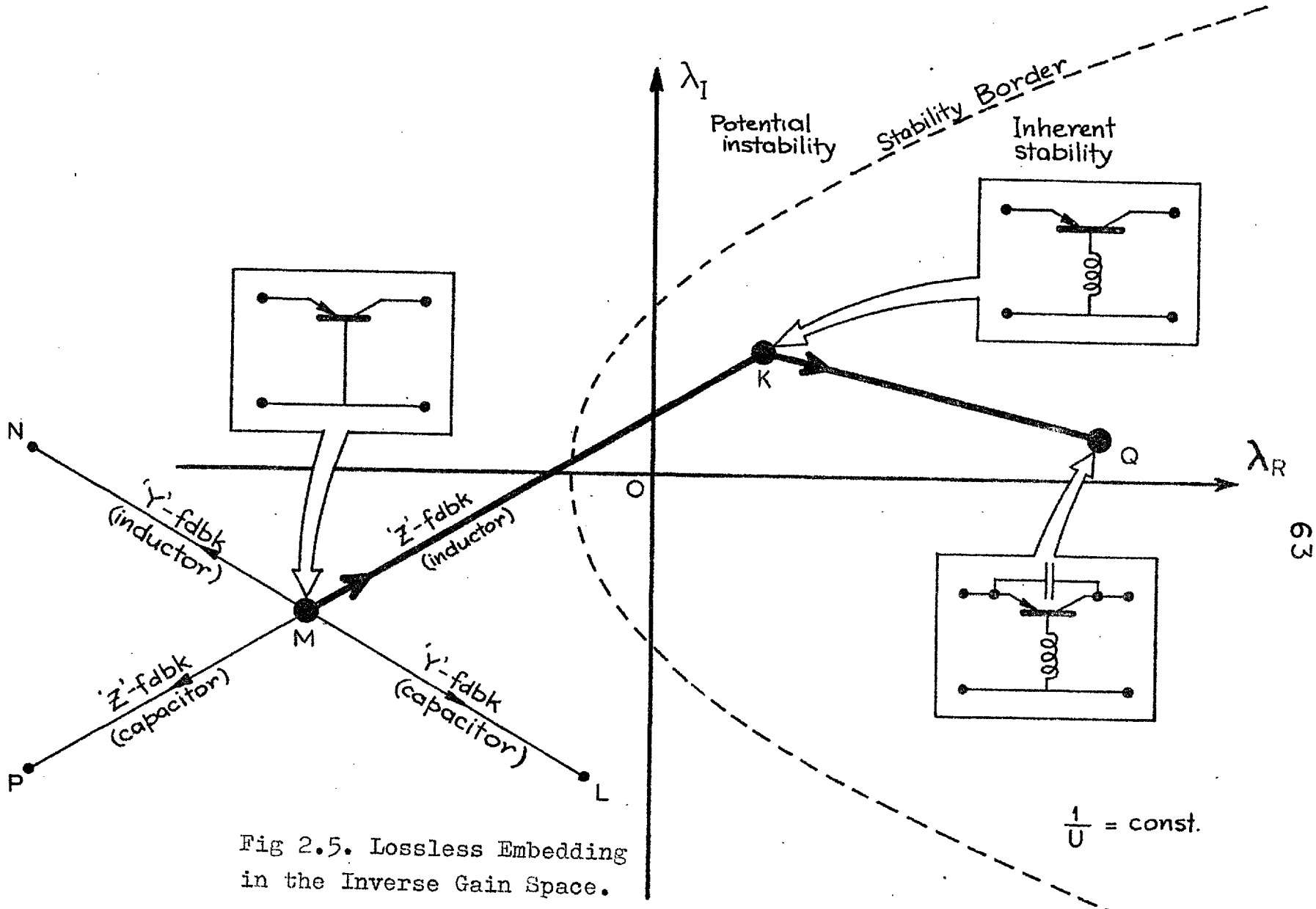
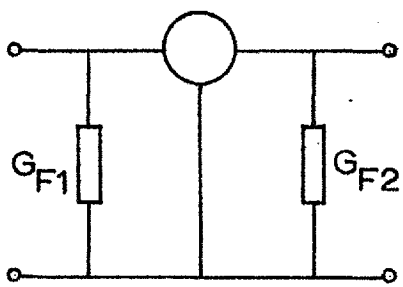
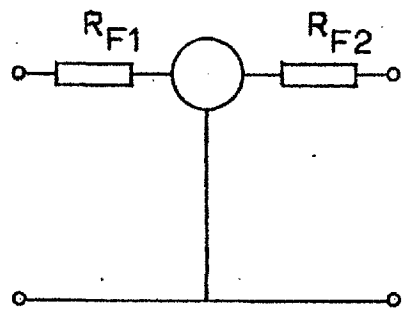


Fig 2.5. Lossless Embedding in the Inverse Gain Space.



Y-mode padding

$$\begin{bmatrix} Y_{11} + G_{F1} & Y_{12} \\ Y_{21} & Y_{22} + G_{F2} \end{bmatrix}$$



Z-mode padding

$$\begin{bmatrix} Z_{11} + R_{F1} & Z_{12} \\ Z_{21} & Z_{22} + R_{F2} \end{bmatrix}$$

Fig 2.6. Y and Z mode Port-padding.

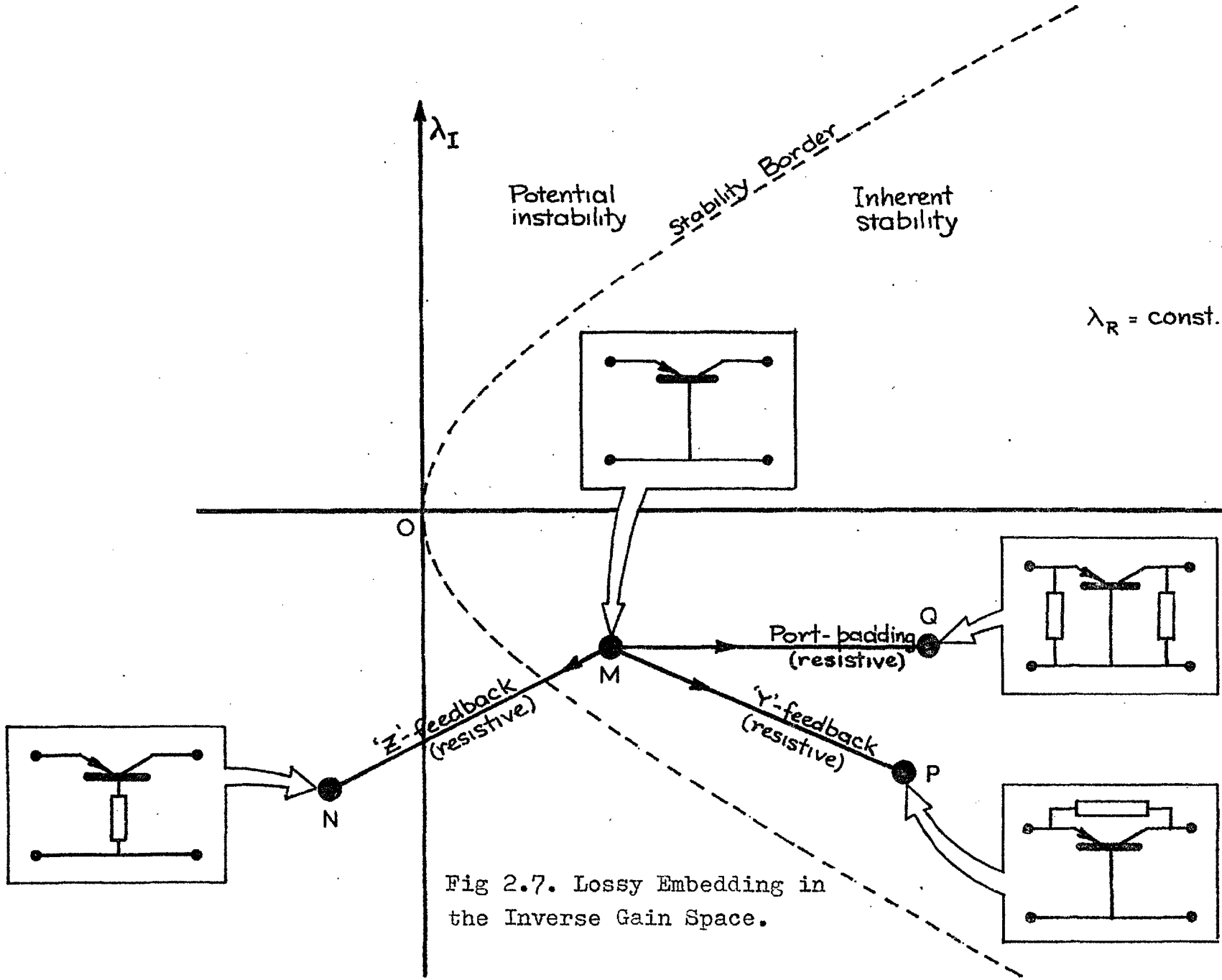


Fig 2.7. Lossy Embedding in the Inverse Gain Space.

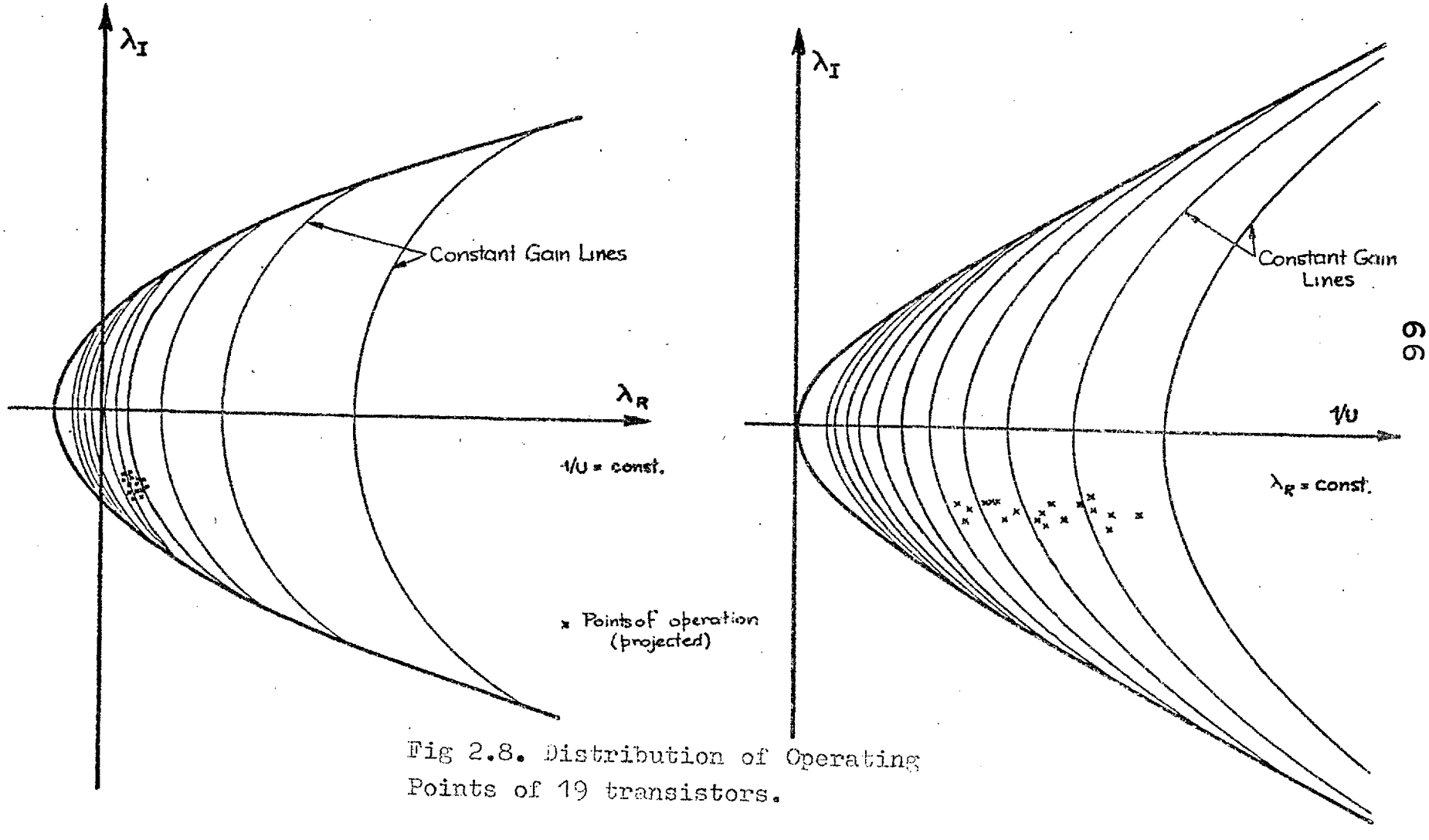


Fig 2.8. Distribution of Operating Points of 19 transistors.

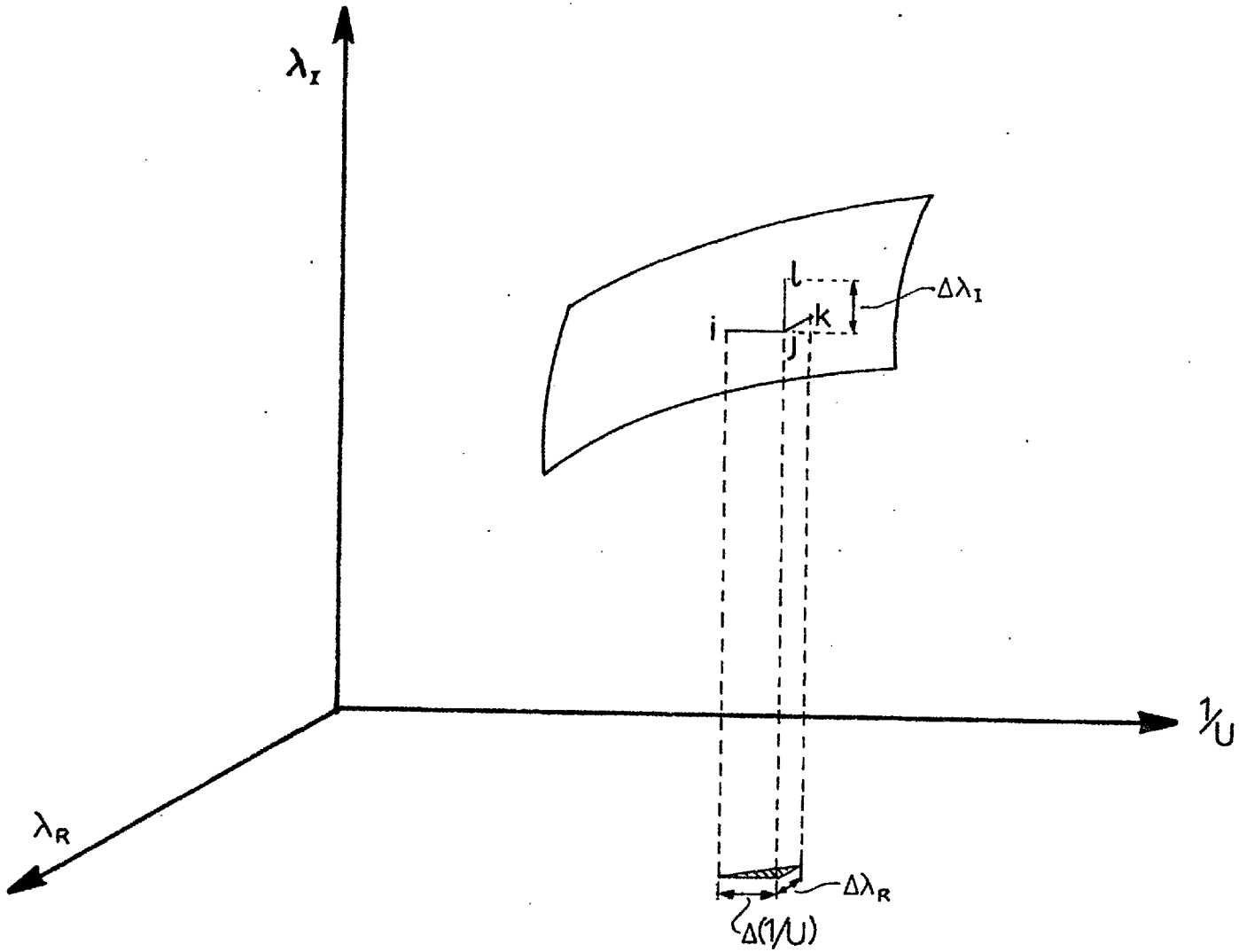


Fig 2.9. Definition of Spread in the Inverse Gain Space.

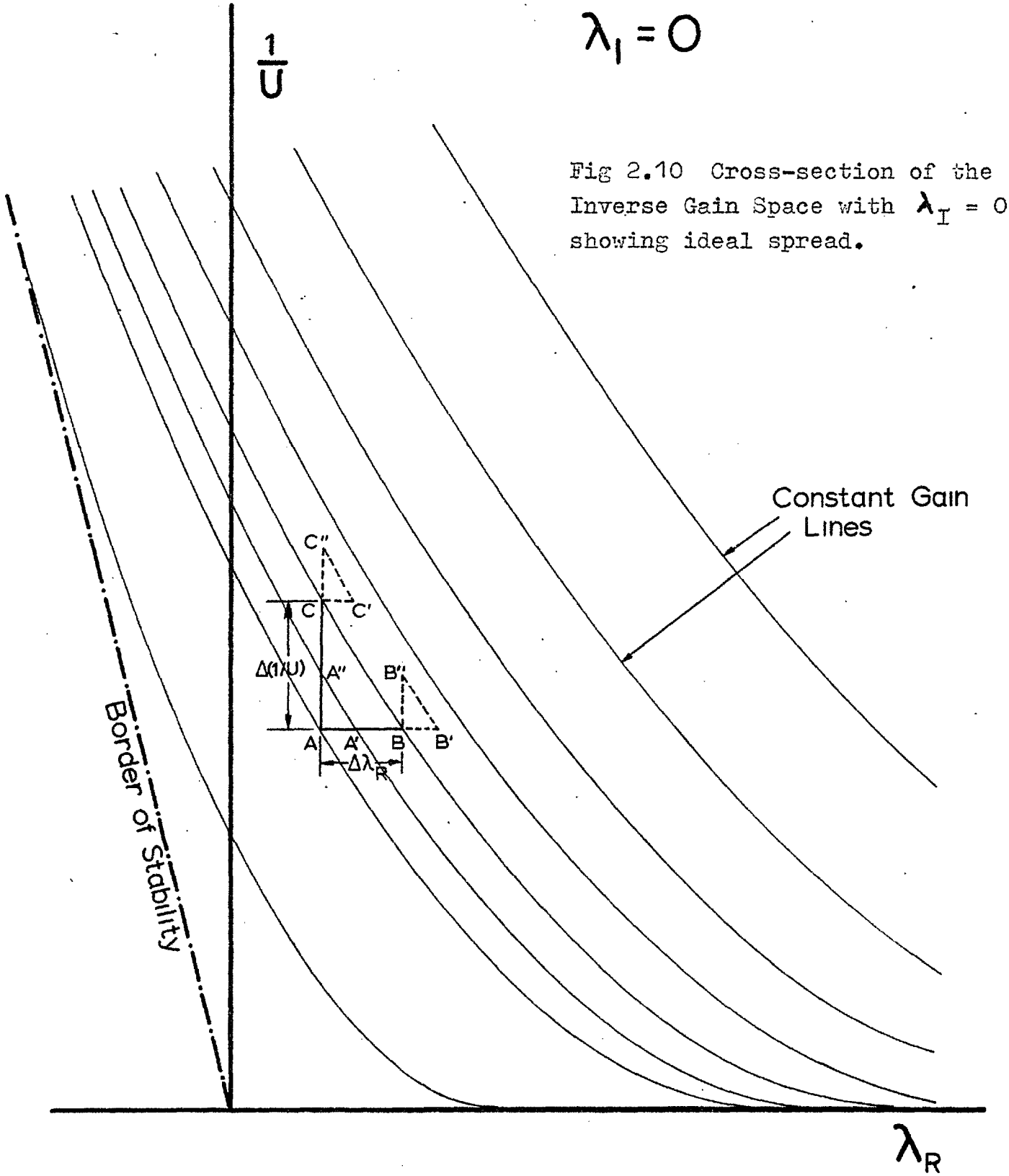


Fig 2.10 Cross-section of the Inverse Gain Space with $\lambda_I = 0$ showing ideal spread.

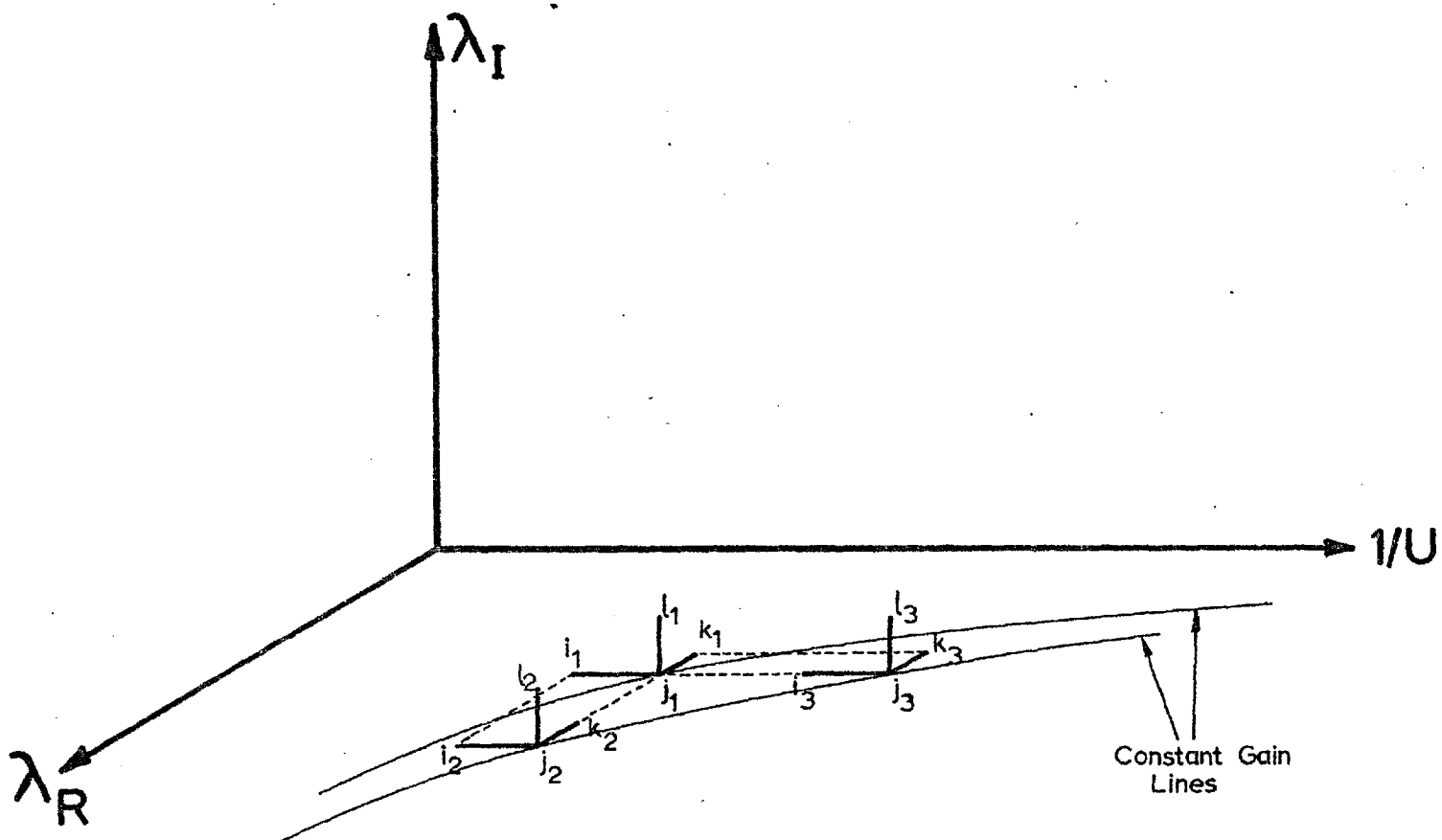


Fig 2.11. Spread and Embedding in the Inverse Gain Space. $\lambda_I = 0$.

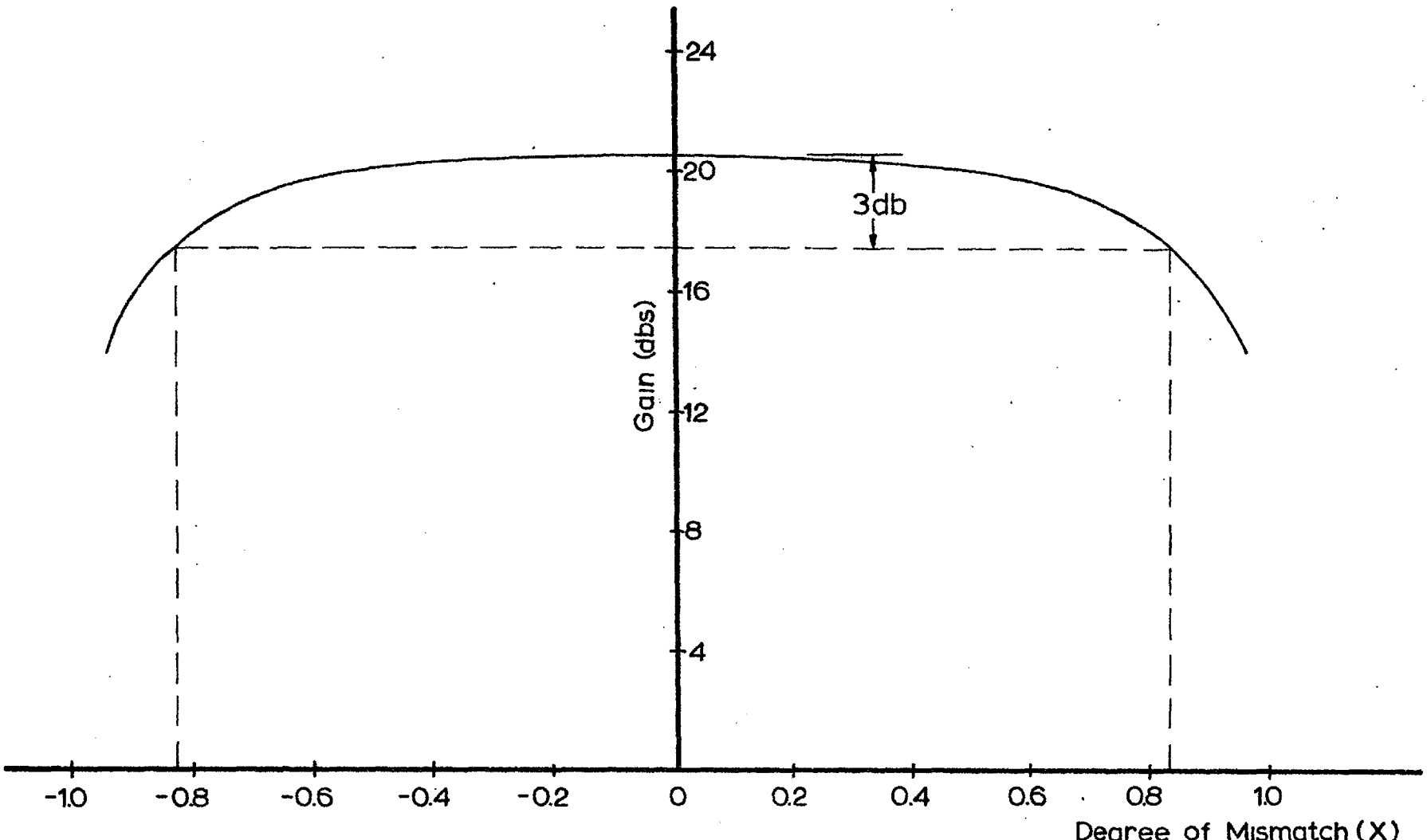


Fig 2.12 Gain Vs Degree of Mismatch.

Chapter 3

ACTIVITY, UNILATERAL GAIN AND STABILITY

3.1 ACTIVITY

A device which is capable of delivering more signal power to a load than it receives, is generally described as 'active'. A device which always returns or dissipates signal power is usually described as 'passive'. Examples of the former are valves, transistors and tunnel-diodes, and of the latter, capacitors, inductors, transformers and positive resistors.

Practically every electronic equipment contains an active element for amplification, oscillation or switching. It is therefore profitable for the circuit engineer to have a clear understanding of activity and, if possible, to devise a way of measuring the activity of a given device for the purposes of comparison.

In general terms, activity manifests itself in two ways. For a three-terminal two-port linear device, if more signal power can be taken out of a port than is fed into another port, the activity displayed is of the transfer variety and is described as transfer activity. Two-port amplifiers employ this type of activity. Negative conductance activity, as the name implies, is due to the presence of a negative conductance seen "looking in" at a pair of terminals. This may be due to a negative $Re(Y_{11})$, a negative $Re(Y_{22})$ and/or a negative

conductance* arising from terminating one port of the device with passive reciprocal elements. This is a one-port property and generally associated with reflexion amplifiers.

3.1.1 Power Flow

For a two-port three-terminal device, it can be shown that the total flow of signal power into the device is given by

$$\frac{P}{|V_1 V_2|} = aY_{11} + a^{-1}Y_{22} + Y_{21}e^{j\alpha} + Y_{12}e^{-j\alpha} \quad (3.1)$$

where

$$a = |V_1/V_2| \quad \text{and} \quad \alpha = \underline{/V_1/V_2}$$

We are interested in the real part of this power as it will give an indication of the activity or passivity of the device. The orientation of the voltages and currents used in (3.1) are defined in Fig. 3.1a.

Taking the real part of (3.1),

$$\mathrm{Re}\left(\frac{P}{|V_1 V_2|}\right) = a\rho_{11} + a^{-1}\rho_{22} + \mathrm{Re}\left[(Y_{21} + Y_{12}^{*})e^{j\alpha}\right] \quad (3.2)$$

Since we are considering the flow of power into the two-port and this has to be negative if the device is active, the minimum value of the real part of $P/|V_1V_2|$ ought to give conditions for activity. The two ways in which the real part of $P/|V_1V_2|$ could be negative are

---

*This happens only if the two-port is potentially unstable.

either that

$$0 > \rho_{11} \tag{3.3}$$

or

$$0 > \rho_{22} . \tag{3.4}$$

However, assuming that both ρ_{11} and ρ_{22} are positive, the first two terms on the right-hand side of (3.2) give the least positive value when $a = +\sqrt{\rho_{22}/\rho_{11}}$ and the third term the most negative when the phase angle is an odd integral multiple of π. Under these conditions, (3.2) becomes:

$$\mathrm{Re}\left(\frac{P}{|V_1 V_2|}\right) = 2\sqrt{\rho_{11}\rho_{22}} - \left|Y_{21} + Y_{12}^{*}\right| \tag{3.5}$$

so that if,

$$\left|Y_{21} + Y_{12}^{*}\right|^2 > 4\,\rho_{11}\rho_{22} , \tag{3.6}$$

the device is active. Several authors such as Raisbeck[39] and Fjaellbrant[40] have derived the above conditions.

3.1.2 Negative Conductance Activity

For a two-port, the admittance 'looking in' at the input and the output ports respectively are

$$Y_{in} = Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22} + Y_L} \tag{3.7}$$

$$Y_{out} = Y_{22} - \frac{Y_{12}Y_{21}}{Y_{11} + Y_s} \tag{3.8}$$

where Y_s and Y_L are the admittances of the source and load respectively.

If the device is inherently stable, then the $Re(Y_{11}) > 0$ and provided that Y_L is passive and reciprocal, the $Re(Y_{in})$ will always be positive. On the other hand, if the device is potentially unstable, the $Re(Y_{11})$ can be negative and/or a passive reciprocal Y_L exists which will make the $Re(Y_{in}) < 0$. The above statement is true if Y_{11} is replaced by Y_{22}, Y_{in} by Y_{out} and Y_L by Y_s.

With passive embedding, the sign of the $Re(Y_{in})$ and the $Re(Y_{out})$ can be changed as desired. Fig. 3.1b shows an embedded device with a positive conductance g, equal to the $Re(Y_{in})$, and a susceptance equal $-Im(Y_{in})$ (for optimum power transfer to g) both connected across the port.

The use of negative conductance activity in amplifying circuits is relatively rare at radio frequencies although at microwave frequencies, the technique is well known. Tunnel-diode amplifiers have been built which make use of the negative conductance characteristics of the device. The reason for the under-development of negative conductance activity amplifiers at radio frequencies is inherent in the one-port nature of the activity. With one-port activity, signal power must be fed into the same port as it is taken out, and while separation of incident and reflected power can be obtained at microwave frequencies by the use of circulators, no reasonable means has been found for use at lower frequencies.

Negative conductance activity can be exploited in the design of 'active impedance transformers'. To illustrate the principle, we may

consider resistances instead of conductances. If R_s and R_L are source and load resistances respectively and $R_s > R_L$, it can be shown that by connecting a negative resistance R_n such that $|R_n| > |R_L|$ the source and input can be conjugately matched. In doing so, the power developed in the load is increased by a factor of $(R_s + R_L)^2/(2R_L)^2$ over that which would have been obtained using a 'passive' transformer. This arrangement (shown in Fig. 3.1c) can be looked upon as an amplifier operating with a source and load both of which are connected to the same terminals.

3.1.3 Transfer Activity and Unilateral Power Gain

When (3.6) holds, the device is capable of exhibiting 'transfer activity' properties and naturally the device must have at least two ports. Subtracting from each side (3.6), the term $4\rho_{12}\rho_{21}$, the condition remains unchanged and we have,

$$|Y_{21} - Y_{12}|^2 > 4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21}). \qquad (3.9)$$

Mason[16] defined a quantity U as,

$$U = \frac{|Y_{21} - Y_{12}|^2}{4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21})} \qquad (3.10)$$

and obtained the condition for transfer activity as $U > 1$. The quantity U has the same value as the gain that can be obtained from the device if it is unilateralised by lossless reciprocal embedding and hence the name unilateral power gain is appropriate.

On condition that $(\rho_{11}\rho_{22} - \rho_{12}\rho_{21}) > 0$, we can divide both sides of (3.9) by $4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21})$ and obtain the result of Mason. Similar forms of the formula given by (3.10) exist for Z-, h- and g-matrices and have the property of giving the same numerical result whichever matrix form is used. U also has the property of remaining invariant with lossless embedding.

When $(\rho_{11}\rho_{22} - \rho_{12}\rho_{21}) < 0$, dividing both sides of (3.9) by $4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21})$ we get

$$\frac{|Y_{21} - Y_{12}|^2}{4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21})} < 1 \qquad (3.11)$$

(the inequality sign is reversed since the divisor is negative). The left hand side of (3.11) is negative since the numerator is always positive and the denominator is negative. Therefore we can write $U < 0$ without violating (3.11). The complete condition for activity is therefore,

$$0 > U \quad \text{or} \quad U > 1 \qquad (3.12)$$

3.1.4 Unilateral Power Gain with Lossy Embedding

Assuming that the $\mathrm{Re}(Y_{11}) > 0$ and the $\mathrm{Re}(Y_{22}) > 0$, Y-mode lossy embedding and port-padding have the common effect of reducing the value of U. This was discussed in section (2.3.2). The effect of lossy embedding in the Z-mode was only briefly mentioned, and will now be discussed in detail.

It can be shown (Appendix D) that if

$$R_{12} + R_{21} > R_{11} + R_{22}, \tag{3.13}$$

then the addition of resistance in series with any of the leads will result in an increase of the value of U provided that

$$R_f \leqslant \frac{R_{12}R_{21} - R_{11}R_{22}}{R_{11} + R_{22} - R_{12} - R_{21}} \tag{3.14}$$

where R_f is the embedding resistor and $Z = R + jX$.
A plot of R_f against U is given in Fig. 3.2 for a transistor which satisfies (3.13). As R_f is increased, U increases rapidly and goes through a discontinuity after which it becomes negative. Measured values are also plotted. No measured points could be obtained for negative values of U as the bridge used for the measurement was not capable of doing this.

If activity is defined as the ability of a device to support oscillation, then the load which the device is capable of supporting during oscillation could be used as a measure of its activity. If the U of a device were a measure of the activity of that device, then it would be surprising if the value of U could be increased by lossy (dissipative) embedding. Contrary to its use as a 'measure of goodness',[34] U remains a condition for the determination of the boundary between activity and passivity as given in (3.12).

The increased value of U obtained as a result of lossy embedding is of dubious value to the designer of amplifiers since it is not possible to obtain the gain which is associated with the increase in U

because of dissipation in the embedding resistor.

It must be noted that the transistor (together with its embedding) remains active when R_f is increased beyond the discontinuity. A small gain can be obtained from it.

3.2 STABILITY

A system is said to be stable if, when it is disturbed, the effects of the disturbance decay with time; if the effects of the disturbance grow with time, the system is said to be unstable. For two-ports, the criterion for determining whether a device is stable or not is the presence or absence of oscillation, with a given pair of terminations. If when the two-port is terminated in passive, reciprocal and infinitely variable elements, it is not possible to obtain oscillation, the two-port is said to be inherently stable. If a pair of terminations can be found which will make the two-port oscillate, the device is said to be potentially unstable. It must be noted that stability is a condition which defines a boundary between two states.

3.2.1 Stability and Activity

The definition of inherent stability rules out the possibility of negative conductance activity in an inherently stable device, given that no change in the embedding is allowed. This is because with passive reciprocal termination, the real part of the port immittance

can never be negative. Such a device can therefore only exhibit transfer activity. When it is possible to make the real part of the port immittance negative by means of passive reciprocal termination, the device is capable of exhibiting negative conductance activity and under conditions of mismatch, transfer activity as well.

3.2.2 Stability Factors

Since a potentially unstable two-port is capable of giving any gain, (infinite gain when it is unstable), it is necessary to have a means of estimating how far or near the device is to the threshold of oscillation. A stability factor is generally taken as a measure of the margin between the point of operation of the device and instability.[36,27] Thus two amplifiers with the same gain will be judged for superiority on the basis of their respective stability factors: the one with the higher numerical value being taken as the better of the two.

The two most popular stability factors were derived by Stern[26] and Venkateswaran[23] and designated the symbols k_i and S_i respectively. Where,

$$k_i = \frac{2\rho_1\rho_2}{L + M} \qquad \text{and} \qquad S_i = \frac{2\rho_{11}\rho_{22} - M}{L}.$$

The stability condition is given by $k_i > 1$ and $S_i > 1$, respectively. The results of assigning numerical values to k_i and S_i and their use as stability factors will now be examined.

If we plot constant values of k_i and S_i on a chart of M against N,

where $M + jN = Y_{12}Y_{21}$, we obtain curves as shown on Fig. 3.3. It can be seen that constant k_i values give parabolae symmetrical about the M-axis and that constant S_i values give ellipses also symmetrical about the M-axis. For the particular case $k_i = S_i = 1$, we have two coincident parabolae which divide the chart into inherently stable and potentially unstable regions. It is possible to obtain values of k_i less than unity whereas S_i breaks down for potentially unstable devices.

From Fig. 3.3, it can be seen that the constant k_i and S_i lines cross and therefore a device with a given S_i value can have quite a large variation in its k_i value and vice-versa.

If we plot the point of operation of a transistor on the chart and study the effect of lossless embedding on the point, we find that the point of operation moves in a straight line and the distance moved is directly proportional to the susceptance of the embedding element. The direction of movement and the elements required to achieve it are given in Fig. 3.4.

Supposing that we have two transistors operating at the points A and X, then each one would have a k_i value equal to 4. Supposing that for some reason they both developed equal inductances between their common terminal and ground of such a value that A moved to B and X moved to Y. It can be seen that the resulting two-ports will exhibit completely different properties: A would have become more 'stable' while X would have become potentially unstable. Therefore the margins between A and the threshold of instability cannot be the

same as that between X and the threshold of instability, and therefore k_i is an unsatisfactory measure of the stability margin.

A similar argument shows that S_i is no better than k_i as a measure of the stability margin.

It appears that stability can only be a 'go - no go' test and that when it is 'go', the only relevant factor we can consider is the sensitivity of the area in which the device is operating, to such changes as embedding elements, biasing point and the active device itself.

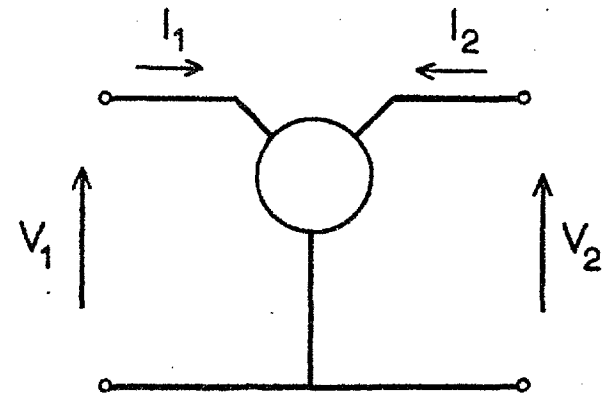


Fig 3.1a Orientation of Two-Port Currents and Voltages.

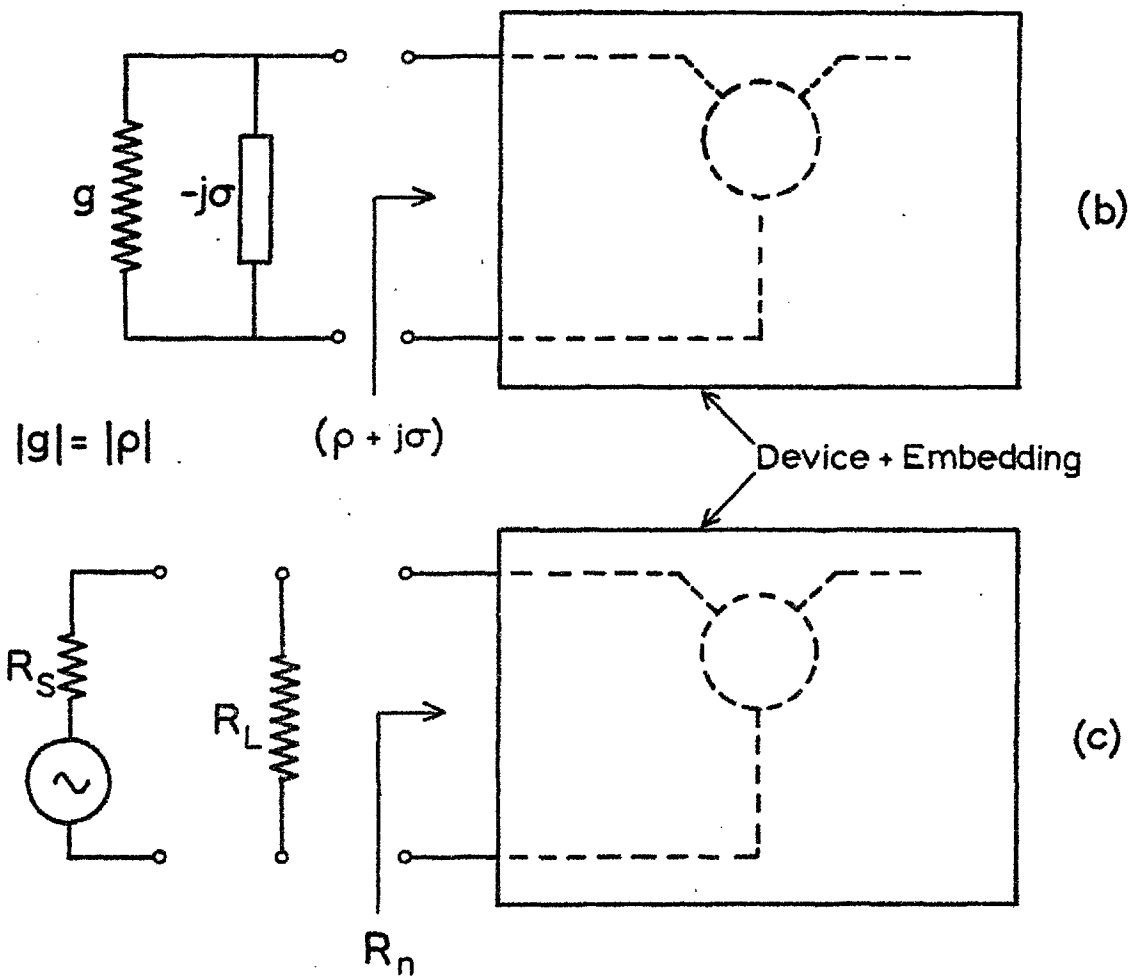


Fig 3.1b Negative Conductance used in an Oscillator.

Fig 3.1c Negative Resistance used in an Amplifier.

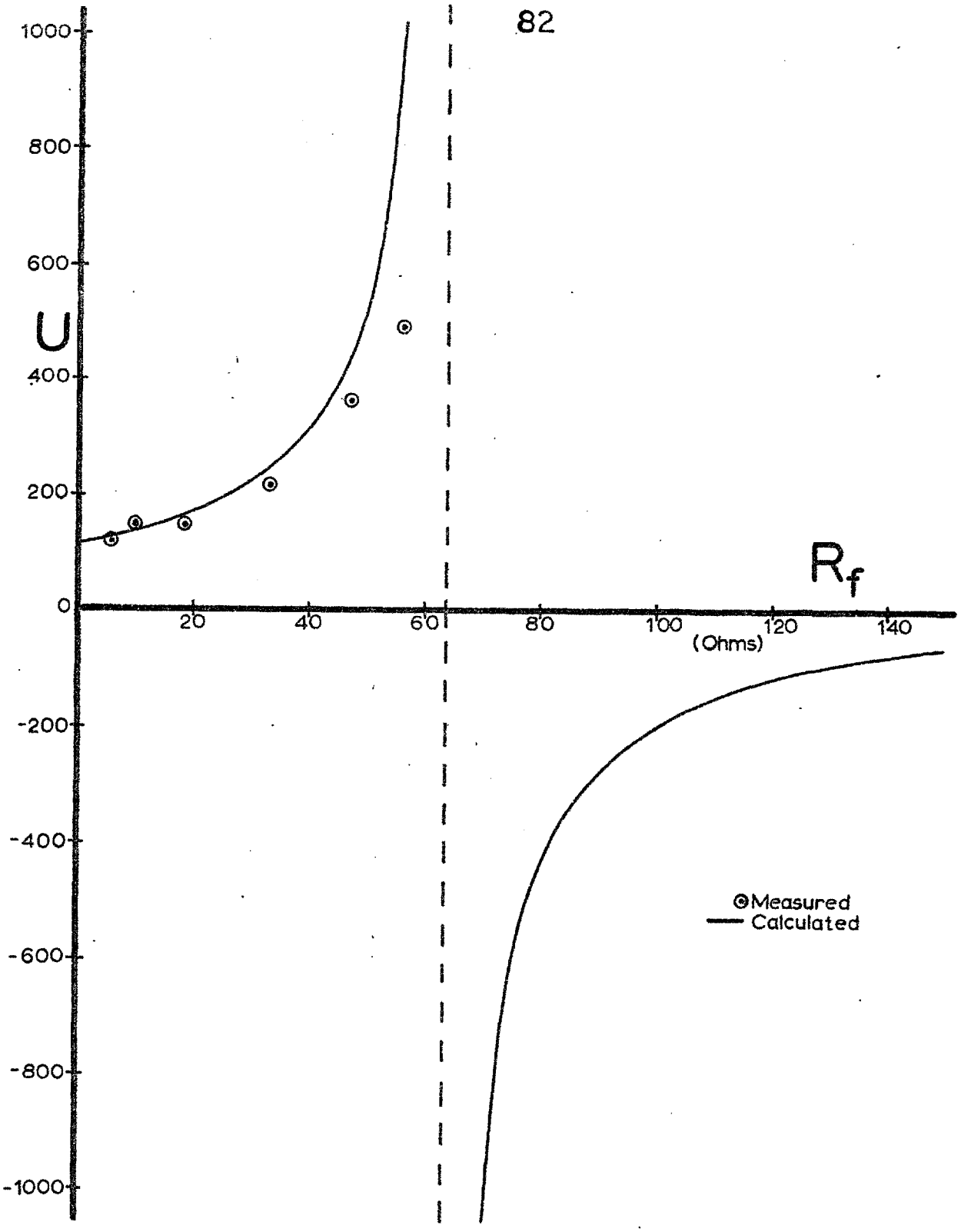


Fig 3.2 Graph of U against Embedding Resistance

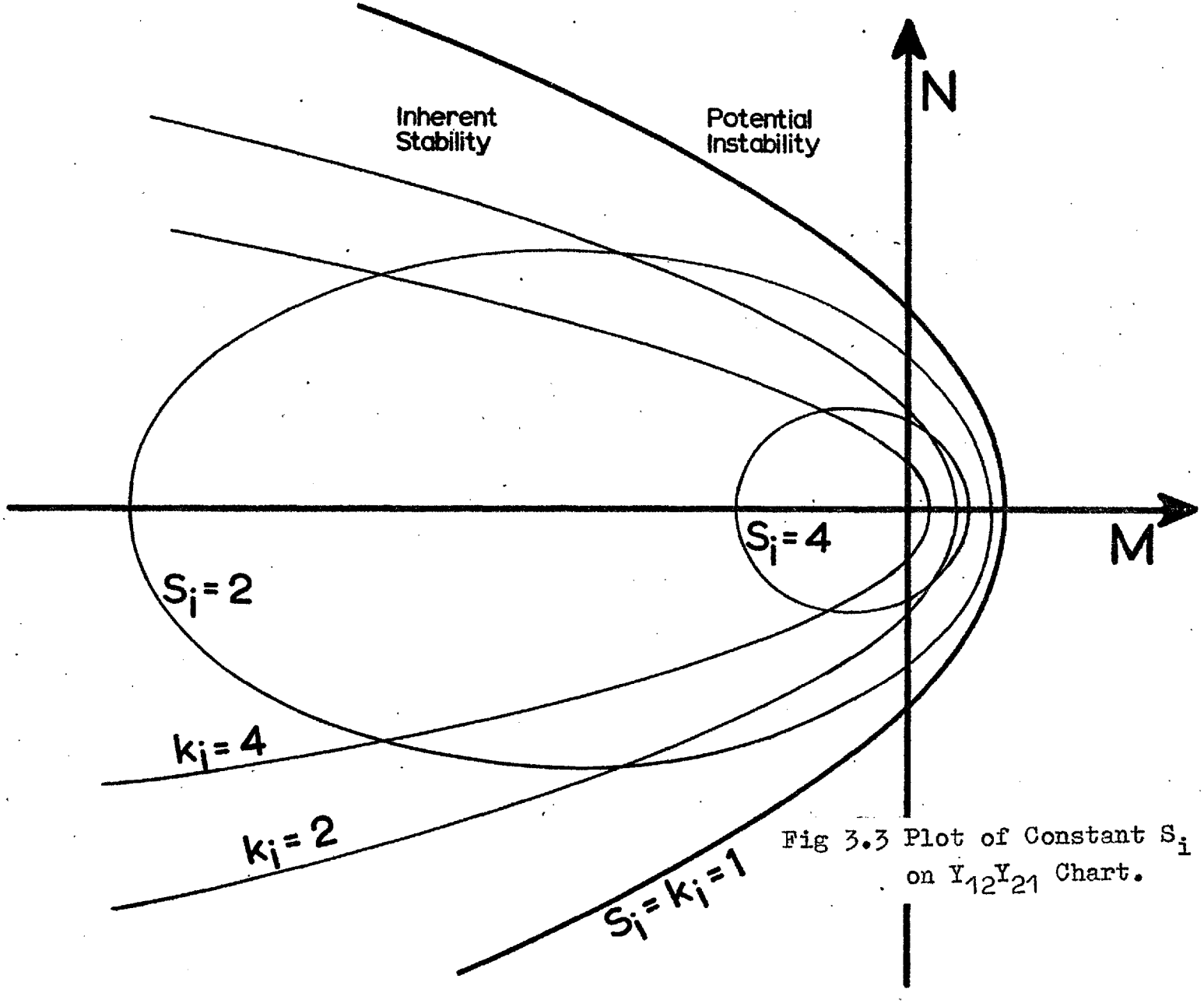


Fig 3.3 Plot of Constant S_i and k_i on $Y_{12}Y_{21}$ Chart.

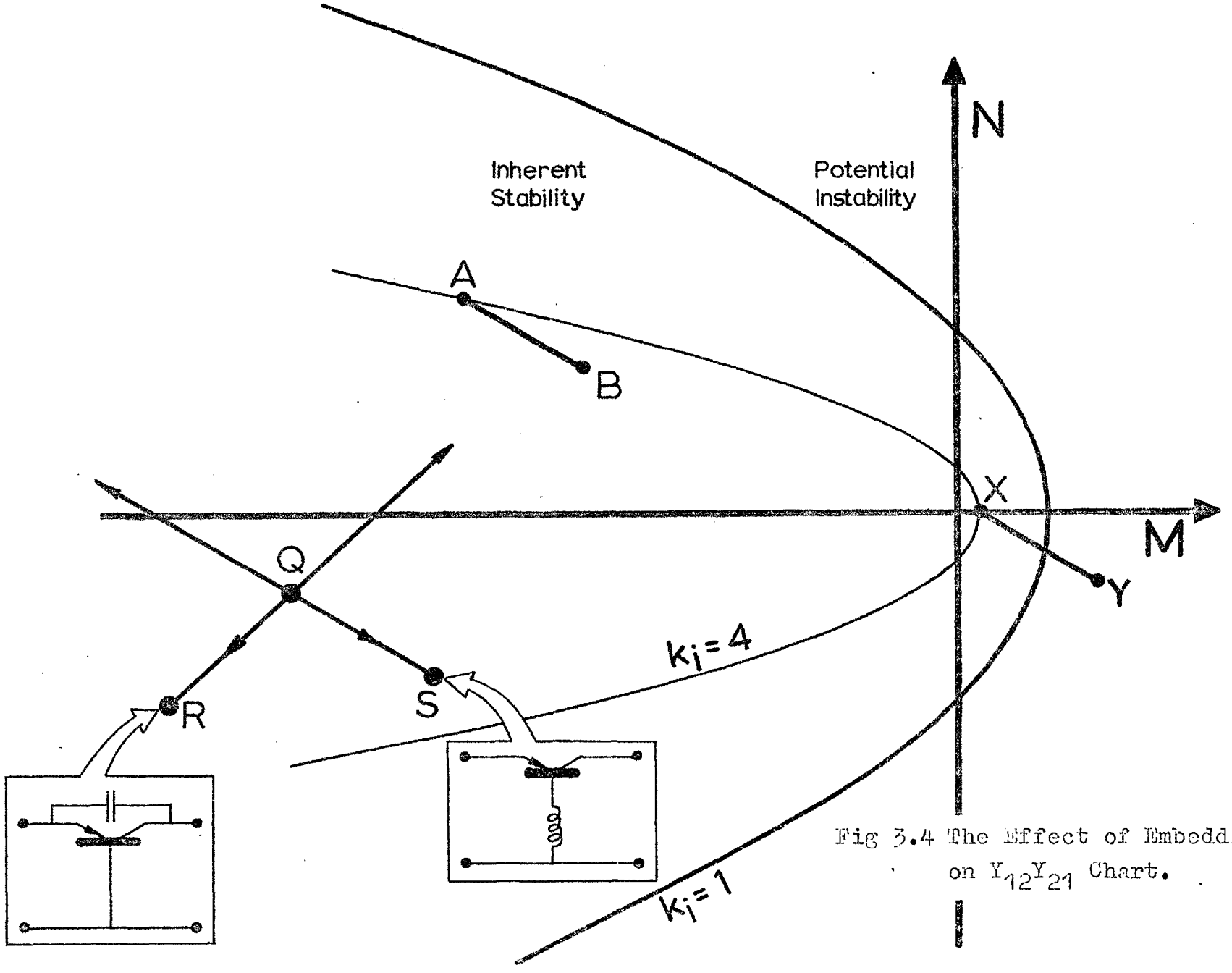


Fig 3.4 The Effect of Embedding on $Y_{12}Y_{21}$ Chart.

Chapter 4

DESIGN EXAMPLES

4.1 INTRODUCTION

In Chapter 2, gain-sensitivity performance was analysed for the conjugately matched two-port with lossless as well as lossy embedding. As a result, formulae were derived for the prediction of gain-sensitivity performance from the parameters of the two-ports.

In this Chapter, some design examples, with a batch of transistors, are given. Brief descriptions of computer programmes written for the purpose are also presented, and where necessary, flow diagrams of the programmes are given.

4.2 THE TRANSISTOR AS A TWO-PORT

4.2.1 Transistor Data

The transistors used in the experiments were Type 2G302 (Texas Instruments). Twenty of these were used and no attempt was made to select them on any basis: the first of the batch developed a fault during the tests and was discarded. The Y-parameters of the transistors were measured at 3Mc/s with an emitter current of 1 mA and -10 volts between emitter and collector on a Wayne Kerr Radio Frequency Bridge Type B601. Adaptors for biasing the transistors were designed for

this purpose.

4.2.2 The Transistor in the Inverse Gain Space

The advantages of using the IGS in the study of gain-sensitivity of active two-ports have been discussed in detail in Chapters 1 and 2. One of its major drawbacks will now be examined. Y-parameters will be used throughout although any other set of parameters could be used with equal facility.

A two-port three-terminal device can be described by a 2X2 matrix. In general, each of the elements of the matrix is complex and therefore the device can be characterised by eight quantities. In order to simplify the design theory, three basic parameters, namely λ_R, λ_I and $1/U$, were calculated from the matrix. However, the effect of embedding on the three parameters cannot be calculated except by using the eight elements in the matrix. This means that we cannot select a point in the inverse gain space and study the effects of embedding on a device which operates there without actually measuring such a device. The problem can be put more clearly if we consider the situation which arises when we start to design a suitable embedding for a batch of transistors to satisfy a given gain-sensitivity requirement. One way of doing this is to base the design on the 'average' transistor: this was the method adopted. Now it might happen that when we have plotted the points of operation of the batch of transistors in the IGS, that one of the transistors sits in the 'middle' of the

batch so far as the coordinates are concerned and has a gain which is equal to the average of the whole batch. Such an occurrence would be fortunate and we can use this peculiar transistor for the design. In general, we have to 'make' such a transistor to be able to design our circuit. This means working backwards from the values of λ_R, λ_I and 1/U to obtain eight Y-parameters.

If we write down the equations relating our coordinates to the Y-parameters namely,

$$\frac{\rho_{12} + j\sigma_{12}}{\rho_{21} + j\sigma_{21}} = \lambda_R + j\,\lambda_I \qquad (4.1)$$

and

$$\frac{4(\rho_{11}\rho_{22} - \rho_{12}\rho_{21})}{|Y_{21} - Y_{12}|^2} = 1/U \ , \qquad (4.2)$$

it is apparent that with a knowledge of λ_R, λ_I and 1/U, it is impossible to obtain values for the other parameters.

4.3 A STATISTICAL SOLUTION

One way of overcoming the problem is to measure a sample of transistors and calculate the corresponding values of λ_R, λ_I and 1/U. We can now use the data in a regression with λ_R, λ_I and 1/U as independent variables and each of the eight elements in the matrix in turn as the dependent variable.

4.3.1 Brief Description of the Regression Program

The program is briefly outlined here; the algorithmn is given in Appendix A.

The data was obtained from the batch of 19 transistors whose Y-parameters had been measured and from which the corresponding values of λ_R, λ_I, and 1/U have been calculated. Each of the eight values constituting the Y-parameters is taken in turn to be the dependent variable and λ_R, λ_I, 1/U are made the independent variables so that the regression model is of the form:

$$\rho_{11} = a + b_1\lambda_R + b_2\lambda_I + b_3(1/U). \qquad (4.3)$$

The coefficients of multiple correlation obtained from the above model are given in Table 1.

As some of the coefficients of multiple correlation for the linear model were rather low, the second order model was adopted instead. The mathematical model was of the form:

$$\rho_{11} = a + b_1\lambda_R + b_2\lambda_I + b_3(1/U) + b_4\lambda_R^2 + b_5\lambda_I^2 + b_6(1/U)^2 + b_7\lambda_R\lambda_I + b_8\lambda_R(1/U) + b_9\lambda_I(1/U). \qquad (4.4)$$

The coefficients of multiple correlation calculated from this model are also given in Table 1.

Table 1

	Coefficient of Multiple Correlation	
Parameter	Linear	2nd Order
ρ_{11}	0.809	0.997
σ_{11}	0.557	0.931
ρ_{12}	0.865	0.996
σ_{12}	0.992	0.999
ρ_{21}	0.991	0.997
σ_{21}	0.809	0.991
ρ_{22}	0.612	0.927
σ_{22}	0.841	0.958

Table 1 indicates that the second order regression provides much better results than the linear one, and also that it would be unnecessary to go to a higher order than second.

It is now possible to synthesise the matrix of a transistor given its coordinates in the inverse gain space. In general, we might be interested in synthesising a transistor with a given value of gain, $1/U$ and λ_R. In this case, we can calculate the value of λ_I which is required from the basic equation,

$$\lambda_I^2 + (\lambda_R - 1/G)^2 - 1/GU = 0 . \qquad (4.5)$$

Having obtained the three coordinates which give the required gain, these can be substituted into (4.4) to evaluate the elements of the matrix which may be in the Y , Z , h , or g form.

Some caution should be exercised in employing this technique. The coefficients obtained from a set of data can be used to make inferences about that particular set of devices to which the data applies. The coefficients have no physical meaning and may give rise to nonsensical results if used outside their range of validity. This is a general rule and should be observed religiously in all statistical techniques.

4.3.2 Synthesis of the Average Transistor

If the coordinates of the centroid of the points of operation of the batch of transistors are used for the synthesis of the matrix of the average transistor, it is found that the synthesised transistor has a gain different from taking the average of the gain of the batch. This is because the average gain surface does not go through the centroid of the points of operation.

To obtain the true average transistor, it is necessary to find a point which lies on the constant gain surface representing the average gain. Since one of the conditions for optimum gain-sensitivity operation is to embed the devices such that $\lambda_I = 0$, assuming that the relative positions of the points of operation are preserved when embedding is applied, the mean value of λ_I must be used in the regression, so that the "moments" of the points of operation about the plane given by $\lambda_I = 0$ are as near to zero as possible. Fig. 4.1a shows the points of operation of the batch before and after

embedding.

The basic equation of the IGS is given by equation (4.5) and so far we have obtained two of its parameters: the gain G and λ_I. We can now choose a value for λ_R and calculate 1/U or vice-versa. Fig. 2.8 shows that the spread in λ_R is much less than that in 1/U and since, statistically, the mean only makes sense when wide divergences do not occur in the sample, it is better to use the mean value of λ_R and then calculate 1/U. We now have the three values we need for calculating the Y-parameters of the average transistor and can proceed to substitute them into the regression model (4.4).

4.3.3 Results of Average Transistor Synthesis

Using the following values in the regression equation, $\lambda_R = 1.87 \times 10^{-3}$, $\lambda_I = 5.17 \times 10^{-3}$ and G = 96.0 which gives $1/U = 9.58 \times 10^{-3}$, we obtain the Y-parameters of the average transistor as follows:

$$\begin{bmatrix} 4.73153 + j6.24221 & -0.04335 - j0.13977 \\ 21.23883 - j16.05998 & 0.16589 + j0.36784 \end{bmatrix} \qquad (4.6)$$

From the Y-parameters, we can calculate the values of λ_R, λ_I and 1/U and compare these to the original. The results are

$$\lambda_R = 1.867 \times 10^{-3}, \quad \lambda_I = 5.168 \times 10^{-3}, \quad 1/U = 9.537 \times 10^{-3}$$

and G = 95.5.

The two sets of values compare favourably and therefore the conclusion

can be drawn that the method is valid.

4.4 EMBEDDING IN THE INVERSE GAIN SPACE

4.4.1 Use of the Computer in Embedding

Given a transistor, we can locate its point of operation in the IGS. Considering lossless embedding, the point might be at P in Fig. 4.2. Supposing we want to move the point to X, then we have to connect in series with the common terminal a reactance of such a value as to move the point from P to A and then connect a susceptance between the input and output leads of such a value as to move the point from A to X. To reach the point W, as before, we have to use a reactance of such a value as to move the point to B and then using a susceptance between input and output the point can be moved to W. It is interesting to note that although we can calculate the direction of the lines PR and PQ, we cannot calculate the direction of the line AX until we have obtained the parameters of the transistor at A. This is because the device at A is a different device from that which was originally at P and therefore the line PQ is not parallel to the line AX. Similarly, the line BW is neither parallel to PQ nor to AX. These can be seen from Fig. 4.3 in which the final points of operation on the λ_R axis are equally spaced.

It appears that the easiest way to tackle the problem manually is to assume a point such as C, in Fig. 4.2, on the line PR, which is reasonably close to where we expect A to be. From the distance PC,

we can calculate the value of a series inductance L_s (refer to Fig. 2.5). The parameters of the device together with the series inductance can now be calculated to give the new device with point of operation at C. We can now calculate the direction of movement which results from connecting a parallel inductance L_p between input and output leads and locate the point of intersection of this line with the λ_R axis. Supposing the point is at U, i.e. larger than X, then we can see that PC is longer than required and we have to take a shorter distance for PC and start the whole process again. The process described above is a fairly straight forward operation which can be done very rapidly by a digital computer.

4.4.2 The Lossless Embedding Routine

The flow chart of the routine is given in Fig. 4.4. In addition, the actual routine is given in Appendix B. A brief description suffices here.

In Fig. 4.4, E and W contain the arbitrary step lengths 0.01. These step lengths are changed automatically in the programme should they turn out too large. K and K' contain either +1 or -1 and determine the sign of the Z-embedding and Y-embedding elements respectively. Y and Z contain the modulis of the final value of the Y-embedding and Z-embedding elements respectively. I' contains the number of times that the iterative process is executed and there is a trap (not shown in the flow chart) which prevents the iteration from continuing after

the 15th time. If this happens, the value of E is divided by 10 and the iteration is resumed. The output contains information indicating that the iteration has been trapped and reasons for this occurrence, so that the programmer can alter, if necessary, the trapping condition. For all the embedding design in this work, $I' \geq 15$ was found adequate. The numbered junctions refer to instruction numbers in Appendix B.

The upper half of the flow chart examines the position of the point of operation of the transistor and determines what element types will move the point of operation of the transistor to the required point on the λ_R axis i.e. it determines whether K and K' should have +1 or -1 stored in them. The second-half does the iteration and jumps out of the cycle when the error in both λ_R and λ_I is less than 5×10^{-5}.

4.4.3 The Y-Mode Port-Padding Routine

It was pointed out in Chapter 2, Y-mode port-padding is better at the output than at the input and Z-mode port-padding is superior at the input than at the output. Since in this work, Y-parameters have been used throughout, this routine was developed only for Y-mode output port-padding.

The routine solely changes the real part of Y_{22} such that 1/U has the required value. It uses an arbitrary but automatically adjustable step length contained in E which is equal to 0.01 and the error permitted is less than 1.0×10^{-5}. The routine is given in

Appendix C.

4.4.4 The Y-Mode Lossy Embedding Routine

It was mentioned in section (2.5.3) that the use of Y-mode lossy embedding had a number of practical objections. Two of these will now be discussed.

The use of lossy Y-mode embedding must be accompanied by lossless embedding if the condition for optimum gain-sensitivity is to be preserved, namely $\lambda_I = 0$. Both of these types of embedding change the gain of the amplifier and it is not at all clear what percentage of the change to assign to each type of embedding.

The second and more serious objection to lossy Y-mode embedding is that it is not possible to reach some points on the $\underline{\lambda}$-plane after this type of embedding has been applied. Fig. 4.5 shows a device which sits at the point D after the application of Y-mode lossy embedding. Z-mode lossless embedding moves the point along the line AE. At the points A, B, C, D, and E, Y-mode lossless embedding is applied to move the point of operation on to the λ_R axis. From Fig. 4.5 it is easy to see that the point of operation cannot be moved to the right of V. This is obviously an unacceptable limitation on the possible points of operation.

4.5 AVERAGE AND EXTREME TRANSISTORS

We have so far synthesised the matrix of the average transistor and from the batch, we can select the two transistors which give extreme gain i.e. the highest and lowest. We make an assumption that the extreme gain transistors before embedding give extreme gain after embedding has been applied. Singhakowinta[34] has shown that the angle of the locus of the point of operation of the transistor when lossless embedding is applied makes an angle approximately equal to $\angle Y_{21}$ with the λ_R axis. Thus it could happen that two transistors which operate at A and B ($G_A \geq G_B$) in Fig. 4.1b could have such angles of $\angle Y_{21}$ that when embedded losslessly, $G'_B \geq G'_A$. Such 'cross-overs' occur within the batch of transistors used in the experiment and lead to small and negligible changes in the 'gain ratings'. However, in three separate batches of 25, 2G302's and two other batches of OC44's, it was found that the extreme transistors before the application of lossless embedding were also the extreme transistors after embedding. This supports the above assumption.

A similar situation occurs in the case of port-padding although in that case cross-overs do not occur.

We are now in a position to design the embedding and apply it to the extreme transistors.

4.5.1 Calculated Limits of Gain

The required average gain is defined in terms of the position of the point of operation on the λ_R axis of the average transistor. With

this value, we enter the lossless embedding routine and at the end we have two values for the elements, namely K'Y and KZ. Taking the Y-parameters of one of the extreme transistors we embed in the Y-mode to obtain:

$$\begin{bmatrix} Y_{11} + K'Y & Y_{12} - K'Y \\ Y_{21} - K'Y & Y_{22} + K'Y \end{bmatrix} \qquad (4.7)$$

The above Y-matrix is then converted into Z-matrix with elements Z'_{11}, Z'_{12}, Z'_{21}, and Z'_{22}. The Z-embedding is then added to obtain:

$$\begin{bmatrix} Z'_{11} + KZ & Z'_{12} + KZ \\ Z'_{21} + KZ & Z'_{22} + KZ \end{bmatrix} \qquad (4.8)$$

The gain of the extreme transistor is then the gain given by the above matrix. In practical terms, we have designed an amplifier to obtain a specified gain from the average transistor. We have then replaced the average transistor by one of the extreme ones and our interest is to find out what gain we get. We can repeat the process with the other extreme transistor and hence define the upper and lower limits of the gain of the batch for the particular average gain we designed for.

In Fig. 4.6 the gains calculated as indicated above are referred to as 'Calculated Gain'.

4.5.2 Predicted Limits of Gain

The limits of gain can be predicted from (2.44), (2.45) and (2.48), (2.49).

To make use of these formulae, we have to calculate the co-ordinates of the extreme transistors in the IGS. Referring to Fig. 2.9, the point of operation of the extreme transistor will be at j. Since we know the value of the natural average gain G_i, and $\lambda_{R_j} = \lambda_{R_i}$ and $\lambda_{I_j} = \lambda_{R_i}$, from (2.3), we can calculate the value of 1/U which is:

$$\frac{1}{U_i} = \frac{\lambda_I^2 + (\lambda_R - 1/G_i)^2}{1/G_i} \qquad (4.9)$$

The value of $\Delta(1/U)_{max}$ is obtained by subtracting $1/U_i$ from $1/U_j$. This value is kept for further use when predicting extreme gain for other average gains. We now have values for all the terms in (2.44) and (2.45) and can therefore calculate the limits of gain, G_{lo} and G_{up}; these are plotted in Fig. 4.6.

It is fairly clear how to deal with (2.48) and (2.49) which are concerned with port-padding. The results of the prediction from the above are shown in Fig. 4.7.

4.6 POTENTIALLY UNSTABLE TRANSISTORS

A batch of potentially unstable transistors will have their points of operation outside the IGS. In this region, there are no constant gain surfaces and therefore the definition of $\Delta\lambda_R$, $\Delta\lambda_I$ and $\Delta(1/U)$ break down. A new technique therefore has to be developed to deal with this case.

4.6.1 Lossless Embedding

Lossless embedding leaves $\triangle(1/U)$ unchanged therefore we can apply an arbitrary lossless embedding to the batch to make them inherently stable. The values of $\triangle(1/U)$ for both upper and lower limits of gain can then be calculated. All the other quantities in (2.44) and (2.45) can be calculated and hence the limits of gain evaluated.

Fig. 4.8 shows the points of operation of the batch of 19 transistors, used in the previous experiment, in the common base connection. It must be noted that the transistors are unstable. The arbitrary embedding applied to them is such as to make the average transistor have a value of λ_R equal to 0.002. The values of $\triangle(1/U)$ are then calculated and stored for later use.

Fig. 4.9 shows the calculated and predicted values of gain against average gain for a batch of potentially unstable transistors using lossless embedding.

4.6.2 Port-Padding

Port-padding leaves $\triangle\lambda_R$ unchanged and therefore we need to apply an arbitrary pad to be able to calculate the values of $\triangle\lambda_R$ for both upper and lower limits of gain. However, for optimum operation, it is necessary to reduce the value of λ_I of the average transistor to zero. This cannot be done using port-padding and therefore we have to apply lossless embedding for this purpose. An arbitrary

port-pad is then used to make the average gain equal to 100. Values of $\triangle\lambda_R$ for both upper and lower cases are calculated. The other quantities in (2.48) and (2.49) can then be calculated and hence the upper and lower limits of gain evaluted.

Fig. 4.10 shows the calculated and predicted values of gain against average gain for the batch of potentially unstable transistors using port-padding.

4.6.3 Discussion of Results

From Fig. 4.9 it can be seen that the predicted values of gain over-estimate the lower limit and under-estimate the upper limit of the gain. The explanation is that the transistors used in this case (the 19 transistors in common base) show a large spread in the direction of λ_I. This can be seen from Fig. 4.8. The calculated gain takes into account the spread in λ_I while the formulae for predicting the limits of gain assume that the change in gain due to $\triangle\lambda_I$ is negligible.

Comparing Fig. 4.9 to Fig. 4.10, it can be seen that lossless embedding produces a smaller gain spread than port-padding for the batch of transistors used in the experiment.

4.7 THE PRACTICAL AMPLIFIER

We are concerned with small changes in gain which occur as a result of changing the environment of the active element. Since these

small changes are of the same order as the losses which would normally occur in the circuit, it is necessary to eliminate, as far as possible, to measure where possible and to estimate where no other means exist, the losses which occur in the circuit.

4.7.1 The Variable Impedance Transformer (VIT)

The signal source used in the experiments was an Airmec Signal Generator Type 201 with an output impedance of 75 ohms resistive. It is evident that since there is spread in the parameters of the transistors and the embedding changes for various tests, we have to find a simple method of matching the signal source to a varying input impedance of the amplifiers.

One of the simplest ways of realizing this is to use the 'reactance transformer' principle. This is illustrated in Fig. 4.11, and requires no further explanation. One snag arises however, and that is R_{out} must be greater than R_s. To overcome this, the circuit in Fig. 4.12 was designed. The transformer steps down the source impedance such that R_s' is less than the minimum required R_{out}. Again Fig. 4.12 is self-explanatory except for the presence of L_{st} and C_{st}. The output of the transformer was found to be slightly inductive due to the leakage inductance L'. However, it was of such a small value that to eliminate it, an impractically large value of capacitance would be required and the resulting Q of the series tuned circuit would consequently be small. Tuning out the leakage inductance would therefore be rather difficult. The series inductance L_{st} was therefore introduced

to reduce the value of C_{st} to an acceptable value and hence to increase the Q of the circuit. The tuning of the circuit was then carried out with greater precision and R_s' measured accurately. Variation of R_{out} is obtained by changing the values of C_o' and C_x. Two variable capacitors were calibrated and used in place of C_o' and C_x. A chart of R_{out} against scale reading was then plotted as shown in Fig. 4.13. R_{out} was then measured for various settings of the scale readings and the results are also plotted in Fig. 4.13. The circuit of the VIT is shown in Fig. 4.14.

4.7.2 Losses in the Variable Impedance Transformer

The presence of the inductors L_{st} and L_o and the transformer introduces losses in the circuit. These losses are calculated by measuring the voltage at the input and output of the VIT when it has been correctly terminated at the output. Fig. 4.15 shows a plot of losses in decibels against R_{out}.

Fig. 4.15 shows that as R_{out} increases, the losses go up rapidly. Since the losses in the transformer and the inductors cannot be expected to rise as sharply as shown, it can be concluded that the increase in loss is partly due to a slight mismatch between the source resistance R_s and the impedance it 'sees' as R_{out} increases.

4.7.3 Measured Limits of Gain

The values of the embedding elements obtained from the computer

program were used to construct amplifiers using both lossless and lossy techniques to obtain the required gain-sensitivity condition. The gain of the amplifiers with the minimum and maximum gain transistors as the active element was measured and the results plotted in Figs. 4.6 and 4.7. Fig. 4.16 shows a partially schematic diagram of the arrangement of the circuit.

4.7.4 Determination of Predominant Spread

In section (2.6.3), a criterion was suggested for the determination of the predominant spread. It must be recalled that $\Delta\lambda_I$ does not cause a significant change in gain for reasons given in section (2.4.3) when λ_I of the average device is reduced to zero.

From the 19, transistors used in this work,

$$\sum\Delta(1/U) = 0.03856$$

and

$$\sum\Delta\lambda_R = 0.02356$$

Thus $\sum\Delta(1/U) \not> 2\sum\Delta\lambda_R$ and therefore the spread in this particular batch of transistors is predominantly due to $\Delta\lambda_R$. Therefore, lossless embedding should give better results than port-padding.

4.7.5 Comparison of Lossless Embedding and Port-Padding

Comparing the spread in gain after the application of lossless embedding to that resulting from port-padding for the same average

gain, (see Figs. 4.6 and 4.7) it can be seen that lossless embedding leads to a much greater reduction in gain spread than port-padding. Closer inspection of Fig. 4.7 reveals that in fact port-padding results in a greater spread in gain than before. Note that lossless embedding was used to reduce the value of λ_I for the average transistor to zero before port-padding was applied. Thus, without this extra 'help', port-padding would have given much worse results. Therefore for the particular set of transistors used in the experiment, port-padding would certainly be the less attractive of the two methods.

4.7.6 Discussion of Predicted and Calculated Gain

Fig. 4.6 shows that there is a discrepancy between predicted and calculated gain, and further that the formula for predicting the upper gain limit overestimates and that for the lower limit underestimates the gain. This is because in (2.31) we used the rate of change of gain with respect to λ_R and $1/U$ at the points k and i respectively, which are on the natural average gain surface. Since the constant gain surfaces on the 'outside' of the natural average gain surface are much closer than those on the 'inside', equation (2.31) will tend to underestimate the total change in inverse gain between the natural average gain surface and a point on the 'outside' of it. Similarly it will tend to overestimate the total change in inverse gain between the natural average gain surface and a point on the 'inside' of it. Hence, the formula for predicting the limits of gain based on

equation (2.31) will tend to overestimate the upper limit and underestimate the lower limit.

From Fig. 4.7, it can be seen that the predicted and calculated values of gain agree more closely in the case of port-padding than for lossless embedding, further that both the upper and lower limits are underestimated. The close agreement can be explained in terms of the relatively lower sensitivity of gain to movement in a direction parallel to the 1/U axis as compared to movement parallel to the λ_R axis. This means that errors arising from the approximation of (2.31) will be small. The fact that the predicted limit of gain line for the upper case is below the calculated gain line might be explained by the fact that when λ_I of the average transistor is reduced to zero, the upper gain transistor may not necessarily have its λ_I equal to zero. In fact, the λ_I of the transistor with the highest gain is not equal to zero after lossless embedding has been applied for this purpose. Fig. 4.laillustrates this argument (transistor 11). The same is true of the transistor with the lowest gain (transistor 15).

4.8 IDEAL SPREADS

4.8.1 Synthesis of Ideal Spread Transistors

To study the advantages and disadvantages of lossless embedding vis-a-vis port-padding to achieve a given gain-sensitivity condition, it is necessary to have say, the Y-parameters of three transistors which exhibit ideal spread (section 2.6.1). Note that when discussing

ideal spread, λ_I is always made equal to zero.

Z-resistive embedding is known to decrease the value of 1/U* and Y output port-padding to increase the value of 1/U. Thus given the parameters of a transistor we can change the value of 1/U to a predetermined value. We cannot guarantee that at this point, the value of λ_I will be equal to zero. So we can apply lossless embedding (keeping 1/U constant) such that the transistor will give the predetermined value of gain, for $\lambda_I = 0$. The parameters of the transistor together with the applied embedding are recorded. In Fig. 4.17, such a transistor will have its point of operation at say A_2. Further lossless embedding can be applied to transistor A_2 to reduce the gain to another predetermined value. The point of operation of the second transistor will then be at B_2. Y-mode output port-padding can then be applied to transistor A_2 to give the parameters of a third transistor whose point of operation is at C_2 and whose gain is equal to that of B_2. By repeating the above method, two other groups of transistors were synthesised such that the gain for the A's were equal and those of the B's and C's were also equal. For the particular case dealt with here, the gain of the A's was chosen to be 100 (20 dbs) and that of the B's and C's 80 (19.03 dbs).

4.8.2 Predicting the Choice of Embedding for Ideal Spread

In section (2.6.2), conditions governing the choice of the type of embedding were derived. A numerical example will now be given. From

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* Refer to Chapter 3.

the coordinates of the points B', B", C" for the three groups of transistors at P, Q, and R in Fig. 4.18 the gain of the transistors were calculated for the points. Table 2 summarizes the results.

Table 2

Group R (high U - high λ_R)

Type of Spread	Gain	Best Type of Embedding
$\Delta\lambda_R$	a)* $G_{B'} = 73.46$ b)* $G_{B''} = 73.35$	Lossless ($G_{B'} > G_{B''}$)
$\Delta(1/U)$	a) $G_{C'} = 73.80$ b) $G_{C''} = 72.48$	Port-padding ($G_{C''} < G_{C'}$)

Group Q (medium U - medium λ_R)

Type of Spread	Gain	Best Type of Embedding
$\Delta\lambda_R$	a) $G_{B'} = 73.45$ b) $G_{B''} = 72.86$	Lossless
$\Delta(1/U)$	a) $G_{C'} = 72.91$ b) $G_{C''} = 73.15$	Port-padding

Group P (low U - low λ_R)

Type of Spread	Gain	Best Type of Embedding
$\Delta\lambda_R$	a) $G_{B'} = 74.24$ b) $G_{B''} = 73.88$	Lossless
$\Delta(1/U)$	a) $G_{C'} = 72.87$ b) $G_{C''} = 75.01$	Port-padding

* a) Lossless Embedding
b) Port-padding

As seen from Table 2, port-padding is, in general, the best way of reducing the spread in gain due to $\Delta(1/U)$ for the same average gain, and lossless embedding for spread in gain arising from $\Delta\lambda_R$.

4.8.3 Embedding the Ideal Spread Transistors

We can now apply lossless embedding and Y output port-padding to each group of transistors in turn and to compare their performance, vis-a-vis the two types of spread (i.e. $\Delta(1/U)$ and $\Delta\lambda_R$).

The computer programme for lossless embedding is used to determine the values of the elements which when applied to say A_2 will give a predetermined gain. The values of these elements are then 'added' to the parameters of B_2 and C_2 and for each, the gain is calculated. The difference in gain between A_2 and B_2 as well as between A_2 and C_2 is calculated for the situation when the embedding has been applied. Fig. 4.19b shows plots of gain spread, ΔG, against the resulting average gain when the appropriate embedding has been applied. The process is repeated for Y output port-padding and the results are plotted in Fig. 4.19b. Figs. 4.19a and 4.19c also shows plots of gain spread against average gain for the two other groups of transistors shown in Fig. 4.17.

4.8.4 Conclusion on Ideal Spreads

It is concluded from Fig. 4.16a, b, and c, that port-padding is the best way of dealing with spread in gain due to $\Delta(1/U)$ but

certainly the least attractive way of reducing the spread in gain when this is due to $\triangle\lambda_R$. Lossless embedding shows slightly better results for gain spreads due to $\triangle(1/U)$ than for gain spreads due to $\triangle\lambda_R$ when the overall value of U is high. For low overall values of U (see Fig. 4.19c), the opposite is true over a large portion of the range of the average gain. The general conclusion is that lossless embedding is far more reliable than resistive port-padding although for the particular case when the spread in gain is predominantly due to $\triangle(1/U)$, port-padding might be a better choice.

The above conclusions are in agreement with the predictions made in section (4.7.2).

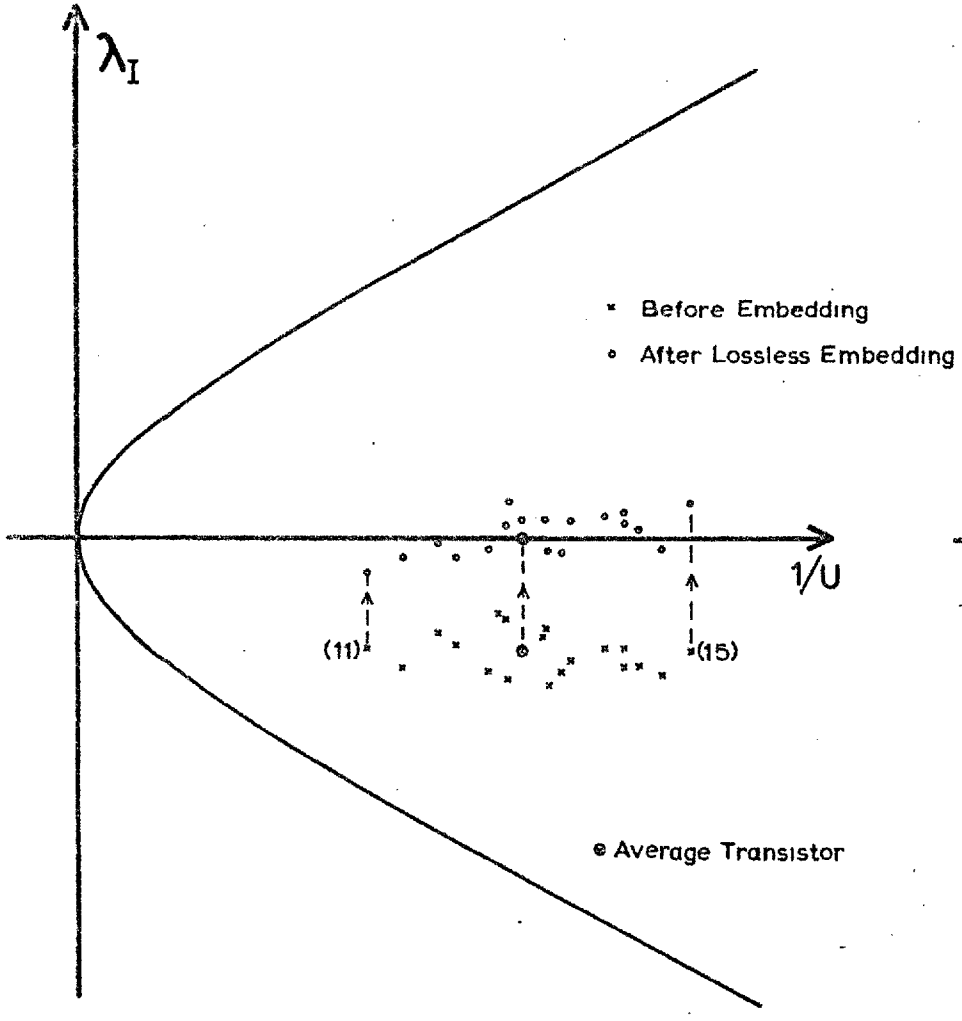

Fig 4.1a Points of Operation of Transistors before and after Lossless Embedding.

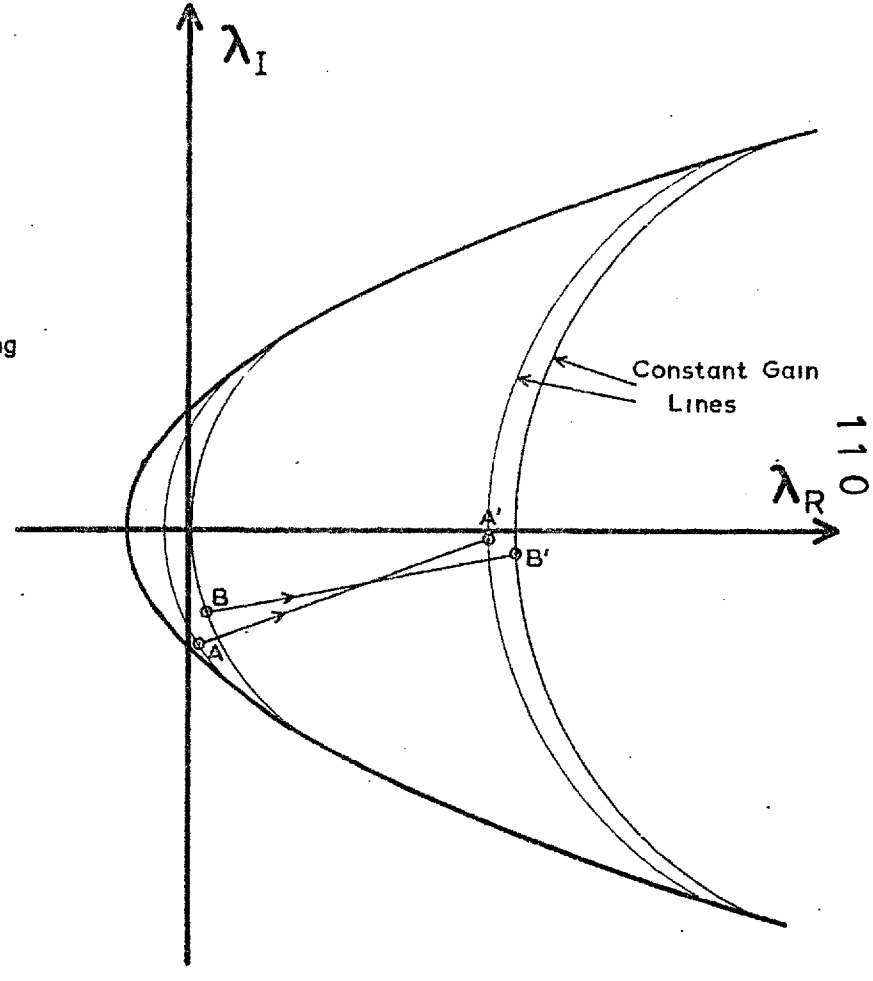

FIg 4.1b 'Cross-over' in Lossless Embedding.

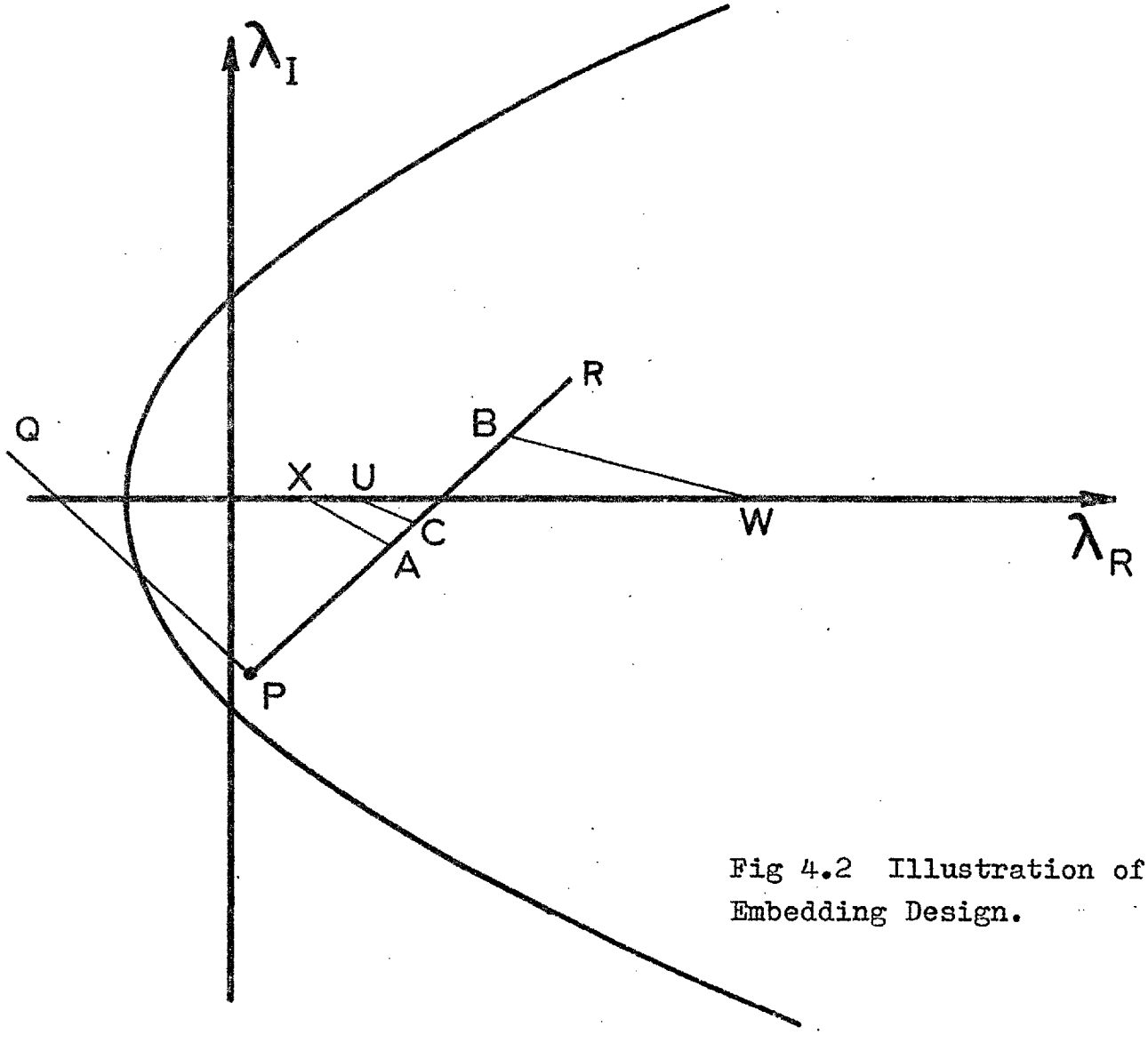

Fig 4.2 Illustration of Iterative Embedding Design.

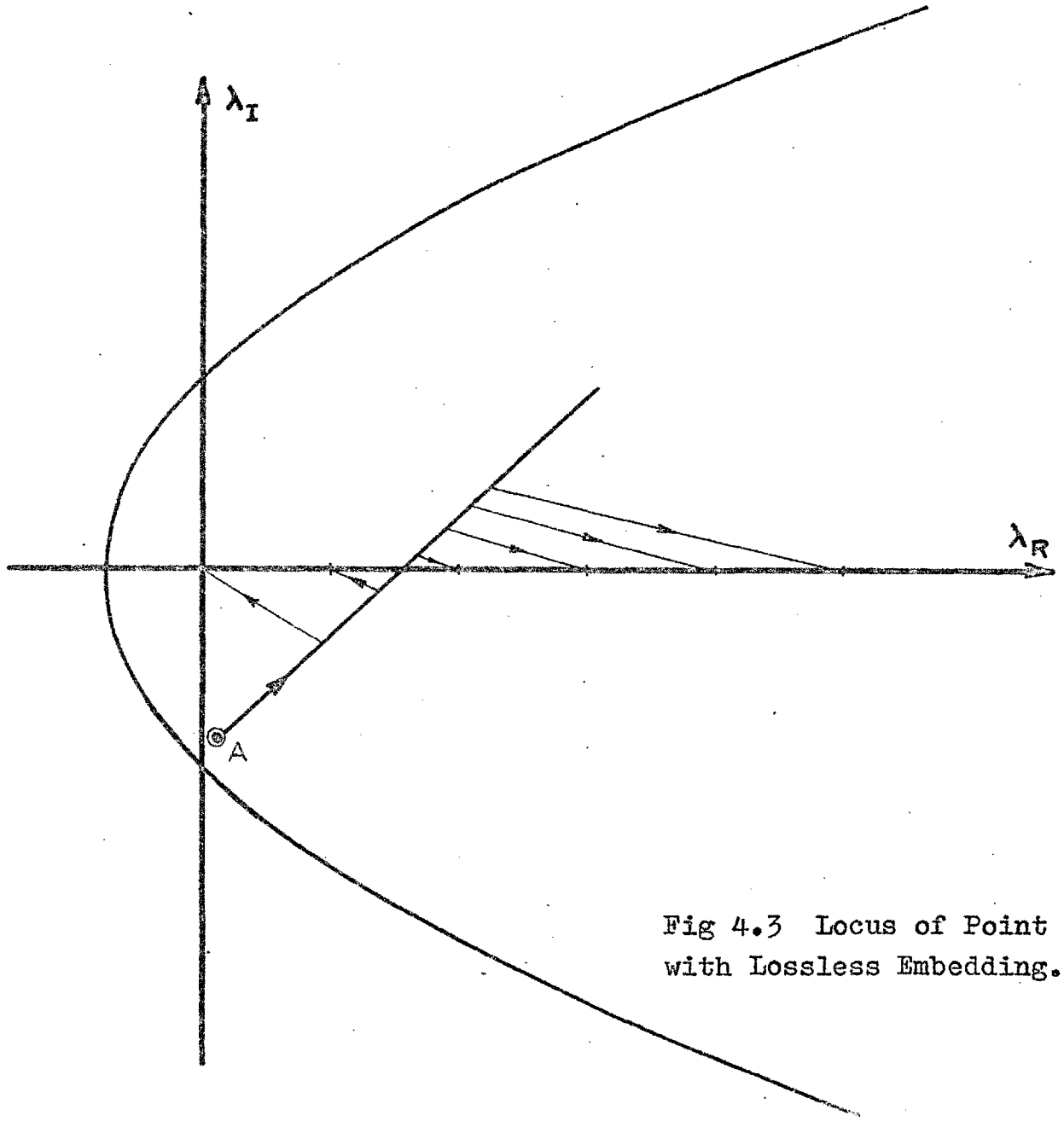

Fig 4.3 Locus of Point of Operation with Lossless Embedding.

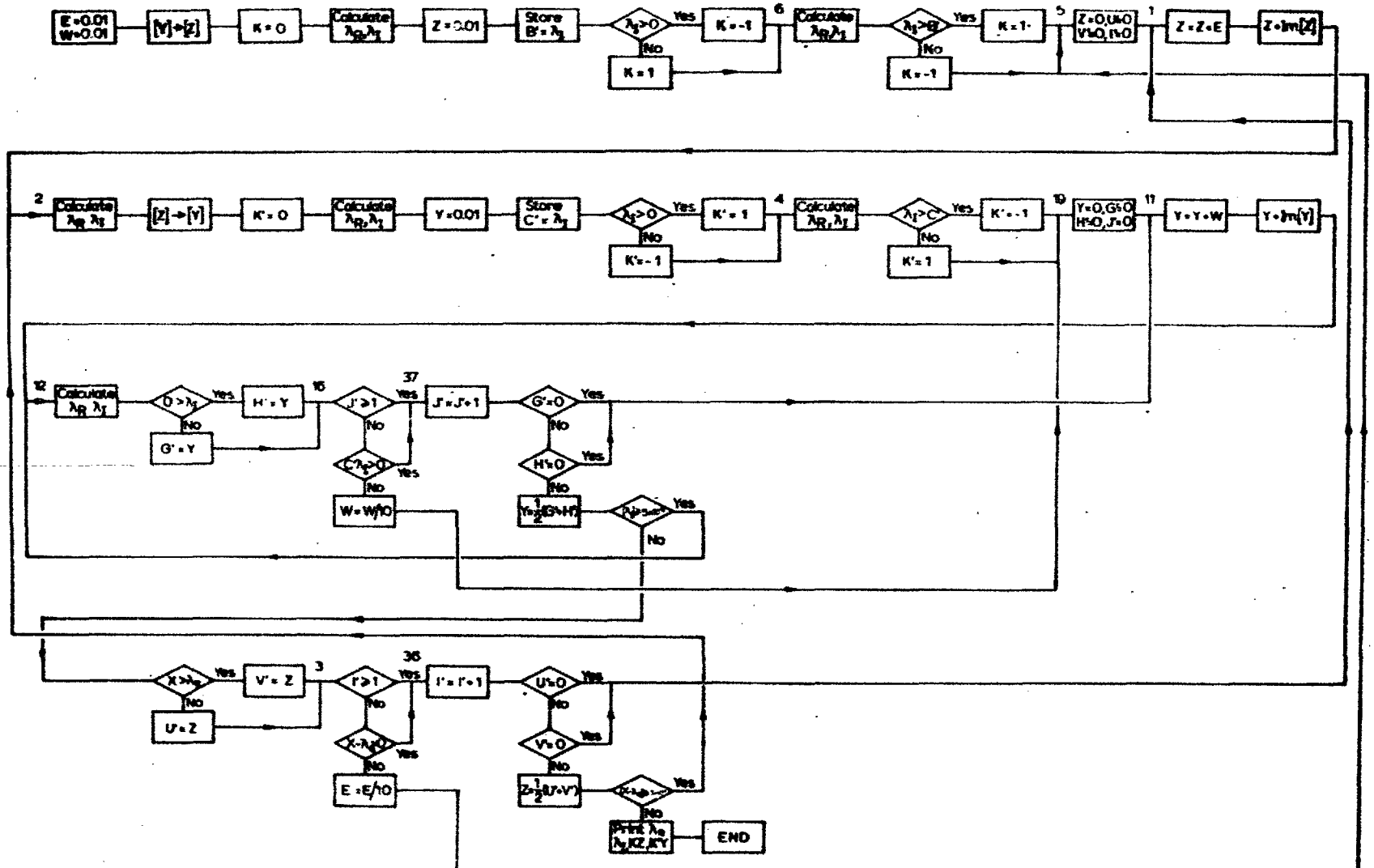

Fig 4.4 Flow diagram for Lossless Embedding Routine.

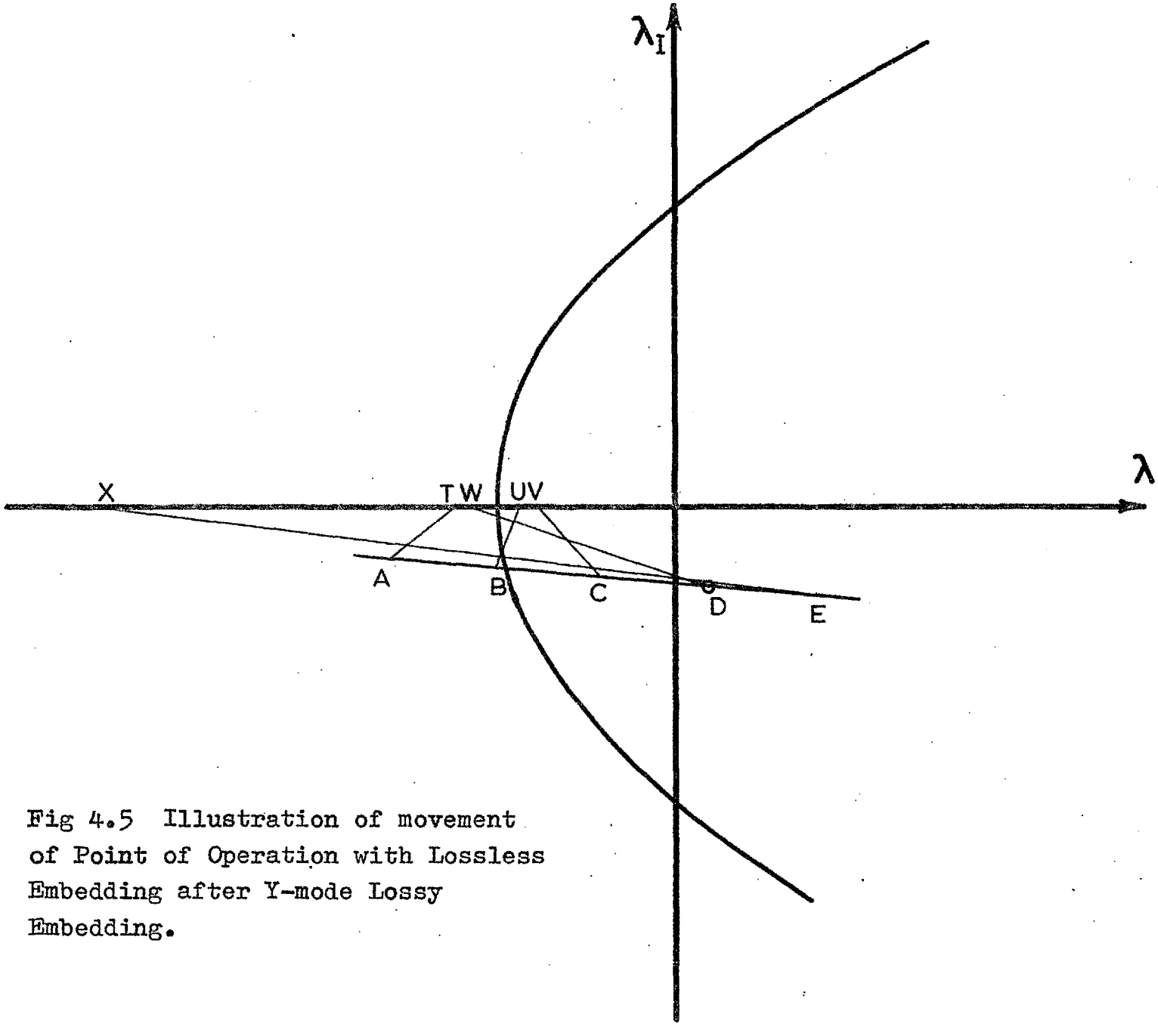

Fig 4.5 Illustration of movement of Point of Operation with Lossless Embedding after Y-mode Lossy Embedding.

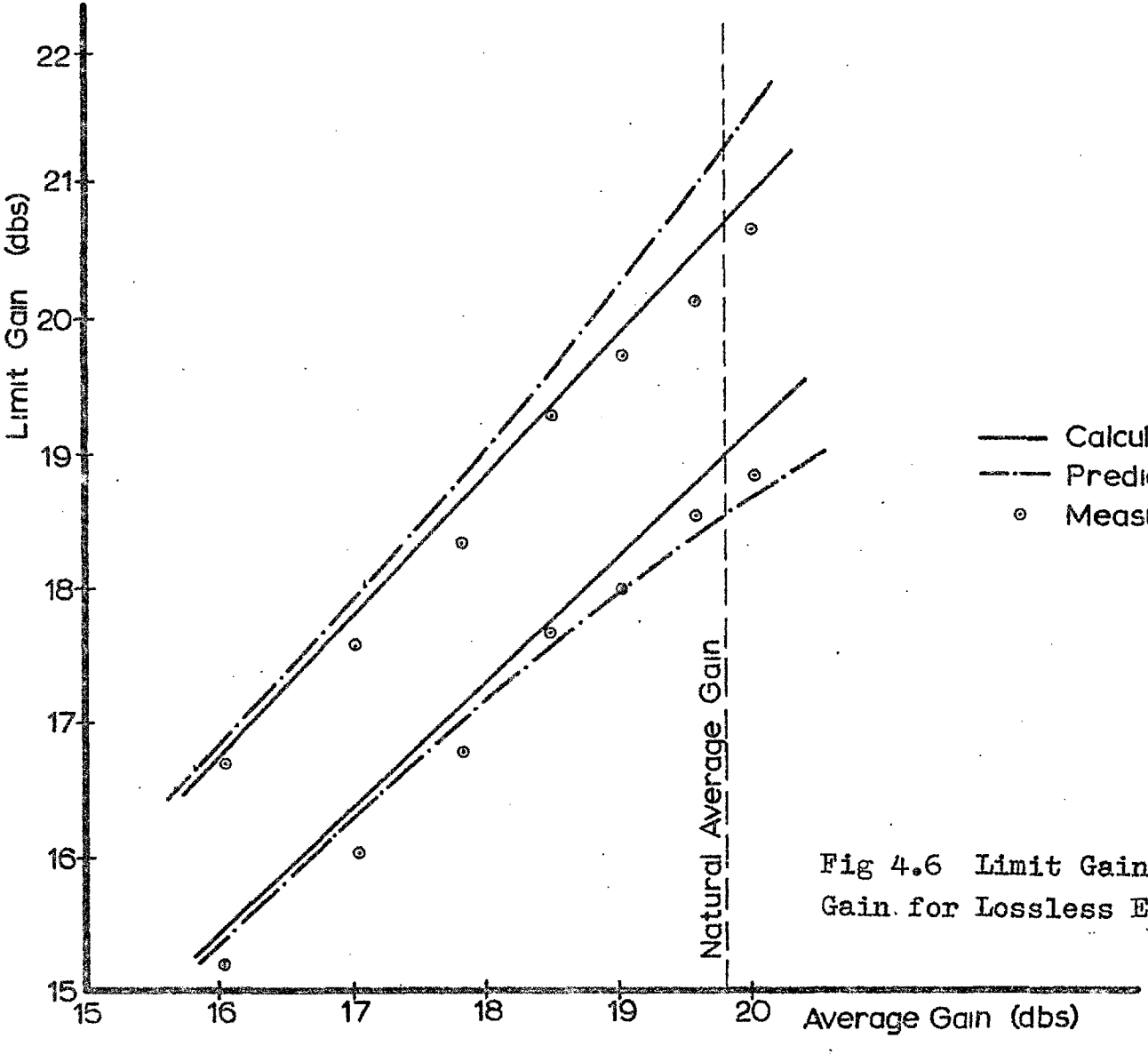

Fig 4.6 Limit Gain Vs. Average Gain for Lossless Embedding.

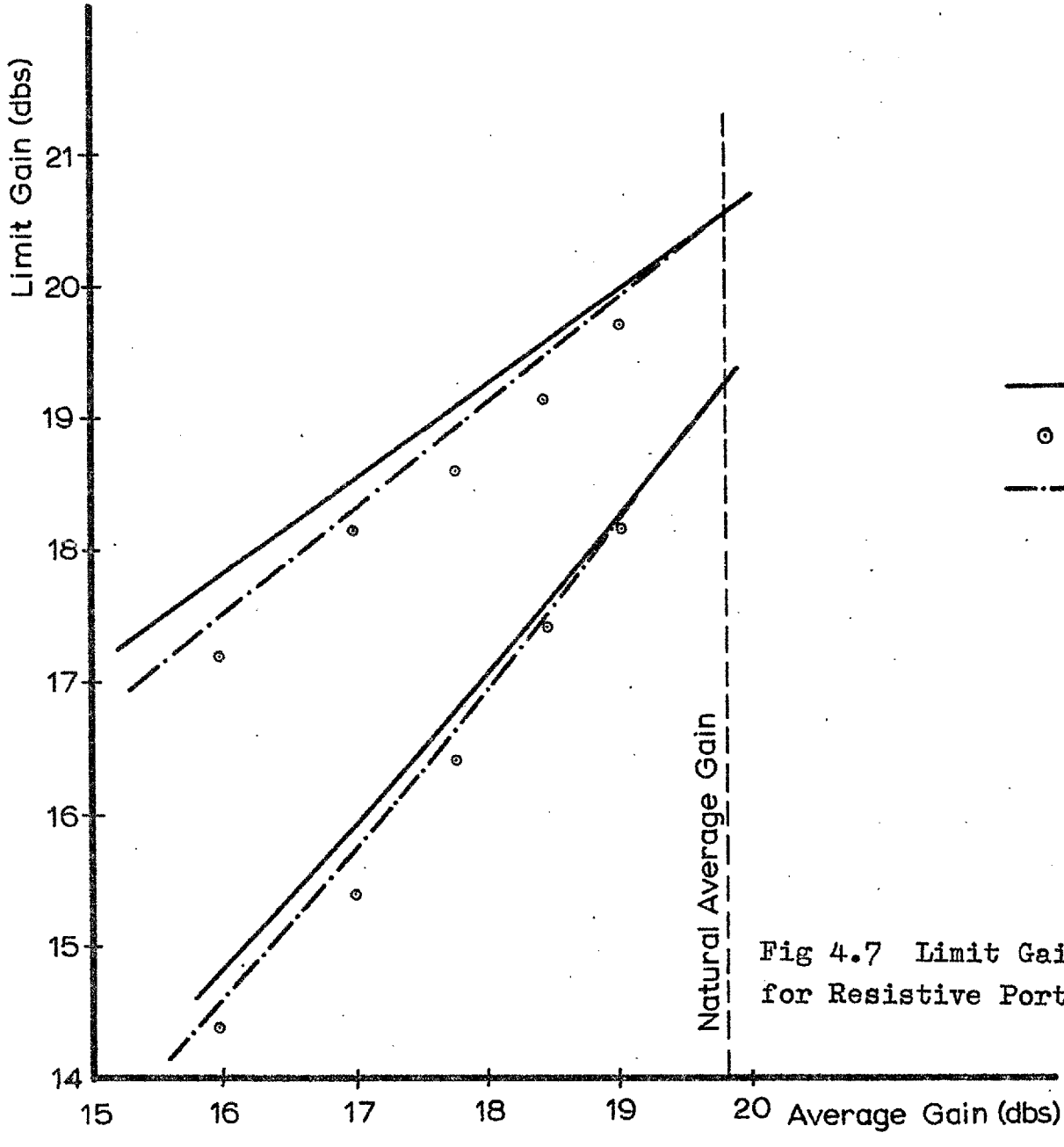

Fig 4.7 Limit Gain Vs. Average Gain for Resistive Port-Padding.

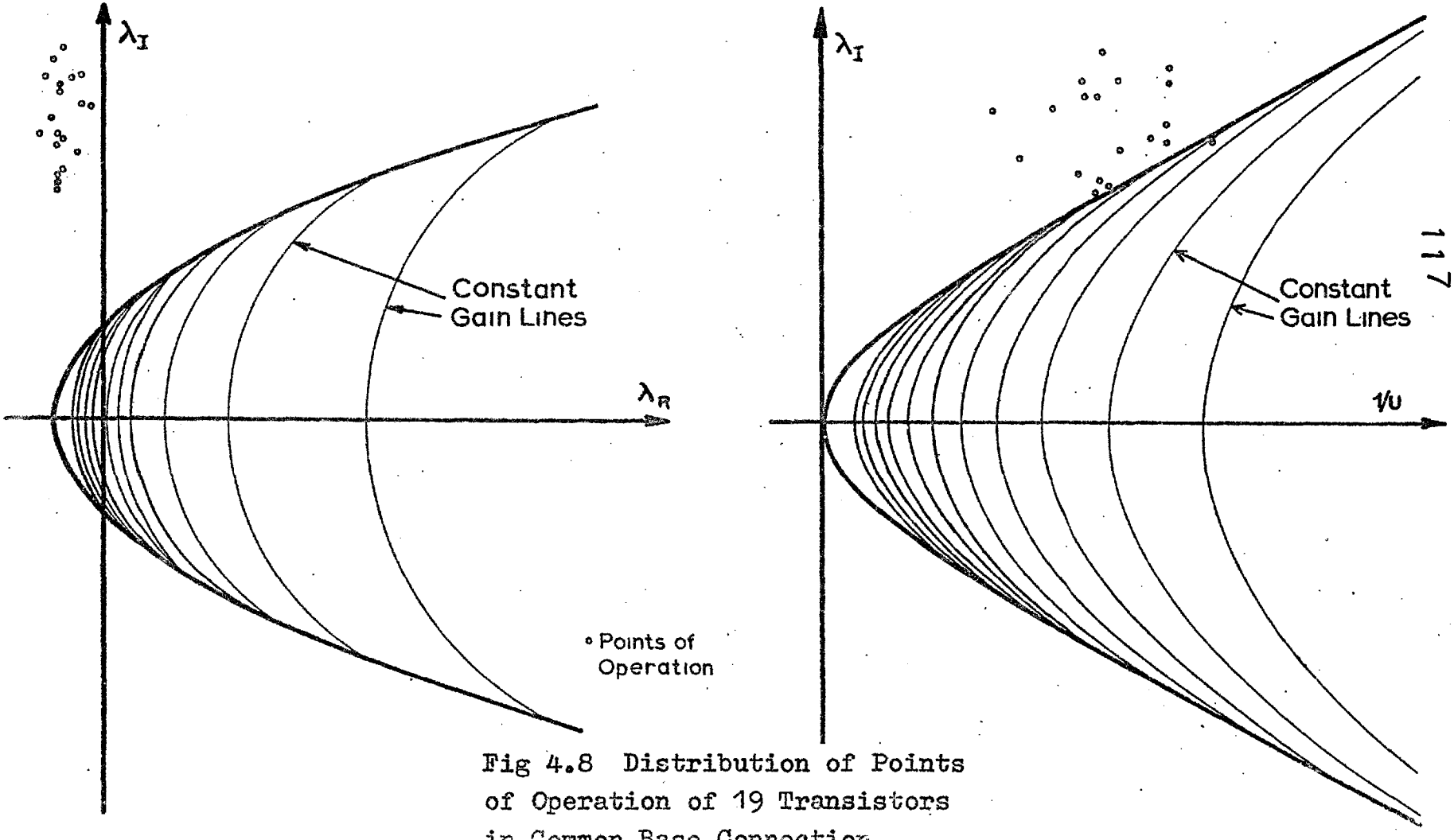

Fig 4.8 Distribution of Points of Operation of 19 Transistors in Common Base Connection. (Potentially Unstable)

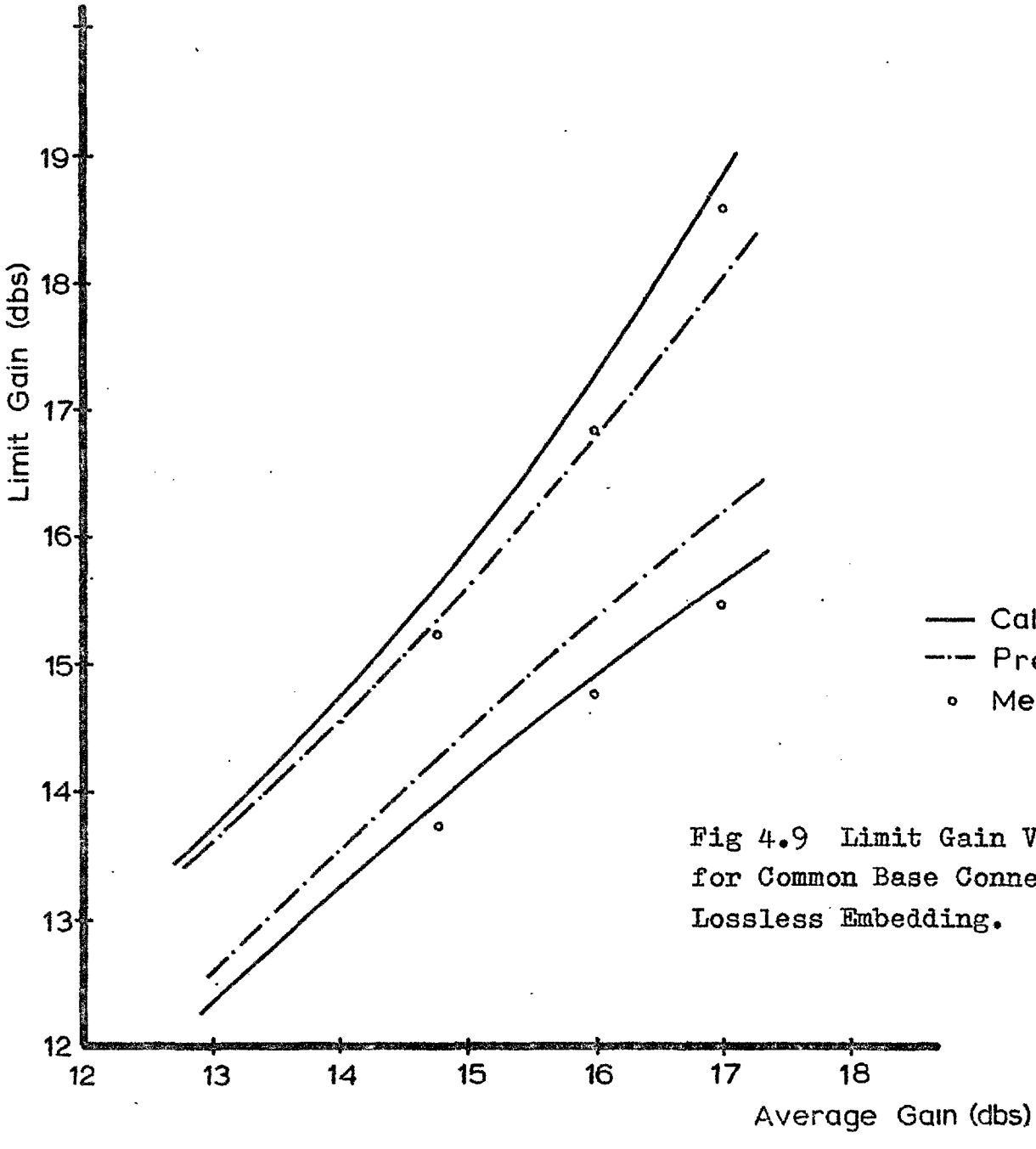

Fig 4.9 Limit Gain Vs Average Gain for Common Base Connection with Lossless Embedding.

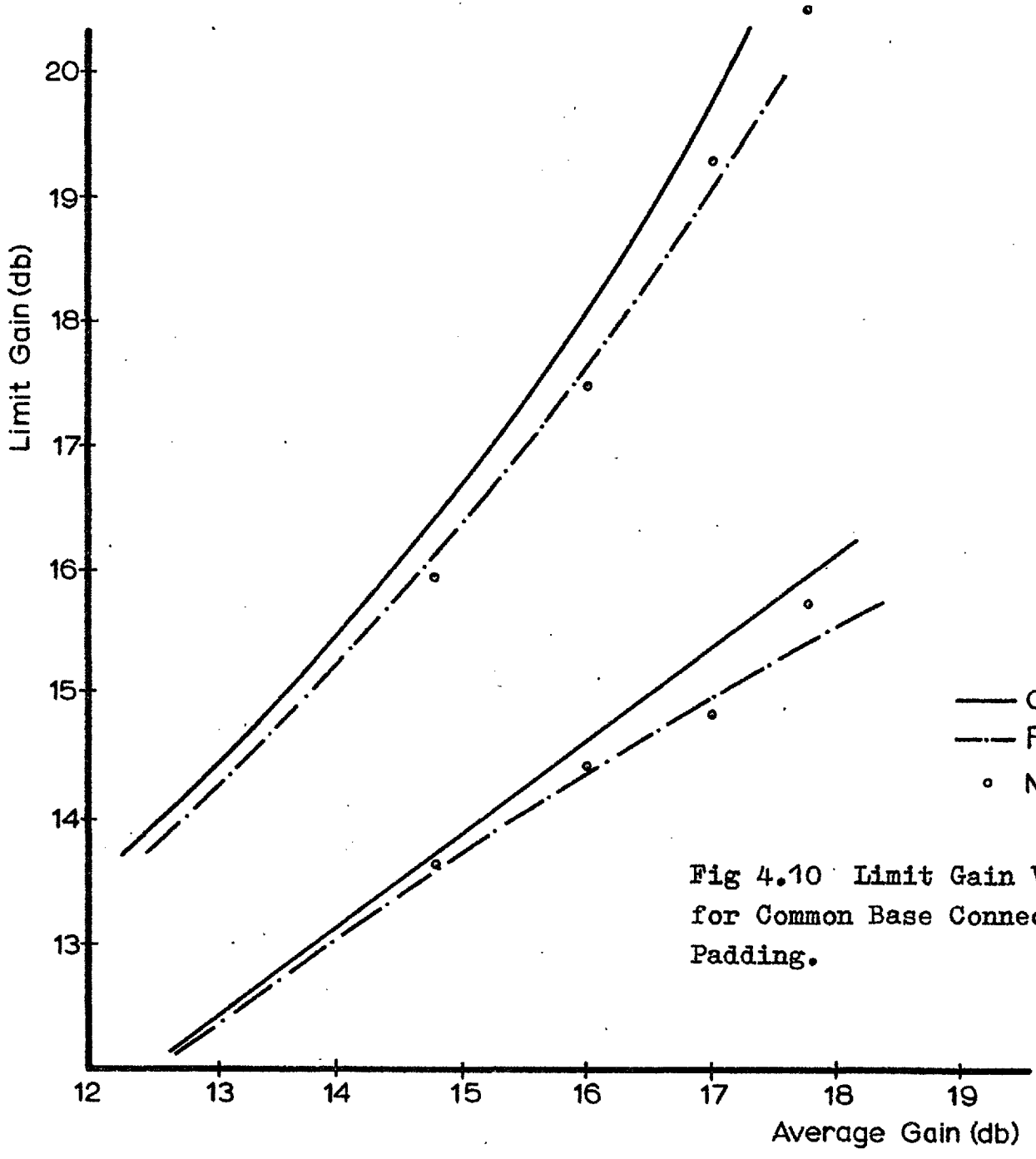

Fig 4.10 Limit Gain Vs Average Gain for Common Base Connection with Port-Padding.

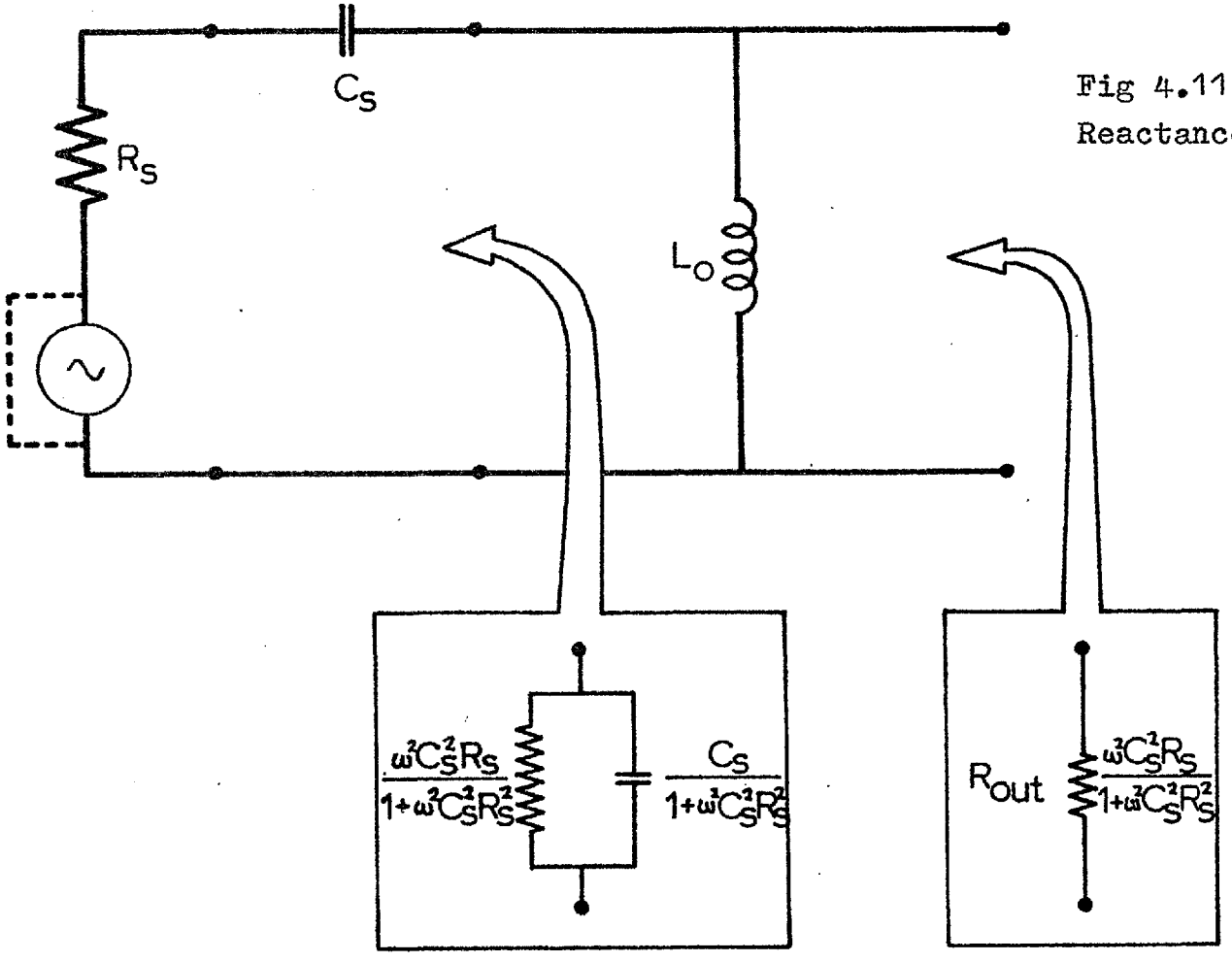

Fig 4.11 The Principle of the Reactance Transformer.

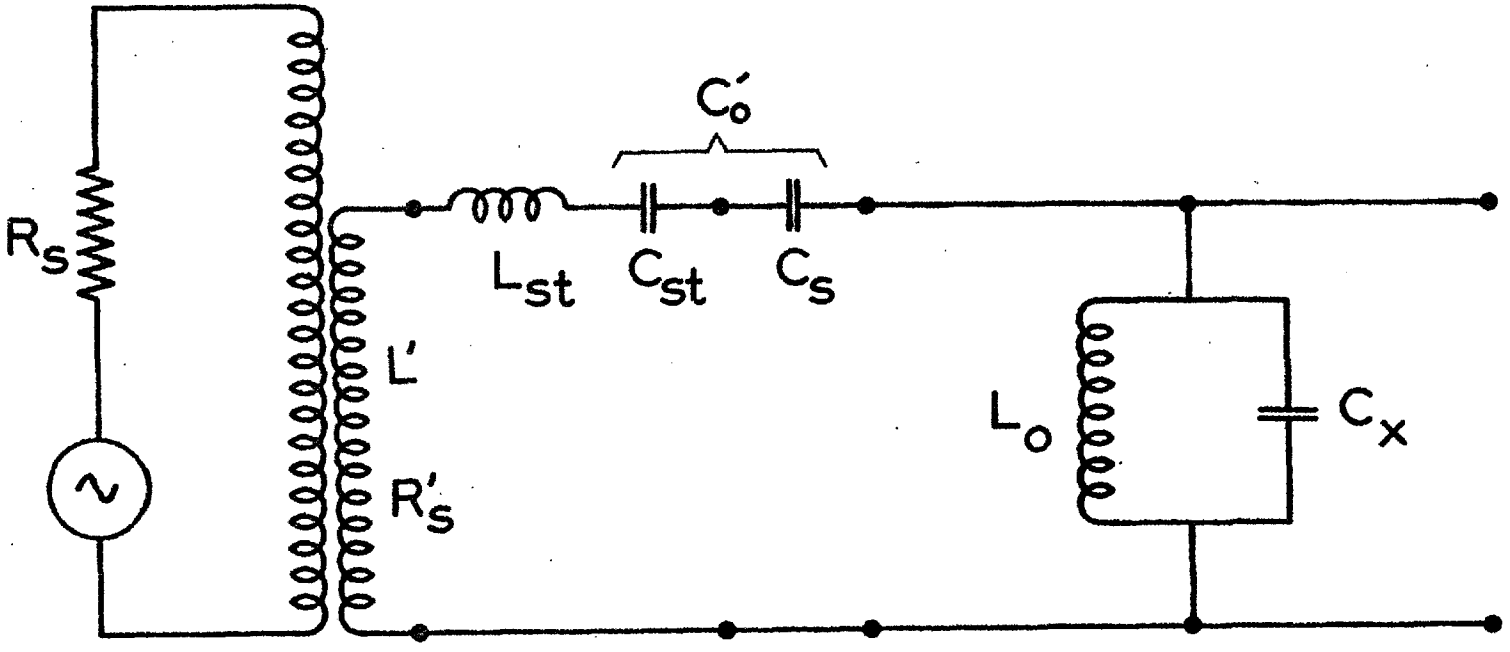

Fig 4.12 Circuit of the Variable Impedance Transformer.

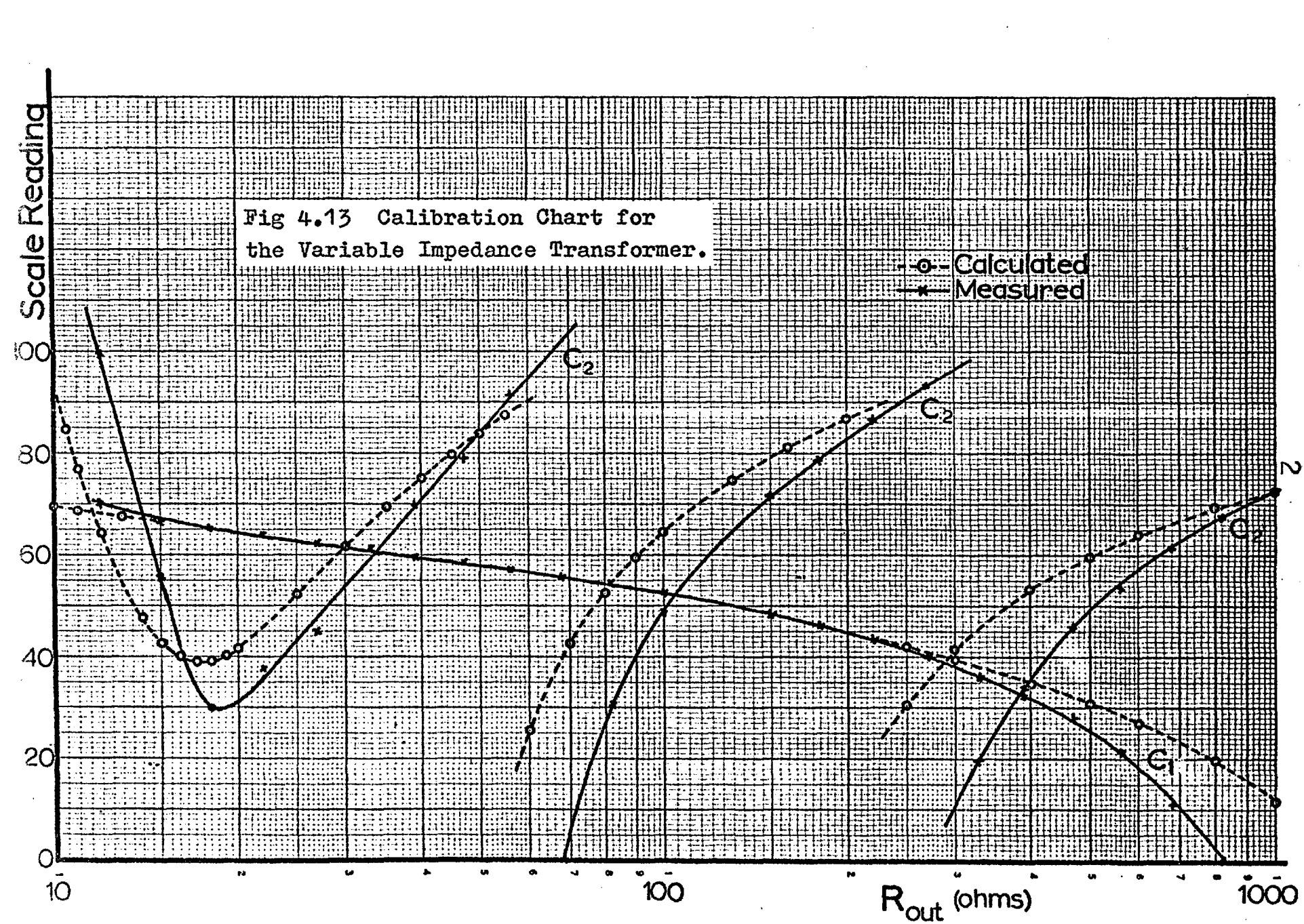

Fig 4.13 Calibration Chart for the Variable Impedance Transformer.

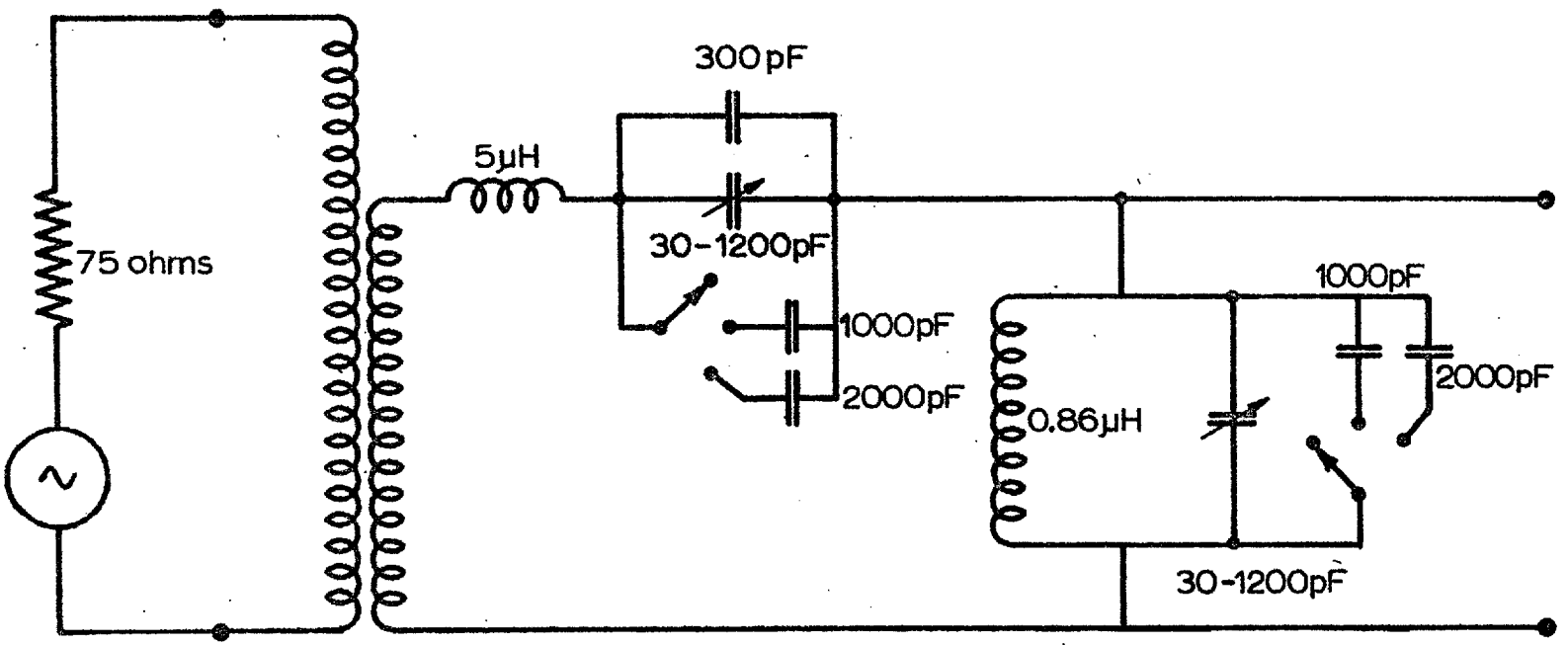

Fig 4.14 Complete Circuit of the Variable Impedance Transformer.

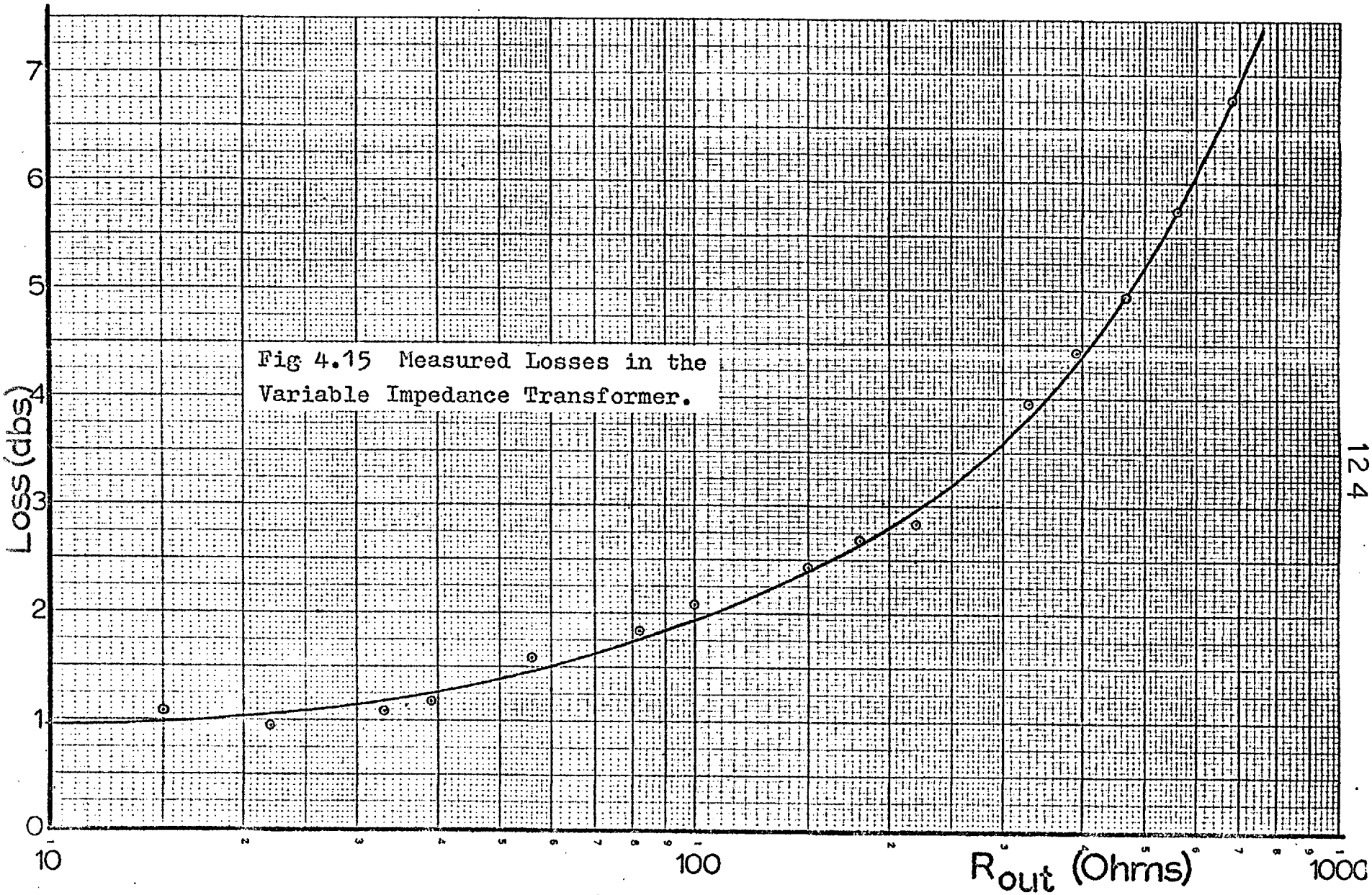

Fig 4.15 Measured Losses in the Variable Impedance Transformer.

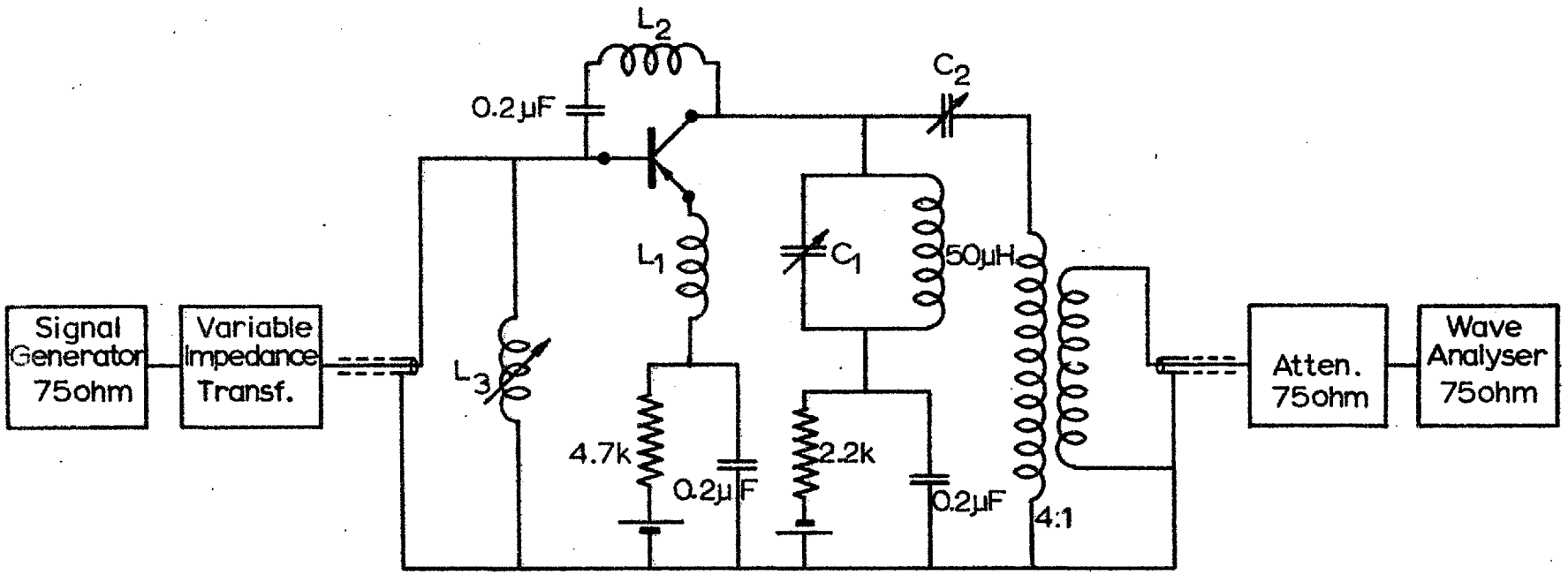

Fig 4.16 Partially Schematic Diagram for measuring Gain.

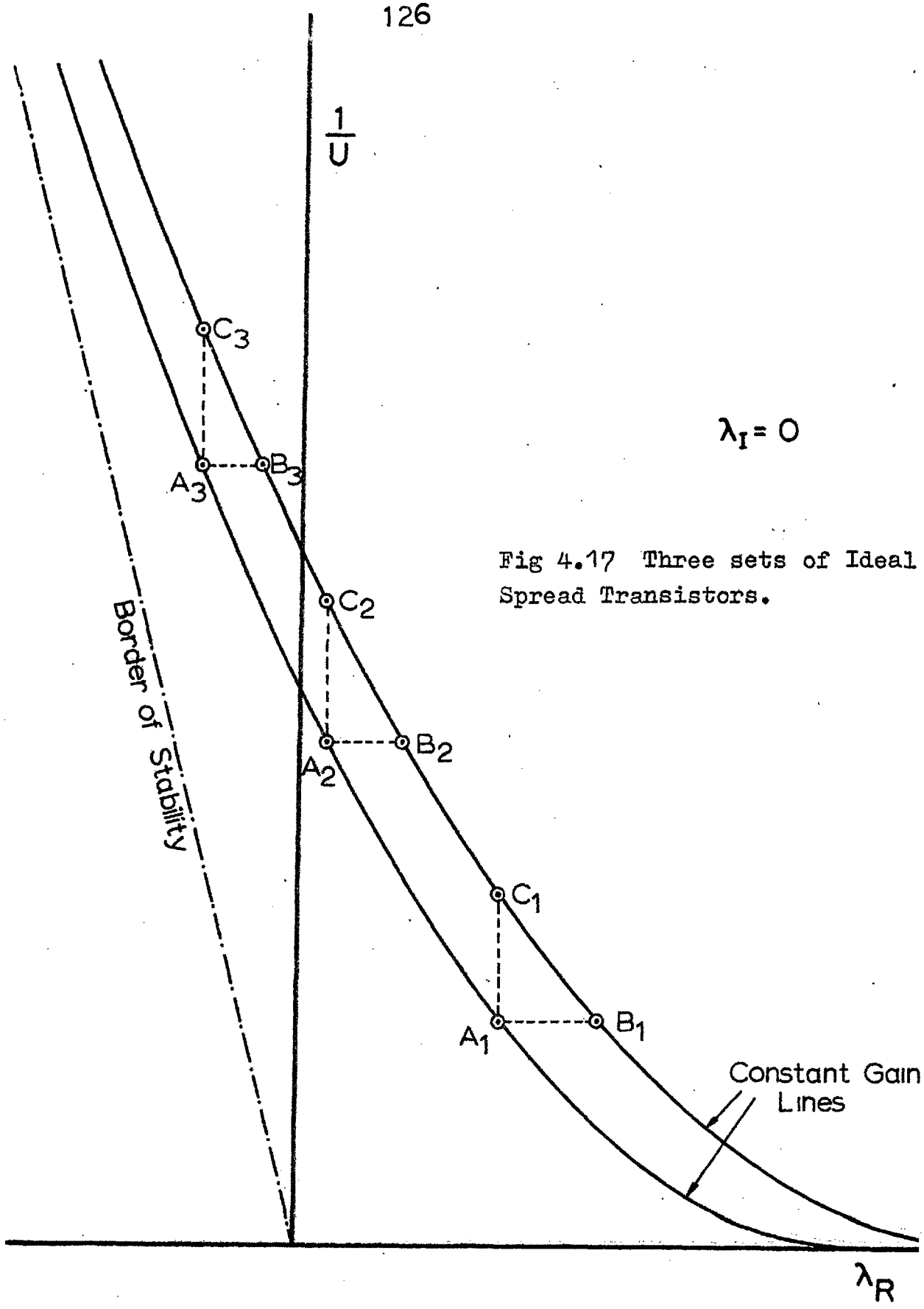

Fig 4.17 Three sets of Ideal Spread Transistors.

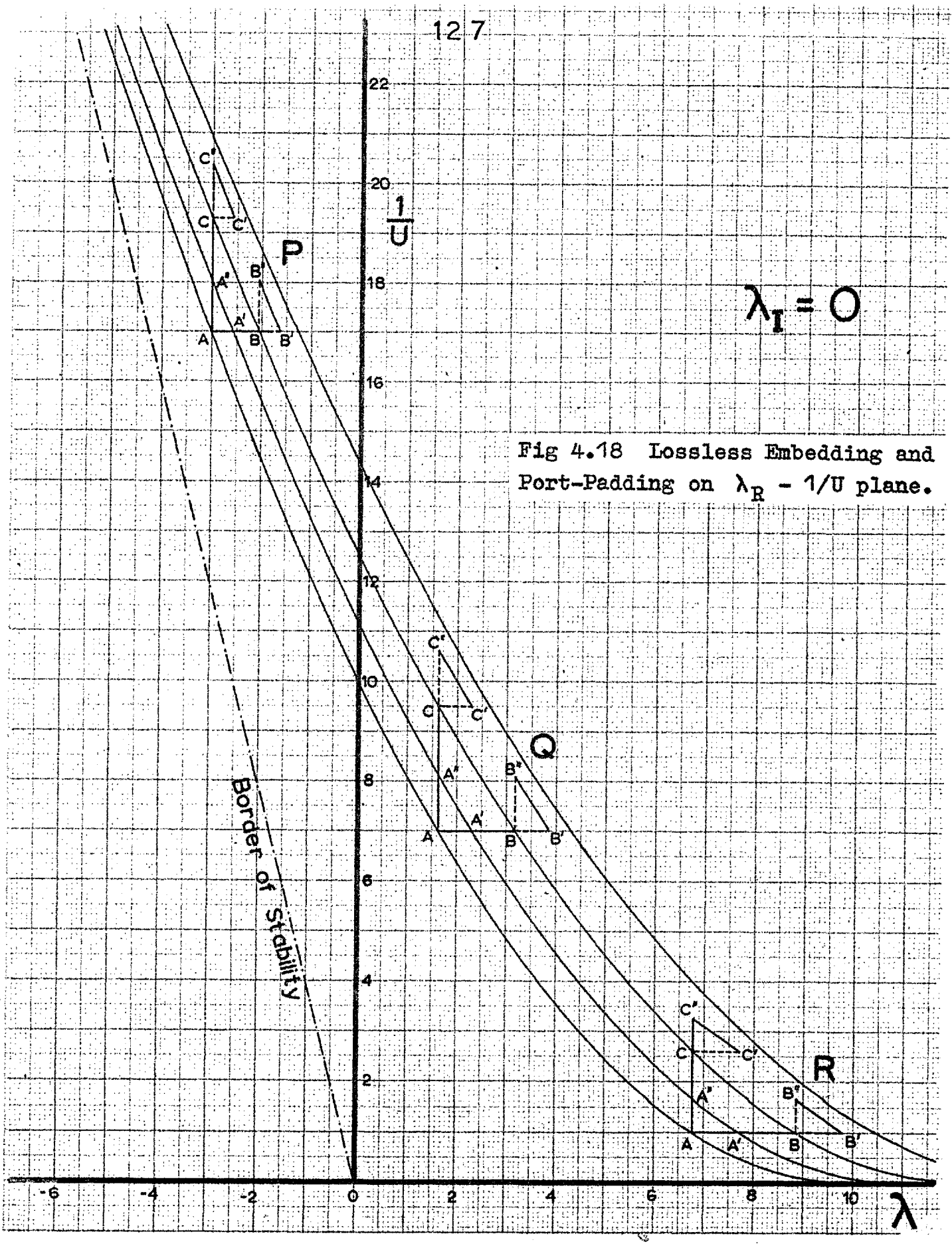

Fig 4.18 Lossless Embedding and Port-Padding on λ_R - 1/U plane.

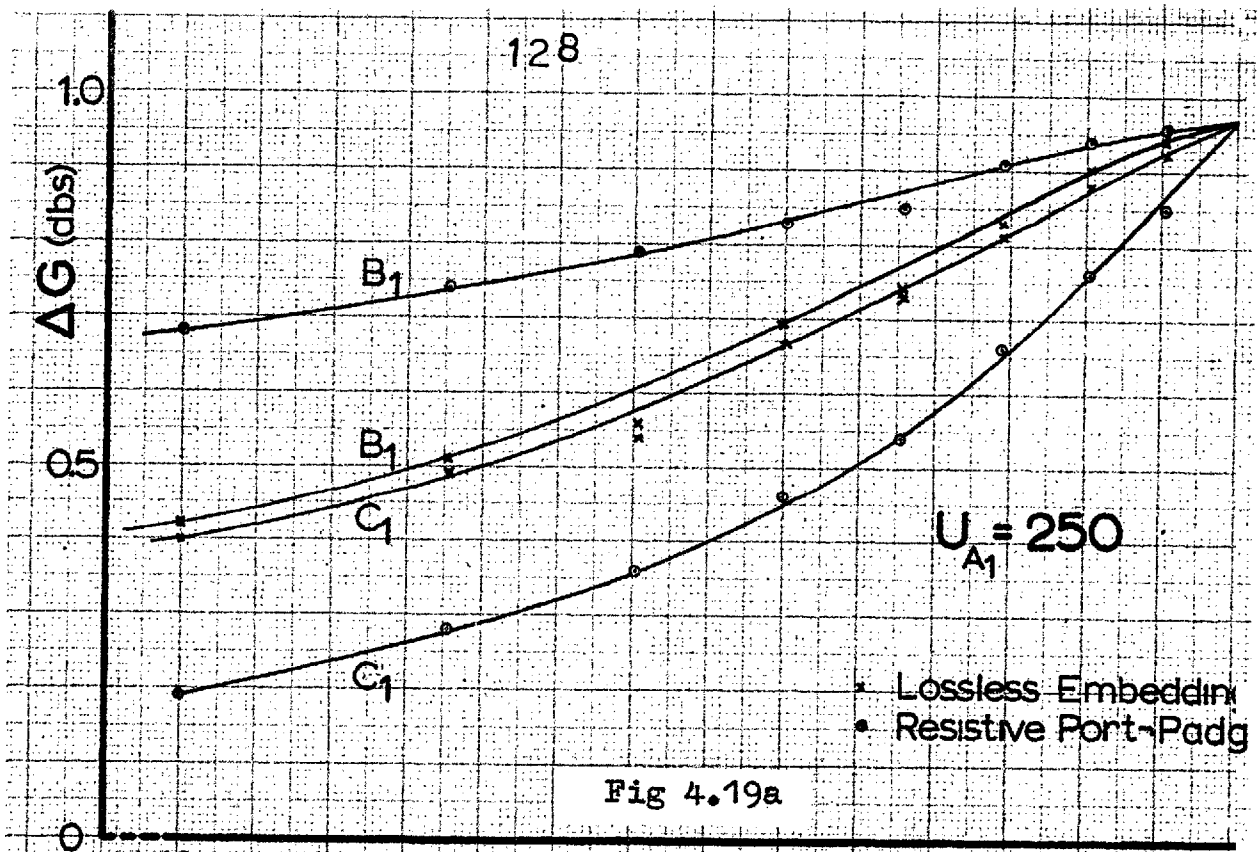

Fig 4.19a

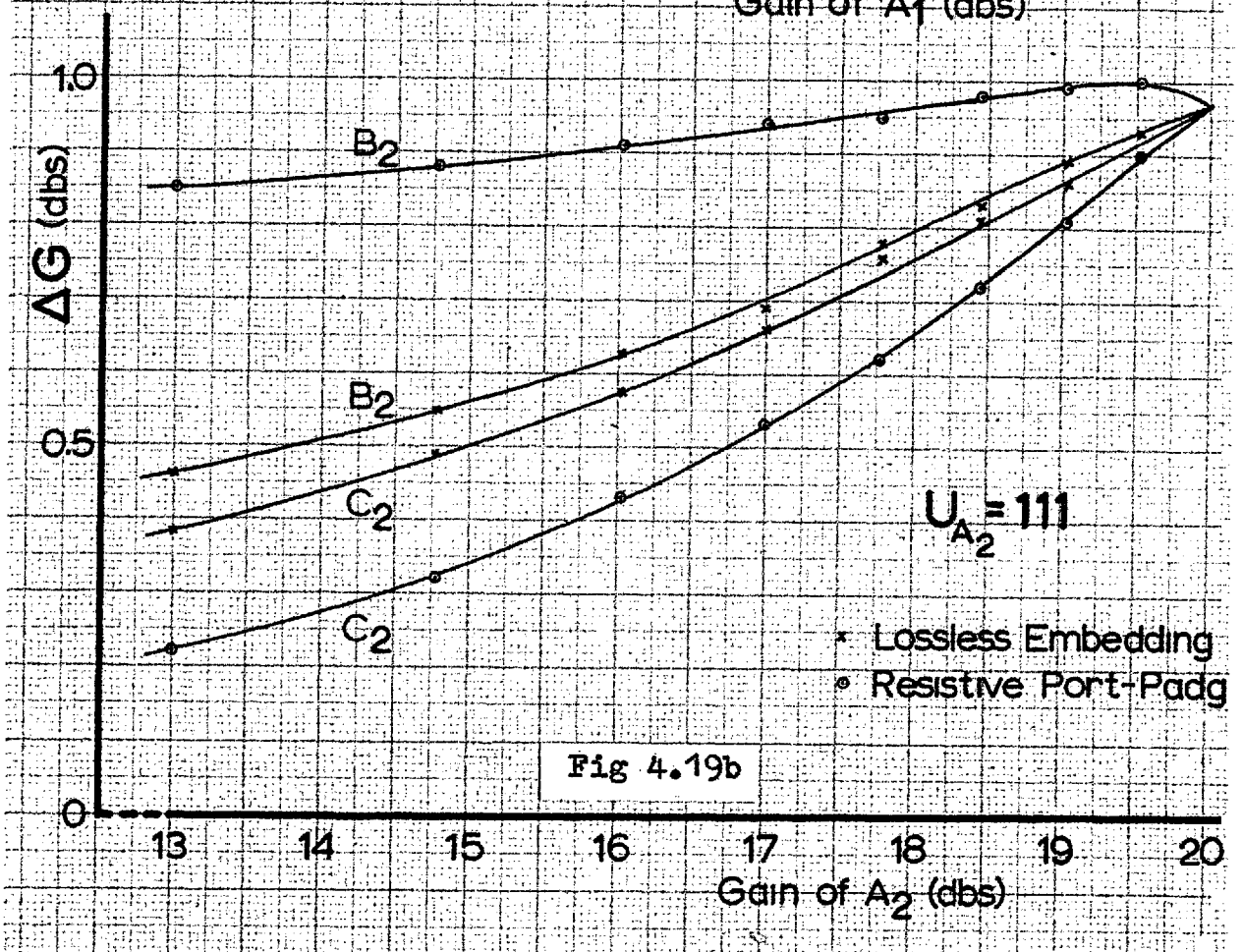

Fig 4.19b

Fig 4.19 Gain Spread Vs Average Gain for Ideal Spread Transistors.

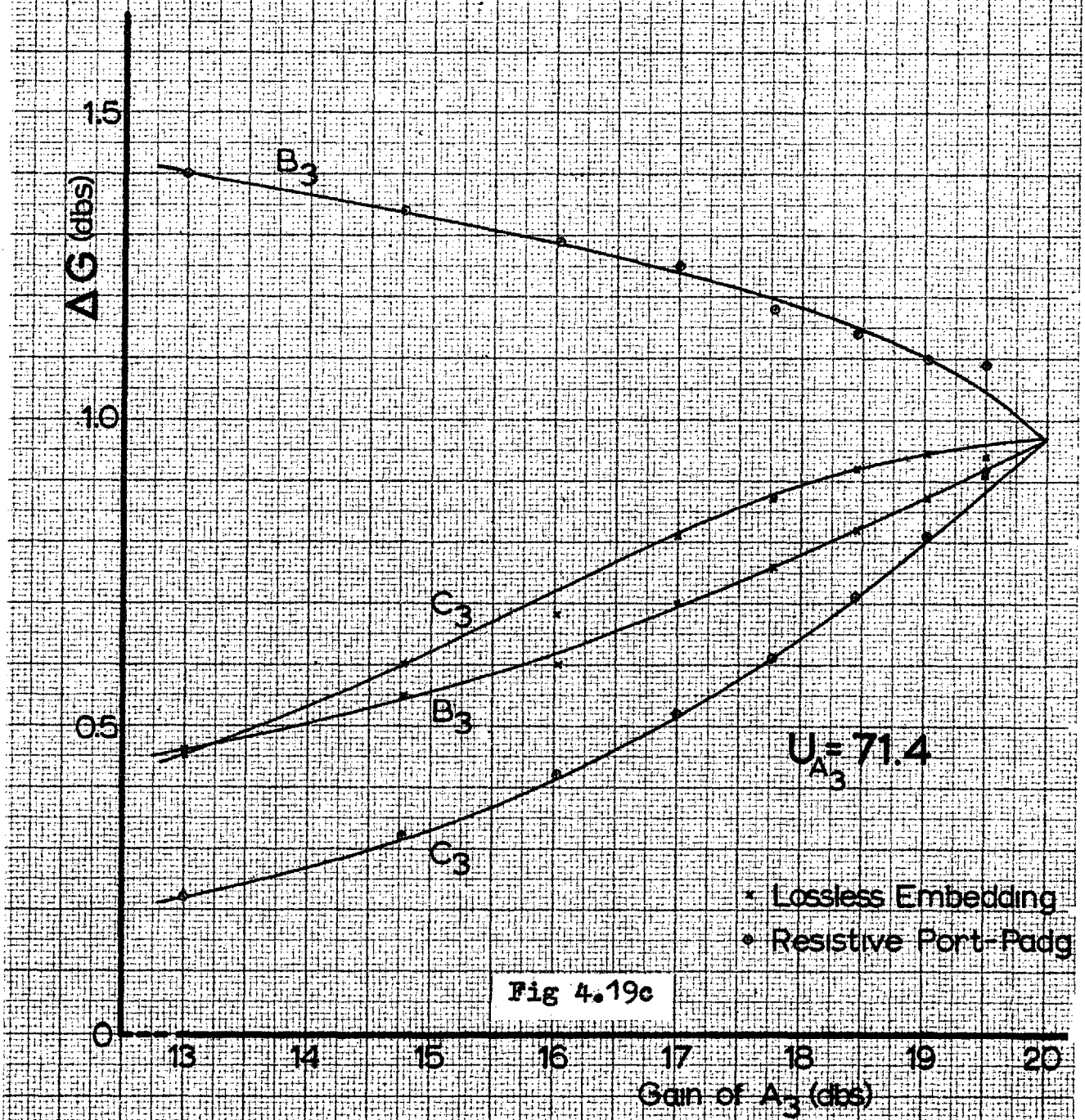

Fig 4.19c

Chapter 5

CONCLUSIONS AND FURTHER RESEARCH PROBLEMS

5.1 CONCLUSIONS

5.1.1 Synthesis of Amplifiers with Specified Gain-sensitivity Performance

It has been shown that for single frequency tuned two-port amplifiers, it is possible to predict the ultimate gain-sensitivity performance of the amplifiers, stated in the form $G \pm \Delta G$, from a knowledge of the natural points of operation of the batch of devices in the IGS. The theory has been shown to be equally applicable to devices which are potentially unstable.

5.1.2 Choice of Embedding

The choice of the mode of embedding to be used to achieve a specified gain-sensitivity performance has been shown to be dependent on the nature of the distribution of the points of operation of the batch of devices in the IGS. The case of 'ideal' spread was found to compare favourably with that of the batch of 19 transistors used in the experiment.

5.1.3 Stability Factors

The numerical values of stability factors S_i and k_i have been

shown to be poor indications of the margin of the devices from instability. It has been suggested that the sensitivity of the gain of the amplifier to changes in the embedding is a more realistic estimate of the margin of stability. The conditions $S_i > 1$ and $k_i > 1$ simply define the border of stability and no other meaning should be given to them.

5.1.4 Unilateral Power Gain (U)

The numerical value of U of a three terminal device has been shown to be an unsuitable measure of its 'activity'. Thus $0 > U$ and $U > 1$ simply define a border between activity and passivity.

5.1.5 Average Transistor

Statistical methods have been developed for the synthesis of the matrix of the average transistor. Since the design of the embedding circuit depends on the average transistor, this method which ensures that it has all the average properties of the batch is a significant step forward.

5.1.6 Use of Digital Computers

The speed and accuracy of the computer in performing the design calculations in this work have distinct advantages over the use of design charts.[34]

5.2 FURTHER RESEARCH PROBLEMS

The present work has led to a better understanding of the gain-sensitivity capabilities of transistors. It has also shown the need for further research into amplifier circuit design and device manufacture. These are discussed below.

5.2.1 Manufacture of Transistors with Specified Tolerances

This study has revealed the wide spreads which occur in a batch of nominally identical transistors. These divergencies arise from the lack of right control during the stages of manufacture. A study aimed at isolating the parameters to which the spread in the transistors are most sensitive and guidelines as to how these parameters may be controlled during manufacture should eliminate a large number of the problems which the author set out to solve in this thesis.

5.2.2 Resistance-Capacitance Amplifiers

The modern tendency to micro-miniaturise circuits have made the use of inductances almost an anachronism. Thus a study of embedding networks for sensitivity control involving only resistors and capacitors should make an interesting research topic. This can be carried to a further stage in which distributed resistance and capacitance embedding may be considered. The study of the manufacturing tolerances and the use of RC embedding could be considered as complimenting each other.

APPENDIX A

TRANSISTOR SYNTHESIS PROGRAM

INTRODUCTION

The program is divided into three parts; a main program and two subroutines. It employs the Doolittle technique[43]. The program is of such a general nature that it can be used in any situation in which curvilinear multiple regression is required. The algorithmn of the constituent parts of the program are given below. The language used is FORTRAN IV.

a) Main Programme

1) Read number of samples, total number of variables, number of dependent variables, number of independent variables, order of regression and the names of the variables.

2) Call Subroutine 'PROCES'.

3) Print (new) independent variables and dependent variables.

4) Call Subroutine 'DOLITL'.

5) Print the coefficients of the regression equation, the standard error of estimate, the standard error of the regression coefficients, the standard deviation of the dependent variable, the coefficients of multiple determination and correlation and the coefficients of partial correlation.

b) Subroutine 'PROCES'

1) If order of regression is unity go to 2, otherwise transfer independent variables into register 'ADEP' and permutate them. Go to 3.

2) Transfer independent variables into 'ADEP'.

3) Transfer dependent variable into 'DEP' registers.

4) Sum independent variable columns and calculate mean.

5) Sum dependent variable columns and calculate mean.

6) Enter $\sum_j (x_{ij} - \bar{x}_i)(x_{i'j} - \bar{x}_{i'})$ into 'A' matrix.

7) Return to main program.

c) Subroutine 'DOLITL'

1) Enter $\sum_j (x_{ij} - \bar{x}_i)(y_j - \bar{y})$ into 'A' column matrix for dependent variable.

2) Compute 'Check Sum Column'.

3) Compute 'C' unity matrix.

4) Apply Doolittle technique to 'A' matrix.

5) Compute coefficients of regression equation.

6) Calculate the constant term of the regression equation.

7) Compute 'C' matrix.

8) Compute the standard error of estimate and of the regression coefficients.

9) Compute the standard error of the dependent variable for the complete model.

10) Calculate the coefficients of multiple determination and correlation.

11) Calculate partial correlation coefficients[44] (i.e. eliminate each independent variable in turn and repeat process starting from step 4 of Subroutine 'PROCES'.

12) Return to main program.

APPENDIX B

LOSSLESS EMBEDDING ROUTINES

(Extended Mercury Autocode)

```
TITLE
LOSSLESS EMBEDDING

ROUTINE 1
(A,B)=(A1,B1)*(A9,B9)-(A3,B3)*(A7,B7)
(U1,V1)=(A9,B9)/(A,B)
(U3,V3)=-(A3,B3)/(A,B)
(U7,V7)=-(A7,B7)/(A,B)
(U9,V9)=(A1,B1)/(A,B)
RETURN
**

ROUTINE 2
Z1=V1+KZ
Z3=V3+KZ
Z7=V7+KZ
Z9=V9+KZ

(Z10,Z11)=(U3,Z3)/(U7,Z7)
(Z12,Z13)=(U7,Z7)-(U3,Z3)
Z14=(4U1U9-4U3U7)/(Z12Z12+Z13Z13)
RETURN
**

ROUTINE 3
(A,B)=(U1,Z1)*(U9,Z9)-(U7,Z7)*(U3,Z3)
(A1,B1)=(U9,Z9)/(A,B)
(A3,B3)=-(U3,Z3)/(A,B)
(A7,B7)=-(U7,Z7)/(A,B)
(A9,B9)=(U1,Z1)/(A,B)
RETURN
**
```

```
ROUTINE 4
Y1=B1+K'Y
Y3=B3-K'Y
Y7=B7-K'Y
Y9=B9+K'Y

(Y10,Y11)=(A3,Y3)/(A7,Y7)
(Y12,Y13)=(A7,Y7)-(A3,Y3)
Y14=(4A1A9-4A3A7)/(Y12Y12+Y13Y13)
RETURN
xx

ROUTINE 5
E=0.01
W=0.01
Z=0

>> DIRECTION FINDING (Z)
JUMPDOWN (R1)
K=0
JUMPDOWN (R2)
B'=Z11
Z=0.01
JUMP 6, B'> 0
K=1
JUMPDOWN (R2)
JUMP 5, Z11> B'
K=-1
JUMP 5
6)K=-1
JUMPDOWN (R2)
JUMP 5, B' > Z11
K=1
5)Z=0
U'=0
V'=0
I'=0
```

```
1)Z=Z+E
2)JUMPDOWN (R2)
>>DIRECTION FINDING (Y)
JUMPDOWN (R3)
K'=0
JUMPDOWN (R4)
B'=Y11
Y=0.01
JUMP 4, B'>0
K'=-1
JUMPDOWN (R4)
JUMP 19, Y11 > B'
K'=1
JUMP 19
4)K'=1
JUMPDOWN (R4)
JUMP 19,B' > Y11
K'=-1
19)Y=0
G'=0
H'=0
J'=0
>>(Y) ITERATION
11)Y=Y+W
12)JUMPDOWN (R4)
JUMP 51,0>Y11
G'=Y
51)JUMP 16,Y11> 0
H'=Y
16)JUMP 37,J'≥1
E'=B'Y11
JUMP 37,E'>0
W=W/10
```

```
JUMP 19
37)J'=J'+1
JUMP 9,J'=500
JUMP 11,G'=0
JUMP 11,H'=0
Y=0.5G'+0.5H'
B0=ØMOD(Y11)
JUMP 12,B0≥0.00005

>>(Z) ITERATION
JUMP 50,X>Y10
U'=Z
50)JUMP 3,Y10>X
V'=Z
3)I'=I'+1
JUMP 7,I'>15
JUMP 1,U'=0
JUMP 1,V'=0
Z=0.5U'+0.5V'
B0=ØMOD(X-Y10)
JUMP 2,B0≥0.00005

>>15 CYCLE TRAP
JUMP 8
7)U'=U'V'
JUMP 8,U'≠0
JUMP 10,0.001≥E
9)E=E/10
Z=0
I'=0
U'=0
V'=0
W=0.01
CAPTION
E TOO LARGE
JUMP 1
```

```
10)K=-K
Z=0
I'=0
U'=0
V'=0
E=0.01
W=0.01
CAPTION
K REVERSED TO
PRINT(K)1,0
JUMP 1
8)A'=Y10+Y14/2÷ØSQRT((Y10+Y14/2)(Y10+Y14/2)-(Y10Y10+Y11Y11))
G=1/A'
RETURN
xx

CHAPTER 0
A→ 10
B→ 10
U→ 10
V→ 10
Y→ 15
Z→ 15

>>READ TRANSISTOR PARAMETERS
I=1(2)9
JUMP 1,I=5
READ(AI)
READ(BI)
1)REPEAT

>>READ LAMBDA(R)
READ(X)
JUMPDOWN (R5)
PRINT(KZ)1,5
PRINT(K'Y)1,5
PRINT (G)1,1
```

```
END
CLOSE

2.48729      0.66042      0.00409     -0.01379
4.30492    -13.65130      0.15765      0.07813

0.0050

xxx Z
```

APPENDIX C

Y-MODE PORT-PADDING ROUTINES

(Extended Mercury Autocode)

```
ROUTINE 9

H0=A9+D
(H2,H4)=(A3,B3)/(A7,B7)
H5=(4A1H0-4A3A7)/(A7-A3)(A7-A3+(B7-B3)(B7-B3))
H6=H2+H5/2+.ØSQRT((H2+H5/2)(H2+H5/2)-(H2H2+H4H4))
H8=1/H6
RETURN
**

ROUTINE 10

C=0.01
6)D=0
L'=0
H10=0
H11=0

JUMPDOWN (R9)

H12=F'-H5
3)D=D+C
4)JUMPDOWN (R9)
JUMP 1,H5>F'
H10=D
1)JUMP 2,F'>H5
H11=D
2)JUMP 5,L'≥1
H13=H12(F'-H5)
JUMP 5,H13≥0
```

```
C=C/10
JUMP 6
5)L'=L'+1
JUMP 7,L'>29
JUMP 3,H10=0
JUMP 3,H11=0
D=0.5H10+0.5H11
B0=øMOD(F'-H5)
JUMP 4,B0≥0.00001
JUMP 8
7)NEWLINE 2
CAPTION
L'>29
PRINT(H10)1,6
PRINT(H11)1,6

8)NEWLINE 2
CAPTION
PORT PAD =
PRINT(D)1,5
PRINT(1000/D)1,0
CAPTION
(OHMS)
NEWLINE
PRINT(H2)1,5
PRINT(H4)1,5
PRINT(H5)1,5
PRINT(H6)1,5
PRINT(H8)1,1
PRINT(4.343øLOG(H8))1,1
NEWLINE 2
RETURN
xx
```

APPENDIX D

UNILATERAL POWER GAIN AND RESISTIVE EMBEDDING

The unilateral power gain can be written in terms of impedances as,

$$U = \frac{|Z_{21} - Z_{12}|^2}{4(R_{11}R_{22} - R_{12}R_{21})} \qquad (D1)$$

When a resistor is connected in series with the common lead, a new value of U is obtained:

$$U' = \frac{|Z_{21} - Z_{12}|^2}{4\,(R_{11}+R_f)(R_{22}+R_f)-(R_{12}+R_f)(R_{21}+R_f)} \qquad (D2)$$

Since the numerator of (D1) is the same as that of D2), the only way in which U' could be greater than U is for the denominator of (D2) to be less than that of (D1).

As $U' \rightarrow \infty$, $(R_{11}+R_f')(R_{22}+R_f')-(R_{12}+R_f')(R_{21}+R_f') \rightarrow 0$.

In the limit,

$$R_f' = \frac{R_{12}R_{21} - R_{11}R_{22}}{R_{11}+R_{22}-R_{12}-R_{21}} \qquad (D3)$$

When $R_f' = \infty$, U cannot be increased by Z-mode lossy embedding. Under these conditions,

$$R_{11} + R_{22} = R_{12} + R_{21} \qquad (D4)$$

Substituting in (D1),

$$U_{min} = \frac{|Z_{21} - Z_{12}|^2}{4(R_{22}-R_{21})(R_{12}-R_{22})} \quad . \tag{D5}$$

Since $U > U_{min}$,

$$R_{12} + R_{21} > R_{11} + R_{22} \tag{D6}$$

Therefore,

$$R_{11} + R_{22} - R_{12} - R_{21} < 0 \tag{D7}$$

Using the indefinite impedance matrix,

$$R_{11} - R_{12} = - R_{13}^{*} \tag{D8}$$

and

$$- R_{21} + R_{22} = - R_{23}^{*} \tag{D9}$$

Therefore,

$$R_{11} + R_{22} - R_{12} - R_{21} = -(R_{13} + R_{23}) = R_{33} \tag{D10}$$

and

$$R_{33} < 0. \tag{D11}$$

It is concluded that:

i) It is possible to increase the value of U of a device if $R_{12} + R_{21} > R_{11} + R_{22}$ (i.e. $R_{33} < 0$).

ii) The embedding resistor

$$R_f \leqslant \frac{R_{12} R_{21} - R_{11} R_{22}}{R_{11} + R_{22} - R_{12} - R_{21}} \tag{D12}$$

for U to remain finite and positive.

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*The sign of the transfer elements of the indefinite impedance matrix have to be changed when they are removed and replaced in the matrix, hence negative R_{12} and R_{21}.

APPENDIX E

SENSITIVITY OF GAIN TO VARIATION IN EMBEDDING ELEMENTS

Variations in the embedding elements and their effect on the gain of the amplifier have not been considered in this thesis. However, results computed for a simple case of lossless embedding are given in Fig. E1. The aim is to give a general idea of what the order of magnitude of these changes are. Fig. E1 shows a plot of gain against percent change in the susceptance Y_f for fixed values of the reactance Z_f.

It can be seen from Fig. E1, that with a nominal Z_f and a variation of $\pm 10\%$ in Y_f, the change in gain is 1.54 db whereas with nominal Y_f and a variation of $\pm 10\%$ in Z_f, the change in gain is 0.82 db.

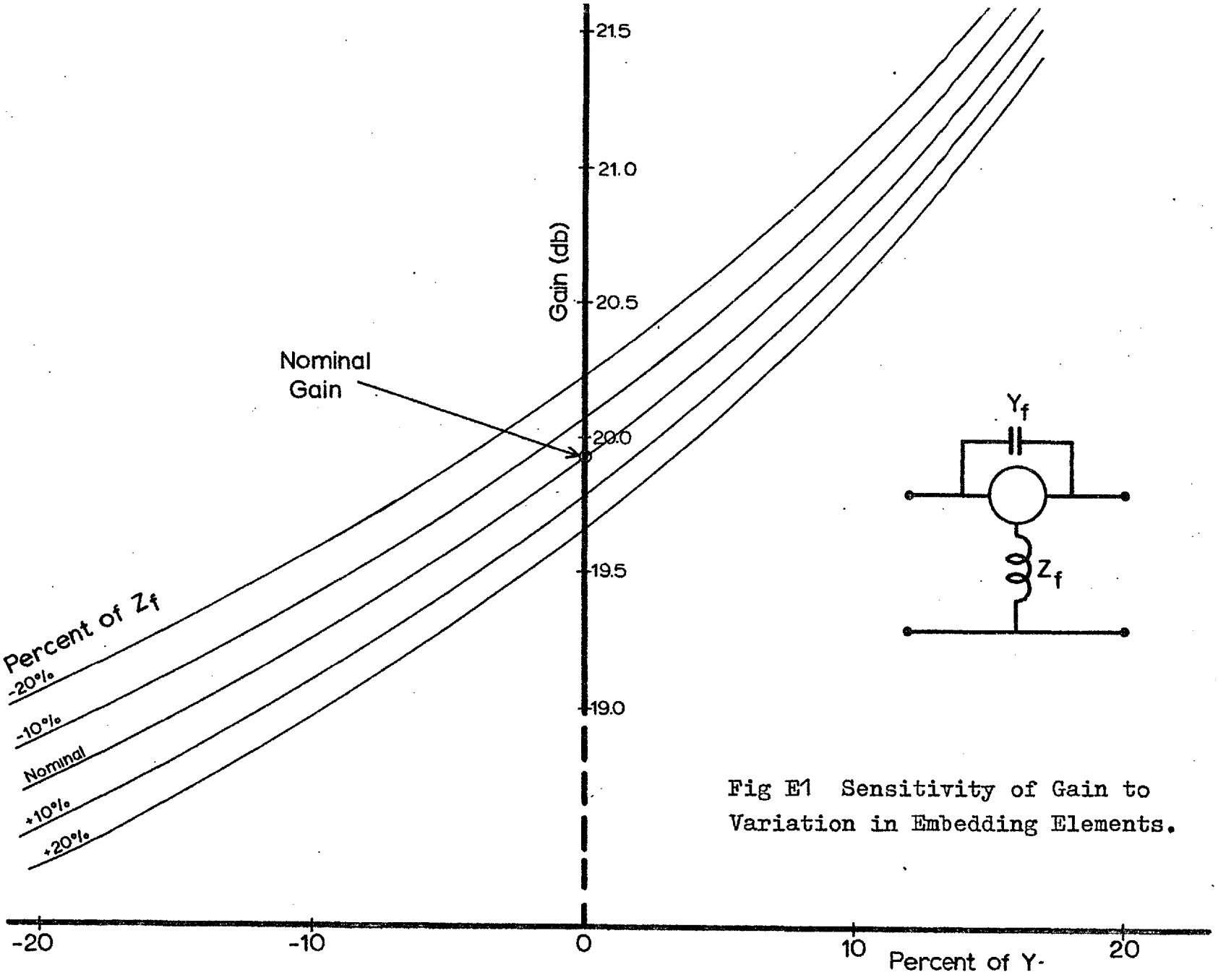

Fig E1 Sensitivity of Gain to Variation in Embedding Elements.

APPENDIX F

SENSITIVITY OF GAIN TO EMITTER CURRENT AND COLLECTOR VOLTAGE

Changes in gain arising from changes in emitter current and collector voltage have not been considered in this thesis. This is because changes in the bias point results in changes in the point of operation of the transistor in the IGS; the theory then applies. Fig. F1 shows a plot of the point of operation of a transistor as the collector voltage and emitter current are varied.

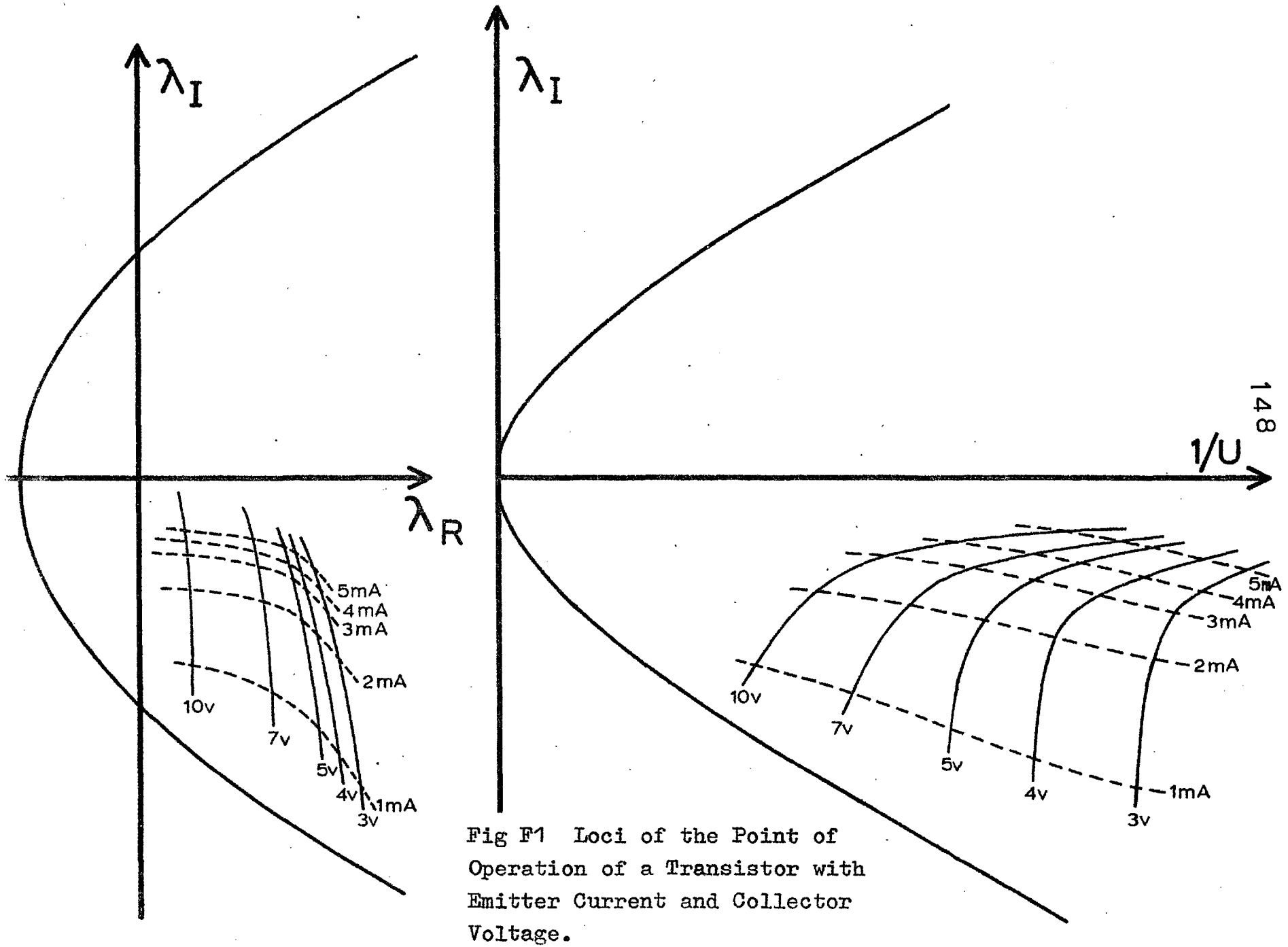

Fig F1 Loci of the Point of Operation of a Transistor with Emitter Current and Collector Voltage.

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