TUNED HIGH-FREQUENCY TRANSISTOR POWER AMPLIFIERS

AND FREQUENCY MULTIPLIERS

A Thesis Presented By

Ronald Harvey Johnston

For the Degree of

DOCTOR OF PHILOSOPHY of the UNIVERSITY OF LONDON

August, 1967

ABSTRACT

This investigation is concerned with transistorised power amplifiers and frequency multipliers operating at high frequencies with maximisied power outputs. An important feature of the work is the derivation of circuit models from which performance characteristics are found. Nonlinear circuit behavior, essential for power amplification and frequency multiplication, is found in the charge storage properties of the input and output junctions of the transistor.

The input nonlinearity is employed, characterised, and analysed for purposes of power amplification and frequency multiplication. The analysis facilitates a comparison of the multiplier and amplifier accounting for transistor limitations. Amplifiers and multipliers, using the input nonlinearity are practicable, the multiplier showing a loss in power gain compared with an amplifier at a given output frequency.

Multiplier circuits utilising the output nonlinearity, have shown excellent performances and demonstrated the inadequacy of previous theoretical treatments. A new theory for the multiplication mechanism developed here, assists in the successful understanding of the transistor multiplier and provides an analysis for diode (step recovery) frequency multipliers. Multiplication at the transistor output can increase the maximum frequency of usefulness by a factor of two or more. Output powers of 2.5 watts (0.80 GHz) and 1.2 watts (1.20 GHz) have been obtained by doubling and tripling, respectively.

Multiplication using the nonlinear output is superior to the nonlinear input particularly at the transistor upper frequency limit.

ACKNOWLEDGEMENT

TABLE OF CONTENTS

APPENDICES

Location of Figures and Tables

List of Principal Symbols

Symbol	Page of first useage	Definition
BV	61	Breakdown voltage of a diode or a transistor junction.
C	68	Capacitance.
C_{BE1}, C_{BC1}	68	Depletion layer capacitance located, electrically, under the extrinsic base resistance r_{bb}.
C_{BE2}, C_{BC2}	68	Depletion layer capacitance located externally to the extrinsic base resistnace r_{bb}.
C_{CBmin}	170	Minimum collector-base capacitance
$C_{CB}(v)$	197	Collector-base capacitance as a function of applied voltage.
C_{Ext}	139	A capacitance added to a diode for multiplication.
D	68	Diode
f	52	Frequency
f_{max}	26	Maximum frequency of oscillation of a transistor.
f_β	20	Frequency at which the current gain of a common emitter transistor falls to 3 db less than the low frequency value
$f_1(\alpha', n, \varepsilon)$	85	Function relating feedback modified harmonic output current to input voltage.
$f_2(\alpha', n, \varepsilon)$	87	Function relating feedback modified direct collector current to input voltage.
$f_3(\alpha', n, \varepsilon)$	89	Function relating feedback modified input power to input voltage.
F_{PDeg}	74	Input power degradation factor.
F_T	24	Unity gain frequency of a transistor in common emitter configuration.

i	29	Current, all harmonic components specified.
i_f	79	Feedback current due to depletion layer capacitance.
$i''_{B1} - i''_{B3}$	73	Base currents flowing into the input depletion layer capacitance.
i'_C	80	Collector current modified by feedback.
i'_D	79	Transistor input diode current modified by feedback.
I	32	Peak current.
$I'_{B1inphase}$	88	Peak fundamental base current inphase with base voltage.
I_{Cnmax}	62	Maximum harmonic collector current permitted by input breakdown voltage.
I'_{Cnmax}	110	I_{Cnmax} including the effect of capacitive feedback.
K_{FM}	141	Multiplier diode figure of merit.
K_G	126	Constant relating the input and output resistances of a diode multiplier.
$K_G K'_{PO}$	139	Low frequency, normalised output power of a diode multiplier.
K_{PO}	136	Maximum normalised output power of a diode multiplier.
L_s	116	Diode series inductance.
m	123	An integer representing diode conduction angle.
MRR	127	Minimum resistance ratio of a diode multiplier.
n	48	An integer representing the output harmonic.
P	32	Electrical power.
P_{BinDeg}	74	Fundamental power input to the base degraded by the input depletion layer capacitance.

P'_{Bin}	89	Input power to base modified by feedback.
P_{Dis}	104	Power dissipation capability of device.
P_{indc}	32	Transistor dc input power.
P_{norm}	168	Varactor normalised power.
q	68	Charge, including all harmonic components.
Q	123	Peak value of charge components.
r_{bb}	55	Extrinsic base resistance of a transistor.
r_{cc}	79	Collector series resistance.
r_s	116	Diode series resistance.
R'_{in}	120	Apparent input resistance of a diode multiplier.
R_L	38	Load resistance of an amplifier or a multiplier.
R'_L	120	Useful load resistance of a diode multiplier.
R_o	78	Output resistance of a common emitter transistor.
t	31	Time in secounds.
v	29	Voltage, with all harmonic components specified.
v''_{IB}	70	Intrinsic base voltage.
V	31	Peak value of voltage components.
V_{Bcon}	61	Threshold conduction voltage of the transistor base.
V_{CC}	31	Collector supply voltage.
V_{Csat}	31	Collector saturation voltage.
α	39	One half of the transistor collector conduction period.

α'	81	One half of the transistor collector conduction period modified by feedback.
γ	170	Exponent of the depletion layer capacitance law.
ϵ	83	Matching factor of a transistor amplifier or multiplier.
η	128	Diode multiplier power conversion efficiency.
η_{CI}	32	Collector current efficiency.
η_{CP}	32	Transistor collector power conversion efficiency.
η_{Cv}	32	Collector voltage efficiency.
η_{LF}	131	Low frequency diode multiplication efficiency.
η_{HF}	131	High frequency diode multiplication efficiency.
τ_f	39	Forward injection charge-control parameter.
ϕ	135	Angle of maximum reverse diode voltage.
ψ	170	Barrier potential of a varactor diode.
ω	29	Angular frequency.
ω_o	131	Angular cutoff frequency of a step recovery diode or a varactor diode.
ω'_{cn}	129	Normalised angular cutoff frequency of a step recovery diode.

Principle Subscripts

B	Base
C	Collector
D	Diode
E	Emitter

in	input
max	maximum value attained
n	an integer representing a particular harmonic
o	output
0,1,2,3 etc.	denotes an average, a fundamental or a harmonic, respectively.

CHAPTER ONE

INTRODUCTION

1.1   Object of Investigation

This thesis is concerned with the theory, design and experimental investigation of high frequency transistor frequency multipliers. A comprehensive study of transistorised frequency multipliers has, hitherto, been absent. The investigation is extended to include transistor power amplifiers. The extension is relevant to the treatment of transistors employing output frequency multiplication, which involves power amplification as part of the total mechanism. In addition, the comparison of frequency multiplier and power amplifier performances is facilitated.

The aim of this study is to establish theoretically sound methods for the design of amplifiers and frequency multipliers, which are both accurate and simple. The various possible modes of frequency multiplication are investigated theoretically and their relative merits are assessed. The emphasis is on circuit analysis, the transistor being represented by the simplest adequate model.

1.2   Historical Background

1.2.1   Power amplifiers and frequency multipliers

The functions of power amplification and frequency multiplication are almost as old as the first significant active electronic device. Class C amplifiers in valve form first made an appearance in 1923[1]; the valve frequency multiplier was developed a few years later[2, 3].

These two valve circuits have been associated ever since. The
association of these circuits has stemmed from the similarity of
operation and application in communication and broadcast transmitters.
Usually a crystal controlled oscillator produced a low frequency
that was increased in a chain of valve frequency multipliers. The
chain drove a power amplifier which was likely to be the output stage
of the transmitter. This configuration allowed the oscillator to
operate at low frequencies (and hence attain good frequency stabil-
ities) and also reduce the likelihood of transmitter oscillation. In
the chain the frequency multipliers were operated, and the power
amplifiers were most likely operated, in the "Class C mode". The
"Class C mode" of operation depends upon a nonlinearity in the valve
transfer characteristic. The drive on the input of the valve is
adjusted and biased so that the anode current flow takes the form of
pulses occuring at the input frequency rate. The voltage on the anode
is sinusoidal and tuned so that the anode voltage is a minimum during
the short interval of the high anode current. This mode of operation
minimises the anode power dissipation allowing a high conversion
efficiency of direct power to radio frequency power.

The operation of the valve multiplier is very similar to the
power amplifier. The anode current pulses have a considerable
harmonic content and a tuned circuit is chosen so that one of these
current harmonics energise the load. Thus the nonlinear transfer
characteristic that is used to increase the power conversion effic-

iency of the power amplifier also provides the harmonic generation
necessary in the frequency multiplier. The mechanisms used in
frequency multiplication and power amplification in the valve are
so similar that most of the design equations are the same and
certainly the same design approach is used. The Class C method of
harmonic generation formed the most important basis for frequency
multiplication for a long time. Multipliers using rectifying diodes
and nonlinear inductive elements were known but did not gain
widespread acceptance.

1.2.2   The transistor

The junction transistor[4], first developed in 1951, was capable
of a gain up to about fifteen megacycles and an audio frequency power
output of about twenty milliwatts. The frenetic research and devel-
opment into semiconductors has raised the power and frequency capa-
bility of the transistor by several orders of magnitude. The power-
frequency capability progressed with each of the following transistor
types: point-contact transistor, grown-junction transistor, alloy-
junction power transistor, diffused-junction transistor, silicon
planar transistor. Today most of the high frequency power transis-
tors are of a double-diffused, epitaxial, multi-emitter, silicon
planar structure. Shown in Fig. 1.1 are state-of-art transistor
power and frequency output capabilities[5,6]. These output capabil-
ities have promoted an intense interest in transistor power

Figure 1.1

High frequency, power characteristic of available
transistors. The manufacturers are represented by
the initials. Circles and squares represented values
obtained from References 5 and 6, respectively.

Output Power in Watts

100

10

1

ITT
ITT
ITT
ITT
RCA
TRW
TI
RCA

x10   x100   x1000

MHz

Output Frequency
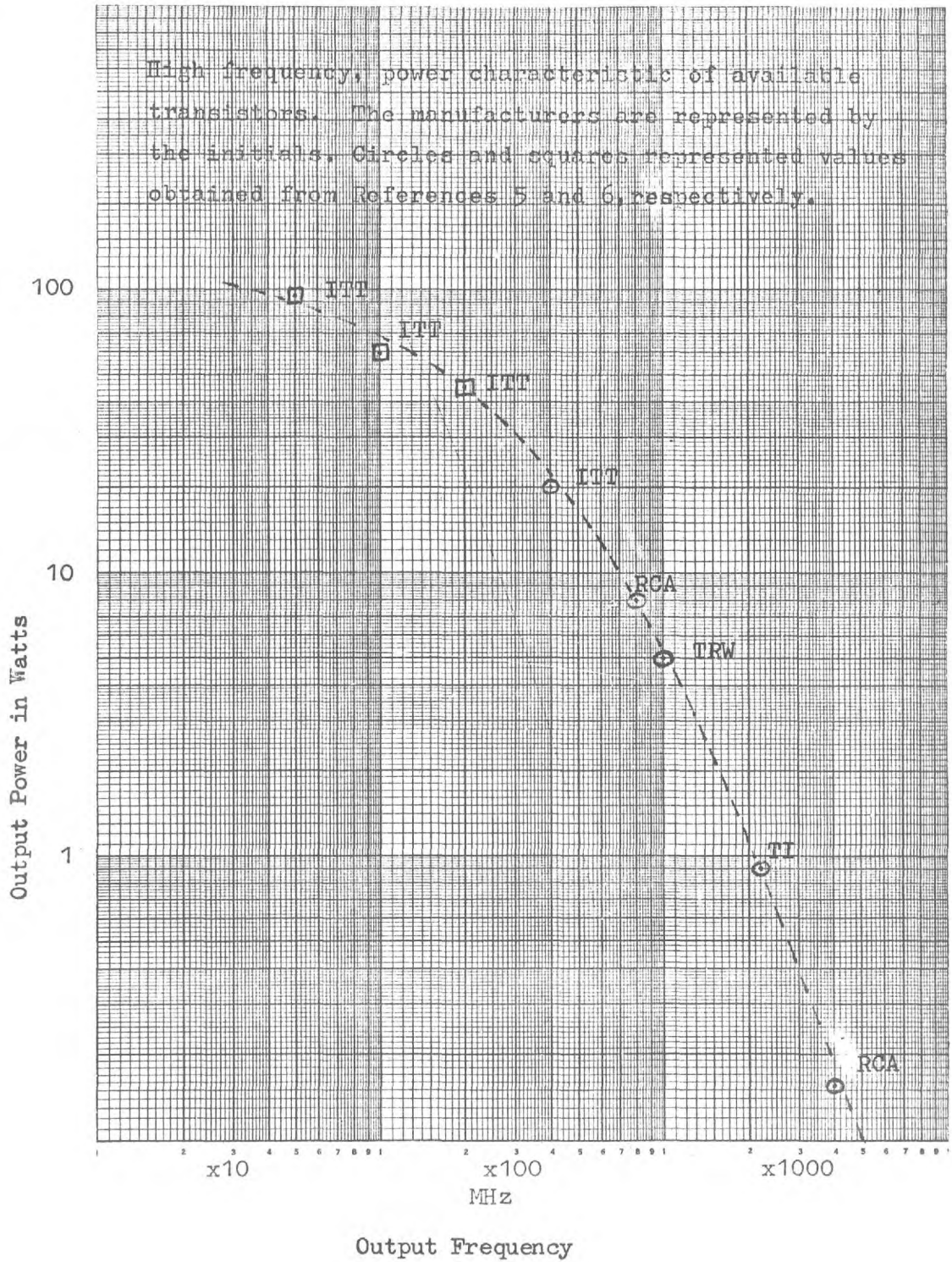
amplifiers and frequency multipliers for use in solid state radio frequency sources in a manner very similar to the valve amplifiers and multipliers used in early transmitters.

1.2.3   The transistor power amplifier and frequency multiplier

The similarity (real and imagined) of the transistor to the valve made it intuitively obvious that the transistor would operate (as a power amplifier or frequency multiplier) in the same circuit as a valve. The transistor did work as an amplifier and as a multiplier and it was assumed that the analysis was the same[7, 8, 9]. The charge storage characteristics of the base were neglected[10], thus inadvertently limiting accurate application of the analysis to frequencies less than f_β. Recently the base charge storage effect was recognised and accounted for in a transistorised Class C amplifier[11, 12].

Another practical method of harmonic generation in the transistor became known[13] recently. In this new method the transistor operates as an amplifier and fundamental power is prevented from leaving the transistor. The fundamental power operates on the nonlinear capacitance of the collector and it is efficiently converted into a harmonic power[14, 15]. This method extends the upper frequency of usefulness of the transistor by a factor of two or three. Other methods of transistor frequency multiplication exist but do not perform better than the above mentioned methods[16].

1.3 Application for Transistor Power Amplifiers and Frequency Multipliers

The newly acquired frequency and power performance of the transistor has caused energetic studies and development of solid state radio frequency power sources. The transistor is often employed in these sources for frequency multiplication and power amplification stages in the way the valve was (and is) used in broadcast transmitters. The transistor converts the direct power into rf power which may be increased in frequency in a varactor (or a multiple varactor) frequency multiplier. These power sources may find application in both the transmitting and receiving sections of transponders, light radar, telecommunication and telemetry systems. Transistors are useful in the above applications, not because of their superior frequency and power output performance (compared with travelling-wave tubes, klystrons and magnetrons), but because of their superior electrical reliability, mechanical ruggedness, size and weight, and power conversion efficiency. These other characteristics ensure the utilisation of the transistor in many demanding environments even where its power and frequency output capabilities are marginal for the application concerned.

Some semiconductor devices, other than the bipolar junction transistor, have shown a great deal of promise for similar applications. Devices such as the avalanche transit time diodes, Gunn effect diodes, and tunnel diodes are most useful for frequencies higher than those easily met by the transistor. Varactor diodes and step recovery diodes

are best thought of as adjuvants to the transistor rather than
as substitutes. The two diodes cannot convert direct power into radio
frequency power but can change the rf power into a more useful frequency
with low loss. The diodes effectively extend the useful frequency
range of the transistor.

The junction transistor is the best solid state device for
conversion of direct power into a significant quantity of radio
frequency power (viz. more than 0.1 watts) in the frequency range of
1.0 MHz to 1.0 GHz. The indications are that the junction transistor
will occupy this position for a long time to come.

1.4   Goals and Approach to Analysis of Transistor Amplifiers
       and Frequency Multipliers

The circuit of a transistor amplifier or frequency multiplier
may be modified at will without affecting a given analysis providing
that the assumed input and output operating conditions are maintained.
Transistors employed in push-pull or parallel configurations can be
treated in terms of a "single transistor analysis". The analyses
developed in this thesis deal specifically with transistors operated
in the common emitter mode. However, much of the following theory
applies to common base operation as well.

1.4.1   Nonlinear input power amplification

The transistor is normally employed for power amplification in a method very analogous to the way the valve is used. A sinusoidal voltage is applied to the transistor input with bias, A sinusoidal voltage of the input frequency is maintained at the transistor output. The output tuned circuit and the load is energised by collector current pulses. This method (frequently called Class C operation, irrespective of collector conduction angle) of operating the transistor as a power amplifier is the most universal and is the most versatile. Other methods[17] of transistor power amplification are known but will not be considered here.

1.4.2   Transistor frequency multiplication capability

For successful frequency multiplication the transistor must contain some nonlinear characteristic. The transistor contains a number of the necessary nonlinearities. It contains two diode sections (the emitter-base diode and the collector-base diode) and each of these diodes contains a nonlinear resistance (with discontinuities from reverse bias to forward bias and from low reverse bias to reverse bias into avalanche breakdown) and a nonlinear capacitance (the nonlinear capacitance (the nonlinear capacitance results from the nonlinear depletion layer capacitance and also nonlinear minority carrier charge storage). Normally either the nonlinear capacitance or the nonlinear resistance predominates depending upon the frequency of operation. These nonlinearities are the predominant ones, and provide plenty of

scope for frequency multiplication. Other nonlinearities, less
pronounced, are also found in the transistor. For example, the high
frequency current gain is dependent upon the collector operating
conditions. See Fig. 1.2.

Figure 1.2
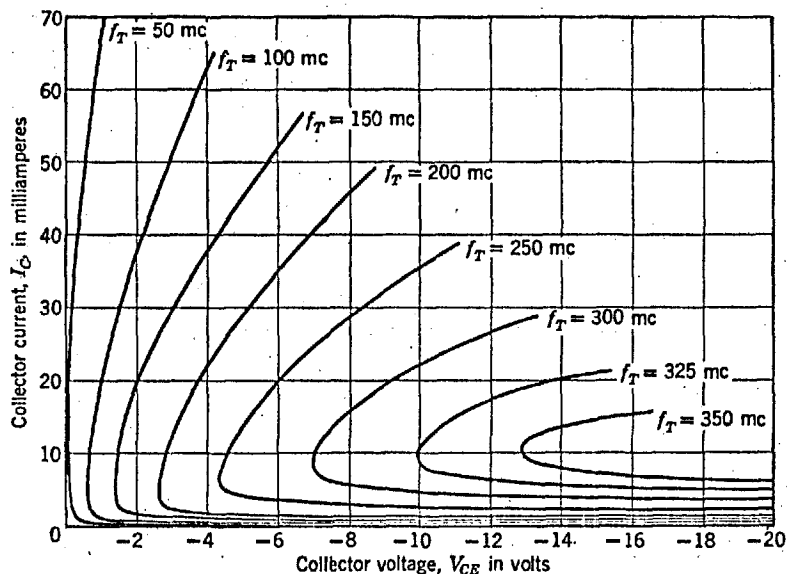
Typical variation of F_T (and hence high frequency common emitter
current gain) as a function of collector operating conditions.
The transistor is a silicon planar type 2N2401[41].

1.4.3   Nonlinear input frequency multiplication

It has been found that the input nonlinearity (base-emitter
nonlinear resistance or nonlinear capacitance depending on operating
frequency) can be used effectively for frequency multiplication. Two

different analyses are required for the nonlinear resistance mode and for the nonlinear charge storage mode. The nonlinear resistance mode is in control at frequencies lower than f_β and the nonlinear charge storage mode is in control at frequencies above; the two modes merge at approximately f_β. Many authors[9, 10] have assumed that the nonlinear resistance mode is applicable at all operating frequencies. Frequency multiplication, using the input nonlinearity, is very similar to power amplification, and for this reason the two will be analysed together. Analyses[9] are presented by other authors which deal with amplifier and multipliers with operating frequencies of less than f_β. For the purposes of this study (i.e. maximum power, high frequency) a transistor operated at frequencies of less than f_β is not being fully utilised. For these two reasons a full analysis of this frequency range will not be made. Instead a rudimentary graphical analysis is presented in Chapter Two.

For operating frequencies higher than f_β a comprehensive analysis is carried out in terms of the nonlinear input charge storage. The analysis is presented in Chapter Two and provides the first analysis, of any kind, of high frequency nonlinear input transistorised frequency multipliers operating in the nonlinear input mode. A charge storage analysis is also developed for the high frequency power amplifier; while this analysis is not the first of its kind, it is believed that it is superior to previous approaches. Nonlinear input amplification or multiplication, using the transistor, shall henceforth be referred to by NIAM.

Chapter Three deals with the effect of depletion layer capacitance on the operation of the power amplifier and frequency multiplier. In this way the limitation of f_{max} (of the transistor) is introduced and the analysis is applicable up to the maximum frequency of usefulness of the transistor. Finally, a complete design procedure is presented for this kind of power amplifier and frequency multiplier.

1.4.4   Nonlinear output frequency multiplication

The transistor has been operated very successfully[13, 14, 15] using the capacitive nonlinearity of the collector diode (in the output circuit). The transistor input circuit is constructed and behaves in a way similar to a conventional amplifier but at the output, the fundamental power is prevented from leaving the transistor. The fundamental power is converted into a harmonic power, by the output nonlinear capacitance, which is dissipated in the load via tuned circuits. Multiplying factors of up to four are attainable with practical power conversion efficiencies. Frequency multiplication using the transistor output nonlinearly will be called NOM (nonlinear output multiplication).

It has, hitherto, been assumed that the nonlinear capacitance of the collector diode depends on the depletion layer charge storage only. Measurements and calculations in this study indicate, however, that the effect of the nonlinear depletion layer capacitance is insufficient to be responsible for the level of harmonic output power actually obtained. Observations of the collector voltage waveforms

indicate that the collector voltage "bottoms" for a large part of the fundamental cycle. These two occurrences suggest strongly that minority carrier charge storage takes place in the collector-base diode. For this reason, an analysis is made of frequency multiplying circuit utilising a minority carrier nonlinear charge storage device. This analysis is presented in Chapter Four and is used, together with another recent work[18] in the later treatment of the high frequency transistor NOM. The analysis of Chapter Four is also important because of its application to frequency multipliers employing step recovery diodes.

In Chapter Five nonlinear output transistor frequency multipliers are constructed and the performance is measured. The minority carrier charge storage multiplication theory is supported by measurements. The operation of the overall stage is treated and then an outline of design and construction methods is presented.

1.5   Originality

Except where reference is made to the work of others, the research and the conclusions reported in this thesis are original as far as the author is aware.

CHAPTER TWO

POWER AMPLIFICATION AND FREQUENCY MULTIPLICATION

USING THE TRANSISTOR NONLINEAR INPUT

2.1   Assumed Circuit Configuration

The operation of the historically developed valve frequency

multiplier and power amplifier depends upon one nonlinear character-

istic;   namely the dependance of anode current on grid voltage in a

common cathode circuit. If a sine wave of voltage is applied to the

grid of the valve, with proper biasing, a distorted sine wave of

current is obtained at the anode. Power may then be extracted at a

fundamental or harmonic frequency. Analysis of this method of power

amplification or frequency multiplication is facilitated by assuming

that the grid and anode voltages consist of sine waves at the input and

output frequencies, respectively. The above mode of circuit operation

is very frequently assumed to be applicable to transistor power

amplifiers and frequency multipliers. The fundamental voltage

(filtering ensures that only the fundamental is present) is applied

to the transistor input (assumed for the moment to be operating in

the common emitter configuration) along with a biasing voltage or

current. The biasing is set so that both the base and the collector

of the transistor conduct for a fractional part of the fundamental cycle.

The base-emitter nonlinear diode characteristic is thus utilised. The

circuit can operate with an infinite number of variations of input

voltage waveshapes and output voltage waveshapes. However, it is
assumed that the input and output voltage waveforms are sinusoidal,
purely in the interests of analytic convenience. The circuit is then
constructed with a view to meeting the above assumptions but experience
shows that actual input and output waveshapes may deviate appreciably
(from the sinusoidal input and output voltage assumptions) without
affecting the performance of the circuit significantly. A simple
example of a circuit that will meet the above assumptions is shown
in Fig. 2.1.

Figure 2.1
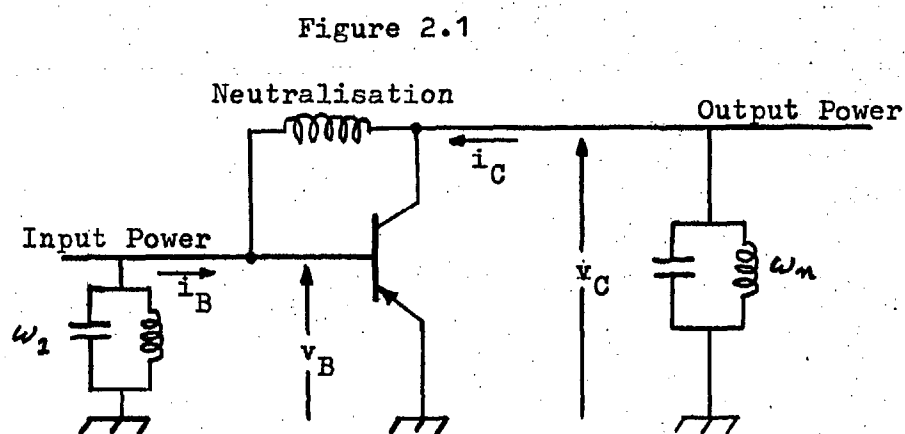
Amplifying and multiplying circuit designed to meet assumptions
of sinousoidal voltages on input and output. Biasing omitted.

Although transistor circuits may in practice take a completely
different configuration, analysis, based on the above circuit, will

be applicable to any circuit that maintains sinusoidal voltages on

the input and the output. For example, multipliers and amplifiers

using a number of transistors (i.e. push-pull, push-push or parallel

circuits) may be treated with the following analysis providing the

sinusoidal voltage assumptions are met. The following analysis is

based on the common emitter configuration because this is the most

widely employed and may be used over a broad range of frequencies.

Much of the above investigation and analysis is applicable to the

common base configuration. The extent of the possible application will

be indicated.

2.2   General Relationships of Output Voltage, Current and Power
       in Power Amplifiers and Frequency Multipliers

The assumption that a sinusoidal voltage is maintained at the

transistor output permits the development of some general relationships

that partially describe the performance of the transistorised power

amplifier and frequency multiplier. The output voltage and a hypo-

thetical current of the transistor are illustrated in Fig. 2.2.

The transistor produces current pulses at a repetition rate equal

to the fundamental frequency. The output tuned circuit filters the

desired and available harmonic current and transfers harmonic power

to the load. The direct input power to the transistor and load is,

Figure 2.2
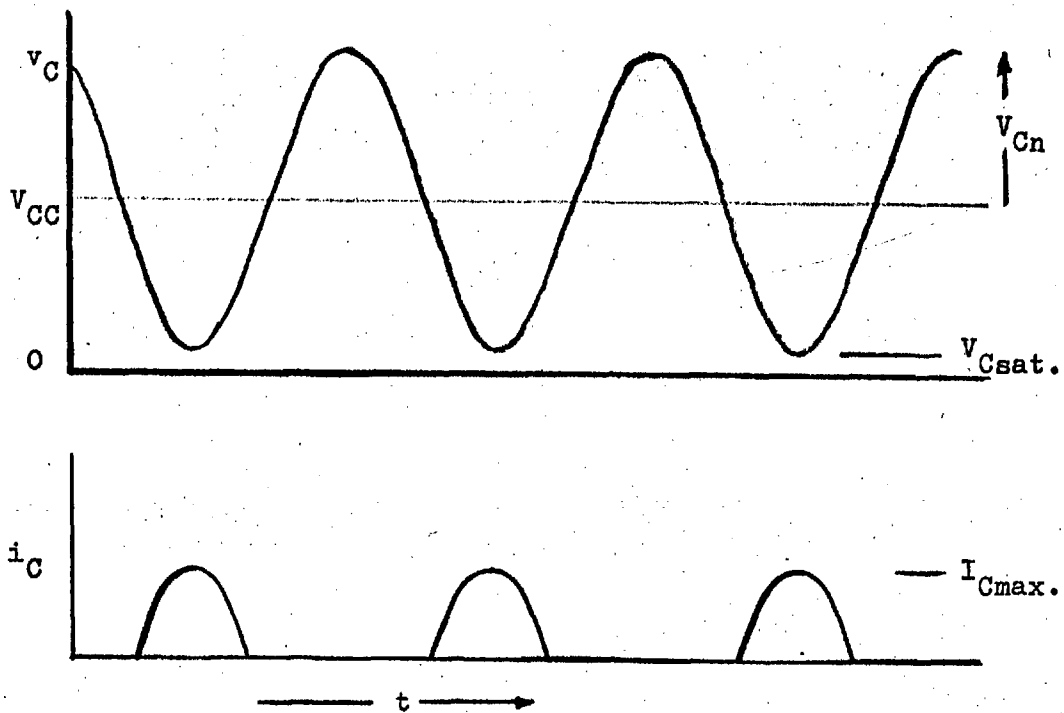
Transistor collector voltage and a hypothetical collector current of a tuned power amplifier.

$$P_{indc} = V_{CC} \cdot I_{CO} \qquad \qquad 2.1$$

where V_{CC} is the supply voltage and I_{CO} is the direct current drawn by the transistor. If the output tuned circuit is adjusted to resonance, the output power is,

$$P_{oC} = 0.5 \cdot V_{Cn} \cdot I_{Cn} \qquad \qquad 2.2$$

where V_{Cn} and I_{Cn} are the peak nth harmonic voltage and current of the collector respectively. The power conversion efficiency of the transistor may be calculated from the above two expressions.

$$\eta_{CP} = \frac{I_{Cn} V_{Cn}}{2 I_{CO} V_{CC}} \qquad \qquad 2.3$$

This power conversion efficiency may be separated into two parts, one a current conversion efficiency, and the other a voltage conversion efficiency. Explanation of the separation will follow.

$$\eta_{CI} = \frac{I_{Cn}}{2 I_{CO}} \qquad \qquad 2.4$$

and

$$\eta_{Cv} = \frac{V_{Cn}}{V_{CC}} \qquad \qquad 2.5$$

where

$$V_{Cn} \leqslant V_{CC} - V_{Csat} \qquad \qquad 2.6$$

The voltage efficiency of Eqn. 2.5 can, for most transistors, be made to exceed .80. The exact value of it depends very much on the transistor in use. The maximum voltage efficiency may be determined very quickly if the appropriate transistor collector characteristics are available and the peak collector current is known. Normally the voltage efficiency will vary between .70 and 1.00 and depends

largely on the transistor in use. The maximum voltage efficiency

must be determined or estimated for each application by the designer.

The current conversion efficiency of Eqn. 2.4 has a broad range

of possible values. For an amplifier it can vary from 0.50 to 1.00.

For a multiplier it can vary between zero and 1.00. It is shown

experimentally that the current efficiency is a definite function

(albeit a complicated one) of transistor conduction angle. At the same

time, current efficiency is essentially independant of the type of or

individual transistor employed in the circuit. Since current efficiency

can not be easily evaluated and is very important, it will receive a

comprehensive study.

2.3   Low Frequency Graphical Analysis

NIAM operation of the transistor at low frequencies is similar

to frequency multipliers and power amplifiers using the valve. The

similarity is widely recognised[7, 8, 9, 19] but has received excessive

attention. It is frequently assumed, incorrectly, to exist at high

frequencies. Because design methods are already available (being

converted from valve methods [7, 8] and also developed specifically for

transistors[10, 20]) only a rudimentary graphical method will be

presented here.

The transistor characteristic at low frequencies (less than $f_\beta/2$)

may be specified quite simply. At low frequencies, the transistor

terminal currents are single valued functions of the terminal

voltages, permitting the transistor action to be defined graphically
on a current versus voltage basis. An example will be given dealing
with a common emitter doubler. The same approach will deal with power
amplifiers through to times-six frequency multipliers. The analysis
may be applied to a common base circuit with the proper choice of
transistor characteristics. As with valve circuits, the analysis of
this circuit is best initiated by examining the effect of the applied
sinusoidal voltage on the input. The input voltage, with biasing, is
set so as to produce a particular peak collector current and a certain
conduction angle. High factors of frequency multiplication or high
current efficiencies (η_{CI}) in amplifiers require small conduction angles.
The input characteristic of the transistor, employed as a doubler, is
shown in Fig. 2.3. After the shape of the input current pulse is
determined the fundamental component of the input current may be deter-
mined using a graphical Fourier analysis. Equations for determining
harmonic components of a symmetrical (about a particular time axis)
waveform are given in Appendix 1. The fundamental current to the input
of the transistor may be calculated, permitting the power input to the
transistor to be evaluated. Since the transistor input behaves like a
nonlinear resistance, the input current is in phase with the input
voltage. This is true for the input and output currents and voltages
of the transistor at low frequencies (viz. all phase angles are zero).
The input operating characteristics such as, biasing voltage on input and

Figure 2.3

Low frequency operation of a
transistor (type BFY88)
employing the nonlinear input
for frequency doubling. A
sine wave of voltage is applied
to the base of the transistor
(in common emitter configuration)
to produce a pulse of base
current.

Input Base Current

Input Base Voltage

Input Voltage

$t=0$

Input Current i_B
Milliamps
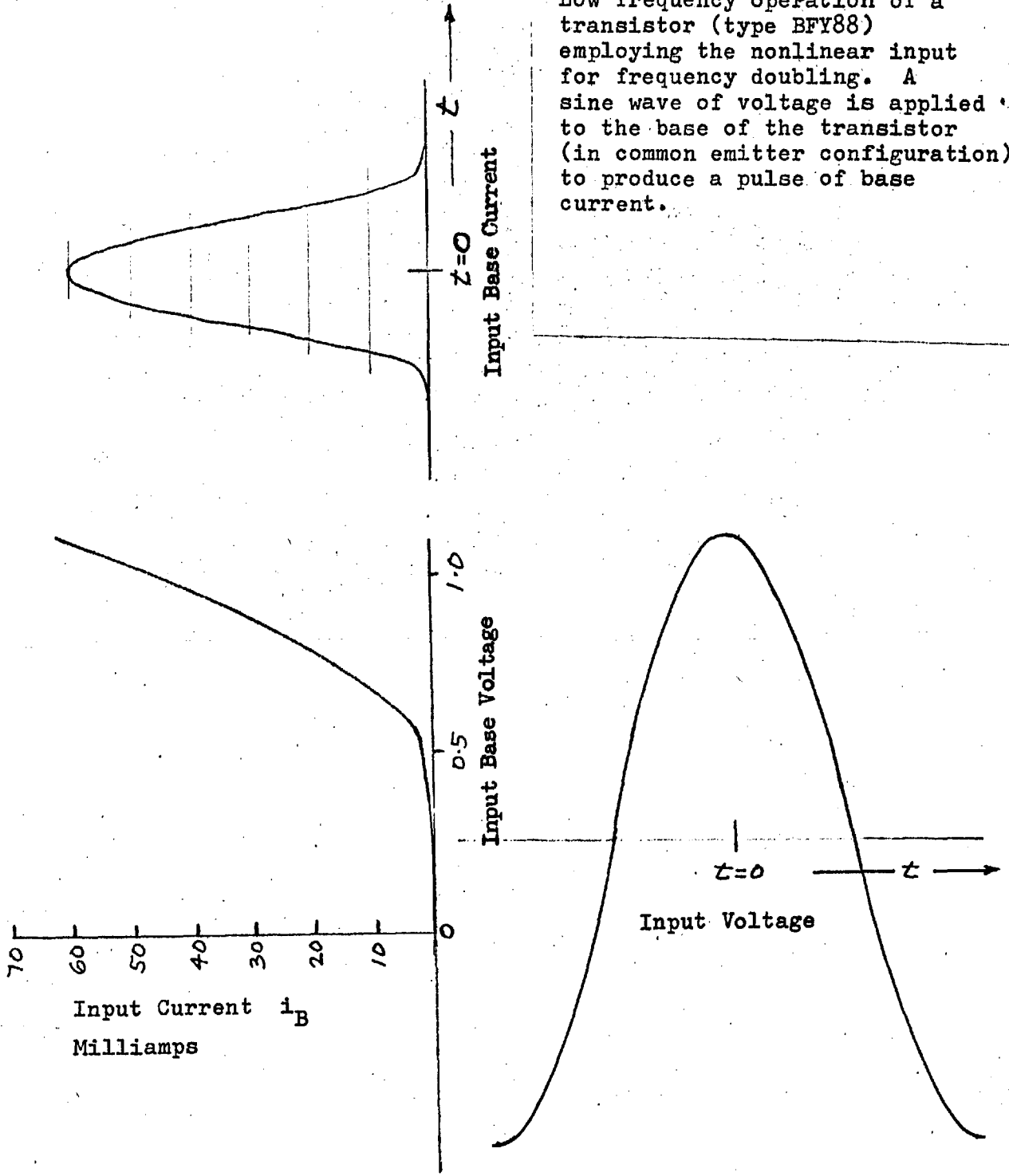
input impedance, may now be determined. From the peak base current
we may find the peak collector current using the appropriate plot of
collector characteristics (see Fig. 2.4). Once the peak collector
current is determined, the minimum collector voltage may be found
(see Eqn. 2.6). The peak harmonic collector voltage may be evaluated
after the minimum collector voltage is known and the supply voltage
V_{CC} is set. The harmonic voltage must be sketched in, permitting the
collector current to be determined as shown in Fig. 2.4. The collector
current pulse may then be determined as a function of base current,
collector voltage and time. The appropriate harmonic and the direct
components of current of the collector current pulse may be determined
graphically by the method outlined in Appendix 1. The evaluation of
I_{CO} and I_{Cn} permits the calculation of the harmonic output power, the
direct power input to the collector, the collector efficiency, the
transistor power dissipation and the load resistance. Equations 2.1
through to 2.5 may be used to advantage in these calculations.

The important parameters of a low frequency power amplifier may
thus be determined.

2.4   Assumed High Frequency Current Waveforms

It is intended here to first find the harmonic current generating
characteristics of the intrinsic base at high frequencies when the
assumed sinusoidal voltages are applied. The high frequency conditions

Figure 2.4

Collector Voltage v_C

Collector Current i_C
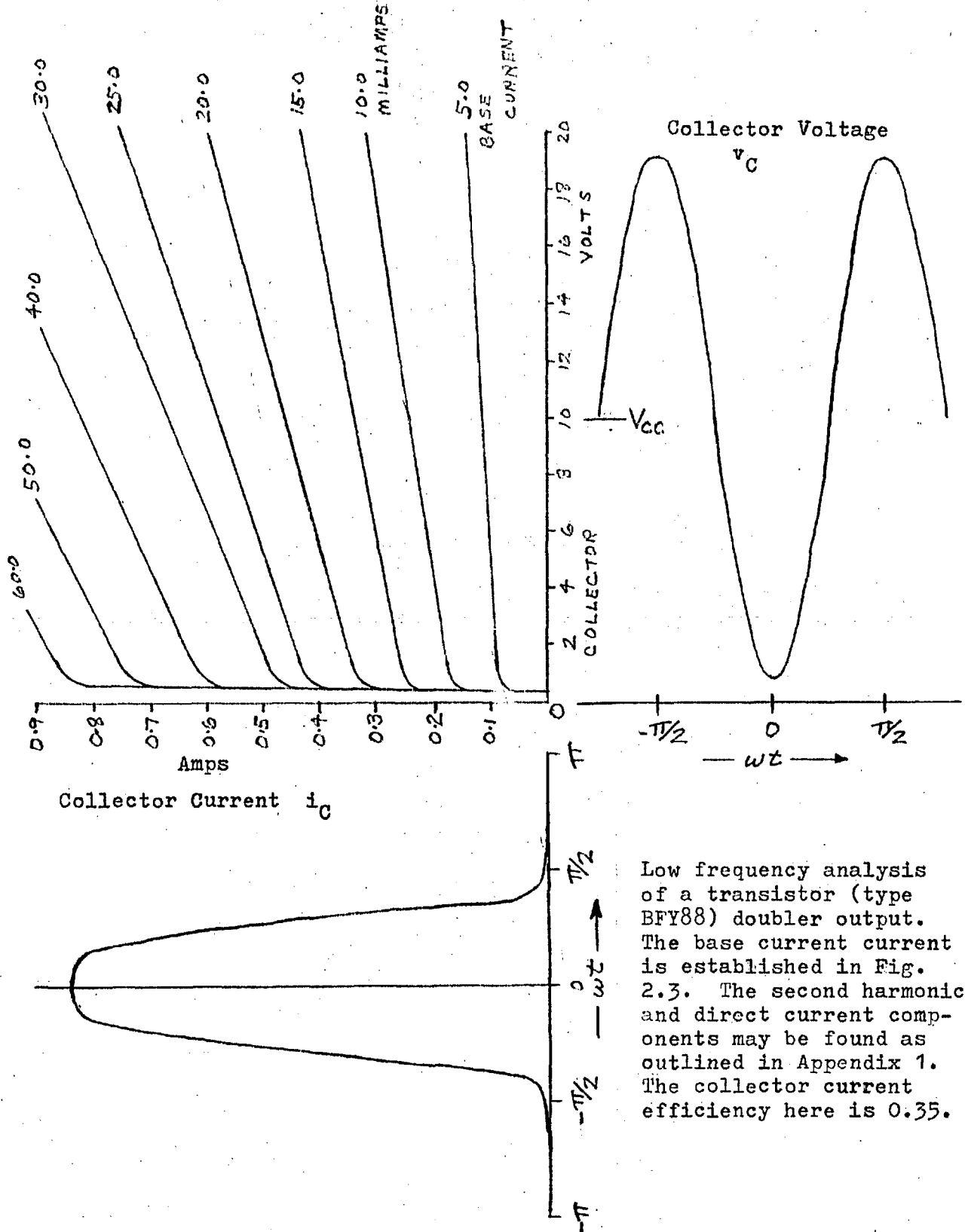
Low frequency analysis of a transistor (type BFY88) doubler output. The base current current is established in Fig. 2.3. The second harmonic and direct current components may be found as outlined in Appendix 1. The collector current efficiency here is 0.35.

exist if the input frequency is greater than $3f_\beta$. Stray effects may be very important but the intrinsic base is essentially the active portion of the transistor providing the power gain and the conversion of direct power into rf power. The effects of the strays are best assessed after the basic multiplication and energy conversion processes are understood. The depletion layer capacitances of the transistor obscure the operation of the base without necessarily degrading the frequency multiplying or amplifying performance. For observation of the current waveforms in actual transistors, a method of balancing out the depletion layer capacitance currents is developed. Two balanced transistors are used, one under normal conditions and the other always reversed biased. In this way the capacitive current flow in the inactive transistor may be subtracted electrically from the current flow in the active transistor. Thus the measurement circuits show only the current flow into the intrinsic base of active transistor. This circuit is shown in Fig. 2.5.

Figure 2.5
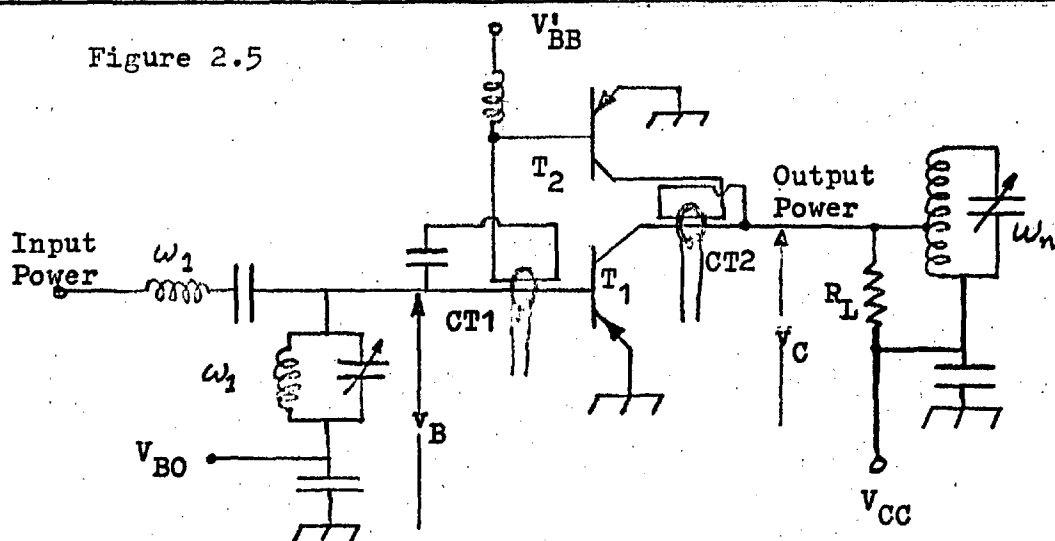
Measurement of currents of the intrinsic base behaviour of a transistor NIAM. The depletion layer capacitance currents of T_2 cancel those of T_1, the transistor being examined.

Insight into the multiplying operation of the intrinsic base may be gained most quickly by a study of the relations between the input voltage and current waveforms as presented in Fig. 2.6. The collector current is proportional to the integral of the base current. From the charge control relations[21] we may write,

$$i_C = \frac{1}{\tau_f} \int i_B \, dt \qquad\qquad 2.7$$

This equation follows from the more usual charge control relations under the present high frequency conditions, where minority carrier recombination is negligible. The clue to the operation of the whole circuit is the behaviour of the base current. The base current is a scaled replica of the input voltage, for a large part of the active cycle (i.e. where $-\alpha < \omega t < \alpha/2$). A detailed knowledge of the input impedance characteristic of the transistor can be obtained from the voltage-current relationship measured at the base terminal and plotted in Fig. 2.7. Input voltage is plotted on the vertical axis, current on the horizontal. Numbers 1 to 4 are marked in Fig. 2.7 to indicate various regions of operation. Small allowances must be made for the incompletely balanced-out depletion layer capacitance currents. The region between numbers 1 and 2 is very similar to that found at very low frequencies in a diode and will be called the exponential region; charge being stored in the base. The region between numbers 2 and 3 is called the "linear charge-discharge"region. The slope of this line is

Figure 2.6

Input Voltage v_B

Input Current i_B

Output Current i_C

Output Voltage v_C
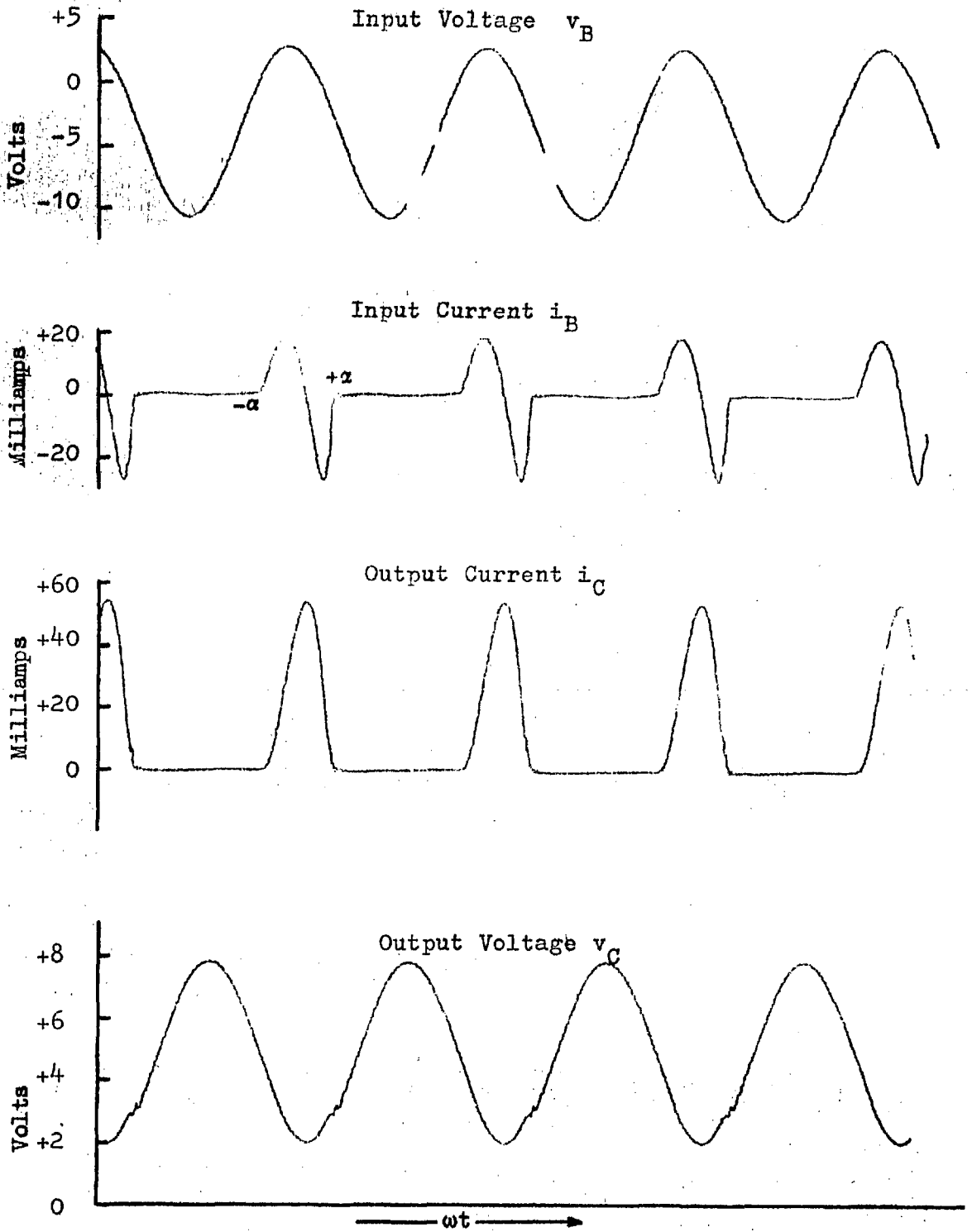
Typical amplifier (or multiplier) voltage and current waveforms, using the nonlinear input. The measurements were made at 2.0 MHz on an OC42. Note that the input current is roughly a scaled replica of the input voltage over the region $-\alpha < \omega t < \alpha/2$.

Figure 2.7
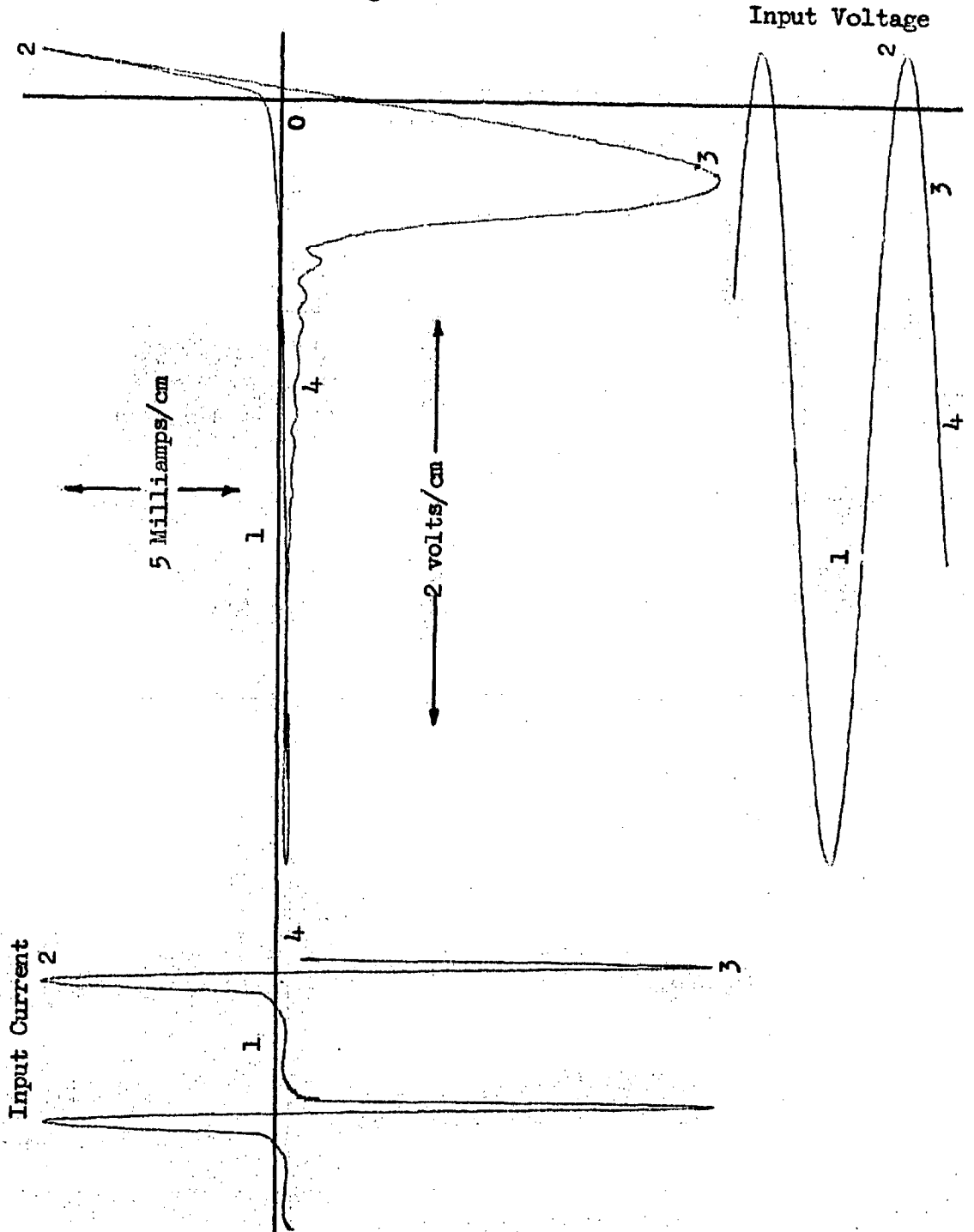
The relationship of input current and voltage of a transistor
(type OC42) NIAM at 2.0 MHz. input. The measurement was obtained
using a dual channel sampling oscilloscope (HP 185B with a 187B
plugin unit). One channel measured i_B and the other v_C. This
plot was then obtained using an x-y recorder. The measured circuit
is shown in Figure 2.5.

controlled by the extrinsic base resistance of the transistor.
The region from numbers 3 to 4 is called the "residual charge removal"
region. The "residual charge" typically amounts to about one half of
the maximum stored charge. Many transistors have been examined and the
first two regions, namely the "exponential" and the "linear charge-
discharge" region are very consistent. However, the shape and the
duration of the last region is very changeable. In diffusion transistors
(where impurity doping is essentially constant across the base) the shape
of the "residual charge removal" region has been found to vary considerably
even among transistors of the same type number. In planar, double
diffused transistors (with both retarding and aiding fields in the base)
the "residual charge removal" region is found to vary considerably both
in shape and duration with a changing conduction angle; the other two
regions maintaining their shape. It has been found experimentally
that a planar transistor may exhibit a step recovery characteristic for
small conduction angles and exhibit an exponential recovery (with a
relatively long time constant) for large conduction angles.

In Fig. 2.8 the three terminal currents of two diffusion
transistors of the same type have been noted in detail. The charge
control relationship between the base current and collector current,
described in Eqn. 2.7, may be verified in these figures. The variation
in the time delay of the collector current pulse, the emitter current
recovery, and the shape of the base "residual charge removal" may be
seen to be significant.

Figure 2.8   43
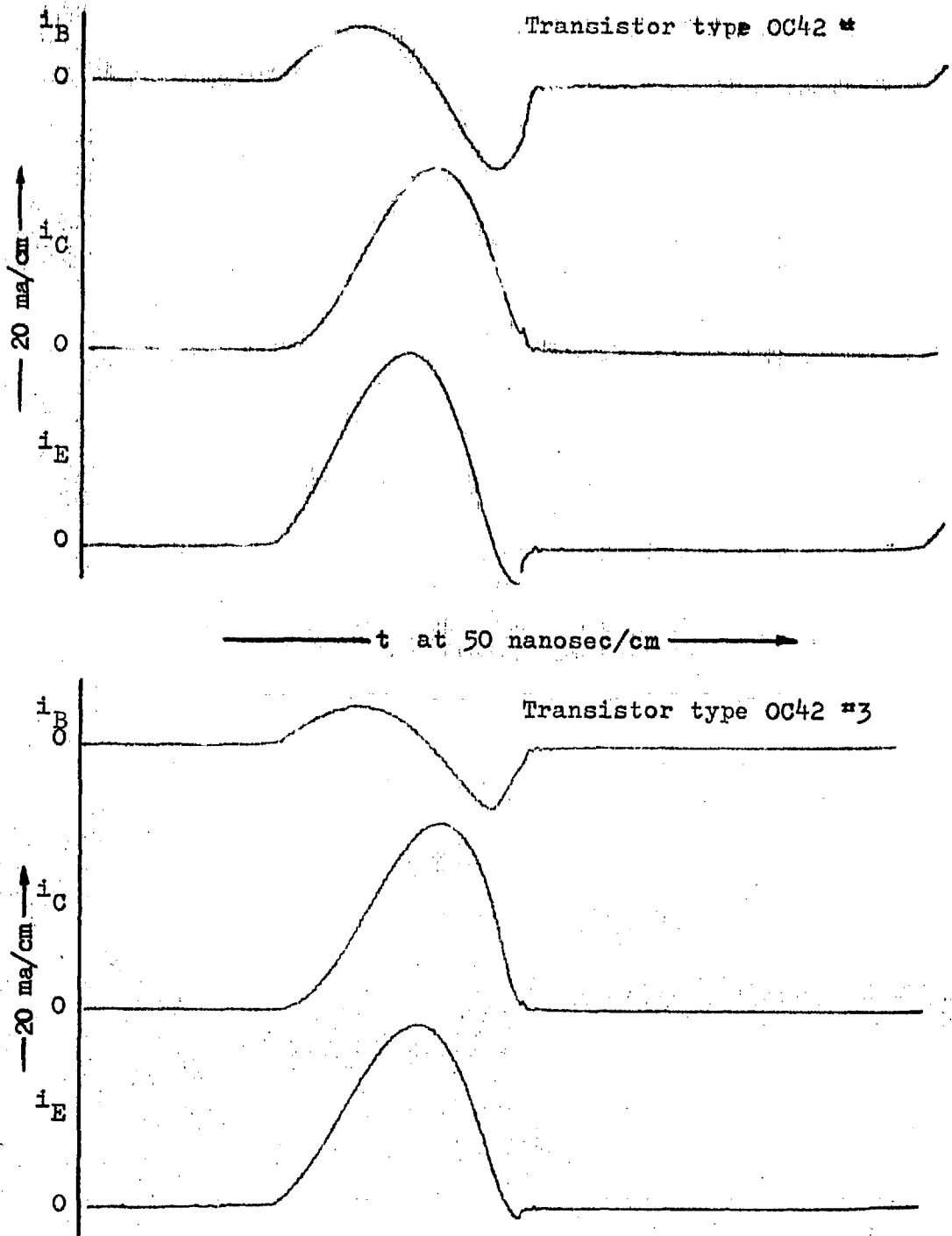
Transistor currents of NIAM operation. Note the differences in the base currents and in the emitter currents. The differences are attributed to different electric fields in the base.

The charge removal problem here is very similar to the charge removal problem in diodes at high frequencies. The charge recovery characteristics are dependant upon operating voltages and currents as well as the electrical and physical construction of the diode or transistor. Analysis of diodes is only partially successful and yet these are much simpler to analyse than transistors. Due to the impossibility of accurate analysis, simplifying assumptions must be made.

Since charge control relations apply at our operating frequencies, we need only assume a certain current waveshape for either the base or collector and the other is implied. The method adopted here assumes a certain base current and then the collector current is determined using the charge control relations. We see that if the transistor is forward biased by the sine wave of voltage on the base, the base current has a waveshape virtually identical to the voltage waveshape. Thus for about one half of the complete cycle the input current is a truncated sine wave. The other half of the input current pulse is extremely variable and one particular current waveshape will not accurately describe all the possibilities. It is advantageous in the following analysis to have a symmetrical waveform. For these reasons it is felt best to assume that the second part of the current pulse has the same shape but opposite sign to the first part of the current pulse. The assumed base current waveshape may be seen in Fig. 2.9.

Figure 2.9

"Partial Sinusoid Model"

$$i_B = I_{Bmax} \frac{\cos(\omega t + \alpha/2) - \cos\alpha/2}{1 - \cos(\alpha/2)}$$

when $-\alpha < \omega t < 0$

$$i_B = -I_{Bmax} \frac{\cos(\omega t - \alpha/2) - \cos(\alpha/2)}{1 - \cos(\alpha/2)}$$

when $0 < \omega t < \alpha$
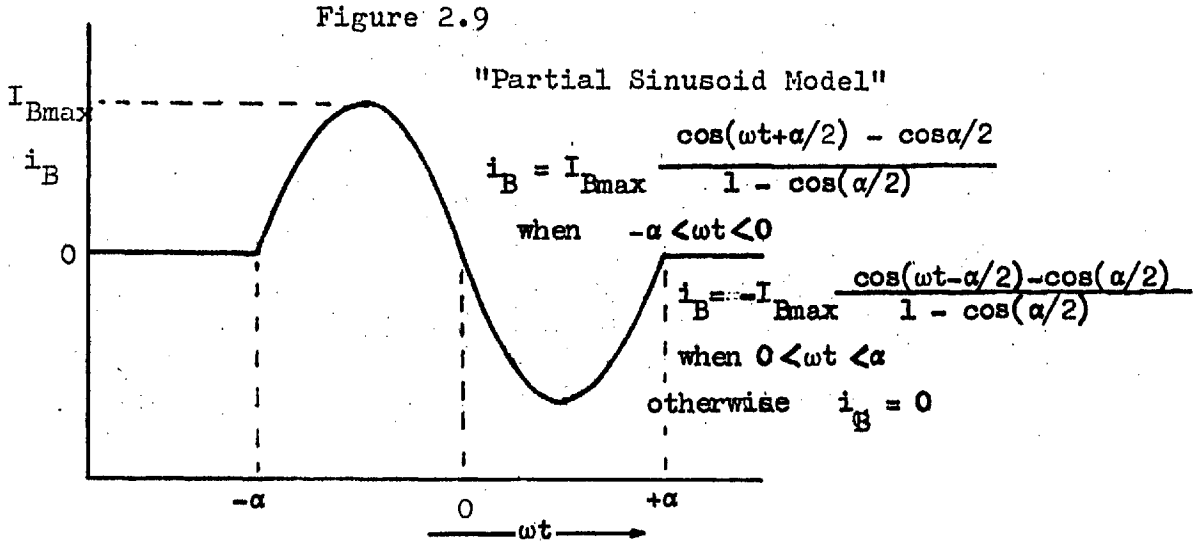
otherwise $i_B = 0$

The base current may be defined algebraically, as follows.

$$i_B = I_{Bmax} \left(\frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right)$$

when $-\alpha < \omega t < 0$
and
$$i_B = - I_{Bmax} \left(\frac{\cos(\omega t - \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right) \qquad 2.8$$

when $0 < \omega t < \alpha$

otherwise $i_B = 0$

This waveshape will be called the partial sinusoid model.

Two other workers[11,12] on transistorised class C amplifiers

have made approximations to the transistor current waveforms.

Slatter[12] developed an approach much the same as above but assumed

a step-recovery characteristic for the base current as shown in

Fig. 2.10.

Figure 2.10

$$i_B = I_{Bmax} \frac{\cos(\omega t + \alpha/2) - \cos(\alpha/2)}{1 - \cos(\alpha/2)}$$

when $-\alpha < \omega t < \phi$

otherwise $i_B = 0$
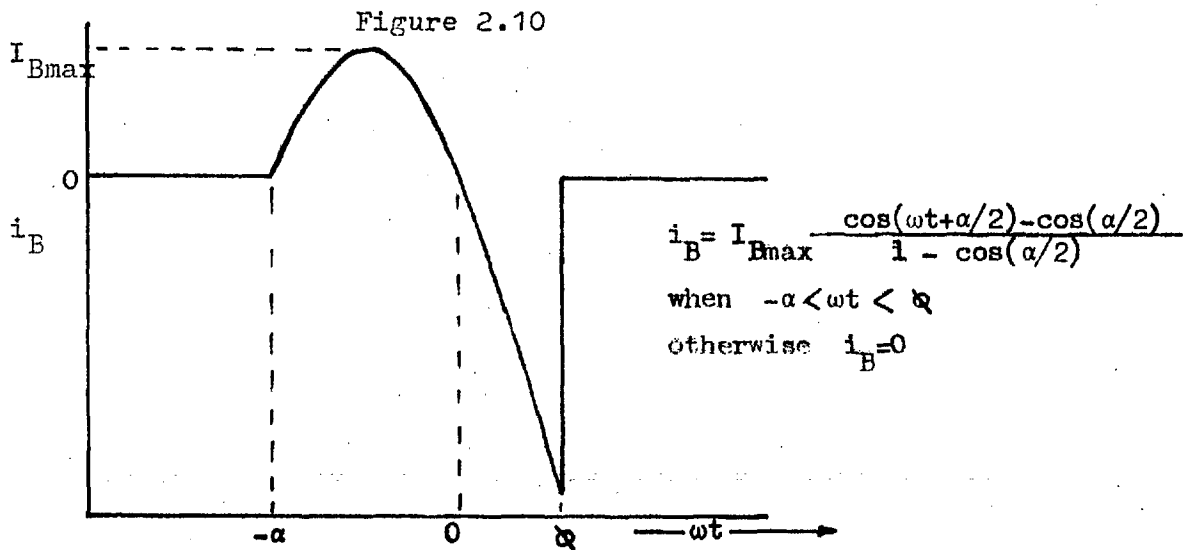
Base current exhibiting a step-recovery characteristic. Ther~ is
no net charge input to the transistor, and ϕ is related to α on
this basis.

Such a characteristic is accurate for some planar transistors operated

at small conduction angles. It is, however, inaccurate for the majority

of transistors. This approach also has the disadvantage that the

harmonic components of the input current waveform contain an associated

phase angle.

In the partial sinusoid model, the phase angle of any harmonic

current is zero due to the symmetry of the waveform. Scott[11] in an

earlier analysis of a transistor class C amplifier assumed a "quartic" output current waveform, shown in Fig. 2.11.

Figure 2.11

$$i_C = I_{Cmax}(1- \frac{\omega^2 t^2}{\alpha^2})$$

when $-\alpha < \omega t < \alpha$
otherwise
$$i_C = 0$$
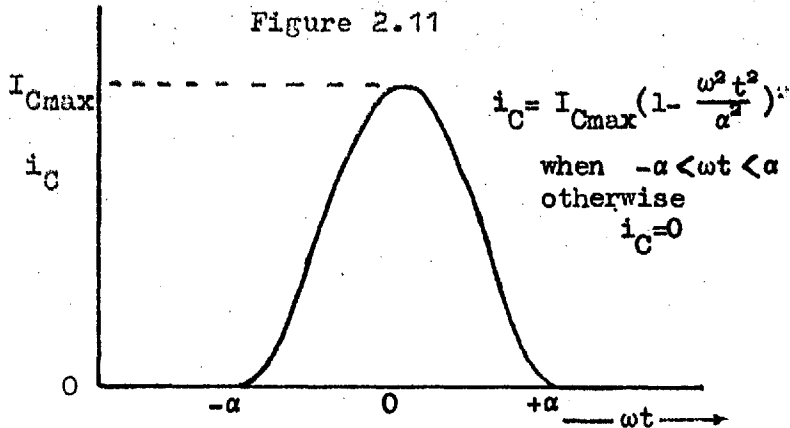
Assumed collector current pulse shape referred to as the "quartic model".

We shall see later that calculated collector efficiencies from this model are good but not as accurate as those produced by the "partial sinusoid model". Other workers have considered idealised collector currents with truncated sine waves or rectangular pulses. These models have only convenience to recommend them for they bear little resemblance to the actual waveforms found in transistor NIAM. The last models will receive no further consideration.

2.5 Collector Current Efficiency

To determine the collector current efficiency we need only

determine I_{Cn} and I_{CO} and by using Eqn. 2.4 the required efficiency can be determined. It may be shown, using Eqn. 2.7, that

$$I_{Cn} = \frac{I_{Bn}}{n\omega\tau_f} \qquad 2.9$$

Thus, in order to determine I_{Cn}, we may do a Fourier analysis on the input base current. That is,

$$I_{Bn} = \frac{I_{Bmax}}{\pi} \int_{-\alpha}^{0} \frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \sin(n\omega t)\,d\omega t$$

$$- \frac{I_{Bmax}}{\pi} \int_{0}^{+\alpha} \frac{\cos(\omega t - \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \sin(n\omega t)\,d\omega t$$

$$= \frac{I_{Bmax}}{\pi(1-\cos\alpha/2)} \left\{ \frac{\cos(n\alpha+\alpha/2) - \cos \alpha/2}{n + 1} + \frac{\cos(n\alpha-\alpha/2) - \cos \alpha/2}{n - 1} \right.$$

$$\left. + \frac{2\cos\alpha/2}{n} (1 - \cos n\alpha) \right\} \qquad 2.10$$

It is now possible to determine I_{Cn}. Next I_{CO} must be evaluated. Using Eqn. 2.7 and part of Eqn. 2.8 we may write,

$$i_C = \frac{I_{Bmax}}{\omega\tau_f} \int_{0}^{\omega t} \frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \,d\omega t$$

$$= \frac{I_{Bmax}}{\omega\tau_f} \left[\frac{\sin(\omega t+\alpha/2) - \omega t \cos\alpha/2}{1 - \cos\alpha/2} \right]_{0}^{\omega t}$$

$$i_C = \frac{I_{Bmax}}{\omega\tau_f} \left(\frac{\sin(\omega t+\alpha/2) - \omega t \cos\alpha/2 + \sin\alpha/2 - \alpha\cos\alpha/2}{1 - \cos\alpha/2} \right)$$

in the interval of $-\alpha < \omega t < 0$

Due to the symmetry of the collector current waveshape we may say that

$$i_C(\omega t) = i_C(-\omega t)$$

$$i_C = \frac{I_{Bmax}}{\omega \tau_f} \cdot \frac{\sin(-\omega t + \alpha/2) + \omega t \cos \alpha/2 + \sin \alpha/2 - \alpha \cos \alpha/2}{1 - \cos \alpha/2}$$

in the interval of $0 < \omega t < \alpha$

Otherwise $i_C = 0$

2.11

To find the collector direct current, it is only necessary to average the collector current. Therefore,

$$I_{CO} = \frac{2I_{Bmax}}{2\pi\omega\tau_f} \int_{-\alpha}^{0} (\sin(\omega t + \alpha/2) - \omega t \cos \alpha/2 + \sin \alpha/2 - \alpha \cos \alpha/2) d\omega t$$

$$= \frac{I_{Bmax}}{\pi\omega\tau_f} \left[\frac{-\cos(\omega t + \alpha/2) - \left(\frac{\omega^2 \tau^2}{2}\right)\cos \alpha/2 + \omega t \sin \alpha/2 - \omega t \alpha \cos \alpha/2}{1 - \cos \alpha/2} \right]_{-\alpha}^{0}$$

$$I_{CO} = \frac{I_{Bmax}}{\pi\omega\tau_f} \cdot \frac{\alpha \cos \alpha/2 - \left(\alpha^2/2\right)\cos \alpha/2}{1 - \cos \alpha/2} \qquad 2.12$$

The collector current efficiency may be determined through the manipulation of Eqns. 2.9, 2.10 and 2.12.

$$\eta_{CI} = \frac{\dfrac{\cos(n\alpha + \alpha/2) - \cos \alpha/2}{n + 1} + \dfrac{\cos(n\alpha - \alpha/2) - \cos \alpha/2}{n - 1} + \dfrac{2\cos \alpha/2}{n}(1 - \cos n\alpha)}{2n(\alpha \sin \alpha/2 - \dfrac{\alpha^2}{2} \cos \alpha/2)} \qquad 2.13$$

This efficiency is plotted as a function of n and 2α in Fig. 2.12. A comparison may be made with efficiency calculations, obtained by Scott*, which are plotted in Fig. 2.13. In Fig. 2.14, the efficiencies are plotted for the partial sinusoidal model and compared with measured

---

*The calculations are extrapolations on Scott's amplifier analysis for application to frequency multipliers.

Figure 2.12

Partial sinusoid model
collector current efficiencies

Collector current efficiency in per cent

Collector conduction angle in degrees ·(2α).

Figure 2.13

Quartic collector current efficiencies.

Collector current efficiency in per cent

Collector conduction angle in degrees(2α),

Figure 2.14

Measured collector current effici-
encies compared with partial
sinusoid predictions. Crosses
represent values of an OC42
(f_{in}=2GHz, n=1to8). Circles,
squares, triangles
pepresent (n=1,2,3
respectively) values
of an AG4200 (f_{in}=
5GHz).

Collector current efficiency in per cent

Conduction angle in degrees (2α).

current efficiencies on two kinds of transistors. Agreement between the calculated and measured values is well within the accuracy of the instruments used. The "partial sinusoid" model is in closer agreement with the measured results than the "quartic" model. The circuit used for the measurements is shown in Fig. 2.5. The circuit measures the harmonic output without feedback and hence permits the measurement of the collector current efficiency. Thus the collector current efficiency has been calculated using Eqn. 2.5. This equation may be used to evaluate the ability of a transistor to convert direct power into radio frequency power.

A careful examination of Fig. 2.12 shows that the efficiency of any harmonic may be found with $n\alpha$ and one equation. That is if $\eta_{CI1} = f_1(\alpha)$ then $\eta_{CIn} = f_1(n\alpha)$, with an accuracy of about 0.1%. This is useful since we now require only one equation or graph to ·determine the current efficiency of any particular harmonic. If a multiplier is to have a practical collector conversion efficiency $n\alpha$ must be less than 360°. The single graph is shown in Fig. 2.15.

The foregoing analysis may be applied to an amplifier or a frequency multiplier in the common base configuration without any modification.

2.6   Input Power Requirements

In a power amplifier or a frequency multiplier the input power requirement is of prime interest. High efficiency amplifying or

Figure 2.15

Partial sinusoid model
collector current efficiency
for any harmonic (n).

Collector conduction angle in degrees (2nα).
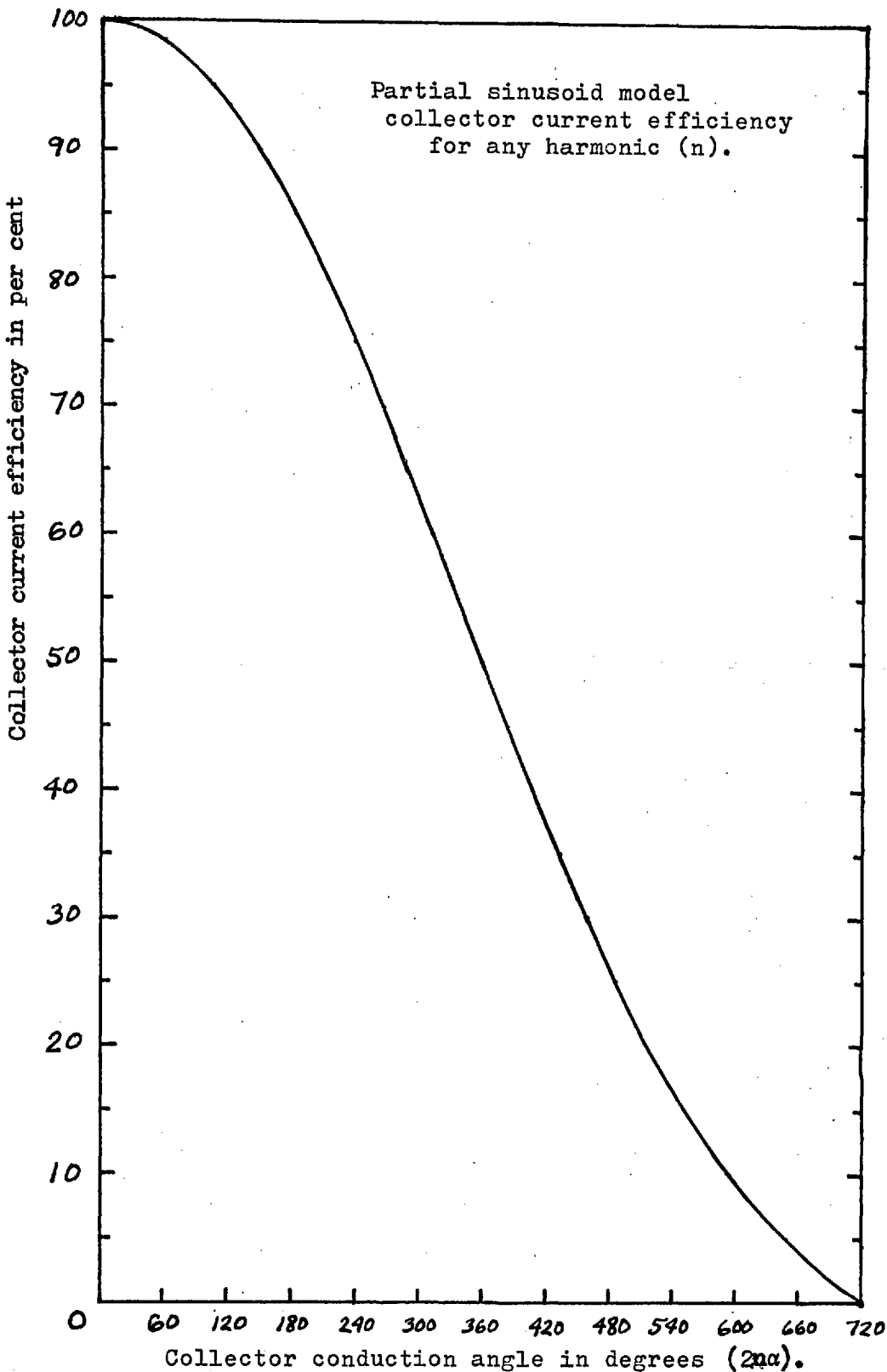
frequency multiplying can only be attained at the expense of increased
input power. The transistor input voltage and current waveforms are
already idealised and calculation of the input power is thus facilita-
ted. The input power requirement is calculated by multiplying the
input voltage with the fundamental input current and the appropriate
phase angle. This is somewhat different from assuming that all of the
input power is dissipated in the base resistance, as previous
analyses[11,12] have done.

$$P_{Bin} = \frac{-I_{B1}}{2} V_{B1} \cos(90 - \alpha/2) \qquad 2.14$$

From Figs. 2.6 and 2.9 it may be seen that,

$$V_{B1} = \frac{I_{Bmax} \; r_{bb}}{1 - \cos^{\alpha}/2} \qquad 2.15$$

Using Eqn. 2.9, with some manipulation, it may be shown that,

$$I_{B1} = \frac{I_{Bmax}}{\pi(1-\cos^{\alpha}/2)} \left(\frac{-\cos^3\alpha/2 + \cos^{\alpha}/2}{2} - \alpha \sin^{\alpha}/2 \right) \qquad 2.16$$

The input power of the multiplier or amplifier may now be
calculated through the manipulation of Eqns. 2.14, 2.15 and 2.16.

$$P_{Bin} = \frac{-I^2_{Bmax}}{(1-\cos^{\alpha}/2)^2} \times \frac{r_{bb}}{2\pi} \times \left(\frac{-\cos^3\alpha/2 + \cos^{\alpha}/2}{2} - \alpha \sin^{\alpha}/2 \right) \sin^{\alpha}/2 \qquad 2.17$$

The input power of Eqn. 2.17 is more usefully expressed in normalised
form; using Eqn. 2.17 and 2.9 we obtain;

$$P_{Bin} = \frac{I^2_{Bn} \; r_{bb}}{2} \times \frac{\pi \left(\frac{-\cos3\alpha/2 + \cos^{\alpha}/2}{2} - \alpha \sin^{\alpha}/2 \right) \sin^{\alpha}/2}{\left(\frac{\cos(n\alpha+\alpha/2)-\cos\alpha/2}{n+1} + \frac{\cos(n\alpha-\alpha/2)-\cos\alpha/2}{n-1} + \frac{2\cos\alpha/2}{n} (1-\cos n\alpha) \right)}$$

$$2.18$$

This expression is plotted in Fig. 2.16 as a function of conduction angle (2α) and of n. It may be noted that there is a very definite conduction angle at which the normalised input power may be minimised for each harmonic. The optimum conduction angle is approximately 360°/n. This value is obtained from examination of Fig. 2.16, and corresponds to a realistic collector efficiency of .50 for each harmonic. Fig. 2.16 permits the comparison of power amplifiers and multipliers that have the same output frequency. By maintaining a constant output frequency, identical output conditions and a constant current gain at the frequency of interest are maintained. The loss in gain, to obtain frequency multiplication for any practical conduction angle may be found in Fig. 2.16. The minimum loss in gain (with respect to that of a class A amplifier) is found to be a factor of (3.0n - 2.0). The input power must be increased by this amount, when the input frequency is decreased by a factor of n, to obtain the same output current magnitude. The output current determines the power output when the other output parameters (such as V_{CC} and R_L) are fixed. In a multiplier, the conduction angle may be decreased, from above, to improve the collector efficiency with an attendant decrease in gain. It is normally bad design to make the conduction angle larger, than that just recommended, since both the power gain and collector efficiency are degraded by doing so.

The curves of Fig. 2.16 have been verified by measuring the input power to a transistor. Figs. 2.17, 2.18 and 2.19 verify

Figure 2.16

Normalised input power requirement of an amplifier or a frequency multiplier

Input power normalised by $\dfrac{I_{Bn}^2 \, r_{bb}}{2.0}$

Collector conduction angle in degrees

Figure 2.17

Measured and calculated input power requirements of a transistor amplifier. Crosses refer to measurements on an OC42 at 2MHz. Circles refer to measurements on an AG200 at 5MHz.

Normalised input power

Collector conduction angle in degrees

Figure 2.18

Measured and calculated input power requirements of a transistor doubler (type AG200, f_{in} = 5MHz).

Normalised input power

Collector conduction angle in degrees

Figure 2.19

Normalised input power

Measured and calculated input power requirement of a transistor tripler. Measurements were made on an AC4200 at an input frequency of 5 MHz.

Collector conduction angle in degrees

experimentally input power requirements for an amplifier, a doubler, and a tripler respectively. The agreement is good although it appears that the assumed value of extrinsic base resistance was slightly large. In Fig. 2.17 the measured input power is lower than that predicted by theory for large conduction angles. However, for small conduction angles the measured input power is larger. The latter effect will be explained in the next chapter. Shown in Fig. 2.20 is the circuit

Figure 2.20

To a selective voltmeter
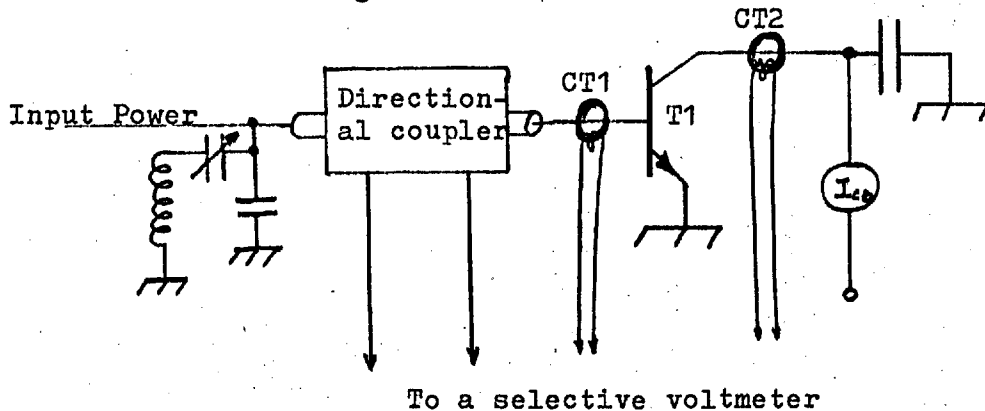
A setup for measuring the input power to a transistor amplifier
or multiplier. This method avoids losses in the input tuned
circuit. The selective voltmeter indicates the forward and
reverse power flow in the directional coupler and also the
harmonic current flow in the base and collector. The collector
is earthed to avoid capacitive feedback.

diagram of the measurement set-up. The input power to the transistor
is measured with a directional coupler. This method eliminates the
input tuned circuit losses which become significant over a large
part of the range of conduction angle.

2.7   Maximum Harmonic Current Flow

Frequently transistors have a very low emitter-base breakdown
potential. It is a serious limitation on transistor power amplifiers
and frequency multipliers where large reverse bias voltages are
necessary to obtain high efficiencies by small conduction angles. The

input voltage may be found using Eqn. 2.8 and adding the threshold

conduction voltage (V_{Bcon}) of the transistor input. Thus,

$$v_B = I_{Bmax} \, r_{bb} \left(\frac{\cos(wt + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right) + V_{Bcon} \qquad 2.19$$

The maximum reverse voltage of v_B is obtained when $wt = \pi - \alpha/2$.

$$BV_{EB} - V_{Bcon} = \frac{I_{Bmax} \, r_{bb}}{2} \times \left(\frac{-1 - \cos \alpha/2}{1 - \cos \alpha/2} \right)$$

Note that BV_{EB} and V_{Bcon} are always of opposite sign and hence are

normally added. Manipulation of the above equation and Eqn. 2.13 makes

it possible to obtain,

$$\frac{I_{Bn}(BV_{EB} - V_{Bcon})}{r_{bb}} = \frac{-0.5\pi(1 + \cos \alpha/2)}{\left[\frac{\cos(n\alpha + \alpha/2) - \cos \alpha/2}{n + 1} + \frac{\cos(n\alpha - \alpha/2) - \cos \alpha/2}{n - 1} + \frac{2\cos \alpha/2}{n} (1 - \cos n\alpha) \right]} \qquad 2.20$$

The equation is plotted in Fig. 2.21 as a function of n and of conduction

angle. Measurements have verified Fig. 2.21 to a high degree of

accuracy, although they are not shown. If the emitter reverse voltage

limitation is very serious, it may be desirable to choose a conduction

angle that provides the maximum possible harmonic current. For an

amplifier the best angle is $360°$ and for any harmonic the best conduction

angle is $512°/n$. This conduction angle is substantially greater than

the conduction angle that results in best gain and results in a

collector current efficiency of only 0.21. The limitation itself

is best avoided either by choosing a transistor with a large reverse

Figure 2.21

Maximum normalised collector harmonic current flow permitted
by the transistor input breakdown voltage.

I_{Cimax}

Collector conduction angle in degrees
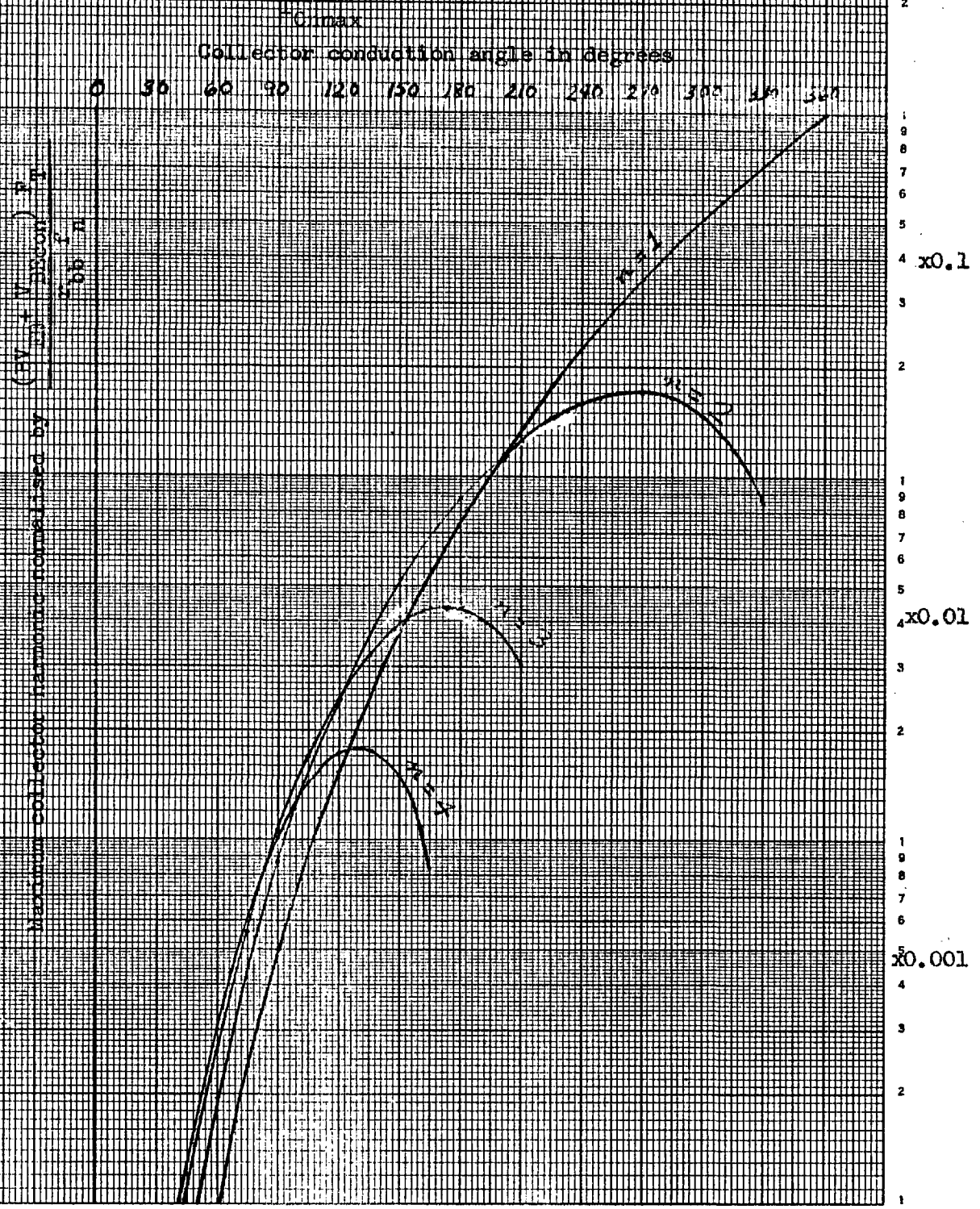
breakdown voltage or by using a low multiplication factor. It is

evident from Fig. 2.21 that the input reverse breakdown limitation is

most serious for the higher harmonics.

2.8   Peak Input and Output Currents

In order that a transistor power amplifier or frequency multi-

plier may be designed, it is necessary to determine the peak collector

and peak base currents. The peak collector current may be determined

by evaluating Eqn. 2.11 when $\omega t = 0$.

We have,

$$I_{Cmax} = \frac{I_{Bmax}}{\omega\tau_f(1-\cos\alpha/2)} (2\sin\alpha/2 - \alpha\cos\alpha/2) \qquad 2.21$$

I_{Cmax} is most useful if it is normalised to the direct collector current.

Hence, using Eqn. 2.12 we have,

$$\frac{I_{Cmax}}{I_{CO}} = \frac{2\sin\alpha/2 - \alpha\cos\alpha/2}{\pi(\alpha\sin\alpha/2 - \alpha^2/2\cos\alpha/2)} \qquad 2.22$$

This equation is displayed in Fig. 2.22.

Now to determine the relationship between the peak base current

and the collector current, Eqn. 2.12 must be examined.

$$\frac{I_{Bmax}}{I_{CO}\omega\tau_f} = \frac{(1-\cos\alpha/2)}{\alpha\sin\alpha/2 - \alpha^2/2\cos\alpha/2} \qquad 2.23$$

This relationship is also presented in Fig. 2.22.

It is useful to determine the biasing voltage necessary to

obtain a certain desired conduction angle by finding the voltage at

which the transistor is turned on. Substituting $\omega t = 90 - \alpha/2$ into

Figure 2.22

Maximum base and maximum collector currents normalised to the direct collector current.

$$\frac{I_{Bmax}}{I_{co}} \cdot \frac{F_T}{f_h}$$

$$\frac{I_{cmax}}{I_{co}}$$

normalised maximum currents

collector conduction angle in degrees
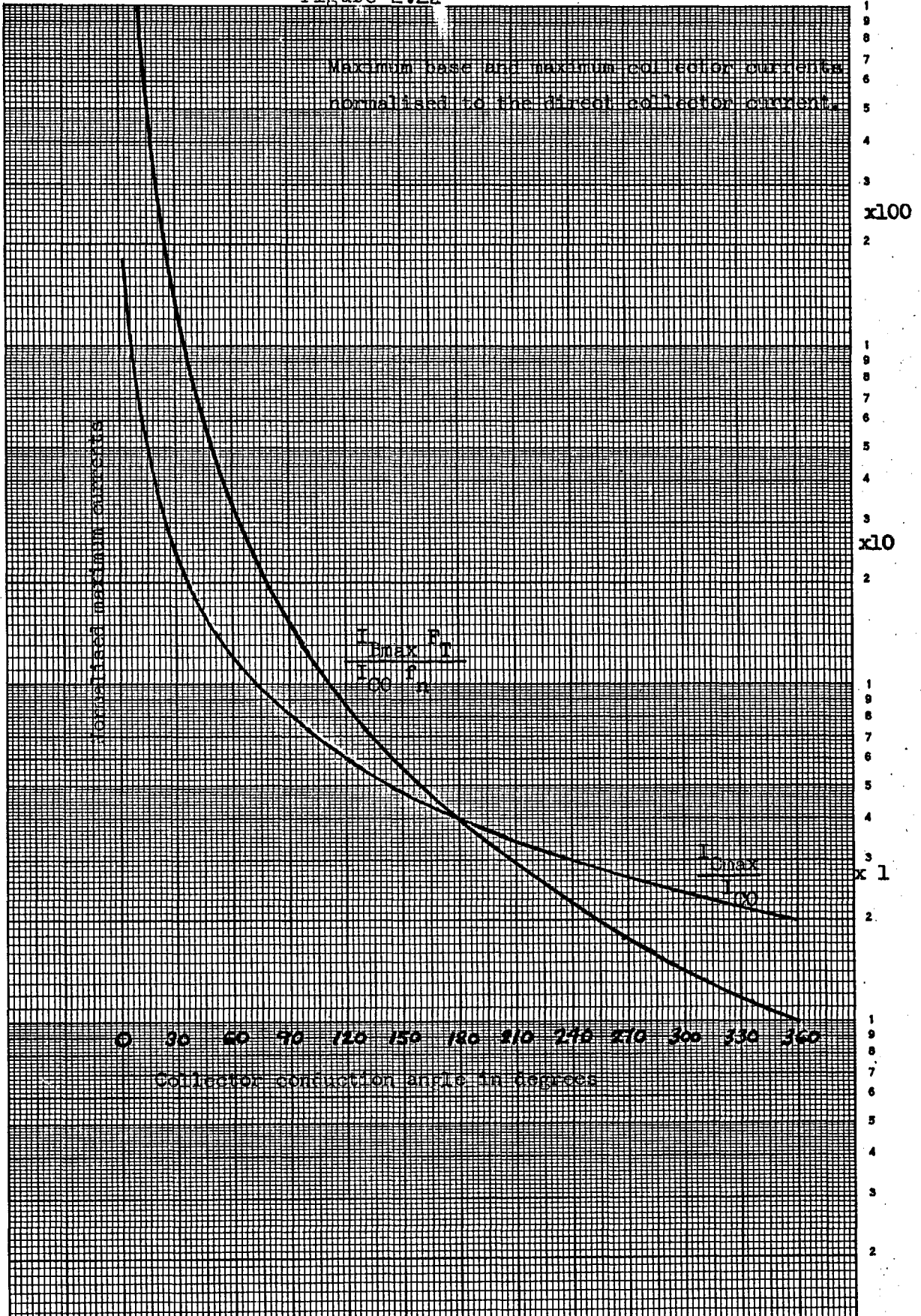
Eqn. 2.19, we have,

$$V_{BO} = I_{Bmax} \, r_{bb} \left(\frac{-\cos^{\alpha}/2}{1-\cos^{\alpha}/2} \right) + V_{Bcon} \qquad\qquad 2.24$$

The input tuned circuit can be designed most effectively after the input impedance of the transistor is determined from the input power and the input voltage (Eqn. 2.15).

$$V_{B1} = \frac{I_{Bmax} \, r_{bb}}{1-\cos^{\alpha}/2}$$

$$\text{Real } Y_{in} = \frac{2P_{Bin}}{V^2_{B1}} \qquad\qquad 2.25$$

2.9 Concluding Comments

In the foregoing chapter theory has been developed, neglecting the effect of depletion layer capacitance currents. Such an approximation for frequencies much lower than F_T and the above theory could be used for many applications at frequencies greater than f_β but much lower than F_T.

The effects of the depletion layer capacitances are treated in the next chapter allowing the theory to be applied up to frequencies of about f_{max}. A design example will be given in the next chapter to illustrate a design method. The above theory will be incorporated into this method.

CHAPTER   THREE

Effects of Transistor Strays on Nonlinear Input Operation

of Multipliers and Amplifiers and Design Methods

3.1   Complete Equivalent Circuit and Simplifications

The basic frequency multiplying and power amplifying character-
istics of the intrinsic transistor (in common emitter configuration
with sinusoidally applied input and output voltages) has been analysed
in Chapter Two.   In that analysis the extrinsic base resistance (r_{bb})
was taken into account in conjunction with the intrinsic base.   This
was most expedient because the limitations caused by r_{bb} are of a very
fundamental nature.

In Chapter Two it was found that current flow in the two depletion
layer capacitances of the transistor were sometimes quite appreciable.
The chief effect of these, if they are small, is only to obscure the
intrinsic base behaviour.   However, if these currents are large, there
is a degradation of the multiplier or amplifier performance.

In this chapter the most significant extrinsic electrical character-
istics of the transistor are investigated, the serious ones are determined
and their effects are analysed.   Some strays cause the transistor cur-
rent and voltage waveforms to deviate from the theoretical ones without
degrading the performance while others degrade the performance, as well.
The latter strays will receive the most attention since the performance

of the resultant transistor circuit is of most interest.

All transistors are electrically distributed devices but can be approximated, with respect to electrical performance, by a network of lumped elements. It is useful to examine a comprehensive equivalent circuit before one is chosen for analysis here. The equivalent circuit shown in Figure 3.1 is much more involved than is necessary for most

Figure 3.1
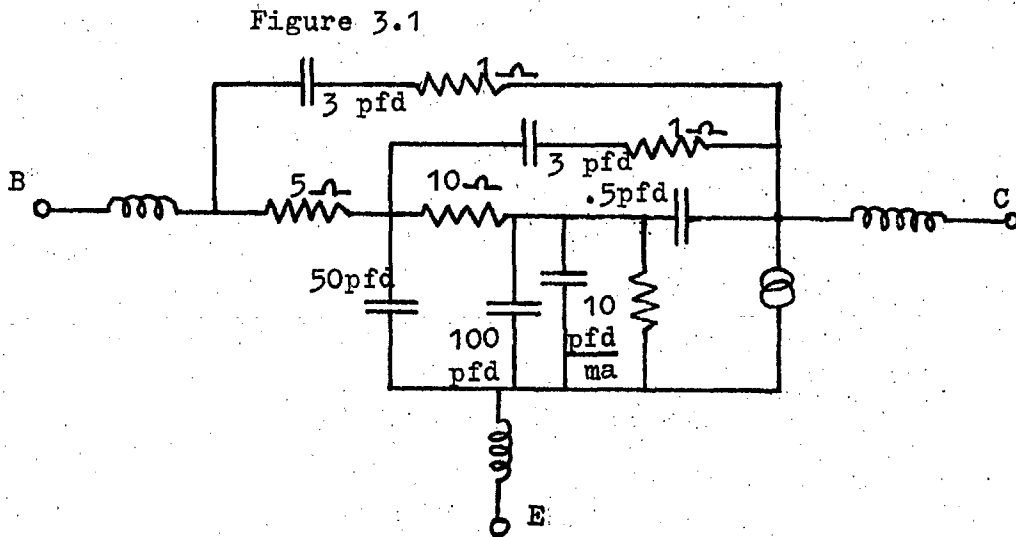
An equivalent circuit of a 2N3375. This transistor will produce 5 watts at 400 MHz as an amplifier. The circuit was derived by A.P. Anderson[22]. The transistor is of a planar construction with 156 separate emitters diffused into a common base and collector structure, permitting high frequency, high power operation.

applications. Normally, strays such as depletion layer capacitances and lead inductances become important in a planar transistor operating at a high frequency and high power. Many of the "strays" depicted in Figure 3.1 will become insignificant if, for example, a low frequency

alloy transistor is examined.

In almost all transistors the base resistance is distributed with capacitive loading from the emitter and collector depletion layers. For a practical circuit it is very difficult to carry out an analysis if the extrinsic base resistance is represented by more than one lump. In transistor data sheets one is fortunate to obtain an equivalent resistance value for a single lump representation (let alone more than one). Further lumping would complicate the analysis and increase difficulty in practical application. The equivalent circuit of Figure 3.1 is simplified by reducing the base resistance to a single lump. An input diode indicates[23] charge storage in the intrinsic base. We then obtain the circuit shown in Figure 3.2. The charge storage characteristic of the

Figure 3.2
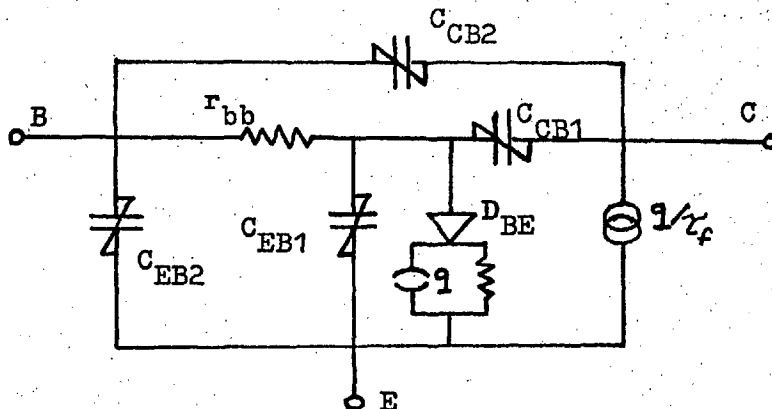
Simplified equivalent circuit of a transistor. The charge storage characteristics of the intrinsic base (D_{be}) is defined in Chapter Two.

intrinsic base (D_{BE}) is assumed to behave according to the "partial sinusoid" idealisation made in Chapter Two. The equivalent circuit

is still quite involved but further reduction is possible. The two

capacitances C_{BE2} and C_{BC2} are completely accessible, electrically.

We are dealing with narrow-band amplifiers and multipliers, and there-

fore the two capacitances may be "tuned out" by external inductances at

the fundamental or harmonic frequencies of interest. The external in-

ductances required for this neutralisation in practice, cause some loss

but for analytical purposes the loss is neglected. The effect of the

other two depletion layer capacitances, C_{BE1} and C_{BC1}, must be con-

sidered separately if a tractable analysis is to result. The simpli-

fying assumption, that the effects of the two capacitances are additive,

is made.

3.2 Effect of Input Depletion Layer Capacitance

In evaluating the effect of the input depletion layer capacitance

C_{BE1}, the amplifier and multiplier operating assumptions, of sinusoidal

input and output voltages and the partial sinusoid recovery of the base,

are maintained. The effect of the depletion layer capacitance is

treated as a small deviation from the previous theory. The circuit of

Figure 3.3 forms the basis of the analysis.

The input capacitance C_{BE1} is nonlinear but for simplicity in

analysis it is assumed linear and in the analysis some further approx-

imations are adopted. First, it is assumed that the effect of the

capacitance is small, and the degradation of performance in regard to

the power input requirement is calculated on this basis; the capacit-

ance is then allowed to become large with the realisation that the analysis

Figure 3.3
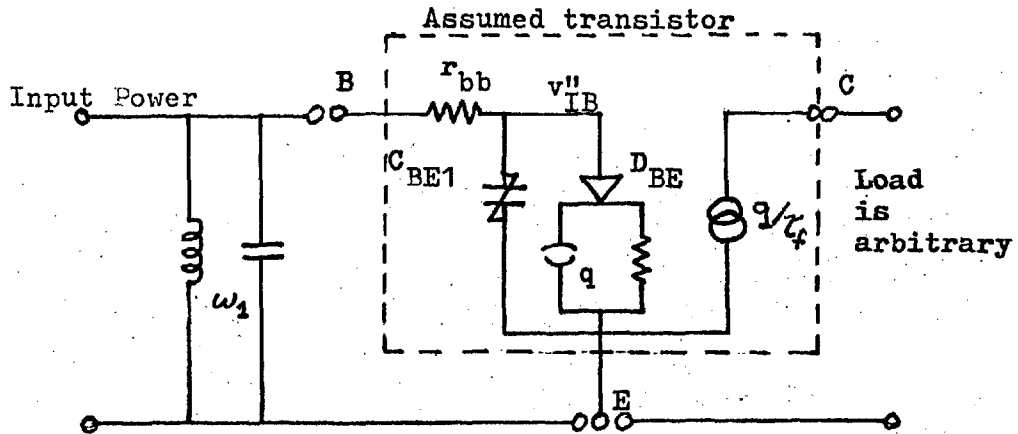
Assumed equivalent circuit to evaluate effect of input depletion layer capacitance.

is approximate for this latter situation. The analysis is approached by calculating the voltage (v_{IB}'' in Figure 3.3) excursions across the capacitance and then deducing the current flow through the capacitance C_{BE1} as a result of the voltage excursions. The power dissipation in the base resistance due to this current flow is then calculated. This method neglects the modification of the voltage (v_{IB}'') due to the capacitance (C_{BE1}) current flow through the base resistance. This is likely to be justifiable as long as $0.1 > r_{bb}\omega C_{BE1}$. It is assumed that the extrinsic base current (i_D) and the input voltage (v_B) are not modified by this capacitance current flow and these last two assumptions are in fact, verified to be well founded.

The input voltages that develop and cause the voltage variation on the input capacitance C_{BE1} are shown in Figure 3.4.

$$v_B = i_B r_{bb} + v''_{IB} \qquad (3.1)$$

where v_B and v''_{IB} are illustrated in Figures 3.3 and 3.4. i_D is

Figure 3.4
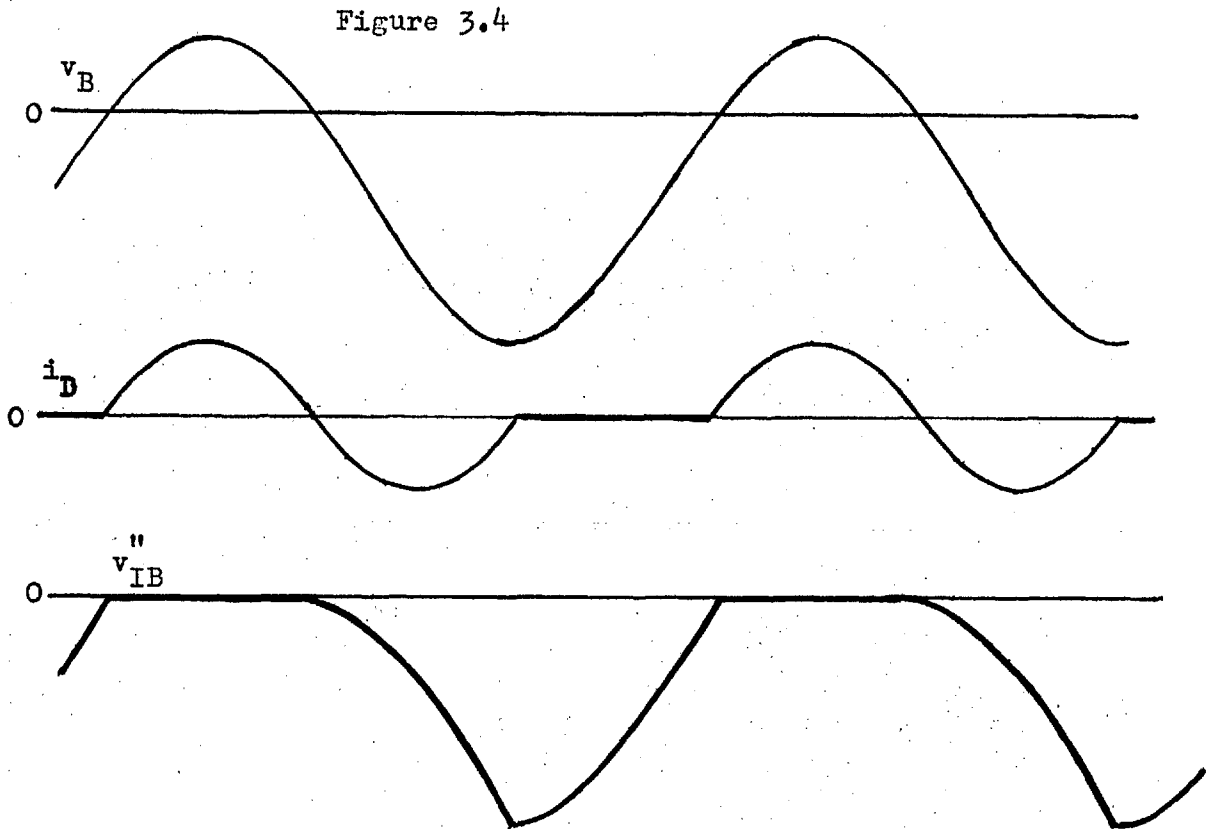
The voltage drop across the extrinsic base resistance is subtracted from the input voltage to obtain the intrinsic base voltage.

the base charging current as defined by the "partial sinusoid" assumption of Chapter Two. We may find the fundamental input voltage (without the direct voltage term) from Eqn. 2.19.

$$v_B = r_{bb} I_{B_{max}} \left(\frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right)$$

From Figure 3.4, we may see that,

$$v_{IB}'' = 0$$

in the interval of $-\alpha < \omega t < 0$

$$(3.2)$$

Now we must find v_{IB}'' in the interval of $0 < \omega t < \alpha$

From Eqn. 2.8

$$i_D = I_{B_{max}} \left(\frac{-\cos(\omega t - \alpha/2) + \cos \alpha/2}{1 - \cos \alpha/2} \right)$$

Substituting this equation and v_B into Eqn. 3.1 we write,

$$v_{IB}'' = r_{bb} I_{B_{max}} \left[\frac{\cos(\omega t + \alpha/2) + \cos(\omega t - \alpha/2) - 2 \cos \alpha/2}{1 - \cos \alpha/2} \right]$$

in the interval of $0 < \omega t < \alpha$

$$(3.3)$$

Now in the interval of $-\alpha > \omega t$ and $\omega t > \alpha$ the base current is essentially zero (the current in the depletion layer capacitance is assumed to be negligibly small for this) and therefore,

$$v_{IB}'' = v_B$$

$$-\alpha > \omega t \quad \text{and} \quad \omega t > \alpha$$

$$(3.4)$$

The voltage swing (v_{IB}'') across the input depletion layer capacitance implies that a current flows into this capacitance. This current flows through the extrinsic base resistance (r_{bb}) causing a power loss which must be calculated. The additional current that flows into this capac-

itance will be called i_B'' and

$$i_B'' = \frac{d \, v_{IB}'' \, C_{BE1}}{dt}$$

$$= C_{BE1} \frac{d \, v_{IB}''}{dt}$$

since C_{BE1} is assumed to be linear.

Now i_B'' is specified over three different time intervals as designated by a subscript notation (i.e. i_{B1}'', i_{B2}'' and i_{B3}''). For the interval $-\alpha < \omega t < 0$ we find that $i_{B1}'' = 0$ by differentiating Eqn. 3.2. For the interval $0 < \omega t < \alpha$ we find i_{B2}'' by differentiating Eqn. 3.3,

$$i_{B2}'' = C_{BE1} r_{bb} I_{B_{max}} \left[\frac{-\omega \sin(\omega t + \alpha/2) - \omega \sin(\omega t - \alpha/2)}{1 - \cos \alpha/2} \right]$$

And for the interval of $\omega t < -\alpha$ and $\omega t > \alpha$ we find i_{B3}'' by differentiating Eqn. 3.4 (or Eqn. 2.19),

$$i_{B3}'' = C_{BE1} r_{bb} I_{B_{max}} \left(\frac{-\omega \sin(\omega t + \alpha/2)}{1 - \cos \alpha/2} \right)$$

Thus, the input base-emitter depletion layer capacitive current flow has been calculated and we are now in a position to calculate the additional input power requirement due to the flow of this current through the base resistance (r_{bb}). The additional power input requirement to the transistor (P_{BinDeg}) due to the input capacitance C_{BE1} may now be calculated in the following way.

$$P_{BinDeg} = r_{bb} \times i_B''^2$$

Now since i_B'' is not a continuously sinusoidal current we must determine the root mean square value of the input currents i_{B1}'', i_{B2}'' and i_{B3}''.

$$P_{BinDeg} = \left(\frac{\omega\, C_{BE1}\, r_{bb}\, I_{B_{max}}}{1 - \cos \alpha/2}\right)^2 \times \frac{r_{bb}}{2\pi} \times$$

$$\left\{\int_0^\alpha \left[\sin^2(\omega t + \alpha/2) + 2\sin(\omega t + \alpha/2)\sin(\omega t - \alpha/2) + \sin^2(\omega t - \alpha/2)\right] d\omega t \right.$$

$$\left. + \int_\alpha^\pi \sin^2(\omega t + \alpha/2) d\omega t + \int_{-\pi}^\alpha \sin^2(\omega t + \alpha/2) d\omega t\right\} \qquad (3.5)$$

$$P_{BinDeg} = \left(\frac{\omega\, C_{BE1}\, r_{bb}\, I_{B_{max}}}{1 - \cos \alpha/2}\right)^2 \times \frac{r_{bb}}{2\pi} \left\{\left[\frac{\omega t}{2} - \frac{\sin(2\omega t + \alpha)}{4} + \omega t \cos \alpha \right.\right.$$

$$\left. - \frac{\sin 2\omega t}{2} + \frac{\omega t}{2} - \frac{\sin(2\omega t - \alpha)}{4}\right]_0^\alpha + \left[\frac{\omega t}{2} - \frac{\sin(2\omega t + \alpha)}{4}\right]_\alpha^\pi$$

$$\left. + \left[\frac{\omega t}{2} - \frac{\sin(2\omega t + \alpha)}{4}\right]_{-\pi}^\alpha\right\}$$

$$P_{BinDeg} = (\omega C_{BE1}\, r_{bb})^2 \left(\frac{I_{B_{max}}}{1 - \cos \alpha/2}\right)^2 \frac{r_{bb}}{2\pi} \left\{\pi + \alpha \cos \alpha - \frac{\sin 2\alpha}{2}\right\}$$

The power P_{BinDeg} is most useful if it is specified in terms of P_{Bin} from Chapter Two. A degradation factor may be evaluated using the following equation as a basis.

$$F_{PDeg} = \frac{P_{BinDeg} + P_{Bin}}{P_{Bin}} \qquad (3.6)$$

Substituting in P_{BinDeg} from above and Eqn. 2.18 into Eqn. 3.6, we have,

$$F_{PDeg} = 1 + \omega^2 C_{BE1}^2 r_{bb}^2 \left(\frac{2\pi + 2\alpha \cos \alpha - \sin 2\alpha}{(\cos 3\alpha/2 - \cos \alpha/2 + 2\alpha \sin \alpha/2)\sin \alpha/2} \right)$$

.... (3.7)

This equation is somewhat unweildy but has been determined for a range of values of $(\omega C_{BE1} r_{bb})^2$ and of conduction angle (2α). These values are displayed graphically in Figure 3.5. It will be noted that this input power degradation is most serious for the smaller conduction angles. The effect, thus, discriminates against the efficient generation of the higher harmonics where small conduction angles are essential.

The exact verification of the theory of input power degradation is difficult. The effect is a modification of an approximated transistor behaviour and the original idealisation and analysis must be accurate. Also, the degradation only becomes marked if the conduction angles are small and small conduction angles are difficult to measure accurately. The method used to measure degradation proceeds as follows. A directional coupler (as illustrated in Figure 2.20) in an amplifier circuit is used to measure the forward and reflected power at the transistor input. The difference between these two quantities is a measure of the power delivered to the transistor input. The conduction angle is varied so that a series of input powers are obtained. These conform approximately to Figure 2.16 after the input power is normalised with respect to fundamental output current and with the choice of an approximate

Figure 3.5

Input power degradation factor due to input depletion layer conduction.
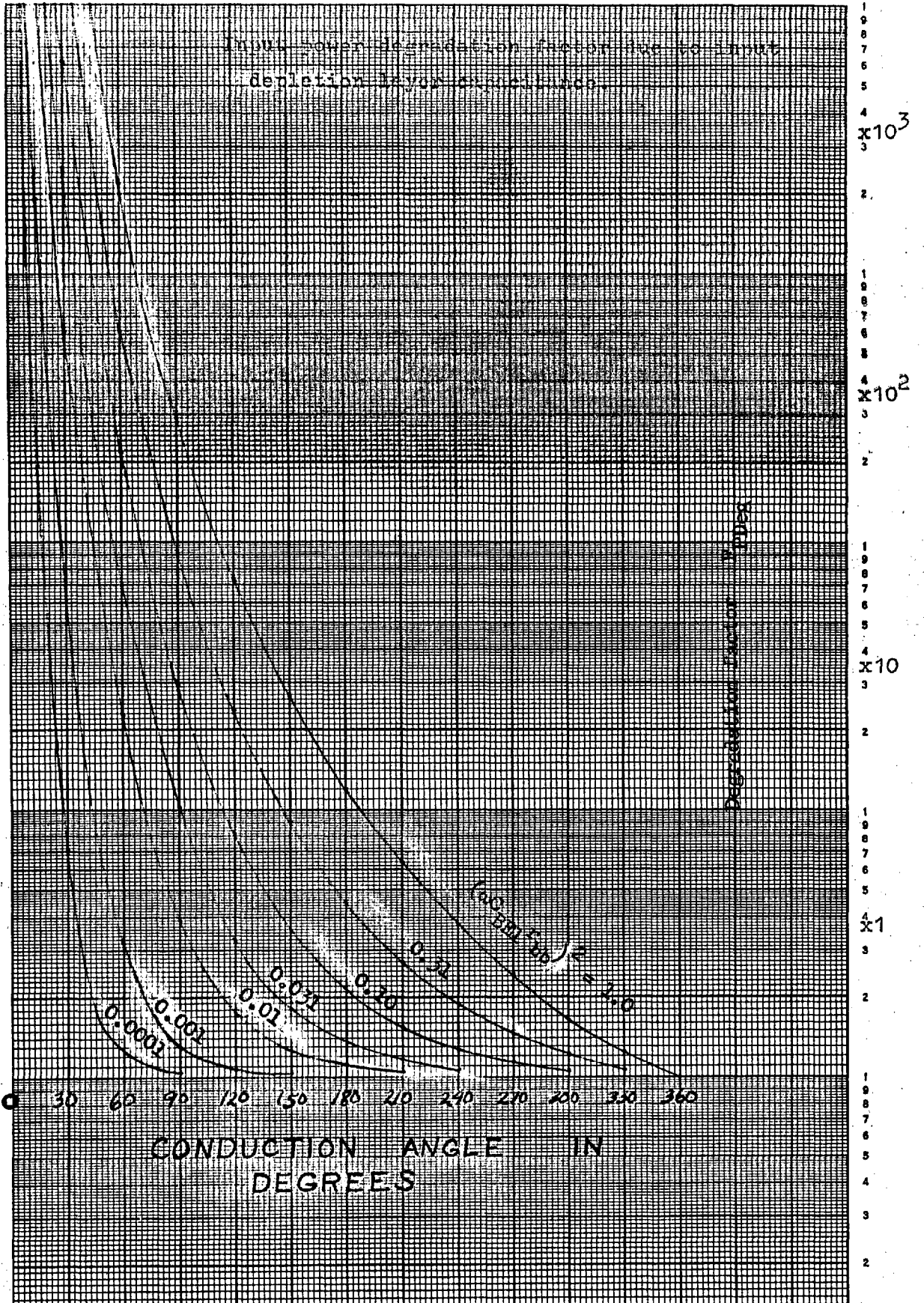
"adjusted" value of extrinsic base resistance (r_{bb} is adjusted so that
the normalised value of the input power is unity when the conduction
angle is $360°$). The measured and normalised input power is then
divided by the calculated "strayless" input power requirement. In this
way a measured degradation factor is obtained. This measurement and
normalisation was done with a transistor, type AG4200 (similar to a
2N1613) at two different frequencies, 5.0 MHz and 10.0 MHz. The
measured degradation factors for the power input are shown in Figure 3.6.

Measured degradation factor caused by the input depletion
layer capacitance at two frequencies, 5 MHz (o noses) and
10 MHz (x noses).
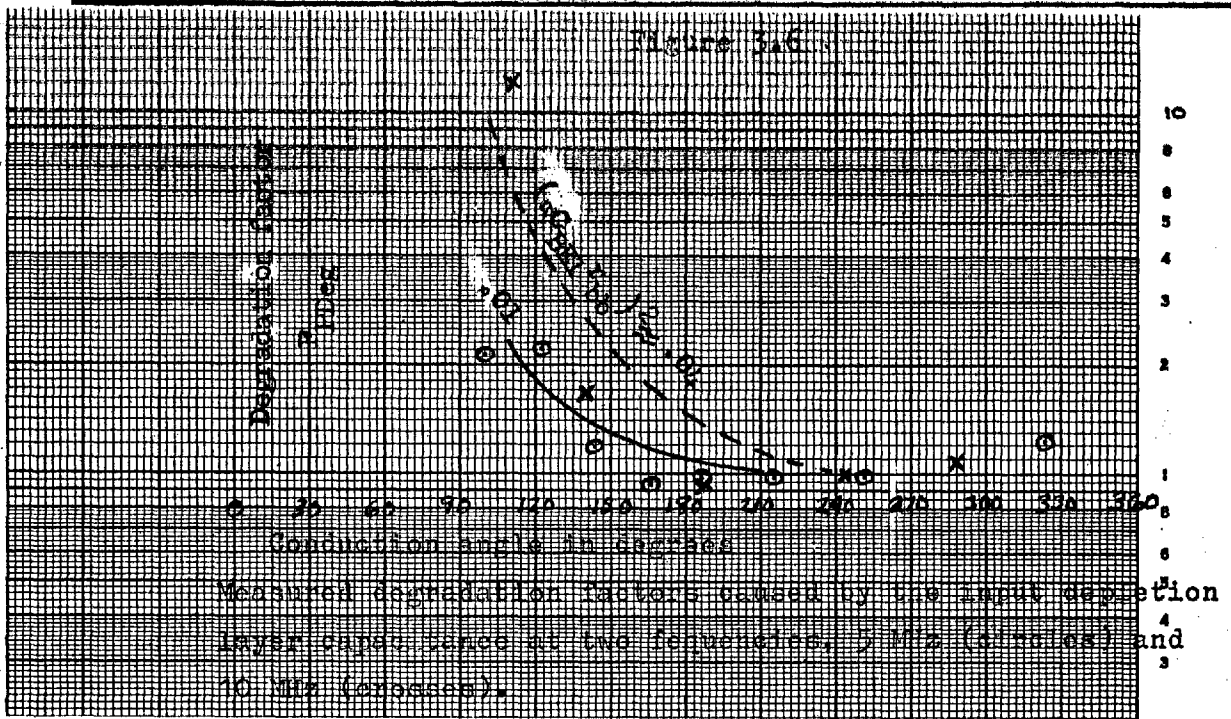
These measurements are fairly consistent with the theory and indicate
that the $r_{bb} C_{BE1}$ product for this particular transistor is about
3.18×10^{-9} sec. The product of the measured r_{bb} and total input
depletion layer capacitance $(C_{BE1} + C_{BE2})$ is 5.2×10^{-9} sec. Thus
for our purposes 60% of the total base-emitter depletion layer capacit-

ance appears to be buried underneath the extrinsic base resistance r_{bb}. Under most circumstances it is not feasible to measure the ratio of $C_{BE1}/(C_{BE1} + C_{BE2})$ and this can only be estimated. It will normally be larger than 30% and less than 80% for a planar transistor. For alloy transistors these percentages will probably range from 50% to 90%.

The effect of input power degradation due to the emitter-base depletion layer capacitance can be serious. However, since the relevant transistor characteristics are not included in manufacture's data sheets and are difficult to measure, the application of the foregoing theory is likely to be approximate.

3.3   Analysis of Effect of Collector Depletion Layer Capacitance

In the transistor the maximum frequency of usefulness (f_{max}) is limited by the joint effect of r_{bb} and the collector-base depletion layer capacitance. This maximum frequency is determined approximately by the following equation[24].

$$f_{max} = (\frac{F_T}{8\pi \, r_{bb} \, C_{BE1}})^{\frac{1}{2}} \qquad (3.8)$$

The feedback capacitance, in conjunction with the transistor forward current gain characteristic, causes a low output resistance (50-500 Ω) to appear across the collector-emitter leads. See Reference 25. A constant output resistance R_o is predicted, but in practice the measured resistance falls with increasing frequency. The falling

resistance is caused by the series collector resistance r_{cc}. This resistance has least effect at the low frequencies, and therefore the low frequency value of R_o will be used in calculations. The feedback capacitance limits the maximum frequency of usefulness of the transistor in a very fundamental way, and therefore must be accounted for in the analysis of high frequency amplifiers or frequency multipliers. The circuit shown in Figure 3.7 uses the transistor idealisation of Figure 3.2 in modified form.

Figure 3.7
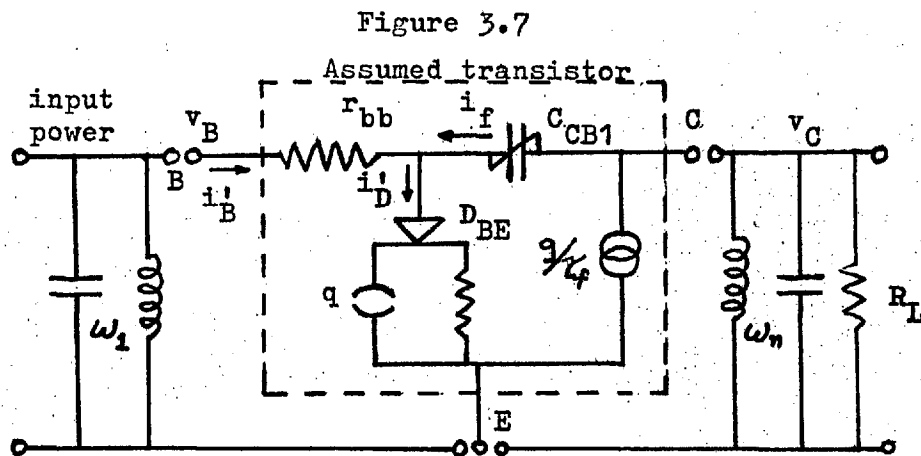
Assumed transistor equivalent circuit and embedding circuit for finding the effect of the transistor feedback capacitance.

In the following analysis, for simplicity, it is necessary to assume that: the current gain of the transistor does not have an excess phase shift term, the feedback capacitance (C_{BC1}) is linear, the base-emitter depletion layer capacitance is small and the input diode (D_{BE}) recovers according to the "partial sinusoid model" developed in Chapter

Two. The operation of the amplifier with feedback is best understood by examining the current and voltage waveforms, throughout the transistor, illustrated in Figure 3.8. The input voltage v_B is unchanged by feedback and initiates the sequence of events. It is biased so that a conduction angle of 2α is established. Assume for the moment that the partial sinusoid current (of Chapter Two) flows into the base. This sets up the usual collector current and voltage. The collector voltage causes a feedback current (i_f) in the collector capacitance (C_{BC1}) to flow. A new intrinsic base (i_D') current results from the simple addition of i_B and i_f (the sum of these two currents causes a new conduction angle of $2\alpha'$ to arise). The modified collector current i_C' may then be determined in terms of the intrinsic base current i_D'. It is worth noting the necessity of the assumptions made. We have assumed that the base-emitter input diode (D_{BE}) is discharged with the same waveshape that it is charged. This has proven to be a realistic assumption and it results in a symmetrical collector output current which simplifies the analysis since the collector phase angle of any harmonic current is zero. The assumption of a linear feedback capacitance C_{BC1} is desirable since this is usually an adequate approximation and the nonlinearity and the operating ranges of the collector voltage on the capacitance are extremely variable. The assumption that the transistor current gain excess phase shift[26] term is zero is justified because this is approximately true and the complication of the analysis that would result from the specification of different values of excess phase shift would lead to

Figure 3.8

input voltage v_B

input current
without feedback

i_B

$-\alpha$ $+\alpha$

0 —————→ wt ————→

collector
voltage v_C

feedback current
i_f

modified base current

i_D'

$-\alpha'$ $+\alpha'$
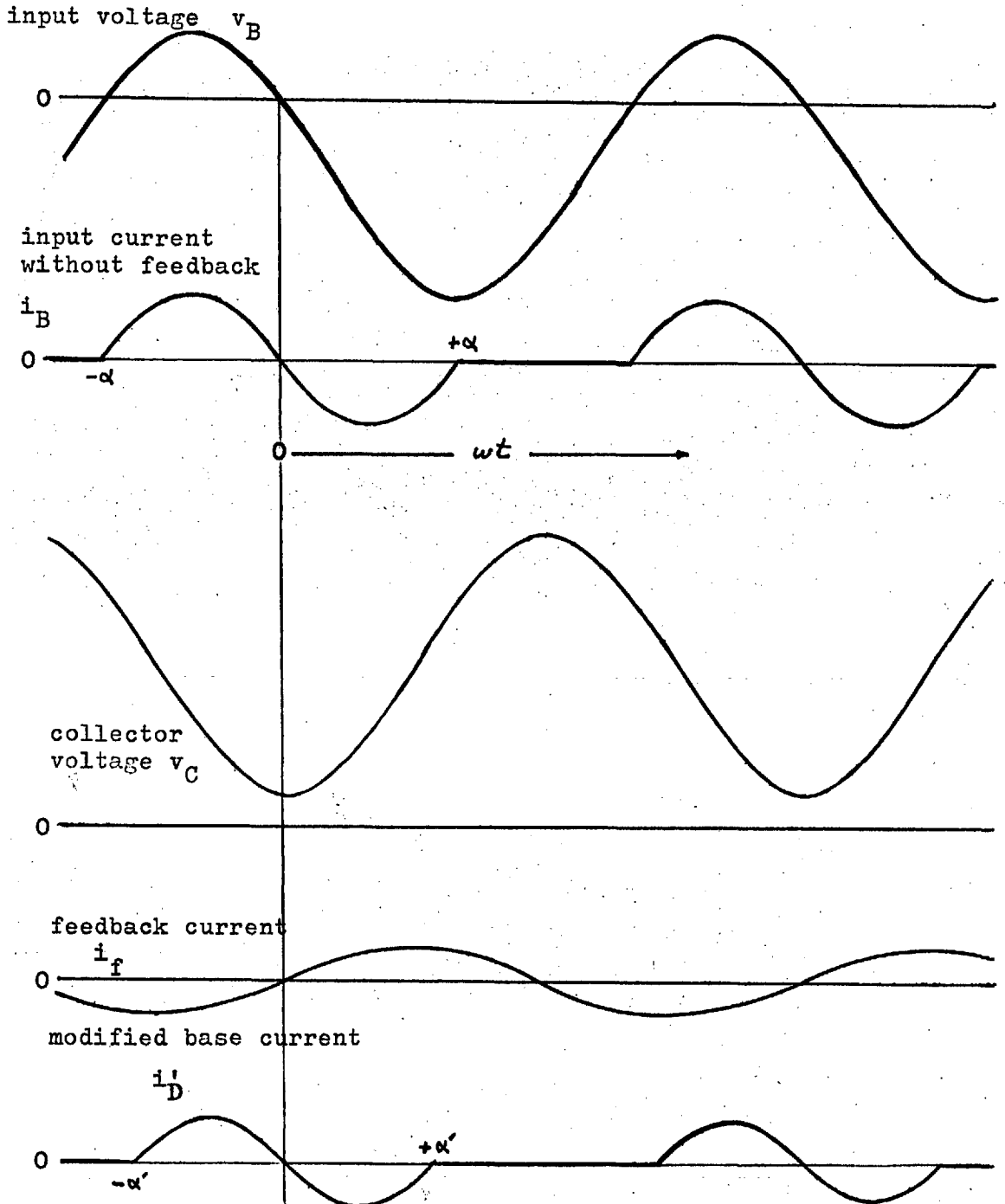
Assumed transistor voltage and current waveforms caused
by capacitive feedback. The collector voltage causes the feedback
current which reduces the magnitude and period of the intrinsic
base current (i_D').

no significant improvement in the accuracy of the analysis.

3.3.1 Analysis of transistor performance with capacitive feedback.

The waveforms assumed for the amplifier and multiplier in Figure 3.8 may be analysed to determine the input power requirement and the collector efficiency of the amplifier or multiplier under a wide range of operating conditions. The analysis begins with an examination of the current input to the base-emitter diode (D_{BE}). As indicated in Figure 3.8 the current i_D' is the sum of the input current of the strayless amplifier and the current (i_f) through C_{BC1}. That is, using Eqn. 2.8

$$i_D' = I_{B_{max}} \left(\frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right) + i_f$$

in the interval of $-\alpha' < \omega t < 0$

$$i_f = \frac{d \, C_{BC1} \, v_C}{dt}$$

and from inspection of Figure 3.8

$$v_C = - V_{Cn} \cos n\omega t + V_{CC} \tag{3.9}$$

$$i_f = n\omega C_{BC1} V_{Cn} \sin n\omega t \tag{3.10}$$

and

$$i_D' = I_{B_{max}} \left(\frac{\cos(\omega t + \alpha/2) - \cos \alpha/2}{1 - \cos \alpha/2} \right) + n\omega C_{BC1} V_{Cn} \sin n\omega t$$

in the interval of $-\alpha' < \omega t < 0$

$$i'_D = I_{B_{max}} \left(\frac{\cos(\omega t - \alpha/2) + \cos \alpha/2}{1 - \cos \alpha/2} \right) + n\omega C_{BC1} V_{Cn} \sin n\omega t$$

in the interval of $\quad 0 < \omega t < \alpha'$

$$i'_D = 0$$

when $\quad \alpha' < \omega t \quad$ and $\quad \omega t < -\alpha'$

Equation 2.15 may be substituted into Eqn. 3.11 with the following result:

$$i'_D = \frac{V_{B1}}{r_{bb}} \left(\cos(\omega t - \alpha/2) + \cos \alpha/2 + \epsilon n \sin n\omega t \right)$$

where

$$\epsilon = \frac{r_{bb} \, \omega \, C_{BC1} \, V_{Cn}}{V_{B1}} \qquad (3.12)$$

It is now relevant to determine the new conduction angle $2\alpha'$ caused by the effect of the feedback capacitance. It will be noted in Figure 3.8 that i'_D begins to flow when the sum of i_B and i_f is greater than zero. We may find $2\alpha'$ from Eqn. 3.11 when i'_D leaves the zero axis. That is

$$0 = \frac{V_{B1}}{r_{bb}} \left[\cos(\alpha' - \alpha/2) + \cos \alpha/2 + \epsilon n \sin n\alpha' \right]$$

$$-\epsilon n \sin n\alpha' = \cos(\alpha' - \alpha/2) + \cos \alpha/2 \qquad (3.13)$$

This may be taken as a definition of α'. If ϵ is small then $\alpha' \approx \alpha$.

Having determined the time at which the conduction period begins

and arrived at a definition of input current, we may, with the charge control relations described in Eqn. 2.7, determine the collector current pulse shape. This is

$$i'_C = \frac{1}{\omega\tau_f} \int_{-\alpha'}^{\omega t} \frac{V_{B1}}{r_{bb}} \left(\cos(\omega t + \alpha/2) - \cos\alpha/2 + \epsilon\, n \sin n\, \omega t\right) d\omega t$$

Thus in the interval of $\quad -\alpha' < \omega t < 0$

$$i'_C = \frac{V_{B1}}{r_{bb}} \times \frac{1}{\omega\tau_f} \left[\sin(\omega t + \alpha/2) - \omega t \cos\alpha/2 - \epsilon \cos n\omega t \right]_{-\alpha'}^{\omega t}$$

$$= \frac{V_{B1}}{r_{bb}\omega\tau_f} \left\{ \sin(\omega t + \alpha/2) - \omega t \cos\alpha/2 - \epsilon \cos n\omega t + K_a + \epsilon K_b \right\}$$

$$\ldots\ldots\ldots (3.14)$$

where $\qquad K_a = -\sin(-\alpha' + \alpha/2) - \alpha' \cos\alpha/2$

$$K_b = \cos(-n\alpha')$$

Only one half of the collector current pulse shape need be determined since the pulse is symmetrical. Having determined the output current pulse it is now relevant to determine the harmonic current components.

$$I'_{Cn} = \frac{2}{\pi} \int_{-\alpha'}^{0} \frac{V_{B1}}{r_{bb}\omega\tau_f} \left[\sin(\omega t + \alpha/2) - \omega t \cos\alpha/2 - \epsilon \cos n\omega t \right.$$

$$\left. + (K_a + K_b \epsilon) \right] \cos n\omega t \, d\omega t$$

$$I'_{Cn} = \frac{V_{B1}}{r_{bb}\omega\tau_f} \times \frac{2}{\pi} \left[-\frac{\cos((n+1)\omega t + \alpha/2)}{2(n+1)} - \frac{\cos((1-n)\omega t + \alpha/2)}{2(1-n)} \right.$$

$$- \cos \alpha/2 \left(\frac{\omega t}{n} \sin n\omega t + \frac{\cos n\omega t}{n^2}\right) - \epsilon\left(\frac{\omega t}{2} + \frac{\sin 2n\omega t}{4n}\right)$$

$$\left. + (K_a + \epsilon K_b) \frac{\sin n\omega t}{n} \right]_{-\alpha'}^{0}$$

$$I'_{Cn} = \frac{V_{B1}}{r_{bb}\omega\tau_f} \times \frac{2}{\pi} \left\{ \frac{\cos(-n\alpha' - \alpha' + \alpha/2) - \cos \alpha/2}{2(n+1)} \right.$$

$$- \frac{\cos(n\alpha' - \alpha' + \alpha/2) - \cos \alpha/2}{2(n-1)} - \cos \alpha/2 \left(-\frac{\alpha'}{n}\sin n\alpha' + \frac{1 - \cos n\alpha'}{n^2}\right)$$

$$\left. - \epsilon\left(\frac{\alpha'}{2} + \frac{\sin 2n\alpha'}{4n}\right) + (K_a + \epsilon K_b) \frac{\sin n\alpha'}{n} \right\}$$

The above equation may be abbreviated as follows,

$$I'_{Cn} = \frac{V_{B1}}{r_{bb}\omega\tau_f} \times f_1(\alpha', n, \epsilon) \tag{3.15}$$

Substituting Eqn. 3.12 into the above equation it may be shown that,

$$\epsilon = \frac{C_{BC1} V_{Cn}}{I'_{Cn} \tau_f} \times f_1(\alpha', n, \epsilon)$$

Now it may be shown that the output resistance (R_o) of a neutralised transistor at high frequencies (common emitter mode) is approximately equal to τ_f/C_{BC1}[25]. This approximation is useful over the range of frequencies from above f_β to near F_T in most transistors. For a tuned amplifier or multiplier it may be shown that,

$$R_L = \frac{V_{Cn}}{I'_{Cn}}$$

And from Reference 25, we have

$$P_o \approx \tau_f / C_{BC1} \qquad\qquad (3.16)$$

$$\varepsilon = \frac{R_L}{R_o} \times f_1(\alpha', n, \varepsilon)$$

$$\frac{R_L}{R_o} = \frac{\varepsilon}{f_1(\alpha', n, \varepsilon)} \qquad\qquad (3.17)$$

For design purposes ε is a cumbersome specification of matching factor to use. However the ratio R_L/R_o is a very useful quantity that is usually easily specified by the designer. Therefore R_L/R_o will be specified whenever possible but ε is useful in the manipulation of the above equations arising out of this analysis.

In the amplifier/multiplier analysis two performance figures are of paramount interest. These are collector efficiency and input power requirement. The collector efficiency may be determined using Eqn. 2.2. In order that this equation may be used I'_{CO} must be calculated. I'_{CO} is simply the average value of the collector current; i.e.

$$I'_{CO} = \frac{V_{B1}}{\pi r_{bb} \omega \tau_f} \int_{-\alpha'}^{0} \left(\sin(\omega t + \alpha/2) - \omega t \cos \alpha/2 - \varepsilon \cos n\omega t \right.$$

$$\left. + K_a + \varepsilon K_b \right) d\omega t$$

$$= \frac{V_{B1}}{\pi r_{bb} \omega \tau_f} \left[- \cos(\omega t + \alpha/2) - \frac{\omega^2 t^2}{2} \cos \alpha/2 - \frac{\varepsilon}{n} \sin n\omega t \right.$$

$$\left. + (K_a + \epsilon K_b)\omega t \right]_{-\alpha}^{0}$$

$$= \frac{V_{B1}}{\pi r_{bb}\omega\tau_f} \left\{ -\cos \alpha/2 + \cos(-\alpha' + \alpha/2) + \frac{\alpha'^2}{2} \cos \alpha/2 \right.$$

$$\left. - \frac{\epsilon}{n} \sin n\alpha' + (K_a + \epsilon K_b)\alpha' \right\}$$

or we may write

$$I'_{CO} = \frac{V_{B1}}{r_{bb}\omega\tau_f} \quad x \quad f_2(\alpha',\epsilon,n) \tag{3.18}$$

and define

$$\eta'_{CI} = \frac{I'_{Cn}}{2I'_{CO}} = \frac{f_1(\alpha',n,\epsilon)}{2f_2(\alpha',n,\epsilon)} \tag{3.19}$$

where $f_1(\alpha',n,\epsilon)$ is defined in Eqn. 3.15.

Thus the modified collector efficiency may be calculated.

It is now pertinent to calculate the input power requirement of the feedback amplifier or multiplier. The input power is found by calculating the component of input current in phase with the input voltage and multiplying these two quantities together. The input voltage, neglecting the direct voltage component, is;

$$v_B = V_{B1} \cos (\omega t + \alpha/2)$$

The fundamental input current, inphase with the above voltage, must be evaluated. With the feedback model of the transistor amplifier/ multiplier the input current is the same as for the complete mismatch

model (of Chapter Two) during the interval of transistor collector current conduction. The input current, outside of this conduction period, is established by the feedback current (i_f). Thus,

$$i_B' = \frac{V_{B1}}{r_{bb}} \left(\cos(\omega t + \alpha/2) - \cos \alpha/2\right)$$

when $-\alpha' < \omega t < 0$

$$i_B' = \frac{V_{B1}}{r_{bb}} \left(\cos(\omega t - \alpha/2) + \cos \alpha/2\right) \hspace{2cm} (3.20)$$

when $0 < \omega t < \alpha'$

otherwise $i_B' = -\varepsilon \, n \, \sin n\omega t$

Note that the sign of i_f is changed because the sense of i_B' and i_f are opposite. A Fourier analysis will be used to determine the fundamental current component in phase with the input voltage.

$$I_{B1 inphase}' = \frac{V_{B1}}{r_{bb}\pi} \int_{-\alpha'}^{0} \left(\cos(\omega t + \alpha/2) - \cos \alpha/2\right)\cos(\omega t + \alpha/2)d\omega t$$

$$+ \frac{V_{B1}}{r_{bb}\pi} \int_{0}^{\alpha'} \left(-\cos(\omega t - \alpha/2) + \cos \alpha/2\right)\cos(\omega t + \alpha/2)d\omega t$$

$$+ \frac{V_{B1}}{r_{bb}\pi} \int_{-\pi}^{-\alpha} \varepsilon\left(-\sin n\omega t \, \cos(\omega t + \alpha/2)\right)d\omega t$$

$$+ \frac{V_{B1}}{r_{bb}\pi} \int_{\alpha'}^{\pi} \varepsilon\left(-\sin n\omega t \, \cos(\omega t + \alpha/2)\right)d\omega t$$

$$I'_{Blinphase} = \frac{V_{B1}}{r_{bb}\pi} \left\{ \frac{\sin \alpha}{4} + \frac{\sin(2\alpha' - \alpha)}{4} + \frac{\alpha'}{2} - \frac{\cos \alpha}{2} \times \right.$$

$$\left[\sin \alpha/2 - \sin(-\alpha' + \alpha/2) \right] - \frac{\sin 2\alpha'}{4} - \frac{\alpha'}{2} \cos \alpha + \sin(\alpha' + \alpha/2)$$

$$x \cos \alpha/2 - \cos \alpha/2 \sin \alpha/2 - \epsilon \left[\frac{-\cos(-n\alpha' - \alpha' + \alpha/2)}{2(n+1)} \right.$$

$$\left. + \cos(-n\pi - \pi + \alpha/2) + \frac{-\cos(-n\alpha' + \alpha' - \alpha/2) + \cos(-n\pi + \pi - \alpha/2)}{2(n-1)} \right.$$

$$\left. + \frac{-\cos(n\pi + \pi + \alpha/2) + \cos(n\alpha' + \alpha' + \alpha/2)}{2(n+1)} \right.$$

$$\left. \left. + \frac{-\cos(n\pi - \pi - \alpha/2) + \cos(n\alpha' - \alpha' - \alpha/2)}{2(n-1)} \right] \right\}$$

$$I'_{Blinphase} = \frac{V_{B1}}{r_{bb}\pi} \, f_3(\alpha', n, \epsilon) \tag{3.21}$$

The input power is;

$$P'_{Bin} = \frac{I'_{B1 \, inphase} \times V_{B1}}{2}$$

$$P'_{Bin} = \frac{V_{B1}^2}{2r_{bb}} \times \frac{f_3(\alpha', n, \epsilon)}{\pi}$$

normalising with respect to I'_{Cn} using Eqn. 3.15.

$$P'_{Bin} = \frac{I'^2_{Cn} \, r^2_{bb} \, \omega^2 \tau^2_f}{2} \times \frac{f_3(\alpha', n, \epsilon)}{f_1^2(\alpha', n, \epsilon)} \tag{3.22}$$

With Eqns. 3.22 and 3.19 it is now possible to calculate the approximate

effect of capacitive feedback in a transistor amplifier or multiplier

(in the common emitter configuration). These equations determine the

collector efficiency and the input power requirement, these two quantities

being of most interest. The equations involved are long and complicated

and can only be solved in practice with the aid of a digital computer.

The computer program used in the solution is shown in Appendix 2 . A

block diagram illustrates the method in which the equations were evaluated.

The program is shown written in an International Computer and Tabulator

Fortran IV. Sample results are also shown in Appendix 2 . The results

of the computer program show that the amplifier conduction angle is

modified by feedback but because the conduction angle is treated as an

independant variable the other characteristics are examined as a function

of the new modified conduction angle. The results show that the collector

current efficiency of the transistor is unaltered by feedback. The amp-

lifier or multiplier characteristic that changes most markedly is input

power requirement; the modified requirements for an amplifier, doubler,

tripler and a quadrupler are shown in Figures 3.9, 3.10, 3.11 and 3.12,

respectively. The input power is shown as a function of modified

conduction angle and of the "match factor (R_L/R_o)". The curves are

indespensible for calculating input power of an amplifier or multiplier

operating near the maximum frequency of useful performance for the

transistor. The specific way in which these curves are best used will

be illustrated later in this chapter. Measurements have been made to

Figure 3.9

Normalized input power requirement of a feedback amplifier.
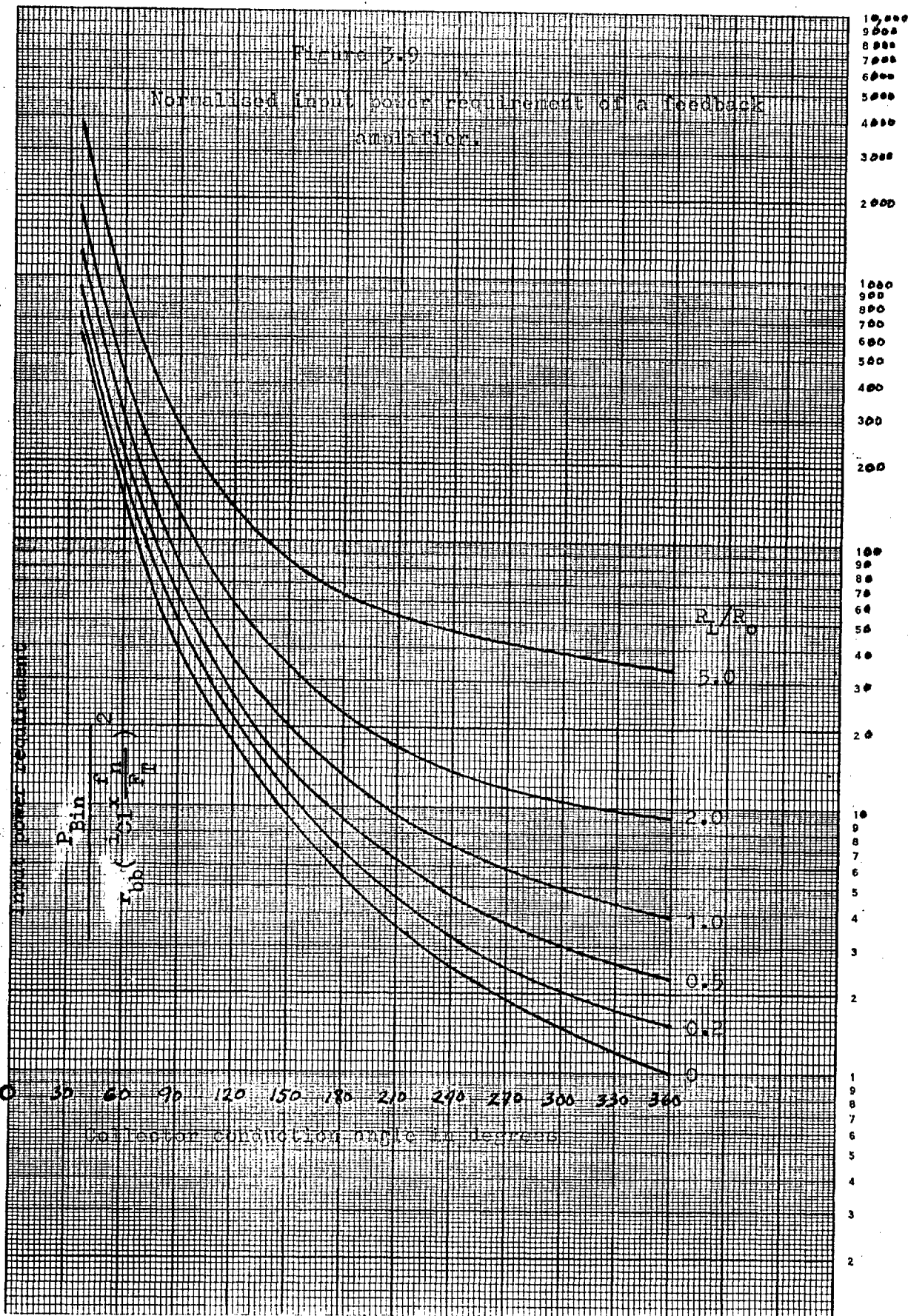
Figure 3.10

Normalised input power requirement of a transistorised feedback doubler.
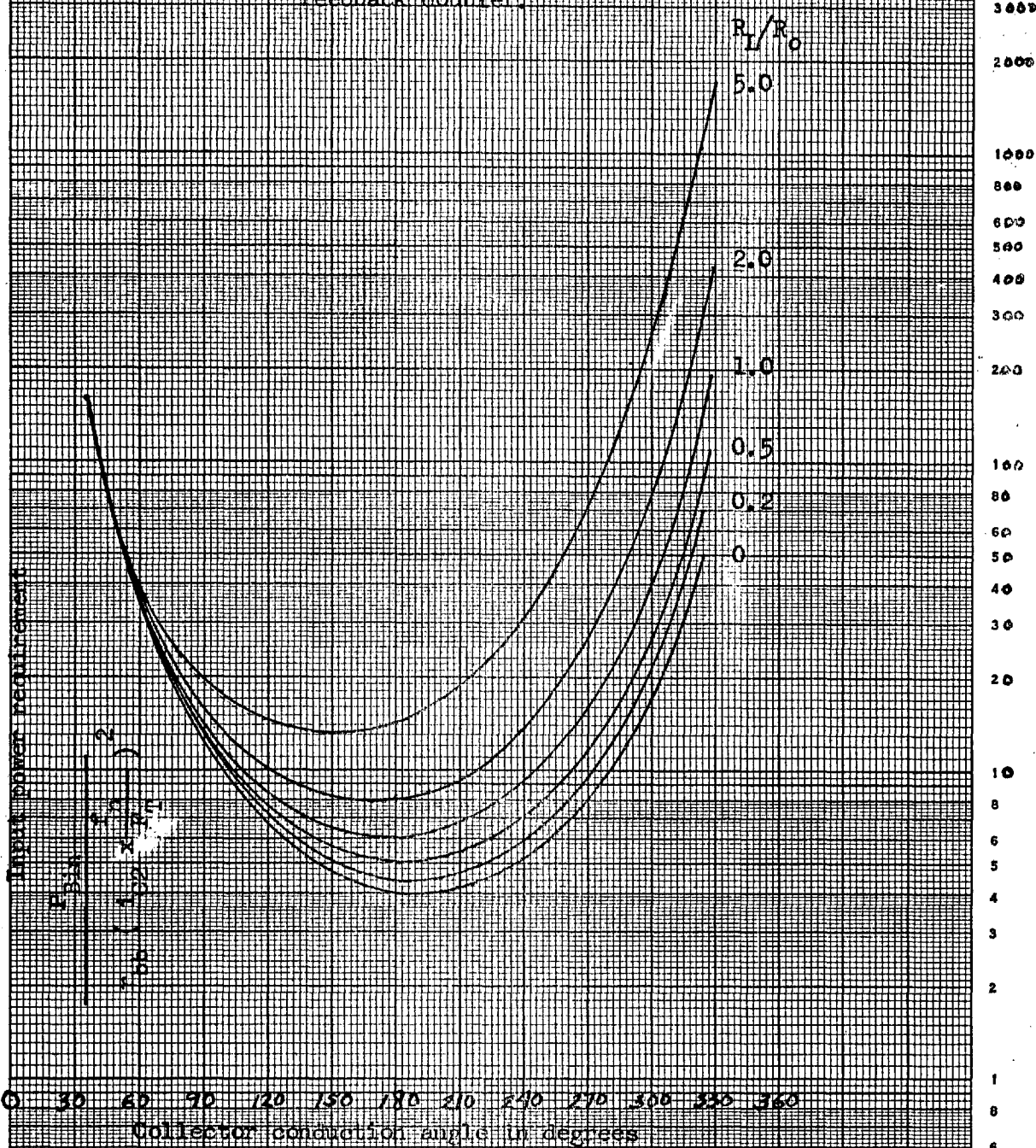
Figure 3.11

Normalised input power requirement of a transistorised feedback tripler.
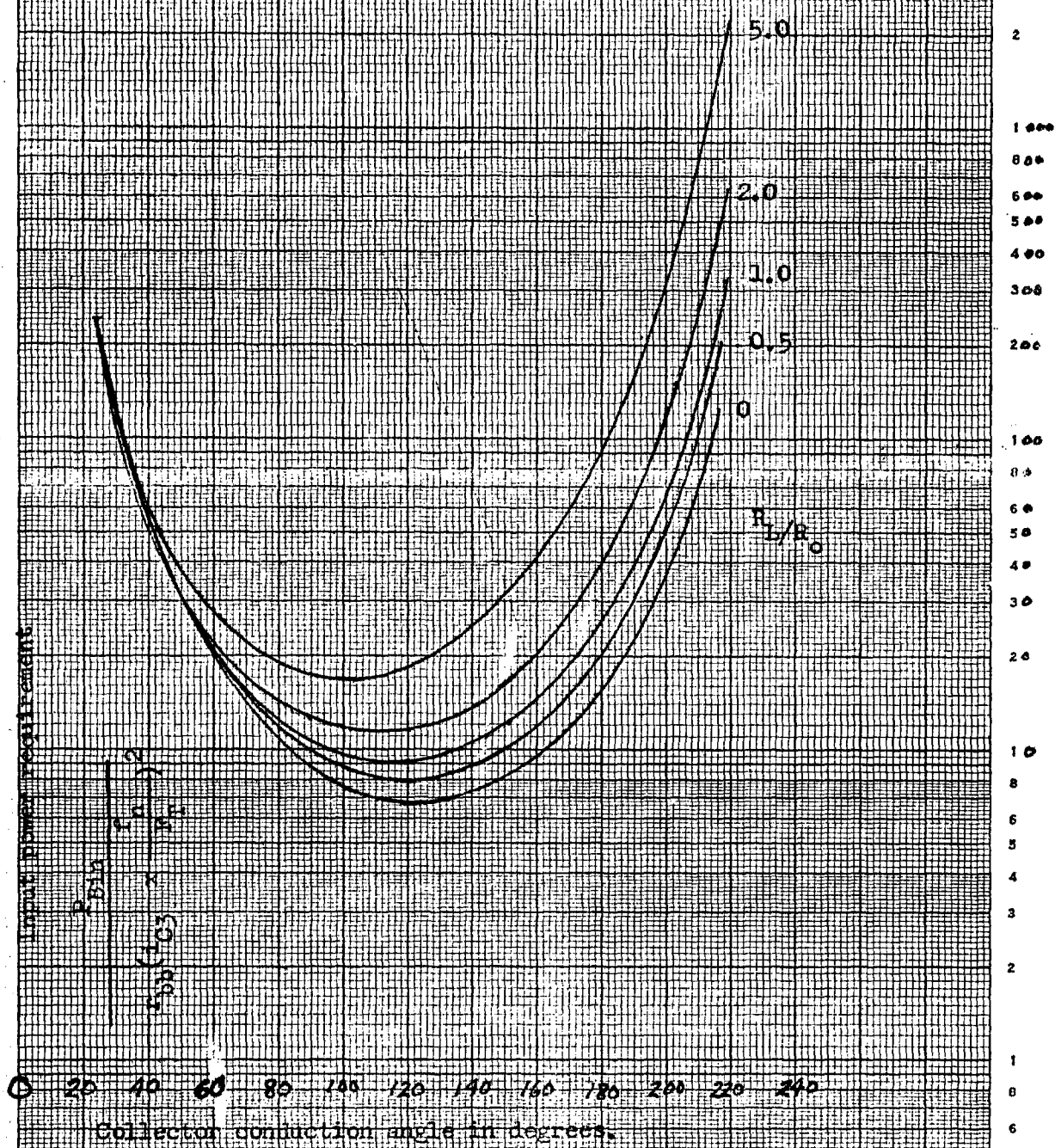
Figure 5.12

Normalised input power requirement of a transistorised feedback quadrupler.
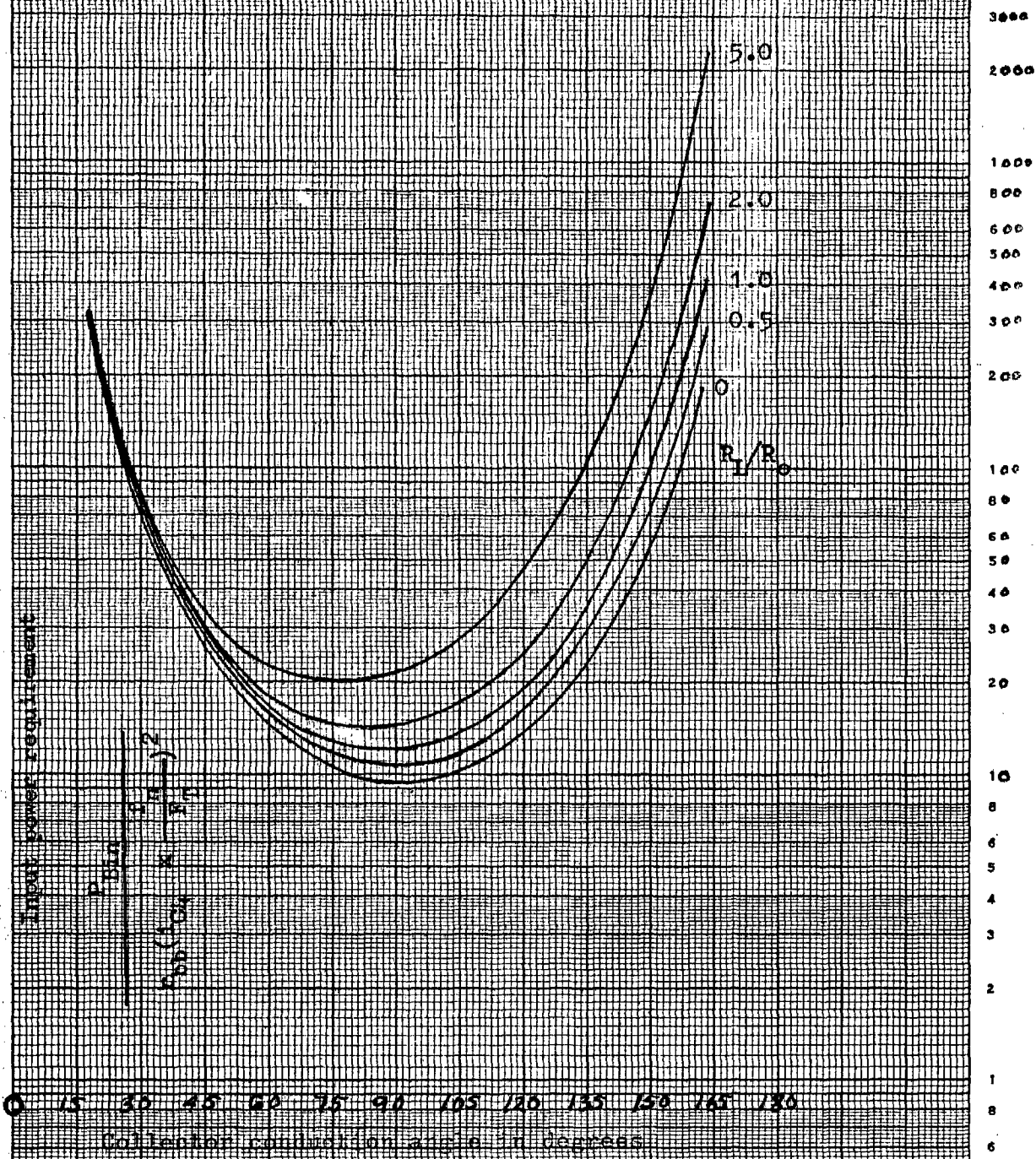
test the accuracy of the computed results. The input power, of an amplifier and a doubler are measured with feedback by a method similar to that used in Chapter Two (see Figure 3.13). The measured input

---

Figure 3.13
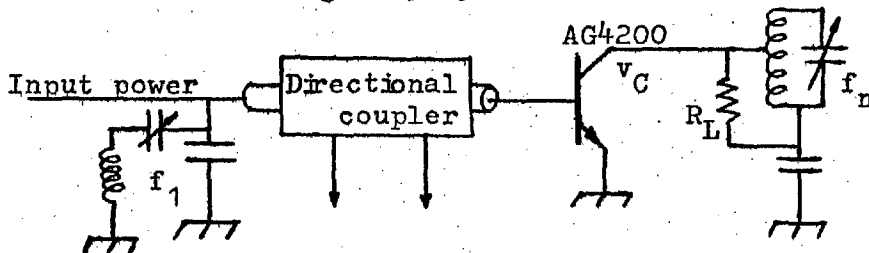
Power input of an amplifier or a multiplier with feedback. The input is measured using the directional coupler. The output current (i_{Cn}) is determined from the collector voltage and the load resistance (R_L).

---

powers are illustrated along with the theoretical input power for an amplifier and a multiplier in Figures 3.14 and 3.15 respectively, and show good agreement.

It is possible to derive the usual expression of f_{max} using the theory developed. This will be done for an amplifier using a conduction angle of $360°$. To obtain the maximum possible gain from the transistor it is necessary to conjugate match the output impedance. Thus R_L is made equal to R_o.

$$P_{oC} = R_o \times i_{C1}'^2$$

Figure 3.14

Measured and theoretical normalised input power
requirement of an amplifier (transistor type
ACY200) with feedback (crosses) and without
feedback (circles). Input frequency is 5 MHz.
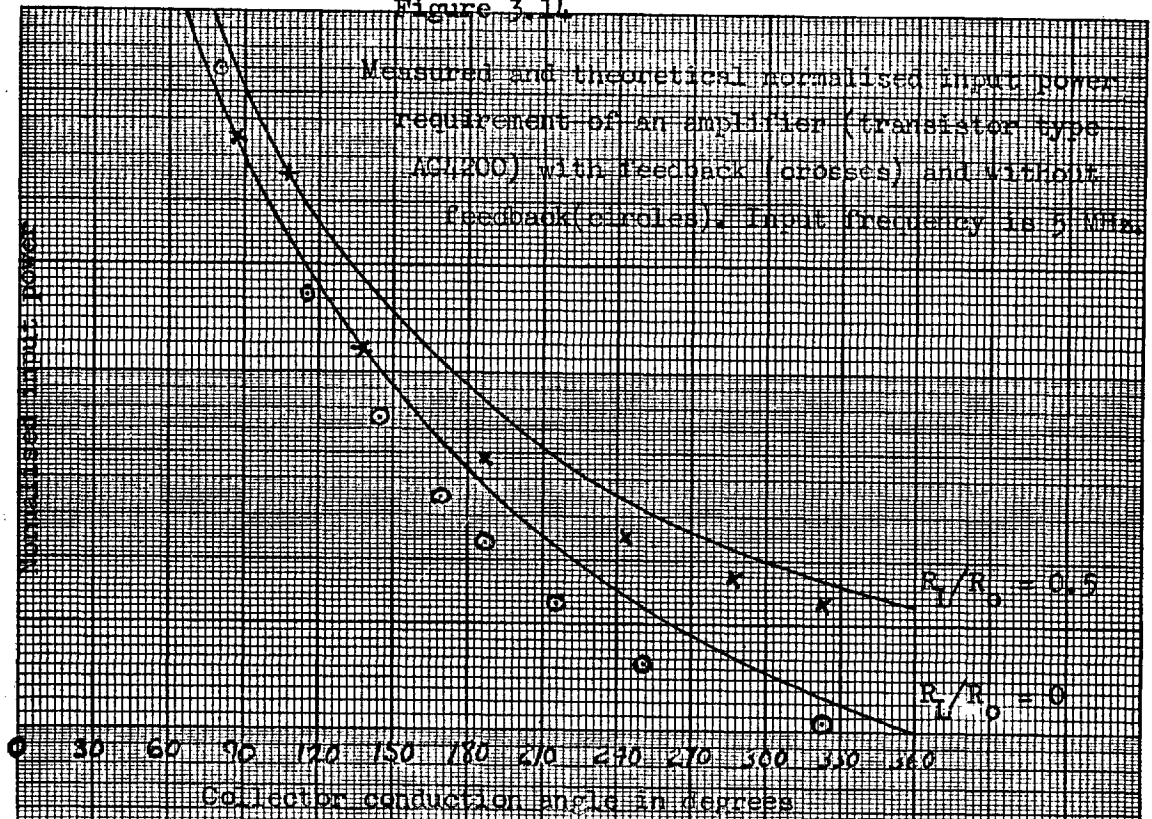
Figure 3.15

Measured and theoretical normalised power requirement of a
doubler (transistor type ACY200) with feedback (crosses) and
without feedback (circles) with an input frequency of 5 MHz.
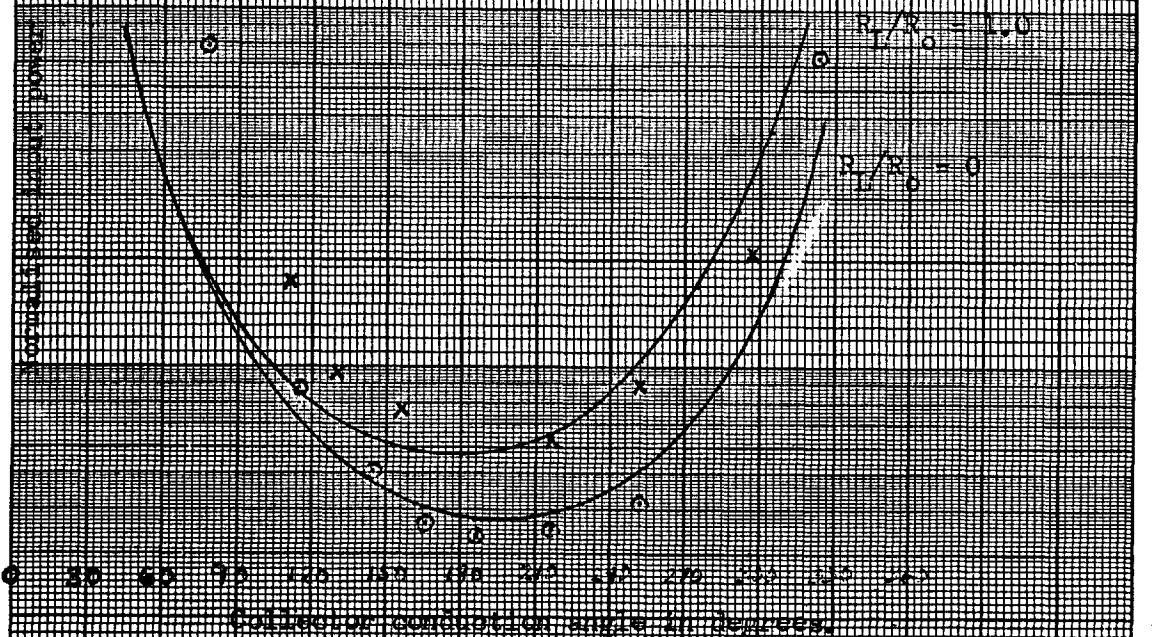
and it may be seen from Figure 3.9 that the input power requirement is,

$$P'_{Bin} = 4.0 \times r_{bb}(i'_{C1} \times \frac{f_1}{F_T})^2$$

f_{max} is defined as being the frequency at which the power gain of the transistor is unity. Therefore

$$4r_{bb} = R_o \frac{F_T^2}{f_{max}^2}$$

Equation 3.16[25] may be rewritten as,

$$R_o = \frac{1}{\omega_T C_{BC1}}$$

since,

$$\tau_f \approx \frac{1}{\omega_T}$$

$$\therefore \quad 4r_{bb} = \frac{1}{C_{BC1}\omega_T} \times \frac{F_T^2}{f_{max}^2}$$

$$f_{max} = \left(\frac{F_T}{8\pi \, r_{bb} \, C_{BC1}}\right)^{\frac{1}{2}}$$

This expression is in agreement with the usual algebraic evaluation[24] of f_{max}, as is expected since both depend upon the same initial assumptions about the current gain characteristics of the transistor.

3.4   Practical Circuits

Good circuit design and layout will ensure that the assumed electrical conditions are attained with a minimum number of available components.   Only experience can indicate the likelihood of good circuit performance with nonideal components.   Amplifier stability is a function of the circuit layout and care must be taken to reduce feedback paths which can cause oscillation.   As the frequency is increased and the upper frequency limit of lumped components is approached the design becomes more critical.   Usually simplicity goes with good design.

The input and output tuned circuits, and particularly the former, must be tapped to obtain an impedance level suitable for the transistor. The original assumptions require that voltage sine waves exist on both the input and output.   The simplest circuit that can be used to fulfill this requirement is a tapped parallel tuned tank circuit.   The reason for tapping the circuit is that a tuned circuit of a good Q cannot be made with the low impedance required by the transistor.   Low impedances can only be obtained by tapping down on the inductance or the capacitance or both simultaneously.   See Figure 3.16.   The circuits have slightly different characteristics which are worth taking note of.

If it is desirable to bypass all the harmonics the tapped capacitance configuration is the best since the higher harmonic frequencies are most effectively bypassed by a capacitance.   Thus on the input a tapped capacitance maintains the most perfect sinusoidal voltage.

Figure 3.16
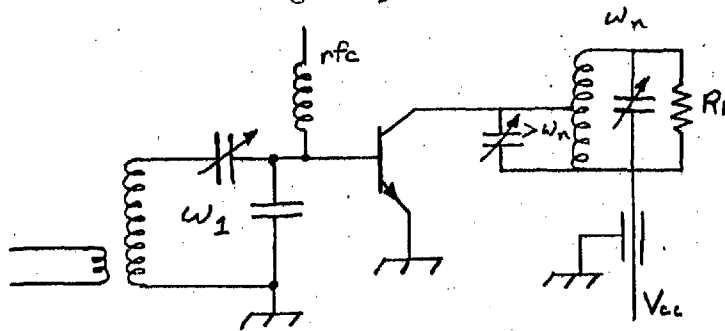
Two useful tuned circuits for NIAM. The input is a tapped capacitance tuned circuit. The output is a tapped inductance tuned circuit.

The tapped capacitance circuit provides a dc block and an rf choke must be used to supply the transistor bias. The rf choke should be operated at a higher frequency than its characteristic "self resonant frequency", where it appears capacitive. The circuit should not be used at both the input and output because most power transistors will tend to oscillate at frequencies slightly lower than the operating frequency. The circuit has a high input impedance at low frequencies, encouraging this oscillation tendency, and should therefore only be used on either the input or output, and preferably the former.

The tapped inductance circuit provides a dc path for biasing and a bypass condenser must be used to ground one end of the coil. This circuit is not as good as the tapped capacitance configuration for bypassing the higher frequencies and may even have another parallel resonance (low Q) at higher frequencies $(> f_1)$. This resonance may distort the output voltage sine wave slightly. The circuit has

a low impedance at low frequencies and will not permit oscillations
as the tapped capacitance circuit does. The circuit is then the best
on the output of a multiplying stage where lower frequencies (than the
output frequency) must be bypassed to ground.

A combination of this circuit and the previous one may be used
to couple two stages together. See Figure 3.17. The modified circuit

Figure 3.17
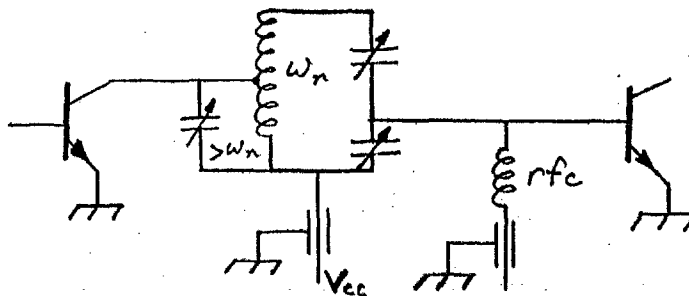
The tapped inductance and tapped capacitance tuned circuits are
combined to become an effective interstage tuned matching circuit.

works well for power amplifiers and frequency doublers.

For higher harmonics, the elimination of the fundamental component
of the waveform becomes more critical if uniform collector current
pulses (free of subharmonics) are to be maintained at the output of
the second transistor. (The nonlinear input, with large reverse biases,
exaggerates the effects of input noise or variation in the amplitude of
the input rf or direct voltage bias.) A good circuit for the elim-
ination of the fundamental is shown in Figure 3.18. The circuit is
somewhat involved and is usually necessary only if the second transistor
(T2) is operating in a highly nonlinear mode (viz. $\alpha' < 3\pi/4$).

Figure 3.18
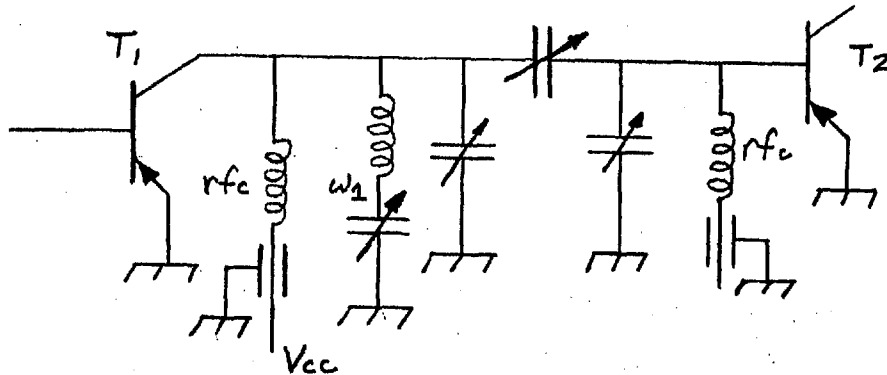
Frequency multiplying interstage tuned matching circuit
where the input frequency (to T_1) is suppressed.

The biasing of the transistor input may be done in three dif-
ferent ways.   The transistor may have a reverse bias direct voltage
applied, or a fixed direct current applied to the emitter in the usual
way.   A better method is a self biasing arrangement, which tends to
maintain a constant conduction angle with a variable rf input.
The biasing circuit consists of a variable resistance connected between
the emitter and base of the transistor (via the usual biasing connect-
ions) with a parallel capacitance to provide a suitable time constant.
Amplitude modulated signals have been successfully frequency doubled
using the self biasing arrangement.

3.5   Design Approach and Examples

3.5.1   Maximising transistor performance.

    In order to obtain the best performance from a transistorised

power amplifier or a frequency multiplier, the transistor must be
utilised to its maximum capability. The limitations on this maximum
capability depend upon the environmental and electrical requirements.
Normally stress, with respect to electrical performance, will fall on
maximum power output, maximum power gain or an optimum trade of one
for the other.

A simple approach to nonlinear input amplification or multiplic-
ation (NIAM) design is to assume that maximum power gain is the
criterion and treat other situations as a variation of this one. In
the analysis, until now, the nonlinear charge storage element D_{BE}
has been assumed to be the only nonlinearity in the transistor. In
Figure 1.2 it is shown that current gain cut off frequency of the
transistor (F_T) is very much a function of collector voltage and
current. The curves of constant F_T, are normally determined on the
basis of small signal measurements, of which the correlation to large
signal charge control time constants is undefined. For purposes here,
it is assumed that the large signal F_T is simply an average of the
small signal F_T. In the interests of obtaining maximum power gain
from the transistor it is necessary to apply maximum voltage to the
collector of the transistor, F_T being a monotonically increasing
function of collector voltage. Some amplifier analyses are based
exclusively on the principle of operating the transistor over a
favourable collector current and voltage range[27].

Class C operation of an amplifier is a method of trading power
gain for collector power conversion efficiency. Maximisation of power

conversion efficiency must be approached both by maximising the collector voltage and current efficiencies. From Figures 2.1 and 2.5, it may be shown that

$$P_{oC} = \frac{V_{Cn}^2}{2R_L} \qquad (3.23)$$

where V_{Cn} is limited by Eqn. 2.6. In the amplifier, output power is essentially set by the direct collector voltage and the load resistance R_L. Since the direct collector voltage is set near the maximum allowable (limited by BV_{CE}), the load resistance is the variable that determines the power output.

$$BV_{CE} \geqslant V_{CC} + V_{Cn} \qquad (3.24)$$

The point of maximum power gain of the transistor, as a multiplier or amplifier, occurs when the transistor is biased such that $2n\alpha' = 360^\circ$. The conduction angle may be decreased to increase the power handling capability of the transistor. The multiplier differs somewhat from the amplifier in that the input nonlinearity is utilised for harmonic generation. Normally it is best to use the above specified conduction angle even when a low collector voltage efficiency is acceptable. This method of operation is good if a low power output, high gain multiplier is required since the F_T may be optimised by the use of large collector voltages (limited by Eqn. 3.24). If good efficiency is required the harmonic collector voltage should be increased up to

the point defined by Eqn. 2.6. A further increase of efficiency is then obtained by a reduction in conduction angle (to less than 360/n).

Normally the limiting factor in regard to the power handling capability of a transistor is the maximum power dissipation in the device. Thus if collector efficiency is increased, the possible power output is increased. If the power gain of the transistor is very high, the maximum power output is, virtually, inversely proportional to the collector power losses. That is

$$P_{Dis} \geqslant P_{Bin} + P_{oC}(\frac{1}{\eta_{CP}} - 1) \qquad (3.25)$$

If the power gain (P_{oC}/P_{Bin}) of the transistor NIAM is low the conduction angle of maximum power output may be found by decreasing the conduction angle (from that of $360^{o}/n$) until the P_{Dis} is a minimum. A plot of power dissipation versus conduction angle is a laborious undertaking if all relevant aspects of the NIAM are included. The best conduction angle will always be greater than zero but less than $360^{o}/n$.

3.5.2   Amplifier design example.

A transistor, type 2N1506, was chosen, largely because of the very extensive data published by the manufacturer, with the objective of producing one watt at 100 MHz. The transistor was to be operated for maximum gain. Some of the device characteristics are;

$$P_{Dis} = 2.0 \text{ watts in air, with heat dissipator}$$

$$BV_{CE} = +60 \text{ volts}$$

$$BV_{EB} = 5.0 \text{ volts}$$

$$V_{Csat} = 1.5 \text{ volts (at } I_C = 100 \text{ ma)}$$

$$f_\beta = 10 \text{ MHz (typical)}$$

On the basis of Eqn. 3.24 and 2.6, it may be shown that;

$$BV_{CE} \geqslant 2V_{Cn} + V_{Csat}$$

Therefore let V_{Cn} = 29.25 volts and V_{CC} = 30.75 volts. In order to obtain 1.0 watts output it is necessary (from Eqn. 3.23) to make R_L equal to 426 ohms. From Eqn. 2.2, it may be shown that,

$$I_{C1} = \frac{2P_{oC}}{V_{C1}}$$

$$= 68.5 \text{ ma.}$$

The transistor, being operated for maximum gain, is made to conduct all of the time. From Figure 2.12 it may be seen that the collector current efficiency is 0.50. Therefore;

$$I_{CO} = 68.5 \text{ ma} \qquad \text{(Eqn. 2.4)}$$

$$I_{C_{max}} = 137 \text{ ma} \qquad \text{(Figure 2.22)}$$

The collector voltage efficiency is;

$$\eta_{Cv} = \frac{29.25}{30.75} \qquad (\text{Eqn. } 2.5)$$

$$= 95.2\%$$

Thus the power conversion efficiency of the collector is,

$$\eta_{CP} = 47.6\% \qquad (\text{Eqn. } 2.3)$$

Now that the operating ranges of the transistor collector have been determined, averaged large signal values of F_T and C_{BC1} may be determined. Both F_T and C_{BC1} must be estimated over the current and voltage operating ranges applicable to the application. The large signal values of F_T and C_{BC1} are best found by averaging (with respect to time) the small signal values for the active period of the transistor. The measured value of R_0 of the transistor is 350 Ω (at I_C = 100 ma and V_{CC} = 30 volts). F_T for this operating point is given to be 250 Mhz, thus implying that C_{CB1} is about 1.7 pfd (about 28% of $C_{CB1} + C_{CB2}$) for this bias level. An average value of F_T is about 200 MHz and the large signal C_{CB1} is about 8.0 pfds. Therefore the large signal value of R is about 101 Ω. The value of r_{bb} is 15.0 Ω (obtained from the manufacturer's data sheet). The input power requirement of the transistor may be calculated when the "match factor" is ascertained.

$$\frac{R_L}{R_o} = 4.2$$

From Figure 3.9 the input power requirement is found to be,

$$P'_{Bin} = 25 \; r_{bb} \; (i'_{Cn} \times \frac{f_n}{F_T})^2$$

$$= 25 \times 15 \; (\frac{.0685}{\sqrt{2}} \times \frac{100}{200})^2$$

$$= .220 \text{ watts.}$$

Thus a gain of 6.6 db is predicted.   The calculated performance may be compared with measured performances in Table 3.1.   The two correspond very closely.

TABLE 3.1

Transistorised   Power   Amplifier

2N1506   f = 100 MHz

Quantity	Calculated Performance	Measured Performance	
		2N1506 [#]1	2N1506 [#]2
P_{indc}	2.10 watts	2.06	2.06
P_{oC}	1.00 watts	1.00	1.04
n_{CP}	47.6%	46.2	50.5
P'_{Bin}	.220 watts	.195	.195
Power Gain	+ 6.6 db	7.1	7.3

3.5.3 Doubler design example.

The same transistor as used above as an amplifier (type 2N1506) was also used as a doubler. Due to the limitation of BV_{EB} the transistor would not produce 1.0 watt of rf at 100 MHz. The input frequency was dropped to 25.0 MHz where the limitation had a reduced effect. This example illustrates a shortcoming that is very common in present day, power, high frequency planar, transistors, which has hitherto not been recognised.

The method of designing a doubler, or any NIAM, is basically the same as the class C amplifier with increased attention given to some aspects. The power output of the doubler was limited by the low reverse breakdown voltage of the transistor input (BV_{EB}). The effect of this limitation is difficult to specify, once it is encountered. The approach here was to build a doubler and then predict its input power requirement. A sample calculation is given in brackets. The measured collector operating powers and voltages are used to estimate the collector current and voltage efficiencies ($\eta_{Cv} = \dfrac{V_{Cn}}{V_{CC}}$, $\dfrac{11.38}{28.0}$,

40.67; Eqn. 2.5 and $\eta_{CP} = \dfrac{P_{oC}}{V_{CC}I_{CO}}$, $\dfrac{.200}{28.0 \times .0455}$, 15.07;

Eqns. 2.2 and 2.5 and $\eta_{CI} = \dfrac{\eta_{CP}}{\eta_{Cv}}$, 38.6%;

Eqns. 2.3, 2.4 and 2.5).

From the current efficiency, the conduction angle is estimated ($2\alpha' = 207^{o}$ using Figure 2.15). Using the collector harmonic voltage and output power the apparent load resistance is estimated ($R_L = \dfrac{V_{Cn}^2}{2P_{oC}}$, 324Ω ; Eqn. 3.23). The collector harmonic current may be evaluated from the

collector direct current and the collector current efficiency.

$(I_{Cn} = 2I_{CO}\eta_{CI}$, 35.1 ma; Eqn. 2.4). The above calculations provide enough information for the evaluation of P_{Bin} where F_T and R_o are assumed to be the same as for the amplifier (F_T = 200 MHz and R_o = 101Ω). Therefore R_L/R_o = 3.2

$$P'_{Bin} = 15 \times 15 \left(\frac{35.1}{\sqrt{2}} \times \frac{50}{200}\right)^2$$

using Figure 3.10.

$$= 8.7 \text{ ma}$$

The degrading effect of the input capacitance must now be accounted for. The total depletion input capacitance is found to be 120 pfd $(C_{BE1} + C_{BE2})$. It is assumed that 60%* of the input depletion layer capacitance is effectively buried beneath the base resistance (C_{BE1} = 72 pfd). It may then be shown that,

$$(\omega C_{BE1} r_{bb})^2 = .029$$

For a conduction angle of 207° it is found that the input power requirement is increased by a factor of 1.19 using Figure 3.5. This is an estimate of the real degradation factor.

The limitation caused by the reverse voltage breakdown (BV_{EB})

---

* The ratio is assumed to be the same as the transistor (type AG4200) examined in Section 3.2.

will be examined. The effect of feedback is considerable and this
reduces the output current (and hence the output power) while the input
voltage (v_B) is unchanged. The input voltage, at its negative most
peak, may cause avalanche breakdown of the base-emitter diode. The
transistor will not, necessarily, be damaged but certainly the input
power requirement will be increased. The input reverse breakdown
limitation may be evaluated in terms of the collector current. It is
seen in Figure 3.8 that the input voltage v_B and current i_B remain
constant (to a first approximation). The effect of feedback is to
reduce the intrinsic base current i_D' and hence the collector current
i_C'. The absolute input power is essentially constant, therefore the
input power normalised to collector current is dependant solely on the
collector current. Thus,

$$\frac{P_{Bin}(n,\alpha',R_L/R_o)}{I_{Cn}'^2} \approx \frac{P_{Bin}(n,\alpha',0)}{I_{Cn}^2}$$

I_{Cnmax} may be determined from Figure 2.21. Using the above equation,
I_{Cnmax}' may be found.

$$I_{Cnmax}' \approx I_{Cnmax} \left(\frac{P_{Bin}(n,\alpha',0)}{P_{Bin}(n,\alpha',R_L/R_o)}\right)^{\frac{1}{2}} \tag{3.26}$$

where $P_{Bin}(n,\alpha',R_L/R_o)$ may be evaluated from Figures 3.9 to 3.12.
For the transistor doubler;

$$I_{Cnmax}' = \frac{.11(BV_{EB} + V_{BECon})}{r_{bb}} \times \frac{F_T}{f_n} \times \left[\frac{P_{Bin}(n,\alpha',0)}{P_{Bin}(n,\alpha',R_L/R_o)}\right]^{\frac{1}{2}}$$

$$I'_{Cnmax} = \frac{.12(5.5)}{15} \quad x \quad \frac{200}{50} \quad x \quad (\frac{4}{15})^{\frac{1}{2}}$$

$$= 91.0 \text{ ma}$$

It would seem unlikely that the I'_{Cnmax} limitation will be met in this example. Measurements indicate that it is not. The measured and calculated performances of two other multipliers are listed in Table 3.2. The agreement between the calculated input powers and measured input powers in Table 3.2 are good. The transistor operating under power level No. 3 (Table 3.2) showed signs of reverse voltage breakdown at the input. It will be noted as well that the input power requirement here is considerably larger than that predicted, indicating that power is lost when the input voltage swings into the breakdown region of the transistor input. The predicted value of I'_{Cnmax} was too large by a factor of 1.15 or slightly more.

3.6   Conclusions

The nonlinear input amplifier and multiplier (NIAM) has been treated in the last two chapters. Practical verification of the theory has been carried out successfully. The chief limitation to the successful application of the theory is the inadequate amount of information that can be obtained from the manufacturer's data sheets. Even the most prolific data sheets do not provide all the desired information.

In a good transistor, for frequency multiplication, collector

TABLE 3.2

Performance of a transistorised frequency doubler.
The transistor is a type 2N1506. The output
frequency is 50 MHz.

Performance Characteristic		Operating Condition		
		1	2	3
Measured	V_{CC}	28.0 volts	27.7	28.0
"	I_{CO}	45.5 ma	74.0	55.0
"	P_{oC}	.200 watts	.429	.600
"	V_{Cn}	11.38 volts	13.75	21.0
estimated	η_{CP}	15.7%	20.9	39.0
"	η_{Cv}	40.6%	49.6	75.0
"	η_{CI}	38.6%	42.1	52.0
"	$2\alpha'$	$207°$	183	177
"	R_L/R_o	3.2	2.2	3.6
"	I'_{Cn}	35.1 ma	62.3	60.4
Theoretical	I'_{Cnmax}	91.0 ma	86.9 ma	69.0 ma
"	F_{Pdeg}	1.19	1.32	1.40
"	P'_{Bin}	8.7 mw	16.2	20.5
"	P'_{BinDeg}	10.3 mw	21.4	28.75
Measured	P'_{BinDeg}	16.0 mw	32.0	71.1
Theoretical	Power Gain	12.9 db	13.0	13.2
Measured	Power Gain	11.0 db	11.3	9.3

power conversion efficiencies can be attained that are equal to those of a power amplifier with an attendant loss in power gain. The circuit of the multiplier is very similar to the power amplifier. Thus this type of multiplier is much simpler, with respect to circuit complexity, than say a transistor amplifier and a varactor multiplier. Examples illustrate some of the diverse limitations that some transistor parameters may have on multiplier or amplifier performance.

Amplitude modulated signals were successfully doubled in frequency when a self biasing input arrangement was used.

CHAPTER FOUR

CHARGE STORAGE FREQUENCY MULTIPLIERS*

4.1   INTRODUCTION

Since its first introduction in frequency multiplying circuits, the varactor diode has dominated the frequency multiplication field, particularly in very high frequency operation. However, it has been found empirically that diode frequency multipliers employing the minority carrier charge storage effect have performance superior to those of multipliers operating with the diode in the varactor mode, employing the non-linear depletion layer property[28, 29]. The minority carrier charge storage effect may be used alone or in conjunction with depletion capacitance variation to obtain efficient frequency multiplication. Doublers employing both effects can have a power handling capability five times greater than predicted by the theory of the conventional varactor[30]. While the advantageous performance features of charge storage frequency multiplying circuits have been examined practically, analytical treatments of circuit operation are not complete for systematic design. In this chapter the analytical treatment of the circuit leads to an effective design method.

The charge-voltage characteristic of a non-linear charge storage element (NLCSE) is shown in idealised form in Fig. 4.1.

---

*This chapter has been submitted as a paper as per Reference 49.

Figure 4.1
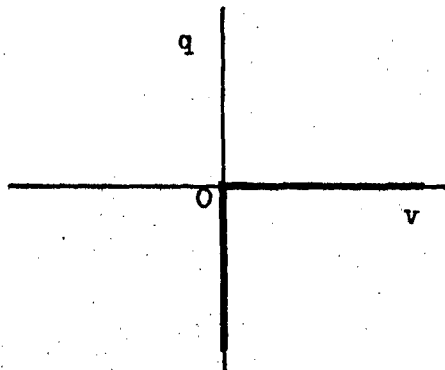
Idealised characteristic of a minority carrier nonlinear

charge storage element.

Usually it is most expedient to consider a two-voltage or a two-charge

(and hence a two-current) circuit (i.e. with suitable filtering, a

fundamental voltage is applied to the diode and one harmonic voltage is

taken from the diode and applied to the load; all other voltages across

the diode are suppressed.) However, Roulston[31] has pointed out that

these circuit assumptions are not possible with the idealised charge

storage characteristic shown in Fig. 4.1. This characteristic defines

that the charge q and the voltage v must be zero for some finite part

of the fundamental cycle. This requirement can only be met with an

infinite number of harmonics components of both charge and voltage

present in the circuit. The zero charge and voltage requirements of the

NLCSE have been met theoretically by Roulston, who analysed and employed

"semituned circuits" (i.e. tuned input, untuned output) and by other

writers who have not employed tuning. However, these circuit config-

urations give a very poor power conversion efficiency. Hedderly[32] considered a high order multiplier (frequency multiplication factor greater than ten) in which the output consisted of a series of damped sine waves, thus implying imperfect output filtering. More recently, Roulston[33] presented an analysis of a double tuned circuit in which the presence of a resistance in series with the diode allows two frequencies to be postulated; in the limit this resistance may be the self series resistance of the diode. Some further consideration will be given to this type of circuit configuration.

The NLCSE characterisation in Fig. 4.1 is useful but very much idealised. It is useful instead to consider a more realistic representation of a charge storage diode, which should exhibit reasonably good step-recovery properties. In all diodes there are at least three strays in addition to the NLCSE represented in Fig. 4.1. The NLCSE always has an associated depletion layer capacitance in parallel, a series resistance and a series inductance as shown in Fig. 4.2.

Figure 4.2
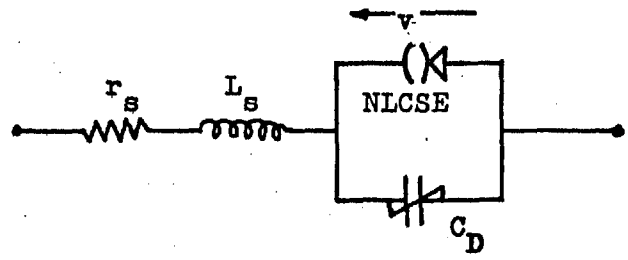
Representation of a practical diode in terms of a nonlinear charge storage element together with the predominant strays.

In addition to these, the NLCSE has imperfect charge storage and does not exhibit exact step recovery. These last two effects will not be accounted for, thereby limiting the following theory to angular frequencies that fall roughly between the inverse of the charge storage time and the charge recovery time. In commercially available step recovery diodes the storage and recovery times may be separated by factors of 200 or greater, thus ensuring a broad frequency range over which the following analysis will be applicable.

4.2 Modes of Operation and Approach to Analysis

The idealised NLCSE of Fig. 4.1 contains both a zero voltage segment and a zero charge segment and for successful operation this element must in the multiplying circuit be presented with a fundamental and an infinite number of harmonics of both charge and voltage. Most other workers have met this requirement through the use of incomplete filtering. Here it will be met by the introduction of broadband idling networks as shown in Fig. 4.3.

Intuition would suggest that a lossless idling network should result in the most efficient multiplying circuit. It is found that the analysis of the circuit is potentially very simple if this idling network is a linear capacitance element. The advantage of this choice is that the idling network may be lumped together with the NLCSE, and the composite network may be described in a very simple manner. The charge-voltage characteristic of the composite network (the NLCSE and

Figure 4.3

(a)
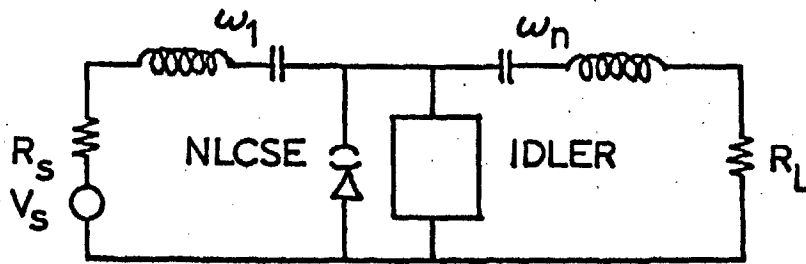
Frequency multiplying circuit where a fundamental current and a single harmonic current flow into the nonlinear element and idler. Referred to as "two-current" or "two-charge" multiplying circuit.
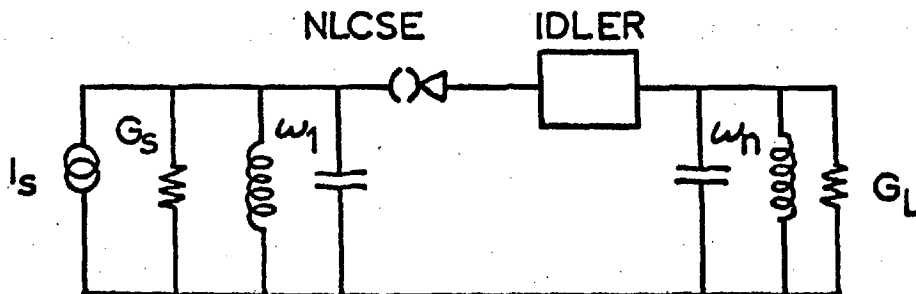
(b)

Frequency multiplying circuit where a fundamental voltage and a single harmonic voltage are applied to the nonlinear element and idler. Referred to as a two-voltage circuit.

Figure 4.4
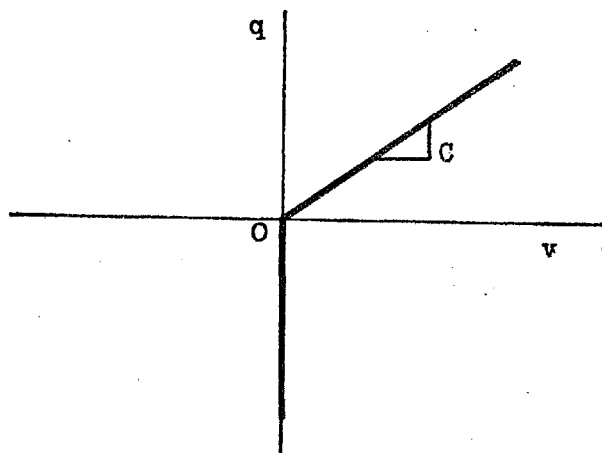
(a)
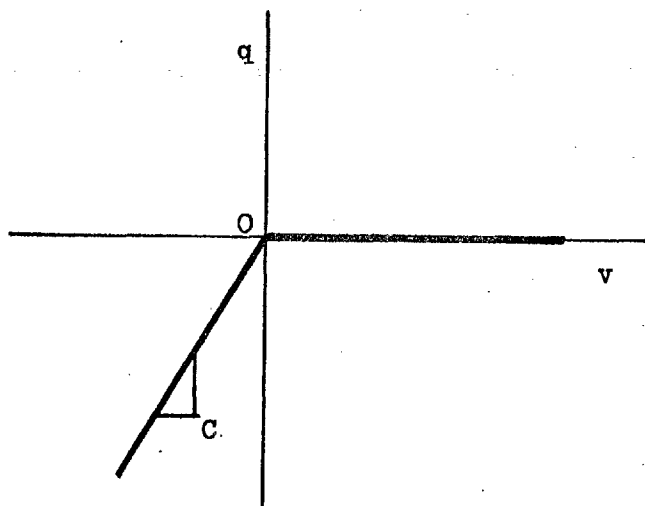
(b)

Modification of idealised characteristic of NLCSE by addition

of parallel (a) or series (b) idling capacitances.

idling capacitance) may be seen in Fig. 4.4. In Fig. 4.3 a series
tuned circuit and a parallel tuned circuit are illustrated. These
circuits will be called, respectively, a two-charge, or two-current
(fundamental charge or current and one harmonic charge or current
applied to the NLCSE and idler) circuit and a two-voltage (fundamental
voltage and one harmonic voltage applied to the NLCSE and idler) circuit.

The strays $(L_s, r_s$ and $C_D)$ of the charge storage diode favour the
two-charge circuit, in practical application, owing to their config-
uration in this circuit (see Fig. 4.5).

Figure 4.5
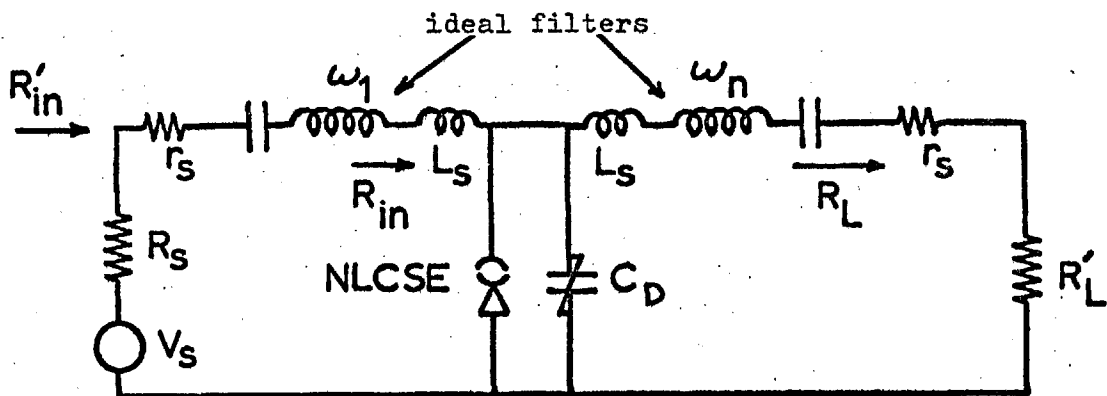
Series tuned circuit (two-charge) redrawn with diode strays to
facilitate circuit analysis. Diode series inductance (L_s) forms
part of the input and output filters. Series resistance (r_s) may
be represented as part of the source and load resistances.
The depletion layer capacitance (C_D) forms an idling capacitance.

The series inductance L_s appears in series with the input and output series tuned circuits, so that it may be "tuned out". The diode series resistance r_s may be thought of as a resistor in series with the input and the load resistances. The depletion layer capacitance C effectively becomes the idling capacitance and plays an important role in the operation of the multiplier circuit. The depletion layer capacitance is assumed constant (with respect to reverse voltage) and this is normally valid since its non-linearity is slight compared with the NLCSE.

The diode strays can present serious limitations in the application of an analysis of the two-voltage configuration of Fig. 4.3b because they cannot be absorbed into the circuit. For example, after recovery the diode will not behave as an open circuit but as a capacitance, and the series inductance and resistance do not allow the diode to behave as a short circuit while it is conducting. A two-voltage analysis based on the circuit of Fig. 4.3b thus fails in these respects to represent the behaviour of an actual diode in this configuration. For these reasons the two-voltage circuit will not be analysed, although the theory of the next section is applicable through duality.

The following discussion and analysis will deal specifically with the series tuned (two-charge) multiplier. It should be noted, however, that the series tuned and parallel tuned (two-voltage) circuits as shown in Fig. 4.3 are duals and therefore the following analysis will apply also the two-voltage circuit with the proper interchange

of charge and voltage. The number of operating modes of this
multiplier, even in a relatively simple two-charge circuit, is large.
In order that an explicit analysis may be made, these modes of
operation are limited to those few that correspond to operation of
the multiplier with superior performance. The following analysis is
similar in approach to the doubler analysis of Scarlett[34], but is much
more comprehensive and of greater scope. It gives consideration to:
any order of multiplication (n), the best relative magnitude of the
fundamental and harmonic charge for maximum efficiency, a number of
possible conduction angles for high order multiplication circuits.
The analysis is completely general with respect to order of multiplication
and relative harmonic charge magnitudes but is, in fact, restricted to
particular phase angles (between the fundamental charge and the
harmonic charge) and particular diode conduction angles. It is felt
that the restrictions of the conduction angle and phase angle are justi-
fied by the generality of the analysis with respect to the other
operating variables, by its simplicity and by the good performance
prediction afforded. Recently, Steinbrecher[18] presented an analysis
for even harmonic frequency multiplication with the conduction angle
adjusted for maximised efficiency. His approach to analysis is very
similar to the one developed here: both may be regarded as a devel-
opment of Scarlett's[34] work. The analysis here is more general in
that it deals with all harmonics and a wide range of conduction angles
(if $n \geqslant 4$). Steinbrecher also analysed the series tuned circuit with
all idlers (these idlers are effective for one frequency only and

every harmonic between the fundamental and the output frequency has an idler) for a conduction angle of 50%. This circuit results in a superior power handling capability and conversion efficiency with an increase in circuit complexity. The modes of operation required here for a simple analysis are obtained by choosing the conduction angle of the diode and the phase angle of the harmonic so that the diode changes state only when the harmonic charge component is crossing the zero axis. It is also assumed that the charge on the diode changes sign only twice per fundamental cycle. The implications of these assumptions are best understood after the preliminary circuit analysis is made. The assumed relationships of charge, current and voltage waveforms are illustrated in Fig. 4.6 for a tripler.

4.3 Circuit Characteristics Calculations

Subject to the above stated conditions the total charge stored in the diode is:

$$q = Q_0 + Q_1 \cos \omega t + Q_n \sin n \omega t$$

where Q_0 is the direct charge and Q_1 and Q_n are the peak values of the fundamental and harmonic charges, respectively. n is the multiplication factor of the circuit. Q_0 is adjusted, in relation to Q_1, so that the charge of the diode charges sign when

$$\omega t = \pm m\pi/n$$

where m is an integer and $o > m > n$. Thus the above charge equation may be written with Q_0 specified in the following way:

Figure 4.6
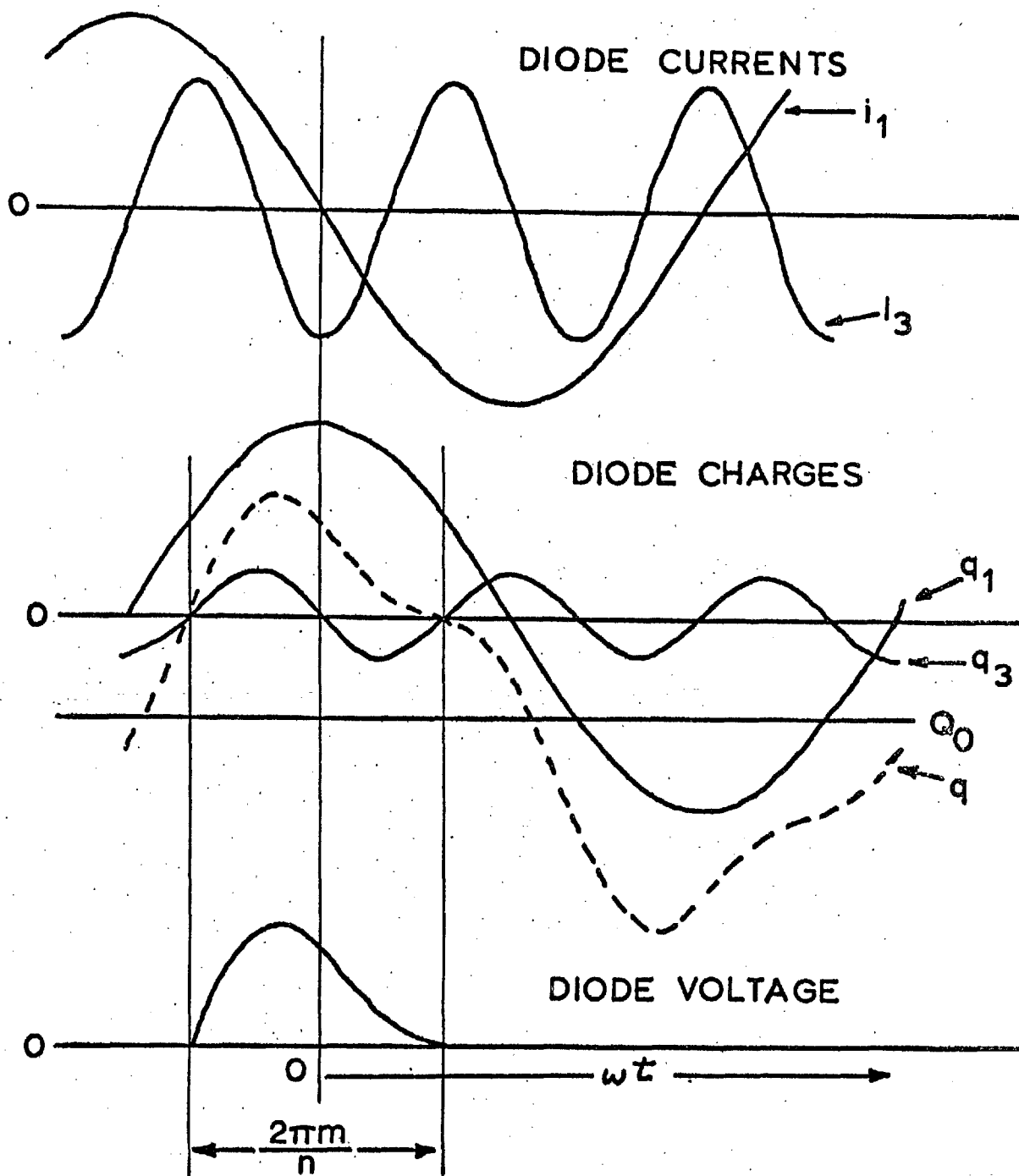
Tripler waveforms to illustrate typical multiplier operation. NLCSE changes state only when harmonic charge component passes through the zero axis (see diode voltage and q_3). The fundamental and harmonic charges are 90 degrees out of phase.

$$q = Q_1(\cos \omega t - \cos m\pi/n) - Q_n \sin n \, \omega t \qquad 4.1$$

From this equation the diode current may be determined as:

$$i = dq/dt$$

$$i = -\omega Q_1 \sin \omega t - n \, \omega Q_n \cos n \, \omega t \qquad 4.2$$

For the NLCSE idealisation of Fig. 4.4a, the voltage v across the diode is:

$$v = q/C_D \quad \text{for } q \geqslant 0$$

and $\quad v = 0 \quad$ for $q \leqslant 0$

By Fourier analysis the component of the diode fundamental voltage in phase with the diode fundamental current may be found. This is the input voltage to the multiplier circuit, in phase with the input current (or diode fundamental current); its amplitude V_1 is:

$$V_1 = \frac{1}{\pi C_D} \int_{-m\pi/n}^{+m\pi/n} \left(Q_1(\cos \omega t - \cos m\pi/n) - Q_n \sin n \, \omega t\right)(-\sin \omega t) d\omega t$$

and since $I_1 = \omega Q_1$ and $I_n = n\omega Q_n$ from Eqn. 4.1 and 4.2,

$$V_1 = \frac{1}{\pi\omega C_D} \left[I_1\left(\frac{\cos 2\omega t}{4} - \cos\frac{m\pi}{n} \cos\omega t\right) + \frac{I_n}{2n}\left(\frac{\sin(n-1)\omega t}{n-1} - \frac{\sin(n+1)\omega t}{n+1}\right) \right]_{-m\pi/n}^{+m\pi/n}$$

$$= \frac{I_n}{\omega C_D} \left(\frac{\sin(m\pi - m\pi/n)}{n\pi(n-1)} - \frac{\sin(m\pi + m\pi/n)}{n\pi(n+1)}\right)$$

$$= \frac{I_n}{\omega C_D} K_1 \qquad 4.3$$

Similarly, the component of diode harmonic voltage in phase with harmonic diode current (or output current) is equal to the load voltage; its amplitude is:

$$V_n = \frac{1}{\pi\omega C_D} \int_{-m\pi/n}^{+m\pi/n} \left(I_1(\cos \omega t - \cos m\pi/n) - \frac{I_n}{n} \sin n \, \omega t\right)(-\cos n \, \omega t) \, d\omega t$$

$$V_n = \frac{-1}{\pi \omega C_D} \left[I_1\left(\frac{\sin(n+1)\omega t}{2(n+1)} + \frac{\sin(n-1)\omega t}{2(n-1)} + \cos\frac{m\pi}{n} \sin n\omega t\right) + \frac{I_n}{n}\left(\frac{-\cos 2n\omega t}{4n}\right)\right]_{-m\pi/n}^{m\pi/n}$$

$$= -\frac{I_1}{\omega C_D}\left(\frac{\sin(m\pi + m\pi/n)}{\pi(n+1)} + \frac{\sin(m\pi - m\pi/n)}{\pi(n-1)}\right)$$

$$= -\frac{I_1}{\omega C_D} K_2 \qquad\qquad 4.4$$

The simplicity of the analysis may now be noted, only two equations are required, defining the parameters K_1 and K_2, and these are exceptionally simple. For example, V_1 is a function of only I_n (assuming a particular multiplication factor n and a particular conduction period m is chosen) and V_n is a function of only I_1. This situation is the outcome of the choice that has been made for the phase and conduction angle relationships. It is found by evaluation of K_1 and K_2 for given values of n and m that the two parameters are, in fact, equal. We shall, therefore, write $K_1 = K_2 = K_G$.

Now the harmonic output is developed across the purely resistive load termination R_L, therefore:

$$V_n = -R_L I_n$$

The input resistance of the multiplier may be determined from the above expression and Eqns. 4.3 and 4.4.

$$R_{in} = \frac{K_1 K_2}{\omega^2 C_D^2} \cdot \frac{1}{R_L}$$

Rewriting we have: $\quad R_{in} = \left(\frac{K_G}{\omega C_D}\right)^2 \cdot \frac{1}{R_L}$ $\qquad\qquad 4.5$

It will be noted that the multiplier, when operated in the assumed mode, has a gyrator like resistance characteristic. Values of K_G are listed for different harmonics and different conduction periods in Table 4.1. Thus the relationship between the input and output resistances of the NLCSE multiplying circuit has been determined.

Earlier it was decided that for simplicity in analysis, the NLCSE would be allowed to enter the forward bias region only once per fundamental cycle. This requirement will be met by ensuring that the rate of change of the harmonic charge is smaller than that of the rate of change of the fundamental charge at the instant the NLCSE changes state.

That is, when: $\omega t = \pm \dfrac{m\pi}{n}$

$$\left| \frac{dq_n}{dt} \right| \leq \left| \frac{dq_1}{dt} \right|$$

From Eqn. 4.1 we have: $\left| n\, Q_n \cos m\pi \right| \leq \left| Q_1 \sin \dfrac{m\pi}{n} \right|$

or $\qquad \dfrac{I_n}{I_1} \leq \sin m\pi/n$

Now since the non-linear capacitance section of the multiplier is 100 per cent efficient with respect to power conversion, we may set a limit on the ratio of the input resistance to the output resistance of the multiplier. This will be called the Minimum Resistance Ratio (MRR).

$$R_{in}\, I_1^{\,2} = R_L\, I_n^{\,2} \qquad\qquad\qquad 4.6$$

Therefore

$$R_L/R_{in} \geqslant \frac{1}{\sin^2(\frac{m\pi}{n})}$$

$$MRR = \frac{1}{\sin^2(\frac{m\pi}{n})} \qquad 4.7$$

From Eqn. 4.7 we can see that R_L must always be greater than or (in special cases) equal to R_{in}. The MRR values are noted in Table 4.1 for various conditions.

4.4 Diode Losses and Efficiency

Earlier, the effect of the diode strays and the way in which these favoured the two-charge circuit configuration was discussed. Accordingly the series resistance will be treated as part of the load resistance and the input resistance as illustrated in Fig. 4.5. Two new resistances will now be defined. R_{in}' is the total input resistance including the loss element r_s and the non-linear multiplying element. R_L' is the useful load resistance connected to the multiplier. That is,

$$R_{in}' = R_{in} + r_s$$

$$R_L = r_s + R_L'$$

The power conversion efficiency of the multiplier may now be determined.

$$\eta = \frac{\text{harmonic power output}}{\text{fundamental power input}}$$

$$= \frac{R_{in}}{R_{in}'} \cdot \frac{R_L'}{R_L}$$

Thus

$$\eta = \frac{R_{in}}{R_{in}+r_s} \cdot \frac{R_L - r_s}{R_L}$$

$$\eta = \frac{1 - r_s/R_L}{1 + r_s/R_{in}} \qquad\qquad 4.8$$

Substituting from Eqn. 4.5 in order to eliminate R_{in}, we have

$$\eta = \frac{1 - r_s/R_L}{1 + r_s R_L (\frac{\omega C_D}{K_G})^2}$$

The most efficient load resistance may be found by differentiating this expression with respect to R_L and setting this equal to zero. It is found that:

$$R_L = \frac{K_G}{\omega C_D} \left[- \frac{\omega}{\omega_{cN}} + (\frac{\omega^2}{\omega_{cN}^2} + 1)^{\frac{1}{2}} \right]^{-1} \qquad\qquad 4.9$$

where

$$\omega_{cN} = \frac{K_G}{r_s C_D}$$

This is the load resistance that results in the maximum possible power conversion efficiency. There are now two conditions to be met by the value of R_L. One is determined by the MRR which ensures that the analysis is applicable and the other condition is that of Eqn. 4.9 for maximum power conversion efficiency. At high frequencies the equation which determines the value of R_L is Eqn. 4.9. At low frequencies Eqn. 4.9 determines the value of R_L if the MRR is equal to 1.0. The effect of a nonunity MRR value on efficiency will be examined later.

The maximum efficiency of the multiplier configuration may be determined by substituting Eqn. 4.9 back into the efficiency expression.

Thus the maximum efficiency of the multiplier is then obtained as:

$$\eta \;=\; 1 + 2\,\frac{\omega^2}{\omega^2_{cN}} - 2\omega/\omega_{cN}(1 + \frac{\omega^2}{\omega^2_{cN}})^{\frac{1}{2}} \qquad\qquad 4.10$$

A plot of maximum efficiency verses normalised frequency is shown in Fig. 4.7 for MRR values of 1.0 and 3.0.

Figure 4.7
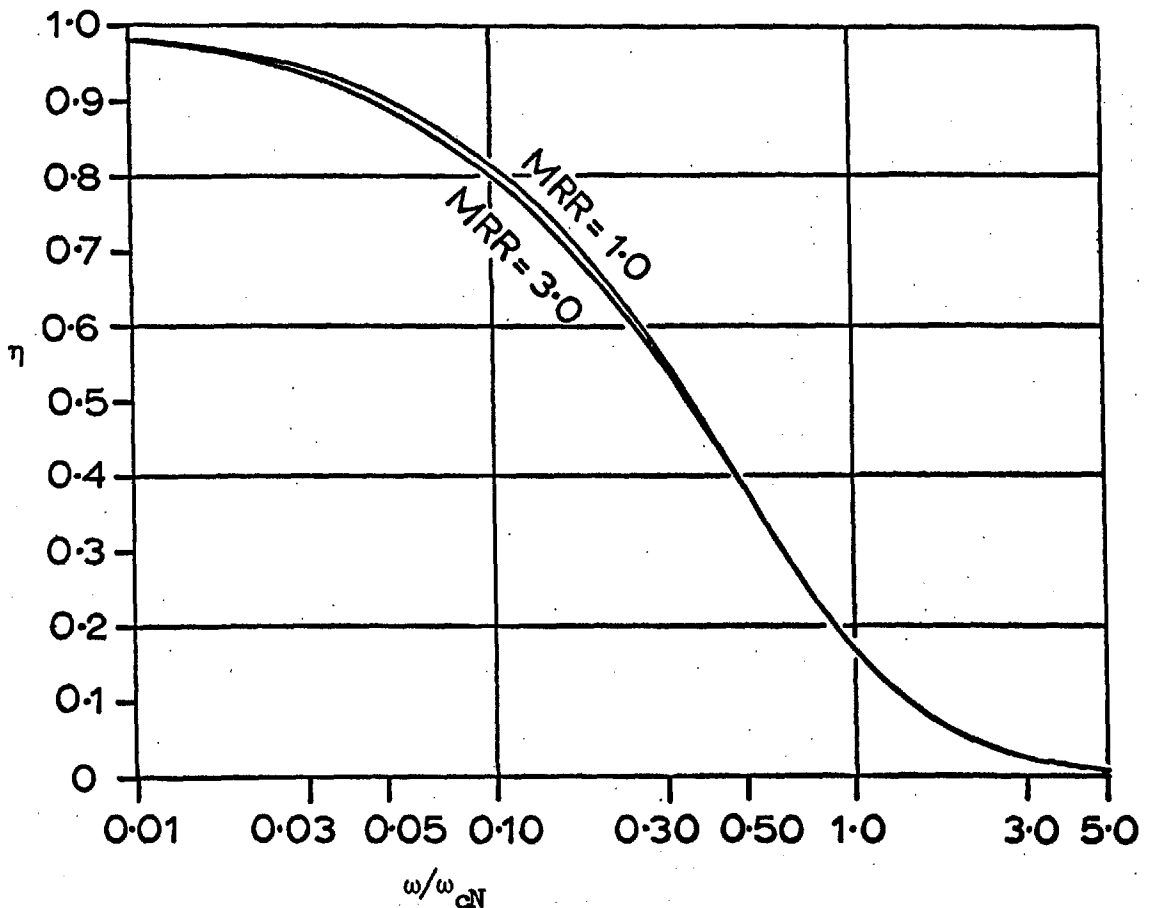
Multiplier efficiency of NLCSE two-charge circuit at medium frequencies for two values of MRR.

The two efficiency curves are separated for low frequencies but merge at about $0.5\omega/\omega_{cN}$; it is noteworthy that the differences between them is always very small. For most practical purposes, the effect on efficiency of a nonunity MRR is almost negligible.

Approximations to Eqn. 4.10 may be developed for high frequencies and low frequencies. At low frequencies the MRR determines the maximum efficiency, and the approximation to this region is best found by referring to Eqns. 4.5, 4.7 and 4.8. Using these equations it may be shown for low frequencies, that:

$$\eta_{LF} = 1 - \frac{\omega}{\omega_{cN}} (MRR^{\frac{1}{2}} + MRR^{-\frac{1}{2}})$$

$$= 1 - \frac{\omega}{\omega_c} K_{LF} \qquad\qquad 4.11$$

where $\omega_c = \dfrac{1}{r_s C}$, $K_{LF} = \dfrac{MRR^{\frac{1}{2}} + MRR^{-\frac{1}{2}}}{K_G}$, $\omega_c = \dfrac{\omega_{cN}}{K_G}$

K_{LF} is referred to as a "loss factor"; values are listed in Table 4.1. In Fig. 4.8 values of K_{LF} are compared with loss factors given by Penfield and Rafuse[35], for varactors operating in the depletion layer capacitance mode with the optimum idler circuit configurations.

To find a high frequency approximation to Eqn. 4.10 it is best to rewrite the equation in terms of a power series:

$$\eta_{hf} = 1 + 2\frac{\omega^2}{\omega^2_{cN}} - 2\frac{\omega^2}{\omega^2_{cN}}(1 + \frac{\omega^2_{cN}}{2\omega^2} - \frac{\omega^4_{cN}}{8\omega^4} + \frac{\omega^6_{cN}}{16\omega^6})$$

$$= \frac{\omega^2_{cN}}{4\omega^2} \qquad\qquad 4.12$$

Figure 4.8

Low frequency loss factor of
multiplier for different multi-
plication numbers (n) where

$$\eta = 1 - K_{LF} \frac{\omega}{\omega_c}$$

Circles represent K_{LF} values for
maximum efficiency solutions
for NLCSE multiplier. Squares
represent values for maximum
figure of merit solutions for
NLCSE multipliers. Crosses
represent values for conventional
varactors with optimum idlers as
per Penfield and Rafuse[35].
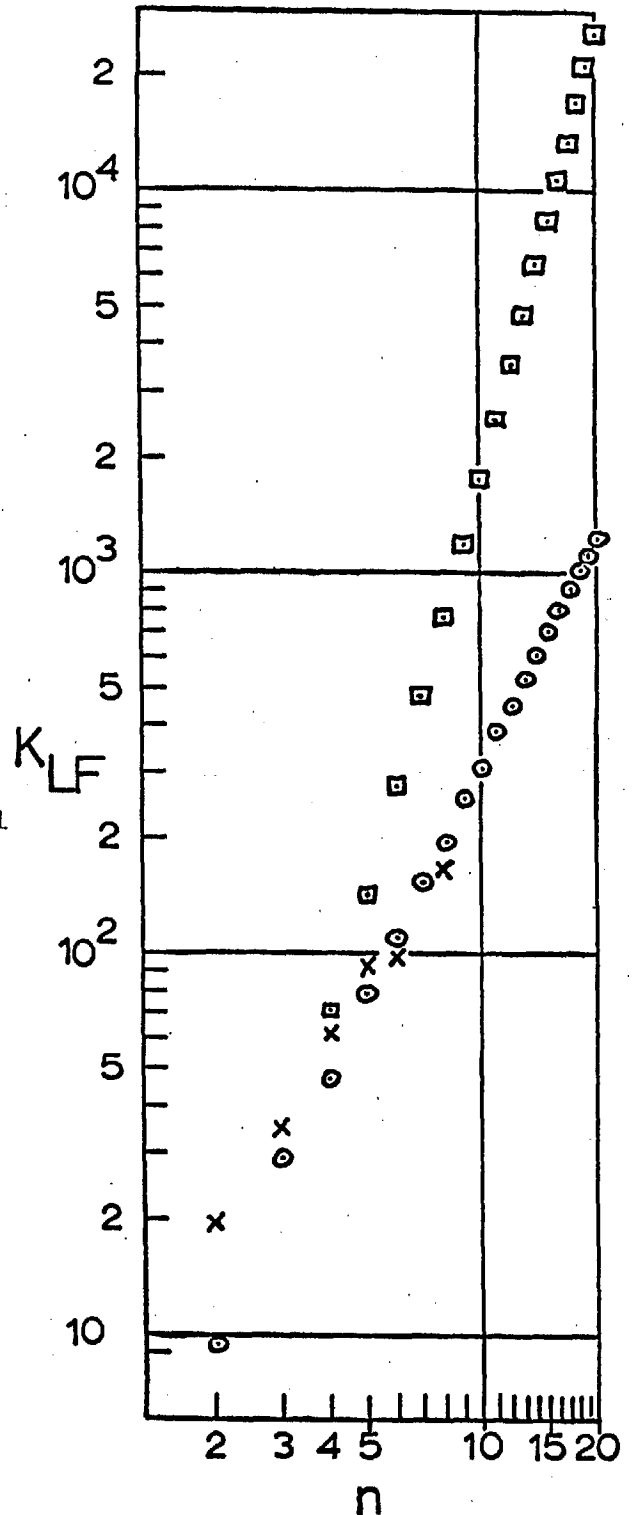
This efficiency is unaffected by the MRR conditions and is accurate if $\omega/\omega_{cN} \geqslant 2$. In the case of the varactor multiplier (depletion layer capacitance mode, with optimum idlers) the efficiency at high frequencies is related to frequency by a higher power than the square law (excepting the doubler) and this makes comparison with the present analysis difficult. Therefore the efficiency will be compared at $\omega = \omega_c$ in Fig. 4.9. The superiority of the charge storage multiplier efficiency increases with increased frequency. At lower frequencies this superiority diminishes.

4.5   Maximum Power Conversion

In the circuit configuration being considered one of three different diode properties may limit the power handling capability of the multiplier. These are reverse breakdown voltage, maximum power dissipation and peak current flow. In a conventional varactor multiplier the reverse breakdown voltage is usually the limiting diode parameter. In the circuit considered here (where, as it will be shown later, efficiency can be traded for an increased power handling capability) the other diode properties, particularly maximum power dissipation, may prove to be the limiting factors.

4.5.1 Reverse breakdown limitation

At low frequencies, it is usually found that the power limiting is caused by the diode reverse breakdown voltage. The following analysis will, however, be made sufficiently general to determine the

Figure 4.9
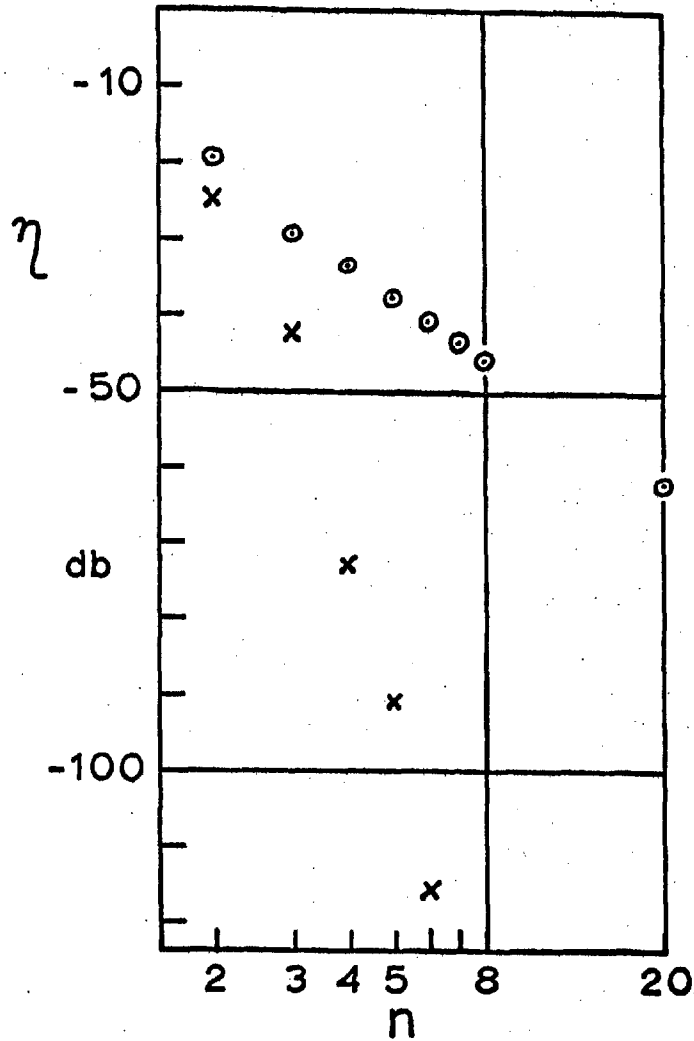
Efficiency of the frequency multiplier at high frequencies $(\omega=\omega_c)$ as a function of harmonic number (n). Circles refer to NLCSE two-charge solutions. Crosses represent solutions for conventional varactors with optimum idlers as per Penfield and Rafuse[35].

output power also at high frequencies. It will be assumed that
the multiplier is operated so that maximum efficiency is attained.
In order that the maximum reverse voltage may be determined we must
determine the maximum charge. To find the maximum value of q we
must first find the relative magnitudes of Q_n and Q_1 in Eqn. 4.1.
The maximum efficiency requirements may determine this ratio, which
may be found through manipulation of Eqns. 4.5, 4.6 and 4.9.
Alternatively the MRR condition of Eqn. 4.7 may define the ratio of
Q_n to Q_1. Defining the corresponding current amplitude ratio as

$$r_I = I_n/I_1 = \frac{nQ_n}{Q_1}$$

we obtain

$$r_I = -\frac{\omega}{\omega_{cN}} + \left(\frac{\omega^2}{\omega^2_{cN}} + 1\right)^{\frac{1}{2}}$$

$$r_I = MRR^{-\frac{1}{2}}$$

we select whichever is the smaller.

4.13

This ratio is substituted into Eqn. 4.1 producing:

$$q = Q_1(\cos \omega t - \cos m\pi/n - r_I/n \sin n \omega t)$$

The maximum value of q is found by setting the derivative of q to
zero. That is:

$$o = \omega Q_1(-\sin\phi - r_I \cos n\phi) \qquad 4.14$$

and $q_{max} = Q_1(\cos\phi - \cos m\pi/n - (r_I/n) \sin n\phi)$

and since $I_1/\omega = Q_1$

$$I_{1max} = \frac{BV_D \, \omega \, C_D}{(\cos\phi - \cos m\pi/n - (r_I/n)\sin n\phi)} \qquad 4.15$$

Where BV_D is the diode reverse breakdown voltage. The input power to the nonlinear charge section of the diode may now be calculated (viz. the input fundamental power dissipated in the diode series resistance having been discounted). Thus

$$P'_{in\ max} = \frac{I_1^2{}_{max}}{2} \cdot R_{in}$$

From Eqns. 4.5, 4.9 and 4.15 we may write:

$$P'_{in\ max} = \frac{BV_D^2 \omega C_D K_G}{(\cos\phi - \cos m\pi/n - (r_I/n)\sin n\phi)^2} \left(-\frac{\omega}{\omega_{cN}} + (\frac{\omega^2}{\omega^2{}_{cN}} + 1)^{\frac{1}{2}} \right) \quad 4.16$$

This is the power input to the nonlinear charge storage section of the diode and to find the output power we need only to subtract the harmonic power loss in the diode; that is, with reference to Fig. 4.5.

$$P_o = P'_{in} \cdot \frac{R_L'}{R_L}$$

$$= P'_{in} \cdot (1 - \frac{r_s}{R_L})$$

Substituting this into Eqn. 4.9 we have:

$$P_o = P'_{in} \left[1 - \frac{\omega}{\omega_{cN}} \left(-\frac{\omega}{\omega_{cN}} + (\frac{\omega^2}{\omega^2{}_{cN}} + 1)^{\frac{1}{2}} \right) \right] \quad 4.17$$

Further, substituting Eqn. 4.16 into Eqn. 4.17 and simplifying, we may write

$$P_{omax} = \frac{BV_D^2 \cdot K_G^2}{r_s} \quad \frac{-2\frac{\omega^2}{\omega^2{}_{cN}}(1 + \frac{\omega^2}{\omega^2{}_{cN}}) + (\frac{\omega}{\omega_{cN}} + 2\frac{\omega^3}{\omega^3{}_{cN}})(1 + \frac{\omega^2}{\omega^2{}_{cN}})^{\frac{1}{2}}}{2(\cos\phi - \cos m\pi/n - (r_I/n)\sin n\phi)^2} \quad 4.18$$

where Eqn. 4.13 defines r_I and Eqn. 4.14 defines ϕ. That is:

$$P_{omax} = \frac{BV_D^2 \ K_G^2}{r_s} \cdot K_{PO}$$

The parameter K_{PO} is a somewhat complicated function of previously defined parameters. In Fig. 4.10 K_{PO} is plotted as a function of normalised operating frequency for conditions of maximum efficiency. The values for odd and even harmonic numbers occupy two different regions, and the extremes of these regions are indicated by solid lines. For the case where the conduction angle is chosen so that efficiency is not maximum, the maximum power output curve is best found by locating the asymptotes of the curve. Once the asymptotes of the K_{PO} versus ω/ω_{cN} curve are found a good approximation to the real curve may be obtained. These asymptotes will now be defined.

For $\omega/\omega_{cN} < 0.2$

we may derive from Eqn. 4.18

$$P_{omax} \approx \frac{BV_D^2 \cdot K_G^2}{r_s} \cdot \frac{\omega/\omega_{cN}}{2(\cos\phi - \cos m\pi/n - \frac{MRR^{-\frac{1}{2}}}{n}\sin n\phi)^2}$$

$$\approx \frac{BV_D^2}{r_s} \cdot \frac{\omega}{\omega_{cN}} \cdot K_G^2 \cdot K'_{PO} \qquad\qquad 4.19$$

Values of K'_{PO} are shown in Table 1.

For the case where $\frac{\omega}{\omega_{cN}} > 1.0$ it may be shown that:

$$P_{omax} \approx \frac{BV_D^2}{r_s} \cdot \frac{K_G^2}{8(1 - \cos m\pi/n)^2} \qquad\qquad 4.20$$

Thus the two asymptotes are defined.

It is useful to compare the low frequency power handling capacity found here with that of a varactor with optimised idler circuits. This comparison will be facilitated if Eqn. 4.19 is rewritt .

Figure 4.10
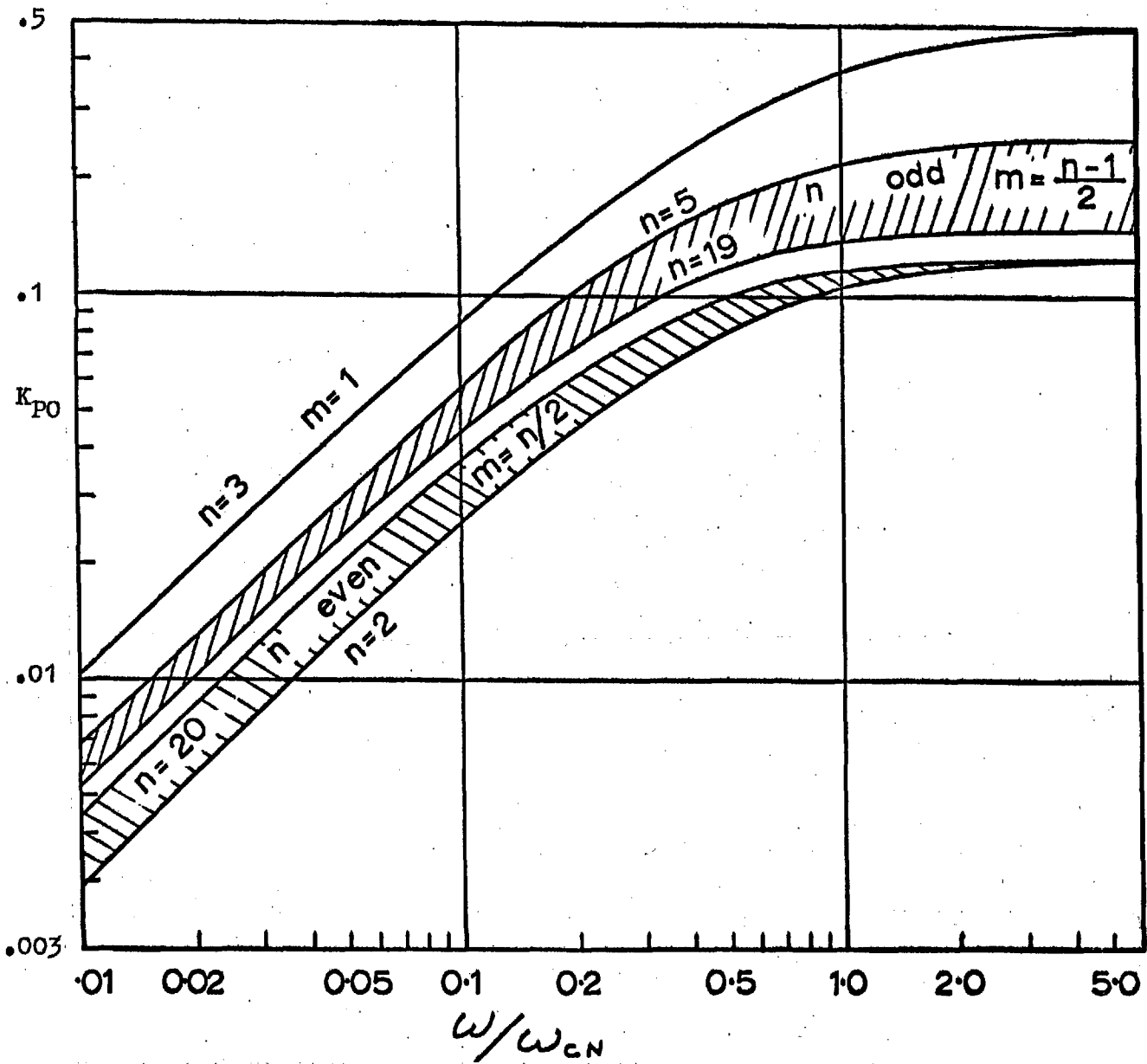
Maximum power output of an NLCSE two-charge multiplier as a function
of frequency, where the diode reverse breakdown voltage is the
limiting parameter.

$$P_{omax} = \frac{BV_D^2}{r_s} \cdot K_G^2 \cdot K_{PO}$$

$$P_{omax} = \frac{BV_D^2}{r_s} \cdot \frac{\omega}{\omega_c} \cdot K_G K'_{PO}$$

where $\omega_c = \omega_{cN}/K_G$

The constant, $K_G K'_{PO}$ is plotted as a function of n and compared with a like constant given by Penfield and Rafuse[35] in Fig. 4.11.

4.5.2 Figure of merit

Step recovery diode multipliers may have, at low frequencies, a very high conversion efficiency but a poor power handling capability (though considerably better than for varactor multipliers). This situation also exists for conventional varactors. However, in the case of a step recovery multiplier, there are methods of increasing the power handling capability. One method, suggested by Scarlett[34] for a doubler, is to add to the depletion layer capacitance (C_D) another external fixed capacitance (C_{EXT}). For example, Eqn. 4.19 may be expressed alternatively as

$$P_{omax} = \frac{BV_D^2}{r_s} \cdot K'_{PO} K_G \cdot \omega r_s C_D$$

and we see that the output power is directly proportional to the magnitude of the idling capacitance C_D. Thus, if this capacitance is doubled, the low frequency power output of the multiplier is doubled. The diode losses are also doubled but this is acceptable if the efficiency of the multiplier is high in the first instance. This external capacitance may be increased to the point where the reactance approaches the impedance of the series strays of the diode. That is:

$$3 \left| r_s + j n \omega L \right| \leqslant \frac{1}{n\omega C_{EXT}}$$

Beyond this point the external capacitance would not behave as an

Figure 4.11

Power handling capability of
a multiplier at low frequencies
as a function of harmonic
number.

$$P_{omax} = \frac{BV_D^2}{r_s} \cdot K_{PO}' K_G \cdot \frac{\omega}{\omega_c}$$

Circles represent values found
for maximum efficiency
solutions for NLCSE multi-
pliers. Squares represent
values found for maximum
figure of merit solutions for
a NLCSE multiplier. Crosses
represent solutions obtained
for conventional varactors
with optimum idlers as per
Penfield and Rafuse[35].
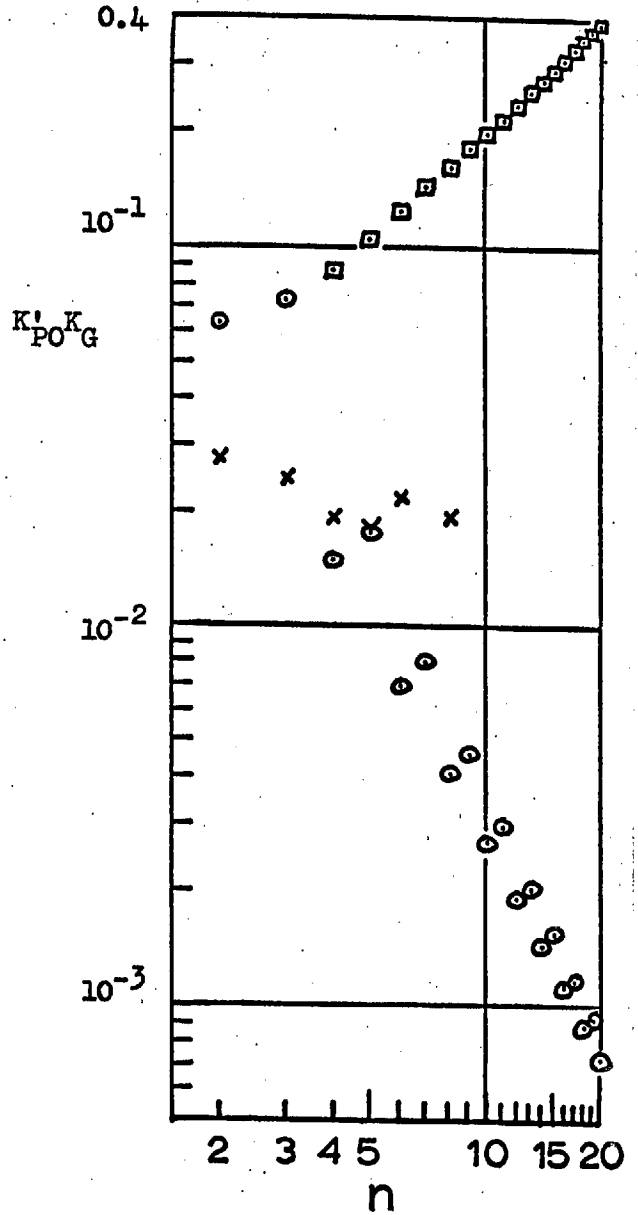
idler in the way predicted. The addition of the external capacitance provides a means of trading efficiency for a better power handling capability. Efficiency calculations, with an added idling capacitance, will be pessimistic because some of the current is shunted around the series resistance r_s, thus reducing the power losses. However, the complication of the analysis necessary for an improved accuracy does not seem warranted. From Eqn. 4.11 we may see that the diode losses are:

$$L_d = K_{LF} \; \omega \; r_s C_D$$

where L_d represents the diode loss.

Now dividing P_{omax} by L_d we obtain a figure of merit for the multiplier operating at low frequencies (P_{omax} being taken from Eqn. 4.19).

$$\frac{P_{omax}}{L_d} = \frac{BV_D^2}{r_s} \cdot \frac{K'_{PO} K_G}{K_{LF}} = \frac{BV_D^2}{r_s} \cdot K_{FM}$$

$$= \frac{BV_D^2}{r_s} \cdot \frac{K_G^2}{2(MRR^{\frac{1}{2}} + MRR^{-\frac{1}{2}})(\cos\phi - \cos m\pi/n - \frac{MRR^{-\frac{1}{2}}}{n}\sin n\phi)^2} \qquad 4.21$$

Thus
$$K_{FM} = \frac{K_G^2}{2(MRR^{\frac{1}{2}} + MRR^{-\frac{1}{2}})(\cos\phi - \cos m\pi/n - \frac{MRR^{-\frac{1}{2}}}{n}\sin n\phi)^2}$$

The constant K_{FM} is a "normalised figure of merit", dependent only on the forward conduction angle: it is evaluated in Table 4.1 for various values of n and m. K_{FM} is, of course, independent of the magnitude of the idling capacitance (C_D).

Another method of increasing the power handling capability for high order harmonics is also available. For low frequencies it has

been found, for high order harmonics, that an increased figure of merit (K_{FM}) may be obtained by choosing a conduction angle larger than the one used for maximum efficiency (i.e. 50% of the fundamental cycle). In this way the power handling capability of a device may be vastly increased and the diode loss will be increased by a much smaller factor. Thus by choosing a longer conduction angle (smaller m) the overall performance of the multiplier is substantially improved for low frequencies. In order to obtain still further increased output power, the conduction angle may be increased to the point of maximum K_{FM} (conduction angle is maximum or m = 1) and then a linear capacitance may be added.

4.5.3   Limit due to diode power dissipation

At very high frequencies, where the conversion efficiency of the multiplier is low, the power handling capability of the circuit is most likely to be limited by maximum power dissipation of the step recovery diode. In this situation maximum output power will always be obtained if the diode is operated in the most efficient mode.

$$P_{in\ max} = \frac{P_{Dis}}{1-\eta}$$

$$P_{omax} = \frac{P_{Dis} \cdot \eta}{1 - \eta} \qquad\qquad 4.22$$

where P_{Dis} is the maximum permitted power dissipation of the diode. Equation 4.21 may be evaluated with the aid of Eqn. 4.11 or 4.12 or Fig. 4.7.

At intermediate frequencies it is difficult to predict which diode parameter will prove to be the limiting one. Equations 4.18

and 4.21 must be evaluated with appropriate constants and diode parameters and the lower value of power accepted as the maximum output power.

4.6   Design Example

The following example has been chosen to verify the foregoing theory and to illustrate some of the practical possibilities that it offers. The multiplier is a tripler (n = 3) with an output frequency of 30 MHz designed to present a 50 ohm input resistance to the source. The diode used had minority carrier lifetime and recovery times of 30 ns. and 300 ps. respectively. The series resistance of this diode was approximately 1.0 ohm and the average value of the depletion layer capacitance (C_D) was 5.0 picofarads. A monitoring current probe used to measure the current through the diode and idling capacitance caused an apparent additional series resistance of 1 . Therefore, effectively $r_s \approx 2.0\Omega$. Design of the multiplier was carried out as follows. For the tripler only one mode of operation is available (n = 3 and m = 1). Calculating ω_{cN} for the diode, using only the diode capacitance as the idler, we find

$$\omega_{cN} = 6.89 \times 10^9 \text{ rad/sec.}$$

and it may then be assumed at 10 MHz ($\omega = 6.28 \times 10^7$) that the low frequency relationships apply.

For

$$R'_{in} = 50\Omega$$

$$R_{in} = 48\Omega \qquad \text{(see Fig. 4.5)}$$

It is likely that the low frequency relations apply even if an idling capacitance is added; thus design is on the basis that the value of R_L is determined by the MRR given in Table 4.1: i.e.

MRR $= 1.33$

$R_L = 1.33 \times 48\Omega$

$ = 64\Omega$

and $R_L' = 62\Omega$

We now determine the correct value of the idling capacitance to give these operating impedances. From Eqn. 4.5 we have,

$$R_L R_{in} = (\frac{K_G}{\omega_C})^2$$

$$C_D = \frac{K_G}{\omega(R_L R_{in})^{\frac{1}{2}}}$$

$$= 19.8 \text{ pfd}$$

$$C_{EXT} = 14.8 \text{ pfd}$$

With the new value of C_D,

$\omega_{cN} = 1.74 \times 10^9 \text{ rad/sec.}$

$\omega/\omega_{cN} = .0361$

From the data of Fig. 4.7 it is found that $\eta = .94$.

The tuned circuits were constructed according to the usual conflicting requirements. Care was taken to ensure that only fundamental and nth harmonic currents would flow in the diode and idler. The circuits should not dissipate significant amounts of the input and output power. The input and output powers should be filtered sufficiently to be free of excessive quantities of unwanted harmonics. In many applications

some of the above requirements will be relaxed. An adjustable self-biasing arrangement was applied to the diode through a choke in the circuit used. The overall filter efficiency was estimated, from measurements, to be 0.57. The calculated overall efficiency (including circuit and diode losses) is 0.536. The measured overall efficiency was 0.555 supporting the theory. A better method of measuring the diode losses alone is by adding a one ohm resistance in series with the diode and measuring the decrease in power output. That is if,

$$\Delta r_s = 1.0\,\Omega$$

it may be shown theoretically that for this particular multiplier

$$\frac{\Delta P_o}{P_o} \approx .033$$

The measured

$$\frac{\Delta P_o}{P_o} \approx .045$$

Thus fair agreement was found between the measured diode series resistance loss and calculated loss. When the output was terminated in 66.0 ohms of resistance the input impedance was measured to be $50 \overset{+}{-} 8\,\Omega$. Agreement is thus obtained with respect to the input and output impedance relationship of the multiplier. The harmonic power output from the diode, after allowances were made for losses in the output tuned circuit, was 68.0 milliwatts. The theoretical output power may be calculated from the observation that the peak reverse voltage on the diode was 22.0 volts. Using Fig. 4.10 the calculated power output is found to be 43.6 milliwatts, which is in approximate agreement with the measurement.

4.7   Discussion and Conclusions

In the analysis presented, perfect filtering circuits have been assumed. For rigorous application of the theory care must be taken to obtain a close approximation of the actual to the assumed circuit environment. For example, all practical filters cause apparent capacitive or inductive paths to ground. If the filters are badly chosen, the filter capacitances may exceed the idling capacitance of the diode. Thus, for accurate application of the theory, the filters should be designed to minimise admittance paths, from the high end of the diode to ground, for all harmonics. For many applications, circuit simplicity will take priority over a close adherance to the theory.

Limitations have been placed on the operation of the multiplier in order that the performance could be evaluated analytically. In spite of these limitations the calculated performance of the simple charge storage multiplier considered, is equal to, or superior to the theoretical performance of conventional varactors operating in optimised (and sometimes complex) circuit environments. The successful construction and adjustment of the simple circuit, analysed here, is much more feasible than the construction and adjustment of a complex circuit involving many idlers.

The analysis presented has given performance figures that are in agreement with figures produced by Steinbrecher[18]; these figures are indicated in Table 4.1. Steinbrecher[36] has also analysed minority carrier charge storage multipliers employing tuned idlers

at all harmonics of the drive frequency below the output frequency
and these normally have efficiency and power output performance
significantly superior to those reported here. The exception occurs
at very high frequencies (i.e. n ω >ω_c), where the simple circuit is
likely to have superior conversion efficiencies. In a multiplier,
the high frequency efficiency falls according to $(\frac{\omega}{\omega_c})^{-P}$. The value
of P increases with the number of idlers used. Thus, at high frequencies
the efficiency of multipliers with idlers falls very rapidly (with
increasing frequency), whereas the efficiencyof multipliers without idlers
falls at a square law rate. Hence, at high frequencies the multiplier
with all idlers will have, at least, a reduced superiority or even
an inferior performance. With all idlers present, the multiplier
requires a very complex circuit, particularly for high orders of
multiplication. Thus, the simple two-charge circuit analysed here is
likely to be preferably in at least two circumstances: where circuit
complexity must be avoided, and where the output frequency is very high
so that nothing is gained by a large number of idlers.

The circuit characteristics of the multiplier vary considerably
as the conduction angle (or m) is varied. In this analysis it is found
that the efficiency is maximum if the conduction period is equal to
one half of the fundamental period. The efficiency decreases
symmetrically if the conduction angle is made shorter or longer
(see how K_{LF} varies as a function of m in Table4.1 with n = 10).
It is found at low frequencies that the maximum power output of the
circuit is greatest if the conduction angle is large (i.e. as m → 0).

The figure of merit used indicates a compromise between power handling capacity and losses in the diode at low frequencies. Thus in Table 4.1, two operating conditions (for $n > 3$) are considered: the point where the best efficiency occurs and the point where the best figure of merit occurs. In the multipliers considered, maximum power handling capacity and maximum figure of merit occur at the same conduction angle. These multipliers are thus very versatile as the conduction angle may be varied to provide high efficiency at high frequencies or alternatively high powers at low frequencies. This flexibility of operation does not exist in conventional varactors where the higher power handling capacity and higher efficiency occur at virtually the same operating conditions. The versatility of this circuit is further enhanced since the characteristic impedance is directly proportional to the idling capacitance, which may be varied. The idling capacitance (as well as conduction angle just discussed) can be varied to favour either high efficiency or high power operation. Thus a given diode operating in the charge storage mode should have a broad range of application, compared with a similar varactor.

Table 4.1

n	m	K_G	MRR	K_{LF}	K'_{PO}	$K_G K'_{PO}$	K_{FM}
2	1*	.2122	1.0	9.42	.296	.629 x 10^{-1}	.667 x 10^{-2}
3	1	.689 x 10^{-1}	1.333	2.93 x 10^4	1.05	.722 x 10^{-4}	.246 x 10^{-2}
4	1*	.3001 x 10^{-1}	2.00	7.069 x 10^4	2.93	.879 x 10^{-4}	.124 x 10^{-2}
	2*	.4244 x 10^{-1}	1.00	4.712 x 10^4	.354	.150 x 10^{-1}	.319 x 10^{-3}
5	1	.1559 x 10^{-1}	2.894	1.468 x 10^2	6.76	.105	.718 x 10^{-3}
	2	.2523 x 10^{-1}	1.106	7.938 x 10^4	.708	.179 x 10^{-1}	.225 x 10^{-3}
6	1*	.9095 x 10^{-2}	4.00	2.749 x 10^4	1.36 x 10^1	.124	.450 x 10^{-3}
	3*	.1819 x 10^{-1}	1.00	1.10 x 10^2	.386	.703 x 10^{-2}	.639 x 10^{-4}
7	1	.5755 x 10^{-2}	5.31	4.759 x 10^2	2.47 x 10^1	.142	.299 x 10^{-3}
	3	.1293 x 10^{-1}	1.052	1.547 x 10^2	.624	.807 x 10^{-2}	.522 x 10^{-4}
8	1*	.3367 x 10^{-2}	6.828	7.747 x 10^2	4.17 x 10^1	.161	.208 x 10^{-3}
	4*	.1011 x 10^{-1}	1.00	1.979 x 10^2	.407	.412 x 10^{-2}	.208 x 10^{-4}
9	1	.2722 x 10^{-2}	8.549	1.200 x 10^2	6.63 x 10^1	.180	.150 x 10^{-3}
	4	.7837 x 10^{-2}	1.031	2.552 x 10^2	.588	.461 x 10^{-2}	.181 x 10^{-4}
10	1	.1937 x 10^{-2}	10.47	1.784 x 10^2	1.00 x 10^2	.200	.112 x 10^{-3}
	2	.3780 x 10^{-2}	2.894	6.056 x 10^2	.873 x 10^1	.330 x 10^{-1}	.545 x 10^{-4}
	3	.5203 x 10^{-2}	1.528	3.931 x 10^2	.215 x 10^1	.112 x 10^{-1}	.285 x 10^{-4}
	4*	.6116 x 10^{-2}	1.106	3.274 x 10^2	.833	.509 x 10^{-2}	.156 x 10^{-4}
	5*	.6431 x 10^{-2}	1.00	3.110 x 10^2	.422	.271 x 10^{-2}	.872 x 10^{-5}
	6	.6116 x 10^{-2}	1.106	3.274 x 10^2	.258	.158 x 10^{-2}	.481 x 10^{-5}
	7	.5202 x 10^{-2}	1.528	3.931 x 10^2	.182	.947 x 10^{-3}	.241 x 10^{-5}
	8	.3779 x 10^{-2}	2.894	6.057 x 10^2	.145	.548 x 10^{-3}	.904 x 10^{-6}
	9	.1986 x 10^{-2}	10.47	1.785 x 10^3	.129	.255 x 10^{-3}	.143 x 10^{-6}
11	1	.1495 x 10^{-2}	12.60	2.563 x 10^2	1.146 x 10^2	.219	.854 x 10^{-4}
	5	.5251 x 10^{-2}	1.021	3.809 x 10^2	.568	.298 x 10^{-2}	.783 x 10^{-5}
12	1*	.1152 x 10^{-2}	14.93	3.578 x 10^2	2.07 x 10^2	.238	.666 x 10^{-4}
	6*	.4452 x 10^{-2}	1.00	4.492 x 10^2	.432	.193 x 10^{-2}	.428 x 10^{-5}
13	1	.9069 x 10^{-3}	17.46	4.871 x 10^2	2.84 x 10^2	.258	.529 x 10^{-4}
	6	.3762 x 10^{-2}	1.015	5.317 x 10^2	.555	.209 x 10^{-2}	.393 x 10^{-5}
14	1*	.7265 x 10^{-3}	20.20	6.492 x 10^2	3.81 x 10^2	.277	.427 x 10^{-4}
	7*	.3265 x 10^{-2}	1.00	6.126 x 10^2	.440	.144 x 10^{-2}	.235 x 10^{-5}
15	1	.5910 x 10^{-3}	23.13	8.491 x 10^2	5.02 x 10^2	.296	.349 x 10^{-4}
	7	.2827 x 10^{-2}	1.011	7.076 x 10^2	.546	.154 x 10^{-2}	.218 x 10^{-5}
16	1*	.4871 x 10^{-3}	26.27	1.092 x 10^3	6.43 x 10^2	.316	.289 x 10^{-4}
	8*	.2497 x 10^{-2}	1.00	8.011 x 10^2	.447	.112 x 10^{-2}	.139 x 10^{-5}
17	1	.4062 x 10^{-3}	29.62	1.385 x 10^4	8.25 x 10^2	.335	.242 x 10^{-4}
	8	.2201 x 10^{-2}	1.009	9.086 x 10^2	.540	.119 x 10^{-2}	.131 x 10^{-5}
18	1*	.3423 x 10^{-3}	33.16	1.733 x 10^4	1.04 x 10^3	.355	.205 x 10^{-4}
	9*	.1971 x 10^{-2}	1.00	1.015 x 10^3	.452	.891 x 10^{-3}	.873 x 10^{-6}
19	1	.2911 x 10^{-3}	36.91	2.144 x 10^4	1.29 x 10^3	.374	.175 x 10^{-4}
	9	.1762 x 10^{-2}	1.007	1.135 x 10^3	.535	.943 x 10^{-3}	.831 x 10^{-6}
20	1*	.2496 x 10^{-3}	40.86	2.623 x 10^4	1.58 x 10^3	.394	.150 x 10^{-4}
	10*	.1596 x 10^{-2}	1.00	1.253 x 10^3	.456	.728 x 10^{-3}	.581 x 10^{-6}

* In these rows, the constants K_G, K_{LF} and $K_G K'_{PO}$ have the same values as constants determined by Steinbrecher[35].

CHAPTER FIVE

TRANSISTORISED NONLINEAR OUTPUT FREQUENCY MULTIPLIERS

5.1 Introduction

It has been known for some time that the base collector depletion layer capacitance of the transistor could be used effectively for parametric applications[37]. The use of the transistor simultaneously as an amplifier and a parametric frequency multiplier[13] was first described in 1964. Since then transistor NOM operation has gained widespread acceptance and now manufacturers often list data of NOM performances for uhf power transistors.

5.1.1 Available output nonlinearities

A systematic study of the transistor underlines the possibility of using the transistor in a NOM mode. The presence of a high quality nonlinear depletion layer capacitance is now very widely recognised and it is clear that efficient frequency multiplication is possible using it.

In Chapter Two another frequency multiplication mode becomes evident. Examination of the operation of the input circuit of the NIAM (using Fig. 2.16) shows that if the conduction angle (2α) is made small the input current of any harmonic (i_{Bn}) is larger than the fundamental base current. The action of charge storage in the intrinsic base causes this and a high efficiency frequency multiplication mechanism is suggested. The mechanism has, in fact, provided very good performance in high efficiency, high power frequency

multipliers. Devices utilising this principle have a variety of
names, including NLCSE and step recovery diodes. Step recovery action
(of current) has already been noticed in the transistor[31, 46] but it
has not hitherto been deliberately applied to the transistor operating
in the NOM mode.

In addition to the above two nonlinear reactances, the collector-
base diode contains two nonlinear resistance transition sections
(discussed in Section 1.4.2). Frequency multiplication using the
nonlinear resistance elements is not considered because the power
conversion efficiency is low[47, 48], and other high efficiency
mechanisms are available.

5.1.2   Merits of using an output nonlinearity

The intrinsic base of the transistor, when operated as a
common emitter amplifier, produces a current gain that falls at
6db/octave at high frequencies. The intrinsic base may be thought
of as a low-pass filter with gain. If the frequency multiplication
is carried out at the transistor input, the desired harmonic current
suffers attenuation (relative to the fundamental current). On the
other hand, in the NOM the transistor amplifies the fundamental
power which is converted into a harmonic power at the transistor
output. The current gain (and hence power gain) of the transistor
is higher in the NOM (than the NIAM) for a given output frequency.
Thus the transistor NOM would be expected to give good performance
on the assumption that the frequency multiplication at the output
is moderately efficient.

5.1.3   Nonlinear output multiplier: assumptions made in analysis

Transistor NOM operation has received analytical treatment, by other workers[14, 22, 38, 39], on the assumption that a normal transistor amplifier and a separate varactor are connected together by ideal tuned circuits. Similar assumptions are adopted here, and the chief deviation from previous work occurs in regard to the mechanism of frequency multiplication.

The above characterisation of the transistor NOM is very much idealised. For example, in the actual device a compromise must be found between the best input resistance for most efficient frequency multiplication and the best load resistance for maximum amplifier output. In addition, the amplifying and multiplying sections of the transistor are not isolated by ideal filters and current and voltage harmonics (generated by the nonlinear output element) are able to feed back into the input circuit of the transistor. The feedback is likely to modify the operation of NOM but a detailed analysis would be impossibly involved. The effect of the feedback is, chiefly, modification of the power gain of the transistor NOM and reduction of stability (possibility of unwanted oscillations). Such feedback seems to stem from the common lead inductance, the magnitude of which depends very much on the transistor packaging[44]. Transistor NOM circuits are operated in both the common emitter and common base configurations, one of which normally has the better stability. The configuration that shows the best stability is likely to be different, depending on the transistor type.

The collector-base varactor of a transistor (or NLCSE, depending on the mode of multiplication) is a distributed device (much more so than for a conventional varactor or NLCSE). See Fig. 3.1. However, for the treatment of analysis the collector-base varactor is represented by a single nonlinear capacitance and a single resistance - the usual representation for a varactor or a NLCSE diode.

When setting up a transistor NOM, it is useful to operate the circuit first as an amplifier. In this way, an efficient input circuit can be arranged and the performance of the transistor as an amplifier can be assessed. Normally the transistor is operated so that the collector conducts during most of the fundamental cycle and harmonic generation due to nonlinear input effects is small. The performance of the amplifier is treated as a function of collector direct current, it being the best indication of the power drive at the transistor input (applied input power plus feedback power to input). The circuit is then modified so that NOM operation is attained. The performance of the NOM may be compared with that of the amplifier and it is possible to deduce the power conversion efficiency of the output multiplication process on the assumption that the performance of the amplifying section of the transistor is unchanged.

5.1.4   Typical NOM circuits

In this section transistor NOM circuits, developed by other workers[14, 39, 42], will be examined and their principles of operation explained. The input circuitry to a transistor NOM is identical to that of an amplifier. The output circuit must be designed so that the

fundamental power is prevented from leaving the transistor, being instead converted into output harmonic power. The nonlinear collector-base capacitance is resonated to the necessary idler frequencies (including the fundamental) of the NOM, the desired harmonic power is filtered off at the collector of the transistor and fed into the load resistance via a matching circuit. Two typical NOM circuits are shown in Fig. 5.1. The circuit shown in Fig. 5.1(a) operates in a fairly obvious way, as noted in the figure, and is most suitable for doubling: a filter blocks the fundamental power from leaving the transistor and another section filters and matches the second harmonic into the load. The circuit of Fig. 5.1(b) is particularly adapted for high factors of frequency multiplication (viz. greater than two): the series tuned idling circuits can be adjusted individually (a minimum of interaction is encountered as each series tuned circuit has a large reactance except at the frequency being tuned). The two series tuned circuits (C_1, L_1 and C_2, L_2) resonate the nonlinear capacitance to the fundamental and second harmonics and the desired output frequency (third or fourth harmonic) is filtered and matched by C_3, L_3 and C_4.

The transistors shown in Fig. 5.1 are operated in the common base configuration, but the common emitter configuration could be used equally well. In the common emitter configuration it is necessary, in theory, to have a series tuned circuit for each harmonic frequency to earth, in order to provide a low impedance path for the

Figure 5.1

Transistor NOM Circuits

Biasing is omitted.
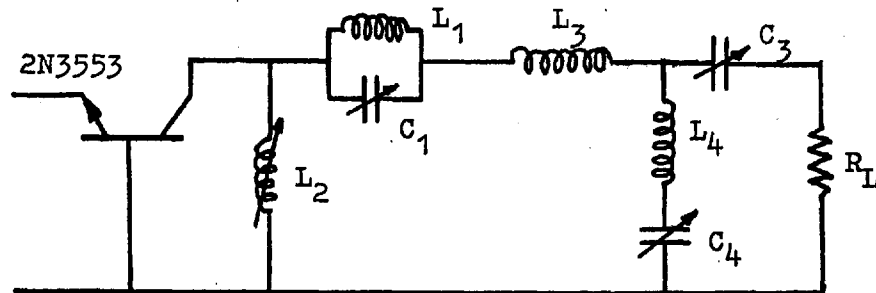
(a)

A doubler circuit[39]. C_1 is adjusted to resonate at, and reject
the fundamental frequency. L_2 is adjusted to resonate the average
value of collector-base capacitance to the fundamental frequency.
C_3 and C_4 are adjusted to filter and match the second harmonic
into the load.
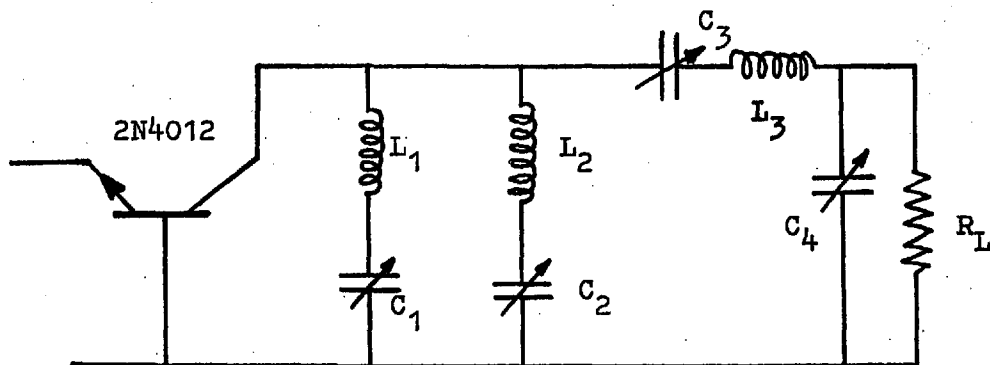
(b)

A transistor tripler or quadrupler[39]. C_1 is used to resonate
the fundamental power; C_2 is used to resonate the second
harmonic power. The output power is filtered and matched by
the adjustment of C_3 and C_4.

harmonic currents passing through the varactor. However, in practice such additional circuitry is not necessary, the reactance to earth of the input circuit to each harmonic being tuned out by the filters at the transistor output.

A simplified equivalent circuit of a transistor NOM output is shown in Fig. 5.2. The output multiplication section is transformed into a circuit similar to that employed in the analysis of varactor or NLCSE frequency multipliers. The transformation is quite accurate. The performance of varactor multipliers may be predicted from the work of Penfield and Rafuse[35]. NLCSE multiplier performance is estimated from the results of Chapter Four and of Steinbrecher[18].

5.2   A VHF Amplifier and Doubler

A VHF doubler using a power transistor was constructed, and the performance and operating conditions were examined carefully. A Pacific Semiconductor Inc. transistor, type PT530, was used both in the common base and emitter configuration. The performances of the two were virtually identical. The common base performance is presented here as more data was collected for this configuration. The collector of the PT530 is connected internally to the encapsulating can and for best heat dissipation the collector must be earthed. Thus the amplifying and multiplying circuits are complicated slightly, but the theory of operation is unchanged. The transistor is first operated as an amplifier for purposes of comparing the amplifier and doubler operation.

Figure 5.2

(a)
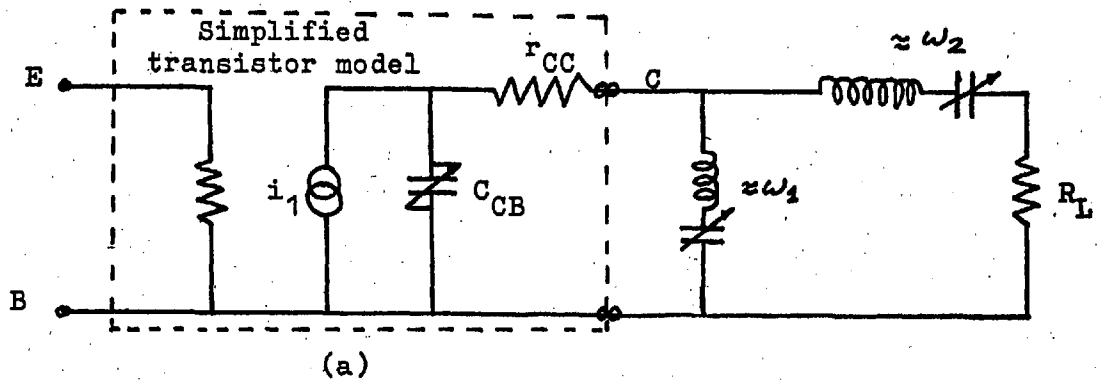
Simplified equivalent circuit of a transistor nonlinear output
doubler. The circuit may be transformed into a familiar
frequency multiplication circuit, as below.

(b)
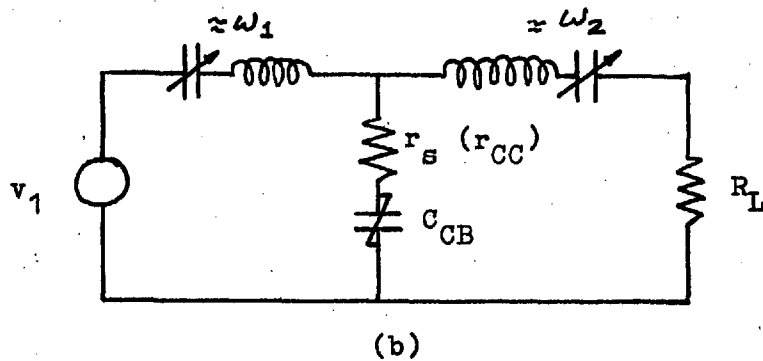
The transformation is quite accurate since the reactive input
and output powers are, typically, five times greater than the
real powers[35].

5.2.1   The vhf amplifier and circuit

Operation of the transistor as an amplifier permitted the optimisation of the circuit layout and components. The transistor was operated with a zero input voltage bias. In this way, the collector conduction angle and hence collector current efficiency (η_{CI}), were essentially constant. The measurement set up and amplifying circuit are shown in Figs. 5.3 and 5.4 respectively. In the amplifier it was important to adjust L_1 and L_2 carefully, to effect the best possible neutralisation. The collector voltage was applied with the output circuit disconnected and a high power, high impedance source connected to the base terminal; L_2 was then adjusted for maximum base voltage swing and L_1 was adjusted for minimum 50 MHz power at the input port which was passively terminated by 50Ω. For final adjustment of L_1 and L_2 the base voltage swing was approximately the same as when the amplifier was operating (about 50 volt peak to peak, in this case). After the neutralisation was carried out the output circuit was reconnected. In operation all variable components (except L_1 and L_2) in the amplifier circuit were adjusted for maximum 50 MHz power in the load. The output power, and collector power conversion efficiency are shown in Fig. 5.5 as a function of direct collector current (I_{CO}). The output power is shown as a function of input power in Fig. 5.6. The input, collector and output voltage waveforms and collector current waveform of the transistor amplifier, operating under typical conditions, are shown in Fig. 5.7. The

Figure 5.3

VHF measurement set up.
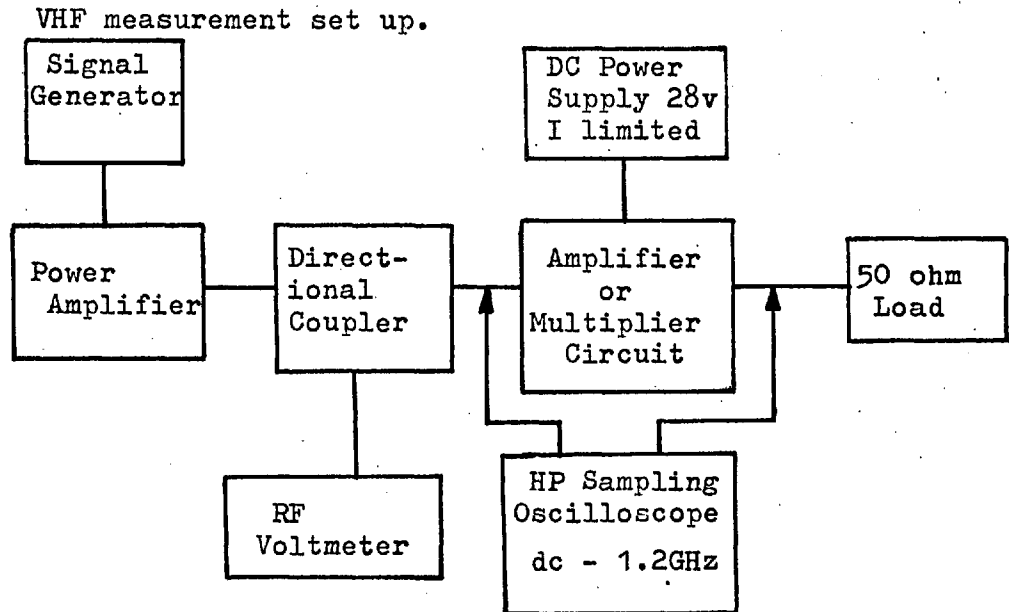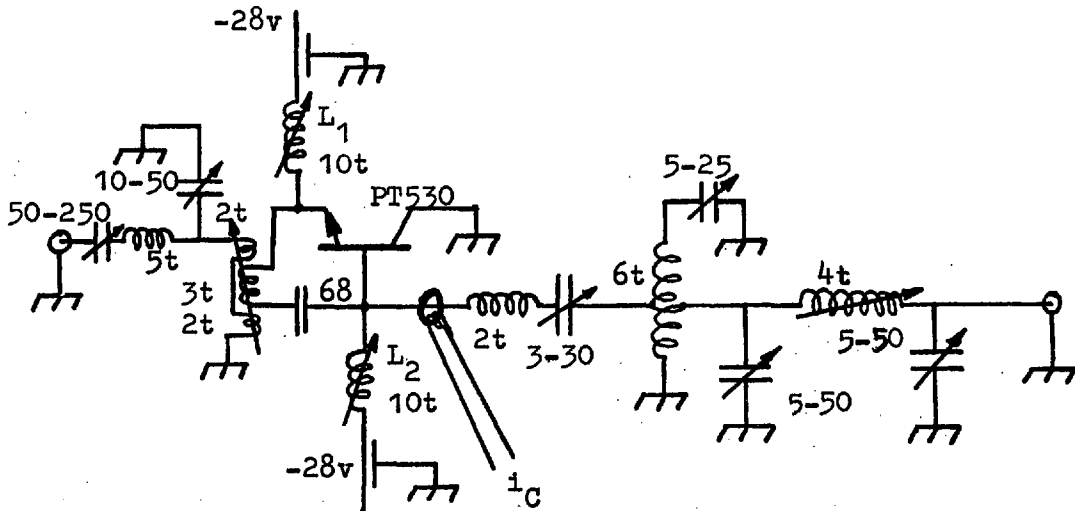
Figure 5.4

VHF amplifier circuit. The input frequency is 50 MHZ. All capacitances are marked in picofarads. All inductances have coil diameters of $\frac{1}{2}$ inch except L_1 and L_2 which have diameters of $\frac{1}{4}$ inch.

Figure 5.5
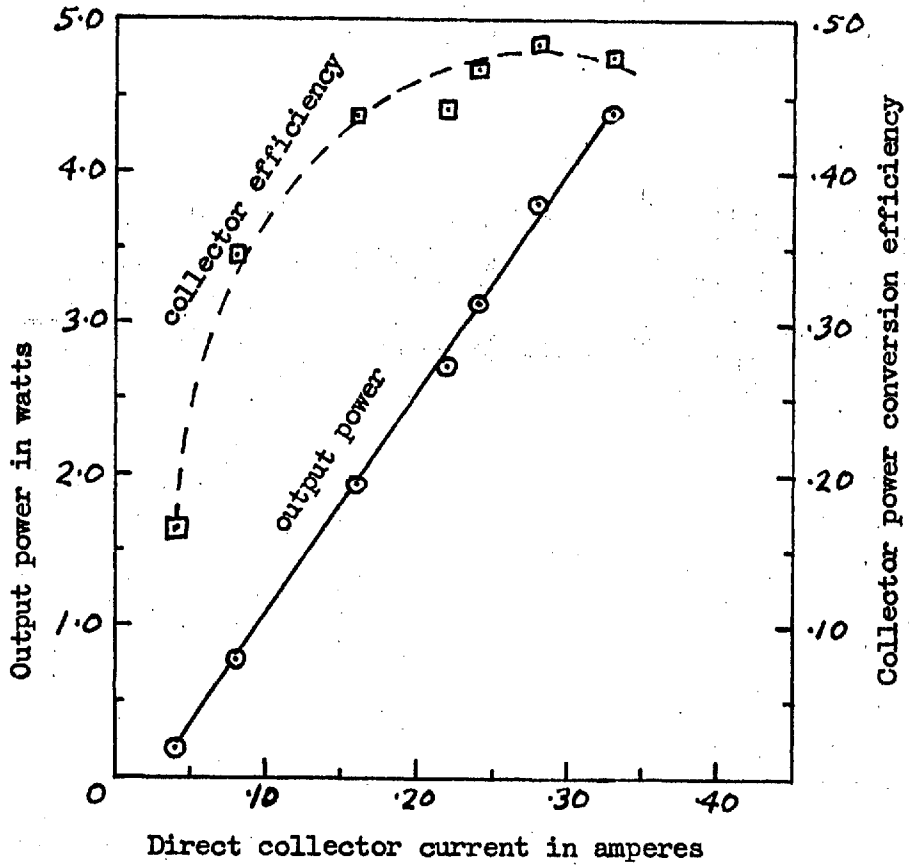
Output characteristics of the transistor amplifier operating at 50 MHz.

Figure 5.6
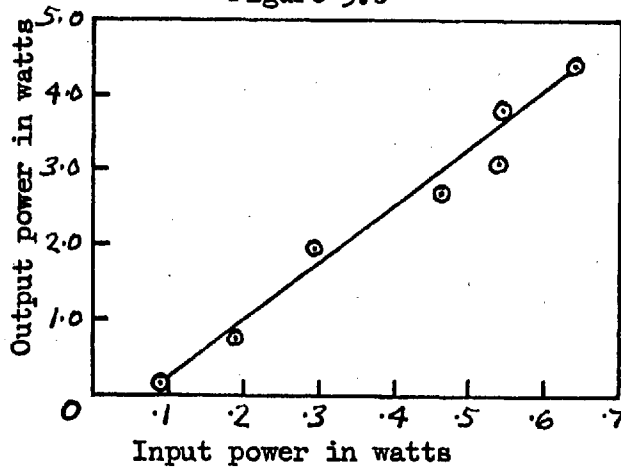
Power gain characteristics of the transistor amplifier operating at 50 MHz.

Figure 5.7   161
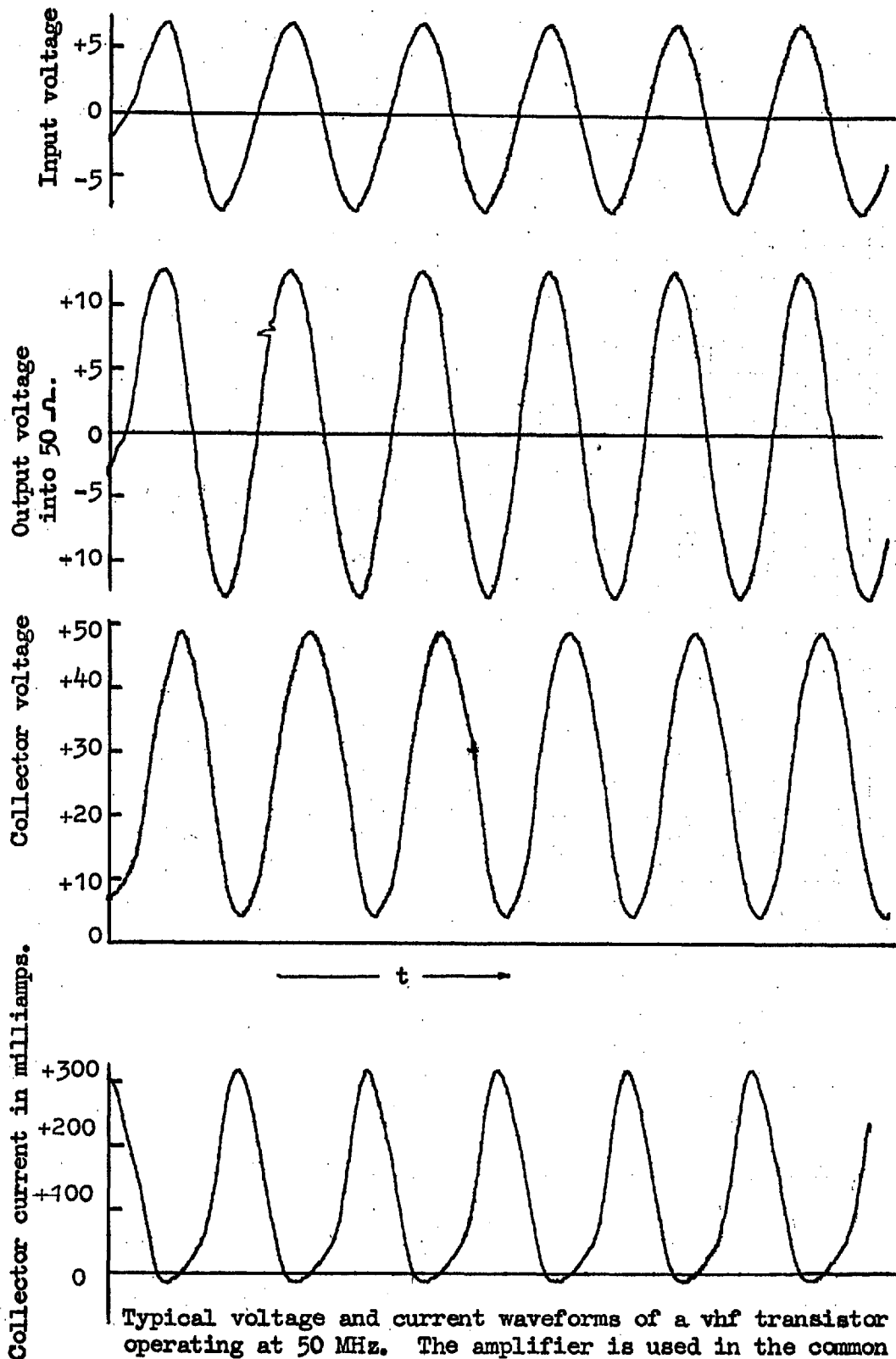
Typical voltage and current waveforms of a vhf transistor amplifier
operating at 50 MHz. The amplifier is used in the common base,
grounded collector mode. Measurements are made treating the base
as zero potential.

amplifier waveforms are very similar to those predicted in Chapters Two and Three, the collector sine voltage has good purity and the collector current showing the effect of capacitive current flow - particularly at one period by a reverse collector current. The performance of the amplifier is not treated theoretically as the theory of Chapters Two and Three has already been verified. The investigation develops a standard here to compare doubler performance with. Successful operation of the amplifier - judged by circuit stability and by the achievement of the manufacturer's electrical specifications for the particular transistor - facilitates the doubler construction.

5.2.2 The vhf doubler circuit and performance

The input section of the doubler circuit was identical to the amplifier. The output section was modified so that the fundamental power was unable to leave the transistor and second harmonic power was extracted from the transistor and matched into the load. The circuit that resulted in the best multiplier performance is shown in Fig. 5.8. The measurement set-up was the same as shown in Fig. 5.3. The tuning elements of the doubler (shown in Fig. 5.8) were adjusted for maximum second harmonic power output. The output power and the collector power conversion (multiplication) efficiency are shown in Fig. 5.9 as a function of direct collector current (I_{CO}). The harmonic output power is shown in Fig. 5.10 as a function of input power.

Figure 5.8
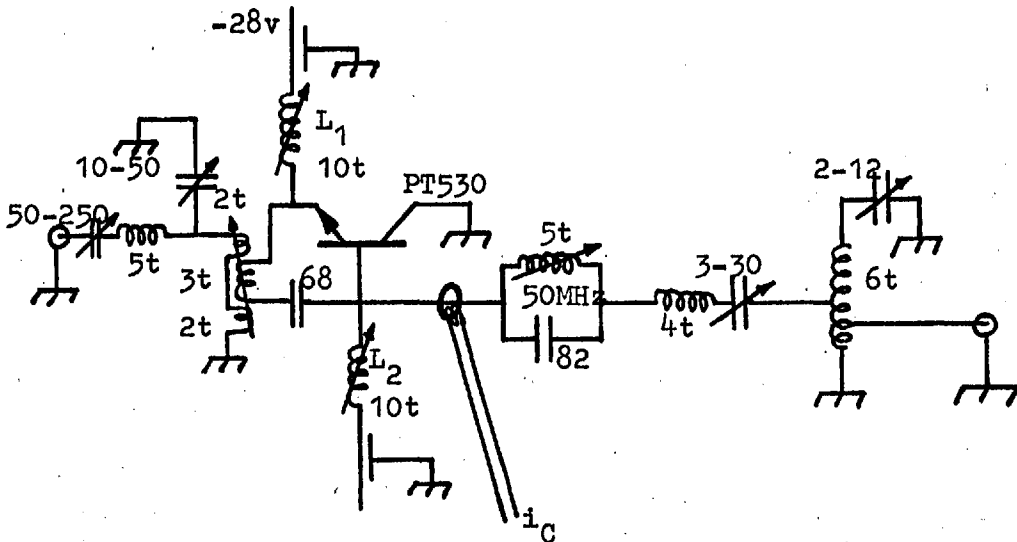
A vhf doubling circuit. The input circuitry is adjusted for best amplifier performance. The output circuitry is adjusted for maximum power output at 100 MHz.

Figure 5.9
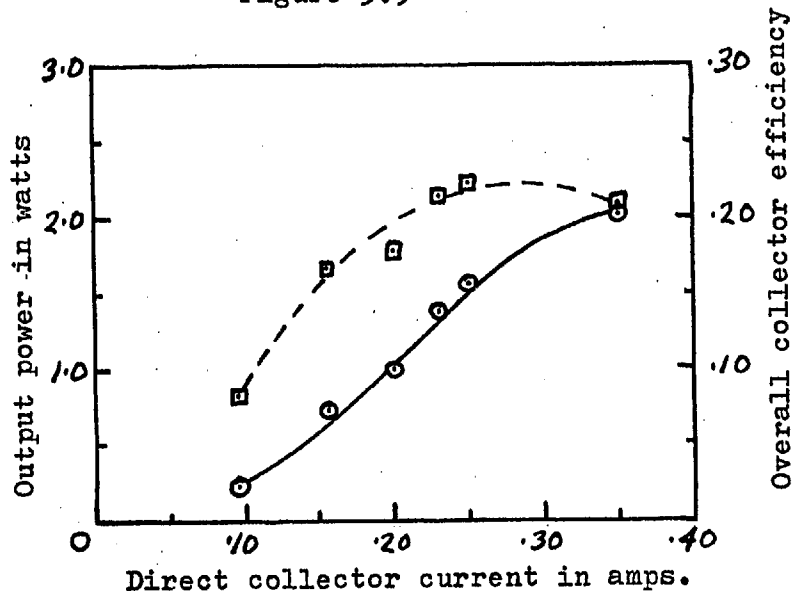
Output characteristics of a vhf transistor nonlinear output doubler. The output frequency is 100 MHz.

Figure 5.10
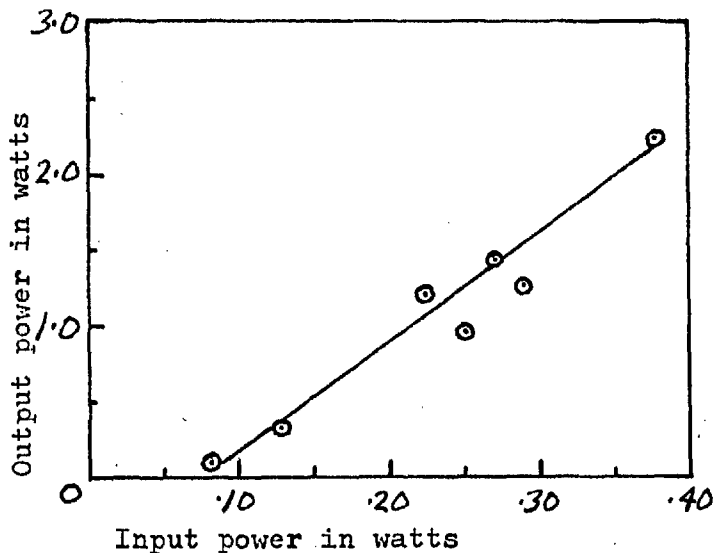
Power gain characteristics of the vhf doubler with an output
frequency of 100 MHz.

The input power to the doubler may be compared with that of the
amplifier and it is found that the output power for a given input
is very nearly the same in spite of frequency multiplication losses.
The similarity is attributed to a positive feedback in the doubler.
Voltage and current waveforms typical of the doubler are displayed
in Fig. 5.11. Characteristic of the doubler is the occurence of
fundamental and second harmonic voltage on the collector with strong
bottoming of the collector voltage. The collector current is
composed, primarily, of the second harmonic.

Figure 5.11
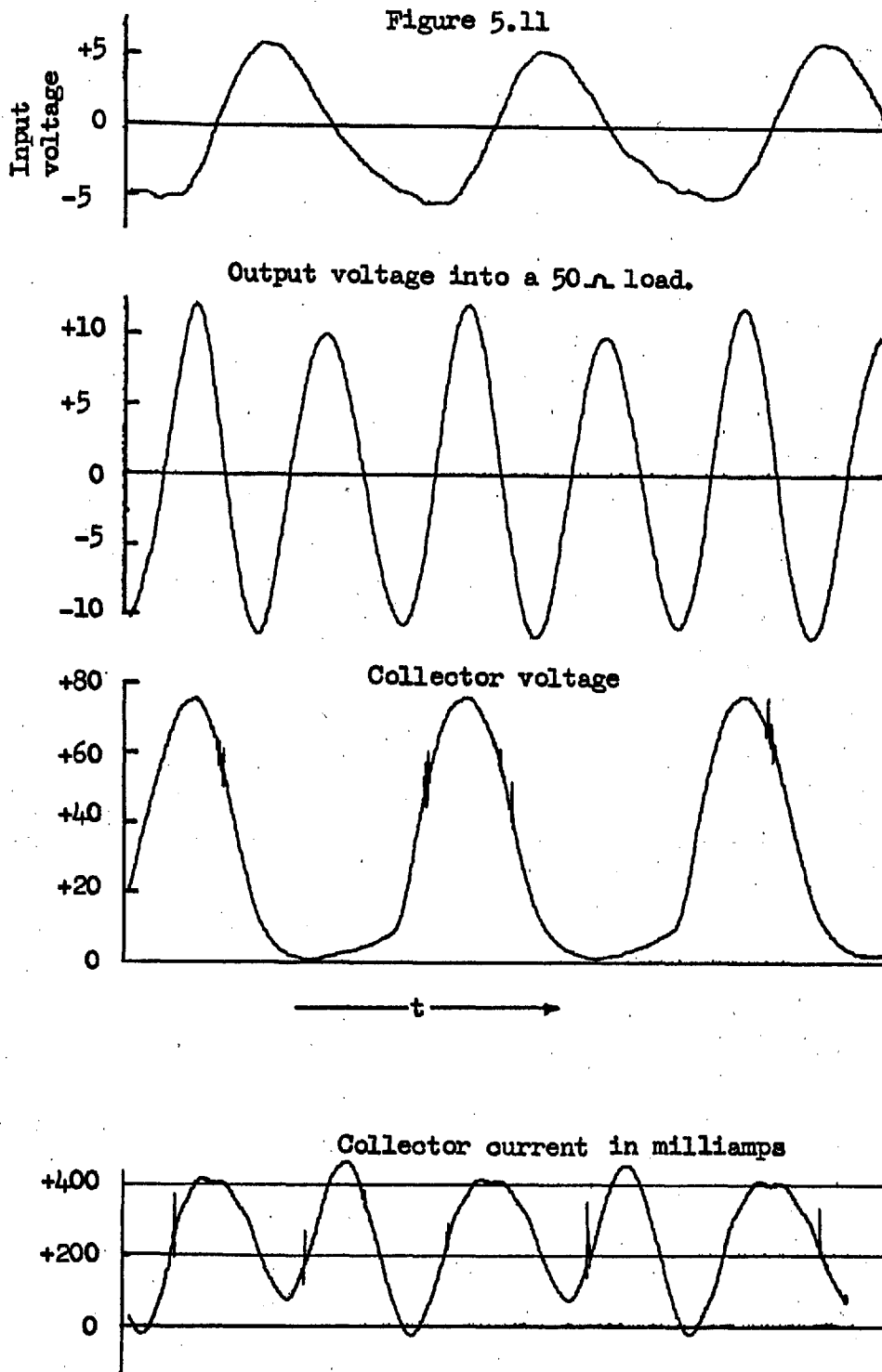
Typical voltage and current waveforms of a vhf transistor doubler
(output frequency is 100 MHz.). The doubler is operated, common
base, grounded collector.

5.2.3   Analysis of the vhf doubler performance

The operation of the doubler will be examined by investigating the power conversion efficiency, power handling capacity and waveforms of the multiplying element. The overall collector conversion efficiency of the doubler is significantly lower than the amplifier conversion efficiency (i.e. approximately 1/2). It is useful to evaluate the multiplication efficiency as outlined in Section 5.1.3. The collector multiplication efficiency is estimated by dividing the multiplier collector power conversion efficiency by the amplifier power conversion efficiency. The results of the division are shown in Fig. 5.12. The maximum power conversion efficiency of doubling, using the collector nonlinear capacitance, is 0.465.

It is now necessary to examine the collector-base capacitance in order to calculate its frequency multiplying performance. The measured capacitance versus reverse voltage is shown in Fig. 5.13. The resistance in series with the collector-base capacitance (r_s), for a range of voltages, was measured and found to be $3.0 \stackrel{+}{-} 0.5 \Omega$. With the above information, multiplication power conversion efficiency may be calculated for both the varactor model and the NLCSE model using Reference 35 and Chapter Four respectively.

For the varactor model $\omega_c = 19.6 \times 10^9$ rad/sec.

where $\omega_c = \dfrac{1}{r_s C_{min}}$ and $C_{min} = 17$ pfds from Fig. 5.13.

From Penfield and Rafuse[35] the maximum efficiency of a doubler with an input frequency of 50.0 MHz is

$\eta = .74.$

Figure 5.12
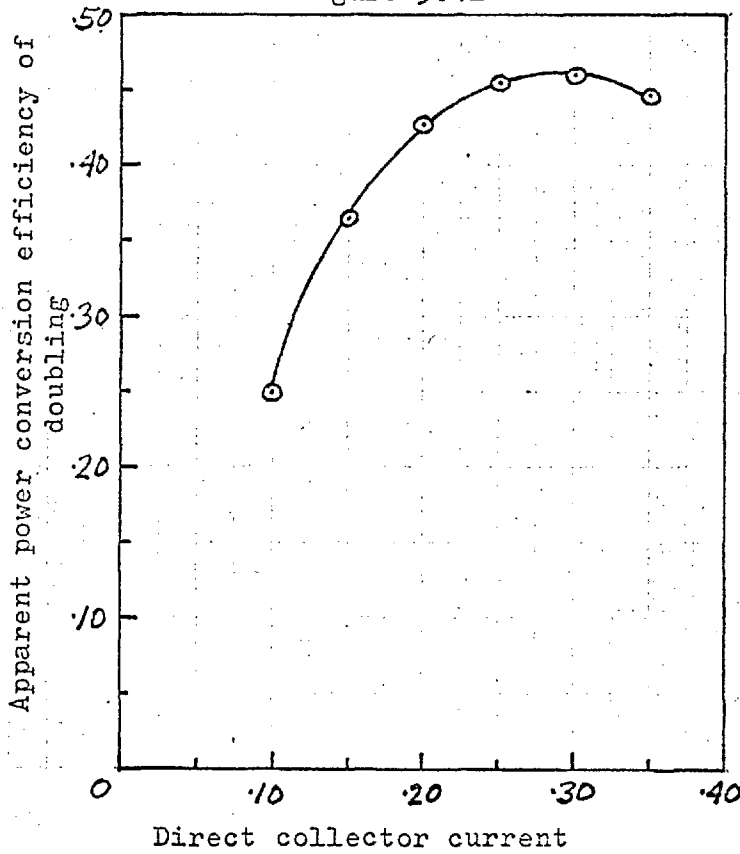
Apparent power conversion efficiency of frequency doubling at the transistor collector. The output frequency is 100 MHz.
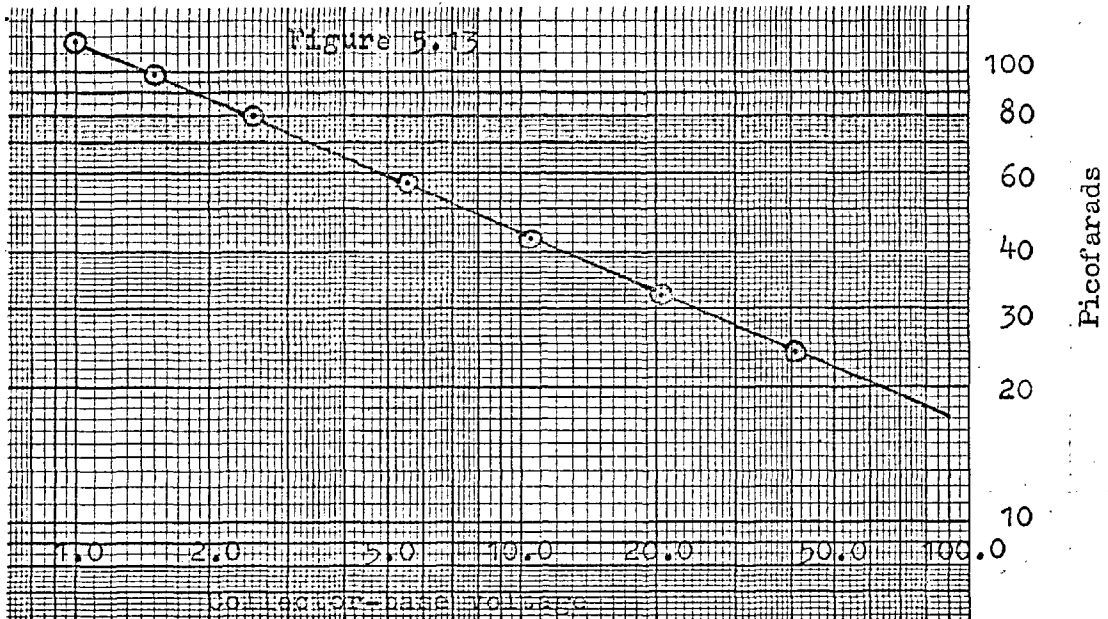
Measured collector-base depletion layer capacitance of the transistor (type PT530) used for doubling, as a function of voltage.

For the NLCSE model ω_c is calculated using an average value of capacitance (see Section 4.6; $C = 40$ pfd from Fig. 5.13)

$$\omega_c = 8.35 \times 10^9 \text{ rad/sec.}$$

and for a doubler with an input frequency of 50 MHz

$$\omega/\omega_{Cn} = 0.177$$

From Fig. 4.7

$$\eta = .70$$

Thus both models (varactor and NLCSE) predict a greater efficiency than is actually obtained. The varactor model is 60% high and the NLCSE model is 51% high. The reduced efficiency in the practical circuit can be attributed to circuit losses.

The maximum output power of the collector-base nonlinear capacitance will be calculated for both the varactor and the NLCSE multiplier. To calculate the maximum output power of the varactor, the cutoff frequency ω_c must be evaluated using r_s and the minimum capacitance, the minimum capacitance being dependent upon maximum reverse voltage as shown in Fig. 5.13. The ratio of the input frequency and the cutoff frequency may be found. The maximum reverse voltage V_{Cmax} is used in the evaluation of the "normalised power" (P_{norm}) of the varactor, giving

$$P_{norm} = \frac{V_{Cmax}^2}{r_s}$$

The maximum output power of the varactor may be calculated using graphs by Penfield and Rafuse[35]. The calculated maximum output power

is shown in Fig. 5.14 as a function of voltage (V_{Cmax}) for comparison with the measured output power. It should be noted that the maximum output power calculated is likely to be too high, as it is assumed that $\gamma = 0.5$ (where $C_{CB} = C_{CBmin} \left(\dfrac{BV_{CB} + \psi}{V_C + \psi}\right)^{\gamma}$).

Examination of Fig. 5.13 shows that γ is approximately equal to 0.42. According to Leonard[45] the maximum power handling of such a varactor is likely to be 30% less than a similar abrupt junction varactor $(\gamma = 0.5)$. The maximum output power according to Leonard is also shown in Fig. 5.14.

The maximum power handling capacity of the output nonlinear charge storage element employed as a frequency doubler is also shown in Fig. 5.14. The maximum power output is calculated from the theory developed in Chapter Four. The theory assumes, incorrectly for this example, that the diode conducts for 50% of the fundamental cycle period. Shorter conduction periods result in less power being converted than that predicted by the theory. From Fig. 4.10

$$P_{omax} = \frac{BV_D^2}{r_s} \cdot K_G^2 \cdot K_{PO}$$

Where K_{PO} may be determined from Fig. 4.10, and in this particular case is equal to 0.042. Thus here

$$P_{omax} = \frac{BV_D^2}{3.0} \times 0.2122^2 \times 0.042$$

In Fig. 5.14 the measured power output is compared with the maximum output power calculations just made. It is concluded that for small harmonic output powers (less than 0.4 watts), of the transistor NOM, frequency multiplication is by the varactor mechanism,

Figure 5.14

Maximum reverse collector voltage
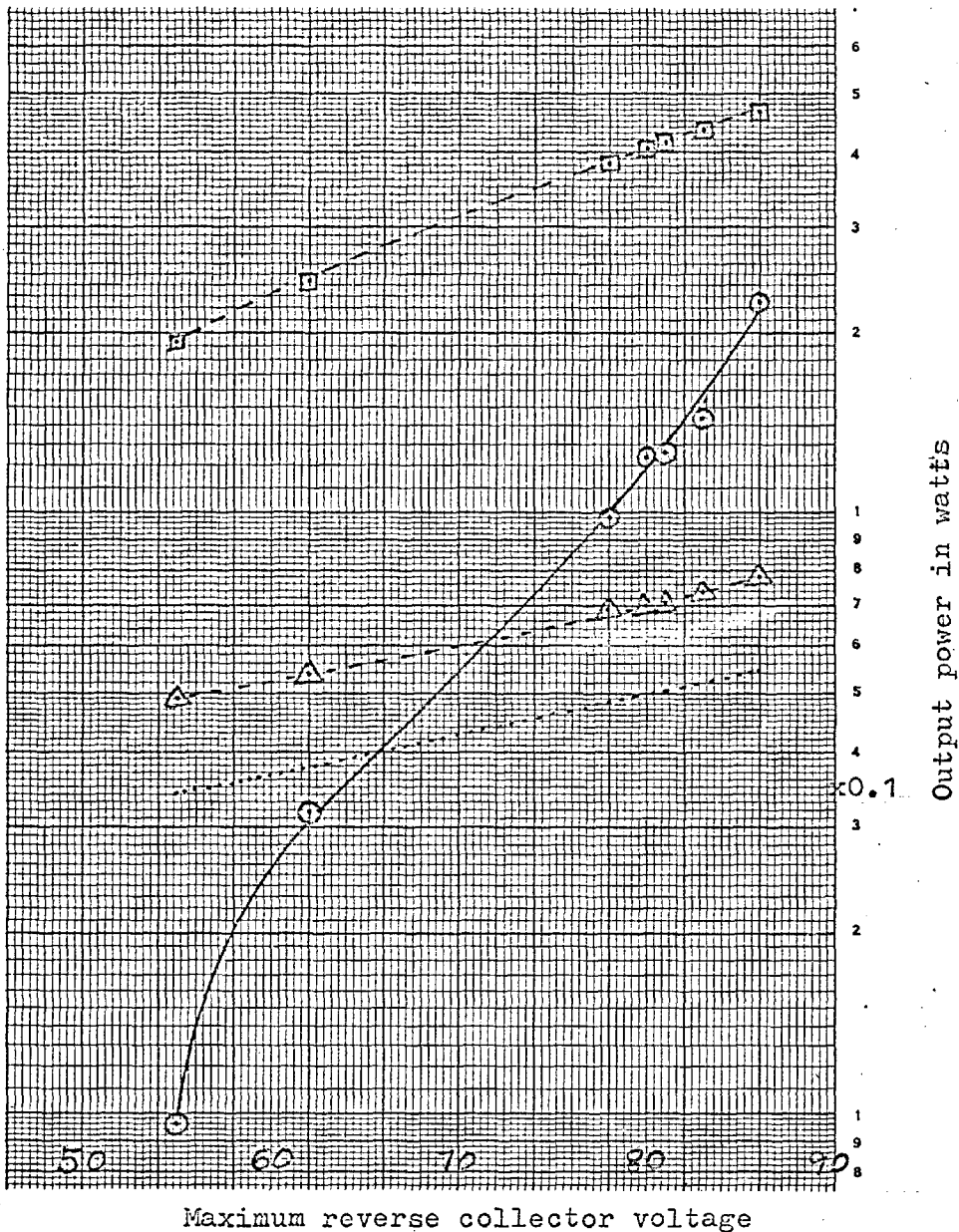
Measured output power of a doubler (output at 100 MHz) as a
function of peak reverse collector voltage indicated by
circles.   Theoretical maximum output power of a NLCSE multiplier
model (Chapter Four) indicated by squares and varactor multi-
plier model (Penfield and Rafuse[35]) indicated by triangles.
Maximum output power predicted from Leonard's analysis [45] shown
by dotted line.

while for powers larger than 0.4 watts the frequency conversion
process is largely due to minority carrier charge storage (NLCSE)
action. The reason for these conclusions is that the maximum power
converted is a factor of three larger than that predicted by the
varactor assumption and is about one half that predicted by the NLCSE
assumption. The only way to account for the varactor model discrepancy
is to assume "over-driving" - i.e. predominance of minority carrier
charge storage effects. The discrepancy, in the measurements as
compared with the performance predicted on the basis of the NLCSE
assumption, may be accounted for by losses in the output circuit
(a hypothesis supported by the discrepancy in the measured and
calculated efficiencies) and also by the fact that the conduction
period of the NLCSE (bottoming of the collector voltage) is shorter
than that assumed by the NLCSE multiplier theory. This last conclusion
is supported by the behaviour of v_C in Fig. 5.11, which is bottomed
for 30% of the fundamental cycle.

5.3   Transistor UHF Amplifier and Multipliers

A uhf transistor of proven amplifier and multiplier performance
became available for experimentation. The transistor - of a silicon
planar, double diffused, epitaxial, multi-emitter structure - is a
type 2N3375. This transistor is very frequently used as a uhf
transistor NOM and is representative of uhf power transistors. The
basic operating frequency adopted, 400 MHz, is near the maximum
frequency of usefulness (f_{max}) of the transistor as an amplifier.

5.3.1   Circuit techniques

Circuits, to date, have been largely composed of lumped elements, with some use of distributed circuit techniques[13,14,15,39,43]. The frequencies of operation are near the upper frequency limit for circuits of lumped components. It was decided that distributed circuit techniques would be used as much as possible because they are more easily used, particularly as operating frequencies increase, filtering using them is usually better, losses can be evaluated more easily.

Distributed circuit techniques are used here for filtering the various harmonics and for matching power into and out of the transistor. Other authors have used distributed circuit techniques but only to the extent of double and triple stub matching systems.

A transistorised doubler was constructed using a "helical line resonator"[43], designed to pass power at the frequency of 800.0 GHz only. The "helical line resonator" consists of a resonant quarter wavelength stub coiled into a cylindrical cavity for small physical dimensions. The resonator worked well and the construction of a more elaborate filter, using four helical line resonator elements, was undertaken. The filter took the form of a multiplexer with the input and the four outputs feeding into 50Ω coax transmission lines. The output ports were tuned to 0.400, 0.800, 1.200 and 1.600 GHz. Thus the fundamental through to the fourth harmonic are each separated into a port. Matching was done by using a line stretcher and a single, paralleled, variable length, shorting stub. Details of the multiplexer are given in Appendix 3.

The helical line resonator multiplexer was used on the output
of the transistor, the common port of the multiplexer being
connected to the collector. The transistor operated as an amplifier
or a multiplier depending on which output port the matching circuit
and load were connected to. The shorting stubs and line stretcher
were General Radio components.

Input filtering to the transistor was not necessary. An efficient
matching system is needed at the input of the transistor, but it was
found that the GR 50Ω coax transmission line components were not
suitable for this purpose. Efficient matching was achieved by adding
a small variable capacitance in parallel with the transistor input.
The low input impedance (too low for efficient matching by GR coax
components) of the transistor was increased by the effect of additional
series inductance (a variable capacitance stray) and the variable
capacitance (the equivalent circuit of the input circuit and
transistor base lead inductance being equivalent to a series m-derived
low-pass filter[50], this filter being capable of matching a low
impedance - here the transistor r_{bb} - to a higher impedance - here
a 50Ω coax transmission line). The added variable capacitance is
necessary[42] for all of the overlay transistors made to date[42].
Alternatively, the low input impedance might be matched efficiently
by the use of a transmission line transformer. In addition to the
capacitance, a line stretcher and a short circuit stub was provided
for purposes of input matching. The multiplexer constructed here
was quite efficient but it is felt that with further work it would

be superior to the best lumped element circuits and filters in
the uhf range.

The overall measurement set-up is shown in Fig. 5.15, and the
connection of the transistor is shown in Fig. 5.16. The exact way
in which the helical line resonator multiplexer was used is shown
in Appendix 3. Initially the transistor was employed in the common
emitter configuration, for all functions, this being the most stable
for the particular transistor used[42]. For other transistors the
common base configuration may be the most stable. It is sometimes
recommended that the emitter lead inductance of the 2N3375 be tuned
out (common emitter configuration) for operation as an amplifier;
however, emitter tuning was not used here, as it complicates ampli-
fier adjustment and would make multiplier adjustment very complicated.
The 2N3375 was used in the common emitter configuration as an
amplifier through to a quadrupler with good stability (but with
decreasing stability as the multiplying factor increases). Perform-
ance data was collected for the four different multiplying factors.

The transistor was then used in the common base configuration
to permit more accurate measurements on the collector voltage swing
even though stable operation was difficult to obtain in the ampli-
fier and the doubler. The collector voltage swing was measured so
that the maximum output power of the collector-base depletion layer
capacitance could be evaluated accurately.

5.3.2   The common emitter amplifier

The amplifying circuit was obtained by connecting the output

Figure 5.15

(a)

Block diagram of essential equipment for measurements on uhf
amplifier and HOM multipliers. All connections are 50Ω coaxial
transmission lines except to oscilloscope and power supply.
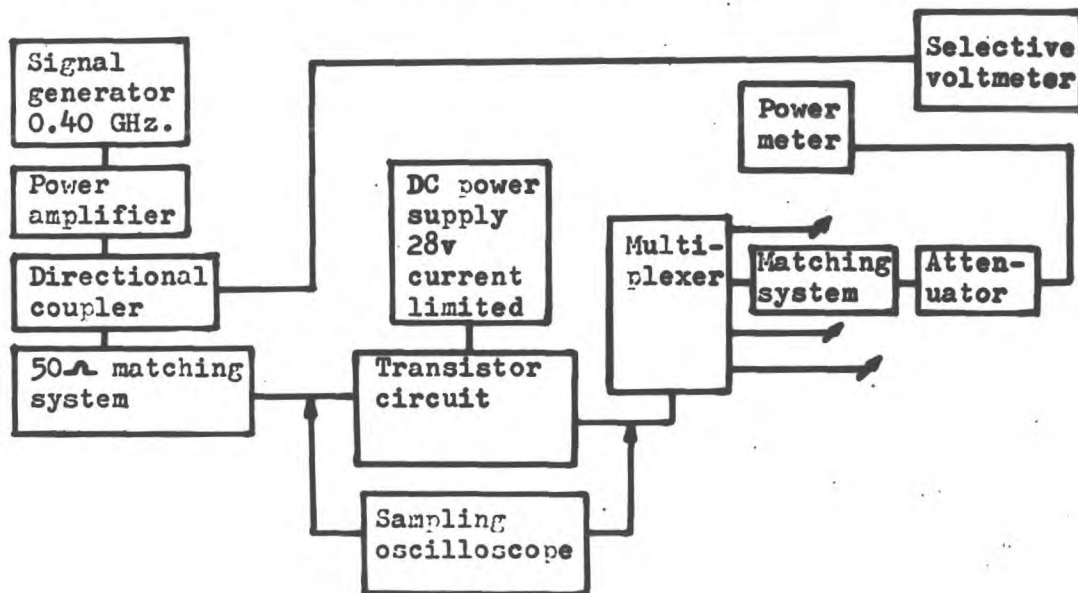
(b)

Photograph of measurement setup with sampling oscilloscope removed.

Figure 5.16

(a)

The circuit of the transistor uhf amplifier/multiplier module.
The two input capacitances are tuned for maximum collector
current. The biasing chokes, on the input and output, are made
small to prevent low frequency oscillations.
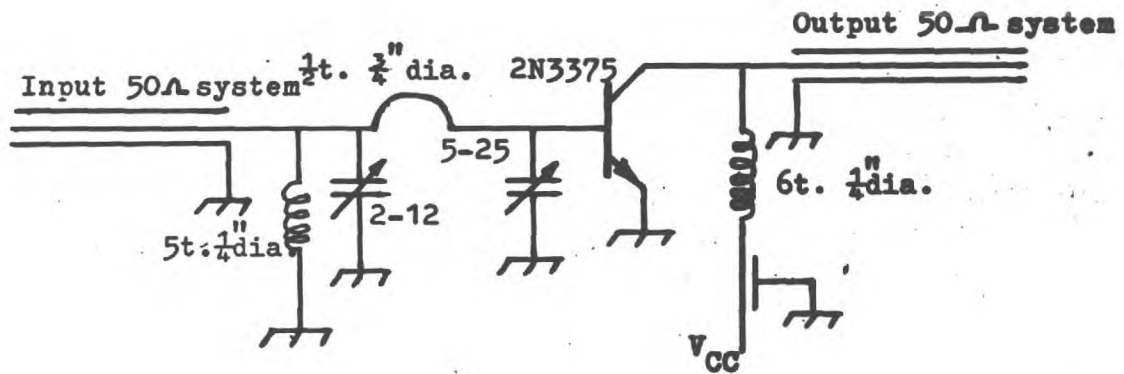
(b)

Photograph of the transistor uhf amplifier/multiplier module.

matching circuit and the load to the fundamental port (0.400 GHz)
of the multiplexer. The measurement set-up and the circuit are shown
in Figs. 5.15 and 5.16. Measured input and output powers and
collector power conversion efficiency are shown as a function of
direct collector current in Fig. 5.17.

Figure 5.17
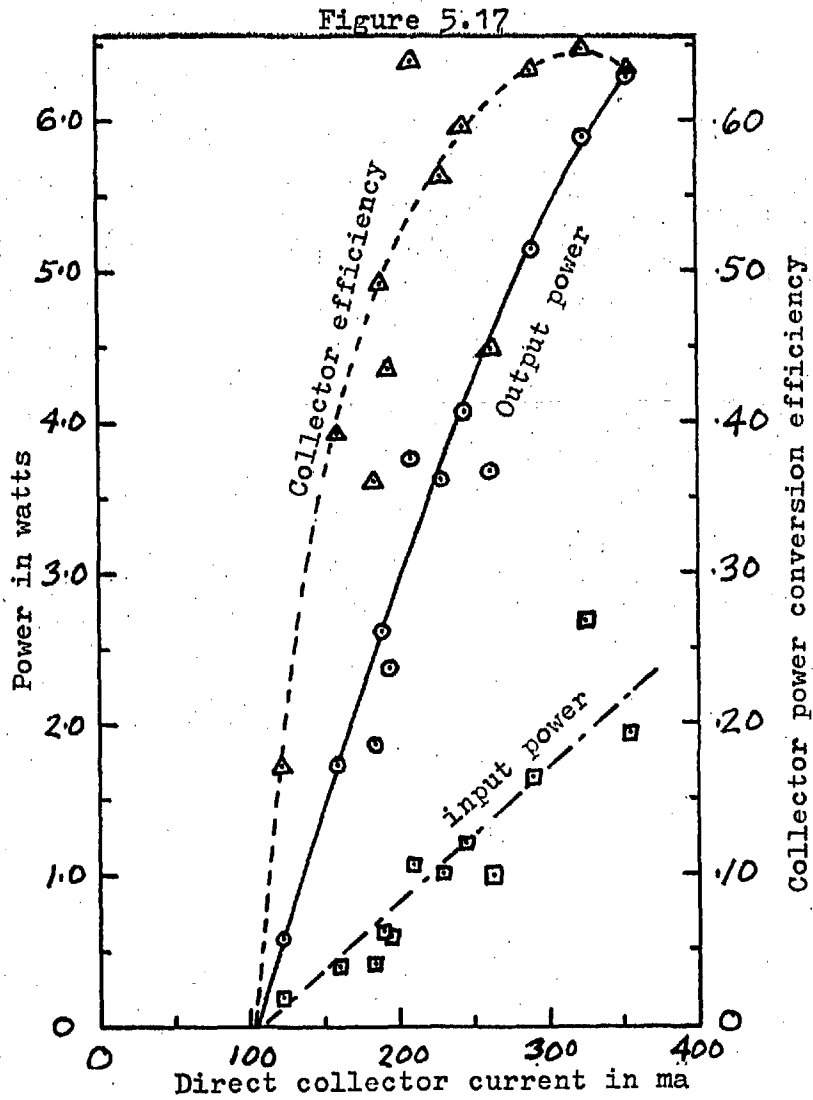
Performance of a 2N3375 amplifying at 400 MHz.

The different operating conditions were obtained by using different input power levels and tuning for maximum output power for each situation. One of the unexpected results was that the tuning of the second harmonic shorting stub (0.800 GHz) was very important. Incorrect tuning of the stub could reduce the power output of the amplifier by as much as 40%. Tuning of the third and fourth harmonic stubs had a slight but not significant effect on the output power.

Typical amplifier voltage waveforms are shown in Fig. 5.18. The high purity of the output power was due to the filtering effect of the multiplexer. Examination of the base voltage v_B indicates that the base was forward biased for about $278°$, corresponding to a collector current efficiency (η_{CI}) of about 0.67. The collector voltage efficiency (η_{Cv}) was about unity. Thus the theoretical collector power conversion efficiency is about 0.67. The measured conversion efficiency of the transistor was 0.646, which is in good agreement with the theoretical value. Examination of the collector voltage v_C of Fig. 5.18 shows why the second harmonic tuning was important. The collector voltage tended to bottom, or swing into forward conduction, but correct tuning of the second harmonic limited the extent of the bottoming. It is even possible that some second harmonic power was being converted into fundamental power through the beneficial usage of the collector-base charge storage diode.

5.3.3   The common emitter doubler

The transistor circuit for doubling is obtained by connecting

Figure 5.18   179

voltage on
input system

←10v/cm→

0

Base voltage

←5v/cm→

0

Collector voltage

←20v/cm→

0

⟶ t ⟶

Output voltage into a 50 Ω system

←10v/cm→

0
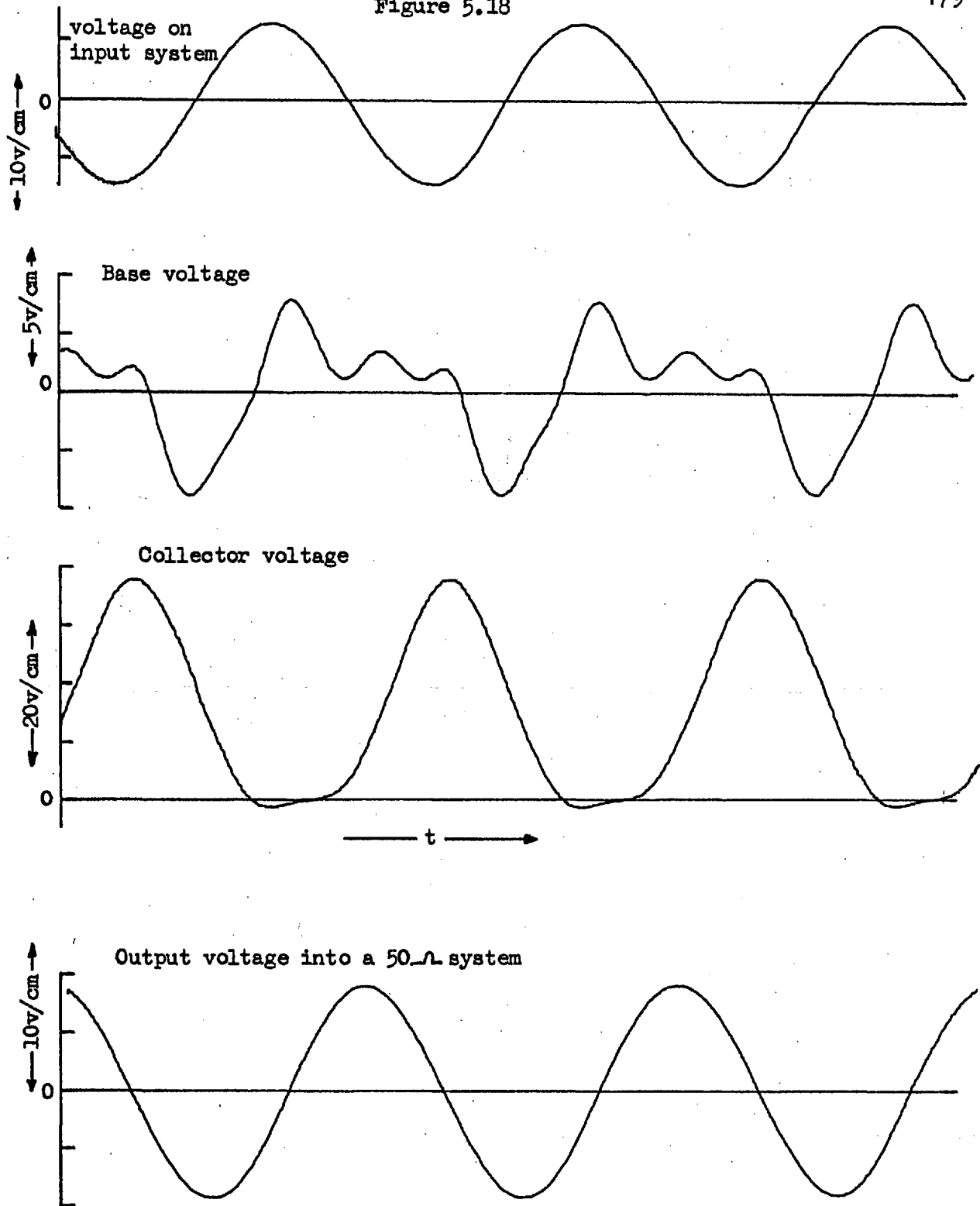
Voltage waveforms of a uhf amplifier. A 2N3375 is used in the common
emitter configuration with an operating frequency of 400 MHz.

a variable length shorting stub to the fundamental port and a
matching circuit and load resistance to the second harmonic port.
The variable length shorting stubs remain at the third and fourth
harmonic ports. The shorting stubs and matching system on the output
were adjusted for maximum output at 0.800 GHz. The input tuning
was essentially the same as for the amplifier. The adjustment of
the fundamental shorting stub was very critical for best output power
and improper adjustment of the third harmonic stub reduced the power
output by as much as 50%. The input and output power and overall
collector efficiency are shown in Fig. 5.19 as a function of
collector current.

Figure 5.19
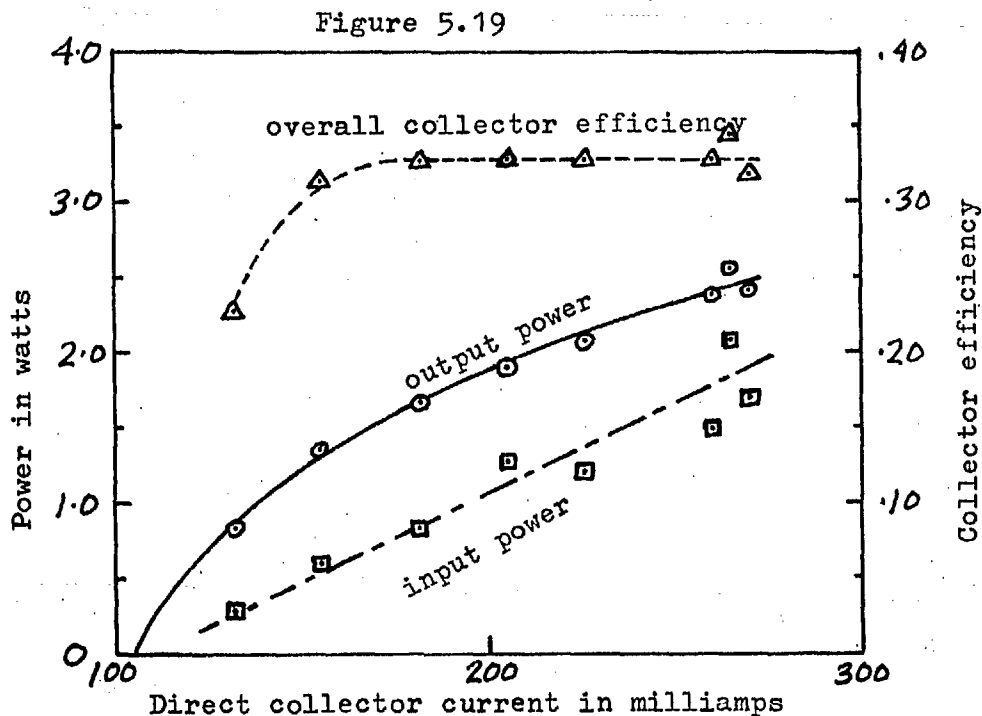
Performance of a transistor NOM doubler with an output frequency of
800 MHz. The transistor is a type 2N3375 used in the common emitter
configuration.

The input, base, collector and output voltage waveforms of
the doubler circuit are shown in Fig. 5.20. The output power at
0.800 GHz is free (to a high degree) of other harmonic power.
The large voltage swing at the collector should be noted. The
maximum reverse swing of v_C was +96 volts, and the maximum forward
swing was -22 volts. Normally a large voltage forward bias swing
would correspond to a very large injection of carriers across the
collector-base junction, except that the base voltage seems to
swing to -20 volts at the same time. The exact voltage across the
collector-base junction is difficult to evaluate from Fig. 5.20,
as the phase relationships have not been maintained between the
voltages. The collector voltage of the common base configuration is
examined later to determine the power handling capacity of the
collector-base varactor: the varactor is likely to have the same
power handling capability whether used in the common base or emitter
configuration.

The collector power conversion efficiency of the doubler is
divided by the amplifier collector power conversion efficiency
(from Section 5.3.2) so that an estimate may be made of the multi-
plication efficiency. It is assumed that the transistor amplifies
with the same collector efficiency in the NOM mode as in the ampli-
fying mode (outlined in Section 5.1.3). The apparent power conversion
efficiency of the doubling action is shown in Fig. 5.21 for various
collector currents. The maximum doubling efficiency is 0.90 and the
average doubling efficiency is about 0.67. The high values of

Figure 5.20
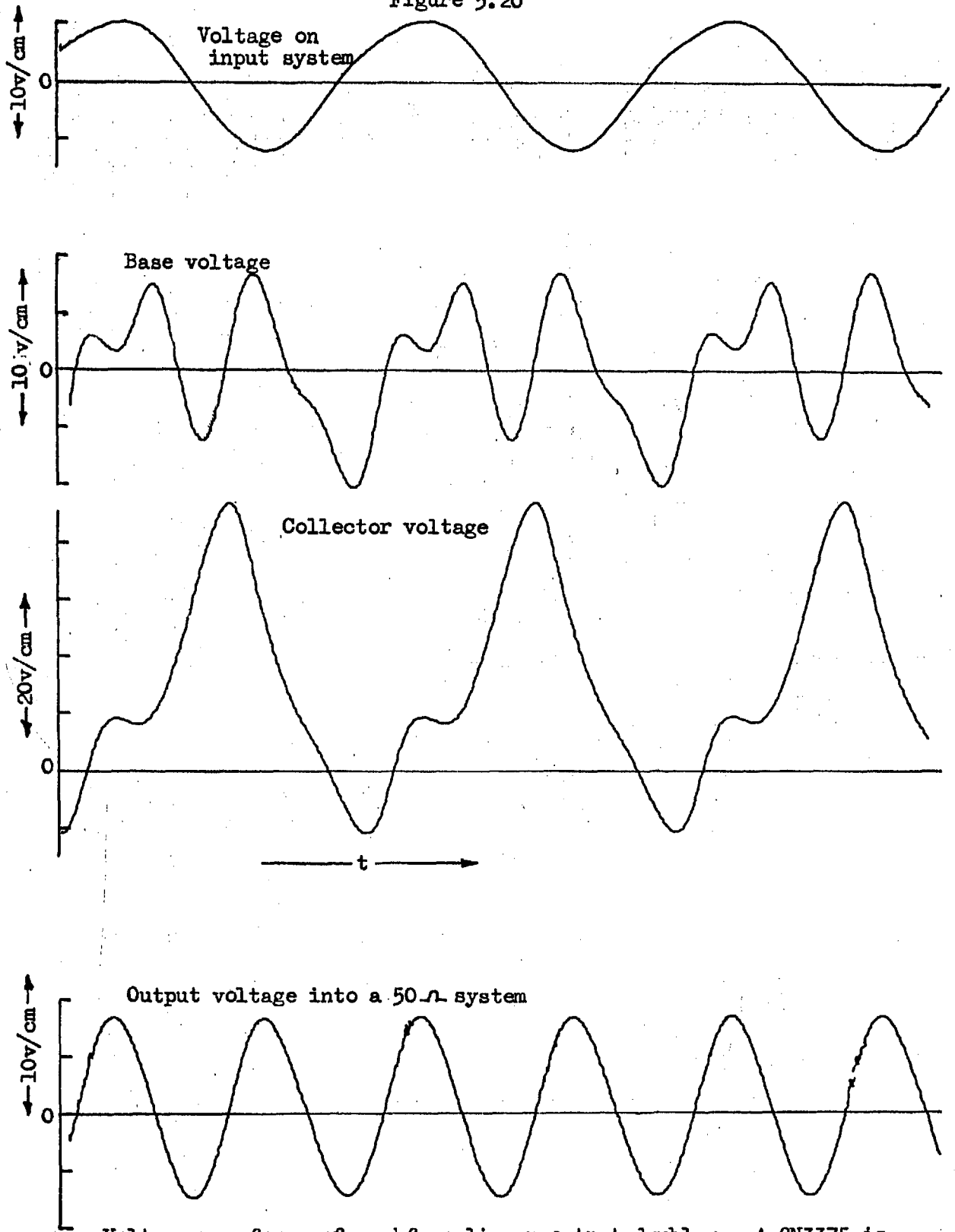
Voltage waveforms of a uhf nonlinear output doubler. A 2N3375 is used in the common emitter configuration with an input frequency of 400 MHz.

Figure 5.21
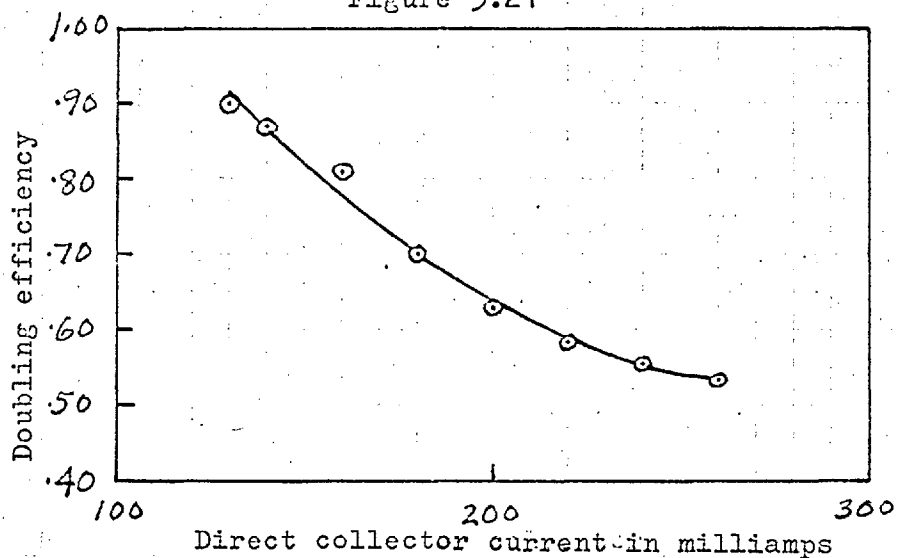
Apparent doubling efficiency of the transistor output, obtained
by dividing the doubler power output by the amplifier power
output.

Figure 5.22

Collector-base voltage of the transistor
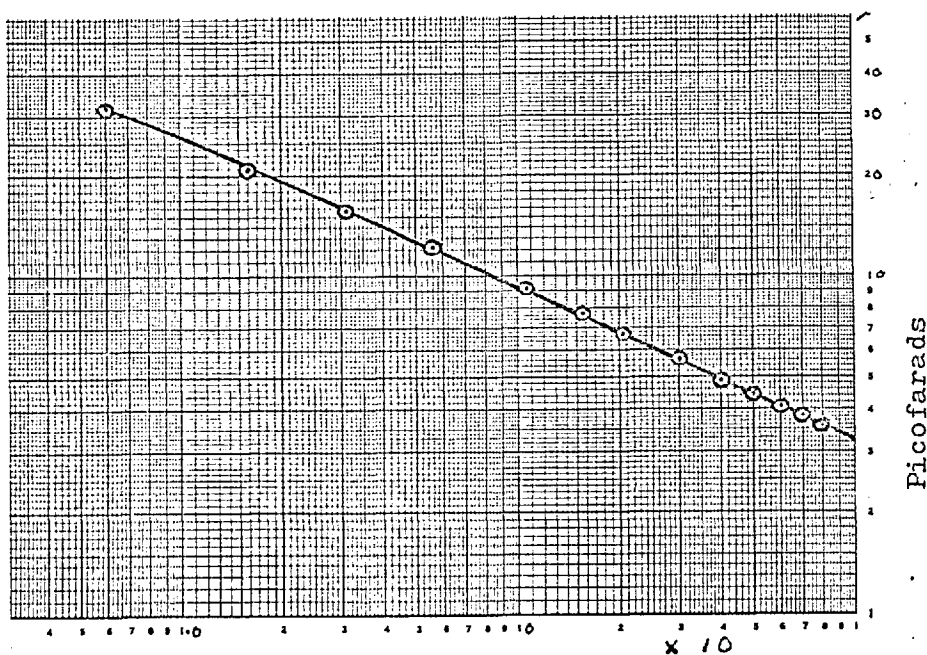
Measured collector-base capacitance of the transistor (type
2N3375) used for doubling 400 MHz.

multiplication efficiency at low collector currents are suspect, however, and it seems likely that the amplifying section of the doubler has a higher efficiency than the amplifier circuit because the collector voltage efficiency (η_{Cv}) is consistently high (the amplifier with low power outputs has a low efficiency because the collector voltage efficiency η_{Cv} is low, the collector current efficiency being approximately constant). The doubler requires large collector voltage swings in order to multiply power using the nonlinear capacitance, and hence a high collector voltage efficiency is attained.

The series resistance of the collector-base depletion layer capacitance was measured and found to be $2.0 \overset{+}{-} 0.3\Omega$. The measured depletion layer capacitance C_{CB} is plotted as a function of collector-base voltage in Fig. 5.22. The minimum capacitance of the junction is about 3.4 pfds. The angular cutoff frequency of the collector-base varactor is 147×10^9 rad/sec. The doubling efficiency of the varactor with an input of 0.400 GHz ($\frac{\omega_{in}}{\omega_c} = 0.0171$) should be 0.73, according to Penfield and Rafuse[35], which is in good agreement with the average measured efficiency.

The prediction of efficiency using the NLCSE multiplication assumption is initiated by finding the average capacitance value. The value is about 9.0 pfds. The angular cutoff frequency of the model, using this capacitance, is 88.3×10^9 rad/sec. , so that,

$$\frac{\omega_{in}}{\omega_c \times .2122} = 0.134.$$

Using Fig. 4.7 the calculated doubling efficiency is found to be
0.66, which is also in good agreement with average measured efficiency.

A number of different transistors (type 2N3375, manufactured
by Motorola, Ferranti and R.C.A.) were tried out in the doubling
circuit. The output power of each transistor is plotted Fig. 5.23
as a function of the direct collector current.

Figure 5.23
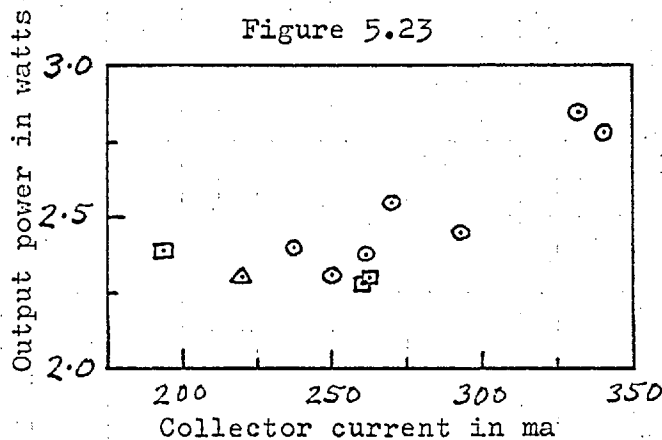
Output power at 800 MHz of different transistors (type 2N3375) used as NOM doublers, manufactured by Ferranti (circles), Motorola (squares) and RCA (triangle).

The input power in all cases is 1.0 watts. The performance of the
different transistors is quite uniform and in many cases the tuning
conditions were almost identical.

5.3.4   The common emitter tripler

The transistor tripling circuit was obtained by connecting
the matching circuit and load to the third harmonic port. Variable
length shorting stubs were connected to the other three output ports.
For maximum output at 1.200 GHz the tuning of the fundamental and
second harmonic shorting stubs was very critical. Incorrect tuning
of the fourth harmonic stub reduced the power output by as much as 50%.

Input and output powers and the collector power conversion

efficiency are plotted as a function of collector current in Fig. 5.24.

Table 5.24
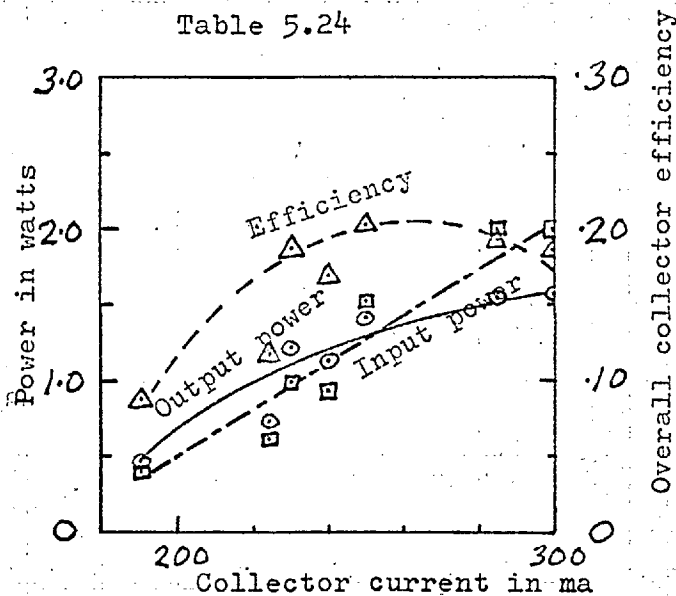
Performance of a transistor tripler (type 2N3375) operated common emitter with an output frequency of 1.2 GHz.

The output power has been corrected to account for losses in the

multiplexer. Thus only the transistor losses should be evident in

the power conversion efficiency evaluations.

The voltage waveforms of the tripler are shown in Fig. 5.25.

The large voltage swing on the collector will be noted (viz. +95 to

-28 volts). It should be explained, however, that the sampling

oscilloscope (a Hewlett Packard 185B with a 187B plug-in, dual

channel vertical amplifier) used to obtain the voltage waveforms

had an estimated bandwidth of 1.2 GHz, so that the waveforms shown

are approximate. The base-emitter voltage deviates a great deal

from the 0.400 GHz sine wave assumed in the case of the amplifier.

Figure 5.25
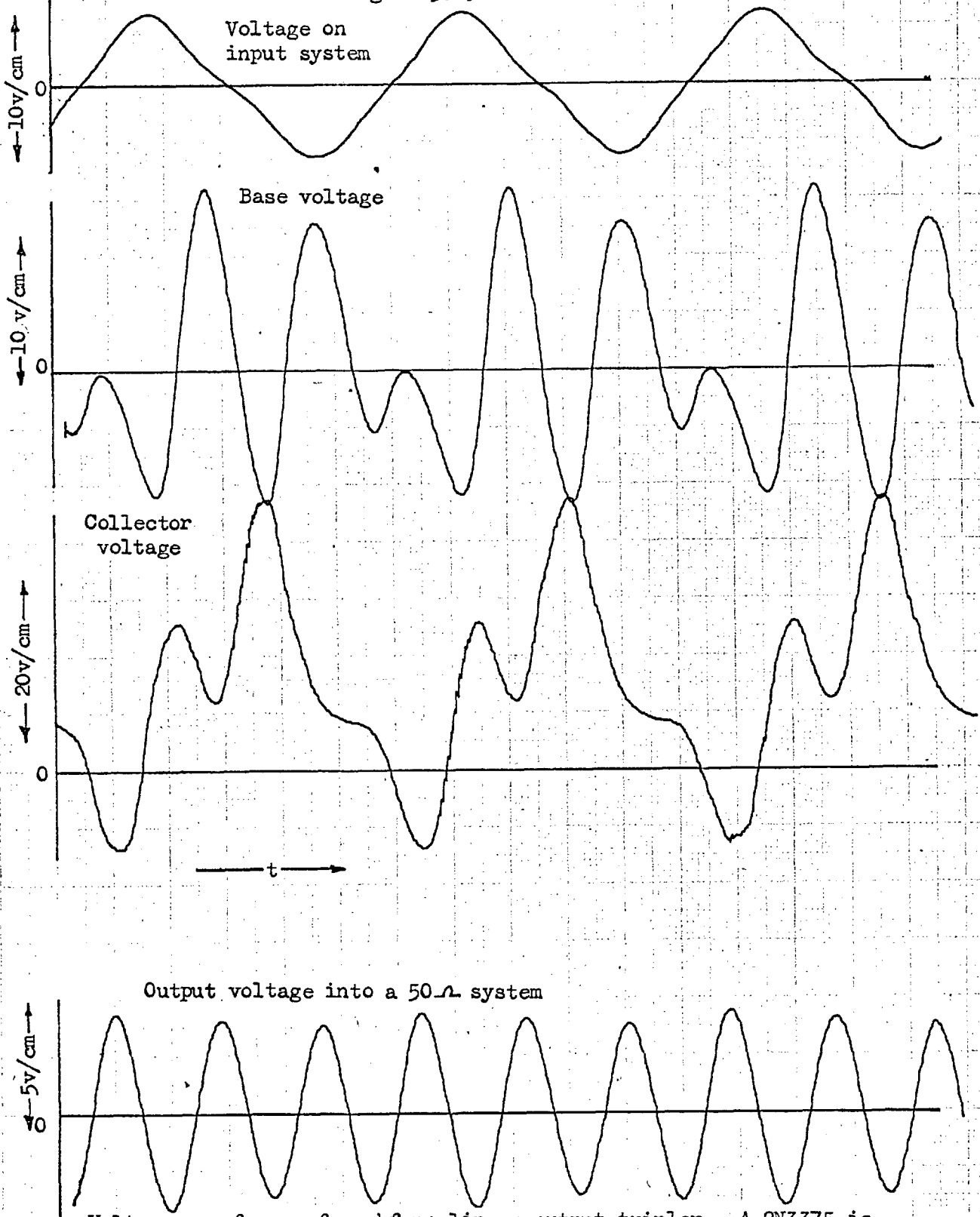
Voltage waveforms of a uhf nonlinear output tripler. A 2N3375 is used in the common emitter configuration with an input frequency of 400 MHz.

The theoretical maximum output power of the collector-base varactor is not calculated because of the uncertainty of the voltage swing across the varactor terminals. The apparent measured efficiency of the varactor is plotted in Fig. 5.26.

Figure 5.26
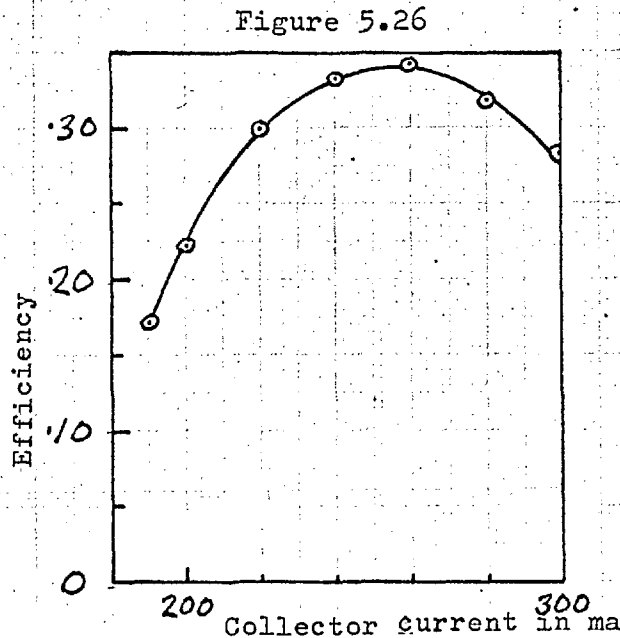
Apparent tripling efficiency of a transistor NOM tripler

The highest multiplication efficiency is 0.34 and the average efficiency is about 0.30. The theoretical power conversion efficiency of the collector conversion efficiency of the collector-base varactor is 0.58, from Penfield and Rafuse[35] (ω_{in}/ω_c = 0.0171 from Section 5.4.3).

The theoretical power conversion efficiency, assuming NLCSE multiplication, is 0.43 from Fig. 4.7 (ω_{in}/ω_c = 0.0285 and ω_{in}/ω_{cN} = 0.413). The derivation of Fig. 4.7 is based on the assumption that no discrete frequency idlers exist, but idlers do actually exist

in the circuit. Steinbrecher[18] treats such a situation and using

his analysis the theoretical efficiency is found to be 0.592. The

calculation carried out on the basis of an idlerless charge storage

multiplier is the closest to the measured value. Steinbrecher's

calculation assumes that the NLCSE is operated with the conduction

angle chosen so as to maximise multiplier efficiency whereas in

the present case the transistor collector voltage is, in fact,

bottomed for a much shorter period. Thus it may well be expected

that both NLCSE multiplier calculations will be optimistic for the

present application.

5.3.5   The common emitter quadrupler

Quadrupler operation of the common emitter circuit was

effected by connecting the matching system and load to the fourth

harmonic port of the multiplexer. Again the 2N3375 was used.

Measurements were made at only one setting as the quadrupler tended

to be unstable. The output power, at 1.600 GHz, was 0.40 watts

with an overall collector conversion efficiency of 0.08. The

separate varactor efficiency was about 0.15.

The input, base collector and output voltage waveforms are

shown in Fig. 5.27. The waveforms are again approximate owing to

the limited bandwidth (1.2 GHz) of the sampling oscilloscope used.

The output power purity (at 1.6 GHz) was probably better than that

indicated by Fig. 5.27 as the oscilloscope was inadequate for this

frequency range, the limited bandwidth of the scope attenuated the

output frequency with respect to the lower frequencies and the

Figure 5.27

Voltage on input
system

0

10v/cm

Base voltage

20 v/cm

0

Collector
voltage

20 v/cm

0

t

Output voltage into a 50 Ω system

5v/cm
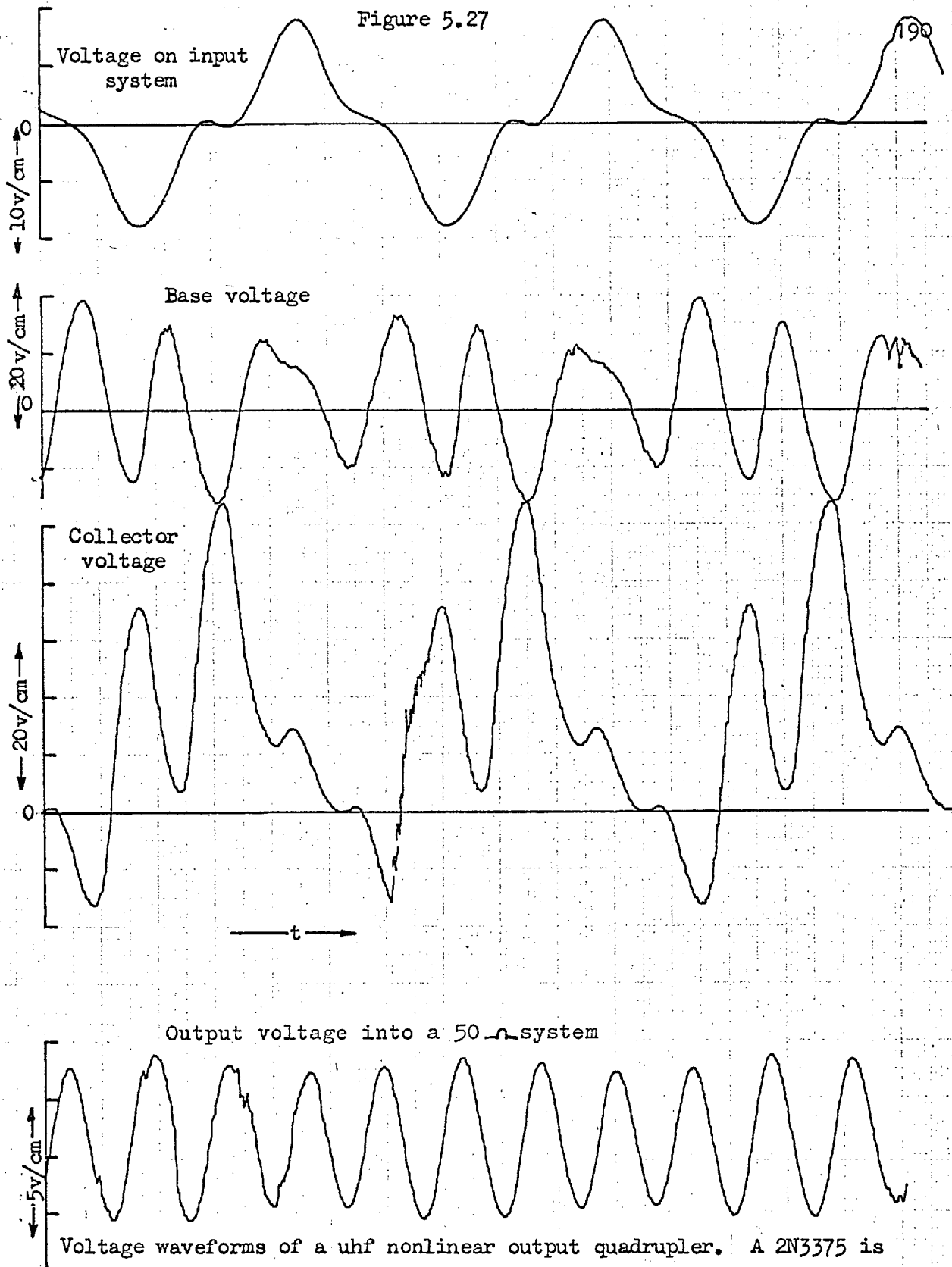
Voltage waveforms of a uhf nonlinear output quadrupler. A 2N3375 is
used in the common emitter configuration with an input frequency of
400 MHz.

scope had appreciable stray pickup - chiefly at 0.4 and 0.8 GHz.

The voltage waveforms are not completley repetitive in Fig. 5.27, as they should be, owing to the failure of the oscilloscope synchronisation to the incoming voltage.

The calculated varactor efficiency is 0.36 according to Penfield and Rafuse[35]. The calculated efficiency using the theory derived in Chapter Four is 0.28 or 0.18 depending on whether the NLCSE conduction angle is assumed to be 50% or 25% respectively. From the NLCSE multiplier theory developed by Steinbrecher[18] the separate multiplier efficiency should be 0.495. Thus the collector multiplying efficiency is appreciably less than all theoretical calculations except that derived on the basis of an idlerless NLCSE multiplier assumption - an inaccurate description of the circuit used which, in fact, contained idlers.

5.3.6   The common base doubler

The common base circuit is examined so that more information may be obtained about the mechanism of multiplication. The common base configuration, using the 2N3375, was generally less stable than the common emitter configuration[42]. The doubler tends to maintain a constant output power irrespective of the input power level. The common base configuration does permit a more exact examination of the collector-base voltage swing (than the common emitter configuration). The exact collector voltage waveform is very difficult to measure at high frequencies. The sampling oscilloscope used had a bandwidth of about 1.2 GHz, whereas exact measurements would require an oscillo-

scope with a bandwidth of about 2.0 GHz. In addition, measurements at the transistor chip were impossible to obtain and the voltage drop across both the collector and base lead inductances was considerable. The effect of lead inductances could be observed, by moving the oscilloscope probe along the collector lead towards the outlet and the voltage was found to vary considerably. Thus observations of collector voltage waveforms are approximate. The common base NOM doubler circuit was identical to the common emitter configuration except that the base terminal was earthed instead of the emitter. The earthing was effected by soldering the base terminal directly to the metal encapsulating can. The can was bolted to the common earthing plate of the circuit. Some perform-ance figures for the common base doubler are shown in Table 5.1.

Table 5.1

Performances of a common base   NOM doubler using a 2N3375

Input Power 0.400 GHz	Output Power 0.800 GHz	Direct Collector Current V_{CC} = 28.0 volts	Peak Collector Voltage
2.06 watts	3.11 watts	298 milliamps	96 volts
0.99	3.02	282	96.
0.90	2.82	272	98
0.855	2.85	282	95
0.594	2.67	255	94
0.165	2.44	295	94

The maximum output power of the collector-base varactor doubler is calculated according to Penfield and Rafuse[35]. The calculation is similar to that for the varactor model in Section 5.2.3, viz.

$$P_{omax} = \frac{BV_D{}^2}{r_s} \times F(\omega_{in}/\omega_c)$$

where the function $F(\omega_{in}/\omega_c)$ is determined from a graph given in Reference 35. From Section 5.3.3 we have $\frac{\omega_{in}}{\omega_c} = 0.0171$ and the value of $F(\omega_{in}/\omega_c)$ for the doubler is 4.5×10^{-4}. The above P_{omax} is derived for an abrupt junction varactor ($\gamma = 0.50$) but examination of the capacitance versus voltage curve (Fig. 5.22) shows that the negative slope is 0.450 (viz. $\gamma = 0.45$) and thus the power handling capability of this particular varactor (in a doubling circuit) is less than the abrupt junction varactor[45]. The ratio of output power (for low frequencies) of the above varactor to the abrupt junction varactor is $0.0220/0.0285 = 0.771$, as derived by Leonard[45]. The maximum power output that would be expected from the collector-base varactor is thus,

$$P_{omax} = \frac{V_{Cmax}{}^2}{2.0} \times 4.5 \times 10^{-4} \times \frac{.022}{.0285}$$

The calculated maximum output power so derived is shown in Table 5.2 and compared with the measured output powers.

Also shown in Table 5.2 are calculated maximum multiplied output powers for a NLCSE doubler. The maximum power is calculated from Fig. 4.10. The normalised input frequency for the charge storage multiplier model is $\omega/\omega_{cN} = 0.134$ (calculated in Section 5.3.3).

Table 5.2

Maximum calculated output powers of a transistor NOM (a 2N3375 doubling to 0.800 GHz.) compared with the measured output power.

V_{Cmax}	P_o measured	P_{omax} Varactor Model	P_{omax} NLCSE Model
96.0 volts	3.11 watts	1.60 watts	7.21 watts
96	3.02	1.60	7.21
98	2.82	1.67	7.41
95	2.85	1.57	6.96
94	2.67	1.54	6.82
94	2.44	1.54	6.82

It is found from Fig. 4.10 that

$$P_{omax} = \frac{V_{C\,max}^2}{2.0} \times .2122^2 \times .034$$

The appropriate values of P_{omax} calculated on this basis are also listed in Table 5.2.

It is evident from the Table that the collector-base varactor action is insufficient to account for the observed power conversion; on the other hand the NLCSE multiplier action is capable of a greater power conversion than observed in practice. In fact, it seems likely that of the useful multiplied output power, part is the result of conversion obtained by varactor multiplication action and part by a NLCSE

multiplication action: in the present case, roughly half the out-

put power is due to the action of each multiplication mechanism.

The power handling capability of the NLCSE doubler is a function of

the conduction angle. The conduction period is assumed to be 50% of

the fundamental period but observations indicate that the real

conduction period is appreciably less and hence the power handling

capability is less. The tripler and quadrupler are not examined in

the common base configuration, due to their inherent instability.

It has been demonstrated that the varactor doubler is not capable of

handling the transistor amplifier output power, and it is well known

that the tripler and quadrupler configurations of a varactor multi-

plier are incapable of handling as much power as a varactor doubler.

5.4   Output Power of the Transistor NOM

In the earlier sections of this chapter it has been shown that

the transistor NOM often uses the minority carrier charge storage

characteristics of the collector-base diode, for frequency multi-

plication. In order that the NOM action may be understood, it is

important to know whether a varactor or NLCSE mechanism predominates.

If the power input to the nonlinear element is small, a varactor

multiplication mechanism is most likely, while if the power is large

the multiplication is likely to occur through a NLCSE mechanism.

It is useful to find an expression describing the maximum power that

the varactor will convert into a harmonic, with the NLCSE mechanism

coming into play if more power is applied to the nonlinear output

element. The maximum power that a varactor will convert depends

chiefly upon the input frequency, the magnitude of the nonlinear capacitance, and the maximum reverse voltage. The maximum reverse voltage depends upon the biasing voltage V_{CC} applied to the transistor, and not directly on the transistor breakdown voltage. Normally a separate varactor multiplying circuit uses a self-biasing arrangement, since for efficient operation a varactor should almost bottom. In the transistor NOM the multiplication cannot be optimised in such a way.

An algebraic expression will be found to describe the maximum input power to the collector-base varactor. Low frequency conditions will be assumed in order to simplify the analysis. The analysis is based on the varactor doubler, as this is employed most frequently and is representative of higher order multipliers. For maximum output power from a doubling varactor the ratio of biasing voltage to peak reverse voltage $\left(\dfrac{V_{DO} + \psi}{BV_B + \psi}\right)$ should be 0.344 from Penfield and Rafuse[35].

Rewriting the equation to suit the transistor NOM,

$$(V_{CC} - V_{Csat}) = .344 \, (V_{Omax} - V_{Csat}) \qquad\qquad 5.1$$

At low frequencies the maximum output power of a varactor doubler as derived by Penfield and Rafuse is,

$$P_{in\ max} = .0285 \times \frac{BV_D^2}{r_s} \times \frac{\omega_{in}}{\omega_c}$$

or

$$P_{in\ max} = .0285 \times BV_D^2 \times C_{CBmin} \times \omega_{in} \qquad\qquad 5.2$$

The application of Eqn. 5.2 to the transistor must be carried out with some caution. The breakdown voltage of the transistor is very difficult to specify at high frequencies. The peak reverse collector

voltage depends chiefly upon the biasing voltage as described
in Eqn. 5.1. The value of C_{CBmin} depends upon the peak reverse
voltage of the varactor or transistor collector. In addition, it is
assumed that the base-collector junction is abrupt rather than graded
(with respect to impurity doping). A graded junction would have,
for example, a power handling capability of less than half that indi-
cated by the above equation. The equation can, however, be corrected
by using the analysis of Leonard[45]. The maximum input power to the
collector-base varactor may be evaluated in terms of the direct
collector voltage V_{CC}. Substituting Eqn. 5.1 into 5.2, we obtain,

$$P_{oCmax} = 0.241(V_{CC} - V_{Csat})^2 \times C_{CB}(\frac{V_{CC} - V_{Csat}}{0.344}) \times \omega_1 \qquad 5.3$$

where P_{oCmax} is the maximum power output of the transistor as an
amplifier (equal to the maximum input power to the varactor), and
$C_{CB}(v)$ is the collector-base capacitance as a function of voltage.
V_{Csat} is the saturation voltage of the collector and should include
inductive effects in the base lead. If the output power from the
transistor (as an amplifier) is significantly greater than that
given by Eqn. 5.3, then it is likely that multiplication is occuring
through the action of the NLCSE.

The maximum power handling capability of the collector-base
nonlinear capacitance as a NLCSE may be found in a way similar to
the varactor. It is assumed that the conduction angle is 50%. The
ratio of direct voltage to peak reverse voltage is 0.245. (Reference
18) This factor may be combined with the equation in Fig. 4.11 to
obtain (similar to the way Eqn. 5.3 is derived),

$$P_{omax} = 1.043 \times (V_{CC} - V_{Csat})^2 \times C \times \omega_1 \qquad 5.4$$

and C is an average value of the depletion layer capacitance which

is normally two or three times greater than C_{CBmin}. Hence the NLCSE

doubler is able to handle about ten times as much power as the

varactor doubler for the same biasing voltage (V_{CC}).

If the input power decreases from that given by Eqn. 5.4 the

conduction angle (or bottoming period) will be less than 50% and

the peak reverse voltage will be less than $\left(\dfrac{V_{CC} - V_{Csat}}{.2450} \right)$.

If the input power is increased the conduction angle will increase

as well as the peak reverse voltage.

5.5   Discussion of the Transistor NOM

Transistor nonlinear output frequency multipliers have been

constructed and analysed. It is evident that multiplication often

occurs through a minority carrier charge storage mechanism in the

collector-base junction. This conclusion is at variance with

assumptions by other workers. The multiplication efficiency in the

transistor output was accurately calculated using the results of

Penfield and Rafuse[35] and also by the results of Chapter Four.

It is clear that the output multiplication is often a combination

of varactor action and minority carrier charge storage action. The

theory of minority carrier charge storage frequency multiplication

of Chapter Four is inadequate to treat the transistor NOM properly

even though it is the best available. The derivation of a complete

theory treating a NLCSE multiplier would, by itself, be a significant

problem. A theory, to be complete, would have to allow for the following: the nonlinear depletion layer capacitance and the minority carrier charge storage, different possible discrete frequency idlers, a wide range of conduction angles (period over which the nonlinear element is bottomed), and the possibility of imperfect charge recovery. It is likely to be sometime before such an analysis is developed and presented in the scientific literature.

Although the available theory is not complete for treatment of the multiplication mechanism, good estimates of NOM performance can be made using varactor theory and the NLCSE theory developed in Chapter Four. The amplifying section of the transistor NOM conforms moderately well to the theory developed in Chapter Two. The effects of feedback have not been analysed, these depending greatly on the circuit construction and tuning of the input and output circuits. Neutralisation can be carried out but difficulty is likely to be experienced in the uhf range, for example, neutralisation might be successful at the operating frequency only to cause oscillations at another frequency. In addition circuit complexity is increased.

The occurence of NLCSE frequency multiplication modifies the emphasis on the limiting transistor characteristics. A large collector-base depletion layer capacitance is not as essential as originally thought,[22] and the charge recovery characteristics of the collector-base diode become important. The operation of the transistor as an amplifier with the collector voltage bottomed becomes important.

The multiplexer, composed of helical line resonating elements, proved to be very effective with the transistor NOM. The multiplexer was, however, bulky and heavy, and would for general usage need to be constructed differently. It is felt, however, that the principle of tuning each harmonic individually is a good one, and a different means could be found to carry this out, providing physical compactness and light weight. The multiplexer was useful as a measurement device because the losses at each harmonic, for any shorting stub setting, could be accurately determined and recorded. Thus it is possible to make accurate estimates of the circuit losses of the transistor NOM. Such estimates would be difficult with conventional lumped circuits.

Frequency multiplication at the transistor output approximately doubles the maximum frequency of usefulness of the transistor. The amplifying section of the transistor (of the uhf NOM) had a power gain of about three or four (at 0.400 GHz), and nonlinear output multiplication increases the output frequency by a factor of two or three with a fairly modest loss. The performance of the transistor NOM is very similar to that of a transistor amplifier and a separate varactor; however, circuit complexity is reduced and the need for a separate varactor diode is eliminated. The transistor NOM is not capable of amplifying amplitude modulated signals, whereas a well design amplifier followed by a step recovery diode frequency multiplier can process amplitude modulated signals.

CHAPTER SIX

CONCLUSIONS

The feasibility of using the transistor as a vhf and uhf energy source has been demonstrated in the foregoing chapters. The transistor not only amplifies but also generates harmonics efficiently permitting frequency multiplication well into the uhf range. From the studies carried out here it is evident that a uhf energy source, deriving frequency stability from a low frequency crystal, can operate effectively using only transistors as both the active and nonlinear harmonic generating elements. The circuitry of a uhf energy source is likely to be simplest if transistors are used as the frequency multiplying elements.

A comprehensive study has been made of the two most useful frequency multiplication modes, one utilising an input nonlinearity, the other an output nonlinearity. The first, nonlinear input frequency multiplication, is examined carefully in order to provide a basic understanding of the multiplication mechanism. The operation of the multiplier is then analysed and performance characteristics are derived. The similarity between nonlinear input amplification and multiplication is exploited so as to extend the potential application of the derived results and also permit a comparison between amplifier and multiplier performance. In addition amplifier studies assist in the analysis of the nonlinear output multiplier.

In Chapter Two it is found that the power gain and collector efficiency performance lost through frequency multiplication (compared with an amplifier of the same output frequency) is not severe provided that the transistor is suited to the application. The theory and analysis of the "intrinsic base" is supplemented by the work of Chapter Three in order to take into account the effect of the depletion layer capacitances, these elements being the most likely to degrade the transistor performance in both the amplifying and multiplying functions. It is found that the limiting transistor characteristics are the same for good frequency multiplication and good class C amplification, both circuits requiring a good high frequency, large signal class A amplifier performance (transistor collector conducting at all times) plus some additional characteristics. The typical large signal class A amplifier requirements are: a high average maximum frequency of oscillation f_{max} (over the full collector current and voltage range), a small ratio of collector saturation voltage to collector breakdown voltage, a large collector power dissipation and a large product of maximum useable collector current and maximum collector voltage. A good transistor for high efficiency class C amplification or frequency multiplication should have in addition to the above characteristics: a large quotient of emitter-base breakdown voltage and extrinsic base resistance, and a small product of extrinsic base resistance and emitter-base depletion layer capacitance ($r_{bb}C_{BE1}$). The latter requirements are of increasing importance as the collector conduction

angle of the transistor is reduced. In many high-frequency power transistor presently available, the reverse breakdown voltage of the emitter-base junction is too low to permit efficient nonlinear input multiplication. Thus before a particular transistor, proven in high frequency class A power amplification, can be considered for use in class C applications, the reverse breakdown voltage of the input and the $C_{BE1}r_{bb}$ product must be checked to ensure suitability for the application.

Much of the analysis of the NIAM has depended upon assumptions that have not in practice been accurately met. The assumptions serve the purpose of simplifying the analytic approach and also reducing the required amount of data concerning the transistor characteristics and equivalent circuit. However the assumptions do not affect seriously the accuracy of the analysis. The chief limitation to an accurate analysis is the limited amount of information available about any particular transistor. The published manufacturer's data sheets seldom provide all desired information required here, and often some information must be inferred, as in Section 3.5. It is undesirable to have to make measurements on an individual transistor before its performance in an amplifying or multiplying circuit can be predicted. The accurate application of the theory of Chapters Two and Three depends upon estimated linearised values for the nonlinear actions of the transistor, such as feedback capacitance, extrinsic base resistance and high frequency current gain.

Further work on the NIAM would be most productive if it were aimed at using the results of Chapters Two and Three, taking into account all of the diverse characteristics and limitations of the transistor, with the object of finding the optimum operating conditions of an amplifier or multiplier for a particular criterion (i,e. maximum power gain, maximum power output, maximum ratio of output power to direct input power).

Chapter Four is devoted to the study of nonlinear charge storage elements that have two capacitive states (an infinite capacitance state and a finite, constant capacitance state) employed as a frequency multiplier. Preliminary measurements with the transistor output nonlinearity used for frequency multiplication, indicated that the nonlinear depletion layer capacitance was generally not capable of converting all the fundamental power that was applied to it. Varactor multipliers operating with more input power than they are theoretically capable of handling are said to be overdriven and power conversion then takes place largely through the action of minority carrier charge storage (occuring at the same time in the same device), none of which are sufficiently extensive and general enough to be applied to the transistor NOM. The analysis presented in Chapter Four is probably the most general (among those without discrete frequency idlers) available. It will deal with any multiplication factor and gives a good indication of the effect of conduction angle variation. The input and output resistances are adjusted for optimum efficiency. The results of the analysis are presentable in very compact form (i.e. two graphs, Figures 4.7 and 4.10

and Table 4.1 will deal with any harmonic).   Also, information on a

particular harmonic, if design information is not given, may easily

be calculated.

The analysis of Chapter Four, although originally derived to

analyse the transistor NOM, should find considerable application to

step recovery diode frequency multipliers.   The analysis is based on

an idealised multiplying circuit of this form.

A complete analysis of the overdriven varactor is a formidable

problem.   For present purposes consideration of a variable conduction

angle for the diode is desirable, as in the NOM the power input to

the varactor is usually the maximum that the transistor will deliver

and not optimised for mulitplication.   Idling circuits should be

considered.   The performance of the NLCSE should be specified as a

function of frequency, the diode losses due to series resistance and

imperfect charge recovery being accounted for.

Chapter Five reports on vhf and uhf amplifiers and nonlinear

output multipliers that have been constructed and analysed.   Examination

of the output waveforms and output powers shows quite conclusively that

minority carrier charge storage action comes into effect in such

multipliers.   The performance of a transistor NOM is comparable with

that of a transistor amplifier and a separate varactor multiplier.

This mode of operation can double or triple the maximum frequency of

usefulness (f_{max}) of the transistor.   For example, the uhf transistor

tripler studied hereconverted a fundamental power of 1.0 watts at

0.400 GHz into about 1.0 watts at 1.200 GHz. Thus the transistor provided a unity power gain as well as tripling to an output frequency of 1.2 GHz. The overall operation of the transistor NOM conforms moderately well to expectations, based on comparison with a transistor amplifier and a separate varactor multiplier. Some expected deviations from the above are found; for example, output multiplication increases feedback in the transistor, so increasing the possibility of instability, while maximum collector voltages are increased (the collector voltage assumes a shape that is a compromise for best amplification and for best multiplication). In the transistor NOM, the bias voltage on the multiplying diode is determined by the collector supply voltage V_{CC} and not by a self biasing arrangement; the amplifying and multiplying sections are not connected by ideal filters.

The conclusion that frequency multiplication occurs partially via a minority carrier charge storage mechanism modifies the requirements upon the transistor characteristics for efficient nonlinear output multiplication. For example, a transistor should have good amplification characteristics, even where the collector is saturated for a large percentage of the time, and the transistor collector-base junction should have a good charge recovery characteristics. A large collector-base capacitance with a good nonlinearity (i.e. $\gamma = 1/2$) is not of the paramount importance previously thought; in fact, a small capacitance with a small nonlinearity would permit good conversion efficiencies.

The measurements, carried out here on the voltage waveforms of the uhf transistor multiplier could be improved to permit a more exact examination of the operation. The transistor lead inductances obscured the transistor multiplication action considerably. Better measurements could be obtained by removing the transistor from its encapsulating can and mounting it directly onto a suitable transmission strip line, so permitting measurements at the transistor contacts. Or alternatively separate leads could be brought out of the transistor encapsulation which would be used purely as measurement probes, the lead inductances not being so important as measurement current flow could be small.

The transistor NOM uses fewer components than a transistor amplifier and varactor multiplier; it is, however, incapable of multiplying amplitude modulated signals.

The transistor, varactor, and step recovery diode have exhibited improved performances with device developments, permitting increased use as solid state microwave energy sources. The improvement is likely to continue for a number of years.

The varactor and step recovery diode are of interest, here because of the way they extend the usefulness of the transistor to higher frequencies. The multiplication efficiency of a step recovery diode may be much higher than the collector power conversion efficiency of a transistor but a chain of such frequency multipliers - following a transistor amplifier - will result in a low overall conversion

efficiency (output rf power to total direct input power). In order to enjoy the best overall conversion efficiency in a rf energy source either a transistor amplifier or a nonlinear input multiplier should be placed as close to the output as transistor performance will permit. A rf energy source (using an amplifying transistor at the output) has an overall efficiency equal to or better than a similar source using devices such as the klystron. On the other hand, a rf energy source using transistor amplifiers followed by a chain of varactor or step recovery diodes - to obtain high frequency multiplication factors - is likely to have power conversion efficiencies inferior to the klystron energy source.

APPENDIX 1

Graphical Fourier Analysis of Symmetrical Waveforms *

Figure A1.1
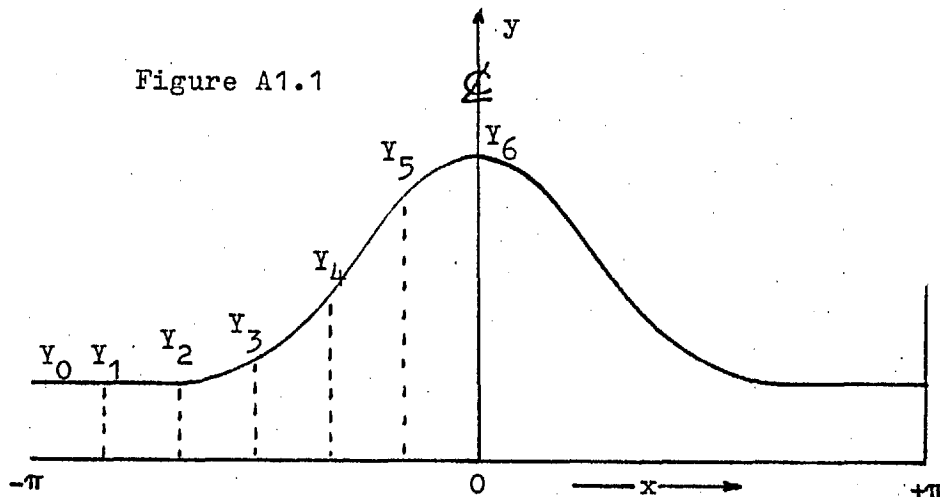
$\bar{y} = f(x)$ and,

$$f(x) \approx A_0 + A_1\cos x + A_2\cos 2x + A_3\cos 3x + A_4\cos 4x + A_5\cos 5x + A_6\cos 6x$$

$$A_0 = \frac{Y_0 + 2Y_1 + 2Y_2 + 2Y_3 + 2Y_4 + 2Y_5 + Y_6}{6}$$

$$A_1 = \frac{Y_0 + Y_2 + 1.733(Y_1 - Y_5) - Y_4 - Y_6}{6}$$

$$A_3 = \frac{Y_0 + 2Y_4 - 2Y_2 - Y_6}{6}$$

$$A_4 = \frac{Y_0 + 2Y_3 + Y_6 - Y_1 - Y_2 - Y_4 - Y_5}{6}$$

$$A_5 = \frac{Y_0 + Y_2 + 1.733(Y_5 - Y_1) - Y_4 - Y_6}{6}$$

$$A_6 = \frac{Y_0 + 2Y_2 + 2Y_4 + Y_6 - 2Y_1 - 2Y_3 - 2Y_5}{12}$$

---

* Taken from Reference 51 in modified form.

APPENDIX 2

Computer Program for the Solution of Transistor Amplifier

and Multiplier Equations.

The computer program is written in International Computer and Tabulator Fortran IV to solve the equations developed in Chapter Three describing the performance of transistor amplifiers and multipliers with feedback. Shown here is the flow chart, the program and sample output. The sample output shows the performance of a doubler. A range of mismatch conduction angles are chosen (2α) and performance is found and displayed in blocks of four numbers, i.e.,

> modified conduction angle
> calculated value of R_L/R_o
> modified collector efficiency
> modified power input

The results of the amplifier through to a quadrupler were plotted in Figures 3.9 to 3.12 in terms of modified conduction angle and the calculated value of R_L/R_o.

Flow Diagram

Select values of
R_L/R_o

Subroutine <u>Angmis</u>
Set value of ε

Calculate R_L/R_o using
Eqn. 3.17. If R_L/R_o
larger than selected
value make ε smaller
and if R_L/R_o smaller
make ε larger and
repeat calculation.
If R_L/R_o has corrpect
value go to master
section.

Subroutine <u>Srang</u>
Determine modified
conduction angle
($2\alpha'$) using
Eqn. 3.13

Subroutine <u>Srmis</u>
Calculate $f_1(\alpha',n,\varepsilon)$
from Eqn. 3.15

Calculate $f_2(\alpha',\varepsilon,n)$
using Eqn. 3.18

Calculate modified
collector efficiency
using Eqn. 3.19

Calculate input power
requirement using
Eqn. 3.22

Print
Modified conduction angle ($2\alpha'$)
Calculated value of R_L/R_o
Modified collector efficiency
Modified input power

```
      LIST(LP)
      SEND TO (MT)
      PROGRAM (PROG FDKAMPMOD)
      INPUT 1=CRO
      OUTPUT 2,(MONITOR)=LPO
      TRACE
      END
```

```
      MASTER FDK AMP
      DIMENSION ARSFM(10),ARCA(10),ARFM(10),AREFF(10),ARPIN(10)
      COMMON AA,AM,NH,CA,FM,SFM
      READ(1,3)(ARSFM(I),I=1,6 )
    3 FORMAT( 6(E8.2))
      DO 1 NH=1,6
      WRITE (2,7) NH
    7 FORMAT (1H1,I9)
      DO 2 IANG = 1,9
      AA = 2.0
      IF (NH .EQ. 1)  AA = 1.0
      AA = AA* .314159 * IANG/NH
      DO 4 JMIS=1,6
      SFM=ARSFM(JMIS)
      CALL ANGMIS
      ARCA(JMIS)=CA*114.59
      ARFM(JMIS)= AM/FM
      DCI = (-COS(AA/2) + COS(-CA+AA/2) + CA**2/2*COS(AA/2)
     1-AM/NH*SIN(NH*CA) + CA*(-SIN(-CA+AA/2) - CA*COS(AA/2)
     2+AM*COS(-NH*CA)))/3.14159
      AREFF(JMIS) = FM*.5/DCI
      PI = 3.14159
      PIN = SIN(AA)/4.0 + SIN(2*CA-AA)/4.0 + CA/2.0-COS(AA/2)
     1*(SIN(AA/2)-SIN(-CA+AA/2))-SIN(2.0*CA)/4.0 - CA/2*COS(AA)
     2+SIN(CA+AA/2)*COS(AA/2)-COS(AA/2)*SIN(AA/2)-NH*AM*((-COS
     3(-NH*CA-CA+AA/2) + COS(-NH*PI-PI+AA/2))/(2.0*(NH+1))+(+COS
     4(+NH*CA+CA+AA/2)-COS(NH*PI+PI+AA/2))/(2.0*(NH+1)))
      IF (NH .EQ. 1 ) GO TO 8
      PINX = (-COS(-NH*CA+CA-AA/2) + COS(-NH*PI +PI-AA/2))/(2.0*
     1(NH-1)) + (-COS(NH*PI-PI-AA/2) + COS(NH*CA-CA-AA/2))/(2.0*(NH-1))
      GO TO 9
    8 PINX = (PI-CA)*SIN(-AA/2)
    9 PINX = PINX*NH*AM
      PIN = PIN - PINX
      PIN = PIN/NH**2
      ARPIN(JMIS) = PIN/(PI*FM**2)
    4 CONTINUE
      AA=AA*114.59
```

```fortran
      WRITE(2,5) AA
    5 FORMAT(1H0,E9.3)
      WRITE(2,6) (ARCA(I),I=1,6 )
      WRITE(2,6) (ARFM(I),I=1,6 )
      WRITE (2,6) (AREFF(I),I=1,6 )
      WRITE(2,6) (ARPIN(I),I=1,6 )
    6 FORMAT (1H , 6(E11.3))
    2 CONTINUE
    1 CONTINUE
      STOP
      END
      SUBROUTINE ANGMIS
      COMMON AA,AM,NH,CA,FM,SFM
      AM = 2.0
      UAM = 2.0*AM
   35 UAM = .5*UAM
      IF (UAM .LT. .0000001) GO TO 38
      CALL SRANG
      CALL SRMIS
      IF (FM .LT. 0.0) GO TO 36
      IF (ABS(1-AM/(FM*SFM)) .LT. .005) GO TO 38
      IF (SFM - AM/FM) 36,38,37
   36 AM = AM-UAM
      GO TO 35
   37 AM = AM+UAM
      GO TO 35
   38 RETURN
      END
      SUBROUTINE SRANG
      COMMON AA,AM,NH,CA,FM,SFM
      CA = -2*AA-.0001
      DANG = -2*AA
   13 DANG=.5*DANG
      IF (DANG.GT.-0.0002) GO TO 11
      IF (COS(CA+AA/2)-COS(AA/2)+AM*NH*SIN(NH*CA)) 10,11,12
   10 CA=CA-DANG
      GO TO 13
   12 CA=CA+DANG
      GO TO 13
   11 CA=-CA
      RETURN
      END
      SUBROUTINE SRMIS
      REAL MIS1
      COMMON AA,AM,NH,CA,FM,SFM
      IF (NH .GT. 1) GO TO 21
   20 MIS1=SIN(AA/2)*CA/2
      GO TO 22
   21 MIS1=-(COS(NH*CA-CA   +AA/2)-COS(AA/2))/(2*(NH-1))
   22 FM=2/3.142*((COS(AA/2-CA*(NH+1))-COS(AA/2))/(2*(NH+1))+MIS1-(COS(A
     1A/2))*(-CA/NH*SIN(NH*CA)+1.0/NH**2-COS(NH*CA)/ NH**2)-AM*(CA/2
     2+SIN(2*NH*CA)/(4.0*NH))+SIN(NH*CA)/NH*(-SIN(-CA+AA/2)-CA*COS(AA/2)
     3+AM*COS(-NH*CA)))
      RETURN
      END
      FINISH
```
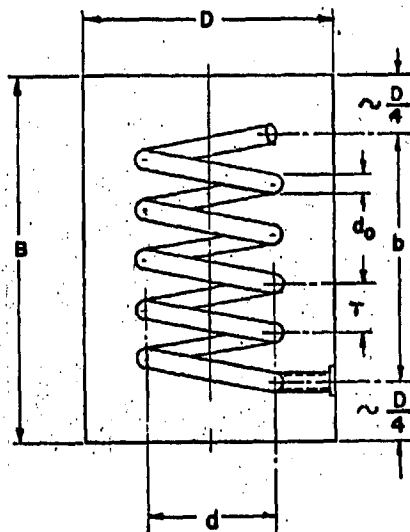
Printout for the Second Harmonic

2

```
0.360E  2
   0.360E  2   0.360E  2   0.359E  2   0.358E  2   0.356E  2   0.351E  2
   0.142E -2   0.200E  0   0.500E  0   0.996E  0   0.201E  1   0.499E  1
   0.974E  0   0.974E  0   0.974E  0   0.974E  0   0.974E  0   0.975E  0
   0.159E  3   0.160E  3   0.161E  3   0.163E  3   0.166E  3   0.177E  3

0.720E  2
   0.720E  2   0.715E  2   0.708E  2   0.697E  2   0.678E  2   0.637E  2
   0.100E -2   0.201E  0   0.499E  0   0.999E  0   0.201E  1   0.501E  1
   0.899E  0   0.900E  0   0.902E  0   0.905E  0   0.910E  0   0.920E  0
   0.227E  2   0.234E  2   0.244E  2   0.260E  2   0.290E  2   0.373E  2

0.108E  3
   0.108E  3   0.107E  3   0.105E  3   0.102E  3   0.972E  2   0.883E  2
   0.100E -2   0.200E  0   0.502E  0   0.100E  1   0.199E  1   0.501E  1
   0.785E  0   0.790E  0   0.797E  0   0.808E  0   0.823E  0   0.853E  0
   0.849E  1   0.902E  1   0.981E  1   0.111E  2   0.134E  2   0.199E  2

0.144E  3
   0.144E  3   0.142E  3   0.140E  3   0.136E  3   0.130E  3   0.118E  3
   0.100E -2   0.201E  0   0.501E  0   0.995E  0   0.201E  1   0.499E  1
   0.645E  0   0.652E  0   0.663E  0   0.678E  0   0.704E  0   0.753E  0
   0.501E  1   0.543E  1   0.605E  1   0.705E  1   0.901E  1   0.144E  2

0.180E  3
   0.180E  3   0.180E  3   0.180E  3   0.180E  3   0.180E  3   0.180E  3
   0.100E -2   0.201E  0   0.500E  0   0.100E  1   0.201E  1   0.500E  1
   0.494E  0   0.494E  0   0.493E  0   0.492E  0   0.489E  0   0.481E  0
   0.404E  1   0.464E  1   0.505E  1   0.608E  1   0.816E  1   0.144E  2

0.216E  3
   0.216E  3   0.219E  3   0.224E  3   0.231E  3   0.239E  3   0.250E  3
   0.100E -2   0.200E  0   0.501E  0   0.999E  0   0.200E  1   0.501E  1
   0.349E  0   0.332E  0   0.307E  0   0.269E  0   0.210E  0   0.120E  0
   0.426E  1   0.490E  1   0.599E  1   0.811E  1   0.136E  2   0.407E  2

0.252E  3
   0.252E  3   0.257E  3   0.263E  3   0.270E  3   0.276E  3   0.283E  3
   0.998E -3   0.201E  0   0.502E  0   0.997E  0   0.200E  1   0.500E  1
   0.221E  0   0.196E  0   0.165E  0   0.129E  0   0.680E -1   0.444E -1
   0.596E  1   0.748E  1   0.102E  2   0.160E  2   0.323E  2   0.117E  3

0.288E  3
   0.288E  3   0.292E  3   0.296E  3   0.300E  3   0.303E  3   0.307E  3
   0.996E -3   0.200E  0   0.499E  0   0.998E  0   0.199E  1   0.498E  1
   0.119E  0   0.100E  0   0.802E -1   0.599E -1   0.397E -1   0.196E -1
   0.121E  2   0.164E  2   0.245E  2   0.417E  2   0.903E  2   0.349E  3

0.324E  3
   0.324E  3   0.325E  3   0.327E  3   0.328E  3   0.329E  3   0.330E  3
   0.997E -3   0.200E  0   0.501E  0   0.100E  1   0.201E  1   0.499E  1
   0.457E -1   0.378E -1   0.300E -1   0.222E -1   0.147E -1   0.729E -2
   0.491E  2   0.699E  2   0.109E  3   0.192E  3   0.431E  3   0.170E  4
```

Appendix 3

The Harmonic Multiplexer

The four output port multiplexer used in the operation of the uhf transistor nonlinear output multiplier is based on helical line resonating elements[43]. The helical line resonator is a variation on a resonating quarter wavelength transmission line stub. The resonant element is gaining widespread usage in the vhf and uhf ranges. A sketch of a single element is shown in Figure A3.1. The element consists of a conductor coiled into a cylindrical cavity, one end of the conductor is earthed, the other is left floating. In this way small physical dimensions are achieved.

Figure A3.1

Sketch of a "helical line resonating" element.

Initially a single resonating element was constructed and used with the transistor for doubling for purposes of filtering the second harmonic power and transferring it into the load. The power was coupled into the cavity by a loop located near the earthed end of the helix (providing a magnetic coupling) and the power was extracted from the helix via a probe located near the floating end of the helix (capacitive coupling output). The single resonator worked well and it was decided to construct a more elaborate filtering arrangement using the helical resonator.

It was decided to make the filter with four output ports tuned to the fundamental through to the fourth harmonic, that is a port tuned to each of the frequencies; 0.40 GHz, 0.80 GHz, 1.20 GHz and 1.60 GHz. A suggested arrangement[43] for such a multiplexer uses an input coaxial transmission line of 50 Ω which is short circuited at one end. The helical resonators are capacitively coupled to the transmission line one quarter wavelength (or a multiple thereof) from the short. In this case the 50 Ω transmission line consists of a round copper conductor placed centrally into a slot with a square cross section. This slot intersects the cylindrical cavities of the resonating elements permitting the capacitive coupling between the transmission line and the resonating elements. Thus power is inserted into the cavities using capacitive coupling and power is extracted from the cavities using magnetic coupling loops. Figure A3.2

shows the approximate construction of the multiplexer. The
multiplexer was made from a brass block and the loops and helices
were placed and adjusted (to pass the correct frequencies with
low loss) and then the complete unit was silver plated. Tuning
screws were placed to modify the resonant frequency of each cavity.
The axis of the screws were placed on the axis of each helix.
Shown in Figure A3.3 is a photograph of the multiplexer with the
top plate (containing the tuning screws) removed. The output
frequencies of each port may be noted. The top of each helix may
be seen, to be in close proximity to the center conductor of the

Figure A3.2

resonating cavities 400 MHz 1600 MHz 800MHz 1200MHz shorting plate
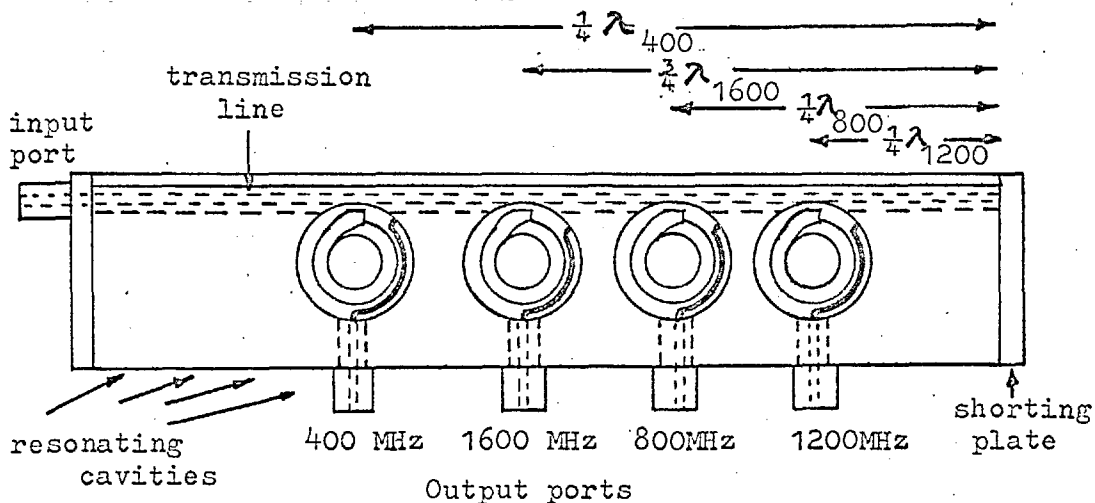
Output ports

Top view of harmonic multiplexer with top plate (containing tuning
screws) removed. The input and output ports are 50 Ω systems.
The tops of the helices are capacitively coupled to the trans-
mission line and the output ports are magnetically coupled (by
a loop marked in black) to each helix.

Figure A3.3

A photograph of the multiplexer with the top plate removed. Each output port may be seen (output frequencies indicated), and the center conductor of the transmission line may be seen in close proximity to the top of each helix.
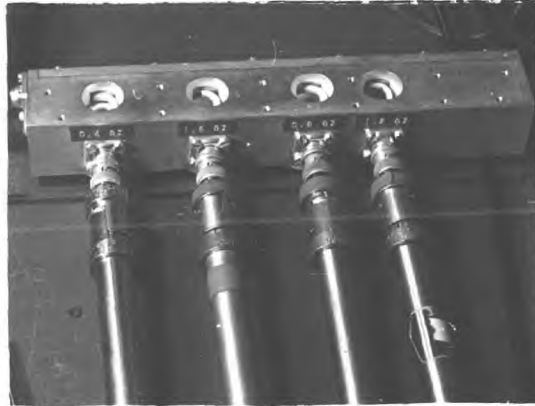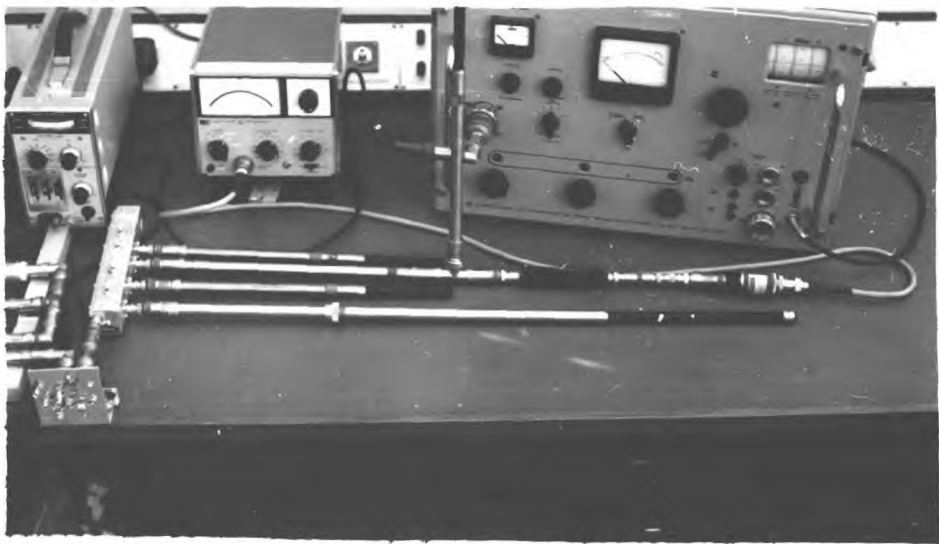
Figure A3.4

A photograph of the multiplexer in use. The transistor collector feeds into the common port. Variable length short circuited stubs are connected to the fundamental, third and fourth harmonic ports. The matching circuit and load are connected to the second harmonic port.

of the transmission line. In Figure A3.4 typical useage of the multiplexer is shown. In this particular setup the useful power output occurs at the second harmonic (800 MHz), the transistor being connected to the common port of the multiplexer. Fundamental power is rejected by the output filter because a variable length shorting stub is connected to the fundamental port. The fundamental power returns to the transistor in an optimum phase (the fundamental short circuit stub is adjusted for this) and is converted into a harmonic by the nonlinear effect of the transistor output. Most of the power will be converted into the second harmonic which is matched into a 50 Ω coaxial attenuator via a line stretcher and a parallel variable length shorting stub. An attenuator and a thermistor power meter measure the output power from the filter. The third and fourth harmonic stubs are also adjusted to maximise second harmonic power output. The performance characteristics of the harmonic multiplexer have been measured. The insertion loss of the multiplexer from the common port to each of the output ports has been measured, 50 Ω systems been used on both the input and output. The performance is shown in Figure A3.5 as a function of frequency. The spurious response of the fundamental port to 1.17 GHz should be noted, this being typical of transmission line resonating elements. Also the isolation of 20db should be noted. Parasitic feed-through occuring by magnetic coupling of the slot (of the transmission line) to the magnetic coupling loop of the output port. The third

Figure A3.5

Insert loss of each port of the multiplexer
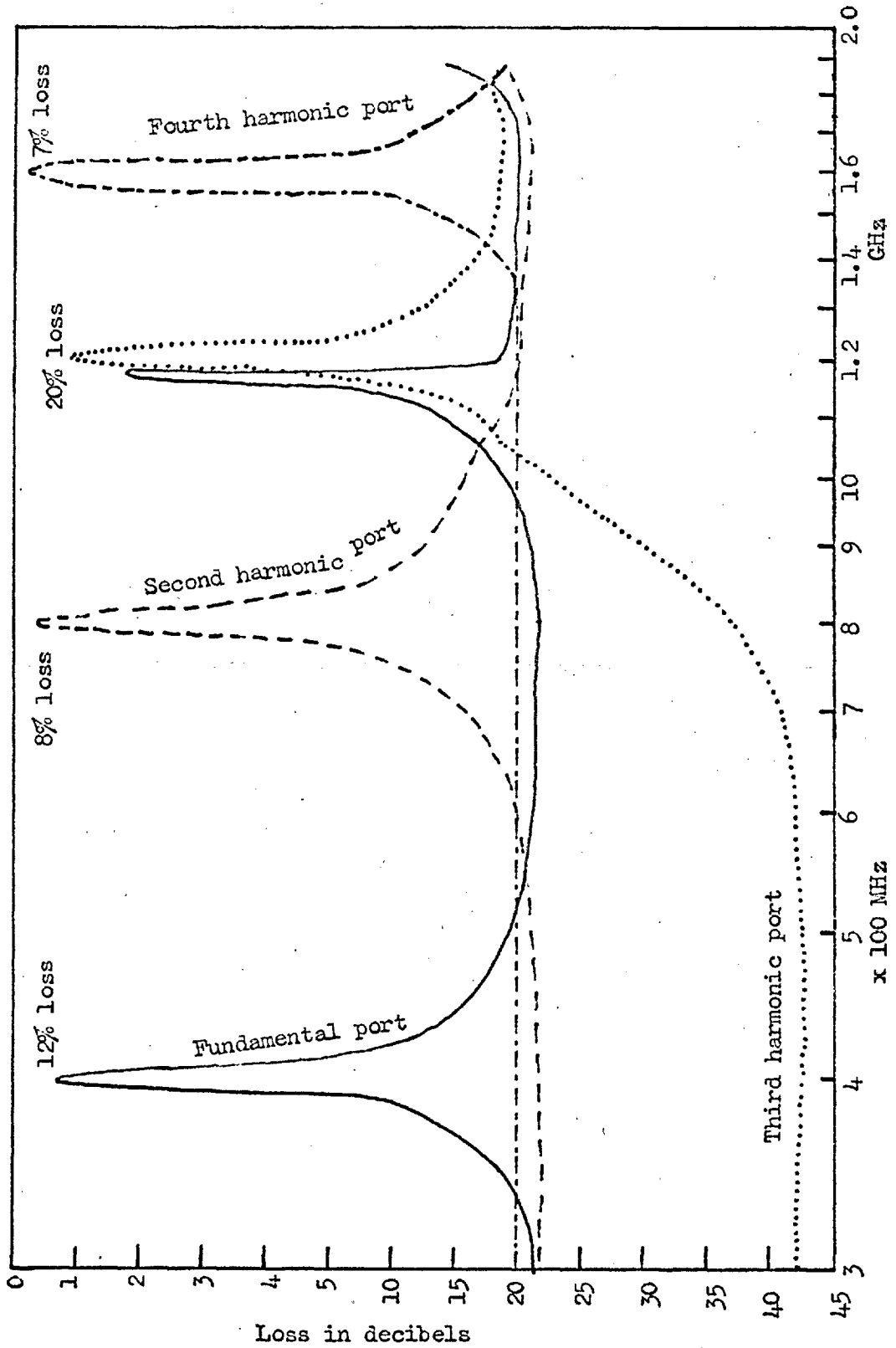
harmonic port had better isolation as modifications were made to this one and eventually the output port was capacitively coupled to the helix.

Another performance of the multiplexer, of interest, is the power lost into the common port when a short circuit is connected to the output port. This is measured for the fundamental to the third harmonic port and the measurements are shown in Figure A3.6. The loss is a function of the distance between the output port and the short circuit. The last two graphs may be used to estimate the circuit loss caused by the multiplexer.

Figure A3.6

Fundamental port (400 MHz)

Stub setting in cm.

Second harmonic port (800 MHz)

Stub setting in cm

Third harmonic port (1200 MHz)

Stub setting in cm
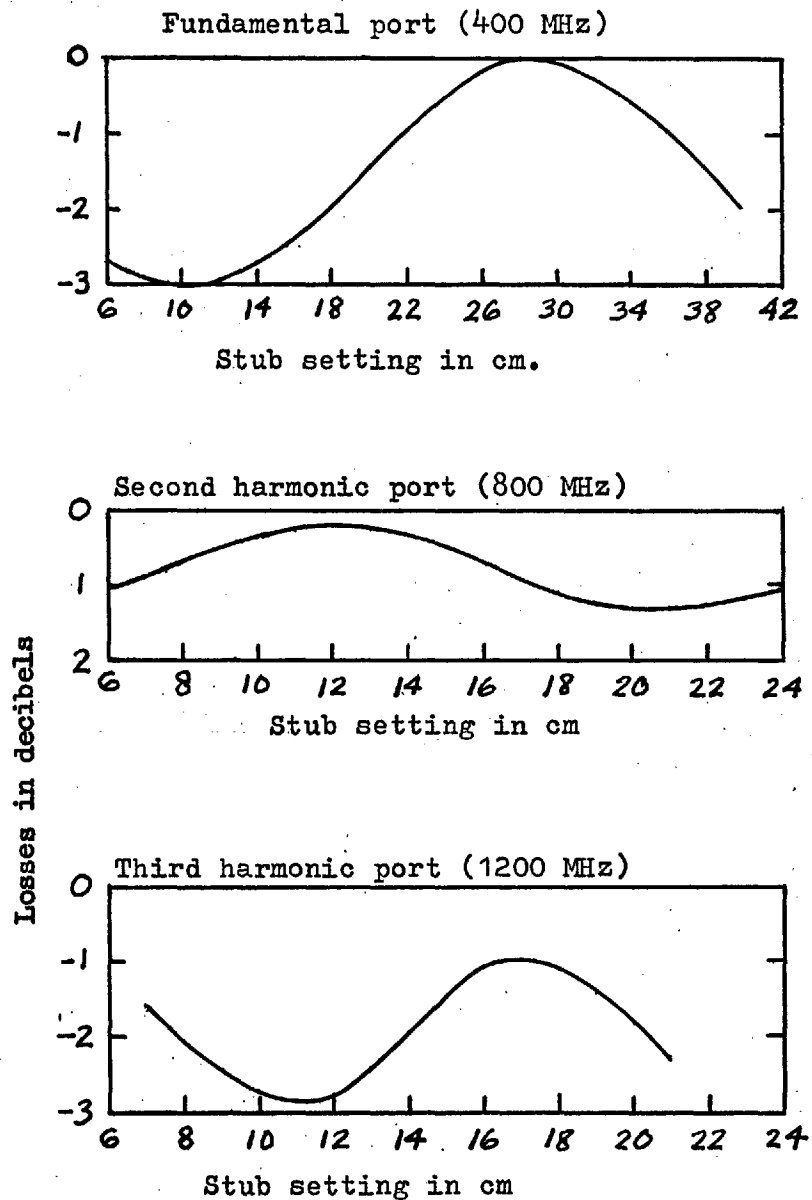
Reflection losses in three of the multiplexer ports, at each center frequency, when the output is terminated in a short circuit. The losses are a function of the distance between the short and the multiplexer. Lengths shown are direct GR shorting stub readings.

REFERENCES

1. D. C. Prince, "Vacuum tube power amplifiers", Proc. IRE, vol. II, pp. 275-313; June, 1923.

2. J. Marique "Note sur le calcul des etages multiplicateurs de frequence a triode", L'Orde Electrique, vol. 8, pp. 1; January 1929.

3. F. E. Ferman, J. H. Ferns, "The calculation of class C amplifiers and harmonic generation performance of screen grid and similar tubes", Proc. IRE, vol. 22, pp. 359-373; March, 1934.

4. R. L. Wallace, Jr., W. J. Pientenpol, "Some Circuit properties and applications of n-p-n transistors", Proc. IRE, vol. 39 pp. 753-767; July, 1951.

5. W. G. Matthei, "Recent developments in solid state microwave devices", Microwave Journal, vol. 9, no. 3, pp. 39-46; March, 1966.

6. J. G. Tatum, "Circuit improvements utilising the new resistor stabilised vhf power transistor", Proc. of the National Electronics Conference, vol. 21, pp. 73-78; October, 1965.

7. A. Evangelisti, "Design problems in transistor high-power output stages", Application Note AR-57, SGS - Agrate - Milano.

8. M. V. Bond, "Transistor rf power amplifiers", Wireless World, vol. 70, pp. 594-600; December, 1964.

9. J. A. Walston, J. R. Miller, "Transistor Circuit Design", Chapter 23, pp. 326-328, McGraw-Hill Book Company Inc., New York, N.Y.; 1963.

10. D. M. Duncan, "Non-linearity in transistor amplifiers", Proc. IREE of Australia, pp. 149-157; March, 1964.

11. T. M. Scott, "Tuned power amplifiers", IEEE Trans. on Circuit Theory, vol. CT-11, pp. 385-389; September, 1964.

12. J. A. G. Slatter, "An approach to the design of transistor tuned power amplifiers", IEEE Trans. on Circuit Theory, vol. CT-12, pp. 206-211; June, 1965.

13. J. K. Pulfer, A. E. Lindsay, "Simultaneous amplification and parametric frequency multiplication in vhf power transistors", Proc. IREE (Correspondence), vol. 52, pp. 212; February, 1964.

14. M. Caulton, H. Sobol, R. L. Ernst, "Generation of microwave power by parametric frequency multiplication in a single transistor", R.C.A. Review, vol. 26, No. 2, pp. 286-311; June, 1965.

15. H. C. Lee, G. J. Gilbert, "Overlay transistors move into micro-Wave region", Electronics, pp. 93-95, March, 1965.

16. R. J. Vilmur, K. Ishii, "Avalanching transistor generates micro-waves", Electronics, October 25, 1963.

17. D. F. Page, W. D. Hindson, W. J. Chudobiak, "On solid-state class D systems", Proc. IEEE (Correspondence), vol. 53, pp. 423-424; April, 1965.

18. D. H. Steinbrecher, "Limitations on parametric amplifiers and improved efficiency varactor multipliers", Ph.D. thesis, Massachusetts Institute of Technology; July, 1966.

19. T. Williams, "The design of triode harmonic generators", The Radio and Electronic Engineer, December, 1964.

20. J. Furlan, "Preliminary analysis of the transistor tuned power amplifier", Proc. IEEE (Correspondence), vol. 52, pp. 311; March, 1964.

21. R. Beaufoy, J. J. Sparkes, "The junction transistor as a charge-controlled device", Eqns. 20 and 21, A. T. E. Journal, Vol. 13, no. 4; 1957.

22. A. P. Anderson, R. J. McIntyre, M. P. Bachynski, "High frequency, high power transistor studies", Report written for R.C.A. Victor Co. Ltd., Montreal, July, 1965.

23. P. E. Gray, D. Dewitt, A. R. Boothroyd, "Physical Electronics and Circuit Models of Transistors", SEEC Notes 1 (PEM), Chapter 9, John Wiley and Sons, Inc. 1962.

24. L. P. Hunter, "Handbook of Semiconductor Electronics", Second Edition, Chapter 12, Equation 12.17, McGraw-Hill Book Company Inc., 1962.

25. Ibid; Chapter 12, equation 12.23.

26. D. F. Thomas, J. L. Moll, "Junction transistor short-circuit current gain and phase determination", Proc. IRE, vol. 46, no. 6, pp. 1166-1176; June, 1958.

27. J. A. Walston, J. R. Miller, "Transistor Circuit Design," Chapter
     25, pp. 345-349, McGraw-Hill Book Company Inc., New York, N.Y.;
     1963.

28. S. M. Krakauer, "Harmonic generation, rectification and lifetime
     evaluation with the step recovery diode", Proc. IRE, vol. 50,
     pp. 1665-1576; July, 1962.

29. G. Schaffner, "Charge storage varactors boost harmonic power",
     Electronics, vol. 37, no. 20, pp. 42-47; July 13th, 1964.

30. A. I. Grayzel, "A note on overdriven abrupt junction varactor
     doublers and frequency converters", Proc. IEEE, (Correspondence)
     vol. 53, pp. 2140; December, 1965.

31. R. J. Roulston, "Efficiency of frequency multipliers using charge-
     storage effect", Proc. IRE (Correspondence), vol. 49, pp. 1961-1962;
     December, 1961.

32. D. L. Hedderly, "An analysis of a circuit for the generation of
     high-order harmonics using an ideal nonlinear capacitor", IRE Trans.
     on Electron Devices, vol. ED-9, pp. 484-491; November, 1962.

33. R. J. Roulston, "Frequency Multiplication using charge storage
     effect: an analysis for high efficiency, high power operation",
     Intern. Jour. of Electronics, vol. 18, no. 1, pp. 77-86;
     January, 1965.

34. R. M. Scarlett, "Harmonic Generation with a capacitor exhibiting
     an abrupt capacitance charge," Proc. IEEE (Correspondence), vol. 52
     no. 5, pp. 612; May, 1964.

35. P. Penfield and R. Rafuse, "Varactor Applications", Chapter 8,
     Technology Press of M.I.T., Cambridge, Mass., John Wiley and
     Sons, Inc., New York, N.Y.; 1962.

36. D. H. Steinbrecher, "Efficiency limits for tuned harmonic
     multipliers with punch through varactors", ISSCC Digest of
     Technical Papers, vol. 9, pp. 20-21; February, 1967.

37. R. Zuleeg, V. W. Vodicka, "Parametric amplification properties
     in transistors", Proc. IRE, (Correspondence), vol. 48, pp. 1785;
     October, 1960.

38. A. P. Anderson, "Circuit aspects of transistor parametric
     frequency doublers", IEEE Transactions on Electron Devices,
     vol. ED-14, no. 2, pp. 86-89; February, 1967.

39. H. C. Lee, "Microwave power generation using overlay transistors", R.C.A. Review, vol. 27, no. 2, pp. 199-215; June, 1966.

40. D. R. Carley, P. L. McGeough, J. F. O'Brien, D. J. Donahue, B. A. Jacoby, J. Eimbinder; "The overlay transistor", Electronics, pp. 70-84, August 23, 1965.

41. R. D. Thornton, D. Hewitt, E. R. Chenette, P. E. Gray, "Characteristics and Limitations of Transistors", Section 1.7, SEEC, vol. 4, John Wiley and Sons Inc., 1966.

42. R. Minton, H. C. Lee, "Designing transistor multipliers", Microwaves, vol. 4, no. 11, pp.18-28; November, 1965.

43. M. Cohen, "Design techniques utilising helical line resorators", Microwave Journal, vol. 8, no. 5, pp. 69-73; May, 1965.

44. A. J. Anderson, H. F. Cook, B. T. Vincent Jr., "Microwave power generation and amplification using transistors", Presented to the Annual Northeast Electronics Research and Engineering Meeting, November 3, 1965.

45. T. C. Leonard, "Prediction of power and efficiency of frequency doublers using varactors exhibiting a general nonlinearity", Proc. IEEE, vol. 51, no. 8, pp. 1135-1139; August, 1963.

46. R. E. Hayes, "Step-recovery action in transistors", Electronics Letters, vol. 3, no. 4, pp. 151; April, 1967.

47. C. H. Page, "Frequency conversion with positive nonlinear resistors", J. Res. Nat, Bur. Stand., vol. 56, pp. 179-181; 1956.

48. R. H. Johnston, A. R. Boothroyd, "Two-port representation of a nonlinear-resistance frequency multiplier", Electronics Letters, vol. 2, no. 7, pp. 246-247; July, 1966.

49. R. H. Johnston, A. R. Boothroyd, "Change storage frequency multipliers using capacitance idling circuits", Paper submitted to Proc. IEEE.

50. H. P. Westman (Editor), "Reference data for radio engineers", p. 166, Fourth Edition, International Telephone and Telegraph Corporation, New York, N.Y.; July, 1961.

51. Ibid; pp. 1009-1011.