CHARGE CONTROL APPROACH TO CHARACTERIZATION OF FIELD EFFECT TRANSISTORS WITH APPLICATION TO LOW LEVEL SWITCHING

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ABSTRACT

The basic charge control relationships for field effect transistors and insulated gate transistors are derived on the basis of operation with open (i.e. unpinched-off) channels. The charge control relationships for field-effect transistors are shown to apply for one- or two-gate structures without regard to channel doping density profile so long as the majority carrier mobility in the channel is constant. Factors affecting the validity of the charge control relationships, such as mobility variations, and wedge-shaped channel effects are studied, and the charge control approach is compared with Shockley's "gradual case" theory.

Measured results on several types of devices are presented and discussed in detail. It is shown that the basic theory is sound, and that, in the case of field-effect transistors, it can be simply modified for use under pinch-off conditions of operation. It is also shown that a considerable amount of information about the behaviour of a device can be obtained from a study of its charge control relationships.

Models are derived and techniques are developed for predicting the low level switching behaviour of field-effect transistors. Comparisons of calculated and measured transients for several models show that the distributed nature of these devices is an important consideration under transient conditions. Thus, multi-lump models are generally required to represent field-effect transistor switching behaviour adequately.

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List of Principal Symbols

B	= Slope of the gate charge versus gate voltage relationship on a log-log graph
C_i, C_p, C_s	= Capacitances associated with the measurement of gate charge
C_{gs}, C_{gd}, C_{ds}	= Stray capacitances
C_L	= Load capacitance
E	= Pulse switching voltage
FX, FY, etc.	= Factors used in models 3T and 1T in the representation of the Q_{gg} versus V_g relationship
g_o	= Conductance of a unit length of channel at zero applied bias
G_{ch}	= Channel conductance
G_{cho}	= Channel conductance with zero applied voltages
I_d	= Drain current
I_i	= Junction leakage current
K	= Dielectric constant
K	= V_2'/V_1' for measurement of gate charge
K_{ox}	= Dielectric constant of oxide
L	= Channel length
L^2/μ ratio	= Slope of gate charge versus channel conductance relationship at zero drain voltage
N_a, N_d	= Doping density
NT	= Normalized computer program time
P,U,V,W,X,Y,Z	= Normalized charges associated with the low level switching models and used in the computer programs

Q_A, Q_B, Q_C, etc. = Charges in the capacitive element of lumps A, B, C, etc. of a low level switching model

Q_{ch} = Majority carrier charge in the channel

Q_g (FET) = Uncovered depletion layer charge on either side of the gate junction, due to applied gate and drain voltages

Q_g (MOST) = $Q_{gg} + Q_{gd}$ = Net gate charge

Q_{gg} (FET) = Component of depletion layer charge due to gate voltage

Q_{gg} (MOST) = Component of gate charge due to applied gate voltage

Q_{gd} (FET) = Component of depletion layer charge due to drain voltage

Q_{gd} (MOST) = Component of gate charge due to drain voltage

Q_o (FET) = Majority carrier charge in the channel with zero applied voltages

Q_o (MOST) = Charge which must be added to or subtracted from the channel to just produce pinch-off

Q_s = Uncovered substrate charge

Q_{st} = Charge in surface traps

R_L = Load resistance

R_{ps}, R_{pd} = Parasitic bulk source and drain contact resistances

S, D = Factors used in models 3T and 1T in the representation of the Q_{gg} versus G_{ch} relationship

t = time

T = Normalized time

T_{ox} = Thickness of gate oxide layer in the MOST

V_1, V_2, V_1', V_2' = Pulse voltages associated with the measurement of gate charge

V_g = Applied gate voltage

V_d	= Applied drain voltage
V_{po}	= Pinch-off voltage assuming zero drain voltage
τ_d	$= L^2/\mu V_d$ = Slope of gate charge versus drain current relationship at constant applied drain voltage
ρ	= Charge density
μ	= Majority carrier mobility

CHAPTER 1

INTRODUCTION

1.1 Historical Background

Records of early experiments on devices operating on the field-effect principle date back to 1926 when the first of a series of patents was filed by Lilenfeld [1-3] of America, and subsequently by Heil of Germany [4]. These devices, though crude in form, resembled the insulated gate type of devices discussed subsequently.

Further studies on the effects of the fields were undertaken at the Bell Telephone Laboratories after the war under the direction of Shockley. This research led directly to the discovery of the point contact transistor by Bardeen and Brattain [5] in 1948. Also at this time, experiments were being carried out by Shockley and Pearson in an attempt to modulate the conductance of a thin film of semiconductor material with an electric field applied perpendicular to the semiconductor surface [6]. Although field-effect modulation was in fact achieved, the extent of the modulation was found to be considerably less than expected. The difference was assumed to be due to bound charges on the semiconductor surface.

Subsequent work by Shockley led to the development and analysis of the bipolar junction transistor in 1949 [7]. He then returned to his earlier field-effect experiments and proposed a new method of achieving field-effect conductance modulation resulting in the junction field-effect transistor (FET) in 1952[8]. In this device, modulation was achieved by the depletion layer associated with a reversed biased P-N junction, and thus the earlier problems associated with surface

effects were effectively bypassed. Experimental verification of field-effect transistor operation, and certain extensions to Shockley's basic theory were presented in papers by Dacey and Ross [9, 10], also of Bell Telephone Laboratories.

The field-effect transistor did not become truly commercially available for nearly ten years after its announcement. During the intervening years, they existed mainly as experimental laboratory items and were investigated in various forms [11-13]: some consideration was given to possible useful applications of such devices [14-19]. The main activity, however, was concentrated on developing and refining manufacturing techniques for the bipolar transistor, which were later to be used to advantage in the production of field-effect transistors.

During this time as well, interest was stimulated in other directions, and several related new devices, such as the analog transistor [20], the chargistor [21], the field-effect tetrode [22], and the field-effect phototransistor [23], were proposed. The most important new development, however, was the insulated gate transistor or metal-oxide-semiconductor transistor (MOST) proposed by Kahng and Atalla in 1960[24-26]. This device, now becoming generally commercially available, was made possible by the advent of surface passivation techniques [27] which were developed after the early conductance modulation experiments by Shockley and Pearson [6]. A related device, the thin film transistor, was announced by Weimer in 1962 [28]. It thus appears that these devices are practical realizations of what the earlier researchers in the field had originally set out to achieve.

1.2 Formulation of the Problem

The field-effect transistor (FET) and the insulated gate transistor (MOST)* differ fundamentally in operation from the conventional bipolar junction transistor. The FET and MOST belong to the class of unipolar transistors in which one type of carrier predominates, so that conduction takes place by means of a flow of majority carriers. It is to be expected therefore that such devices show marked differences in their characteristics as compared with the bipolar transistor, and have different advantages and disadvantages.

Early investigations concerned initially with the FET indicated that this device had several important advantages over the bipolar transistor. In addition to its high input impedance which can often be advantageous [15,29], it is relatively noise free [30]; it has a higher resistance to nuclear radiation damage [31]; it is often more conveniently used in certain integrated circuits than the bipolar transistor [32]; and because the drain current is self-limiting, it is less likely to be burned out than the bipolar transistor.

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* In this and in all subsequent parts of this thesis, the term "field-effect transistor" (abbreviated "FET") is assumed to refer specifically to a Shockley-type junction unipolar transistor unless otherwise indicated. Similarly the term "insulated-gate transistor" (sometimes called metal-oxide-semiconductor transistor, and abbreviated in both cases as "MOST") is assumed to refer specifically to the Kahng-Atalla type unipolar transistor.

One of the most interesting features about this device to the author, however, is the fact that due to the absence of rectifying junctions between the source and drain, virtually no offset voltage is present in the "on" condition [33]. This, together with its very high "off" resistance, suggested that the FET might be advantageously used as a low level switch or "chopper". A comparison study by Fattal [34] has confirmed that this is the case.

After the original papers on field-effect transistors by Shockley [8], Dacey and Ross [9,10], and Prim and Shockley [35], a considerable period of time elapsed with no significant contributions to the knowledge of the device. Possibly the next major contribution was a study of field-effect transistor noise in August 1962 by van der Ziel [30]. Toward the end of 1962, however, with the FET becoming commercially available, a new interest was being shown in this device.

It was at this time also that research on this project was started. Certainly the major contribution to the understanding of the FET at that time was contained in Shockley's original paper. His "gradual case" analysis is the landmark in the field, and became increasingly important as the same approach was used in the analyses of the MOST [36-38]. A somewhat more general form of this approach was also used by Bockemuehl early in 1963 in a study of FET's with arbitrary charge distributions [39].

Shockley's work was concerned with D-C and small signal behaviour, and consequently little was known of the transient performance of the FET. It was also apparent that certain aspects of FET operation,

concerning for example the pinch-off process, were not entirely clear. Further, the full implications of Shockley's "gradual case" assumption did not appear to be generally realized. Nor was it always easy to tell over what ranges of operation in a given device that this basic assumption was valid. It therefore become evident that further device characterization was necessary before switching studies could be carried out.

Having thus decided on the basis for the project, the approach to the problem was considered. Several important points emerged. Firstly, facilities were not available for the construction of special devices, and it was considered desirable to work with standard commercially produced devices. Just as with bipolar transistors, commercial FET's were being produced by several different manufacturing processes, eg., alloying, diffusion, etc., and as a result, FET's of a variety of different structures could be expected. To be at all practical, any method of characterization would have to enable these differences to be understood and accommodated.

Secondly, although interest centered mainly on the low level switch, it would be valuable if the method of device characterization were to contribute to the knowledge of device operation as a whole, and at the same time, cover or permit extension of its range to cover, completely general switching processes.

Thirdly, other than the "gradual case" assumption, it became increasingly clear that certain assumptions common to both the work of Shockley [8], and of Bockemuehl [39], would not always be valid in practical devices. One such assumption is that the doping density

on the gate side of the P-N junction or junctions, is much greater than that in the channel. In other words, the applied gate voltage is assumed to take place only across the depletion layer(s) in the channel.

It is true that voltage drop across a depletion layer on the gate side of the junction serves no useful purpose. However " In today's practical structures, the design compromise thus entailed frequently involves approximately equal doping in the gate and channel regions. This gives reasonable efficiency, and at the same time gives acceptably low parasitic capacitance per unit area. It also makes the critical dimensions less subject to change through solid-phase diffusion during heat treatment procedures." *

One further such assumption is that the majority carrier mobility is constant throughout the channel. A consideration of basic solid-state physics (41) indicates that such an assumption is true only if certain conditions are placed on the doping density levels in the channel. These conditions do not always apply to commercial FET's.

In 1957, Beaufoy and Sparkes(42), and subsequently Beaufoy (43), and Sparkes(44,45), showed that it was highly advantageous to treat the bipolar transistor as a charge controlled device. Further, it was shown by Johnson and Rose (46), that certain aspects of this type of approach could usefully be applied to other electronic devices with emitter, control and collector functions. It was decided to adopt this approach in the study of field-effect transistors. It was felt that this approach might provide a satisfactory answer to the characterization requirements,

*Ref. 40, page 217

not only for FET's , but for MOST's as well. This approach also showed promise of forming the basis of equivalent circuits for studying the low level switching performance of these devices.

This thesis is thus effectively divided into two parts. The early chapters are concerned with general problems of characterizing the FET from the charge control point of view. The remaining chapters are concerned with the application of the charge control approach to low level switching. Consideration from this point of view is also given to the MOST.

1.3 Statement of Original Work

Except where reference is made to the work of others, the contents of this thesis represent the results of original research carried out independently by the author.

CHAPTER 2

FIELD-EFFECT TRANSISTORS AND CHARGE CONTROL

2.1 Introduction

It is the object of Chapter 2 firstly to present the charge control point of view, and to establish the charge control relationships for both field-effect transistors (FET's) and insulated gate transistors (MOST's). Sections 2.3, 2.4, and 2.5 are devoted to this. Charge control models covering FET and MOST operation with unpinched-off channels are developed and presented in Section 2.6.

It is also intended in this chapter to compare in greater detail the approach of Shockley with the charge control point of view. This is the work of Section 2.7.

By way of introduction to FET's, Shockley's basic theory is presented in Section 2.2. Although it is not required for the development of the charge control relationships, it is necessary for the work of Section 2.7.

2.2 Shockley's Basic Theory

As an introduction to the field-effect transistor, and so that it may be compared with the charge control approach, Shockley's basic theory [8] of field-effect transistor operation will be briefly presented in this section.

The structure to be analyzed is shown in Fig. 2.2.1. It consists essentially of an N-type bar of semiconductor material , on top and bottom of which are layers of P-type semiconductor material forming

P-N junctions. A low resistance contact is assumed at each end of the N-type bar labelled source and drain, and at the P-type layers, labelled gates. The two gates are assumed to be tied together.

Under normal operating conditions, a positive voltage V_d is applied to the drain with respect to the source terminal, and a negative voltage is applied to the gates. Current flows in the N-type bar, due to V_d, and consists essentially of majority carriers, in this case electrons, flowing from source to drain. A depletion layer or space charge region is formed at each gate junction due to the reverse bias effect of the gate voltage V_g and the drain voltage V_d. The effect of these space charge regions is to vary the area through which the source-drain current can flow (called the channel), and thus vary the resistance between source and drain, and, consequently, the amount of current flow in the channel.

For purposes of the analysis, it is assumed that:

(1) The gate junctions are abrupt.

(2) The reverse bias junction leakage currents are negligibly small.

(3) Electron mobility in the channel is constant.

(4) The charge density in the P-regions is much greater than that in the N-region.

(5) Complete depletion holds true for the space charge regions.

(6) Source and drain contact resistances are zero.

(7) Device terminal voltages are such that Shockley's "gradual case" approximation is valid.

(8) The junction equilibrium potential is negligible.

Symmetry is assumed with respect to the center of the channel as

y=0. Thus 2a is the distance between junctions, and 2b is the distance between space charge layers. The relationship between depletion layer width and junction voltage is obtained from Poisson's equation.

$$K \frac{d^2V}{dy^2} = - K \frac{dE_y}{dy} = -\rho(y) \qquad (2.2.1)$$

where K is the dielectric constant, V is the potential, and E is the electric field.

As a consequence of assumption (4), the space charge region is assumed to exist mainly in the N-region, giving negligible voltage drop in the P-region. From the complete depletion assumption, (5), it follows that

$$E_y = 0 \text{ at } y = b \qquad (2.2.2)$$

Then, by integration of equation (2.2.1)

$$E(y) = + \frac{\rho_n (y-b)}{K} \qquad (2.2.3)$$

where ρ_n is the charge density in the N-type material and is given by

$$\rho_n = q (N_d - N_a) \approx q N_d \qquad (2.2.4)$$

N_d and N_a are the densities of donors and acceptors respectively, and q is the electronic charge.

If V_d is zero, the voltage drop across the depletion layer can be found by integrating equation 2.2.3, giving

$$\int_{V=0}^{V=V_{gate}} dv = - \int_{y=b}^{y=a} E(y)\, dy \qquad (2.2.5)$$

$$V_{gate} = -\frac{\rho n}{2K} (a-b)^2 \qquad (2.2.6)$$

since the channel voltage equals zero. The gate voltage required to make the channel width 2b equal to zero is called the pinch-off voltage (V_{po}) and from equation 2.2.6 is defined as

$$V_{po} \equiv \frac{\rho n}{2K} a^2 \qquad (2.2.7)$$

Also, from equation 2.2.6

$$b = \left[1 - \left(\frac{V_g}{V_{po}}\right)^{1/2} \right] a \qquad (2.2.8)$$

If now a small positive drain voltage V_d is applied such that conditions along the channel vary gradually (this assumption is considered in more detail in Section 2.7) , the one-dimensional form of Poisson's equation is assumed to apply.

The channel height (b) at any point along the channel will then be determined by the total reverse bias (V) across the channel depletion layer as follows :

$$b(v) = a \left[1 - \left(\frac{V}{V_{po}}\right)^{1/2} \right] \qquad (2.2.9)$$

The resulting current flowing in the channel is then calculated from

$$I_d = g(v) \frac{dV}{dx} \qquad (2.2.10)$$

where

$$g(v) = 2\mu q N_d Bb(v) = 2\mu q N_d B a \left[1 - \left(\frac{V}{V_{po}}\right)^{1/2} \right] \qquad (2.2.11)$$

$$g(V) = g_o\left[1 - \left(\frac{V}{V_{po}}\right)^{1/2}\right] \qquad (2.2.12)$$

and where μ = majority carrier mobility

B = channel width

L = channel length

$g_o = 2\mu qN_d Ba$ = conductance of a unit length of channel at zero bias

and V = drop across the depletion layer potential at any point along the channel = channel voltage minus gate voltage = $V_{ch}(x) - V_g$

Substituting equation 2.2.12 into equation 2.2.10 , and integrating,gives

$$I_d \int_{x=0}^{x=L} dx = g_o \int_{V=-V_g}^{V=V_d-V_g}\left[1 - \left(\frac{V}{V_{po}}\right)^{1/2}\right] dV \qquad (2.2.13)$$

where I_d is independent of x, and

$$I_d = \frac{V_d g_o}{L}\left[1 - 2/3\left\{\frac{(V_d + V_g)^{3/2} - (V_g)^{3/2}}{V_d\ (V_{po})^{1/2}}\right\}\right] \qquad (2.2.14)$$

Equation 2.2.13 holds only for

$$V_g + V_d \leq V_{po} \qquad (2.2.15)$$

the drain current being assumed constant with further increases in drain voltage V_d. The resultant family of drain characteristics is shown in Fig. 2.2.2.

2.3 FET Charge Control Relationships

2.3.1 Basic Theory

The term charge control is not new. References to its use extend as far back as 1954 [47] in connection with photoconductor studies. In 1957, this concept was used to advantage by Beaufoy and Sparks [42] to describe the performance of bipolar transistors. Johnson and Rose [46] used the charge control concept in their simple, general comparative analysis of amplifying devices in 1959, and subsequently it has been used extensively by Sparks [44, 45] and others in the literature on bipolar transistors.

For the purposes of this thesis, the term "charge control" is used to refer to the effect that an amount of charge in the gate or controlling electrode of a device, has on the output characteristics of that device (i.e. on output current or conductance). "True charge control" is assumed to exist in a field-effect transistor for example, when there is a proportional relationship between the amount of gate charge and the output current, or channel conductance.

The charge control relationships are derived with reference to Fig. 2.3.1. This is a more general and extended treatment based on the approach used by Johnson and Rose [46] in their discussion of field-effect transistors.

Fig. 2.3.1 shows a bar of semiconductor material with dimensions L, B, and H, with a gate junction on one side. The doping density in the semiconductor bar is assumed to be arbitrary and of the form

$$\rho = \rho(y, z) \tag{2.3.1}$$

On either side of the gate junction, a depletion layer is formed, the

size and shape of which depend on the applied potentials V_g and V_d, the doping densities and their profiles on either side of the junction, and on the shape of the structure.

The application of Gauss's Theorem [48] to an enclosed area surrounding a P-N junction requires that the amount of uncovered charge on one side of a P-N junction be equal and opposite to that on the other side of the junction. Further, this must hold true regardless of the doping profile on either side of the junction. From a knowledge of basic P-N junction theory [49], the essential operating mechanism of the field-effect transistor can be understood.

If a given number of electrons N are injected into the P-side of a junction, as illustrated in Fig. 2.3.2, they will combine with holes to uncover an equal number N of negative fixed charges on the P-side. But the electrons, having been drawn from the N-side originally as a result of the application of the voltage V, have left an equal number N of positive fixed charges on the N-side. The important point as far as FET's are concerned, is that the number of electrons available for conduction in the N-type channel is reduced by the number N, and as a result the conductance of the channel has been decreased proportionally.

In practical junctions, there is a small but finite leakage current across the junction. If the voltage V is removed by opening the external circuit, the leakage current will gradually reduce the number of uncovered charges on each side down to the number corresponding to equilibrium junction potential.

If, on the other hand, the external voltage V were maintained,

an external current equal to the junction leakage current would flow. Thus the junction leakage current causes neither an increase nor a decrease in the average number of conduction electrons in the channel.

In both cases therefore, charge equality on both sides of the junction is maintained. Depending on the application, however, the size of the leakage current may or may not be significant in comparison with the current flowing in the other terminals of the device.

The relationship between channel conductance and the amount of charge in the channel will be obtained firstly with $V_d=0$. Let dG be the conductance of the differential volume element of height dy, width dz, and length L, at any point (y, z) in the channel. Then from Ohm's Law for this volume element [50],

$$dG = \frac{\rho(y,z)\ \mu dy\ dz}{L} \tag{2.3.2}$$

where μ is the majority carrier mobility in the differential volume. The total conductance is given by integration over the cross section area of the channel, i.e.,

$$G_{ch} = \frac{1}{L} \iint_{z\,y} \rho(y,z)\ \mu\ dy\ dz \tag{2.3.3}$$

Similarly, the charge in the differential volume is given by

$$dQ = L\rho(y,z)\ dy\ dz \tag{2.3.4}$$

and the total charge in the channel is also found by integration over the channel cross section ; therefore,

$$Q_{ch} = L \iint_{z\,y} \rho(y,z)\ dy\ dz \tag{2.3.5}$$

For many devices, the level of doping density in the channel is below

$10^{15}/cm^3$ or so, in which case the carrier mobility can be assumed constant. (The effects of non-constant mobility will be considered in Section 2.3.2.) The relationship between channel charge and channel conductance is then simply

$$\frac{Q_{ch}}{G_{ch}} = \frac{L^2 \int\limits_z \int\limits_y \rho(y,z)\, dy\, dz}{\mu \int\limits_z \int\limits_y \rho(y,z)\, dy\, dz} \qquad (2.3.6)$$

or

$$Q_{ch} = \frac{L^2}{\mu} G_{ch} \qquad (2.3.7)$$

From the previous discussion, the charge in the channel can be represented by

$$Q_{ch} = Q_{oo} - Q_{gt} \qquad (2.3.8)$$

Q_{gt} is the amount of charge in the depletion layer on the channel side of the junction and is equal to the amount of charge in the depletion layer on the gate side of the junction. Q_{gt} is given by

$$Q_{gt} = Q_g + Q_{eqm} \qquad (2.3.9)$$

where Q_{eqm} is the amount of equilibrium depletion layer charge, and Q_g is the extra charge in the depletion layer due to external reverse bias on the gate junction. Q_{oo} is constant for the device, and is the total mobile charge due to doping within the extreme bounds of the channel with no depletion layers present. For the structure in Fig. 2.3.1, it is given by

$$Q_{oo} = L \int_{z=0}^{B} \int_{y=0}^{2a} \rho(y,z)\, dy\, dz \qquad (2.3.10)$$

Equation 2.3.7 then becomes

$$G_{ch} = \frac{\mu}{L^2} (Q_{oo} - Q_{gt}) \qquad (2.3.11)$$

and

$$G_{choo} = \frac{\mu}{L^2} Q_{oo} \qquad (2.3.12)$$

where G_{choo} is the conductance of the total bar of dimensions L, B, and H.

In practice , G_{choo} cannot be measured externally , so it is useful to define

$$Q_o = Q_{oo} - Q_{eqm} \qquad (2.3.13)$$

and

$$G_{cho} = \frac{\mu}{L^2} Q_o \qquad (2.3.14)$$

where Q_o is the zero bias majority carrier channel charge and G_{cho} is the zero bias channel conductance.

Equation 2.3.11 can therefore be rewritten in the form

$$G_{ch} = \frac{\mu}{L^2} (Q_o - Q_g) = G_{cho} - \frac{\mu Q_g}{L^2} \qquad (2.3.15)$$

Equation 2.3.15 indicates that a plot of gate charge Q_g versus channel conductance at zero drain voltage should give a straight line relationship with L^2/μ as its slope as shown in Fig. 2.3.3.

A drain voltage V_d with respect to the source will now be applied to the structure in Fig. 2.3.1 In general, this drain voltage can be considered to produce three main effects. (1) It causes current to flow from source to drain which is composed essentially of majority carriers; (2) it produces an additional amount of reverse bias across the gate junction, and therefore an additional component of depletion

layer charge on both sides of the gate junction ($\equiv Q_{gd}$) ; and (3) it modifies both the distribution or shape of the depletion layer charge, and the field in the channel. The extent of both these effects is most certainly dependent on position along the channel from source to drain. The net result is that the channel conductance can be partly determined by the shape of the channel as well as by the amount of mobile charge in the channel.

For present purposes, the effects of the channel shape distortion referred to in point (3) above will be assumed to be small. In Section 2.5 the validity of this assumption is considered further, and its validity in practical devices will be considered in Chapter 3. Also, in Section 2.7 this assumption is compared with Shockley's "gradual case" assumption.

Accordingly, then, with both gate voltage and drain voltage present with respect to the source, G_{ch} is assumed to be given by

$$G_{ch} = \frac{\mu}{L^2}(Q_o - Q_{gg} - Q_{gd}) \qquad (2.3.16)$$

where now

$$Q_g \equiv Q_{gg} + Q_{gd} \qquad (2.3.17)$$

and where Q_{gg} is the component of depletion layer charge due to V_g at constant drain-source voltage,

Q_{gd} is the component of depletion layer charge due to V_d at constant gate-source voltage.

Q_g thus still represents the total amount of uncovered charge in the depletion layer in excess of Q_{eqm}. Equation 2.3.16 is therefore similar to equation 2.3.15 , and states that the channel conductance is determined

only by the amount of the mobile charge remaining in the active channel with both gate and drain voltages applied to the device. Equation 2.3.16 reduces to equation 2.3.15 of course , when the applied drain-source voltage is reduced to zero. Equation 2.3.16 neglects any channel shape effects, these being considered later as previously indicated.

Drain current I_d is then

$$I_d = G_{ch} V_d$$

or

$$I_d = \frac{\mu V_d}{L^2} (Q_o - Q_{gd} - Q_{gg}) \qquad (2.3.18)$$

where V_d is the drain-source voltage. The ratio $L^2/\mu V_d$ has units of time and is called the channel time constant τ_d. Therefore in general

$$I_d = \frac{Q_{ch}}{\tau_d} = \frac{(Q_o - Q_{gd} - Q_{gg})}{\tau_d} \qquad (2.3.19)$$

or if desired

$$I_d = I_o - \frac{Q_{gg}}{\tau_d} \qquad (2.3.20)$$

where I_o is the drain current for zero gate voltage which flows with a given V_d applied to the drain.

Thus if gate charge Q_g is plotted against drain current for various values of V_d , a family of straight lines results each of which has a slope determined by $L^2/\mu V_d$ as shown in Fig. 2.3.4. Note that these equations apply within the assumptions made, but only to the open channel, and therefore hold only up to the point where the applied drain voltage V_d is equal to the voltage across the channel length

L. At some value of V_d ($=V_{po}$), the effective channel height at the drain end of the channel is reduced essentially to zero and the channel is said to be pinched off at that point. It can only be assumed for the present that the voltage drop along the channel remains at V_{po} for further increases in V_d. This aspect will be considered further in Chapter 3.

The significance of the channel time constant τ_d should be commented upon. It is identically the time taken by a charged particle or a group of charged particles with mobility μ , to travel a distance L in field V_d/L. The L^2/μ ratio is therefore a fundamental and very important device parameter which directly affects the time required by a device to return to steady state conditions after the application of a transient. This ratio will be used extensively in the chapters that follow.

The structure in Fig. 2.3.1 used in conjunction with the derivation of the basic charge control relationships was a single gate structure. The effects on these relationships of a double gate structure will now be considered. Such a structure is shown in Fig. 2.3.5.

For the purposes of this analysis symmetry will not be assumed, and each junction will be associated with a different doping profile. The structure is again of length L. The channel is divided into two sections one of which has a doping profile $\rho_1(y,z)$ while the other is given by $\rho_2(w,z)$. For emphasis, the dividing line will be taken as $y=0$, $w=0$ with the positive y direction upwards toward gate 1, and the positive w direction downwards toward gate 2. V_d is taken to be zero corresponding to the situation for the development of equation 2.3.7.

For section 1 of the channel, then

$$dQ_1 = L\,\rho_1(y,z)\ dy\ dz \qquad (2.3.21)$$

and

$$dG_1 = \frac{\mu_1 \rho_1(y,z)\ dy\ dz}{L} \qquad (2.3.22)$$

Similarly for section 2,

$$dQ_2 = L\,\rho_2(w,z)\ dw\ dz \qquad (2.3.23)$$

and

$$dG_2 = \frac{\mu_2\,\rho_2(w,z)\ dw\ dz}{L} \qquad (2.3.24)$$

Use will be made of the relationships in equation 2.3.21 through 2.3.24 in their present differential form, rather than the integral of equation 2.3.6 . It is not necessary to use the differential form here, but it is used in preparation for the work in Section 2.3.2 , where it will be found convenient. Thus,

$$dQ = dQ_1 + dQ_2 \qquad (2.3.25)$$

and

$$dG = dG_1 + dG_2 \qquad (2.3.26)$$

Therefore, by substitution,

$$\frac{dQ}{dG} = L^2 \frac{\rho_1(y,z)\ dy\ dz + \rho_2(w,z)\ dw\ dz}{\mu_1(y,z)\ \rho_1(y,z)\ dy\ dz + \mu_2(w,z)\ \rho_2(w,z)\ dw\ dz} \qquad (2.3.27)$$

It can thus be seen from equation 2.3.27 that so long as the majority carrier mobility can be assumed constant throughout the active channel, i.e. that part of the channel contributing to conduction, then

for the complete structure

$$Q_{chT} = \frac{L^2}{\mu} G_{ch} \qquad (2.3.28)$$

just as for equation 2.3.7.

The effects of mobility variations will be considered in the next section.

2.3.2 Mobility Effects

One way of obtaining a larger value of transconductance in a field effect transistor is to decrease the height of the channel while at the same time increasing the channel doping density to maintain the same value of zero bias channel conductance (51). It is therefore quite possible that at some point in the channel, the doping density will be large enough to reduce the mobility of the carriers below the value for low doping. In order to understand what to expect in such a case, it is helpful to consider further the effects of mobility variation on the charge control relationships.

Before proceeding, it should be noted that variations in mobility can also occur from two other main sources : temperature variations , and as a result of the field at some point in the channel exceeding the "critical" value. If the field exceeds a "critical value, Ohm's law begins to fail, and the carrier mobility decreases with increasing electric field. Dacey and Ross (10) considered this situation in terms of Shockley's "gradual case" assumption by assuming that beyond the "critical" field, mobility decreased as the half power of the electric field. Most FET's are as yet low power devices , so internal heating is normally not a serious problem. The L^2/μ ratio can be expected to vary somewhat

however, according to the ambient temperature affecting mobility μ.[52] The work in this section is sufficiently general that mobility variations can be due to any cause, but such considerations are not the main concern here.

Figures 2.3.6 and 2.3.7 are curves showing the relationship between majority carrier mobility and doping density for germanium and silicon respectively. The curves in Fig. 2.3.6 are taken from Prince[53], while the curves in Fig. 2.3.7 are from Conwell[54]. It can be seen from these curves that mobility is essentially constant for values of doping density below about $10^{15}/cm^3$. The mobility gradually decreases but at a faster rate as the doping density increases beyond this point. Thus at a doping density of $10^{17}/cm^3$ or so, the change in mobility could be quite significant.

For this investigation, the two-gate structure of Fig. 2.3.5 will be used. For convenience it will be assumed that the doping density in section 1 of the structure is a function of y alone, and that in section 2, it is a function of w alone. The differential form of the charge-conductance relationship in equation 2.3.27 will be used. Assuming a constant width B in the z-direction, equation 2.3.27 then becomes

$$\frac{dQ}{dG} = L^2 \frac{\rho_1(y)\ dy + \rho_2(w)\ dw}{\mu_1(y)\ \rho_1(y)\ dy + \mu_2(w)\ \rho_2(w)\ dw} \tag{2.3.29}$$

If b is assumed to be the height of the active channel in section 1, and c the height of the active channel in section 2, equation 2.3.29 can be rewritten to give the total channel charge relationship. Thus

$$\frac{dQ_{chT}}{dG_{chT}} = L^2 \frac{\rho_1(b)\,db + \rho_2(c)\,dc}{\mu_1(b)\,\rho_1(b)\,db + \mu_2(c)\,\rho_2(c)\,dc} \qquad (2.3.30)$$

Firstly, if only one section of the structure is present, or if only one gate is operated (gate 1 for example), equation 2.3.30 reduces to

$$\frac{dQ_{chT}}{dG_{chT}} = L^2 \frac{\rho_1(b)\,db}{\mu_1(b)\,\rho_1(b)\,db} = \frac{L^2}{\mu_1(b)} \qquad (2.3.31)$$

The slope of the charge conductance plot thus depends on the mobility at the edge of the channel depletion layer. The mobility in turn depends on the value of the doping density at that point. Equation 2.3.31 is therefore a potentially useful result for diagnostic purposes, particularly for high channel doping levels when the change in mobility with doping density is larger.

The general case in which two gates are operated simultaneously is, of course, more complicated. If symmetry exists, however, with two identical gate junctions, $\rho_1(y) = \rho_2(w)$, and $\mu_1(y) = \mu_2(w)$. Then, if $db = dc$ and $b = c$, we have as before

$$\frac{dQ_{chT}}{dG_{chT}} = \frac{L^2}{\mu_1(b)} = \frac{L^2}{\mu_2(c)} \qquad (2.3.32)$$

In the general two-gate junction case, symmetry does not exist. It will be found helpful to consider this situation in terms of practical junction profiles.

2.3.2.1 Double Abrupt Gate Junctions

Firstly, the case with two abrupt junctions with constant doping densities will be considered. The channel profile for this type of structure is illustrated in Fig. 2.3.8. Gate junction 1 is assumed to be at $y=H_1$ and gate junction 2 is at $w=H_2$. The depletion layer widths in the channel are then given by $H_1 - b$ and $H_2 - c$ for sections 1 and 2 respectively.

From basic diode junction theory, assuming complete depletion, the depletion layer width in the channel is given by [49]

$$H_1 - b = \left[\frac{2K}{q\,N_{ch_1}} \left(\frac{N_{g_1}}{N_{ch_1} + N_{g_1}} \right) \left(\psi_{o_1} + V_1 \right) \right]^{1/2} \tag{2.3.33}$$

where
K = dielectric constant
q = electronic charge
N_{ch_1} = doping density in section 1 of channel
N_{g_1} = doping density on gate side of junction 1
ψ_{o_1} = equilibrium barrier potential of junction 1
V_1 = applied voltage, junction 1

Squaring both sides and differentiating with respect to V, gives

$$(H_1 - b)\,db = \frac{-K\,N_{g_1}}{q\,N_{ch_1}\left(N_{ch_1} + N_{g_1}\right)}\,dV_1 \tag{2.3.34}$$

Similarly, for section 2,

$$H_2 - c = \left[\frac{2K}{q\,N_{ch_2}} \left(\frac{N_{g_2}}{N_{ch_2} + N_{g_2}} \right) \left(\psi_{o_2} + V_2 \right) \right]^{1/2} \tag{2.3.35}$$

and
$$(H_2 - c)\, dc = \frac{-K N_{g2}}{q N_{ch2} (N_{ch2} + N_{g2})} dV_2 \qquad (2.3.36)$$

where
N_{g2} = doping density on gate side of junction 2

N_{ch2} = doping density in section 2 of channel

ψ_{o2} = equilibrium barrier potential of junction 2

V_2 = applied voltage, junction 2

Combining equations 2.3.34 and 2.3.36 gives

$$\frac{db}{dc} = N' \frac{(H_2 - c)}{(H_1 - b)} \frac{dV_1}{dV_2} \qquad (2.3.37)$$

where
$$N' = \frac{N_{g1} N_{ch2} (N_{ch2} + N_{g2})}{N_{g2} N_{ch1} (N_{ch1} + N_{g1})}$$

Multiplying equation 2.3.37 by $\frac{N_{ch1}}{N_{ch2}}$ gives

$$\frac{\rho_1(b)\, db}{\rho_2(c)\, dc} = \frac{N_{ch1}}{N_{ch2}} \frac{db}{dc} = N \frac{(H_2 - c)}{(H_1 - b)} \frac{dV_1}{dV_2} \qquad (2.3.38)$$

where
$$N = \frac{N_{g1} (N_{ch1} + N_{g2})}{N_{g2} (N_{ch1} + N_{g1})}$$

Substituting equation 2.3.38 into 2.3.30 then yields

$$\frac{d\, Q_{chT}}{d\, G_{chT}} = \frac{L^2}{\mu_2(c)} \left[\frac{N \left(\frac{H_2 - c}{H_1 - b} \right) \frac{dV_1}{dV_2} + 1}{\frac{\mu_1(b)}{\mu_2(c)} N \left(\frac{H_2 - c}{H_1 - b} \right) \frac{dV_1}{dV_2} + 1} \right] \qquad (2.3.39)$$

Often the two gates of a field-effect transistor are tied together, and to a good approximation it may be assumed that $\psi_{o_1} + V_1 = \psi_{o_2} + V_2$. Then from equations 2.3.33 and 2.3.35,

$$\frac{H_2 - c}{H_1 - b} = \left[\frac{N_{g_2}(N_{ch_1} + N_{g_1})\, N_{ch_1}}{N_{ch_2}(N_{ch_2} + N_{g_2})\, N_{ch_1}}\right]^{1/2} \qquad (2.3.40)$$

and

$$N\left(\frac{H_2 - c}{H_1 - b}\right) = \left[\frac{N_{g_1}\, N_{ch_1}\,(N_{ch_2} + N_{g_2})}{N_{g_2}\, N_{ch_2}\,(N_{ch_1} + N_{g_1})}\right]^{1/2} \qquad (2.3.41)$$

With abrupt junctions, it is often possible to assume that the level of doping density on the gate side of the junction is much greater than that on the channel side. Thus, if $N_{g_2} \gg N_{ch_2}$ and also $N_{g_1} \gg N_{ch_1}$, equation 2.3.41 would become

$$N\left(\frac{H_2 - c}{H_1 - b}\right) = \left[\frac{N_{ch_1}}{N_{ch_2}}\right]^{1/2} \qquad (2.3.42)$$

and equation 2.3.39 becomes

$$\frac{d\,Q_{chT}}{d\,G_{chT}} = \frac{L^2}{\mu_2(c)}\left[\frac{\left(\dfrac{N_{ch_1}}{N_{ch_2}}\right)^{1/2} + 1}{\dfrac{\mu_1(b)}{\mu_2(c)}\left(\dfrac{N_{ch_1}}{N_{ch_2}}\right)^{1/2} + 1}\right] \qquad (2.3.43)$$

It can be seen then from equation 2.3.43 that as N_{ch_1} approaches N_{ch_2},

$$\frac{d\,Q_{chT}}{d\,G_{chT}} \longrightarrow L^2\left[\frac{2}{\mu_1(b) + \mu_2(c)}\right]$$

Also, as $\left(\frac{N_{ch_1}}{N_{ch_2}}\right)^{1/2}$ becomes $\gg 1$

$$\frac{d\,Q_{chT}}{d\,G_{chT}} \longrightarrow \frac{L^2}{\mu_1(b)}$$

where μ_1 (b) is the lower mobility.

It can thus be seen from equations 2.3.39 and 2.3.43 that the slope of the channel-charge-conductance plots for this type of structure can be expected to depend on the mobility at each depletion layer boundary , the doping densities, and if the gates are not tied together, on the channel depletion layer widths, and on the voltage change at each gate.

2.3.2.2 Double Linear Gate Junctions

Consideration will now be given to a structure with two diffused gate junctions, each of which is assumed to have a linear grading. This results in a channel charge density profile as shown in Fig. 2.3.9. The doping profiles are a_1 and a_2 for junctions 1 and 2 respectively.

For this case, it can be assumed that (49)

$$H_1 - b = \left[\frac{3/2K}{qa_1}(\psi_{O_1} + V_1)\right]^{1/3} \qquad (2.3.44)$$

and

$$H_2 - c = \left[\frac{3/2K(\psi_{O_2} + V_2)}{qa_2}\right]^{1/3} \qquad (2.3.45)$$

where

K = dielectric constant

q = electronic charge

ψ_{O_1} = junction 1 equilibrium barrier potential

ψ_{o_2} = junction 2 equilibrium barrier potential

a_1, a_2 = linear junction grading slopes

$(H_1 - b)$ = section 1 depletion layer width

$(H_2 - c)$ = section 2 depletion layer width

V_1, V_2 = applied reverse bias junction voltages

In the same manner as for the abrupt junction case previously considered, by differentiation from equations 2.3.44 and 2.3.45 one can obtain

$$\frac{db}{dc} = \frac{a_2}{a_1} \frac{(H_2 - c)^2}{(H_1 - b)^2} \frac{dV_1}{dV_2} \tag{2.3.46}$$

Now $\rho_1(b) = qa_1 (H_1 - b)$ and $\rho_2(c) = qa_2(H_2 - c)$. Therefore

$$\frac{\rho_1(b)\ db}{\rho_2(c)\ dc} = \left(\frac{H_2 - c}{H_1 - b}\right) \frac{dV_1}{dV_2} \tag{2.3.47}$$

giving from equation 2.3.30

$$\frac{dQ_{chT}}{dG_{chT}} = L^2 \left[\frac{\left(\frac{H_2 - c}{H_1 - b}\right) \frac{dV_1}{dV_2} + 1}{\mu_1(b) \left(\frac{H_2 - c}{H_1 - b}\right) \frac{dV_1}{dV_2} + \mu_2(c)} \right] \tag{2.3.48}$$

As before, if it can be assumed that $\psi_{o_1} + V_1 \approx \psi_{o_2} + V_2$, then from equations 2.3.44 and 2.3.45 (with gates tied together),

$$\frac{dQ_{chT}}{dG_{chT}} = L^2 \left[\frac{\left[\frac{a_1}{a_2}\right]^{1/3} + 1}{\mu_1(b) \left(\frac{a_1}{a_2}\right)^{1/3} + \mu_2(c)} \right] \tag{2.3.49}$$

This situation is thus similar to equations 2.3.39 and 2.3.43 for the double abrupt junction case.

Other junction combinations, such as one abrupt and one graded junction, are possible in the two-gate structure and these could be solved for. However, the treatment of the double abrupt and double linearly graded junction cases provides a good basis for understanding mobility effects throughout the channel. If the parameters of the structure are known, as equations 2.3.39 and 2.3.48 show, it is always possible to calculate the slope of the charge conductance relationship throughout the whole of the channel. Equally important however, as will be shown in Chapter 3, the reverse is true. The charge conductance relationship can always be used to obtain information about the parameters of an unknown device.

2.4 MOST Charge Control Relationships

Although the main emphasis in this thesis is on junction field-effect transistors, the applicability of the charge control relationships to insulated gate field-effect transistors will also be studied. The insulated-gate field-effect transistor structure to be considered here is shown in Fig. 2.4.1. This type of structure was first suggested by Kahng and Atalla [24-26], and has also been called a surface-field-effect transistor, and a metal-oxide-semiconductor transistor. The term MOST, an abbreviation from the last name mentioned above, is used to refer to this structure.

The MOST is a particularly interesting type of field-effect transistor to consider from the charge control point of view. Because

of its very high gate resistance and consequent low gate leakage current, a quantity of charge placed on the open circuited gate of an MOST will remain there for a very considerable length of time before disappearing. The time required for this charge to be leaked away can be in the order of several hours to a day in some devices [55].

The MOST would thus appear to closely approach an ideal charge controlled device which could be defined as one which (a) requires only the presence of charge on its controlling electrode to achieve control in the output circuit, and (b) does not require a sustaining current or voltage to maintain the controlling charge. In practical MOST's, these requirements will only be exactly achieved over a more limited period of time during which the amount of charge leaked away is negligibly small.

In applications involving logic, for example, the main interest is to determine which state the device is in. The tolerance to gate charge variations due to leakage is relatively high, permitting an operating period of the order of the gate discharge time constant. In the logic application, a non-destructive read-out of the state of the device is available from a measure of the channel conductance. This example thus serves to illustrate one possible advantageous use of the near ideal charge control properties of the MOST.

The structure in Fig. 2.4.1 represents an N-channel device and consists of a P-type substrate into which are diffused heavily doped N regions forming the source and drain contacts. Silicon dioxide is grown over the region between the source and drain contacts and on this is deposited metal which forms the gate contact. The

silicon dioxide is a very high resistance region and effectively isolates the gate contact from the remainder of the device.

In normal operation, a thin region of mobile electrons exists in the area between source and drain forming a resistive path from source to drain. The application of a positive voltage to the drain with respect to the source results in a flow of electrons from source to drain. The number of mobile channel carriers and thus the amount of current flow, can be increased or decreased by increasing or decreasing the amount of positive bias on the gate with respect to the source. The substrate is usually connected to the source.

MOST's can be fabricated as enhancement-type devices or depletion-type devices [37]. A depletion-type MOST is designed to have a large number of conduction electrons present in the channel before the application of terminal voltages. This type of device closely resembles the junction FET and is operated with a positive drain voltage and negative gate voltage with respect to source. The application of a negative gate voltage removes or depletes mobile carriers from the channel and if large enough, will cause pinch-off at some point in the channel.

For the MOST the pinch-off voltage is assumed to be the voltage drop across the oxide layer which will just cause the mobile charge concentration in the channel to go to zero.

The enhancement-type device is usually designed with no mobile carriers in the channel initially. In fact, the surface channel region often has an effective heavy P-doping. In this case, a considerable positive gate voltage is required to overcome the effects of the surface P-doping, and to produce mobile electrons in the channel for conduction.

Pinch-off voltages for enhancement devices therefore can be zero or positive while depletion devices have negative pinch-off voltages.

Similar analyses for the voltage-current relationships for an ideal enhancement-type MOST structure have been carried out by Ihantola[36], Hofstein and Heiman [37], and more recently by Sah [38]. Shockley's method of solution [8] is applied in all cases. It is usually assumed that

(1) The average mobility μ is constant in the channel.

(2) The gate oxide layer is much thicker than the channel depth.

This allows the channel to be considered as a surface sheet with essentially all the gate control voltage appearing across the oxide. It also means that the gate capacitance is assumed to be constant and independent of variations in the channel height.

(3) Shockley's "gradual case" applies to the channel.

(4) The effects of surface states or traps are constant.

These analyses result in an equation for the voltage characteristics of an enhancement-type MOST in common source operation of the form [37]

$$I_d = \frac{K_{ox} \mu B}{L T_{ox}} \left[(V_g - V_{po}) V_d - \frac{V_d^2}{2} \right] \quad (2.4.1)$$

where I_d = drain current

V_d = drain voltage

V_g = gate voltage

K_{ox} = oxide dielectric constant

μ = channel mobility

B = width of channel

L = Length of channel

T_{ox} = thickness of gate oxide layer

V_{po} = pinch -off voltage

The Shockley condition, and thus equation 2.4.1, does not hold for voltages beyond pinch-off such that

$$V_d > V_g - V_{po} \qquad (2.4.2)$$

Equation 2.4.1 results in a family of curves as shown in Fig. 2.4.2. The drain current is assumed constant beyond pinch-off as in the corresponding curves for the FET.

These analyses will not be repeated here, the main purpose in this section being to consider both enhancement-type and depletion type MOST's in terms of the charge control relationships previously presented for junction FET's.

From the previous discussion, the MOST channel is analogous to its FET counterpart in that conduction in both devices is by majority carriers. Further, the channel conductance depends on the number of channel carriers in both cases. It is thus clear that under conditions of zero drain voltage and constant mobility, equation 2.3.7 is applicable to the MOST channel as well as the FET channel. Thus for the MOST, with reference to Fig. 2.4.1 ,

$$Q_{ch} = \frac{L^2}{\mu} G_{ch} \qquad (2.4.3)$$

where L = channel length

μ = channel mobility, assumed constant

As in the FET case, it will be assumed that the application of a drain voltage to the unpinched-off channel, although it may modify the amount of charge therein, does not distort the channel shape sufficiently to invalidate the basic equation 2.4.3. Therefore

$$I_d = G_{ch} V_d = \frac{\mu V_d}{L^2} Q_{ch}$$

$$= \frac{Q_{ch}}{\tau_d} \qquad (2.4.4)$$

where $\tau_d = L^2 / \mu V_d$ as before.

As with the FET, Gauss's Theorem (48) requires that the charge on the gate be balanced by an equal amount of charge of opposite polarity below the insulating oxide layer. In the N-channel device, the gate charge can be balanced by Q_{ch} consisting of majority carrier electrons in the surface channel, and by Q_s consisting of depletion region charge of uncovered acceptor impurities in the substrate, assuming negligible intrinsic hole and electron concentrations. Note that if the field at the substrate surface is sufficiently large, this depletion layer can extend a considerable distance down into the substrate bulk.

A further component of charge Q_{st} must also be considered. This is the charge in the surface traps as a result of incomplete bonds at the silicon-silicon dioxide interface. Q_{st} depends somewhat on manufacturing processes, but generally surface traps in N-channel devices with P-type substrates are donor-type and therefore contain positive charge. The doping level of the substrate is then usually adjusted to produce the desired number of conduction electrons in the surface channel. (56)

The more lightly doped substrate produces a relatively larger number of conduction electrons at zero applied gate voltage. A heavily doped substrate could result in no conduction electrons, just holes and ionized acceptors in the surface channel region. The lightly doped substrates thus produce depletion-type MOST's while the more heavily doped substrates produce enhancement-type MOST's.

The relationship between these charge components, as illustrated in Fig. 2.4.8, is then, from Gauss's Theorem,

$$Q_g + Q_{st} + Q_{ch} + Q_s = 0$$

or

$$Q_{gg} + Q_{gd} + Q_{st} + Q_{ch} + Q_s = 0$$

Therefore

$$Q_{ch} = -(Q_{gg} + Q_{gd}) - Q_{st} - Q_s \qquad (2.4.5)$$

where

Q_{ch} = conduction charge in the channel (in this case, negative electron charge)

Q_g = net gate charge = $Q_{gg} + Q_{gd}$

Q_{gg} = component of gate charge due to applied gate bias. In this N-channel case, Q_{gg} is positive for positive V_g indicating electrons removed from gate contact. In depletion mode operation, V_g is negative, indicating that for this device electrons are added to the gate contact.

Q_{gd} = component of gate charge due to drain voltage. In this N-channel device, Q_{gd} is negative. It can thus be seen that in the enhancement mode of operation, Q_{gd} is in opposition to Q_{gg}.

Q_{st} = charge in surface traps (usually positive in an N-channel device)

Q_s = uncovered substrate charge (negative for P-type substrate)

Combining equation 2.4.5 with 2.4.4 gives

$$I_d = \frac{Q_{ch}}{T_d} = \frac{-(Q_{gg} + Q_{gd}) - Q_{st} - Q_s}{T_d} \qquad (2.4.6)$$

or

$$= \frac{-(Q_{gg} + Q_d\ ) + Q_o}{T_d} \qquad (2.4.7)$$

where
$$Q_o \equiv -Q_{st} - Q_s \qquad (2.4.8)$$

Q_o is negative for a device with an initial inversion layer at zero applied voltage . It is equal to the charge which must be added to or subtracted from the channel (by Q_{gg}) to just produce pinch-off all along the channel with zero drain voltage applied.

It will be assumed initially in connection with equation 2.4.7 that the charge in the surface states is fixed. Also , it will be assumed that Q_s is independent of gate voltage. This effectively assumes a sufficiently low applied gate field, and/ or a sufficiently thick gate oxide layer. The range of validity of these assumptions for practical MOST's will be clearly shown in Chapter 3. The resulting family of constant drain voltage (constant Q_{gd}) characteristics predicted by equation 2.4.7 is shown in Fig. 2.4.4 . Note that if Q_o is negative, equation 2.4.7 should not be interpreted to mean that current will flow in the opposite direction at Q_{gg} = 0, but rather that con-

duction electrons must be present in the channel before current can flow.

Equations 2.4.3 and 2.4.7 describe MOST operation under conditions of constant mobility. By analogy, it is seen that these equations can be affected by mobility variations just as in the single gate FET case. Nevertheless, as will be shown in Chapter 3, these relationships are of considerable use in the study of practical MOST's.

2.5 Charge Control and the Wedge-Shaped Channel

In order to illustrate the effects of channel shape on the charge control relationships, and to study further the assumption in Section 2.3.1 neglecting channel shape effects, the charge-conductance relationship for a channel in the shape of a wedge will now be considered. This shape of channel cannot of course be assumed to apply exactly to all FET's under all biasing conditions, but it will help to provide a good understanding of the factors involved.

The wedge-shaped channel to be analyzed is shown in Fig. 2.5.1. The height of the structure at the base in the y direction is H, tapering to zero at x=P. The width of the structure in the z direction is assumed to be constant and equal to B. The distance from x=0 to x=L is assumed to be the active channel length while the point P is merely a reference point at the peak of the triangle. Symmetry will be assumed about the y=0 plane.

Equation 2.3.2 will be used in the form

$$dR = \frac{dx}{\rho \mu A(x)} \qquad (2.5.1)$$

where dR is the differential resistance of a differential section of channel length dx and area A(x),

ρ is the charge density in the channel and will be assumed constant here,

μ is the majority carrier mobility, also assumed constant.

Equation 2.5.1 is applicable as long as the current flow is essentially in the x-direction. It will thus be valid for small wedge angles such that the length of the chord at x=0 drawn from the point P is not significantly different from the height H. At any point x along the channel, the height is given by

$$y = \frac{H}{2}\left(1 - \frac{x}{P}\right) \tag{2.5.2}$$

and

$$A(x) = 2By(x) = BH\left(1 - \frac{x}{P}\right) \tag{2.5.3}$$

Substituting equation 2.5.3 into 2.5.1 and integrating from x=0 to x=L gives

$$R_{ch} = \frac{P}{\rho \mu BH} \log_e \left(\frac{1}{1 - \frac{x}{P}}\right)\Bigg|_{x=0}^{L} \tag{2.5.4}$$

or

$$R_{ch} = \frac{L}{\rho \mu BH}\left[\frac{P}{L} \log_e \left(\frac{P}{P - L}\right)\right] \tag{2.5.5}$$

The charge Q_{ch} in the channel is obtained by

$$Q_{ch} = \rho \, Vol_{ch} \tag{2.5.6}$$

The channel volume is calculated as follows:

$$Vol = 2B \int_{x=0}^{x=L} y(x)\, dx \qquad (2.5.7)$$

Substituting equation 2.5.2 into equation 2.5.7 and integrating gives

$$Vol_{ch} = BLH \left[1 - \frac{L}{2P} \right] \qquad (2.5.8)$$

Therefore, from equation 2.5.6 ,

$$Q_{ch} = \rho BLH \left[1 - \frac{L}{2P} \right] \qquad (2.5.9)$$

From 2.5.5 and 2.5.9 then,

$$\frac{Q_{ch}}{G_{ch}} = \frac{L^2}{\mu} F \qquad (2.5.10)$$

where

$$F = \left(\frac{P}{L} - \frac{1}{2} \right) \log_e \left(\frac{\frac{P}{L}}{\frac{P}{L} - 1} \right) \qquad (2.5.11)$$

It can be seen from Fig. 2.5.1 that

$$\frac{H}{H_L} = \frac{P}{P - L} = \frac{\frac{P}{L}}{\frac{P}{L} - 1} \qquad (2.5.12)$$

where H_L is the channel height at $x=L$, so that F can also be written as

$$F = \frac{\left(\frac{H}{H_L} + 1 \right)}{2\left(\frac{H}{H_L} - 1 \right)} \log_e \left(\frac{H}{H_L} \right) \qquad (2.5.13)$$

Thus as P/L goes from 1 to a large value, H/H_L goes from a large value to 1.

Fig. 2.5.2 shows a plot of F as a function of P/L. It can be seen that for values of P/L greater than about 2, the value of F is not significantly different from 1. As P/L approaches 1, F rises very rapidly to infinity. Conditions of validity of equation 2.5.1 break down at that point however, as the channel is no longer open. It also represents a physically impossible situation in the practical device, as it would require a field of infinite size to sustain current flow through a channel which gradually tapers to zero.

Current does flow in the physical device with the drain end of the channel "pinched-off". It therefore appears probable that the pinch-off condition is represented by an <u>effective limiting</u> of the P/L ratio to some value greater than 1.

In practical devices, the effective P/L ratio can be made large (H/H_L ratio approaching 1) in two main ways. The first is by constructing the device with a smaller physical channel height. The second is by increasing the channel depletion layer width at the source end of the channel relative to that at the drain end by the application of appropriate gate and drain voltages.

In view of this second point, and also of the fact that the results in Fig. 2.5.2 indicate that a fairly severe distortion of channel shape can occur without seriously changing the effective device L^2/μ ratio, true charge control operation should be achieved with all practical FET's over a good range of gate bias conditions, even if the drain voltage is large. Similar conclusions can also be seen to apply to the MOST.

2.6 FET's and MOST's Modelled Below Pinch-off

It is intended in this section to develop models describing FET and MOST operation from the charge control point of view. The charge control models presented in this section are intended to apply for FET and MOST operation with open or unpinched -off channels. The subject of modelling the complete range of device operation is discussed in Chapter 3.

The purposes in developing these models are mainly two-fold. It is intended firstly that the model should provide a simple yet general representation to aid in the description and understanding of device operation. Secondly, it is desired to provide the basis for an equivalent circuit representation of these devices to facilitate the calculation and prediction of their performance, with particular emphasis on low level switching transient performance.

Since the FET and MOST are essentially alike, the criteria for the models will be developed with reference to the FET.

2.6.1 Development of FET Model

As previously mentioned, the term "low level switching" is taken from "chopper" terminology and indicates that the FET (or MOST) will switch a relatively low signal voltage on the drain. Typically, the signal to be "chopped" is below 100 millivolts or so. The gate voltage or switching voltage must be large enough to produce a considerable variation in the source-drain resistance during its application. The model must therefore accomodate values of gate voltage up to the pinch-off voltage. A somewhat more general model allowing larger drain voltages, will in fact be presented, so the main requirements mentioned

above will be accommodated. The main restriction in this section is that the channel should remain unpinched-off.

In order to calculate the time response of the FET in the general case, the distributed nature of the gate junction and the channel will undoubtedly have to be incorporated into the model. The reason for this is that it is quite conceivable that differential charging of the gate depletion layer can occur. In other words, the rate of charging of the depletion layer throughout the transient may be different at various points along the channel depending not only on the channel resistance, load terminations, etc., but on the distribution of resistance along the channel at any given time. This is illustrated in Fig. 2.6.1.

If differential charging does occur in the depletion layer during the switching transient, it is of course consistent with saying that the resistance at various points along the channel must also vary accordingly. It is also consistent with saying that the shape of the channel may vary at different points along the length of the channel at different times throughout the transient.

A more detailed consideration of all the factors affecting the switching process, and its representation, is presented in Chapter 5, Section 5.2. Nevertheless, it is clear from the preceding discussion and from the work in the earlier parts of this chapter that both differential charging effects and large drain voltages could in general distort the channel shape severely enough to cause significant deviations in the L^2/μ ratio. The approach used in this work is to divide the depletion layer and channel into a number of sections or lumps from source

to drain. It can readily be seen that, if the number of lumps is large enough, the distributed nature of the depletion layer and channel, from source to drain, should be adequately represented.

It will be shown in Section 2.6.2 specifically how this approach allows the problem of severe channel shape distortion, due either to differential charging or to large drain voltages, to be effectively overcome. The relationship will first be presented, however, assuming negligible channel shape distortion. Majority carrier mobility will be assumed constant in the derivation of the models in this section.

The lumping technique is illustrated in Fig. 2.6.2. Each lump is assumed to consist of a charge storage element and a variable resistance element. The charge storage element represents the charge in its section of gate depletion layer, and the resistive element represents the resistance of its section of the channel. Ideally there should be an infinite number of lumps representing the device, but in practice, it will be shown that seldom are more than four or five lumps required to represent the device adequately.

Other lumping configurations will be studied in Chapters 4 and 5, but the "L" section of Fig. 2.6.2 was chosen in the interests of simplicity and convenience. A typical 3-lump gate-channel charge-conductance representation is shown in Fig. 2.6.3.

The channel resistance of a given lump will be calculated by applying the previously derived charge control relationships to that lump. In other words, it is assumed that each lump essentially acts like a small field-effect transistor to which equation 2.3.16 is applicable. For a given section "u" then

$$G_{ch} = \frac{\mu}{L_u^2} (Q_{ou} - Q_{gu}) \qquad (2.6.1)$$

and

$$G_{ch} = G_u \left(1 - \frac{Q_{gu}}{Q_{ou}}\right) \qquad (2.6.2)$$

where G_{ch} = conductance of section u of the channel

L_u = length of section u of the channel

Q_{ou} = total majority carrier charge in section u of the channel = amount of gate charge required to pinch-off section u of the channel

Q_{gu} = amount of depletion layer or gate charge in section u, including both gate and channel voltage effects

$G_u = \frac{\mu Q_{ou}}{L_u^2}$ = zero bias conductance of section u of the channel

If the channel is divided into n sections of equal length, then

$$L_u = L/n \qquad (2.6.3a)$$

$$Q_{ou} = Q_o/n \qquad (2.6.3b)$$

$$G_u = nG_{cho} \qquad (2.6.3c)$$

where L, Q_o , and G_{cho} represent corresponding values for the complete device as previously defined. The total channel resistance is then given by

$$R_{ch} = \frac{1}{G_{chA}} + \frac{1}{G_{chB}} + \frac{1}{G_{chC}} + \text{---} \qquad (2.6.4)$$

Therefore by substitution

$$R_{ch} = \frac{R_o}{n}\left[\frac{1}{1-\frac{Q_{gA}}{Q_{ou}}} + \frac{1}{1-\frac{Q_{gB}}{Q_{ou}}} + \frac{1}{1-\frac{Q_{gC}}{Q_{ou}}} + ---\right] \qquad (2.6.5)$$

where $R_o = 1/G_{cho}$ = zero bias total channel resistance. Note that the total device depletion layer charge due to both gate and drain voltages is

$$Q_g = Q_{gA} + Q_{gB} + Q_{gC} + --- \qquad (2.6.6)$$

In the simple case where $Q_{gA} = Q_{gB} = Q_{gC}$ etc., equation 2.6.5 simply becomes

$$R_{ch} = \frac{R_o}{n}\left[n\left(\frac{1}{1-\frac{n\,Q_{gA}}{Q_o}}\right)\right] = \frac{R_o}{\left(1-\frac{Q_g}{Q_o}\right)} \qquad (2.6.7)$$

since $Q_g = nQ_{gA} = nQ_{gB}$ etc. Equation 2.6.7 is then identical with equation 2.3.16.

2.6.2 Lumping and the Wedge-Shaped Channel

Consideration will now be given to the way in which lumping overcomes the problem of a severely distorted channel shape and the resultant deviation in the simple charge control relationships. This will be done with reference to Fig. 2.6.4 by considering the effects of lumping on the wedge-shaped channel as used in Section 2.5.

Fig. 2.6.4 shows a linearly tapered uniformly doped channel of length L and divided into four equal sections L_1, L_2, L_3, and L_4. P is the distance to the peak of the triangle and for convenience P is equal to $\frac{5L}{4}$. It will be recalled that in Section 2.5 the true relationship for

such a channel was given by equation 2.5.10 ,

$$\frac{Q_{ch}}{G_{ch}} = \frac{L^2}{\mu} F = \frac{L^2}{\mu}\left[\left(\frac{P}{L} - \frac{1}{2}\right) \log_e \left(\frac{\frac{P}{L}}{\frac{P}{L} - 1}\right)\right] \quad (2.6.8)$$

and also, that the simple charge control relationships only apply well when $F \approx 1$ corresponding to a large P/L ratio.

Table 2.6.1 compares the P/L ratio for the whole device, and for each section of the structure of Fig. 2.6.4. This table clearly shows that the P/L ratio is larger (i.e. better) for each section than for the device treated as a whole. Improvement in P/L ratio is shown to be greatest in the sections near the open end of the channel.

Table 2.6.2 shows the improved results obtained when the number of channel lumps is doubled to eight. A further improvement in the P/L ratio for each section has resulted while the P/L ratio for the whole device has remained as before.

Although the channel shape in practice will not always vary linearly, the principle remains unchanged, and it can be assumed that the simple charge control representation of each lump will be better than that for the device if treated as a whole. A better overall representation of the total channel resistance then results. Note that even if the P/L ratio in one section is poor (i.e. low) , its effect on the total channel resistance is effectively reduced according to the number of lumps used.

The complete charge control FET model for the unpinched-off channel is shown in Fig. 2.6.5, with the total channel resistance being given by equation 2.6.5. R_{ps} and R_{pd} are bulk parasitic source

Table 2.6.1

4-Lump Wedge-Shaped Channel P/L Ratios (See Fig. 2.6.4)

(Channel Length = 4P/5 ; Section Length = P/5)

Channel Section	Section Peak Distance	P/L Ratio
Whole Channel	P	5/4 = 1.25
Section 1	$P_1 = P$	5
Section 2	$P_2 = 4/5\ P$	4
Section 3	$P_3 = 3/5\ P$	3
Section 4	$P_4 = 2/5\ P$	2

Table 2.6.2

8-Lump Wedge-Shaped Channel P/L Ratios (See Fig. 2.6.4)

(Channel Length = 8P/10 ; Section Length = P/10)

Channel Section	Section Peak Distance	P/L Ratio
Whole Channel	P	10/8= 1.25
Section 1	$P_1 = P$	10
Section 2	$P_2 =9/10\ P$	9
Section 3	$P_3 =8/10\ P$	8
Section 4	$P_4 =7/10\ P$	7
Section 5	$P_5 =6/10\ P$	6
Section 6	$P_6 =5/10\ P$	5
Section 7	$P_7 =4/10\ P$	4
Section 8	$P_8 =3/10\ P$	3

and drain contact resistances respectively. R_{pg} is the bulk parasitic gate contact resistance. C_{gs} , C_{gd} , and C_{ds} are stray capacitances. The current sources (assumed to be constant), represent the reverse biased junction leakage current. The total leakage current I_1 is given by

$$I_1 = I_A + I_B + I_C + \text{---} \qquad (2.6.9)$$

where $I_A = I_B = I_C$ etc.

The number of lumps required depends on the device and its circumstances of use. In the d-c or steady state situation, only one lump is required to represent an FET under conditions of negligible channel shape distortion. In the large drain voltage transient situation, several lumps may be required. Evaluation of parameters and other model forms, will be considered in the low level switching study in Chapters 4 and 5.

2.6.3 MOST Model

Bearing in mind the operational similarities previously discussed, it can be concluded that the basic principles, presented in this section relating to FET's, can also be applied to MOST's . The form of the MOST charge control model for the unpinched-off channel will thus be similar except for the differences now to be discussed.

One difference is that the gate leakage current is not constant, but depends on the amount of charge on the gate. It is so small that it can usually be neglected , but in general will be represented by a leakage resistance from gate to source, and from gate to drain.

Equation 2.4.7 from Section 2.4 applied to a gate-channel lump gives

$$G_{chu} = \frac{\mu}{(L_u)^2} (-Q_{gu} + Q_{ou}) \qquad (2.6.10)$$

and as before

$$R_{ch} = \frac{1}{G_{chA}} + \frac{1}{G_{chB}} + \frac{1}{G_{chC}} + \text{---}$$

Therefore

$$R_{ch} = \frac{1}{L\frac{\mu}{A^2}(-Q_{gA}+Q_{ou})} + \frac{1}{L\frac{\mu}{B^2}(-Q_{gB}+Q_{ou})} + \frac{1}{L\frac{\mu}{C^2}(-Q_{gC}+Q_{ou})} + \text{--} \qquad (2.6.11)$$

Equation 2.6.11 applies to both enhancemant type and depletion type MOST's. Note however, that it applies only to the unpinched-off channel. Therefore $(-Q_{gA} + Q_{ou})$, $(-Q_{gB} + Q_{ou})$ etc., must all be such that there is electron conduction charge in each section of this N-type channel.

One other complicating factor must be considered for the MOST model and that is depletion layer capacitance C_d as illustrated in Fig. 2.6.6. If the substrate is connected to the source as is common, the depletion layer capacitance of the N^+ - P junction at the drain contact effectively shunts the channel from drain to source. This capacitance is drain voltage dependent but may be quite small depending on the junction area. Note that the depletion layer below the device channel partially balances the charge on the metal gate contact (and the surface traps), and is assumed to be accounted for in the model's gate charge storage elements.

Depletion layer capacitance C_s also exists between the N+ source

contact and P-type substrate. R_{sub} is the bulk substrate resistance, and R_{cs} is the resistance of the contact to the substrate. The resulting MOST charge control model for the unpinched-off channel is shown in Fig. 2.6.7 where channel resistance is calculated from equation 2.6.11.

It should be noted that the model is normally unnecessarily complex, particularly if the device is operated with the substrate connected to the source. Usually R_{ps}, R_{pd}, R_{pg} and R_{cs} are negligibly small. This means that for operation with substrate connected to source, essentially no voltage appears across C_s so it can be removed from the equivalent circuit.

As in the case of the FET model, one or more gate-channel lumps are required depending on its use. Evaluation of parameters for this model will also be carried out in Chapter 5.

2.7 Shockley's Approach and Charge Control Compared

The "gradual case" assumption made by Shockley is fundamental to his work and is of great importance. In this section the "gradual case" assumption will be studied in greater detail with the view to providing a better understanding of it, and to compare Shockley's approach with the charge control approach.

To do this, Shockley's assumptions and expressions will be used to calculate the charge $Q_{ch}(V)$ in the channel volume of an FET in terms of the applied drain and gate voltages. The channel time constant τ_d will then be obtained by dividing $Q_{ch}(V)$ by the drain current $I_d(V)$, also in terms of gate and drain voltages (i.e. equation 2.2.14).

The abrupt juncture structure of Fig. 2.2.1 used for the derivation of Shockley's basic equations, will also be used here. The charge in the channel is given by

$$Q_{ch}(V) = \rho_n(\text{channel volume}) = 2\rho_n B \int_{x=0}^{x=L} b(x)\,dx \quad (2.7.1)$$

where

$2b(x)$ = channel height at any point x along the channel

ρ_n = channel charge density, assumed constant as in Chapter 2

B = channel width

From equation 2.2.9 the relationship between "b" and the voltage across the depletion layer is given by

$$b = a\left[1 - \left(\frac{V}{V_{po}}\right)^{1/2}\right] \quad (2.7.2)$$

b(x) will be obtained from equation 2.7.2 by assuming a specific relationship (equation 2.7.3) between V and x . This relationship will be tested (equations 2.7.5 through 2.7.7), as indicated below, before it is used to obtain $Q_{ch}(V)$ from equation 2.7.1. The assumption is as follows:

$$V = \left(-V_g + \frac{V_d\, x}{L}\right) \tag{2.7.3}$$

Thus giving

$$b(x) = a\left[1 - \left(\frac{-V_g + \frac{V_d\, x}{L}}{V_{po}}\right)^{1/2}\right] \tag{2.7.4}$$

Before proceeding to calculate $Q_{ch}(V)$, equation 2.7.4 will be used to calculate I_d to emphasize that equation 2.7.4 is in fact consistent with Shockley's assumptions. Thus from equation 2.2.11

$$I_d \int_{x=0}^{x=L} dx = g_o \int_{x=0}^{x=L} \left[1 - \left(\frac{-V_g + \frac{V_d x}{L}}{V_{po}}\right)^{1/2}\right] \frac{V_d dx}{L} \tag{2.7.5}$$

where $dV = (V_d/L)\, dx$ from equation 2.7.3. Thus

$$I_d L = \frac{V_d g_o}{L}\left[x - \frac{2L\, V_{po}}{3V_d}\left(\frac{V_d\, x}{L\, V_{po}} - \frac{V_g}{V_{po}}\right)^{3/2}\right]\Bigg|_{x=0}^{x=L} \tag{2.7.6}$$

and therefore

$$I_d(V) = \frac{V_d g_o}{L}\left[1 - \frac{2/3}{V_d\left(V_{po}\right)^{1/2}} \left\{\left(V_d - V_g\right)^{3/2} - \left(-V_g\right)^{3/2}\right\}\right] \tag{2.7.7}$$

which is identical with Shockley's current -voltage relationship (i.e., equation 2.2.14, thus verifying equations 2.7.3 and 2.7.4.

Shockley's "gradual case" assumption therefore assumes a constant field and a linear voltage variation along the channel as expressed by equation 2.7.3. This can only really be true, however, if the channel height is constant along its length from source to drain. From equation 2.7.4 it can be seen that this situation can only prevail if the $V_d x/L$ term is negligible with respect to V_g everywhere along the channel from source to drain. It is believed that the derivation of the Shockley current-voltage relationship by the method expressed by equations 2.7.3 through 2.7.7 on the assumption of a linear voltage variation along the channel, not only helps to provide a better understanding of the "gradual case" assumption, but also provides a convenient method for determining over what portion of the channel length the "gradual case" assumption applies.

Continuing with the $Q_{ch}(V)$ calculations, substitution of equation 2.7.4 into equation 2.7.1 gives

$$Q_{ch}(V) = 2\rho B_a \int_{x=0}^{x=L} \left[1 - \left(\frac{-V_g + \frac{V_d x}{L}}{V_{po}} \right)^{1/2} \right] dx \qquad (2.7.8)$$

Therefore

$$Q_{ch}(V) = 2\rho B_a L \left[1 - \frac{2}{3V_d V_{po}^{1/2}} \left\{ (-V_g + V_d)^{3/2} - (-V_g)^{3/2} \right\} \right] \qquad (2.7.9)$$

Dividing equation 2.7.9 by equation 2.7.7 produces

$$\tau_d = \frac{Q_{cd}(V)}{I_d(V)} = \frac{2\rho B_a L^2}{V_d \varepsilon_o} = \frac{2\rho B_a L^2}{V_d 2\mu\rho B_a} = \frac{L^2}{\mu V_d} \qquad (2.7.10)$$

Equation 2.7.10 thus shows that on the basis of Shockley's assumptions, the ratio of channel charge to channel current is always directly proportional to the square of the channel length divided by the product of mobility and applied drain voltage. It is thus identically equal to the channel time constant as defined in equation 2.3.19.

It can therefore be concluded that Shockley's "gradual case" assumption is identical to the true charge control or constant τ_d assumption from the charge control approach.

Charge control thus provides a completely general relationship incorporating Shockley's main assumption of gradual conditions in the channel. It can be used for FET's with any doping profile in the channel, and is also applicable to the study of MOST's. Its use with a particular FET does not require a knowledge of the junction law(s), nor does it depend on the assumption that the doping density on the gate side of the device junction(s) is very much greater than the channel doping density. In addition, its use does not require a detailed knowledge of the exact device structure.

As the measurements in the next chapter will show, the charge control relationships prove to be of considerable value in the study of FET parameters and characteristics. In this regard, by studying deviations in τ_d , or in the L^2/μ ratio, it is possible to determine

under what operating conditions the assumption of true charge control operation, or Shockley's "gradual case" assumption, is valid. In addition, it provides a practical method for studying the effects of mobility variations, structural effects, manufacturing tolerances, and in short, anything which significantly affects either the channel time constant τ_d, or the device L^2/μ ratio.

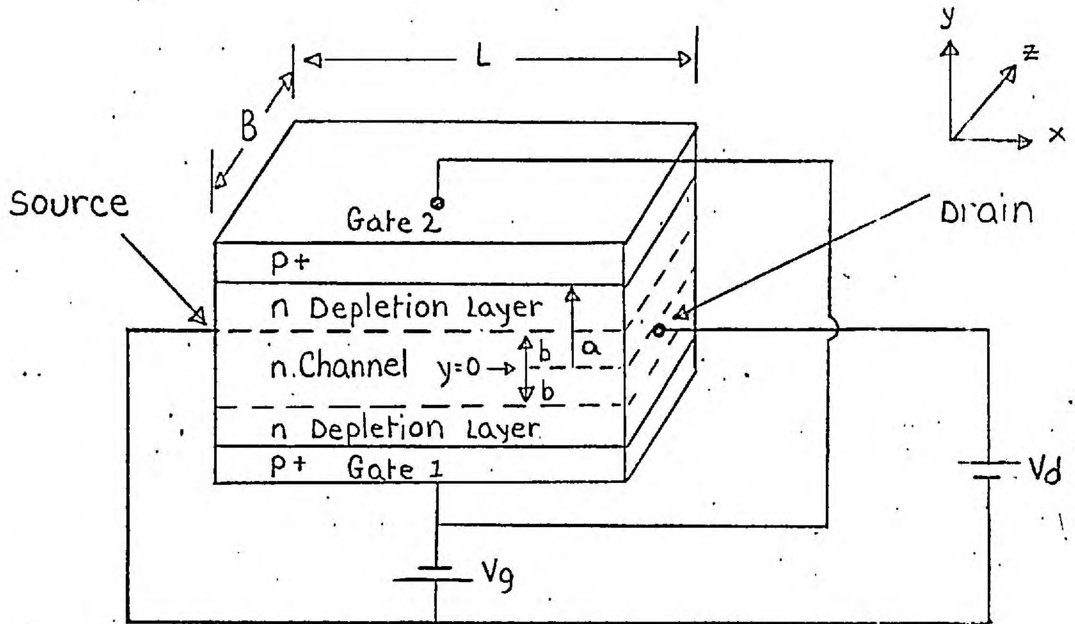


Fig. 2.2.1. : Shockley's FET Structure

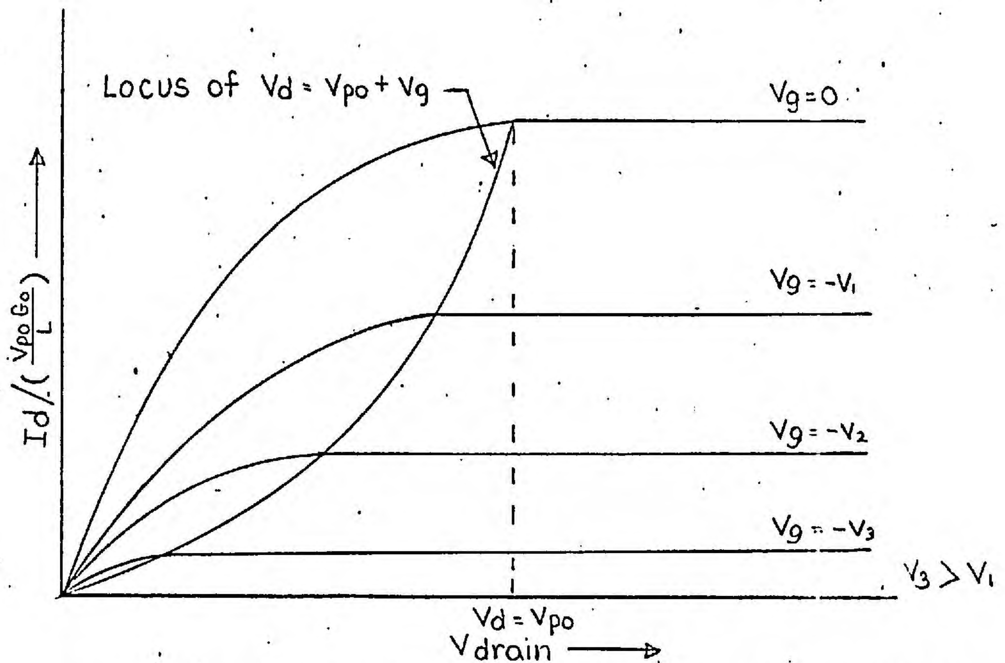


Fig. 2.2.2. : FET Drain Characteristics for Shockley's Basic Theory (Equation 2.2.14.)

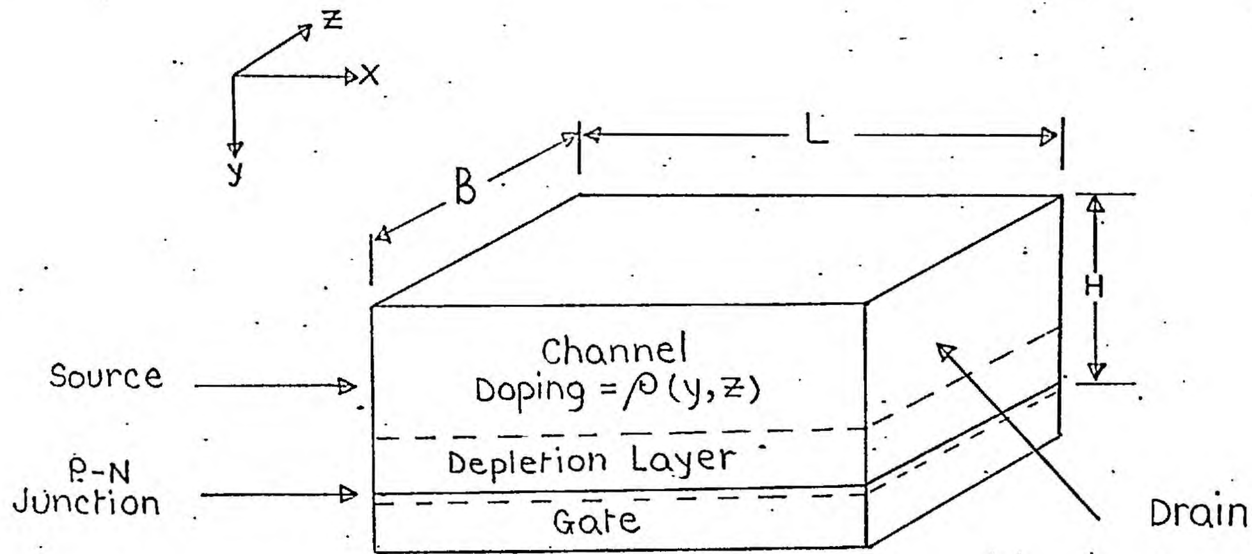


Fig. 2.3.1. : Structure for Derivation of Basic Charge Control Theory

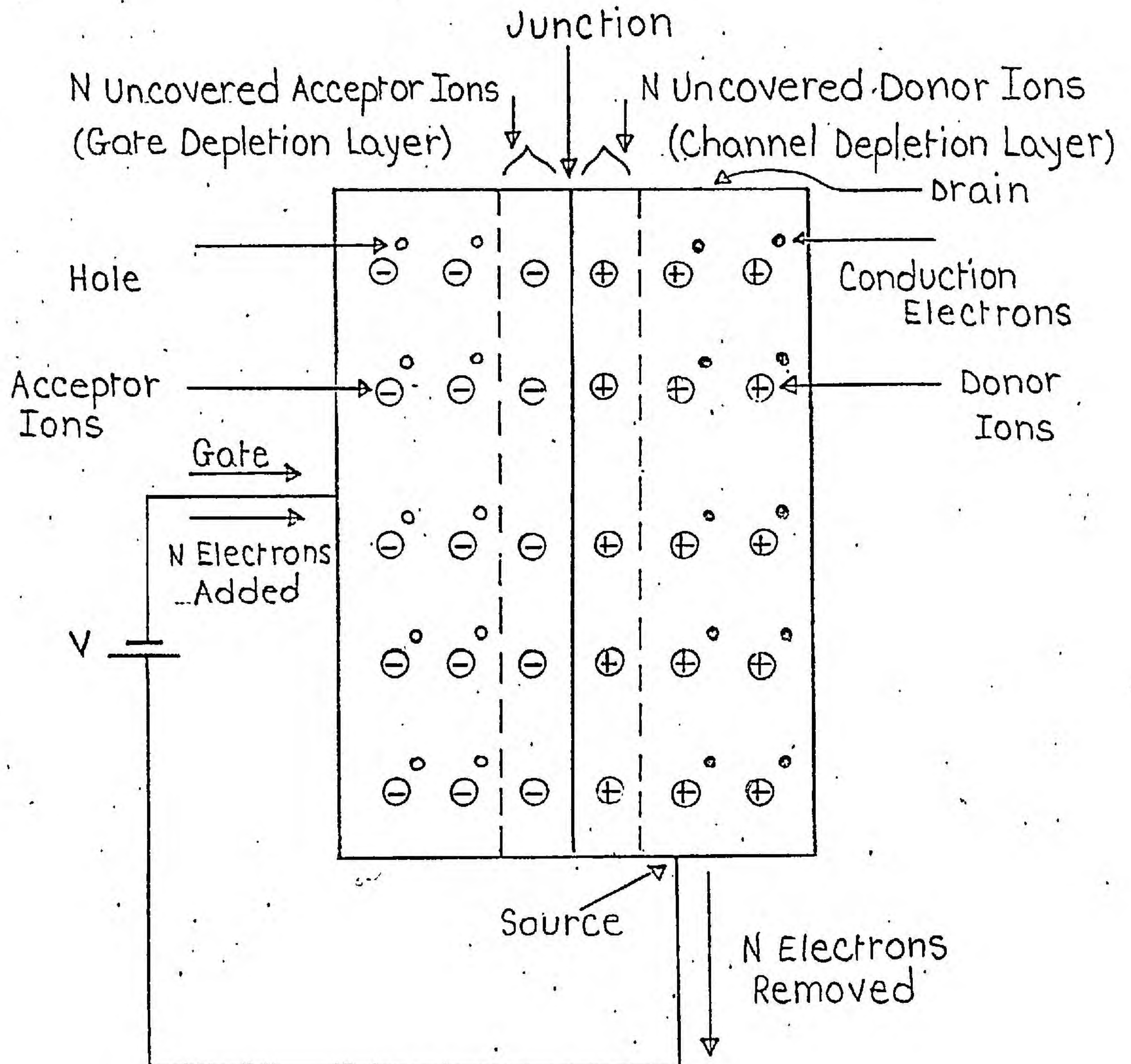


Fig. 2.3.2. : Illustration of FET Charge Particles

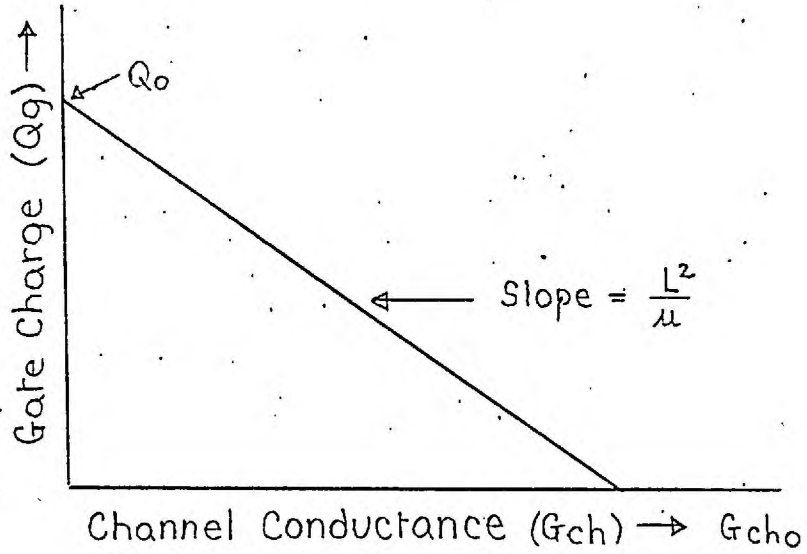


Fig. 2.3.3. : FET Gate Charge-Channel Conductance Relationship (Equation 2.3.15.)

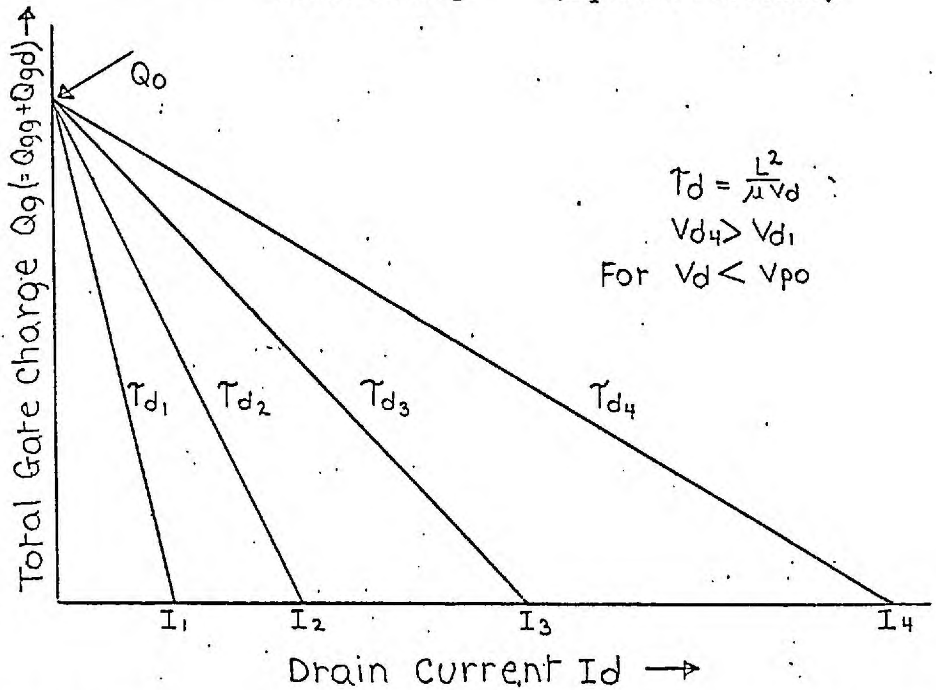


Fig. 2.3.4. : FET Charge Control Family (Equation 2.3.19.)

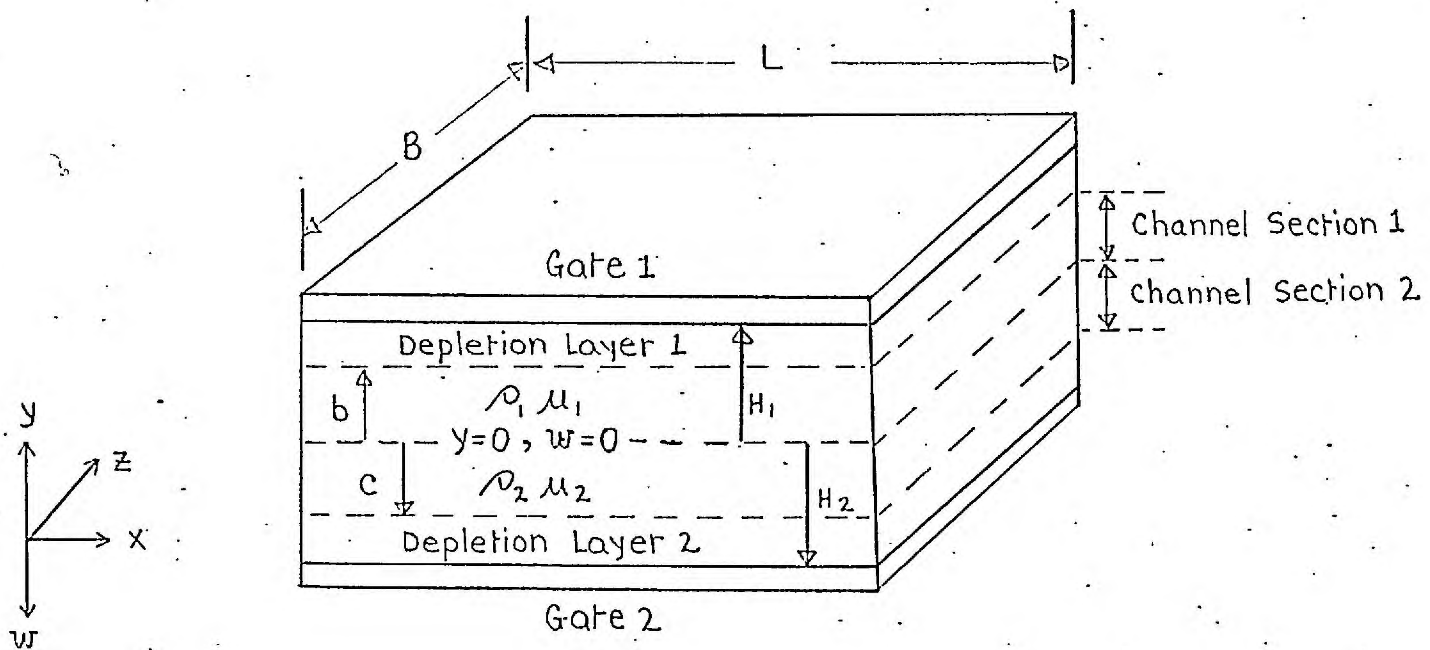


Fig. 2.3.5. : Double Gate FET Structure with Arbitrary Channel Doping Profiles

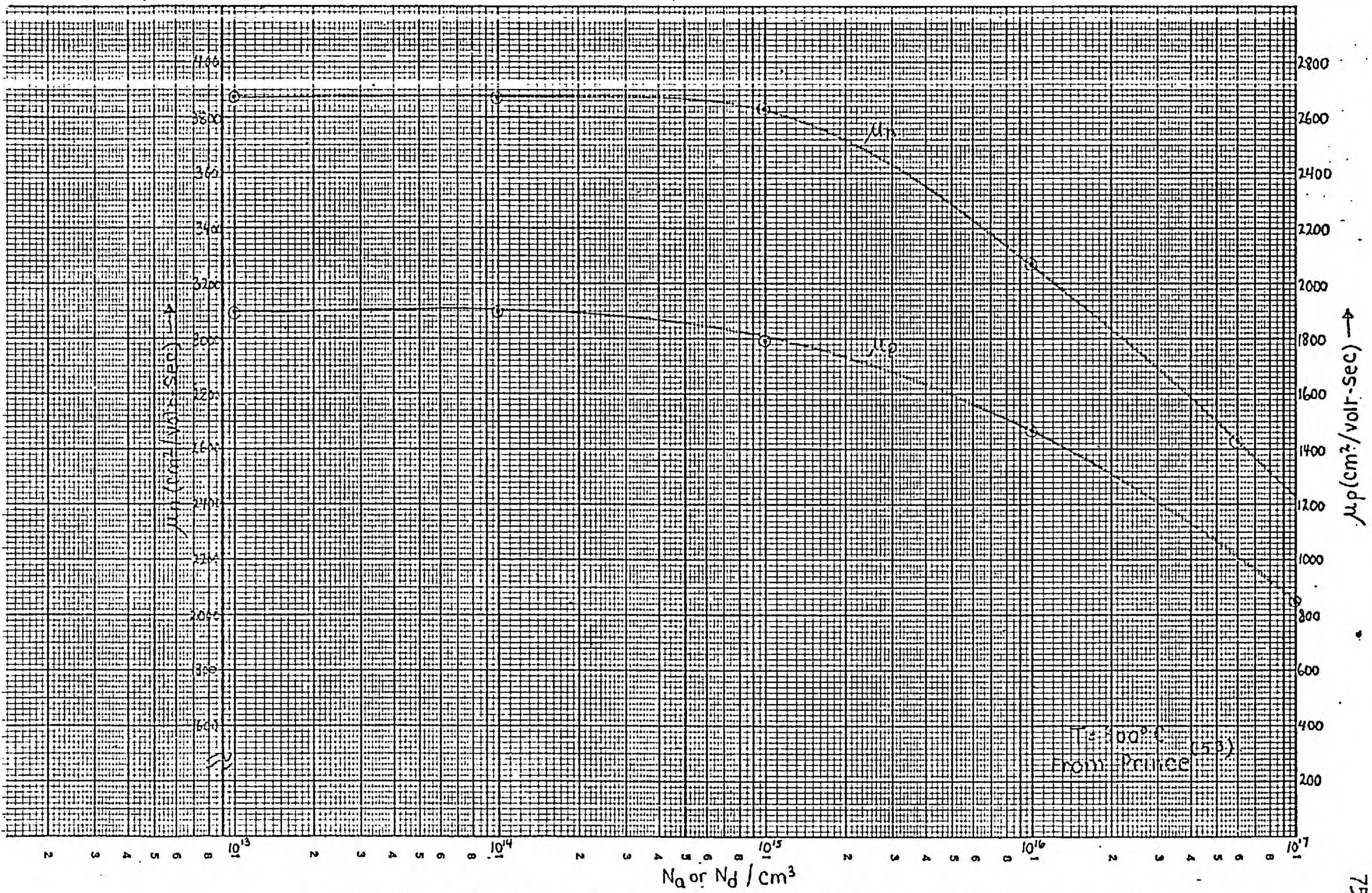


Fig. 2.3.6. : Majority Carrier Mobility Vs Doping in Germanium

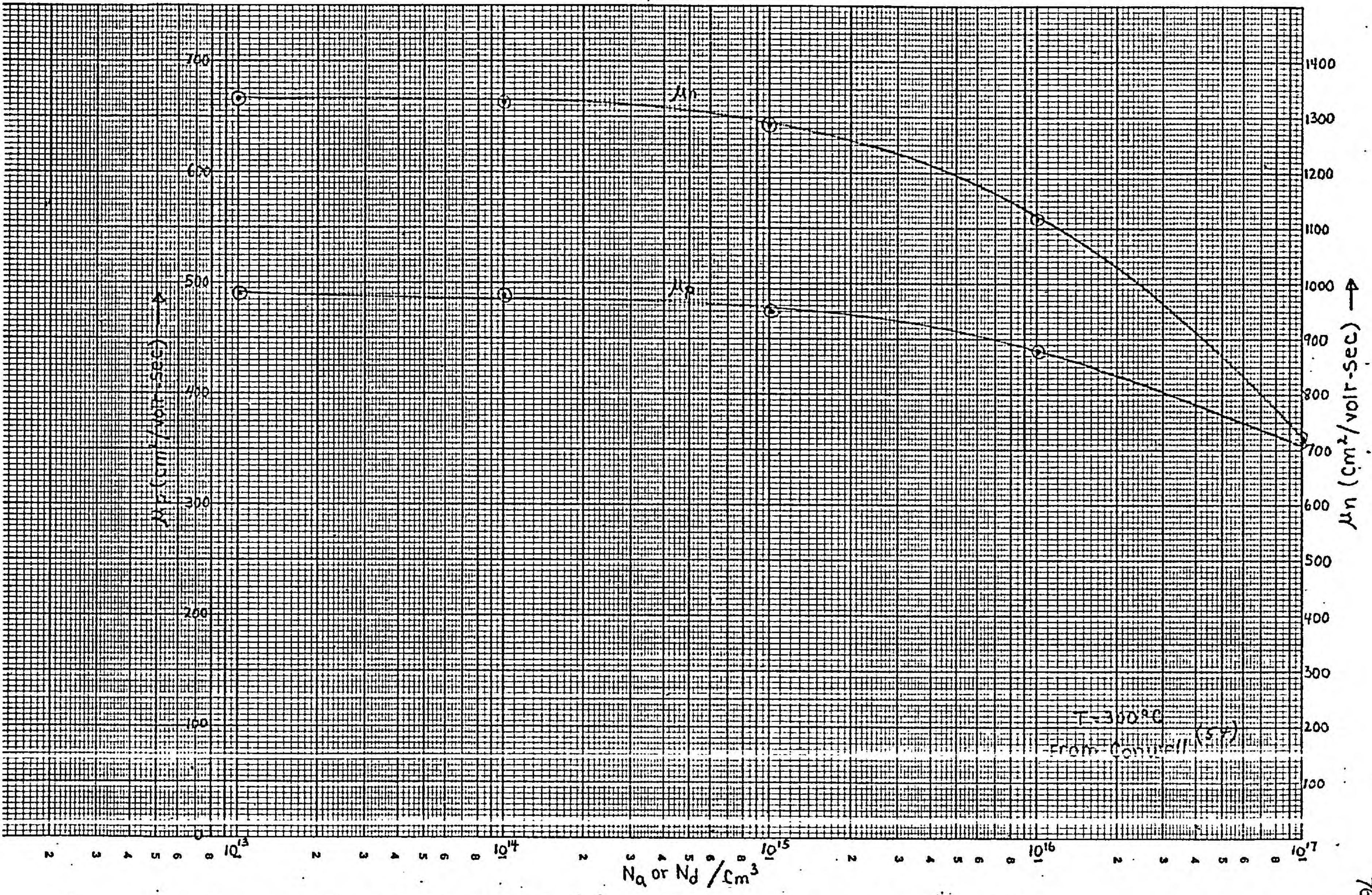


Fig. 2.3.7 : Majority Carrier Mobility Vs. Doping in Silicon

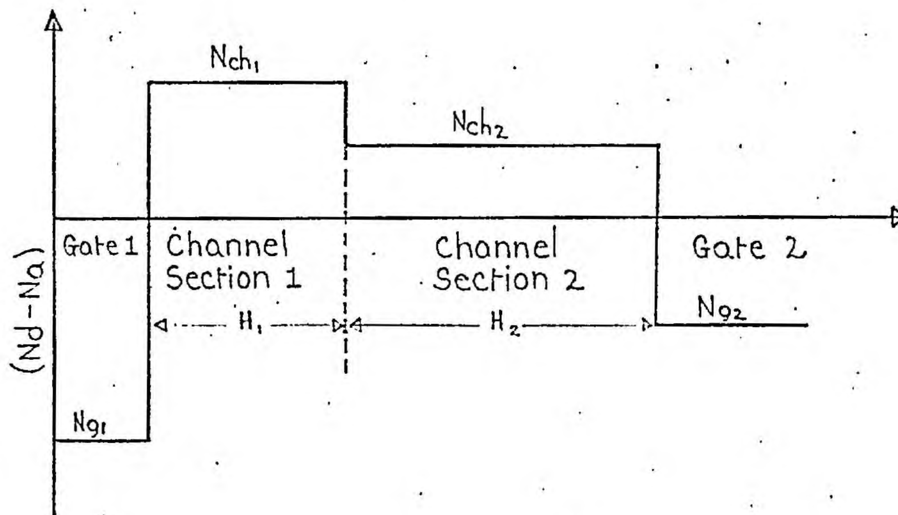


Fig. 2.3.8. : Double Abrupt Junction Doping Profile Illustration (N-Channel Device)

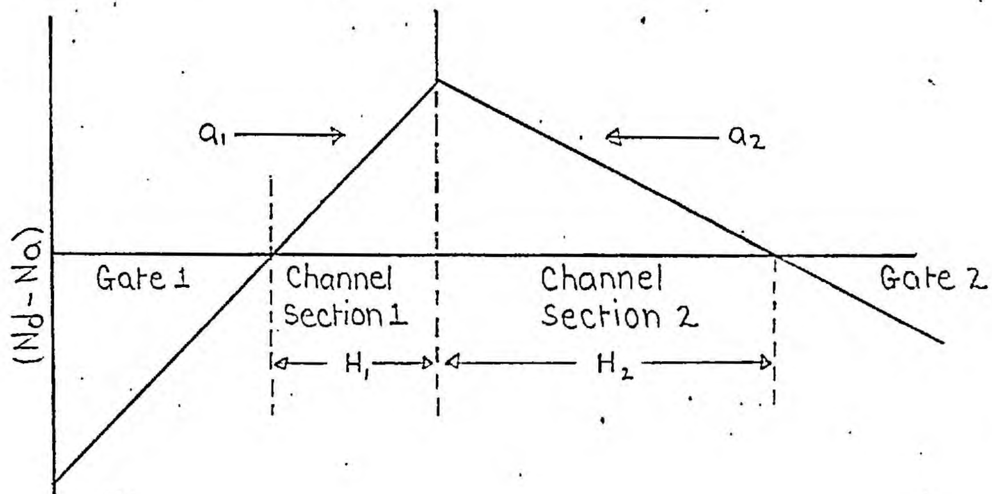


Fig. 2.3.9. : Double Linear Junction Doping Profile Illustration (N-Channel Device)

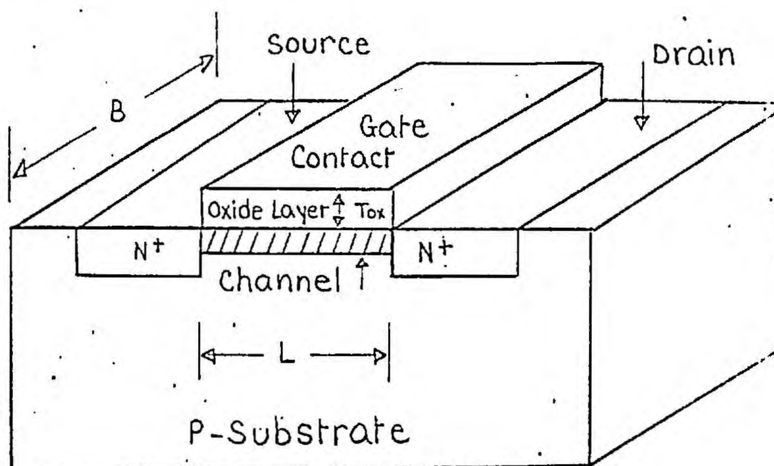


FIG. 2.4.1. : MOST Structure

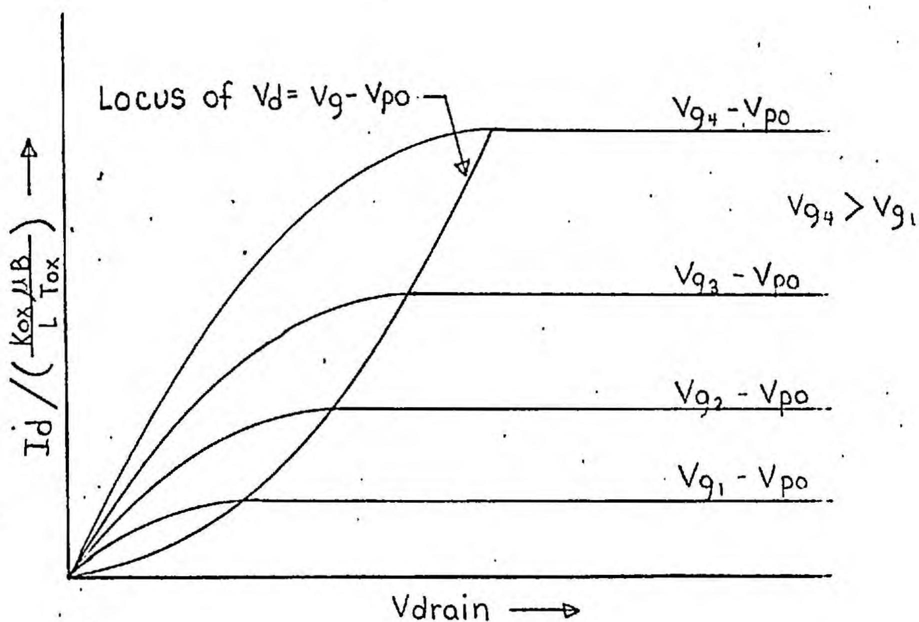


FIG. 2.4.2. : MOST Drain Characteristics Using Shockley's Basic Theory (Equation 2.4.1.)

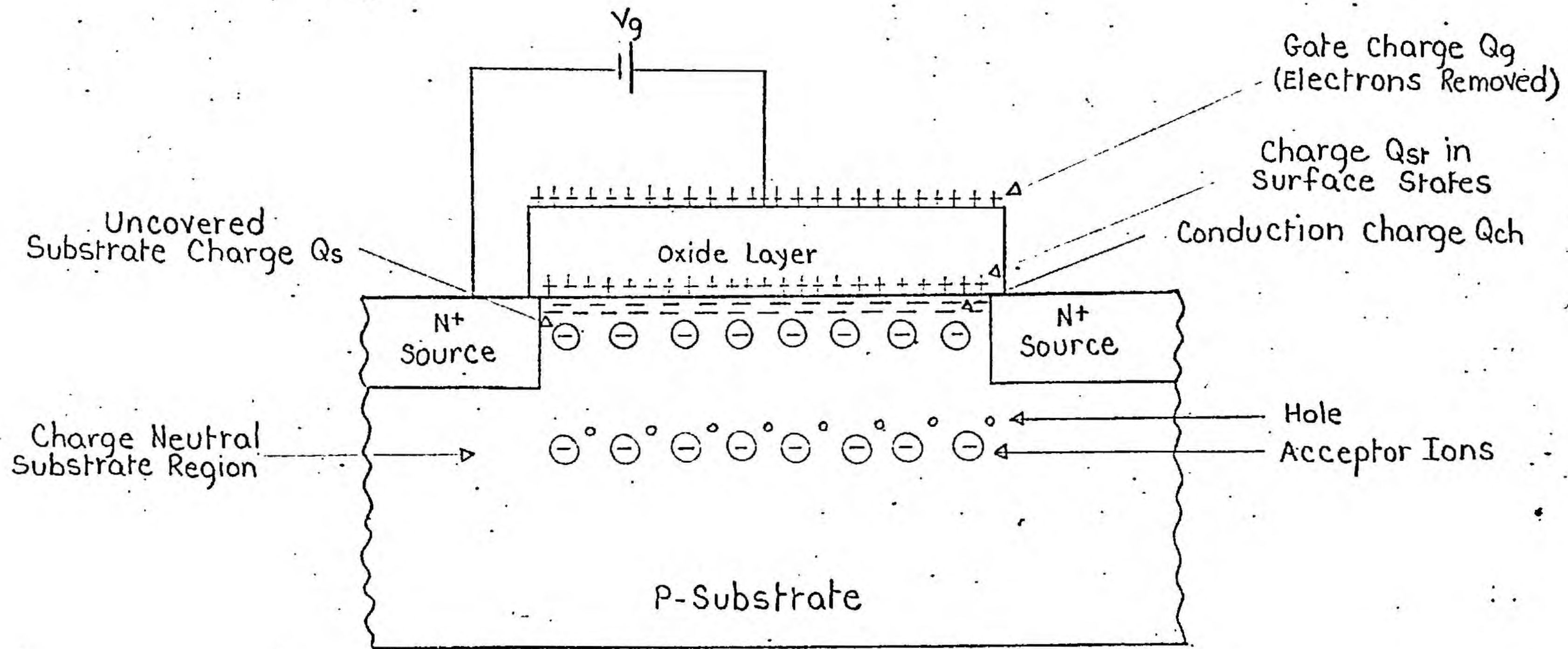


Fig. 2.4.3. : N-Channel MOST Charge Components

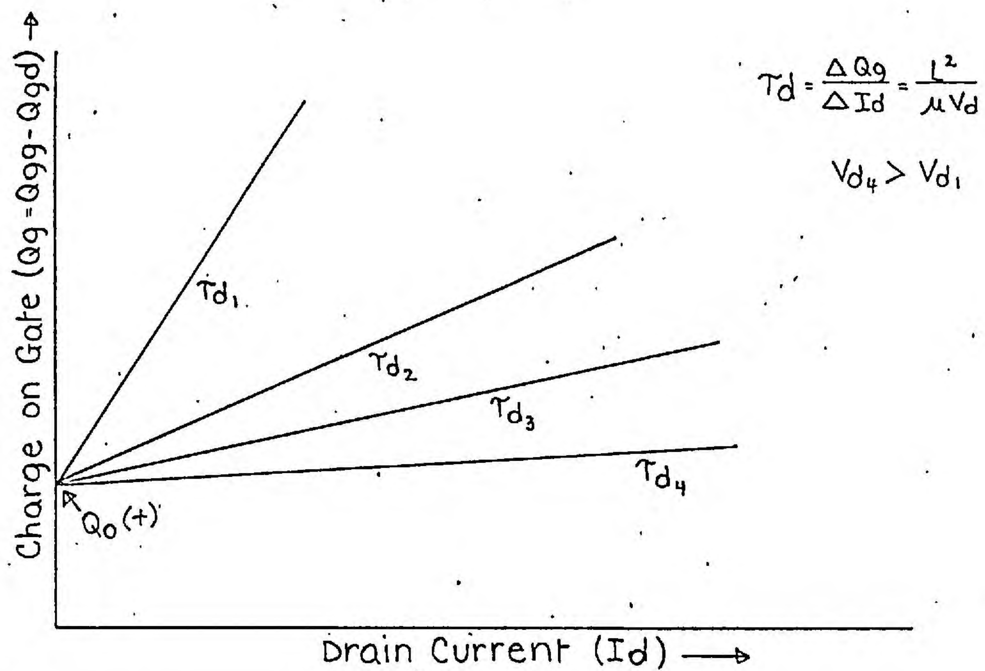


Fig. 2.4.4a. : MOST Charge Control Family (Equation 2.4.7.) For Enhancement Device

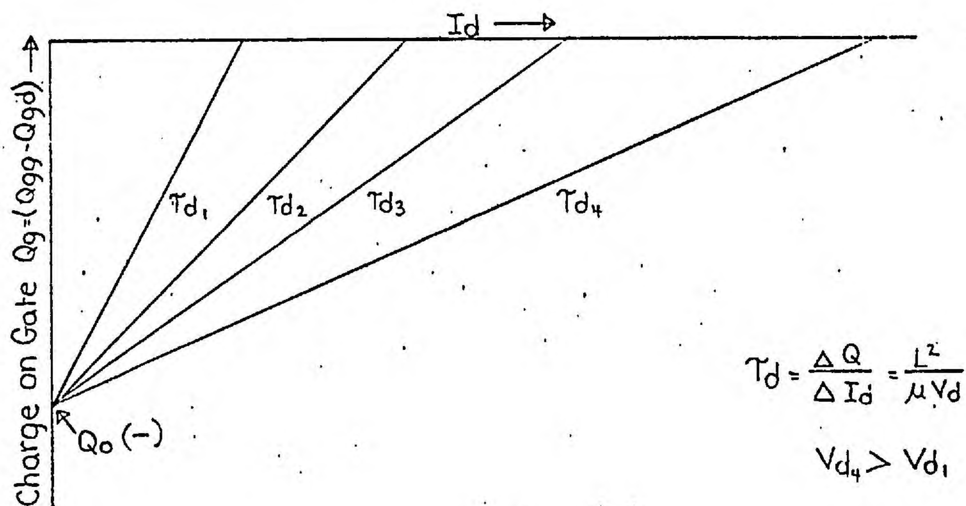


Fig. 2.4.4b. : MOST Charge Control Family (Equation 2.4.7.) For Depletion Device

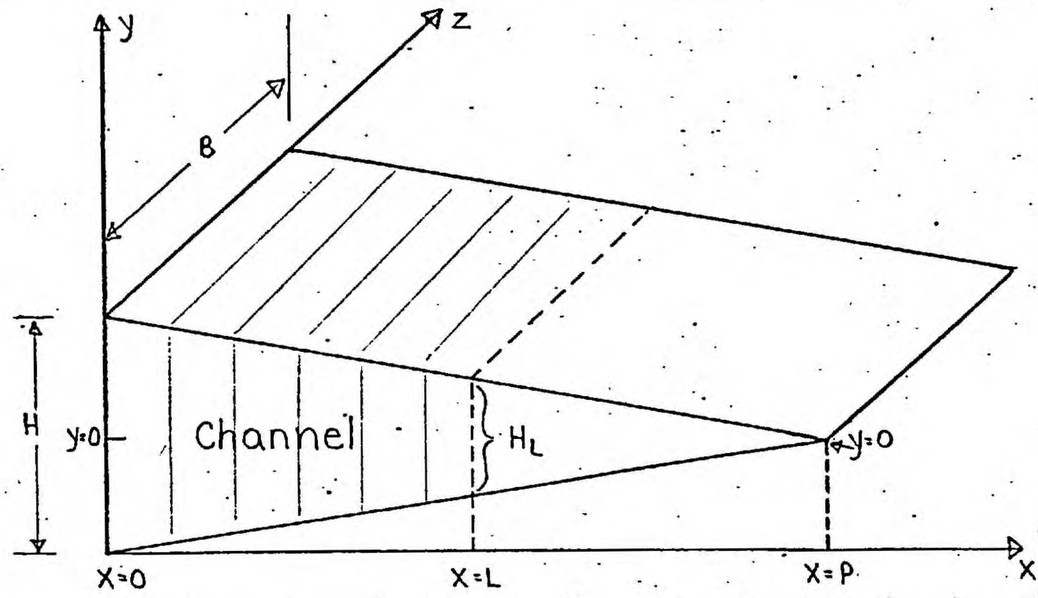


Fig. 2.5.1. : Wedge-Shaped Channel

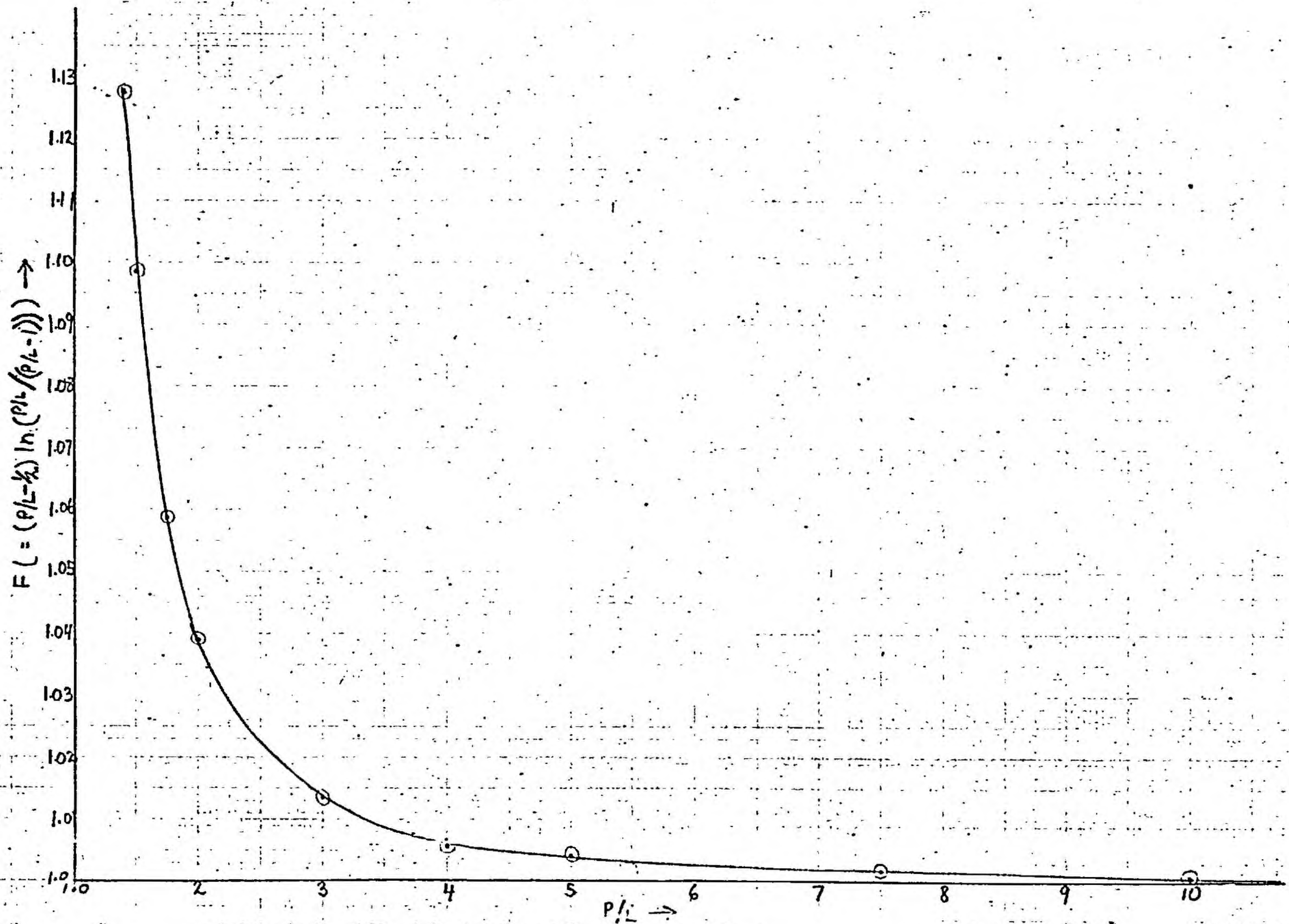


Fig. 2.5.2. Plot of F verses P/L for Wedge-Shaped Channel (EQUATION 2.5.11)

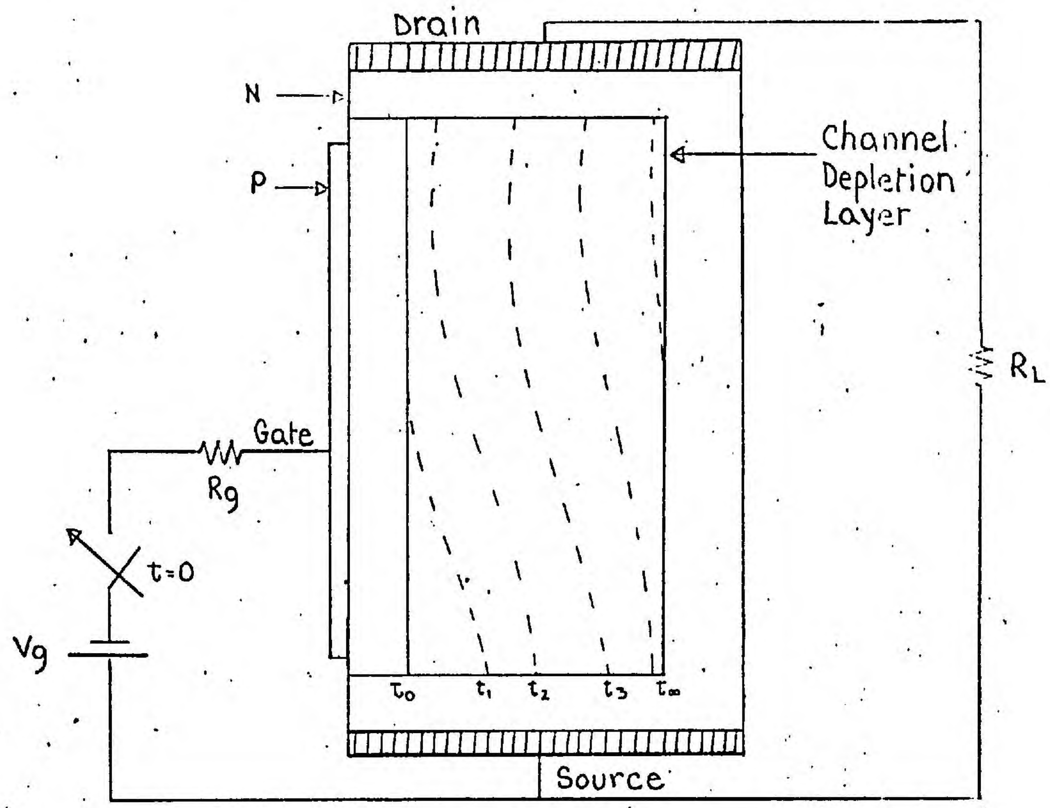


Fig. 2.6.1. : Idealized Illustration of Differential Charging Along Channel Length Throughout Switching Transient

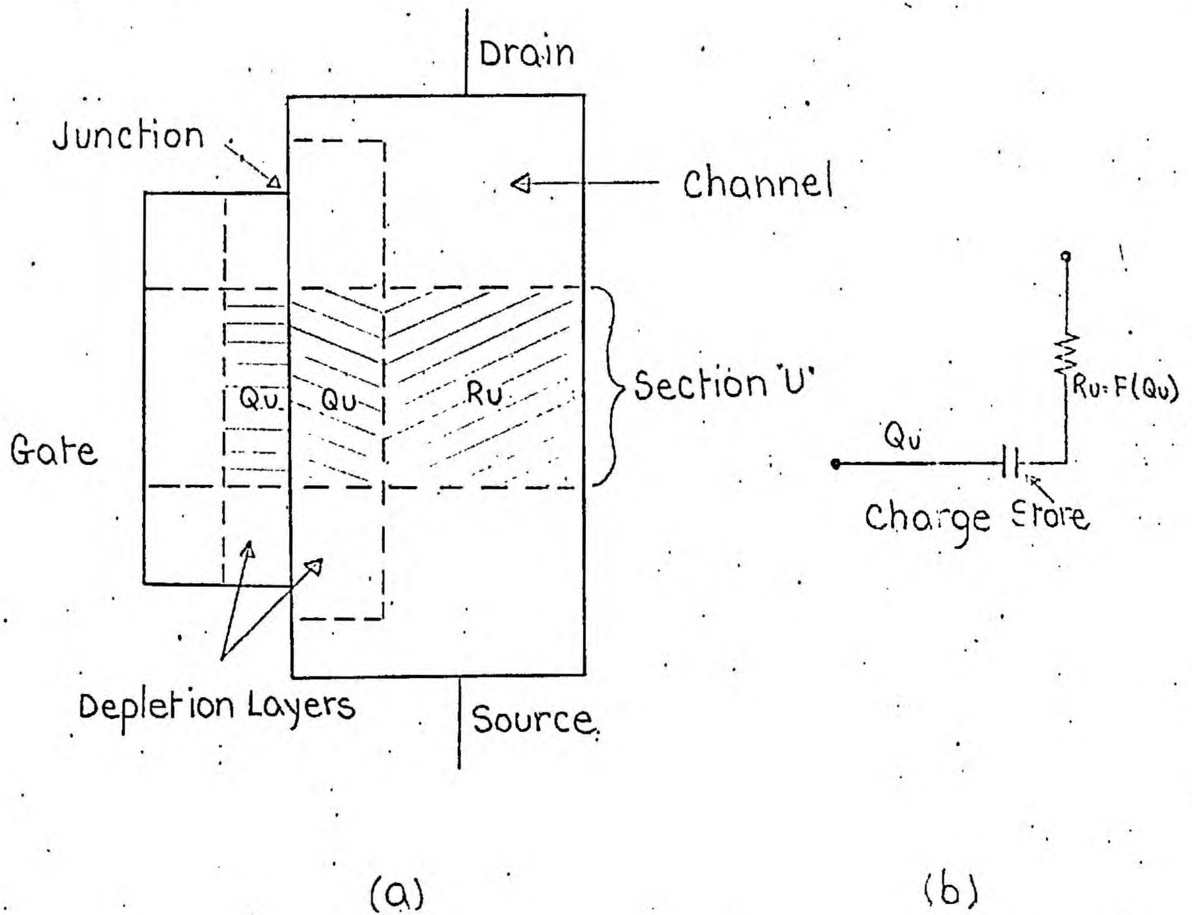


Fig. 2.6.2. : (a) FET with Section to be Lumped

(b) Lumped Equivalent Circuit Representation of Section "U" of Junction Depletion Layer and Channel

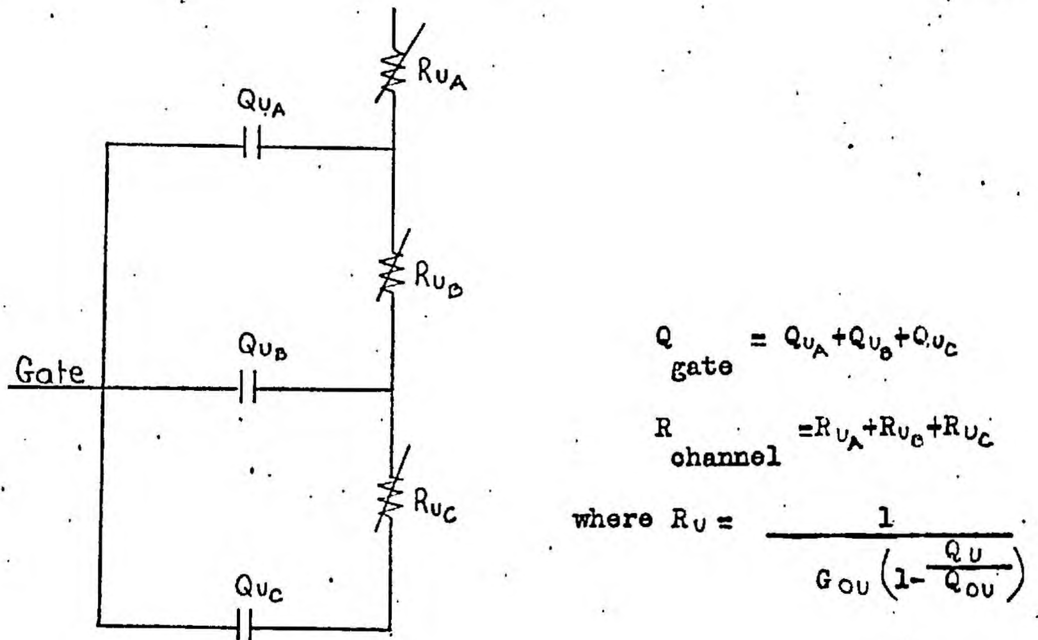


Fig. 2.6.3. : 3-Lump Gate Channel Representation (Model Incomplete)

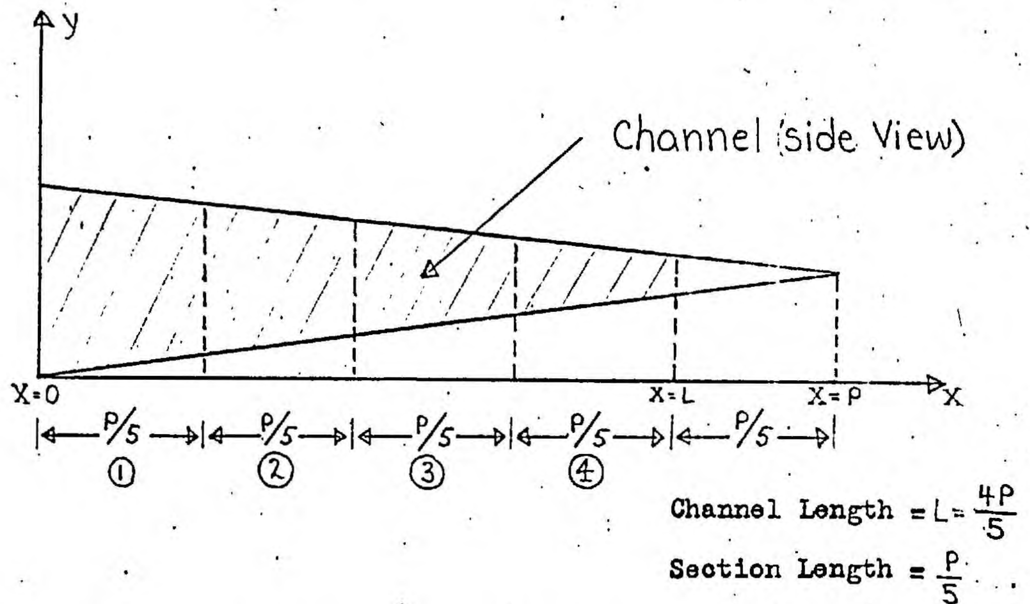
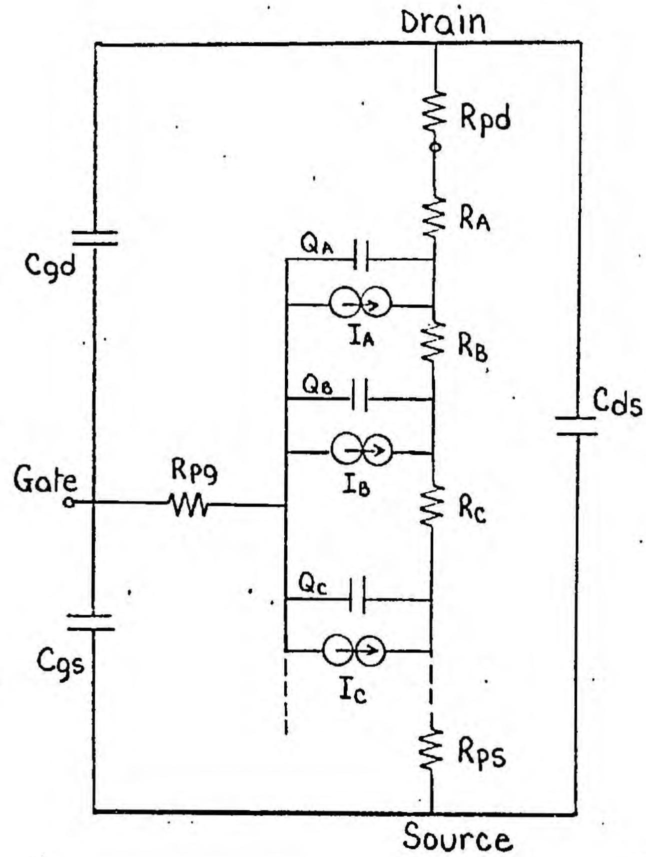


Fig. 2.6.4. : Lumping and the Wedge-Shaped Channel



I_A, I_B, I_C are Junction Leakage Current Generators

Fig. 2.6.5. : FET Charge Control Model
(Below Pinch-Off)

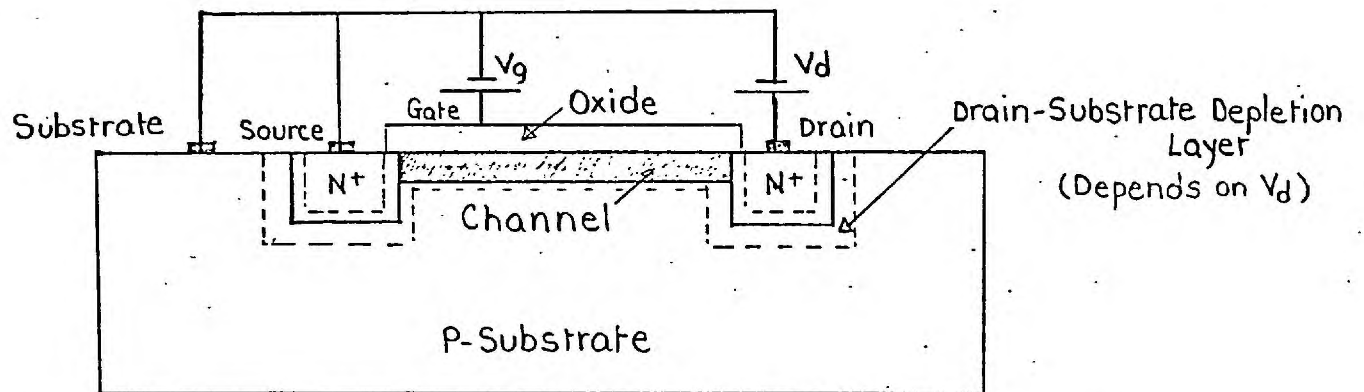


Fig. 2.6.6. : MOST Drain-Substrate Depletion Layer Capacitance

R_{ps}, R_{pd}, R_{pg}, and R_{cs} are small (see text).
C_{gd}, C_{gs}, and C_{ds} are strays.
R_{L_1} and R_{L_2} are very large gate leakage resistances.

Fig. 2.6.7. : MOST Charge Control Model for Unpinched-off Channel

CHAPTER 3

CHARGE CONTROL MEASUREMENTS AND RESULTS

3.1 Introduction

The material of Chapter 2 has been concerned with presenting the charge control relationships for both FET's and MOST's , and with considering the main factors which affect these relationships. In this chapter, the applicability of these relationships to practical devices will be considered. In addition, methods will be developed which illustrate the factors affecting device operation, and which allow these devices to be studied in greater detail.

As indicated in Chapter 2, the L^2/μ ratio of the device, and the channel time constant τ_d at various operating conditions, are very important quantities and are basic to device operation. The approach in this chapter is to study these quantities in detail for several types of practical devices throughout their ranges of operation by direct measurement of gate charge and channel current, and gate charge and channel conductance.

The necessary measurements and their methods for this study are developed and presented in Section 3.2. The results of measurements on several devices are presented in Section 3.3. A detailed discussion of these results in terms of device operation and device structure is presented in Section 3.4 for the FET's and in Section 3.5 for the MOST's. Overall conclusions regarding the effectiveness and applicability of the charge control approach as applied to field-effect transistors, and insulated gate field-effect transistors are given in Section 3.6. A brief

discussion of charge control models for devices operating with unpinched-off channels is also included.

3.2 Charge Control Measurements

Measurements of the types described in this section inevitably depend to a large extent on the availability of specific pieces of equipment. While the detailed measurement methods and jig forms presented here have thus been developed around certain instruments, alternative methods will be suggested, and sufficient general information will be given to enable the measurements to be made under other conditions.

As will be seen, the methods favoured in this section provide, where possible, continuous displays of measured quantities as obtained from an X-Y recorder or camera, as opposed to discrete point by point measurements. The main reasons for this are threefold.

Firstly, the continuous nature of the results means that the complete range of the measurements is covered without the danger of missing information "between points". Complete information in any section of the results is always available for immediate or some future use. There is no question of having to repeat the measurements because one or two points on some part of a curve seem to be in doubt, or are too widely spaced. Even if readings are taken from these curves to be operated on further, they can be conveniently and intelligently chosen, and they can easily be supplemented by others where required.

Secondly, the accuracy of this type of measurement is comparable

to or better than most point by point measurements. Usually the overall system can be correctly calibrated at some point, so that the main accuracy limitation is imposed by any non-linearities within the system.

The third main aspect of this type of measurement is that once the system is set up and calibrated, a wide range of results can be obtained on a large number of devices relatively quickly. In addition, this type of measurement is usually far less tedious and fatiguing to the operator than equivalent point by point measurements.

The measurements required here are gate charge as a function of drain current for various values of drain voltage, and of gate charge as a function of channel conductance. These measurements are not entirely unrelated, but for convenience, they will be described in three parts ; gate charge measurements, drain current measurements, and conductance measurements. In all cases, the conditions of measurements are such that the derived data represents operation in the d-c steady state.

3.2.1 Gate Charge Measurements

In considering the gate charge measurements, it is helpful to consider the effects of the high gate impedance of FET's and MOST's. It means that the gate time constant may be very large and is not basically as important in the same way as the base time constant (44) is for bipolar transistors. As previously indicated in Section 2.5, the charge decays from an open circuited gate at a rate determined by the approximately constant reverse junction leakage current in the case of FET's ; and in the case of MOST's , by the very high resistance leakage paths from gate contact to source or drain. In both cases, these quantities

can be conveniently determined by d-c measurements with a pico-ammeter.

For our purposes, the high input impedance permits short duration pulse measurements (or measurements near the start of the pulse) of gate charge without the need for a resistor in parallel with the driving capacitor as used in charge measurements on bipolar transistors (44).

On the other hand, in both the FET and the MOST, the amount of charge supplied to the device gates of these high impedance devices, is intimately related to the gate voltage. Since this gate voltage can be as large as 10 volts or more in the normal ranges of operation of these devices, it can vitally affect the drive conditions during the gate charge measurements. It is therefore necessary to measure and account for the gate voltage during these measurements.

The gate voltage is measured here with the probe of an oscilloscope. The undesirable effect of such a probe, however, is to increase unwanted capacitance across the gate. This unwanted capacitance must then be accounted for, so that it does not introduce an error in the measurement of gate charge. Before describing the specific measurement methods used here, the points discussed above are illustrated in connection with Fig. 3.2.1 , which shows a simple method which could be used to measure gate charge. This method requires an oscilloscope capable of measuring and displaying two voltages, but it need not be a sampling oscilloscope .

In Fig. 3.2.1 , C_g and R_g represent the gate capacitance and effective parrallel gate resistance of the FET or MOST ; C_p represents the capacitance of the gate probe plus stray socket and empty can capacitance. R_p is the probe resistance , and C_i and C_s represent the total series drive capacitance. Probes 1 and 2 measure the driving voltage pulse V_1 and

the gate voltage pulse V_2 respectively.

For these measurements, it is assumed that the duration of the pulse is small enough that that parallel combinations of R_p and R_g produce negligible sag in the gate voltage pulse V_2 at the time of interest. In practice, this is not difficult to obtain since the probe resistance R_p is normally the limiting factor, and that is typically 100 kilohms or 1 megohm. Normally C_s is calibrated from "zero" while C_i is an uncalibrated trimmer capacitance. If desired, however, C_i could be dispensed with, requiring that initial and final readings of C_s be taken to obtain their difference.

With C_s set to "zero", and with an empty transistor can in the transistor socket in place of the FET or MOST, C_i is adjusted initially to make the series drive capacitance equal to the probe plus stray capacitances. With an actual device in the circuit, only C_s is then adjusted to be equal to the added gate capacitance of the device itself which in general depends on the gate voltage V_2. The device gate capacitance C_g is then read directly from the calibrated dial of C_s. The charge supplied to the gate is then directly obtainable from C_s ($=C_g$) and V_2. The conditions to which C_i and subsequently C_s must be adjusted, and the equations which apply, are given below.

Firstly, for the initial adjustment of C_i with C_s set to "zero",

$$C_i = C_p ,$$

where

$$(V_1 - V_2)C_i = V_2 C_p$$

and

$$V_1 = 2V_2 \tag{3.2.1}$$

The final adjustment is made with the transistor in place by adjusting C_s from "zero" to the required value by noting V_1 and V_2. At this new condition,

$$V_1 = 2V_2$$

and $$C_s = C_g \tag{3.2.2}$$

so that the gate charge at that point is given by

$$Q_{gg} = V_2 C_g = V_2 C_s = V_1 C_s/2 \tag{3.2.3}$$

New final adjustments of C_s at other values of V_1 (and hence V_2) are then required to obtain the relationship between gate charge and gate voltage over the desired operating range of the device.

3.2.1.1 Initial Compensation Measurement Method

The measurement method actually used here involves an initial measurement to enable compensation to be made for C_p . It uses a single fixed known capacitance C_s as shown in Fig. 3.2.2, resulting in considerable simplicity in measurement jig construction. Probes 1 and 2 are now sampling oscilloscopes probes, the outputs from which are fed to the Y and X axis respectively of an X-Y recorder. A block diagram of this system appears in Fig. 3.2.3. The instruments actually used in these measurements are indicated in the diagram, but eqivalent instruments can be substituted.

The method depends upon two important features of the sampling oscilloscope. One is the X-Y recorder output facility, and the other is that the output from the sampling oscilloscope can be made proportional

to signal amplitude at any given point in the time domain. Essentially it means that the output can be made proportional to the vertical position of any one of the many samples composing the oscilloscope trace. On the Hewlett-Packard model 185B sampling oscilloscope, for example, this is accomplished by positioning the spot (or trace sample) in the desired position on the time axis by placing the "scanning" switch to "manual", and adjusting the "scan" control to the desired position. Any amplitude variations in the trace at the time-position of the spot will then result in an output relative to the "zero" or base line position. Further details of sampling oscilloscope operation can be found in the appropriate instrument manual, in this case, the operating and service manual for the Hewlett-Packard 185B (57).

In terms of the pulse measurements, the sample for each oscilloscope channel is chosen in the flat top portion of the pulse so that channel 1 output is proportional only to pulse amplitude V_1, and channel 2 output is proportional only to pulse amplitude V_2. This situation is illustrated in Fig. 3.2.4.

The entire system is calibrated for use by firstly adjusting the vertical position controls of the oscilloscope for zero voltage output with probes shorted, and then applying to both probes a d-c voltage which is accurately measured with a digital voltmeter. The gain of each oscilloscope channel and of each channel of the X-Y recorder is then set to produce the desired deflections from zero on the recorder.

Once set up, the results are obtained by merely rotating the amplitude control of the pulse generator. By so doing, the pulse voltages V_1 and V_2 are increased from zero, and a continuous recording of V_1 as

a function of V_2 is obtained on the X-Y recorder.

With an empty transistor can in the transistor socket, an initial measurement of V_1 versus V_2 is made, these initial values being subsequently denoted by primes. This results in a straight line with a slope determined by the values of C_s and C_p. For this measurement, the amount of charge in C_s is equal to the amount of charge in C_p, thus

$$Q_s = Q_p$$

or

$$(V_1' - V_2') C_s = V_2' C_p \qquad (3.2.4)$$

and

$$C_p = \frac{(V_1' - 1) C_s}{V_2'} \qquad (3.2.5)$$

where the primes denote compensating measurement quantities, and V_1' / V_2' is the constant slope of the initial measurement plot.

With this measuring method, it is important to ensure that there is no base line shift on the oscilloscope trace as the output amplitude of the pulse generator is varied, since the position of the base line is used to fix the "zero" output voltage. Base line shift can occur with some pulse generators over a region near the start of the pulse, particularly when using the combination of large pulse amplitudes and the faster oscilloscope time scale settings. In such cases, it is important during "zeroing", to set the "spot" sufficiently far from the start of the pulse that no base line disturbance is present. Otherwise, "zeroing" must be carried out with the amplitude of the pulse generator reduced to a low value. With a high quality pulse generator such as the Hewlett-Packard type 214A, the pulse is well defined, and such effects are normally

measurement.

With the desired FET or MOST in place of the empty can, V_1 is similarly measured as a function of V_2 although a straight line does not generally result. In this case

$$Q_s = Q_{gg} + Q_p \qquad (3.2.6)$$

where Q_{gg} = injected gate charge = $V_2 \; C_g$

Thus
$$(V_1 - V_2) \, C_s = V_2 \, (C_g + C_p) \qquad (3.2.7)$$

and
$$Q_{gg} = V_2 \, C_g = (V_1 - V_2) \, C_s - V_2 C_p \qquad (3.2.8)$$

Substituting for equation 3.2.5, gives

$$Q_{gg} = V_2 \, C_g = C_s \, (V_1 - V_2 \, (V_1' \, / \, V_2')) \qquad (3.2.9)$$

Equation 3.2.9 is in a form suitable for algebraic manipulation. A form more suitable for graphical manipulation can be obtained by rearranging. Thus from equation 3.2.4,

$$V_1' = V_2' \, (C_s + C_p) \, / \, C_s \qquad (3.2.10)$$

and from equation 3.2.7

$$V_1 = V_2 \, (C_s + C_p + C_g) \, / \, C_s \qquad (3.2.11)$$

Graphical subtraction at a given value of V_2 $(=V_2)$ gives

$$V_1 - V_1' = V_2 \, C_g \, / \, C_s = Q_{gg} \, / \, C_s \qquad (3.2.12)$$

Thus a plot of $Q_{gg} \, / \, C_s$ as a function of V_2 $(=V_{gate})$ can be conveniently obtained by graphically subtracting the initial plot made without the transistor, from the final plot made with the FET or MOST

in place.

3.2.1.2 Potentiometer Method of Measuring Gate Charge

A further measurement technique, called the potentiometer method, has been developed for measuring gate charge, and will be presented because of its great convenience in use. With this method, a plot directly proportional to Q_{gg} is obtained immediately on the X-Y recorder, without algebraic or graphical manipulation. It requires, however, an X-Y recorder with a differential input on one channel ; or the equivalent signal differencing obtained with a separate differential amplifier, or with two operational amplifiers.

Rearranging equation 3.2.9 , gives

$$\frac{(V_2'/V_1')}{C_s} Q_{gg} = (V_2'/V_1')\, V_1 - V_2 \qquad (3.2.13)$$

or

$$= KV_1 - V_2$$

where

$$K = (V_2'/V_1')$$

K is measured with the transistor out of the socket, and is less than 1. If then the voltage V_1 is reduced by the factor K with a potentiometer, and KV_1 and V_2 fed to the differential input of the X-Y recorder, $KV_1 - V_2$, or $\frac{(V_2'/V_1')}{C_s} Q_{gg}$, can be directly plotted against V_2 as the pulse amplitude V_1 is increased from zero. The block diagram for this method is illustrated in Fig. 3.2.5.

The value of the V_2'/V_1' ratio is obtained from an initial measurement with an empty transistor can in place of the FET or MOST

to be measured. The capacitor C_s is conveniently measured on a component bridge such as the Wayne Kerr B221.

An X-Y recorder with the required differential input was not available. The existing recorder, a Moseley model 2K-4M, was, however, slightly modified, and used in a circuit which produced the required differencing.

This recorder, in common with other equivalent recorders (for example the Houston-Advance model HR-100), has a pair of inputs for each channel, both of which can be isolated from ground for d-c voltages. The recorder deflection on a given axis depends on the potential between these two terminals, and the setting of the recorder potentiometer. The input circuit of the Moseley 2D-4M is illustrated schematically in Fig. 3.2.6.(65) When at standstill, essentially the only current drawn by the recorder is that in the potentiometer, as the balance situation requires effectively zero potential applied to the servo amplifier (i.e. across points A and B in Fig. 3.2.6).

For use in this method, the recorder internal potentiometer in the vertical axis (Y) is disconnected as shown in Fig. 3.2.7. The resultant circuit effectively sets independently the potential at each input terminal with respect to ground so that the recorder deflection is proportional to $V_{T_1} - V_{T_2}$. Beckman Helipot Model LP10 1000 ohm 10 turn potentiometers were found to be very satisfactory for use in this circuit, permitting convenient and relatively rapid system calibration.

All components in the system used for the potentiometer method with this recorder, as illustrated in Fig. 3.2.8, are calibrated similarly as before, by first adjusting the oscilloscope vertical position controls

with probes shorted to produce zero output voltage, and then by applying a measured d-c voltage to the probes (including 10:1 dividers) of both channels. With the gain of the oscilloscope channels set, the horizontal axis (X) gain (for V_2) is first set by adjusting the X-axis recorder potentiometer to produce the desired deflection. The connection to the X-axis of the recorder is then left in place so that any loading effects due to the input impedance of the internal potentiometer of the recorder X-axis is compensated for in the subsequent procedures.

Still with reference to Fig. 3.2.8, the point C is grounded by adjusting the "wiper" of potentiometer P1 to the "ground" position. The desired amount of Y-axis deflection, corresponding to the d-c voltage at the probes, is produced by adjusting potentiometer P2. Potentiometer P1 is then adjusted from the "ground" position to produce a net zero Y-axis deflection, thus setting the gains equal in each part of the differential circuit.

In its present state, the system is used to obtain the value of K ($= V_2' / V_1'$) from pulse measurement of V_2' and V_1' with only an empty transistor can in the measuring socket. K is then easily obtained from a plot of the X-Y recorder of ($V_1' - V_2'$) versus V_2' at any value of V_2'. Once obtained, the gain of channel 1 is reduced by the factor K simply by setting the dial of potentiometer P1 to its new reading, where

$$\text{New reading} = K \times \text{Previous reading}$$

Thus the entire system is calibrated to directly produce the required plot of ($KV_1 - V_2$) versus V_2.

The jig used for these charge control measurements is illustrated in Fig. 3.2.9. It is constructed on a piece of double copper clad

1/16" fibre board. 50 ohm strip line (line width $\approx$ 3.5 mm) was constructed on this board by peeling off superfluous copper on one side. Co-axial connection to this strip line is conveniently achieved with BNC 50 ohm bulkhead sockets. A socket is incorporated on the gate side of the series drive capacitor to accommodate the sampling oscilloscope probe for the measurement of V_2 . A low capacitance transistor socket was constructed from small diameter hollow tubing to accept the transistor leads. V_1 was measured across the 50 ohm line terminating resistor with the oscilloscope probe of the other channel. A socket is alsomprovided to enable the drain to be shorted to the source during these measurements as desired.

R_b is a large bias resistor through which a reverse bias can be applied to the gate during the measurements if desired. It can be used with high current devices at large drain voltages to prevent power dissipation and temperature rise, by maintaining the gate voltage at or just beyond pinch-off. In this case, the polarity of the applied pulse voltage is such as to tend to reduce the gate voltage toward zero during the pulse.

3.2.2 Drain Current Measurements

In order to ensure that the characteristics of the device alone were being observed, it was desired to measure the changes in drain current with little or no external resistance in the drain circuit. Two methods for accomplishing this will be described. One is a pulse measurement using a current transformer, and the other is a d-c measurement. Note that either a d-c or a pulse measurement of I_d is applicable

to these devices , as there is a unique relationship between gate charge and gate voltage at each constant value of drain voltage.

It is desired to correlate the gate charge and drain current measurements. Since both oscilloscope probes are required for the measurement of gate charge, these measurements must of necessity be made in two stages. The drain current measurements are made as a function of gate voltage and are thus easily correlated with measurements of gate charge as a function of gate voltage.

Drain current measurements are made using a current transformer in a manner similar to that previously described for the gate charge measurements. In this case, however, one sampling oscilloscope probe measures a voltage proportional to the magnitude of the drain current pulse, and X-Y recorder is calibrated to plot drain current versus V_2 ($=V_{gate}$) as the generator pulse voltage is changed. The same measuring jig previously described for the gate charge measurements is used with the addition of the current transformer as shown in Fig. 3.2.10.

A Tektronix type CT-1 current transformer with P6040 probe was found to be ideal for this purpose. It has a rise time of 0.35 nano-seconds, and , owing to a large decay time constant, its response is down by less than 1°/o after 50 nano seconds. Its sensitivity (5mv/ma into a 50 Ω load) is more than adequate, particularly if the type 187-C pre-amp is available for the HP 185-B sampling oscilloscope.

The CT-1 transformer has an insertion impedance of less than one ohm with the output voltage being measured across 50 ohms. The drain current is monitored by passing a short length of wire (no. 18 gauge) through the transformer. The drain voltage is applied across a capacitor,

so providing an effective short circuit for the current pulses.

Most present day FET's are relatively low current devices, but in order to prevent temperature rise within the FET at large drain voltages, a d-c reverse bias can be applied to the gate through the large resistor R_b as previously described. Another method for accomplishing this uses long reverse bias pulses with a relatively high repetition rate so that the FET is biased off for all but a relatively short time during each off-on period. The use of long pulses does not invalidate the measurement technique so long as the pulse voltage is monitored in the first 50 nano-seconds or so from the start of the reverse biasing pulse. In this situation the pulse generator voltage is maintained at a value just beyond the pinch-off voltage, and reduced to zero during the actual measurement.

Continuous d-c plots of drain current versus gate voltage can also be made on the X-Y recorder, particularly if the devices in question are relatively low current devices. The circuit for this method is shown in Fig. 3.2.11. For this method the drain current is measured across a high accuracy (or accurately measured) 1-ohm resistor so that the drain is essentially short-circuited. It is especially convenient if the gate power supply has a single knob providing continuous control of voltage over the range of interest. After X-Y recorder calibration, the FET gate is kept at or beyond pinch-off. To make the measurement, the gate voltage is reduced to zero by rotating the control knob on the power supply. The plot can be obtained relatively quickly so that for most devices negligible temperature rise results.

3.2.3 Channel Conductance Measurements

Small signal channel conductance measurements as a function of gate voltage were made in order to obtain plots of gate charge versus channel conductance for FET's and MOST's at zero drain voltage. The measurements in this chapter were made on the Wayne Kerr B221 component bridge using an external source and detector to ensure small signal conditions. The use of this bridge involves point by point measurements unless the autobalance adapter AA221 is available, or unless the newer Wayne Kerr B641 autobalance bridge is available. The autobalance principle [58] permits continuous recording of the value of the unknown so that a continuous plot of channel conductance as a function of gate voltage could then be easily obtained on an X-Y recorder.

The B221 (or B641) directly measures conductance with an accuracy of about 0.1 %. The connections for this measurement are shown in Fig. 3.2.12.

Actually, the effects of any contact and parasitic bulk are also included in this measurement. This parasitic resistance is often small in comparison with the channel resistance. If it is not negligible, it will affect the gate charge versus channel conductance relationship, as discussed later. References to the channel conductance measurements thus include this qualification.

3.3 Measured Results and Observations

It is intended in this section to present the results of measurements of several FET's and MOST's, correlate them with the measurement methods previously described, and briefly note their form. These results will be discussed in detail in Section 3.4.

For this study, charge control measurements were made on the following devices:

5 type 2N2498 P-channel diffused silicon planar FET's

3 type TIX883 N-channel alloyed gate germanium FET's

2 type TIX881 N-channel alloyed gate germanium FET's

3 type 2N3824 N-channel epitaxial layer diffused planar FET's

4 type 95BFY N-channel MOST's

At the time of writing, all the above devices are available commercially; the FET's from Texas Instruments Limited, and the MOST's from Mullard Limited. Selected manufacturer's data on each of these device types is given in the Appendix.

Since the results of the charge control measurements inevitably depend to a large extent on the structure of the device in question, a brief note on the structure of each of these types of devices will be given before proceeding to the results. The manufacturing processes used in the fabrication of these devices are similar to those used in the manufacture of bipolar transistors, and further details can be found in the literature (40).

The TIX881 and TIX883 FET's are single gate N-channel germanium devices as illustrated in Fig. 3.3.1. They consist essentially of a thin cylinder of N-type germanium on one side of which is alloyed a P-type

gate. The source contact is placed opposite the gate in an etched well. The channel length (assuming essentially one-dimensional current flow) is defined by the diameters of the etched well and of the source contact. The drain contact is made to the unetched material surrounding the well.

The 2N2498's are double gate, double diffused P-channel planar devices with a structure as shown in Fig. 3.3.2. The first diffusion forms the channel region and defines the lower gate-channel junction. The second diffusion defines the upper gate-channel junction, and is also used to connect the two gates together. The channel length in this device is ideally determined by the width of the second diffused gate region.

The type 2N3824 FET is an N-channel epitaxial layer structure as shown in Fig. 3.3.3. The epitaxial layer forms the channel and defines the lower gate-channel junction. A P-type diffusion into the epitaxial layer determines both channel length and channel height. It also connects both gates together. The source and drain are completely symmetrical in this device.

The structure of the type 95BFY MOST's is illustrated in Fig. 3.3.4. It is a diamond-like structure with a central source contact. The gate contact on the oxide layer completely surrounds the source contact, and is between the source and drain. As noted previously, these MOST's operate with an N-type channel, and are constructed on a P-type substrate.

The results presented here are divided into two types, preliminary results, and final results. Sample preliminary results on a representative FET (TIX881-2) and on a representative MOST (MOST D) are presented and discussed in Section 3.3.1. These include the pulse measurements of V_1

versus V_a ($=V_{gate}$), the drain current versus gate voltage measurements for various values of drain voltage, and the channel conductance versus gate voltage measurements. The measurement methods employed for these measurements have all been discussed in Section 3.2. These preliminary measurements are used to obtain the desired final results.

The final results for a selection of devices are presented in Section 3.3.2. These final results for each device are obtained from the above mentioned preliminary measurements, as discussed in Section 3.2, and are the gate charge versus channel conductance relationship at zero drain voltage, and the gate charge versus drain current relationship for each of several values of drain voltage.

The devices whose final results are presented in Section 3.3.2, and discussed in detail in Sections 3.4, and 3.5 are as follows: TIX881-2, 2N2498-3, 2N2498-5, 2N3824-3, MOST D and MOST 6. Some results are also presented for devices TIX883-1 and 2N3824-2 for comparison purposes. These representative devices have been chosen to illustrate results in several different types of devices with different structures and made by different manufacturing processes ; and also to illustrate differences within devices of the same type.

As discussed in greater detail in Section 3.4 and Section 3.5, these charge control measurements were made on each device at various values of drain voltage (including zero) to test the validity of the basic theory presented in Chapter 2 for the unpinched-off channel, and to investigate the applicability of the charge control approach over a wide range of conditions, specifically beyond pinch-off.

3.3.1 Preliminary Results

In this section it is intended to present a sample set of preliminary results for one FET (TIX881-2) and for one MOST (MOST D). Final results are presented in Sections 3.3.2 for these and the other devices to be discussed in detail in Section 3.4 and 3.5.

Figures 3.3.5 and 3.3.6 show graphs, as produced form an X-Y recorder, of V_1 versus V_2 for a family of drain voltages (positive) for devices TIX881-2 and MOST D respectively. These pulse measurements were made as described in Section 3.2.1.1 and illustrated in Figures 3.2.2 and 3.2.3, with the measurement jig illustrated in Fig. 3.2.9. As indicated in Fig. 3.3.5, a series drive capacitor $C_s = 9.79$ pf was used for the measurements on device TIX881-2. An initial compensation measurement with an empty transistor can in the socket gave a value of 1.39 for V_1' / V_2'. For MOST D, a value of $C_s = 15.0$ pf was used, and the initial compensation measurement gave $V_1' / V_2' = 1.48$.

It is to be noted that the zero or starting position for each of the curves in Figures 3.3.5 and 3.3.6 is moved horizontally on the V_2 (V_{gate}) axis. This was done for convenience in separating the individual curves. The basic difference between the plots for the two devices is that those for TIX881-2 are quite curved, while those for MOST D are essentially straight lines. The curves for TIX881-2 (and for the other junction FET's) result from the non-constant capacitance versus voltage relationship of the gate junction.

The straight line plots in Fig. 3.3.6 for MOST D, indicate a constant gate capacitance at a given drain voltage. The slope of each plot is slightly different, however, indicating that the drain voltage

has some effect on the gate capacitance. The reasons for this will be brought out in the discussions in Section 3.5. Not all of the MOST's measured produced straight line plots of V_1 versus V_2. Some curvature was noted particularly at large drain voltages in the plots for MOST 6 for example. The reasons for this will also be discussed in Section 3.5.

Fig. 3.3.7 shows d-c measurements of drain current versus gate voltage, as obtained on an X-Y recorder, for several drain voltages for device TIX881-2 measured as illustrated in Fig. 3.2.11, and described previously in Section 3.2.2. The current scale, though convenient for presentation here, is normally more sensitive. Note that the zero current position for each curve is shifted vertically as indicated, for convenient separation of the individual curves. Being an N-channel device, the drain voltages are positive. Gate voltage increases negatively to the right, thus reducing I_d to zero. The drain current versus gate voltage curves for other FET's are similar to those in Fig. 3.3.7. For a P-channel device, however, the polarity of the applied voltages is reversed.

Figures 3.3.8 and 3.3.9 each show similar curves for MOST D, but for different drain voltages. The zero current position for each of the curves in Fig. 3.3.9 is shifted as described above, but those in Fig. 3.3.8 are not. The curves in both figures are made with positive drain voltages, and for gate voltage increasing positively to the right. Being also an N-channel device, greater drain current flows for larger values of gate and drain voltage, indicating enhancement operation.

Two important basic effects emphasized in Fig. 3.3.8 as well as in the final results, are noted here. They will be discussed in Section 3.5. The first is that for this device, approximately +2 volts on the

gate are required to produce current flow, irrespective of the drain voltage. The second is that drain current saturation occurs with increasing gate voltage, particularly at the lower values of drain voltage.

The remaining preliminary relationship to be presented for each of these devices is the relationship between gate voltage and small signal channel conductance measured at zero applied drain voltage. These relationships are shown in Fig. 3.3.10 for TIX881-2 and in Fig. 3.3.11 for MOST D. These measurements were obtained as discussed in Section 3.2.3 and as illustrated in Fig. 3.2.12.

In Fig. 3.3.10 for TIX881-2, the vertical scale is the applied reverse bias gate voltage increasing negatively in the upward direction. As the applied gate voltage is increased, the channel moves closer to pinch-off, and the channel conductance G_{ch} decreases. The form of this plot for other FET's is similar, but the exact shape varies from device to device depending on the junction law, the pinch-off voltage, and other device properties.

The V_g versus G_{ch} plot in Fig. 3.3.11 for MOST D shows gate voltage increasing positively upwards. It is seen that increasing gate voltage increases channel conductance. There is a considerable straight line section in the mid-region of this plot. Since the V_1 versus V_2 plot in Fig. 3.3.6 for this device indicates a constant gate capacitance as a function of gate voltage, it may be expected that the shape of the Q_{gg} plot presented in the next section will be very similar. The form of the V_g versus G_{ch} plots for the other MOST's measured is similar to that of Fig. 3.3.11, the main difference being a shift up or down relative to the G_{ch} axis, depending on device pinch-off voltage. This will be

clearly shown also by the final results presented in the following section for MOST 6.

3.3.2 Final Results

As indicated earlier in Section 3.3, it is intended in this section to present final charge control results for the selected representative devices, to comment on them briefly, and to note their form as a preliminary to more detailed considerations later, in Sections 3.4 and 3.5. The gate charge versus channel conductance relationships will be presented first for each of the devices TIX881-2, 2N2498-3, 2N2498-5, 2N3824-3, MOST D and MOST 6. The family of gate charge versus drain current relationships for each of the above devices will then be presented. Both types of charge control relationships for each of these devices will then be studied and discussed in detail in Section 3.4 for the FET's and in Section 3.5 for the MOST's.

The final results presented in this section were obtained from preliminary measurements on each device similar to the preliminary measurements previously discussed in Section 3.3.1 for device TIX881-2 and MOST D (Figures 3.3.5 through 3.3.11). The values of gate charge Q_{gg} in each case were obtained from equation 3.2.9 from the corresponding plot of V_1 versus V_2 (knowing C_s and V_1' / V_2'). The Q_{gg} values thus obtained were then plotted against the corresponding values of G_{ch} or I_d at a given drain voltage. Note that for MOST D where the V_1 versus V_2 relationship is constant, the calculation of Q_{gg} from equation 3.2.9 is considerably simplified.

3.3.2.1 Gate Charge Versus Channel Conductance Relationship

The gate charge (Q_{gg}) versus channel conductance (G_{ch}) relationship for device TIX881-2, together with that for TIX883-1, is shown in Fig. 3.3.12. Similarly the Q_{gg} versus G_{ch} relationships for devices 2N2498-3 and 2N2498-5 are shown in Fig. 3.3.13. The Q_{gg} versus G_{ch} relationship for device 2N3824-3 is shown in Fig. 3.3.14. A very high conductance device, 2N3824-2, is also shown in Fig. 3.3.14 for comparison. Figures 3.3.15 and 3.3.16 present the gate charge versus channel conductance relationships for MOST D and MOST 6 respectively. The vertical scale for the FET's (Figures 3.3.12 through 3.3.14) indicates the amount of charge injected into the gate and removed from the channel. Thus, increasing Q_{gg} decreases the channel conductance, and moves towards pinch-off. Increasing Q_{gg} upward for the MOST's, corresponding to the application of a positive gate voltage, increases the amount of conduction charge in the channel, and thus increases the channel conductance. MOST 6 in Fig. 3.3.15 has a channel conductance of 4.5 mmhos at zero injected gate charge (zero applied gate voltage). If charge is removed from the channel (downward on the Q_{gg} scale) corresponding to the application of a negative gate voltage, the channel conductance is decreased similar to a junction FET.

The gate charge versus channel conductance relationship is important in that it allows the FET or MOST to be studied in the simplest way without having to consider any possible disturbing effects due to drain voltage. The gate charge versus channel conductance relationship corresponds to equation 2.3.15 for the FET and to the conductance relationship obtained from equation 2.4.3 (together with equation 2.4.5 for $Q_{gd}=0$) for

the MOST. These basic equations predict a straight line relationship, and thus the regions of constant slope corresponding to regions of constant L^2/μ ratio are of interest in these plots.

It can be seen that a straight line or constant slope region exists in the Q_{gg} versus G_{ch} relationship for each of these devices. In general, however, it does not extend over the complete range of the Q_{gg} versus G_{ch} plot for these devices. The reasons for this observed behaviour will be dealt with in Section 3.4.1 for FET's , and in Section 3.5.1 for MOST's.

3.3.2.2 Gate Charge Versus Drain Current Relationships

The gate charge versus drain current relationships for various drain voltages are shown in Figures 3.3.17 through 3.3.2 for devices TIX881-2, 2N2498-3, 2N2498-5, 2N3824-3, MOST D, MOST 6 respectively. Note that some of the relationships, for devices TIX881-2, 2N2498-3, and 2N2498-5, as specifically indicated on the figures concerned, have their "zero" position vertically shifted for clear presentation.

The Q_{gg} versus I_d relationships for the FET's correspond to equation 2.3.19 derived in Chapter 2. Similarly, the Q_{gg} versus I_d relationships for the MOST are equivalent to equation 2.4.7. As indicated in Chapter 2, the straight line or constant slope aspect of these relationships are of interest. As expected in the FET case, the Q_{gg} versus I_d relationships at very low drain voltages are similar in shape to the corresponding Q_{gg} versus G_{ch} relationship at zero drain voltage. Compare for example, the Q_{gg} versus I_d relationship for TIX881-2 for $V_d = 0.5$ volts in Fig. 3.3.17 with the Q_{gg} versus G_{ch} relationship for this device in Fig. 3.3.12. The extent of the linearity observed in the Q_{gg} versus I_d

relationships for FET's at large values of drain voltage (Figures 3.3.17 through 3.3.20), however, is very interesting and highly significant, as will be shown in Section 3.4, in that it is not predicted by the Shockley theory. The Q_{gg} versus I_d relationships for the MOST's particularly those for MOST D in Fig. 3.3.21, exhibit considerable straight line regions. Deviations from constant slope do occur in general, however, in both the FET and the MOST relationships in certain regions just as was noted in Section 3.3.2.1 in connection with the Q_{gg} versus G_{ch} relationships.

A detailed study of these relationships will be carried out in Section 3.4.2 for the FET's and Section 3.5.2. for the MOST's. The deviations from constant slope will be considered and these plots will be related to the Q_{gg} versus G_{ch} relationships. Further, the effects of drain voltage on these relationships and on device operation will be established.

3.4 Discussion of Results on Field-Effect Transistors

In this section, the charge control results presented in Section 3.3.2 relating specifically to the FET's, are studied and discussed in detail. The MOST results presented also in Section 3.3.2 are similarly considered in Section 3.5. The object of this section is to determine from a detailed study of these results, the validity and applicability of the basic charge control relationships derived in Chapter 2, Section 2.3, to the several representative types of FET's, over a wide range of operating conditions.

As previously indicated, the basic theory predicts straight line relationships for both the Q_{gg} versus G_{ch} and the Q_{gg} versus I_d relationships. Although straight line regions occur in each of these relationships, serious deviations do occur in certain regions of operation. These deviations will be considered in detail to determine if the basic theory is inadequate, or whether these deviations are due to the physical process within the device. Further, it is intended to investigate the effects of drain voltage on the observed charge control relationships, and to determine the validity of the assumption made in Chapter 2, Section 2.3, neglecting channel shape distortion.

The study of these results is divided into two parts. Firstly, in Section 3.4.1, the Q_{gg} versus G_{ch} relationships for these FET's are considered and discussed. Since these results were obtained with zero applied drain voltage, this complicating factor is removed, and thus is not considered in Section 3.4.1.

The second part, in Section 3.4.2, is concerned with the Q_{gg} versus I_d relationships, and thus is specifically concerned with drain voltage

effects. In this section, the Q_{gg} versus I_d results are related to the discussion of the Q_{gg} versus G_{ch} results in Section 3.4.1, and the additional effects due to drain voltage considered. The interpretation of these results involves a detailed discussion of the internal operating mechanisms of the device both below and above pinch-off.

3.4.1 Gate Charge Versus Channel Conductance Graphs

It was shown in Chapter 2, Section 2.2, that for a device with negligible parasitic source and drain resistances, with constant channel length, and with constant majority carrier mobility throughout the channel, the relationship between gate charge and channel conductance should be a straight line (equation 2.3.15). Further, this straight line relationship is to be expected whether the device has one or two gates, and whether its junction(s) are abrupt or diffused so long as the majority carrier mobility does not vary throughout the channel (equation 2.3.28).

The measured gate charge versus channel conductance relationships for the FET's in Figures 3.3.12, 3.3.13, and 3.3.14 , for convenience in the discussion, will each be assumed to consist of three regions : a mid-region consisting of the straight line portion of the plot, an upper region or high gate charge, low channel conductance region where the plot curves upward, and a lower region or low gate charge, high channel conductance region , where the plot curves downwards.

All regions of operation need not necessarily be present in any device. As can be seen from Fig. 3.3.12, the plot for TIX883-1 contains no lower region. The straight line region starts from zero injected gate charge for this device. The plots for 2N3824-2 and 2N3824-3 in

Fig. 3.3.14 show only a very small upper region.

3.4.1.1 Mid-Region

In the region of constant slope, it can be assumed as indicated above that true charge control operation exists, and that the requirements for its existence have been met. Thus in this region, both channel length and the majority carrier mobility are effectively constant, and any parasitic bulk source and drain contact resistances are negligible. Further, each unit of gate charge must be directly employed in affecting channel conductance.

One important aspect which is common to all these plots is that the straight line region in every case corresponds to the minimum slope that exists for each plot. This means that the effective L^2/μ ratio in this region is at its smallest value, corresponding ideally to a minimum value of majority carrier mobility μ. Note that for the abrupt junction devices studied here, the effective channel length is defined by the dimensions of the etched well, and source contact diameter (Fig. 3.3.1). In the other FET's, however, (Figures 3.3.2 and 3.3.3) the effective channel length depends on the bounds of the upper gate diffusion , and length of any associated depletion region along the channel.

The slope of the straight line region for each device obtained from Figures 3.3.12 through 3.3.14 is listed in Table 3.4.1. It can be seen from this table that a considerable range in the value of this slope (i.e. L^2/μ ratio) is covered with these devices, ranging from 74.6×10^{-9} volt-sec for TIX881-2 to 1.65×10^{-9} volt-sec for 2N3824-2. It is interesting also that this progression in L^2/μ ratio corresponds to the age of each type from the oldest, TIX881's , to the youngest, 2N3824's.

TABLE 3.4.1

L^2/μ RATIO FROM Q_{gg} VERSUS G_{ch} RELATIONSHIPS FOR TIX881-2, TIX883-1, 2N2498-3, 2N2498-5, 2N3824-2 AND 2N3824-3.

FET	$L^2/\mu \times 10^{-9}$ (volt-sec)
TIX881-2	74.6
TIX883-1	28.35
2N2498-3	16.85
2N2498-5	8.32
2N3824-3	2.63
2N3824-2	1.65

Undoubtedly, this trend will continue with newer devices, as a small value of L^2/μ uses gate charge more effectively, and tends to increase device transconductance (40).

In abrupt junction devices such as those of Fig. 3.3.12, it is to be expected that essentially uniform doping should prevail throughout the channel region, producing a constant majority carrier mobility in the channel according to the doping concentration as indicated in Figures 2.3.6 and 2.3.7. Note that the N-channel germanium devices of Fig. 3.3.12 have a higher mobility than the other devices measured. The P-channel silicon devices in Fig. 3.3.13 have the lowest mobility at a given doping level.

In the double gate, double diffused devices, (Fig. 3.3.13), the value of the doping density throughout the channel is usually at least an order of magnitude lower than the base region of an equivalent double diffused bipolar transistor (40). A typical channel doping profile for this type of structure might then appear as illustrated in Fig. 3.4.1 with a peak doping value of the order of $10^{16}/cm^3$. This corresponds to the considerably idealized profile (Fig. 2.3.9) used in the theory of Section 2.3.2.

It was found in Section 2.3.2 (equation 2.3.48) that for this type of structure with both gates tied together, the slope of the charge versus conductance plot depends on the depletion layer widths in the channel, and on the mobility at each depletion layer boundary of the channel. It is extremely unlikely in the practical profile of Fig. 2.3.9 that the depletion layer widths in the channel due to each gate junction should maintain a constant ratio to each other for any significant range

of injected gate charge. It is therefore reasonable to assume that the constant slope in the straight line region for each of these devices in Fig. 3.3.13 is a result of essentially constant and equal mobility at each channel- depletion layer boundary.

The most likely condition for this to occur is where the doping density at each depletion layer boundary in the channel is at or below the value corresponding to essentially constant and maximum mobility ($\approx 10^{15}/cm^3$). It is therefore assumed that in this constant slope region, the depletion layer in the channel due to the upper gate, has "gone down the hill" and reached the point where the doping density is below about $10^{15}/cm^3$. This situation is also illustrated in Fig. 3.4.1.

If the channel doping profile had a rather wide flat-topped peak, it is possible that both depletion layer boundaries could be in a region of almost constant doping density, and therefore constant and equal mobility over a region of injected gate charge. This situation is not normally produced by the double diffusion process, however.

The channel doping profile for the diffused epitaxial channel devices (Fig. 3.3.14) is similar to the illustration in Fig. 3.4.2. Before the upper gate diffusion, the epitaxial layer should have a reasonably constant doping level, depending on its thickness, and on the amount of out-diffusion which has occured during epitaxial layer growth. The upper gate diffusion is normally of relatively high concentration, but shallow in depth. As previously mentioned, this diffusion fixes the channel height, but the channel resistivity is better controlled by the properties of the epitaxial layer. Thus, the central channel region can be expected to remain with a fairly constant doping density.

It is expected therefore that the straight line portions of the plots in Fig. 3.3.14 are as a result of constant and equal mobility where the channel depletion layer boundaries from both gates are in the relatively flat top of the doping density profile. The mobility would then be determined by the doping density in this region. Depending on the device design, the mobility in this region may be somewhat less than the maximum possible value (or low doping value).

Before proceeding to the discussion of the low gate charge region, and the high gate charge region of this type of plot, it should be noted that the slope of the straight line region can be affected by parasitic gate charge under certain circumstances. By parasitic gate charge is meant any charge injected into the gate which does not directly affect the resistance of the active channel. If over a region, the amount of parasitic charge were to be maintained in fixed relationship to the amount of active gate charge injected, this would appear on the gate charge versus channel conductance relationship as a straight line with a larger slope (i.e. a larger effective L^2/μ ratio), than would be expected on the basis of the channel length and mobility alone. This situation could occur in the alloyed gate devices with the structure shown in Fig. 3.3.1 , for example, if the gate junction were made to extend significantly beyond the extent of the etched well.

3.4.1.2 Low Gate Charge High Channel Conductance Region

The region of the gate charge versus channel conductance relationships containing the deviation from constant slope at low values of injected gate charge will now be considered. Since, in general, a straight line region indicating true charge control operation occurs at higher levels of gate charge in all the devices measured, it must be assumed that one or more of the necessary requirements are not being met in this lower region. In other words, the deviations from constant slope must be caused by one or more of the following : variation in mobility, variation in channel length, significant contact or parasitic bulk resistance at either end of the channel, or parasitic gate charge. Note that although parasitic bulk resistance at the ends of the channel can cause a non-linear charge versus conductance plot for the overall device, it does not necessarily mean that the gate charge versus channel conductance plot for the intrinsic channel is non-linear.

As previously noted, device TIX883-1 (Fig. 3.3.12) shows no lower region deviation. Device TIX881-2 , on the other hand, shows essentially a straight line in this region , whose slope is slightly larger than in the mid-region. It is possible that the mobility in this region is lower due to higher doping density than in the mid-region, but this is not normally expected with an alloyed structure, Parasitic bulk resistance alone does not explain the situation observed. If it were due to parasitic resistance alone, it would have to be assumed that the constant Q_{gg} versus G_{ch} slope in the mid-region resulted when the channel resistance became so large as to make the parasitic bulk resistance negligible in comparison with it. Further, it would have to be

assumed that the difference between the actual measured channel conductance with $Q_{gg} = 0$, and the value obtained by extrapolating the mid-region slope to the G_{ch} axis is due to parasitic resistance. The resultant value of parasitic resistance predicted, however, is too large to have a negligible effect on the total measured G_{ch} at the start of the mid-region slope as gate charge is increased from zero, and the channel resistance is increased from its equilibrium value.

A more likely explanation is that the gate extends significantly beyond the bounds of the etched well, forming in this device a parasitic FET in series with the main channel. The parasitic FET would be expected to have a very short channel length , but a somewhat larger channel height than the main channel. With this situation, the parasitic charge causes some modulation of overall conductance, but its effect very quickly becomes negligible in comparison with the main channel due to its much smaller height. It is to be expected that, although conductance modulation in the parasitic FET will become insignificant at higher levels of total device gate charge, parasitic charge will still be consumed in a fairly constant ratio to the active gate charge, allowing a constant overall Q_{gg} versus G_{ch} slope in the mid-region.

It is also quite possible that in this particular device, the dimensions of the annular structure may be such that significant contribution to the deviation from the mid-region slope results from the fact that the structure is not truly one-dimensional. Just as for the wedge-shaped channel considered in Chapter 2, Section 2.5, it could be expected that an increase in the effective L^2/μ ratio would result from such a situation. With the application of gate voltage, the

channel depletion layer is widened so that the channel height is decreased. The result is that the channel tends to become more truly one-dimensional, and eventually in the mid-region, the contribution from this cause becomes negligible.

The low region of the Q_{gg} versus G_{ch} relationship for the double diffused (Fig. 3.3.13) and diffused epitaxial devices (Fig. 3.3.14) tends to be large in extent. Since both types are structurally similar (see Figures 3.3.2 and 3.3.3), they will be discussed together. The common aspect of their structures, which is very important in this region, is that in both types of devices the lower gate junction is considerably larger than the active channel length. The active channel length in these devices is essentially defined by the length of the depletion layer boundary between the channel and upper gate. This situation is illustrated in Fig. 3.4.3. A considerable and varying amount of parasitic charge can thus be contained in this excess depletion layer length. Undoubtedly, a considerable amount of parasitic FET action also takes place at low gate charge levels beyond either end of the active channel as a result.

A similar situation exists along the sides of the upper gate depletion layer. The whole situation is of course worse if the channel is located relatively deeply below the surface of the semiconductor. In this case, deeper diffusions are required, resulting in a longer parasitic gate length.

Considerable mobility variations undoubtedly occur in this lower region also in both device types, but particularly so in the double diffused devices. Normally, special low resistance diffusions are made in the source and drain contact regions. Some contribution from parasitic

bulk resistance effects is still possible in this region, however, as these devices (particularly the 2N3824's) have a relatively low channel resistance under zero bias conditions.

3.4.1.3 High Gate Charge Low Channel Conductance Region

All devices exhibit a deviation from the constant slope at high gate charge levels as the zero G_{ch} axis is approached. This deviation, in the plots for the epitaxial channel devices, 2N3824's (Fig.3.3.14), is relatively small in size and extent on the scale shown, but nevertheless occurs at very small G_{ch} values. Other devices such as TIX883-1 and 2N2498-3 show quite a considerable deviation from constant slope in this region. This region most certainly affects the pinch-off characteristics of an FET, causing in most cases, a gradual rather than an abrupt change in channel resistance as pinch-off is approached.

Each of these devices has been checked to ensure that a very high source drain resistance is achieved for large values of reverse gate voltage. It can therefore be concluded that there is no significant contribution to the deviations in this region by low resistance leakage paths in parallel with the channel.

It is expected that one of the causes of the deviation here is a decrease in the average mobility of the carriers that occurs when the channel height becomes very small. In addition, it is probably no longer valid to assume that complete depletion exists in the channel depletion layer. Thus the channel dimensions become ill-defined, and parts of the channel region itself become gradually depleted with a consequent decrease in average carrier mobility.

In this region it is also expected that depletion layer "spillage"

takes place. By this it is meant that the depletion layer extends progressively outwards beyond the ends of the active channel as the channel region becomes more and more depleted. This maintains charge equality in the depletion layers on both sides of the gate, but it increases the effective length of the channel in a manner similar to that illustrated in Fig. 3.4.3, and thus causes the slope of the Q_{gg} versus G_{ch} relationships to increase.

In the alloyed germanium devices, it is also possible that surface imperfections in the etched well are involved (see Fig. 3.3.1). At high gate charge levels, as the channel narrows, any abrasions, roughness, or contamination as a result of the etching process, on what is one side of the channel, would have a progressively greater effect on the Q_{gg} versus G_{ch} relationship. Such imperfections could be expected to decrease the average majority carrier mobility, and thus increase the L^2/μ ratio.

3.4.2 Gate Charge Versus Drain Current Relationships

The results of the gate charge versus drain current measurements presented in Section 3.3.2 in Figures 3.3.17 through 3.3.20, are discussed in this section. For clarity in presentation, as previously noted, some of the graphs in Figures 3.3.17, 3.3.18, and 3.3.19 have a shifted zero line as indicated. Note, however, that the zero line is not shifted for any of the graphs in Fig. 3.3.20.

Each figure shows a family of gate charge (Q_{gg}) versus drain current (I_d) relationships made on a particular FET at various values of drain voltage (V_d). Each relationship in these figures shows a considerable straight line or mid-region with deviations appearing in

general in the upper and lower gate charge regions just as with the gate charge versus channel conductance relationships for zero drain voltage previously discussed. Again, both upper and lower region deviations need not necessarily be present on every graph.

Equation 2.3.19 predicts a family of straight lines , each with slope r_d (= $L^2/\mu V_d$), but was derived only on the basis of an unpinched-off channel. Gate charge versus drain current relationships were obtained for these devices for a wide range of applied drain voltages both above and below the pinch-off voltage. The Q_{gg} versus I_d relationships for drain voltage values much below the pinch-off voltage V_{po}, were obtained in order to study the applicability of the basic theory under conditions such that the channel shape departs significantly from the conditions of uniform channel height applying to the Q_{gg} versus G_{ch} relationships discussed in Section 3.4.1. The Q_{gg} versus I_d relationships for large drain voltage values are intended to investigate the extension of the theory of charge control operation into the pinch-off region and beyond.

Just as in Section 3.4.1, it is convenient to study the "family" of Q_{gg} versus I_d relationships for each device according to the region of operation. Thus the mid-region or constant slope region of each Q_{gg} versus I_d relationship in the family is discussed in Section 3.4.2.1. Similarly, the low gate charge or high drain current region deviation is considered in Section 3.4.2.3. Finally in Section 3.4.2.4, a discussion of the operating mechanisms within the FET is given, based on the charge control results, and their discussion in Sections 3.4.2.1 through 3.4.2.3.

3.4.2.1 Mid-Region

As previously noted in Section 3.2.2, it can be seen from Figures 3.3.17 through 3.3.20 that the entire Q_{gg} versus I_d relationship including the mid- or constant slope region for very low values of drain voltage, is very similar in shape to the corresponding Q_{gg} versus G_{ch} relationship for each device shown in Figures 3.3.12 through 3.3.14. This is perhaps not unexpected, since a very small value of drain voltage with respect to the pinch-off voltage V_{po} , can be expected to have a negligible effect on the conditions in the channel. Thus the channel height is essentially uniform along its length just as it is for the Q_{gg} versus G_{ch} measurement.

What is perhaps surprising is the form of the curves and the extent of the straight line region of each Q_{gg} versus I_d relationship at large values of drain voltage. For all these devices, the extent of the constant slope region of the Q_{gg} versus I_d relationship is increased at higher values of drain voltage. For several devices. notably 2N2498-3, 2N2498-5, and 2N3824-3 in Figures 3.3.18 through 3.3.20, the constant slope region extends right down to the I_d axis. This point will be taken up later in this sub-section.

A further important feature of each family of Q_{gg} versus I_d relationships is that the slope of each plot in the mid-region decreases with increasing values of drain voltage. In addition, the slope of each plot appears to saturate and remain essentially constant beyond some applied drain voltage irrespective of further increases in drain voltage. For devices TIX881-2, 2N2498-3 and 2N2498-5 (Figures 3.3.17, 3.3.18, and 3.3.19 respectively), the plots at high drain voltages are essentially

identical, and would normally fall on top of each other had their "zero" position not been shifted vertically to avoid confusion.

The basic charge control equation (equation 2.3.19) derived in Chapter 2, Section 2.3.1, is presented here for convenience. Thus

$$I_d = \frac{Q_{ch}}{\tau_d} = \frac{(Q_o - Q_{gd} - Q_{gg})}{\tau_d} \qquad (3.4.1)$$

where

$$\tau_d = \frac{L^2}{\mu V_d} \qquad (3.4.2)$$

As noted, however, equation 3.4.1 was derived on the basis of an open or unpinched-off channel. It might therefore be expected on the basis of Shockley's theory (8) that equation 3.4.1 would no longer be valid when the combination of applied gate voltage and drain voltage is such as to produce pinch-off at the drain end of the channel, i.e., when

$$|V_g| + |V_d| \geq V_{po} \qquad (3.4.3)$$

In terms of the Q_{gg} versus I_d results measured at constant applied drain voltage V_d , it might be expected that at some point on each Q_{gg} versus I_d relationship, a value of gate voltage would be obtained at which the situation represented by equation 3.4.3 occurs. Further, this situation should occur at progressively lower values of gate voltage, on the Q_{gg} versus I_d relationships as drain voltage is increased, until the applied drain voltage equals V_{po} when according to equation 3.4.3, no increase in gate voltage (or corresponding gate charge) is allowed.

If at a point on any Q_{gg} versus I_d relationship , equation 3.4.1 were violated, it would be reasonable to assume that the slope of the Q_{gg} versus I_d relationship (i.e. τ_d) would begin to deviate from the

straight line. Deviations from the straight line slope in the mid-region do in general occur (see Sections 3.4.2.2 and 3.4.2.3), but it can quite readily be seen that these deviations do not appear on each plot in the Q_{gg} versus I_d family according to the situation expressed by equation 3.4.3.

It is of course possible that a complicated interaction of the parameters involved in equation 3.4.1 occurs beyond the situation represented by equation 3.4.3, such that the straight line slope of each Q_{gg} versus I_d plot is maintained unchanged at the value which existed below this point. It is extremely unlikely, however, that such a situation could be the case with all the different FET's measured representing devices with completely different structures, different junction voltage laws, different channel doping density profiles, and with one- and two-gate junctions.

Thus, in general, except for the deviations to be discussed later, and which it must be recalled also appeared in the Q_{gg} versus G_{ch} relationships measured for these devices, each Q_{gg} versus I_d relationship appears as a straight line over most of its length with a constant slope which decreases with increasing drain voltage, just as predicted by equations 3.4.1 and 3.4.2, to some limiting drain voltage. It therefore appears that the situation expressed by equation 3.4.3 from the basic Shockley theory, does not affect the charge control relationships, or does not apply. This situation will be discussed further in Section 3.4.2.4.

In view of the above discussion in terms of the measured charge control results, it would appear that equations 3.4.1 and 3.4.2 correctly represent device operation essentially irrespective of applied gate voltage

or injected gate charge, for values of applied drain voltage below a "saturation voltage". Thus it can be postulated that the applied drain voltage (V_d) is essentially equal to the effective voltage drop (V_{ch}) along the length of the channel for drain voltages below the saturation voltage. Further, for drain voltages above the saturation voltage, the effective channel voltage (V_{ch}) remains essentially constant and independent of the applied drain voltage.

Since a straight line relationship is observed in general between Q_{gg} and I_d for a particular drain voltage regardless of whether this voltage is above or below the saturation voltage, it would appear, firstly, that the effective L^2/μ ratio is constant with increasing gate charge (or reverse bias gate voltage). Secondly, it appears that the injected gate charge is all being effectively utilized to control the drain current in the straight line or constant τ_d region. In addition, since the Q_{gg} versus I_d plots are essentially coincident beyond the saturation voltage on the drain, as previously noted, the Q_{gd} term in the channel from equation 3.4.1. must be affected only by V_{ch}. As subsequently discussed, any excess drain voltage beyond saturation must produce excess junction reverse bias voltage and therefore excess depletion layer charge, but not necessarily in the active channel region. In general, for drain voltages beyond saturation, for a given value of gate charge, it appears as though V_{ch}, Q_{gd}, and channel conditions generally, remain essentially unaffected.

In connection with the application of equation 3.4.1, one further aspect is clearly illustrated by these Q_{gg} versus I_d results - namely, the variation of the Q_{gd} term with the drain voltage. In Fig. 3.3.20

for 2N3824-3, for example, it can be seen that as V_d is increased from 0.5 volts to 6.0 volts, the amount of injected gate charge required to produce pinch-off decreases from about 19.8 pico-coulombs to about 11.3 pico-coulombs (from straight line projection) ; thus indicating that Q_{gd} has increased by the difference.

In order to study the charge control results of Figures 3.3.17 through 3.3.20 in more detail, the information for each family of Q_{gg} versus I_d relationships for each device has been summarized firstly in Fig. 3.4.4. Results for device TIX883-1 are also shown for comparison. This figure shows a plot of τ_d (obtained from the mid-region of each Q_{gg} versus I_d relationship) for each device plotted as a function of applied drain voltage. This figure clearly shows the degree of saturation of τ_d as a function of drain voltage. It can be seen that for large values of drain voltage, τ_d is constant for all practical purposes. In fact τ_d decreases very slightly with large changes in drain voltage beyond saturation. The difference in the saturated value of τ_d for each of these devices is also clearly illustrated, varying from 28.5 nano-seconds for TIX881-2, to 1.75 nano-seconds for 2N3824-3.

Fig. 3.4.5 shows plots of effective L^2/μ ratio for each device plotted also as a function of drain voltage. These L^2/μ values were obtained from the mid-region slopes of the Q_{gg} versus I_d relationships for each device from equation 3.4.2 as follows:

$$L^2/\mu = \tau_d V_d \qquad (3.4.4)$$

Equation 3.4.4 is strictly valid in accordance with the previous discussion so long as the applied drain voltage equals the effective

channel voltage (i.e., below saturation). The plots of r_d versus V_d in Fig. 3.4.4 indicate that the onset of saturation is a gradual process in these devices, and therefore a saturation voltage cannot strictly be specified. The L^2/μ ratios are therefore only plotted for low values of drain voltage. The L^2/μ ratio obtained from the mid-region of the Q_{gg} versus G_{ch} relationship for each device from Figures 3.3.12 through 3.3.14 is also shown for comparison.

Fig. 3.4.5 serves to show the character and amount of variation in L^2/μ for each device. The L^2/μ ratio is by no means constant for these devices, but in general, the variation with drain voltage is perhaps not as drastic as might be expected. In the case of device TIX883-1, for example, there is little change in L^2/μ as drain voltage is first applied . In other devices, such as 2N2498-5 and 2N3824-3, the L^2/μ ratio increases as the applied drain voltage is increased right from zero.

In practical devices, there are undoubtedly several reasons for the observed increase in the L^2/μ ratio with increasing drain voltage. One important cause of the increase is believed to be due to a "pulling" of the drain end of depletion layer(s) in the channel toward the drain as drain voltage is increased. The full drain voltage is applied to the drain end of the gate to channel junction , causing a larger depletion region at this end of the channel. Particularly in the diffused gate junction devices (see also Fig. 3.4.3), the effective channel length is increased as the depletion region extends outwards toward the drain, as well as into the channel. Since the square of the channel length is involved in the L^2/μ ratio, a small change in channel length can produce

a significant change in L^2/μ. Certainly, the significance of changes in channel length depend on the structure of the device, and on the channel length in particular.

As noted earlier in connection with Fig. 3.4.4, the onset of τ_d saturation with drain voltage is a rather gradual process. It is therefore probable that as drain voltage is increased, the effective channel voltage V_{ch}, which actually produces the slope τ_d, starts to become a decreasing proportion of V_d at relatively low values of applied drain voltage. Eventually the saturation process, which is discussed in Section 3.4.2.4. results in a channel voltage which is essentially independent of applied drain voltage. The important point, however, is that the use of V_d in equation 3.4.4 may start to overestimate the effective L^2/μ ratio for values of drain voltage considerably below the point at which essentially complete saturation occurs. It is highly probable, therefore, that Fig. 3.4.5 presents a considerable overestimate of the actual amount of variation which occurs in the L^2/μ ratio with effective channel voltage for these devices.

In Chapter 2, Section 2.5, it was shown that for an idealized wedge-shaped channel, the effective L^2/μ ratio of such a channel depended on the angle of the wedge, or on the P/L ratio. Specifically, it was shown that the effective L^2/μ ratio was found to increase for large wedge angles as the P/L ratio approached 1. Although in the practical device, the channel is not truly wedge-shaped under conditions of applied drain voltage, the situation is analogous. The L^2/μ ratios in question, however, have all been obtained from the constant slope or mid-region, of the Q_{gg} versus I_d relationship. It is believed that such channel shape

effects are not significant in this mid-region, otherwise a constant Q_{gg} versus I_d relationship would not be observed at a particular value of V_d. It is therefore believed that channel shape effects in these devices are not a significant factor in the increase in the L^2/μ ratio with increasing drain voltage in Fig. 3.4.5.

It was noted earlier in this section that the Q_{gg} versus I_d relationships for these devices in Figures 3.3.17 through 3.3.20, in general have an extended constant slope or mid-region at the larger values of drain voltage, as compared with the mid-region of the Q_{gg} versus I_d relationships at low drain voltages, or of the corresponding Q_{gg} versus G_{ch} relationships in Figures 3.3.12 through 3.3.14. The main reasons for this behaviour will now be discussed.

Considered first is device TIX881-2 in Fig. 3.3.17, whose structure is illustrated in Fig. 3.3.1. The application of drain voltage removes mobile charge from the channel (i.e., Q_{gd}), and thus by itself increases the channel resistance. By so doing, the effects of any bulk parasitic source and drain resistances, as well as any parasitic FET action beyond the ends of the active channel as discussed previously in Section 3.4.1.2, have been made less significant. Thus the onset of the mid-region can be expected to occur at lower values of gate charge as drain voltage is increased. One further aspect, concerning this particular structure, is that the application of drain to source voltage could conceivably tend to concentrate the current flow lines on the side of the source and drain contacts away from the gate side of the structure, and thus tend to make the overall channel conditions more closely one-dimensional.

The diffused gate devices, 2N2498-3, 2N2498-5, and 2N3824-3, whose Q_{gg} versus I_d relationships are shown in Figures 3.3.18 through 3.3.20, and whose structures are illustrated in Figures 3.3.2 and 3.3.3, will now be considered. With these structures, the application of drain to source voltage can be expected to increase the channel resistance by the removal of majority carrier charge, and thus make parasitic effects less significant as noted above for device TIX881-2.

In addition, with these structures, it is believed that drain voltage has two effects on the channel. Firstly, by the removal of charge from the channel (i.e., increasing the size of the channel depletion layer), the channel height is reduced progressively from the source to the drain end of the channel. Thus the mean height of the channel is reduced. As discussed in Section 3.4.1.1, this restricts the active channel more towards the center, for these double gate devices, similar to the situation illustrated in Fig. 3.4.3, and tends to place channel operation into a region of either low doping density or constant doping density as illustrated in Figures 3.4.1 and 3.4.2, which corresponds to an operating region with constant channel mobility. Hence the mid-region can be considerably extended at the larger values of drain voltage.

The second effect of drain voltage referred to in the preceding paragraph is that it appears, on the basis of the discussion of the Q_{gg} versus I_d results earlier in this section, that drain voltage (or channel voltage) has a very strong effect on conditions at the drain end of the channel. Thus it may in fact tend to better define the channel length for each Q_{gg} versus I_d relationship at the larger values of drain voltage. At zero or low values of drain voltage, however, as

was noted in connection with the illustration in Fig. 3.4.3, some increase in the L^2/μ ratio in these devices (depending on the channel length) may result from the depletion layer being extended along the channel in the low gate charge region as gate voltage is first applied.

Before proceeding specifically to a discussion of the deviations from the mid-region of constant slope of the Q_{gg} versus I_d relationships, it can be concluded on the basis of these charge control results and the discussion in this section, that the charge control approach adequately applies to field-effect transistor operation over a wide range of operating conditions, so long as the effective channel voltage V_{ch}, and not always the applied drain voltage, is assumed to apply to the device channel. Further, the assumption made in Chapter 2, Section 2.3.1, neglecting the effects of channel shape distortion, has been shown to be valid over a wide range of operating conditions. The mechanism producing saturation in the slope of these relationships with applied drain voltage is considered in Section 3.4.2.4.

3.4.2.2 Low Gate Charge High Drain Current Region

This section is concerned specifically with the deviations from the straight line slope of the mid-region, observed in the Q_{gg} versus I_d relationships for the devices in Figures 3.3.17 through 3.3.20 in the low gate charge or high drain current region.

The study of the deviations in this region from the mid-region slope has already been well introduced near the end of the preceding section in the discussion on the behaviour of the mid-region with changes in drain voltage. It can be expected that the causes of the deviations in these plots at low values of drain voltage are primarily just those

which caused the deviations in the Q_{gg} versus G_{ch} relationships as discussed in Section 3.4.1.2. Under conditions of very low drain voltage, the channel shape can be expected to remain essentially uniform as previously discussed, and hence the conditions in the channel are essentially the same as those applying for the Q_{gg} versus G_{ch} relationships.

The deviation from constant slope in the low gate charge region of the Q_{gg} versus I_d relationships for device TIX881-2 in Fig. 3.3.17 does not disappear entirely at large values of drain voltage as was seen for the diffused gate devices. For this device, it is possible that the change in channel resistance as a result of the application of drain voltage is not sufficient to completely swamp out parasitic effects. It is also probable that some non-one-dimensional effects are present, and that, at the larger drain voltages especially, the effective L^2/μ ratio (and thus τ_d) is increased as a result of the wedge-shaped channel effects as discussed in Chapter 2, Section 2.5.

3.4.2.3 High Gate Charge Low Drain Current Region

The deviations from the straight line slopes of the Q_{gg} versus I_d relationships in Figures 3.3.17 through 3.3.20 in the high gate charge or low drain current region are considered here. The character and amount of the deviation observed on each Q_{gg} versus I_d relationship varies considerably from device to device, but generally increases somewhat at the larger values of drain voltage.

In this high gate charge region under conditions of applied drain voltage, it can be expected that the conditions noted in Section 3.4.1.3 in the discussion of the high gate charge region of the Q_{gg} versus G_{ch} relationships (eg. depletion layer spillage), also apply. The situation

situation is further complicated by the flow of current and the existence of fields along the channel a result of the applied drain voltage.

In this region, it is quite probable that the large gate voltages involved (being comparable to or greater than the applied drain voltage), begin to exert a greater influence on channel conditions, particularly at the drain end. The result could well be that the effective channel voltage V_{ch} is reduced, with the consequent increase in τ_d. Further clarification of the factors involved in this region will result from the discussion of device operation in Section 3.4.2.4.

3.4.2.4 Discussion of Device Operation

It is the object in this section to present a discussion of the important operating mechanisms within the FET on the basis of the measured charge control characteristics, and their interpretations in the earlier parts of Section 3.4.2. Specifically, it is intended to consider the validity of the basic Shockley criterion expressed by equation 3.4.3, and the mechanism which produces saturation in the slope of the Q_{gg} versus I_d relationships at large values of applied drain voltage.

Shockley Criterion

From the basic Shockley theory presented in Chapter 2, Section 2.2, the pinch-off voltage V_{po} was defined in connection with equation 2.2.7 to be the gate to source voltage required to reduce the channel height to zero under conditions of zero applied drain voltage. This corresponds to the situation illustrated in 3.4.6a where the depletion layer just fills the whole channel. The single gate structure with an N-type channel has been chosen here for simplicity in the discussion, but the situation is also analogous for the double gate structure. Strictly,

Shockley assumed that no voltage drop appears across the depletion layer on the gate side of the junction, but it is immaterial to this discussion so long as the chosen reference gate voltage V_{po} completely depletes the channel.

If the applied gate voltage were increased beyond V_{po}, the channel depletion layer would be forced to spread outwards toward the source and drain contacts to maintain an equal amount of depletion layer charge on both sides of the gate junction (thus satisfying Gauss's Theorem). Further, the potential along the side of the channel away from the junction (eg. point A in Fig. 3.4.6b) would be forced to drop (thus satisfying Poisson's equation).

The above pinch-off situation will now be considered under conditions of applied drain voltage. Complete depletion in the space charge region will be specifically assumed, so that no interference due to the flow of majority carrier charges is assumed to exist. This corresponds essentially to the assumption by Shockley (8) in his calculations beyond pinch-off where he assumed that all the current was concentrated in the y=0 plane, and that the mobile charge carriers had negligible effect on the depletion region potentials. Fig. 3.4.6c illustrates a possible pinch-off situation just having been reached at the drain end of the channel under the above assumptions for some value of applied gate and drain voltages. Thus from the Shockley criterion of equation 3.4.3, it is assumed at the drain end of the channel that

$$|V_d| + |V_g| = V_{po} \qquad (3.4.5)$$

If now the applied gate voltage were increased while maintaining

constant applied drain voltage, it could be expected under the above assumptions that the increased gate voltage would not only expand the pinched-off region, possibly toward the drain somewhat, as well as into the channel, but more importantly, it would force a decrease in the voltage V_{ch} at the drain end of the channel to maintain the equality of equation 3.4.5 at the pinch-off point. This situation is illustrated in Fig. 3.4.6d. The results of the gate charge versus drain current measurements, however, indicate that the channel voltage V_{ch} must remain essentially constant over a wide range of values of gate voltage (or gate charge), in order to produce the observed straight line relationships between gate charge and drain current. It therefore appears that the assumptions made above assuming complete depletion in the space charge region, and neglecting the effects of the majority carrier current charges are not valid.

The situation at the drain end of the channel which actually exists when it is "pinched-off" is extremely complex. On the basis of the charge control measurements, and the examples considered in Figures 3.4.6b and 3.4.6d, it appears that the device behaviour, however, is vitally affected by the majority carrier charges in this pinch-off region.

In order to investigate this further, let it be specifically assumed that the source and drain are always effectively "resistively coupled" together (so long as drain current flows), due to the presence of significant majority carrier charge particles, either in the space charge region or in a narrow channel, or both, at the end of the main channel. The conditions applying to Figures 3.4.6c and 3.4.6d are then considerably altered, and the effects of the gate and drain voltages are quite different.

Under the assumed conditions of significant majority carrier charge in this pinch-off region, the voltage conditions applying to the illustration in Figures 3.4.6c and 3.4.6d could produce the results illustrated in Figures 3.4.6e and 3.4.6f respectively. In these cases, it can be seen that the pinch-off situation might be less distinct, but that the voltage across the active channel length is determined primarily by the applied drain voltage and the drop across the region coupling the channel to the drain contact. What also is very important, is that the channel voltage is no longer under the direct control of the applied gate voltage as was required by the conditions applying to Figures 3.4.6c and 3.4.6d. Hence the Shockley criterion of equation 3.4.3 is no longer applicable under these assumptions.

In this connection, it is to be noted that although the applied voltages are assumed to be the same in Figures 3.4.6d and 3.4.6f, the presence of the majority carrier charge in what was formerly assumed to be a completely depleted region, requires that the channel depletion layer be expanded elsewhere to maintain the same amount of uncovered charge in the depletion layers on both sides of the junction. It therefore follows that the channel conditions are somewhat different in these two figures.

As the gate voltage is increased at constant drain voltage (i.e., going from Fig. 3.4.6e to Fig. 3.4.6f), the drain current is reduced as a result of the expanding depletion layer in the channel, but it would appear that conditions at the drain end of the channel are affected very little except for a reduction in the amount of majority carrier charge in the pinch-off space charge region. Further, it can be seen that under

conditions of a larger drain voltage (below saturation), the drain current, and hence the amount of majority carrier charge in this pinch-off region is increased. This must be compensated for by an expansion of the channel depletion layer elsewhere, in addition to that which normally occurs as a result of the greater reverse bias effect of the increased drain voltage. Thus there is a tendency for the current to saturate.

From the above discussion, it appears that the presence of significant majority carrier charge in the space charge region beyond the end of the channel accounts for the straight line Q_{gg} versus I_d relationships observed at a given value of applied drain voltage. Specifically, it accounts for the fact that the voltage across the active channel remains essentially constant over a wide range of applied gate voltages, and hence for the fact that the Shockley criterion (equation 3.4.3) is not really meaningful or applicable to these devices in the straight line regions of the Q_{gg} versus I_d relationships. Note that in the high gate charge or low drain current region of these relationships, the drain current becomes small as does the majority carrier charge in the space charge region. Thus complete depletion in the space charge region is more closely approached, so that the Shockley criterion may begin to have an effect in this region of the Q_{gg} versus I_d relationships. The result of such an effect, as noted in Section 3.4.2.3, is that the gate voltage forces a decrease in the effective channel voltage and hence an increase in the slope r_d.

Saturation

The specific effects within the FET producing saturation in the

slope of the Q_{gg} versus I_d relationships with applied drain voltage will now be considered. As previously noted in connection with the plots of τ_d versus drain voltage in Fig. 3.4.4, saturation in these devices starts as a rather gradual process. Once saturation is complete, however, only a very small change in the value of τ_d is observed for large changes in applied drain voltage for the devices measured. On this basis, it was suggested in earlier discussions that the effective channel voltage V_{ch}, and channel conditions generally, remained essentially constant for values of applied drain voltage beyond saturation. The difference between V_d and V_{ch} would then be dropped across the depleted region beyond the end of the channel, which must increase in size as a result of the increased applied drain voltage.

There are basically two schools of thought on the pinch-off or saturation process. One (59) is that the channel never really closes down, but that the current flows through a narrow channel between the depletion layer and side of the channel, or between the two depletion layers in a double gate device. The other (8,37) is that the drain end of the channel can be assumed to be pinched-off (i.e., depleted), but that the majority carrier current charges are injected into the depleted region and carried through to the drain contact by the drain field. In both cases, it is assumed that with a constant voltage on the gate (eg. zero), the effective channel voltage and hence the drain current remain essentially unchanged as the applied drain voltage is increased, with any excess voltage being dropped across a very high resistance region in the first case, and across a practically depleted region in the other.

Essentially, as saturation starts to become complete with increasing drain voltage, with gate voltage equal to zero for example, a near perfect "balance" is set up between the opposing tendencies involved. The increasing drain voltage tends to increase the effective channel voltage V_{ch} and thus the drain current. At the same time, it tends to increase the size of the depletion region both in the active channel and outwards toward the drain contact. This tends to oppose the increase in the drain current, and to limit the effective channel voltage as a result of a larger voltage drop across the extended depleted region beyond the end of the channel.

As discussed in connection with the Shockley criterion, the presence of significant majority carrier charge can be expected to cause an ill-defined channel depletion layer boundary at the drain end of the channel, and also to violate the assumption that the depleted region beyond the channel can be considered to be completely depleted. The shape of the depletion layer must then be affected elsewhere in order to maintain equality in the amount of depletion layer charge on both sides of the gate junction(s). Thus the conditions at which "balance" or saturation occurs will also be affected, and the effective channel voltage V_{ch} (sat) in saturation, will not in general be equal to V_{po} as defined at zero drain voltage by Fig. 3.4.6a.

Saturation for two values of applied drain voltage is illustrated in Figures 3.4.7a and 3.4.7b. For large applied drain voltages beyond saturation (as in Fig. 3.4.7b), the voltage drop across the extended depleted region beyond the channel, which must satisfy Poisson's equation, may produce very large fields in this region, such that the

majority carriers flowing through it may become velocity limited. On the basis of the essentially constant values of τ_d observed for these devices in saturation, it appears that the main effects of this region are to "collect" the charges flowing from the channel, and to drop the excess applied drain voltage beyond V_{ch} (sat), without appreciably changing conditions in the active channel.

The description of device operation in this section, based on the results of the charge control measurements, involves important differences from Shockley's ideal "gradual case" theory. It can be seen, however, that this description is not incompatible with the general form of the current-voltage characteristics predicted on the basis of the "gradual case" theory (see Fig. 2.2.2), or observed in practical devices. Thus the tendency of the drain current to saturate with increasing drain voltage for a given gate voltage has been noted in this description.

In practical devices, however, this saturation is generally far from being complete anywhere on the current-voltage characteristics. It is therefore extremely difficult to determine the "pinch-off" voltage from such gradually changing characteristics. Further, the difference between V_{po} at zero drain voltage (Fig. 3.4.6a), and V_{ch}(sat), may be small in some devices. Thus Dacey and Ross (9) concluded that, for their particular structures, the "pinch-off" voltage obtained from the current-voltage characteristics at zero gate voltage was in fair agreement with the predicted value of V_{po} .

3.5 Discussion of Results on Insulated Gate Field-Effect Transistors

In this section, the results of the charge control measurements presented in Section 3.3.2 on MOST 6 and MOST D will be discussed and interpreted in a manner similar to that of Section 3.4 for FET's. Specifically , it is intended to investigate the validity and applicability of the charge control theory, developed and presented for MOST's in Chapter 2, Section 2.4, over a wide range of operating conditions.

3.5.1 Gate Charge Versus Channel Conductance Relationship

3.5.1.1 Mid-Region

As discussed in Section 3.4.1.1 for FET's, it can be assumed in this mid-region or constant slope region of the gate charge versus channel conductance relationships (in Figures 3.3.15 and 3.3.16), that true charge control operation exists. Therefore it can be concluded that in this region, equation 2.4.3 applies to these devices, with a constant value of L^2/μ ratio. Further, it can be concluded that the assumptions made in Section 2.4 (i.e., that the charge in the surface traps Q_{st} is fixed, and that the uncovered substrate charge Q_s is independent of gate voltage), are both valid in this mid-region of operation under conditions of zero applied drain voltage.

On the basis of the observed constant L^2/μ ratio in this region, the channel length L, and mobility μ of the carriers in the surface channel must also be constant. The slope of the Q_{gg} versus G_{ch} relationship for each of these MOST's is at its minimum value in this region (just as for the FET's), corresponding to the maximum change in channel conductance per unit of gate charge. The L^2/μ ratios in this region are found from

Figures 3.3.15 and 3.3.16 to be 8.75×10^{-9} volt-sec for MOST D and 15.82×10^{-9} volt-sec for MOST 6.

It has been noted (60) that the mobility applying to the carriers in a surface channel is less than that applying to majority carrier flow in the bulk of the semiconductor material. With a knowledge of the channel dimensions, the slope of the gate charge versus channel conductance relationship in this mid-region thus provides a method for studying the average mobility of the carriers in such a surface channel. Note, however, that an over-estimate of the true L^2/μ ratio could be obtained in a given device if the gate contact significantly over-lapped the diffused regions for the source and drain contacts.

Although the range covered by the MOST D graph is limited, the slope of this graph also increases at high values of Q_{gg} such that effective saturation eventually occurs, and little or no increase in G_{ch} results from an increase in Q_{gg}, just as for MOST 6. Aside from different slopes in the mid-region, the main difference between the two graphs appears to be one of scaling. The MOST D graph covers a much wider G_{ch} range, and is effectively shifted vertically up the Q_{gg} axis. It can reasonably be assumed that this vertical shift is accomplished by a change in the right-hand side of equation 2.4.8, and most probably, mainly in the size of the Q_s term as a result of a reduction in the level of the doping density in the substrate for MOST 6 (56). The resultant difference in Q_o (equation 2.4.8) between these two devices is clearly shown from Figures 3.3.15 and 3.3.16. For MOST D, Q_o = +8.4 pico-coulombs, while for MOST 6, Q_o = -7.2 pico-coulombs (taking the value at the Q_{gg} axis extrapolated from the mid-region slope in each case).

3.5.1.2 Low Channel Conductance Region

Assuming that the charge in the surface traps (Q_{st}) is fixed, it appears that, in general, there are two main causes of the deviation from straight line slope in the low channel conductance region of the gate charge versus channel conductance relationships. They are the combination of some of the conduction charge particles with doped substrate charge particles in the surface channel area, and mobility variations.

With no initial inversion layer present in the channel in the MOST D device, it is expected that some of the initial electrons placed in the surface channel region due to applied gate charge, will combine with holes (in this P-type substrate device). This results in the production of uncovered substrate charge Q_s, but it also means that these electrons are no longer available for conduction, and therefore cannot contribute to the channel conductance. Gradually with the injection of gate charge, an electron inversion layer is built up, the holes in the surface channel area having combined with electrons, producing an essentially constant value of Q_s, and the straight line section of the Q_{gg} versus G_{ch} relationship is reached.

This effect is expected to be less important in a device such as MOST 6 which has an initial inversion layer. Note that if the pinch-off point is used as reference, the discussion of the previous paragraph applies to MOST 6. It is probable [56] that the negative pinch-off voltage is produced by using a lower doping in the P-type substrate relative to that in MOST D, though it could also be achieved by surface processing during or prior to oxide layer formation [38,61]. With

a lower substrate doping, combination of holes and electrons during the formation of the surface channel must be less. It is believed that this is the main reason that the deviation from constant slope in this low channel conductance region is relatively greater in MOST D than MOST 6.

Varying majority carrier mobility can also be expected to produce deviation from the constant Q_{gg} versus G_{ch} slope in this low gate charge region. Initially each of the first few mobile electrons forming the actual channel between source and drain near the semiconductor surface has a large mean free path (62). This means that each electron has a high probability of collision with a scattering center. The average mobility of these electrons is thus quite low.

As Q_{gg} is further increased, more electrons accumulate under the semiconductor surface, and the mean free path of each electron decreases. The result is that the probability of collision of a given electron with a scattering center is lower since the conducting channel remains essentially on the surface and spreads very little into the semiconductor bulk material. The average electron mobility in the surface channel thus increases with increasing Q_{gg} until it reaches its constant and maximum value in the mid-region of the Q_{gg} versus G_{ch} relationships.

3.5.1.3 High Channel Conductance Region

As previously noted in Section 3.3.2.1, the deviation from the mid-region slope of the gate charge versus channel conductance relationships in the high channel conductance region of these plots is in the form of increasing slope with eventual saturation. The application of a positive voltage to the metal gate contact causes a bending (reduction)

of the potential of the conduction band in the silicon substrate with respect to the Fermi level. This process effectively allows more states in the conduction band to be filled and thus increases the conductivity of the channel between source and drain. The bending of the substrate conduction band is effectively halted, however, at the (lower) conduction band potential formed with the heavily doped source and drain N-type regions, which are electron conduction regions just as the channel is in these devices.

As this occurs. (38), it can be expected that the inversion layer will rapidly become degenerate as the heavily doped source and drain regions contain a high concentration of majority carriers. Although the concentration of carriers in the channel increases with increasing Q_{gg}, the mobility of the added degenerate carriers will be very low. The result is that the added charge contributes very little to channel conductance. Eventually, the concentration of degenerate carriers in the surface channel will predominate, and the channel conductance essentially saturates and increases only slightly with further increases in Q_{gg}. The values of gate charge and channel conductance at which saturation begins to occur depend considerably on the doping levels in the source and drain regions, and are quite different for these two devices.

3.5.2 Gate Charge Versus Drain Current Relationship

The gate charge versus drain current relationships to be discussed here were presented in Section 3.3.2, in Figures 3.3.21 and 3.3.22 for MOST D and MOST 6 respectively. The family of Q_{gg} versus I_d relationships for each of several values of drain voltage for MOST D and MOST 6

are again discussed in the same way as the FET relationships. Thus the mid-region or constant slope region of each relationship is discussed in Section 3.5.2.1 with the deviations from the constant slope of the mid-region being discussed in Section 3.5.2.2 for the low drain current region, and in Section 3.5.2.3 for the high drain current region. Finally, in Section 3.5.2.4, a discussion of the more important operating mechanisms within the MOST is given.

3.5.2.1 Mid-Region

The Q_{gg} versus I_d relationships for MOST D in Fig. 3.3.21 are perhaps simpler. The form of the relationship at low drain voltages (eg. V_d= .49 volts) is the same as the Q_{gg} versus G_{ch} relationship, as expected. The mid-region slope of each of the other relationships can be seen to decrease as drain voltage is increased. Further, it can be seen that the start of the constant slope region occurs at a progressively larger value of Q_{gg} (and I_d) on each relationship as drain voltage is increased.

Although it is perhaps more difficult to see, the behaviour of each relationship with increased drain voltage for MOST 6, in Fig. 3.3.22 , is exactly the same. The Q_{gg} versus I_d relationship for low values of drain voltage (eg. for V_d = .49 volts) is much the same shape as the Q_{gg} versus G_{ch} relationship in Fig. 3.3.16, with much of its straight line or mid-region occuring at "negative" values of Q_{gg} (negative values of Q_{gg} are not shown in Fig. 3.3.22, however). At larger values of drain voltage, the relationship is shifted (just as for MOST D), but in this case, the straight line regions are placed in the "positive" Q_{gg} region.

Equation 2.4.7, describing MOST operation with unpinched-off channels, was derived in Chapter 2, Section 2.4. It is

$$I_d = \frac{-(Q_{gg} + Q_{gd}) + Q_o}{\tau_d} \qquad (3.5.1)$$

where

$$\tau_d = L^2/\mu\, V_d \qquad (3.5.2)$$

It is thus reasonable to assume, on the basis of the charge control results in Figures 3.3.21 and 3.3.22, that equation 3.5.1 adequately describes MOST operation in the mid-region of each of these relationships with a constant value of τ_d. Further, it can be assumed that the assumptions made in Section 2.4 in connection with equation 3.5.1, are valid in the mid-region of these relationships just as was noted in Section 3.5.1.1 for the Q_{gg} versus G_{ch} relationships. Note that for MOST's, the mid-region (and beyond for larger values of I_d) of each of the Q_{gg} versus I_d relationships must be assumed in fact to correspond to device operation with unpinched-off channels since an increase in Q_{gg} puts more electrons in the channel, and hence moves the channel conditions further from the pinch-off situation. Thus the slope of each Q_{gg} versus I_d relationship in the mid-region(τ_d), is found to decrease as predicted by equation 3.5.2 as V_d is increased.

The effect of drain voltage on the Q_{gd} term in equation 3.5.1 can be clearly seen from the relationships for MOST D in Fig. 3.3.21, for example. As was noted in Chapter 2, Section 2.4, the Q_{gd} term, as a result of applied drain voltage, works in opposition to the Q_{gg} term for devices such as these operating in the enhancement mode. This is shown

in these relationships by the fact that it requires a larger value of Q_{gg} on a relationship at a large value of V_d, than at a low value of V_d, to overcome the pinch-off region and reach the constant slope or mid-region. Thus at least +2.0 volts are required on the gate of MOST D to produce current flow, as noted in Section 3.3.1, in order to overcome the effects of both Q_{gd} and Q_o, and put conduction charge in the channel.

The L^2/μ ratio obtained for each device at each of several values of drain voltage from the mid-region of each Q_{gg} versus I_d relationship is shown in Table 3.5.1. This ratio was obtained from equation 3.5.2 aas the $r_d V_d$ product. The L^2/μ ratio obtained from the mid-region of the Q_{gg} versus G_{ch} relationships in Figures 3.3.15 and 3.3.16 are also shown for comparison. It can be seen that for MOST D ,the L^2/μ ratios are essentially constant, and therefore independent of drain voltage. The results for MOST 6 show some variation with drain voltage.

Undoubtedly, the limited extent of the mid-region of many of the graphs for MOST 6 is a factor in limiting the accuracy of determining the L^2/μ ratio. It also illustrates that the extent of the low gate charge region could be sufficiently large, in some devices, and the onset of the high gate charge region sufficiently low under certain circumstances, to effectively mask out the mid-region altogether.

One important point illustrated by these results is that in the MOST, the effective channel voltage does not saturate in the mid-region, in the way that was observed in Section 3.4 for FET's. This will be discussed further subsequently. It does indicate, however, that since the full applied drain voltage appears across the channel length, it is possible

TABLE 3.5.1

MOST D AND MOST 6 : L^2/μ RATIO ($= \tau_d V_d$) FOR VARIOUS DRAIN VOLTAGES

Drain Voltage (Volts)	$L^2/\mu \times 10^{-9}$ (volt-sec)	
	MOST D	MOST 6
0	8.75	15.82
0.49	8.22	-
0.99	8.61	-
2.5	-	13.80
5.0	8.30	12.18
7.5	-	12.2
10.0	9.73	13.65

that such high fields are set up in the channel at the higher values of drain voltage that some decrease in the mobility of the carriers may result. This could account, for example, for the slightly increased value of L^2/μ for both devices in Table 3.5.1 at 10.0 volts on the drain.

It has been pointed out (60,62) that the average mobility of the carriers in a surface channel is affected by surface scattering. It is quite probable that this process is affected to some extent by the field along the channel even at relatively low drain voltages. This could account for the fact that, particularly for MOST 6, the L^2/μ ratios are generally smaller under conditions of applied drain voltage than that obtained for zero drain voltage.

3.5.2.2 Low Drain Current Region

As noted in the previous section, the deviation from the constant slope of the mid-region of the Q_{gg} versus I_d relationships in the low drain current region for these devices is considerably greater at the larger values of drain voltage. Certainly the factors discussed in Section 3.5.1.2, concerning the deviations observed in the low channel conductance region of the Q_{gg} versus G_{ch} relationships, are still present in this region of the Q_{gg} versus I_d relationships.

It is expected that the main reason for the extended deviation in this region at large drain voltages, is an increase in the Q_{gd} term of equation 3.5.1 with drain voltage. This is a distributed effect along the channel from source to drain, and depending on the device and the applied gate voltage, the applied drain voltage may be large enough to remove sufficient carriers to cause the drain end of the channel to be

effectively pinched-off. Thus it is also possible that an increase in the effective τ_d (or L^2/μ ratio) may result in this region as a result of wedge-shaped channel effects as discussed in Chapter 2, Section 2.5. Probably the main effect of the increased size of the Q_{gd} term is that a larger amount of gate charge Q_{gg} must be suppled to the device to compensate for Q_{gd} and to overcome the pinch-off situation all along the channel before the constant slope of the mid-region is reached. The pinch-off situation in the MOST is discussed more fully in Section 3.5.2.4.

It was noted in Section 3.3.1, in connection with the graphs of V_1 versus V_2 for MOST D that the slope of each graph was slightly different for different values of drain voltage. This different capacitance is quite probably due to the difference in distribution of channel and substrate depletion layer charge under the surface of the oxide layer. For MOST 6, the V_1 versus V_2 relationships showed some curvature, particularly at large drain voltages. It was noted earlier, that on the basis of the charge control relationships, it is expected that MOST 6 has a lower doping level in the substrate. It is therefore to be expected that the depletion region under the oxide layer extends much deeper into the substrate, and that its dimensions are more readily affected by applied device potentials than for MOST D. Such a distributed "lower plate" forming the gate capacitor is therefore much more liable to cause a variation in the gate capacitance and thus in the V_1 versus V_2 ratio with applied voltages. Also, of course, MOST 6 may have a thinner oxide layer ; in which case, the charge variations under the oxide layer could be expected to produce a more significant variation in gate capacitance.

3.5.2.3 High Drain Current Region

A deviation from the constant slope of the mid-region of each of the Q_{gg} versus I_d relationships in Figures 3.3.21 and 3.3.22 is present, just as was noted for the Q_{gg} versus G_{ch} relationships in the high channel conductance region in Section 3.5.1.3. It is believed that exactly the same process is involved in all these relationships, but it is quite evident that this eventual saturation or limiting with respect to drain current, is considerably affected by drain voltage. As noted in Section 3.5.2.1, the start of the deviation from the mid-region slope in this high drain current region occurs at progressively larger values of Q_{gg} (or V_g) and I_d on each relationship with larger drain voltage. This is the same saturation which was noted in connection with the preliminary measurements of I_d versus V_g in Section 3.3.1 for MOST D.

It is believed that the main cause of this observed behaviour is again the size of the Q_{gd} term in equation 3.5.1. As noted earlier, drain voltage V_d has an opposing effect to gate voltage (or Q_{gg}), in that it tends to remove conduction charge from the channel, progressively more towards the drain end. Thus , under conditions of a given applied gate and drain voltage in this high current region, it is expected that part of the channel towards the source can be highly degenerate , corresponding to the situation applying to the total channel with V_d=0. As a result of V_d , however, the concentration of carriers decreases towards the drain, such that a region at the drain end of the channel may not necessarily be degenerate. With increasing gate charge Q_{gg} , more of the channel will become degenerate, resulting in eventual saturation of drain current, similar to the saturation of channel conductance discussed in Section

3.5.1.3.

For a larger applied drain voltage, it can thus be seen that a larger value of gate charge (or V_g) is required to cause the complete channel tc become degenerate (i.e., to produce saturation). Since the drain voltage is larger, the resulting drain current is increased, such that it saturates at a larger value.

3.5.2.4 Discussion of Device Operation

It has been shown by the results of the charge control measurements, and noted in the previous discussions, that two important limiting processes occur in the MOST. One is the limiting of drain current (or channel conductance) which occurs with increasing Q_{gg} (or gate voltage) while maintaining a constant (or zero) voltage on the drain. This has been discussed previously,and is not to be confused with the second limiting process (i.e., pinch-off), which will be the main concern of the discussion in this section. The difference between these two processes will be made clear in the subsequent discussion.

The pinch-off region of these constant drain voltage Q_{gg} versus I_d relationships corresponds to the low drain current region for devices such as these operating in the enhancement mode . Under conditions of zero applied drain voltage, pinch-off is assumed to occur when the concentration of conduction charges in the channel (i.e., electrons for these devices) is just reduced to zero. Under such conditions, due to the presence of charge Q_{st} in the surface traps, and any required gate voltage, it can be assumed that the area near the surface of the substrate is completely depleted . Thus for MOST 6 and MOST D with P-type substrates, this area would consist of uncovered fixed negative charges.

It has been noted that for a fixed gate voltage, the effect of drain voltage is to remove conduction charge from the channel (i.e. Q_{gd} term), with more charge being removed from the drain end of the channel. It can therefore be expected that under conditions of sufficiently large drain voltage, the concentration of mobile carriers over a region at the drain end of the channel will be sharply reduced.

The charge control relationships for MOST D and MOST 6 in Figures 3.3.21 and 3.3.22 indicate that this pinch-off region is characterized by a deviation from the constant slope of the mid-region which is greater on the relationships at the larger values of drain voltage. Further, this deviation is in the form of an increase in the effective value of τ_d ($= L^2/\mu V_d$). Since the bounds of the maximum channel length in these devices are fixed by the source and drain heavily doped contact regions, the unpinched-off or effective length of the channel can only decrease under conditions of pinch-off. Though there may be some change in the average mobility under these conditions, it is quite evident that there must be a decrease in the effective channel voltage V_{ch} in this region in order to cause τ_d to increase.

It therefore appears that a situation corresponding to the Shockley criterion (equation 3.4.3) must apply to these devices. Thus the effective channel voltage V_{ch} on a constant V_d relationship must be forced to vary in this pinch-off region depending on the size of Q_{gg} , or gate voltage. The result is a situation which much more closely approaches the classical one-dimensional theory (as expressed by equation 2.4.1) for the MOST , than was observed for the junction FET.

A decrease in gate voltage (at constant drain voltage) in this

region forces a decrease in V_{ch} , as predicted by the Shockley criterion for this device, as a result of a decrease in the charge in the unpinched-off channel, and thus a decrease in the effective channel length. The difference in voltage between the applied V_d and V_{ch} must be dropped across the extended pinched-off end of the channel through which the drain current is flowing. In pinch-off then, a balance must be set up between the drain current, the applied drain voltage, the gate voltage, and the length of the channel which is pinched-off.

It is important to note that in the MOST, unlike the situation in the FET, the channel voltage V_{ch} is effectively determined by the applied gate voltage which becomes the forcing condition in the pinch-off region. The depletion regions do not control the basic operation of the MOST as they do in the FET, and thus the MOST is relatively unaffected by the presence of current carriers in the pinched-off region of the channel. Just as for the FET, relatively high fields may be set up across the pinch-off region in the MOST, thus acting as a "collector" for the current carriers from the channel.

3.6 Overall Conclusions

The results of measurements have been presented in this chapter to study the validity and applicability of the basic charge control theory derived on the basis of unpinched-off channels. Further, measurements have been made over a wider range of operating conditions on both types of devices in order to investigate the possibility of extending the applicability of the basic charge control relationships into the pinch-off region of operation.

True charge control operation (i.e., constant L^2/μ ratio, or constant r_d) has been shown to apply to a variety of commercial FET's over a wide range of values of drain voltage, from zero to beyond pinch-off. The basic charge control theory thus has a wide range of validity for these devices, if the effective channel voltage V_{ch}, and not the full applied drain voltage is used in these relationships. By so doing, the effects of saturation with drain voltage are accounted for. Deviations from true charge control operation have been observed for these devices, even under conditions of zero applied drain voltage. The reasons for this behaviour have been discussed.

A study of the charge control results has led to a better understanding of the operating mechanisms within the device, particularly with regard to the pinch-off process. These results have shown that it is no longer meaningful to apply the pinch-off voltage criterion as measured under conditions of zero applied drain voltage, to the FET under conditions such that there is a significant amount of majority carrier charge in the "depleted" region beyond the end of the open channel. It has been seen, in fact, that the effective voltage V_{ch} across the channel remains essentially

unaffected over a wide range of applied gate voltage.

It is interesting to note that the presence of significant majority carrier charge in the depleted region beyond the channel in the FET, has a somewhat analogous counterpart in the bipolar transistor. Thus, in the bipolar transistor [63,64], the collector depletion region can be forced to contract at high bias current levels, causing a widening of the base region.

The results of the charge control measurements on MOST's discussed in Section 3.5 have shown that, in general, the charge control theory for MOST's and the assumptions made in the derivation of that theory, are valid over a significant range of operation for a wide range of applied drain voltages. It has been shown that constant τ_d or true charge control operation, does not, however, apply to the MOST in the region of operation where the drain end of the channel is pinched-off. In addition to the current limiting process which occurs with the drain end of the channel pinched-off, this study has emphasized that a limiting of the drain current also occurs in the enhancement mode of operation as gate voltage (or Q_{gg}) is increased with constant applied drain voltage. The reasons for this behaviour have been discussed in terms of the basic operating mechanisms within the device.

The charge control approach has thus proved to be useful as a basis for studying the basic behaviour of various types of field-effect transistors and insulated gate transistors, without special regard to junction law(s), geometry , or method of fabrication. One very important aspect of this approach as applied in this chapter, is that it reveals, in the nature of its straight line relationships, or deviations therefrom, the

ranges of device operation over which the charge control theory and its associated assumptions are valid, or are in seriously in error.

In Chapter 2, Section 2.6, the subject of modelling FET's and MOST's from the charge control point of view was introduced. The models presented in Section 2.6 were specifically concerned only with device operation such that the channel was always open or unpinched-off. In these models, the distributed nature of these devices was emphasized by the use of several models lumps. As will be seen, this aspect is taken up again in considerably more detail in Chapters 4 and 5. Specifically, it will be shown that several lumps are generally required to model the switching transient behaviour of these devices adequately.

The results of the charge control measurements of FET's and MOST's, and the discussions in this chapter have shown that the saturation or limiting processes within these devices are highly complex. Further, particularly in the case of the FET, the various regions within the device become difficult to define for various degrees of saturation. There is no reason to believe that the distributed nature of the channel and the other regions of the device will become significantly less important under conditions of large drain voltages where the device is in saturation. Hence it can be expected that any attempt to model these devices for large drain voltages in saturation, in a manner similar to the approach used in Section 2.6, to account for distributed effects, will be both difficult and involved. This is considered to be beyond the scope of the present project, and will not be attempted here.

Steady state charge control models specifying the terminal behaviour of FET's and MOST's under any operating conditions can, however, be pro-

posed on the basis of the work in this chapter. Such a model for the FET, for example, is shown in Fig. 3.6.1. It consists, in its simplest form, of a current generator and a charge store, and expresses the relationship between drain current I_d and the majority carrier charge Q_{ch} in the channel, for a given set of applied bias conditions. The necessary parameters for the model (i.e., Q_o, Q_{gg}, Q_{gd}, τ_d) for the conditions of operation can all be obtained for a given device from a family of charge control relationships measured at each of several values of drain voltage from zero to beyond saturation as shown and discussed previously in this chapter. It is to be noted in particular, that τ_d is not constant, but is a function of drain voltage. Although the parameters for the model in Fig. 3.6.1 are perhaps more complex, it is analogous to the simple form of charge control model often used for bipolar transistors.(42).

Without becoming extremely involved, even for the steady state situation, it is difficult to go beyond the form of the model shown in Fig. 3.6.1, and break up the charge store into its components Q_{gg} and Q_{gd}, and at the same time account for the effects of saturation. Note that from the charge control measurements made in this chapter, it is not possible to determine the amount of charge in the depletion region extending beyond the end of the channel towards the drain contact at large drain voltages. This component of charge has not been included in the model in Fig. 3.6.1. If this were desired, it would need to be obtained from a pulse measurement of charge delivered to the drain corresponding to various values of drain voltage. For a first approximation, however, its effects can be neglected, just as the effects of the space charge regions, and base width modulation are often neglected, for example, in

the charge control model for the bipolar transistor.

Thus, although considerably more difficult to apply, it is conceivable that a steady state model for the FET based on that shown in Fig. 3.6.1 could, within the restrictions noted, also be used to obtain large signal transient information. As is done for bipolar transistors, this would involve the assumption that the transient is slow enough so that the device can be represented by a succession of steady states. However, due to the distributed nature of the FET, it is expected that the restrictions on the use of the above method would be far more severe in the case of FET's than for bipolar transistors. Chapters 4 and 5 are concerned specifically with transients under low level switching conditions, but in these chapters, the importance of the effects of the distributed nature of the FET on the switching transients will be established.

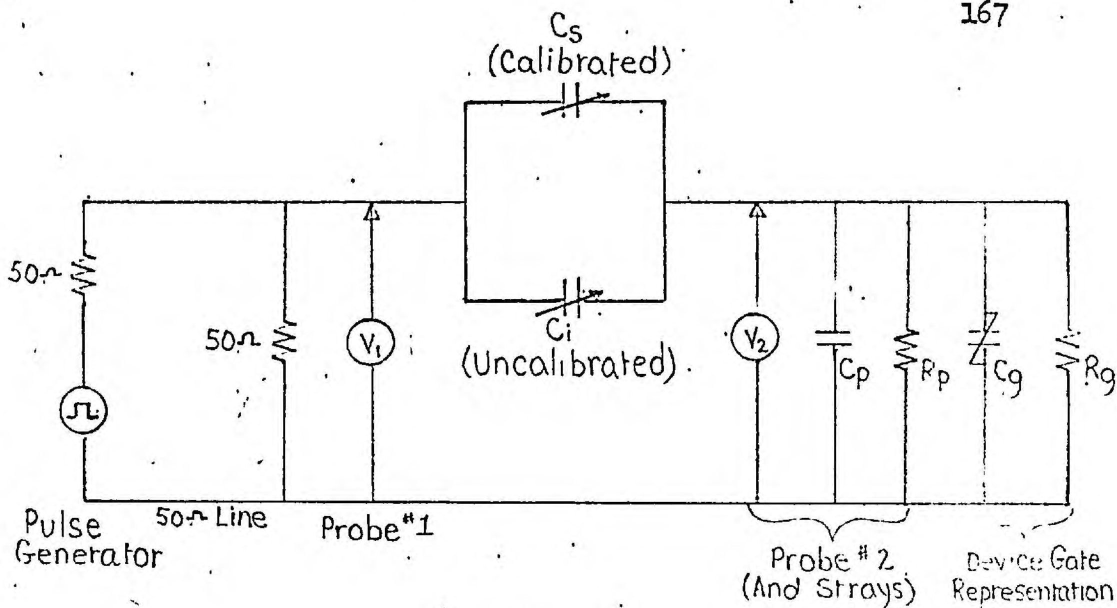


Fig. 3.2.1 : Illustration of Possible Gate Charge Measurement Circuit

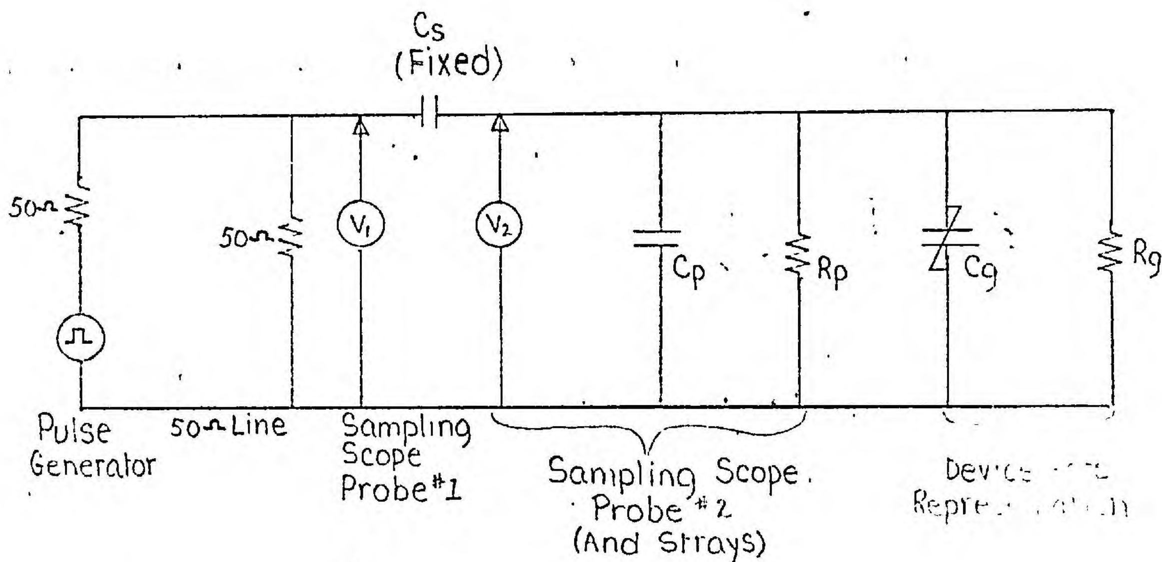


Fig. 3.2.2 : Circuit for Initial Compensation Measurement Method

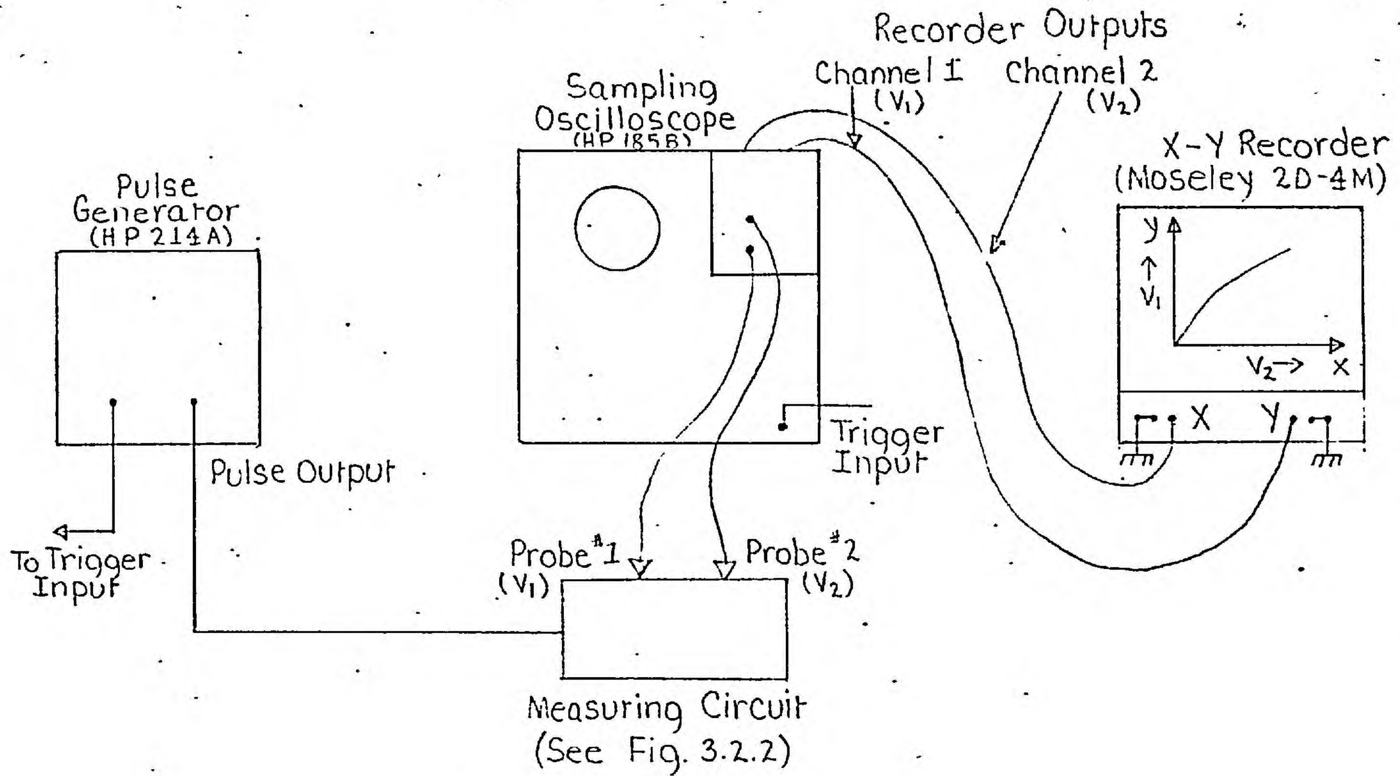
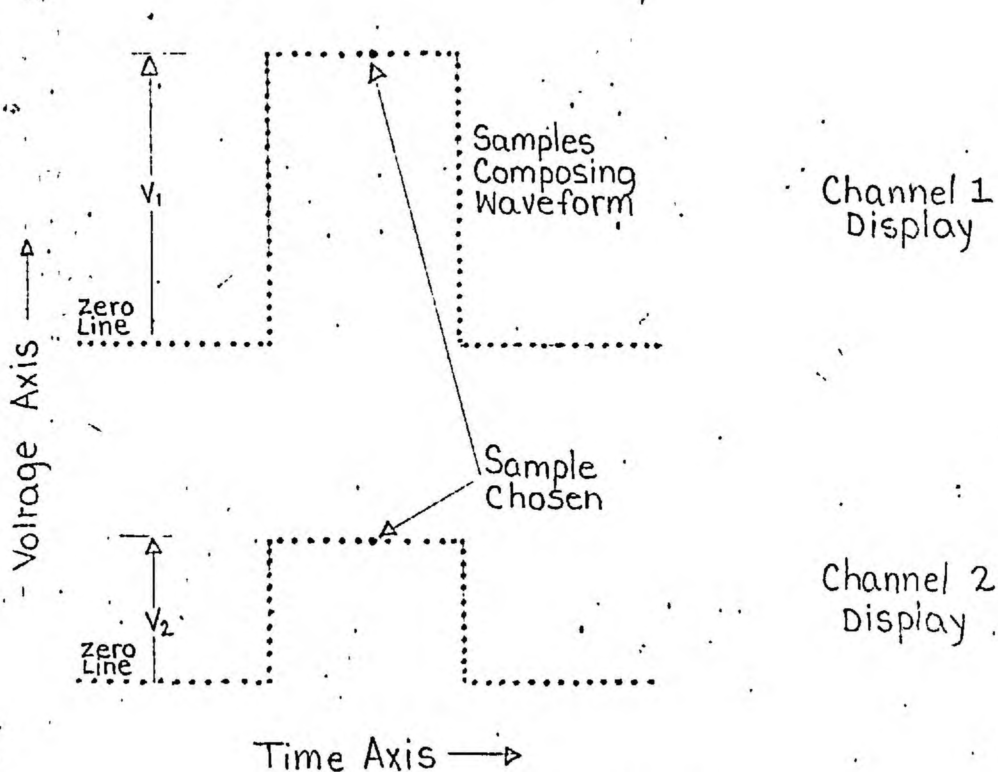


Fig. 3.2.3 : Block Diagram of System for Initial Compensation Measurement



With the spots positioned as shown, channel 1 and channel 2 outputs are time independent and proportional to pulse amplitudes V_1 and V_2 respectively.

Fig. 3.2.4 : Obtaining Output from Sampling Oscilloscope Proportional to Pulse Amplitude

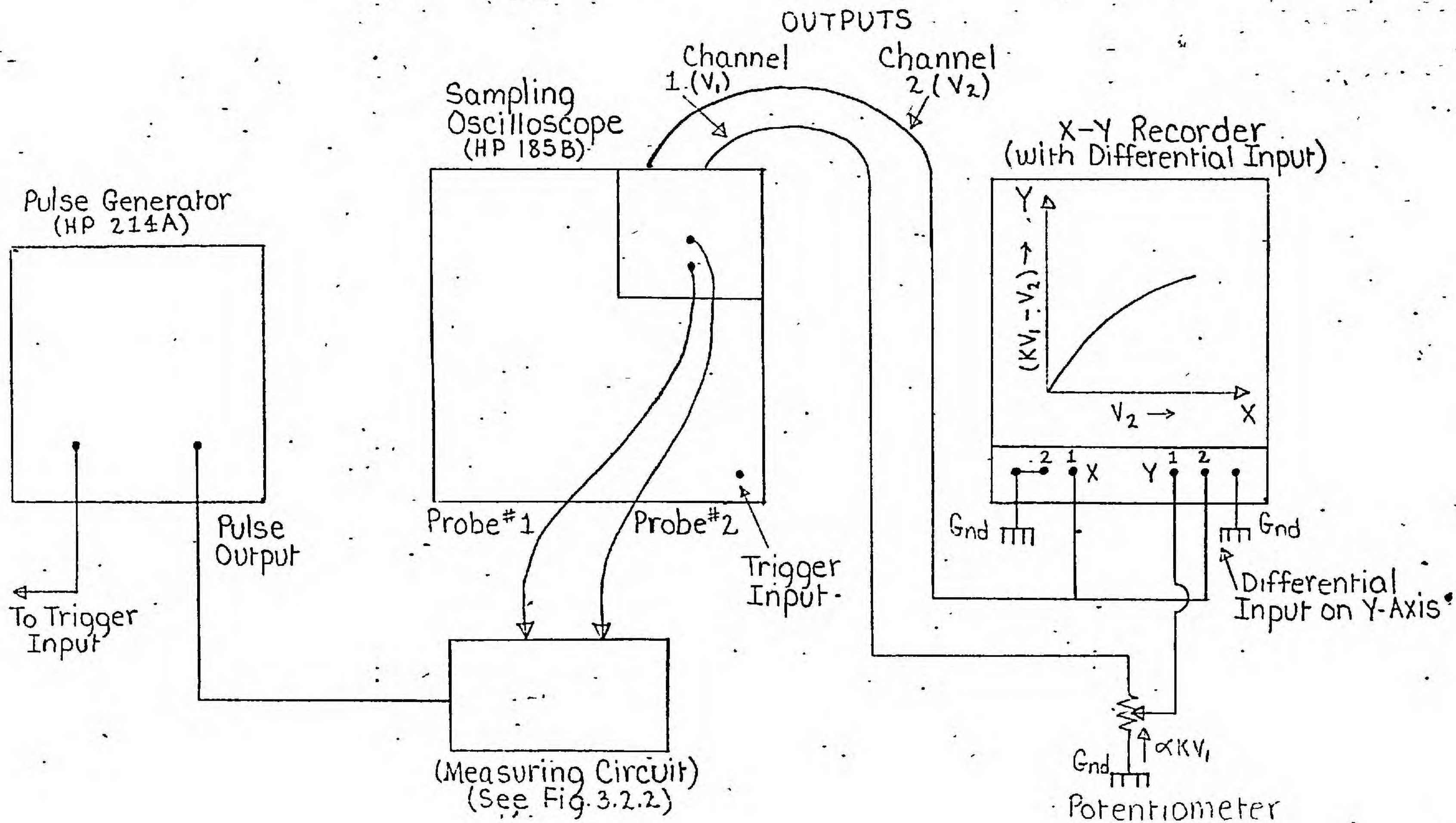
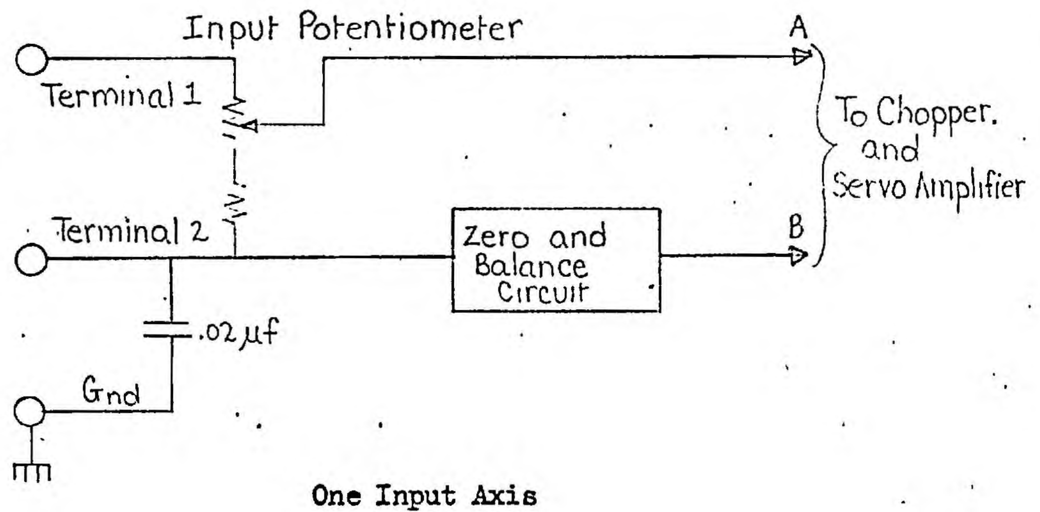
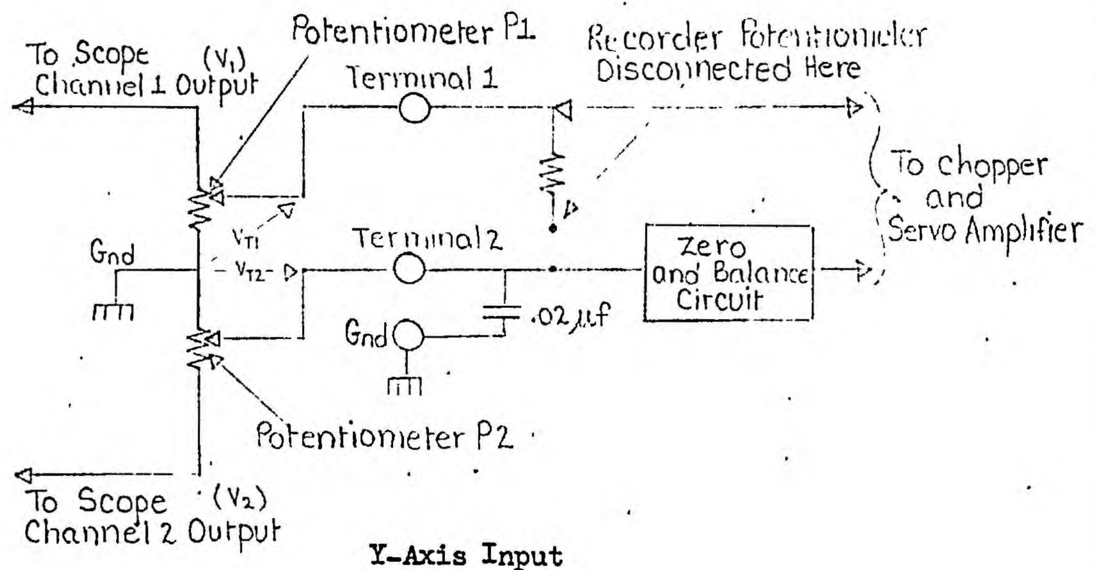


Fig. 3.2.5 : Block Diagram of Potentiometer Method Requiring an X-Y Recorder With Differential Input



One Input Axis

Fig. 3.2.6 : Moseley 2D-4M Simplified Input Circuit Representation



Y-Axis Input

Fig. 3.2.7 : Method of Producing Effective Differential Input with Moseley 2D-4M X-Y Recorder

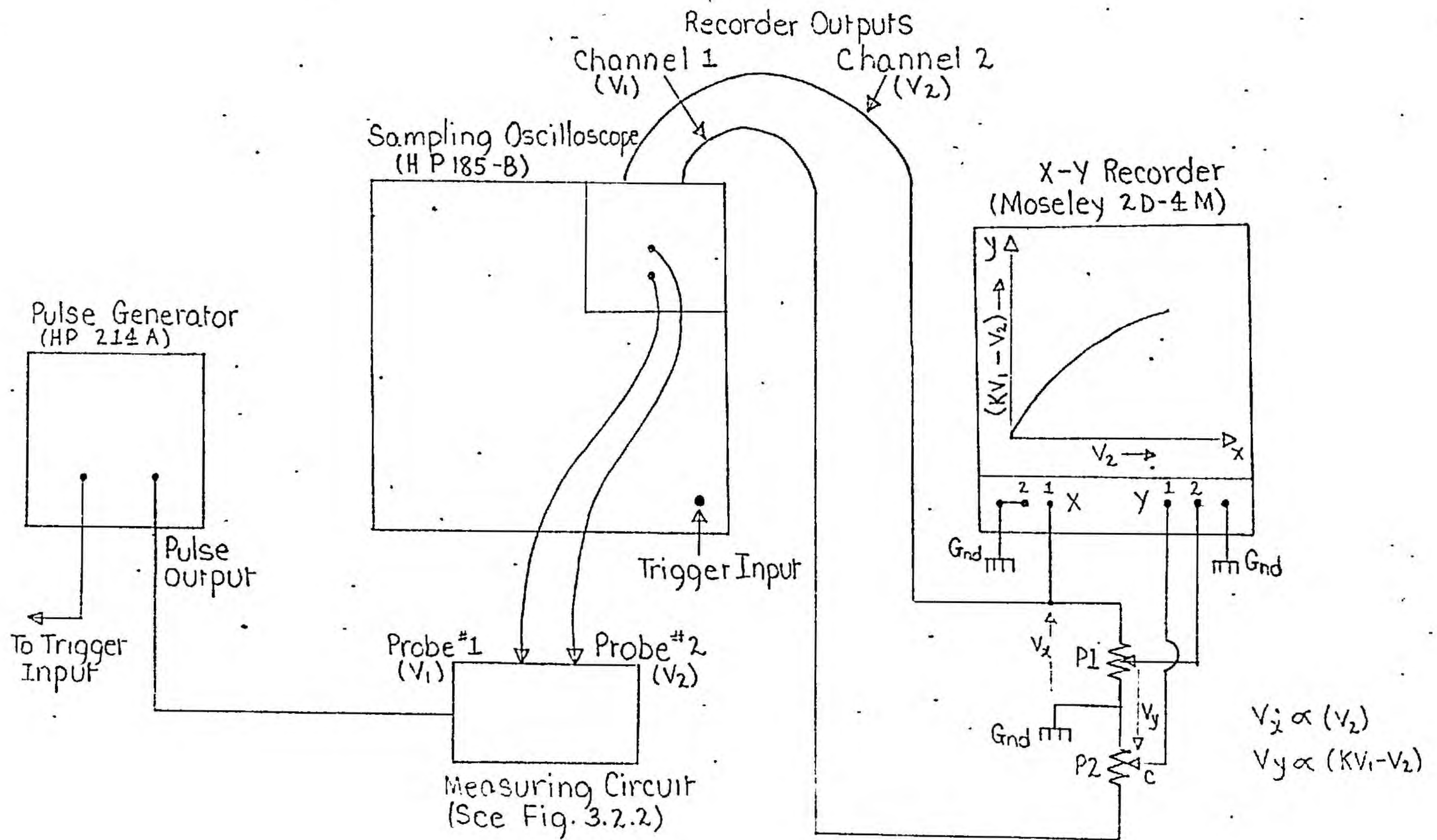


Fig. 3.2.8 : Block Diagram of Potentiometer Method Using Moseley Model 2D- 4M

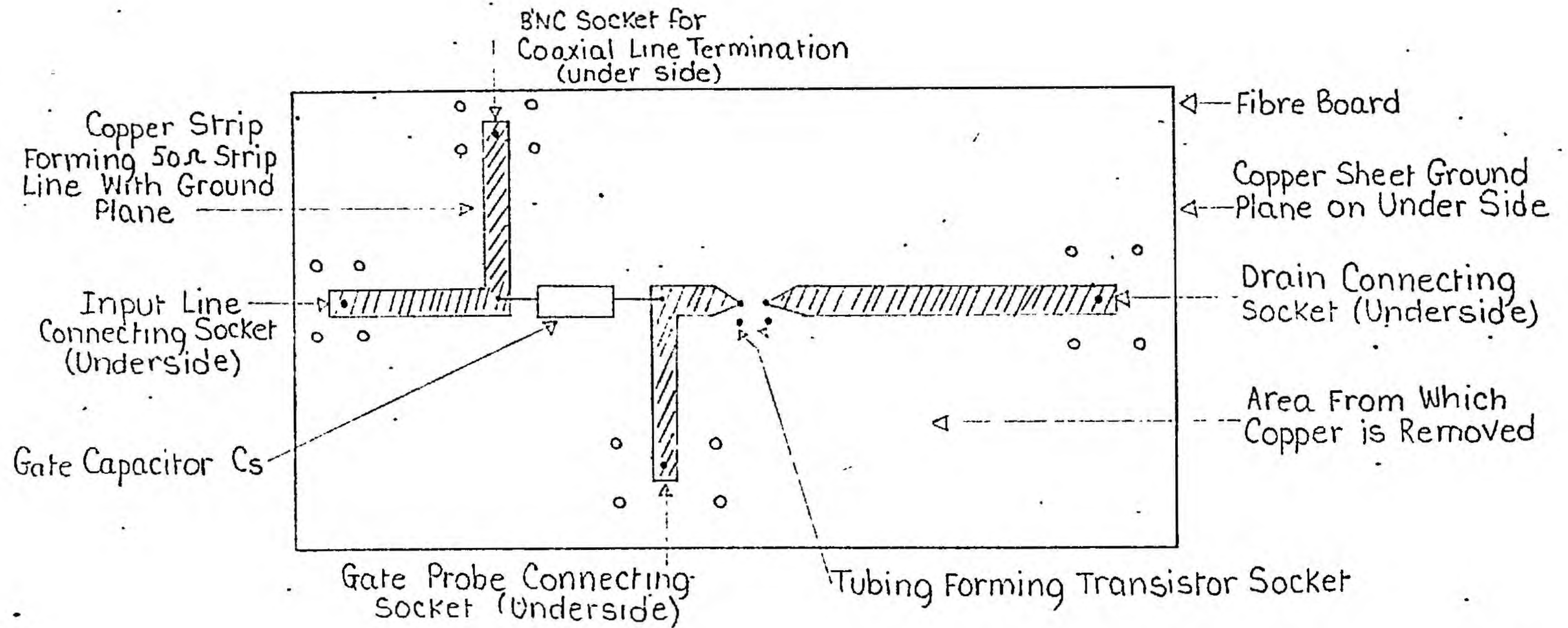
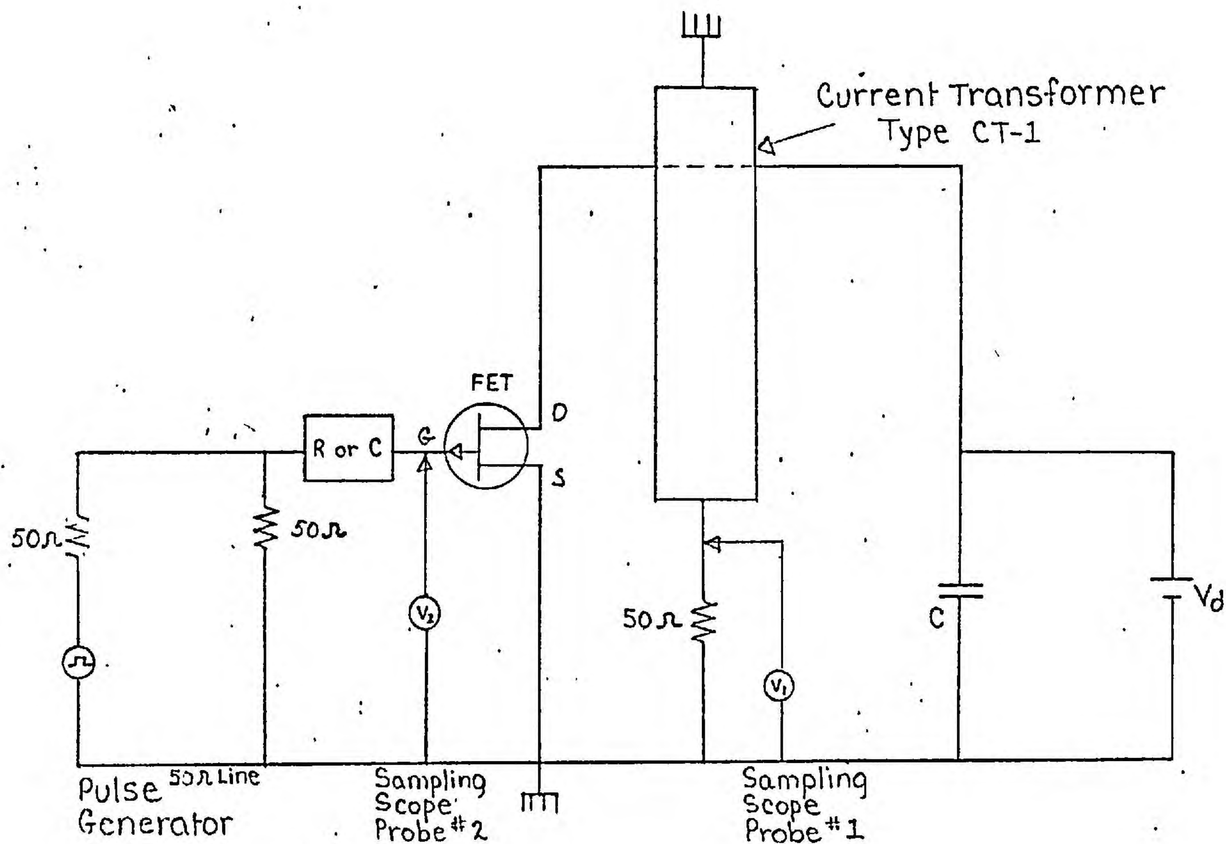


Fig. 3.2.9 : Charge Control Measurement Jig



V_2 measures gate voltage pulse amplitude

V_1 measures drain current pulse amplitude

(5 mv/ma across 50 Ω load)

Fig. 3.2.10 : Pulse Measurement of Drain Current Versus Gate Voltage Using Current Transformer with "Sampling Oscilloscope"

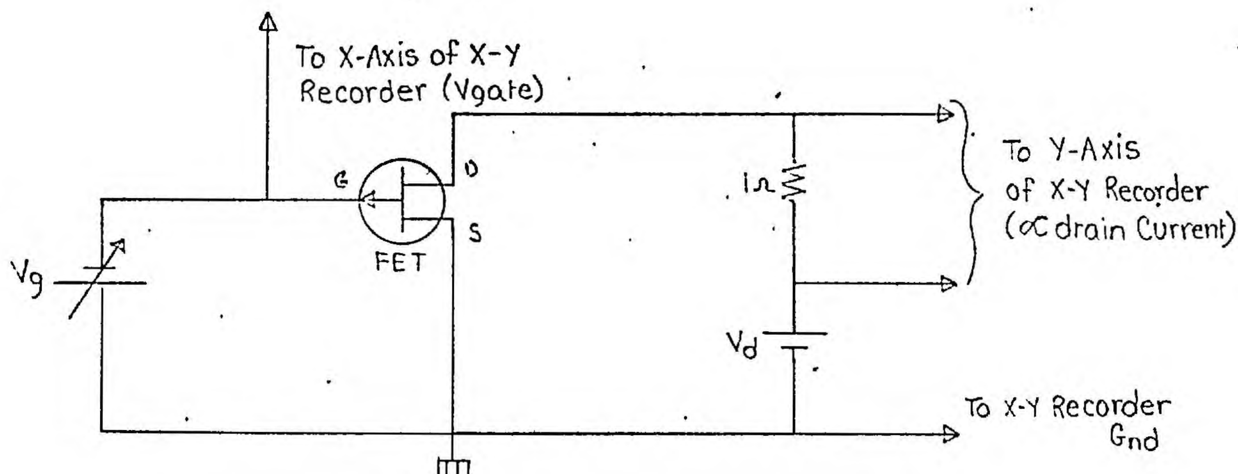


Fig. 3.2.11 : D-C Measurement of Drain Current Versus Gate Voltage with X-Y Recorder (Moseley 2D-4M)

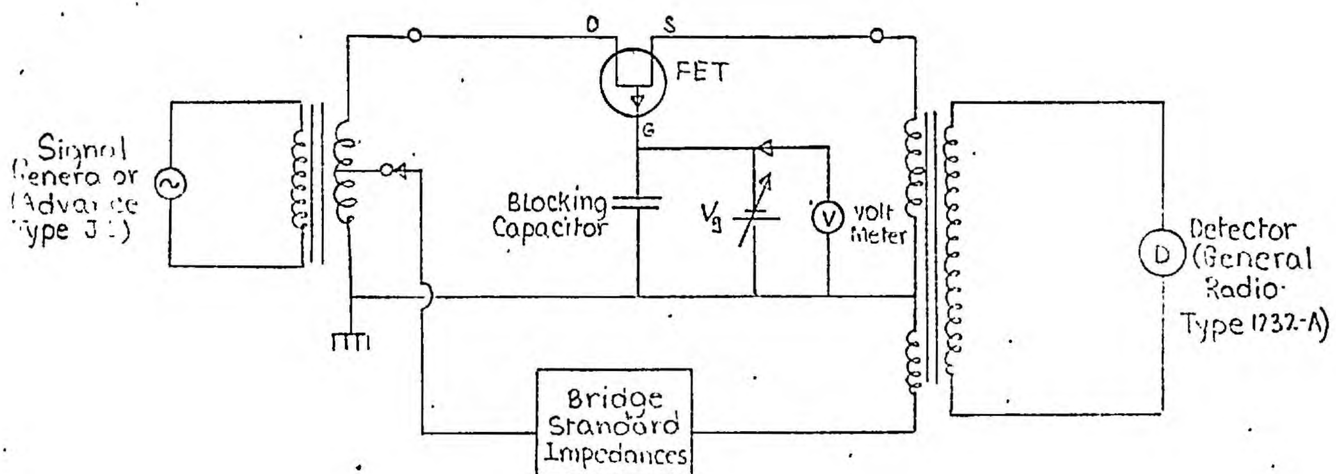
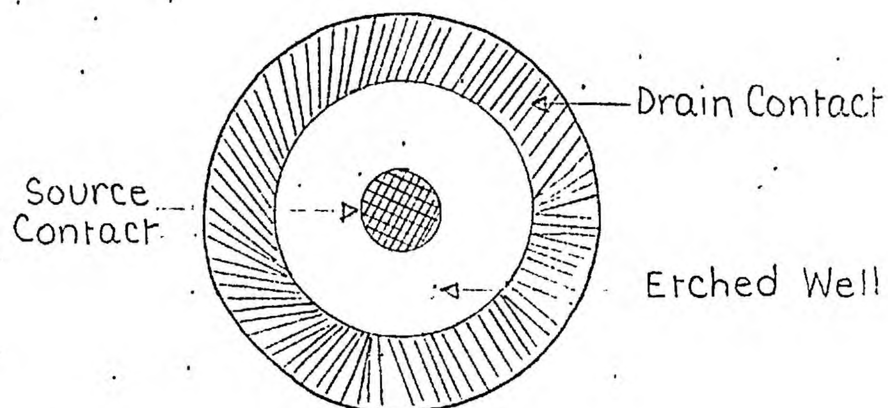
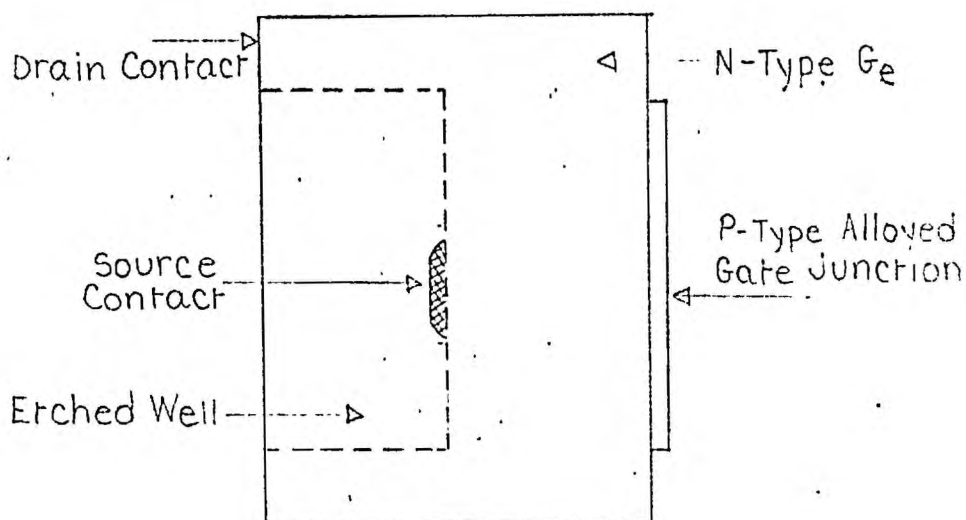


Fig. 3.2.12 : Measurement of Small Signal Channel Conductance Versus Gate Voltage on Wayne Kerr B221 Bridge

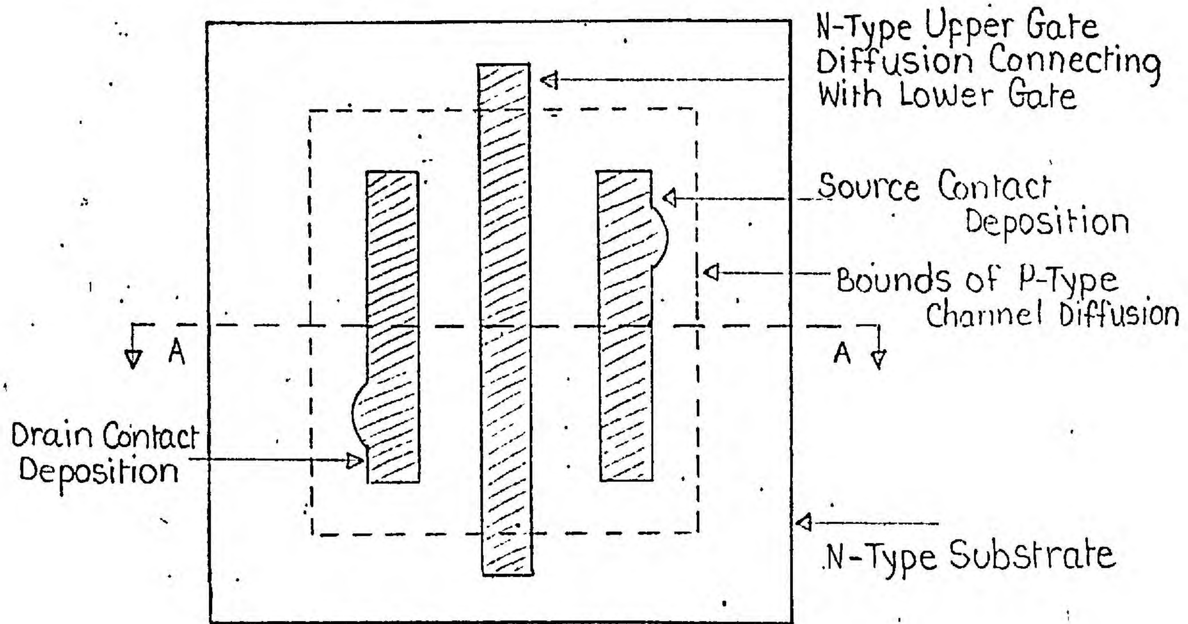


Top View

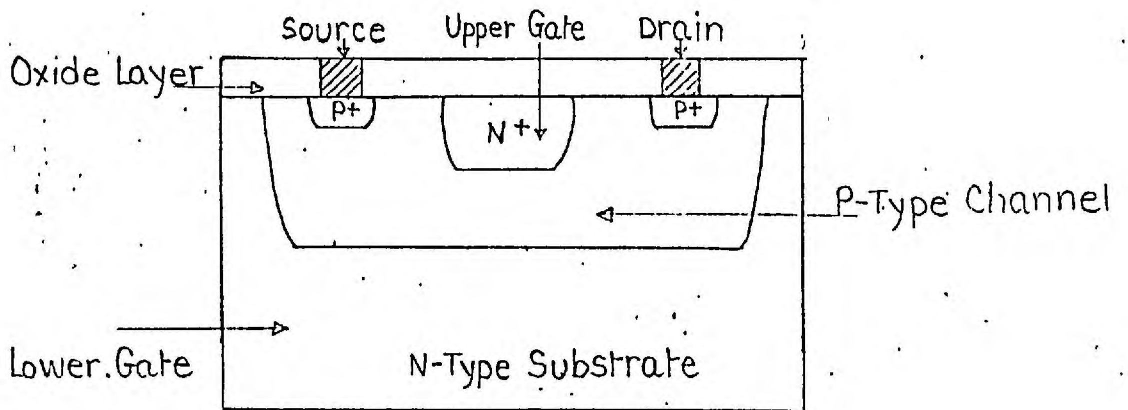


Section View

Fig. 3.3.1 : Structure for FET Types TIX881 and TIX883

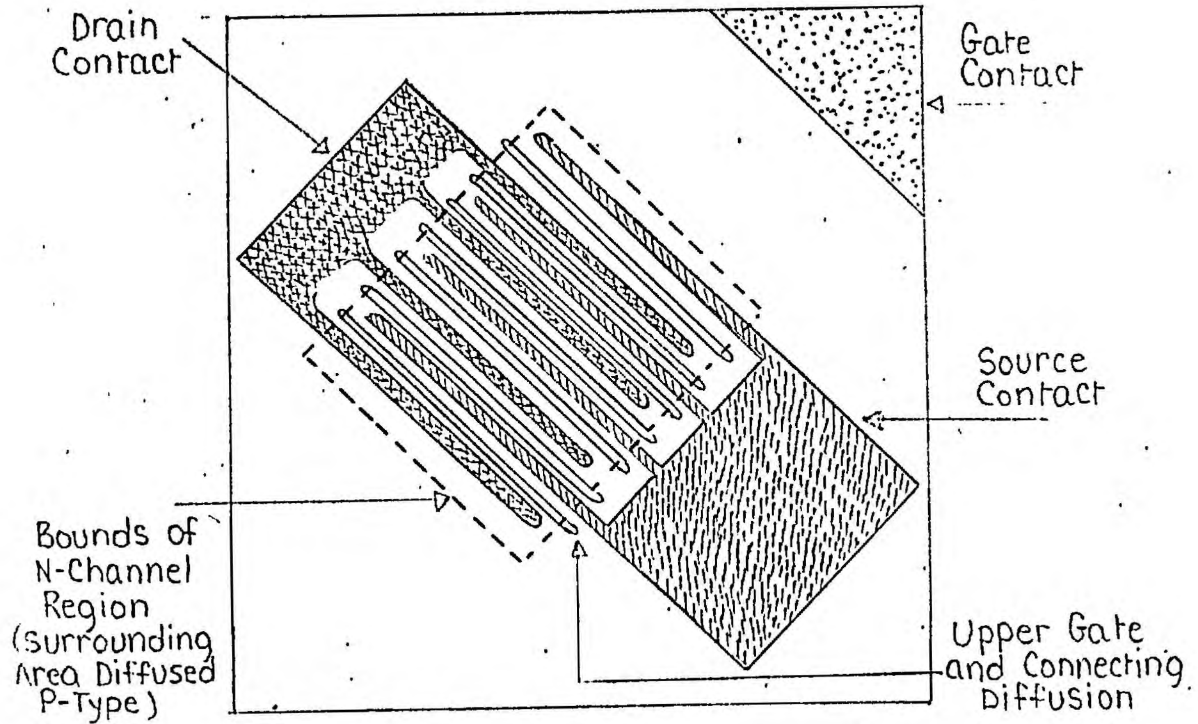


Top View



Section A-A

Fig. 3.3.2 : Structure for FET Type 2N2498



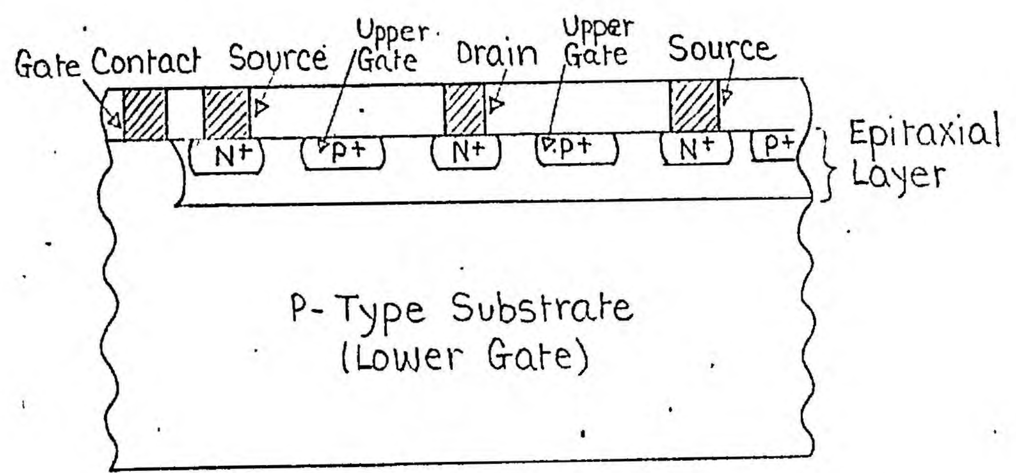


Fig. 3.3.3 : Structure for FET Type 2N3824

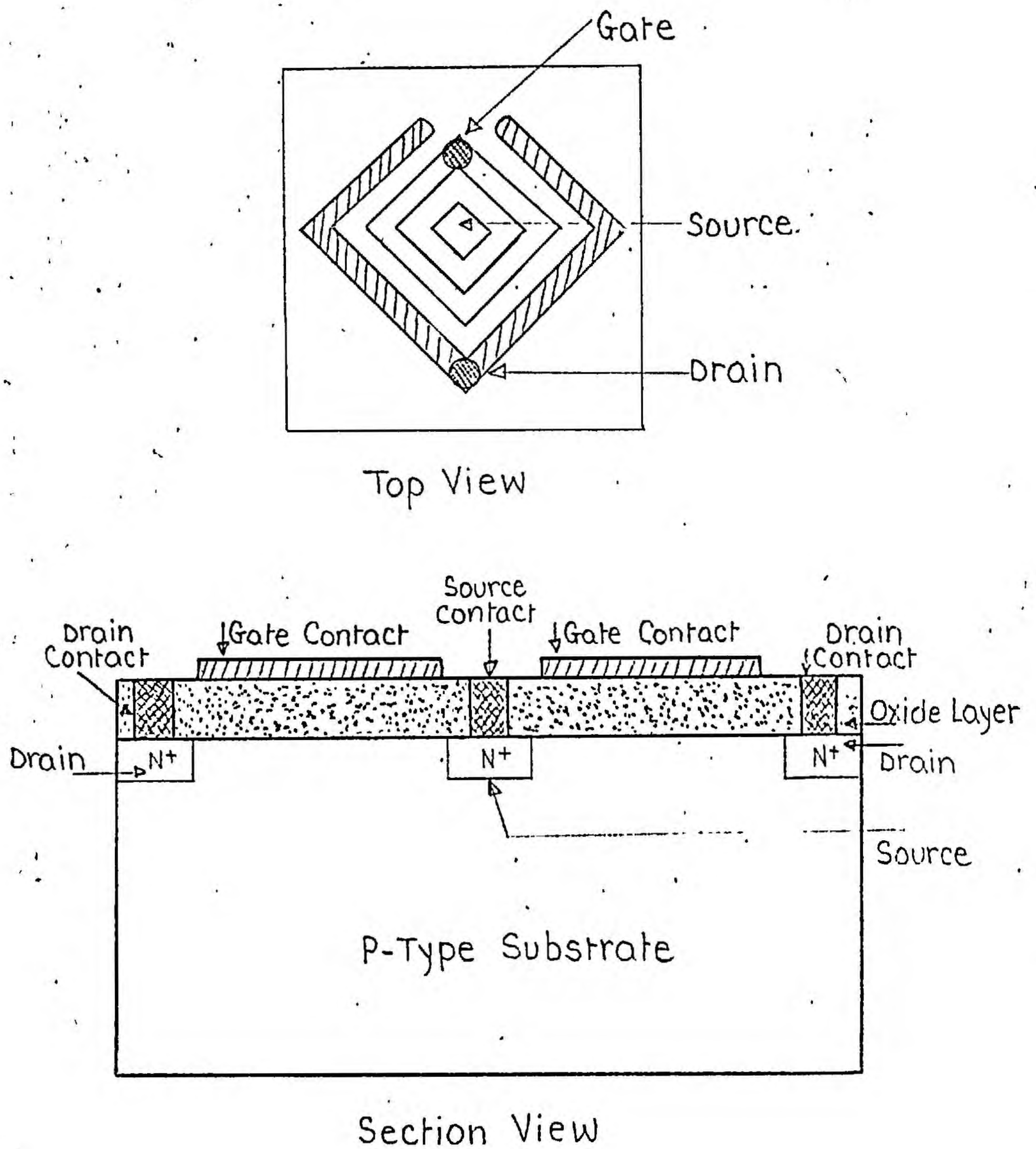


Fig. 3.3.4 : Structure for MOST Type 95BFY

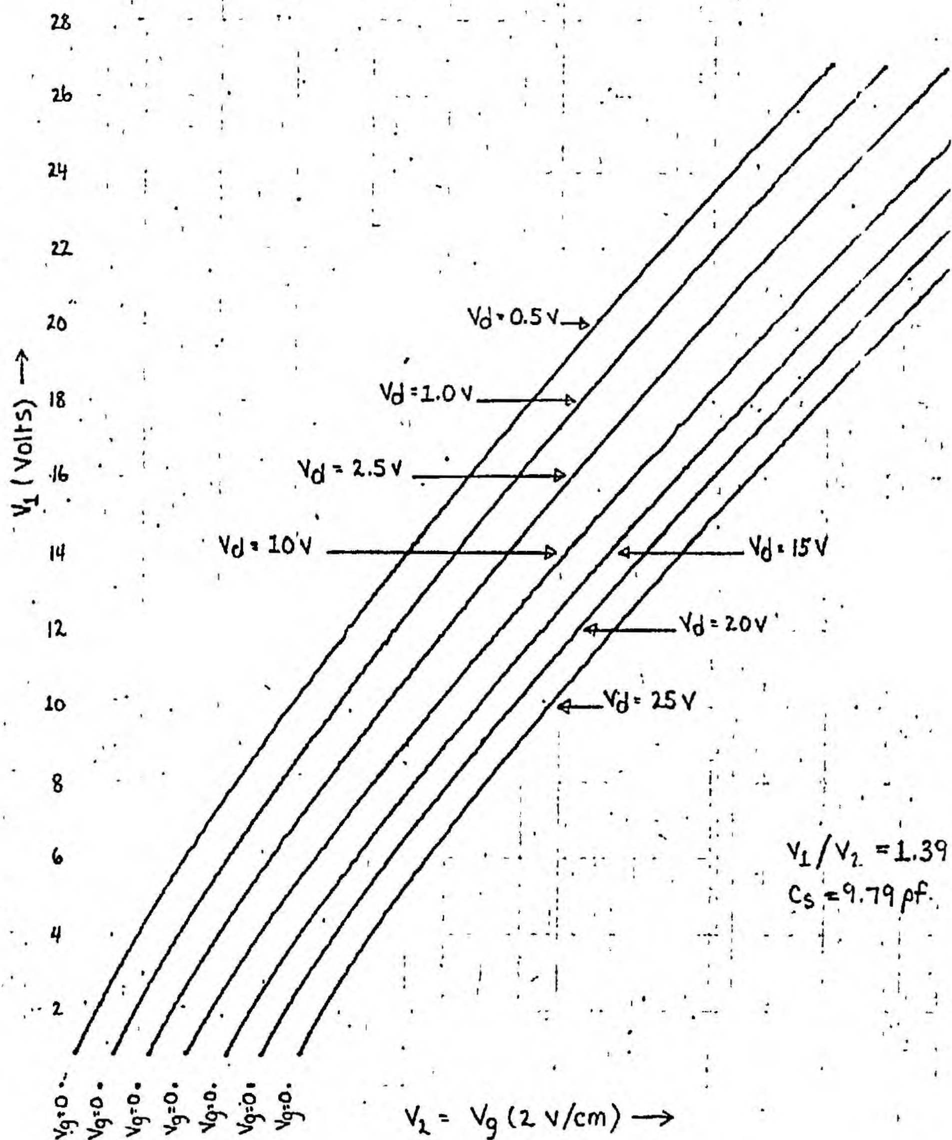


Fig. 3.3.5 : V_1 Versus V_2 ($=V_g$) Graphs for Various Drain Voltages for Device TIX881-2

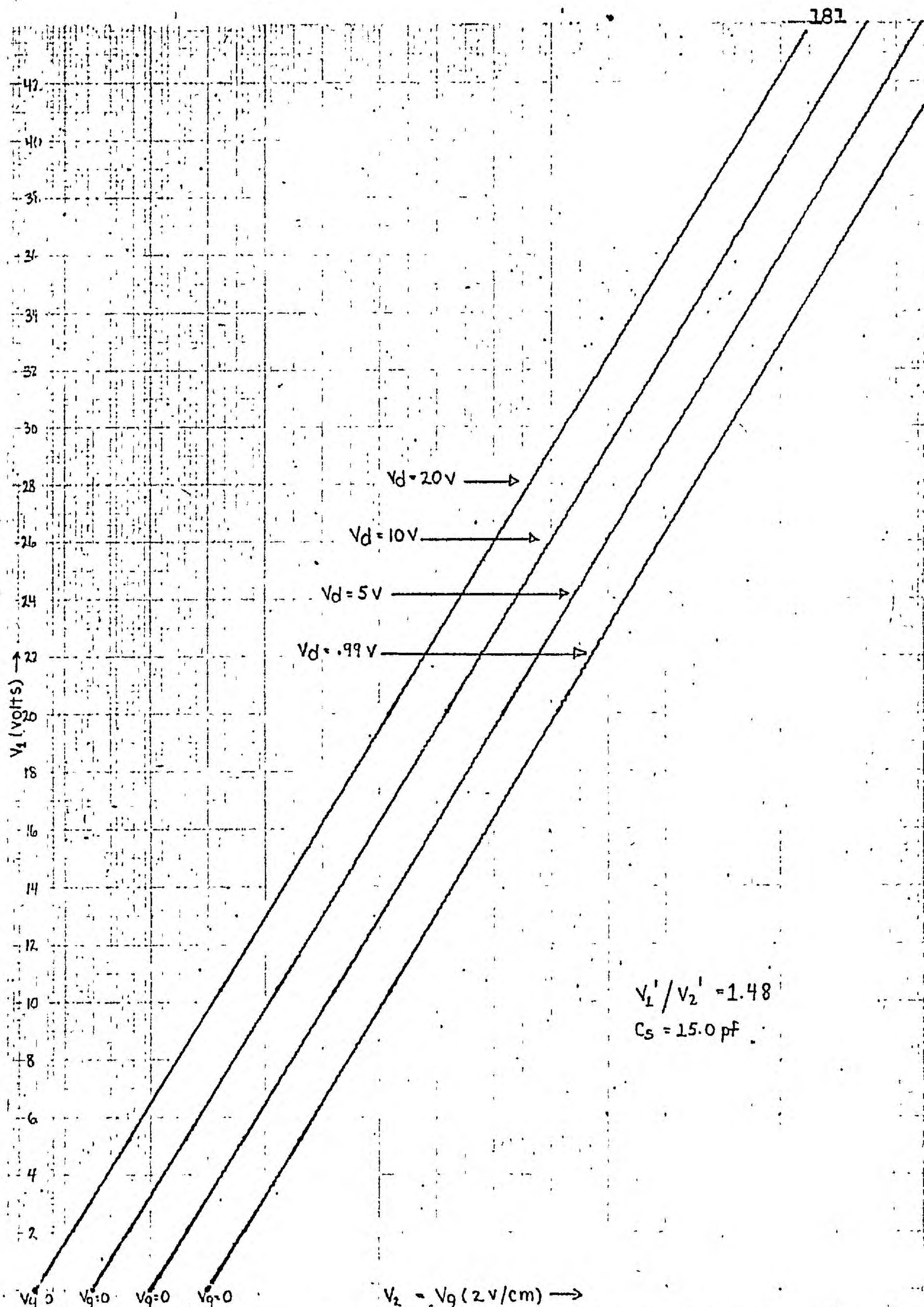


Fig. 3.3.6 : V_1 Versus V_2 ($=V_g$) Graphs for Various Drain Voltages for Device MOST D

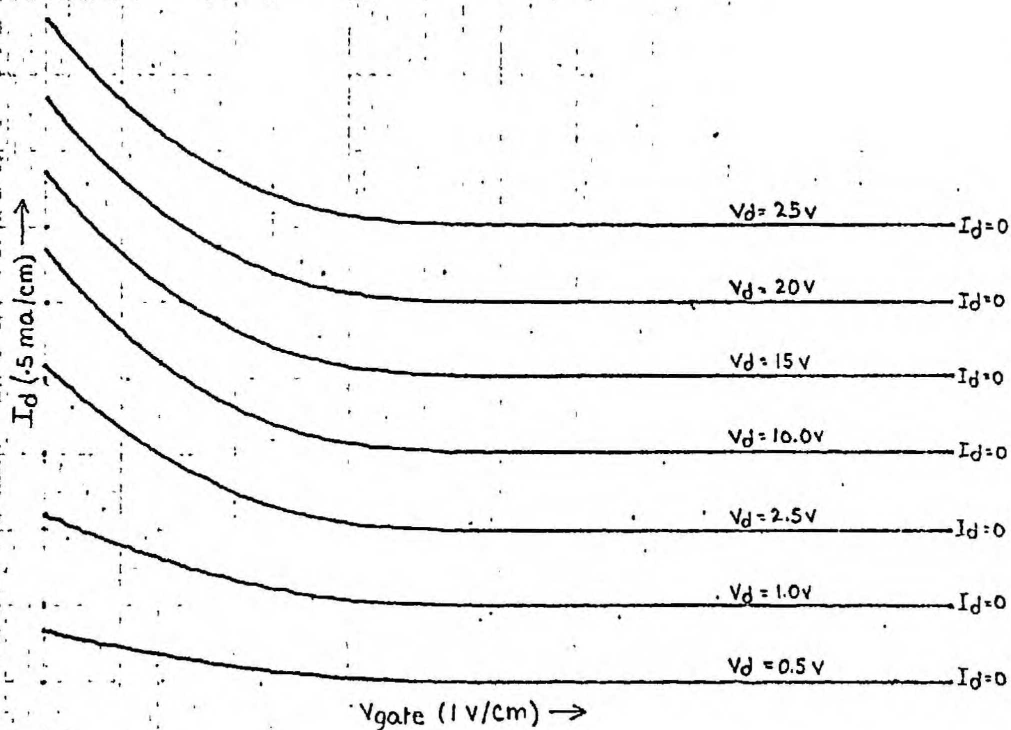


Fig. 3.3.7 : I_d Versus V_g Graphs for Various Drain Voltages for Device TIX881-2

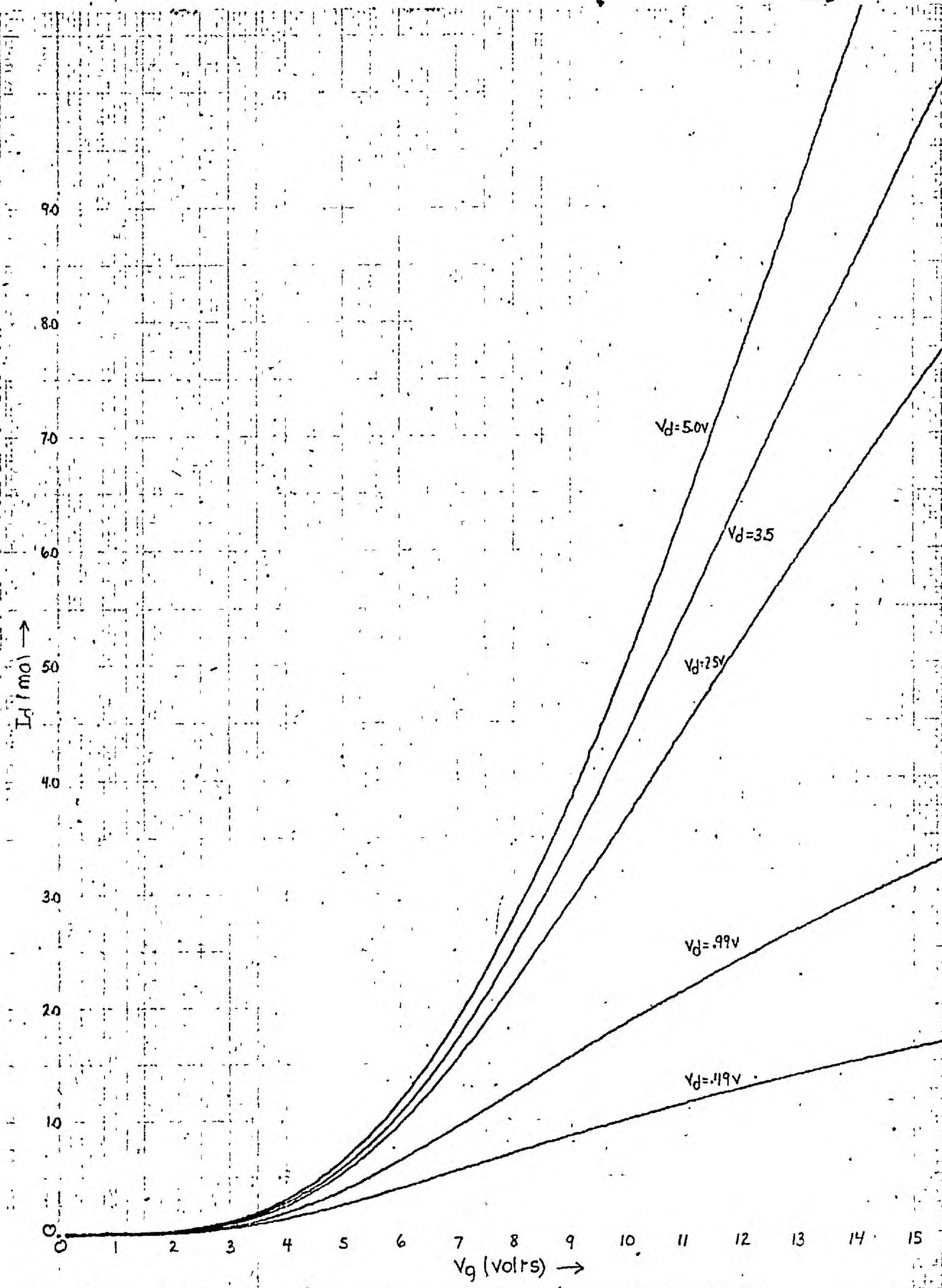


Fig. 3.3.8 : I_d Versus V_g Graphs for Small Drain Voltages for Device MOST D

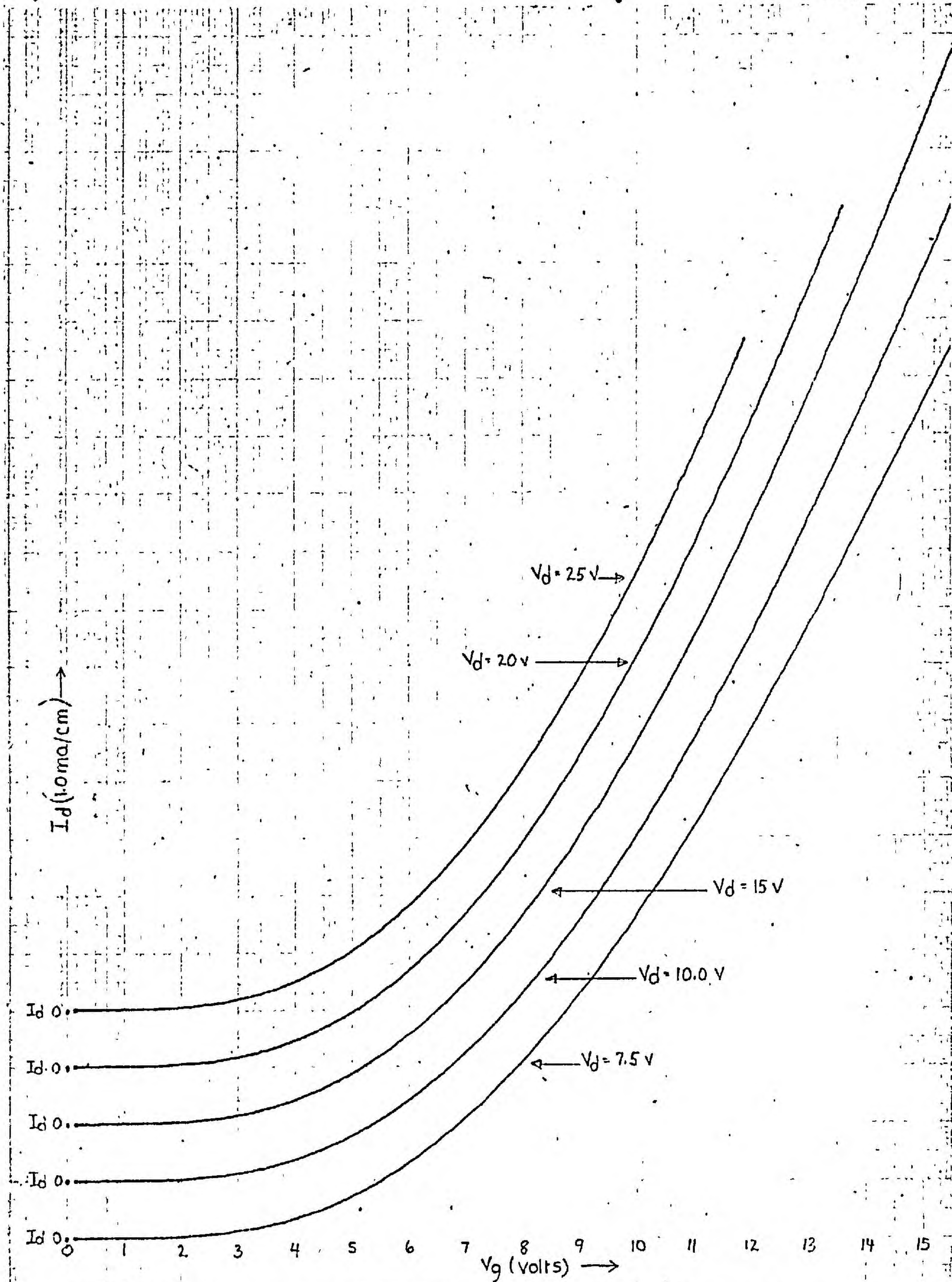


Fig. 3.3.9 : I_d Versus V_g Graphs for Large Drain Voltages for Device MOST D

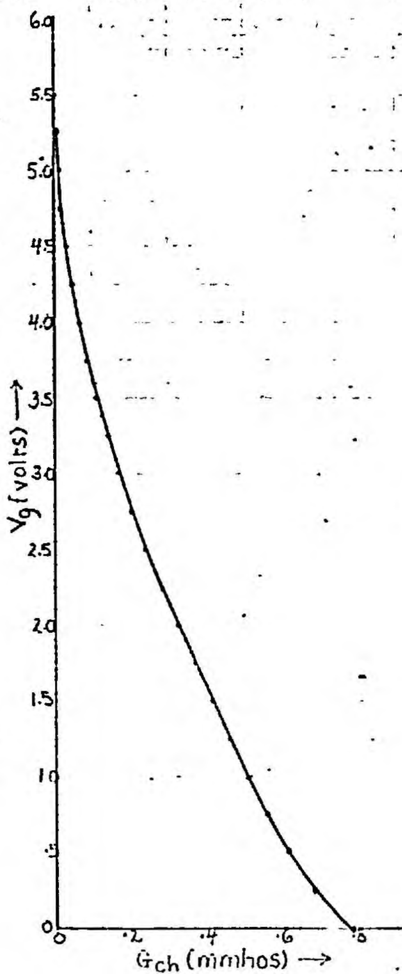


Fig. 3.3.10 : V_g Versus G_{ch} for Device TIX881-2

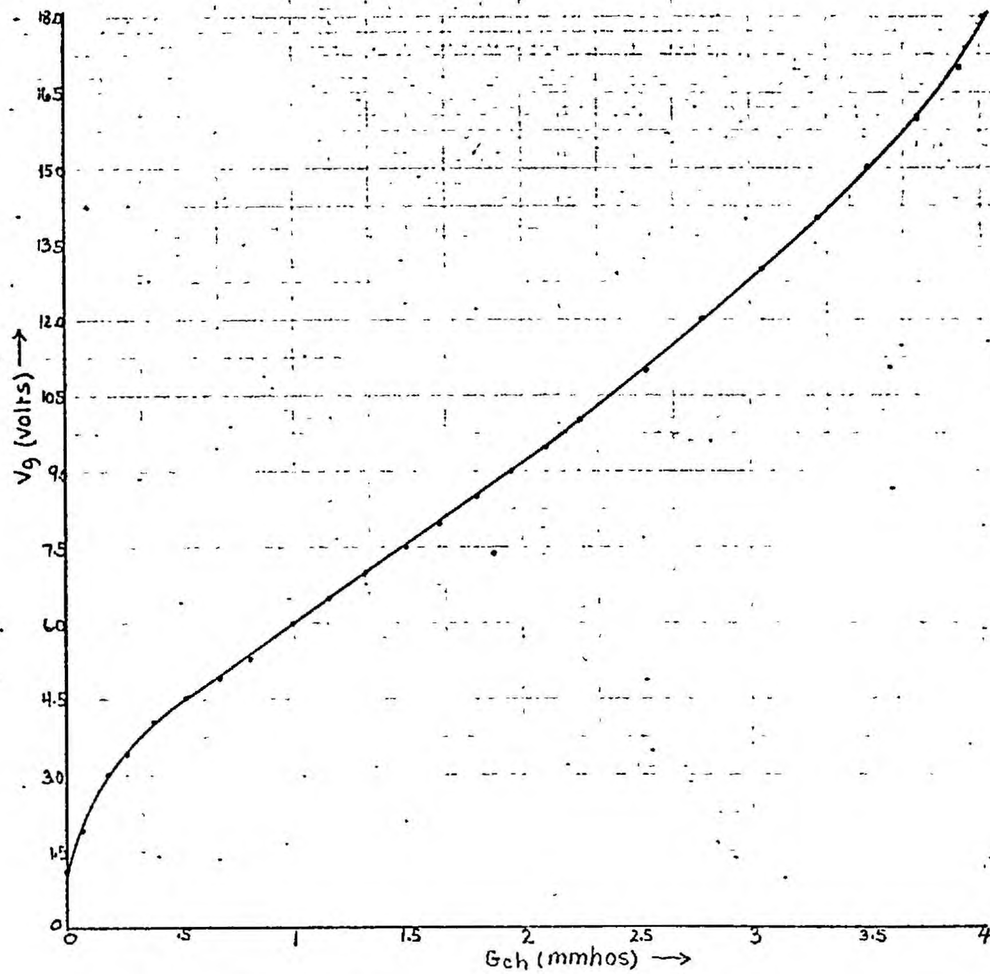


Fig. 3.3.11 : V_g Versus G_{ch} for Device MOST D

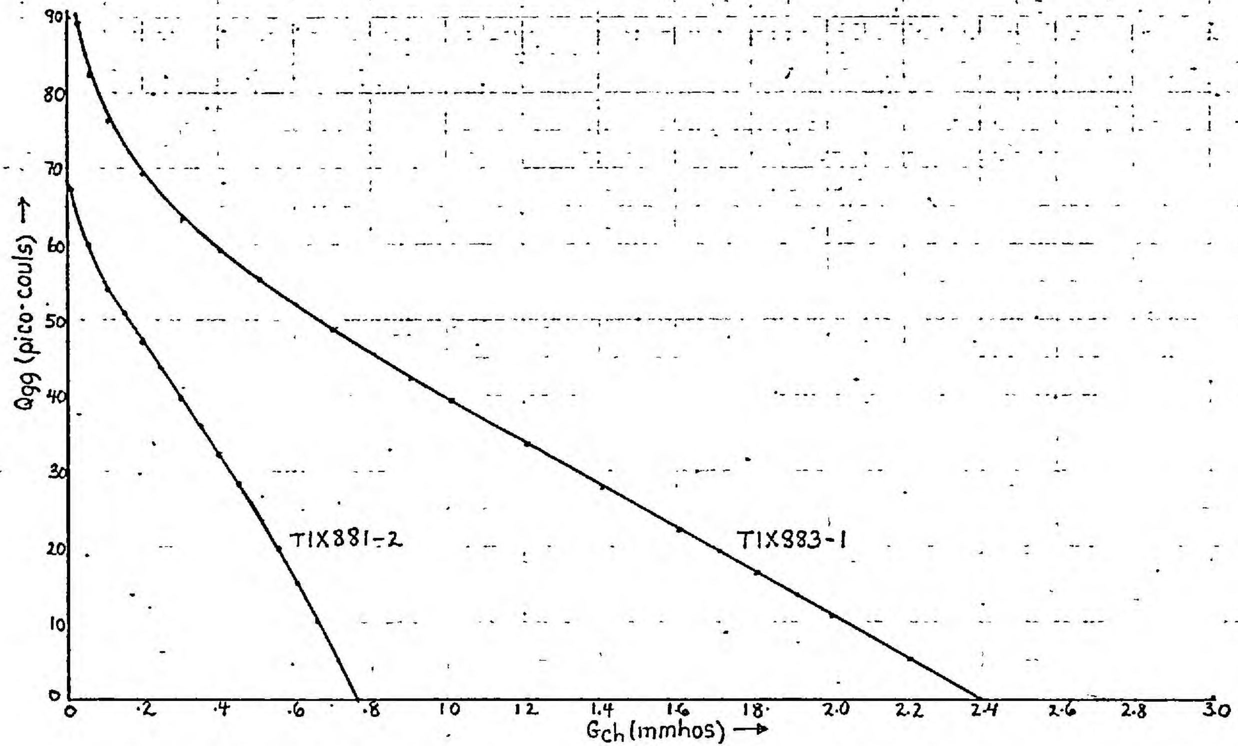


Fig. 3.3.12 : Q_{gg} Versus G_{ch} Relationship for Devices TIX881-2 and TIX883-1

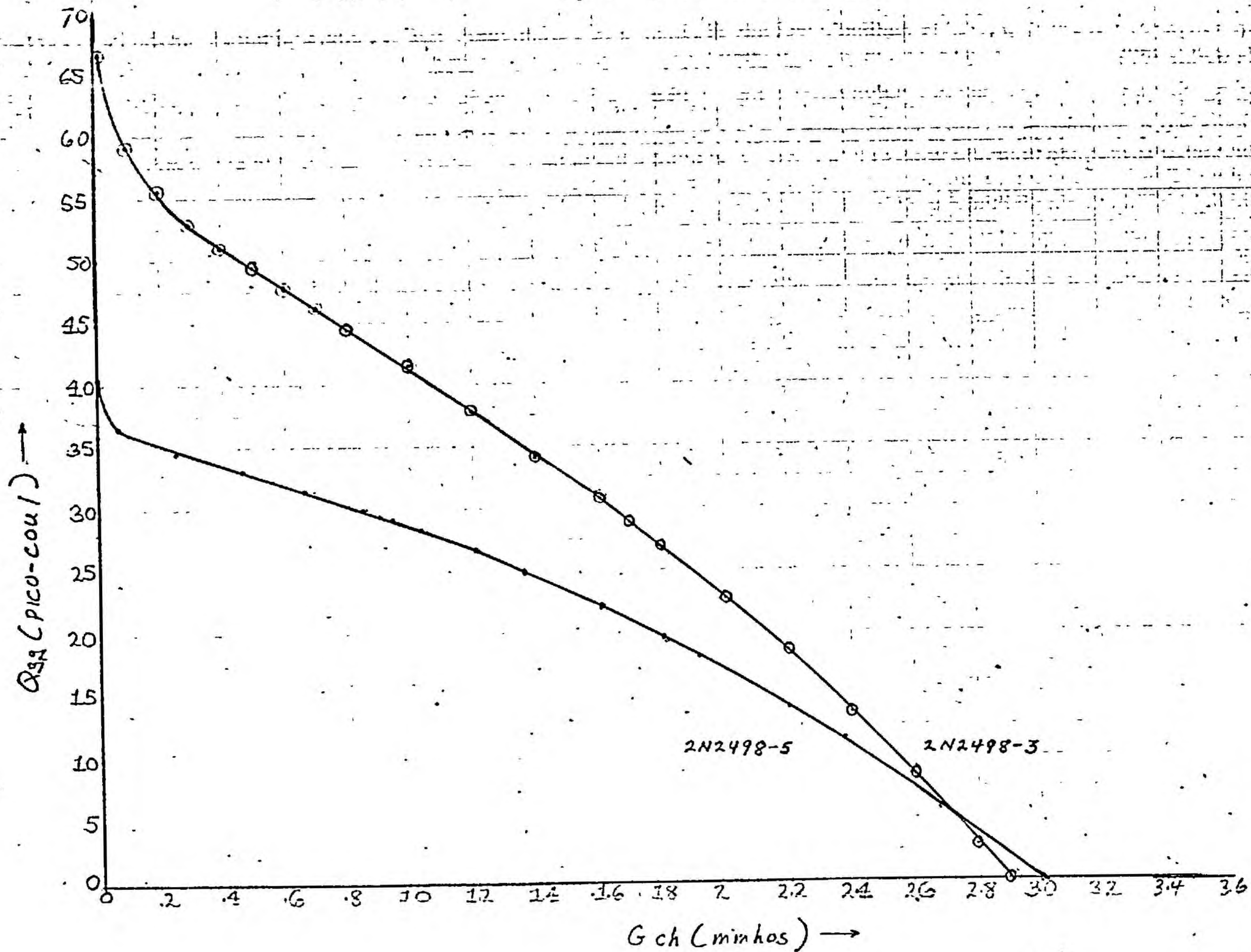


Fig. 3.3.13 : Q_{gg} Versus G_{ch} Relationship for Devices 2N2498-3 and 2N2498-5

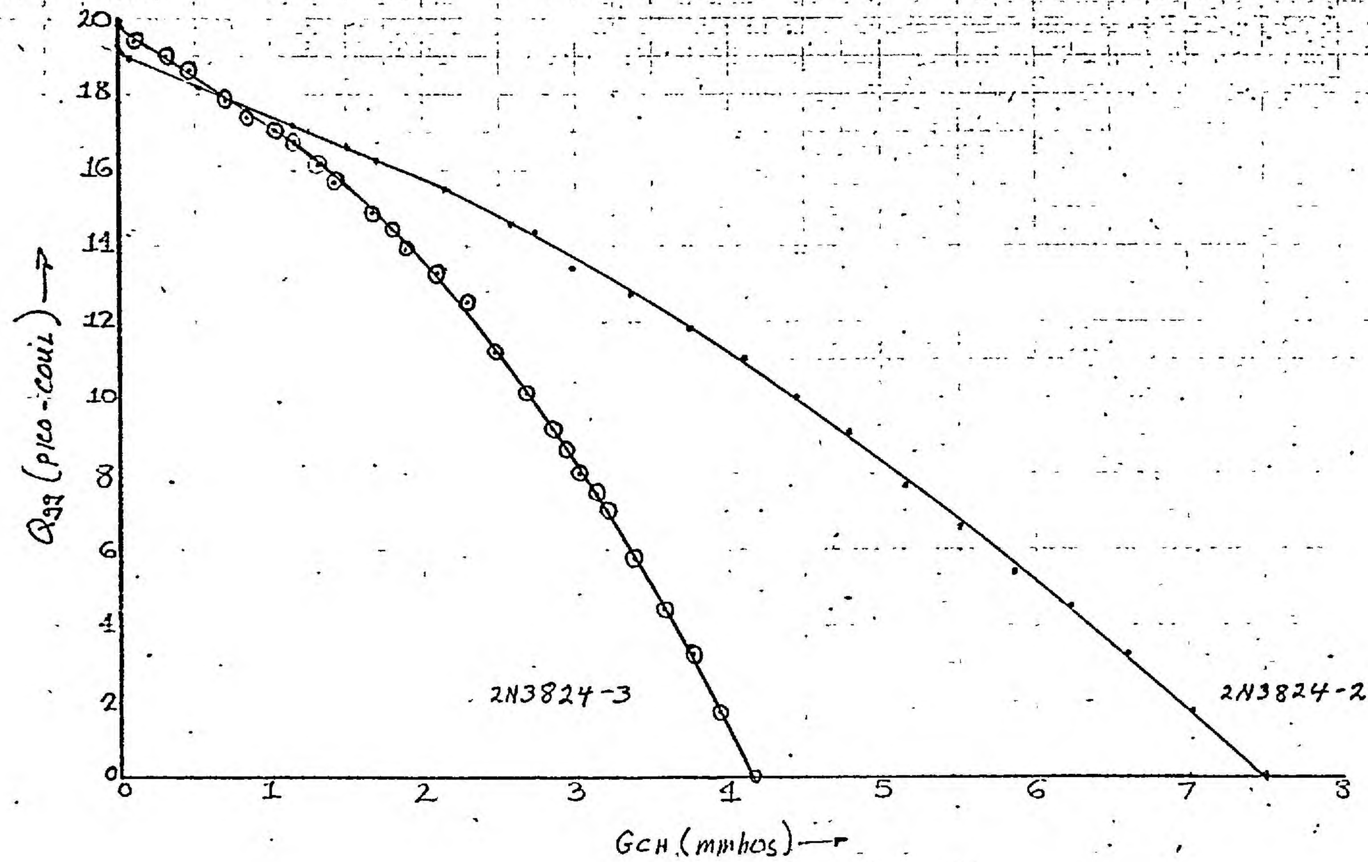


Fig. 3.3.14 : Q_{gg} Versus G_{ch} Relationship for Devices 2N3824-2 and 2N3824-3

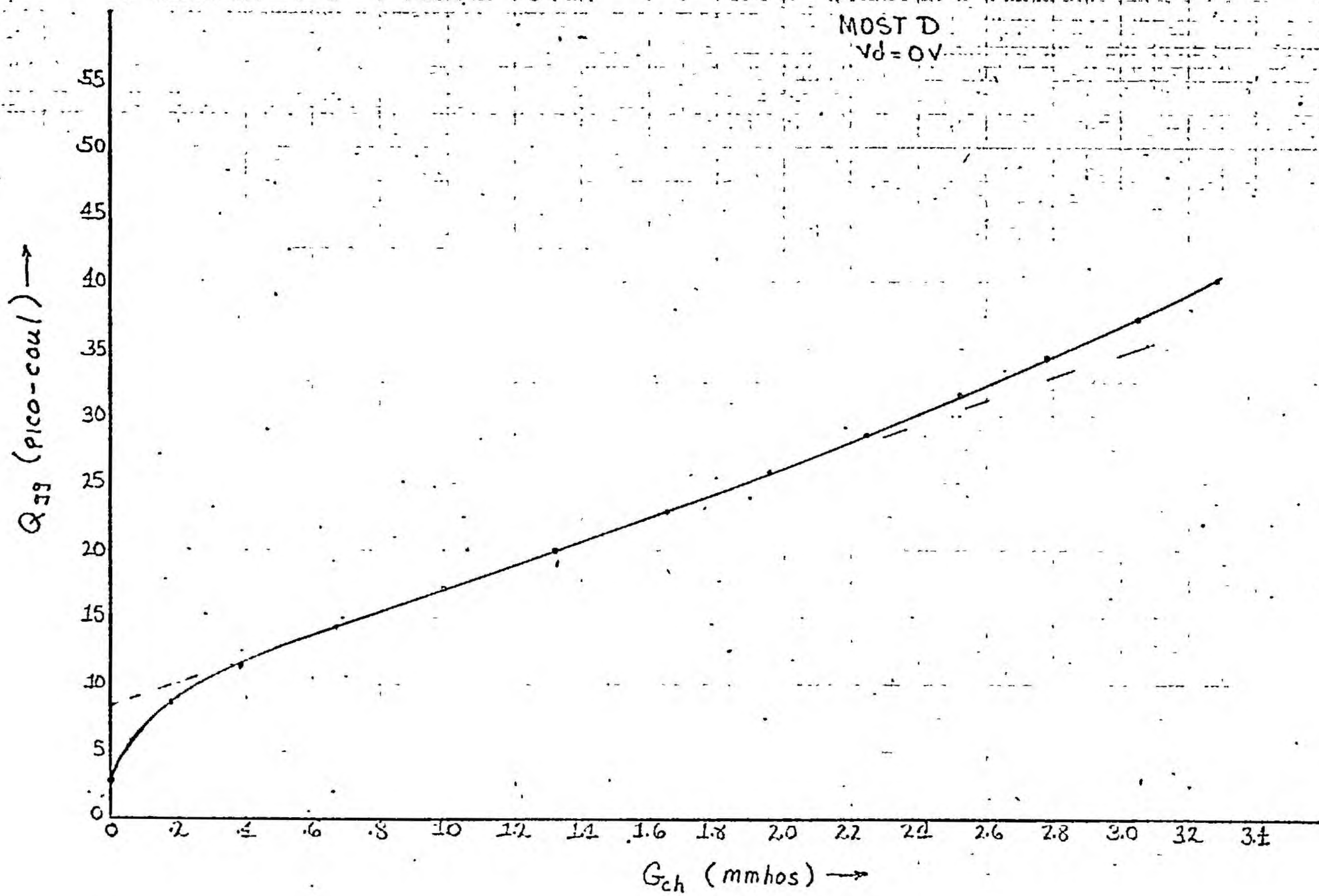


Fig. 3.3.15 : Q_{gg} Versus G_{ch} Relationship for Device MOST D

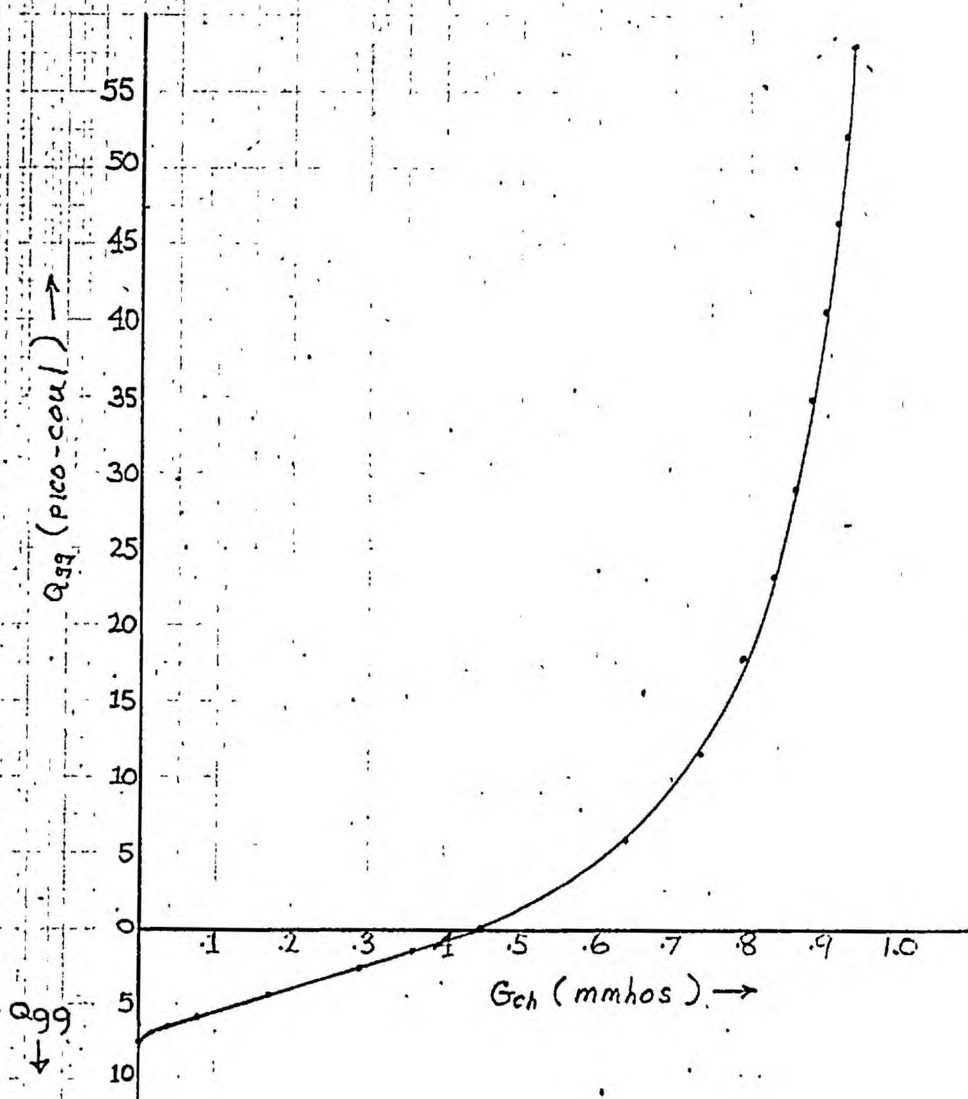


Fig. 3.3.16 : Q_{gg} Versus G_{ch} Relationship for Device MOST 6

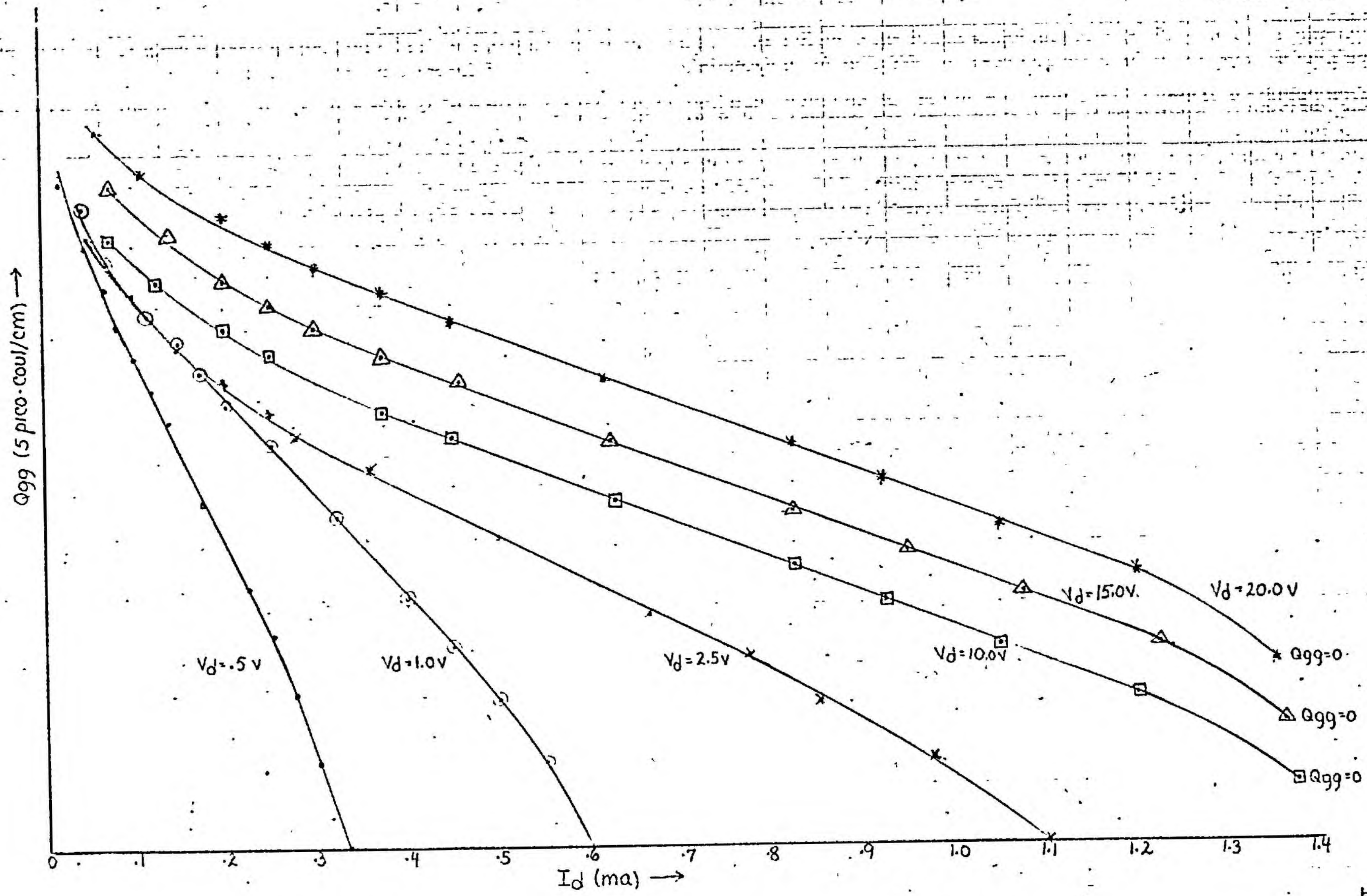


Fig. 3.3.17 : Q_{gg} Versus I_d Relationships for Device TIX881-2

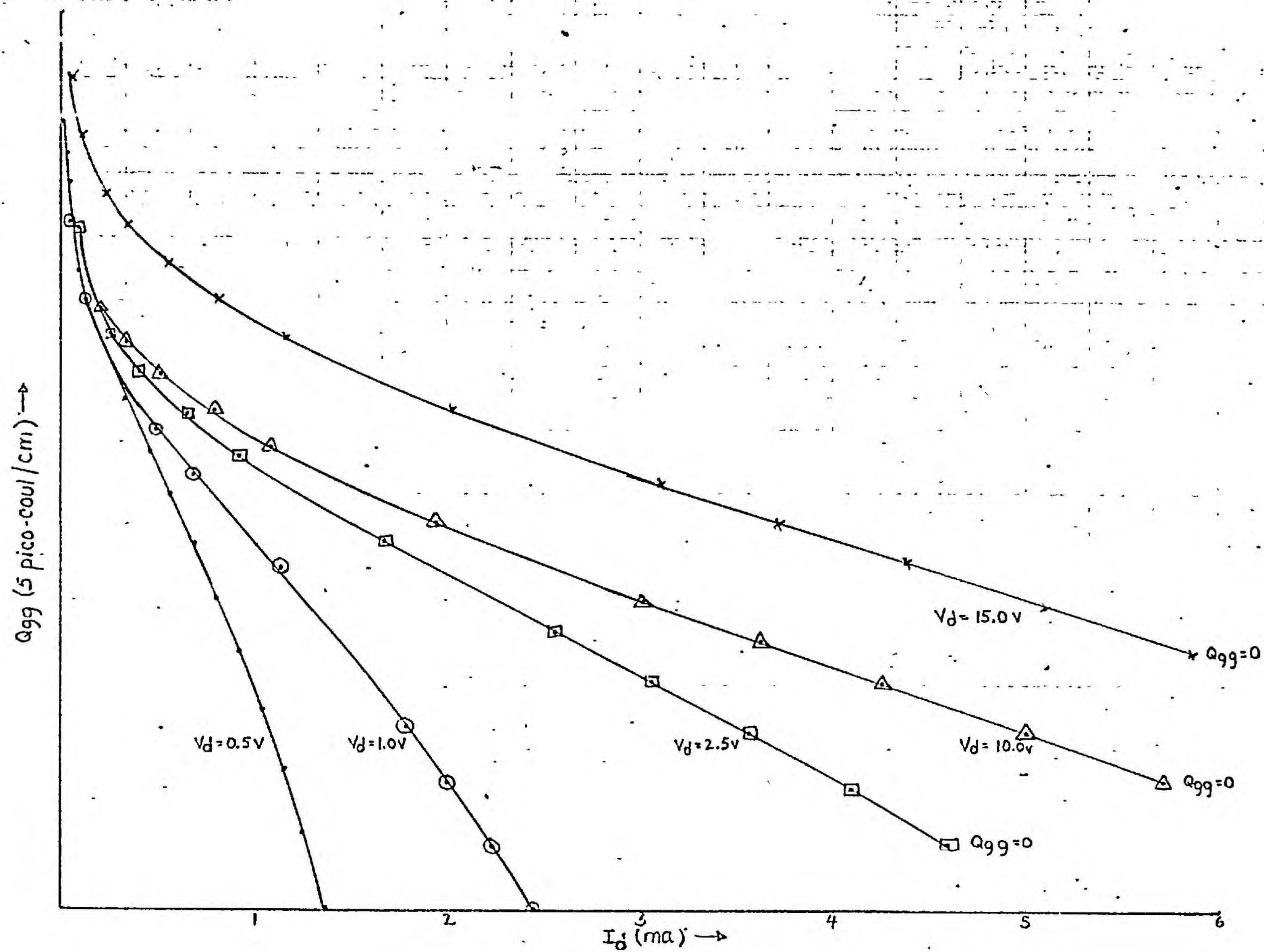


Fig. 3.3.18 : Q_{gg} Versus I_d Relationships for Device 2N2498-3

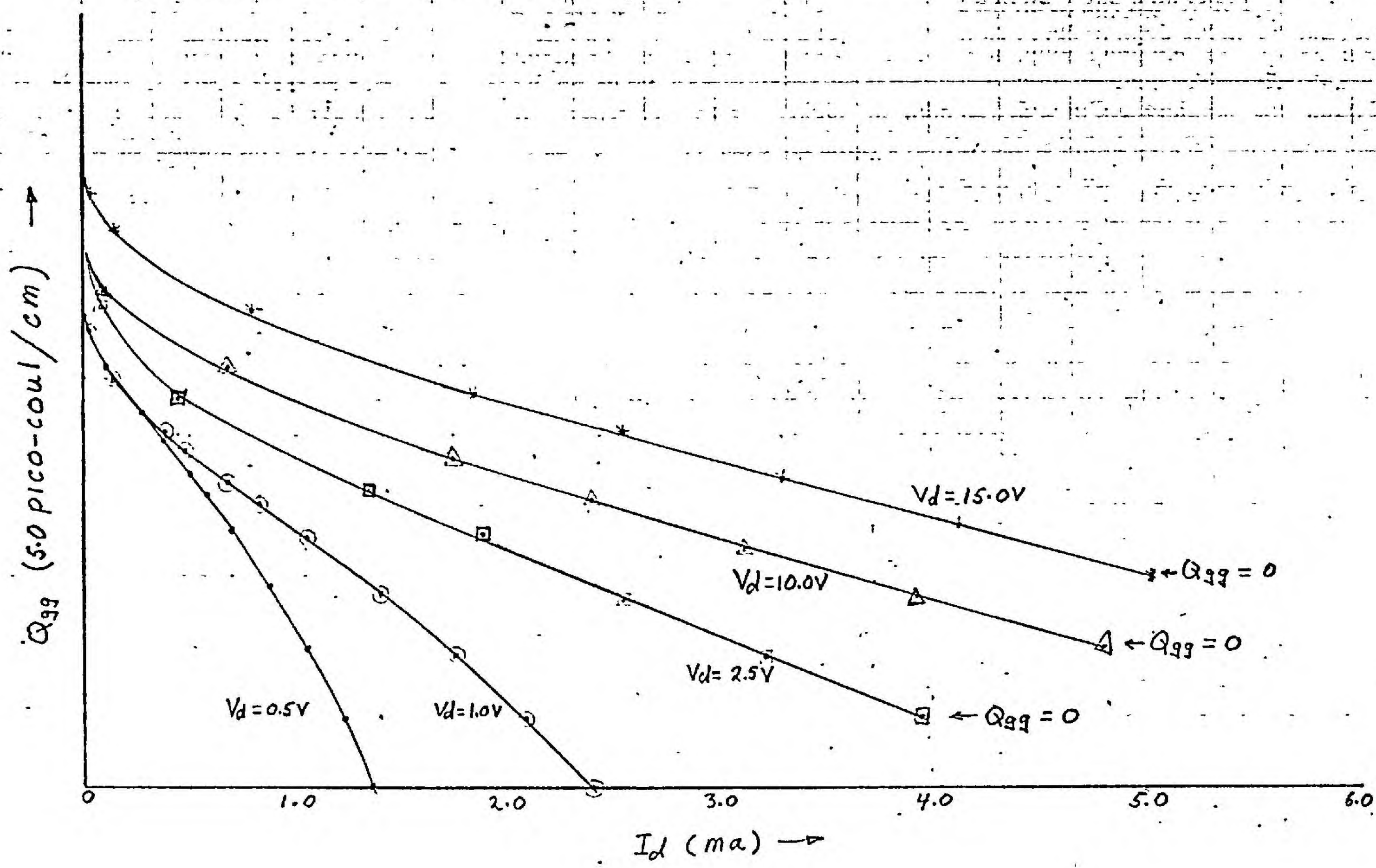


Fig. 3.3.19 : Q_{gg} Versus I_d Relationships for Device 2N2498-5

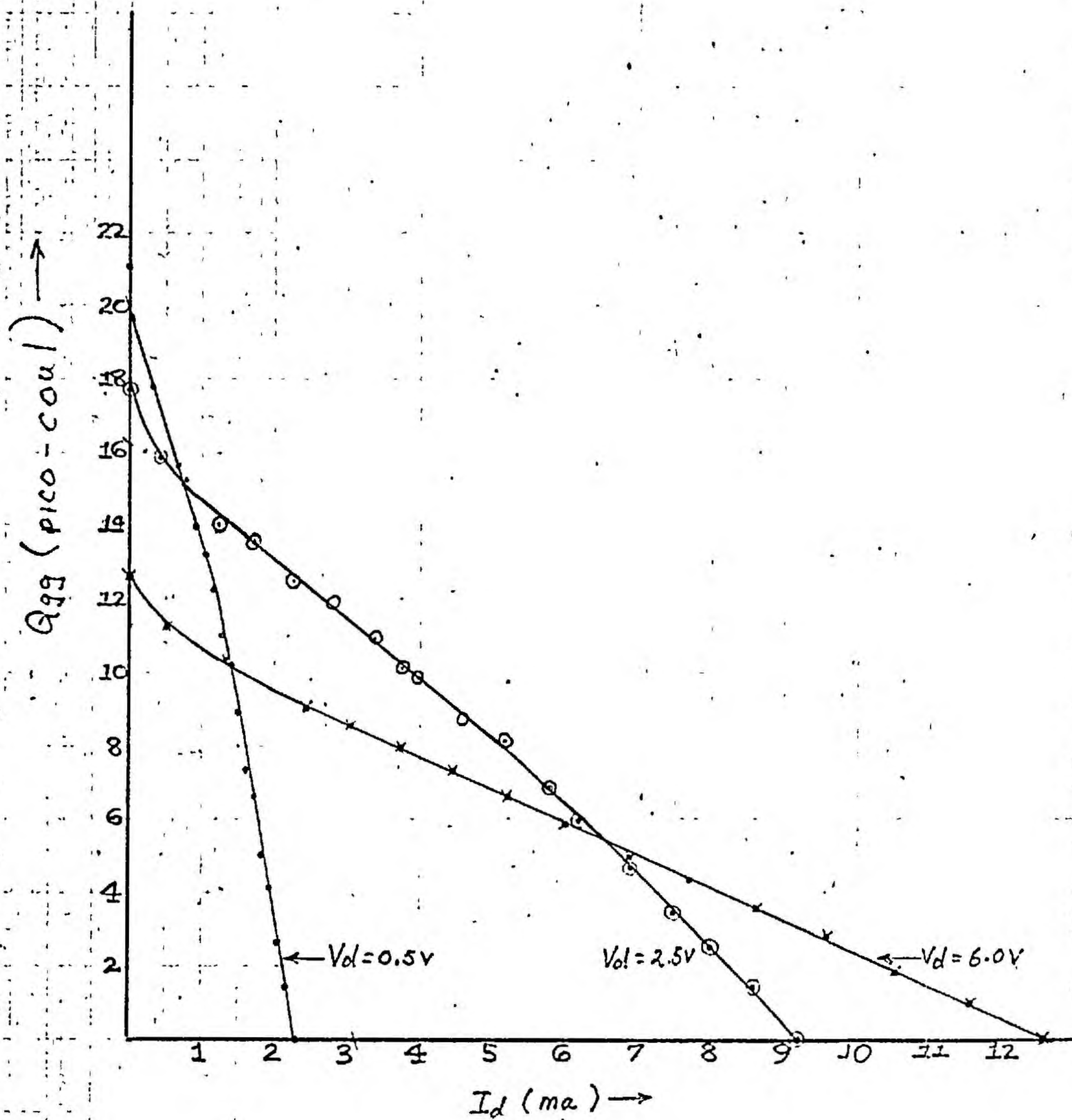


Fig. 3.3.20 : Q_{gg} Versus I_d Relationships for Device 2N3824-3

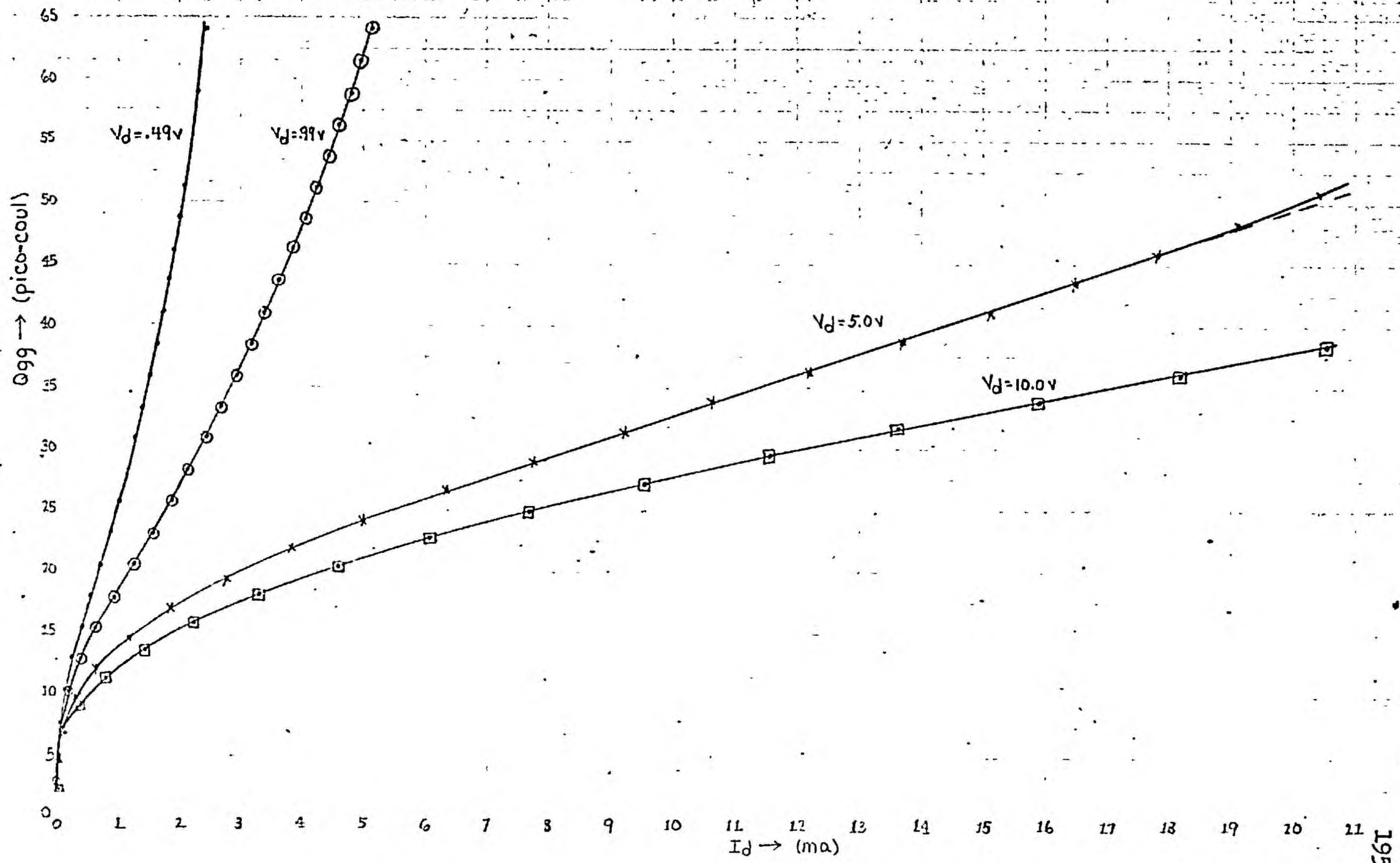


Fig. 3.3.21 : Q_{gg} Versus I_d Relationships for MOST D

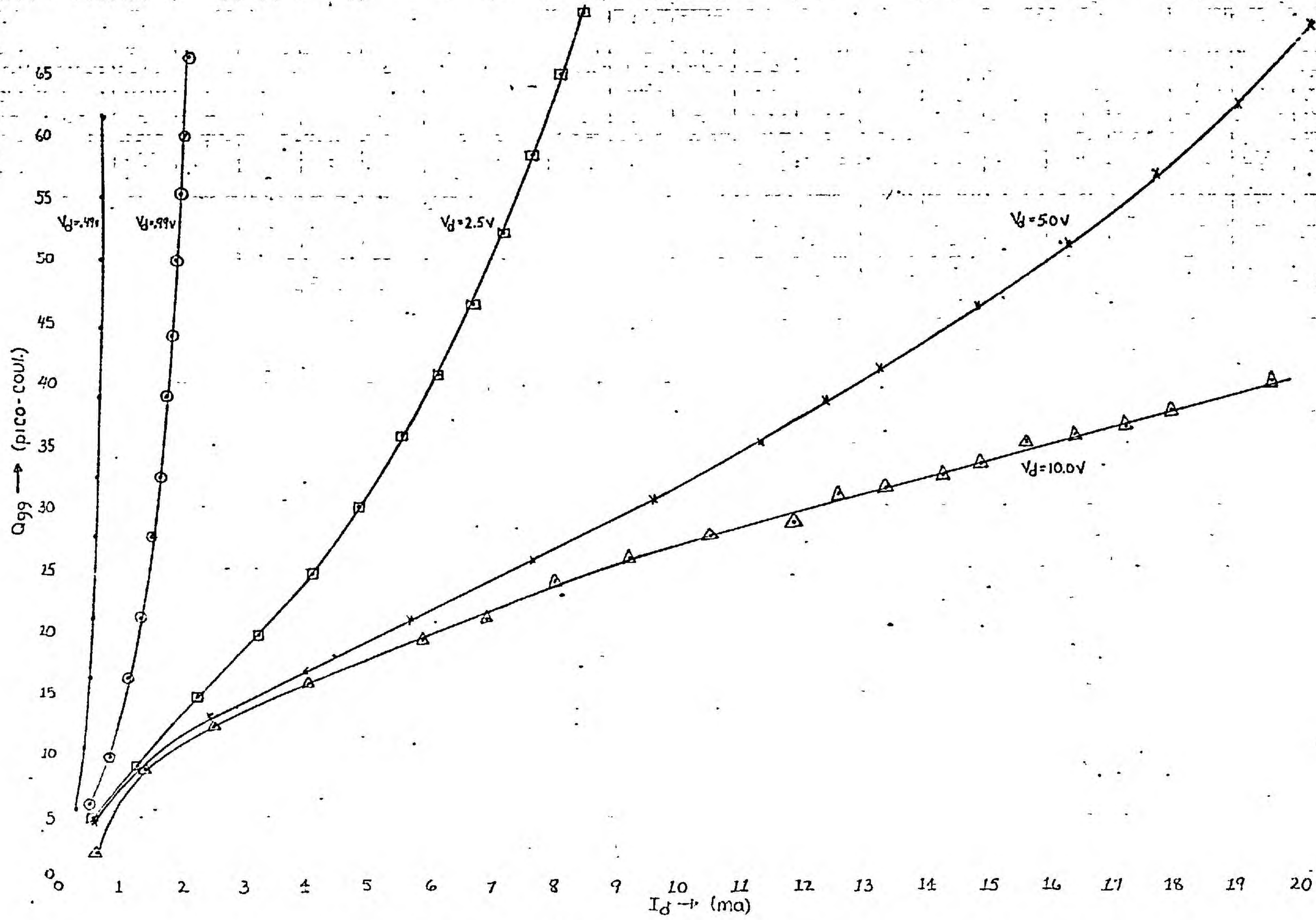


Fig. 3.3.22 : Q_{gg} Versus I_d Relationships for MOST 6

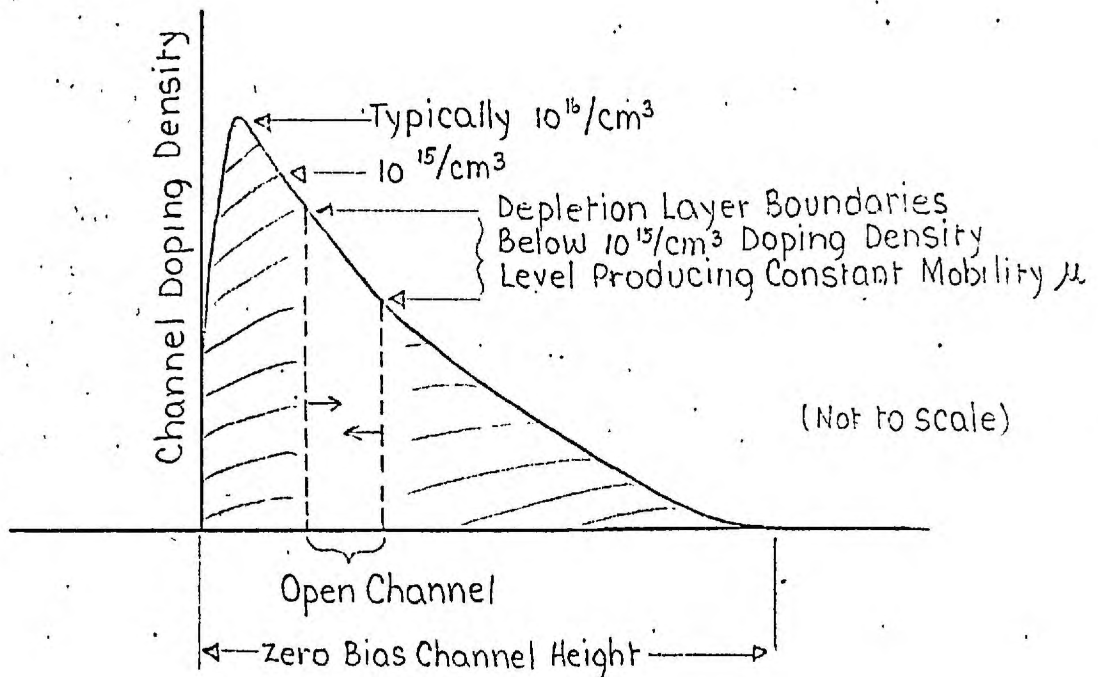


Fig. 3.4.1 : Illustration of Channel Doping Profile and Depletion Layer Boundaries for Constant Q_{gg} Versus G_{ch} Slope in Double Diffused Device

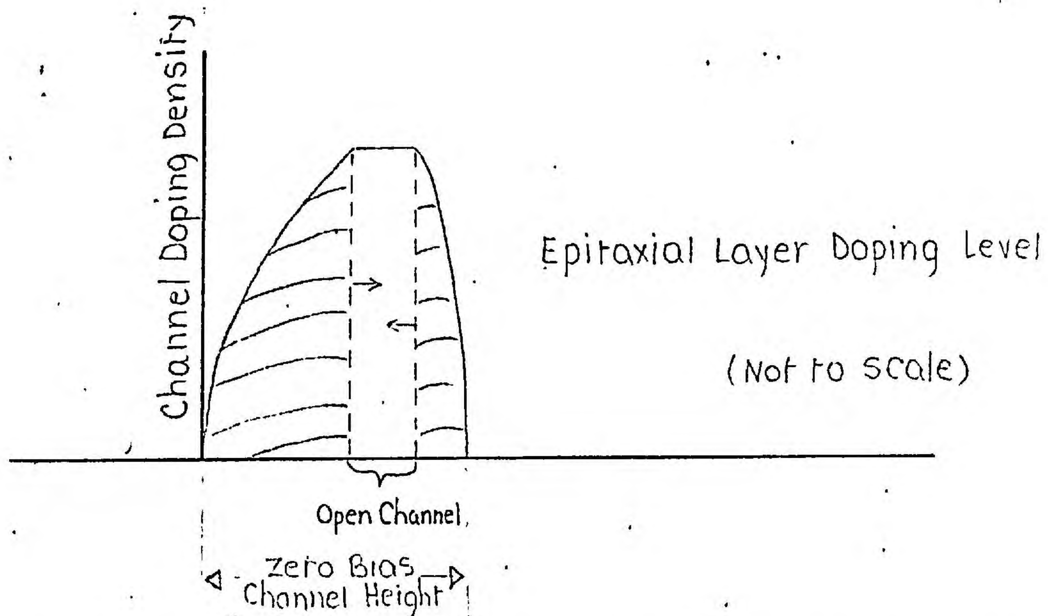
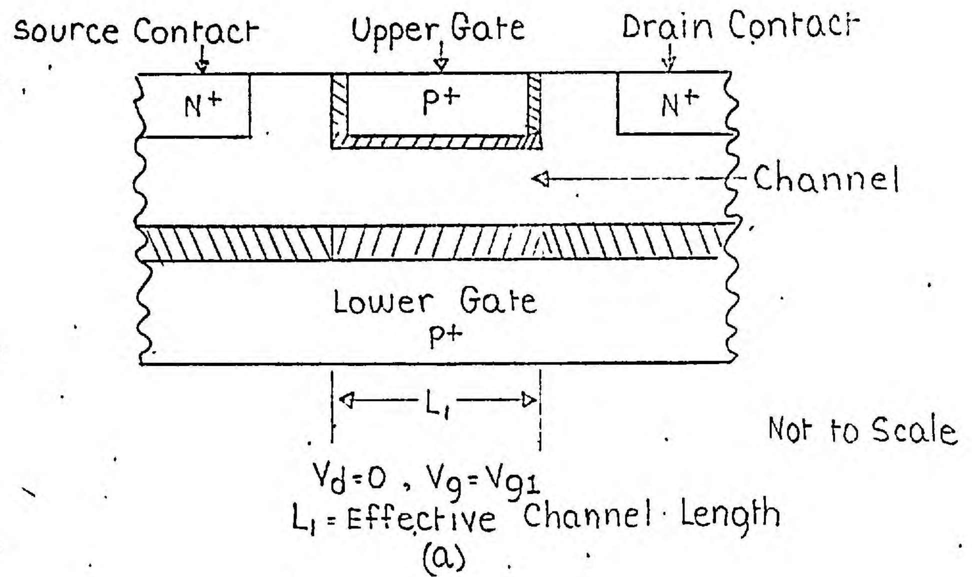
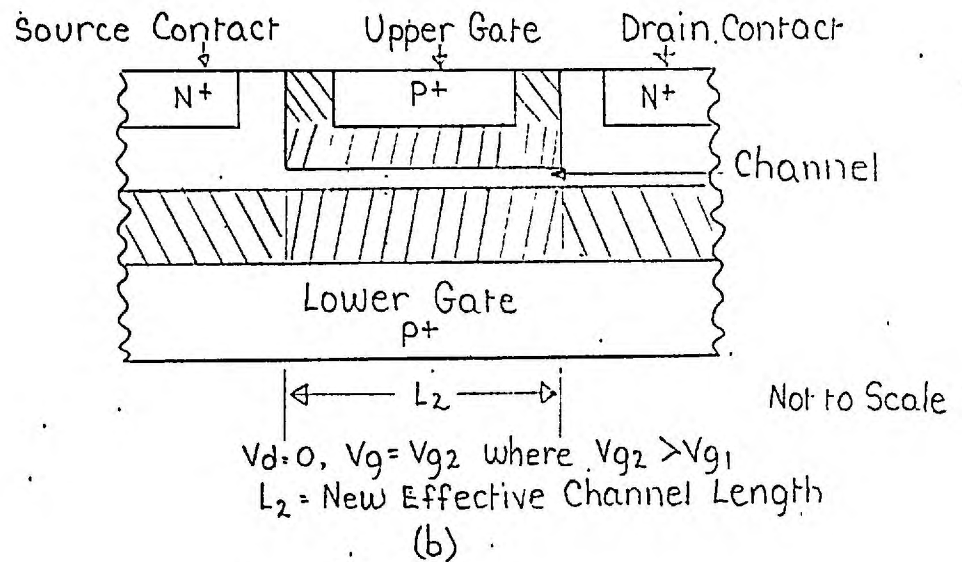


Fig. 3.4.2 : Illustration of Channel Doping Profile for Diffused Epitaxial Device Showing Depletion Layer Boundaries for Constant Q_{gg} Versus G_{ch} Slope

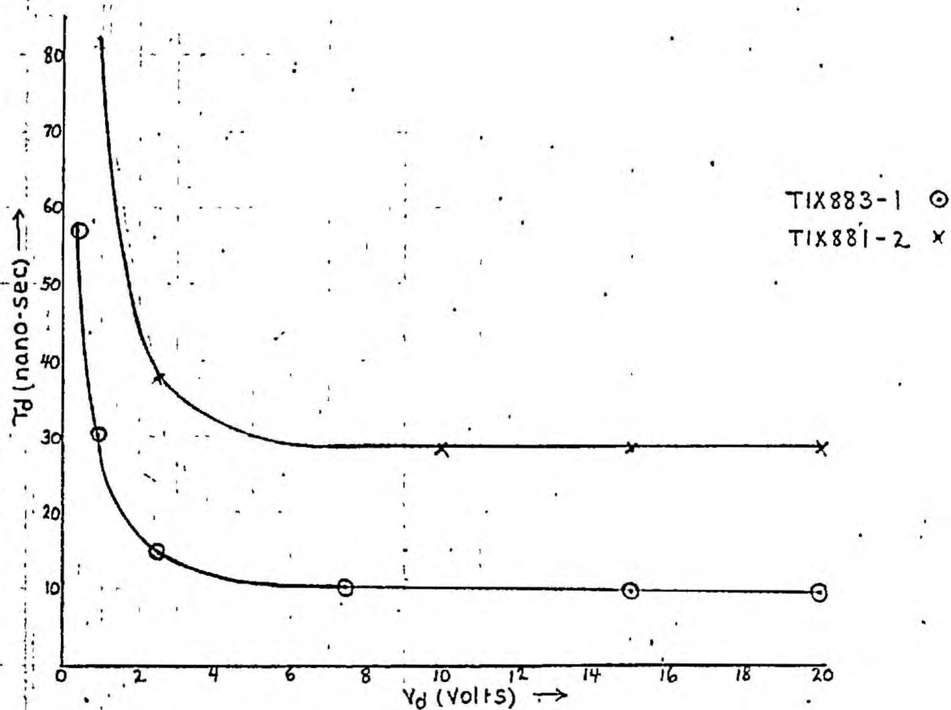




Active Depletion Layer Charge

Parasitic Depletion Layer Charge

Fig. 3.4.3 : Illustration of Formation of Effective Channel Length and Regions of Parasitic Charge in Diffused Structures



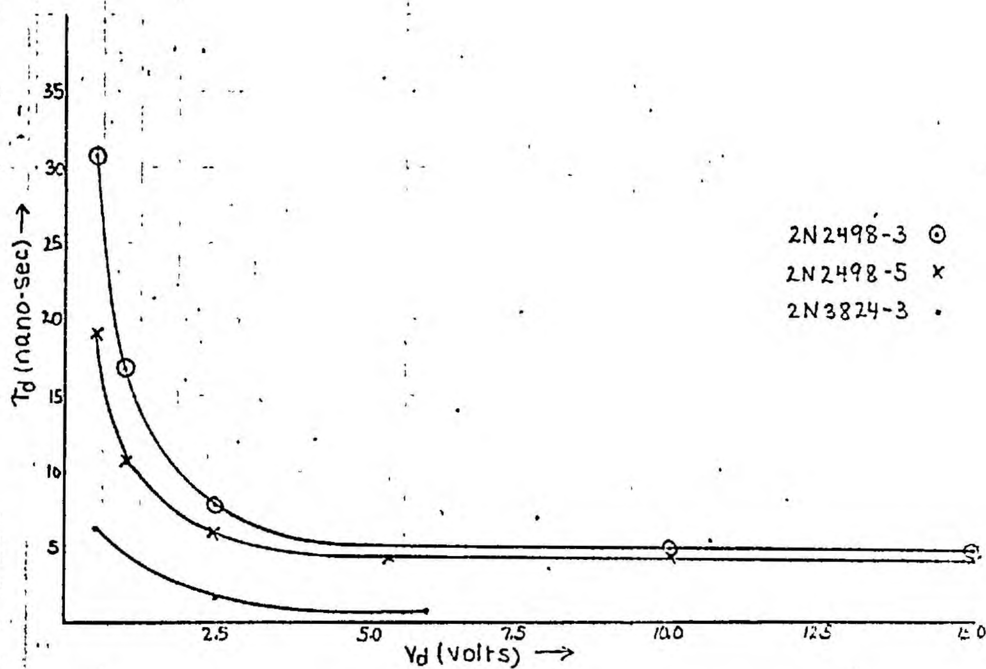
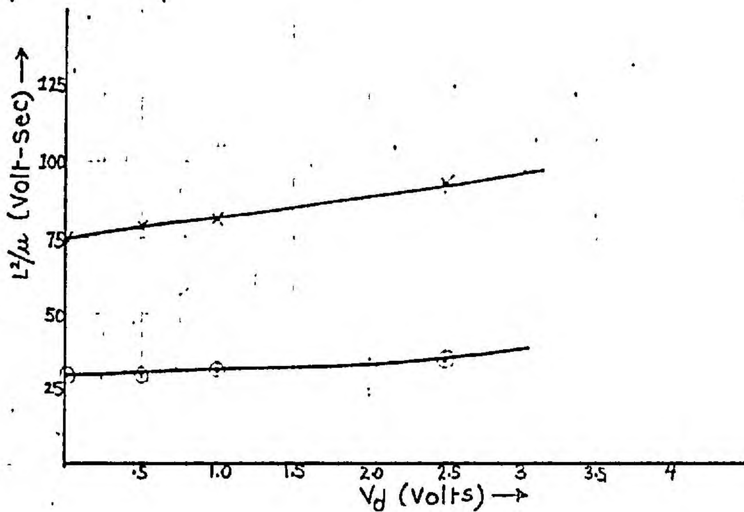
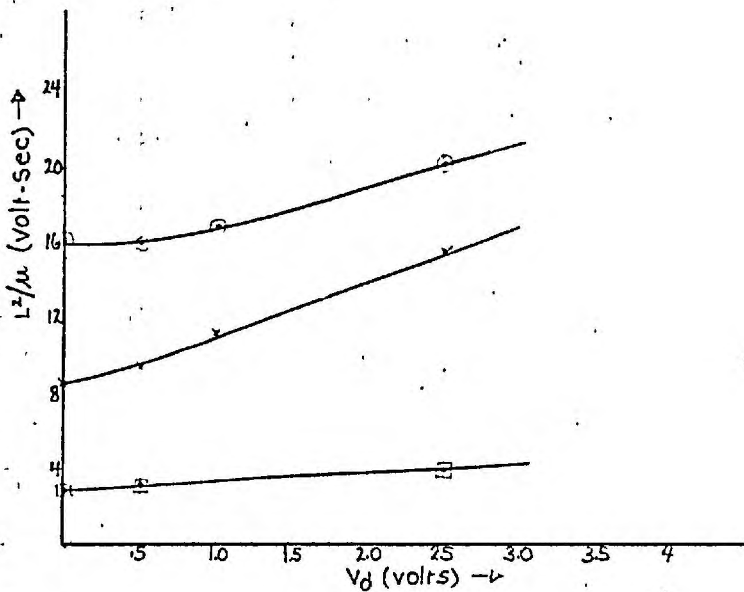


Fig. 3.4.4 : τ_d Versus Applied Drain Voltage V_d



TIX883-1 ⊙
TIX861-2 ×



2N2478-3 ⊙
2N2478-5 ×
2N3821-3 ⊡

Fig. 3.4.5 : L^2/μ Ratio Versus Applied Drain Voltage V_d

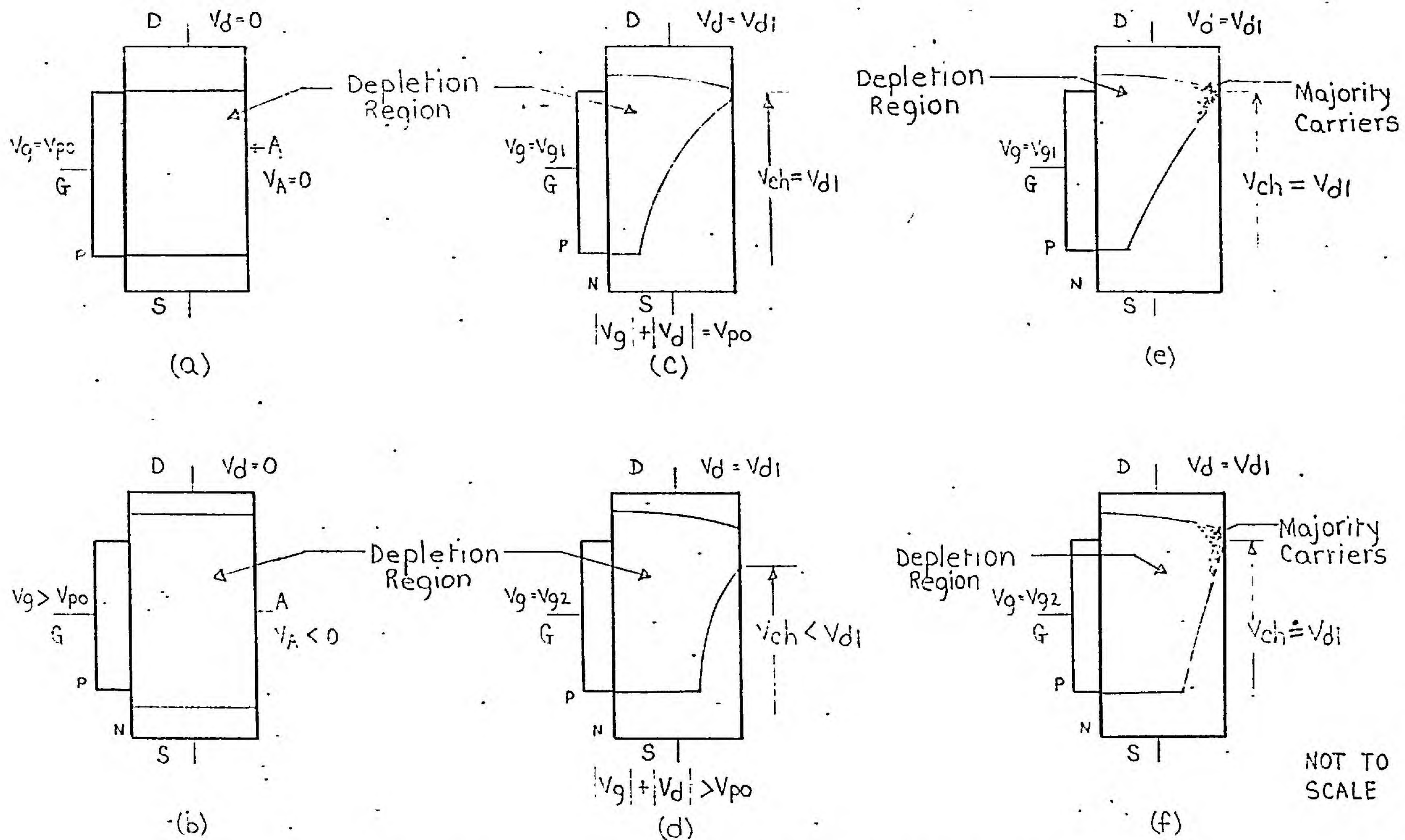
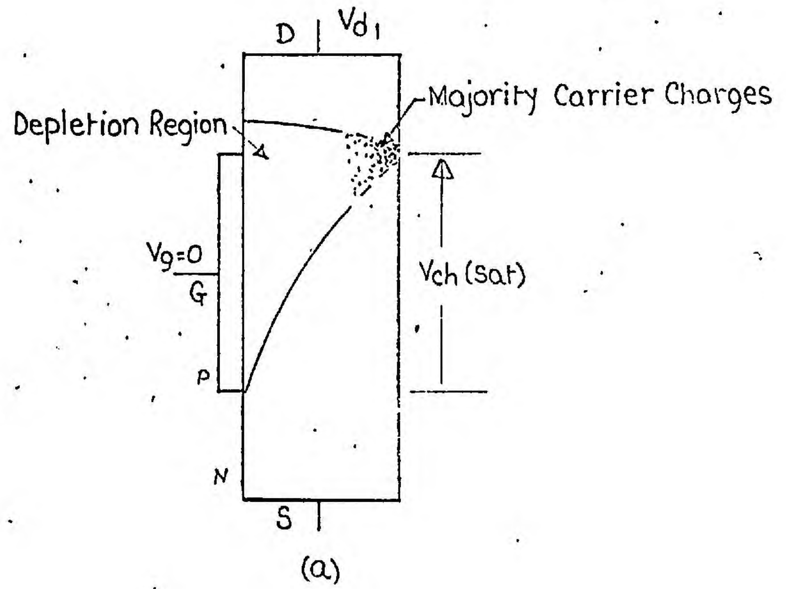


Fig. 3.4.6 : Illustration of "Pinch-Off" Conditions

(a,b,c,d assume depletion regions unaffected by I_d ; e,f as for c,d , but assume significant majority carrier charge in "depletion region" beyond active channel length)



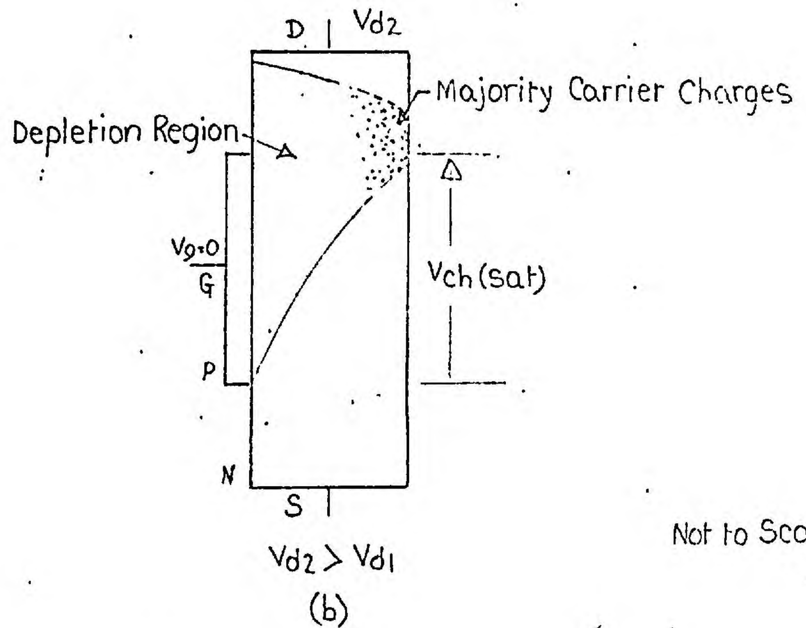
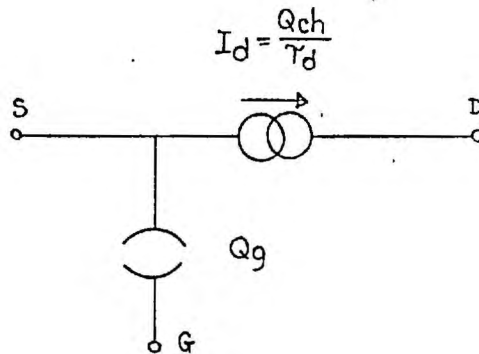


Fig. 3.4.7 : Illustration of Saturation with Majority Carrier Charge in Depletion Region for Two Values of Drain Voltage



$$I_d = \frac{Q_o - Q_{gg} - Q_{gd}}{\tau_d} = \frac{Q_o - Q_g}{\tau_d} .$$

where $\tau_d = f_1 (V_{ds})$ for true charge control operation *
and Q_o is derived from Q_{gg} versus G_{ch} relationship at $G_{ch} = 0$
(or from Q_{gg} versus I_d relationship as $V_{ds} \longrightarrow 0$)

* With departure from true charge control operation, τ_d depends on Q_{gg} as well as V_{ds}.

Additionally : V_{gs} is also defined by Q_g and V_{ds} via measured charge control relationships

i.e., $V_{gs} = f_2 (Q_g, V_{ds}) = f_3 (Q_g, Q_{gd}) = f_4 (Q_{gg})$

where Q_{gd} is obtained from Q_{gg} versus I_d relationships and f_4 is as measured for $V_{ds} = 0$

Fig. 3.6.1 : Steady State Terminal Charge Control Model for FET's

CHAPTER 4

APPLICATION OF THE CHARGE CONTROL APPROACH TO LOW LEVEL SWITCHING

4.1 Introduction

In presenting the charge-control models in Chapter 2, Section 2.6, some of the factors relating to modelling, switching performance, etc., were briefly discussed. It is intended in this chapter to consider further the various factors relating to the low level switching performance, and to develop and establish techniques for understanding and predicting the switching performance of devices under various circumstances.

The approach to this switching study is developed in Section 4.2 from the charge-control point of view, and is based on the work of the earlier chapters of this thesis. Modelling of device operation plays an important part in this study. This subject is considered further in Sections 4.3 and 4.4 where the various models used in this work are presented and discussed. Computer programs have been developed to facilitate convenient solution of the switching equations for the models concerned. These programs are presented and discussed also in Sections 4.3 and 4.4. The calculated and measured results pertaining to this study are presented and discussed in Chapter 5.

Throughout this work, the emphasis has been on providing a good understanding of the factors involved in the switching process, and its representation. Attention has thus concentrated on establishing the requirements for satisfactory representation (models) of device switching processes, and on developing tools (computer programs) for obtaining the desired switching solutions. The computer programs have been written

in the international standard programming language (Fortran IV) and thus can normally be used on most present-day computer installations without modification. The computer program is a convenient and labour-saving method of obtaining solutions of the processes expressed by the switching model. A computer program is thus closely associated with a given model, and is considered to be a logical and necessary extension of that model.

The models presented in Sections 4.3 and 4.4 are primarily intended for FET's rather than MOST's. Although the same approach is equally applicable to both devices, the MOST generally requires a slightly different form of model as was seen in Chapter 2, Section 2.6. Under certain circumstances, however, the FET models can be used to obtain result on MOST's. This will be considered in Chapter 6 where switching results for an MOST will be presented.

4.2 Low Level Switching Characterization

4.2.1 Chopper Considerations

This section is devoted to a brief consideration of the more important factors relating to the specific use of a field-effect transistor as a chopper or low level switch. The purpose here is to provide a basis for establishing the requirements for an adequate characterization of the FET in this application. Aspects related to the use of FET's as choppers have been considered by Fattal (34) and more recently by Barton (66). Much of the material used in the discussion in this section is taken from these sources. From comparisons, Fattal has shown that the drift performance of an FET chopper can normally be expected to be as good as, or better than, that of an equivalent bipolar transistor chopper. Barton has described a complete FET chopper amplifier which affords a considerable saving in components over an equivalent bipolar transistor chopper amplifier, and does not require a temperature controlled oven to obtain comparable results.

A chopper or low level switch commonly exists in two forms: the series chopper, and the parallel chopper. These can be represented in the steady state, neglecting leakage effects as shown in Figures 4.2.1 and 4.2.2. It can easily be seen from these figures that the equation describing chopper operation is simply

$$e_{out} = \frac{e_s}{1 + \frac{R_{ch}}{R_L} + \frac{R_s}{R_L}} \qquad (4.2.1a)$$

for the series chopper, and

$$e_{out} = \frac{e_s}{1 + \frac{R_s}{R_{ch}} + \frac{R_s}{R_L}} \qquad (4.2.1b)$$

for the parallel chopper, where

e_{out} = voltage fed to a-c amplifier

R_{ch} = resistance of FET switch in "on" or "off" state

R_s = resistance of signal source

R_L = chopper load resistance

e_s = source voltage to be chopped and amplified

It is immediately evident from equations 4.2.1 that in order to maximize the value of e_{out}, (i.e. maximize chopping efficiency), a large value of R_L must be used. With a given value of R_L, e_{out} then depends on the relative values of R_s, R_{ch} (on), and R_{ch} (off).

Fattal [34] has pointed out that there are three main sources of error in FET choppers which are associated with (1) variation of channel "on" resistance with temperature, (2) effects of leakage currents, and (3) effects of transients. It can easily be seen from equations 4.2.1 that variation in R_{ch} (on) with temperature results in an unwanted variation in the value of e_{out}. Various methods are used to minimize this effect, such as constant temperature operation, and use of feed-back. Possibly the most common, however, is to swamp out the effect by using a large value of R_L. Hence there is a second requirement for a large value of R_L. This will be shown to be an important consideration in Section 4.2.2.

Leakage current variations can result in an output variation pri-

marily in the "off" condition. Its effect is minimized by a small value of R_L, but in view of the requirements for high chopping efficiency, and low "on" errors, leakage current variations are usually compensated for by other means such as the use of a reverse biased diode having the same leakage current-temperature law as the FET.

Transient voltages associated with switching cause trouble in two main ways. The amplitude of the transient can overload or saturate the following a-c amplifier, and the transient duration imposes a fundamental limit on the chopping frequency. Characterization of these transients is the main concern of Chapters 4 and 5 of this thesis. The objects are firstly to consider the various device and circuit factors affecting chopper performance, and secondly to establish the requirements for a model to represent FET chopper consideration adequately.

4.2.2 Factors Relating to Switching Performance

4.2.2.1 Basic Device Processes

The basic switching process in the FET (see Chapter 2, Section 2.3) involves a transfer of charges from one side of the gate junction to the other. This transfer process adds to, or removes mobile majority carriers from, the channel, and thus at the same time directly increases or decreases the conductance of the channel. In being added to or removed from the channel, these carriers must themselves flow through some portion of the active channel bulk material in reaching the source or drain contacts. The resistance to their flow, and thus the rate of transfer of these charges, can therefore be expected to vary quite considerably throughout the switching transient.

As will be confirmed in Chapter 5, one of the results of this situation is that the transient produced as a result of turning the FET off (i.e. increasing channel resistance), is usually of considerably longer duration than the turn-on transient. Thus in the turn -off case, the channel resistance change tends to impede the transient build-up and decay, while the transient tends to be "shorted out" in the turn-on situation. The situation in the MOST is very similar. In this case, however, the charge particles added to or removed from the channel are removed from or added to the gate contact which is separated from the channel by an insulating oxide layer.

One further important deduction can be made from the above discussion. Differential charging , as indicated in Chapter 2, Section 2.6, can occur along the gate length. It can be seen, for example, that if a large external resistance is present between the source and drain (zero applied drain-source voltage is assumed) , the rate of transfer of charge carriers from or to the channel will be greater at the source end of the channel. The result of this situation is that during the early stages of the transient, the rate of change of channel resistance is greater at the source end of the channel than at the drain end. Additionally, it means that the rate of change of channel height at the source end of the channel is greater than at the drain end.

On the basis of the above, it can be expected that both the distribution of channel shape from source to drain, and the distribution of channel resistance from source to drain, will vary throughout the transient. Both the magnitude of the transient voltage, and the distribution of channel resistance at any time throughout the switching process, are

intimately tied up with the charge transfer process. Therefore, unless the correct distribution of charging (or discharging) along the length of the gate is accounted for throughout the switching transient, neither the correct overall channel resistance , not the correct transient voltage as a function of time, can be calculated. Hence, it can be expected that in general, more than one "lump" will be required in the charge control model to adequately represent the distributed nature of the charging (or discharging) currents throughout the switching transient.

In Chapter 2, Section 2.6, it was shown that the larger the number of "lumps" in the model, the better the effects of channel shape distortion were handled. It was further indicated that it was immaterial whether the cause of channel shape distortion was differential charging during a switching transient, or a large voltage gradient along the channel. It thus appears that a multi-lump representation is basic to these devices.

4.2.2.2 Device Parameters

The basic factors relating to the switching process are as indicated in the preceding paragraphs in this section. It can therefore be expected that anything which affects any of the related basic factors, will affect not only the switching performance of a device in a circuit, but also the adequacy of the representation of that device. In particular, it can be expected that the number of lumps required to represent the device to a given degree of accuracy will depend on both the parameters of that device, and the associated circuit parameters.

The important field-effect transistor parameters will be considered here. They are of course interrelated, but can be considered

to be : channel length (L), zero bias channel height (H), zero bias channel resistance (R_{cho}), and the L^2/μ ratio. The main effect of R_{cho} is to affect the rate of charging or discharging generally, particularly near the low channel resistance portion of the transient. The L^2/μ ratio, as was seen in the earlier chapters, directly relates to the amount of charge which must be transferred during switching to produce a unit change in channel conductance. Although the effective L^2/μ ratio may change in some devices throughout the transient as was indicated in Chapter 3, it is basic to the switching process, and will be used in the switching characterization as discussed in Section 4.2.3.

The channel length directly affects the channel resistance, but it also directly relates to the distributed nature of the device. Thus, by itself, and in conjunction with the channel height, the channel length relates to the amount of channel shape distortion, and to the distribution of charging currents during the switching process, and hence affects the number of lumps required to represent the device.

In the MOST, it can be seen that Q_o (equation 2.4.8) and the L^2/μ ratio directly affect the switching charge requirements, and consequently the switching times, for this device. Q_o determines the amount of charge from zero which must be added to or removed from the channel to just produce channel conduction. As with the FET, the MOST L^2/μ ratio relates to the amount of charge which must be transferred to produce a unit change in channel conductance. Also in the MOST, the channel length L relates to distributed effects, and thus the distribution of charging (or discharging) currents along the channel.

4.2.2.3 Circuit Parameters

In addition to the parameters of the device itself, the switching process and its description can be expected to depend on such circuit factors as load resistance (R_L), load capacitance (C_L), applied source drain voltage (V_d), gate driving resistor (R_g), gate driving voltage (E), and, of course, stray capacitances. It can be expected that R_L in conjunction with C_L will generally slow down the switching process. In addition, as indicated earlier, R_L affects the distribution of charging currents from source to drain, and also tends to increase channel shape distortion. In Section 4.2.1, it was shown that a large value of R_L is desirable from the point of view of obtaining a high chopping efficiency. As a result of this requirement, more lumps will be required in the model than would otherwise be necessary.

Note that the effect of R_L on the switching transient and on device representation, can be expected to vary somewhat, throughout the transient. In the turn-off situation, for example, R_L can be expected to have an important effect on the rate and distribution of charging (or discharging) during the part of the transient when the channel resistance is small. If the channel resistance becomes large compared with R_L, it can be expected that R_L in conjunction with C_L will become the limiting factor in the decay time of the switching transient. Hence, in the chopper application, some compromise is usually necessary between the chopping efficiency, and the chopping rate.

The series drive resistor R_g directly affects the rate of switching throughout the whole process. A low value of R_g speeds up the switching transient, but in addition, it can generally be expected to increase

the severity of any differential charging and channel shape effects due to the presence of a large R_L ; there thus tends to be the need for more lumps than are required when working with higher R_g values.

Values of applied drain voltage V_d under true low level switching conditions can be expected to have a negligibly small effect of the switching process. Large values of drain voltage, as was seen in Chapter 2, can distort the channel shape sufficiently to require more than one lump to represent the device. The gate driving voltage E, as well as determining the amount of charge added to or removed from the channel, also affects the rate of charge transfer. It can therefore be expected that large values of E , just as with low values of R_g, will tend to emphasize the distributed effects of the device, particularly when a large value of R_L is present, so making necessary more lumps in the device model in order to adequately represent the switching process.

4.2.3 Approach to Device Switching Description

4.2.3.1 General Considerations

On the basis of the previous discussion in this chapter, and from the results in Chapter 3, it can be expected that adequate characterization of the switching process in practical field-effect transistors cannot generally be achieved with a very simple model. Part of the reason for this as indicated in Section 4.2.2 is the essentially distributed nature of these devices from source to drain. The distributed channel and gate length are fundamental to device operation and are intimately related in a particular device to the time-dependent charge transfer process, and correspondingly, the time-dependent channel resistance relationship during switching.

As indicated in Chapter 3, as manufacturing technology advances, it can be expected that devices with shorter channels than those presently available will be forthcoming. Even then, however, it is unlikely that the distributed charging effects will ever become completely negligible. In addition, it is to be expected that channel shape distortion effects will become more severe as the channel length is reduced in relation to the channel height. As was seen in Chapter 2, Section 2.6, this can actually result in a requirement for more lumps in the model to adequately represent such a device.

It thus appears that there are opposing tendencies involved in representing the device which are closely related to channel length. A device with a very long channel can be expected to require several lumps in its model to account for the flow of charging (or discharging) currents along the channel length. In a device with a very short chan-

nel, on the other hand, the rate of change in effective channel height is very large, requiring in general several lumps to account for the effects of channel shape distortion.

Representation of field-effect transistor action is further complicated by the fact that its operation depends on pliable, non-fixed boundaries (depletion layers). Not only can the effective channel height vary along the channel length, and by different amounts throughout the switching process, but the effective channel length can vary in some devices in certain ranges of operation as discussed in Chapter 3. Related also is the fact that significant parasitic FET action can occur in some devices as a result of depletion layer spreading beyond the ends of the effective channel length.

In a double gate device whose gates are tied together, it is impossible to separate and characterize the action of each gate. Thus, it is difficult to work in terms of junction voltage laws, particularly in the case where the doping density in the channel is not constant (eg. a diffused device). In such a case, the law for each junction can be affected by variations in doping profile, and by an effectively varying junction area (i.e. depletion layer spreading). Related also to channel doping density variation, is majority carrier mobility variation as discussed in Chapter 3. It was shown that this can introduce a complication by resulting in a non-proportional relationship between channel charge and channel conductance in some ranges of this relationship.

The approach to the switching characterization of FET's (and MOST's) adopted here is that of charge control, and centers specifically on the

gate charge versus channel conductance relationship with zero drain voltage. The result is a model with one or more lumps as indicated in Chapter 2, Section 2.6. Once characterized, each lump can be considered to be equivalent to one of several independent FET's (or MOST's) in series. Further aspects relating to the practical application of such a model will now be discussed.

4.2.3.2 Effective L^2/μ Ratio

The parameters for the model for a given device are obtained from a Q_{gg} -G_{ch} plot measured as described in Chapter 3. The effective slope of this plot (L^2/μ)ratio) is not generally constant throughout its complete range. In its non-constant range, however, as illustrated in Chapter 5, Section 5.3, it can if necessary be approximated by one or two sections of constant slope. Thus for use in the charge control model, generally more than one value of effective L^2/μ ratio must be used to cover the complete conductance range of a given device. It will be shown in Sections 4.3 and 4.4 that this requirement is conveniently incorporated in the computer programmed solution of the models.

In the general case, derivation of an effective L^2/μ ratio from the measured data ensures that the total device charge-conductance relationship is properly characterized. It is then implied in the model that all depletion layer charge in an FET is active in modifying the conductance of the channel. Parasitic charge in the depletion layers at the ends of the active channel length does not, however, bear a constant ratio to the remaining depletion layer charge throughout the complete Q_{gg} range, and is therefore impossible to characterize accurately in such a model.

Where significant parasitic charge exists, this method of specifying the model can be expected to produce some inaccuracy in the distribution and rate of charging (or discharging) currents during a switching transient. The effect, in the model, is to place more bulk resistance in the path of more charge carriers than should be the case, and therefore to slow down the switching process slightly. The degree of inaccuracy introduced is undoubtedly related to the speed of the switching process, being less severe at lower switching rates.

4.2.3.3 Q_{gg} -V_g Relationships

One further device relationship is required in order to obtain a solution from the charge control model. This is the relationship between gate charge Q_{gg} and applied gate voltage V_g , and it is obtained in the process of arriving at the device Q_{gg} - G_{ch} plots from the measurements previously described for that purpose. Since these quantities are related by some "power" , it is convenient to plot Q_{gg} versus V_g on log-log graph paper , as will be shown in Chapter 5 , Section 5.3, for several devices.

Assuming an ideal junction on the basis of complete depletion, the charge-voltage relationship is obtained from basic diode junction theory as[49]

$$(Q_{gg} + Q_{eqm}) = K\,(V_g + \psi_{o})^{n} \qquad (4.2.2)$$

where

Q_{gg} = uncovered depletion layer charge due to the application of reverse bias V_g

Q_{eqm} = uncovered depletion layer charge under equilibrium conditions with zero applied reverse bias

K = a constant involving junction area and doping densities

V_g = applied reverse bias junction voltage

ψ_o = equilibrium barrier potential

and n = junction "power" ; 1/2 for "abrupt junction, and 1/3 for "linear" junction

In the single gate junction FET case, assuming the above relationship, ψ_o can be obtained as described in Chapter 4 from gate capacitance measurements by plotting $\frac{1}{C_g^n}$ versus V_g if the value of n is known. A plot of $(V_g + \psi_o)^n$ versus Q_{gg} could then be used to determine Q_{eqn} and K, and hence complete the junction characterization.

In practical single gate junction FET's, the situation is somewhat complicated by factors which can effectively result in non-constant values of K and n. In particular, as was discussed in Chapter 3, significant depletion layer spreading can occur around the ends of the gate junction, especially in the range near pinch-off. In addition, particularly with diffused or epitaxial junctions, the power law can vary throughout the range from "linear" to "abrupt" in various parts of the channel depending on gate voltage.

In practical double gate structures, particularly with both gates internally tied together, the situation is considerably more involved. Especially in double diffused structures, it can be expected that the power law for each junction will vary, and not necessarily in the same way or by the same amount.

The method used here is completely general and can be used for FET's with single gate junctions or double gate junctions with any

doping density profile or profiles. It consists of representing the device $Q_{gg} - V_g$ relationship throughout the whole range below pinch-off by one or more straight line segments on the log-log graph, as required. Just as with the effective L^2/μ ratio, this requirement is conveniently incorporated into the computer programmed solution for the model. Note that the MOST is a special case of the above, with an effective "junction power" of one, since the gate capacitance is usually constant for low drain voltages as was shown in the results in Chapter 3.

G_{cho}, obtained from the $Q_{gg} - G_{ch}$ plot, is also required by the charge control model. Thus, all the required information for device characterization, is derived in the course of obtaining the device L^2/μ ratio. The application of this approach will become further clarified in subsequent sections of this chapter, and in Sections 5.2 and 5.3 of Chapter 5.

4.2.3.4 Other Approaches

It is perhaps helpful to compare briefly the charge control approach used in this thesis with that of others reported in the literature (67-72) on FET modelling. With one main exception, notably that of Hudson, Lindholm and Hamilton (71), discussed below, other work has concentrated on small signal resistance-capacitance-generator models, valid over a range of operating frequencies, and for a given set of bias conditions, and often only for an FET with a specific structure (eg. single abrupt gate junction). The work of Richer (70) is valid for an arbitrary channel doping profile, but is intended only for small signal, low frequency applications.

The work of Hudson, Lindholm and Hamilton (71) is notable in that theirs is a transient resistance-capacitance-generator model. It is valid however, only under small signal conditions (i.e. for small perturbations about the gate voltage operating point. Again, the model is valid only for an assumed structure, in this case, a double "abrupt" junction structure with independent access to each gate. The model is interesting, however, because in theory it might be used to cover a larger change in gate voltage providing the parameters of the model were obtained by an averaging process throughout the range. Thus in such a case, it would approach the requirements imposed on the charge control models developed here, but with somewhat poorer performance capabilities. It would still lack the generality and applicability of the charge control approach, however.

4.3 Early Switching Models and Computer Programs

In this section, the early models used in the low level switching study are presented, and their describing equations derived. The computer programs used in the solution of these models are also discussed. Calculated device transients from each of these models will be presented in Chapter 5, and compared with corresponding measured transients. The models appearing in this section have been chosen primarily in order to study the effectiveness of device switching representation with a relatively simple lumping configuration, and with different numbers of model lumps.

The models used in this section are similar to the one presented in Chapter 2, Fig. 2.6.5. For the purposes here, however, the effects of junction leakage currents will be neglected and thus do not appear in these models. Generally, leakage current can be expected to have little effect on the actual switching transients. Leakage currents are more important in the steady state, particularly in the "off" state as indicated in Section 4.2.1, where these effects can easily be solved for as indicated in the model of Fig. 2.6.5. If desired, leakage currents could also be incorporated into the computer programmed transient solution.

The equations for each of these models are presented in a form compatible with the Runge-Kutta [73] method of numerical solution of differential equations. This method requires that each highest-order derivative be expressed as a function of the variables and any lower-order derivatives. Details of this method are presented in the Appendix. This method was chosen because it is relatively simple to

use. It does not require special starting methods , its interval length can be changed at any time; furthermore, the procedure contains a relatively small number of formulas, which is particularly advantageous in the solutions of systems of differential equations as is the case here.

4.3.1 5-Lump L-Model

Fig.4.3.1 . . shows the 5-Lump "L"- model (model 5L) to be considered first. Model 5L was primarily intended to be used to investigate the effect of a different number of lumps on device representation. Consequently, stray gate to source and gate to drain capacitances have been neglected with the consequent saving of two "loops". These stray capacitances are included in the second generation models of Section 4.4, however. Gate contact and bulk resistance is neglected. Parasitic source and drain bulk resistances are included, though not particularly significant in these particular devices as indicated in Chapter 3.

Writing loop equations as indicated in Fig. 4.3.1 gives

$$E = I_1 (R_g + R_{ps}) + V_E - I_6 R_{ps} \qquad (4.3.1)$$

$$V_B = V_A + (I_2 - I_6) R_B \qquad (4.3.2)$$

$$V_C = V_B + (I_3 - I_6) R_C \qquad (4.3.3)$$

$$V_D = V_C + (I_4 - I_6) R_D \qquad (4.3.4)$$

$$V_E = V_D + (I_5 - I_6) R_E \qquad (4.3.5)$$

$$-V_L = I_6 (R_A + R_B + R_C + R_D + R_E + R_{ps} + R_{pd}) - I_1 R_{ps} - I_5 R_E - I_4 R_D - I_3 R_C - I_2 R_B \qquad (4.3.6)$$

and
$$V_{ds} + V_L = I_7 R_L \qquad (4.3.7)$$

It is convenient to work in terms of the charge (Q_1 to Q_7) delivered by each loop current (I_1 to I_7) and solve for the charge (Q_A to Q_E) in each gate capacitance lump. Thus, by rearranging and substituting from the above equations, the following are obtained:

$$I_2 \equiv \frac{dQ_A}{dt} = \frac{V_B - V_A}{R_B} + \frac{dQ_6}{dt} \qquad (4.3.8)$$

$$(I_3 - I_2) \equiv \frac{dQ_B}{dt} = \frac{V_C - V_B}{R_C} - \frac{V_B - V_A}{R_B} \qquad (4.3.9)$$

$$(I_4 - I_3) \equiv \frac{dQ_C}{dt} = \frac{V_D - V_C}{R_D} - \frac{V_C - V_B}{R_C} \qquad (4.3.10)$$

$$(I_5 - I_4) \equiv \frac{dQ_D}{dt} = \frac{V_E - V_D}{R_E} - \frac{V_D - V_C}{R_D} \qquad (4.3.11)$$

$$(I_1 - I_5) \equiv \frac{dQ_E}{dt} = \frac{E - V_E}{R_g + R_{ps}} + \left(\frac{R_{ps}}{R_g + R_{ps}} - 1\right)\frac{dQ_6}{dt} - \frac{V_E - V_D}{R_E} \qquad (4.3.12)$$

$$I_6 \equiv \frac{dQ_6}{dt} = \frac{1}{R_A + R_{AT}}\left[-V_L + \frac{R_{ps}E}{R_g + R_{ps}} - \left(\frac{R_{ps}}{R_g + R_{ps}} - 1\right)V_E - V_A\right] \qquad (4.3.13)$$

$$I_7 \equiv \frac{dQ_7}{dt} = \frac{V_{ds} + V_L}{R_L} \qquad (4.3.14)$$

where in equation 4.3.13

$$R_{AT} = R_{ps} + R_{pd} - \left(\frac{R_{ps}^2}{R_g + R_{ps}} \right) \qquad (4.3.15)$$

The junction charge-voltage relationship as measured for the whole device at zero drain voltage, is assumed to apply to each capacitance lump. This assumption is valid so long as there are sufficient lumps , so that the shape of the section of channel depletion layer represented by each lump is not severely distorted from the rectangular situation (zero drain voltage) which applied during the measurement. As discussed in Section 4.2.3.3, a plot of gate charge Q_{gg} versus gate voltage V_g on log-log graph in the general case, is adequately represented by one or more straight line sections. In a given straight line section, it is then valid to write

$$V_g = K_1 (Q_{gg})^B \qquad (4.3.16)$$

and also in the same section

$$V_o = K_1 (Q_{gq})^B \qquad (4.3.17)$$

where B = slope of straight line section on log-log graph

K_1 = constant of proportionality

V_g, Q_{gg} = any set of corresponding gate voltage and gate charge values on the straight line

V_o, Q_{gq} = particular corresponding values on the straight line section to be used for normal-iation.

Note that V_o could be chosen equal to V_{po} , the pinch-off voltage, but is not necessarily the case as explained below. By division from equations 4.3.16 and 4.3.17, the normalized form is obtained. Thus

$$\frac{V_g}{V_o} = \left(\frac{Q_{gg}}{Q_{gq}} \right)^B \qquad (4.3.18)$$

Equation 4.3.18 is strictly valid for given values of V_o , Q_{gq} , and B only over a range of V_g and Q_{gq} such that when plotted on a log-log graph they are related by a straight line.

As indicated in Section 4.2.3.3, it will be shown in Chapter 5, Section 5.3, that the range of gate voltage up to pinch-off can be approximated by two or three straight line sections on the log-log plot. Equation 4.3.18 can thus be used in each of these sections, but with different values of V_o , Q_{gq}, and B. In this and other early models, this "re-normalization" is effected by the computer program, with the values obtained as illustrated in Figures 4.3.2 and 4.3.3. In the later models, this situation is better accommodated by a multipying factor in the equation itself, and will be discussed in connection with the appropriate models.

Two possible straight line sections are assumed for both the $Q_{gg} - G_{ch}$ relationship and the $Q_{gg} - V_g$ log-log relationship (Figures 4.3.2 and 4.3.3) for the present model. The Q_{gq} values are obtained (Fig. 4.3.2) by extrapolating to the Q_{gg} axis, the constant slopes in sections 1 and 2 of the $Q_{gg} - G_{ch}$ relationship. Thus for values of gate charge in section 1 , $Q_{gq} = Q_{gq_1}$, and the corresponding V_o (i.e. V_{o_1}) is obtained by extrapolating on the log-log $Q_{gg} - V_g$ relation-

ship as shown in Fig. 4.3.3. The case is similar for gate charge values in section 2 of the $Q_{gg} - G_{ch}$ relationship, but here $Q_{gg} \equiv Q_{gq_2}$ and $V_o \equiv V_{o_2}$

The charge components Q_A to Q_E and Q_6 and Q_7 will be normaliaed to Q_{ou} where

$$Q_{ou} \equiv \frac{Q_{gq}}{n} \qquad (4.3.19)$$

and where Q_{gq} = extrapolated pinch-off charge corresponding to V_o (see Fig. 4.3.2 and Fig. 4.3.3)

n = number of model lumps

Thus

$$X = \frac{Q_B}{Q_{ou}} \text{ ; for lump B} \qquad (4.3.20a)$$

$$Y = \frac{Q_A}{Q_{ou}} \text{ ; for lump A} \qquad (4.3.20b)$$

$$Z = \frac{Q_E}{Q_{ou}} \text{ ; for lump E} \qquad (4.3.20c)$$

$$P = \frac{Q_C}{Q_{ou}} \text{ ; for lump C} \qquad (4.3.20d)$$

$$U = \frac{Q_D}{Q_{ou}} \text{ ; for lump D} \qquad (4.3.20e)$$

$$V = \frac{Q_7}{Q_{ou}} \text{ ; from } I_7 \qquad (4.3.20f)$$

$$W = \frac{Q_s}{Q_{ou}} \quad ; \text{ from } I_s \qquad (4.3.20g)$$

The resistance of each channel lump is then obtained as discussed in Chapter 2, Section 2.6. Thus for lump A, for example,

$$R_A = \frac{R_{ou}}{1 - Y} \qquad (4.3.21)$$

where R_A = resistance of channel lump A

$R_{ou} = \frac{R_{cho}}{n}$ = zero bias resistance of each of n sections of the channel (see discussion below).

The resistance of lumps B to E is similarly calculated with the corresponding normalized charge from equations 4.3.20. Equation 4.3.21 is strictly valid only over a region of constant L^2/μ slope. As discussed in Section 4.2.3.2, however, the complete $Q_{gg} - G_{ch}$ range can be composed of more than one region with different L^2/μ slopes. In each region, R_{cho} is obtained by extrapolation as illustrated in Fig. 4.3.2. Thus in region 1 of operation, $R_{cho} \equiv R_{ch_1}$ and in region 2, $R_{cho} \equiv R_{ch_2}$. This situation is also accommodated by a "re-normalization" which in these earlier models is accomplished in the computer program with data obtained, as described, from Fig. 4.3.2. In the later models, just as for the charge-voltage relationship, this is accomplished by a multiplying factor and will be discussed in connection with the appropriate models.

The charge-voltage relationship for each lump is obtained from equation 4.3.18. Thus, for lump A, for example,

$$V_A = V_o \; Y^B \qquad (4.3.22)$$

where V_o is obtained as indicated in Fig. 4.3.3 corresponding to a gate charge of Q_{gq}, or Q_{ou} for each lump. The charge-voltage relationship for each other lump is similarly obtained with the corresponding normalized charge from equations 4.3.20.

Substituting equations 4.3.21 and 4.3.22 for each lump into equations 4.3.8 through 4.3.14, and using the normalized charge components from equations 4.3.20, gives in alphabetical sequence,

$$\frac{dP}{dt} = \frac{d\,(Q_C / Q_{ou})}{dt} = \frac{V_o}{R_{ou}\,Q_{ou}} \left[(1-U)\,U^B - (2-U-P)\,P^B + (1-P)\,X^B \right] \qquad (4.3.23)$$

$$\frac{dU}{dt} = \frac{d(Q_D / Q_{ou})}{dt} = \frac{V_o}{R_{ou}Q_{ou}} \left[(1-Z)\,Z^B - (2-U-Z)\,U^B + (1-U)\,P^B \right] \qquad (4.3.24)$$

$$\frac{dV}{dt} = \frac{d(Q_7 / Q_{ou})}{dt} = \frac{1}{Q_{ou}\,R_L} \left[V_{ds} + \frac{Q_{ou}\,(W-V)}{C_L} \right] \qquad (4.3.25)$$

$$\frac{dW}{dt} = \frac{d(Q_8 / Q_{ou})}{dt} = \frac{1}{Q_{ou}\left[\dfrac{R_{ou}}{(1-Y)} + R_{AT}\right]} \left[-\frac{Q_{ou}(W-V)}{C_L} + \frac{R_{ps}E}{R_g + R_{ps}} - V_o Y^B - V_o \left(\frac{R_{ps}}{R_g + R_{ps}} - 1 \right) Z^B \right] \qquad (4.3.26)$$

$$\frac{dX}{dt} = \frac{d\,Q_B / Q_{ou}}{dt} = \frac{V_c}{Q_{ou}R_{ou}} \left[(1-P)\,P^B - (2-X-P)\,X^B + (1-X)\,Y^B \right] \qquad (4.3.27)$$

$$\frac{dX}{dt} = \frac{d(Q_A / Q_{ou})}{dt} = \frac{V_o}{Q_{ou}\ R_{ou}} (1-X)\ (X^B - Y^B) + \frac{dW}{dt} \qquad (4.3.28)$$

$$\frac{dZ}{dt} = \frac{d(Q_E / Q_{ou})}{dt} = \frac{E - V_o Z^B}{Q_{ou}\ (R_g + R_{ps})} + \left(\frac{R_{ps}}{(R_g + R_{ps})} - 1\right)\frac{dW}{dt} - \frac{V_o}{Q_{ou} R_{ou}} (1-Z)\ (Z^B - W^B)$$

(4.3.29)

where

$$V_L = \frac{Q_{ou}(W-V)}{C_L} \qquad (4.3.30)$$

corresponding to the amount of normalized charge in C_L.

Finally, equations 4.3.23 through 4.3.29 are normalized with respect to time such that

$$T \equiv \frac{t\ V_o}{Q_{ou}\ RF} \qquad (4.3.31)$$

where

T = normalized time (dimensionless)

t = real time

V_o = normalizing voltage

Q_{ou} = zero bias majority carrier charge assumed to exist in each section of the channel

F = dimensionless scaling factor which is found convenient in connection with controlling the computer output

R = normalizing resistance which can be specified as desired. In this work, normalization is mainly for computing convenience. Since so many factors affect the transient, a given choice of R may not be the most

convenient for all situations. The factor F helps in this regard. In these earlier models, R was chosen to be equal to $(R_g + R_{ps})$.

Equations 4.3.23 through 4.3.29 therefore become

$$\frac{dP}{dT} = \frac{RF}{R_{ou}} \left[(1-U)\, U^B - (2-U-P)\, P^B + (1-P)\, X^B \right] \qquad (4.3.32)$$

$$\frac{dU}{dT} = \frac{RF}{R_{ou}} \left[(1-Z)\, Z^B - (2-U-Z)\, U^B + (1-U)\, P^B \right] \qquad (4.3.33)$$

$$\frac{dV}{dT} = \frac{RF}{V_o\, R_L} \left[V_{ds} + \frac{Q_{ou}}{C_L} (W-V) \right] \qquad (4.3.34)$$

$$\frac{dW}{dT} = \frac{RF}{V_o \left[\frac{R_{ou}}{(1-Y)} + R_{AT} \right]} \left[\frac{-Q_{ou}(W-V)}{C_L} + \frac{R_{ps} E}{R_g + R_{ps}} - V_o Y^B - V_o \left(\frac{R_{ps}}{R_g + R_{ps}} - 1 \right) Z^B \right] \qquad (4.3.35)$$

R_{AT} is defined in equation 4.3.15.

$$\frac{dX}{dT} = \frac{RF}{R_{ou}} \left[(1-P)\, P^B - (2-X-P)\, X^B + (1-X)\, Y^B \right] \qquad (4.3.36)$$

$$\frac{dY}{dT} = \frac{RF}{R_{ou}} (1-X)\, (X^B - Y^B) + \frac{dW}{dT} \qquad (4.3.37)$$

$$\frac{dZ}{dT} = \frac{RFE}{V_o\, (R_g + R_{ps})} + \left(\frac{R_{ps}}{R_g + R_{ps}} - 1 \right) \frac{dW}{dT} - \frac{RF}{(R_g + R_{ps})} Z^B - \frac{RF}{R_{ou}} (1-Z)\, (Z^B - U^B)$$

(4.3.38)

Two other equations for the model are useful. The total channel resistance R_{ch} is given by

$$R_{ch} = R_{cu}\left(\frac{1}{1-X} + \frac{1}{1-Y} + \frac{1}{1-Z} + \frac{1}{1-P} + \frac{1}{1-U}\right) \quad (4.3.39)$$

The output drain source voltage is given from equation 4.3.14. Thus

$$V_L = I_7 R_L - V_{ds}$$

$$= \frac{R_L V_o}{RF} \frac{dV}{dT} - V_{ds} \quad (4.3.40)$$

4.3.2 3-Lump L-Model

The 3-lump L-model (model 3L) is shown in Fig. 4.3.4. Model 3L is identical with model 5L except for the number of L-section lumps representing the device.

The equations for this model are derived in identically the same way as those for model 5L in Section 4.3.1 Hence they will only be briefly summarized here. The loop equations indicated in Fig. 4.3.4 are as follows:

$$E = I_1 (R_g + R_{ps}) + V_C - I_4 R_{ps} \quad (4.3.41)$$

$$V_B - V_A = (I_2 - I_4) R_B \quad (4.3.42)$$

$$V_C - V_B = (I_3 - I_4) R_C \quad (4.3.43)$$

$$-V_L = I_4 (R_A + R_B + R_C + R_{ps} + R_{pd}) - I_1 R_{ps} - I_3 R_C - I_2 R_B \quad (4.3.44)$$

$$V_L + V_{ds} = I_5 R_L \qquad (4.3.45)$$

The defined normalized charges for this model are

$$Y = \frac{Q_A}{Q_{ou}} \quad ; \text{ for lump A} \qquad (4.3.46a)$$

$$X = \frac{Q_B}{Q_{ou}} \quad ; \text{ for lump B} \qquad (4.3.46b)$$

$$Z = \frac{Q_C}{Q_{ou}} \quad ; \text{ for lump C} \qquad (4.3.46c)$$

$$W = \frac{Q_4}{Q_{ou}} \quad ; \text{ from } I_4 \qquad (4.3.46d)$$

$$V = \frac{Q_5}{Q_{ou}} \quad ; \text{ from } I_5 \qquad (4.3.46e)$$

Note that the effects of both gate and drain voltages are included in Q_A, Q_B, etc. for each lump. The resistance of each lump is calculated in the same manner as indicated by equation 4.3.21, and the voltage-charge relationship for each lump is calculated in the same manner as indicated by equation 4.3.22. Thus after substitution and normalization just as in Section 4.3.1, equations 4.3.41 through 4.3.45 become

$$\frac{dV}{dT} = \frac{RF}{R_L V_o} \left[\frac{Q_{ou}\,(W-V)}{C_L} + V_{ds} \right] \qquad (4.3.47)$$

$$\frac{dW}{dT} = \left[\frac{RF}{\frac{R_{ou}}{(1-Y)} + R_{AT}}\right] \left[\frac{R_{ps}E}{V_o\,(R_g + R_{ps})} - \frac{Q_{ou}(W-V)}{V_o\,C_L} - Y^B + 1 - \frac{R_{ps}}{R_g + R_{ps}}\,Z^B\right] \quad (4.3.48)$$

$$\frac{dX}{dT} = \frac{RF}{R_{ou}}\left[(1-Z)(Z^B - X^B) - (1-X)(X^B - Y^B)\right] \quad (4.3.49)$$

$$\frac{dY}{dT} = \frac{RF}{R_{ou}}\,(1-X)\,(X^B - Y^B) + \frac{dW}{dT} \quad (4.3.50)$$

$$\frac{dZ}{dT} = \frac{RFE}{V_o\,(R_g + R_{ps})} - \frac{RF}{(R_g + R_{ps})}\,Z^B - \left(1 - \frac{R_{ps}}{R_g + R_{ps}}\right)\frac{dW}{dT} - \frac{RF}{R_{ou}}\,(Z^B - X^B) \quad (4.3.51)$$

where $R_{At} \equiv R_{ps} + R_{pd} - \dfrac{R_{ps}^2}{R_g + R_{ps}}$ as for equation 4.3.15.

The channel resistance is given by

$$R_{ch} = R_{ou}\left[\frac{1}{1-X} + \frac{1}{1-Y} + \frac{1}{1-Z}\right] \quad (4.3.52)$$

and the output voltage is given from equation 4.3.45, i.e.,

$$V_L = I_s\,R_L - V_{ds}$$

Therefore

$$V_L = \left(\frac{R_L\,V_o}{RF}\right)\frac{dV}{dT} - V_{ds} \quad (4.3.53)$$

4.3.3 Computer Programs

In this section, a brief description of the purpose and operation of the computer programs used in the solution of models 5L and 3L will be given. The data required for operating the program will also be discussed. The programs used for model 5L and 3L are identical in all respects except in the number of equations solved. The program for model 3L will therefore not be presented. A complete print-out of the statements of the program for model 5L appears in the Appendix. The block diagram (Fig4.3.5) and the subsequent discussion, however, apply equally to both programs.

4.3.3.1 Discussion of Operation

The purpose of the computer program represented by the block diagram in Fig. 4.3.5, is to solve the appropriate model equations numerically at various discrete times throughout the switching transient, and to provide a print-out of the total device channel resistance and output voltage appearing across the load resistance as a function of time. As previously mentioned, this is accomplished here by the Runge-Kutta (73) method for solving differential equations, which is described in the Appendix. For details regarding the computer language (Fortran IV) used for this program , IBM publication C28-6390-1 (74) should be consulted.

The block diagram in Fig. 4.3.5 illustrates the overall composition and flow of the program. Block 1 consists essentially of statements called function statements which are general forms of the equations derived previously in connection with the models. These function statements are then later "called" in Block 4 and solved with particular

values in place of their "dummy" arguments (i.e., U, P, X, etc.). Two locations are also reserved in Block 1 for the variable FET holding the device name.

In Block 2 the program data is read in according to the specified format. Each component of data will be discussed in Section 4.3.3.2 and related to the device and/or its purpose in the program. a test is made after reading the first of each group of data cards. If an "I" appears in column 72 of this card, program operation is stopped. The various constants used in the program, and in particular, those used in the function statements of Block 1, are then calculated. The program then calculates by means of an iterative process, the initial voltages and charges (PI, UI, etc.) appearing in the various parts of the model as a result of the presence of an applied drain voltage, or an applied gate voltage in the case of a discharge transient.

On the basis of the initial charge values calculated in Block 2, the function statements of Block 1 are called to calculate the initial charge derivatives in Block 3. The remainder of Block 3 is miinly concerned with producing a print-out, for checking purposes and for operator information, of many of the device parameters and calculated constants.

Block 4 contains the heart of the numerical solution process where on the basis of the known (old) values of P, U, V, etc., and their derivatives, new values of P, U, V, etc., and their derivatives are obtained at a later increment in time. From these new values, the channel resistance and the output voltage , and the time from the begin-

ning of the transient are calculated and printed out. Output is controlled by statements in Block 4. In the program, time is controlled and incremented as an integer variable to avoid summation errors.

At the end of Block 4 is a test to determine whether the maximum specified time has been reached. If not, control is transferred to Block 5. If it has, a test is made to determine if a discharge transient is also desired. If it is not, control is transferred back to Block 2 where the next card is read and the program is stopped, or calculation of the next transient is started as desired. If a discharge transient is specified, control is transferred to Block 6.

In Block 5, tests are made to determine if a "break point" has been encountered. A "break point" indicates a change in slope on the $Q_{gg} - G_{ch}$ plot, or on the log-log plot of Q_{gg} vs V_g as indicated in Figures 4.3.2 and 4.3.3. If a "break point" is encountered, appropriate re-normalization is carried out with respect to new values of V_o ,Q_{gg} , G_{cho} and B as indicated in Fig. 4.3.2. Substitutions are then carried out in which the newly calculated values of P, U, V, etc., and their derivatives are put in place of the corresponding old values. Control is then transferred to Block 4 where the previously described Block 4 processes are repeated at a new value of time.

When Block 6 is entered from the previously referred to test, it indicates that the gate charging transient is complete, and that a gate discharging transient is desired. Block 6 resets program time to zero, prepares the initial charge values, and sets the applied gate voltage E to zero. A statement is printed out indicating the discharging calculation, and control is transferred to Block 3. The normal processes are then

followed except that the amount of gate charge is decreased and the channel resistance is decreased as the transient progresses. Block 6 also increments a tested variable to ensure that the discharge transient cannot be repeated for this same set of data.

4.3. .2 Data Required

The various components of data required by the program will now be discussed. Each component of data, its location on the data card, and its description is shown in Table 4.3.1. Data which starts with "I-M", is an "integer" variable, and is written in the indicated card columns without a decimal point (eg. 300). All remaining items are "real" variables, and are specified with an "E" format. Thus the number 10.05, for example, is written as 1.005E +01, and must be right justified in the allocated columns.

Program time referred to here is defined as

$$NT = 1000 \times T$$

where NT = program time

T = normalized time defined in equation 4.3.31

The reason for this is that it is desirable to make program time an integer variable , thus avoiding summation errors due to rounding in the computer.

The dimensionless normalizing factor F is normally set to 1. It can however, be made larger or smaller, in which case it has the effects of "shifting" normalized or program time with respect to real time. In some cases, this can be used to obtain a slightly more convenient format of print-out results.

TABLE 4.3.1

DATA FOR COMPUTER PROGRAMS FOR MODELS 5L and 3L

Data Card 1

Item	Location on Card	Description
FET	cc 1-10	Device code name (eg. TIX881-2)
QO	cc11-20	Q_{gq_1} - see Fig. 4.3.2
QOFIN	cc21-30	Q_{gq_2} - see Fig. 4.3.2
DK	cc31-40	V_{O_1} - see Fig. 4.3.3
DKFIN	cc41-50	V_{O_2} - see Fig. 4.3.3
RO	cc51-60	$1 / G_{cho_1}$ - see Fig. 4.3.2
ROFIN	cc61-70	$1 / G_{cho_2}$ - see Fig. 4.3.2
I	cc72	I = 1 indicates program stop
J	cc73	J = 1 indicates discharge transient desired. $J \geq 1$ also sets NTNCH 2(see NMULT 2; second card)

TABLE 4.3.1 Continued

Data Card 2

Item	Location on Card	Description
B	cc1-10	section 1 "slope" on log-log Q_{gg}-V_g plot (see Fig. 4.3.3)
BFIN	cc11-20	section 2 "slope" on log-log Q_{gg}-V_g plot (see Fig. 4.3.3)
RPS	cc21-30	bulk parasitic source resistance
RPD	cc31-40	bulk parasitic drain resistance
E	cc41-50	applied gate driving voltage -see model
VD	cc51-60	applied drain voltage - see model
RG	cc61-70	external series gate resistance
NMULT2	cc71-80	multipying factor for second change in program time increment at NTNCH2 = NTNCH (1 + J/5)

Data Card 3

Item	Location on Card	Description
RL	cc1-10	load resistance
CL	cc11-20	load and stray drain source capacitance
F	cc21-30	dimensionless normalizing factor -see text
TF	cc31-40	specified final normalized transient time
NTNCH	cc41-50	program time at which first time increment change occurs
NMULT	cc51-60	Multipying factor for first change in program time increment
NDT	cc61-70	initial program time increment
GSDBK	cc71-80	break point - see Fig. 4.3.2

Values for each of these items of data will be given for several practical devices in Chapter 5, Section 5.3.

4.4 Second Generation Models and Computer Programs

4.4.1 3-Lump T-Model

Figure 4.4.1 shows a 3-lump model (model 3T) in which each lump is arranged in the form of a "T". Stray gate-drain and gate-source capacitances are included in this model. Model 3T is a "second generation" model and is based partly on experience gained with the simpler L-models.

The purpose of this model is to account for the effects of stray capacitances, and to investigate the effectiveness of a more sophisticated lumping configuration. The main characteristics of this T lumping configuration is that for a given number of lumps compared with the L configuration, the T model provides a better distribution of the charging (or discharging) currents along the channel from each capacitive element. It is therefore expected to provide a better representation of the switching process under a given set of conditions than the equivalent L-model.

Writing loop equations for model 3T as indicated in Fig. 4.4.1 gives

$$E = I_1 R_g + V_E \qquad (4.4.1)$$

$$V_A - V_F = (I_2 - I_6) R_1 \qquad (4.4.2)$$

$$V_B - V_A = (I_3 - I_6)\, R_2 \qquad (4.4.3)$$

$$V_C - V_B = (I_4 - I_6)\, R_3 \qquad (4.4.4)$$

$$V_E - V_C = (I_5 - I_6)\, R_4 \qquad (4.4.5)$$

$$V_L = V_E - V_F \qquad (4.4.6)$$

$$V_L + V_D = I_7\, R_L \qquad (4.4.7)$$

where

$$R_1 = R_A + R_{pd} \qquad (4.4.8a)$$

$$R_2 = R_A + R_B \qquad (4.4.8b)$$

$$R_3 = R_B + R_C \qquad (4.4.8c)$$

$$R_4 = R_C + R_{ps} \qquad (4.4.8d)$$

From equation 4.4.6, one gets

$$\frac{1}{C_L}\int (I_6 - I_7)\, dt = \frac{1}{C_{gs}}\int (I_1 - I_5)\, dt - \frac{1}{C_{gd}}\int I_2\, dt \qquad (4.4.9)$$

Differentiating equation 4.4.9 gives

$$\frac{I_6 - I_7}{C_L} = \frac{I_1 - I_5}{C_{gs}} = \frac{I_2}{C_{gd}} \qquad (4.4.10)$$

The defined normalized charges for model 3T are

$$X \equiv Q_A / Q_{ou} \text{ ; for lump A from } (I_3 - I_2) \qquad (4.4.11a)$$

$Y \equiv Q_B / Q_{ou}$; for lump B from $(I_4 - I_3)$ (4.4.11b)

$Z \equiv Q_C / Q_{ou}$; for lump C from $(I_5 - I_4)$ (4.4.11c)

$P \equiv (Q_1 - Q_5) / Q_{ou}$; for Cgs from $(I_1 - I_5)$ (4.4.11d)

$U \equiv Q_2 / Q_{ou}$; for C_{gd} from (I_2) (4.4.11e)

Time normalization for this model is given by

$$T = \frac{t V_o}{Q_o RF} \qquad (4.4.12)$$

where T = normalized time

t = real time

V_o = normalizing voltage (see also Section 5.3)

Q_o = zero bias majority carrier charge in the channel. Q_o is used here to provide a result independent of the number of program lumps

F = dimensionless scaling factor

R = normalizing resistance;

Rearranging and combining equations 4.4.1 through 4.4.10, and normalizing as indicated by equations 4.4.11 and 4.4.12 produces the following:

$$\frac{dX}{dT} = \frac{FRn}{V_o}\left[\frac{V_B - V_A}{R_2} - \frac{V_A - V_F}{R_1}\right] \qquad (4.4.13)$$

$$\frac{dY}{dT} = \frac{FRn}{V_o}\left[\frac{V_C - V_B}{R_3} - \frac{V_B - V_A}{R_2}\right] \tag{4.4.14}$$

$$\frac{dZ}{dT} = \frac{FRn}{V_o}\left[\frac{V_E - V_C}{R_4} - \frac{V_C - V_B}{R_3}\right] \tag{4.4.15}$$

$$\frac{dP}{dT} = \frac{FRn}{V_o}\left[\frac{\frac{C_{gd}}{C_{gs}}\left(\frac{C_{gs}}{C_{gd}} + \frac{C_{gs}}{C_L}\right)}{1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}}\right]\left[\frac{E - V_E}{R_g} - \frac{V_E - V_C}{R_4}\right]$$

$$+ \frac{FRn}{V_o}\left(\frac{V_L + V_D}{R_L}\right)\left[\frac{\frac{C_{gd}}{C_L}\left(\frac{C_{gs}}{C_{gd}} + \frac{C_{gs}}{C_L}\right)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)} - \frac{C_{gs}}{C_L}\right]$$

$$+ \frac{FRn}{V_o}\left(\frac{V_A - V_F}{R_1}\right)\left[\frac{\left(\frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)\left(\frac{C_{gs}}{C_{gd}} + \frac{C_{gs}}{C_L}\right)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)} - \frac{C_{gs}}{C_L}\right] \tag{4.4.16}$$

$$\frac{dU}{dT} = \frac{(FRn / V_o)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)}\left[\frac{C_{gd}}{C_{gs}}\left(\frac{E - V_E}{R_g}\right) - \frac{C_{gd}}{C_{gs}}\left(\frac{V_E - V_C}{R_4}\right) + \frac{C_{gd}}{C_L}\left(\frac{V_L + V_D}{R_L}\right) + \left(\frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)\left(\frac{V_A - V_F}{R_1}\right. \tag{4.4.17}$$

where n= number of model lumps; in this case, 3.

Equations 4.4.13 through 4.4.17 are in a form suitable for computation, where V_A, V_B, V_C, V_E, V_F, R_1, R_2, R_3, and R_4 are obtained as indicated in the following discussion, and substituted in the above equations to obtain the desired solutions.

The methods used in this model to accommodate changes in slope on the $Q_{gg} - G_{ch}$ plot, and on the log-log plot of Q_{gg} versus V_g, will now be described. As indicated previously, this will be accomplished by means of multipying factors in the equations concerned. The methods described here allow the corresponding multipying factors to be independently set for each model lump depending on its region of operation, i.e., the amount of charge in the capacitive element of each lump. This system is thus flexible, and it should be more accurate than the methods used for the earlier models in Section 4.3. The gate charge versus channel conductance relationship will be discussed first.

Experience has shown that the gate charge versus channel conductance plots for these FET's can generally be well represented with one to four straight line sections. Thus the general $Q_{gg} - G_{ch}$ plot might appear as shown in Fig. 4.4.2, where all four regions need not appear for any given device. The entire charge-conductance range for the whole channel is covered with an equation of the form

$$R_{ch} = \frac{D}{\left[S - \left(\frac{Q_{gg}}{Q_o} \right) \right]} \qquad (4.4.18)$$

where R_{ch} = device channel resistance

Q_{gg} = gate charge

Q_o = zero bias majority carrier charge and is equal to the amount of gate charge to produce pinch-off ($V_D = 0$) (see Fig. 4.4.2)

S,D = factors which are set depending on whether operation is in region 1, 2, 3, or 4 (see Fig. 4.4.2)

The values which S and D may assume are derived with reference to Fig. 4.4.2. In region 1, the total channel resistance is given by

$$R_{ch} = \frac{1}{G_o\left(1 - \frac{Q_{gg}}{Q_{e1}}\right)} = \frac{1}{\frac{G_oQ_o}{Q_{e1}}\left(\frac{Q_{e1}}{Q_o} - \frac{Q_{gg}}{Q_o}\right)} \qquad (4.4.19)$$

Therefore,

$$R_{ch} = \frac{\frac{Q_{e1}}{G_oQ_o}}{\left(\frac{Q_{e1}}{Q_o} - \frac{Q_{gg}}{Q_o}\right)} = \frac{D_1}{\left(S_1 - \frac{Q_{gg}}{Q_o}\right)} \qquad (4.4.20)$$

where

$$D_1 = \frac{Q_{e1}}{Q_oG_o} \quad \text{and} \quad S_1 = \frac{Q_{e1}}{Q_o} \qquad (4.4.21)$$

It is convenient to work in terms of the "break point" values of the curve which will be used by the computer program. Therefore from Fig. 4.4.2:

$$\frac{G_o - G_1}{Q_1} = \frac{G_o}{Q_{e1}} \qquad (4.4.22)$$

giving

$$Q_{e_1} = \frac{G_o Q_1}{(G_o - G_1)} \tag{4.4.23}$$

Thus

$$D_1 = \frac{Q_1}{Q_o\,(G_o - G_1)}$$

and

$$S_1 = \frac{G_o Q_1}{(G_o - G_1)\, Q_o} \tag{4.4.24}$$

Similarly in region 2,

$$R_{ch} = \frac{\dfrac{Q_{e_2}}{G_{e_2} Q_o}}{\left(\dfrac{Q_{e_2}}{Q_o} - \dfrac{Q_{gg}}{Q_o}\right)} = \frac{D_2}{\left(S_2 - \dfrac{Q_{gg}}{Q_o}\right)} \tag{4.4.25}$$

and from Fig. 4.4.2

$$\frac{Q_{e_2}}{G_{e_2}} = \frac{Q_2 - Q_1}{G_1\ G_2} \tag{4.4.26}$$

Also,

$$\frac{Q_{e_2} - Q_1}{G_1} = \frac{Q_2 - Q_1}{G_1 - G_2} \tag{4.4.27}$$

giving

$$Q_{e_2} = \left(\frac{Q_2 - Q_1}{G_1 - G_2}\right) G_1 + Q_1 \tag{4.4.28}$$

Thus,

$$D_2 = \frac{Q_2 - Q_1}{Q_0 (G_1 - G_2)}$$

and
$$S_2 = \frac{1}{Q_0} \left[G_1 \frac{Q_2 - Q_1}{G_1 - G_2} + Q_1 \right] \qquad (4.4.29)$$

In the same way for regions 3 and 4, the values for S and D are found to be

$$D_3 = \frac{(Q_3 - Q_2)}{Q_0 (G_2 - G_3)} \quad \text{and} \quad S_3 = \frac{1}{Q_0} \left[G_2 \frac{(Q_3 - Q_2)}{(G_2 - G_3)} + Q_2 \right] \qquad (4.4.30)$$

and

$$D_4 = \frac{Q_0 - Q_3}{Q_0 G_3} \quad \text{and} \quad S_4 = 1.0 \qquad (4.4.31)$$

Further, it can readily be seen that for a channel represented as shown in Fig. 4.4.1, the values of D and S for each half-lump resistance, for lump A for example, are given by

$$R_A = \frac{D_A}{S_A - X} \qquad (4.4.32)$$

where $D_A = \dfrac{D}{2n}$, $S_A = S$ — where $D = D_1$ --- D_4 and $S = S_1$ --- S_4 depending on range of operation

$X = \dfrac{Q_A}{Q_0 / n}$ = normalized charge in capacitance element A (including reverse bias effect at lump A due to V_{ds} if present)

n = number of identical channel lumps (=3 in Model 3T)

The situation is identical for lumps B and C, but D_B and S_B , and D_C and S_C are set independently as required. Thus in accordance with equations 4.4.8, it can be seen that

$$R_1 \equiv \frac{D_A}{S_A - X} + R_{pd} \tag{4.4.33a}$$

$$R_2 \equiv \frac{D_A}{S_A - X} + \frac{D_B}{S_B - Y} \tag{4.4.33b}$$

$$R_3 \equiv \frac{D_B}{S_B - Y} + \frac{D_C}{S_C - Z} \tag{4.4.33c}$$

$$R_4 \equiv \frac{D_C}{S_C - Z} + R_{ps} \tag{4.4.33d}$$

Attention is now given to the gate charge - gate voltage relationship. It is found that in general, good representation of this relationship can be obtained with three or fewer straight line regions on a log-log graph as illustrated for the general case in Fig. 4.4.3. The general form used for this relationship is

$$\frac{V_g}{V_o} = F\left(\frac{Q_g}{Q_o}\right)^B \tag{4.4.34}$$

where

V_g = gate voltage

Q_g = gate charge

Q_o = amount of gate charge to produce pinch-off

V_o = pinch-off voltage corresponding to Q_o

F,B = values depend on region of operation

The values of F and B for each of the three regions for the total device are derived with reference to Fig. 4.4.3. Firstly, for region 3,

$$\frac{V_g}{V_o} = F_3 \left(\frac{Q_{gg}}{Q_o}\right)^{B_3} \tag{4.4.35}$$

Since equation 4.4.35 is already in the correct form with respect to (Q_{gg} / Q_o), then $F_3 = 1.0$.

It can also be seen from Fig. 4.4.3 that B_3 is given by

$$B_3 = \frac{\log_e\left(\frac{V_o}{V_2}\right)}{\log_e\left(\frac{Q_o}{Q_5}\right)} \tag{4.4.36}$$

Now, in region 2,

$$\frac{V_g}{V_2} = \left(\frac{Q_{gg}}{Q_5}\right)^{B_2} \tag{4.4.37}$$

and also at the junction of regions 2 and 3 , one can write

$$\frac{V_2}{V_o} = \left(\frac{Q_5}{Q_o}\right)^{B_3} \tag{4.4.38}$$

Combining equations 4.4.37 and 4.4.38 gives

$$\frac{V_g}{V_o} = \left(\frac{Q_5}{Q_o}\right)^{B_3} \left(\frac{Q_{gg}}{Q_5}\right)^{B_2} \tag{4.4.39}$$

$$\frac{V_g}{V_o} = \left(\frac{Q_5}{Q_o}\right)^{B_3} \left(\frac{Q_o}{Q_5}\right)^{B_2} \left(\frac{Q_{gg}}{Q_o}\right)^{B_2} \qquad (4.4.40)$$

$$= F_2 \left(\frac{Q_{gg}}{Q_o}\right)^{B_2} \qquad (4.4.41)$$

where

$$F_2 = \left(\frac{Q_5}{Q_o}\right)^{B_3} \left(\frac{Q_o}{Q_5}\right)^{B_2} \qquad (4.4.42)$$

As before, it can be seen that

$$B_2 = \frac{\log_e\left(\frac{V_2}{V_1}\right)}{\log_e\left(\frac{Q_5}{Q_4}\right)} \qquad (4.4.43$$

Similarly, for region 1, it is found that

$$F_1 = \left(\frac{Q_5}{Q_o}\right)^{B_3} \left(\frac{Q_4}{Q_5}\right)^{B_2} \left(\frac{Q_o}{Q_4}\right)^{B_1} \qquad (4.4.44)$$

and

$$B_1 = \frac{\log_e\left(\frac{V_1}{V_{34}}\right)}{\log_e\left(\frac{Q_4}{Q_{34}}\right)} \qquad (4.4.45)$$

where the point V_{34} , Q_{34} is any convenient point on the straight line part of region 1.

For a given lump, such as lump A, equation 4.4.34 takes the form

$$\frac{V_A}{V_o} = F_A (X)^{B_{A1}} \qquad (4.4.46)$$

where X= normalized charge in lump A and V_A is the total reverse bias across capacitive element A due to V_g and to V_{ds} if present.

F_A, $B_A = F_1 \longrightarrow F_3$, $B_1 \longrightarrow B_3$ as derived above. For lumps B and C, F_B, B_B and F_C, B_C are all set independently as required. Thus also

$$\frac{V_B}{V_o} = F_B\ (Y)^{B_B} \qquad (4.4.47)$$

$$\frac{V_C}{V_o} = F_C\ (Z)^{B_C} \qquad (4.4.48)$$

Also it can be seen that

$$V_E = \frac{Q_{ou}\ P}{C_{gs}} \qquad (4.4.49)$$

$$V_F = \frac{Q_{ou}\ U}{C_{gd}} \qquad (4.4.50)$$

and from equation 4.4.6

$$V_L = V_E - V_F \qquad (4.4.51)$$

and from equations 4.4.33

$$R_{ch} = R_1 + R_2 + R_3 + R_4 - R_{ps} - R_{pd} \qquad (4.4.52)$$

Thus all the information required for the solution of equations 4.4.13 through 4.4.17 is now available.

4.4.2 1-Lump T-Model

In order that the effects of lumping may be further illustrated, it is interesting to investigate how well or how poorly the switching process is represented by a model with only one lump. Two very simple possible 1-lump configurations are shown in Fig. 4.4.4. The model in Fig. 4.4.4a can be seen to be degenerate, however, in that the rate of charging of the capacitive element is essentially unaffected by either the channel resistance (R_A) or by the load resistance (R_L). It can therefore be expected that the speed of response of drain voltage predicted by this model will be too rapid.

The results predicted by the model of Fig. 4.4.4b, on the other hand, depend very drastically on the size of R_L. If R_L is small with respect to R_A, the rate of charging will be too rapid; if R_L is large, the rate of charging will depend on the total channel resistance (R_A) and will therefore be too slow. Note also that if the applied drain voltage V_{ds} is large, neither model will correctly account for the fact that V_{ds} causes a voltage drop along the channel, and thus a progressively increasing amount of reverse bias on the gate-channel junction from source to drain. In the device, this results in more uncovered charge in the depletion layer near the drain end of the channel than near the source end. In the model in Fig. 4.4.4a, the charge Q_A contains essentially no component due to V_{ds}, since R_{ps} is small. In Fig. 4.4.4b, however, it can be seen that as V_{ds} approaches the pinch-off voltage V_{po}, it can by itself cause R_A to become infinite. Thus neither model is at all satisfactory in this regard.

Although more sophisticated, it is expected that a much better

compromise, in regard to the factors discussed above, is incorporated in the 1-lump T-model shown in Fig. 4.4.5. The relevant relationships for this model will now be presented, and calculated results from it will be given in Chapter 5, Section 5.4.

Writing equations as indicated in Fig. 4.4.5, gives

$$E = I_1 R_g + V_E \qquad (4.4.52)$$

$$V_A - V_F = (I_2 - I_4)/R_1 \qquad (4.4.53)$$

$$V_E - V_A = (I_3 - I_4)R_2 \qquad (4.4.54)$$

$$V_L = V_E - V_F \qquad (4.4.55)$$

$$V_L + V_D = I_5 R_L \qquad (4.4.56)$$

where

$$R_1 \equiv R_A + R_{pd} \qquad (4.4.57)$$

$$R_2 \equiv R_A + R_{ps} \qquad (4.4.58)$$

From equation 4.4.55 by differentiation,

$$\frac{I_4 - I_5}{C_L} = \frac{I_1 - I_3}{C_{gs}} - \frac{I_2}{C_{gd}} \qquad (4.4.59)$$

The defined normalized charges for model 1T are

$$X \equiv Q_A / Q_{ou} \text{ ; for lump A from } (I_3 - I_2) \qquad (4.4.59a)$$

$$Y \equiv (Q_1 - Q_3) / Q_{ou} \text{ ; for } C_{gs} \text{ from } (I_1 - I_3) \qquad (4.4.59b)$$

$$Z \equiv Q_2 / Q_{ou} \text{ ; for } C_{gd} \text{ from } (I_2) \qquad (4.4.59c)$$

Rearranging and combining from equations 4.4.52 through 4.4.56, and

equation 4.4.58, and normalizing in identically the same way as for model 3T in Section 4.4.1, produces

$$\frac{dX}{dT} = \frac{FRn}{V_o}\left[\frac{V_E - V_A}{R_2} - \frac{V_A - V_F}{R_1}\right] \qquad (4.4.60)$$

$$\frac{dY}{dT} = \frac{FRn}{V_o}\left[\frac{\left(\frac{C_{gs}}{C_L} + \frac{C_{gs}}{C_{gd}}\right)\left(\frac{C_{gd}}{C_{gs}}\right)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)}\right]\left[\frac{E - V_E}{R_g} - \frac{V_E - V_A}{R_2}\right]$$

$$+ \frac{FRn}{V_o}\left[\frac{\left(\frac{C_{gs}}{C_L} + \frac{C_{gs}}{C_{gd}}\right)\left(\frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)} - \frac{C_{gs}}{C_L}\right]\left[\frac{V_A - V_F}{R_1}\right]$$

$$+ \frac{FRn}{V_o}\left[\frac{\left(\frac{C_{gs}}{C_L} + \frac{C_{gs}}{C_{gd}}\right)\left(\frac{C_{gd}}{C_L}\right)}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)} - \frac{C_{gs}}{C_L}\right]\left[\frac{V_L + V_D}{R_L}\right] \qquad (4.4.61)$$

$$\frac{dZ}{dT} = \left[\frac{\frac{FRn}{V_o}}{\left(1 + \frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)}\right]\left[\frac{C_{gd}}{C_{gs}}\left(\frac{E - V_E}{R_g}\right) - \frac{C_{gd}}{C_{gs}}\left(\frac{V_E - V_A}{R_2}\right) + \left(\frac{C_{gd}}{C_{gs}} + \frac{C_{gd}}{C_L}\right)\left(\frac{V_A - V_F}{R_1}\right) + \frac{C_{gd}}{C_L}\left(\frac{V_L + V_D}{R_L}\right)\right] \qquad (4.4.62)$$

where n=1 for model 1T

Similar to Section 4.4.1 , the following equations also apply to model 1T. Thus

$$R_1 \equiv \frac{D_A}{S_A - X} + R_{pd} \qquad (4.4.63)$$

$$R_2 \equiv \frac{D_A}{S_A - X} + R_{ps} \qquad (4.4.64)$$

$$\frac{V_A}{V_o} = F_A (X)^{E_A} \qquad (4.4.65)$$

$$V_E = \frac{Q_{ou}}{C_{gs}} Y \qquad (4.4.66)$$

$$V_F = \frac{Q_{ou}}{C_{gd}} Z \qquad (4.4.67)$$

The output voltage and channel resistance for this model are given by

$$V_L = V_E - V_F \qquad (4.4.68)$$

and

$$R_{ch} = R_1 + R_2 - R_{ps} - R_{pd} \qquad (4.4.69)$$

4.4.3 Computer Programs

The computer programs used in the solution of models 3T and 1T are based on the earlier programs, but a number of improvements have been incorporated. The main overall difference is that these programs have been developed in the form of a main program with several subroutine sub-programs. This not only aids in program development, as each sub-program can be compiled and tested individually, but also facilitates the understanding and use of the programs. In addition to the main program, there are seven sub-routine sub-programs, named as follows: INITIL, SET, PRIME , BKUPS, BKDNS, BKUPP, and BKDNP. Block diagrams are presented for the main program in Fig. 4.4.6, and for the subroutines in Figures 4.4.7 through 4.4.11. A complete print-out of the statements for the main program and each subroutine appears in the Appendix.

Subroutine PRIME is the only part of this system of programs which must be changed depending on the model to be solved. The remaining programs in the system will accommodate both gate-charging and discharging transients, for models of either one or three lumps. Such a system is easily modified to accommodate a larger number of model lumps if desired.

A greater number of different straight line sections in the device $Q_{gg} - G_{ch}$ plot, and in the log-log $Q_{gg} - V_g$ plot is accommodated in this set of programs than in the early programs. Thus the complete switching range up to pinch-off can be accommodated with better accuracy. Separate "break-points" are included for the $Q_{gg} - G_{ch}$ relationship, and for the $Q_g - V_g$ relationship, and the factors F, B, D, and S, previously des-

cribed, are all set independently for each lump depending on the region of operation of that lump.

4.4.3.1 Discussion of Operation

The main program in Fig. 4.4.6 is basically similar to that shown in Fig. 4.3.5 and described in Section 4.3.3. The main difference here is that many of the program functions are carried out by subroutines which are called into operation as indicated. Block 1 appears quite different in that it contains essentially common statements instead of function statements which are not used. The purpose of a common statement as used here is merely to specify that variables having the same name in one or more programs and/or sub-programs have in fact the same physical storage location within the machine. Otherwise, the computer would treat them as being completely different and unrelated variables.

The test statements at the end of Block 4 are different from the corresponding ones in Fig. 4.3.5. In this program, a discharging transient can be calculated without first having gone through a discharging transient, depending on the specification in the data. As subsequently discussed, the factors F, B, D, and S for each lump must be differently set at a "break-point" depending on whether charging or discharging is in progress. This is handled by subroutines BKUPS and BKUPP, and subroutines BKDNS and BKDNP respectively.

The purpose of subroutine INITIL (Fig. 4.4.7) is to calculate from the data read into the machine, all the values associated with "break-points" in the Q_{gg} - G_{ch} and Q_{gg} - V_g relationships, and to correctly set all the factors for each lump to their region 1 values

(see Figures 4.3.2 and 4.3.3). BK1 through BK5 are the normalized charge "break-point" values. SX, FX, DX, BX in the program are the factors associated with lump A of the 3-lump model and so on. BKSX , BKSY, and BKSZ are the "break-point" values associated with the S and D factors, while BKPX, BKPY, and BKPZ are associated with the F and B factors. Note that SY , SZ, FY, FZ, DY, DZ, BY, and BZ are not required for the 1-lump model, so BKSY, BKSZ, BKPY and BKPZ are deliberately set so that they will have no further effect on the program.

The operation of subroutines BKUPS, BKDNS, BKUPP, and BKDNP is evident from the block diagrams in Figures 4.4.10 and 4.4.11. Subroutines BKUPS and BKUPP handle charging transients, while subroutines BKDNS and BKDNP handle discharging transients. The purpose of these subroutines is to test the normalized charge values for each lump X, Y, and Z, to determine if one or more associated "break-points" have been encountered. If not, control is returned to the calling program. If a "break-point" has been encountered for a particular lump for either the Q_{gg} - G_{ch} relationship, or the Q_{gg} - V_g relationship, the appropriate values of BKS, S and D, or of BKP, F and B are reset, according to whether a charging or discharging transient is involved.

Subroutine PRIME (Fig. 4.4.9) is designed so that the first time it is called, operation starts in Block 3 where all the fixed constants, used in the solution of the equations for a particular models, are calculated. Thereafter, when it is called, it goes directly to Block 4, where the variables such as R_1 ,R_2, R_3 ,V_A, V_B, etc., which depend on the normalized charge values, are calculated in preparation for substitution into the appropriate model equations in Block 5. After

solution of the equations, the calculated values are returned to the calling program.

The main purpose of the subroutine SET (Fig. 4.4.8) is to calculate the initial values of the normalized charges X, Y, and Z, depending on whether a charging or a discharging transient has been specified. In so doing, it also calls a subroutine BKUPS and BKUPP, and therefore correctly sets the values of BKS, BKP, S, D, F, and B for each lump according to the amount of initial charge in its capacitance element. This is accomplished by iteration to within a specified error tolerance .

4.4.3.2 Data Required

The data required by the programs for models 3T and 1T is similar to, though somewhat more extensive than, that required by the early programs. Each component of data, its location on the data card, and its description is shown in Table 4.2.

Comments in Section 4.3.1.2 relating to the type of each variable, its format on the card, etc., also apply to the data in Table 4.2. Values for each of these items of data will be obtained for several practical devices in Chapter 5, Section 5.3.

Chapter 5 will be concerned with illustrating the relative importance of the various factors discussed in this chapter. Calculated results for the various models presented here will be given and compared with measured transients in order to evaluate their effectiveness in representing the device.

TABLE 4.4.1

DATA FOR COMPUTER PROGRAMS FOR MODELS 3T AND 1T

Data Card 1

Item	Location on Card	Description
FET	cc1-10	Device code name (eg. TIX881-2)
QUICK	cc11-20	Gate voltage corresponding to Q_o - see Fig. 4.4.3
GO	cc21-30	G_{cho} - see Fig. 4.4.2
QO	cc31-40	Gate pinch-off charge - see Fig. 4.4.2
RPS	cc41-50	bulk parasitic source resistance
RPD	cc51-60	bulk parasitic drain resistance
VD	cc61-70	applied drain voltage - see model
I	cc72	I = 1 indicates program stop
LUMP	cc73	number of program lumps (i.e. 1 or 3)
LDISCH	cc74	= 1 indicates discharge transient desired, otherwise, gate charging transient assumed.

Data Card 2

Item	Location on Card	Description
G1	cc1-10	Total channel conductance at first "break-point" see Fig.4.4.2
G2	cc11-20	Total channel conductance at second "break-point" see Fig.4.4.2
G3	cc21-30	Total channel conductance at third "break-point" see Fig.4.4.2
V34	cc31-40	Point on straight line of section 1 (corresponding to Q_{34}) see Fig.4.4.3
V1	cc41-50	First "break-point" on $Q_{gg} - V_g$ relationship see Fig. 4.4.3
V2	cc51-60	Second "break-point" on $Q_{gg} - V_g$ relationship see Fig. 4.4.3
Q1	cc61-70	Gate charge at first "break-point" see Fig.4.4.2
Q2	cc71-80	Gate charge at second "break-point" see Fig.4.4.2

TABLE 4.4.1 Continued

Data Card 3

Item	Location on Card	Description
Q3	cc1-10	Gate charge at third "break-point" see Fig.4.4.2
Q34	cc11-20	Gate charge corresponding to V_{34} see Fig.4.4.3
Q4	cc21-30	Gate charge corresponding to V_1 see Fig.4.4.3
Q5	cc31-40	Gate charge corresponding to V_2 see Fig.4.4.3
E	cc41-50	Applied gate driving voltage see model
R_G	cc51-60	External gate series resistance
R_L	cc61-70	Load resistance
C_L	cc71-80	Load and stray drain source capacitance

Data Card 4

Item	Location on Card	Description
CGS	cc1-10	Stray gate-source capacitance see model
CGD	cc11-20	Stray gate-drain capacitance see model
F	cc21-30	Dimensionless normalizing factor see text, Section 4.3.1.2
TF	cc31-40	Specified final normalized time for transient
NTNCH	cc41-50	Program time at which first change in increment size occurs
NTNCH2	cc51-60	Program time at which second change in increment size occurs
NDT	cc61-65	Program time initial increment size
NDT1	cc65-70	Program time second increment size
NDT2	cc71-75	Program time third increment size

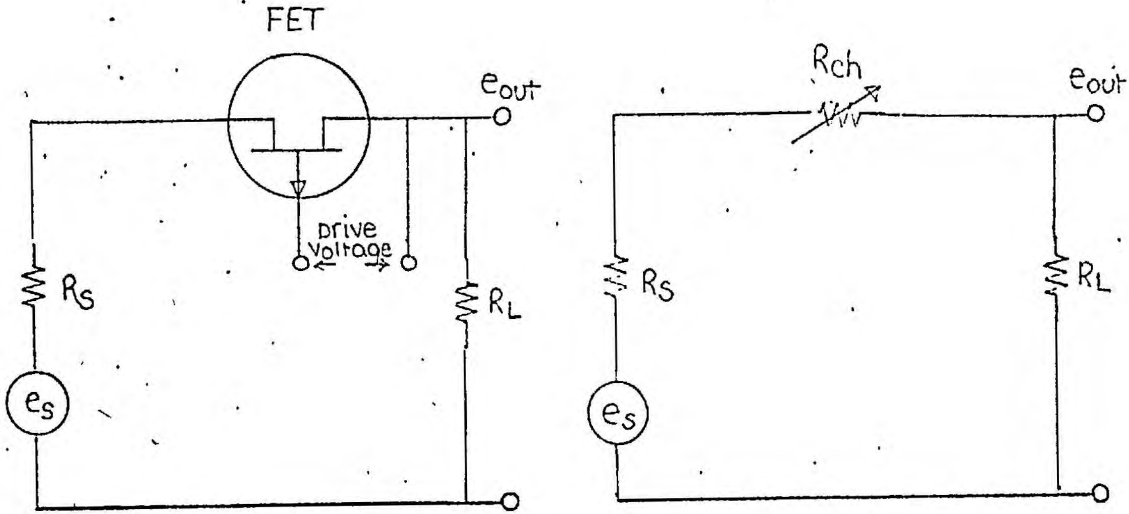


Fig. 4.2.1 : Series FET Chopper

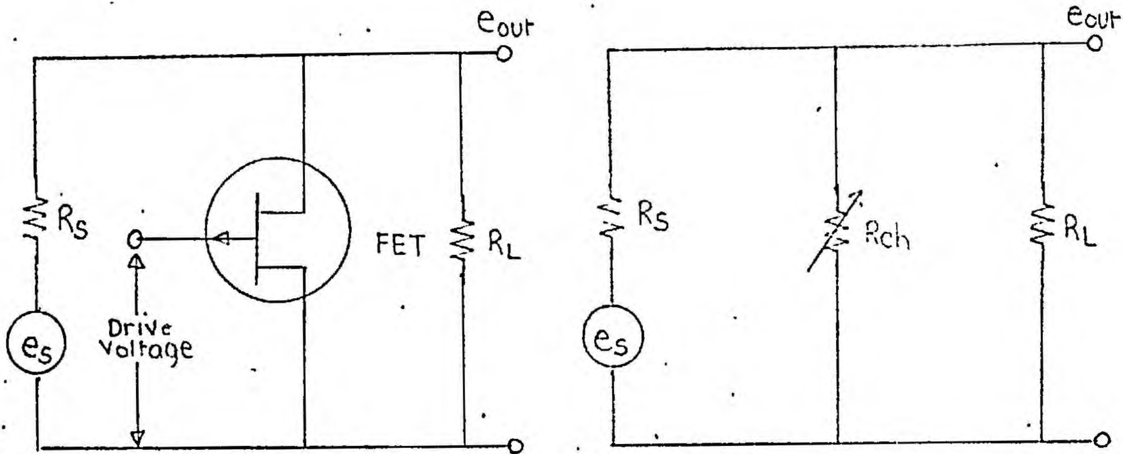


Fig. 4.2.2 : Parallel FET Chopper

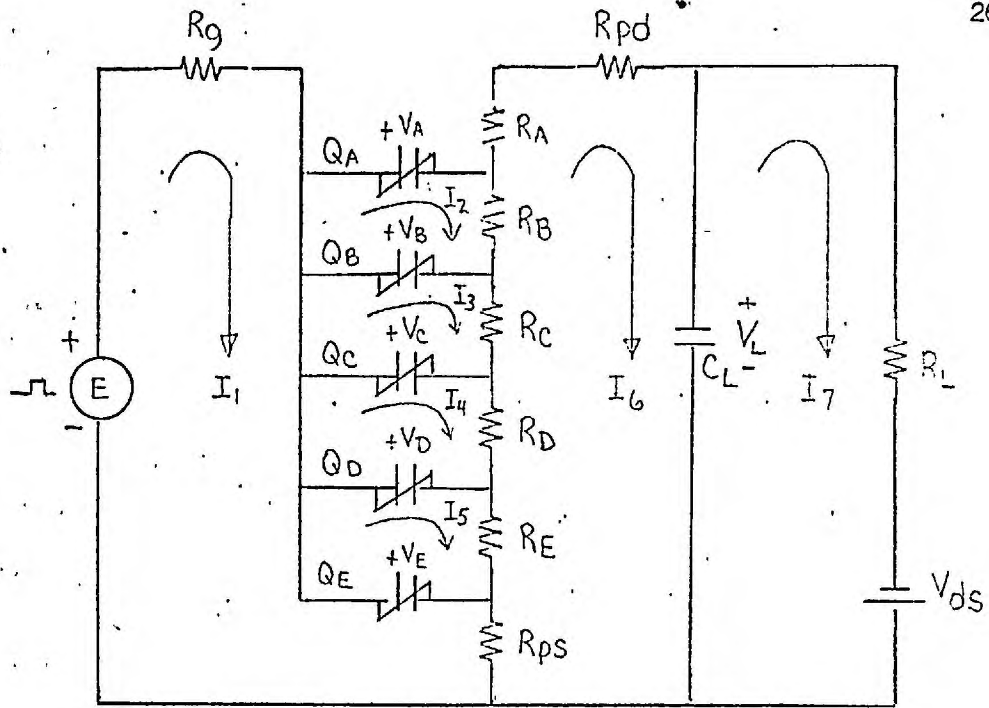
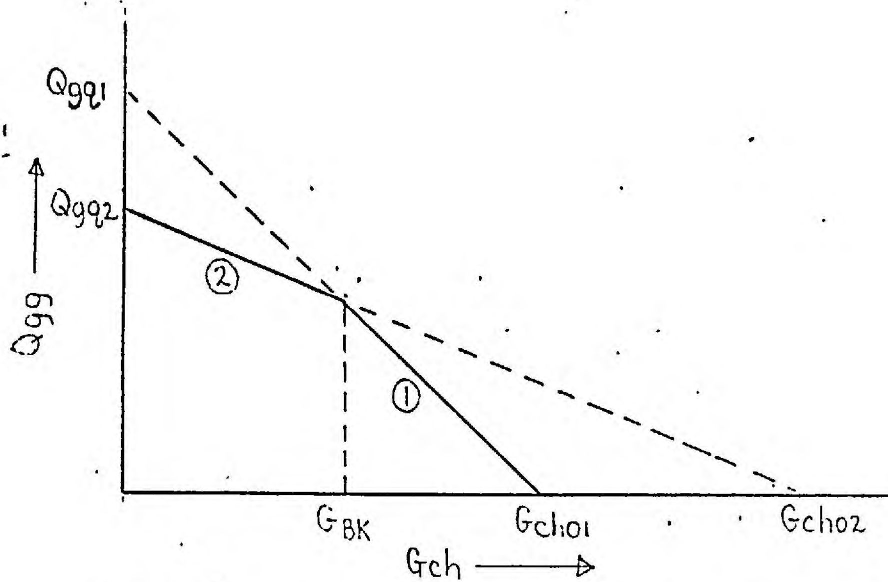
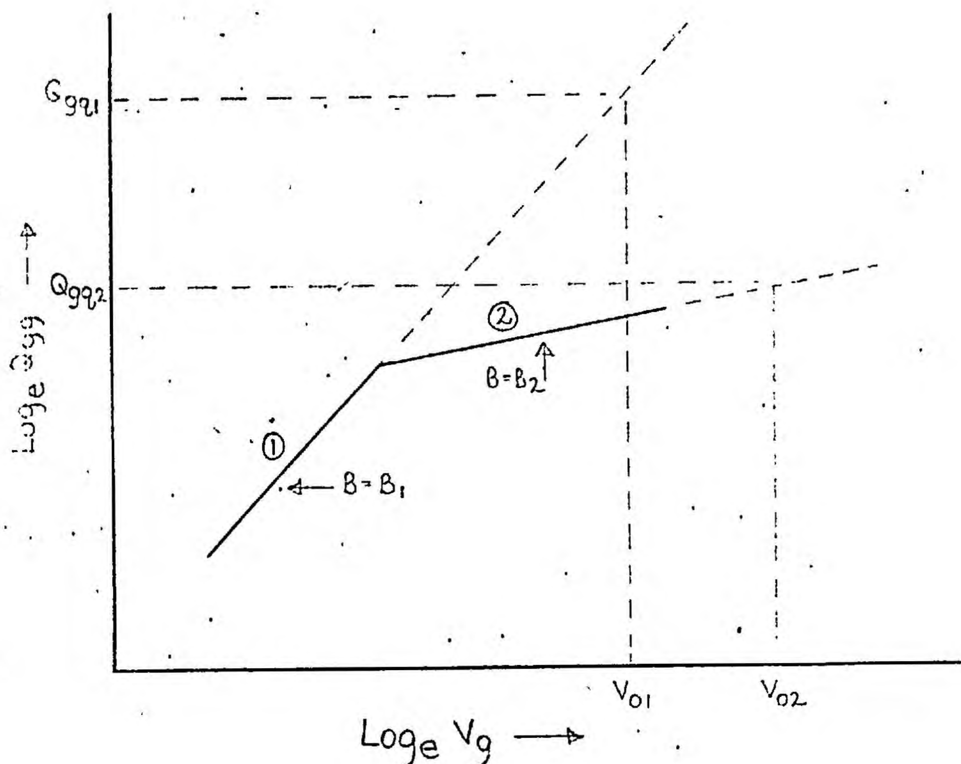


Fig. 4.3.1 : 5-Lump "L"-Model



Where Q_{gq_1} , G_{cho_1} = values used in Section 1
Q_{gq_2} , G_{cho_2} = values used in Section 2

Fig. 4.3.2 : Assumed Form of Q_{gg} - G_{ch} Plot for Early Models



where Q_{gq_1} , V_{o_1} = values used for section 1 in equation 3.5.3.18.

Q_{gq_2} , V_{o_2} = values used for section 2 in equation 3.5.3.18.

(see also Fig. 4.3.2)

Fig. 4.3.3 : Assumed Log-Log Q_{gg} - V_g Plot For Early Models

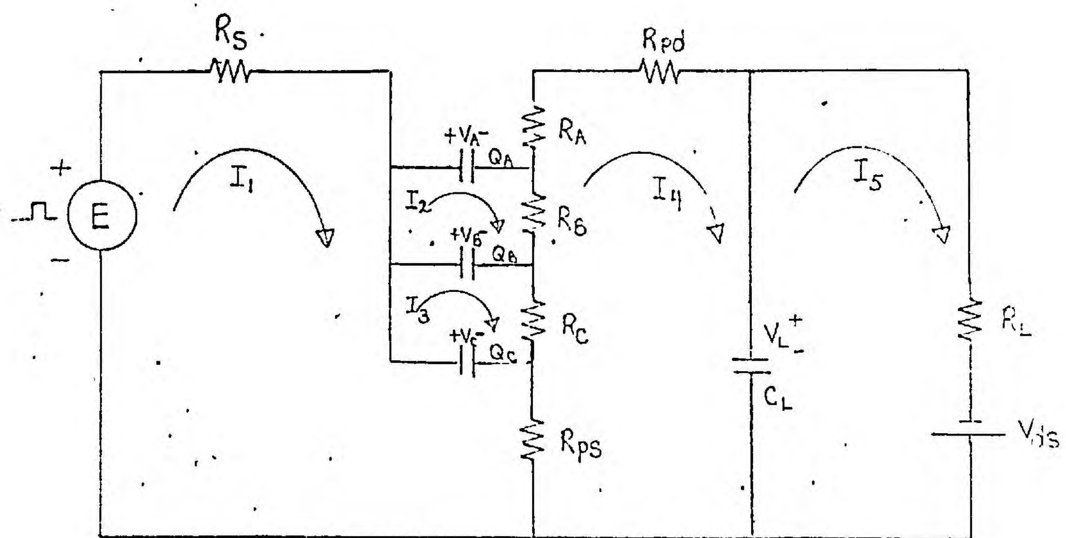


Fig. 4.3.4 : 3-Lump L-Model

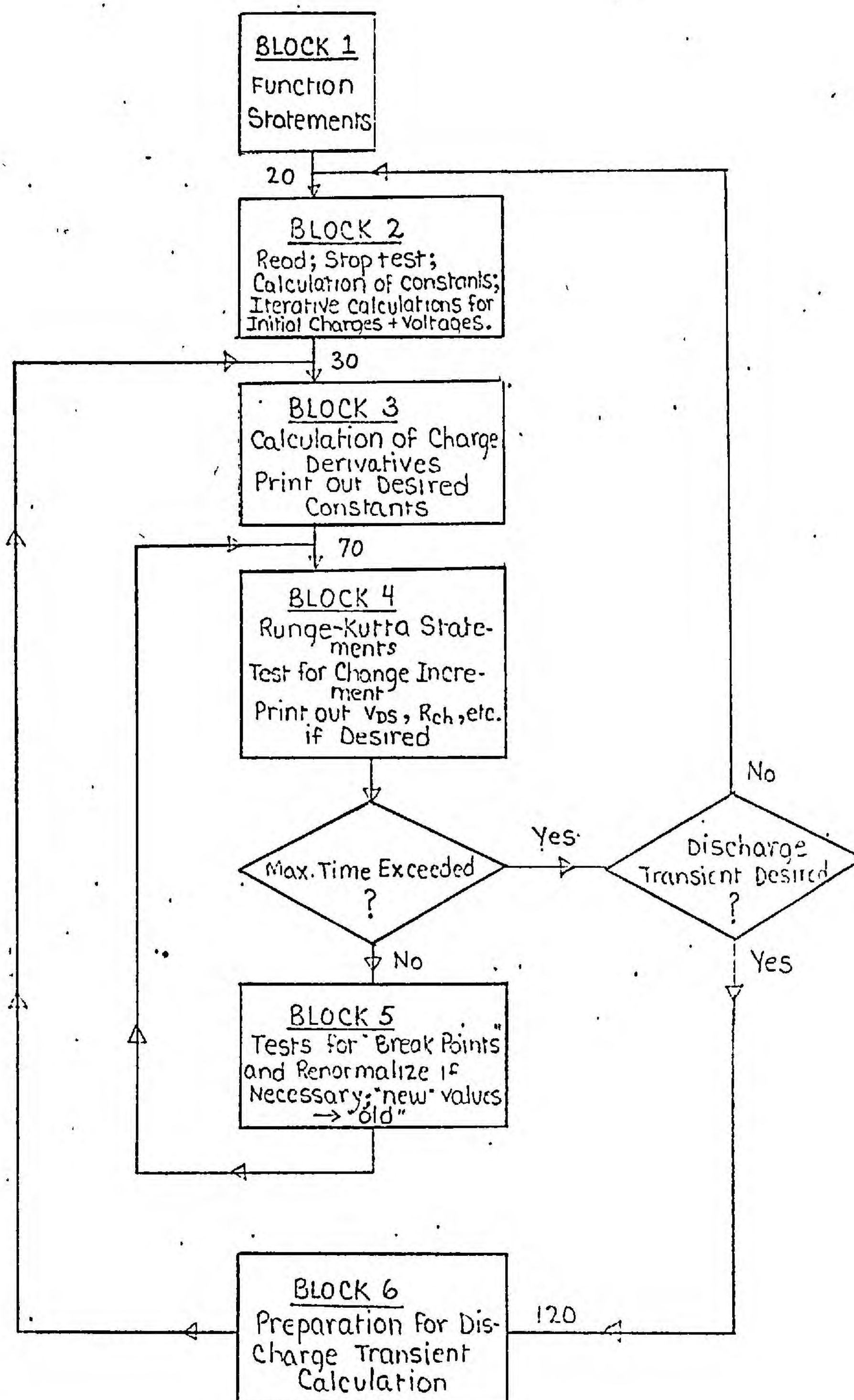


Fig. 4.3.5 : Overall Block Diagram of Computer Program for Models 5L and 3L

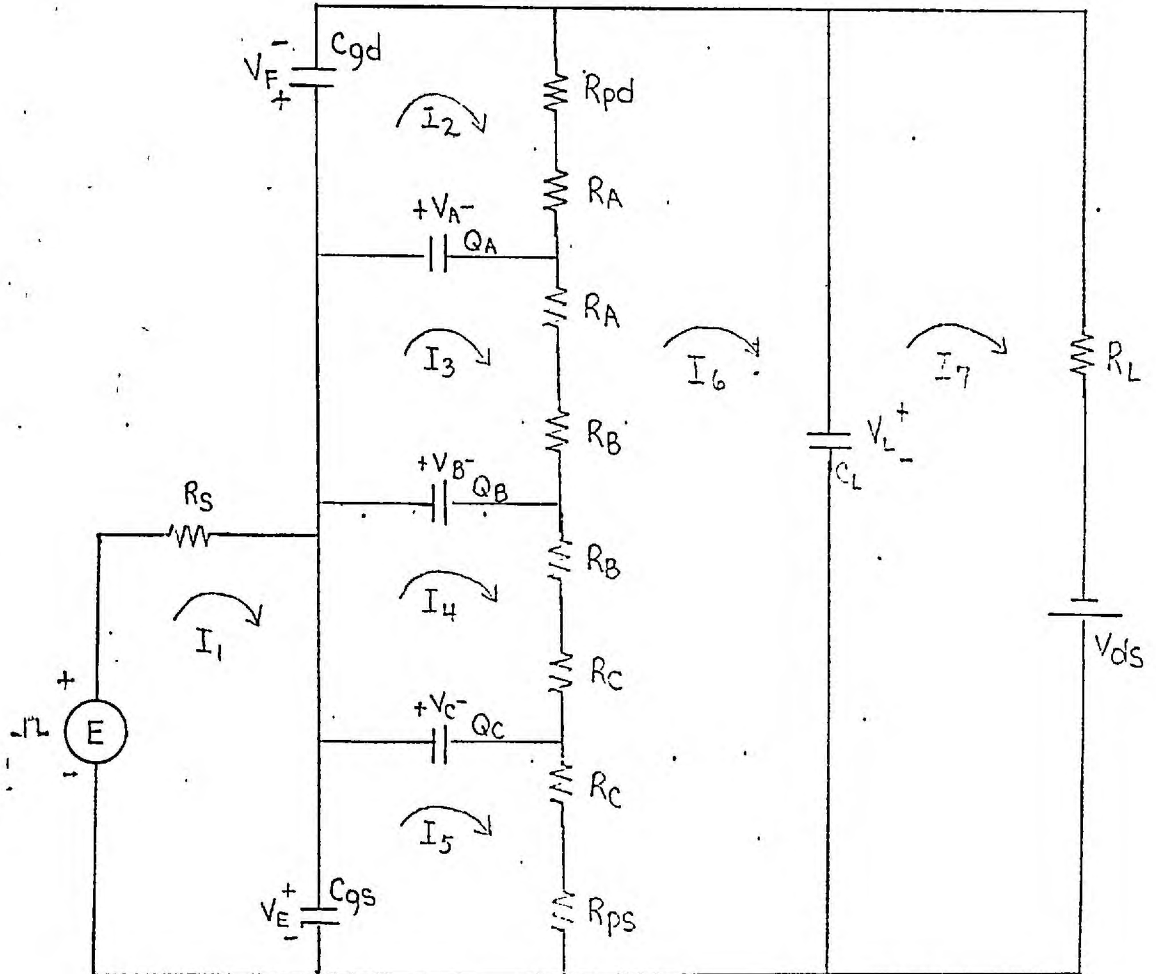


Fig. 4.4.1 : 3-Lump T-Model

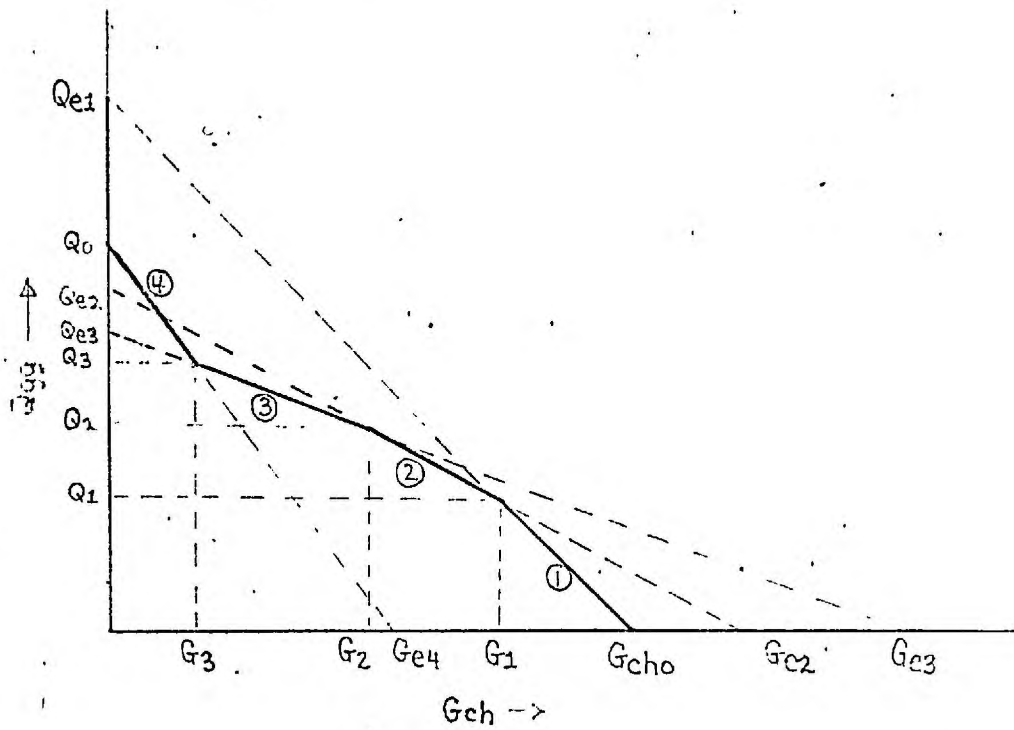


Fig.4.4.2 : Generalized Gate Charge-Channel Conductance Plot Represented by Four Straight Lines

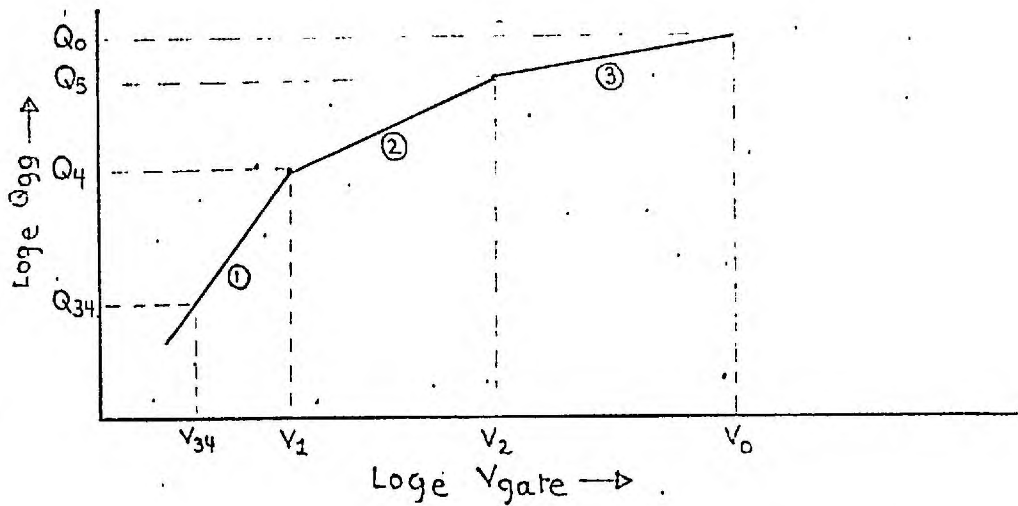
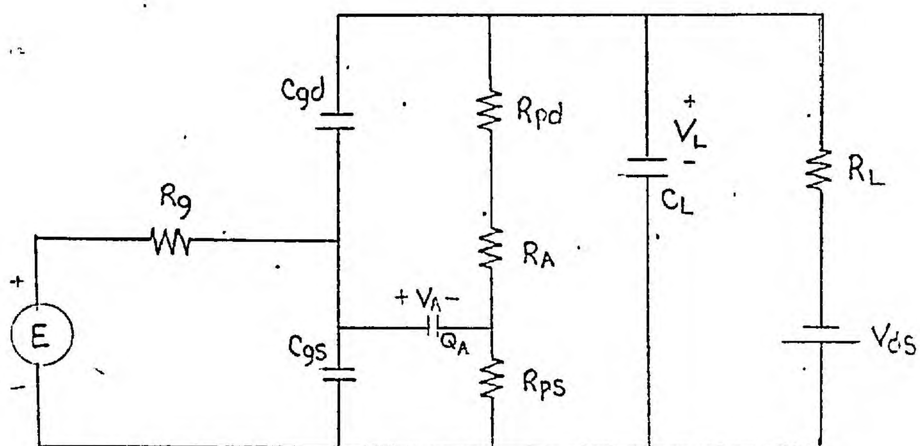
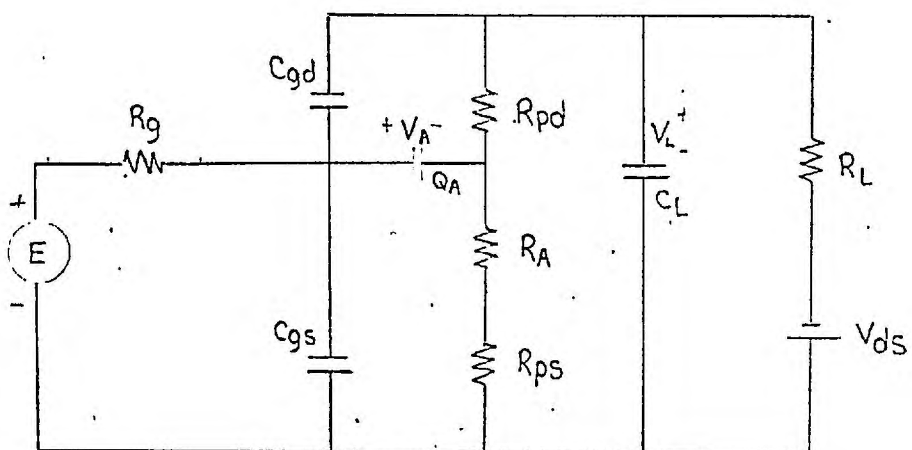


Fig. 4.4.3 : Generalized Log-Log Q_{gg} - V_g Plot



(a)



(b)

Fig. 4.4.4 : Possible 1-Lump Model Configurations

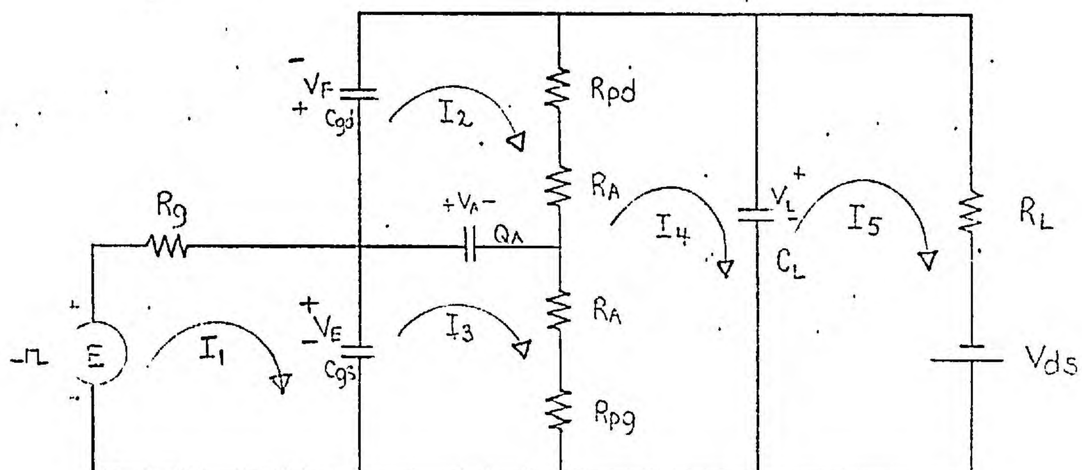


Fig. 4.4.5 : 1-Lump T-Model

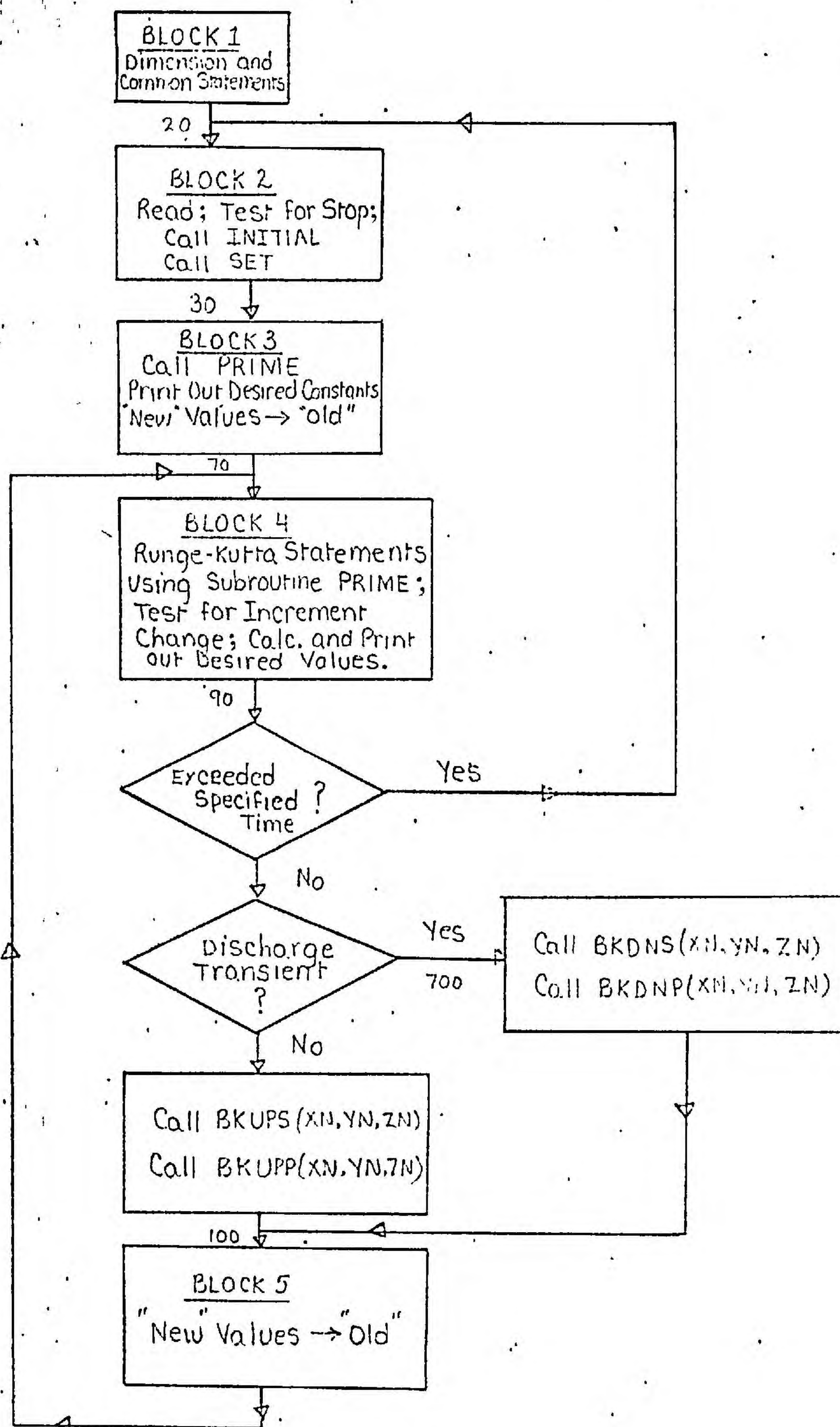


Fig. 4.4.6 : Block Diagram of Main Program for Models 3T and 1T

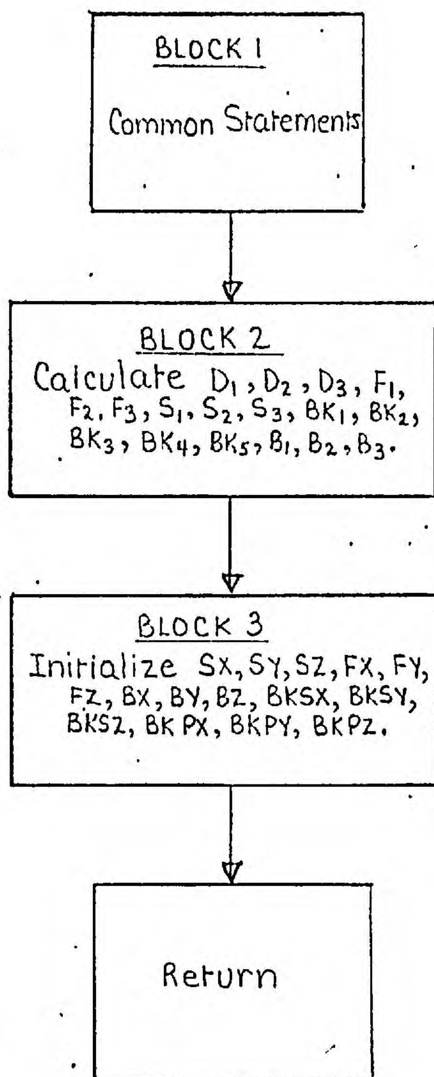


Fig. 4.4.7 : Block Diagram for Subroutine INITIL

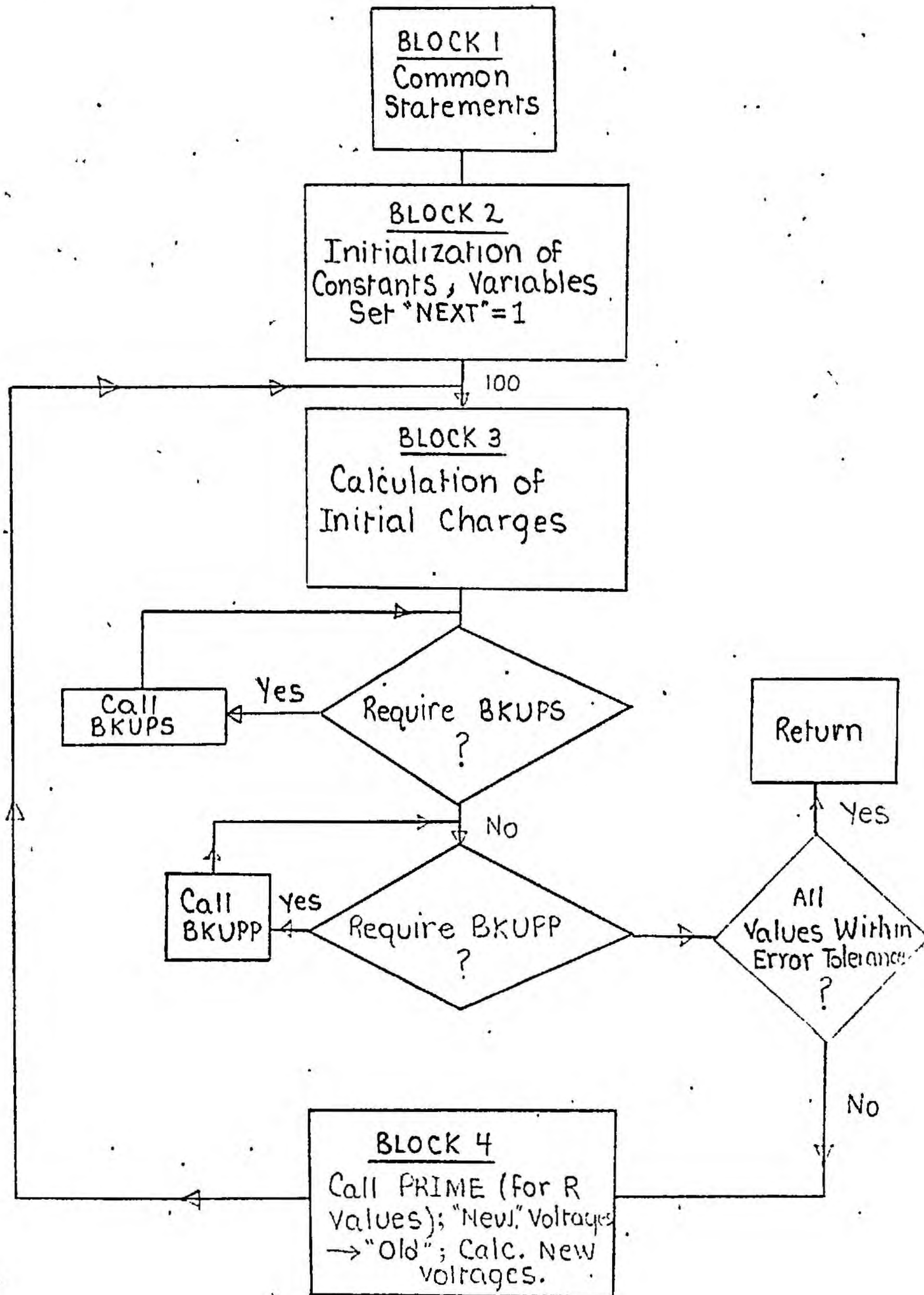


Fig. 4.4.8 : Block Diagram for Subroutine SET

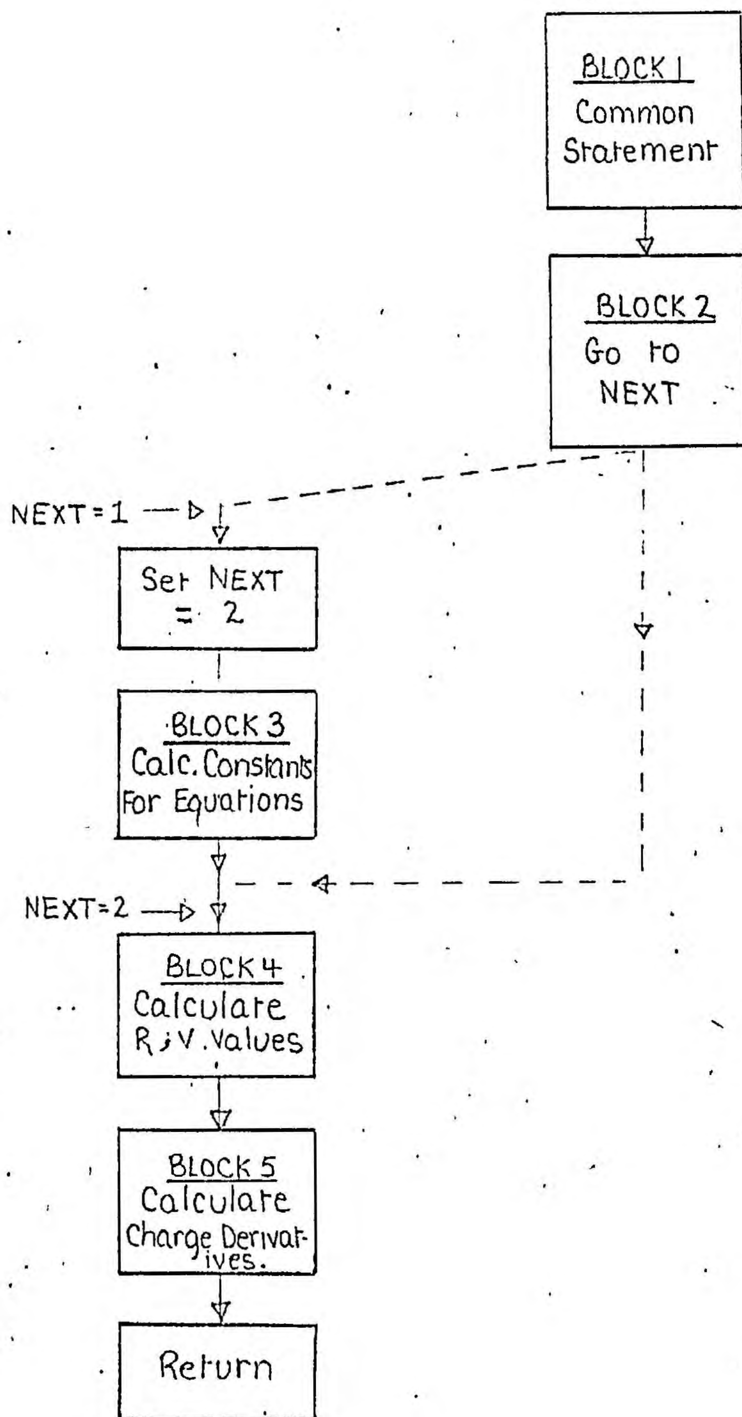


Fig. 4.4.9 : Block Diagram of Subroutine PRIME

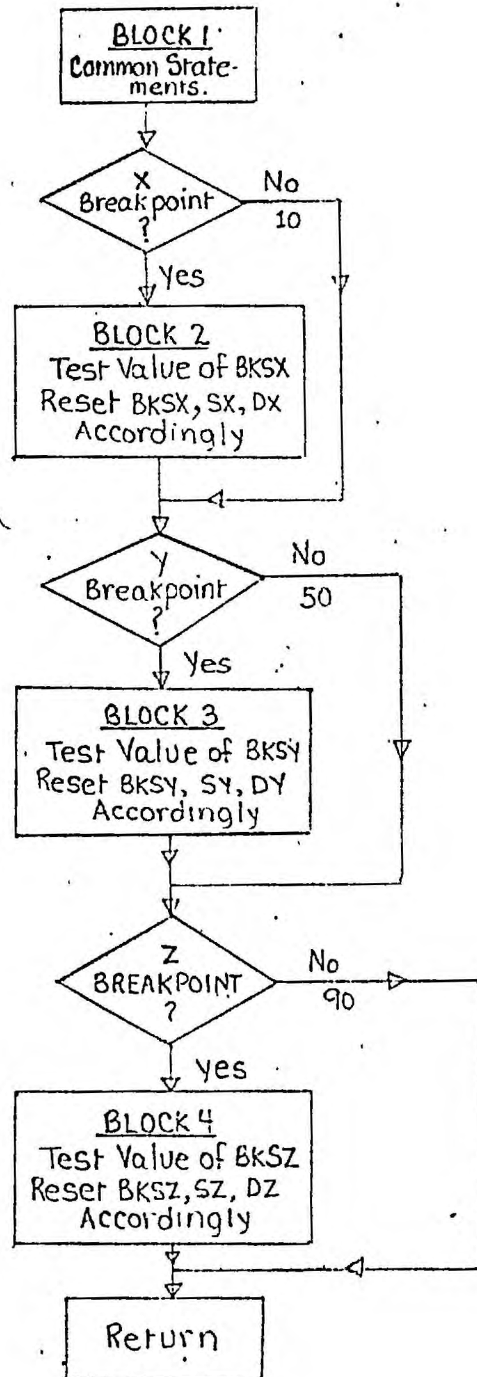


Fig. 4.4.10 : Block Diagram for Subroutines BKUPS and BKDNS

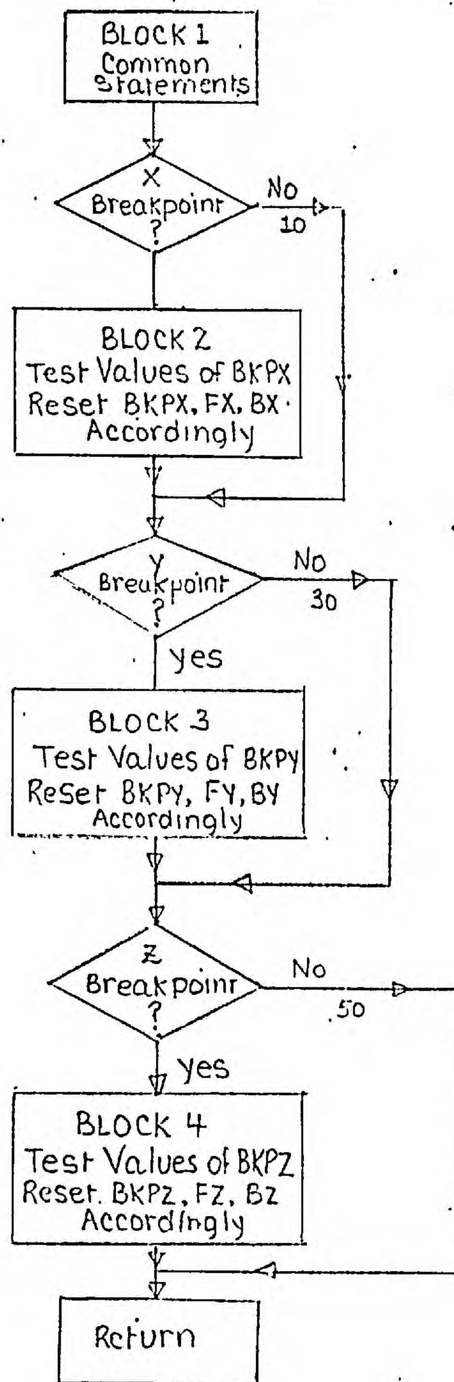


Fig. 4.4.11 : Block Diagram for Subroutines BKUPP and BKDNP

CHAPTER 5

LOW LEVEL SWITCHING MEASUREMENTS AND RESULTS

5.1 Introduction

In Chapter 4, the main factors affecting the low level switching processes in field-effect transistors were discussed, and switching models representing the device were presented. This chapter is concerned with illustrating typical switching transients, and presenting the results of measurements on representative devices to demonstrate the relative importance of the factors affecting switching. Further, calculated results from each of the models are presented and compared with corresponding measured transients for four representative FET's and an MOST.

A block diagram and description of the method of measurement used to obtain the results for the switching transients, are presented in Section 5.2. The method of determining the switching parameters for the devices studied is illustrated, and the switching parameters involved are summarized in Section 5.3. The calculated and measured switching transients are presented and discussed in Section 5.4.

5.2 Switching Transient Measurement Method

Output transient switching voltages were measured for several different device samples under various operating conditions, using the measurement jig illustrated in Fig. 5.2.1. This is constructed on a piece of double copper clad fibre board, A section of 50 Ω strip line is included, which enables the pulse to be conveniently brought to the jig and terminated with a coaxial 50 Ω load. Low capacitance transistor

sockets are constructed on the jig in the form of short lengths of fine bore metal tubing. Similar, but larger bore tubing is used to make easy connection and removal of the series gate resistor and a load resistor. Metal film high frequency resistors are used for these purposes. A socket is provided in the output circuit to accept the probe of the sampling oscilloscope which measures the output voltage.

When used in this way, the isolator (75) must be used on the sampling oscilloscope probe. The reason for this is that the impedance of the drain circuit is changing throughout the transient. Without the isolator, such an impedance change can produce a shift in the base line of the oscilloscope trace as a result of reflections of the very short sampling pulses from the probe. The isolator is basically a short length of transmission line which delays any reflections until after the sampling diodes have stopped conducting, so that they can no longer have any effect on the base line.

A block diagram of the complete system used for the measurement of switching transients is shown in Fig. 5.2.2. A coaxial outside coupling capacitor (76) is used to supply the external voltage to the mercury relay switch. The purpose of the rather complicated arrangement of attenuators and blocking capacitors, is to provide an accurate 50 Ω source impedance for the pulse transmission line to the measuring jig. The use of a trigger "take-off" system in the pulse line itself was found to produce unwanted reflections on the line. This is due to the capacitive effects of charge being delivered to the FET or MOST, during which time the transmission line termination is not a true 50 Ω.

The outside coupling capacitor at the jig end of the transmission

line, is unnecessary for charging transients applied with respect to zero voltage, but is used to fix the device gate bias when measuring discharging transients. In such a case, the system is adjusted so that the closing of the mercury relay switch produces a net voltage such that the fixed bias at the device gate is reduced to zero, thus discharging the gate.

The measuring system was calibrated against a measured d-c voltage to produce the transient voltage of the desired sensitivity on the vertical (Y) axis of the X-Y recorder. The time scale of the sampling oscilloscope was used to calibrate the horizontal axis of the X-Y recorder to time. The measured output transients were then produced directly on graph paper by the X-Y recorder. Measured transients for several devices are shown in Section 5.4.

5.3 Switching Parameters

5.3.1 Device Parameters

Calculated and measured results are presented in Section 5.4 on devices representative of the types studied in the earlier parts of this thesis. The required switching data for each device for both the early computer programs and the second generation computer programs are derived and presented in this section. The alloyed gate germanium devices are represented here by device TIX881-2 and TIX883-1. Device 2N2498-1 represents the double diffused silicon planar structures, and device 2N3824-2, the diffused epitaxial planar class of device. Some results will also be presented on MOST 6 to illustrate the MOST or insulated gate class of devices.

As indicated in Chapter 4, all the necessary switching parameters for each FET are obtained from the Q_{gg} versus G_{ch} relationships, and from the log-log plot of Q_{gg} versus V_g. The log-log plot is unnecessary in the case of the MOST, however, as a result of the constant gate capacitance for these devices. R_{ps} and R_{pd} are assumed to be zero in accordance with earlier work, since the Q_{gg} versus G_{ch} relationship for the total device will be used.

Switching results are presented in Section 5.4 for devices TIX881-2, TIX883-1, 2N2498-1, 2N3824-2, and MOST 6. The gate charge versus channel conductance relationships for TIX881-2, TIX883-1, 2N3824-2, and MOST 6 have been presented and discussed in Chapter 3. The gate charge versus channel conductance relationship for device 2N2498-1 was obtained in the same way, and this device is used to represent the double diffused silicon planar FET's in this chapter.

Figures 5.3.1 and 5.3.2 show the Q_{gg} versus G_{ch} relationship, and the log-log Q_{gg} versus V_g relationship for device TIX881-2. The construction lines indicated on these figures are specifically intended to illustrate the method of obtaining data for the early computer programs for models 5L and 3L for a practical device. These figures correspond to the general form of these relationships discussed in Chapter 4, Section 4.3, and presented in Figures 4.3.2 and 4.3.3 respectively.

Figures 5.3.3 and 5.3.4 show the Q_{gg} versus G_{ch} relationship, and the log-log Q_{gg} versus V_g relationship for device TIX881-2. The construction lines on these figures are intended to illustrate the method of representing these relationships for a practical device for the second generation computer programs, for models 3T and 1T. These relationships thus corres-

pond to the generalized forms assumed in Chapter 4, Section 4.4 in Figures 4.4.2 and 4.4.3 respectively.

The data thus obtained for each device, and used for the computed results given in Section 5.4, is summarized in Table 5.3.1 for the early computer programs for models 5L and 3L, and in Table 5.3.2 for models 3T & 1T for the second generation computer programs. The data for MOST 6 assumes that it will be used only as a depletion device. In other words, it will be used only with negative applied gate voltages which remove conduction charge from the channel, and increase the channel resistance from the $V_g = 0$ value. This is comparable to reverse biasing the gate of a junction FET, and is thus easily compatible with the existing computer programs.

5.3.2 Circuit Parameters

The jig and circuit parameters used in the calculations in Section 5.4 were measured on the Wayne Kerr B221 component bridge with an external signal generator and detector. High frequency, metal oxide resistors were used in the jig, but some small changes in the effective component values inevitably occur throughout the transient associated with frequency effects. A frequency of 10 KHz was used for these measurements. The B221 bridge was preferred due to its very high inherent accuracy (0.1%).

The probe plus isolator were incorporated into the measurement of R_L and C_L. It should be noted that the probe sampling diodes are continuously being switched off and on, thus changing their instantaneous impedance, although their "on" periods are extremely short. The repetition frequency of the pulse generator in such a system directly affects the average "on" time of the sampling diodes since they are turned on

TABLE 5.3.1

SWITCHING DATA FOR EARLY PROGRAMS FOR DEVICES 2N3824-2, TIX881-2, TIX883-1, 2N2498-1, AND MOST 6 (see also TABLE 4.3.1)

Parameter	Device				
	2N3824-2	TIX881-2	TIX883-1	2N2498-1	MOST 6
B	1.23	1.56	1.46	1.26	1.0
BFIN	1.23	1.56	1.73	1.26	1.0
RO (Ω)	132.1	1328.0	420.0	359.7	2222.2
QO (picocoulombs)	24.0	74.1	67.5	49.2	7.1
DK (volts)	6.15	5.45	3.1	2.82	1.23
GSDBK (mmhos)	3.29	0.49	0.66	1.43	0.0
ROFIN (Ω)	87.15	1190.5	555.0	274.35	0.0
QOFIN (picocoulombs)	19.1	62.2	77.5	39.5	0.0
DKFIN (volts)	4.58	4.18	4.24	2.15	0.0
Drain-source Capacitance (pf)	-	-	-	-	6.8

TABLE 5.3.2

SWITCHING DATA FOR SECOND GENERATION PROGRAMS FOR DEVICES 2N3824-2, TIX881-2, TIX883-1, 2N2498-1, and MOST 6. (see also TABLE 4.4.1)

Parameter	Device				
	2N3824-2	TIX881-2	TIX883-1	2N2498-1	MOST 6
QUICK (volts)	4.56	5.2	5.7	2.65	1.23
GO (mmhos)	7.5	0.76	2.38	2.78	0.45
QO (pico-coulombs)	19.1	69.3	91.6	45.6	7.1
R_{ps} , R_{pd} (Ω)	0	0	0	0	0
G_1 (mmhos)	6.22	0.49	0.81	1.88	0.0
G_2 (mmhos)	4.1	0.06	0.25	1.13	0.0
G_3 (mmhos)	2.15	0.0	.08	0.28	0.0
V_{34} (volts)	0.3	0.25	0.3	0.3	0.5
V_1 (volts)	0.546	0.62	2.0	1.5	1.23
V_2 (volts)	2.0	3.28	5.7	2.65	1.23
Q_1 (pico-coulombs)	4.5	26.2	44.6	16.8	7.1
Q_2 (pico-coulombs)	11.05	57.75	65.0	30.2	7.1
Q_3 (pico-coulombs)	15.5	69.25	77.5	36.4	7.1
Q_{34} (pico-coulombs)	2.05	9.09	13.75	8.2	2.9
Q_4 (pico-coulombs)	3.45	18.08	50.4	30.0	7.1
Q_5 (pico-coulombs)	9.95	53.7	91.6	45.6	7.1
Drain-source Capacitance(pf)	-	-	-	-	6.8

once for each pulse generator pulse. With the mercury relay pulse generator used in these measurements, the repetition rate is very low (approximately 700 pulses per second), and it was found that the measured R_L and C_L values were independent of oscilloscope control settings. The load capacitance C_L in each case also includes the effect of stray capacitance from drain to ground of the empty transistor can. This results in a slightly different value of C_L for each device, since the can configuration is different (eg. 4-lead TO-5 can and 3-lead TO-5 can). The same situation also applies to the stray can-plus-jig gate to source capacitance, and to the stray can-plus-jig gate to drain capacitance.

The load capacitance for the MOST also includes an additional component due to the depletion layer capacitance associated with the junction between the N-type drain contact and the P-type substrate. Throughout the work, the MOST's have been used with the substrate connected to the source . As discussed in Chapter 2, Section 2.6, the main result of this is an added component of capacitance between drain and source. This capacitance is , of course, voltage dependent, but under low level switching conditions, the drain-source voltage is small enough that this capacitance can conveniently be assumed constant at its zero voltage value.

Small signal measurements of this capacitance were made on the Wayne-Kerr B221 bridge on a total of four MOST's after initially balancing the bridge with an empty can in the transistor socket. The measurements were made at zero drain to source voltage, covering a wide range of channel resistance. The measured capacitance for each device was found to be essentially independent of gate bias. For MOST 6, used here, the drain to source capacitance was found to be 6.8 pf.

An outside coupling capacitor was also found to provide a convenient method of applying a voltage through the load resistor to the drain. In this case, an equivalent load resistance and applied voltage were obtained and used for calculation in the models. Similarly, an equivalent pulse voltage E and gate series resistance were also used in the calculations.

The measured stray gate to source capacitance, and gate to drain capacitance for each device are summarized in Table 5.3.3. The measured values of R_L, R_g and C_L applying to each transient are shown on the corresponding figures. The value of C_L varies in each case depending on the stray drain to source can capacitance, and also on the preamplifier (i.e. 187B or 187C, which require different probe socket configurations) used with the sampling oscilloscope for a particular measurement.

5.4 Calculated and Measured Results

It is intended to present firstly in Section 5.4.1, the results of measurements to illustrate typical transients and to indicate the relative importance of the various factors affecting the switching transients. In addition, in Section 5.4.2, comparisons between calculated and measured results will be presented to study the effectiveness of the various models derived in Chapter 4, in representing the low level switching performance of these devices.

As previously indicated, the main emphasis throughout is on FET switching, but some results will be presented on one MOST for comparison. The pertinent data for each of the devices used here has been presented in Section 5.3.

TABLE 5.3.3

MEASURED STRAY CAPACITANCES C_{gs} AND C_{gd}.

Parameter	Device				
	2N3824-2	TIX881-2	TIX883-1	2N2498-1	MOST 6
C_{gs} (picofarads)	1.66	1.31	1.31	2.42	1.46
C_{gd} (picofarads)	.11	0.21	0.21	0.86	0.10

5.4.1 Measured Transients

For use as a chopper, as discussed in Chapter 4, both the amplitude and duration of the transients associated with the switching are important. Two transients are produced in the output circuit during each cycle, one while turning the device on (i.e., discharging the gate of an FET), and one while turning the device off (i.e., charging the gate of an FET). Fig. 5.4.1 shows a typical pair of charging and discharging transients measured for device TIX881-2 under the conditions noted on the figure.

The main point illustrated by Fig. 5.4.1 is that the gate charging transient is both larger in amplitude, and longer in duration, than the gate discharging transient. This is generally the case for these devices, though the difference between the two transients depends on the device, the circuit parameters, and on the applied gate voltage. The reasons for this will be brought out in subsequent discussions. It is thus clear, however, that the longer gate charging transient is the more important of the two from the point of view of switching. Consequently, the work in this chapter is mainly concerned with the transients, associated with charging the FET gate, which increase the channel resistance and tend to turn the device off. Most of the results presented in this chapter have also been obtained with zero external voltage applied to the drain. This is valid , as the small drain voltages applicable to the low level switching situation are normally small enough not to affect the switching processes in the device. Calculated and measured results will be presented in Section 5.4.2 to further illustrate a discharge transient, and to illustrate a typical transient with an external applied drain voltage.

In order to study the switching processes further, gate charging transients were measured on each of three representative FET's (TIX881-2, 2N2498-1, and 2N3824-2) for a range of switching voltage E, load resistance R_L, and gate resistance R_g. A representative transient waveform is shown in Fig. 5.4.2. The transient waveforms for the MOST are similar in form, as will be seen in Section 5.4.2. From each of the transients, as indicated in Fig. 5.4.2, the peak value of the transient (V_{peak}) was noted, as was the time (T_{peak}) at which the peak occurred, and the time (T_{fall}) required for the transient to fall to 10% of its peak value. This information for one of the devices (2N2498-1) is summarized in Fig. 5.4.3 in the form of "trend plots". Fig. 5.4.3 shows V_{peak}, T_{peak}, and T_{fall} plotted against R_g with the gate switching voltage E as a parameter, for each of three values of load resistance R_L. These plots are intended to show at a glance the relative importance of the factors affecting the FET switching processes, and the trends associated with changing these factors. The main points illustrated by Fig. 5.4.3 will now be discussed briefly.

The peak value of the switching transient (Figures 5.4.3a, b, c) is found to depend markedly on the size of R_g and the gate driving voltage E, and hence on the rate at which charge is delivered to the gate. The largest transients occur at the largest value of E, and lowest value of R_g. It is interesting to note that increasing R_L from 1KΩ to 100KΩ has little effect on the peak value of the transient for E= 1.0 volt and 1.75 volts. Further, the increase in R_L causes only a small increase in V_{peak} for E=2.5 volts, more noticeably at the larger values of R_g.

The time (T_{peak}) at which the peak value of the transient occurs (Figures 5.4.3d,e,f) is relatively independent of R_L and E at the lowest value of R_g (=35Ω). At a given value of R_L, T_{peak} increases with both E and R_g, being largest when E=2.5 volts and R_g =1KΩ. Increasing R_L from 1KΩ to 100kΩ produces a relatively small increase in T_{peak} for the lower values of E and higher values of R_g. T_{peak} increases by about a factor of three, however, for E=2.5 volts at R_g=1KΩ in going from R_L=1KΩ to R_L= 10.8KΩ. A much smaller increase occurs as R_L is further increased to 100kΩ.

In Figures 5.4.3g, h, i, the fall time at a given value of R_L is seen to be largest corresponding to the largest values of E and R_g at 2.5 volts and 1.0KΩ. At the largest value of E, T_{fall} is found to increase very considerably by a factor of approximately 10 , as R_L is increased from 1KΩ to 100kΩ. Thus the transient decay time is primarily determined by R_L (and C_L) at the larger values of switching voltage where the channel resistance is large in comparison with R_L.

The form of the "trend plots" for devices TIX881-2 and 2N3824-2 is similar to those for device 2N2498-1 shown in Fig. 5.4.3. The main difference is one of scaling. Direct comparison between devices is complicated by the fact that they have different values of V_{po}, R_{cho}, and L^2/μ ratios. In general, however, the plots for device TIX881-2 were poorer than those for 2N2498-1 in Fig. 5.4.3, while those for device 2N3824-2 were generally better than those for 2N2498-1, from the point of view of switching.

Thus, for a corresponding value of switching voltage E to produce the same ratio of R(off)/R(on)in the channel resistance of each device,

the values of V_{peak}, T_{peak}, and T_{fall}, were all generally larger for device TIX881-2 than for device 2N2498-1 in Fig. 5.4.3. Correspondingly, the values of V_{peak}, T_{peak}, and T_{fall} for device 2N3824-2 were generally smaller than those for 2N2498-1. The "progression" in the quality of these devices for switching purposes, corresponds to the "progression" of their values of R_{cho}, and their L^2/μ ratios. Thus, the best switching device (2N3824-2) has the lowest value of R_{cho}, and also the lowest value of L^2/μ ratio.

The models derived in Chapter 4 will be evaluated in the subsequent section. On the basis of the results in Figure 5.4.3, it can be assumed that a severe test of a model representing the switching processes in a device occurs under conditions of a large driving voltage E with a small value of gate resistance R_g. Under these conditions, as seen in Fig. 5.4.3, the rate of charging of the gate circuit is very high, and thus the rate of change of channel resistance must be very high. If a relatively large load resistor is also present, the bulk of the charging current in the channel must flow out of the source lead, causing differential charging which can contribute to channel shape distortion as discussed in Chapter 4. Additionally, the size of the transient voltage on the drain can, by itself, be large enough under these circumstances to violate the assumed true low level switching conditions.

5.4.2 Comparison of Low Level Switching Models

As discussed in Chapter 4, and in Section 5.4.1 above, the switching processes in the FET are very considerably affected by the circuit parameters as well as by the device parameters. Thus the effectiveness of a given model, in representing the switching processes, particularly in regard to the lumping configuration, and to the number of lumps used, depends not only on the device, but also on the conditions under which the device is switched. It is therefore virtually impossible to calculate and present results from each of these models for several devices covering the complete range of switching conditions.

The results in this section are presented with the following objects in mind. Firstly, it is intended that they should demonstrate the applicability of the charge control approach and the methods used in this low level switching study of field-effect transistors. Secondly, it is desired to present sample results to compare the effectiveness of the models presented in Chapter 4, with particular regard to the effects of the number of model lumps, and to the complexity of the lumping configuration. In addition, it is desired to demonstrate the versatility of the approach by presenting results which illustrate the capacity of the models and computer programs to accommodate gate discharging as well as gate charging transients, transients under conditions of an applied drain voltage, and transients for MOST's.

Fig. 5.4.4 shows a gate charging transient for device TIX883-1, measured with E= 1.75 volts, R_g =1K Ω, and $R_L \doteq 10k\Omega$. The calculated points shown on the figure were obtained with the 5-lump "L" model (model 5L), and with the 3-lump "L" model (model 3L), described in Chapter

4, using the data summarized in Table 5.3.1. The results from model 5L more closely approach the measured curve than those from model 3L, indicating that model 5L provides a better representation of the switching processes in this device. The only difference between model 5L and model 3L is in the number of lumps (5 and 3 respectively). Thus these results definitely emphasize the importance of using a sufficient number of lumps in a switching model to represent the distributed nature of the device throughout the transient.

Figure 5.4.5 is again a gate charging transient for device TIX883-1 with E= 1.75, and $R_L \doteq 10K\Omega$, but with $R_g = 125\,\Omega$. It is thus a faster transient than that shown in Fig. 5.4.4, and of considerably greater amplitude. Calculated points from each of the models (5L, 3L, 3T, and 1T) discussed in Chapter 4 are shown for comparison. As previously discussed, the data used with models 3L and 5L is summarized in Table 5.3.1, while the data used with models 3T and 1T is summarized in Table 5.3.2. As was the case with Fig. 5.4.4, model 3L again "under-calculates" model 5L at the peak value of the transient, and also , model 1T "under-calculates" model 3T. In this case, both model 5L and model 3T calculate slightly larger values of V_{peak} than actually are measured. The peak value calculated with model 5L could be expected to be somewhat larger if it incorporated stray capacitances, particularly that between gate and drain. The lowest value of V_{peak}, and generally the poorest representation of the transient was obtained with model 3L. The T-lumping configuration compares well with the L-configuration (using a larger number of lumps), and appears to provide a relatively good distribution of the charging currents involved throughout the transient.

The portion of the transient shown in Fig. 5.4.6 was measured on device TIX883-1 with E= 1.75 volts, $R_L \doteq 10K\Omega$, and with $R_g = 35\Omega$. It is intended to be a relatively severe test of the models. It can be seen that considerable rounding of the transient peak results from each of the models 3T, 1T, and 5L shown. As expected, model 1T produces the poorest representation of the transient peak. Some overshoot corresponding to the delayed peak occurs for models 5L and 3T, but they eventually approach the measured curve fairly closely. On the whole, the device representation with models 5L and 3T is adequate in spite of the relatively large transient peak voltage ($\approx$1000 mv).

Figure 5.4.7 shows a gate charging transient for device 2N3824-2 measured with E =4.25 volts, $R_g = 125\Omega$ and $R_L \doteq 10K\Omega$. Since this transient is for a large driving voltage and a relatively low value of R_g, it also is a severe test of the models. It can be seen that the results from model 3T and 1T are quite similar, thus indicating that this device may have a relatively short channel length, and that distributed charging effects may be less important than for device TIX883-1. The transient voltages calculated from model 5L are generally less than those from models 3T and 1T near the transient peak and beyond. This is a device with a relatively low value of gate junction capacitance. Thus the effects of stray capacitances could have a relatively greater effect on the transients for this device, and could account for the difference between the results from model 5L and from model 3T. Also, since this device is switched with a large gate voltage, differences in the ability of the two sets of computer programs to represent the Q_{gg} versus G_{ch} and Q_{gg} versus V_g relationships can be expected to be more severe in this

case than for device TIX883-1. Except for some overshoot on the peak value of the transient, agreement between calculated and measured results is relatively satisfactory.

The transient in Fig. 5.4.8 for TIX881-2 was measured with an applied drain voltage of 1.8 volts through a 10KΩ load resistor. Models 3T and 1T show some over-calculation of the transient peak value , but the interesting aspect of the calculated results shown here, is concerned with the initial and final values of drain voltage. The calculated initial value of the drain voltage is approximately correct for each of the models, being in fact slightly higher than the measured value. The final value of the transient is approximately correct for models 5L and 3T, but too large a value results from model 1T. Thus, model 1T can be seen to be considerably poorer than the multi-lumped models in this regard. These results again demonstrate the importance of the distributed nature of these devices, and show that a model with a sufficient number of lumps can be used to represent the FET under conditions of significant applied drain voltage as discussed in Chapter 2, Section 2.6.

The results in Fig. 5.4.9 are included to emphasize that the basic approach is applicable to MOST's as well as FET's. Caution ,however, must be used in dealing with MOST's , as emphasized by the relatively poor agreement between calculated and measured results. One of the reasons for this is believed to be the fact that for this particular transient, the polarity of the transient voltage itself is negative, which tends to forward bias the P-N junction between the N^+ drain region and the P-type substrate. This may cause some forward conduction to occur in this junction, but it is likely to produce considerable changes

in the depletion layer capacitance associated with this junction , from the value measured at zero drain voltage. Other factors, such as the time dependence of the charge in the surface traps, and distributed capacitance effects between the channel and substrate are also expected to be involved in the transients associated with this device. Thus a more sophisticated form of model than that used here may be required to calculate MOST switching transients more accurately.

A gate discharging transient is shown in Fig. 5.4.10 for device 2N2498-1. The calculated results are in substantial agreement with the measured results, and illustrate the capacity of the models and computer programs to handle this transient as well as the gate charging transients. As noted earlier, the shape of both transients is similar, but the gate discharging transient tends to be lower in amplitude, and shorter in duration. Basically, the reason for this is that the initial rate of discharging tends to be slower because the initial value of channel resistance is at some higher value than for the corresponding gate charging transient. Thus the peak value of the transient tends to be lower. The transient duration tends to be shorter for the gate discharging transient as a result of a progressively decreasing channel resistance, and thus a progressively decreasing transient time constant.

Sample switching transients have been presented in this section covering a wide range of devices and switching conditions. Calculated results from the various models have shown that the adequacy of a given device model depends on the circuit and drive conditions under which it is used. They have also emphasized the need for representing the distributed nature of the device during the switching process, which gen-

erally requires a multi-lump model.

In general, the T-lumping configuration has been found to be superior to the simpler L-configuration. Each T-lump actually "distributes" the channel resistance, and indicates that possibilities exist for using better lumping configurations as a substitute for increasing the number of model lumps.

Differences in calculated results using different model configurations, particularly with a small number of model lumps, are bound to occur. Some of the differences noted in the results presented here are due to the effects of stray capacitances which were not included in model 5L, and also to the inaccuracies associated with measuring and using such small stray capacitances in the T-models. Considering the generality of the approach, and the variety of FET's studied, the charge control methods and the computer programmed techniques of solution have been found to work well in the calculations of the low level switching performance of these devices.

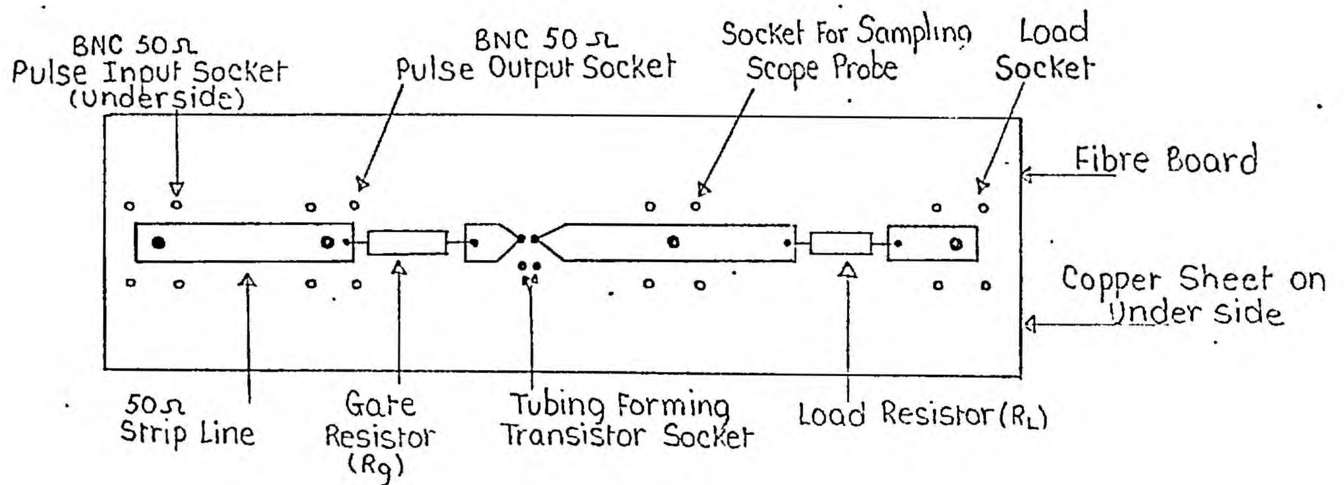


Fig. 5.2.1 : Switching Transient Measurement Jig

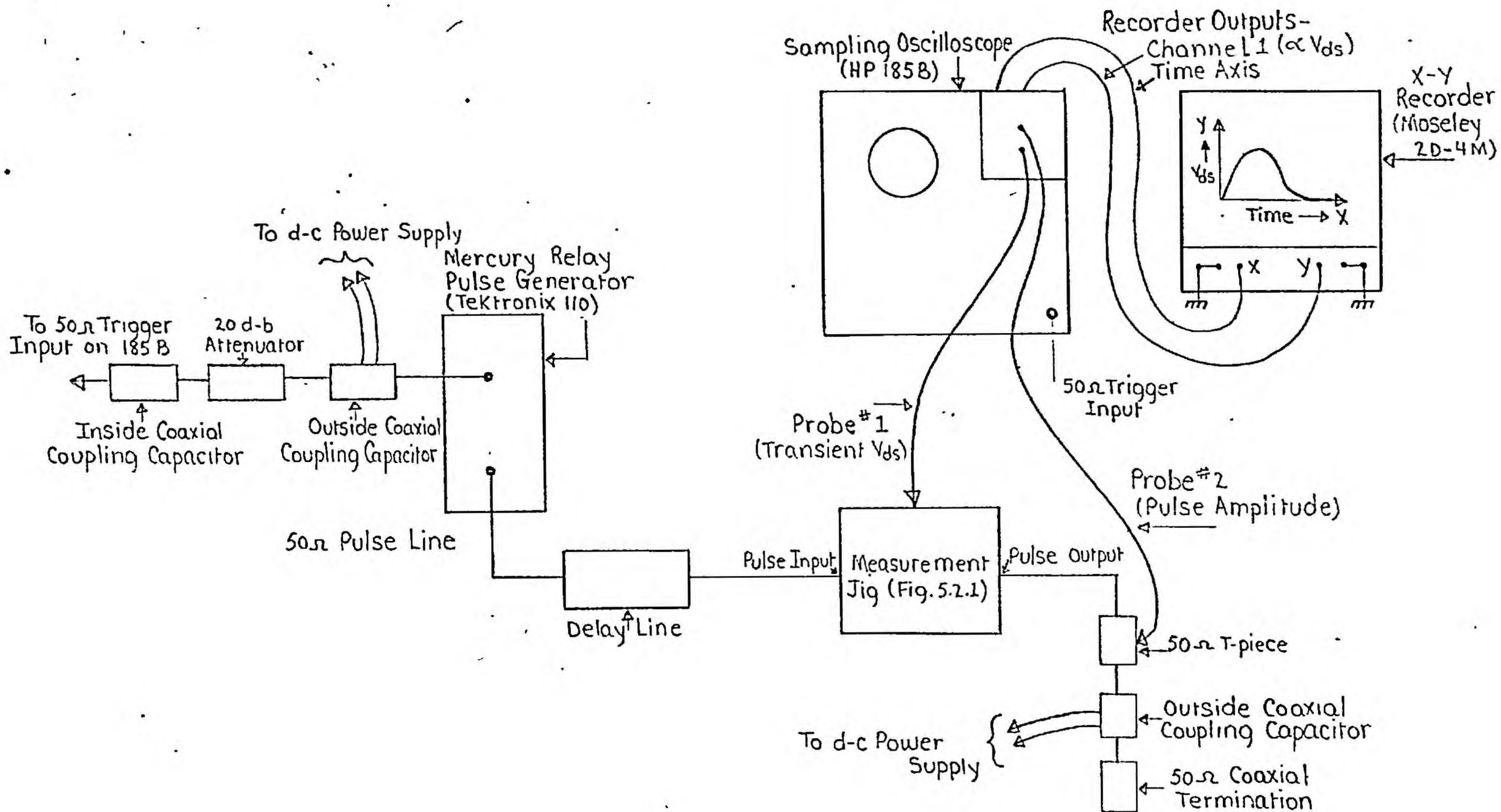


Fig. 5.2.2 : Block Diagram of System for Measuring Switching Transient

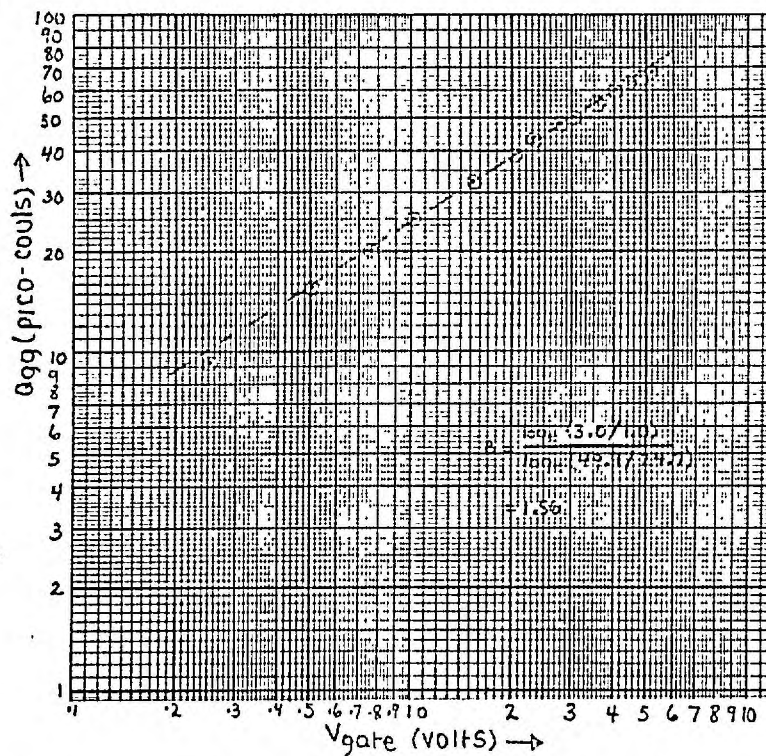


Fig. 5.3.1 : Representation of the Q_{gg} Versus G_{ch} Relationship for Device TIX881-2 for Models 5L and 3L with the Early Computer Programs

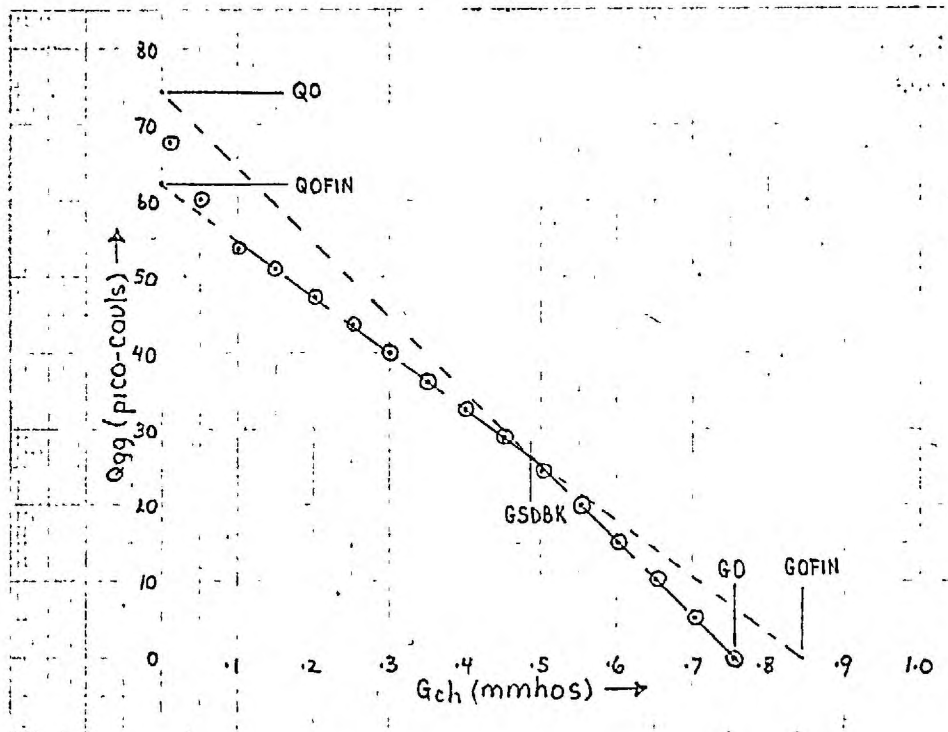


Fig. 5.3.2 : Representation of the Log-Log Q_{gg} Versus V_g Relationship for Device TIX881-2 for Models 5L and 3L with the Early Computer Programs

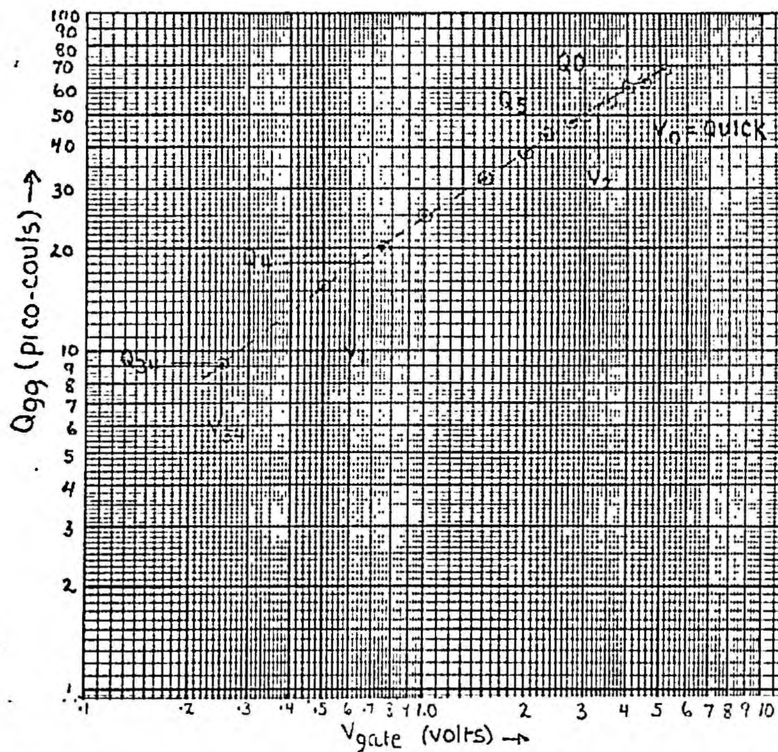


Fig.5.3.3 : Representation of the Q_{gg} Versus G_{ch} Relationship for Device TIX881-2 for Models 3T and 1T with the Second-Generation Computer Programs

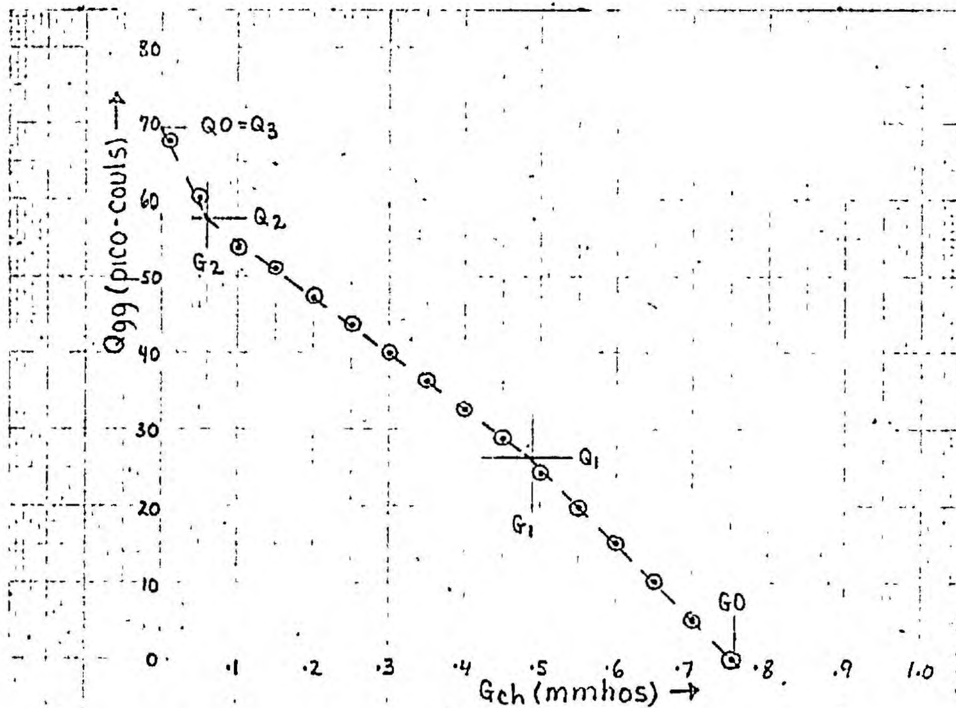


Fig.5.3.4 : Representation of the Log-Log Q_{gg} Versus V_g Relationship for Device TIX881-2 for Models 3T and 1T with the Second-Generation Computer Programs

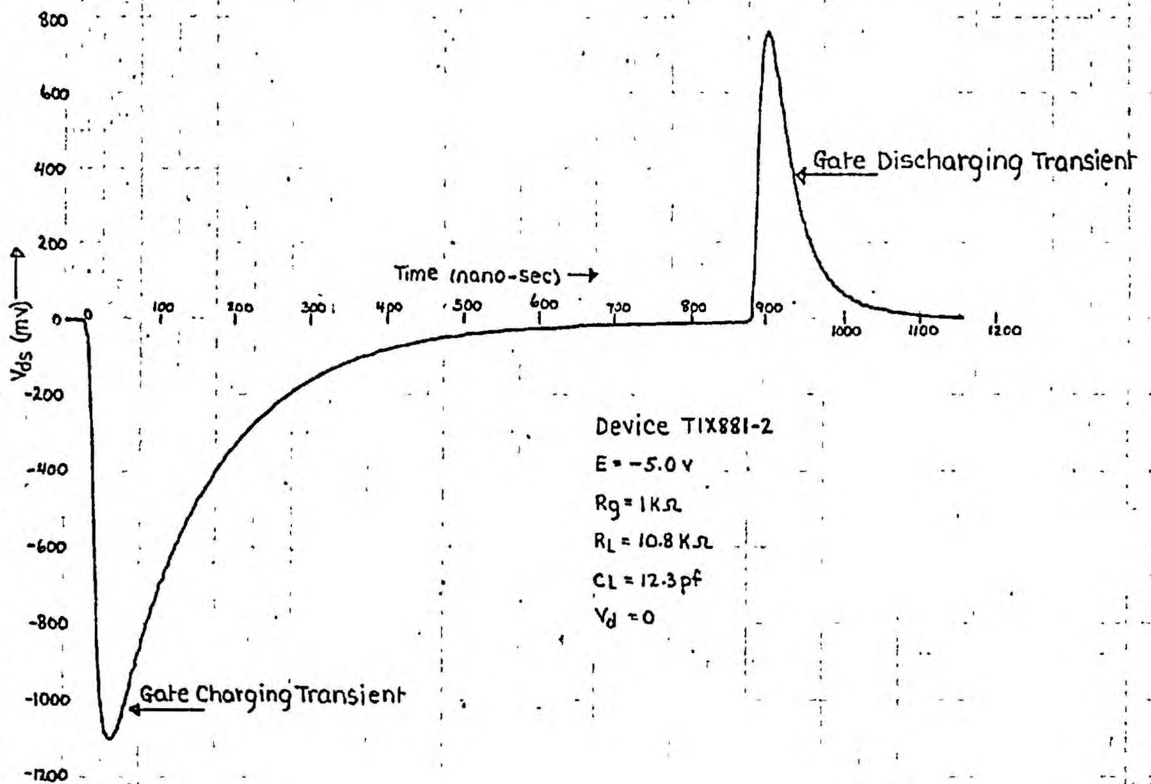


Fig. 5.4.1 : Typical Gate Charging and Discharging Transients

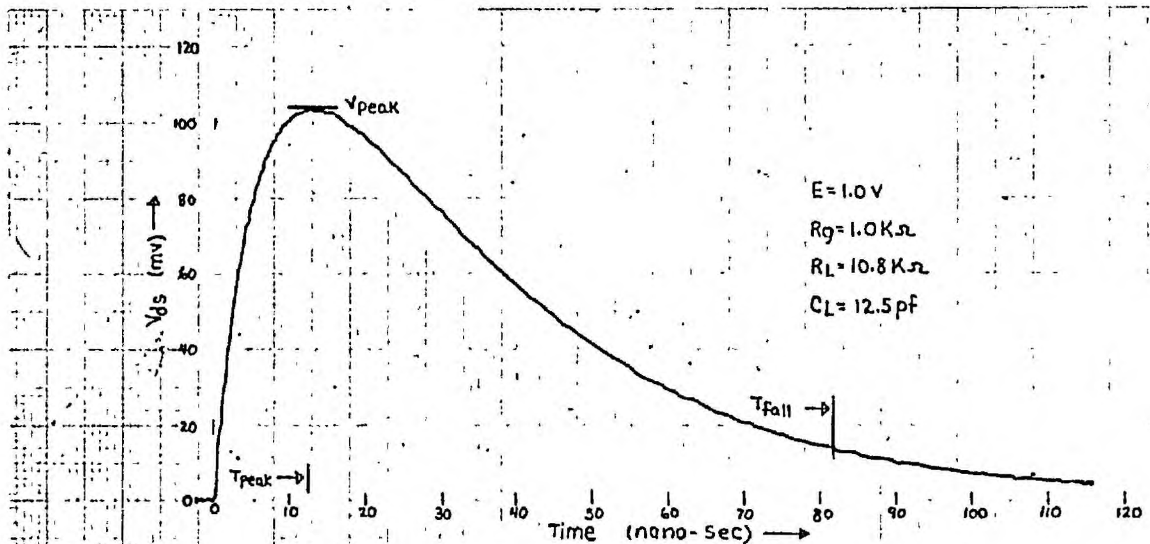


Fig. 5.4.2 : Representative Gate Charging Transient for Device 2N2498-1

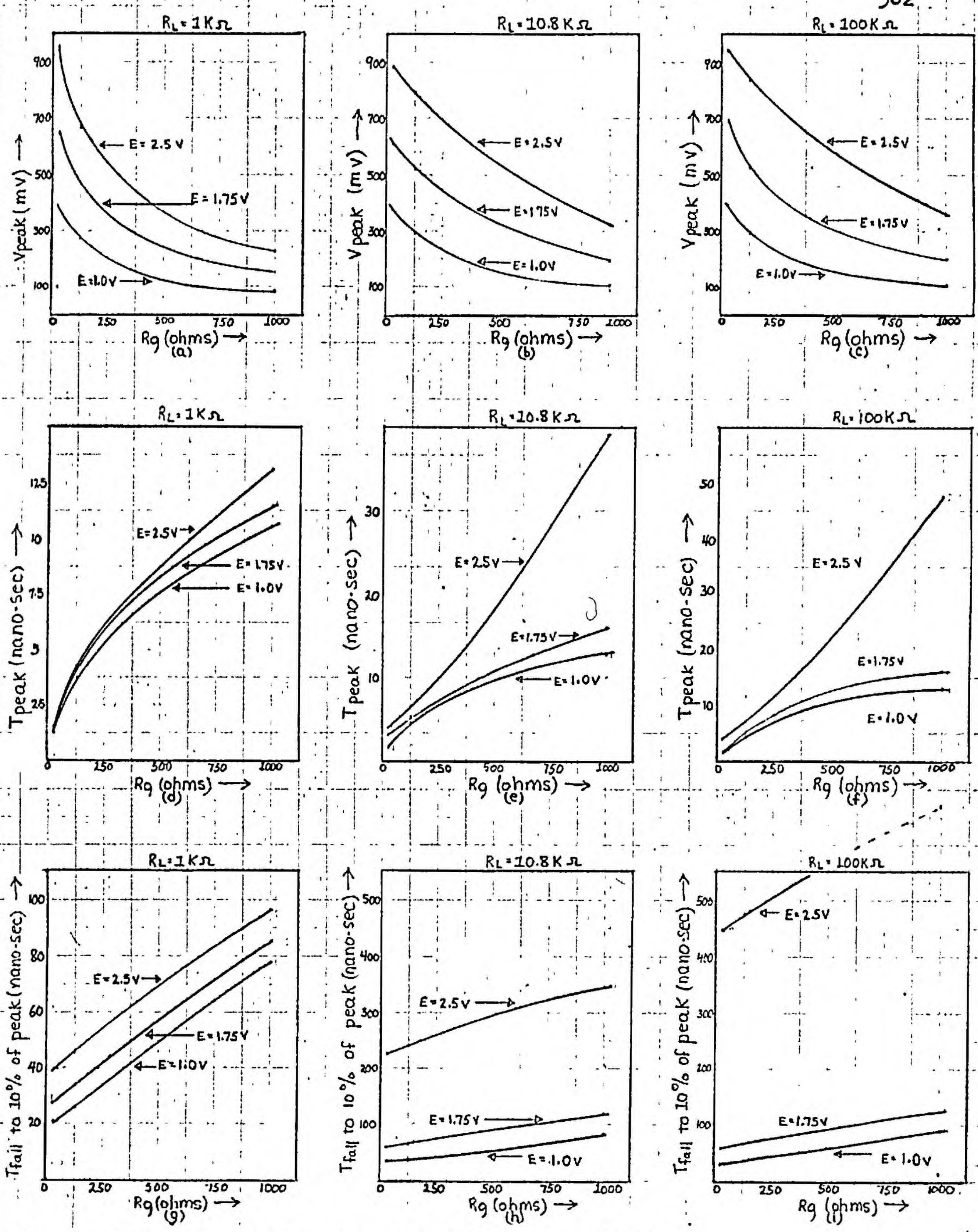


Fig. 5.4.3 : Switching Transient Trend Plots for 2N2498-1

a,b,c - Transient peak voltage for R_L=1.0KΩ,10.8KΩ,and 100KΩ respectively

d,e,f - Time to transient peak for R_L=1.0KΩ,10.8KΩ,and 100KΩ respectively

g,h,i - Fall time to 10% of peak amplitude for R_L =1.0KΩ,10.8KΩ,and 100KΩ respectively

C_L = 12.5 pf ; V_{po} = 3.1 V.

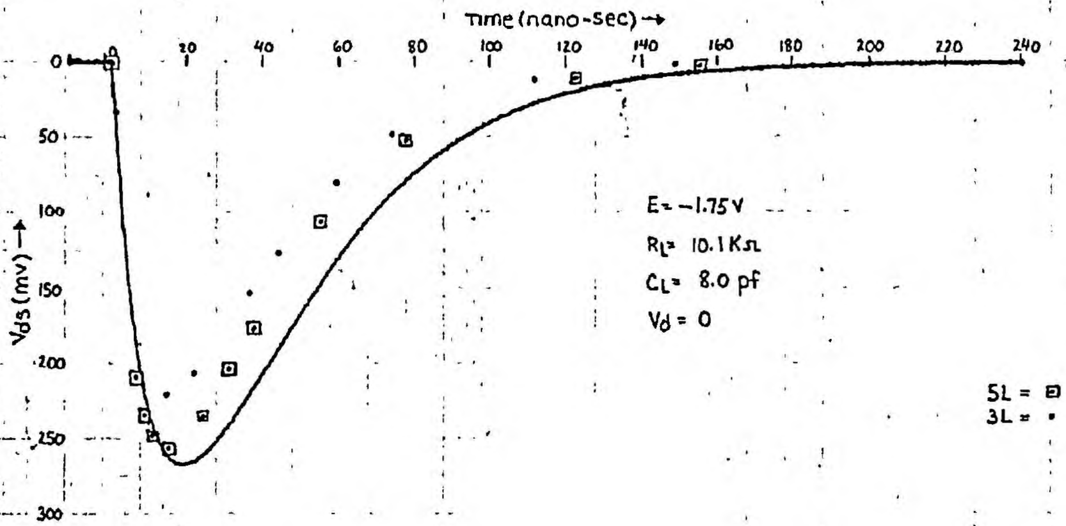


Fig. 5.4.4 : Calculated and Measured Transients for Device TIX883-1 With R_g = 1.0KΩ

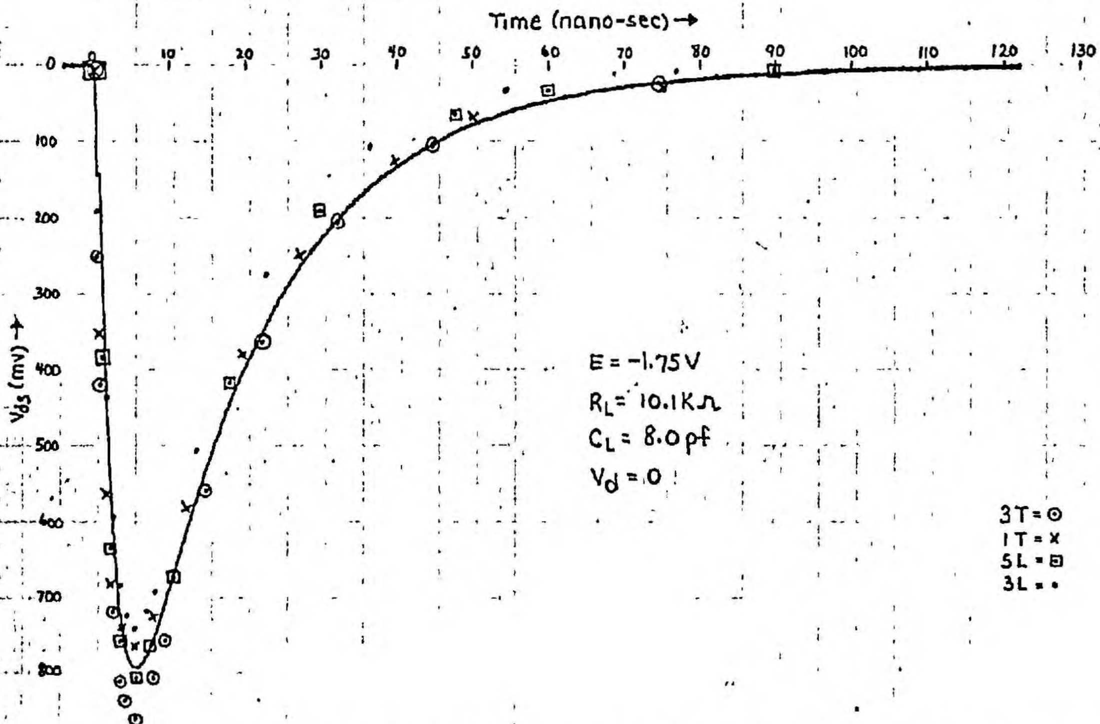


Fig. 5.4.5 : Calculated and Measured Transients for Device TIX883-1 With R_g = 125.5Ω

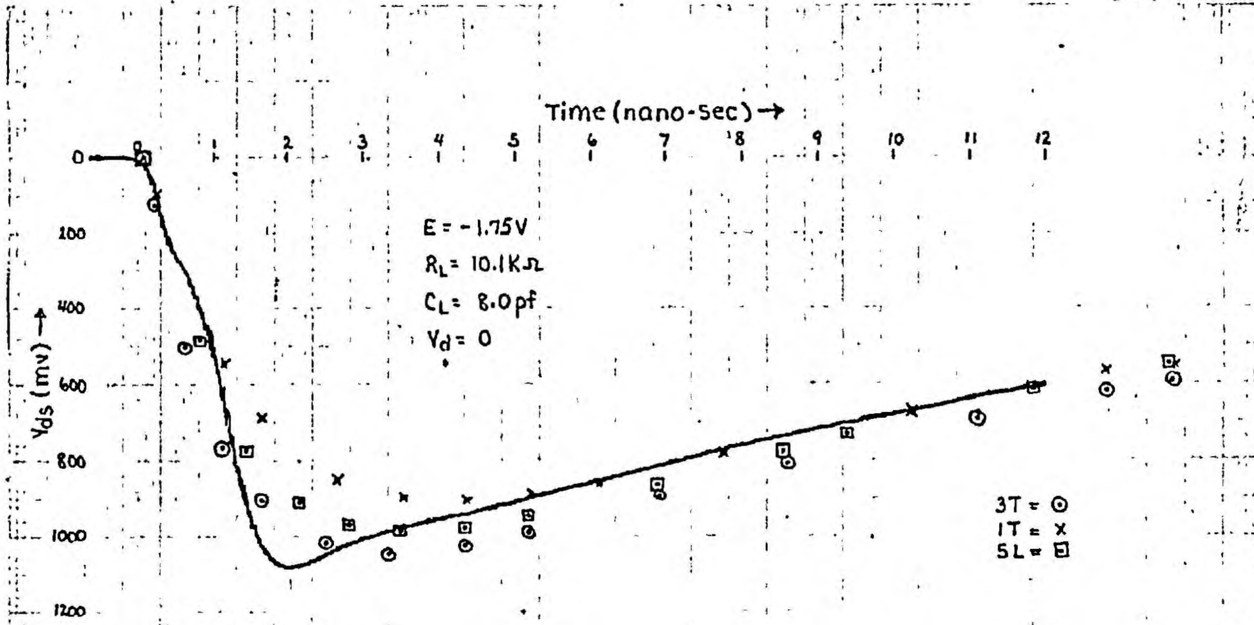


Fig. 5.4.6 : Calculated and Measured Transients for Device TIX883-1 With $R_g = 35.1\,\Omega$

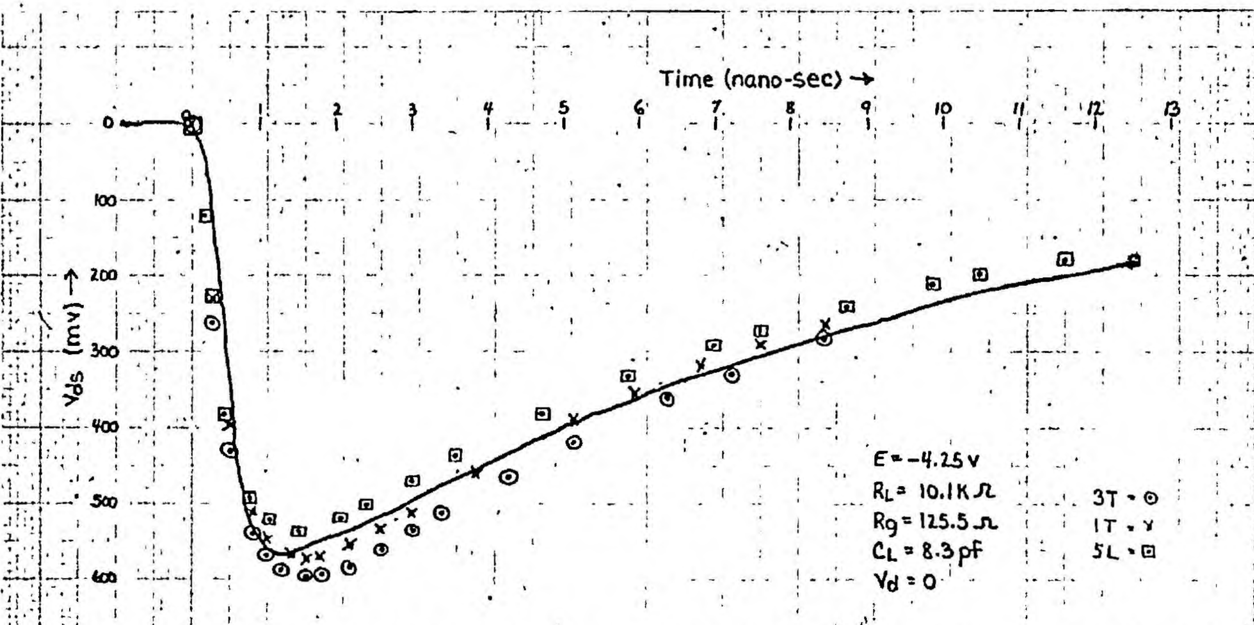


Fig. 5.4.7 : Calculated and Measured Transients for Device 2N3824-2

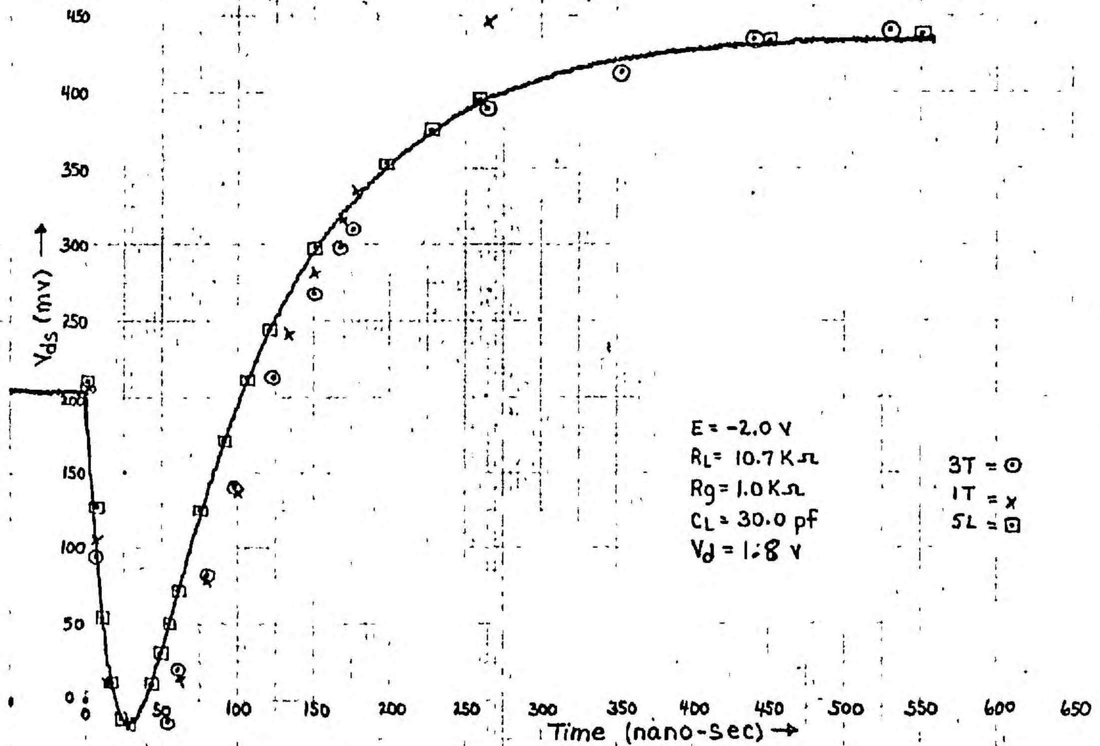


Fig. 5.4.8 : Calculated and Measured Transients for Device TIX881-2 With Applied Drain Voltage

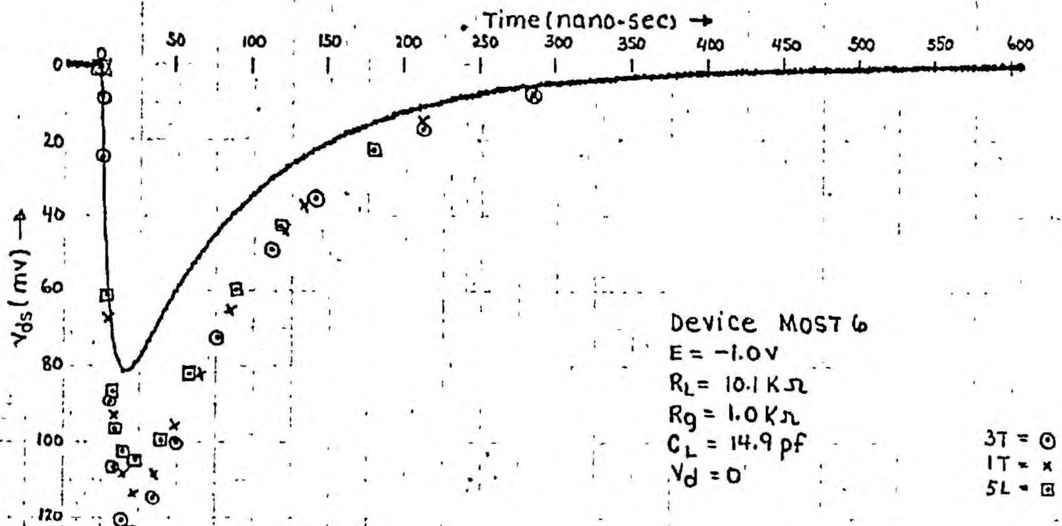


Fig. 5.4.9 : Calculated and Measured Transients for an Insulated Gate Transistor (turn-off)

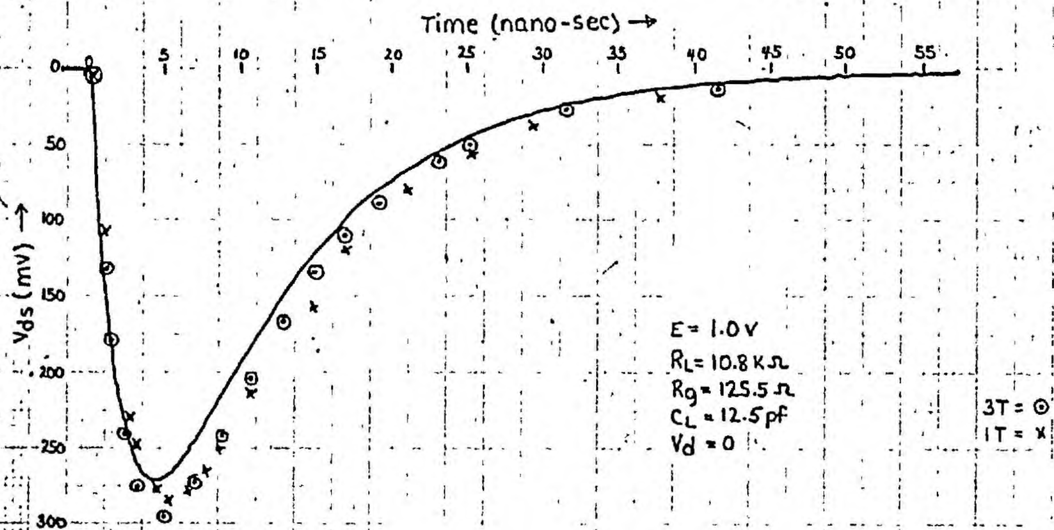


Fig. 5.4.10 : Calculated and Measured Gate Discharging Transient for Device 2N2498-1

CHAPTER 6

CONCLUSIONS

The main objectives of this thesis have been, first, to investigate the usefulness of the charge control approach as a method of studying the steady state behaviour of several types of practical field-effect transistors. Secondly, it was desired to apply the methods, developed in the study of these devices from the charge control point of view, specifically to an investigation of the low level transient switching behaviour of field-effect transistors.

The basic charge control relationships have been derived for both field-effect transistors, and insulated gate transistors. True charge control operation for these devices corresponds to a constant slope (L^2/μ ratio) on the gate charge versus channel conductance relationship, and to a constant slope (τ_d) on the gate charge versus drain current relationship at constant applied drain voltage. In comparisons with Shockley's basic theory, it was concluded that his "gradual case" theory in effect assumed the existence of true charge control operation.

Methods have been developed for measuring the charge control relationships for FET's and MOST's. Charge control relationships have been measured on several types of commercial FET's and MOST's over a wide range of operating conditions. The results of the measurements on the FET's have shown that the basic charge control theory applies over a wide range of values of drain voltage from zero to beyond pinch-off. Saturation in the slope (τ_d) of these relationships occurs with drain voltage, however, and thus the effective channel voltage (V_{ch}) must be

used in the relationships to account for this.

A detailed study of the charge control relationships, including both the regions of constant slope or true charge control operation, and the regions where deviations in the constant slope occur, has been shown to provide a considerable amount of information about device operation. These results indicate that the effective voltage V_{ch} across the channel remains essentially unaffected over a wide range of applied gate voltage. This means that the pinch-off voltage criterion as measured under conditions of zero applied drain voltage does not strictly apply to the FET when drain voltage and drain current are present. It was concluded that the reason for this is the presence of a significant amount of majority carrier charge in the "depleted" region beyond the end of the open channel.

The results of the charge control measurements on MOST's have shown that the true charge control or constant τ_d assumption only applies in the region of operation where the drain end of the channel is not pinched-off. Thus a situation similar to that predicted on the basis of classical theory has been observed for this device in pinch-off. In addition to pinch-off, a second process also occurs in this device in the enhancement mode of operation, which limits the drain current as gate voltage is increased with constant applied drain voltage.

The charge control approach has proved to be useful as a basis for studying the behaviour of various types of commercial field-effect transistors and insulated gate transistors. The approach is general, and does not require the doping density in the gate(s) to be much greater than that existing in the channel. In addition , it can be applied

without special regard to the junction law(s), to the number of gates, to the doping density profile in the channel, to the type of geometry, or to the methods of fabrication. It is also important that the charge control approach reveals by straight line relationships, or by deviations from these straight line relationships, the ranges over which true charge control device operation is valid, or is seriously in error.

The low level switching performance of field-effect transistors has been studied on the basis of the charge control approach. Switching models and computer programs have been developed to enable the transients associated with the switching process to be calculated. The models for a given device are based on the gate charge versus channel conductance relationship measured at zero drain voltage, and also on the corresponding log-log relationship of gate charge versus gate voltage.

Comparisons between calculated and measured transients for a variety of FET's have shown firstly that there is an important interplay between the circuit and the device, and that the effectiveness of a given model for a device depends on the circuit parameters and drive conditions. Secondly, it has been shown that a model must normally account for the distributed nature of these devices in order to represent the switching process adequately. Thus a multi-lump or distributed model is generally required. Similarly, the multi-lump models have also been found to represent the device more correctly in the steady state under conditions of significant external applied drain voltage. Generally, the approach and the methods used in this study have been found to apply well to the calculation of transients for several types of FET's over a wide range of conditions. The main requirement is that a sufficient

number of lumps of a given type be used in the model.

Two main possibilities for future work follow, which were considered to be beyond the scope of the present project. Firstly, a more detailed investigation specifically of lumping configurations could be carried out for the low level switching models. The object would be to determine which of many possible arbitrary forms generally provides the best representation of the FET switching processes with a minimum number of lumps. Various configurations, such as L, T, or π, could be investigated, as well as various combinations of all three. The same techniques used in this thesis would be applicable to such a study. A new subroutine PRIME would be required for each model, and if desired, the second generation programs could easily be extended to accommodate the solution of more equations.

The second possibility is an investigation of the representation of the FET under high level switching conditions, such that the drain voltage may be beyond the saturation value. On the basis of the work in this thesis, it is expected that such an investigation may be extremely involved for practical devices with a large number of parameters to be considered, in addition to the distributed nature of the device. Two possible approaches suggest themselves. One is to use a "succession of steady states" approach based on a terminal charge control model as suggested in Chapter 3, Section 3.6. The other is an attempt to extend the distributed low level switching models, as used in the work here, into the saturation region and beyond. Such an approach would require a considerably more complicated, and perhaps arbitrarily specified model, but the techniques and computer programs used in Chapter 4 would be more directly applicable.

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APPENDIX A

Selected Data from Manufacturers' Specification Sheets

Maximum Ratings at 25° C Free-air Temperature

Parameter	Device Type				
	TIX881	TIX883	2N2498	2N3824	95BFY
V_{dg}(volts)	25(typ. 60)	35(typ. 60)	20	50	35
V_{ds}(volts)	25(typ. 60)	35(typ. 60)	20	50	35
V_{gs}(volts)	25(typ. 60)	35(typ. 60)	20	50	35
I_{gate}(ma)	15	15	10	10	-
Dissipation(mw)	150	150	500	300	300

Electrical Characteristics at 25 C Free-air Temperature

Parameter	Test Conditions	TIX881			TIX883		
		Min.	Typ.	Max.	Min.	Typ.	Max
$I_{D(on)}$ (ma)	V_{ds}=20V ; V_{gs}=0	1.0	1.7	2.5	4.0	6.0	7.5
Drain-Source Resistance (Ω)	I_d=100μa; V_{gs}=0	-	1000	1800	-	500	1200
Small Signal Common-Source Forward Transfer Admittance (μ mhos)	V_{ds}=15v ; f=1Kc/s I_d=1ma for TIX881 I_d=4ma for TIX883	-	0.05	0.5	-	0.05	0.5
Common-Source Short-Circuit Input Capacitance (pf)	V_{gs}=0 ; V_{ds}=20v f= 1mc/s	-	26	-	-	26	-

Electrical Characteristics at 25° C Free-Air Temperature (Cont.)

Parameter	Test Conditions	2N2498	
		Min.	Max.
$I_{D(on)}$ (ma)	V_{ds}= -10; V_{gs}=0	-2	-6
Drain-Source Resistance (Ω)	I_d=-100μa; V_{gs}=0	-	800
Small Signal Common-Source Forward Transfer Admittance(μmhos)	V_{ds}= -10; I_d= -2ma f= 1Kc	1500	3000
Common-Source Short-Circuit Input Capacitance (pf)	V_{gs}= 0 ; V_{ds}= -10v f= 140 Kc/s	-	32

Parameter	Test Conditions	2N3824	
		Min.	Max.
Drain-Source Resistance (Ω)	V_{gs}= 0 ; I_d=0 ; f=1Kc/s	-	250
Common-Source Short-Circuit Input Capacitance (pf)	V_{ds}= 15 v ; V_{gs}= 0 f= 1 mc/s	-	6
Drain Cut off Current (na)	V_{ds}= 15v ; V_{gs}= -8v	-	0.1

Parameter	Test Conditions	95BFY (MOST)		
		Type A	Type B	Type C
Pinch-off Voltage (volts)	V_{ds} = +20 v I_d = 20 μa	-1 to -5	-4 to -8	+1 to +4
Drain Current (ma)	V_{ds}= 20v ; V_{gs}= 0	1.0(typ.)	4.0(typ.)	-
Input Resistance	V_{ds}= 0v ; V_{gs}=±15v	10^{10} ohms (min.) ; 10^{12} ohms (typ.)		
Input Capacitance	V_{ds}= +20 v; I_{ds} = 1ma	4 pf (max.)		
Mutual Conductance	V_{ds}= +20v ; I_{ds}= 3ma	1 ma/volt (min)		

APPENDIX B

Numerical Solution of Differential Equations by the Runge-Kutta Method

The Runge-Kutta method is used in the computer programs as the basis for the numerical solutions of the system of differential equations associated with each of the low level switching models. This method is briefly outlined here as applied to a single differential equation, in order to illustrate the techniques used in the programs.

Consider a first order differential equation of the form

$$\frac{dy}{dt} = y' = f(t,y) \qquad \text{A1}$$

where t_o and y_o are the initial values. It is desired to find the solution to equation A1 at a new value of time (t_1) such that

$$t_1 = t_o + \Delta t \qquad \text{A2a}$$

and

$$y_1 = y_o + \Delta y \qquad \text{A2b}$$

In the Runge-Kutta method (73), this is accomplished by taking a weighted average of four approximate calculated values of the dependent variable. This is a fourth order process, and corresponds to taking the first four terms of the Taylor series solution. Thus, the increment for advancing the dependent variable is given by

$$\Delta y = 1/6 \ (k_1 + 2k_2 + 2k_3 + k_4) \qquad \text{A3}$$

where

$$k_1 = \Delta t \ f(t_o, y_o) \qquad \text{A4a}$$

$$k_2 = \Delta t \ f(t_o + 1/2 \ \Delta t \ , \ y_o + 1/2k_1) \qquad \text{A4b}$$

$$k_3 = \Delta t \ f(t_o + 1/2 \ \Delta t \ , \ y_o + 1/2k_2) \qquad \text{A4c}$$

$$k_4 = \Delta t \; f(t_0 + \Delta t \; , \; y_0 + k_3 \;) \qquad \text{A4d}$$

The increment (Δy) for each subsequent interval is computed by the same formulas with (t_0, y_0) replaced by (t_1, y_1). Thus the value of y for each of several values of t is obtained throughout the range of interest.

The Runge-Kutta method is advantageous in that it requires no special methods to start the solution, and it is easily applicable to the solution of systems of equations. The interval length Δt can be changed at any time during the solution. The accuracy of this method depends on the interval length, and is of the order of $(\Delta t)^5$, but the errors involved are difficult to determine exactly. It is therefore standard practice to check a solution with two or three different interval lengths to establish that a small enough interval length is being used to result in negligible error in the calculated results.

APPENDIX C

Print-out of Statements of Early Computer Program

```
      OVPP(P,U,V,W,X,Y,Z)=FORM* ((1.0-U)*U**B -(2.0-U-P)*P**B+(1.0-P) *
     1  X**B )
      OVUP(P,U,V,W,X,Y,Z)=FORM* ((1.0-Z)*Z**B -(2.0-U-Z)*U**B+( 1.0-U)*
     1  P**B )
       VVP(P,U,V,W,X,Y,Z)=FAT*(W-V) +FAME*VD
      OVWP(P,U,V,W,X,Y,Z)=((1.0-Y)/(RAT*(1.0-Y)+RU))*(      -FATA*(W-V)
     1  +FATB -FATC*Z**B     -FATD *Y**B )
      OVXP(P,U,V,W,X,Y,Z,WPRIME)=FORM*((1.0-P)*P**B -(2.0-X-P)*X**B +
     1  (1.0-X)*Y**B )
       VYP(P,U,V,W,X,Y,Z,WPRIME)= FORM*(1.0-X)*(X**B-Y**B)+WPRIME
      OVZP(P,U,V,W,X,Y,Z,WPRIME)= RISK*WPRIME +FATE -(F    +FORM*(1.0-Z))
     1 *Z**B +FORM*(1.0-Z)*U**B
      OVFCH(P,U,V,W,X,Y,Z )=RU*(1.0/(1.0-(Y      ))+1.0/(1.0-X      )
     1 +1.0/(1.0-(P      ))+1.0/(1.0-(U      ))+1.0/(1.0-(Z      )))
       TI=0.0
   10 DIMENSION FET(2)
   20 READ(5,25)FET,QO,QOFIN,DK,DKFIN,RO,ROFIN,I,J
   25 FORMAT(2A5,6E10.3,1X,I1,I1)
      K=0
      IF(I.EQ.1)STOP
     OREAD(5,26)B,BFIN,RPS,RPD,E,VD,RG,NMULT2,RL,CL,F,TF,NTNCH,NMULT,NDT
     1  ,GSDBK
   26 FORMAT(7E10.3,I10/4E10.3,3I10,E10.3)
      NTNCH2=NTNCH+NTNCH*J/5
      IF(J.EQ.0)NMULT2=1
      B1=1.0/B
      GSDOLD=100.0
      WRITE(6,28)
   28 FORMAT(1H1,23H CHARGING GATE CIRCUIT )
  710 QUICK= DK
      QU=QO/5.0
      RU=RO/5.0
      R=RG+RPS
      RAT=RPS+RPD-RPS**2/R
      RISK=RPS/R-1.0
      FORM = R*F/RU
      FAT=R*F*QU/(QUICK*RL*CL)
      FAME=R*F/(QUICK*RL)
      FATA=QU*R*F/(CL*QUICK)
      FATB=F*RPS*E/QUICK
      FATC=RISK*R*F
      FATD=R*F
      FATE = F*E/QUICK
      GO TO 890
   30 PPI=VPP(PI,UI,VI,WI,XI,YI,ZI)
```

```
      UPI=VUP(PI,UI,VI,WI,XI,YI,ZI)
      VPI=VVP(PI,UI,VI,WI,XI,YI,ZI)
      WPI=VWP(PI,UI,VI,WI,XI,YI,ZI)
      XPI=VXP(PI,UI,VI,WI,XI,YI,ZI,WPI)
      YPI=VYP(PI,UI,VI,WI,XI,YI,ZI,WPI)
      ZPI=VZP(PI,UI,VI,WI,XI,YI,ZI,WPI)
   40 DT=FLOAT(NDT)/1000.0
      NTI=TI*1000.0
      RCHO= VFCH(PI,UI,VI,WI,XI,YI,ZI)
 7300WRITE(6,61)FET,WI,XI,YI,ZI,WPI,XPI,YPI,ZPI,TI,TF,DT,QO,DK,E,RO,RL
     1,RPS,    RG,QUICK,RPD,RCHO
  610FORMAT(1HO, 6HFET - ,2A5,2X,3HWI=,F6.3,2X,3HXI=,F6.3,2X,3HYI=,F6.3
     1,2X,3HZI=,F6.3,2X,4HWPI=,F14.9,2X,4HXPI=,F14.9,2X,4HYPI=,F14.9/1H
     2,4HZPI=,F14.9,5X,3HTI=,F6.3,5X,3HTF=,E14.4,5X,3HDT=,E14.4,5X,
     3 3HQO=,E14.4,5X,3HDK=,E14.4/1H ,2HE=,E14.4,5X,3HRO=,E14.4,5X,
     4 3HRL=,E14.4,5X,4HRPS=,E14.4,5X,3HRG=,E14.4/1H , 6HQUICK=,E14.4,
     5 5X,4HRPD=,E14.4,5X,5HRCHO=,E14.4)
      WRITE(6,930)L2,VAO,VBO,VCO,VLO,VD,BFIN,CL ,VDO,VEO
 9300FORMAT(1H , 3HL2=,I4,   5X, 4HVAO=,E14.4,5X, 4HVBO=,E14.4,5X,
     1   4HVCO=,E14.4,5X, 4HVLO=,E14.4,5X,4HVDS=,E14.4/1H ,2X,5HBFIN=,
     2  E14.4,5X,3HCL=,E14.4,5X,4HVDO=,E14.4,5X,4HVEO=,E14.4)
      WRITE(6,55)QOFIN,DKFIN,ROFIN,B,NMULT2,F,NTNCH,NMULT,GSDBK,NTNCH2
  550FORMAT(1H ,5HQOFIN,E14.4,5X,6HDKFIN=,E14.4,5X,6HROFIN=,E14.4,5X,
     1 2HB=,E14.4,5X,7HNMULT2=,I10  /1H ,2HF=,E14.4,5X,6HNTNCH=,I10,5X,
     2 6HNMULT=,I10,5X,6HGSDBK=,E14.4,5X,7HNTNCH2=,I10)
   50 PO=PI
      UO=UI
      VO=VI
      WO=WI
      XO=XI
      YO=YI
      ZO=ZI
      NTO=NTI
      PPO=PPI
      UPO=UPI
      VPO=VPI
      WPO=WPI
      XPO=XPI
      YPO=YPI
      ZPO=ZPI
      NB=200
      WRITE(6,62)
  620FORMAT(1HO,129HT(NORM)        W          WPRIMED          X          XPRIMED
     1          Y            YPRIMED          Z            ZPRIMED    RCH(K)    VDS(M
     2V)  T(N-SEC) )
   70 NTN1=NTO
      PN1=PO
      UN1=UO
      VN1=VO
      WN1=WO
      XN1=XO
```

```
YN1=YO
ZN1=ZO
PPN1=PPO
UPN1=UPO
VPN1=VPO
WPN1=WPO
XPN1=XPO
YPN1=YPO
ZPN1=ZPO
PN2=PN1+PPN1*(DT/2.0)
XN2=XN1+XPN1*(DT/2.0)
VN2=VN1+VPN1*(DT/2.0)
WN2=WN1+WPN1*(DT/2.0)
UN2=UN1+UPN1*(DT/2.0)
YN2=YN1+YPN1*(DT/2.0)
ZN2=ZN1+ZPN1*(DT/2.0)
PPN2=VPP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2)
UPN2=VUP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2)
VPN2=VVP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2)
WPN2=VWP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2)
XPN2=VXP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2,WPN2)
YPN2=VYP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2,WPN2)
ZPN2=VZP(PN2,UN2,VN2,WN2,XN2,YN2,ZN2,WPN2)
PN3=PN1+PPN2*(DT/2.0)
XN3=XN1+XPN2*(DT/2.0)
VN3=VN1+VPN2*(DT/2.0)
WN3=WN1+WPN2*(DT/2.0)
UN3=UN1+UPN2*(DT/2.0)
YN3=YN1+YPN2*(DT/2.0)
ZN3=ZN1+ZPN2*(DT/2.0)
PPN3=VPP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3)
UPN3=VUP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3)
VPN3=VVP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3)
YPN3=VYP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3,WPN3)
ZPN3=VZP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3,WPN3)
PN4=PN1+PPN3*DT
XN4=XN1+XPN3*DT
VN4=VN1+VPN3*DT
WN4=WN1+WPN3*DT
UN4=UN1+UPN3*DT
YN4=YN1+YPN3*DT
ZN4=ZN1+ZPN3*DT
PPN4=VPP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4)
UPN4=VUP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4)
VPN4=VVP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4)
WPN4=VWP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4)
XPN4=VXP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4,WPN4)
YPN4=VYP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4,WPN4)
ZPN4=VZP(PN4,UN4,VN4,WN4,XN4,YN4,ZN4,WPN4)
DP=(DT/6.0)*(PPN1+2.0*PPN2+2.0*PPN3+PPN4)
DX  = (DT/6.0)*(XPN1+2.0*XPN2+2.0*XPN3+XPN4)
```

```
      DV=(DT/6.0)*(VPN1+2.0*VPN2+2.0*VPN3+VPN4)
      DW=(DT/6.0)*(WPN1+2.0*WPN2+2.0*WPN3+WPN4)
      DU=(DT/6.0)*(UPN1+2.0*UPN2+2.0*UPN3+UPN4)
      DY  = (DT/6.0)*(YPN1+2.0*YPN2+2.0*YPN3+YPN4 )
      DZ=(DT/6.0)*(ZPN1+2.0*ZPN2+2.0*ZPN3+ZPN4)
      NTN=NTN1+NDT
      TN=FLOAT(NTN)/1000.0
      PN=PN1+DP
      XN=XN1+DX
      VN=VN1+DV
      WN=WN1+DW
      UN=UN1+DU
      YN=YN1+DY
      ZN=ZN1+DZ
      PPN=VPP(PN,UN,VN,WN,XN,YN,ZN)
      UPN=VUP(PN,UN,VN,WN,XN,YN,ZN)
      VPN=VVP(PN,UN,VN,WN,XN,YN,ZN)
      WPN=VWP(PN,UN,VN,WN,XN,YN,ZN)
      XPN=VXP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      YPN=VYP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      ZPN=VZP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      IF(NTN.EQ.NTNCH) GO TO 970
      IF(NTN.EQ.NTNCH2) GO TO 980
  200 IF(NTN.LE.100)GO TO 85
      IF((NTN-NB).NE.0)GO TO 90
      NB=NB+200
      IF(NTN.GE.1000)NB=NB+800
      IF(NTN.GE.20000)NB=NB+4000
      IF(NTN.GE.100000)NB=NB+45000
   85 RCH=VFCH(PN,UN,VN,WN,XN,YN,ZN)/1000.0
      VDS=1000.0*(RL*QUICK*VPN/(R*F)-VD)
      TREAL=TN*R*QU*1000000000.0/QUICK *F
      WRITE(6,87)TN,WN,WPN,XN,XPN,YN,YPN,ZN,ZPN,RCH,VDS,TREAL
   87 FORMAT(1H ,F6.2,8F12.8,3F9.3)
   90 IF(TN.GT.TF)GO TO 120
      GSDNEW=1.0/VFCH(PN,UN,VN,WN,XN,YN,ZN)
      IF((GSDOLD-GSDBK).GT.0.0.AND.(GSDNEW-GSDBK).LE.0.0) GO TO 950
      IF((GSDOLD-GSDBK).LT.0.0.AND.(GSDNEW-GSDBK).GE.0.0) GO TO 960
  700 GSDOLD=GSDNEW
  100 NTO=NTN
      PO=PN
      XO=XN
      VO=VN
      WO=WN
      UO=UN
      YO=YN
      ZO=ZN
      PPO=PPN
      XPO=XPN
      VPO=VPN
      WPO=WPN
```

```
      UPO=UPN
      YPO=YPN
      ZPO=ZPN
  110 GO TO 70
  120 IF(J.NE.1)GO TO 20
      GSDOLD=0.0
      NDT=NDTST
      K=K+1
      IF(K.GT.1)GO TO 20
      WI=WN
      VI=VN
      PI=PN
      XI=XN
      UI=UN
      YI=YN
      ZI=ZN
      RA=RU/(1.0-(YI        ))
      RB=RU/(1.0-(XI        ))
      RC=RU/(1.0-(PI        ))
      RD=RU/(1.0-(UI        ))
      RE=RU/(1.0-(ZI        ))
      RIO=VD/(RA+RB+RC+RD+RE+RPS+RPD+RL)
      VEO=RIO*RPS+E
      VDO=VEO+RIO*RE
      VCO=VDO+RIO*RD
      VBO=VCO+RIO*RC
      VAO=VBO+RIO*RB
      VLO=RIO*RL-VD
      E=0.0
      FATB=F*RPS*E/QUICK
      FATE = F*E/QUICK
      WRITE(6,130)
  130 FORMAT(1H1,30H  DISCHARGING GATE CIRCUIT     )
      GO TO 30
  890 RIO=VD/(RO+RPS+RPD+RL)
      VEO=RIO*RPS
      VDO=VEO+RIO*RU
      VCO=VDO+RIO*RU
      VBO=VCO+RIO*RU
      VAO=VBO+RIO*RU
      VLO=-RIO*(RPS+RPD+ RO)
      HLEVEL=0.1
      L2=0
      ERROR=0.005
      VCOO=0.0
      VEOO=0.0
      VBOO=0.0
      VDOO=0.0
      VAOO=0.0
      VLOO=0.0
      VI=0.0
```

```
  920 PI=(VCO/QUICK)**B1
      WI=VLO*CL/QU
      UI=(VDO/QUICK)**B1
      XI=(VBO/QUICK)**B1
      YI=(VAO/QUICK)**B1
      ZI=(VEO/QUICK)**B1
      IF(ABS(VD).LE.HLEVEL)GO TO 30
     0IF(ABS((VCO-VCOO)/VCO).LE.ERROR.AND.ABS((VBO-VBOO)/VBO).LE.ERROR
     1 .AND.ABS((VAO-VAOO)/VAO).LE.ERROR.AND.ABS((VLO-VLOO)/VLO).LE.
     2 ERROR.AND.ABS((VDO-VDOO)/VDO).LE.ERROR.AND.ABS((VEO-VEOO)/VEO)
     3 .LE.ERROR)GO TO 30
      L2=L2+1
      VCOO=VCO
      VDOO=VDO
      VBOO=VBO
      VEOO=VEO
      VAOO=VAO
      VLOO=VLO
      RIO=VD/(VFCH(PI,UI,VI,WI,XI,YI,ZI) +RPS+RPD+RL)
      VEO=RIO*RPS
      VDO=VEO+RIO*RU/(1.0-(ZI      ))
      VCO=VDO+RIO*RU/(1.0-(UI      ))
      VBO=VCO+RIO*RU/(1.0-(PI      ))
      VAO=VBO+RIO*RU/(1.0-(XI      ))
      VLO=RIO*RL-VD
      GO TO 920
  950 BST=B
      ALPHA=QU/QUICK
      DKST=DK
      QOST=QO
      ROST=RO
      B=BFIN
      B1=1.0/B
      QUICK= DKFIN
      QU=QOFIN/5.0
      RU=ROFIN/5.0
      RENORM=QOST/(QU*5.0)
  990 PN=PN*RENORM
      UN=UN*RENORM
      VN=VN*RENORM
      WN=WN*RENORM
      XN=XN*RENORM
      YN=YN*RENORM
      ZN=ZN*RENORM
      FORM = R*F/RU
      FAT=R*F*QU/(QUICK*RL*CL)
      FAME=R*F/(QUICK*RL)
      FATA=QU*R*F/(CL*QUICK)
      FATB=F*RPS*E/QUICK
      FATC=RISK*R*F
      FATD=R*F
```

```
      FATE = F*E/QUICK
      PPN=VPP(PN,UN,VN,WN,XN,YN,ZN)
      UPN=VUP(PN,UN,VN,WN,XN,YN,ZN)
      VPN=VVP(PN,UN,VN,WN,XN,YN,ZN)
      WPN=VWP(PN,UN,VN,WN,XN,YN,ZN)
      XPN=VXP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      YPN=VYP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      ZPN=VZP(PN,UN,VN,WN,XN,YN,ZN,WPN)
      NTNF=FLOAT(NTN)*ALPHA*QUICK/QU
      L3=NTNF/NDT
      NTNA=L3*NDT
      NTNB=NTNA+NDT
      IF(ABS(NTNF-NTNA).LE.ABS(NTNF-NTNB))NTN=NTNA
      WPN3=VWP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3)
      XPN3=VXP(PN3,UN3,VN3,WN3,XN3,YN3,ZN3,WPN3)
      IF(ABS(NTNF-NTNB).LT.ABS(NTNF-NTNA))NTN=NTNB
  995 JUDGE=NB-NTN
      IF(JUDGE.GT.0) GO TO 700
      IF(NTN.LT.100) GO TO 700
      NB=NB+200
      IF(NTN.GE.1000) NB=NB+800
      IF(NTN.GE.20000)NB=NB+4000
      IF(NTN.GE.100000) NB=NB+45000
      GO TO 995
  960 B=BST
      ALPHA=QU/QUICK
      B1=1.0/B
      QUICK= DK
      QU=QOST/5.0
      RU=ROST/5.0
      RENORM=QOFIN/(QU*5.0)
      GO TO 990
  970 NDTST=NDT
      NDT=NDT*NMULT
      DT=FLOAT(NDT)/1000.0
      GO TO 200
  980 NDT=NDT*NMULT2
      DT=FLOAT(NDT)/1000.0
       GO TO 200
      END
```

APPENDIX D

Print-out of Statements of Second-Generation Computer Programs

```
 10 DIMENSION FET(2)
    COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
   0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
   1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
   0COMMON /THREE/LUMP,Q0,Q1,Q2,Q3,Q4,Q5,G0,G1,G2,G3,QUICK,V2,V1,V34,
   1Q34
   0COMMON/FOUR/RPS,RPD,RO,RAA,RBB,RCC,RDD,QU,R,RAT,RISK,ROT,RUT,ROPE
   1,RUN,FORM,F,SIXX,I,L2,NOW,NEXT,ERROR,EDOWN,VAO,VBO,VCO,VEO,VFO,
   2 VLO,VD,RL,E,RG,CL,CGS,CGD,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10
    TI=0.0
 20 READ(5,25)FET,QUICK,G0,Q0,RPS,RPD,VD,I,LUMP,LDISCH
 25 FORMAT(2A5,6E10.3,1X,3I1)
    K=0
    IF(I.EQ.1)STOP
   0READ(5,26)G1,G2,G3,V34,V1,V2,Q1,Q2,
   1  Q3,Q34,Q4,Q5,E,RG,RL,CL,
   2  CGS,CGD,F,TF, NTNCH  , NTNCH2  ,NDT ,NDT1 , NDT2
 26 FORMAT( 8E10.3/ 8E10.3 / 4E10.3 ,2I10, 3I5 )
    IF(LDISCH.EQ.1)GO TO 35
    WRITE(6,28)
    EDOWN=0.0
 28 FORMAT(1H1,23H CHARGING GATE CIRCUIT )
    GO TO 710
 35 WRITE(6,29)
 29 FORMAT(1H1, 24HDISCHARGING GATE CIRCUIT )
    EDOWN=E
710 RO=1.0/G0
    QU=Q0/FLOAT(LUMP)
    CALL INITIL
    CALL SET (PI,UI,VI,WI,XI,YI,ZI)
 30 CALL PRIME (PPI,UPI,VPI,WPI,XPI,YPI,ZPI,PI,UI,VI,WI,XI,YI,ZI)
 40 DT=FLOAT(NDT)/1000.0
    NTI=TI*1000.0
    RCHO=RAA+RBB+RCC+RDD -RPS-RPD
7300WRITE(6,61)FET,PI,XI,YI,ZI,PPI,XPI,YPI,ZPI,TI,TF,DT,Q0,DK,E,RO,RL
   1,RPS,    RG,QUICK,RPD,RCHO
 610FORMAT(1H0, 6HFET - ,2A5,2X,3HPI=,F6.3,2X,3HXI=,F6.3,2X,3HYI=,F6.3
   1,2X,3HZI=,F6.3,2X,4HPPI=,F14.9,2X,4HXPI=,F14.9,2X,4HYPI=,F14.9/1H
   2,4HZPI=,F14.9,5X,3HTI=,F6.3,5X,3HTF=,E14.4,5X,3HDT=,E14.4,5X,
   3 3HQ0=,E14.4,5X,3HDK=,E14.4/1H ,2HE=,E14.4,5X,3HRO=,E14.4,5X,
   4 3HRL=,E14.4,5X,4HRPS=,E14.4,5X,3HRG=,E14.4/1H , 6HQUICK=,E14.4,
   5 5X,4HRPD=,E14.4,5X,5HRCHO=,E14.4)
   0WRITE(6,930)L2,VAO,VBO,VCO,VLO,VD,CL,F,LUMP,TF,NDT,NDT1,NDT2,
   1 NTNCH,NTNCH2
9300FORMAT(1H ,3HL2=,I4,3X, 4HVAO=,E14.4,3X,4HVBO=,E14.4,3X, 4HVCO=,
```

```
     1  E14.4,3X, 4HVLO=,E14.4,5X, 4HVDS=,E14.4/1H ,2X, 3HCL=,E14.4,2X,
     2  2HF=,E14.4,3X, 6HLUMPS=,I5,3X, 3HTF=,E14.4,3X, 4HNDT=,I5,3X,
     3  5HNDT1=,I5,5X, 5HNDT2=,I5,5X/1H , 6HNTNCH=,I10,5X, 7HNTNCH2=,
     4  I10,5X  )
      WRITE(6,931)S1,S2,S3,S4,B1,B2,B3,F1,F2,F3,BK1,BK2,BK3
  9310FORMAT(1H , 3HS1=,E9.3,5X, 3HS2=,E9.3,5X, 3HS3=,E9.3,5X,3HS4=,
     1 E9.3,5X,3HB1=,E9.3,5X,  3HB2=,E9.3,5X, 3HB3=,E9.3,5X  /1H ,
     2 3HF1=,E9.3,5X, 3HF2=,E9.3,5X,3HF3=,E9.3,5X, 4HBK1=,E9.3,5X,
     3 4HBK2=,E9.3,5X, 4HBK3=,E9.3,5X )
      WRITE(6,932) D1,D2,D3,D4,DX,DY,DZ
932   FORMAT(1H , 7E15.4)
C INITIALIZATION FOR CALCULATIONS AT START OF T LOOP
   50 PO=PI
      UO=UI
      XO=XI
      YO=YI
      ZO=ZI
      NTO=NTI
      PPO=PPI
      UPO=UPI
      XPO=XPI
      YPO=YPI
      ZPO=ZPI
      NB=200
      WRITE(6,62)
   620FORMAT(1H0,129HT(NORM)      P        PPRIMED          X          XPRIMEI
     1          Y            YPRIMED            Z          ZPRIMED   RCH(K)   VDS(M
     2V)  T(N-SEC) )
   70 NTN1=NTO
      PN1=PO
      UN1=UO
      XN1=XO
      YN1=YO
      ZN1=ZO
      PPN1=PPO
      UPN1=UPO
      XPN1=XPO
      YPN1=YPO
      ZPN1=ZPO
      PN2=PN1+PPN1*(DT/2.0)
      XN2=XN1+XPN1*(DT/2.0)
      UN2=UN1+UPN1*(DT/2.0)
      YN2=YN1+YPN1*(DT/2.0)
      ZN2=ZN1+ZPN1*(DT/2.0)
     0CALL PRIME (PPN2,UPN2,VPN2,WPN2,XPN2,YPN2,ZPN2,PN2,UN2,VN2,WN2,
     1   XN2,YN2,ZN2)
      PN3=PN1+PPN2*(DT/2.0)
      XN3=XN1+XPN2*(DT/2.0)
      UN3=UN1+UPN2*(DT/2.0)
      YN3=YN1+YPN2*(DT/2.0)
      ZN3=ZN1+ZPN2*(DT/2.0)
```

```
     OCALL PRIME (PPN3,UPN3,VPN3,WPN3,XPN3,YPN3,ZPN3,PN3,UN3,VN3,WN3,
     1    XN3,YN3,ZN3)
      PN4=PN1+PPN3*DT
      XN4=XN1+XPN3*DT
      UN4=UN1+UPN3*DT
      YN4=YN1+YPN3*DT
      ZN4=ZN1+ZPN3*DT
     OCALL PRIME (PPN4,UPN4,VPN4,WPN4,XPN4,YPN4,ZPN4,PN4,UN4,VN4,WN4,
     1    XN4,YN4,ZN4)
      PD=(DT/6.0)*(PPN1+2.0*PPN2+2.0*PPN3+PPN4)
      XD  = (DT/6.0)*(XPN1+2.0*XPN2+2.0*XPN3+XPN4)
      UD=(DT/6.0)*(UPN1+2.0*UPN2+2.0*UPN3+UPN4)
      YD  = (DT/6.0)*(YPN1+2.0*YPN2+2.0*YPN3+YPN4 )
      ZD=(DT/6.0)*(ZPN1+2.0*ZPN2+2.0*ZPN3+ZPN4)
      NTN=NTN1+NDT
      TN=FLOAT(NTN)/1000.0
      PN=PN1+PD
      XN=XN1+XD
      UN=UN1+UD
      YN=YN1+YD
      ZN=ZN1+ZD
     OCALL PRIME (PPN ,UPN ,VPN ,WPN ,XPN ,YPN ,ZPN ,PN ,UN ,VN ,WN ,
     1    XN ,YN ,ZN )
      IF(NTN.LT.NTNCH)GO TO 200
      NTNCH=NTNCH2
      NTNCH2=1000000
      NDT=NDT1
      NDT1=NDT2
      DT=FLOAT(NDT)/1000.0
  200 IF(NTN.LE.100)GO TO 85
      IF((NTN-NB).NE.0)GO TO 90
      NB=NB+200
      IF(NTN.GE.1000)NB=NB+800
      IF(NTN.GE.20000)NB=NB+4000
      IF(NTN.GE.100000)NB=NB+45000
 85   RCH=(RAA+RBB+RCC+RDD-RPS-RPD)/1000.0
      VDS=(SIXX-VD)*1000.0
      TREAL=(QO*R*F*TN/QUICK)*100000000.0
C RCH IS IN K-OHMS, VDS IS IN MILLIVOLTS AND TREAL IS IN NANO-SECONDS
      WRITE(6,87)TN,PN,PPN,XN,XPN,YN,YPN,ZN,ZPN,RCH,VDS,TREAL
   87 FORMAT(1H ,F6.2,8F12.8,3F9.3)
   90 IF(TN.GT.TF)GO TO 20
      IF(LDISCH.EQ.1)GO TO 700
      CALL BKUPS(XN,YN,ZN)
      CALL BKUPP(XN,YN,ZN)
      GO TO 100
  700 CALL BKDNS(XN,YN,ZN)
      CALL BKDNP(XN,YN,ZN)
  100 NTO=NTN
      PO=PN
      XO=XN
```

```
      UO=UN
      YO=YN
      ZO=ZN
      PPO=PPN
      XPO=XPN
      UPO=UPN
      YPO=YPN
      ZPO=ZPN
  110 GO TO 70
      END
```

```
      SUBROUTINE SET(P ,U ,V ,W ,X ,Y ,Z )
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
     0COMMON /THREE/LUMP,Q0,Q1,Q2,Q3,Q4,Q5,G0,G1,G2,G3,QUICK,V2,V1,V34,
     1Q34
     0COMMON/FOUR/RPS,RPD,RO,RAA,RBB,RCC,RDD,QU,R,RAT,RISK,ROT,RUT,ROPE
     1,RUN,FORM,F,SIXX,I,L2,NOW,NEXT,ERROR,EDOWN,VAO,VBO,VCO,VEO,VFO,
     2 VLO,VD,RL,E,RG,CL,CGS,CGD,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10
      ERROR=0.005
      L2=0
      NEXT=1
C     CAN SET  W=0
      W =0.0
      V =0.0
      VAOO=0.0
      VBOO=0.0
      VCOO=0.0
      VEOO=0.0
      VFOO=0.0
      VAO=EDOWN
      VBO=EDOWN
      VCO=EDOWN
      VEO=EDOWN
      VFO=EDOWN
      VLO=-VD
      VLOO=0.0
      IF(EDOWN.EQ.E)A1=0.0
      IF(EDOWN.EQ.0.0)A1=E
      IF(EDOWN.GT.V2) GO TO 1
      IF(EDOWN.GT.V1) GO TO 2
      FX=F1
      FY=F1
      FZ=F1
      BX=B1
      BY=B1
      BZ=B1
      GO TO 100
1     FX=F3
```

```
      FY=F3
      FZ=F3
      BX=B3
      BY=B3
      BZ=B3
      GO TO 100
2     FX=F2
      FY=F2
      FZ=F2
      BX=B2
      BY=B2
      BZ=B2
  100 BXR=1.0/BX
      BYR=1.0/BY
      BZR=1.0/BZ
      IF(LUMP.EQ.1) GO TO 10
      P=VEO*CGS/QU
      U=VFO*CGD/QU
      X = (VAO/(FX*QUICK))**BXR
      Y = (VBO/(FY*QUICK))**BYR
      Z = (VCO/(FZ*QUICK))**BZR
      GO TO 20
   10 X = (VAO/(FX*QUICK))**BXR
      Y=VEO*CGS/QU
      Z=VFO*CGD/QU
      P=0.0
      U=0.0
20    IF( BKSX.GT.X.AND.BKSY.GT.Y.AND.BKSZ.GT.Z)GO TO 40
      CALL BKUPS (X,Y,Z)
      GO TO 20
40    IF( BKPX.GT.X.AND.BKPY.GT.Y.AND.BKPZ.GT.Z)GO TO 50
      CALL BKUPP (X,Y,Z)
      GO TO 40
   50 IF(ABS((VAO-VAOO)/VAO).LE.ERROR.AND.ABS((VBO-VBOO)/VBO).LE.ERROR
     1.AND.ABS((VCO-VCOO)/VCO).LE.ERROR.AND.ABS((VEO-VEOO)/VEO).LE.ERROR
     2.AND.ABS((VFO-VFOO)/VFO).LE.ERROR.AND.ABS((VLO-VLOO)/VLO).LE.ERROR
     3 ) RETURN
      CALL PRIME (PP,UP,VP,WP,XP,YP,ZP,P,U,V,W,X,Y,Z)
      VAOO=VAO
      VBOO=VBO
      VCOO=VCO
      VEOO=VEO
      VFOO=VFO
      VLOO=VLO
      L2=L2+1
      RIO=VD/(RAA+RBB+RCC+RDD+RL)
      VCO=EDOWN+RIO*RDD
      VBO=VCO+RIO*RCC
      VAO=VBO+RIO*RBB
      VEO=EDOWN
      VFO=VAO+RIO*RAA
      VLO=-VFO+EDOWN
      GO TO 100
      END
```

```
      SUBROUTINE BKUPS(X,Y,Z)
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
      IF(BKSX.GT.X) GO TO 10
      IF(BKSX-BK2)20,30,40
   20 BKSX=BK2
      SX=S2
      GO TO 10
      DX=D2
   30 BKSX=BK3
      SX=S3
      DX=D3
      GO TO 10
   40 BKSX=1.0
      SX=S4
      DX=D4
10     IF(BKSY.GT.Y) GO TO 50
      IF(BKSY-BK2)60,70,80
   60 BKSY=BK2
      SY=S2
      DY=D2
      GO TO 50
   70 BKSY=BK3
      SY=S3
      DY=D3
      GO TO 50
   80 BKSY=1.0
      SY=S4
      DY=D4
50    IF(BKSZ.GT.Z) GO TO 90
      IF(BKSZ-BK2)100,110,120
  100 BKSZ=BK2
      SZ=S2
      DZ=D2
      GO TO 90
  110 BKSZ=BK3
      SZ=S3
      DZ=D3
      GO TO 90
  120 BKSZ=1.0
      SZ=S4
      DZ=D4
   90 RETURN
      END
```

```
      SUBROUTINE BKDNS (X,Y,Z)
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
      IF(BKSX.LT.X) GO TO 10
      IF(BKSX-BK2) 20,30,40
20    BKSX=0.0
      SX=S1
      DX=D1
      GO TO 10
30    BKSX=BK1
      SX=S2
      DX=D2
      GO TO 10
40    BKSX=BK2
      DX=D3
      SX=S3
10    IF(BKSY.LT.Y)GO TO50
      IF(BKSY-BK2)60,70,80
60    BKSY=0.0
      SY=S1
      DY=D1
      GO TO 50
70    BKSY=BK1
      SY=S2
      DY=D2
      GO TO 50
80    BKSY=BK2
      SY=S3
      DY=D3
50    IF(BKSZ.LT.Z)GO TO 90
      IF(BKSZ-BK2 )100,110,120
100   BKSZ=0.0
      SZ=S1
      DZ=D1
      GO TO 90
110   BKSZ=BK1
      SZ=S2
      DZ=D2
      GO TO 90
120   BKSZ=BK2
      SZ=S3
      DZ=D3
90    RETURN
      END
```

```
      SUBROUTINE BKUPP (X,Y,Z)
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
      IF(BKPX.GT.X) GO TO 10
      IF(BKPX.EQ.BK4) GO TO 20
      BKPX=1.0
      FX=F3
      BX=B3
      GO TO 10
   20 BKPX=BK5
      FX=F2
      BX=B2
10    IF(BKPY.GT .Y) GO TO 30
      IF(BKPY.EQ.BK4) GO TO 40
      BKPY=1.0
      FY=F3
      BY=B3
      GO TO 30
   40 BKPY=BK5
      FY=F2
      BY=B2
30    IF(BKPZ.GT.Z) GO TO 50
      IF(BKPZ.EQ.BK4) GO TO 60
      BKPZ=1.0
      FZ=F3
      BZ=B3
      GO TO 50
   60 BKPZ=BK5
      FZ=F2
      BZ=B2
   50 RETURN
      END
```

```
      SUBROUTINE BKDNP(X,Y,Z)
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
      IF(BKPX.LT.X)GO TO 10
      IF(BKPX.EQ.BK4)GO TO 20
      BKPX = BK4
      FX=F2
      BX=B2
      GO TO 10
20    BKPX=0.0
      FX=F1
      BX=B1
10    IF(BKPY.LT.Y)GO TO 30
      IF(BKPY.EQ.BK4) GO TO 40
      BKPY=BK4
```

```
      FY=F2
      BY=B2
      GO TO 30
40    BKPY=0 .0
      FY=F1
      BY=B1
30    IF(BKPZ.LT.Z)GO TO 50
      IF(BKPZ.EQ.BK4)GO TO 60
      BKPZ=BK4
      FZ=F2
      BZ=B2
      GO TO 50
60    BKPZ=0.0
      FZ=F1
      BZ=B1
50    RETURN
      END
```

```
      SUBROUTINE INITIL
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
     0COMMON /THREE/LUMP,Q0,Q1,Q2,Q3,Q4,Q5,G0,G1,G2,G3,QUICK,V2,V1,V34,
     1  Q34
      BK1=Q1/Q0
      BK2=Q2/Q0
      BK3=Q3/Q0
      BK4=Q4/Q0
      BK5=Q5/Q0
      S1=(G0*Q1)/((G0-G1)*Q0)
      D1=Q1/(Q0*(G0-G1)*FLOAT(LUMP))
      IF(G1.EQ.G2) GO TO 50
      S2=(1.0/Q0)*(G1*(Q2-Q1)/(G1-G2)+Q1)
      D2=(Q2-Q1)/(Q0*(G1-G2)*FLOAT(LUMP))
      IF(G2.EQ.G3) GO TO 60
      S3=(1.0/Q0)*(G2*(Q3-Q2)/(G2-G3)+Q2)
      D3=(Q3-Q2)/(Q0*(G2-G3)*FLOAT(LUMP))
      IF(G3.EQ.0.) GO TO 70
      S4=1.0
      D4=(Q0-Q3)/(Q0*G3*FLOAT(LUMP))
      GO TO 80
50    S2=S1
      D2=D1
60    S3=S2
      D3=D2
70    S4=S3
      D4=D3
80    A1=ALOG(QUICK)
      A2=ALOG(V2)
      A3=ALOG(V1)
      A4=ALOG(V34)
      A5=ALOG(Q0)
```

```
      A6=ALOG(Q5)
      A7=ALOG(Q4)
      A8=ALOG(Q34)
      B1=(A3-A4)/(A7-A8)
      IF(A6.EQ.A7) GO TO 2
      B2=(A2-A3)/(A6-A7)
      IF(A5.EQ.A6) GO TO 3
      B3=(A1-A2)/(A5-A6)
      GO TO 4
2     B2=B1
3     B3=B2
4     F3=1.0
      F2=((Q5/Q0)**B3)* (Q0/Q5)**B2
      F1=((Q5/Q0)**B3)*((Q4/Q5)**B2)*(Q0/Q4)**B1
      SX=S1
      SY=S1
      SZ=S1
      DX=D1
      DY=D1
      DZ=D1
      FX=F1
      FY=F1
      FZ=F1
      BX=B1
      BY=B1
      BZ=B1
      BKSX=BK1
      BKSY=BK1
      BKSZ=BK1
      BKPX=BK4
      BKPY=BK4
      BKPZ=BK4
      IF(LUMP.EQ.1) GO TO 10
      RETURN
   10 BKSY=10.0
      BKSZ=10.0
      BKPY=10.0
      BKPZ=10.0
      RETURN
      END
```

Subroutine PRIME for 3-Lump Model

```
      SUBROUTINE PRIME (PP,UP,VP,WP,XP,YP,ZP,P,U,V,W,X,Y,Z)
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
     0COMMON /THREE/LUMP,Q0,Q1,Q2,Q3,Q4,Q5,G0,G1,G2,G3,QUICK,V2,V1,V34,
     1Q34
     0COMMON/FOUR/RPS,RPD,RO,RAA,RBB,RCC,RDD,QU,R,RAT,RISK,ROT,RUT,ROPE
     1,RUN,FORM,F,SIXX,I,L2,NOW,NEXT,ERROR,EDOWN,VAO,VBO,VCO,VEO,VFO,
     2 VLO,VD,RL,E,RG,CL,CGS,CGD,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10
      GO TO (7,8),NEXT
7     NEXT=2
      R=RO
      FORM=F*R*FLOAT(LUMP)/QUICK
      C= CGD/CGS + CGD/CL
      D= 1.0/(1.0+C)
      F11=D*(1.0+CGD/CL)
      RAT=FORM*F11
      RISK=FORM*(1.0/RL)*(D*(CGS/CL+(CGS/CL)*(CGD/CL))-CGS/CL)
      ROT=FORM*(D*(1.0+CGS/CL+CGD/CL+(CGS/CL)*(CGD/CL))-CGS/CL)
      RUT=FORM*D*(CGD/CGS)
      RUN =FORM* C*D
      ROPE=FORM*D*(CGD/CL)/RL
      WRITE(6,10) FORM,F11,RAT,RISK,ROT,RUT,RUN,ROPE
10    FORMAT(1H ,8E14.4)
8     RAA=RPD+0.5*DX/(SX-X)
      RBB=0.5*(DX/(SX-X)+DY/(SY-Y) )
      RCC=0.5*(DY/(SY-Y)+DZ/(SZ-Z))
      RDD=RPS+0.5*DZ/(SZ-Z)
20    VA=QUICK*FX*X**BX
      VB=QUICK*FY*Y**BY
      VC=QUICK*FZ*Z**BZ
      VE=QU*P/CGS
      VF=QU*U/CGD
      ONEE=(VA-VF)/RAA
      TWOO=(VB-VA)/RBB
      THRE =(VC-VB)/RCC
      FOU = (VE-VC)/RDD
      FIV=(A1-VE)/RG - FOU
      SIXX= VE-VF+VD
      XP = FORM*(TWOO-ONEE)
      YP = FORM*(THRE  - TWOO)
      ZP = FORM*(FOU  - THRE )
      PP =RAT*FIV  +RISK*SIXX+ROT*ONEE
      UP =RUT*FIV  +ROPE*SIXX+RUN*ONEE
      RETURN
      END
```

Subroutine PRIME for 1-Lump Model

```
      SUBROUTINE PRIME (PP,UP,VP,WP,XP,YP,ZP,P,U,V,W,X,Y,Z)
      COMMON/ONE/S1,S2,S3,S4,BK1,BK2,BK3,SX,SY,SZ,BKSX,BKSY,BKSZ
     0COMMON /TWO/F1,F2,F3,B1,B2,B3,BK4,BK5,FX,FY,FZ,BX,BY,BZ,BKPX,
     1BKPY,BKPZ,D1,D2,D3,D4,DX,DY,DZ
     0COMMON /THREE/LUMP,Q0,Q1,Q2,Q3,Q4,Q5,G0,G1,G2,G3,QUICK,V2,V1,V34,
     1Q34
     0COMMON/FOUR/RPS,RPD,RO,RAA,RBB,RCC,RDD,QU,R,RAT,RISK,ROT,RUT,ROPE
     1,RUN,FORM,F,SIXX,I,L2,NOW,NEXT,ERROR,EDOWN,VAO,VBO,VCO,VEO,VFO,
     2 VLO,VD,RL,E,RG,CL,CGS,CGD,A1,A2,A3,A4,A5,A6,A7,A8,A9,A10
C     ONE LUMP T MODEL
      GO TO (7,8),NEXT
7     NEXT=2
      R=RO
      FORM=F*R*FLOAT(LUMP)/QUICK
      C= CGD/CGS + CGD/CL
      D= 1.0/(1.0+C)
      F11=D*(1.0+CGD/CL)
      RAT=FORM*F11
      RISK=FORM*(1.0/RL)*(D*(CGS/CL+(CGS/CL)*(CGD/CL))-CGS/CL)
      ROT=FORM*(D*(1.0+CGS/CL+CGD/CL+(CGS/CL)*(CGD/CL))-CGS/CL)
      RUT=FORM*D*(CGD/CGS)
      RUN =FORM* C*D
      ROPE=FORM*D*(CGD/CL)/RL
      WRITE(6,10) FORM,F11,RAT,RISK,ROT,RUT,RUN,ROPE
10    FORMAT(1H ,8E14.4)
8     RAA= RPD+0.5*DX/(SX-X)
      RBB = 0.0
      RCC = 0.0
      RDD = RPS+0.5*DX/(SX-X)
20    VA=QUICK*FX*X**BX
      VE = QU*Y/CGS
      VF = QU*Z/CGD
      ONEE = (VE-VA)/RDD
      TWOO = (VA-VF)/RAA
      THRE =(A1-VE)/RG
      SIXX = VE-VF+VD
      PP= 0.0
      UP = 0.0
      XP = FORM*(ONEE-TWOO)
      YP = RAT*(THRE-ONEE) + ROT*TWOO + RISK*SIXX
      ZP = RUT*(THRE-ONEE) + RUN*TWOO + ROPE*SIXX
      RETURN
      END
```