SEMI-CONDUCTOR THREE-PHASE INVERTERS FOR OPERATING INDUCTION MOTORS AT VARIABLE SPEED

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by

B. L. Jones.

(Berwyn Lloyd Jones.)

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ABSTRACT.

This investigation is concerned with the application of variable frequency S C R inverters supplying a.c. motors, particularly induction motors, in variable speed drives.

The inverters dealt with are all based upon the three phase bridge circuit, the main difference between them is the method adopted for turning off the S C Rs and transferring load current from one phase to the next.

The main body of the thesis deals with the inverters used and all aspects of their performance. Methods are developed for predicting the current and voltage waveforms in the circuits, the harmonic content of the load waveforms, and the power losses in the circuits for inductive loads. Wherever possible simplified formulae are devised to assist in the initial design of the inverters.

An elementary examination is made of the effects of the inverter output waveforms upon the performance of the motor. This shows that the motor efficiency is affected only by 1% to 3% by the harmonic content of the inverter waveforms.

A large component of the power loss in each of the inverter circuits studied is caused by the commutation method employed and depends greatly upon operating frequency. Methods of reducing this commutation loss are discussed.

At the end of the thesis the main results of the investigation are summarised in a typical design calculation for a large system.

ACKNOWLEDGEMENTS.

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LIST OF SYMBOLS

The following is a list of the more important symbols which have been used consistently throughout this thesis. Some other symbols have different definitions in each chapter and are defined as they occur in the text.

$V_\ell, V_1, V_5, V_7, \ldots V_n, \ldots$	: Total r.m.s. value, fundamental, 5th, 7th,..nth,.. harmonic component of inverter output line-to-line voltage.
$I_\ell, I_1, I_5, I_7, \ldots I_n, \ldots$	: Total r.m.s. value, fundamental, 5th, 7th,...nth,.. harmonic component of inverter output line current.
i_a, i_b, i_c	: Current in phases A, B, C, of load.
v_{ab}, v_{bc}, v_{ca}	: Voltage between lines A and B, B and C, C and A, of load.
V_d, V_a	: Main and auxiliary d.c. supply voltages.
f, T	: Frequency and period of inverter output waveforms.
$t_1, t_2, \ldots t_6$	: Instant of firing of CR1, CR2, .. CR6.
R, L	: Resistance and inductance per load phase.
C	: Capacitance of commutatating capacitor.
δ	: Time for which reverse voltage is applied to S C R at turn-off.

INTRODUCTION

For many years the only motors capable of providing high power variable speed drives have been of the commutator type or of the slip-ring type of induction motor, the latter being rendered inefficient on account of the large amounts of energy dissipated in the controlling resistances at speeds much lower than synchronous speed.

The main objections to the commutator motor are the restrictions imposed by the commutator upon the operating voltage and current, the space taken up by the commutator and, perhaps more important, the careful maintenance required to keep the motor in perfect condition. Alternative methods of producing variable speed drives without resorting to the use of mechanical commutators have, therefore, been continually sought after.

To be viable any alternative system should be robust, reliable, efficient, compact (for many applications), and should require little or no maintenance. Many schemes have been developed over the years but most have been abandoned because they did not satisfy all the above requirements or were too costly. The advent of the silicon controlled rectifier has focussed attention once more, however, on the possibility of controlling motor speed without resorting to commutators or forms of resistance control.

The silicon controlled rectifier, or Thyristor, as it is becoming known, is a semiconductor device which is capable of switching high powers very rapidly. It is many times smaller than a thyratron or ignitron of comparable power rating, is entirely metallic with ceramic insulation and, therefore, very robust, can be turned on in about a hundredth and off in about a fortieth of the time taken by a mercury vapour device, and has a much smaller voltage drop when conducting. It is, therefore, far more likely that a device such as the SCR (silicon controlled rectifier) should, unlike the mercury vapour devices, be suitable for use in circuits employing switching techniques for motor speed control.

Three possible methods of using switching techniques were considered at the outset of the investigation:-

(a) Employing the principle of the mechanical commutator for maintaining the stator and rotor fields in a fixed relative position, but replacing the commutator and brushgear by an arrangement of SCRs connected to the stator winding. By arranging for the current to enter and leave at opposite ends of the stator winding, and making these points progress by sequentially switching the SCRs on and off, the commutator function could be copied almost exactly. Then by connecting the armature winding appropriately any form of d.c. motor characteristic could be reproduced.

(b) Employing a slipring induction motor together with a rectifier - inverter combination in place of the speed controlling resistance used hitherto. By rectifying the slip power and inverting it back into the motor supply it would be possible to arrange for the motor to run efficiently at any desired speed. Speed control could be effected by varying the amount of slip power converted.

(c) Employing a frequency changer or variable frequency inverter to supply an induction motor and thus cause it to run near any desired synchronous speed.

It will be seen that in (a) and (b) an electrical connection must be made with the armature to provide the field excitation or extract the slip power. In (c), however, brushgear and sliprings could be dispensed with entirely by using a squirrel cage type of induction motor which is an extremely robust and relatively cheap form of motor. Mainly for this reason it was decided that the method (c) was of greatest merit and it was upon this method that attention was concentrated in the investigation reported in the pages that follow.

The objects of the investigation may be stated as follows:-

(a) to contruct a practicable inverter-motor system for a 5 H.P. motor,

(b) to determine what requirements should be fulfilled by the inverter for supplying loads at lagging power factors,

(c) to measure the system efficiency and account for the losses,

(d) to measure the torque-speed characteristics of the system and investigate its capacity for regenerative braking,

(e) to determine the effect upon the motor of the harmonics inevitably produced by the inverter,

(f) to determine whether any limits should be imposed upon the operation of the system,

(g) to determine the ratings required of the various components of the system,

(h) to analyse the operation of the circuit with a view to predicting the behaviour of a similar, but much larger system.

In the early stage of the investigation it was realised that the transient analysis of the inverter circuit would be incompatible with the harmonic analyses available for induction motors. It was, therefore, decided that the operation of the motor under "continuous transient" conditions warranted a separate full-scale investigation. Accordingly it will be found that this thesis deals primarily with the inversion problem and that observations made upon the behaviour of the motor are, as a result, of a somewhat elementary nature.

It is hoped that the investigations into the circuit arrangements described in the thesis will contribute considerably to the knowledge of and confidence in the design and operation of variable speed motor controllers using SCRs.

CHAPTER 1

THE SILICON CONTROLLED RECTIFIER (S C R)

1.1 General Characteristics of the S C R.

The S C R is a semiconductor device consisting of four layers alternately of p- and n- type silicon as outlined in Fig. 1.1. The anode, cathode and gate connections are made to the points shown. The circuit symbol shown in Fig. 1.2 is used to represent the S C R throughout this thesis.

The device possesses characteristics similar to those of the thyratron or ignitron. It is a rectifier and can therefore pass current in one direction only - the forward direction from anode to cathode. It is a controlled rectifier and can therefore block forward voltage until conduction is initiated by a control signal applied to its gate terminal.

The main characteristics of the S C R as they affect the operation of the inverter circuits to be described will now be briefly described.

1.2 Blocking (Off) and Conducting (On) States.

The normal state of the S C R is blocking, or off. In this state the device allows only a very small leakage current to flow whether the voltage on the anode is positive or negative with respect to the cathode, i.e. whether the device is forward or reverse biased. In each direction, however, there is a limit to the voltage which the S C R can safely block. In the reverse direction this is the rated peak reverse voltage (P R V) above which the reverse leakage current increases sharply. This reverse voltage should never be exceeded, even for very

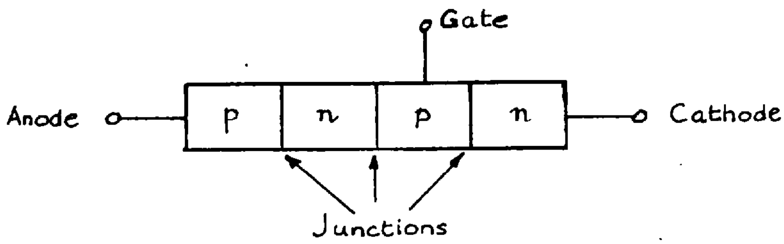


Fig. 1.1: Electrical structure of SCR.

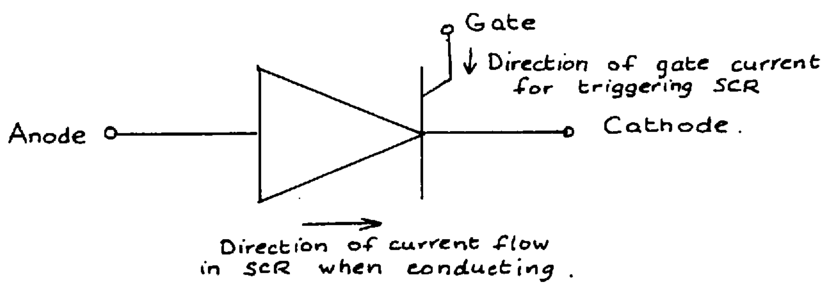


Fig. 1.2 : Circuit symbol for SCR used in thesis.

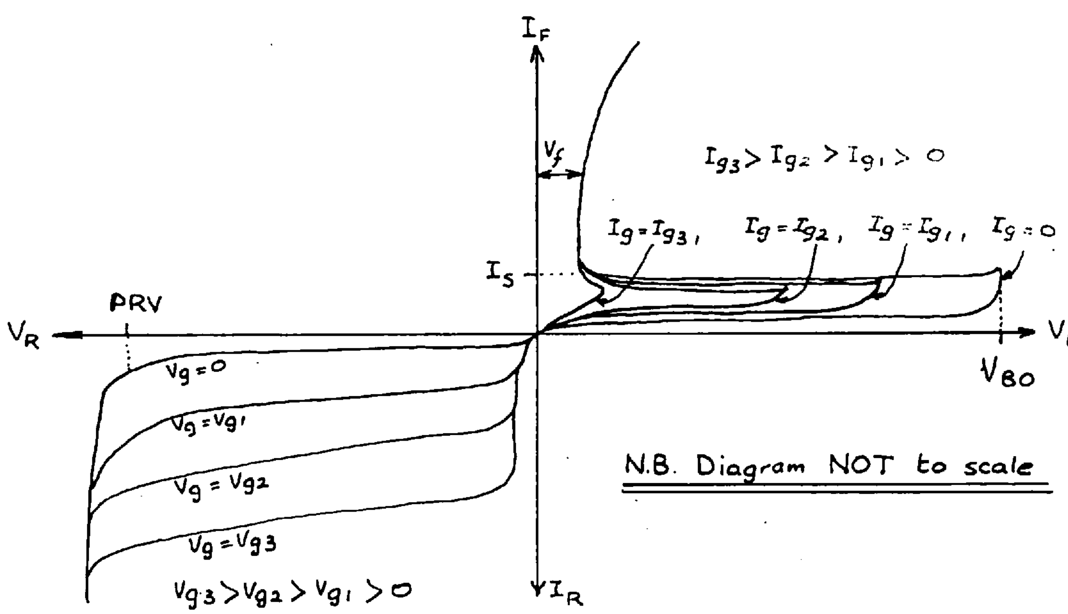


Fig. 1.3 : Typical features of the forward and reverse voltage - current characteristics of the SCR.

short periods of the order of 1 μ sec, because the resulting high power dissipation causes localised heating in the junctions and almost invariably damages the S C R permanently, destroying forever its blocking properties. In the forward direction the voltage limit is the forward breakover voltage (VBO) at which point the forward leakage current increases sharply and sets off, by transistor action, an avalanche process which causes the S C R to switch rapidly into the conducting state. This conducting state is self sustaining and the current in the device is limited only by the external circuit, the forward voltage across the S C R having fallen to about 1 V. For the S C R to remain in the conducting state the forward current must be kept above a certain minimum value known as the holding or sustaining current (I_s). If the current is reduced below this value the S C R reverts to the blocking state.

Fig. 1.3 shows the voltage-current characteristics of the S C R. When conducting the forward voltage drop (V_f) is low (about 1 to 1.5 v), but rises a little with current. Fig. 1.3 also shows the results of passing current into the gate. Gate current has the effect of reducing the forward breakover voltage, the higher the gate current then in general the lower the breakover voltage. To switch on the S C R it is thus necessary only to inject sufficient gate current to reduce the breakover voltage below the forward voltage being blocked. It is usual, however, because of the widely differing firing characteristics of individual S C Rs, to inject gate current sufficient to reduce the breakover voltage almost to zero as for $Ig = Ig_3$ in Fig. 1.3.

When the S C R is reverse biased the leakage current is increased if positive gate to cathode voltage is applied. The resulting power dissipation can become so high that it is necessary to specify a maximum gate to cathode voltage of about 0.25 V which may be applied during reverse bias without derating the S C R.

Between the four layers of the S C R are three junctions where the n-type silicon of one layer merges with the p-type silicon of the adjacent layer. These junctions are the regions of the S C R which support any blocked voltages and are very thin. Consequently each junction has a certain small amount of capacitance between the layers on either side. Because of this capacitance it is possible for a fast-rising forward voltage to produce sufficient charging current in the S C R to initiate conduction in the same way as an injected gate current. A maximum rate of rise of forward voltage is therefore specified for the S C R.

1.3 Turning on the S C R

Turning on the S C R by increasing the anode voltage above the breakover level is not recommended, particularly in the case of high voltage S C Rs. This is because it is possible that the intrinsic breakover voltage is higher than the breakdown voltage at which point the leakage current increases due to surface irregularities in the S C R junctions. Local heating could then cause degradation of the blocking properties or other permanent damage to the junctions.

The recommended turn-on method is to inject gate current at the instant when conduction is required to commence, thereby reducing the breakover voltage to a low level. The gate current pulse should be maintained long enough for the current in the S C R and its external circuit to rise well above the sustaining current level. After this the gate loses control and the gate current can be discontinued, conduction being self-sustaining thereafter.

After the start of the gate current pulse there is a delay before the anode voltage begins to fall appreciably. The delay can be reduced to some extent by increasing the magnitude and/or decreasing the rise time of the gate current pulse but is generally of the order of 1 to 5 μsecs. Following this delay there is a period which is confusingly called the rise time during which the anode voltage falls and the load voltage rises. The rise time, defined as the time taken for the anode voltage to fall from 90% to 10% of its original value, depends upon the nature of the load and the current being switched on. The anode voltage falls more quickly when the load is inductive than when the load is purely resistive and more slowly when the current is increased. Typical values of the rise time are 1 μsec for inductive loads and 3 or 4 μsecs for purely resistive loads.

When conduction is initiated the conducting region of the S C R expands radially from the gate, the radius increasing at an approximately uniform rate. If current in the S C R is allowed to rise too quickly during turn on, the concentration of current into the expanding but as yet small, conducting region can create very high current densities. Local melting can thus occur in the gate region and destroy the blocking properties of the S C R. This is particularly troublesome in high current S C Rs since the prospective currents are higher than in low current S C Rs while the conducting region expands at approximately the same rate in both types. A maximum rate of rise of current of about 20 to 30 A/μsec is therefore recommended for the first 5 to 10 μsecs of conduction to eliminate the possibility of local fusing in the vicinity of the gate.

1.4 Turning Off the S C R.

The S C R can be made to turn off merely by reducing the current below the sustaining value but the resulting turn off time is long, being of the order of 100 to 200 μsecs. Before the S C R can recover its blocking properties the holes and electrons near the two outer junctions shown in Fig. 1.1 must diffuse to the appropriate sides of these junctions. This process can be speeded up by applying a reverse voltage to the S C R and allowing a reverse current to flow. The diffusion process then takes a few μ secs instead of a few hundred μ secs. After this process is complete the holes and electrons in the vicinity of the centre junction must recombine before the S C R becomes capable of blocking forward voltage. The recombination process takes between 10 and 30 μ secs normally, depending on the S C R, and is virtually independent of the reverse voltage.

In a.c. circuits where the S C R is used as a rectifier the current falls to zero and reverse voltage is applied to the S C R at the end of each conducting period. This also happens when the S C R is used in an oscillatory circuit, e.g. when charging a capacitor from a d.c.

supply through a choke. When the S C R is used as a switch in a d.c. pulsing circuit, such as an inverter, some other means must be used to cut off the S C R current and apply reverse voltage to the S C R. This is most conveniently done by connecting a negatively charged capacitor across the S C R as shown in Fig. 1.4. The capacitor voltage is applied to the S C R, reverse biasing it, and the S C R current is diverted into the capacitor charging it towards a positive voltage. Reverse voltage must be maintained long enough for the S C R to recover, after which forward voltage may be reapplied to the S C R. The means of connecting the capacitor across the S C R is usually through a second S C R, either an S C R in the circuit which turns on when the first is required to turn off, or an auxiliary S C R which is used only for turning off the main S C R.

The charge which must be removed from the S C R during the first part of turn off increases with the forward current and the rate of fall of forward current immediately before turn off. Apart from the effect of the reverse current upon commutation (the capacitor current being the sum of the load current previously flowing in the S C R and the S C R reverse current), voltage transients can be set up by the sudden cessation of reverse current. These can be limited by the inclusion of suitable suppression circuits (see Section 1.7).

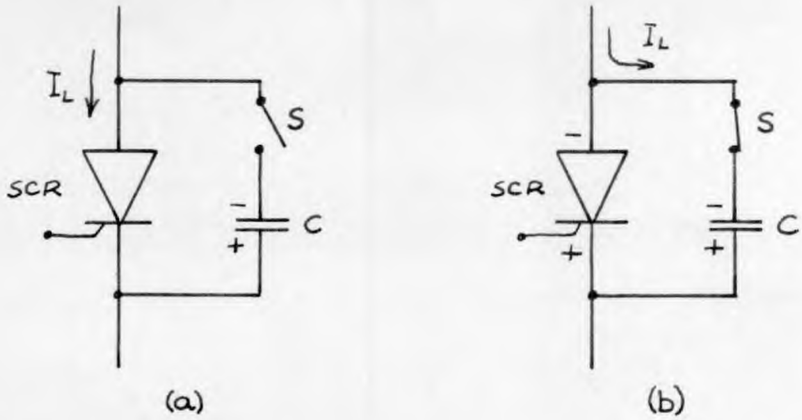


Fig. 1.4 : Usual method of turning off SCRs in circuits with d.c. supplies.

(In (a) the SCR conducts. Turn-off is achieved by connecting the negatively-charged capacitor C across the SCR when switch S is closed, as in (b). The load current I_L then flows into C and charges C towards opposite polarity.)

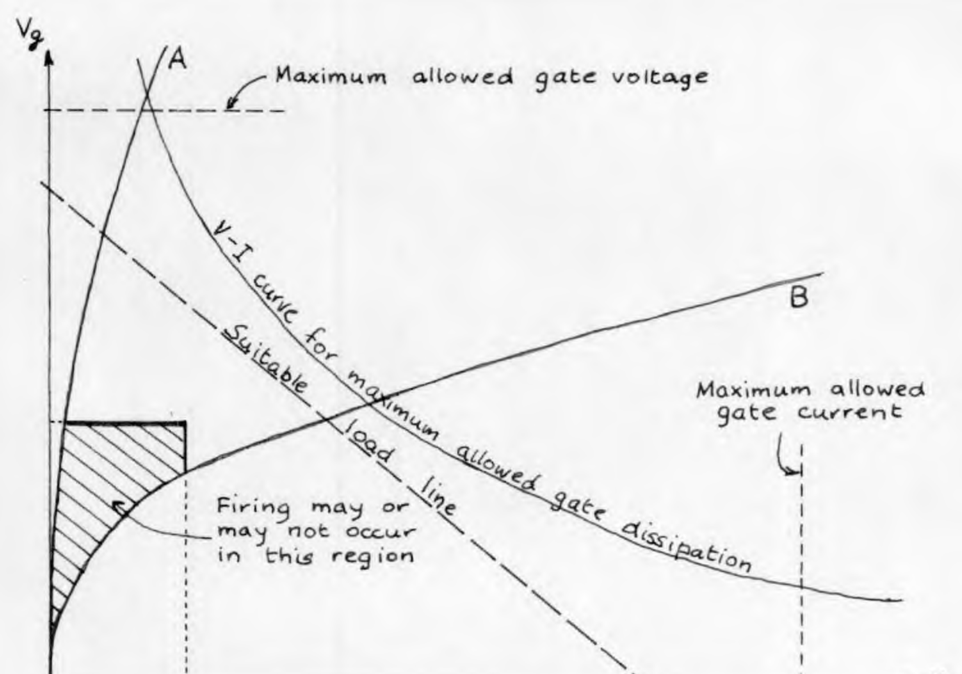


Fig. 1. 5 : Essential features of gate and firing characteristics of SCR.

1.5 Current Ratings of the S C R.

At all except very high switching frequencies, where the power loss during switching (i.e. the product of the falling S C R voltage and rising current) becomes significant, almost all the power dissipated in the S C R is composed of forward conduction losses. The power loss at any instant is therefore the product of the forward current and the forward voltage drop.

The current rating assigned to the S C R under any given set of conditions is that which causes the junction temperature to rise to the maximum permitted value. Consequently the current which may safely be passed through the S C R must be reduced when the ambient temperature is increased. The S C R, together with the heat sink on which it must be mounted, has a steady state thermal resistance from which the mean junction temperature above ambient can be calculated for any given power dissipation. When direct current passes through the device the mean and peak junction temperatures are the same. Because the S C R has a relatively short heating time constant the peak junction temperature must rise above the mean when the S C R current consists of pulses. Consequently the current rating varies with the conduction angle, or duty cycle, of the S C R. It is also clear that the current rating must depend upon the capacity of the S C R and its heat sink to dissipate the power losses due to conduction.

The current rating is usually expressed as the mean current over a complete switching cycle. An r.m.s. current rating is also assigned to the S C R. This is intended to indicate the current level at which the ohmic contacts and leads inside the S C R construction start to become warm and is of interest when the r.m.s. current is much greater than the mean S C R current, as when the duty cycle is small.

If the maximum permitted junction temperature is exceeded, the first things that normally happen are that the breakover voltage starts to fall and the leakage currents increase. However, a margin of safety is allowed in rating the devices and therefore higher temperatures can be tolerated for short times. The surge rating of the S C R indicates the magnitude of the surge current which can be allowed to flow for a given length of time. This rating is higher, of course, if the junction temperature is low before the surge and also if the voltage applied to the S C R intermittently during the surge is kept well below the rated values.

The "I^2t" rating of the S C R applies when surges of less than about 10 msecs duration are encountered and is an indication of the absolute maximum current which can be allowed to pass through the S C R without damaging it by setting up extreme thermal stresses. Its main purpose is to help the circuit designer to choose a fuse, connected in series with the S C R, which will interrupt the current before the S C R is damaged, i.e. a fuse with a smaller I^2t rating than the S C R's must be used.

1.6 Gate Characteristics.

The gate characteristics and triggering requirements of S C Rs, even of the same type, vary considerably. Fig. 1.5 shows the form of gate characteristic given on S C R data sheets. Some S C Rs require a relatively high gate voltage to drive a relatively small current into the gate, as shown by characteristic A, whilst for some other S C Rs the reverse is true (characteristic B). Some S C Rs require a relatively high gate current for reducing the breakover voltage almost to zero whilst others fire with much smaller gate currents. It is usual to show a region on the published gate characteristics where firing may or may not occur. Outside this region (shown by hatched lines in Fig. 1.5) firing can be guaranteed for all S C Rs of the same type. It is then necessary only to ensure that the gate is supplied from a source with sufficient voltage and series resistance to ensure that the load line passes only through the guaranteed firing region. It is also necessary to ensure that at no point on the load line is the maximum permitted gate dissipation exceeded. (The gate region is small and hence the gate power rating is also small.) A suitable load line is shown in Fig. 1.5.

1.7 Protection of the S C R.

The S C R should be protected against fault currents either by a fuse of a lower I^2t rating than the S C R or by incorporating some special overcurrent protection in the supply feeding the S C R circuit. In either case the current should be interrupted before any damage is done to the S C R.

Too rapid an increase of current at turn on can be prevented by ensuring that there is sufficient inductance in series with the S C R. This reduces the switching loss during the turn on rise time and prevents overheating of the gate region.

Rapid rates of rise of forward voltage can be reduced by connecting across the S C R a capacitive filter circuit. This should be designed to prevent the forward voltage from rising at a rate greater than the specified limit and so eliminate the possibility of the S C R's firing spuriously due to capacitive action between the layers of the S C R.

Absolute overvoltages can only be prevented by ensuring that under no possible conditions of operation does the circuit voltage exceed the S C R rating or by connecting across each S C R some surge suppressing device. Filter circuits can help to limit transient voltage peaks but care should be taken to ensure if a capacitor is connected directly across an S C R for this purpose that its energy is not sufficient to damage the S C R at turn on.

For a more detailed account of the characteristics of S C Rs the various S C R manuals[1,2,3] should be consulted.

CHAPTER 2

THE BASIC THREE PHASE BRIDGE-CONNECTED INVERTER AND ITS USE WITH A THREE PHASE SYNCHRONOUS MOTOR.

An inverter is a device which converts direct current into alternating current. The most usual method of conversion is to switch the direct current into and out of each of the load phases in sequence so as to generate what is essentially a stepped form of alternating current. Controlled rectifiers can be used as the switching elements in the inverter circuit.

There is a wide variety of types of inverter circuit but all those dealt with in this thesis are based on the three phase bridge-connected circuit.

In the early stages of the investigation no S C Rs were available and it was felt that a useful introduction to the subject would be to study a system in which thyratrons could be used. This system consisted of a three phase bridge-connected inverter and a three phase synchronous motor. The a.c. voltages generated by the motor were used for turning off the thyratrons at the required instants. This is a method of inversion often used[4,5] when it is required to transfer power from a d.c. supply to an existent a.c. system. The circuit was not exhaustively investigated but some conclusions relevant to the main investigation were reached. First, however, follows a brief description of the principle of the three phase bridge-connected inverter.

2.1 The Three Phase Bridge-Connected Inverter.

2.1.1 Principle of operation and basic waveforms for resistance load.

Fig. 2.1 shows the three phase bridge circuit in which CR1, CR2, ... CR6 are controlled rectifiers. The a.c. output lines are connected as indicated and the polarity of the d.c. supply shown is correct for inversion.

Current flows from the d.c. supply through one of the rectifiers in the upper row and one of the load phases and returns to the supply through another of the load phases and one of the rectifiers in the lower row. The rectifiers are fired in the order 1.2.3.4.5.6.1.... and some method (not shown at this stage because methods vary from one inverter to another) is used to turn off a rectifier when the next one in the same row is fired, i.e. CR1 turns off when CR3 is fired, CR2 turns off when CR4 is fired, and so on. In this way it is arranged that each rectifier conducts for one third of a firing cycle.

The basic current and voltage waveforms shown in Fig. 2.2 have been drawn for a balanced resistive star-connected load. It has been assumed that the current and voltage on the d.c. side are perfectly smooth and that transfer, or commutation, ofcurrent from one load phase to the next is instantaneous. When CR1 conducts the current I_d flows from the d.c. supply into phase A and returns first through B and CR6 and later through phase C and CR2. The current in phase A consists of a rectangular pulse of current I_d for one third of a cycle while CR1 conducts, zero when neither CR1 nor CR4

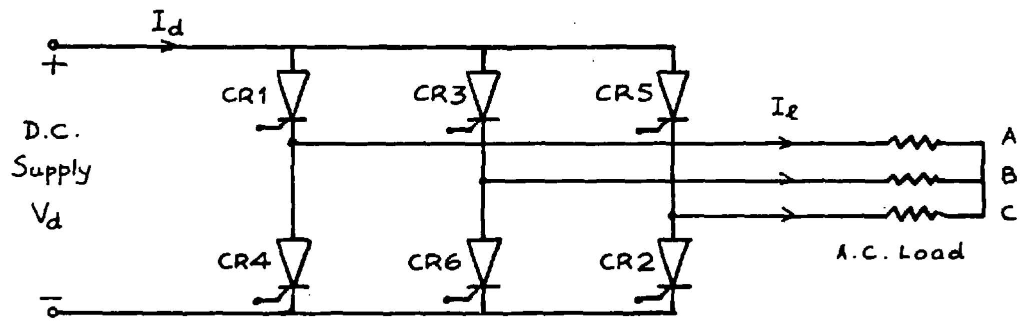


Fig. 2.1: Basic circuit of three-phase bridge-connected inverter.

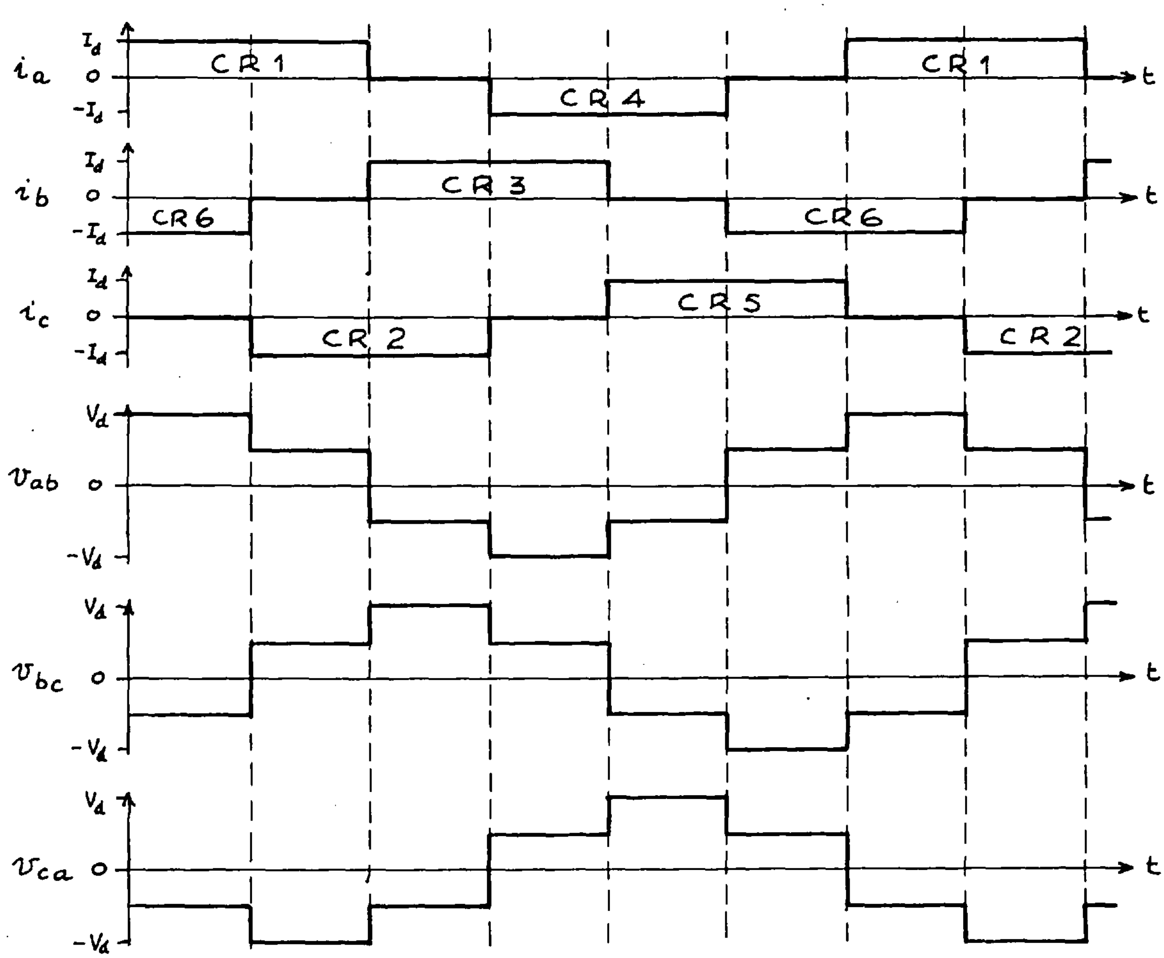


Fig. 2.2: Basic inverter output waveforms (for resistive load.)

conducts, $-I_d$ for a third of a cycle while CR4 conducts, and then zero again while neither CR4 nor CR1 conducts. The other load phase currents are similar to the current in phase A but displaced by one third of a cycle in either direction. On the current waveforms are indicated which rectifiers conduct. Since the load is resistive the line-to-neutral load voltage waveforms are identical in form with the current waveforms. The magnitude of these voltage waveforms is $\frac{1}{2}V_d$ since the supply current always passes through two load phases, effectively in series. The line-to-line voltages can then be found by taking the difference between the appropriate line-to-neutral voltages.

These basic waveforms are seen to constitute a three phase alternating system in which the fundamental sinusoidal components are displaced between phases by one third of a cycle.

The frequency of the a.c. output from the inverter depends only upon the frequency with which the rectifier firing sequence is repeated.

2.1.2 Harmonic content of basic waveforms.

When a Fourier analysis is made of the basic waveforms of Fig. 2.2 it is found that both current and voltage waveforms contain only odd harmonics, none of these being a multiple of three. This is an advantage of this type of waveform since it has been found[6] that it is the third harmonics which have the greatest deteriorating effect upon the performance of a three phase motor.

The rms values of the harmonics in terms of the d.c. voltage V_d and current I_d are given in Table 2.1. The total rms values of the voltages and currents are also given. The harmonic analysis for obtaining these values is given in most books on rectifiers.[4,5]

Order of Harmonic	Line-to-neutral voltage, $V_{\ell n}$	Line-to-line voltage, V_ℓ	Phase Current I_ℓ
1	$0.39\ V_d$	$0.67\ V_d$	$0.78\ I_d$
5	$-0.078V_d$	$-0.13\ V_d$	$-0.16\ I_d$
7	$0.056V_d$	$-0.10\ V_d$	$0.11\ I_d$
11	$-0.039V_d$	$0.062V_d$	$-0.08\ I_d$
13	$0.030V_d$	$0.052V_d$	$0.06\ I_d$
Total rms values	$0.41\ V_d$	$0.71\ V_d$	$0.82\ I_d$

Table 2.1 : Rms Values of Harmonics contained in Basic Current and Voltage Waveforms.

It is seen from Table 2.1 that the magnitude of the largest harmonic is 20% of that of the fundamental sinusoidal in each case and that the total rms values are about 5% greater than those of the fundamental components.

2.2 The Use of the Basic Three Phase Bridge Inverter with a Three Phase Synchronous Motor.

The technique for transferring power from a d.c. supply to an existent a.c. system using controlled rectifiers is well known and a fairly comprehensive theoretical analysis has been made of the process.[5]

An excited synchronous machine, when it is rotating, constitutes a three phase a.c. system. A brief description will now be given of an introductory investigation into the use of the basic bridge circuit in conjunction with a synchronous motor to provide a variable speed drive.

2.2.1 Circuit

Fig. 2.3 shows the circuit which was used for the investigation. The circuit was constructed from apparatus which was readily available and mismatching between the ratings of the various components was unavoidable.

The bridge circuit consisted of six thyratrons, each rated at 1000 V peak reverse voltage and 2.5 A mean forward current, and was therefore capable of converting a maximum of 7.5 A taken from the d.c. supply.

The synchronous motor was rated at 110 V, 30 A, 5.5 H P at 1500 r.p.m. A step down transformer was connected between the inverter and the motor so as to make more use of the ample voltage rating of the thyratrons. The transformer had 110 V windings on primary and secondary sides and was used with these star-connected on the inverter side and delta-connected on the motor side. The resulting step down ratio was thus $\sqrt{3} : 1$.

A very simple pulse generator, consisting of a three phase peaking transformer, was used for firing the thyratrons. To allow control over the position of the firing signal relative to the a.c. cycle the pulse

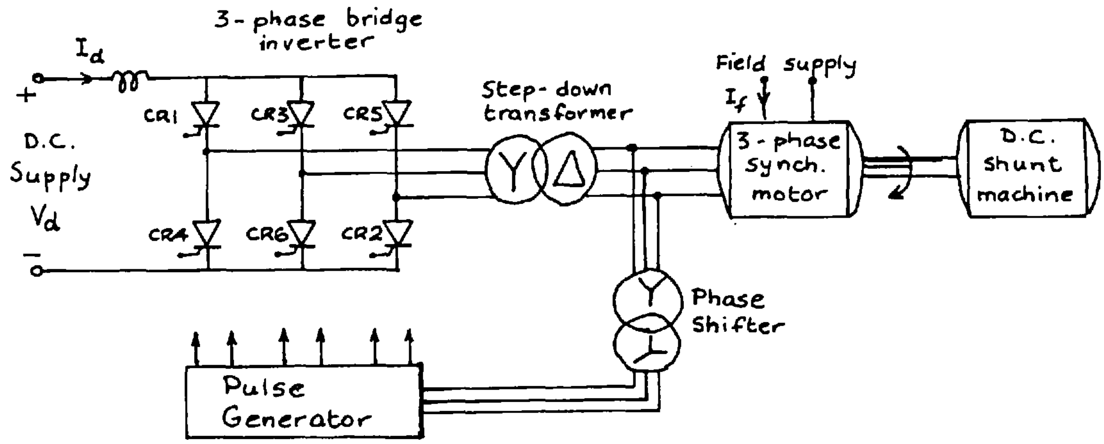


Fig. 2.3 : Circuit for inverter-fed synchronous motor.

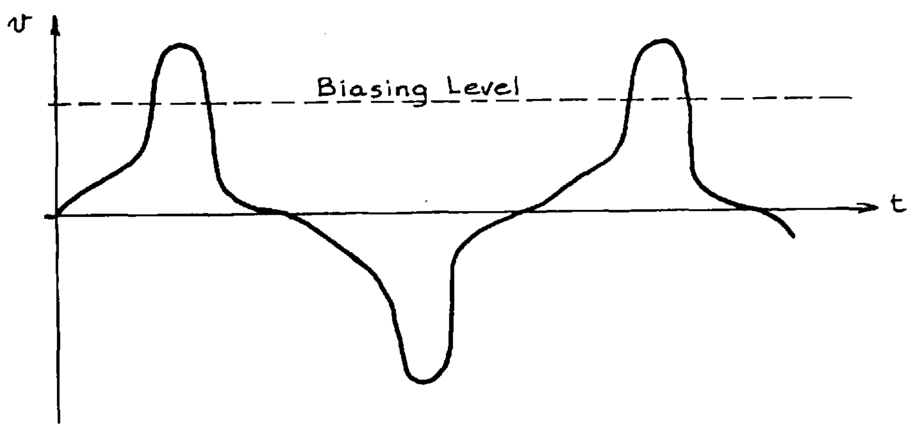


Fig. 2.4 : Form of output voltage waveform from peaking transformer.

generator was connected to the transformer through a phase shifter. The phase shifter was rated at 110 V and was therefore connected to the motor side of the transformer. A typical example of the peaking transformer output voltage waveform is shown in Fig. 2.4. An attenuator was connected between the pulse generator and the thyratron grid circuit. To ensure that the thyratrons were fired at the steepest rising part of the grid voltage waveform the grids were negatively biased individually by batteries.

A choke was connected in series with the d.c. supply to smooth the d.c. current and so to absorb the instantaneous differences between the steady d.c. supply voltage and the voltage appearing at the inverter input terminals.

The synchronous motor was coupled to a d.c. shunt mchine which was used for loading purposes and for running up the synchronous motor to a speed at which it could be connected to the inverter.

2.2.2 Principle of Operation.

When the excited synchronous motor is rotating it generates a set of three phase a.c. voltages. Fig. 2.5(a) shows these voltages as they appear at the inverter output terminals. The thyratrons are fired in sequence so that in general the d.c. supply is connected to the pair of a.c. lines with the greatest voltage difference. The "cross-over" points, at which the line-to-neutral voltages become equal near the firing points of the thyratrons, are marked X. It will be seen that if a thyratron is fired far enough ahead of the appropriate cross-over point,

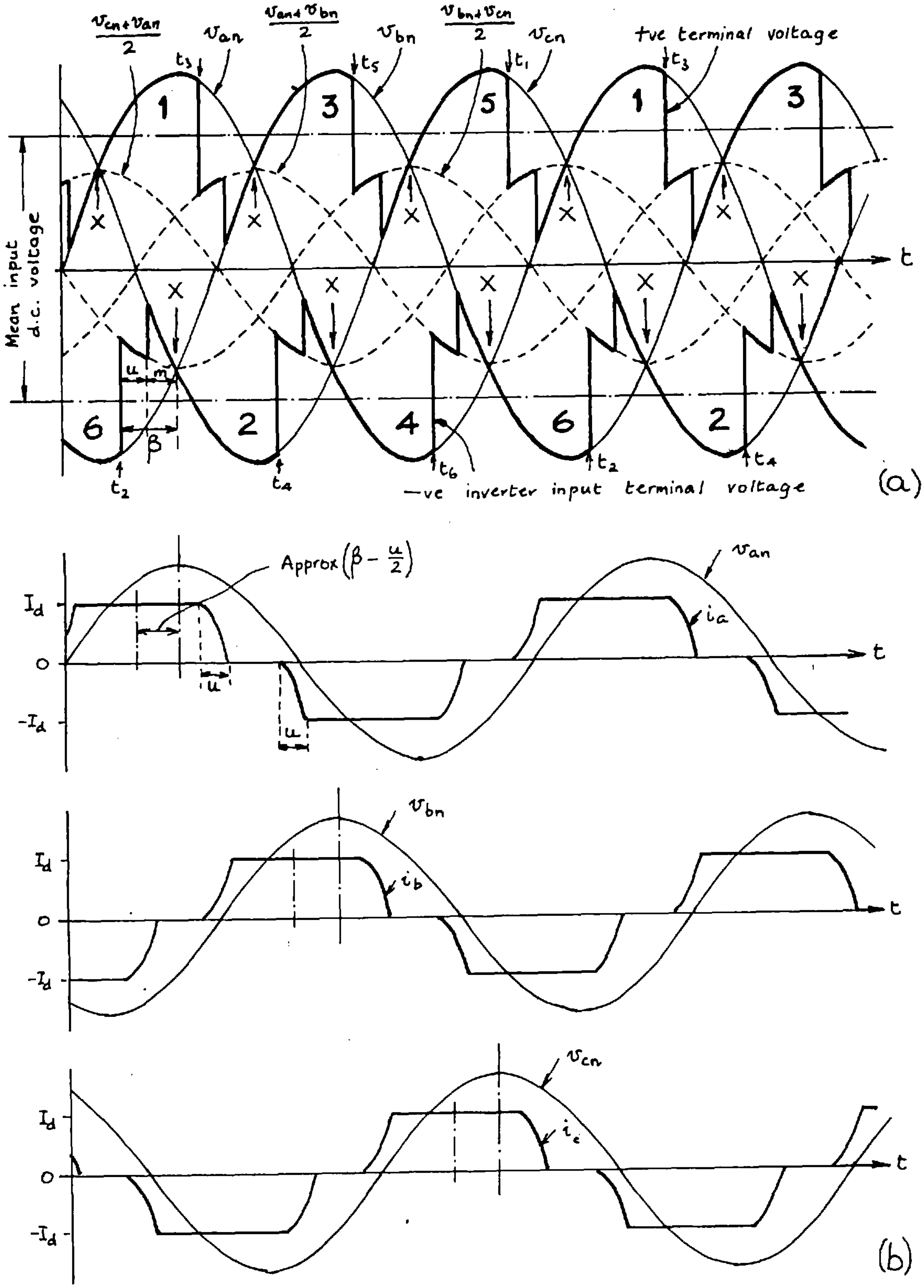


Fig. 2. 5 : Voltage and current waveforms for three phase bridge-connected inverter. (A.C. load.)

turn off of the conducting thyratron in the same row can be achieved.

t_1, t_2, ... t_6 are shown in Fig. 2.5(a) and are instants in the a.c. cycle at which CR1, CR2 ... CR6 are fired. Consider commutation between thyratrons CR6 and CR2 which occurs when CR2 is fired at instant t_2. If commutation were instantaneous, CR6 would at once be reverse biased by the difference between v_{bn} and v_{cn}, since the cathodes of CR6 and CR2 are connected together, and would turn off immediately. However, the inductance of the a.c. system prevents the current in CR6 from falling instantly to zero and a period of time, known as commutation overlap, elapses while i_b falls to zero and i_c increases from zero to the current on the d.c. side of the inverter. The overlap period is expressed as an electrical angle u . When the overlap period is complete CR6 becomes reverse biased until the cross-over point is reached whereupon the anode voltage become positive.

The time between the end of overlap and the cross-over point must be long enough to allow deionization of the thyratron with a certain safety margin. Hence the period by which the firing point is advanced from the cross-over point must be sufficient to allow for overlap, deionization and a safety margin.

i.e. $\beta > u + \delta + m$ where δ is the deionization time and the safety margin expressed as electrical angles.

The duration of the overlap period is determined by the current to be commutated, the a.c. system inductance, the magnitude and frequency of the a.c. voltage, and the value of β . During overlap the common voltage between the lines concerned and the neutral point is the mean of the two line-to-neutral voltages.

In Fig. 2.5(b) the individual line-to-neutral voltages and line currents are shown. Because the firing points of the thyratrons must be advanced from the cross-over points a fundamental feature of this type of inverter circuit is that power is delivered to the motor at a leading power factor. Consequently the synchronous motor, to accept the power supplied at a leading power factor and also supply the reactive power consumed by the transformer and phase shifter, etc., must be over-excited.

There is a relationship[5] between the d.c. supply voltage, the voltage at the motor terminal, the d.c. current, and β which determines the steady state condition of the system. This relationship can be derived by finding by integration the mean voltage appearing at the inverter input terminal and gives

$$V_d = 2.34\ Vp \cos\beta + 0.956\ \omega\, \ell_s\, I_d \qquad (2.1)$$

where Vp is the a.c. line-to-neutral voltage, $\omega = 2\pi f$ (where f is the a.c. frequency in $^c/s$) and ℓ_s is the effective series inductance per phase of the a.c. system. The last term in equation (2.1) indicates a voltage drop which is proportional to current but although it affects the mean d.c. voltage it is not a resistive voltage drop and does not represent any power dissipation. The voltage drop is entirely due to the effect of the inductance of the a.c. system in causing the overlap period during commutation.

Rearranging equation (2.1) to obtain V_p in terms of V_d,

$$V_p = \frac{V_d - 0.956\,\omega \ell_s I_d}{2.34 \cos\beta} \tag{2.2}$$

This is the equilibrium equation for the system. For any given values of V_d, β and I_d the motor will run at such a speed that the line-to-neutral voltage at its terminals is given by equation (2.2). Clearly this speed must be affected by the excitation of the motor and the effect of the motor current upon the motor voltage. To obtain the no-load speed, however, the second term in the numerator of equation (2.2) can be neglected in comparison with V_d and it can be assumed that on no load $V_p = k.I_f.N$ where k is a constant, I_f is the field current and N the speed of the synchronous motor. The following equation can then be obtained after eliminating V_p :-

$$N = \frac{V_d}{2.34\,kI_f \cos\beta}$$

or

$$N = \frac{K\,V_d}{I_f \cos\beta} \tag{2.3}$$

where K, another constant, $= \dfrac{1}{2.34\,k}$

It is seen that, in principle, the speed of the motor is proportional to V_d and inversely proportional to I_f and $\cos\beta$. In obtaining equation (2.3) it has been assumed that the current in the system is zero and that the magnetic circuit of the motor does not saturate.

2.3 No-Load Tests on System.

2.3.1 Test Conditions.

It was found in practice that the inverter was capable of supplying little more than the no-load losses of the combined synchronous and d.c. machines and hence the d.c. machine was used to supply the friction and windage losses. Consequently the results given are for a fictitious machine but indicate how a properly designed system would operate.

Because of the sensitivity of the peaking transformers to voltage and frequency the speed range over which the system could be tested was rather restricted. Even in the range covered some distortion in the shape and magnitude of the voltage applied to the thyratron grids was evident. For the same reason the d.c. supply voltage was maintained within a small range.

2.3.2 Open Circuit Magnetisation Curve of Synchronous Machine.

Fig. 2.6 shows the magnetisation curve of the synchronous machine. This curve is drawn to show phase voltage per r.p.m. plotted against field current and was obtained by driving the synchronous machine as a generator by means of the d.c. machine. From this curve the speed necessary at no-load to generate the required value of V_p for given values of V_d, β and I_f can be approximately determined.

It is seen from Fig. 2.6 that the synchronous machine showed a tendency to saturation at field currents greater than 30A.

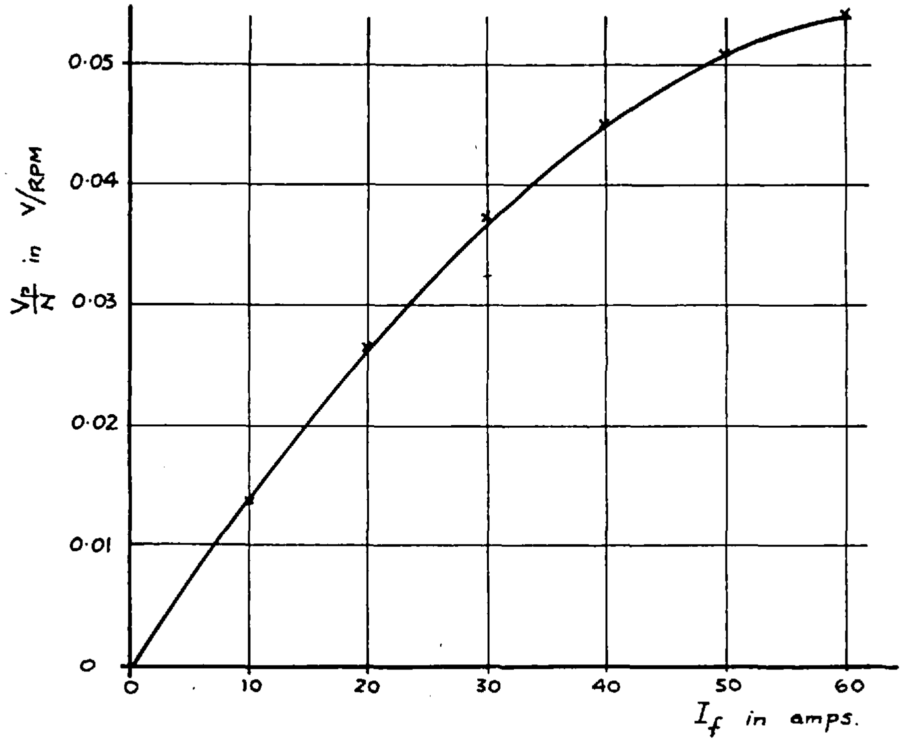


Fig. 2.6: Open circuit magnetisation curve of synchronous motor.

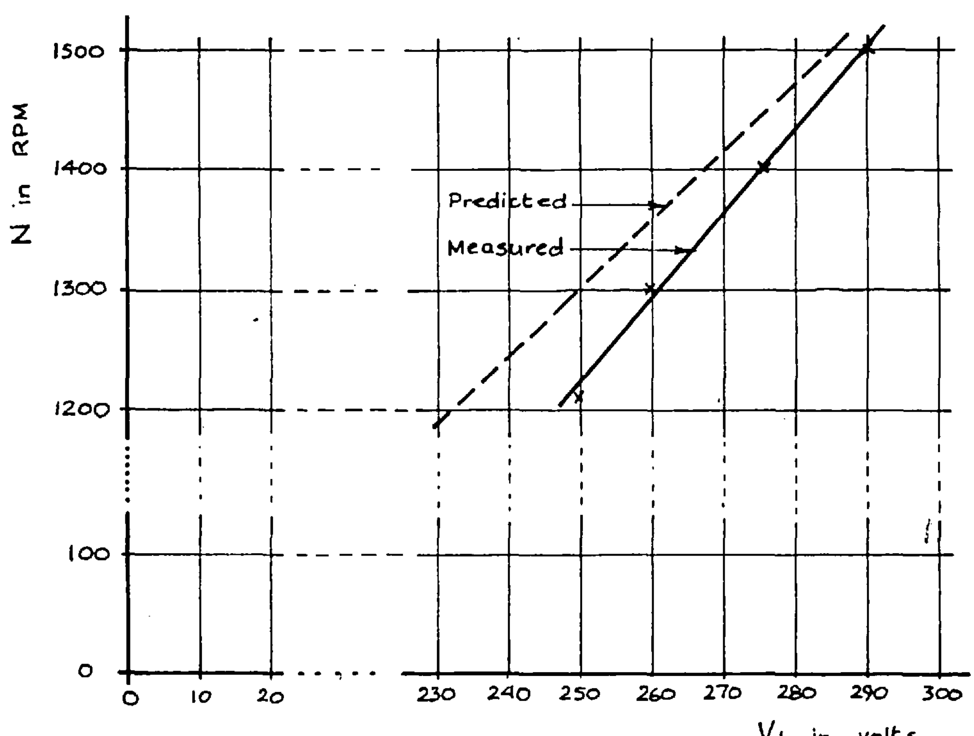


Fig. 2.7: Variation of no-load speed with V_d.
(I_f = 56A, β = 35°)

2.3.3 Variation of Speed with V_d.

Although the study of the system was made at a constant d.c. supply voltage some readings were taken at other supply voltages during the setting up procedure. The readings were taken with the d.c. machine disconnected from its supply and were not, therefore, no-load readings as defined in section 2.3.1 above.

In Fig. 2.7 the variation of speed with V_d is shown for one pair of values of I_f and β. For comparison the predicted variation of speed with V_d is shown on the same graph. The prediction has allowed for the thyratron voltage drops and, of course, the transformer ratio, but not the effect of the transformer and motor reactances. The measured speed is lower than predicted in consequence. Fig. 2.7 shows that the motor speed was proportional to V_d.

2.3.4 Variation of Speed with I_f and β.

Using a single value of V_d and several values of β in turn the variation of speed with I_f was measured. For each reading the speed was adjusted before measurement until the d.c. machine absorbed just enough power from its supply to account for the two machines' friction and windage losses.

Fig. 2.8 shows how the no-load speed varied with I_f and β and for comparison the corresponding predicted curves are also shown. Good agreement between measured and predicted results can be seen, showing that the no-load speed was inversely proportional to $\cos\beta$. The

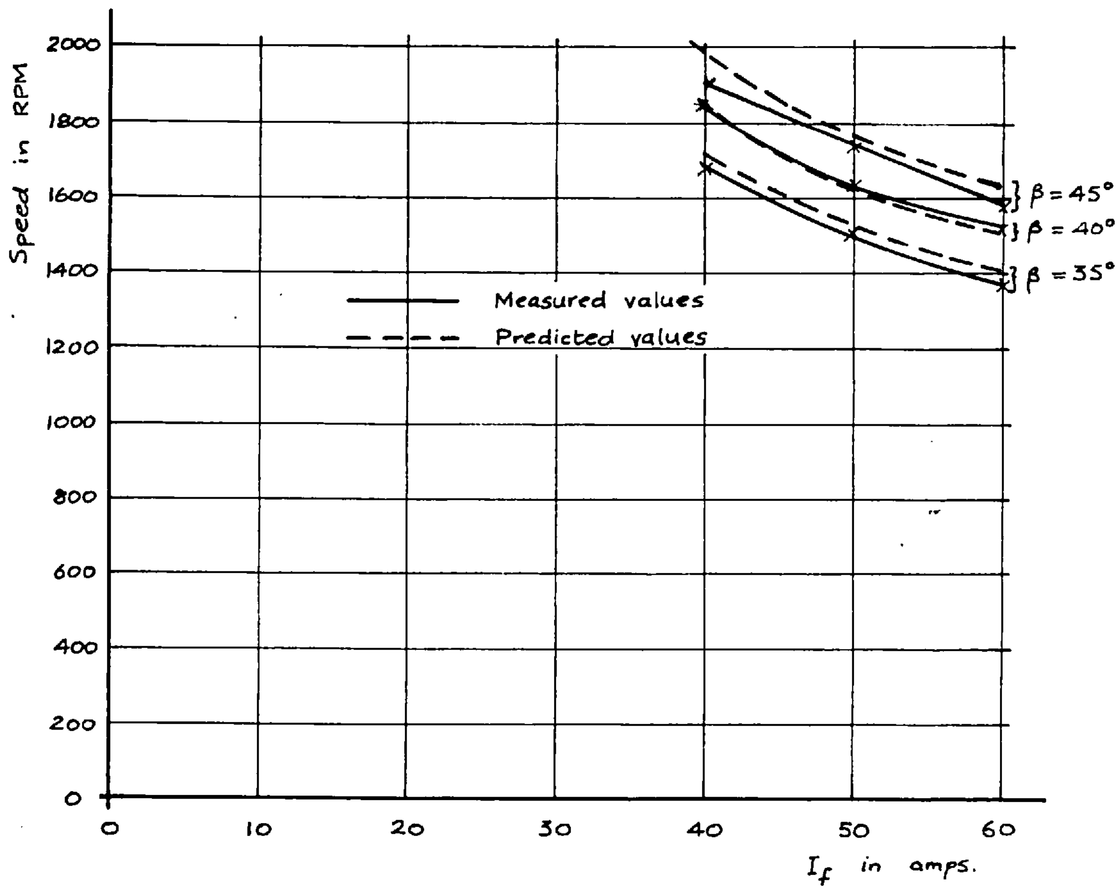


Fig. 2.8 : Variation of no-load speed with I_f and β.

(V_d constant at 280 v)

non-linearity of the magnetisation curve has been allowed for in the predictions and hence it can also be concluded that with an unsaturated machine the no-load speed would be inversely proportional to I_f.

2.4 Load Tests on System.

2.4.1 Test Conditions.

The d.c. supply voltage V_d was kept constant at 280 V throughout the load tests. The procedure adopted for the load tests was to adjust the speed until the d.c. machine absorbed just enough power from its supply to account for friction and windage losses. For each combination of I_f and β the power supplied to the d.c. motor was then reduced, and eventually reversed,until the inverter input current reached its safe limit. From the measurements made of the power absorbed or genrrated by the d.c. machine and its speed the gross torque developed by the synchronous motor was calculated.

2.4.2 Torque-speed Characteristics of the System.

The torque-speed characteristics obtained from the load tests are shown in Fig. 2.9. For I_f = 60 A these characteristics were much as would be expected, i.e. the speed falling slightly with load because of the voltage drop caused by the a.c. line reactance. For I_f = 50 A the speed fell or remained steady as torque was applied except for $\beta = 45^\circ$ when the speed showed a tendency to rise with increasing torque. When I_f was reduced to 40 A the increase in speed with load was even more marked. In fact the speed began to rise so rapidly at

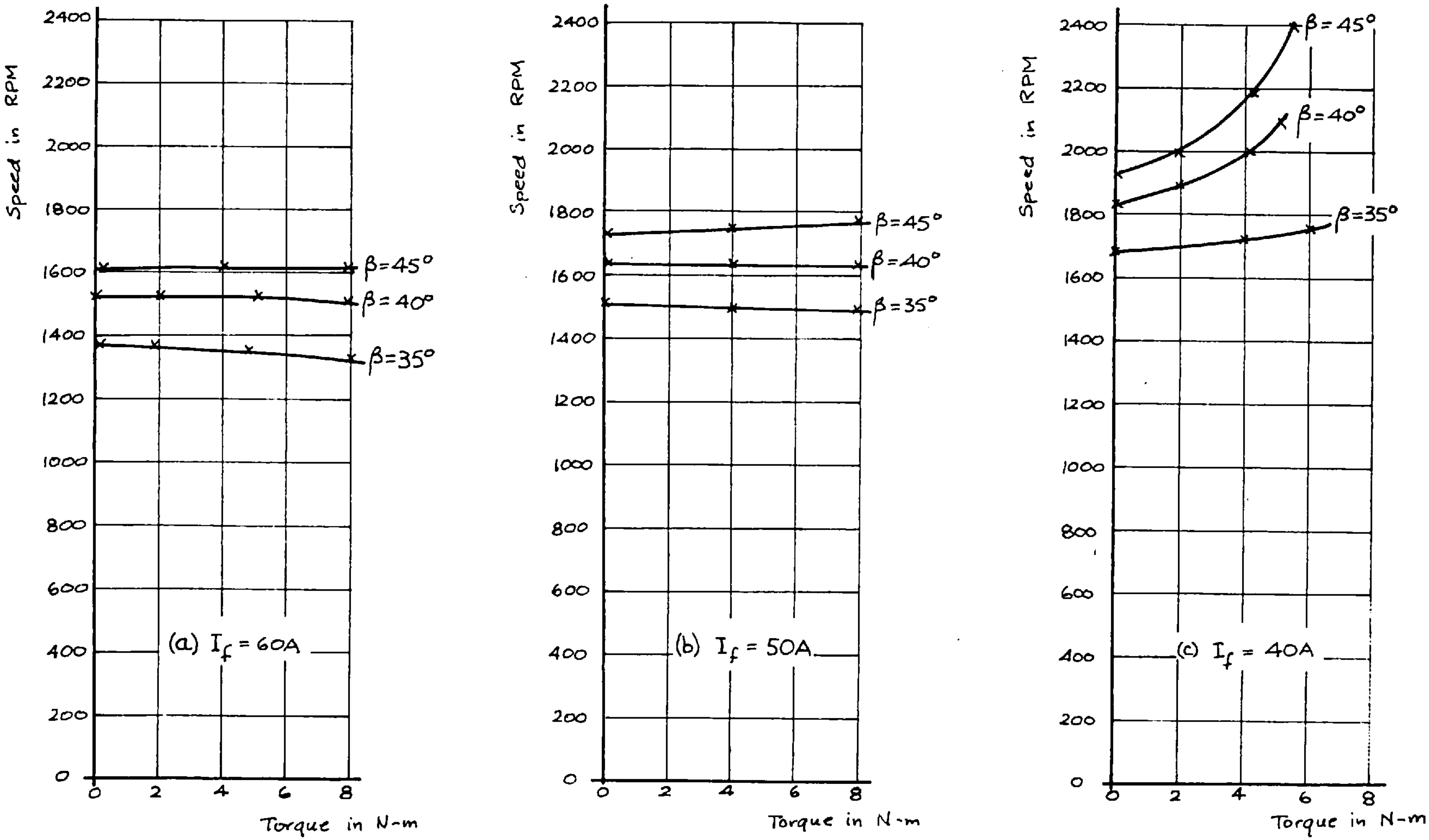


Fig. 2.9 : Torque-speed characteristics of inverter-motor system for constant inverter supply voltage of 280 V.

the higher values of β that the system became almost uncontrollable.

The main reason for the rising speed-torque characteristic is that the synchronous motor was, of necessity, operated at a leading power factor. Not only did it supply the reactive power demanded by the inverter but also the reactive power absorbed by the transformer and the peaking transformer circuit. Fig. 2.10 is a vector diagram for the synchronous motor in a typical condition. V_p and I are the motor terminal voltage and current with a phase angle ϕ leading, between them. E_o is the open circuit voltage which would be produced with the same speed and excitation. V_p is then the vector sum of E_o and $j\,X.I$ where X is the synchronous reactance of the motor (the motor resistance is neglected here).

If the motor load is increased slightly but the phase angle between terminal voltage and current kept constant (as is approximately the case when β is kept constant), I increases by a small amount Δ I as shown. The new value for V_p, i.e. $V_p + \Delta V_p$, is obtained by drawing a vector to represent $j\,X\,(I + \Delta I)$ parallel to the $j\,X\,I$ vector and joining the V_p reference line with the circle which is the locus of the E_o vector. It can be seen that the value of V_p is reduced and the load angle δ is also reduced. However, since β is unchanged, V_p must return to its original value for equilibrium to be restored and can only do so if the motor speed increases. For a given value of Δ I, ΔV_p is clearly greater when X is greater or when ϕ is nearer to 90°. X is proportional to frequency and hence speed and therefore the speed shows a greater tendency to rise with load at lower values of I_f. ϕ is almost equal

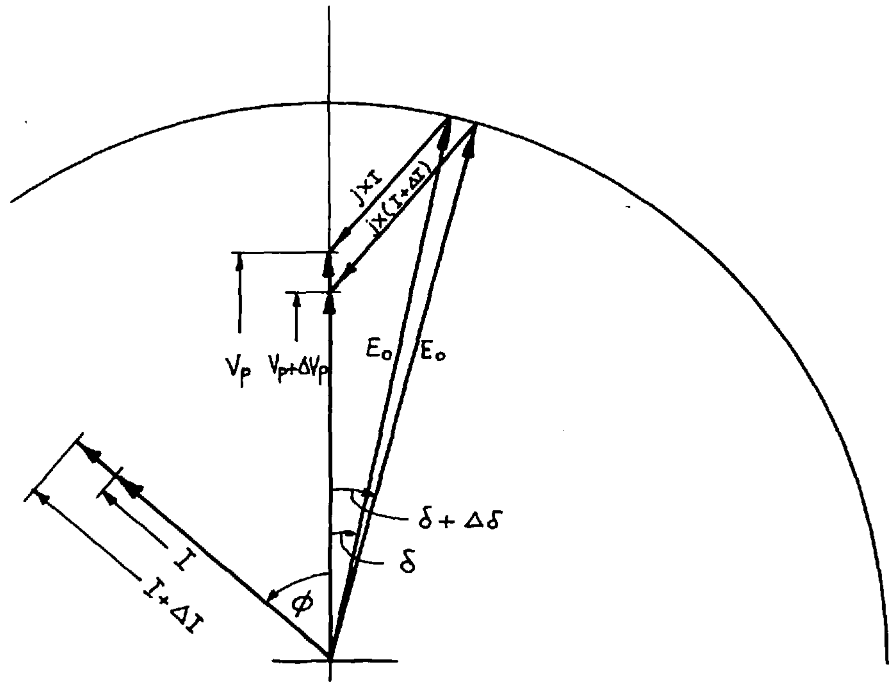


Fig. 2.10 : Vector diagram for the synchronous motor under a typical condition of operation.

to β and hence the speed tends to increase more when β is increased.

Countering the tendency for the motor speed to rise with load is the voltage drop caused by the reactance of the a.c. circuit. At $I_f = 60$ A the tendency for the motor speed to fall with load is obviously dominant, while at $I_f = 50$ A the two effects cancel each other nearly. At $I_f = 40$ A the tendency for the speed to rise is much more dominant.

Other factors which could have affected the speed-torque characteristics of the system are the changes in voltage and frequency applied to the pulsing circuit and the phase shift across the step down transformer. The changes in voltage and frequency did cause some distortion of the thyratron grid voltage waveform and so altered the firing point. However, the voltage and speed ranges were restricted so as to minimise this effect and it can be treated as a secondary effect. The phase shift introduced by the step down transformer was very small and can be neglected.

2.4.3 Power Factor and Efficiency.

Fig. 2.11 shows how the motor power factor varied with load when I_f was 50 A. The motor supplied the reactive power absorbed by the transformer and pulsing circuit and at light load the power factor was, therefore, very low. However, as load was applied the flow of power from the inverter, operating at almost constant power factor, caused the motor power factor to improve. The inverter power factor depended upon the values of β and u, the fundamental component power factor being approximately cos $(\beta - \frac{u}{2})$. Allowing for an average value of 5°

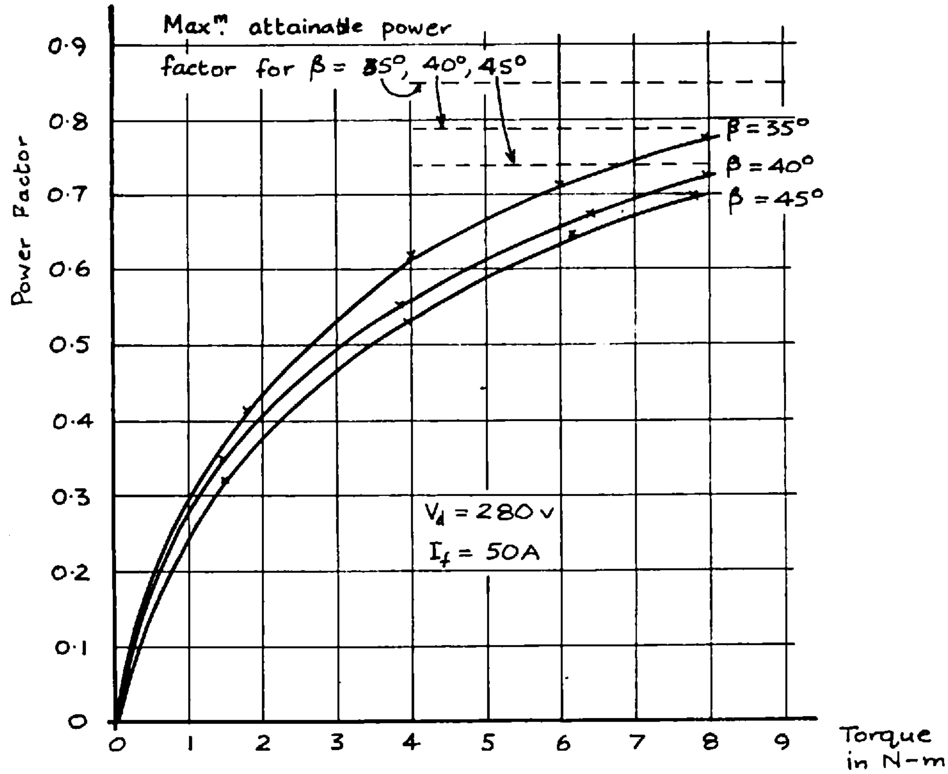


Fig. 2.11: Variation of motor power factor with load for typical condition.

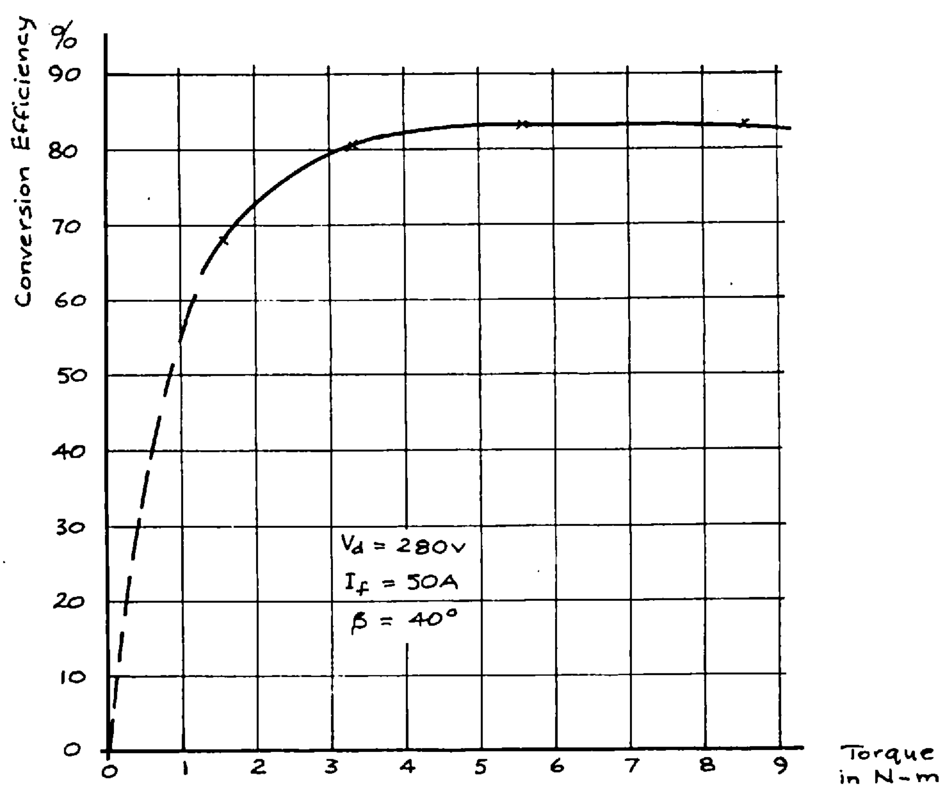


Fig. 2.12 : Variation of overall conversion efficiency with load for a typical condition.

for u the maximum attainable power factors, on this basis, for $\beta = 35^{\circ}$, 40° and 45° could have been 0.85, 0.79 and 0.74 respectively. These values are shown on Fig. 2.11 but it is realised that they are approximate because of the harmonic content of the inverter output current waveform.

Fig. 2.12 shows the variation of conversion efficiency with load. The conversion efficiency is defined as the ratio of gross mechanical power developed by the motor (before friction and windage losses are deducted) to total inverter input power. The curve shown is drawn for $I_f = 50$ A and $\beta = 40^{\circ}$ but is typical of the nine combinations of I_f and β studied.

The electrical power supplied to the inverter was consumed in four ways:-

(a) conversion by the motor into mechanical power

(b) supplying the almost constant power losses in the transformer and pulsing circuit

(c) supplying the losses in the thyratrons, these losses being a constant percentage loss of efficiency since the d.c. supply voltage and the arc drops were constant

(d) supplying the I^2R losses in the circuit, these losses being approximately proportional to the square of the inverter input current and hence also inverter input power.

It would therefore be expected that the efficiency would be low at light load because of the constant losses, rise to a maximum value and then fall away as the I^2R became significant. The maximum recorded efficiency was about 83%. Of the 17% percentage loss 9% could be attributed to the thyratron losses, each arc drop being about 12 V.

2.4.4 Limits of Operation.

Several limits of operation were observed in the course of the investigation. The first concerns the firing angle β. When β was increased above approximately 40° the speed-torque characteristic of the system began to rise, tending to make the system unstable. When, on the other hand, β was reduced below about 35° the thyratrons began to mis-fire resulting in a breakdown of inversion. This was because the deionization time of the thyratrons represented an electrical angle of about 20° at a speed of 1500 r.p.m., and the smaller the value of β the longer the overlap process of commutation. The safety margin, i.e. $(\beta - \delta - u)$, therefore decreased very rapidly when β was reduced below 35°.

Secondly it was found that the field current had to be kept as high as possible to make the system stable under all conditions. When I_f was reduced below about 50 A the speed-torque characteristics began to rise very sharply.

The current which the inverter could commutate and hence the power handling capacity of the inverter was restricted but depended on the value of β. The higher the value of β the longer was the time allowed for overlap and hence the greater was the current that could be commutated safely.

The upper speed limit was not investigated but it is clear that at the higher speeds the deionization time of the thyratrons would occupy a greater proportion of the a.c. cycle and β would have to be increased for safe commutation. The lower speed limit was also not investigated but it was clear that the system was capable of running at lower speeds than those studied. Redution of the d.c. supply voltage would be necessary at lower speeds. It is very doubtful whether the inverter could have functioned at very low speeds, and it is almost certain that the motor could not be started from standstill, because of the lack of any generated a.c. voltage for turning off the thyratrons.

Finally automatic regeneration was not possible with the system. If the motor were to be driven above the set no-load speed, no current would flow through the inverter and the motor would free-wheel. It would be possible to arrange for regenerative braking by advancing the firing pulses by nearly half a cycle and reversing the polarity of the d.c. supply. It would also be possible to arrange for rheostatic braking by connecting a resistor in place of the d.c. supply and advancing the firing pulses by nearly half a cycle. In each of these two cases the inverter would then operate as a rectifier.

2.5 Conclusions.

The investigation into the inverter-fed synchronous motor was carried out as an introduction to the subject of motor speed control by means of controlled rectifiers. For this reason it was far from comprehensive. Despite this, several useful conclusions may be drawn from the tests which were carried out on the system.

It has been demonstrated that even the simplest form of the three phase bridge inverter can be used for producing a variable speed drive. The simplicity and the efficiency of the system were its main virtues.

Although it was found that the motor speed could be controlled by adjusting the motor field current I_f and the rectifier firing angle β it is considered that speed control would best be achieved by variation of the d.c. supply voltage. β should then be maintained at the smallest value compatible with safe commutation.

It was found that the system as used possessed characteristics similar to those of a d.c. shunt motor. This could be expected since the rectifiers performed a function similar to that of the commutator of a conventional d.c. machine (in the case studied the commutator would have had three segments) and were, in effect, fired when the rotor passed through six distinct positions in each revolution. By connecting the field winding in series with the inverter at its input terminals it would be possible, in principle, to give the system a series motor type of speed-torque characteristic.

Because of the characteristics of the inverter the motor was forced to operate at a leading power. If S C Rs had been used in place of thyratrons, it is clear that the power factor could have been improved because of the S C R's much shorter turn off time. Commutations overlap would still have to be catered for, however, and the system would still possess an inherently rising speed-torque characteristic. In general this would be an undesirable feature but could probably be corrected to a large extent by compounding the motor field.

The system proved to be very susceptible to transient load or voltage surges. The current in the inverter depended upon the difference between the d.c. supply voltage and the counter-voltage generated by the motor. A small increase in the d.c. supply voltage or a reduction in motor speed could result in a large enough current surge for commutation to fail. Clearly some method of maintaining the safety margin, e.g. by quickly increasing β when an increase in current is detected, would be required in practice.

The system could not be started from standstill, neither could it run at very low speeds. Unless these obstacles could be overcome the system would have a very limited practical application.

The field current was fed into the motor by means of sliprings and brushgear. One of the important features of a variable speed motor control using S C Rs should be the elimination of all sliding contacts.

The analysis of motor performance is usually based upon the fundamental sinusoidal components, and higher harmonics, of the motor voltage and current, whereas rectifier circuit analysis is based upon instantaneous values of current and voltage. It is clear, therefore, that conventional machine theory is incompatible with conventional rectifier circuit theory and that new methods of analysis must be developed.

CHAPTER 3.

THE THREE PHASE BRIDGE-CONNECTED INVERTER WITH A SIMPLE FORM OF ARTIFICIAL COMMUTATION.

As a result of the preliminary investigation outlined in Chapter 2 it was decided to concentrate upon the problems associated with the use of a variable frequency inverter to feed an induction motor. Such a scheme would meet many of the objections to the synchronous motor scheme. For instance, no sliding contacts would be necessary if a squirrel cage motor were to be used and the system would not be so susceptible to voltage and speed transients. A sudden increase in the d.c. supply voltage would produce a proportional increase in current instead of a large current surge as in the synchronous motor scheme.

To produce a torque in the induction motor the frequency of the alternating current generated by the inverter must be such that the motor's synchronous speed, or field flux rotating speed, is greater (for motoring) or less (for braking) than its actual speed. Hence the inverter output frequency would not be tied exactly to the motor speed as in the synchronous motor scheme.

In the simple induction motor scheme the inverter would not be able to use any voltage generated by the rotating motor for turning off the controlled rectifiers and it would have to employ instead some form of forced or artifical commutation. In this chapter some tests on the basic three-phase bridge inverter using S C Rs with a simple form of artificial commutation are described. The inverter circuit used was adapted from the basic single phase parallel inverter circuit shown in most S C R manuals, [1,2,3] the three phase bridge being a logical development.

3.1 Circuit and Principle of Operation into a Resistive Load.

The first circuit adopted for the inverter was as shown in Fig. 3.1. To the basic three-phase bridge have been added only the three capacitors C, one connected between each pair of inverter output terminals, and damping circuits (not shown in Fig.3.1) consisting of a small capacitor in series with a resistor were connected across each rectifier to suppress voltage transients. The rectifiers in this circuit were S C Rs and were triggered by pulses from a transistor pulse generator. The pulse generator was driven by a signal at a frequency 6f from a master oscillator and fed a pulse to each S C R in turn at a repetition frequency f. The inverter output frequency was thus determined by the setting of the master oscillator frequency.

In the circuit shown the function of the capacitor is to turn off each conducting S C R when the next S C R in the same row is triggered. Consider the sixth of a cycle between instants t_1 and t_2 in which CR6 and CR1 conduct. If by the end of the period all transients have died away, the distribution of voltage aroundthe circuit immediately before instant t_2 is as shown in Fig. 3.2. Current flows in CR1, phase A, phase B, and CR6 and the supply voltage is shared equally between phases A and B. The anode-cathode voltage of CR2 is therefore $\frac{1}{2}V_d$. At instant t_2 CR2 is triggered

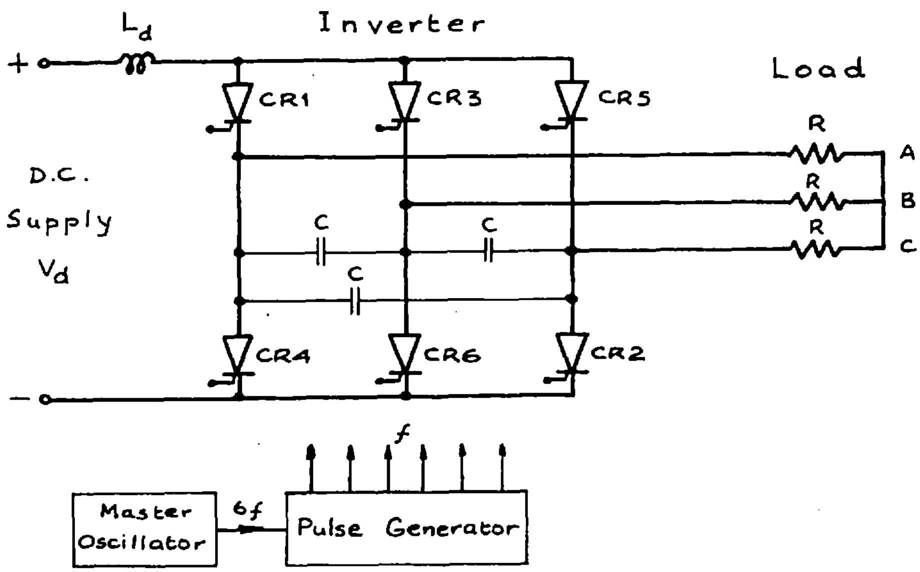


Fig. 3.1 : Basic three phase inverter with simple form of artificial commutation.

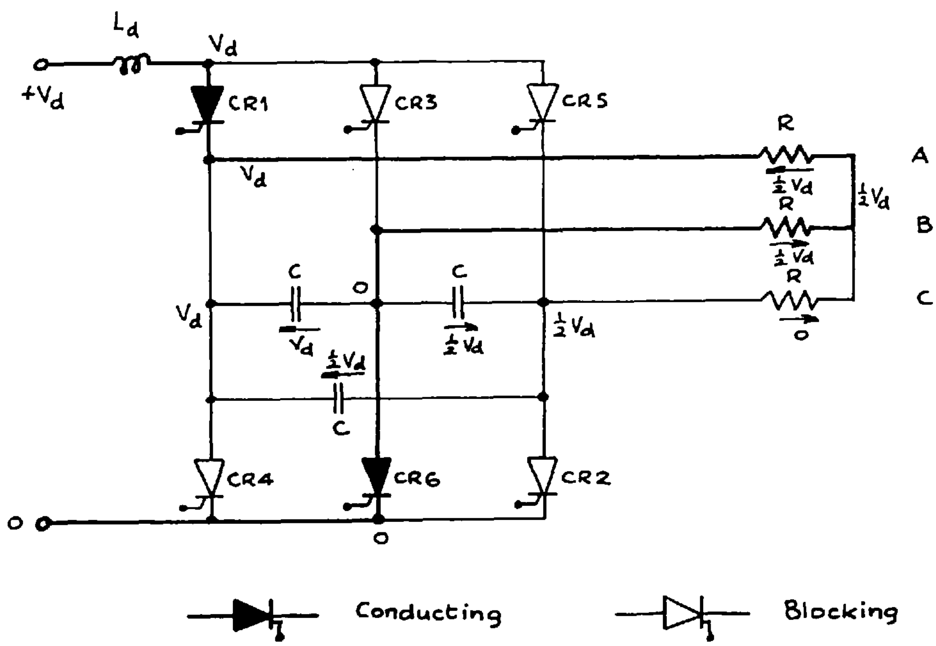


Fig. 3.2 : Voltage distribution around circuit immediately before instant t_2.

and its anode-cathode voltage falls instantly almost to zero. The capacitors cannot discharge instantly since all possible discharge paths include resistance or inductance. At instant t_2, therefore, the anode-cathode voltage of all the S C Rs in the bottom row fall instantly by $\frac{1}{2}V_d$. That of CR4 falls from V_d to $\frac{1}{2}V_d$ but that of CR6, which had been zero previously, now becomes $-\frac{1}{2}V_d$ and CR6, therefore turns off. Provided that during the re-charging of the capacitors to their new steady-state voltages the anode-cathode voltage of CR6 remains negative for longer than the turn-off time, CR6 stays off when forward voltage is reapplied.

During the next sixth of a cycle CR1 and CR2 conduct until CR3 is triggered, at which instant CR1 turns off by a method similar to that described above. Commutation between the other phases and S C Rs at the other triggering instants is effected in exactly the same way. The commutation process has the effect of distorting the basic current and voltage waveforms shown in Fig. 2.2, each sudden change in current or voltage becoming an exponential change.

3.2 Tests with Resistance Load.

Some tests were carried out on the inverter with a purely resistive load. The purpose of these tests was to gain a clear understanding of the inverter in its simplest mode of operation and to find a suitable method of analysis for the circuit. A sample calculation of the waveforms of current and voltage in the circuit is given below and the predicted results are compared with those obtained by experiment.

3.2.1. Test Conditions

At frequencies low enough for all commutation transients to die away in each sixth of a cycle the current and voltage waveforms were very similar to those given in Fig. 2.2 as the basic bridge circuit waveforms. All the sudden changes in current and voltage, however, had become distorted to exponential or oscillatory changes. For these conditions the current in the choke L_d and the voltages on the capacitors C at the beginning of each cycle were easily found, being their steady state values.

At higher frequencies it could not be assumed that the circuits and voltages had reached their steady state values and it was therefore necessary to calculate these values before predicting the waveforms. A sample calculation is given for a high frequency condition and shows how the initial values of current and voltage can be derived.

The conditions for the calculation were as follows:-

$$V_d = 36 \text{ v} \;,\; L_d = 0.25 \text{ H} \;,\; C = 8 \mu\text{F}$$
$$R = 18\,\Omega \;,\; f = 333^c/s \,.$$

A frequency of $333^c/s$ was chosen for convenience in dividing the cycle into six equal parts.

3.2.2. Current and Voltage Equations for One Sixth of a Cycle.

In appendix A the equations for the currents and voltages in the circuit are derived for the sixth of a cycle between instants t_2 and t_3.

The initial values, I_o of the current in the choke L_d, and E_1, E_2, E_3 of the voltages v_{ab}, v_{eb}, v_{ac} at the instant t_2 are obtained from equations (A.18), (A.22) and (A.23). On reducing these equations to linear simultaneous equations in I_o, E_1 and E_3 by the method described in section A.2.2 of appendix A and solving, the following values are obtained:-

$$I_o = 1.96 \quad A$$

$$E_1 = 52.7 \quad V$$

$$E_3 = 41.1 \quad V$$

$$\therefore \quad E_2 = E_1 - E_3 = 11.6 \text{ V}$$

Using these initial values in the equations (A.18) and (A.22) to (A.27) derived in appendix A the following voltage and current equations may be obtained:-

(A.18)... $$i_1 = 1 - 0.123e^{-2.16\times10^3 t} + 1.086e^{-0.15\times10^3 t} \qquad (3.1)$$

(A.22)... $$v_{ac} = 36 - 66.25e^{-2.16\times10^3 t} + 41.88e^{-0.15\times10^3 t} \qquad (3.2)$$

(A.23)... $$v_{bc} = 18 - 33.12e^{-2.16\times10^3 t} + 20.94e^{-0.15\times10^3 t} - 46.93e^{-2.3\times10^3 t} \qquad (3.3)$$

(A.24)... $$v_{ab} = 18 - 33.12e^{-2.16\times10^3 t} + 20.94e^{-0.15\times10^3 t} + 46.93e^{-2.31\times10^3 t} \qquad (3.4)$$

(A.25)... $$i_a = 1 - 1.840e^{-2.16\times10^3 t} + 1.164e^{-0.15\times10^3 t} + 0.869e^{-2.31\times10^3 t} \qquad (3.5)$$

(A.26)... $$i_b = -1.738e^{-2.3\times10^3 t} \qquad (3.6)$$

(A.27)... $$i_c = -1 + 1.840e^{-2.16\times10^3 t} - 1.164e^{-0.15\times10^3 t} + 0.869e^{-2.3\times10^3 t} \qquad (3.7)$$

i_1 is the current taken from the d.c. supply. In the above equations currents are in amperes, voltages in volts, time in seconds.

3.2.3. Derivation of Waveforms from Equations for One Sixth of a Cycle.

From the equations obtained in section 3.2.2 the complete inverter input and output waveforms may be derived. This is possible because positive and negative half cycles of the generated a.c. are identical and the a.c. cycles for each of the load phases are identical but for a displacement of a third of a cycle. Hence every part of each waveform is described by one of the equations obtained in section 3.2.2.

(a) Inverter input voltage waveform.

Between instants t_2 and t_3 CR1 and CR2 conduct and the input voltage must vary in the same way as v_{ac}. This variation is repeated in every sixth of a cycle and the input voltage waveform is therefore as shown in Fig. 3.3(a).

(b) Inverter input current waveform.

Between instants t_2 and t_3 the value of the inverter input current at any instant is given by the equation for i_1. This variation is repeated in every sixth of a cycle and hence the inverter input current waveform is as shown in Fig. 3.3(b).

(c) Inverter output line-to-line voltage waveforms.

Between instants t_2 and t_3 the instantaneous values of the line-to-line voltages are given by the equations for v_{ac}, v_{bc} and v_{ab}. It is easily seen that the variation in v_{ac} between t_2 and t_3 is repeated for v_{bc}, v_{ba}, v_{ca}, v_{cb}, v_{ab} in the sixths of a cycle

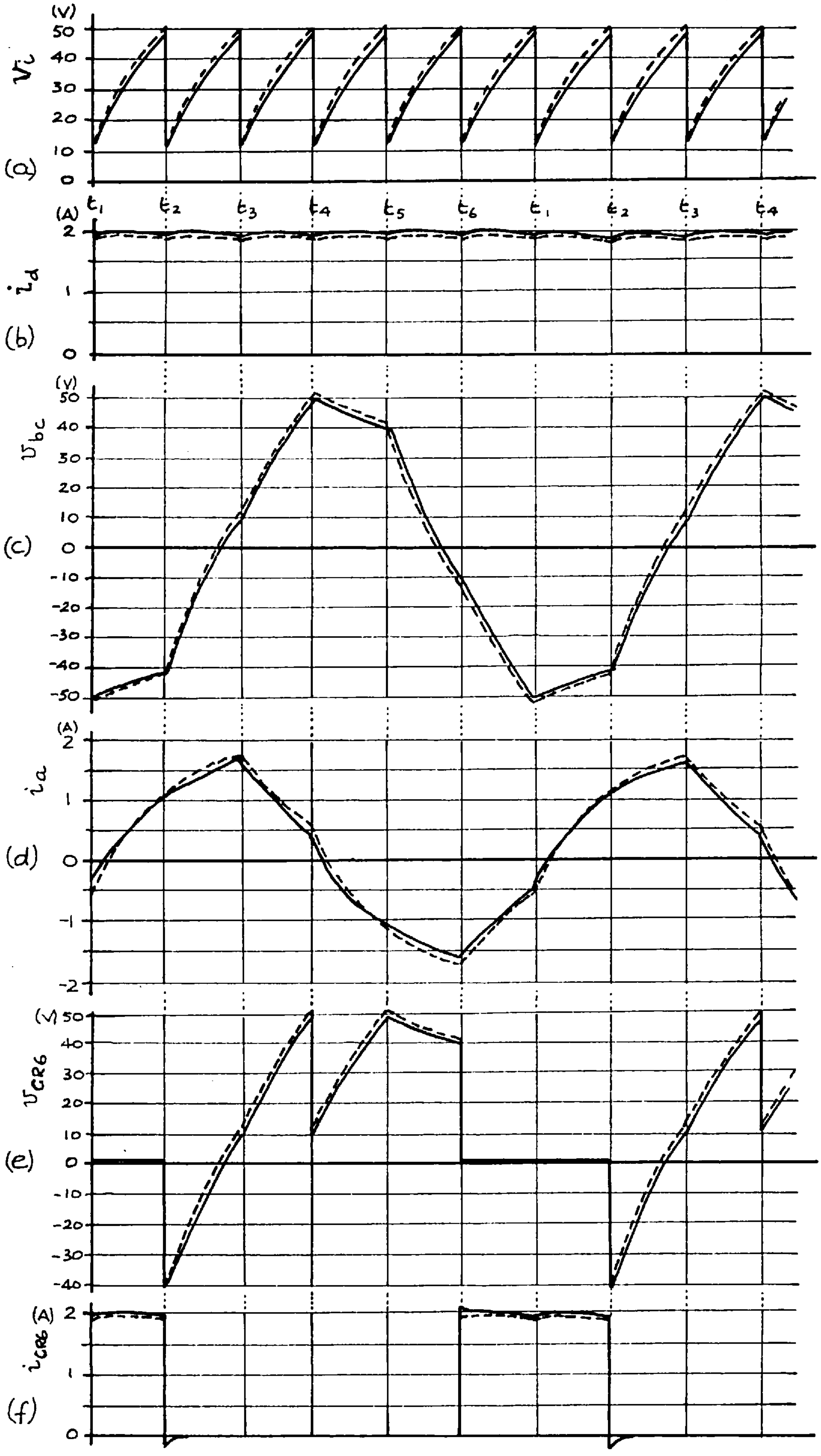


Fig. 3.3: Current and voltage waveforms for resistive load.

commencing at instants t_3, t_4, t_5, t_6, t_1 respectively. It can also be seen that the values of v_{ac} at any instants in the sixth of a cycle commencing at t_2, t_3, t_4, t_5, t_6, t_1 are given by the equations for v_{ac}, v_{ab}, $-v_{bc}$, $-v_{ac}$, $-v_{ab}$, v_{bc} respectively which are valid between t_2 and t_3, provided that t is set equal to zero at the start of each sixth of a cycle. The complete waveform for v_{ac} can therefore be obtained from the equations in section 3.2.2 and is shown in Fig. 3.3(c).

The waveforms for the other line-to-line voltages may be found in a s imilar manner.

(d) Inverter output current waveforms.

The values of the output currents in the sixth of a cycle commencing at instant t_2 are given by the equations for i_a, i_b, i_c. By an argument similar to that in (c) above it can be shown that in the sixths of a cycle commencing at the instants t_2, t_3, t_4, t_5, t_6, t_1 the values of i_a are given by the equations for i_a, $-i_c$, i_b, $-i_a$, i_c, $-i_b$ respectively which are valid between t_2 and t_3. The complete waveform for i_a can therefore be derived from the equations in section 3.2.2 and is shown in Fig. 3.3(d).

The waveforms for the other output currents may be found in a similar manner.

(e) S C R voltage waveform.

Between the instants t_6 at which it is fired and t_2 at which it is turned off CR6 conducts and hence $v_6 = 0$.

Between t_2 and t_3 CR1 and CR2 conduct and hence $v_6 = v_{bc}$.

Between t_3 and t_5 CR3 conducts and hence v_6 is equal to the inverter input voltage whose waveform is shown in Fig. 3.3(a).

Between t_5 and t_6 CR4 and CR5 conduct and consequently $v_b = v_{ba}$. However, the variation of v_{ba} between t_5 and t_6 is the same as the variation of v_{ab} between t_2 and t_3 which is given by the equation for v_{ab} in section 3.2.2.

Hence it is possible to derive the complete voltage waveform for CR6 from the equations in section 3.2.2 and it is shown in Fig. 3.3(e).

The voltage waveforms for the other S C Rs may be obtained in a similar manner, all being similar to that of CR6 but delayed by the appropriate number of sixths of a cycle.

(f) S C R current waveform.

CR6 does not conduct between instants t_2 and t_6 and hence the current flowing in it is zero. Between t_6 and t_2 CR6 conducts and is the only S C R which conducts during this period in the lower row. Hence between t_6 and t_2 the current in CR6 is the inverter input current and its waveform is shown in Fig. 3.3(f).

3.2.4. Mean and rms Values of Voltage and Current.

It has been seen that the value of any current or voltage in the circuit at any instant can be found from one of the equations in section 3.2.2. Consequently the mean or rms value of any current or voltage can be found by integrating the appropriate equations or by applying Simpson's rule to the values obtained for plotting the waveforms.

(a) Mean d.c. curren I_d.

The mean d.c. durrent I_d can be obtained by finding the mean value of i_1 over one sixth of a cycle.

$$\text{i.e.} \quad I_d = \frac{10^6}{500} \int_0^{500\times10^{-6}} (1 - 0.123e^{-2.16\times10^3 t} + 1.086e^{-0.15\times10^3 t})dt$$

$$= \underline{1.97\ A}$$

(b) Rms output line current I_ℓ

The rms value I_ℓ of the output line current can be found by squaring all the calculated values of i_a, i_b, i_c over one sixth of a cycle, finding the mean square value by Simpson's Rule, and then taking the root mean square value.

Thus $I_\ell = \underline{1.15\ A}$

(c) Rms output line-to-line voltage V_ℓ

The rms value V_ℓ of the output line-to-line voltage can be found by Simpson's Rule after squaring all the calculated values of v_{ac}, v_{bc}, v_{ab} as in (b) above)

Then $V_\ell = 36.0$ V.

(d) Effect of S C R forward voltage drop.

The voltage and current equations were derived in appendix A on the assumption that the S C Rs had zero voltage drop when conducting. In fact the voltage drop is almost constant at about 1 volt. Since two S C Rs are conducting in series at all times the effect of the

S C R voltage drop can be allowed for approximately by multiplying the mean and rms values of current and voltage by a factor

$\frac{V_d - 2}{V_d}$, i.e. $\frac{34}{36}$ in the case considered.

Applying this correction factor the values of I_d, I_ℓ, V_ℓ become

$$I_d = 1.86 \text{ A}$$

$$I_\ell = 1.09 \text{ A}$$

$$V_\ell = 34.0 \text{ V}$$

3.2.5 Comparison between Predicted and Measured Results.

A comparison between the predicted and the measured results is made on the basis of waveforms, the mean and rms values of current and voltage, and the values of δ .

(a) Waveforms.

In Fig. 3.3 the predicted and measured waveforms are compared by plotting the theoretical waveforms on the same axes and to the same scale as tracings of oscillograms obtained experimentally. It can be seen that agreement between the two sets of waveforms for the current in an S C R (Fig. 3.3 (f)). At turn-off a short peak of reverse current flows in each S C R and this is shown in the measured waveform but not, of course, in the predicted waveform. The same current flows into the S C R which is turned on at the same time and is superimposed upon the current which flows into or from the d.c. supply.

(b) Means and rms values.

The predicted mean and rms values of voltage and current, after applying the correction factor to take into account the S C R forward voltage drop, may be compared directly with instrument readings noted during actual operation. The values given in brackets following are the predicted results

$$I_d = 1,97 \text{ A } (1.86 \text{ A})$$

$$I_l = 1.05 \text{ A } (1.09 \text{ A})$$

$$V_l = 32.5 \text{ V}(34.0 \text{ A})$$

(c) Values of δ .

The predicted value of δ is obtained from the S C R voltage waveform of Fig. 3.3 (e). δ is the time for which the S C R is reverse biased at turn off. δ can also be measured experimentally with an oscilloscope. The value of δ given in brackets is the predicted value.

$$\delta = 350 \ \mu \text{Secs } (330 \ \mu \text{Secs})$$

(d) Accuracy of prediction.

From the above results it can be seen that the predictions are accurate to within about 5%. The errors introduced by neglecting minor circuit components, such as transient suppressing capacitors and resistors, and by the assumptions made in formulating the theory in Appendix A would probably account for between 1% and 2% of the discrepancy. The remainder can be attributed to experimental error.

3.2.6 Determination of the Required Value of C.

The function of the capacitors C is to turn off the S C Rs when they have conducted for a third of a cycle. The capacitors achieve this by causing the S C Rs to be reverse biased for a time δ which must be greater than the turn off time of the S C Rs.

In Fig. 3.3 (e) an S C R voltage waveform is shown and the time δ is the time between the end of conduction and the instant at which the anode voltage becomes positive. The variation of voltage over this part of the S C R waveform is given by the equation for v_{bc} derived in Appendix A. In this equation $t = \delta$ when $v_{bc} = 0$. However, it is impossible to obtain a solution for δ from this equation, except by a numerical method, and so it is not possible to obtain an accurate expression for the required value of C.

If the frequency of operation is low enough for the commutation transients to die away in one sixth of a cycle, it is possible to simplify the equation for v_{bc} by inserting the steady state values of current and voltage for I_0, E_1, E_2, E_3.

Putting $I_0 = \frac{V_d}{2R}$, $E_1 = V_d$, $E_2 = E_3 = \frac{1}{2} V_d$ we obtain

$$v_{bc} = \frac{V_d}{2} - \frac{3V_d}{4} e^{-2\alpha t} - \frac{V_d\left[(\alpha+\beta) . L_d - 2R\right]}{24\, RC\, L_d\, \beta(\alpha+\beta)} e^{-(\alpha+\beta)t}$$

$$+ \frac{V_d\left[(\alpha-\beta)L_d - 2R\right]}{24\, RC\, L_d \beta(\alpha-\beta)} e^{-(\alpha-\beta)t}$$

If R is small and L_d is large so that

$$\frac{1}{36R^2C^2} \gg \frac{2}{3C\, L_d} \quad \text{then } \beta \simeq \alpha$$

Thus $(\alpha + \beta) \simeq 2\alpha$ and $(\beta - \alpha) \simeq 0$

When $\alpha \simeq \beta$, the last term in equation for v_{bc} has a small coefficient and can be neglected.

Inserting $\beta = \alpha$ and putting $\alpha = \frac{1}{6RC}$ the equation simplifies to

$$v_{bc} \simeq \frac{V_d}{2} - V_d\, e^{-2\alpha t}$$

Then, since $t = \delta$ when $v_{bc} = 0$

$$\delta \simeq \frac{1}{2} \log_e 2$$

$$\simeq 3RC \log_e 2$$

$$\simeq \underline{2.08 \text{ RC secs}} \qquad (3.8)$$

Thus when the magnitude of R is known and the value of δ required is found from the S C R characteristics (allowing for a safety margin) the size of capacitor required is given by

$$\underline{C = \frac{\delta}{2.08 R} \text{ F}} \qquad (3.9)$$

This formula for C is valid when R is small and L_d is large and when the frequency of operation is low enough for commutation transients to die away in a sixth of a cycle. At higher frequencies it is found that the voltage by which an S C R is reverse biased at turn off becomes greater than $\frac{1}{2} V_d$ and the resulting value of δ is larger. Hence if the formula for C is used the value of δ resulting will err on the safe side. For example, in the case considered above δ was found from the predicted waveform to be 330μ Secs. Inserting $R = 18\Omega$, and $C = 8\mu F$ in the formula $\delta = 2.08$ RC gives $\delta = 302\mu$ Secs.

3.2.7. Conclusions.

It has been shown that the basic three phase bridge circuit with capacitors connected between the output terminals is capable of inversion into a resistive load. Because of the short turn off time of the S C Rs used the size of capacitors necessary to achieve commutation was small. From the approximate formula given in equation 3.9 it can be estimated that for a 1000 KW load operating from a 1000 V d.c. supply capacitors of only 30 μ F would be necessary to provide an S C R reverse bias time of 30 μ Secs for turn off.

It has also been shown that the theory developed in appendix A is capable of predicting the performance of the inverter with an accuracy of about 5%. More important, however, is the fact that the analysis of the circuit was, by necessity, of a piecemeal nature, each sixth of a cycle having to be considered separately. A relatively simple programme would enable the calculations of waveforms, harmonics, mean values, etc. to be carried out on a digital computer, but it was not found possible to make any accurate generalisations about the effect of varying the circuit parameters upon the operation of the circuit.

3.3 Tests with Inductive Load.

The inverter was tested with a star-connected inductive load consisting of a series combination of inductance L and resistance R per phase as shown in Fig. 3.4. It was found that the inverter did not function at all satisfactorily over a range of frequency and an attempt will be made to show why this was so.

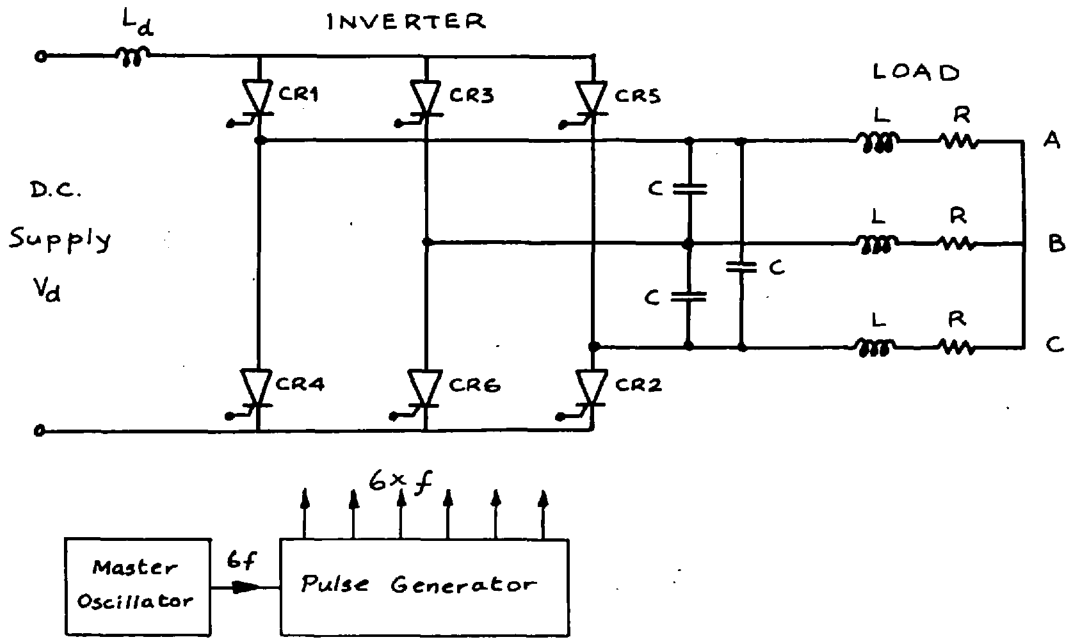


Fig. 3.4 : Circuit of inverter with inductive load.

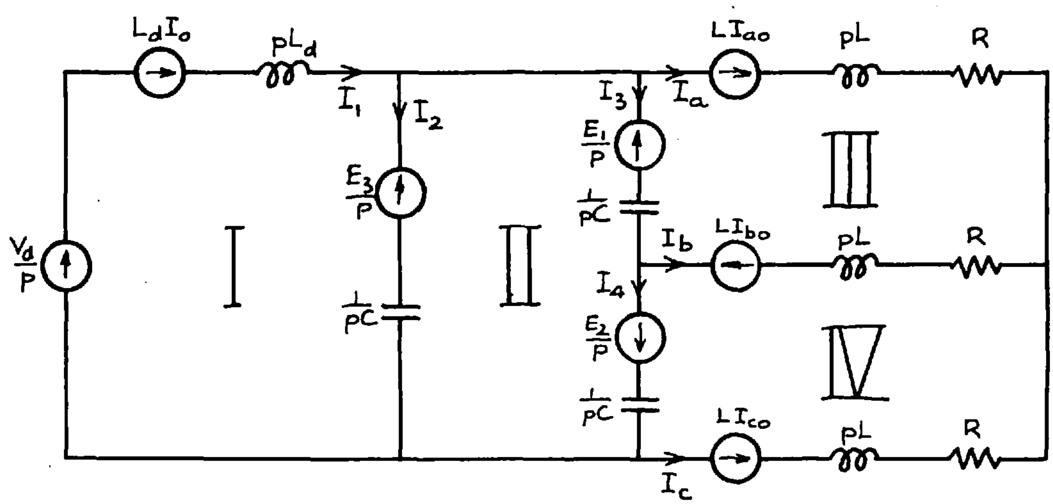


Fig. 3.5 : Laplace operational form of basic inverter circuit, valid between instants t_2 and t_3 while CR1 and CR2 conduct.

3.3.1 Voltage and Current Equations.

The circuit may be analysed by the method employed for the resistive load case. Fig. 3.5 shows the operational circuit which is valid between instants t_2 and t_3. I_0, E_1, E_2, E_3 are, as before, the initial values of the current in L_d and of the voltages v_{ab}, v_{cb}, v_{ac} and I_{ao}, I_{bo}, I_{co} are the initial values of the currents in phase A, B, C respectively.

The circuit equations, after being manipulated in the same way as those for the resistive load case in Appendix A, reduce in their operational form to :-

$$I_2 = I_3 + I_4 = \frac{C\left\{p^2 L.Ld(2I_o - I_{ao} + I_{co}) + p(2L\left[V_d - E_3\right] + 2RL_d I_o - L_d E_3) + 2R(V_d - E_3)\right\}}{3p^3 CL.L_d + 3P^2 RCL_d + p(L_d + 2L) + 2R} \tag{3.10}$$

$$I_3 - I_4 = -\frac{3pLCI_{bo} + C(E_1 + E_2)}{3p^2 LC + 3pRC + 1} \tag{3.11}$$

$$I_1 = \frac{pL(I_{ao} - I_{co}) + E_3}{2p^2 L + 2pR} + I_2 \left(\frac{3}{2} + \frac{1}{2p^2 LC + 2pRC}\right) \tag{3.12}$$

The equations for the other voltages and currents can be obtained from the three above.

$$I_3 = \tfrac{1}{2}\left\{(I_3 + I_4) + (I_3 - I_4)\right\} \tag{3.13}$$

$$I_4 = \tfrac{1}{2}\left\{(I_3 + I_4) - (I_3 - I_4)\right\} \tag{3.14}$$

$$I_a = I_1 - I_2 - I_3 \tag{3.15}$$

$$I_b = I_3 - I_4 \tag{3.16}$$

$$I_c = -I_1 + I_2 + I_4 \tag{3.17}$$

$$V_{ac} = \frac{E_3}{p} + I_2 \quad \frac{1}{pC} \tag{3.18}$$

$$V_{bc} = -\frac{E_2}{p} + I_4 \ \frac{1}{pC} \tag{3.19}$$

$$V_{ab} = V_{ac} - V_{bc} \tag{3.20}$$

In the equation for $(I_3 - I_4)$ the denominator is a quadratic in p and it is therefore possible to obtain a general expression for $(i_3 - i_4)$ in term s of time t. However, the denominator in the equations for $(I_3 + I_4)$ is a cubic in P and cannot, in general, be factorised until the numerical values of R, L, L_d, C have been inserted and only by a numerical method. Consequently the voltage and current equations must be derived separately for each set of circuit parameters from their operational form.

To obtain the initial values I_o, I_{ao}, I_{bo}, I_{co} of current and E_1, E_2, E_3 of voltage, equations (3.12), (3.15), (3.16), (3.18) and (3.19) can be used. When t is put equal to $\frac{T}{6}$ these equations can be reduced to five linear simultaneous equations in I_o, I_{ao}, I_{bo}, E_1 and E_3 from the solutions of which the values of I_{co} and E_2 can be found directly.

It can be seen that the calculation of current and voltage waveforms is an involved process. At low frequencies, however, the calculations are made easier when the assumptions that $I_o = I_{ao} = I_{bo} = \frac{V_d}{2R}$,

$I_{co} = 0$, $E_1 = V_d$, and $E_2 = E_3 = \frac{V_d}{2}$ are made. These assumptions are valid if all the commutation transients die away in one sixth of a cycle.

3.3.2 Sample Calculation for S C R Voltage Waveform at Low Frequency.

A sample calculation for the voltage waveform of an S C R is made below. The calculation is carried out for a low frequency condition and the waveform is plotted in Fig. 3.6. The condition for the calculation is as follows:-

$V_d = 100$ V, $R = 2.1\ \Omega$, $L = 0.012$ H,

$L_d = 0.019$ H, $C = 100\ \mu F$, $f = 5\ ^c/s$.

The initial current and voltage values are then

$I_o = I_{ao} = I_{bo} = 23.8$ A

$I_{co} = 0$

$E_1 = 100$ V

$E_2 = E_3 = 50$ V

Inserting these numerical values, equations (3.10) and (3.11) simplify to :-

$$(3.10):-\ \ I_2 = I_3+I_4 = \frac{7.93\ p^2+31.4\times10^2 p+30.7\times10^4}{p^3+1.75\times10^2 p^2+62.9\times10^4 p+61.4\times10^6} \qquad (3.21)$$

$$(3.11):-\ \ I_3 - I_4 = -\ \frac{23.8\ p+41.6\times10^2}{(p+87.5)^2+(520)^2} \qquad (3.22)$$

The denominator in equation (3.21) can be factorised by a numerical method. Hence

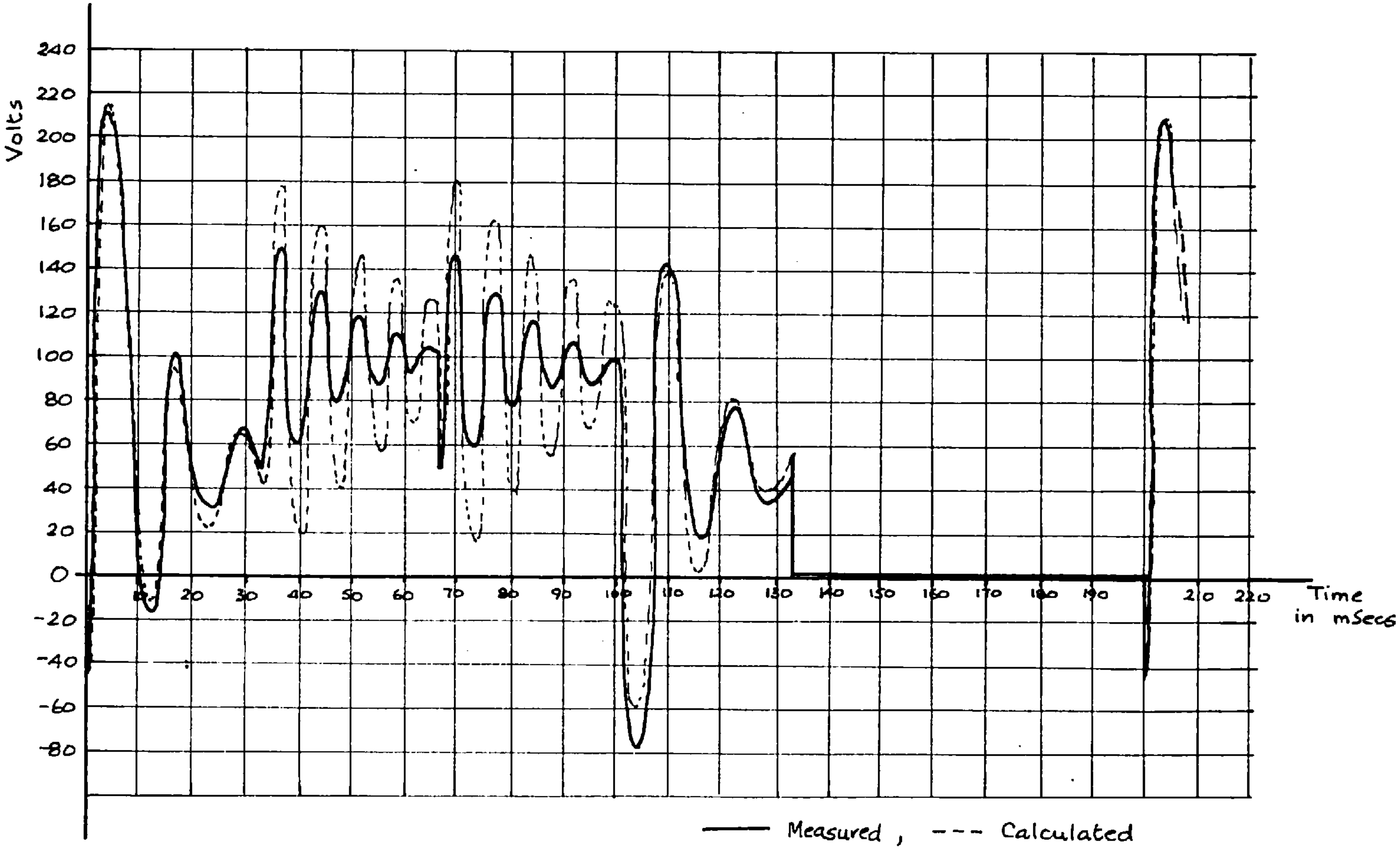


Fig. 3.6.: Calculated and measured SCR voltage waveforms for inductive load.
($V_d = 100v$, $C = 100\mu F$, $L_d = 19mH$, $L = 12mH$, $R = 2.1\Omega$, $f = 5c/s$)

$$I_2 = I_3 + I_4 \triangleq \frac{7.93\,p^2 + 31.4\times10^2 p + 30.7\times10^4}{(p+99.1)([p+37.9]^2 + [787]^2)} \qquad (3.23)$$

Then $V_{ac} = \frac{V_d}{2p} + I_2 \, \frac{1}{pc}$

$$\triangleq \frac{50}{p} + 10^4 \quad \frac{7.93\,p^2 + 31.4\times10^2 p + 30.7\times10^4}{p(p+99.1)([p+37.9]^2 + [787]^2)} \qquad (3.24)$$

Carrying out the inverse transformation to obtain v_{ac} in terms of time t we eventually obtain

$$v_{ac} \triangleq \underline{100 - 11.2e^{-99.1t} + 107 \sin (787t - 28^{\circ})e^{-37.9t}} \qquad (3.25)$$

Also $V_{bc} = - \frac{V_d}{2p} + I_4 \frac{1}{pc}$ which gives

$$v_{bc} \triangleq 50 - 5.6e^{-99.1t} + 53.5 \sin (787t - 28^{\circ})e^{-37.9t} + 230 \sin (520t - 18^{\circ})e^{-87.5t} \qquad (3.26)$$

Then $v_{ab} = v_{ac} - v_{bc}$

$$\triangleq 50 - 5.6e^{-99.1t} + 53.5 \sin (787t - 28^{\circ})e^{-37.9t} - 230 \sin (520t - 18^{\circ})e^{-87.5t} \qquad (3.27)$$

The voltage equations (3.25), (3.26) and (3.27) are valid between the instants t_2 and t_3 but it has been shown in section 3.2.3 that in the first, second, third and fourth sixths of a cycle after turn off the S C R voltages are given by the equations for v_{bc}, v_{ac}, v_{ac} and v_{ab} respectively, putting $t = 0$ at the start of each sixth of a cycle. During conduction the S C R voltage is assumed to be zero.

In Fig. 3.6. the S C R voltage waveform has been plotted using equations (3.25), (3.26) and (3.27). For comparison the waveform obtained by experiment for the same circuit parameters is drawn to the same scale on the same axes. (The predicted and measured frequencies of the oscillations were, in fact, slightly different but have been shown equal in Fig. 3.6 for clarity.) Good agreement between predicted and measured waveforms is seen, except for the amplitudes of the oscillations in the second and third sixths of a cycle after turn off. The circuit used in practice contained resistance in series with the d.c. supply to protect the S C Rs against high fault currents. This resistance damped the oscillations in the inverter input voltage more than the oscillations in the inverter output voltage.

The predicted and measured values of δ were both about 250 μSecs.

3.3.3 The S C R Voltage Waveform.

From Fig. 3.6 it is seen that δ is approximately 250 μsecs, which is nearly ten times more than is really necessary to turn off the S C Rs. However, after turn off the S C R voltage rises to over double the d.c. supply voltage. This means that the d.c. supply voltage must be kept well below half the S C R forward voltage rating.

The value of δ and the amplitude of the oscillations in the voltage waveforms are inter-related, both depending on the size of the commutating capacitors C. Fig. 3.7 shows the variation with C of δ and the peak value of the S C R forward voltage. These values were measured experimentally under low frequency conditions so that the initial voltages on

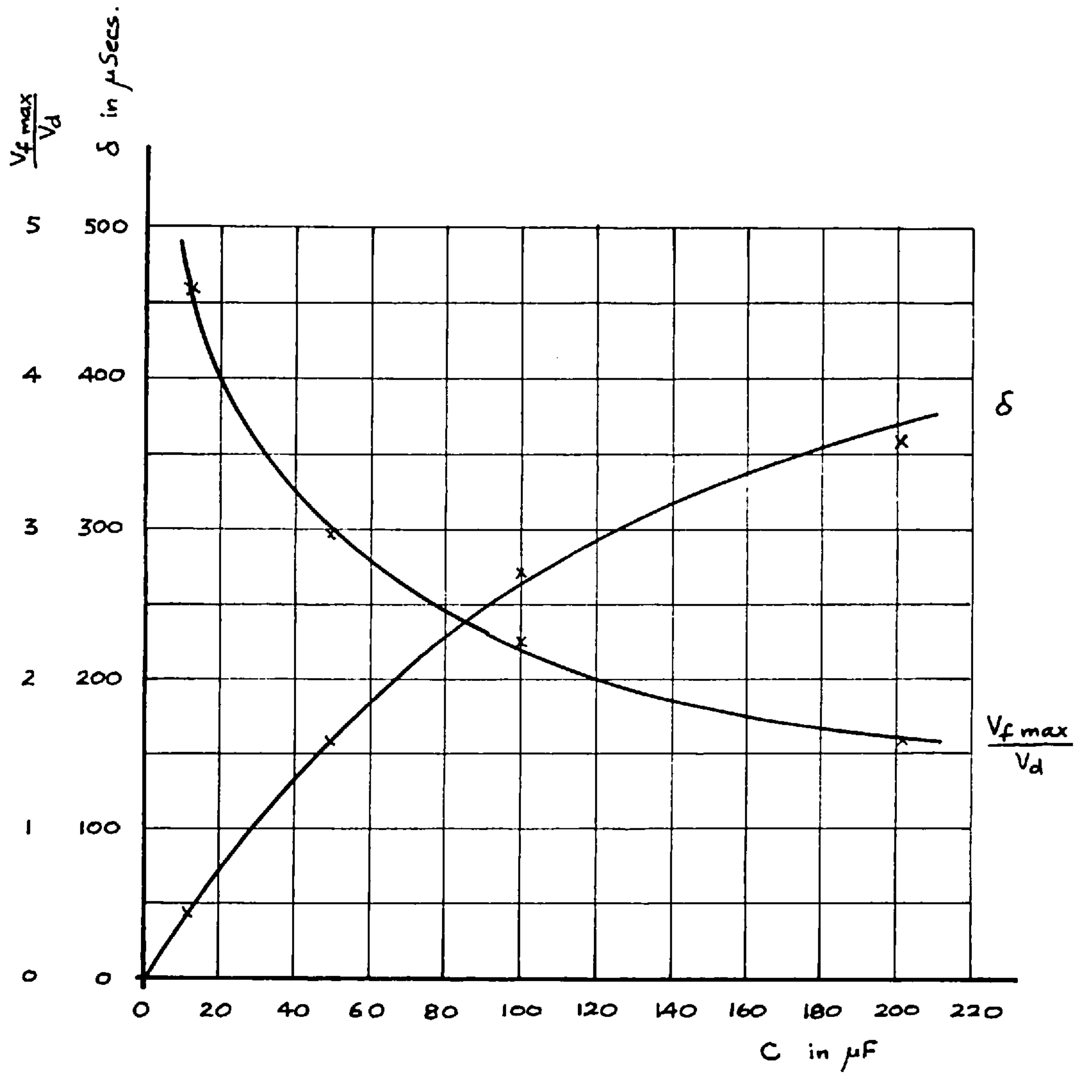


Fig. 3.7: Variation of δ and $\frac{V_{f\,max}}{V_d}$ with C under low frequency conditions.

the capacitors were the same in every case. Since the initial current flowing into the commutating capacitors was the same in each case δ would be expected to increase proportionally with C. For low values of C this is seen to be so but for higher values of C δ tends to increase more slowly. This was because the capacitor current rises from its initial value during commutation, the increase being dependent on the volt-secs applied to the inductance in the circuit. Hence the longer the value of δ , the greater the increase in capacitor charging current, and the greater the divergence from a linear relationship between δ and C. When C is large enough for the oscillatory currents to exceed greatly the initial charging current, δ would be expected to become proportional to the square root of C, i.e. δ would be a fixed proportion of the oscillatory cycle. The tendency for this to happen is seen in Fig. 3.7.

The S C R forward voltage peak, V_f max, is reached when the capacitors reach their peak voltage. This voltage is clearly a function of d.c. supply voltage and the stored energy in the load phase from which current is commutated. In the case for which the graph in Fig. 3.7 is drawn the load stored energy is constant for all values of C. In absorbing this energy the capacitor voltage must rise to a value which varies in an inverse manner with C. If the load stored energy is much larger than the initial capacitive stored energy it would be expected that V_f max would vary inversely with the square root of C. This tendency at low values of C is seen in Fig. 3.7.

It is clear that in choosing a suitable value of C it would not be sufficient to consider only the required value of δ. In the circuit for which the graphs in Fig. 3.7 are drawn the use of a capacitor giving a δ of 30μSecs resulted in a value of V_f max of just over $3.5\ V_d$.

A fundamental feature of the S C R voltage waveform is that the initial value, V_{RO}, of the reverse voltage at turn off should be equal to V_{FF}, the forward voltage on the S C R immediately before turn on. This is the effect of the commutating capacitor connected between the S C Rs being turned on and off at the same instant. When the S C R voltage waveform consists of a series of violent oscillations, as in Fig. 3.6 for example, V_{FF} can vary very considerably when the firing point is moved relative to the oscillations. This happens when the inverter operating frequency is changed and results in a variation of δ with frequency. If the oscillations are prticularly severe V_{FF} can become very small and even tend to go negative and this leads to commutation failure.

The effect of the oscillations upon V_{FF} at a number of frequencies is illustrated in Fig. 3.8. In Fig. 3.8 (a) the S C R voltage waveform at a frequency of 5 $^c/s$ is shown. At this low frequency the oscillations have almost died away completely and V_{FF}, and thus V_{RO}, are approximately equal to $\frac{1}{2}V_d$. At 9 $^c/s$, as shown in Fig. 3.8 (b), the firing points have been moved back along the oscillations, in effect, and V_{FF} is nearly zero. A small increase in frequency would cause V_{FF} to become too small to provide a large enough value of δ and commutation would fail. At 10.5 $^c/s$, shown in Fig. 3.8 (c), V_{FF} has become sufficiently positive once more and the circuit functions until the

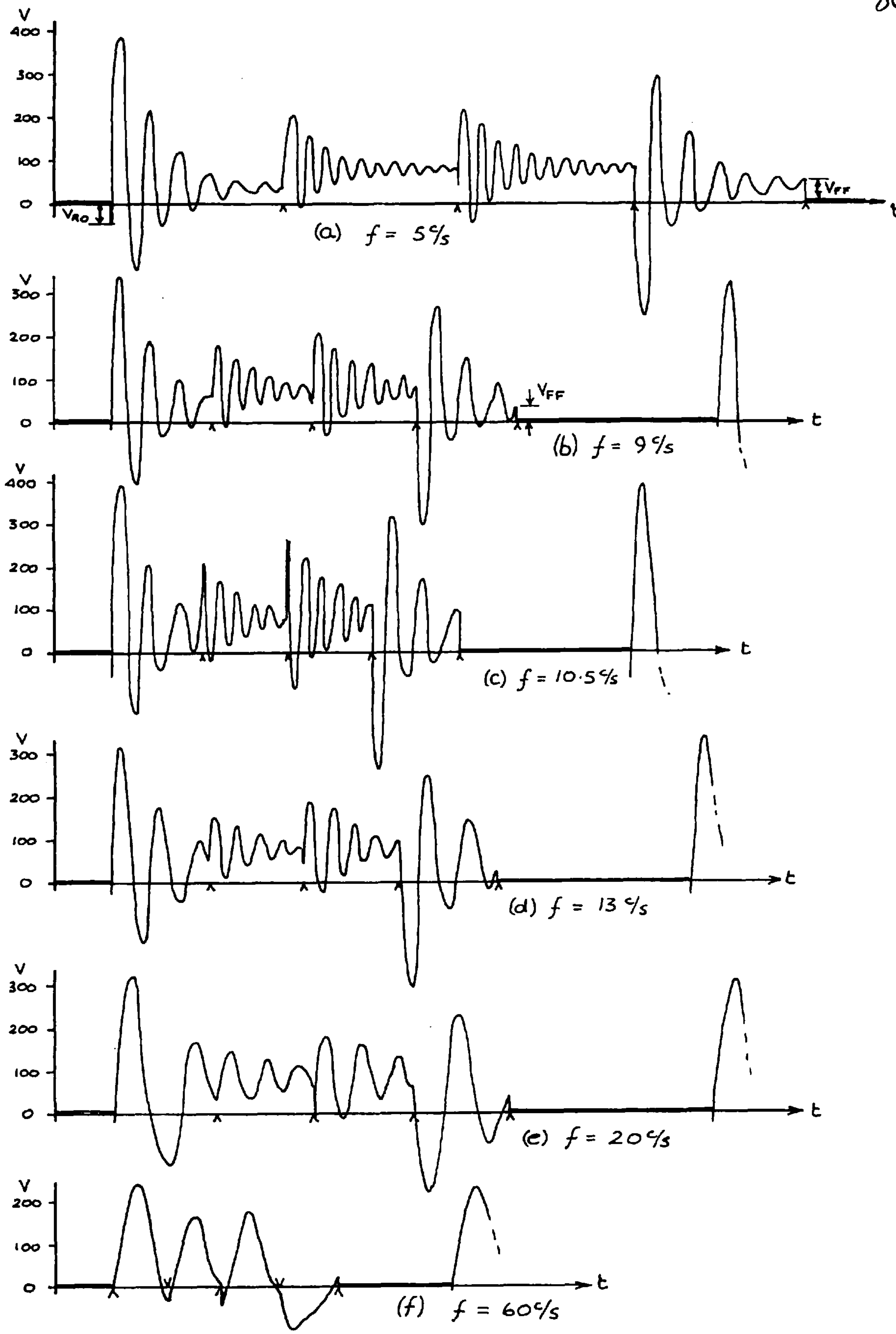


Fig. 3.8 : S.C.R. voltage waveforms over a range of frequencies.

($R = 2{\cdot}1\,\Omega$, $L = 12\,mH$, $L_d = 19\,mH$, $C = 8\,\mu F$, $V_d = 80\,v$.)

frequency reaches 13 $^c/s$, shown in Fig. 3.8 (d). Here V_{FF} tends to go negative once more and between 13 $^c/s$ amd the next frequency at which V_{FF} becomes positive again, i.e. 20 $^c/s$ as in Fig. 3.8 (e), the circuit cannot function. At 60 $^c/s$, shown in Fig. 3.8 (f), the circuit ceases to function again.

It can be seen, therefore, that if C is chosen on the basis of providing an adequate value of δ at low frequencies it is probable that the S C R voltage waveform will contain oscillations of large amplitude. It is then possible that the frequency range of the inverter will contain gaps in which the circuit will not function.

For the circuit to operate satisfactorily over a wide range of frequencies the value of C must clearly be large enough to keep the voltage oscillations to as low an amplitude as possible.

3.3.4 Output Voltage Waveforms.

When the S C R voltage waveforms consist of series of oscillations so, too, do the inverter output voltage waveforms. It is desirable that as far as possible the output voltage waveforms should resemble sinewaves. Fig. 3.9 shows the output voltage waveform corresponding to the S C R voltage waveforms shown in Fig. 3.8 (f). This waveform contains a high proportion of harmonics, the largest harmonic having about half the amplitude of the fundamental component. Fig. 3.10 shows how the output voltage waveform would appear if the frequency were raised by five times so that only a small portion of the oscillation would be included in each sixth of a cycle. It is seen that at such a frequency

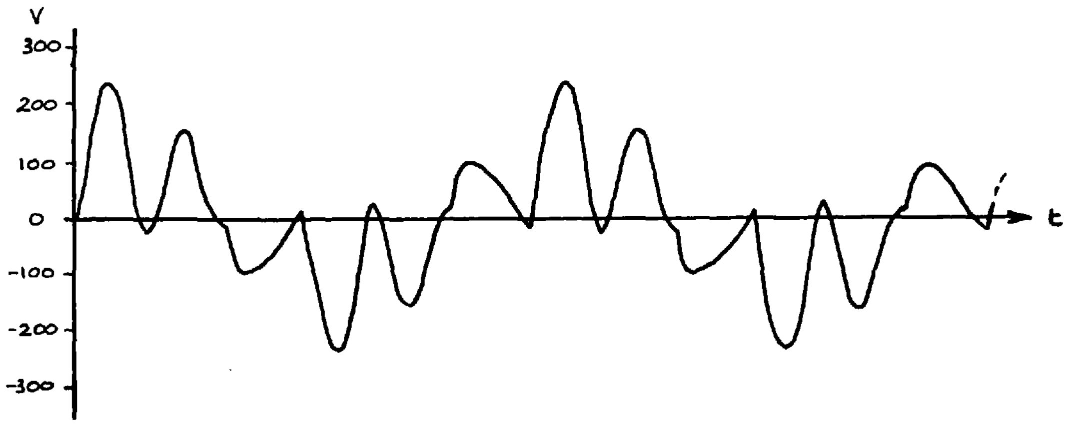


Fig. 3.9 : Output voltage waveform corresponding to SCR voltage waveform shown in Fig. 3.8.(f).

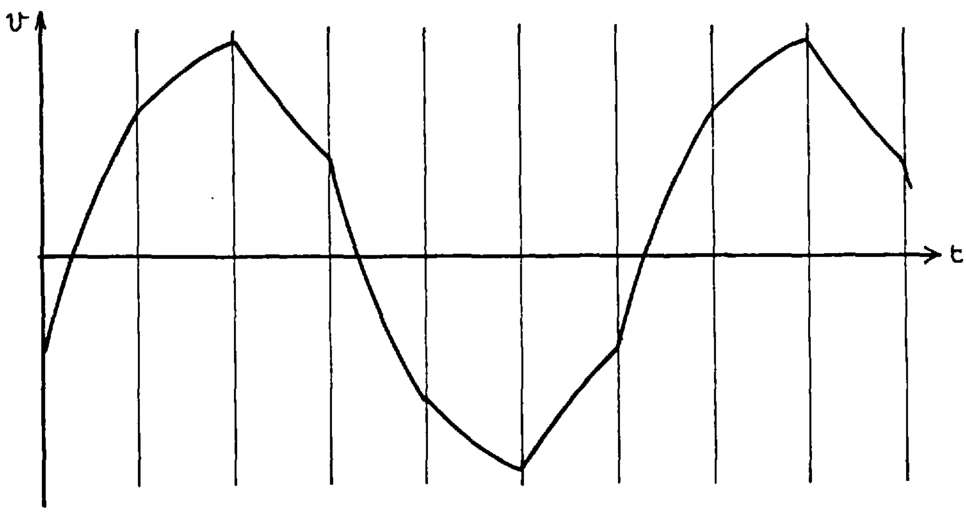


Fig. 3.10 : Output voltage waveform which would appear at about five times the frequency of that shown in Fig. 3.9.

the output voltage waveform would contain a large fundamental sinusoidal component and few harmonics.

It is interesting to note that at this frequency the value of C is such that it would correct the load power factor to unity if the load were to be fed from a three phase sinusoidal supply of the same frequency.

3.4 Tests with Inverter Feeding Induction Motor.

The circuit was tested with an induction motor as its load. It was found impossible to run up the motor to full speed, even with sufficient commutating capacitance to correct the full load power factor to unity at 50 $^c/s$, unless a certain amount of resistance was connected in series with each motor phase. This resistance had a damping effect upon the oscillations between the motor inductance and commutating capacitance after each commutation. Even with the damping resistors it was not possible to run the motor satisfactorily at 50 $^c/s$, especially at light or no load. The value of V_{FF} under these conditions was small and tended to reverse and this was attributed to rotation voltages generated by the motor.

It was clear that the circuit was not suitable, in its simple form, for the supply of induction motors and it was therefore abandoned.

3.5. Conclusions.

It has been demonstrated that the basic three phase bridge circuit with capacitors connected across the output lines for artificial commutation is capable of operation with resistive loads using relatively small commutating capacitors. It was estimated that if S C Rs were used in an inverter for supplying a 1000 KW load from a 1000 V d.c. supply capacitor of only 30 μF would be required. The resistive load condition, however, is of purely academic interest since the heating effect produced in the load could be achieved equally well by direct current or constant frequency alternating current.

When the load was inductive the inverter could be made to operate satisfactorily at any given frequency by making the commutating capacitances high enough to correct the local power factor to unity. The output voltage waveforms were then very good approximations to sinewaves, few harmonics being present, but the time δ was very much greater than the minimum required for turning off the S C Rs. When smaller capacitors were used the output voltage waveform deteriorated and commutation failed over certain ranges of frequency because of the oscillatory nature of the S C R voltage waveform.

In an inverter-motor system operating over a range of load and frequency it would obviously be quite impracticable to vary the commutating capacitance to correct the load power factor to unity under all conditions. Even if it were found sufficient to merely provide an adequate value of δ and disregard the harmonic content of the output voltage waveform some variation of C with frequency would still be necessary. This is because the d.c. supply voltage would have to be reduced with frequency to prevent the motor's magnetic circuit from saturating.

Clearly the basic three phase bridge is not suitable for supplying an induction motor over a wide range of loads and frequencies. The tests carried out on the system gave some indication of the modifications that would be necessary, however, and these will now be discussed.

When an inductive three phase load is fed from a normal three phase supply power flows instantaneously both to and from the load. The basic three phase bridge inverter is a unidirectional circuit and the reverse energy flow from the load must be absorbed by the commutating capacitors. This, basically, is why the capacitors should be large. Smaller capacitors would absorb the same energy but only by charging to higher voltages. The inverter can be made bidirectional by connecting a diode, so that it would not normally conduct, between each output line and each d.c. supply terminal (see Fig. 5.1). These diodes constitute a three phase bridge which can pass power in the opposite direction to that of the S C R bridge. Small capacitors can then be used for commutation, the diodes preventing the capacitor voltages from exceeding the d.c. supply voltage, and the load stored energy can flow through the diodes to the d.c. supply.

The problem of maintaining sufficient voltage on the commutating capacitors when changes in the d.c. supply voltage or S C R voltage waveform occur can be solved by charging a capacitor, or capacitors, to a voltage which is independent of the d.c. supply voltage or S C R voltage waveform.

It will be seen that in the inverters considered in later chapters the principles stated in the two paragraphs above are used.

CHAPTER 4

A D.C. SWITCH USING S C RS AND AUXILIARY SUPPLY.

In the previous chapter it was concluded that for coping with inductive loads the inverter would need to incorporate some means for disposing of the load stored energy at commutation. It was suggested that diodes might be suitable for achieving this end and thus avoid large commutating capacitors. At the same time the diodes might be connected in such a way that the inverter could be capable of allowing power flow both from and to the d.c. supply.

It was also concluded that for reliable commutation, particularly with an induction motor load, some method of charging a capacitor to a fixed voltage and then discharging the capacitor into the inverter circuit for turning off the S C Rs would have to be incorporated.

Because of a delay in the delivery of components for an inverter incorporating the improvements suggested above it was decided to study the problem of using an S C R for turning on and off a d.c. supply to a simple inductive load. The problem is, of course, very similar to that encountered in inversion. The results of this study proved to be so interesting and relevant to the inversion problem that the whole of this chapter is devoted to this d.c. switch.

4.1. Circuit and Principle of Operation.

The circuit for the d.c. switch is shown in Fig. 4.1. The main part of the circuit consists of the load, mdde up of resistance R and

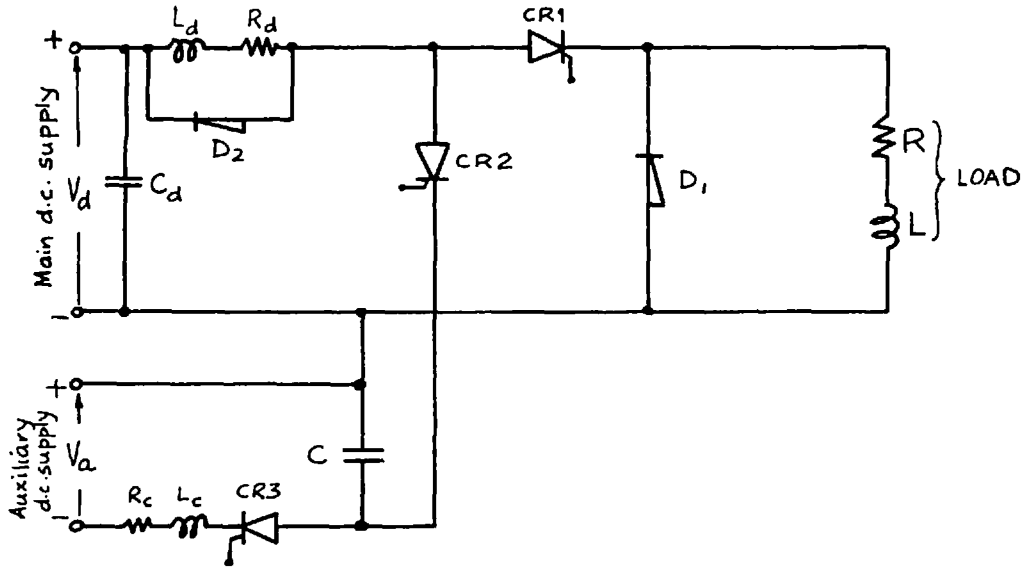


Fig. 4.1 : Circuit of D.C. switch.

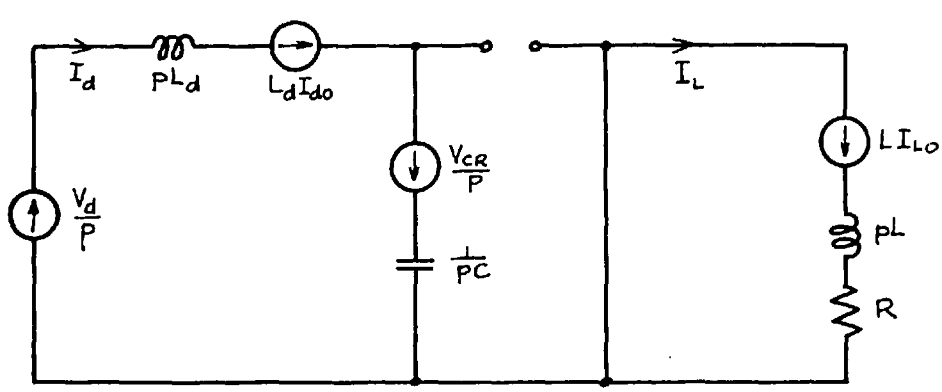


Fig. 4.2 : Laplace operational form of circuit valid only while CR2 conducts.

inductance L in series, the d.c. supply of voltage V_d, and the S C R CR_1 which is used for turning on and off the supply to the load. In series with CR_1, on the supply side, is a choke L_d which possesses a small resistance R_d. Diode D_1 is connected across the load and does not normally conduct.

The auxiliary circuit consists of the second d.c. supply of voltage V_a, the capacitor C, the S C R CR_3 which is used to charge the capacitor C to a fixed voltage from the supply V_a, and CR_2 which is used to discharge C so as to reverse bias and turn off CR_1. R_c and L_c are the resistance and inductance of the auxiliary supply. Diode D_2 is connected across L_d in such a way that it is normally non-conducting.

C_d is a large capacitor connected across the main d.c. supply terminals to reduce the voltage surges due to supply inductance when the supply current undergoes sudden changes.

Not shown in Fig. 4.1 are the R - C series filters connected between anode and cathode of each S C R to suppress voltage transients, the small choke connected in series with CR_2 to limit the magnitude of the current peak occurring when CR_1 is reverse biased at turn off, and the transistor pulse generator for firing the S C Rs in the correct sequence.

Current is supplied to the load by firing CR_1. If all currents in the circuit are zero at the instant of firing CR_1, the current rises towards a steady value $\frac{V_d}{R}$ with a time constant $\frac{L + L_d}{R}$ (ignoring R_d). During this period diodes D_1 and D_2 are reverse-biased and pass no current.

CR_1 can be turned off by firing CR_2. This connects the anode of CR_1 to the negative potential terminal of capacitor C. The cathode potential of CR_1 is prevented from going negative by the action of D_1 which immediately conducts to allow the load current to decay. Consequently CR_1 is reverse-biased by the voltage on capacitor C and turns off. The voltage across C now rises as current flows into the capacitor from the d.c. supply V_d, the initial rate of voltage rise depending upon the initial current in the choke L_d. Eventually the voltage on C becomes positive but, provided it has remained negative long enough for CR_1 to regain its forward blocking property, CR_1 remains off when forward voltage is reapplied.

During the oscillation now taking place between C and L_d the voltage on C would reach a very high value. Diode D_2 conducts, however, as soon as the capacitor voltage becomes equal to the main d.c. supply voltage and prevents the capacitor voltage from rising further. The charging current into C ceases and CR_2 turns off. At this instant the current in L_d is at its peak value and is left to decay slowly through diode D_2 at a rate depending upon the forward voltage drop of D_2 and upon R_d.

In the meantime the load current is decaying through D_1 at a rate depending upon the load resistance and inductance (neglecting the forward voltage drop of D_1).

Before firing CR_1 again CR_3 should be fired to recharge C to a negative voltage from the auxiliary supply.

It can be seen that when CR_1 is turned off the capacitor C is isolated from the load. Hence the size of capacitor required is independent of the load inductance and depends mainly upon the magnitude of current flowing in the load at the instant of interruption. The load stored energy is not returned to the supply but is dissipated in the load resistance and hence does not cause any large voltage transients.

4.2 Theory of Operation.

Because of the isolation of the commutating capacitor from the load the derivation of the current and voltage equations is very straightforward.

Unless stated otherwise it is assumed in the following theory that the S C Rs and diodes can be regarded as short circuits between anode and cathode (i.e. zero voltage drop) when conducting, and open circuits (i.e. zero leakage current) when not conducting.

4.2.1 Turning off CR_1.

It is assumed that when CR_2 fires CR_1 turns off and D_1 conducts at once, the currents flowing in L_d and L are I_{do} and I_{Lo} (not necessarily equal because of possible current in D_2), and that the voltage on C is V_{CR} (not necessarily equal to V_a because of auxiliary supply inductance).

While CR_2 conducts the operational circuit shown in Fig. 4.2 is valid, CR_1 being considered as an open circuit between anode and cathode. The two meshes in the circuit may then be considered quite separately.

Taking the load current first,

$$I_L = \frac{L\, I_{LO}}{pL + R} = \frac{I_{LO}}{p + \frac{R}{L}}$$

Inverting, to obtain i_L in terms of time,

$$i_L = I_{LO}\, e^{-\frac{R}{L} t} \qquad (4.1)$$

i.e. the load current decays exponentially from its initial value with time constant $\frac{L}{R}$. This equation for i_L is valid until CR_1 is fired once more.

Now considering the current in the other mesh,

$$I_d = \frac{\frac{V_d}{p} + \frac{V_{CR}}{p} + L_d\, I_{do}}{p\, L_d + \frac{1}{pC}}$$

R_d is neglected since its effect here is small.

$$= \frac{p\, I_{d0} + \frac{V_d + V_{CR}}{L_d}}{p^2 + \frac{1}{C\, L_d}}$$

Inverting, we obtain

$$i_d = I_{d0} \cos \omega t + \frac{V_d + V_{CR}}{\omega\, L_d} \sin \omega t$$

$$= \underline{\hat{I} \cos (\omega t - \phi)} \qquad (4.2)$$

where $\omega^2 = \frac{1}{CL_d}$, $\tan \phi = \frac{V_d + V_{CR}}{\omega L_d\, I_{d0}} = \frac{\omega C(V_d + V_{CR})}{I_{do}}$, and $$\hat{I} = \sqrt{I_{do}^2 + \left[\frac{V_d + V_{CR}}{\omega L_d}\right]^2} = I_{do}\sqrt{1 + \tan^2\phi}$$

Since CR_2 and D_1 are conducting the voltage across CR_1 is equal to the voltage across C and is given by

$$V_c = -\frac{V_{CR}}{p} + I_d \frac{1}{pC}$$

$$= -\frac{V_{CR}}{p} + \frac{p\, I_{do} + \frac{V_d + V_{CR}}{L_d}}{pC\,(p^2 + \omega^2)}$$

Inverting we obtain

$$v_c = V_d + \frac{I}{\omega C} \sin(\omega t - \phi) \qquad (4.3)$$

From equation (4.3) may be found the time δ for which CR_1 is reverse biased. For $t = \delta$ when $v_c = 0$

$$\therefore \quad 0 = V_d + \frac{I}{\omega C} \sin(\omega\delta - \phi)$$

Hence $$= \frac{1}{\omega}\left(\phi - \sin^{-1}\frac{V_d \omega C}{\hat{I}}\right) \qquad (4.4)$$

Equations (4.2) and (4.3) are valid only until v_c reaches the value $+ V_d$. At this point D_2 starts to conduct and CR_2 turns off.

When $v_c = V_d$

(from (4.3):- $$V_d = V_d + \frac{\hat{I}}{\omega C} \sin(\omega t - \phi)$$

Hence $$\underline{t = \frac{\phi}{\omega}} \qquad (4.5)$$

i.e. CR_2 conducts for a time $\frac{\phi}{\omega}$.

The value of i_d when CR_2 turns off and D_2 starts to conduct may be found from equation (4.2) by putting $t = \frac{\phi}{\omega}$.

Then $i_d = \hat{I} \cos\left(\omega \cdot \frac{\phi}{\omega} - \phi\right)$

$$\text{i.e. } i_d = \hat{I} \tag{4.6}$$

This value of i_d is left to decay through diode D_2.

4.2.2 Effect of D_2.

If D_2 were absent from the circuit, CR_2 would continue to conduct until i_d became zero

i.e. until $\hat{I} \cos(\omega t - \phi) = 0$

$$\text{i.e. until } \underline{t = \frac{1}{\omega}\left(\phi + \frac{\pi}{2}\right)} \tag{4.7}$$

This would mean that no current would be left to decay through D_2 but the voltage v_c would reach a very high value given by

$$v_c = V_d + \frac{\hat{I}}{\omega C} \tag{4.8}$$

The magnitude of this voltage peak would depend largely upon the current being interrupted and the relative values of L_d and C and could be as much as twenty times greater than V_d. The presence of D_2 is therefore imperative. (This is similar to the problem referred to in section 3.3.3. Here the problem is solved by the use of diode D_2.)

4.2.3 Decay of $\hat{I}$ through L_d and D_2.

When CR_2 turns off the current I flowing in L_d is left to decay through D_2. Since the decay is a relatively slow one it is essential to take into account both the resistance R_d of the choke and the forward voltage drop V_f of D_2. V_f can be assumed constant over most of the current range though its value does in fact fall sharply at very low currents.

Fig. 4.3 shows the operational circuit which may be used for calculating the decay. During the decay the current I_6 in D_2 is equal to the current I_5 in L_d.

$$I_5 = \frac{L_d \hat{I} - \frac{V_f}{p}}{p L_d + R_d}$$

$$= \frac{p \hat{I} - \frac{V_f}{L_d}}{p(p + \frac{R_d}{L_d})}$$

Inverting, we obtain

$$i_5 = -\frac{V_f}{R_d} + (\hat{I} + \frac{V_f}{R_d})\, e^{-\frac{R_d}{L_d} t} \qquad (4.9)$$

i.e. the current in the choke decays with time constant $\frac{L_d}{R_d}$ towards a steady state value $-\frac{V_f}{R_d}$. In fact, of course, the current in D_2 cannot become negative and hence the decay would cease when i_5 becomes zero.

N.B. In equation (4.9) $t = 0$ at the instant at which CR_2 turns off whereas in equations (4.1) to (4.8) $t = 0$ when CR_2 turns on.

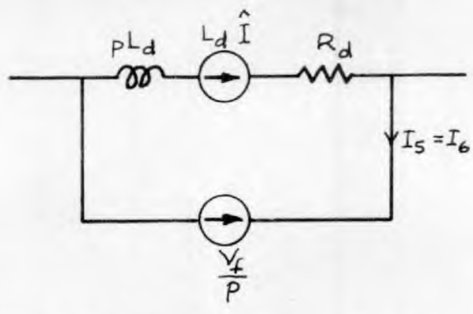


Fig. 4.3: Operational circuit for calculating the decay of $\hat{I}$ through L_d and D_2.

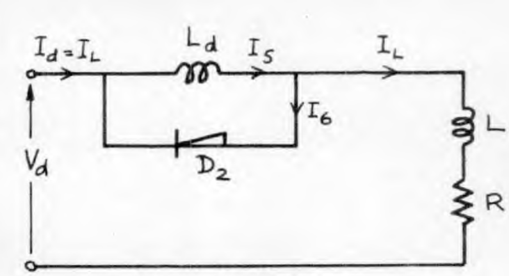


Fig. 4.4: Circuit for calculating the rise of load current after triggering CR1.

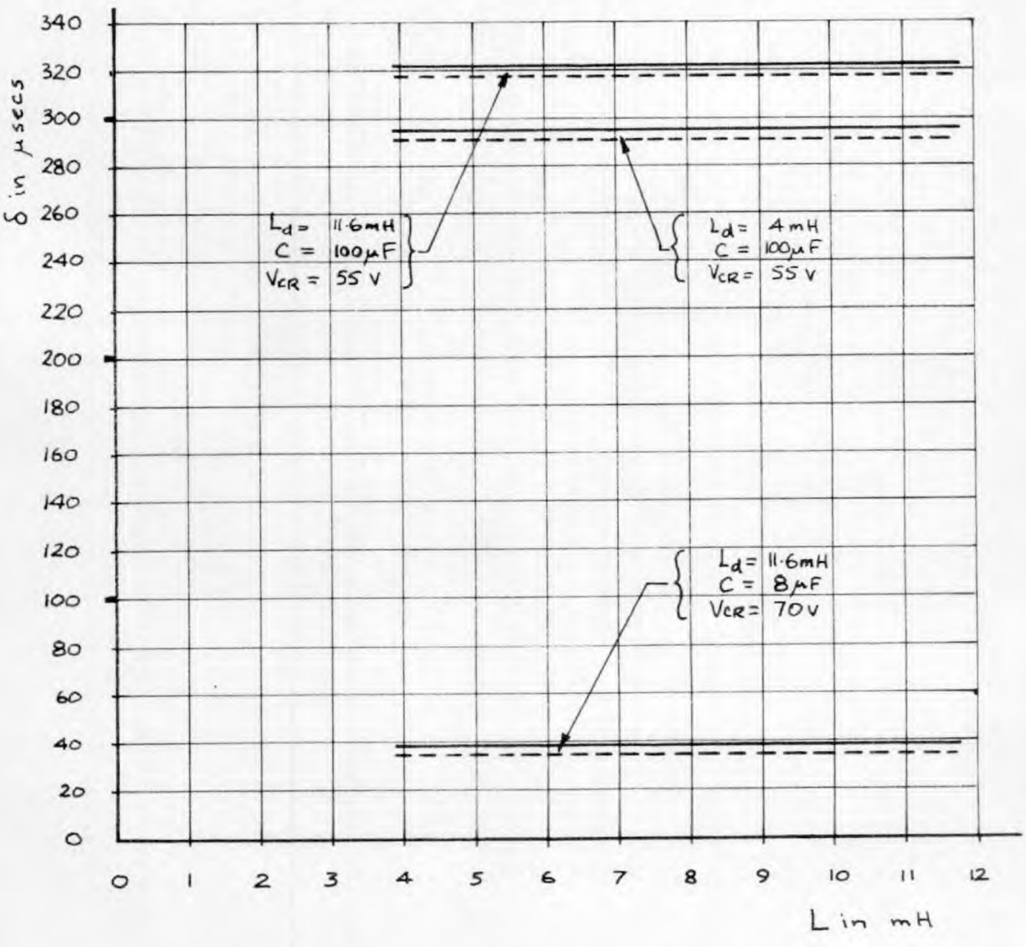


Fig. 4.5: Variation of δ with load inductance L.

$R = 2.5\Omega$, $V_d = 50v$, $I_{do} = I_{Lo} = 15.0A$.

Combinations of L_d, C and V_{CR} as shown.

—— values of δ measured on oscillograph.

- - - - calculated values of δ.

4.2.4 Rise of Load Current when CR_1 is fired.

Fig. 4.4 shows the circuit which can be used for considering how the load current i_L rises when CR_1 is fired. i_5 and i_6 are the currents in the choke L_d and diode D_2.

If the currents in the load and the choke L_d have decayed completely after the previous turning off of CR_1, then i_L and i_5 are equal during the whole of the time for which CR_1 conducts. The rise of load current is then given by

$$\underline{i_L = \frac{V_d}{R}\left(1 - e^{-\frac{R}{L + L_d}t}\right)} \tag{4.10}$$

If, however, the current in L_d has not completely decayed when CR_1 is fired, the situation is changed. During the time when i_L is smaller than the current i_5 still decaying in L_d the balance of current flows in D_2

$$\text{i.e.} \quad i_6 = i_5 - i_L$$

During this period the voltage across L_d is almost zero and hence L_d has no effect upon the load current rise. Therefore, while D_2 conducts

$$i_L = \frac{V_d}{R}\left(1 - e^{-\frac{R}{L}t}\right) \tag{4.11}$$

However, the current in D_2 cannot become negative, so as soon as i_L reaches the same value as i_5, D_2 ceases to conduct and becomes reverse biased, enabling L_d to impede current rise. Consequently i_L

rises thereafter towards its steady value with a time constant $\frac{L + L_d}{R}$.

4.2.5 Re-charging of C from Auxiliary Supply.

When CR_3 is fired the voltage on C reverses towards the auxiliary supply voltage V_a. Because of the supply inductance the voltage overshoots V_a and at the overshoot voltage peak, V_{CR}, the capacitor charging current is prevented from reversing by CR_3. CR_3 therefore turns off, leaving C with the voltage V_{CR}.

4.2.6 Approximate Expression for δ.

Immediately after CR_1 is turned off the current flowing into C through CR_2 varies between I_{do} and $\hat{I}$. If $\hat{I}$ is not much greater than I_{do}, the voltage on C rises approximately linearly with time from its initial value $-V_{CR}$. δ is, therefore, approximately equal to the time taken for C to charge from a voltage $-V_{CR}$ to zero voltage with a charging current I_{do}.

i.e. $$\delta \simeq \frac{C\,V_{CR}}{I_{do}} \tag{4.12}$$

Hence the values of C and V_{CR} required to give the required value of δ at a given value of I_{do} may be found from the following formulae.

$$C \simeq \frac{\delta . I_{do}}{V_{CR}} \tag{4.13}$$

and

$$V_{CR} \simeq \frac{\delta . I_{do}}{C} \tag{4.14}$$

From equation (4.2) it can be seen that $\hat{I}$ is not much greater than I_{do} if L_d or I_{do} is large and these are the conditions for which the above formulae are most accurate.

4.3 Variation of δ with Load $\frac{L}{R}$ ratio, C, L_d, V_{CR} and I_{do}.

A series of tests were (was) carried out to investigate the effect upon δ of varying the load $\frac{L}{R}$ ratio and the values of C, L_d, V_{CR} and I_{do} and to check the accuracy of the theory in section 4.2. δ is the parameter which, above all, must be of a suitable value if the circuit is to function properly.

In these tests the circuit was used as a d.c. chopper, i.e. a repetitive on-off switch, at a frequency of 5 $^c/s$. This frequency was low enough for the currents and voltages to reach their steady values, and yet high enough for the voltage and current variations to be observed by means of an oscilloscope. δ, V_{CR} and I_{do} were then measured directly from the oscilloscope.

4.3.1 Variation of δ with Load $\frac{L}{R}$ Ratio.

The formula for δ given in equation (4.4) made no reference to the load inductance or resistance and δ would, therefore, seem to be independent of L and R. In fact the value of I_{do} is very much dependent upon R and this test was designed to show that δ is independent of the load $\frac{L}{R}$ ratio, which would correspond to the load power factor in an inverter.

Keeping R, and hence I_{do} constant, L was varied over a range of 3 to 1 for several combinations of C, L_d and V_{CR} and δ was measured for each value of L. The results of this test are shown in Fig. 4.5 and it can be seen that the variation of L had no effect upon the value of δ . This was as predicted by the theory. The corresponding calculated results are also plotted in Fig. 4.5 to show the close agreement between calculated and experimentally measured results.

4.3.2 Variation of δ with L_d.

In this test and all the remaining tests described in section 4.3 the load inductance was set at a constant value and the value of I_{do} was varied by adjusting the load resistance R. The graphs in Fig. 4.6 and Fig. 4.7 show δ plotted as a function of I_{do}. The families of curves obtained then show the effect upon δ of varying any of the circuit parameters.

For this test C and V_{CR} were kept constant and L_d was varied over a range of about 6 to 1, the variation of δ with I_{do} being measured for each value of L_d. This procedure was repeated for several combinations of C and V_{CR}.

Fig. 4.6 shows the experimental and calculated results. For the sake of clarity the curves for only the extreme values of L_d used have been drawn. The good agreement between calculated and experimental results should again be noted. It was seen that increasing L_d by a factor of six had little effect upon the value of δ particularly at

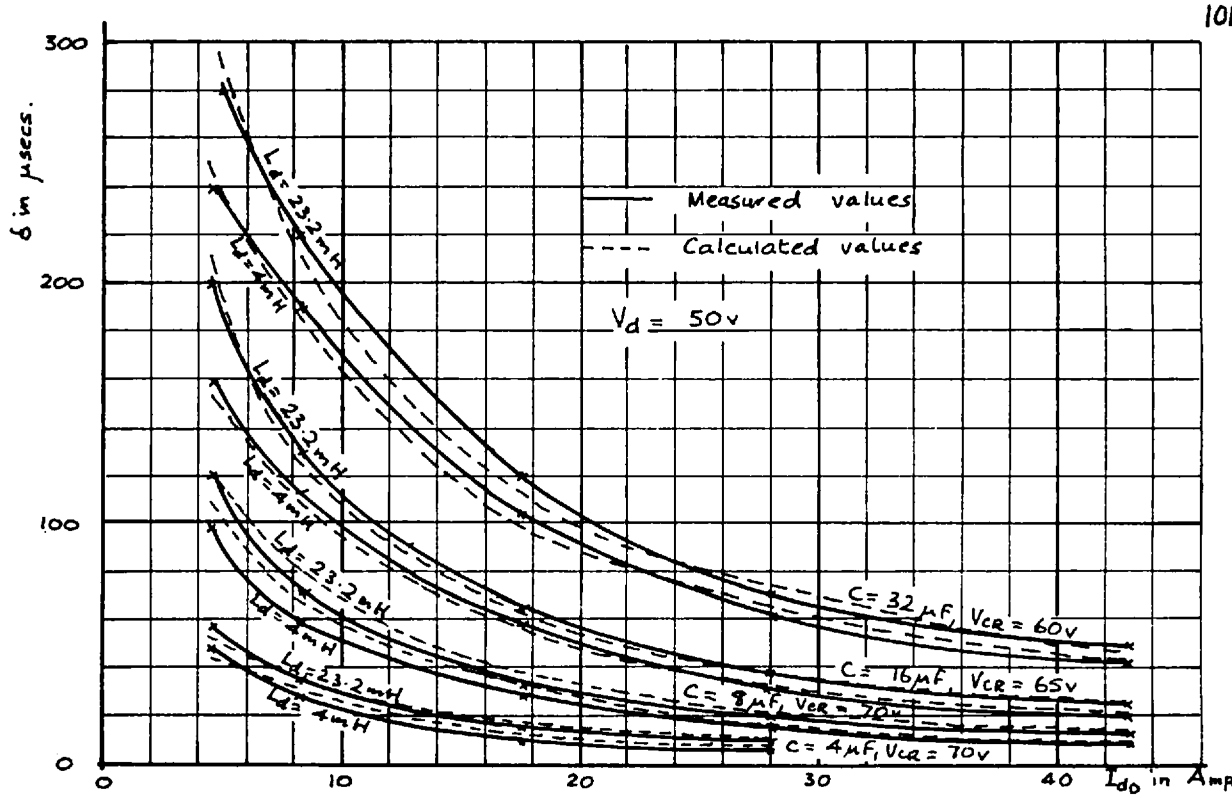


Fig. 4.6 : Variation of δ with I_{do} for various combinations of C, V_{CR} and L_d.

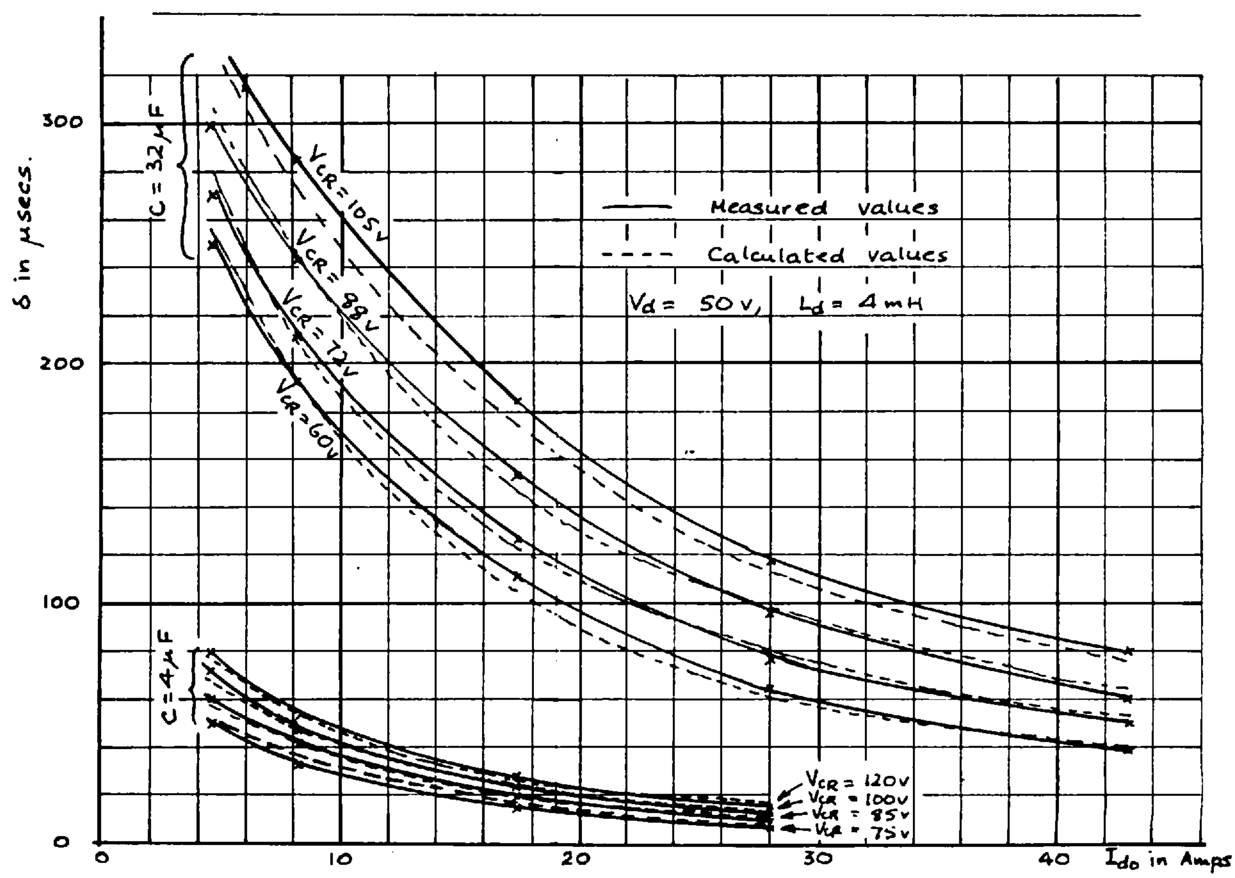


Fig. 4.7 : Variation of δ with I_{do} for various combinations of C and V_{CR}.

the higher values of I_{do}. This was to be expected since the approximate expression for δ in equation (4.12) made no reference to L_d.

4.3.3 Variation of δ with C.

From Fig. 4.6 the variation of δ with C can also be determined. It can be seen that by doubling the value of C the value of δ was also approximately doubled, again as predicted in equation (4.12).

4.3.4 Variation of δ with V_{CR}.

Keeping L_d and C constant V_{CR} was varied over a range of about 2 to 1 and δ plotted as a function of I_{do} for each value of V_{CR}. This was repeated for a different value of C. Fig. 4.7 shows the calculated and experimental results. It can be seen that at the higher values of I_{do} δ was almost proportional to V_{CR}, as predicted by equation (4.12).

4.3.5 Variation of δ with I_{do}.

From both Fig. 4.6 and Fig. 4.7 it may be seen that δ was approximately inversely proportional to I_{do}, once more as predicted in equation (4.12).

4.4 Voltage and Current Waveforms.

To obtain the voltage and current waveforms sketched in Figs. 4.8 and 4.9 the circuit was used as a d.c. chopper at a frequency of 5 $^c/s$. and the waveforms observed by means of an oscilloscope. Fig. 4.8 shows the waveforms for a light load, Fig. 4.9 for a heavy load. The waveforms sketched are as follows:-

V_d - the main d.c. supply voltage

V_1 - the anode-cathode voltage of CR_1

V_{Ld} - the voltage across the choke L_d and diode D_2

V_{a_1n} - the voltage between the anode of CR_1 and the negative d.c. supply terminal

V_L - the voltage across the load and diode D_1

V_c - the voltage on capacitor C

V_2 - the anode-cathode voltage of CR_2

I_d - the current taken from the main d.c. supply

I_5 - the current in the choke L_d

I_6 - the current in the diode D_2

I_1 - the current in CR_1

I_2 - the current in CR_2

I_L - the load current

I_4 - the current in diode D_1

t_1, t_2, t_3 are the instants at which CR_1, CR_2, CR_3 are fired.

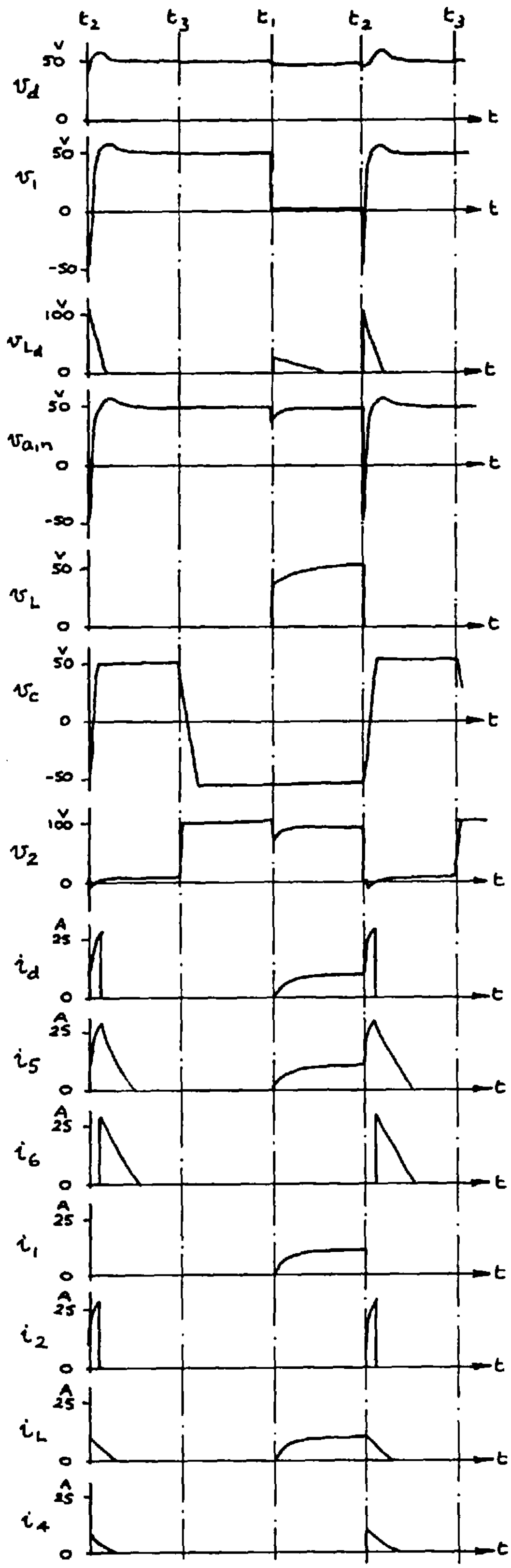


Fig. 4.8

(I_{do} = 10A)

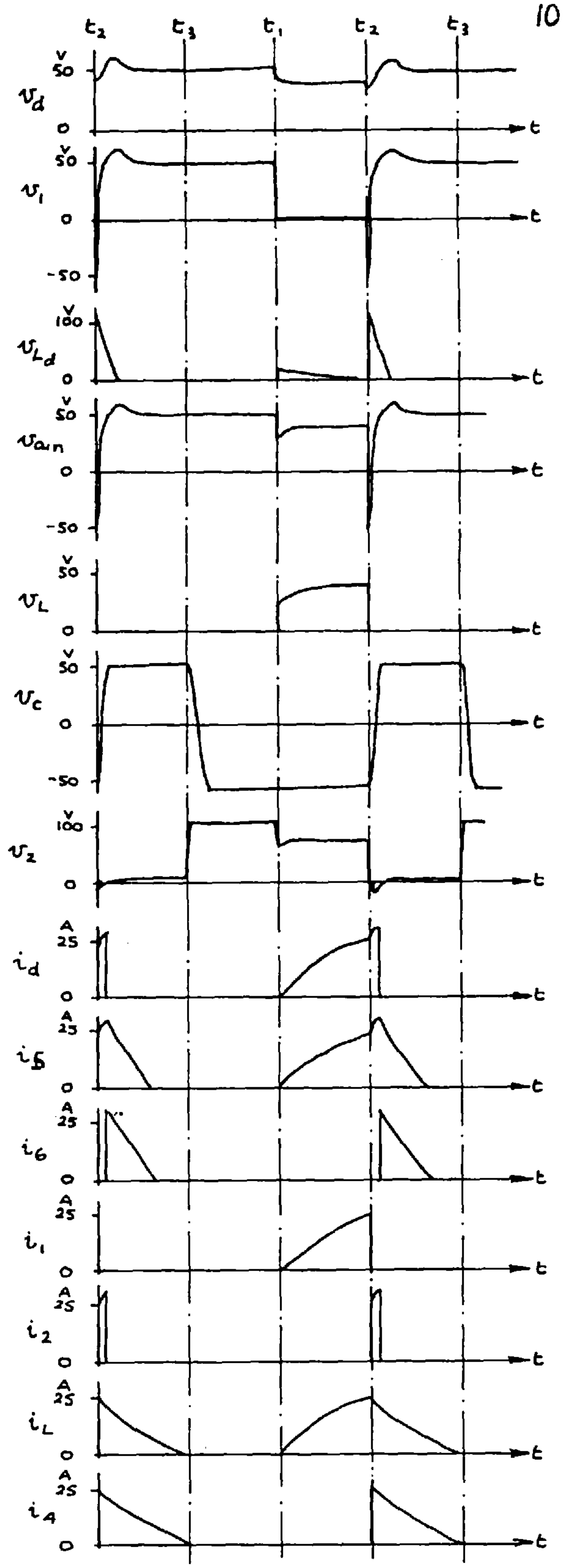


Fig. 4.9

(I_{do} = 25A)

Voltage and current waveforms.

(V_d = 50v, V_{CR} = 60v, C = 32μF, L_d = 4 mH, L = 11·6mH)

4.4.1 Explanation of Waveforms.

At instant t_1 V_d falls because of the regulation of the supply and V_1 falls almost to zero. Currents I_d, I_5, I_1, I_L are the same current and build up to their steady state value with time constant $\frac{L + L_d}{R}$ and a decaying voltage appears across choke L_d. No current flows in D_1 and D_2, these diodes being reverse biased. No current flows in CR_2. V_{a_1n} and V_L are equal to $(V_d - V_{Ld})$ and V_c remains steady at the value to which it has been charged from the auxiliary supply. V_2 is equal to $(V_d - V_c)$.

At instant t_2 CR_2 is fired and V_2 falls almost to zero. V_d rises to its open circuit value with some overshoot caused by the combination of supply inductance and the reservoir capacitor C_d. CR_1 is reverse biased by the voltage on C and turns off, I_1 falling at once to zero. I_L decays through diode D_1 and now, therefore, $I_4 = I_L$. V_L falls to zero because of the conduction of D_1. Capacitor C charges through L_d from the main d.c. supply and for a short period V_{Ld} is equal to $(V_d - V_c)$. $I_d = I_5 = I_2$, rising from the value of I_5 at instant t_2 to a peak value $\hat{I}$. When V_c reaches the value $+V_d$ diode D_2 starts to conduct and CR_2 turns off and is reverse biased by a small voltage. I_2 and I_d fall instantly to zero while I_5 decays from its peak value $\hat{I}$ through diode D_2. Hence $I_5 = I_6$ during this decay. V_c remains at the value to which it had been charged when CR_2 turned off and $V_2 = (V_d - V_c)$ again.

At instant t_3 capacitor C is re-charged to a negative voltage through CR_3 from the auxiliary supply. $V_2 = (V_d - V_c)$ and hence as V_c falls, V_2 rises by the same amount.

At instant t_1 the whole cycle is repeated again.

4.5 Comparison between Measured and Predicted Results.

For the sake of clarity the calculated waveforms have not been drawn in Figs. 4.8 and 4.9. A comparison between calculated and experimentally obtained results will be made on the basis of the peak current value $\hat{I}$ and the time taken for $\hat{I}$ to decay through diode D_2. Because of the poor regulation of the d.c. supply the values of I_{do} used have not been calculated but measured experimentally. In each of the two cases considered $V_d = 50$ V, $V_{CR} = 65$ V, $L_d = 4$ mH, $R_d = 0.1\,\Omega$, $C = 32\,\mu$F, $V_f = 1.6$ V.

4.5.1 Peak Value $\hat{I}$.

(a) $\underline{I_{do} = 4.6 \text{ A}}$

From equation (4.2) $\hat{I} = \underline{11.85 \text{ A}}$

(Experimentally obtained value of $\hat{I} = 12$ A)

(b) $\underline{I_{do} = 25 \text{ A}}$

From equation (4.2) $\hat{I} = \underline{27.3 \text{ A}}$

(Experimentally obtained value of $\hat{I} = 28$ A)

4.5.2 Period of Decay of $\hat{I}$ through L_d and D_2.

When CR_2 turns off the current in L_d has reached the value $\hat{I}$ and this current decays through D_2. The equation for the decay is that for I_5 in section 4.2.3, i.e. equation (4.9).

(a) $I_{do} = 4.6$ A, $\hat{I} = 11.85$ A

$$i_5 = -16 + 27.85\, e^{-25t}$$

$$\therefore i_5 = 0 \text{ when } t = \frac{1}{25} \log_e \frac{27.85}{16} = 22 \text{ msecs}$$

(By experiment $i_5 = 0$ when $t = 26$ mSecs.)

(b) $I_{do} = 25$ A, $\hat{I} = 27.3$ A

$$i_5 = -16 + 43.3\, e^{-25t}$$

$$\therefore i_5 = 0 \text{ when } t = \frac{1}{25} \log_e \frac{43.4}{16}$$

$$= \underline{\underline{40 \text{ mSecs}}}$$

(by experiment $i_5 = 0$ when $t = 46$ mSecs.)

It can be seen that the theory gives very accurate results for the value of $\hat{I}$. The predicted decay times ~~are times~~ are a little low but this is to be expected since V_f is not absolutely constant but falls quite sharply at currents less than about 5 A.

4.6 Variation of I_{do} and δ with Chopping Frequency.

When the circuit was used as a d.c. chopper it was found that I_{do}, and hence δ, varied with the chopping frequency. This section shows how this variation occurred and gives some theory from which the variation may be predicted.

4.6.1 Effect of Increasein Chopping Frequency upon the Waveforms of I_5 and I_L.

In Fig. 4.10 the waveforms of the current I_5 in choke L_d and the current I_L in the load are shown for a typical set of circuit parameters at five different operating frequencies.

In Fig. 4.10(a) the frequency is 5 $^c/s$ and I_5 and I_L are both zero when CR_1 is fired at instant t_1. I_5 and I_L then rise together with time constant $\frac{L + L_d}{R}$ towards a steady value and are still equal at instant t_2 when CR_2 is fired. I_L then starts at once to decay through diode D_1. I_5, however, rises to the peak value $\hat{I}$ in the charging of capacitor C before decaying through diode D_2. At this low frequency both I_5 and I_L have ample time to decay to zero before CR_1 is re-fired.

At the higher frequencies of 25 $^c/_s$ and 50 $^c/_s$, illustrated by Figs. 4.10(b) and 4.10(c), I_L still has time to decay to zero between instant t_2 and t_1 but I_5 has not. I_L therefore starts to rise at t_1 with time constant $\frac{L}{R}$ until it becomes equal to I_5 and thereafter both I_L and I_5 rise together with time constant $\frac{L_d + L}{R}$ towards a steady state value. At 25 $^c/_s$ they almost reach their steady value but at 50 $^c/s$ CR_2 is fired some time before the steady value is attained and hence I_{do} and I_{Lo} are lower than their low frequency values. δ is therefore greater than its low frequency value since it is approximately inversely proportional to I_{do}.

At 100 $^c/s$, for which Fig. 4.10(d) is drawn, I_L is still zero at t_1 but the interval between t_2 and t_1 is now too short for I_5 and I_L to

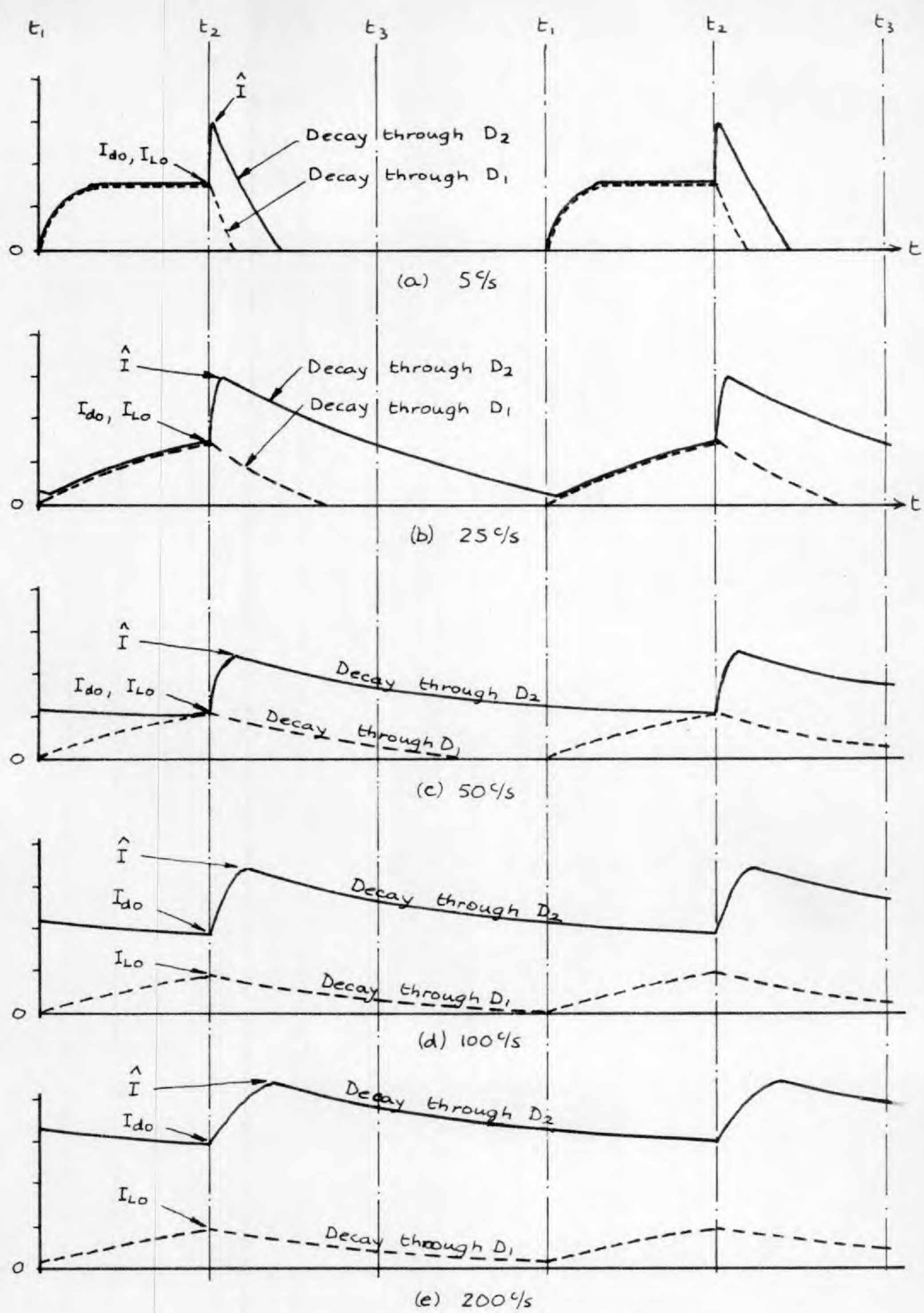


Fig. 4.10: Effect of frequency upon the waveforms of i_S (——) and i_L (- - -).

become equal. I_{do} is therefore greater than I_{Lo}, though still smaller than its low frequency value.

At 2oo $^{c}/s$, shown in Fig. 4.10(e), I_{do} has become much greater than I_{Lo} and is now completely independent of I_L. I_{do} now depends only upon the frequency of firing CR_2, the difference between I_{do} and $\hat{I}$, and the rate of decay of I_5. At even higher frequencies I_{do} settles down at such a value that I_5 can rise from I_{do} to $\hat{I}$ just after CR_2 is fired and decay from $\hat{I}$ back to I_{do} before CR_2 is again fired.

4.6.2 Approximate Analysis of Variation of I_{do} and δ with Frequency.

By writing ω^2 as $\frac{1}{C\,L_d}$ the peak value $\hat{I}$ reached by I_5 after instant t_2 may be expressed as

$$\hat{I} = I_{do}\sqrt{1 + \frac{C(V_d + V_{CR})^2}{L_d\ I_{do}^{\ 2}}} \tag{4.15}$$

If $\hat{I}$ is not very much greater than I_{do}, we obtain on expanding the RHS by the binomial theorem

$$\hat{I} = I_{do}\left\{1 + \tfrac{1}{2}\ \frac{C(V_d + V_{CR})^2}{L_d\ I_{do}^{\ 2}} + \frac{1}{8}\left[\frac{C(V_d + V_{CR})^2}{L_d I_{do}}\right]^2 + \dots\right\}$$

$$\doteq I_{do} + \frac{C(V_d + V_{CR})^2}{2L_d\ I_{do}}$$

$$\text{i.e.}\quad \hat{I} - I_{do} \doteq \frac{C(V_d + V_{CR})^2}{2L_d\ I_{do}} \tag{4.16}$$

It is assumed that I_5 decays from $\hat{I}$ to I_{do} linearly at its initial rate and that the decay lasts for a time $\frac{1}{f}$, where f is the chopping frequency, (i.e. it is assumed that $\frac{\phi}{\omega}$ is small compared with $\frac{1}{f}$). The rate of decay depends upon the values of L_d, R_d, $\hat{I}$ and the forward voltage drop of diode D_2. From equation (4.9) we obtain

$$\frac{dI_5}{dt} = -\left\{\frac{R_d\,\hat{I}}{L_d} + \frac{V_f}{L_d}\right\} \tag{4.17}$$

If $\hat{I} \simeq I_{do}$, i.e. $(\hat{I} - I_{do})$ much less than $\hat{I}$ or I_{do}, and the effect of V_f can be represented by adjusting the value of R_d to R'_d

$$\frac{dI_5}{dt} \simeq - \frac{R'_d\, I_{do}}{L_d} \tag{4.18}$$

Since I_5 must decay from $\hat{I}$ to I_{do} at this decay rate in time $\frac{1}{f}$

$$\hat{I} - I_{do} \simeq + \frac{R'_d\, I_{do}}{L_d} \cdot \frac{1}{f}$$

$$\text{i.e.} \quad \frac{C(V_d + V_{CR})^2}{2\, L_d I_{do}} \simeq \frac{R'_d\, I_{do}}{L_d} \cdot \frac{1}{f}$$

$$\therefore \quad I_{do} \simeq \sqrt{\frac{C(V_d + V_{CR})^2}{2R'_d} \cdot f} \tag{4.19}$$

$$\text{i.e.} \quad I_{do} \simeq k\sqrt{f} \quad \text{where } k = \sqrt{\frac{C(V_d + V_{CR})^2}{2R'_d}} \tag{4.20}$$

It may be seen, therefore, that at the higher frequencies I_{do} becomes approximately proportional to the square root of frequency. The value of L_d would appear to have little or no effect upon the constant of proportionality, k. At these higher frequencies the value of I_{do} is quite independent of load.

The variation of δ may now be found by using the approximate expression given in equation (4.12) and substituting the value of I_{do}

obtained from equation (4.19)

$$\text{i.e. } \delta \simeq \frac{C\,V_{CR}}{I_{do}}$$

$$\simeq \frac{C\,V_{CR}}{\sqrt{\left\{\dfrac{C(V_d + V_{CR})^2}{2\,R'_d}\right\}}} \cdot \frac{1}{\sqrt{f}}$$

$$\text{i.e. } \delta \simeq \frac{\sqrt{2\,CR'_d}}{1 + \dfrac{V_d}{V_{CR}}} \cdot \frac{1}{\sqrt{f}} \qquad (4.21)$$

i.e. At the higher frequencies δ is approximately inversely proportional to frequency and is independent of L_d and the load. Equations (4.20) and (4.21), it should be emphasized, are valid only when the frequency is high enough for I_{do} to become independent of the load

4.6.3 Comparison between Observed and Predicted Variations of I_{do} and δ with Frequency.

The circuit was tested over a range of frequency under four operating conditions with V_d, V_{CR} and C kept constant. Two values of L_d and load resistance R were used. At each chopping frequency the values of I_{do} and δ were measured on an oscilloscope and Figs. 4.11 and 4.12 show the observed variations of I_{do} and δ respectively with frequency.

In Fig. 4.11 it is seen that at the lower frequencies I_{do} remained

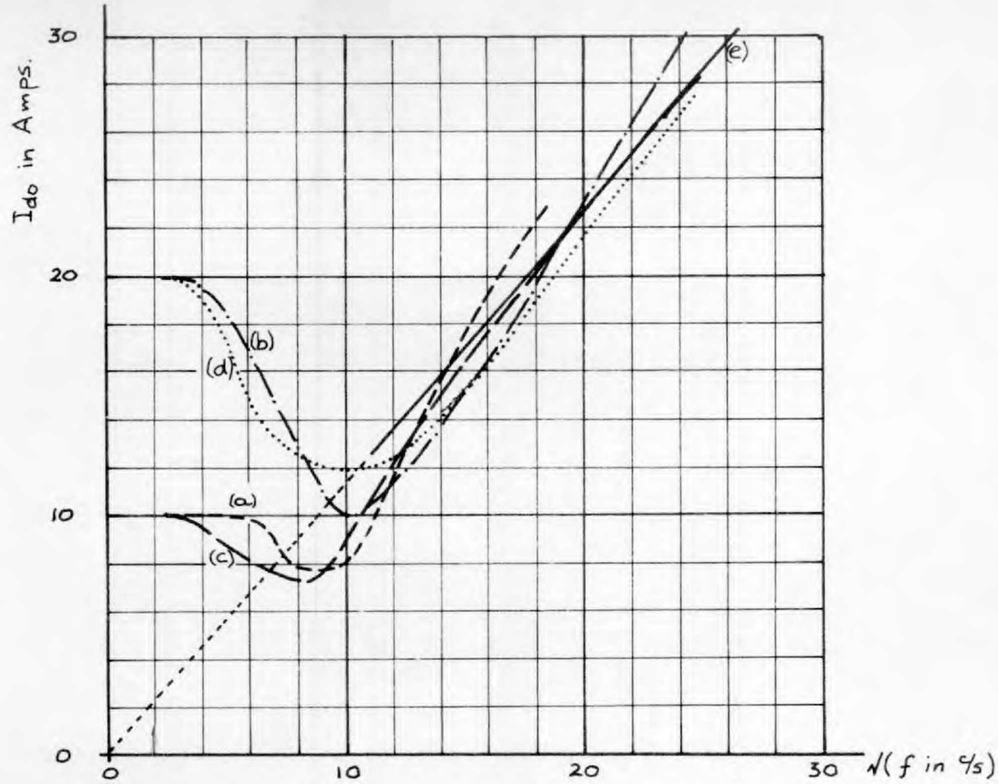


Fig. 4.11: Variation of I_{do} with frequency.*

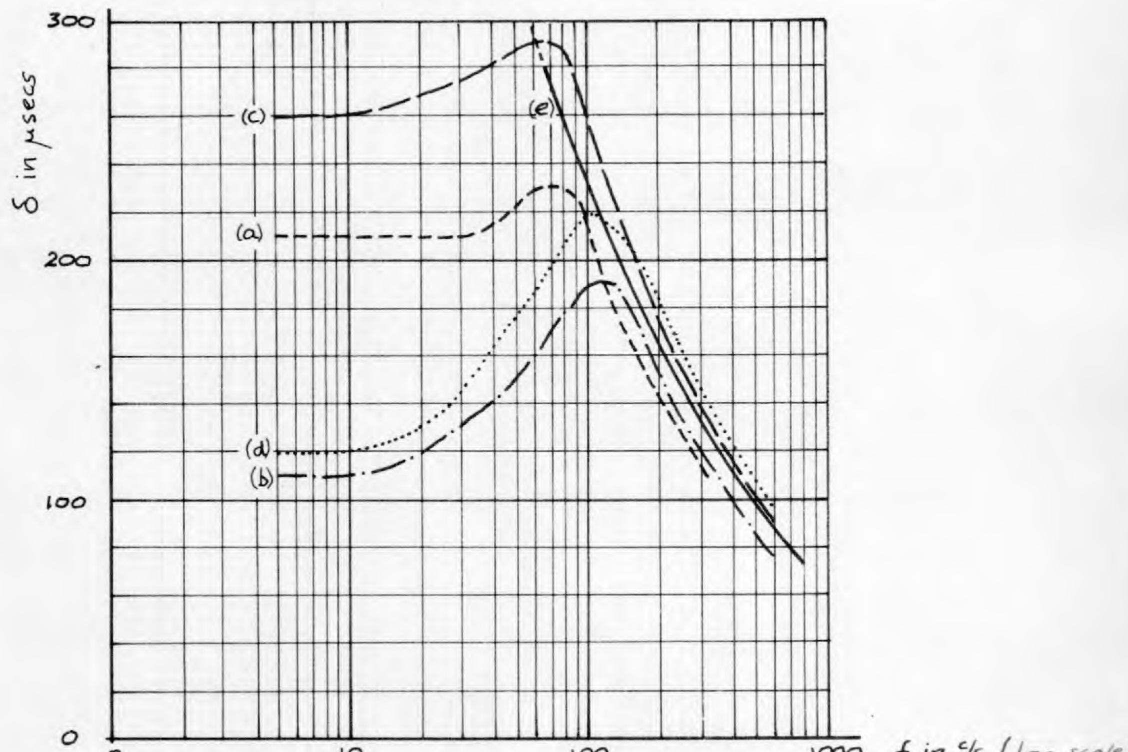


Fig. 4.12: Variation of δ with frequency *

* $V_d = 50v$, $V_{CR} = 70v$, $C = 32\mu F$, $L = 11{\cdot}6mH$, $R_d' = 0{\cdot}18\Omega$
(a) $R = 5\Omega$, $L_d = 4mH$; (b) $R = 2\Omega$, $L_d = 4mH$; (c) $R = 5\Omega$, $L_d = 11{\cdot}6mH$;
(d) $R = 2\Omega$, $L_d = 11{\cdot}6mH$; (e) predicted curve, applicable above approx. 100c/s

constant but later fell as the frequency was increased, reaching a minimum value at a frequency of about 100 $^{c}/s$. At these frequencies I_{do} was either equal to I_{LO} or a little more than I_{LO}. At higher frequencies I_{do} rose with frequency and became approximately proportional to $\sqrt{f}$.

The two curves drawn for each value of L_d are seen almost to merge at the high frequencies. This shows that I_{do} had become independent of the load.

Despite the fact that the higher value of L_d used was almost three times greater than the lower value it is seen that the values of I_{do} for each value of L_d are not significantly different. The difference can, in fact, be attributed to the slightly greater value of R_d in the case of the higher value of L_d which caused the effective resistance R'_d of the choke and diode D_2 to be increased slightly. This shows that I_{do} was independent of the value of L_d.

The theoretical variation of I_{do} with frequency, determined from equation (4.19) is also shown in Fig. 4.11. In calculating the slope of this line the characteristics of diode D_2 were represented by an equivalent resistance which, however, changes with current. At the higher frequencies the values of I_{do} would be expected to increase at a faster rate, due partly to the fall of the equivalent resistance of diode D_2 and partly to the increasing significance of the time $\frac{\phi}{\omega}$ which would shorten the decay time of I_5 through diode D_2.

Fig. 4.12 shows the corresponding variations of δ with frequency. Since δ is approximately inversely proportional to I_{do} the variation of δ would be expected to be the inverse of that of I_{do}. It is seen that δ rises to a maximum at about 100 $^c/s$, due to the fall of I_{do}, and thereafter falls with frequency. Again it is seen that the two curves drawn for each value of L_d tend to merge at the high frequencies, demonstrating that δ had become independent of the load. It is also seen that δ was relatively unaffected when L_d was increased by a factor of three, demonstrating that δ was independent of L_d. The curve representing the theoretically predicted variation of δ with frequency is also shown in Fig. 4.12.

Due again to the fall in the equivalent resistance of diode D_2 at higher values of I_{do} and to the increasing significance of the time $\frac{\phi}{\omega}$ resulting in a shortening of the decay time, the values of δ would be expected to fall even more rapidly at higher frequencies.

In both Fig. 4.11 and Fig. 4.12 the agreement between the observed and predicted variations of I_{do} and δ with frequency is seen to be good, showing that the theory developed is valid within the conditions imposed.

4.7 Switching Losses.

When CR_1 is conducting the losses in the circuit are caused by the forward voltage drop of CR_1, the resistance, R_d of the choke, and the resistance of leads, etc. CR_1 had an almost constant voltage drop of about 1.6V when conducting and its power dissipation can therefore be found by multiplying the mean current flowing in it by 1.6V.

When CR_1 is switched off, however, the energy stored in the load inductance and in the choke L_d is left to be dissipated in paths completed by diodes D_1 and D_2. The load stored energy is mainly dissipated in the load resistance, a small amount being dissipated in D_1, but this is not considered as a loss.

The energy stored in the choke L_d is dissipated in the diode D_2 and in the choke resistance R_d and this is certainly a loss in the accepted sense. At low frequencies, when the current in the choke decays completely from $\hat{I}$ to zero, the energy loss E_d is given by

$$E_d = \tfrac{1}{2} L_d \hat{I}^2$$

$$= \tfrac{1}{2} L_d \left(I_{do}^2 + \frac{C(V_d + V_{CR})^2}{L_d}\right)$$

$$= \underline{\tfrac{1}{2} L_d I_{do}^2 + \tfrac{1}{2} C(V_d + V_{CR})^2} \text{ joules} \qquad (4.22)$$

At a chopping frequency f $^c/s$ this represents a lower loss P_d given by

$$P_d = E_d \cdot f$$

$$= \underline{\tfrac{1}{2} L_d .f. I_{do}^2 + \tfrac{1}{2} Cf(V_d + V_{CR})^2} \text{ Watts} \qquad (4.23)$$

At these low frequencies $I_{do} = I_{LO}$, i.e. the load current being switched off.

At higher frequencies, where I_{do} is independent of load, the decay time is short enough for the current in L_d to rise from I_{do} to $\hat{I}$ and decay back to I_{do} only. The energy dissipated in this case is given by

$$E_d = \tfrac{1}{2} L_d (\hat{I}^2 - I_{do}^2)$$

$$= \tfrac{1}{2} L_d \left(I_{do}^2 + \frac{C(V_d + V_{CR})^2}{L_d} - I_{do}^2\right)$$

$$= \underline{\tfrac{1}{2} C(V_d + V_{CR})^2} \quad \text{Joules} \tag{4.24}$$

This then represents a power loss given by

$$P_d = \underline{\tfrac{1}{2} C.f(V_d + V_{CR})^2 \quad \text{Watts}} \tag{4.25}$$

i.e. For given values of C, V_d and V_{CR} the power loss is proportional to frequency.

In addition, there is a loss in the resistor R_c in the auxiliary circuit which can be minimised by making R_c as small as possible.

It should be noted that the formulæ for P_d take into account the power taken from the auxiliary supply in re-charging capacitor C to the negative voltage $- V_{CR}$ and also the power taken from the main supply during the turning off of CR_1, i.e. the period in which the current in the choke rises from I_{do} to $\hat{I}$.

4.8 Conclusions.

The tests carried out on the d.c. switch as described above have shown that the circuit provides a very effective method of turning on and off the d.c. supply to an inductive load. By charging the capacitor from a fixed auxiliary voltage supply and isolating it from the load during turn off it was found that the nature of the load had no effect upon the ability of the switch to turn off. Consequently the circuit was equally suitable for highly inductive as well as resistive loads. It was possible also to use a relatively small capacitor since the capacitor was not called upon to absorb any of the load stored energy at turn off.

The other novel feature of the circuit was the use of diodes to provide decay paths for inductive stored energy. These diodes were found to be very successful and made possible not only the use of a small capacitor but also the elimination of severe switching transients.

It has been shown that the theory developed for the circuit was valid and capable of predicting the circuit's performance to a high degree of accuracy. From the theory, and verified by experiment, it was found that δ was approximately equal to $\frac{CV_{CR}}{I_{do}}$ and so by adjusting the values of C and V_{CR} it was possible to obtain any required value of δ for each value of I_{do}.

At low chopping frequencies I_{do} was equal to I_{LO}, the load current at turn off. At higher frequencies, after an initial reduction due to the change in the waveform of the load current, I_{do} increased in proportion to the square root of frequency. This resulted in a corresponding decrease in the value of δ. The increase in I_{do} was shown to be due to the effect of D_2 which limited the rate of decay of the current trapped in the choke L_d after each turn off. This resulted in the build up of a circulating current in the L_d - D_2 path to a level where the energy absorbed by L_d at each turn off was dissipated in the choke resistance R_d and the diode D_2 in each switching cycle.

The energy dissipated in R_d and D_2 was the sum of the energy taken from the auxiliary supply by the capacitor during re-charging and the energy taken from the main d.c. supply immediately after the turn off of CR_1. At low chopping frequencies, or when the circuit was used intermittently as a d.c. contactor, the energy lost in this way would be unimportant. At higher frequencies, however, the energy loss, repeated in each switching cycle, could represent a substantial power loss and consequent reduction in operating efficiency.

It was seen that the value of L_d had very little effect upon the magnitude of δ and I_{do}. Obviously L_d could not be made zero, otherwise the capacitor would charge instantly from the main d.c. supply and result in too short a reverse bias time for CR_1 to turn off correctly. However, provided that L_d was sufficiently large to prevent $\hat{I}$ from becoming very much larger than I_{do}, the value of L_d was relatively unimportant. It was found that the values of I_{do} at high frequency were reduced by increasing L_d but this was attributed not to the increase in L_d but to the accompanying small increase in the winding resistance of the choke.

Reduction of the magnitude of I_{do} at high frequencies, to increase δ without altering V_{CR} and C, was possible by adding resistance in series with D_2. This caused the decay of the current trapped in L_d to become more rapid or, in other words, enabled the energy absorbed in L_d at each turn off to be dissipated in a higher resistance at a lower current level. Such reduction of I_{do} would enable a reduction in the value of C or V_{CR} to be made which would result in a smaller energy loss and further reduction in I_{do}.

Although the study of the d.c. switch was mainly to assess the suitability of the turn off technique for inversion, the circuit has many uses in its own right. Two examples are the voltage control of a d.c. motor and the checking of S C R turn off times. Voltage control can be effected by varying the ratio of the on and off periods so as to vary the mean output voltage from a very low value to full supply voltage. S C R turn off times can be measured by connecting the S C R to be checked in place of CR_1 and measuring δ on an oscilloscope. By increasing the load current, or by reducing V_{CR}, the value of δ at which the S C R just fails to turn off can be found.

It is clear at this stage that in an inverter using the turn off method described above, the power loss due to cummutation will prove to be a serious problem. This will be shown in Chapters 5 and 6. In a d.c. switch other equally effective but more efficient circuits[1,2,3] could be used which would avoid the commutation loss altogether.

CHAPTER 5

PRINCIPLE AND THEORY OF OPERATION OF A "D.C.-COMMUTATED THREE-PHASE INVERTER" WITH A SERIES R-L LOAD.

In the conclusions on Chapter 3 a comparison was made between an inductive load fed from the basic three phase inverter circuit and from an ordinary three phase sinusoidal supply. It was appreciated that in the case of the sinusoidal supply it was possible for power to flow instantaneously both from and to the supply whereas in the case of the inverter this was not so because of the unidirectional characteristics of the rectifiers. To obtain inverter output voltage and current waveforms which were not far distorted from sinewaves it was therefore necessary to use capacitors on the output side of the inverter to absorb the reverse power flow from the load. It was pointed out that this was tantamount to correcting the load power factor to unity and that it was necessary to vary the capacitance with load and frequency.

Smaller capacitors could be used merely to effect commutation but their use resulted in highly distorted output waveforms and large oscillations initiating at each commutation. Another shortcoming of the basic inverter circuit was the variation of voltage on the commutating capacitors. This sometimes resulted in failure of the commutation process. For reliable commutation it was concluded that a method should be employed for charging the commutating capacitors to a fixed voltage before each commutation. Such a method is known as "forced commutation", as opposed to "artificial commutation" in which the current and voltage waveforms are distorted to effect commutation by means of some component which is part of the inverter load.

In the next three chapters is described an inverter circuit which satisfies the requirements statedabove. A reverse diode bridge is used to permit a two-way flow of power through the circuit and for commutation a single capacitor, charged to a fixed voltage from an auxiliary supply, is discharged into the d.c. side of the inverter. The auxiliary circuit is that used for the d.c. switch described in Chapter 4.

This chapter deals with the principle and theory of operation of the inverter circuit with a star-connected R-L load. Chapters 6 and 7 deal with experiments carried out on the circuit with an R-L and an induction motor load.

5.1 Circuit and Principle of Operation.

Fig. 5.1 shows the circuit of the inverter. The S C R's CR_1, CR_2... CR_6 are connected in a three phase bridge, input lines being connected to the bridge at the common anode connection of CR_1, CR_3, CR_5 and the common cathode connection of the CR_4, CR_6, CR_2, and output lines to the cathodes of CR_1, CR_3, CR_5 as in the basic bridge circuit. For symmetry the choke is split into two halves, L_d each, one in each line from the main d.c. supply, and to ensure equal voltage sharing the two halves are wound on a single core. Diodes D_1, D_2... D_6 are connected between each output terminal and each main d.c. supply terminal in such a way that they are normally non-conducting and would only return current from the load to the supply. Diodes D_7, D_8 are connected,

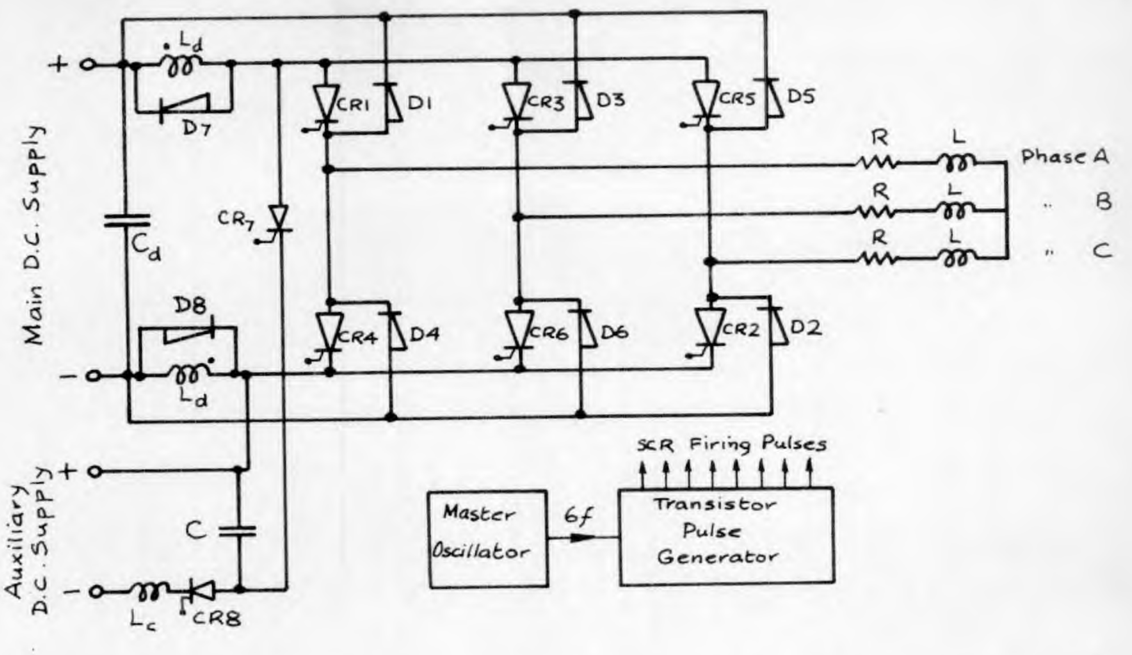


Fig. 5.1: Circuit of "d.c. commutated three phase inverter".

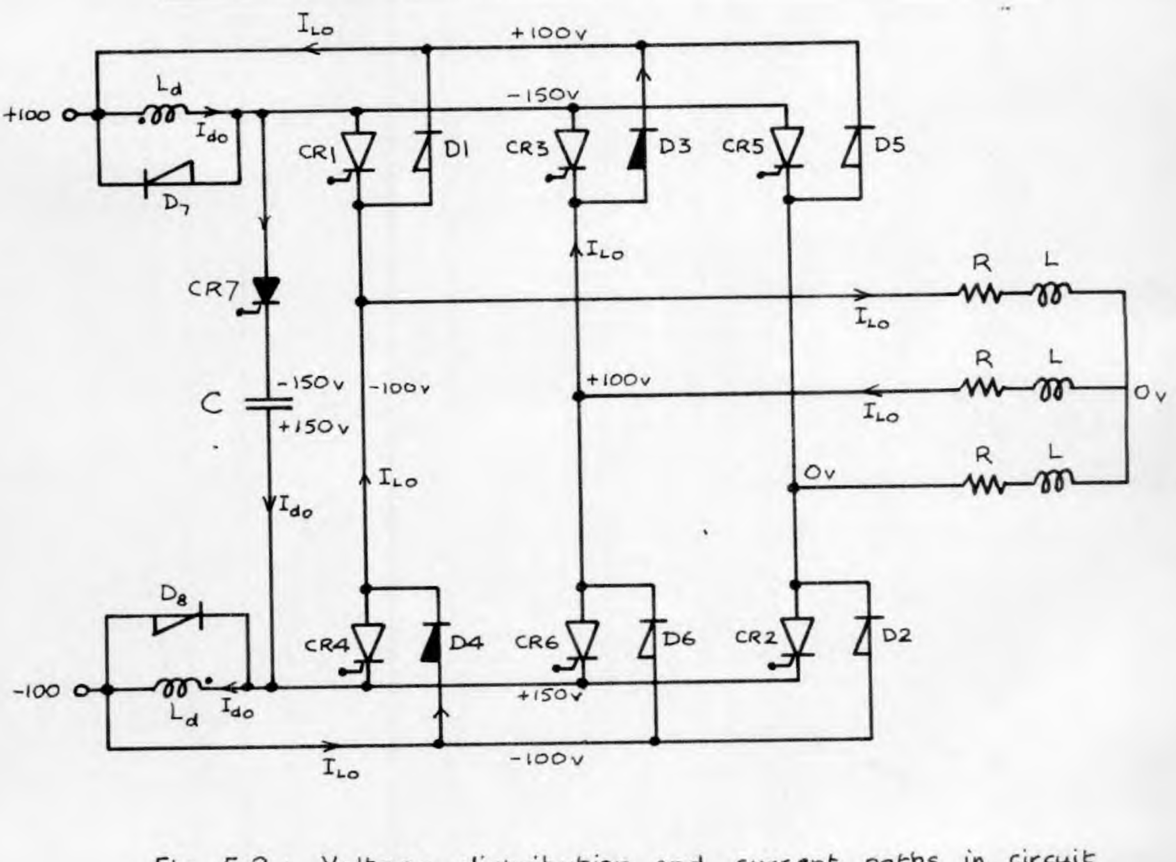


Fig. 5.2: Voltage distribution and current paths in circuit at instant of firing CR7.

(& conducting ; & non-conducting)

one across each half of the choke in the d.c. lines, so that they, too, are normally non-conducting. C_d is a large reservoir capacitor connected across the main d.c. supply to suppress the transient effects of the supply impedance during sudden current changes. R and L are the resistance and inductance of each phase of the star-connected three-phase load.

Capacitor C is charged from the auxiliary supply through CR_8. L_c is the inductance of the auxiliary supply. CR_7 is used to connect the negatively charged capacitor C between the input terminals of the bridge so as to turn off the bridge S C Rs for commutation.

The S C Rs are fired in the correct sequence by pulses fed to them from a transistor pulse generator. The frequency of the pulses from the generator is governed by an input signal from a master oscillator, the output frequency of which can be varied at will. The pulse generator is briefly described in section 5.2.

V_d and V_a are the voltages of the main and auxiliary d.c. supplies. (Both supplies were taken from d.c. generators and could be varied as required.)

In its principle of operation the inverter is a combination of the basic three phase bridge inverter and the d.c. switch. Each of the bridge S C Rs conducts for one third of a cycle as in the basic circuit and the inverter therefore gives the same basic output current and voltage waveforms as the basic circuit of Chapter 3. In each sixth of a cycle capacitor C is charged to a negative voltage from the auxiliary supply by firing CR_8. Because of the auxiliary supply inductance L_c the voltage on the capacitor overshoots the value $-V_a$ and at the peak of the overshoot, at a voltage $-V_{CR}$, the charging current tends to reverse but is prevented from doing so by CR_8. Capacitor C therefore remains at the voltage $-V_{CR}$ and CR_8 turns off, being reverse biased by the difference between V_{CR} and V_a.

At the end of each sixth of a cycle, when commutation is required to take place, CR_7 is fired. This connects the negatively-charged capacitor C between the input terminals of the bridge, causing all the S C Rs in the bridge to become reverse biased and, therefore, turns off the two S C Rs which were conducting. The instantaneous difference between the main d.c. supply voltage V_d and the capacitor voltage $-V_{CR}$ is sustained by the chokes in the d.c. lines and is shared equally between them. However, the load is inductive and the currents in the two phases which had been supplied through the two conducting S C Rs are now forced to flow through two of the diodes in the reverse diode bridge and hence back to the supply.

Fig. 5.2 shows the distribution of current and voltage in the circuit at the instant of firing CR_7 for a case in which V_d = 200 V and V_{CR} = 300 V. CR_1 and CR_6 had been conducting immediately before and CR_2 is about to be fired. I_{LO} is the current which had been flowing in phases A and B of the load (it will be seen later that the current in phase C at this instant would be zero under most conditions) and I_{do} the current in the chokes L_d.

Since the difference between the supply and capacitor voltages is shared equally between the two halves of the choke the voltages on the plates of the capacitor must be -150 V and +150 V if the supply terminals are at +100 V and -100V. The common anode connections of CR_1, CR_3 and CR_5 must therefore be at a voltage -150 V while the common cathode connections of CR_4, CR_6 and CR_2 must be at +150 V. The current in phase A flows through diode D_4, the current in phase B through D_3, and lines A and B are therefore at voltage -100 V and +100 V respectively. Since the same current flows in phases A and B and none in phase C the load star point and hence line C must be at zero voltage. It can be seen that CR_1 and CR_6, the S C Rs which had been conducting, are reverse-biased by only 50 V or half the difference between V_{CR} and V_d, and are only reverse-biased while the capacitor voltage is greater than V_d. CR_3 and CR_4 are reverse-biased by 250 V, i.e. $\frac{1}{2}(V_d + V_{CR})$, and CR_2 and CR_5 by 150 V, or $\frac{1}{2}V_{CR}$.

The capacitor eventually charges to the voltage $+V_d$, at which point diodes D_7 and D_8 conduct to prevent the capacitor voltage from rising further. CR_7 then turns off and the currents in the two halves of the choke decay through D_7 and D_8. Having turned off the S C Rs in the bridge it now remains to fire the two S C Rs which are required to conduct in the next sixth of a cycle, i.e. CR_1 and CR_2 in the case considered above. CR_8 must also be fired at some stage to re-charge the capacitor to $-V_{CR}$ ready for the next commutation.

The current in phase B now continues to decay through diode D_3 towards zero, during which period the star point of the load is no longer at zero voltage. When the current in phase B reaches zero the currents in the other two phases become equal and rise together thereafter towards their steady values.

5.2 Pulse Generator.

5.2.1 Pulse Schedule.

In Fig. 5.3 the pulse required for controlling each of the S C Rs in the circuit are shown. At the end of each sixth of a cycle a single pulse of short duration is all that is required to fire CR_7 and so turn off the bridge S C Rs. At some point in the middle of each sixth of a cycle a short pulse is applied to the gate of CR_8 to re-charge the commutating capacitor from the auxiliary supply. Under some circumstances it is possible for the current in the bridge S C Rs to fall to zero and for the S C Rs to become reverse-biased temporarily. Gate drive is therefore required over the whole of the conduction period of one third of a cycle. Partly because of the difficulty in passing rectangular pulses through small output transformers at low frequencies, and partly because of the necessity for keeping the mean gate voltage as small as possible during reverse-bias of the S C R, the gate drive for each bridge S C Rs consists of a high frequency pulse train, as shown in Fig. 5.4. The pulses in the train are 20 μSecs long, 140 μSecs apart, and have a magnitude of about 2 V. The mean gate voltage is thus kept at the 0.25 V recommended maximum during reverse-bias conditions and the drives for the S C Rs can be isolated from each other by using relatively small output transformers in the pulse generator. Each pulse train is of one third of a cycle duration, commencing at instant t_1 for CR_1, t_2 for CR_2 and so on.

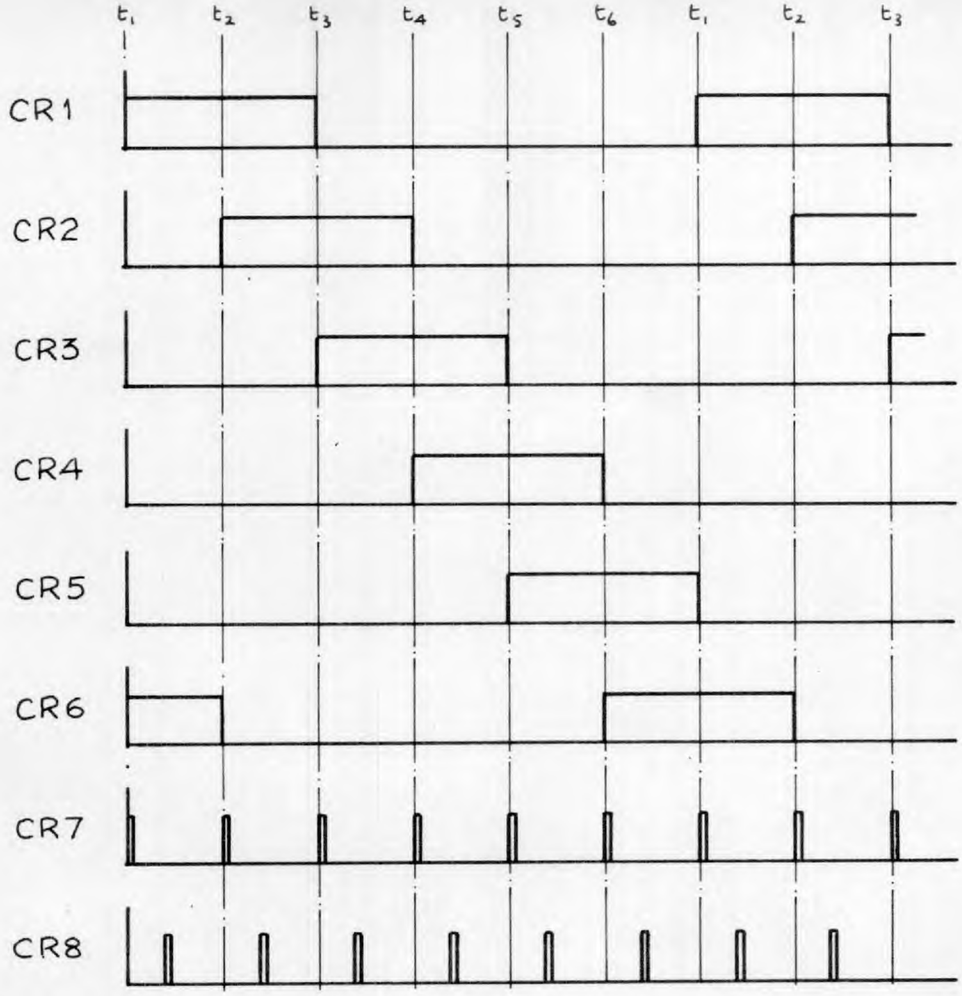


Fig. 5.3: Pulse schedule required from pulse generator.

Fig. 5.4: Form of pulse train applied to the SCRs in bridge during conduction.

The 20μ Secs pulse duration was long enough to allow the current in each S C R to rise above the holding current with the inductive inverter loads used.

5.2.2 Principle of Operation.

Fig. 5.5 shows in block diagram form the layout of the components of the pulse generator.

A signal from the master oscillator is fed with a wave shaper and thence into a scale of six ring counter. For each input cycle a pulse is produced at one of the ring counter output terminals in sequence, and the ring counter output pulse frequency is therefore one sixth of the oscillator frequency. Six pulse train gating circuits, one for each bridge S C R, are connected to the ring counter as shown. A pulse at the "N" terminal opens the gate, a pulse at the "F" terminal closes the gate. When the gate is open the pulse train from the pulse train oscillator is passed to the S C R gate. The "P" terminal is the input for the pulse train. The "N" terminal of the gating circuit for CR_1 is connected to ring counter output 1 and the "F" terminal to output 3. Consequently the gating circuit for CR_1 passes the pulse train to CR_1 between the appearances of pulses at ring counter outputs 1 and 3, i.e. for one third of a cycle. The other gating circuits operate similarly, displaced by the appropriate number of sixths of a cycle.

For CR_7 a pulse is required at the start of each sixth of a cycle. All the ring counter outputs are therefore connected to an OR gate and

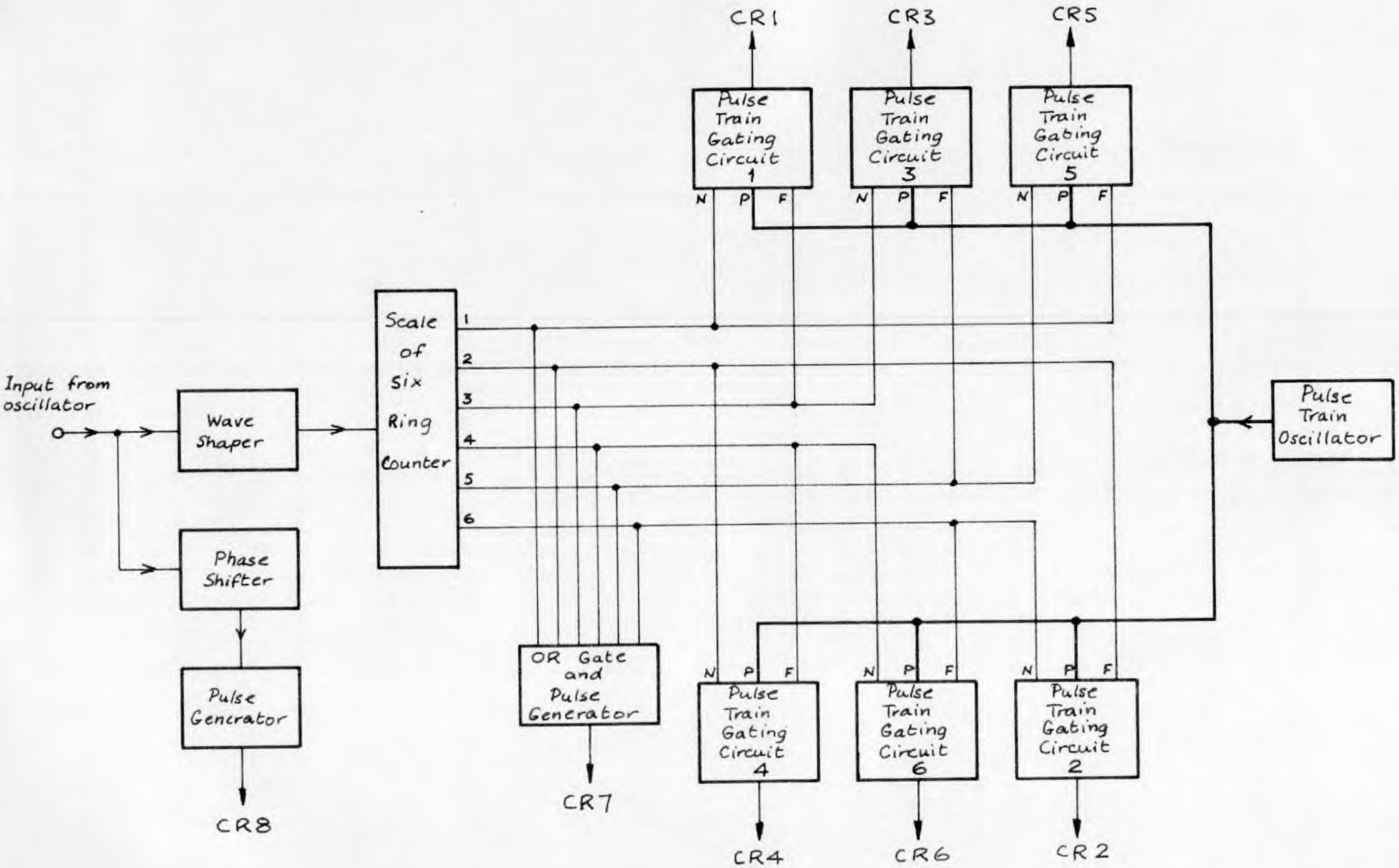


Fig. 5.5: Block diagram of pulse generator.

a pulse is then supplied to CR_7 each time a pulse appears at any of the ring counter output terminals.

CR_8 requires a pulse each sixth of a cycle but between the pulses fed to CR_7. The master oscillator signal is therefore passed through a phase shifter, to allow adjustment of the pulse positioning, and thence to a pulse generator which produces a pulse each sixth of a cycle.

All the output pulses fed to S C Rs are electrically isolated from each other by means of small output transformers.

5.3 Theory of Operation on Star-Connected R-L Load with "Power Factor" > 0.5 (approx.).

5.3.1 Basis of Theory and General Assumptions made.

In the following theory it is assumed, unless otherwise stated, that the S C Rs and diodes can be regarded as open circuits between anode and cathode (i.e. zero leakage current) when non-conducting and as short circuits (i.e. zero voltage drop) when conducting.

The load for which the circuit is analysed is a star-connected load in which each phase consists of resistance R and inductance L in series. Magnetic coupling between phases is assumed to be absent. Most loads in practice have a power factor greater than 0.5. Since the theory for very low power factor loads is slightly different it is left over until section 5.4. The difference between the two cases is that for high power factor loads current flows in only two phases at the end of each sixth of a cycle whereas in the low power factor case all three phases carry current. The actual value of power factor at which the transition takes place depends upon the commutation process to some degree but would normally be of the order of 0.5. In the section heading "power factor" is written between quotation marks because the power factor in the inverter circuit, as will be seen later, cannot be specified in the same way as in a system supplied by sinusoidal voltage and current.

The method of analysis used is to consider one sixth of a cycle only, to begin the analysis at the start of this period when certain S C Rs and diodes are known to conduct, and to use known or assumed initial current and voltage values. Voltage and current equations can then be formulated which are valid until the current or voltage associated with any S C R or diode reverses or tends to reverse. The resulting change in the circuit is then taken into account and new equations formulated, using new initial current and voltage values. This procedure is repeated until the end of the sixth of a cycle is reached. From the current and voltage variations in this single sixth of a cycle the complete waveforms etc. can then be determined.

It is assumed throughout that the main d.c. supply has no impedance and that the supply voltage therefore suffers no fluctuations under transient conditions. The reservoir capacitor C_d is considered as part of the supply and ignored in the theory.

In the practical circuit R-C filters were connected across each S C R to suppress transient voltage peaks and a small air-cored choke was connected in series with the commutating capacitor to limit the reverse current peak in the S C Rs being turned off. The effect of these components was small and is neglected in the theory.

The sixth of a cycle chosen for study in the analysis is that occurring between instants t_2 and t_3. At t_2 CR_6 is turned off and CR_2 turned on instead, commutation therefore taking place between phases B and C of the load.

5.3.2 States of Circuit in the Sixth of a Cycle.

After CR_7 is fired to turn off the bridge S C Rs at the start of the sixth of a cycle the state of the circuit, i.e. the position of conducting S C Rs and diodes, changes several times. The states of the circuit as they occur are shown in Figs. 5.6 to 5.13. In these diagrams the arrows indicate current flow, the voltage distribution is indicated by numerical values which give potentials as percentages of half the d.c. supply voltage, and the letters R and F indicate which S C Rs and diodes are reverse-biased and forward-biased respectively.

State 1 :- CR_7 conducting, all bridge S C Rs off, $V_c < - V_d$.

The circuit is arranged so that when CR_7 is fired the voltage V_c on the capacitor C is greater than and opposite to the main d.c. supply voltage V_d. The state shown in Fig. 5.6 therefore occurs with all the bridge S C Rs reverse-biased and turned off. Since the two halves of the d.c. choke are tightly coupled the voltage drops across each are the same. The current flowing in phases A and B decays at such a rate that D_3 and D_4 are forced to conduct. It will be shown later that the current in phase C would be zero at this time for a high power factor

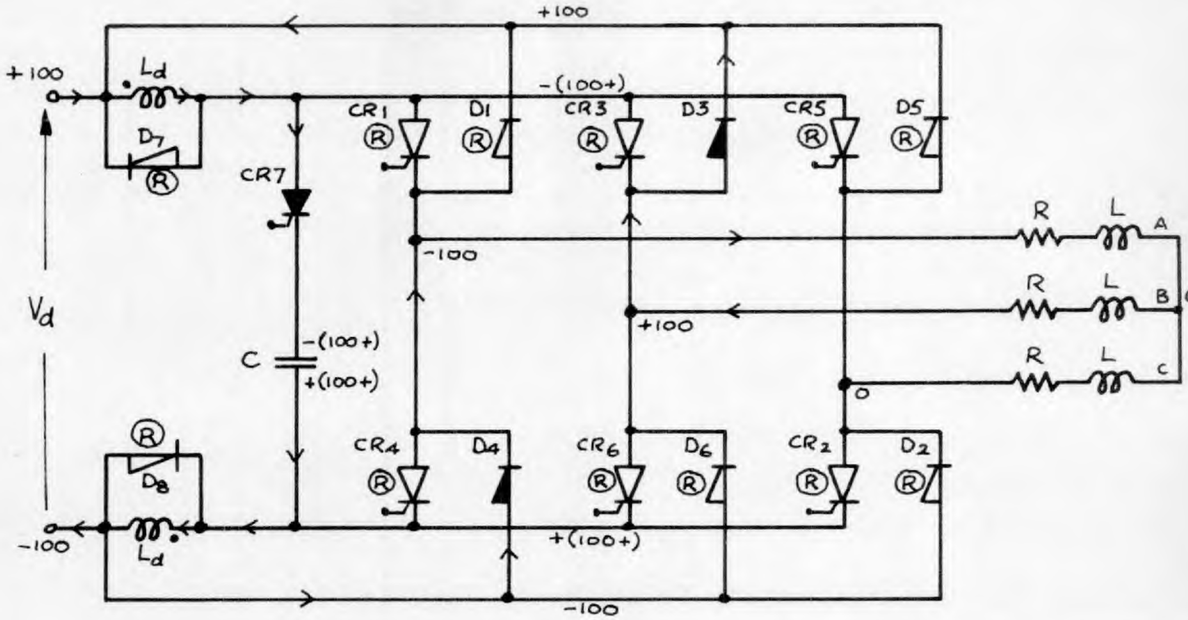
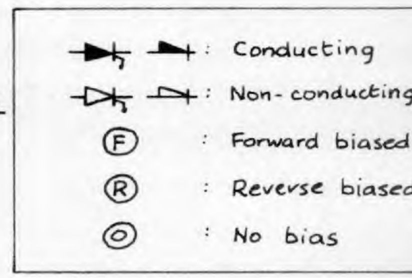


Fig.5.6 : Distribution of voltage and current.
State 1 : CR7 conducting and $(-V_c) > V_d$



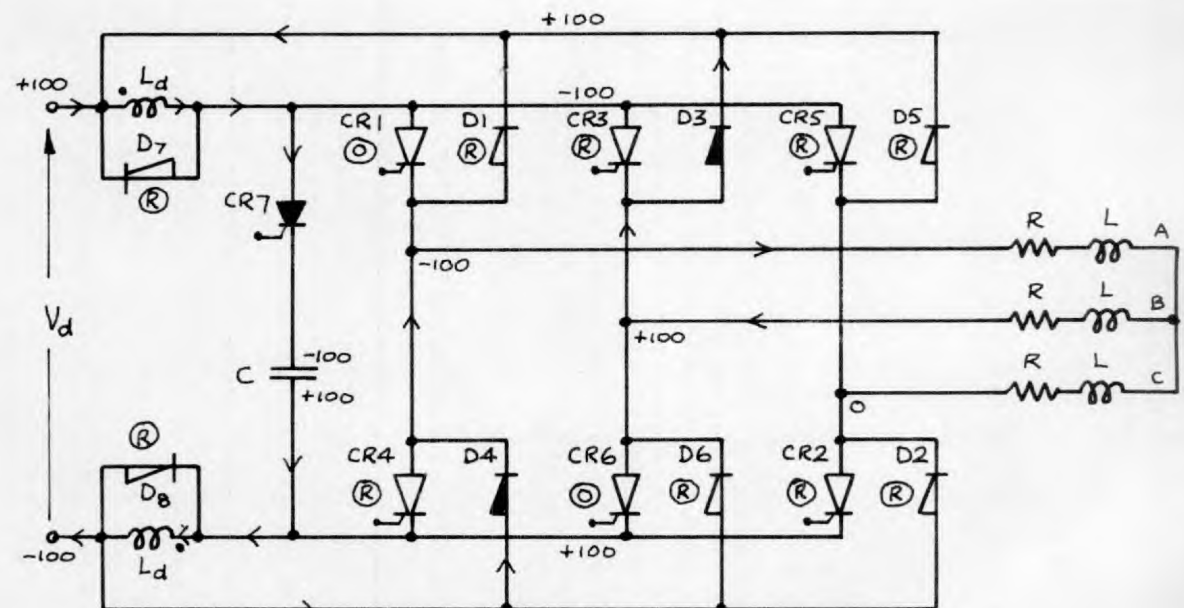


Fig. 5.7 : Distribution of voltage and current.
Transition from state 1 to state 2 : CR7 conducting and $(-V_c) = V_d$.

load. Current flows from the d.c. supply through the d.c. chokes and into capacitor C causing its voltage to rise towards the d.c. supply voltage.

This state is maintained at least until V_c reaches the value $(-V_d)$. At this instant it is seen from Fig. 5.7 that the voltages across CR_1 and CR_6 are zero and any further rise of V_c would make these two S C Rs become forward biased. However, no gate signal is applied to CR_6 and this S C R would remain off though forward biased. CR_1, on the other hand, is required to conduct again and will conduct as soon as the first pulse in the pulse train is applied to its gate. When CR_1 conducts again the circuit changes to the next state, described below.

State 2 :- CR_7, CR_1, D_3 conducting, $V_c > -V_d$.

Fig. 5.8 shows the circuit when V_c has risen above $(-V_d)$ and CR_1 has turned on. It is seen that D_4 becomes reverse-biased and therefore turns off. This means that the current which had flowed through D_4 is suddenly transferred to CR_1 and hence must flow through the upper half of the d.c. choke. Because the two halves of the choke are tightly coupled this instantaneous increase of current in one half is possible and is balanced by an equal decrease in the other half, the condition to be obeyed being that the sum of the currents in the two halves must be instantaneously unchanged. However, this means that the current flowing into the capacitor is now reduced and the rate of rise of V_c is therefore reduced.

It should be noted that because the currents in phases A and B

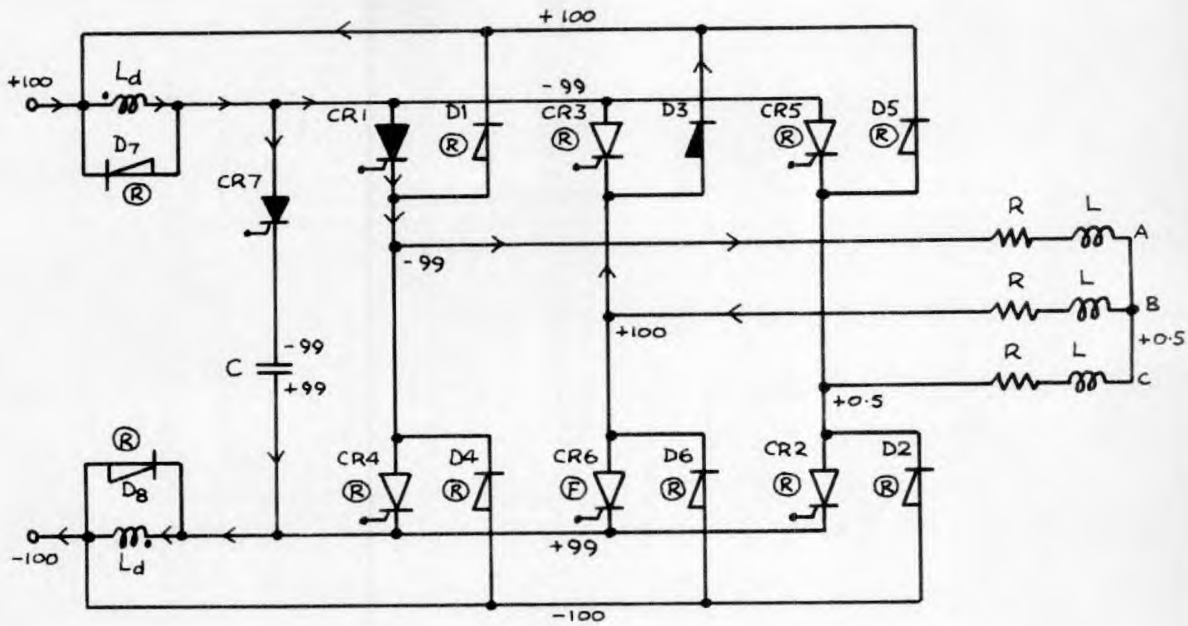
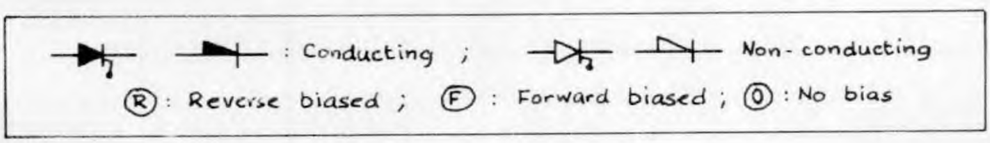


Fig. 5.8: Distribution of voltage and current.

State 2: CR_7 conducting and $(-V_c) < V_d$. (Shown for $(-V_c) = 0{\cdot}99V_d$)



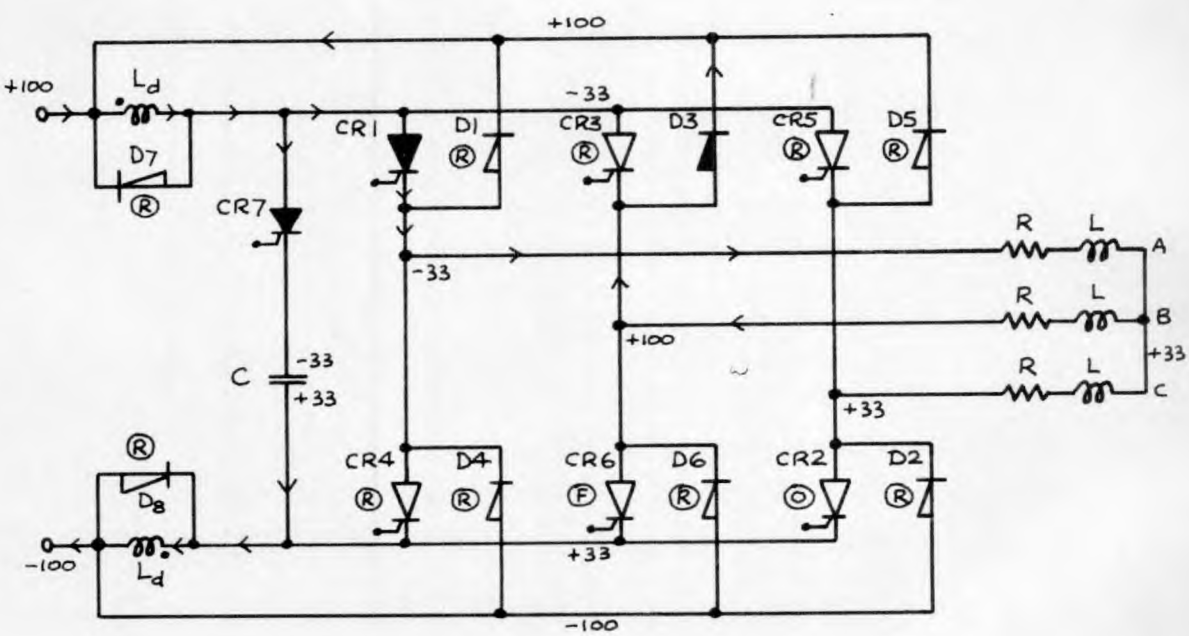


Fig. 5.9: Distribution of voltage and current.

Transition from state 2 to state 3: CR7 conducting and $(-V_c) = \frac{1}{3}V_d$

are the same the voltage at the load star point must be the mean of the voltage of lines A and B. The star point voltage is also the voltage at the anode of CR_2 since no current flows in phase C.

This state is maintained at least until V_c rises to the value $(-\frac{1}{3} V_d)$. At this instant, if CR_1 is conducting as shown in Fig. 5.9, the voltage across CR_2 becomes zero and CR_2 is therefore liable to conduct. When CR_2 conducts the circuit changes to the next state described below.

State 3 :- CR_7, CR_1, CR_2, D_3 conducting, $V_c > (-\frac{1}{3} V_d)$.

Fig. 5.10 shows what happens when V_c rises above the value $(-\frac{1}{3} V_d)$ and CR_2 conducts. No other change occurs in the circuit, all diodes apart from D_3 being reverse-biased. Current starts to rise in phase C and flows to the d.c. supply through the lower half of the d.c. choke. The current in phase B continues to flow through diode D_3, no other path being available since CR_6 has been turned off. Because V_c is still less than V_d diodes D_7 and D_8 are still reverse-biased by the equal voltage drops across the halves of the d.c. choke.

This state is maintained until the voltage V_c becomes equal to the supply voltage V_d.

State 4 :- CR_1, CR_2, D_3, D_7, D_8 conducting, $V_c = V_d$.

When V_c becomes equal to V_d diodes D_7 and D_8 conduct and prevent V_c from rising further. The capacitor charging current therefore ceases

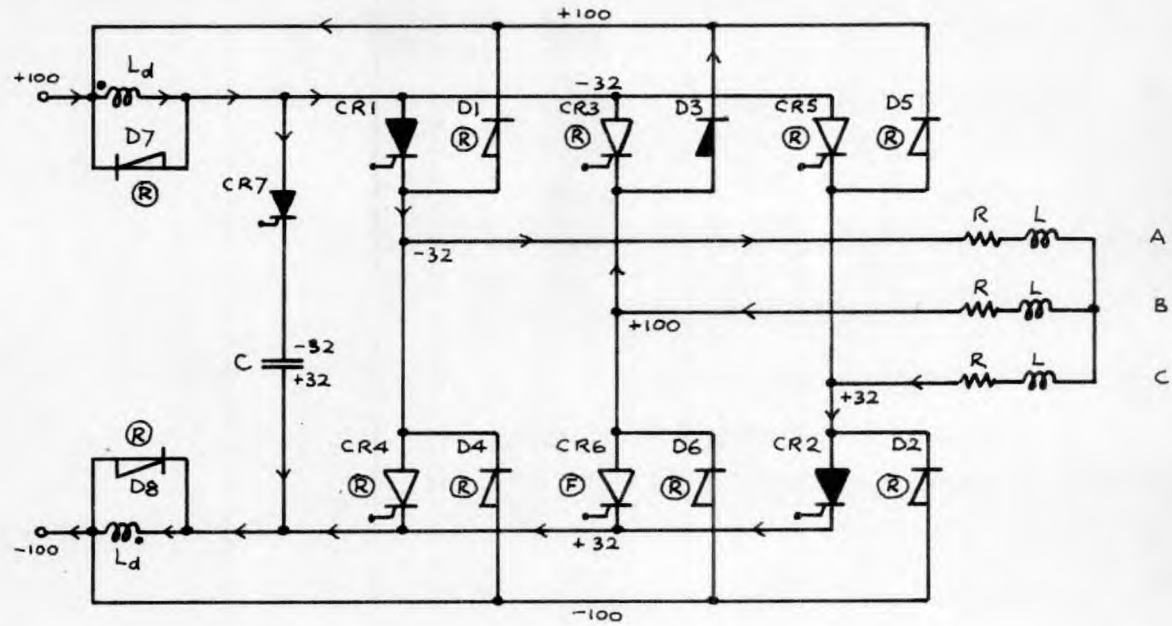


Fig. 5.10 : Distribution of voltage and current.

State 3 : CR7 conducting and $(-V_c) < \frac{1}{3}V_d$. (Shown for $(-V_c) = 0.32V_d$)

: Conducting ; : Non-conducting

(F) : Forward-biased ; (R) : Reverse-biased ; (0) : No bias

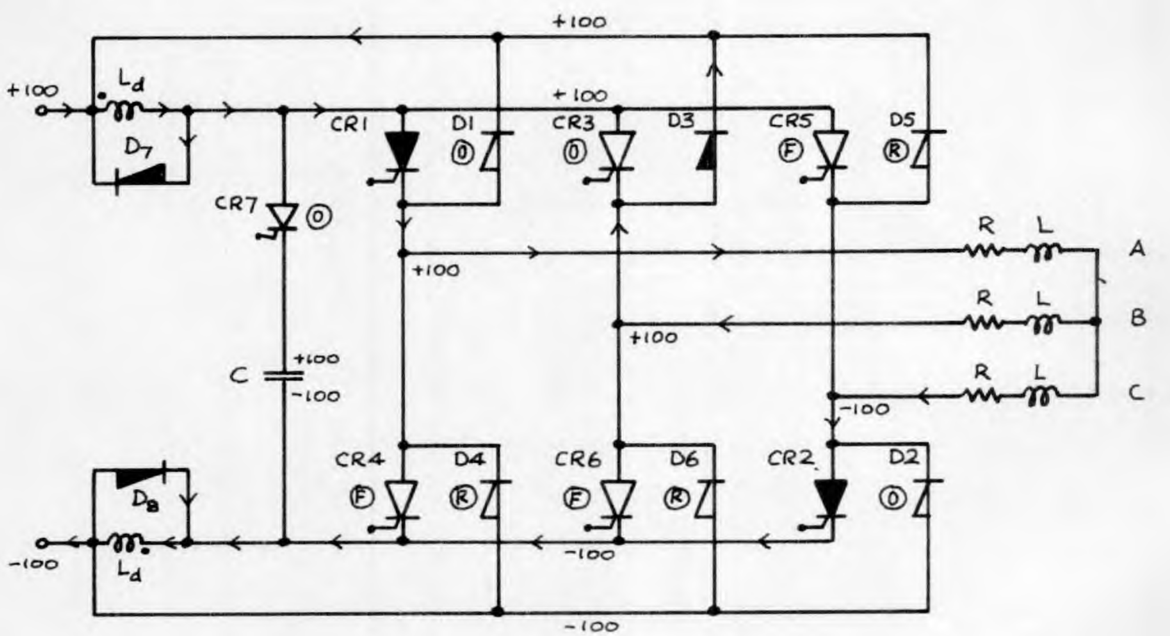


Fig. 5.11 : Distribution of voltage and current.

State 4 : $V_c = V_d$, CR7 turns off, D7 and D8 conduct.

and CR_7 turns off leaving the currents in the two halves of the choke to decay through D_7 and D_8. This is shown in Fig. 5.11.

Current continues to flow through CR_1 and CR_2 into and from the load and the current in phase B continues to decay through diode D_3 (assuming that the capacitor charging time is very short compared with the load time constants).

This state is maintained until the current in phase B reaches zero at which point diode D_3 becomes reverse-biased.

State 5 :- CR_1, CR_2, D_7, D_8 conducting, CR_7 off.

When diode D_3 becomes reverse-biased currênt flows into the load through CR_1 and CR_2 only and the current in phase B remains zero. The current in phase A is now the same as that in phase C and both rise together towards a steady state value. The currents in the two halves of the choke continue to decay through D_7 and D_8 (assuming that this decay time constant is greater than the load time constant).

This state shown in Fig. 5.12 is maintained until the currents in D_7 and D_8 become zero or until the end of the sixth of a cycle.

State 6 :- CR_1, CR_2 conducting, D_7, D_8 off.

The current flowing in each diode D_7 or D_8 is equal to the difference between the current in each half of the d.c. choke and the current in CR_1 and CR_2. If the choke current should decay to the value of the current in the load, the currents in D_7 and D_8 become zero and the choke

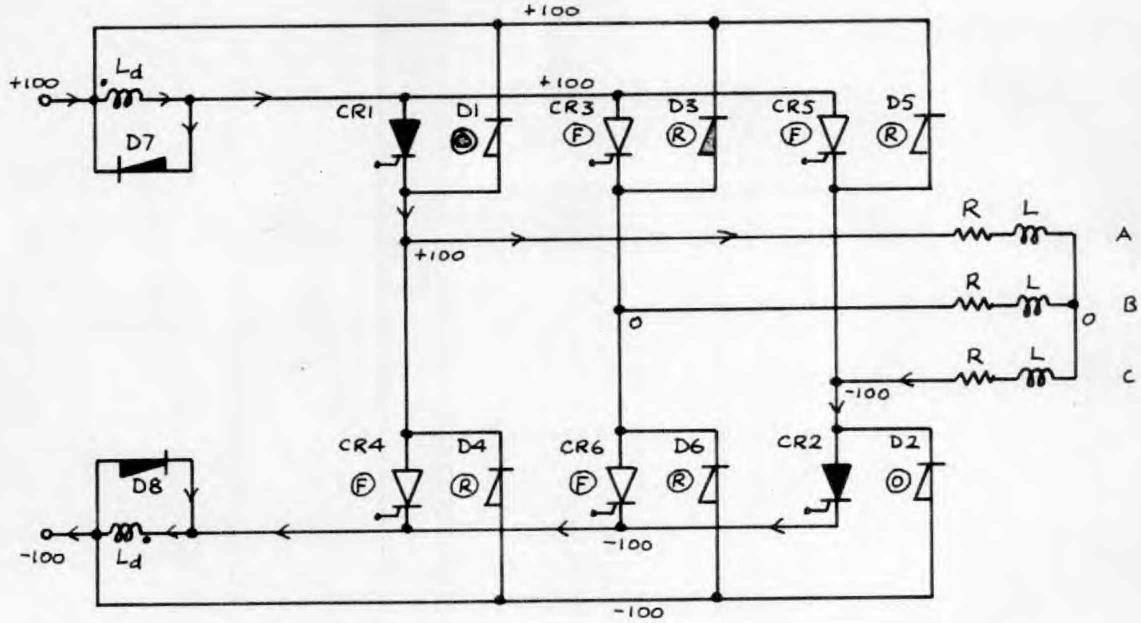
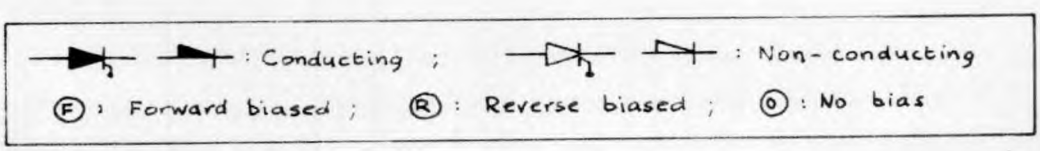


Fig. 5.12 : Distribution of voltage and current.

State 5 : D_3 has ceased conduction, D_7 and D_8 conduct.



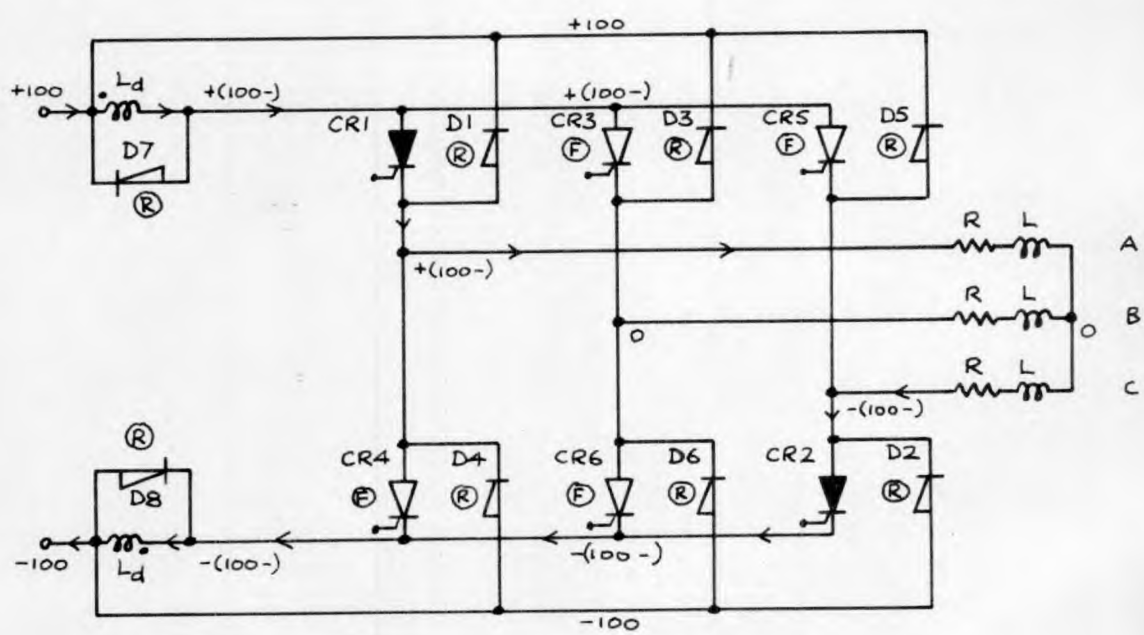


Fig. 5.13 : Distribution of voltage and current.

State 6 : D_7 and D_8 have ceased conduction.

becomes free to impede current rise again. Such a case is shown in Fig. 5.13. The impedance of the choke to current rise causes a voltage drop at the bridge terminals and D_7 and D_8 become reverse-biased.

At high frequencies it is common for the choke current always to be greater than the load current and this last state does not then occur.

5.3.3 Simplifications for Theory.

During the discharge of the capacitor C the circuit has three possible states. The first state occurs immediately when the discharge of C starts, the second state can occur at any instant after V_c reaches the voltage $-V_d$, and the third state can occur at any instant after V_c reaches the value $-\frac{1}{3} V_d$. For the analysis of each state it is necessary to find the voltages and currents at the end of the previous state in order to obtain the initial voltage and currents. Because the firing signal applied to the S C Rs consists of a train of pulses 140 μSecs apart the instant at which the circuit switches from each state to the next can vary within a range of about 140 μSecs. To analyse each state separately would not therefore be worth while and in the theory some simplifications are made.

The time occupied by the discharge of capacitor C represents a very small fraction of the sixth of a cycle and in most conditions would not be very much greater than the 140 μSecs possible variation of the firing instants of CR_1 and CR_2. The assumption is therefore made that the capacitor discharge is complete, with $V_c = V_d$ and diodes D_7 and D_8 conducting, when CR_1 and CR_2 fire together. In other words it is assumed that the circuit switches directly from the first state described in section 5.3.2 to the fourth state described in section 5.3.2.

This assumption does not involve any inaccuracy in the calculated value of δ, the time for which the bridge S C Rs are reverse-biased at turn off, since δ is calculated from the first part of the voltage variation in state 1. In state 2 the current in phases A and B would decay, the voltage applied to the two phases in series falling from - 200% to - 133% of $\frac{1}{2} V_d$ (see Figs. 5.7, 5.8 and 5.9) if CR_1 and CR_2 were to conduct at the earliest possible instants. Because of the sudden reduction in the current flowing into the capacitor when the circuit switches into state 2 the capacitor would take longer to charge from $- V_d$ to $- \frac{1}{3} V_d$ if state 2 occurred than it would if state 1 persisted. Consequently the assumption that state 2 does not occur should not produce any significant error in the amount by which the load current decays.

5.3.4 Voltage and Current Equations.

5.3.4.1 Period 1 - period of discharge of capacitor C.

Fig. 5.14 shows the parts of the circuit which are assumed to conduct during the discharge of capacitor C. Current i_d flows into capacitor C from the supply through CR_7 and the two halves of the d.c. choke. The current which had flowed in phases A and B before the firing of CR_7 now flows through D_3 and D_4 back to the supply. This current is labelled i_g and the total current taken from the supply labelled i_s.

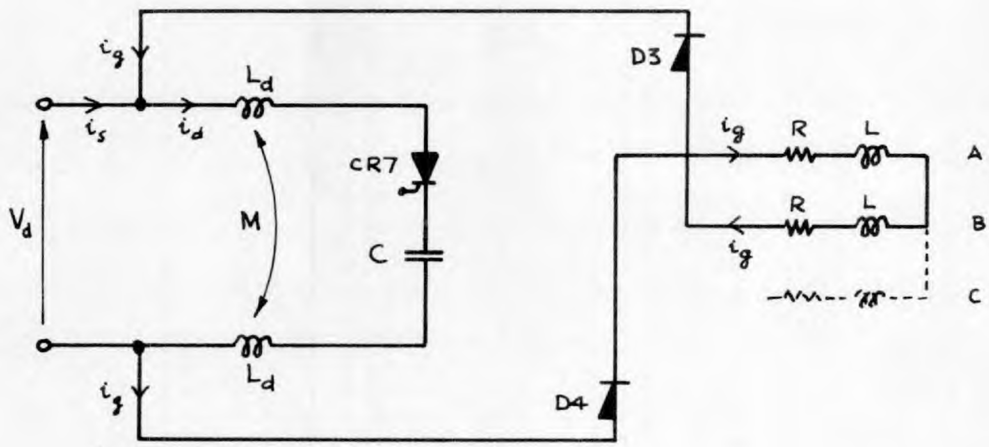


Fig. 5.14 : Conducting paths during discharge of capacitor C.

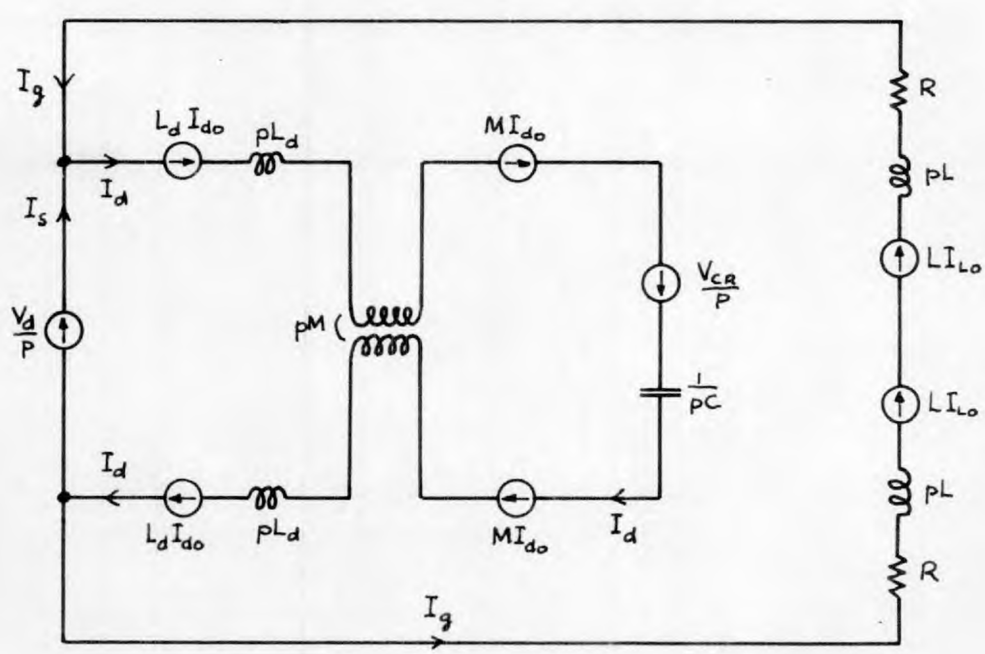


Fig. 5.15 : Operational form of circuit during period of discharge of capacitor C.

The two halves of the choke have self inductance L_d and mutual inductance M. The self inductance of each half is measured with the other half open circuited. Since it is assumed that all the flux linking one half also links the other half the coupling coefficient is unity and M is equal to $\sqrt{L_d^{\,2}}$, i.e. $M = L_d$.

Fig. 5.15 shows the circuit in its operational form with the initial current and voltage values included. V_{CR} is the initial voltage on capacitor C, I_{LO} the current flowing in phases A and B and I_{do} the current flowing in both halves of the d.c. choke at the instant of firing CR_7.

The circuit consists of two closed loops joined only at the supply terminals. Each loop can therefore be treated separately. Taking the load current I_g first,

$$\frac{V_d}{p} - 2\,L\,I_{LO} = -\,I_g(2\,p\,L + 2\,R)$$

$$\therefore\quad I_g = \frac{-\,V_d}{2\,p\,L(p + \frac{R}{L})} + \frac{I_{LO}}{p + \frac{R}{L}}$$

Inverting this equation to obtain i_g in terms of time, t, we obtain :

$$i_g = -\,\frac{V_d}{2R}\left(1 - e^{\frac{-Rt}{L}}\right) + I_{LO}\,e^{\frac{-Rt}{L}}$$

$$\text{i.e.}\quad i_a = -\,i_b = i_g = -\,\frac{V_d}{2R} + \left(\frac{V_d}{2R} + I_{LO}\right)\,e^{\frac{-Rt}{L}} \qquad (5.1)$$

i.e. i_g falls exponentially from I_{do} towards the steady state value $-\frac{V_d}{2R}$ with time constant $\frac{L}{R}$.

Now taking the capacitor current,

$$\frac{V_d}{p} + \frac{V_{CR}}{p} + 2\,L_d\,I_{do} + 2\,M\,I_{do} = I_d\,(2pL_d + 2pM + \frac{1}{pc})$$

But $M = L_d$

$$\therefore \quad I_d = \frac{\dfrac{V_d + V_{CR}}{4\,L_d} + p\,I_{do}}{p^2 + \dfrac{1}{4\,CL_d}}$$

Inverting to obtain i_d in terms of time, t, we obtain :-

$$i_d = \hat{I}\cos(\omega t - \phi) \qquad (5.2)$$

where $\omega^2 = \dfrac{1}{4\,CL_d}$

$$\tan\phi = \frac{V_d + V_{CR}}{4\omega\,L_d I_{do}} = \frac{\omega\,C(V_d + V_{CR})}{I_{do}}$$

and $$\hat{I} = \sqrt{I_{do}^{\;2} + \left(\frac{V_d + V_{CR}}{4\,\omega\,L_d}\right)^2} = I_{do}\sqrt{1 + \tan^2\phi}$$

In equation (5.2) the resistance of the d.c. choke is neglected, its effect during rapid current changes being small.

From the equation for i_d the voltage v_c across the capacitor may be found

$$v_c = -V_{CR} + \frac{1}{C}\int_0^t \hat{I}\cos(\omega t - \phi)\,dt$$

$$= -V_{CR} + \frac{\hat{I}}{\omega C}\sin(\omega t - \phi) + \frac{\hat{I}}{\omega C}\sin\phi$$

But $\sin\phi = \dfrac{\omega C(V_d + V_{CR})}{\hat{I}}$

$$\therefore\ \underline{\underline{v_c = V_d + \frac{\hat{I}}{\omega C}\sin(\omega t - \phi)}} \qquad (5.3)$$

The time δ for which CR_1 and CR_6 are reverse-biased may be found from equation (5.3). Since the voltage across CR_1 and CR_6 passes through zero when $v_c = -V_d$, $t = \delta$ when $v_c = -V_d$.

$$\therefore\ -V_d = V_d + \frac{\hat{I}}{\omega C}\sin(\omega\delta - \phi)$$

$$\text{i.e. } \underline{\underline{\delta = \frac{1}{\omega}\left(\phi - \sin^{-1}\frac{2V_d\,\omega C}{\hat{I}}\right)}} \qquad (5.4)$$

This is the exact expression for δ. Since δ is the time taken for the capacitor to charge from $-V_{CR}$ to $-V_d$ with a current, initially I_{do}, flowing into it an approximate expression for δ may be given as

$$\underline{\underline{\delta \simeq \frac{C(V_{CR} - V_d)}{I_{do}}}} \qquad (5.5)$$

Since the charging current flowing into C rises from I_{do} towards $\hat{I}$ during the charging period this approximate expression will tend to give slightly optimistic values for δ.

The voltage on capacitor C rises until it reaches the value V_d when D_7 and D_8 conduct and CR_7 turns off. The time, T_1, taken for C to charge to the voltage V_d may be found from equation (5.3). Then

$$V_d = V_d + \frac{\hat{I}}{\omega C} \sin (\omega T_1 - \phi)$$

i.e. $\sin(\omega T_1 - \phi) = 0$

or $$\underline{\underline{T_1 = \frac{\phi}{\omega}}} \tag{5.6}$$

T_1 is the period for which the first state of the circuit, that with CR_7, D_3 and D_4 conducting only, is assumed to persist.

The current flowing in the two halves of the d.c. choke at the end of this first period should be $\hat{I}$. This can be checked by putting $t = T_1$ in equation (5.2). Then

$$i_d = \hat{I} \cos (\omega . \frac{\phi}{\omega} - \phi)$$

i.e. $$\underline{\underline{i_d = \hat{I}}} \tag{5.7}$$

This peak of current is left to decay through D_7 and D_8.

The current, I_{L1}, flowing in phases A and B at the end of this first period may be found from equation (5.1).

$$\underline{\underline{I_{L1} = - \frac{V_d}{2R} + \left(\frac{V_d}{2R} + I_{LO}\right) e^{-\frac{RT_1}{L}}}} \tag{5.8}$$

From equations (5.7) and (5.8) the initial currents for the analysis of the next state of the circuit may be found.

The current i_s taken from the supply during the first period is given by

$$i_s = i_d - i_g$$

$$\text{i.e.} \quad i_s = \hat{I}\cos(\omega t - \phi) + \frac{V_d}{2R} - \left(\frac{V_d}{2R} + I_{LO}\right) e^{-\frac{Rt}{L}} \qquad (5.9)$$

5.3.4.2 Period 2 - period of decay of current in phase B.

It is assumed that the circuit switches directly from State 1 described in section 5.3.2 to State 4 described in section 5.3.2. The next state of the circuit to be analysed, therefore, is that in which CR_7 has turned off and CR_1 and CR_2 conduct, with D_3 carrying the decaying current in phase B. This period ends when the current in phase B and diode D_3 decays to zero, at which stage D_3 turns off and becomes reverse-biased. It is also assumed that throughout this period diodes D_7 and D_8 remain conducting.

Fig. 5.16 shows the paths which carry current during the period of decay of current in phase B. The current taken from the supply is i_s, currents i_p and i_n flow in the two halves of the d.c. choke, currents i_q and i_r in the diodes D_7 and D_8. Currents i_a, i_b, i_c in phases A, B, C flow through CR_1, D_3, CR_2. The resistance R_d of each half of the d.c. choke is also included.

Since it is assumed that D_7 and D_8 conduct while the current i_b decays to zero, the voltage drop across each half of the choke is limited to the forward voltage drops of D_7 and D_8. To obtain the

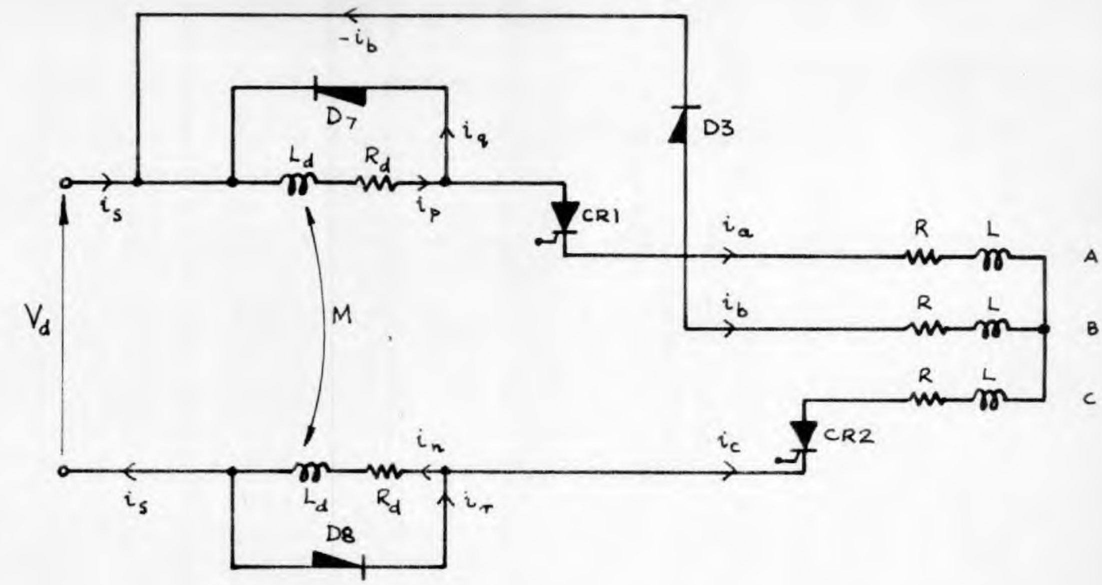


Fig. 5.16 : Conducting paths during decay of current in phase B.

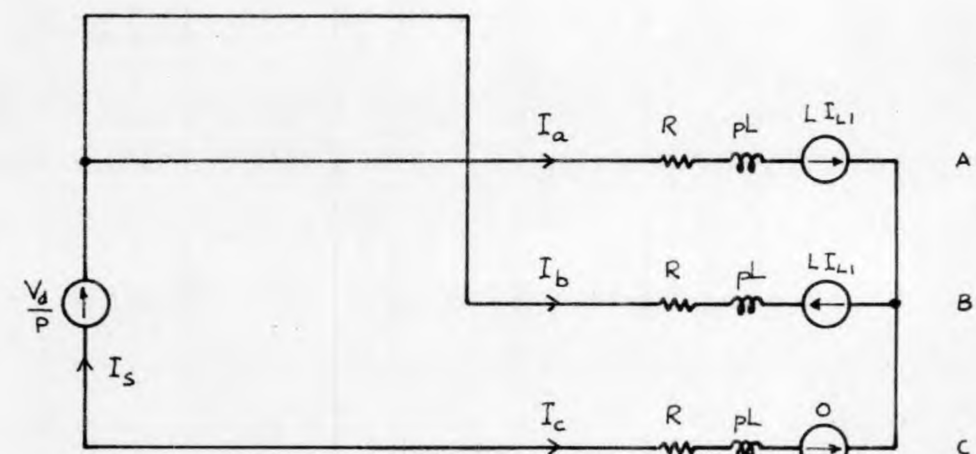


Fig. 5.17 : Operational circuit, valid during decay of current in phase B, for determining load currents.

variations of current in the load during this time the effect of the d.c. choke can be neglected. The variation of current in each half of the choke and in D_7 and D_8 can then also be found separately.

Fig. 5.17 shows the operational circuit used for obtaining the load currents. The initial value of i_a is I_{L1}, of i_b is $-I_{L1}$, and of i_c is zero and these initial values are allowed for in the operational circuit.

Applying Kirchhoff's First Law to the load star point

$$I_a + I_b + I_c = 0$$

$$\therefore \quad I_c = -(I_a + I_b) \tag{5.10}$$

Equations for I_a and I_b may be obtained as follows:-

$$\frac{V_d}{p} + L\,I_{L1} = I_a(pL + R) - I_c(pL + R)$$

$$\text{i.e.}\ \frac{V_d}{p} + L\,I_{L1} = 2I_a(pL + R) + I_b(pL + R) \tag{5.11}$$

$$2\,L\,I_{L1} = I_a(pL + R) - I_b(pL + R) \tag{5.12}$$

Eliminating I_b from equations (5.11) and (5.12),

$$\therefore\ I_a = \frac{pI_{L1} + \frac{V_d}{3L}}{p(p + \frac{R}{L})} \tag{5.13}$$

Inverting to obtain i_a in terms of time t, we obtain

$$i_a = \frac{V_d}{3R} + (I_{L1} - \frac{V_d}{3R})e^{-\frac{Rt}{L}} \tag{5.14}$$

Eliminating I_a from equations(5.11) and (5.12)

$$\therefore \quad I_b = \frac{\frac{V_d}{3L} - p\, I_{L1}}{p(p + \frac{R}{L})} \tag{5.15}$$

Inverting to obtain i_b in terms of time t, we obtain

$$i_b = \frac{V_d}{3R} - \left(\frac{V_d}{3R} + I_{L1}\right) e^{-\frac{Rt}{L}} \tag{5.16}$$

Then

$$I_c = -(I_a + I_b)$$

$$= \frac{\frac{2V_d}{3L}}{p(p + \frac{R}{L})} \tag{5.17}$$

and

$$i_c = -\frac{2V_d}{3R}(1 - e^{-\frac{Rt}{L}}) \tag{5.18}$$

It is seen that during the decay of the current in phase B, after the completion of the capacitor discharge, i_a changes from I_{L1} towards a steady state value $\frac{V_d}{3R}$, i_b from $-I_{L1}$ towards $\frac{V_d}{3R}$, and i_c from zero towards $-\frac{2V_d}{3R}$, all with time constant $\frac{L}{R}$.

This period ends when i_b reaches zero. The time, T_2 taken for this is obtained from equation (5.16).

$$\text{Thus } 0 = \frac{V_d}{3R} - \frac{V_d}{3R} + I_{L1}\; e^{-\frac{RT_2}{L}}$$

$$\text{i.e. } \underline{\underline{T_2 = \frac{L}{R}\log_e\left(1 + \frac{3RI_{L1}}{V_d}\right)}} \qquad (5.19)$$

T_2 is the duration of the second assumed state of the circuit, that with CR_1, CR_2, D_3, D_7 and D_8 conducting.

Fig. 5.18 shows the operational circuit for the two halves of the d.c. choke with D_7 and D_8 conducting. The resistance R_d of each half of the choke was included since the decay of choke current is slow during this period and V_f is the assumed constant forward voltage drop of D_7 and D_8. The possibility of difference between the initial values of current in each half of the choke is allowed for. If CR_1 and CR_2 had been fired immediately before D_7 and D_8 started to conduct, the initial currents would be as shown, I_{L1} being the initial value of I_a, The other currents entering the part of the circuit considered are also shown.

The following two equations may be obtained by considering the two closed loops separately :-

$$L_d(\hat{I} + \tfrac{1}{2} I_{L1}) + M(\hat{I} - \tfrac{1}{2} I_{L1}) - \frac{V_f}{p}$$

$$= I_p(pL_d + R_d) + I_n(pM) \qquad (5.20)$$

$$L_d(\hat{I} - \tfrac{1}{2} I_{L1}) + M(\hat{I} + \tfrac{1}{2} I_{L1}) - \frac{V_f}{p}$$

$$= I_p(pM) + I_n(pL_d + R_d) \qquad (5.21)$$

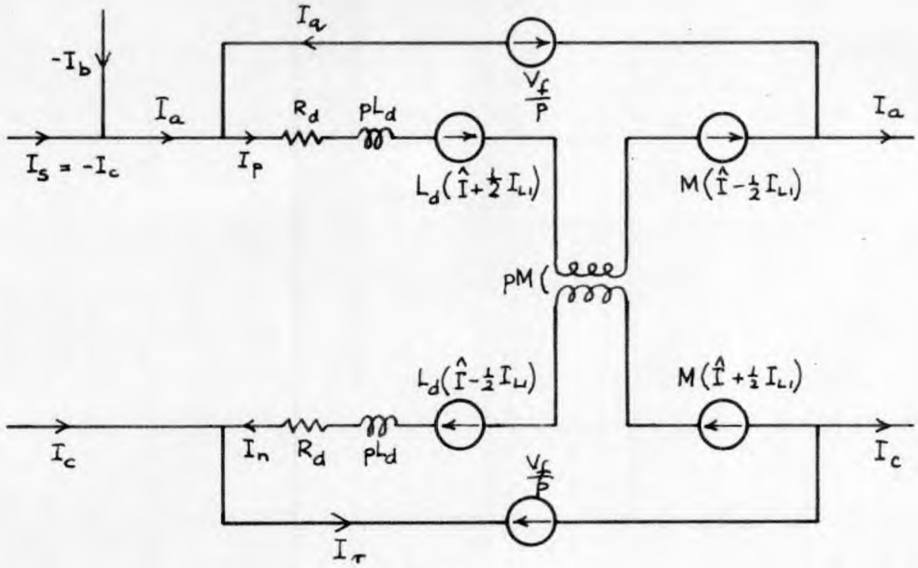


Fig. 5.18 : Operational circuit for obtaining choke currents during conduction of diodes D7 and D8.

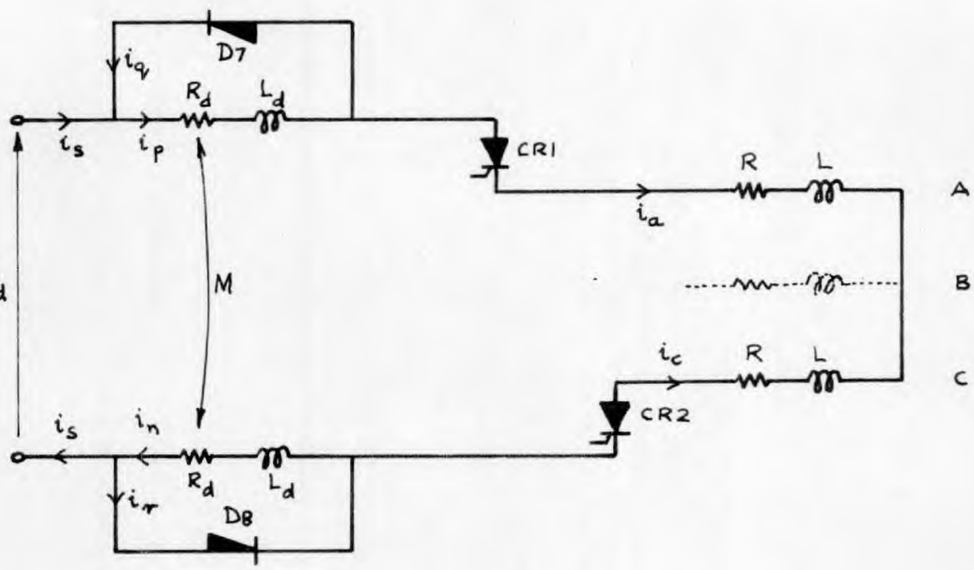


Fig. 5.19 : Conducting paths in circuit during period 3.

But $M = L_d$

$$\therefore \; 2 L_d \hat{I} - \frac{V_f}{p} = I_p (pL_d + R_d) + I_n(pL_d) \qquad (5.22)$$

$$\text{and} \;\; 2 L_d \hat{I} - \frac{V_f}{p} = I_p (pL_d) + I_n(pL_d + R) \qquad (5.23)$$

Subtracting equation (5.23) from equation (5.22)

$$0 = I_p (R_d) - I_n(R_d)$$

$$\text{i.e.} \;\; \underline{\underline{I_p = I_n}} \qquad (5.24)$$

Adding equations (5.22) and (5.23)

$$I_p = I_n = \frac{p\hat{I} - \frac{V_f}{2L_d}}{p(p + \frac{R_d}{2L_d})}$$

Inverting to obtain i_p and i_n in terms of time t, we obtain

$$\underline{\underline{i_p = i_n = -\frac{V_f}{R_d} + (\hat{I} + \frac{V_f}{R_d})\, e^{-\frac{R_d}{2L_d} \cdot t}}} \qquad (5.25)$$

It is seen, therefore, that when D_7 and D_8 conduct the currents in the two halves of the d.c. choke are equal even if their initial values are not equal. Each current falls from $\hat{I}$ towards a steady state value $\frac{V_f}{R_d}$ with time constant $\frac{R_d}{2L_d}$. This is true, of course only if the forward voltage drops of D_7 and D_8 are equal and if no resistance is connected in series with D_7 and D_8.

The currents flowing in the diodes are then given by

$$\underline{\underline{i_q = i_p - i_a}} \qquad (5.26)$$

and $$\underline{\underline{i_r = i_n + i_c}} \qquad (5.27)$$

During this period the supply current is given by

$$\underline{\underline{i_s = - i_c}} \qquad (5.28)$$

At the end of this period the current in phase B becomes zero. The currents flowing in phases A and C therefore become equal in magnitude and their values I_{a2}, I_{c2}, at the end of the period are obtained by putting $t = T_2$ in equations (5.14) and (5.18).

Then $$\underline{\underline{I_{a2} = \frac{2V_d}{3R}\left[\frac{1}{1+\dfrac{V_d}{3RI_{L1}}}\right]}} \qquad (5.29)$$

and $$\underline{\underline{I_{c2} = -\frac{2V_d}{3R}\left[\frac{1}{1+\dfrac{V_d}{3RI_{L1}}}\right]}} \qquad (5.30)$$

If I_{L1}, the value to which the currents in phases A and B fall during the period of discharge of the capacitor, is nearly equal to $\frac{V_d}{3R}$ it can be seen that I_{a2} and $- I_{c2}$ are even more nearly equal to $\frac{V_d}{3R}$. For, if $I_{L1} = \frac{V_d}{3R}(1 + x)$, where x is small compared with unity,

$$I_{a2} = -I_{c2} = \frac{2V_d}{3R}\left(\frac{1}{1 + \frac{1}{1+x}}\right)$$

$$\doteq \frac{2V_d}{3R}\left(\frac{1}{1 + 1 - x}\right) \text{ neglecting } x^2,\ x^3, \text{ etc.}$$

i.e. $I_{a2} = -I_{c2} \doteq \frac{V_d}{3R}\left(1 + \frac{x}{2}\right)$ (5.31)

i.e. The difference between I_{a2} or $-I_{c2}$ and $\frac{V_d}{3R}$ is approximately half the difference between I_{L1} and $\frac{V_d}{3R}$.

For convenience, let $I_{a2} = -I_{c2} = I_{L2}$.

5.3.4.3 Period 3 - remainder of period of decay of currents in D_7 and D_8.

During this period current continues to flow in diodes D_7 and D_8 and hence the d.c. choke has no effect upon the rise of current in the load. Load current flows only in phases A and C and the current carrying paths are therefore as shown in Fig. 5.19. The same current flows through phases A and C and from the supply. Hence $i_s = i_a = -i_c$.

Fig. 5.20 shows the operational circuit used for obtaining the load current variations during this period. The choke is disregarded in this circuit, its effect being limited by the conduction of diodes D_7 and D_8. The initial values of the currents in phases A and C are allowed for in the circuit. The load and supply currents are therefore given by

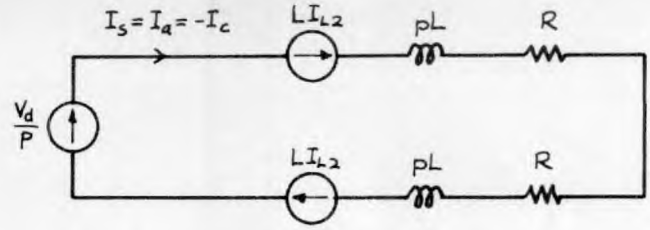


Fig. 5. 20 : Operational circuit for obtaining load currents during period 3.

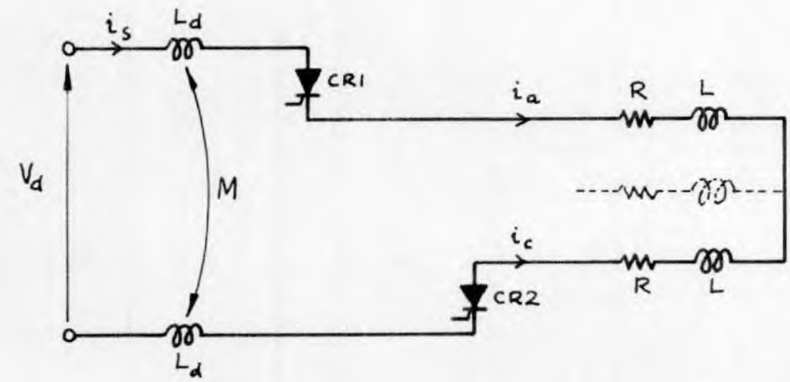


Fig. 5. 21 : Conducting paths during period 4.

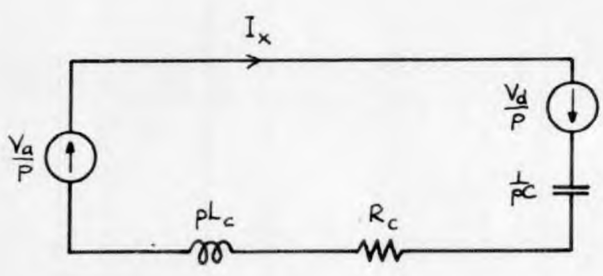


Fig. 5. 22 : Operational circuit for obtaining voltage and current equations for the re-charging of capacitor C from the auxiliary supply.

$$I_s = I_a = - I_c = \frac{\frac{V_d}{2L} + p\, I_{L2}}{p(p + \frac{R}{L})}$$

Inverting to obtain the equations in terms of time, t,

$$\underline{\underline{i_s = i_a = - i_c = \frac{V_d}{2R} + (I_{L2} - \frac{V_d}{2R})e^{\frac{-Rt}{L}}}} \qquad (5.32)$$

i.e. the load and supply current rises from its initial value I_{L2} towards a steady state value $\frac{V_d}{2R}$ with time constant $\frac{L}{R}$.

During this time the equations for the choke currents are as for period 2 but modified to take account of the new time origin.

$$\text{Hence} \quad \underline{\underline{i_p = i_n = - \frac{V_f}{R_d} + (\hat{I} + \frac{V_f}{R_d})e^{-\frac{R_d}{2L_d}(t + T_2)}}} \qquad (5.33)$$

The currents flowing in diodes D_7 and D_8 are the differences between the choke currents and the supply current. Hence

$$i_q = i_r = i_p - i_s = i_n - i_s$$

Period 3 ends either when the sixth of a cycle is complete or when the currents in D_7 and D_8 become zero. In the latter case this happens when the choke current falls to the value to which the supply current has risen. That is when

$$i_p = i_n = i_s$$

$$\text{i.e. when } -\frac{V_f}{R_d} + (\hat{I} + \frac{V_f}{R_d})e^{-\frac{R_d}{2L_d}(t + T_2)} = \frac{V_d}{2R} + (I_{L2} - \frac{V_d}{2R})e^{-\frac{Rt}{L}} \qquad (5.34)$$

At this instant let the values of i_s, i_p, i_n, i_a and $-i_c$ be I_{L3}.

5.3.4.4. Period 4 - remainder of the sixth of a cycle.

In period 4, when it occurs, the diodes D_7 and D_8 do not conduct and the d.c. choke is once more able to impede the rise of load current. The effect is a change in the time constant of rise of load current. Fig. 5.21 shows the conducting paths during period 4. Current flows between the supply and the phases A and C through CR_1 and CR_2 and the two halves of the d.c. choke.

It has been shown that the d.c. choke may be regarded as two separate chokes, of inductance $2L_d$ each, when the same current flows through both halves. The current in the load phases and in the chopke at the start of period 4 is I_{L3} and the steady state value to which the current must rise is $\frac{V_d}{2R}$, neglecting the choke resistance R_d. The total inductance in the conducting path is $2(L + 2L_d)$, the total resistance is 2R. Hence the current in the circuit must now be given by

$$i_s = i_a - i_c = \frac{V_d}{2R} + (I_{L3} - \frac{V_d}{2R})e^{-\frac{Rt}{L+2L_d}} \qquad (5.35)$$

i.e. the load current continues to rise towards the same steady state value but with time constant $\frac{L + 2L_d}{R}$ instead of $\frac{L}{R}$. During this period the diodes D_7 and D_8 become feverse-biased by the voltage induced in the two halves of the choke.

At the end of period 4 let the magnitude of i_s, i_a, $-i_c$ be I_{L4}.

5.3.4.5 Re-charging of capacitor C from auxiliary supply.

After CR_7 has turned off CR_8 must be fired to re-charge the capacitor from the auxiliary supply. The instant at which this is done is not critical but must be arranged so that CR_8 turns off before CR_7 is fired again. During the re-charging period the capacitor is isolated from the main circuit and the process may be considered separately. Fig. 5.22 shows the operational circuit used to obtain the re-charging voltage and current equations. Capacitor C initially is charged to a voltage $+ V_d$ and the auxiliary supply current is initially zero. The auxiliary supply current after CR_8 is fired is therefore given by

$$I_x = \frac{\frac{V_a}{p} + \frac{V_d}{p}}{pL_c + R_c + \frac{1}{pC}}$$

If R_c can be neglected

$$I_x = \frac{V_a + V_d}{L_c(p^2 + \frac{1}{CL_c})}$$

Inverting to obtain i_x in terms of time t, we obtain

$$\underline{\underline{i_x = \frac{V_a + V_d}{zL_c} \sin z\, t}} \qquad (5.36)$$

where $$z = \frac{1}{CL_c}$$

CR_8 continues to conduct and capacitor C to charge until i_x becomes zero. This occurs when sin z t becomes zero, i.e. when $t = \frac{\pi}{z}$. Then the voltage, $-V_{CR}$, to which capacitor C has charged is given by

$$- V_{CR} = V_d - \frac{1}{C}\int_0^{\frac{\pi}{z}} \frac{V_a + V_d}{z\, L_c} \sin z\, t.dt$$

$$= V_d + \frac{V_a + V_d}{z^2 L_c C} \Big[\cos z\, t\Big]_0^{\frac{\pi}{z}}$$

i.e. $$+ V_{CR} = +(V_d + 2V_a) \; \ldots \text{ since } z^2 = \frac{1}{CL_c} \qquad (5.37)$$

In practice, because of the effect of the small supply resistance V_{CR} would be less than the value given by equation (5.37).

5.3.4.6. Note on current and voltage equations.

It should be noted that in the voltage and current equations derived above t = 0 at the start of each period for which the equations are given, i.e. in 5.3.4.1 t = 0 when CR_7 is fired, in 5.3.4.2 t = 0 when CR_7 turns off and CR_1 and CR_2 are fired, etc.

5.3.5 Typical Output Waveforms for Series R-L Load.

Fig. 5.23 shows typical load current waveforms for a series R-L star-connected load. It is assumed that diodes D_7 and D_8 remain conducting until the end of each sixth of a cycle and that therefore period 4, discussed in section 5.3.4.4., does not occur. Period 4 as shown is of exaggerated duration so that the current change in this period can be seen clearly.

The first sixth of a cycle shown, that between t_2 and t_3, is the one considered in the preceding theory and is further sub-divided into the periods 1, 2 and 3 discussed previously. All current changes are exponential and have a common time constant. The initial rates of change and the steady state values towards which the currents change are indicated by means of dotted lines.

In period 1 i_c is assumed to be zero while i_a falls from its initial value I_{L0} towards $-\frac{V_d}{2R}$ with time constant $\frac{L}{R}$. i_b rises from $-I_{L0}$ towards $+\frac{V_d}{2R}$ with time constant $\frac{L}{R}$. Period 1 ends when CR_7 turns off, diodes D_7 and D_8 and CR_1 and CR_2 conduct, and i_a and $-i_b$ are then equal to I_{L1}.

In period 2 i_a rises from I_{L1} towards $\frac{V_d}{3R}$, i_b rises from $-I_{L1}$ towards $\frac{V_d}{3R}$, and i_c falls from zero towards $-\frac{2V_d}{3R}$, all with time constant $\frac{L}{R}$. Period 2 ends when i_b becomes zero and i_a and $-i_c$ are equal to I_{L2}.

In period 3 i_b is zero. i_a rises from I_{L2} towards $\frac{V_d}{2R}$ and i_c falls from $-I_{L2}$ towards $-\frac{V_d}{2R}$, both with time constant $\frac{L}{R}$. It is assumed that period 3 continues until the end of the sixth of a cycle

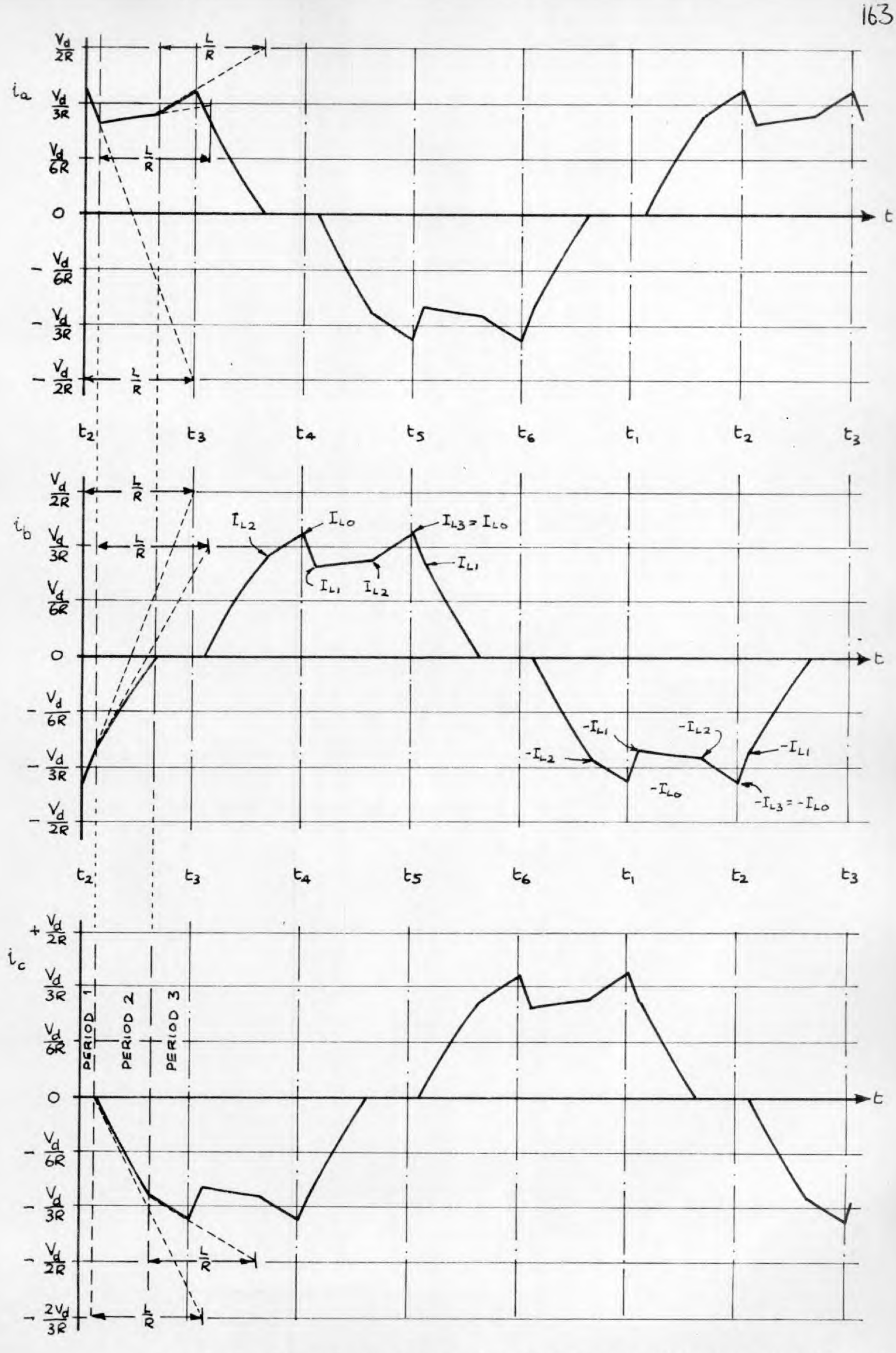


Fig. 5.23: Typical waveforms of output line current for series R-L load.

when i_a and $-i_c$ are equal to I_{L3}. These values of i_a and i_c at the end of period 3 are clearly the starting values for the next sixth of a cycle and hence $I_{L3} = I_{L6}$.

From the sixth of a cycle considered in the theory the complete currentwaveforms can be built up. The pattern of current changes in each phase is repeated one third of a cycle later in one of the other phases and two thirds of a cycle later in the third phase. Moreover each negative half cycle is a mirror image of the positive half cycle, displaced by half a cycle.

In Fig. 5.24 the corresponding line-to-line output voltage waveforms are shown. Again the first sixth of a cycle shown is subdivided into periods 1, 2 and 3.

In priod 1 diodes D_3 and D_4 conduct and no current flows in phase C. Hence $v_{ab} = V_d$, $v_{bc} = \frac{1}{2} V_d$ and $v_{ca} = \frac{1}{2} V_d$.

In period 2 CR_1, CR_2 and diode D_3 conduct and hence $v_{ab} = 0$, $v_{bc} = V_d$ and $v_{ca} = - V_d$.

In period 3 CR_1 and CR_2 conduct and no current flows in phase B. Hence $v_{ab} = \frac{1}{2} V_d$, $v_{bc} = \frac{1}{2} V_d$ and $v_{ca} = - V_d$.

From the patterns of voltage changes for the first sixth of a cycle the complete voltage waveforms may be built up in the same way as the current waveforms.

It is seen that the current waveforms possess a high fundamental sinusoidal component but that the corresponding voltage waveforms have a very much larger harmonic content. This is to be expected since the harmonic reactance of the load is proportional to the order of the harmonic.

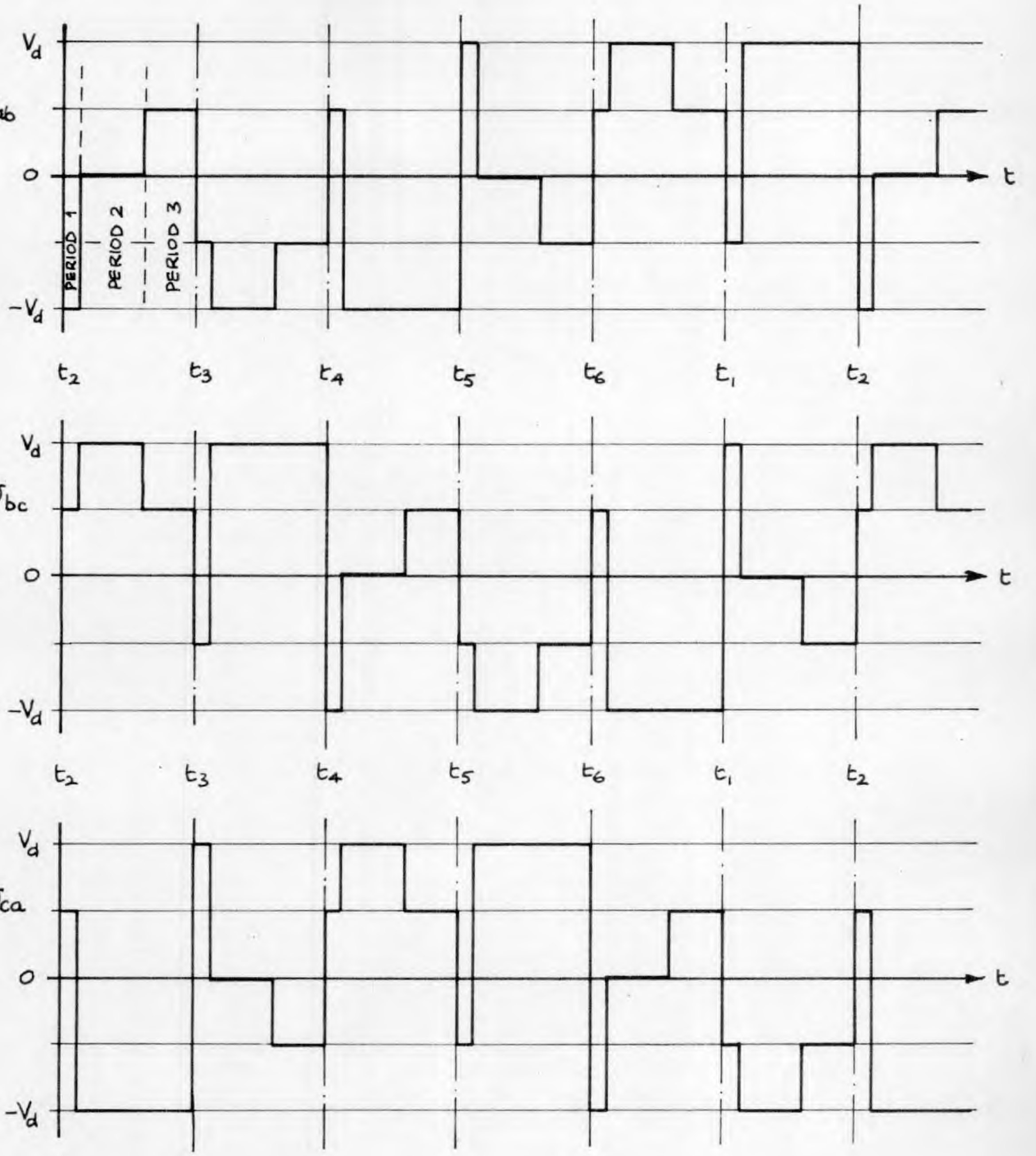


Fig. 5.24 : Typical output line-to-line voltage waveforms for series R-L load.

The method used for constructing the current waveforms shown in Fig. 5.23 can be used to obtain the current waveforms graphically. This will be discussed further in the next section.

5.3.6 Calculation of Output Waveforms for Series R-L Load.

In section 5.3.2 it was shown that in each sixth of a cycle there are six states which the circuit can assume, one by one. To calculate accurately the output waveforms, or indeed any waveform, it would be necessary to take into account all six of these states. Each state, however, has its own voltage and current equations and the initial current and voltage values for each state have to be found. The labour involved in calculating the waveform for a single combination of supply voltages, output frequency, and load and circuit parameters would be enormous and would produce little information on the general behaviour of the system.

In obtaining the voltage and current equations in section 5.3.4 the number of circuit states was reduced to four by combining the first three of the possible six states into one. In the following discussion on methods of calculating the output waveforms it will be further assumed that the last state does not occur, i.e. that diodes D_7 and D_8 conduct up to the end of each sixth of a cycle. In many cases this assumption is perfectly valid. In other cases D_7 and D_8 cease to conduct towards the end of the sixth of a cycle when the load current has nearly reached its steady state value and the error introduced by the assumption is therefore quite small. The number of states occurring in each sixth of a cycle is therefore assumed to be three, which simplifies the calculation considerably.

There still remains the problem of finding the values of the currents in the load phases at the start of each period. The problem is not very severe at low output frequencies, when the load time constant is considerably less than one sixth of a cycle, since the load currents reach steady state values by the end of each sixth of a cycle. At higher frequencies these starting current values must be determined. Suitable methods are discussed below.

5.3.6.1 Low output frequency, i.e. $\frac{1}{6f} \gg \frac{L}{R}$.

At low frequencies where the load time constant is much shorter than one sixth of a cycle the value of I_{LO} may be taken to be $\frac{V_d}{2R}$. The period T_1 of the discharge of capacitor C may also be found quite easily from equation 5.6. The value of I_{do} required in finding T_1 may be taken to be $\frac{V_d}{2R}$ or found from equation 5.97 when the frequency is such that this latter course is necessary.

T_1 would normally be much smaller than the load time constant and hence the change of current during this period can be assumed linear. This is shown in Fig. 5.25. i_a and $- i_c$ therefore change linearly from $\frac{V_d}{2R}$ so as to reach $- \frac{V_d}{2R}$ in time $\frac{L}{R}$ and after a time T_1 reach the value I_{L1}. Hence I_{L1} is approximately given by

$$I_{L1} \triangleq \frac{V_d}{2R} - \frac{V_d}{L} \cdot T_1 \qquad (5.38)$$

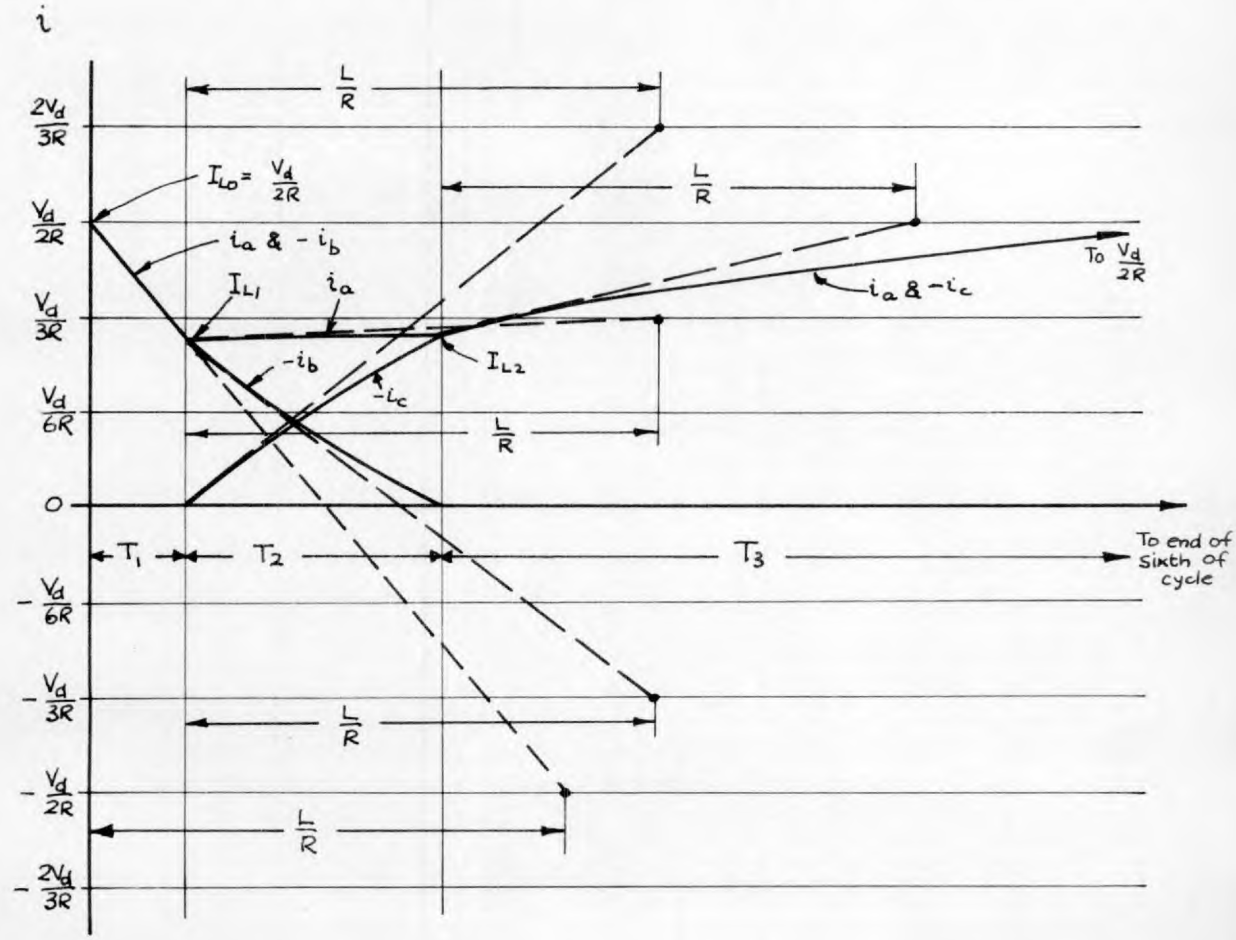


Fig. 5.25: Current changes in the sixth of a cycle between t_2 and t_3 at low inverter output frequency.

In the next period, which is of duration T_2, i_a changes from I_{L1} towards $\frac{V_d}{3R}$, $- i_b$ from I_{L1} towards $- \frac{V_d}{3R}$, and $- i_c$ from zero towards $\frac{2V_d}{3R}$, all with time constant $\frac{L}{R}$. T_2 is then the time taken for $- i_b$ to reach zero and is given by equation (5.19). The value I_{L2} of i_a and $- i_c$ at the end of the second period is given by equation (5.29).

In the third period, which is assumed to continue until the end of the sixth of a cycle, i_a and $- i_c$ rise from I_{L2} to $\frac{V_d}{2R}$ with time constnat $\frac{L}{R}$ while i_b remains at zero.

It is seen that the derivation of the value I_{L1} and I_{L2} is simple in this case of low inverter output frequency because I_{L0} can be assumed to be $\frac{V_d}{2R}$. The calculations resolve into simple substitutions in formulae which have already been derived in the preceding theory.

The waveforms of output current and voltage may now be drawn and would be similar to those shown as typical waveforms in Figs. 5.23 and 5.24.

5.3.6.2. Higher output frequencies.

At higher inverter output frequencies, where $\frac{L}{R}$ is comparable with or greater than one sixth of a cycle, I_{L0} can no longer be assumed equal to $\frac{V_d}{2R}$ and must be calculated in some way. The following is an iterative method of finding I_{L0}. I_{do} can be taken as equal to I_{L0} or found from equation (5.97).

The steps in the iterative method are as follows :-

1) Choose arbitrarily a value for I_{L0} (must be less than $\frac{V_d}{2R}$).

2) Find T_1 from equation 5.6 using $I_{do} = I_{L0}$ or the value of I_{do} found from equation 5.97, whichever value is greater.

3) Assume linear current changes in period 1 and hence find I_{L1} from

$$I_{L1} = I_{L0} - (I_{L0} + \frac{V_d}{2R}) . \frac{R\,T_1}{L} \tag{5.39}$$

4) Find I_{L2} from equation 5.29, i.e.

$$I_{L2} = \frac{2V_d}{3R} \left(\frac{1}{1 + \frac{V_d}{3RI_{L1}}} \right)$$

5) Find T_2 from equation 5.19, i.e.

$$T_2 = \frac{L}{R} \log_e \left(1 + \frac{3R\,I_{L1}}{V_d}\right)$$

6) Find T_3 from $T_3 = \frac{1}{6f} - (T_1 + T_2)$

7) Find I_{L3} from equation 5.32, i.e.

$$I_{L3} = \frac{V_d}{2R} + (I_{L2} - \frac{V_d}{2R}) e^{-\frac{RT_3}{L}}$$

If the chosen value of I_{L0} is correct, the value of I_{L3} thus obtained would be equal to I_{L0}. If I_{L0} and I_{L3} differ, a new value for I_{L0} should be chosen and the procedure repeated. The new value of I_{L0} chosen should be between the old value and the value obtained for I_{L3}.

The procedure may be carried out graphically. Fig. 5.26 shows the procedure when the correct value of I_{L0} has been chosen. i_a changes from L_{L0} towards $-\frac{V_d}{2R}$ with time constant $\frac{L}{R}$, the change during T_1 being almost linear. In T_2, $-i_b$ falls from I_{L1} towards $\frac{V_d}{3R}$ with time constant $\frac{L}{R}$, T_2 being the time taken by $(-i_b)$ to reach zero. During period 2, i_a changes from I_{L1} towards $\frac{V_d}{3R}$ and, after time T_2, reaches the value I_{L2}. In period 3, i_a and $(-i_c)$ rise together from I_{L2} towards $\frac{V_d}{2R}$ with time constant $\frac{L}{R}$ and reach the value I_{L3} after time T_3. I_{L3} is then equal to I_{L0}. If the change in $(-i_c)$ from zero to I_{L2} in period 2 is also inserted, all the current variations needed to draw the complete current waveforms will be found in the diagram.

Fig. 5.27 shows how the iterative process may be carried out. A value of I_{L0} is assumed and all the above steps in the above process carried through to obtain graphically a value of I_{L3} which is not equal to I_{L0}. A new value of I_{L0}, half way between the original value of I_{L0} and the resulting value of I_{L3}, is taken and the procedure repeated. The value of I_{L3} obtained from the second construction is compared with I_{L0} and a new value of I_{L0} chosen, and so on. The iteration can be stopped when I_{L3} becomes equal to the preceding value of I_{L0} used. The values of I_{L1} and I_{L2} thus obtained are also correct.

It is seen from Fig. 5.27, and will also be seen from sample calculations given later, that the most rapid method of progressing in this iterative process is to use for the new value of I_{L0} the value of I_{L3} obtained from the preceding stage in the calculation.

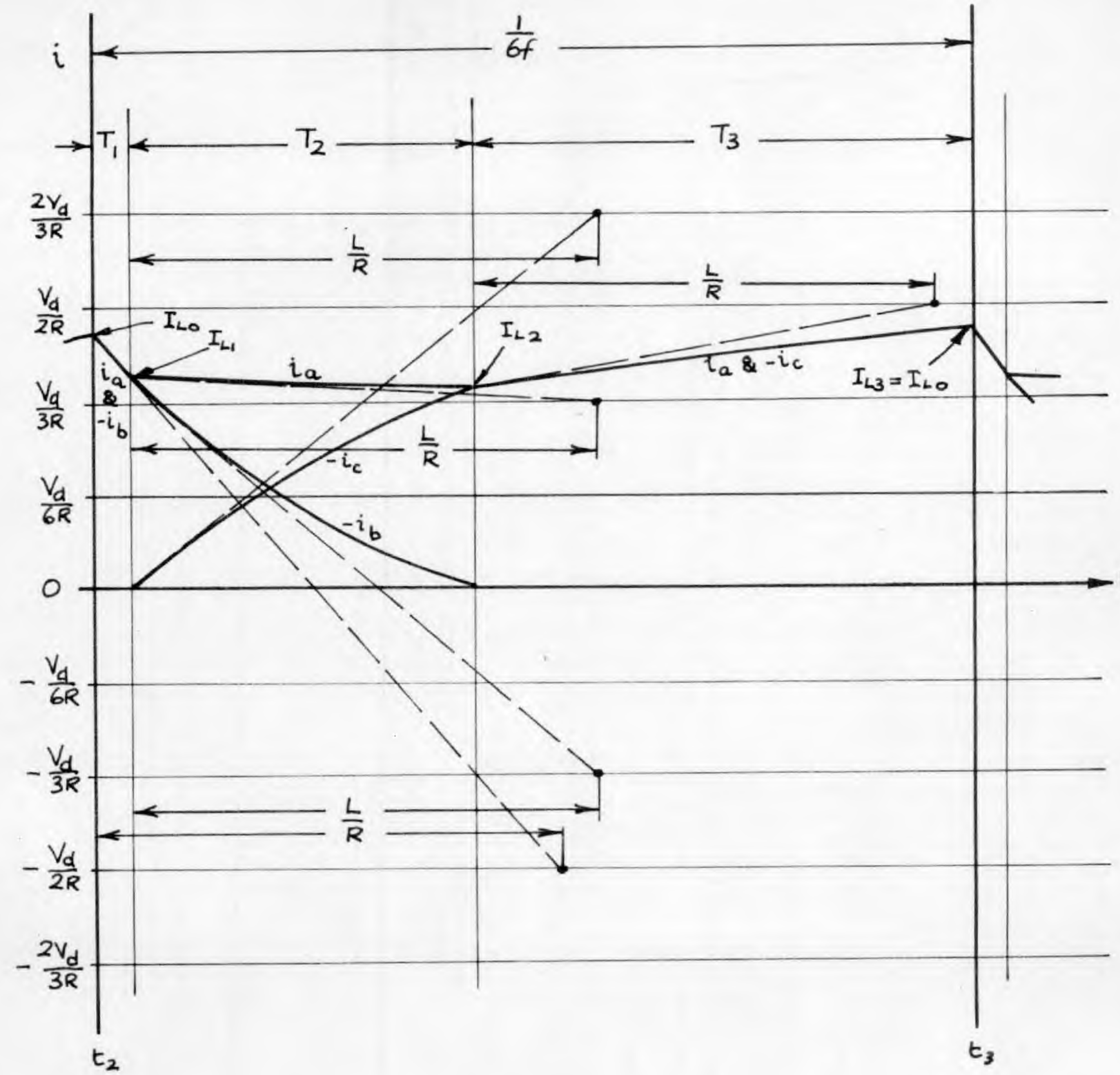


Fig. 5.26 : Current changes in the sixth of a cycle between t_2 and t_3 at the higher inverter output frequencies.

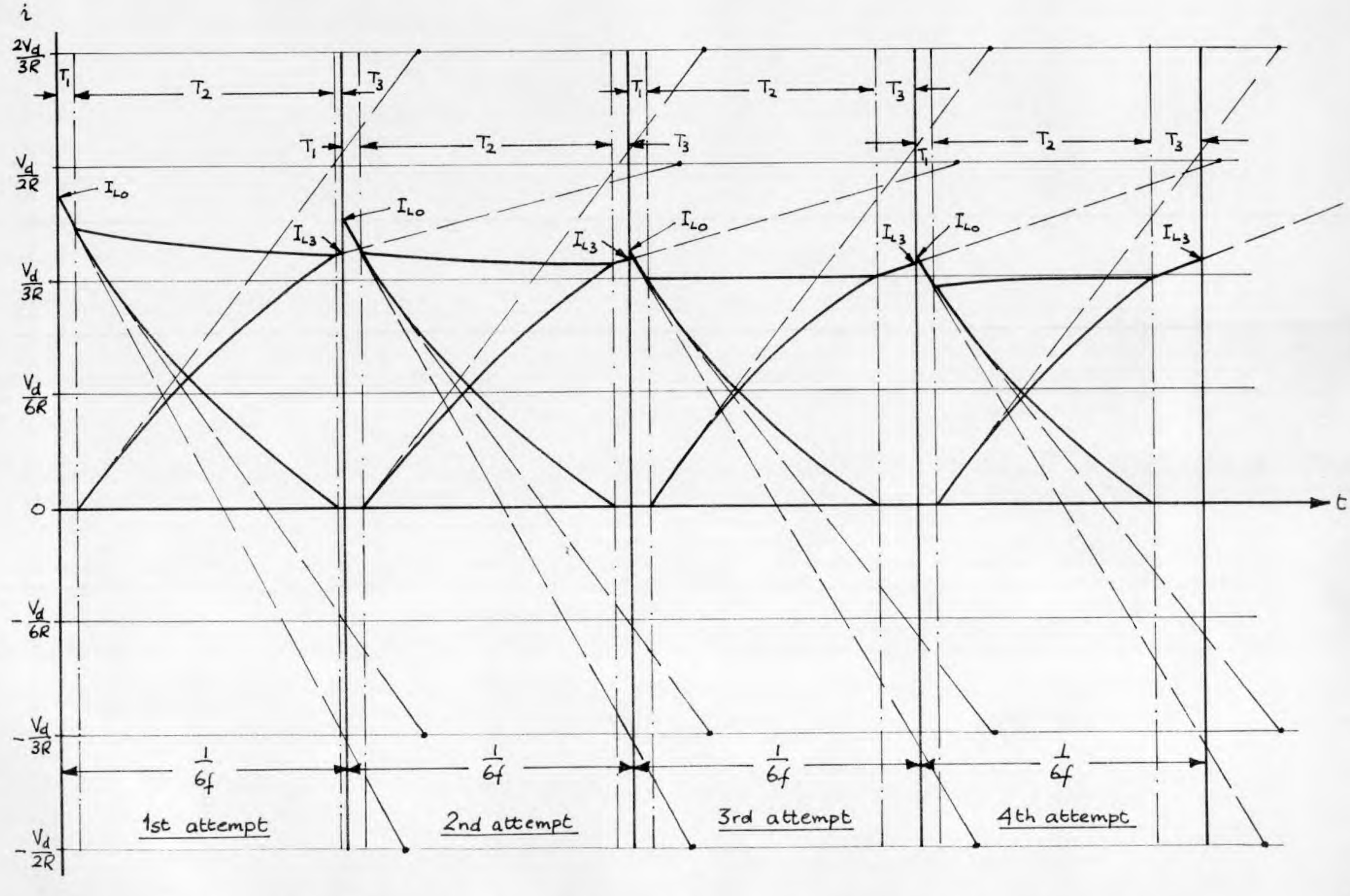


Fig. 5.27: Graphical determination of current waveforms by iterative method.

5.4 Theory of Operation on Star-Connected R-L Load with "Power Factor" < 0.5 (approx.).

In section 5.3 it was assumed that the current in phase C would be zero at the beginning of the sixth of a cycle considered under most conditions. This would be true under most operating conditions if the power factor of the load ~~were~~ was not very low.

The calculation for a highly inductive load is a little simpler than for the higher power factor load because only two periods in each sixth of a cycle are involved (provided that it can be assumed that D_7 and D_8 remain conducting throughout the sixth of a cycle after commutation). Period 2 considered in 5.3.4.2 ended when the current in phase B decayed to zero. In this case we consider the position when the current in phase B still flows at the end of the sixth of a cycle and consequently period 2 extends from the end of the commutation period to the end of the sixth of a cycle.

5.4.1 States of Conduction of Circuit.

As before, the sixth of a cycle considered is that between t_2 and t_3. CR_1 conducts for the second half of its third of a cycle, CR_2 is fired for the beginning of its third of a cycle of conduction, and CR_6 has turned off at instant t_2.

State 1 :- Commutation period.

During the commutation period CR_7 conducts and all other S C Rs are off. The load currents therefore flow as shown in Fig. 5.28 by

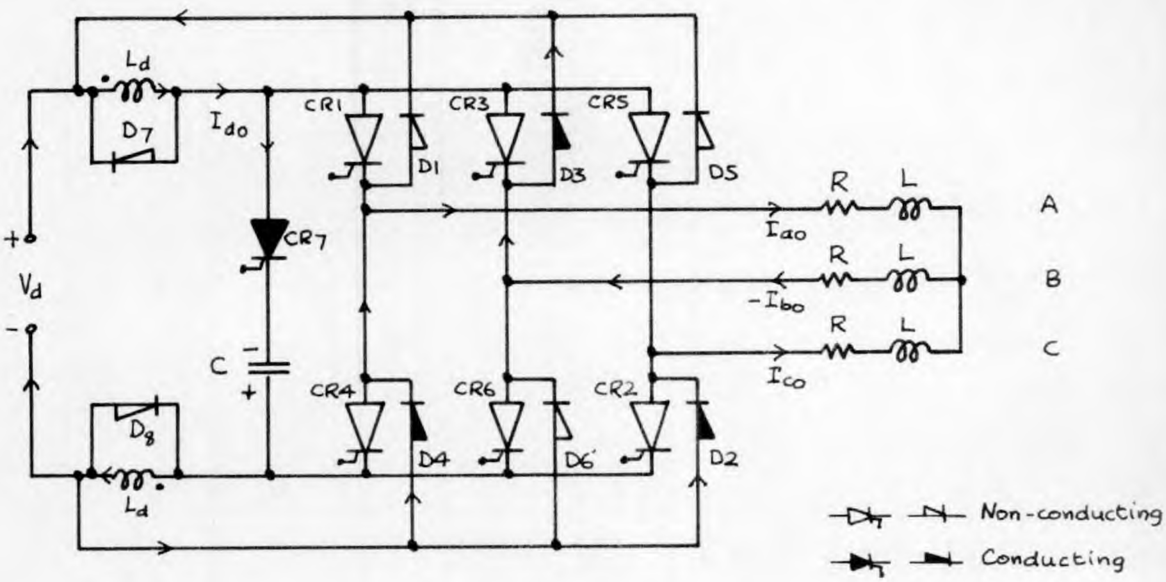


Fig. 5.28: State of conduction of circuit at instant, t_2, of firing CR_7 for highly inductive load.

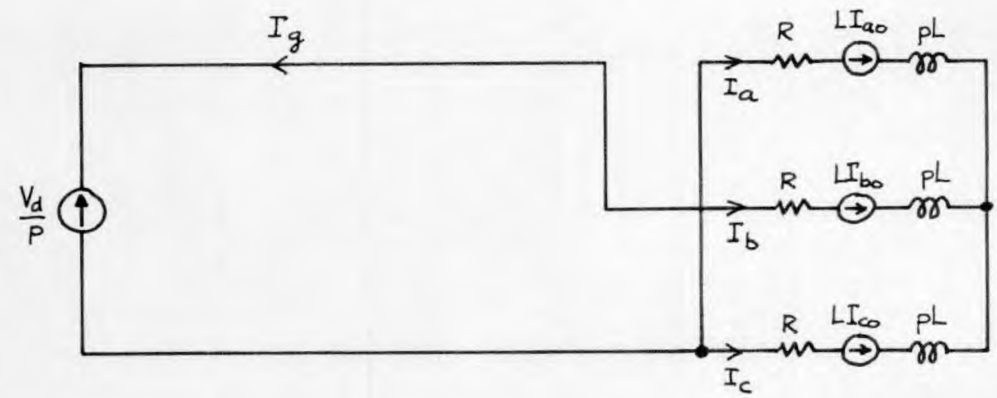


Fig. 5.29: Operational circuit for obtaining load currents during commutation period.

the long arrows. i_a starts at its initial value I_{ao} and flows through diode D_4 from the supply negative terminal. Since CR_6 has just turned off i_b flows in the direction shown, via diode D_3, starting at its initial value I_{bo}. At instant t_2 i_c was still decaying from the value it had when CR_5 turned off and therefore flows in the direction shown via D_2 from its initial value I_{co} at t_2.

At the end of the commutation period i_a, i_b and i_c change to the values I_{a1}, I_{b1} and I_{c1} respectively.

The current flowing through CR_7 into C during the commutation period is fully dealt with in section 5.3.4.1.

State 2 :- Remainder of sixth of a cycle.

After the commutation period CR_1 and CR_2 are free to conduct. Current flows in phase A through CR_1 as shown in Fig. 5.30 by the long arrow starting at the new initial value I_{a1}. Current in phase B continues to decay through diode D_3 in the direction indicated by the long arrow. Unless the current in phase C had fallen to zero during the commutation period it would still flow in the direction shown through diode D_2 and CR_2 would not, therefore, conduct.

The value of i_c would eventually fall to zero and the voltage appearing across phase C would tend to drive i_c in the opposite direction. Since CR_2 is fired i_c would immediately flow through it and in this way change direction during the course of the sixth of a cycle. Apart from the difference in the direction of the forward voltage drop of D_2 and CR_2 the circuits for both directions of flow of i_c during this

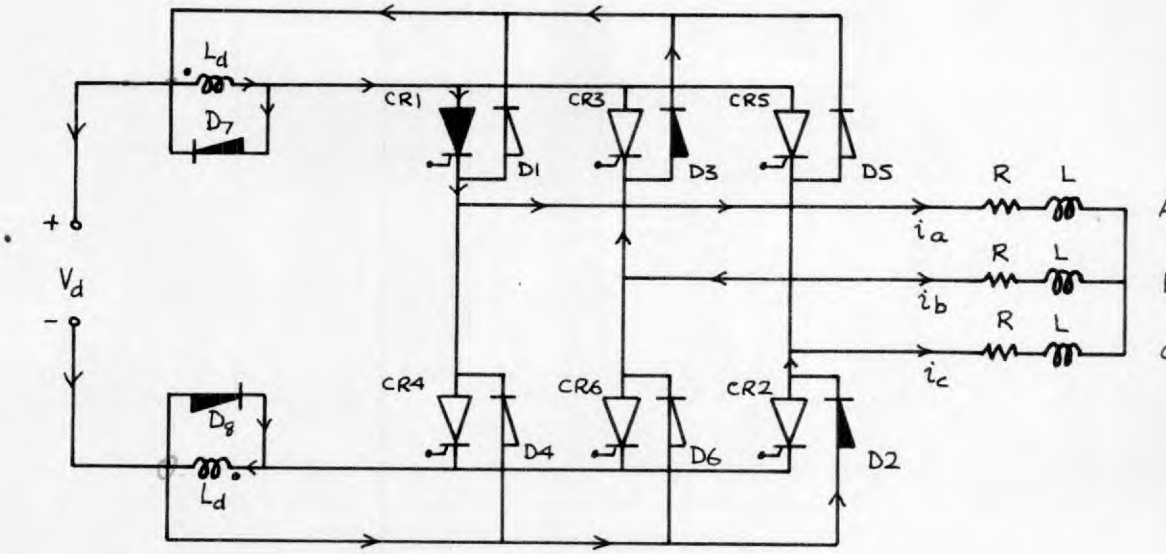


Fig. 5.30: Current paths after commutation. I_c is still positive and CR_2, though triggered, cannot conduct yet.

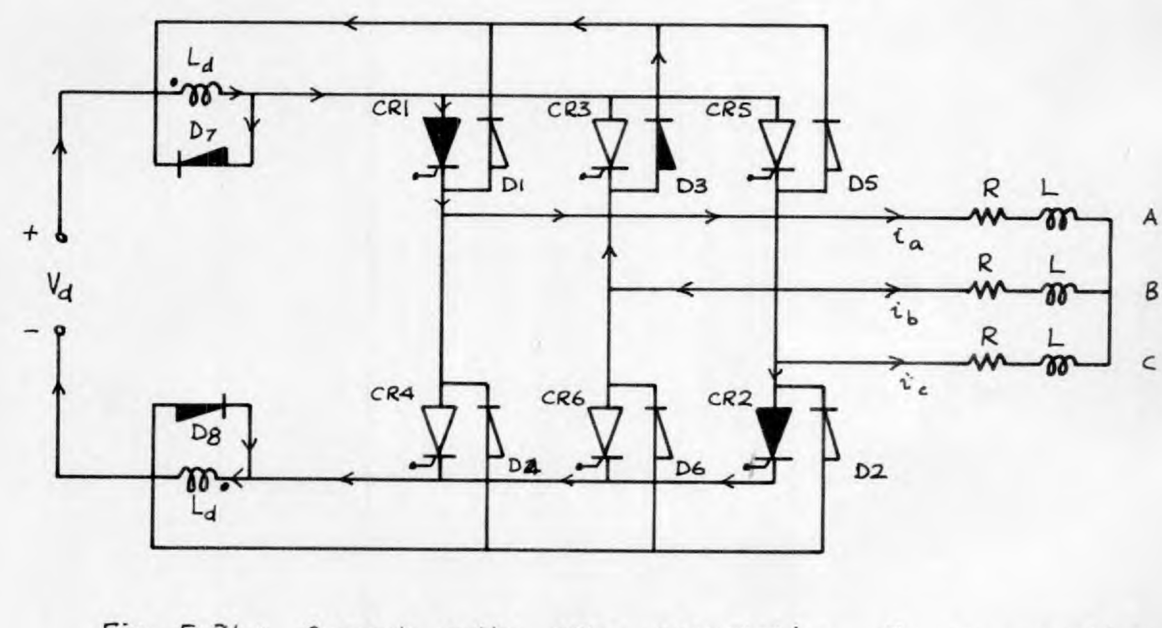


Fig. 5.31: Current paths after commutation. I_c now negative and flows in CR_2 instead of D2.

(& : Non-conducting ; & : conducting.)

period are identical. (Compare Figs. 5.30 and 5.31.)

At the end of the sixth of a cycle i_a, i_b, i_c reach the values I_{a2}, I_{b2}, I_{c2}.

5.4.2 Current and Voltage Equations.

5.4.2.1 Commutation period.

Fig. 5.29 shows the operational circuit which is valid during the commutation period. The commutation circuit is omitted because it has been dealt with in section 5.3.4.1.

Since I_{ao}, I_{bo}, I_{co} are instantaneous values of i_a, i_b, i_c

$$I_{ao} + I_{bo} + I_{co} = 0 \qquad (5.40)$$

also

$$I_a + I_b + I_c = 0 \qquad (5.41)$$

Taking the closed loop formed by phases A and C,

$$I_a(pL + R) - I_c(pL + R) = L\,I_{ao} - L\,I_{co} \qquad (5.42)$$

Taking the loop formed by the supply and phases B and C and substituting for I_b from equation (5.40) and for I_{bo} from equation (5.41)

$$I_a(pL + R) + 2I_c(pL + R) = L\,I_{ao} + 2L\,I_{co} - \frac{V_d}{p} \qquad (5.43)$$

Eliminating I_a from equations (5.42) and (5.43) we obtain

$$I_c = \frac{I_{co}}{p + \frac{R}{L}} - \frac{V_d}{3Lp(p + \frac{R}{L})}$$

Inverting this gives

$$i_c = -\frac{V_d}{3R} + (I_{co} + \frac{V_d}{3R})e^{-\frac{Rt}{L}} \qquad (5.44)$$

Eliminating I_c from equations (5.42) and (5.43)

$$I_a = \frac{I_{ao}}{p + \frac{R}{L}} - \frac{V_d}{3L_p(p + \frac{R}{L})}$$

Inverting, this gives

$$i_a = -\frac{V_d}{3R} + (I_{ao} + \frac{V_d}{3R})e^{-\frac{Rt}{L}} \qquad (5.45)$$

Then, putting $i_b = -(i_a + i_c)$

$$i_b = \frac{2V_d}{3R} + (I_{bo} - \frac{2V_d}{3R})e^{-\frac{Rt}{L}} \qquad (5.46)$$

At the end of the commutation period $t = T_1$ and i_a, i_b, i_c become equal to I_{a1}, I_{b1}, I_{c1}. If T_1 is small compared with $\frac{L}{R}$, which is a reasonable assumption for a highly inductive load,

$$e^{-\frac{RT_1}{L}} \simeq 1 - \frac{RT_1}{L}$$

and then

$$I_{a1} = I_{ao} - (I_{ao} + \frac{V_d}{3R})\frac{RT_1}{L} \qquad (5.47)$$

$$I_{b1} = I_{bo} - (I_{bo} - \frac{2V_d}{3R}) \frac{RT_1}{L} \qquad (5.48)$$

$$I_{c1} = I_{co} - (I_{co} + \frac{V_d}{3R}) \frac{RT_1}{L} \qquad (5.49)$$

During the commutation period diodes D_2, D_3, D_4 conduct and hence

$$v_{ab} = - V_d \qquad (5.50)$$

$$v_{bc} = V_d \qquad (5.51)$$

$$v_{ca} = 0 \qquad (5.52)$$

i_g, the current returned to the supply from the load during the commutation period is given by

$$i_g = - i_b \qquad (5.53)$$

5.4.2.2 Remainder of sixth of a cycle.

During the remainder of the sixth of a cycle between t_2 and t_3 CR_1, diode D_3 and either diode D_2 or CR_2 conduct. The operational circuit shown in Fig. 5.32 is therefore valid during this period.

Since I_{a1}, I_{b1}, I_{c1} are the values of i_a, i_b, i_c at the same instant

$$I_{a1} + I_{b1} + I_{c1} = 0 \qquad (5.54)$$

Taking the closed loop formed by phases A and B,

$$I_a(pL + R) - I_b(pL + R) = L\,I_{a1} - L\,I_{b1} \qquad (5.55)$$

Taking the loop formed by the supply and phases A and C and substituting for I_c and I_{c1} from equations (5.41) and (5.54),

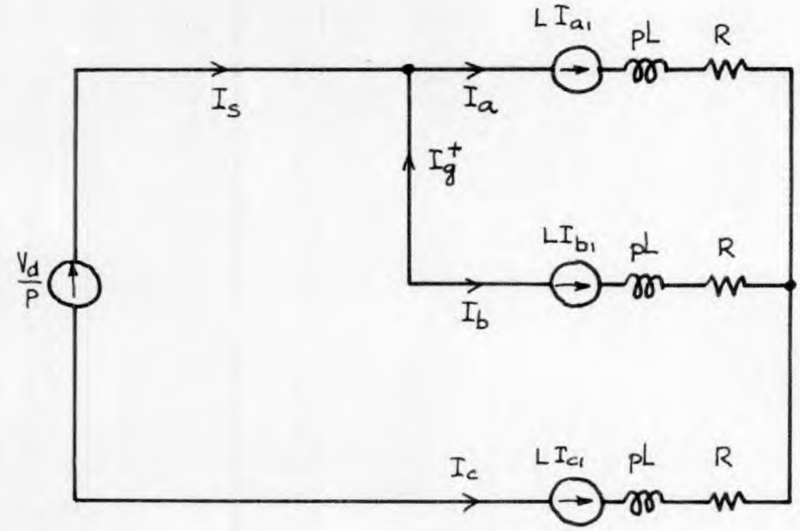


Fig. 5.32 : Operational circuit for obtaining load currents after commutation.

$$2I_a(pL + R) + I_b(pL + R) = \frac{V_d}{p} + 2\,L\,I_{a1} + L\,I_{b1} \qquad (5.56)$$

Eliminating I_b from equations (5.55) and (5.56)

$$I_a = \frac{I_{a1}}{p + \frac{R}{L}} + \frac{V_d}{3Lp(p + \frac{R}{L})}$$

Inverting, we obtain,

$$\underline{\underline{i_a = \frac{V_d}{3R} + (I_{a1} - \frac{V_d}{3R})e^{-\frac{Rt}{L}}}} \qquad (5.57)$$

Similarly,

$$\underline{\underline{i_b = \frac{V_d}{3R} + (I_{b1} - \frac{V_d}{3R})e^{-\frac{Rt}{L}}}} \qquad (5.58)$$

and then,

$$\underline{\underline{i_c = -\frac{2V_d}{3R} + (I_{c1} + \frac{2V_d}{3R})e^{-\frac{Rt}{L}}}} \qquad (5.59)$$

At the end of the sixth of a cycle $t = T_2$ where

$$T_2 = \frac{T}{6} - T_1 \qquad (5.60)$$

and i_a, i_b, i_c are equal to I_{a2}, I_{b2}, I_{c2}.

Hence

$$\underline{\underline{I_{a2} = \frac{V_d}{3R} + (I_{a1} - \frac{V_d}{3R})e^{-\frac{RT_2}{L}}}} \qquad (5.61)$$

$$I_{b2} = \frac{V_d}{3R} + (I_{b1} - \frac{V_d}{3R})e^{-\frac{RT_2}{L}} \qquad (5.62)$$

$$I_{c2} = \frac{2V_d}{3R} + (I_{c1} + \frac{2V_d}{3R})e^{-\frac{RT_2}{L}} \qquad (5.63)$$

During the period CR_1, D_3 and either D_2 or CR_2 conduct. Hence

$$v_{ab} = 0 \qquad (5.64)$$

$$v_{bc} = V_d \qquad (5.65)$$

$$v_{ca} = -V_d \qquad (5.66)$$

The current i_s taken from supply is equal to i_c, independent of whether this current flows in CR_2 or D_2.

The current in CR_1 is equal to i_a.

The current in the positive line of the reverse diode bridge is equal to $(-i_b)$.

The current in the negative line of the reverse diode bridge is equal to i_c when i_c is positive and zero when i_c is negative.

The current in CR_2 is equal to $(-i_c)$ when i_c is negative and zero when i_c is positive.

5.4.3 Relationship between I_{ao}, I_{bo}, I_{co} and I_{a2}, I_{b2}, I_{c2}.

Since the values of i_a, i_b, i_c at the end of the sixth of a cycle are the starting values for the next sixth of a cycle the values of I_{ao}, I_{bo}, I_{co} must be related to I_{a2}, I_{b2}, I_{c2}. In fact it can be seen that

$$I_{a2} = -I_{bo} \tag{5.67}$$

$$I_{b2} = -I_{co} \tag{5.68}$$

$$I_{c2} = -I_{ao} \tag{5.69}$$

5.4.4. Determination of I_{ao}, I_{bo} and I_{co}.

During a complete half cycle starting at instant t_2, i_a starts with a value I_{ao} and changes according to equations (5.45) and (5.57) until it becomes I_{a2} at instant t_3. From t_3 to t_4 i_a varies in the same manner as $(-i_b)$ did between t_2 and t_3 starting with a value $-I_{bo}$ which is equal to I_{a2}. At t_4 i_a reaches the value $-I_{b2}$ which is equal to I_{co}. In the next sixth of a cycle i_a starts with the value I_{co} and varies in the same way as i_c did between t_2 and t_3 and at t_5 reaches the value I_{c2} which is equal to $-I_{ao}$.

This gives a very convenient method of finding I_{ao}, I_{bo} and I_{co}. A value of I_{ao} may be assumed and the sequence described in the above paragraph followed using in turn equations (5.47), (5.61), (5.67), (5.48), (5.62), (5.68), (5.49), (5.63). The value of I_{c2} obtained at the end of this sequence should be equal to the assumed value of $(-I_{ao})$. If not, the sequence should be repeated with new assumed values of I_{ao} until agreement is obtained. Then I_{ao}, I_{a1}, I_{bo}, I_{b1}, I_{co}, I_{c1} will also have been calculated in the process.

5.4.5. Calculated Waveforms for Zero Power Factor Load with Commutation Effects neglected.

If the commutation period can be assumed to be of negligible duration I_{a1}, I_{b1}, I_{c1} are equal to I_{ao}, I_{bo}, I_{co} respectively.

If R is zero, equations (5.57), (5.58), (5.59) can be modified by putting $e^{-\frac{Rt}{L}} = (1 - \frac{Rt}{L})$ and then putting $R = 0$.

Then under these conditions, neglecting commutation,

$$i_a = I_{ao} + \frac{V_d t}{3L} \tag{5.70}$$

$$i_b = I_{bo} + \frac{V_d t}{3L} \tag{5.71}$$

$$i_c = I_{co} - \frac{2V_d t}{3L} \tag{5.72}$$

Then, putting $t = \frac{T}{6}$,

$$I_{a2} = I_{ao} + \frac{V_d T}{18L} \tag{5.73}$$

$$I_{b2} = I_{bo} + \frac{V_d T}{18L} \tag{5.74}$$

$$I_{c2} = I_{co} - \frac{2V_d T}{18L} \tag{5.75}$$

Now from equations (5.67) and (5.73)

$$I_{bo} = -I_{a2} = - I_{ao} - \frac{V_d T}{18L}$$

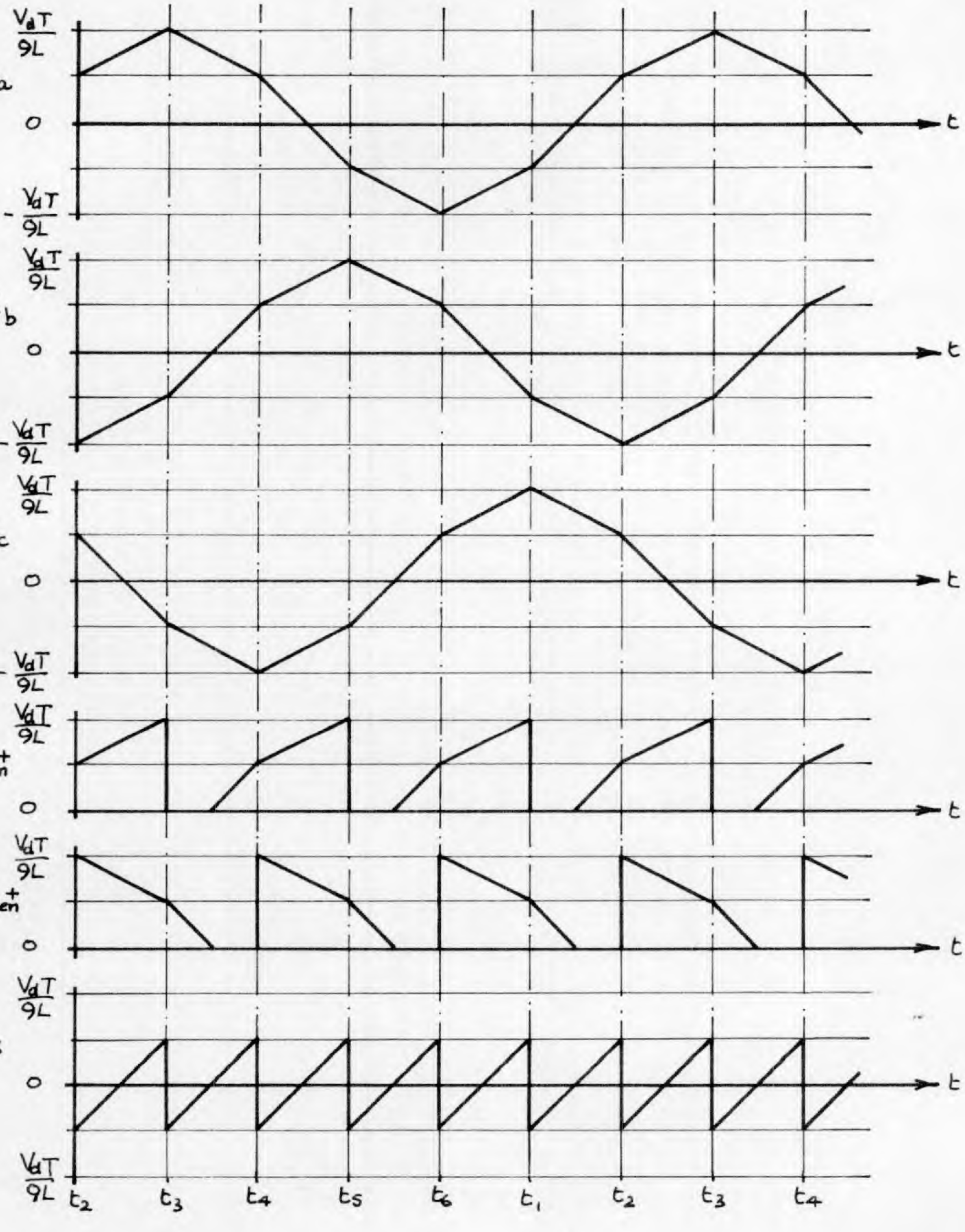


Fig. 5.33: Waveforms of i_a, i_b, i_c and i_{in}^+, i_{gen}^+, i_s. Calculated for zero power factor load (R=0), ignoring commutation period.

Then from equation (5.74)

$$I_{b2} = I_{bo} + \frac{V_d T}{18L}$$

$$= - I_{ao}$$

Then from equation (5.68)

$$I_{co} = - I_{b2} = I_{ao}$$

Thus from equation (5.75)

$$I_{c2} = I_{ao} - \frac{2 V_d T}{18L}$$

But I_{c2} should be equal to $- I_{ao}$

$$\therefore \quad 2 I_{ao} = \frac{2 V_d T}{18L}$$

and $$\underline{\underline{I_{ao} = \frac{V_d T}{18L}}}$$

Then $$\underline{\underline{I_{bo} = - \frac{V_d T}{9L}}}$$

and $$\underline{\underline{I_{co} = \frac{V_d T}{18L}}}$$

Using these initial values in equations (5.70), (5.71) and (5.72) the variations in i_a, i_b and i_c between instants t_2 and t_3 have been calculated and plotted on Fig. 5.33. The complete waveforms of i_a, i_b and i_c have then been derived from the variations. Also shown in Fig. 5.33 are the waveforms of current in the S C R bridge and reverse diode bridge d.c. lines and of the current taken from the d.c. supply. It should be noted that the currents in the S C R and reverse diode bridges have the same mean value and that there is, therefore, no mean power supplied to the load. This is further emphasized by the supply current waveform which has a mean value of zero.

5.4.6. Typical Load Current and Voltage Waveforms.

Fig. 5.34 shows typical load current and voltage waveforms for a low power factor load. In the case shown the load time constant, $\frac{L}{R}$, is equal to one cycle. The dotted lines indicate how the first half cycle of the current waveform has been constructed.

During the commutation period, of duration T_1, following instant t_2 i_a starts from its initial value I_{ao} and changes towards the value $-\frac{V_d}{3R}$ with time constant $\frac{L}{R}$. At the end of the commutation period i_a attains a value I_{a1}. In the remainder of the sixth of a cycle before instant t_3 i_a changes from I_{a1} towards $+\frac{V_d}{3R}$ with time constant $\frac{L}{R}$ and reaches a value I_{a2} at t_3. I_{a2} is equal to the value $-I_{bo}$, i.e. the value of i_b at instant t_2, and in the next sixth of a cycle i_a changes in the same way as $-i_b$ had done between instants t_2 and t_3. First i_a changes from $-I_{bo}$ towards $-\frac{2V_d}{3R}$ and then from $-I_{b1}$ towards $-\frac{V_d}{3R}$, each time with time constant $\frac{L}{R}$. At instant t_4 i_a is equal to $-I_{b2}$ which is equal to I_{co}, i.e. the value of i_c at instant t_2. In the next sixth of a cycle i_a changes as i_c had done between t_2 and t_3, changing first from I_{co} towards $-\frac{V_d}{3R}$ and then from I_{c1} towards $\frac{2V_d}{3R}$, each time with time constant $\frac{L}{R}$. The next half cycle is identical with the first half cycle except that the direction of i_a is reversed.

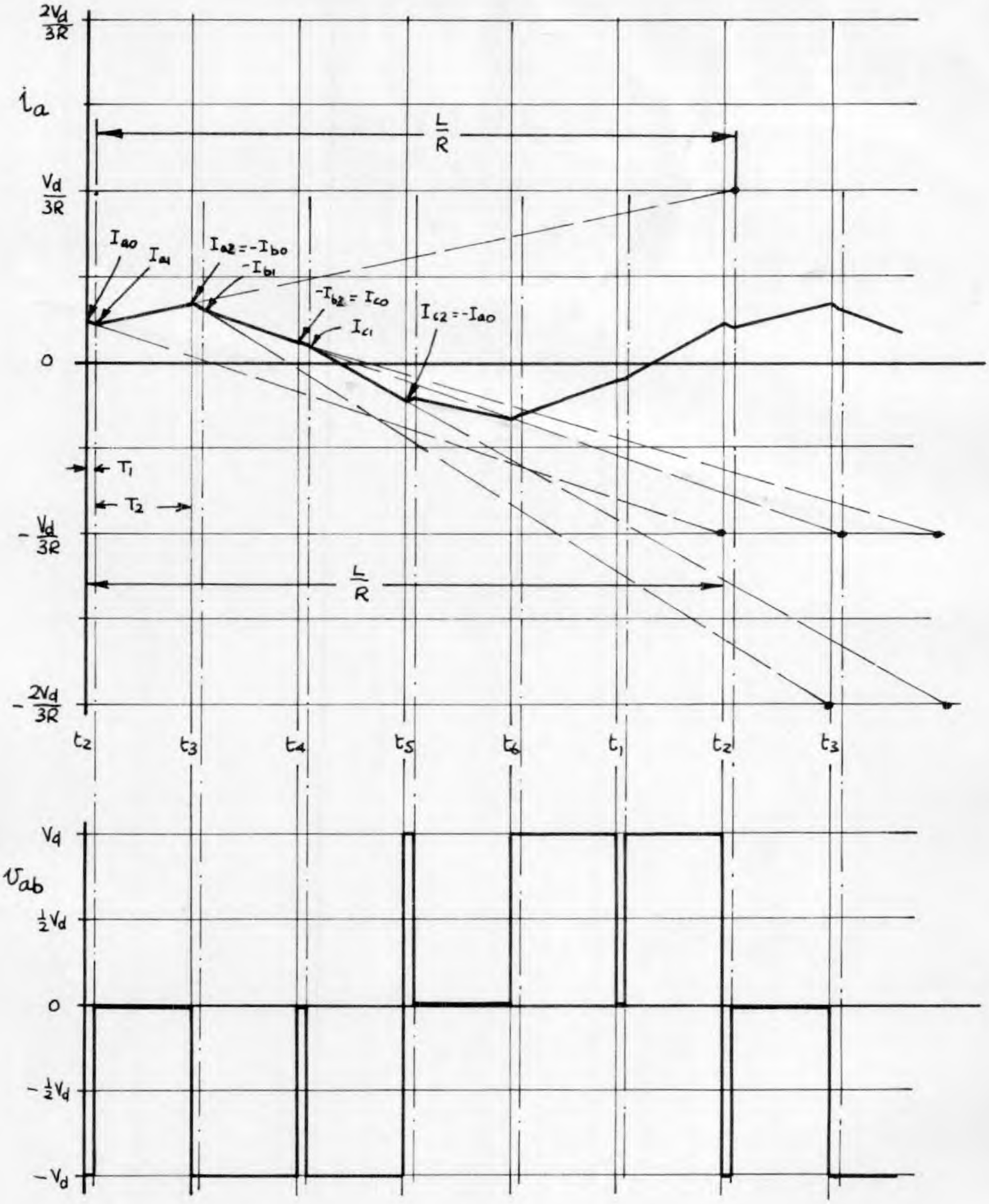


Fig. 5.34 : Typical load current and voltage waveforms for low power factor loads.

The waveforms of v_{ab} shown in Fig. 5.34 is very similar to the waveform of v_{ab} shown in Fig. 5.24 except that period 2 extends to the end of each sixth of a cycle. It should also be noted that the voltages between output lines during the commutation periods in Fig. 5.34 are zero or $\pm V_d$ whereas in Fig. 5.24 they are $\pm V_d$ or $\pm \frac{1}{2} V_d$. This is because in the low power factor case three diodes conduct during the commutation periods whereas in the high power factor case only two diodes conduct.

5.5. Approximate Harmonic Content of Output Line-to-Line Voltage Waveform for High Power Factor Load.

5.5.1 Analysis of Line-to-Line Voltage Waveform.

If the typical output line-to-line voltage waveforms shown in Fig. 5.24 are examined closely, it is seen that they consist of the basic three-phase bridge output voltage waveforms together with deviations caused by the operation of the diodes D_1, D_2.... D_6. Fig. 5.35(a) shows the basic component of the waveform of v_{ab} and Fig. 5.35(b) shows the deviations which when added to the basic waveform give the waveform in Fig. 5.24.

The deviations consist of positive and negative rectangular pulses, one set of magnitude $\frac{3\ V_d}{2}$ and duration T_1, the other set of magnitude $\frac{V_d}{2}$ and duration T_2. The duration T_1 of the first set of pulses is largely independent of load, being the period of discharge of the commutating capacitor, while the duration T_2 of the second set is very much dependent upon the load current and the load time constant.

Under normal circumstances the time T_1 would be very small compared with one sixth of a cycle. A typical figure for T_1 would be 100 to 150 μ Secs, i.e. T_1 would be 3 to 5% of a sixth of a cycle at 50 $^c/s$. T_2, on the other hand, may occupy anything from a small fraction to almost the whole of a sixth of a cycle.

In order to obtain a relatively simple approximation for the variation with load of the harmonic content it is proposed to concentrate upon the effects of the pulses of duration T_2. To enable

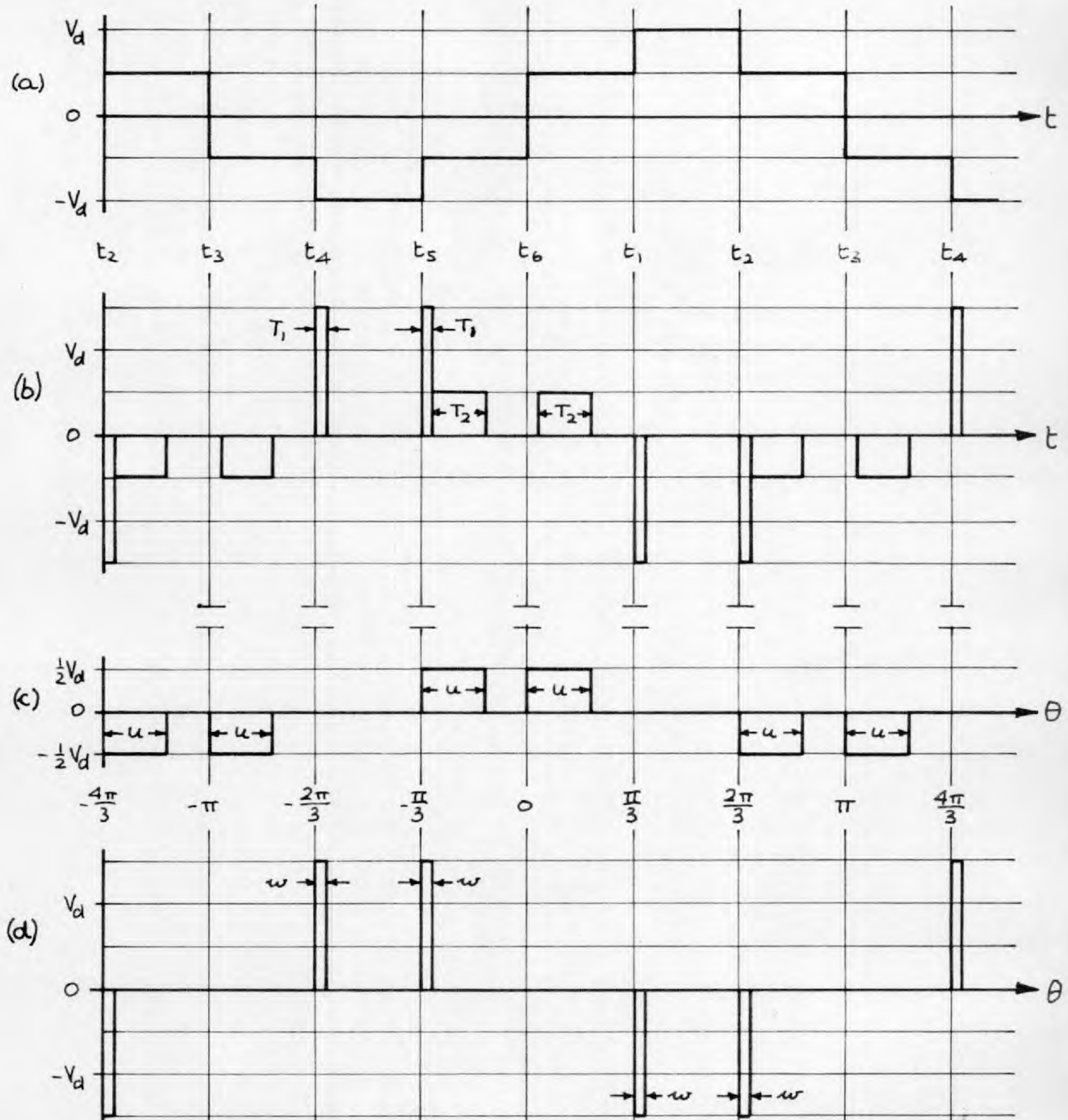


Fig. 5.35 : (a) Basic waveform of line-to-line voltage v_{ab}.

(b) Difference between typical and basic waveforms.

(c) Approximate period 2 deviations from basic waveforms.

(d) Period 1 deviations from basic waveforms.

allowance to be made for the effects of the pulses of duration T_1, where this should prove necessary, e.g. at the high frequencies, formulae for the harmonic contribution of these pulses will also be given.

Fig. 5.35(c) shows an approximation for the deviations from the basic waveform, neglecting period 1, plotted against θ, where $\theta = 2\pi ft$. The pulses have an angular width u, where $u = 2\pi f\, T_2$, and are assumed to start at the beginning of the sixths of a cycle in which they occur. This introduces a small error in the phase relationship of these pulses to the basic waveform. Fig. 5.35(d) shows the deviations from the basic waveform which are of duration T_1, i.e. neglecting period 2. The angular width of these pulses is w, where $w = 2\pi f\, T_1$. θ is taken to be zero at the instant t_6.

The harmonic content of the output voltage v_{ab} may thus be separated into three parts, i.e. the constant basic harmonics, the load-dependent harmonics due to period 2, and the harmonics due to commutation. Each part's contribution will now be found from a Fourier Analysis.

5.5.2. <u>Harmonic Content of Basic Waveform.</u>

If θ is taken to be zero at instant t_6, the harmonic components of the basic waveform consist of sine terms only, the waveform being made an odd function. Hence the basic waveform may be expressed as

$$(v_{ab})_{basic} = \sum_{n=1}^{n=\infty} a_n \sin n\,\theta \quad \text{where } a_n \text{ is the peak}$$

value of the nth harmonic.

$$\text{Then } a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} (v_{ab})_{basic} \sin n\,\theta\, d\theta$$

$$= \frac{V_d}{\pi}\left\{ \int_{0}^{\frac{\pi}{3}} \sin n\theta\, d\theta + 2\int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \sin n\theta\, d\theta + \int_{\frac{2\pi}{3}}^{\pi} \sin n\theta\, d\theta \right.$$

i.e. $$\underline{\underline{a_n = \frac{4V_d}{n\pi} \sin\frac{n\pi}{3} \sin\frac{n\pi}{2} \cos\frac{n\pi}{6}}} \qquad (5.76)$$

When n is even $\sin\frac{n\pi}{2} = 0$ and hence the basic waveform contains only odd harmonics.

When n is any multiple of three $\sin\frac{n\pi}{3} = 0$ and hence the basic waveform contains only odd harmonics which are not multiples of three, i.e. n = 1, 5, 7, 11, 13, 17, 19, 23, etc.

Table 5.1 gives the peak and r.m.s. values of the first five harmonics in the basic waveform calculated from equation (5.76).

n	Peak value, a_n	R.m.s. value, $\frac{a_n}{\sqrt{2}}$
1	$+ 0.955\ V_d$	$+ 0.675\ V_d$
5	$+ 0.191\ V_d$	$+ 0.135\ V_d$
7	$+ 0.136\ V_d$	$+ 0.096\ V_d$
11	$+ 0.087\ V_d$	$+ 0.062\ V_d$
13	$+ 0.073\ V_d$	$+ 0.052\ V_d$

Table 5.1 : <u>Harmonic content of basic output voltage waveform.</u>

5.5.3. Harmonic Content of the Period 2 Deviations from the Basic Output Voltage Waveform.

Since $\theta = 0$ at instant t_6 the waveform of these deviations is neither an even nor an odd function and therefore contains sine and cosine terms. Hence the period 2 deviations may be expressed as

$$(v_{ab})_{deviations_2} = \sum_{n=1}^{n=\infty} b_n \sin n\theta + c_n \cos n\theta \qquad \text{where}$$

b_n and c_n are the peak values of the sine and cosine components of the nth harmonic.

$$\text{Then } \; b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} (v_{ab})_{deviations\ 2} \sin n\theta \; d\theta$$

From Fig. 5.35(c) it may be seen that

$$b_n = \frac{V_d}{2\pi}\left\{\int_{-\pi}^{-\pi+u} -\sin n\theta \, d\theta + \int_{-\frac{\pi}{3}}^{-\frac{\pi}{3}+u} \sin n\theta \, d\theta + \int_{0}^{u} \sin n\theta \, d\theta \right.$$

$$\left. + \int_{\frac{2\pi}{3}}^{\frac{2\pi}{3}+u} -\sin n\theta \, d\theta \right\}$$

This expression for b_n may be reduced to

$$b_n = \frac{2V_d}{\pi n} \sin\frac{n\pi}{2} \sin\frac{n\pi}{3}\left\{\cos\frac{n\pi}{6} - \cos n\left(u - \frac{\pi}{6}\right)\right\} \qquad (5.77)$$

By a similar method an expression for c_n may be obtained. This gives

$$c_n = \frac{2V_d}{\pi n} \sin\frac{n\pi}{2} \sin\frac{n\pi}{3} \left\{ \sin\frac{n\pi}{6} + \sin n(u - \frac{\pi}{6}) \right\} \qquad (5.78)$$

When n is even $\sin\frac{n\pi}{2} = 0$ and when n is any multiple of three $\sin\frac{n\pi}{3} = 0$. Hence the period 2 deviations contribute only odd harmonics which are not multiples of three, just as the basic waveforms did.

Table 5.2 below gives the r.m.s. values of the sine and cosine components of the first five harmonics contributed by the deviations. The values are given in terms of u and are calculated from equations (5.77) and (5.78).

n	$\frac{1}{\sqrt{2}} b_n$	$\frac{1}{\sqrt{2}} c_n$
1	$+ 0.390\ V_d\{0.866 - \cos(u - 30^\circ)\}$	$+ 0.390\ V_d\{0.5 + \sin(u - 30^\circ)\}$
5	$+ 0.078\ V_d\{0.866 + \cos5(u - 30^\circ)\}$	$- 0.078\ V_d\{0.5 + \sin5(u - 30^\circ)\}$
7	$+ 0.056\ V_d\{0.866 + \cos7(u - 30^\circ)\}$	$+ 0.056\ V_d\{0.5 - \sin7(u - 30^\circ)\}$
11	$+ 0.035\ V_d\{0.866 - \cos11(u - 30^\circ)\}$	$- 0.035\ V_d\{0.5 - \sin11(u - 30^\circ)\}$
13	$+ 0.028\ V_d\{0.866 - \cos13(u - 30^\circ)\}$	$+ 0.028\ V_d\{0.5 + \sin13(u - 30^\circ)\}$

Table 5.2 : Harmonic content of the period 2 deviations from the basic output voltage waveform.

u may have any value between 0 and 60°. Fig. 5.36 shows how the values of $\frac{b_n}{\sqrt{2}}$ and $\frac{c_n}{\sqrt{2}}$ vary with u.

5.5.4. Harmonic Content of the Period 1 Deviations from the Basic Output Voltage Waveform.

Since $\theta = 0$ at instant t_6 the waveform of the period 1 deviations

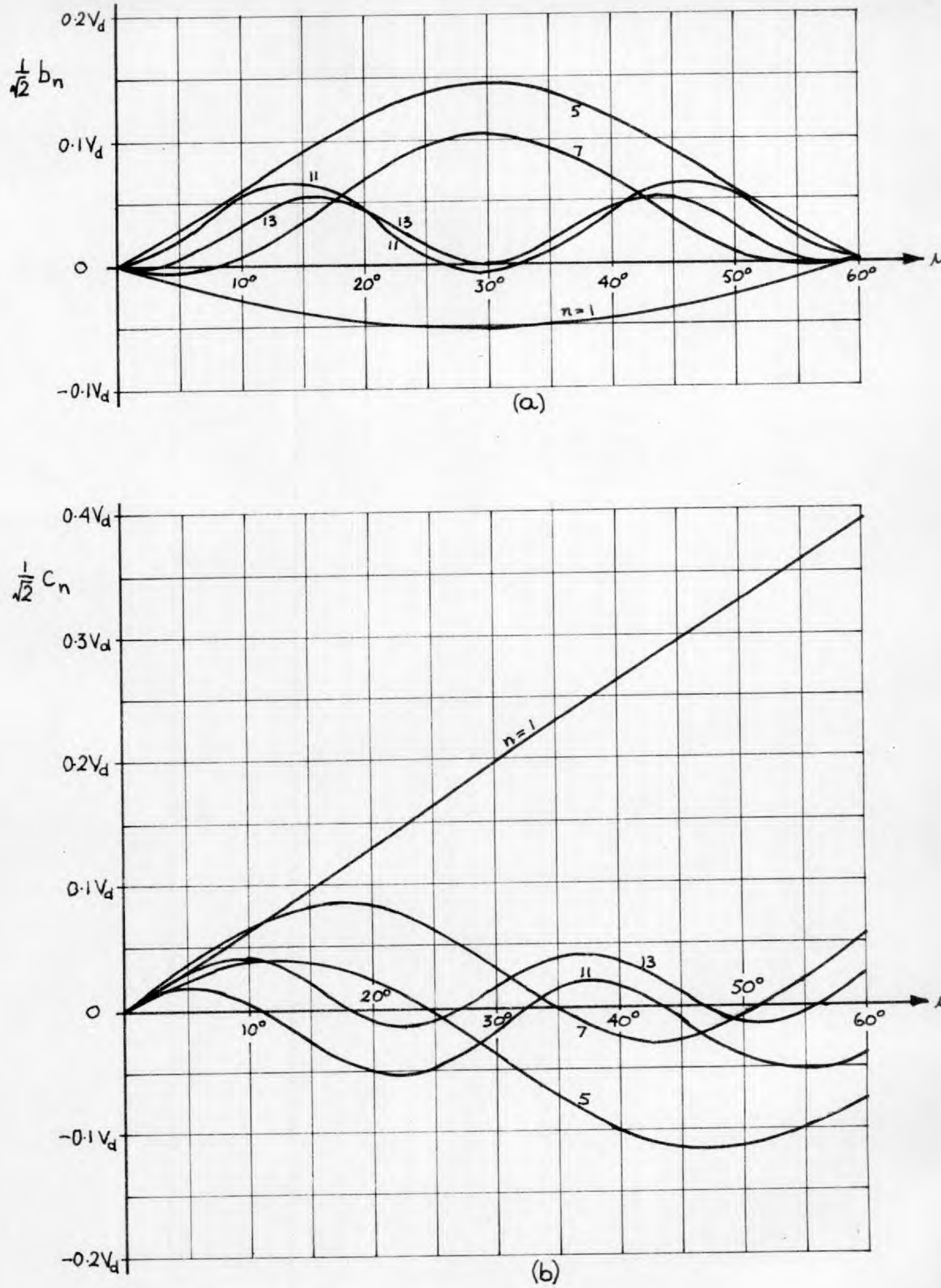


Fig. 5. 36 : Variation with u of (a) $\frac{1}{\sqrt{2}} b_n$, (b) $\frac{1}{\sqrt{2}} c_n$.

is neither an even nor an odd function and consequently contains both sine and cosine terms. The period 1 deviations may therefore be expressed as

$$(v_{ab})_{\text{deviations } 1} = \sum_{n=1}^{n=\infty} \left\{ b'_n \sin n\theta + c'_n \cos n\theta \right\}$$ where b'_n and c'_n are the peak values of the sine and cosine components of the nth harmonic.

Then

$$b'_n = \frac{1}{\pi} \int_{-\pi}^{\pi} (v_{ab})_{\text{deviations } 1} \sin n\theta \, d\theta$$

Taking the values of $(v_{ab})_{\text{deviations } 1}$ from Fig. 5.35(d),

$$b'_n = \frac{3V_d}{2\pi} \left\{ \int_{-\frac{2\pi}{3}}^{-\frac{2\pi}{3}+w} \sin n\theta \, d\theta + \int_{-\frac{\pi}{3}}^{-\frac{\pi}{3}+w} \sin n\theta \, d\theta + \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+w} (-\sin n\theta) d\theta + \int_{\frac{2\pi}{3}}^{+\frac{2\pi}{3}+w} (-\sin n\theta) d\theta \right\}$$

i.e. $$b'_n = -\frac{6V_d}{\pi n} \sin n w \sin \frac{\pi n}{2} \cos \frac{\pi n}{6} \qquad (5.79)$$

Similarly,

$$c'_n = \frac{3V_d}{2\pi} \left\{ \int_{-\frac{2\pi}{3}}^{-\frac{2\pi}{3}+w} \cos n\theta \, d\theta + \int_{-\frac{\pi}{3}}^{-\frac{\pi}{3}+w} \cos n\theta \, d\theta + \int_{\frac{\pi}{3}}^{\frac{\pi}{3}+w} (-\cos n\theta) d\theta + \int_{\frac{2\pi}{3}}^{\frac{2\pi}{3}+w} (-\cos n\theta) d\theta \right\}$$

$$\text{i.e.}\quad c'_n = \frac{6V_d}{\pi n}(1 - \cos nw)\sin\frac{\pi n}{2}\cos\frac{\pi n}{6} \tag{5.80}$$

When n is an even number $\sin\frac{\pi n}{2} = 0$ and when n is any odd multiple of three $\cos\frac{\pi n}{6} = 0$. Hence the period 1 deviations contribute only odd harmonics which are not multiples of three.

Table 5.3 gives the rms values of the magnitudes of the sine and cosine components for the first five harmonics contributed by the period 1 deviations from the basic waveforms. The values are given in terms of w and are calculated from equations (5.79) and (5.80).

n	$\frac{1}{\sqrt{2}} b'_n$	$\frac{1}{\sqrt{2}} c'_n$
1	$-1.17\ V_d \sin w$	$1.17\ V_d(1 - \cos w)$
5	$0.234\ V_d \sin 5w$	$-0.234\ V_d(1 - \cos 5w)$
7	$-0.167\ V_d \sin 7w$	$0.167\ V_d(1 - \cos 7w)$
11	$0.106\ V_d \sin 11w$	$-0.106\ V_d(1 - \cos 11w)$
13	$-0.090\ V_d \sin 13w$	$0.090\ V_d(1 - \cos 13w)$

Table 5.3: Harmonic content of the period 1 deviations from the basic output voltage waveform.

5.5.5. Total Harmonic Content of Output Voltage Waveform.

When the values of b_n, b'_n, c_n and c'_n have been found for each value of u and w the total r.m.s. value of each harmonic can be found. Normally w would be very small and the b'_n and c'_n terms neglected. In this case the sine and cosine components of the output voltage waveform would have r.m.s. values $(\frac{1}{\sqrt{2}} a_n + \frac{1}{\sqrt{2}} b_n)$ and $\frac{1}{\sqrt{2}}$ c_n respectively. The total r.m.s. value, $\frac{1}{\sqrt{2}}$ d_n, of the nth harmonic would then be obtained by adding vectorially the sine and cosine terms, i.e.

$$\frac{1}{\sqrt{2}} d_n = \sqrt{(\frac{1}{\sqrt{2}} a_n + \frac{1}{\sqrt{2}} b_n)^2 + \frac{1}{2} c_n^2} \tag{5.81}$$

V_ℓ (r.m.s.), which is the total r.m.s. value of the line-to-line output voltage, may then be found for each value of u from

$$V_{\ell\,(r.m.s.)} = \sqrt{\sum_{n=1}^{\infty} \frac{d_n^2}{2}}$$

i.e.

$$V_{\ell\,(r.m.s.)} = \sqrt{\tfrac{1}{2}(d_1^2 + d_5^2 + d_7^2 + d_{11}^2 + d_{13}^2 + \ldots)} \tag{5.82}$$

In Fig. 5.37 the total r.m.s. values of the first five harmonics are shown as a function of u. The effect of the period 1 deviations is neglected. The values of $V_{\ell\,(r.m.s.)}$, also shown in Fig. 5.37 have been calculated from the first five values of $\frac{1}{\sqrt{2}} d_n$ and higher harmonics neglected.

The phase advance, γ_n of each harmonic from the corresponding waveform in the basic harmonic may be found from

$$\gamma_n = \tan^{-1}(\frac{c_n}{a_n + b_n}) \tag{5.83}$$

Fig. 5.38 shows γ_n plotted against u for the first five harmonics. γ_1 is seen to increase almost linearly with u

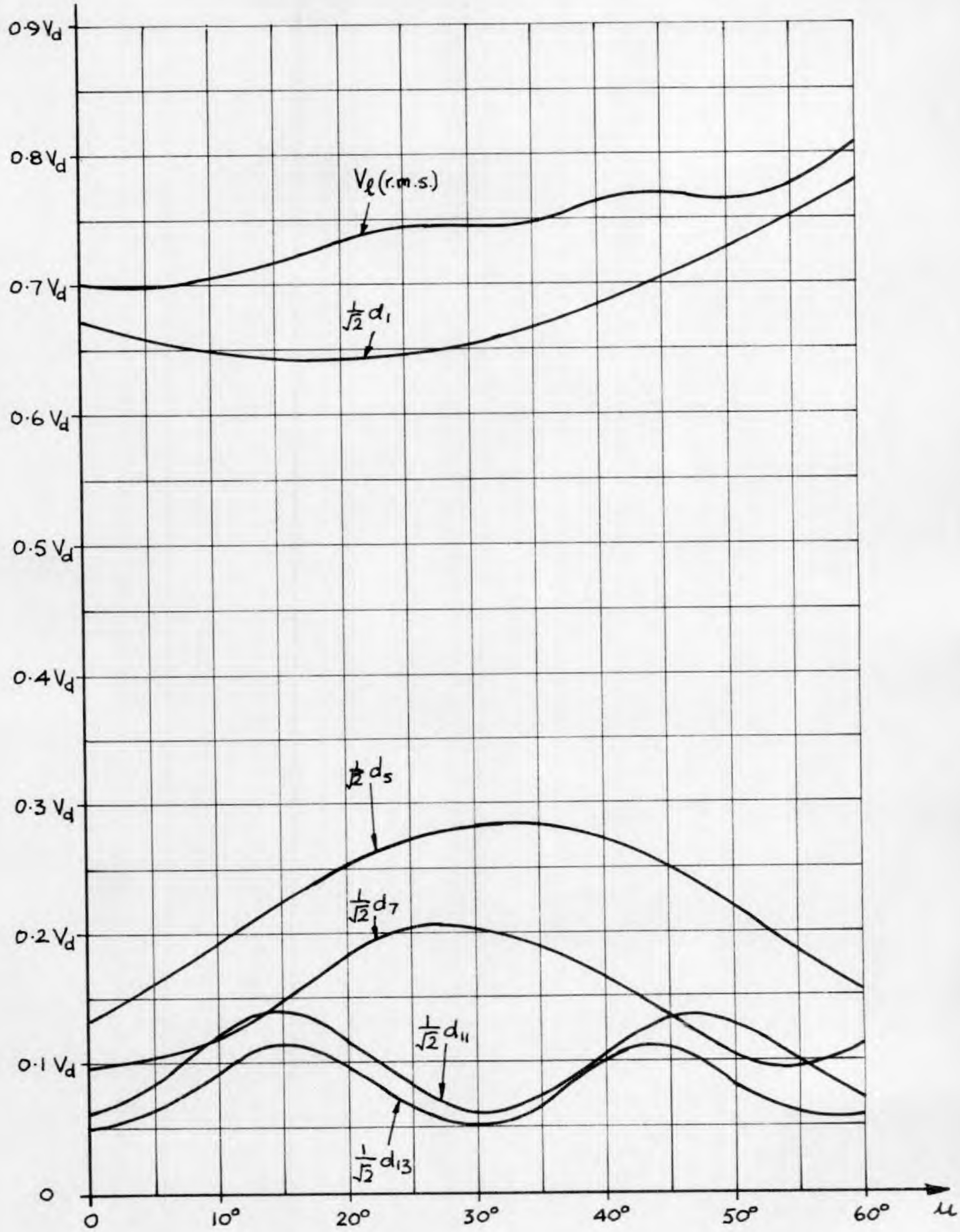


Fig. 5.37 : Variation with u of the r.m.s. values of the first five harmonics and the total r.m.s. value of the output line-to-line voltage.

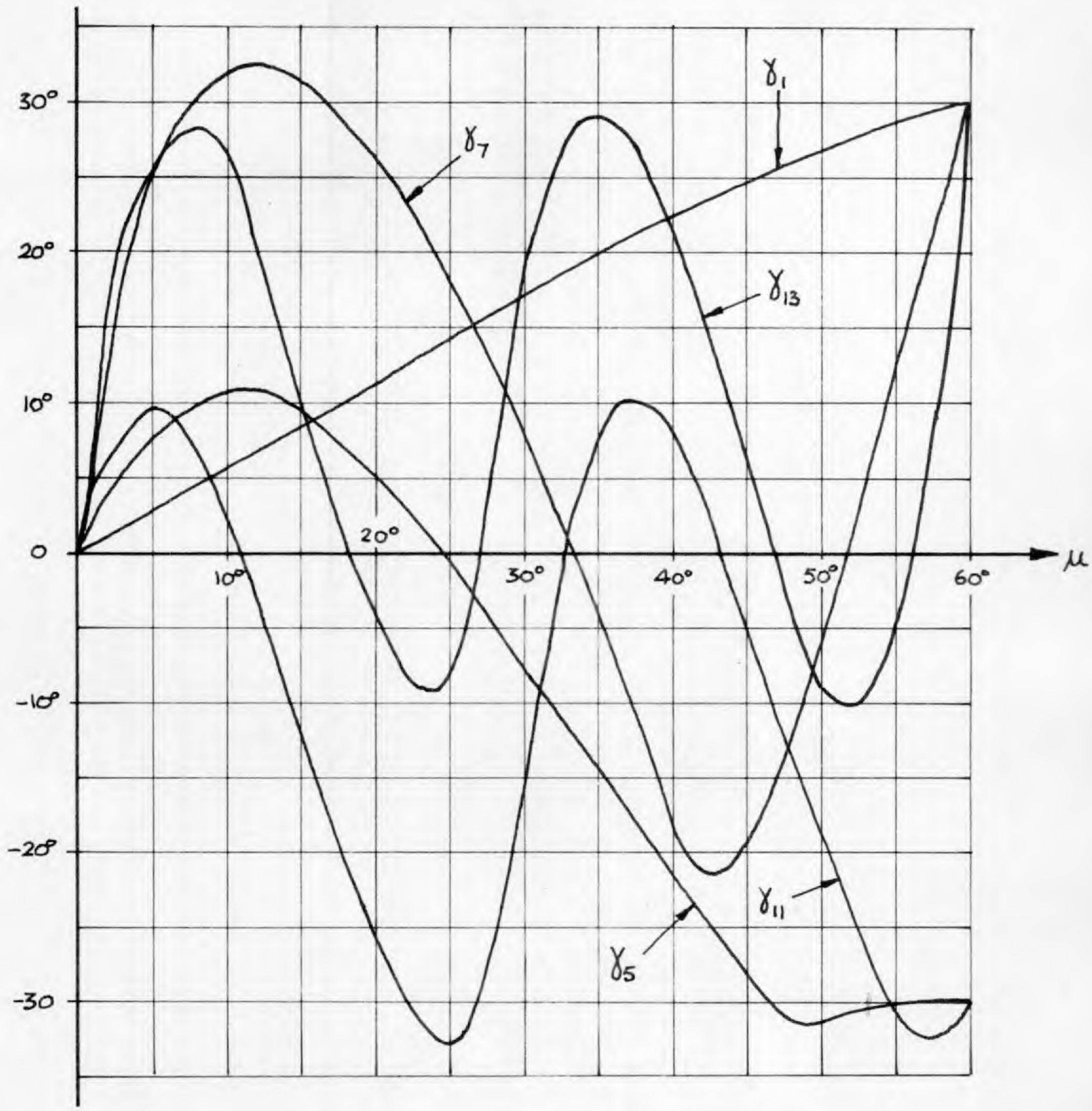


Fig. 5.38 : Variation of γ_n with u.

When w is not so small that b'_n and c'_n can be neglected its effect can be easily allowed for by adding b'_n to b_n and c'_n to c_n before finding $\frac{1}{\sqrt{2}} d_n$. Then equations (5.81 and (5.83) can be modified to

$$\frac{1}{\sqrt{2}}\ d_n = \sqrt{\left(\frac{1}{\sqrt{2}}\, a_n + \frac{1}{\sqrt{2}}\, b_n + \frac{1}{\sqrt{2}}\, b'_n\right)^2 + \left(\frac{1}{\sqrt{2}}\, c_n + \frac{1}{\sqrt{2}}\, c'_n\right)^2} \qquad (5.84)$$

and

$$\gamma_n = \tan^{-1} \frac{c_n + c'_n}{a_n + b_n + b'_n} \qquad (5.85)$$

5.5.5. Approximate value of u.

In the approximate analysis of the inverter output voltage waveform the harmonic content and derived quantities are given in terms of the angle u. To obtain the value of u accurately for each load condition it would strictly be necessary to calculate the complete load current waveform as in section 5.3.6.2. However, it is possible to derive an approximate expression for u which can be useful for determining the approximate performance of the inverter.

Referring to the typical current waveform shown in Fig. 5.26 it is seen that T_2 is defined as the term for $-i_b$ to fall from I_{L1} to zero or for $-i_c$ to rise from zero to I_{L2}. In equation (5.31) it was shown that if $I_{L1} = \frac{V_d}{3R}(1 + x)$ then I_{L2} is approximately $\frac{V_d}{3R}(1 + \frac{x}{2})$, i.e. whatever value I_{L1} has, I_{L2} is always closer to $\frac{V_d}{3R}$. If I_{L2} can be assumed equal to $\frac{V_d}{3R}$, T_2, found from equation (5.19), is equal to $\frac{L}{R} \log_e 2$, i.e. $0.7\,\frac{L}{R}$.

This is a very approximate value, since a small change in the value of I_{L2} can produce a much larger change in the value of T_2, but it is a useful guide to the harmonics to be expected. Then u can be found from

$$u = 2\pi f T_2$$

$$\text{i.e. } u \approx \frac{0.7 \times 2 f L}{R} \qquad (5.86)$$

5.6. Harmonic Content of Output Line-to-Line Voltage Waveform for Low Power Factor Load.

The output line-to-line voltage waveform shown in Fig. 5.34 for a low power factor load can be broken down into the parts shown in Fig. 5.39. These constituent waveforms are very similar to those shown in Fig. 5.35 (a), (c) and (d) but in this case they add together exactly to give the complete waveform of Fig. 5.34. The period 2 deviations shown in Fig. 5.39(b) correspond to those of Fig. 5.35 (c). In Fig. 5.39(b), however, period 2 extends over the whole of the sixth of a cycle and u is therefore $\frac{\pi}{3}$, or 60°. The period 1 deviations shown in Fig. 5.39(c) correspond to those of Fig. 5.35(d) but are of two thirds the amplitude of those shown in Fig. 5.35(d).

It is clear, therefore, that the harmonic analyses carried out in section 5.5 for the high power factor load can be used again for the low power factor load. It is necessary only to put $u = \frac{\pi}{3}$ or 60° and to use values of b'_n and c'_n which are two thirds of those given in Table 5.3 for each value of w. Table 5.4 gives the values of $\frac{1}{\sqrt{2}}\ b'_n$ and $\frac{1}{\sqrt{2}}\ c'_n$ to be used for low power factor loads.

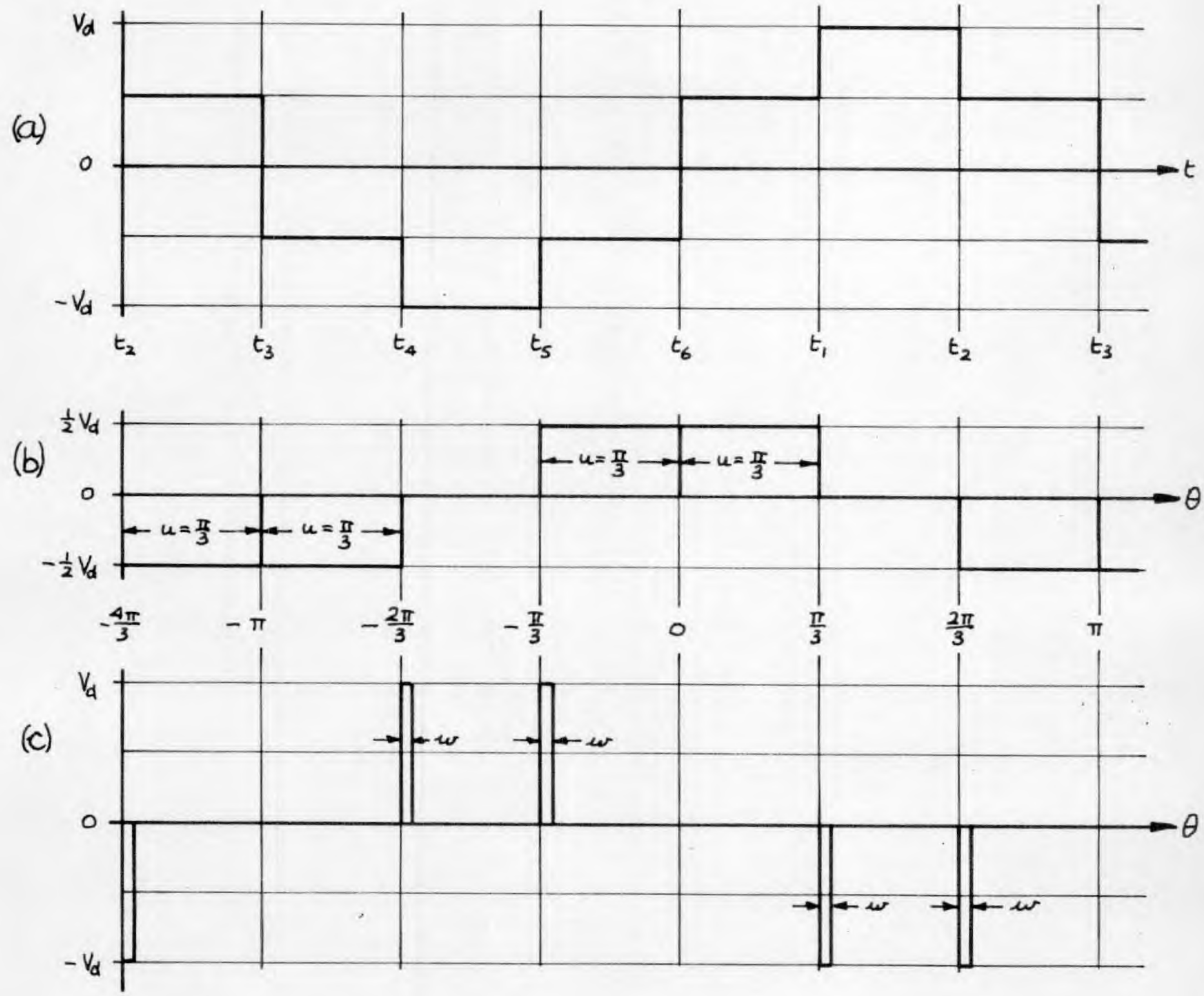


Fig. 5.39: Analysis of line-to-line output voltage waveform for low power factor load.

(a) Basic waveform of v_{ab}

(b) Period 2 deviations from basic waveform

(c) Period 1 deviations from the sum of waveforms (a) and (b)

n	$\frac{1}{\sqrt{2}} b'_n$	$\frac{1}{\sqrt{2}} c'_n$
1	$- 0.78 V_d \sin w$	$0.78 V_d (1 - \cos w)$
5	$0.16 V_d \sin 5 w$	$0.16 V_d (1 - \cos 5 w)$
7	$- 0.11 V_d \sin 7 w$	$0.11 V_d (1 - \cos 7 w)$
11	$0.07 V_d \sin 11 w$	$0.07 V_d (1 - \cos 11 w)$
13	$- 0.06 V_d \sin 13 w$	$0.06 V_d (1 - \cos 13 w)$

Table 5.4: Values of $\frac{1}{\sqrt{2}} b'_n$ and $\frac{1}{\sqrt{2}} c'_n$ to be used in equations (5.84) and (5.85) when the load power factor is low.

5.7 Commutation and Resulting Power Loss.

The S C Rs in the main bridge are turned off by introducing the negatively-charged capacitor C into the d.c. side of the bridge. The capacitor then charges to the main d.c. supply voltage and it is arranged that the charging is slow enough for the S C Rs to be reverse-biased long enough for correct turn off. During the capacitor charging period energy is taken from the main d.c. supply and it will be shown that this energy, together with the energy taken from the auxiliary supply, is transferred to the d.c. choke and thereafter dissipated in the form of an energy loss. At high frequencies this energy loss, repeated six times in each cycle, represents a significant power loss.

5.7.1. Re-charging Capacitor C from Auxiliary Supply.

The re-charging of capacitor C from the auxiliary supply was dealt with in section 5.3.4.5. It was shown that the capacitor voltage changed from $+V_d$ to $-V_{CR}$, where V_{CR} is equal to $(V_d + 2V_a)$. The resistance of the auxiliary circuit was neglected and the current in the current-limiting choke L_c was zero at the beginning and end of the re-charging process. Hence the energy E_a taken from the auxiliary supply during re-charging must be equal to the increase in stored energy of capacitor C.

$$\therefore \quad E_a = \tfrac{1}{2} C \left\{ (-V_{CR})^2 - V_d^{\,2} \right\}$$

$$= \tfrac{1}{2} C \left\{ (V_d + 2V_a)^2 - V_d^{\,2} \right\}$$

$$\text{i.e.} \quad \underline{\underline{E_a = 2\,C\,V_a(V_d + V_a) \quad \text{Joules}}} \qquad (5.87)$$

This energy is not lost at this stage but merely stored in capacitor C.

5.7.2. Discharging Capacitor C for Commutation.

During turn-off of the bridge S C Rs capacitor C is charged from $-V_{CR}$ to V_d. Any current flowing from the main supply in this time flows only through the d.c. choke and capacitor C and cannot flow into the load since all S C Rs are off. The current taken from the supply during this period is given by

$$i_d = \hat{I} \cos(\omega t - \phi) \text{ and flows for a time}$$

$$T_1 = \frac{\phi}{\omega} \quad \text{(See section 5.3.4.1.)}$$

Hence the energy E_d taken from the main supply during this period is given by

$$E_d = \int_0^{\frac{\phi}{\omega}} V_d \hat{I} \cos(\omega t - \phi)\, dt$$

$$= \frac{V_d \hat{I}}{\omega} \sin\phi$$

$$= \frac{V_d I_{do}}{\omega} \tan\phi$$

$$= \frac{V_d I_{do}}{\omega} \cdot \frac{V_d + V_{CR}}{I_{do}} \cdot \omega C$$

$$= C\, V_d\, (V_d + V_{CR})$$

i.e. $$\underline{E_d = 2\, C\, V_d\, (V_d + V_a) \text{ Joules}} \qquad (5.88)$$

Capacitor C is now back to its original state, charged to voltage $+V_d$, and so has no net gain in energy. Energy has been taken from the auxiliary and main supplies in the meantime, however, and hence the d.c. choke, being the only other storage element in the circuit, must have absorbed the sum of $E_a + E_d$. The current in the d.c. choke has increased from I_{do} to $\hat{I}$ and hence ΔE_{Ld} = increase in stored energy of the d.c. choke.

$$= \tfrac{1}{2} \times 4\, L_d\, (\hat{I}^2 - I_{do}^2)$$

$$\Delta E_{Ld} = 2 L_d \left\{ I_{do}^2 \left(1 + \frac{(V_d + V_{CR})^2}{16\omega^2 L_d^2 I_{do}^2}\right) - I_{do}^2 \right\}$$

$$\Delta E_{Ld} = \tfrac{1}{8} C(V_d + V_{CR})^2 \quad \text{since } \omega^2 = \frac{1}{4CL_d}$$

i.e. $$\underline{\underline{\Delta E_{Ld} = 2C(V_d + V_a)^2 \text{ Joules}}} \qquad (5.89)$$

As a check, $E_d + E_a = 2C\left\{ V_d^2 + V_dV_a + V_aV_d + V_a^2 \right\}$

i.e. $$\underline{\underline{E_d + E_a = 2C\,(V_d + V_a)^2 \text{ Joules}}} = \Delta E_{Ld} \qquad (5.90)$$

i.e. all the energy taken from the main supply during commutation and from the auxiliary supply is stored in the d.c. choke.

Between each commutation and the next the current in the d.c. choke decays from $\hat{I}$ back to I_{do} through the diodes D_7 and D_8 and hence the energy ΔE_{Ld} stored in the choke is dissipated as a loss in the circuit. The elements of the circuit in which the loss is dissipated are the resistance of the choke, the diodes D_7 and D_8, and any resistance associated with D_7 and D_8.

5.7.3. Power Loss due to Commutation and its Minimisation.

Since commutation takes place six times per cycle, the energy ΔE_{Ld} is dissipated at six times the output frequency of the inverter. Hence the mean power loss, P_{com}, due to commutation at an output frequency f $^c/s$ is given by

$$P_{com} = 6\,f\,.\,\Delta\,E_{Ld}$$

i.e. $$P_{com} = 12\,C\,f\,(V_d + V_a)^2 \text{ Watts} \qquad (5.91)$$

By choosing suitable values for V_a and C it is possible to minimise the power loss P_{com}. The basic requirement of the commutation circuit is that it should reverse bias the S C Rs in the inverter bridge for a long enough time for proper turn-off. If the minimum reverse bias time required is δ_m, it can be seen that the values of V_a and C necessary to give the minimum time δ_m are related to V_d and I_{do} approximately by the formula

$$\delta_m \simeq \frac{C(V_{CR} - V_d)}{I_{do}} \qquad \text{(from equation 5.5)}$$

Since $$V_{CR} = V_d + 2V_a$$

$$\delta_m \simeq \frac{2\,C\,V_a}{I_{do}} \qquad (5.92)$$

Hence the value of C required for given values of δ_m and V_a is given by

$$C = \frac{\delta_m I_{do}}{2V_a} \qquad (5.93)$$

Substituting for C in the expression for P_{com} in equation (5.91) we obtain

$$P_{com} = 6\,f\,\delta_m\,I_{do}\left\{\frac{V_d^2}{V_a} + 2\,V_d + V_a\right\} \qquad (5.94)$$

This formula is valid when C is adjusted for each combination of V_a and I_{do} to give the required value of δ_m.

Differentiating P_{com} with respect to V_a we obtain

$$\frac{d\,P_{com}}{d\,V_a} = 6\,f\,\delta_m\,I_{do}\left\{-\frac{V_d^2}{V_a^2} + 1\right\}$$

$$= 0 \text{ when } V_a = V_d$$

i.e. P_{com} is minimum when $V_a = V_d$

The minimum value $(P_{com})_{min}$ of P_{com} is then given by

$$(P_{com})_{min} = 6\,f\,\delta_m\,I_{do}\,(4\,V_d)$$

i.e. $$(P_{com})_{min} = 24\,f\,\delta_m\,V_d\,I_{do} \text{ Watts} \tag{5.95}$$

Since $V_d\,I_{do}$ is approximately equal to the power converted by the inverter the minimum power loss may be expressed as a percentage drop in efficiency.

i.e. $$\left(\frac{P_{com}}{P_{converted}}\right)_{min} \simeq 2400\,f\,\delta_m\,\% \tag{5.96}$$

It is seen that this loss is proportional to frequency and to δ_m and it is evidently important to select S C Rs with turn-off times as short as possible for inverter duty.

To attain the minimum possible commutation power loss under all operating conditions would in practice involve keeping V_a equal to V_d whilst varying C continuously with I_{do}. This would be quite impracticable but the formula can be used to find the maximum attainable efficiency of the inverter at any particular output frequency assuming, of course, that I_{do} is nearly equal to I_d.

For example, with $\delta_m = 50\ \mu$ Secs and at an output frequency of 50 $^c/s$ the minimum possible efficiency drop is equal to $2400 \times 50 \times 50 \times 10^{-6} = 6\%$, i.e. the maximum attainable efficiency of the inverter would be 94% neglecting all other losses in the circuit.

5.7.4. Variation of I_{do} and δ with Frequency.

At low inverter output frequencies when the current in diodes D_7 and D_8 becomes zero before the end of each sixth of a cycle, the currents in the load and the d.c. choke are equal at the start of the commutation process and hence $I_{do} = I_{Lo}$. I_{do} is therefore completely dependent upon the load at these low frequencies.

When the frequency is increased a stage is reached where the current in D_7 and D_8 just decays to zero at the end of each sixth of a cycle. Above this frequency the current in D_7 and D_8 cannot decay to zero and I_{do} assumes a value which is greater than I_{Lo}. This new value is such that the current in the d.c. choke can increase from I_{do} to $\hat{I}$ in the capacitor discharge period and decay from $\hat{I}$ back to I_{do} in the remainder of the sixth of a cycle. Consequently I_{do} would be expected to rise with frequency in some manner thereafter and become independent of the load to a lrge extent.

In the d.c. switch circuit it was found that the same thing happened and that I_{do} became proportional to the square root of frequency. An approximate analysis of the increase of I_{do} with frequency was carried out in section 4.6.2 and was based on the rate of decay of the d.c. choke current and the decrease of $(\hat{I} - I_{do})$ with increasing I_{do}. Exactly the same result may be obtained by studying the energies involved and it is felt that this method of analysis may give a clearer picture of the problem.

At commutation the stored energy of the d.c. choke is increased by ΔE_{Ld} where

$$\Delta E_{Ld} = 2 C (V_d + V_a)^2 \quad \text{(from equation 5.89)}$$

Before the next commutation takes place this energy must be dissipated in the resistance R_d of each half of the d.c. choke and in the diodes D_7 and D_8. If $\hat{I}$ is not very much greater that I_{do}, the r.m.s. values of the current flowing in the choke can be taken to be approximately equal to I_{do}. It is also assumed that the current in diodes D_7 and D_8 is equal to that flowing in the choke and that the effect of the diodes can be represented as an effective resistance which when added to R_d gives a total effective resistance R'_d per half of the d.c. choke. Then, neglecting the duration T_1 of the commutation process compared with $\frac{1}{6f}$, the energy dissipated in one sixth of a cycle in the resistance of both halves of the d.c. choke and in the diodes D_7 and D_8 is $2 I_{do}^2 R'_d \times \frac{1}{6f}$, i.e. power multiplied by time. This energy must be equal to ΔE_{Ld} and hence

$$\Delta E_{Ld} \doteq 2 I_{do}^2 R_d' \times \frac{1}{6f} = 2C(V_d + V_a)^2$$

$$\therefore I_{do}^2 \simeq \frac{6Cf(V_d + V_a)^2}{R_d'}$$

$$\text{i.e.} \quad I_{do} \simeq (V_d + V_a)\sqrt{\frac{6Cf}{R_d'}} \tag{5.97}$$

or alternatively

$$I_{do} \simeq \tfrac{1}{2}(V_d + V_{CR})\sqrt{\frac{6Cf}{R_d'}} \tag{5.98}$$

since $\quad (V_d + V_{CR}) = 2(V_d + V_a)$

It is seen that I_{do} becomes proportional to the square root of frequency and independent of the inductance of the d.c. choke.

From equation 5.5 the reverse-bias time δ of the bridge S C R being turned off is given approximately by

$$\delta \simeq \frac{C(V_{CR} - V_d)}{I_{do}}$$

Substituting for I_{do} from equation (5.98)

$$\text{i.e.} \quad \delta \simeq \frac{2(V_{CR} - V_d)}{V_{CR} + V_d}\sqrt{\frac{R_d'}{6Cf}} \tag{5.99}$$

or alternatively, since $(V_{CR} - V_d) = 2V_a$ and $(V_{CR} + V_d) = 2(V_a + V_d)$

$$\delta \simeq \frac{2V_a}{V_a + V_d}\sqrt{\frac{R_d'}{6Cf}} \tag{5.100}$$

It is seen that δ becomes inversely proportional to the square root of frequency and independent of the inductance of the d.c. choke.

5.7.5. Variation of I_{do} with Load Current at High Frequency.

In the previous section where the variation of I_{do} with frequency was discussed no account was taken of the effect of the load current upon the decay of choke current from I to I_{do}. Current drawn from the supply has the effect of reducing the current flowing in diodes D_7 and D_8 and consequently reduces the voltage applied to the choke. It is clear, therefore, that the load current must have some effect upon the value of I_{do} at high frequency.

Fig. 5.40 shows the distribution of current and voltage in one half of the d.c. choke and its decay circuit. R_7 is the resistance in series with D_7, i_d is the current which flows through the conducting bridge S C R into the load, v_{Ld} is the voltage across the choke causing the choke current i_p to decay from $\hat{I}$ to I_{do}, and i_q is the current in diode D_7. It is assumed that $\hat{I}$ is little greater than I_{do} and that the mean and r.m.s. values of i_p may be taken as I_{do}. The forward voltage drop, V_f, of diode D_7 is assumed constant.

Whatever the value of I_{do} the decrease in stored energy, ΔE_{Ld}, of the choke when its current falls from $\hat{I}$ to I_{do} is constant, depending only upon the supply voltages and the size of the commutating capacitor. This energy decrease is given by

$$\Delta E_{Ld} \triangleq \int_{0}^{\frac{T}{6}} v_{Ld}\, i_p\, dt \qquad (5.101)$$

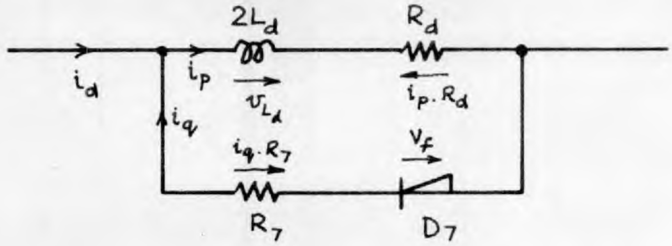


Fig. 5.40 : Distribution of currents and voltages around loop formed by one half of the d.c. choke and diode D7 during decay of current in the choke.

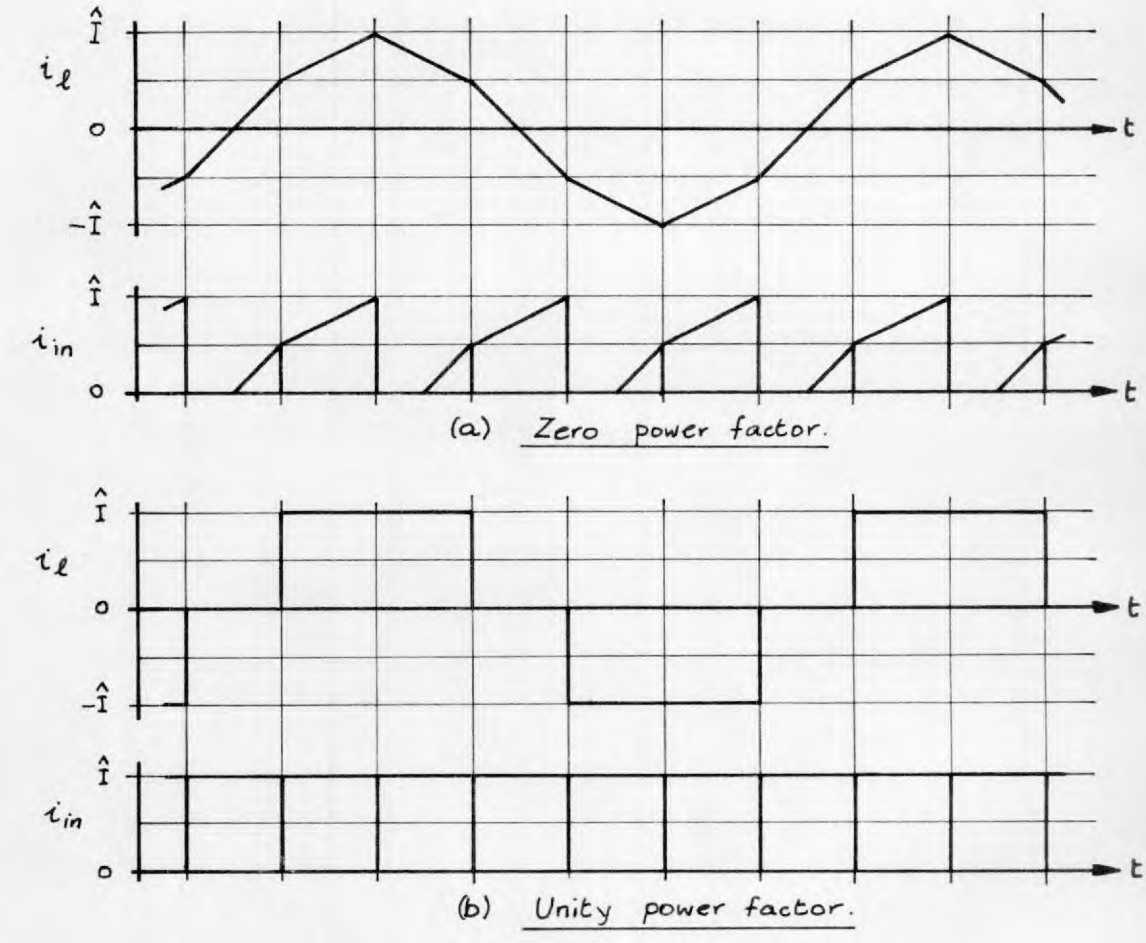


Fig. 5.41 : Corresponding waveforms of i_ℓ and i_{in} for zero and unity power factor loads.

When no load current flows i_q is equal to i_p and the no-load value, I_{do1}, of I_{do} may be found from equations (5.97) or (5.98). In this case ΔE_{Ld} is equal to the energy dissipated in the decay circuit

$$\text{i.e.}\quad \Delta E_{Ld} = \frac{T}{6}\left(I_{do1}^{2}\left[R_d + R_7\right] + I_{do1} V_f\right) \qquad (5.102)$$

When load current flows i_q is equal to $(i_p - i_d)$ and v_{Ld} is given by

$$v_{Ld} = i_p(R_d + R_7) - i_d R_7 + V_f \qquad (5.103)$$

$$\text{Then}\quad \Delta E_{Ld} = \int_0^{\frac{T}{6}} v_{Ld}\, i_p \, dt$$

$$= \int_0^{\frac{T}{6}} \left\{ i_p^{2}(R_d + R_7) - i_p\, i_d\, R_7 + V_f\, i_p \right\} dt$$

$$= \frac{T}{6}\left(I_{do2}^{2}\left[R_d + R_7\right] - I_{do2}\, I_d\, R_7 + V_f\, I_{do2}\right) \qquad (5.104)$$

where I_d is the mean value of i_d, and I_{do2} is the new mean and r.m.s. value of i_p.

Since ΔE_{Ld} isthe same in each case

$$I_{do2}^{2}(R_d + R_7) - I_{do2}(I_d R_7 - V_f) - I_{do1}^{2}(R_d + R_7) + I_{do1} V_f = 0$$

i.e.

$$I_{do2}^{\ 2} - I_{do2}\left[\frac{I_d R_7 - V_f}{R_d + R_7}\right] - \left[I_{dol}^{\ 2} + \frac{I_{dol}\ V_f}{R_d + R_7}\right] = 0$$

Solving for I_{do2} we obtain

$$I_{do2} = \frac{I_d R_7 - V_f}{2(R_d + R_7)} \pm \sqrt{\left[\frac{I_d R_7 - V_f}{2(R_d + R_7)}\right]^2 + I_{dol}^{\ 2} + \frac{I_{dol}\ V_f}{R_d + R_7}}$$

Taking the positive sign since the negative sign is meaningless

$$I_{do2} = \frac{I_d R_7 - V_f}{2(R_d + R_7)} + I_{dol}\left\{1 + \frac{V_f}{I_{dol}(R_d + R_7)} + \left[\frac{I_d R_7 - V_f}{2I_{dol}(R_d + R_7)}\right]^2\right\}^{\frac{1}{2}}$$

On expanding,

$$I_{do2} \simeq \frac{I_d R_7 - V_f}{2(R_d + R_7)} + I_{dol}\left\{1 + \frac{V_f}{2I_{dol}(R_d + R_7)} + \tfrac{1}{2}\left[\frac{I_d R_7 - V_f}{2I_{dol}(R_d + R_7)}\right]^2 \cdots\right\}$$

neglecting higher order terms

i.e.

$$I_{do2} \simeq \frac{I_d R_7 - V_f}{2(R_d + R_7)} + I_{dol} + \frac{V_f}{2(R_d + R_7)} + \frac{1}{8\ I_{dol}}\left[\frac{I_d R_7 - V_f}{R_d + R_7}\right]^2 + \cdots$$

$$\underline{I_{do2} \simeq I_{dol} + \frac{I_d R_7}{2(R_d + R_7)}} \qquad (5.105)$$

Equation (5.105) shows that I_{do} does increase with load but that the rate of increase depends upon the relative magnitude of R_d and R_7. If the choke possessed no resistance, i.e. $R_d = 0$, I_{do} would increase approximately by $\frac{1}{8} I_d$. If R_7 were small compared with R_d, I_{do} would increase very little with load.

Choosing a particular value of R_7 to give minimum power losses is very difficult. If R_7 is made small, I_{do} can increase rapidly with frequency. This makes a larger commutating capacitor necessary and results in higher power losses. If, on the other hand, R_7 is made larger, the voltage drop across R_7 and the diode in series with it forces part of the decaying choke current to flow through the conducting bridge S C Rs and the reverse bridge diodes. This leads to a reduction in the effective value of R_7 and also increases the current flowing through the bridge S C Rs and diodes. To overcome this it would be necessary to insert some resistance in the d.c. lines of the reverse diode bridge but this leads to an increase in the I^2R losses due to the current flowing along these lines.

It is clear, therefore, that a general expression for the optimum value of R_7 cannot begiven. Each case should be treated on its own merits, making sure that the reduction of commutation losses following an increase in R_7 is not accompanied by a greater increase in I^2R losses in the reverse diode bridge d.c. lines.

5.8 Relationship between the Load and the Distribution of Inverter Current between the S C R and Reverse Diode Bridges.

When the inverter load is, or can be treated as, a simple R-L series circuit for each phase the exact current and voltage waveforms can be calculated for all parts of the circuit using the methods developed in sections 5.3.6 and 5.4. Such calculations, although straightforward, are laborious especially when a range of load conditions is required to be covered.

It was not found possible to derive a general formula which would be simple yet exact for determining the mean values of S C R and reverse diode bridge currents. By making some assumptions about the relative magnitude of V_d and V_ℓ and of I_{in} and I_ℓ, however, it is possible to obtain some useful approximate formulae which would also be valid in the case of an induction motor load on the inverter.

Fig. 5.41 shows the waveforms of load current i_ℓ and the corresponding waveforms of the S C R bridge input current i_{in} for zero and unity load power factors. The waveforms for zero load power factor are taken from Fig. 5.33 and the waveforms for unity power factor are the basic inverter waveforms. Both pairs of waveforms are drawn with the effects of commutation ignored. $\hat{I}$ is the peak value of the load and S C R currents in each case.

For zero power factor it may be shown that I_ℓ, the r.m.s. value of i_ℓ, is equal to $0.646\,\hat{I}$ whereas I_{in}, the mean value of i_{in}, is equal to $0.437\,\hat{I}$. Hence in this case,

$$I_{in} = \frac{0.437}{0.646} I_\ell$$

i.e.

$$\underline{I_{in} = 0.680 \; I_\ell}$$

For unity power factor I_ℓ is equal to $\sqrt{\frac{2}{3}}\,\hat{I}$, i.e. 0.816 $\hat{I}$, while I_{in} is equal to $\hat{I}$. Hence in this case

$$I_{in} = \frac{1}{0.816} I_\ell$$

i.e.

$$\underline{I_{in} = 1.23 \, I_\ell}$$

Now let us assume that between zero and unity power factors the ratio I_{in}/I_ℓ varies linearly with F, the power factor of the load. Then the value of I_{in} varies with I_ℓ and power factor F according to:-

$$\underline{I_{in} = (0.68 + 0.55 \, F) \, I_\ell} \tag{5.106}$$

It is seen from Fig. 5.37 that the r.m.s. value of load line to line voltage, V_ℓ, varies with the nature of the load but is always between 0.7 V_d and 0.8 V_d. Let us assume that V_ℓ has the typical value 0.75 V_d at all power factors.

Now the power supplied to the load is equal to the power taken from the main d.c. supply minus the losses in the inverter circuit (excluding the commutation losses which do not normally cause additional losses in the bridges).

i.e. $V_d I_d - P_{cx} \doteq \sqrt{3}\, V\ I\ F$

$$\therefore \quad I_d \doteq \frac{\sqrt{3}\, V_\ell I_\ell F}{1.33V} + \frac{P_{cx}}{V_d}$$

$$\text{i.e.} \quad \underline{\underline{I_d \doteq 1.3\, I_\ell\, F + \frac{P_{cx}}{V_d}}} \qquad (5.107)$$

Hence, since $I_{gen} \doteq I_{in} - I_d$

$$\underline{\underline{I_{gen} \doteq (0.68 - 0.75\, F)I_\ell \quad - \frac{P_{cx}}{V_d}}} \qquad (5.108)$$

Fig. 5.42 shows these relationships between I_{in}, I_d, I_{gen} and I_ℓ and F in graphical form with P_{cx} ignored. When F is nearly unity I_{gen} is shown to be zero, which cannot be quite true except when F = 1. This is because the typical value taken for V_ℓ in terms of V_d is not the value which V_ℓ would have at unity power factor. Strictly, I_d and I_{gen} should start to depart from the lines shown at a power factor of about 0.5 and curve away to reach 1.23 I_ℓ and zero respectively at unity power factor.

5.9 Predicted Current and Voltage Waveforms.

Fig. 5.43 shows a set of typical predicted current and voltage waveforms. Each will be briefly described in turn.

The current i_a in phase A of the load has been fully dealt with in section 5.3.6. This current flows through CR_1 or CR_4 and D_1 or D_4.

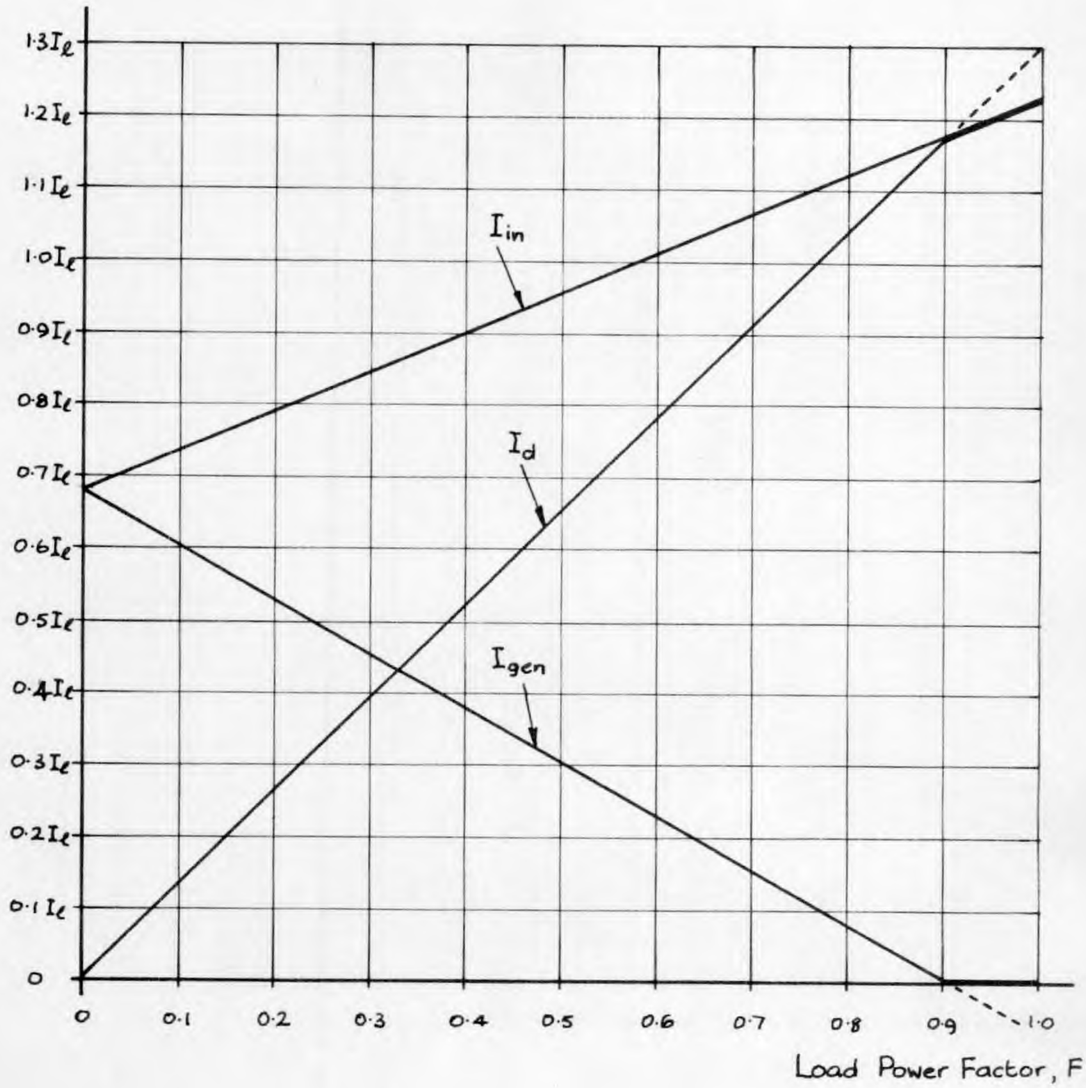


Fig. 5.42 : Approximate variation, in terms of load current I_ℓ, of I_{in}, I_{gen}, and I_d with load power factor.

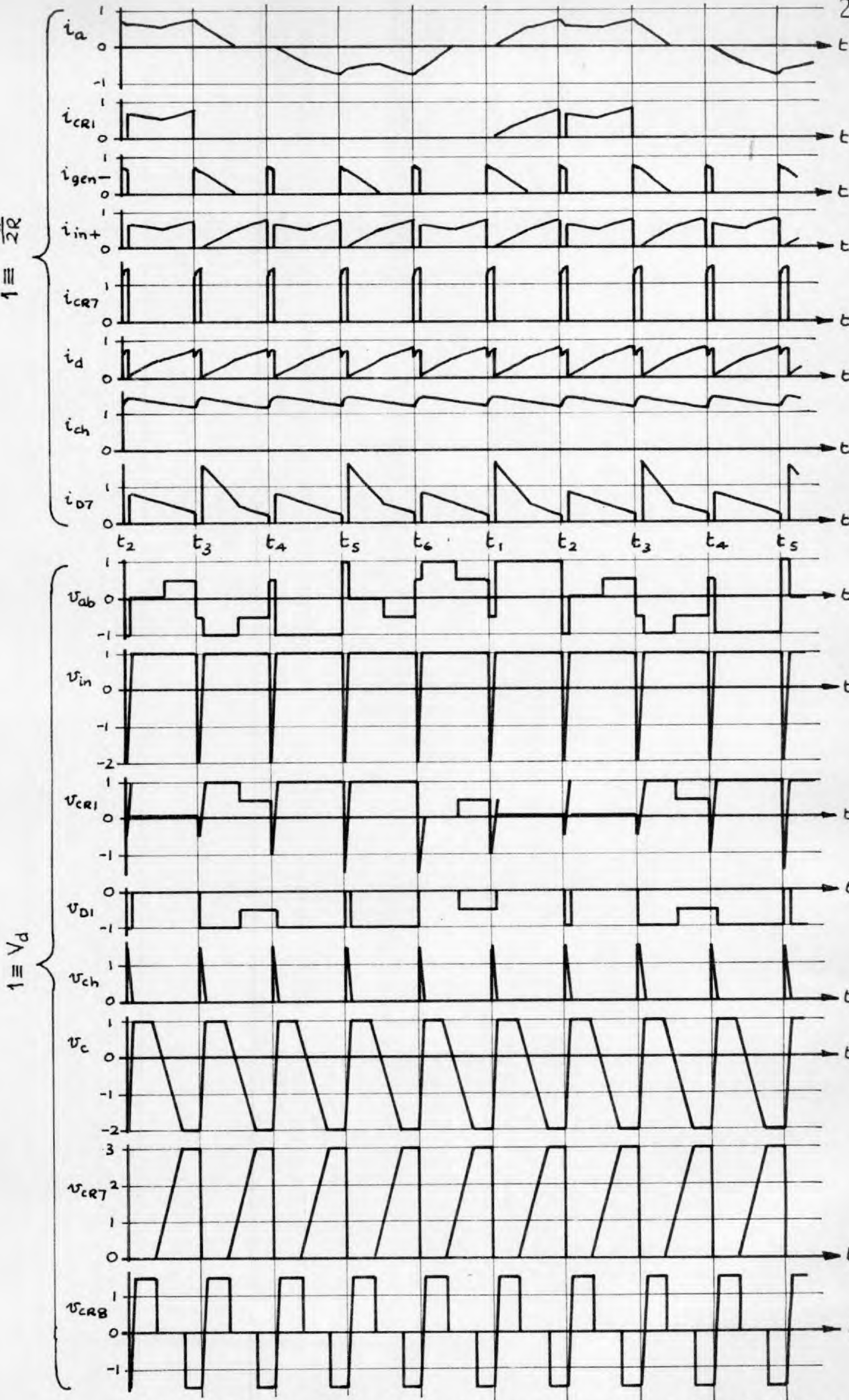


Fig. 5.43: Typical predicted waveforms for series R-L load.

The current i_{CR1} in CR_1 is zero for two thirds of a cycle since each S C R in the bridge conducts for only one third of a cycle. During the third of a cycle from t_1 to t_3 the current i_{CR1} is the same as i_a except during the commutation periods when CR_1 is off and no current flows.

The current i_{gen} flows in the reverse diode bridge during the commutation period and when the load current in each phase decays to zero. The current i_{gen} - shown in that which flows into the negative terminal of the main supply. A peak of current flows at each commutation period followed in alternate sixths of a cycle by the decay to zero of the current in a load phase.

i_{in+} is the current flowing into the common anode connection of the S C R bridge and therefore consists in form of the current i_{CR1} repeated in each third of a cycle.

i_{CR7} is the current flowing through CR_7 into the commutating capacitor at commutation. It consists of a pulse of current whose magnitude starts at I_{do} and rises to $\hat{I}$ and occurs six times per cycle.

i_d is the current taken from the main supply and is equal to $(i_{in+} + i_{CR7} - i_{gen+})$. During the commutation periods i_d is equal to $(i_{CR7} - i_{gen+})$ since no current flows in the S C R bridge, and in the remainder of each sixth of a cycle i_d varies in the same manner as i_a between t_1 and t_2.

i_{ch} is the current in one half of the d.c. choke and rises from I_{do} to $\hat{I}$ in each commutation period and decays back to I_{do} in the remainder of each sixth of a cycle. The waveform is shown for the case in which

i_{ch} is always greater than i_{in}.

i_{D7} is the current flowing in diode D_7 and is the difference between i_{ch} and i_{in+} except during the commutation periods when D_7 is reverse biased and hence i_{D7} is zero.

v_{ab} is the voltage between output lines A and B and has been fully dealt with in section 5.3.6.

v_{in} is the voltage between the common anode and common cathode connections of the S C R bridge. Since D_7 conducts in this case for the whole of each sixth of a cycle v_{in} is equal to the main d.c. supply voltage v_d except during commutation when v_{in} is equal to v_c, the voltage across the commutating capacitor.

v_{CR1} is the voltage across CR_1. During the commutation periods after conduction at t_2 and t_3 negative peaks of voltage of magnitude $\frac{1}{2}(V_{CR} - V_d)$ appear across CR_1. The other negative voltage peaks are of magnitude $\frac{1}{2}V_{CR}$ and $\frac{1}{2}(V_{CR} + V_d)$. Between t_1 and t_3 CR_1 conducts and hence v_{CR1} is zero. Between t_4 and t_6 CR_4 conducts and hence v_{CR1} is equal to v_{in}. Between t_3 and t_4 CR_2 and CR_3 conduct and hence v_{CR1} is equal to $-v_{ab}$. From t_6 to t_1 CR_5 and CR_4 conduct and hence v_{CR1} is equal to v_{ca} (which varies in this period as v_{ab} between t_2 and t_3).

v_{D1} is the voltage across diode D1. Except during commutation periods v_{D1} is equal to $- v_{CR1}$ since D_7 conducts until the end of each sixth of a cycle. During the commutation periods starting at t_5 and t_6 diode D_1 conducts and hence $v_{D1} = 0$. In the commutation periods beginning at t_2 and t_3 D_4 conducts and hence v_{D1} is equal to the main supply voltage V_d. In the other two commutation periods neither D_1

nor D_4 conduct and hence v_{D1} and v_{D4} are equal to $\frac{1}{2}$ V_d.

During commutation the difference between the main d.c. supply voltage and the commutating capacitor voltage is shared equally between the two halves of the d.c. choke. v_{ch} is the voltage across one half of the d.c. choke and therefore consists of a voltage peak which starts at $\frac{1}{2}(V_d + V_{CR})$ and falls to zero in each commutation period. During the remainder of each sixth of a cycle v_{ch} is equal to the voltage across D_7 or D_8 which conduct and hence v_{ch} is nearly zero.

v_c is the voltage across the commutating capacitor and rises from $-V_{CR}$ to $+V_d$ during each commutation period. Approximately half way through each sixth of a cycle the commutating capacitor is re-charged from the auxiliary supply and v_c falls from $+V_d$ back to $-V_{CR}$.

v_{CR7} is the voltage across CR_7 and is the difference between v_{in} and v_c. When the commutation capacitor is re-charged v_{CR7} rises from approximately zero to $(V_d + V_{CR})$.

v_{CR8} is the voltage across CR_8 and is equal to $(V_a + v_c)$ except during re-charging when CR_8 conducts and $v_{CR8} = 0$. Hence before re-charging v_{CR8} is $(V_a + V_d)$ and is $(-V_{CR} + V_a)$ for the remainder of each sixth of a cycle.

CHAPTER 6.

TESTS ON THE "D.C. COMMUTATED THREE PHASE INVERTER" WITH A SERIES R-L LOAD.

The inverter was tested with a series R-L load and with an induction motor load. The tests with the R-L load were carried out in order to check the validity of the theory developed in Chapter 5 while the tests with the induction motor load were for studying the overall performance of the speed control system. In this chapter attention will be concentrated upon commutation, current and voltage waveforms and harmonics. The efficiency of the inverter and the ratings of the components of the circuit are left for consideration in Chapter 7 which is devoted to the tests with an induction motor load.

6.1 Typical Current and Voltage Waveforms.

In Fig. 6.1 a set of current and voltage waveforms is shown. They are given at this point so that they may be compared with the predicted waveforms of Fig. 5.43. The waveforms have been traced from oscillograms and are not to a common scale. A load condition was chosen in which the currents in diodes D_7 and D_8 were still flowing at the end of each sixth of a cycle and the decay of load current through the diode bridge occupied approximately the same proportion of a sixth of a cycle as in the waveforms of Fig. 5.43.

The voltage waveforms are very similar to those predicted in Fig. 5.43, the only differences resulting from the ripple on the main supply

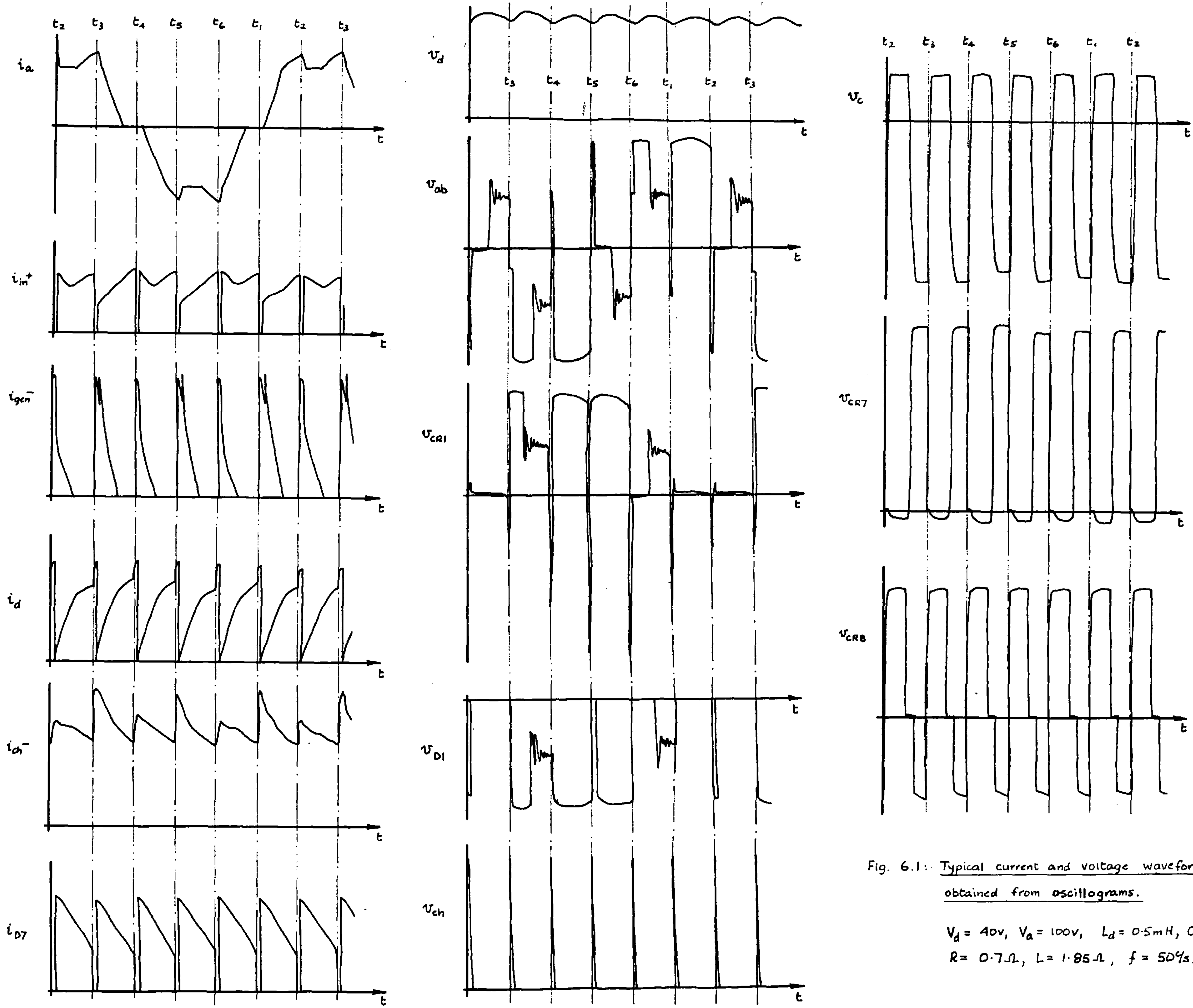


Fig. 6.1: Typical current and voltage waveforms obtained from oscillograms.

$V_d = 40\text{v}$, $V_a = 100\text{v}$, $L_d = 0{\cdot}5\,\text{mH}$, $C = 30\,\mu\text{F}$,
$R = 0{\cdot}7\,\Omega$, $L = 1{\cdot}85\,\Omega$, $f = 50\text{c/s}$.

voltage, v_d, and the oscillations between the small capacitors connected across each S C R for voltage surge protection and the inductance of the phase whose current has decayed to zero. The main supply voltage ripple is caused by the surge of current taken from the supply at commutation followed by a sudden drop in the supply current as the current in a load phase rises from zero.

The waveforms of the load current i_a and supply current i_d are as predicted. The other current waveforms are seen to differ from prediction and this is due to the decay of current in diodes D_7 and D_8 after commutation. In the theory it was assumed that D_7 and D_8 possess constant voltage drops while conducting and that there was no resistance in series with them. In fact, the voltage drop of these diodes, whilst not increasing linearly with current, does rise with current and in series with each diode was connected a small resistance for current monitoring.

Since the two halves of the d.c. choke were tightly coupled magnetically the induced voltages in each half had to be identical and hence the instantaneous diode currents had to be identical. This is why the diode current waveform, i_{D7}, is almost the same in each sixth of a cycle and not as predicted. However, the balance between choke current, diode current, and inverter input current had still to be maintained. Because of the tight coupling the current in one half could change instantaneously, provided that it was balanced by an equal and opposite change in the other half. Consequently the choke current is seen to rise to a greater value in one sixth of a cycle than in the next and the peaks of the choke current should then be $\hat{I} \pm \frac{1}{2} I_{L1}$.

If the current in D_7 and D_8 is high enough, the voltage across each half of the d.c. choke can become greater than the sum of the forward voltage drops of a conducting S C R and the diode connected to it. When this occurs the choke current can also decay through such a path, e.g. through CR_1 and D_1 when CR_1 is conducting. This is seen to occur in the waveforms of the inverter input current i_{in} and the diode bridge current i_{gen}. These waveforms consist of those predicted in Fig. 5.33 with a decaying pulse of current superimposed after commutation in each sixth of a cycle. The additional pulse only persists until the voltage drop across D_7 or D_8 and its series resistance falls below the sum of the voltage drops of an S C R and a diode.

Some small fluctuations in the waveforms from one cycle to the next were observed. These were caused by variations in the firing points of the bridge S C Rs at the end of commutation. The fluctuations were most evident in the value of S C R voltage after commutation and the value, I_{L1}, of load current at the end of commutation.

6.2. Commutation.

The auxiliary circuit provided to effect commutation in the inverter is essentially that used in the d.c. switch. The commutation theory was checked in the same way as in the d.c. switch and the results are given below.

6.2.1. Definition of Symbols used for the Commutation Process.

Fig. 6.2 shows the theoretical waveforms of v_c, i_c, v_{CR1} during the commutation period when CR_1 is turned off. At the instant t_3 of triggering CR_3 and CR_7 the capacitor voltage v_c starts to rise from $-V_{CR}$ towards $+ V_d$, following part of a sinewave of angular frequency ω . The time taken to reach $+ V_d$ is $\frac{\phi}{\omega}$. Meanwhile the capacitor current i_c rises from its initial value I_{do} to a peak value $\hat{I}$, again following part of a sinewave. v_{CR1} rises from $- \frac{1}{2}(V_{CR} - V_d)$ to $+ V_d$ in the time $\frac{\phi}{\omega}$ but the time taken for v_{CR1} to reach zero is δ and it is vitally important that δ should be greater than the S C R turn-off time for reliable commutation.

The time $\dfrac{C(V_{CR} - V_d)}{I_{do}}$ is the approximate value of δ given in equation (5.5) and is seen to be the time which v_c would take to charge from $- V_{CR}$ to $- V_d$ if the charging current were to remain at the initial value I_{do}. It can be seen that this approximation will always give an optimistic value of δ i.e. one which is greater than that obtained in practice.

6.2.2. Variation of δ with Load Power Factor.

Some tests were carried out to find if δ was affected by the load power factor. These tests were carried out at a low frequency and in each case the supply voltage, load resistance, and hence the value of I_{do} were kept constant while the load inductance was varied. The tests were carried out for several combinations of commutating capacitance C and I_{do} and the results of three of these tests are shown in Fig. 6.3.

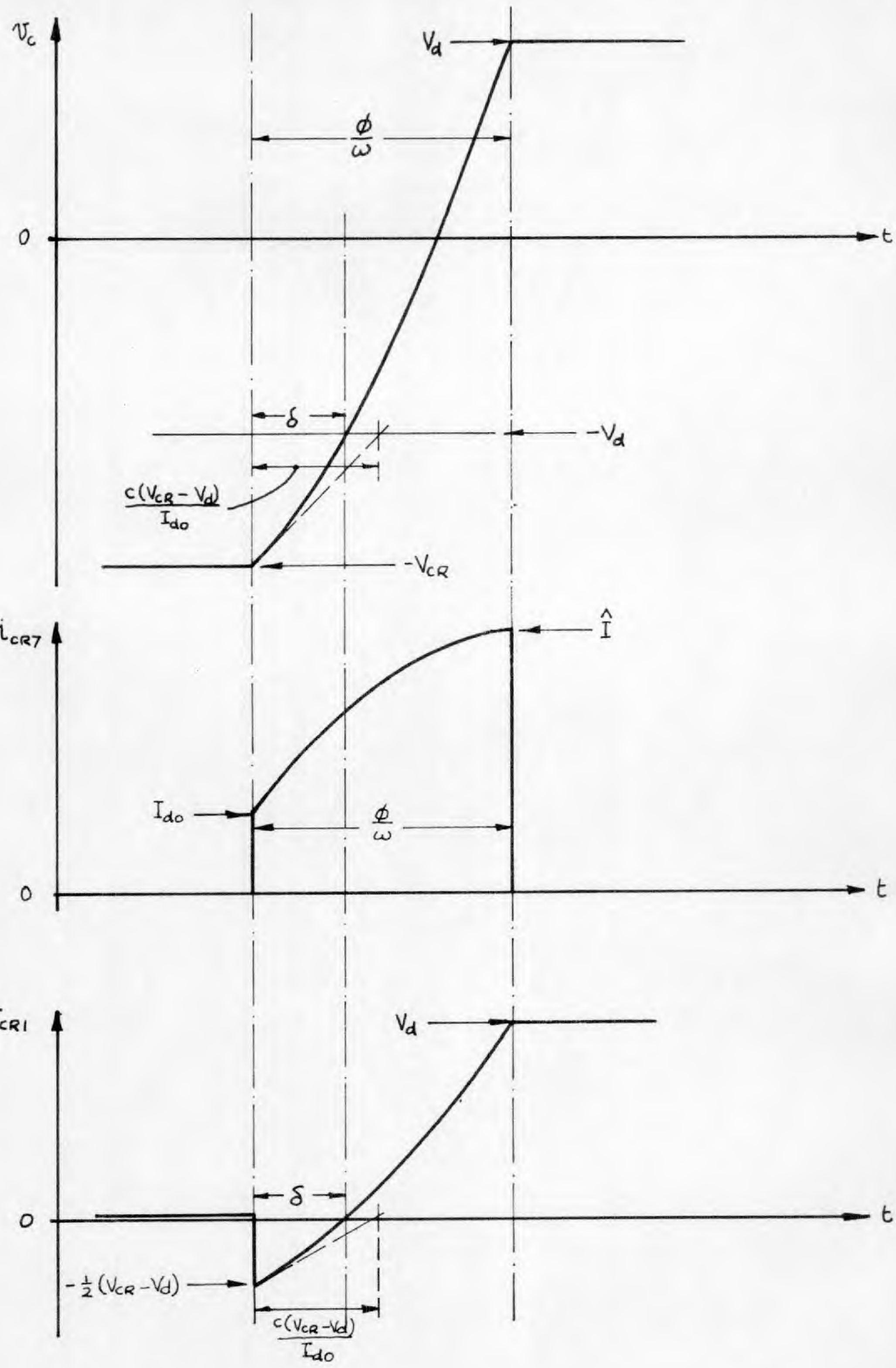


Fig. 6.2 : Waveforms of v_c, i_{CR7}, v_{CR1} during turn-off of CR1.

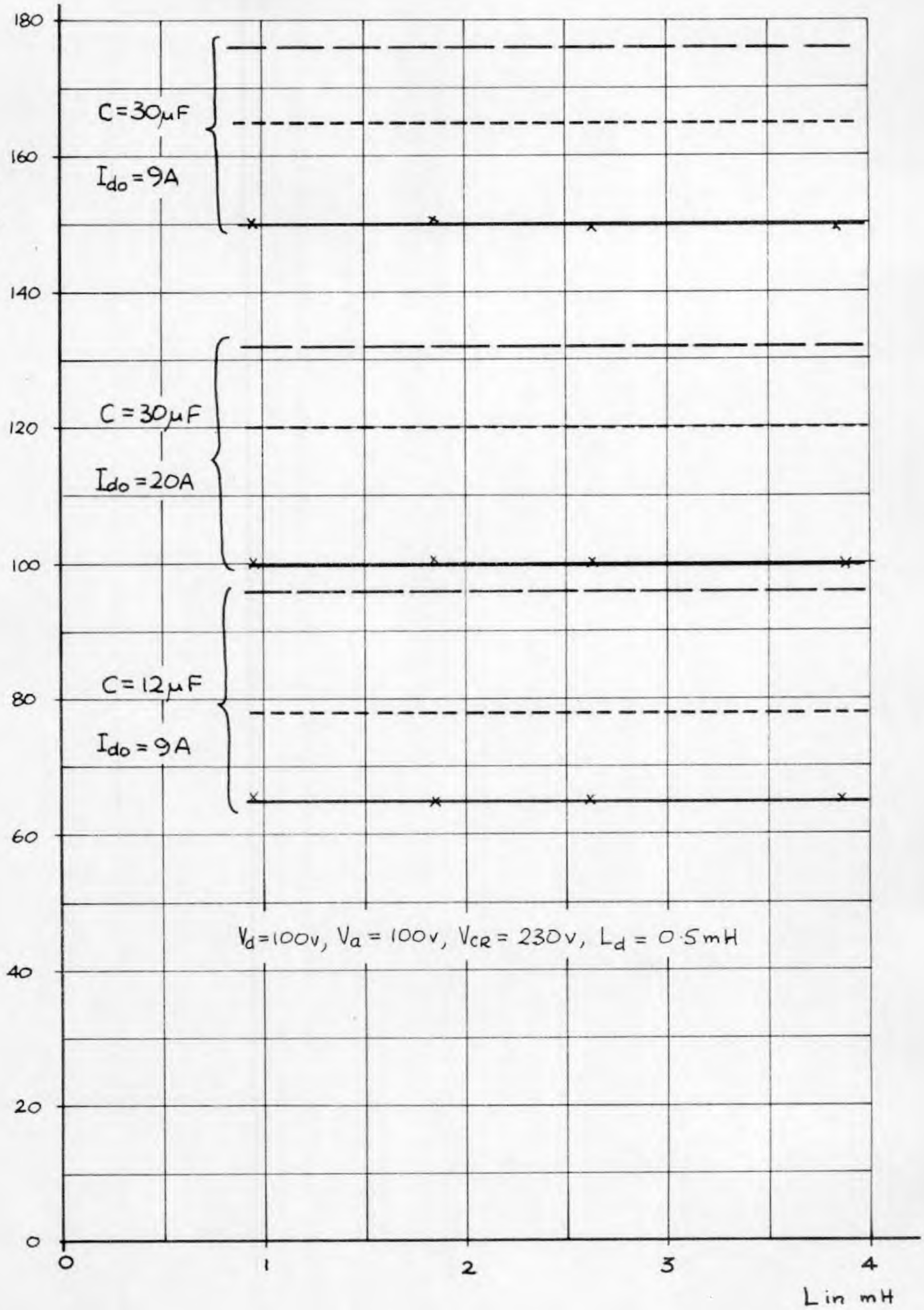


Fig. 6.3 : Variation of δ with load inductance.

——— Measured values

— — Calculated values

- - - - Values calculated from "corrected V_{CR}"

It is seen that in each case the measured value of δ is somewhat lower than that predicted. There are several reasons for this. The first is that all the rectifier forward voltage drops and lead resistance drops operate against effective commutation by making the effective value of V_{CR} lower and V_d higher so that $(V_{CR} - V_d)$ becomes smaller. The rectifier drops account for an error of about 4% under the condition of the test since the effective value of V_{CR} would be about 2.5 V low and the effective value of V_d about 2.5 V high (two rectifiers in series in each case).

The second cause of the discrepancy is the stray inductance of all the loops of the circuit where current transfer takes place during commutation. The effect of this inductance is to delay the fall of current in the conducting bridge S C Rs. after the commutating capacitor has begun to discharge so that when the S C Rs eventually become reverse-biased the commutating capacitor has already lost some of its charge. The exact result of this phenomenon is difficult to predict but the delay in reducing the S C R current to zero is clearly proportional to the inductance of the circuit and the current being commutated and inversely proportional to the voltage which forces the current to transfer from the S C R to another path. In the tests discussed here the reduction in δ from this cause probably amounted to no more than four or five microseconds at the highest currents commutated.

A further reason for the discrepancy is the reverse recovery current which flows in an S C R when it is turned off. The magnitude and duration of this current depend on the current flowing in the S C R immediately before turn-off and its rate of reduction to zero. This reverse current must flow in the commutating capacitor in addition to the current from the d.c. chokes and thus charges the capacitor more rapidly in the first few microseconds. Until the reverse current ceases to flow the S C Rs do not become reverse-biased and δ can therefore be reduced significantly.

The last, but probably the most significant, reason for the discrepancy has been allowed for in Fig. 6.3 in the lines showing "Corrected values" of δ. During the tests a $1\mu F$ capacitor was connected across each S C R in the bridge to suppress some troublesome voltage transients. At commutation the voltage across the bridge input terminals is reduced suddenly from $+V_d$ to some negative voltage by the action of the commutating capacitor. Some transfer of charge therefore occurs between the commutating capacitor and the network of $1\mu F$ capacitors. This transfer of charge can be allowed for by assuming that the effective value of the bridge capacitance is $1.5\mu F$ (made up of three parallel pairs of $1\mu F$ capacitors in series) and that the effective value of commutating capacitance then becomes $(C + 1.5\mu F)$, the initial voltage across this effective capacitor being $-V_{C'R}$ where $V_{C'R}$ is given by

$$\underline{V_{C'R} = \frac{C\,V_{CR} - 1.5\mu F \times V_d}{C + 1.5\mu F}} \qquad (6.1)$$

It is seen in Fig. 6.3 that the accuracy of prediction is much improved when this allowance is made.

The important conclusion to be drawn from these tests, however, is that δ is independent of the load inductance and hence the load power factor, as predicted.

6.2.3. Variation of δ with I_{do}.

To measure the variation of δ with I_{do} the circuit was again operated at a low frequency with the main and auxiliary supply voltages and the load inductance kept constant. I_{do} was varied by changing the load resistance and δ and I_{do} were measured on an oscilloscope for each value of load resistance. Measurements were taken for several values of the commutating capacitance and the results of two of the tests are presented in Fig. 6.4.

Once more it is seen that the calculated values of δ are greater than the measured values but that the correction applied to the calculated values considerably improves the accuracy of prediction. The form of the measured variation of δ with I_{do}, however, accords very favourably with that predicted. The values of δ calculated from the approximate expression of equation (5.5) are seen to be grossly inaccurate at low currents (where $\hat{I}$ is much greater than I_{do}) but at the higher values of I_{do} (where $\hat{I}$ becomes more nearly equal to I_{do}) the approximate expression is seen to give useful predictions. δ, as predicted, therefore varies inversely with I_{do}.

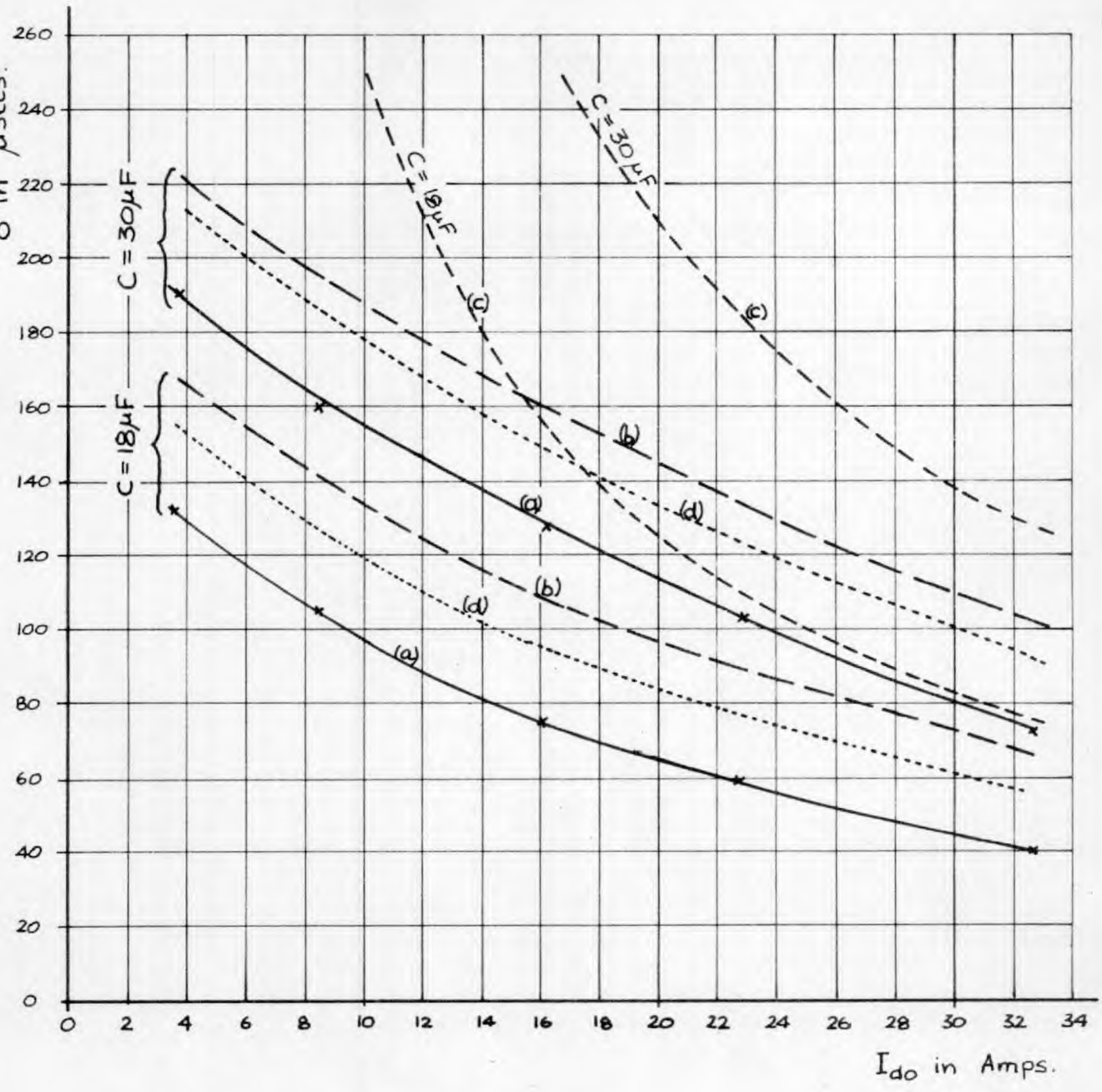


Fig. 6.4: Variation of δ with I_{do}

$V_d = 80v$, $V_a = 100v$, $V_{CR} = 220v$, $C = 18\mu F$ and $30\mu F$, $L_d = 0{\cdot}5mH$

(a) Experimentally obtained values.

(b) Calculated values.

(c) Values calculated from approximate expression for δ.

(d) Calculated values, corrected for effect of R-C filter connected across each main SCR.

6.2.4. Variation of δ with C and V_{CR}.

Some tests were carried out to find how δ varied with C and V_{CR}, the two main commutation parameters. The circuit was operated at low frequency with V_d and I_{do} kept constant and δ was measured on an oscilloscope for various combinations of C and V_{CR}, V_{CR} also being measured on an oscilloscope. Fig. 6.5 shows the measured and predicted variations of δ with C for two values of V_{CR}, the predicted values being corrected for the effective bridge capacitance.

It is seen that δ does not increase quite proportionally with C, the ratio $\frac{\delta}{C}$ diminishing as C is increased. This is because an increase in C causes an increase in $\hat{I}$ and hence an increase in the mean current charging C from $- V_{CR}$ to $- V_d$. For the same reason an increase of $(V_{CR} - V_d)$ from 140 V to 220 V does not cause a proportional increase in δ. However, both sets of measured values compare favourably with the predicted curves within the limits enumerated in section 6.2.2 and it may therefore be concluded that the theoretical expressions for δ are valid.

6.2.5. Variation of I_{do} and δ with Frequency.

In section 5.7.4 it was shown that at high inverter output frequencies I_{do} could become much greater than its low frequency value and largely independent of load current. In consequence δ would fall as the frequency is increased. It was in fact predicted that I_{do} would become approximately proportional to the square root of the inverter output

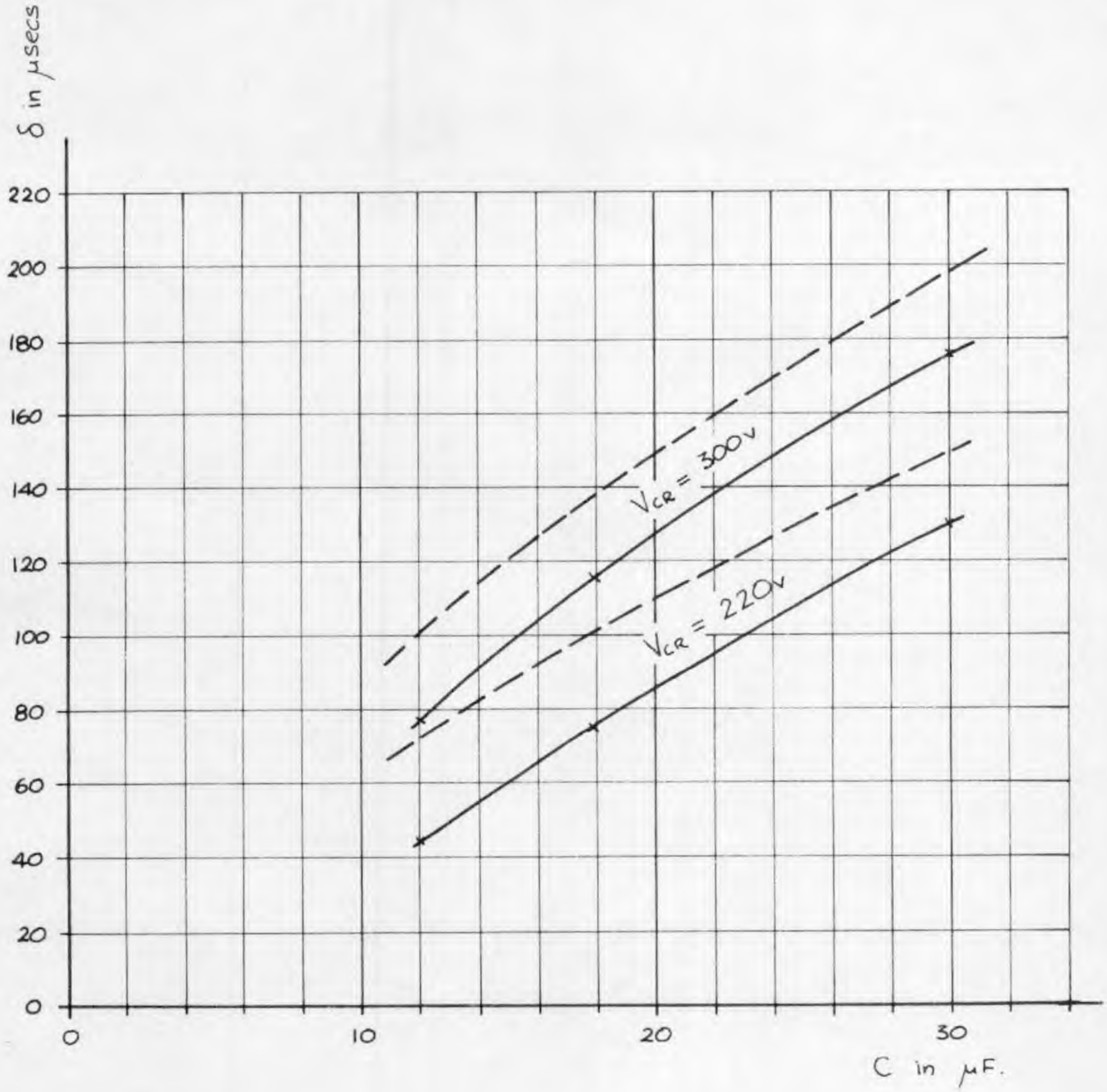


Fig. 6.5 : <u>Variation of δ with C and V_{CR}.</u>

$V_d = 80v$, $L_d = 0.5$ mH, $I_{do} = 16.6$ A, V_{CR} as shown

——— Measured values

- - - - "Corrected" calculated values

frequency. It was also predicted that by increasing the effective resistance of each half of the d.c. choke the rate of increase of I_{do} with frequency could be reduced.

To test the validity of this theory the circuit was operated over a range of frequencies with all circuit parameters and supply voltages kept constant. At each frequency the values of I_{do}, $\hat{I}$ and δ were measured on an oscilloscope. A resistance of $0.1\,\Omega$ was then added in series with each half of the d.c. choke and the measurements repeated.

In Fig. 6.6 the two sets of results are plotted. It is seen that with no added resistance I_{do} starts to rise above its low frequency value at about 12 $^c/s$ causing a corresponding increase in $\hat{I}$ and reduction in δ. With $0.1\,\Omega$ resistance added, however, the value of I_{do} actually falls at first with the peak load current as the frequency is increased and does not start to rise until a frequency of 32 $^c/s$. is reached. Thereafter I_{do} increases much less rapidly than in the first case which had no added resistance.

The values of I_{do} and δ calculated from equations (5.98) and (5.100) are also shown for comparison with the measured values and for verification of the theory. The calculations are based on a resistance of $0.032\,\Omega$ for each half of the d.c. choke, a mean resistance of $0.014\,\Omega$ for the leads to diodes D_7 and D_8, and an effective resistance of $0.019\,\Omega$ for diodes D_7 and D_8. These values were measured by the ammeter-voltmeter method. The effective resistance in the choke current decay circuit was then $0.065\,\Omega$ in the first case and $0.165\,\Omega$ in the second.

The calculated values of I_{do} and δ are seen in Fig. 6.6 to vary

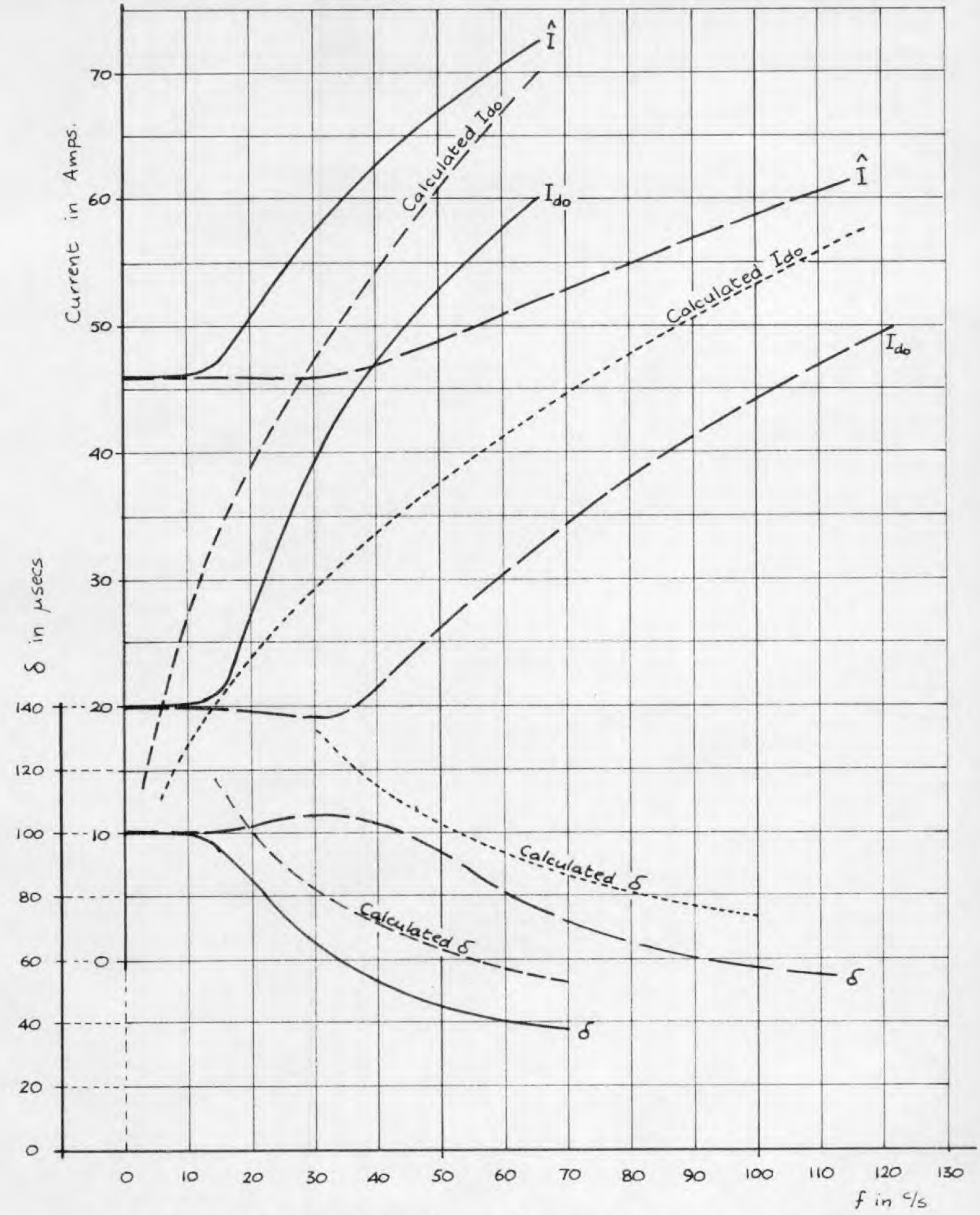


Fig. 6.6: Variation of I_{do}, $\hat{I}$ and δ with inverter output frequency, f.

$V_d = 100v$, $V_a = 100v$, $V_{cR} = 230v$, $L_d = 0.5\,mH$, $C = 30\mu F$, $R = 2.0\,\Omega$, $L = 1.85\,mH$

—— and – – – no added choke resistance ($R_d' = 0.065\,\Omega$)

— — and ······ 0.1Ω added in series with each half of d.c. choke ($R_d' = 0.165\,\Omega$)

with frequency in much the same manner as the measured values once the values of I_{do} have begun to rise above their low frequency value. Agreement between the measured and calculated values of δ is seen to be only alittle worse than in the tests discussed in the previous sections, showing that the approximate theory gives useful results. The calculated values of I_{do} lie approximately half way between the measured values of I_{do} and $\hat{I}$ at each frequency. This is to be expected since the calculated value of I_{do} really represents the r.m.s. value of the current in each half of the d.c. choke. Since this current rises quickly from I_{do} to $\hat{I}$ and then decays almost linearly back to I_{do} in each sixth of a cycle its r.m.s. value actually lies nearly half way between I_{do} and $\hat{I}$.

It may be concluded from these tests that at high frequencies I_{do} rises almost proportional to the square root of frequency and δ inversely proportional to the square root of frequency. The resistance of the d.c. choke is one of the main factors upon which depends the rate of increase of I_{do} with frequency and increasing the resistance has the predicted effect upon the rise of I_{do}.

6.2.6. Variation of I_{do} with Load Current at High Frequency.

Some tests were carried out to determine how far I_{do} was independent of load current at high inverter output frequencies. The tests were carried out at a high frequency and all supply voltages and circuit parameters were kept constant except for the load (and hence the main supply current) which was varied. The values of I_{do} for several values of supply current were measured and the measurements were repeated with several combinations of circuit parameters.

Fig. 6.7 shows how the values of I_{do} and $\hat{I}$ varied with I_d in one of these tests. The calculated variation of I_{do} with I_d is also shown and has been obtained by calculating the no-load value of I_{do} from equation (5.98) and using equation (5.105) afterwards.

It is seen that the measured I_{do} varies in a similar manner to its calculated variation and that once more the calculated values of I_{do} lie approximately half way between the measured values of I_{do} and $\hat{I}$. The graph therefore shows that the flow of load current has the effect of increasing the value of I_{do} and that the increase in I_{do} can be approximately predicted from equation (5.105).

6.2.7. Conclusions on Commutation.

In an inverter circuit the arrangement made for turning off the load current carrying S C Rs forms one of the most important features of the circuit. The commutation circuit must be reliable or the inverter will fail to function, each failure normally being accompanied by a large d.c. fault current.

The tests on the commutation circuit which have been described above have shown that the theory developed in section 5.3.4.1 and elaborated in section 5.7 is adequate for use in designing a suitable commutation circuit for the inverter circuit under discussion.

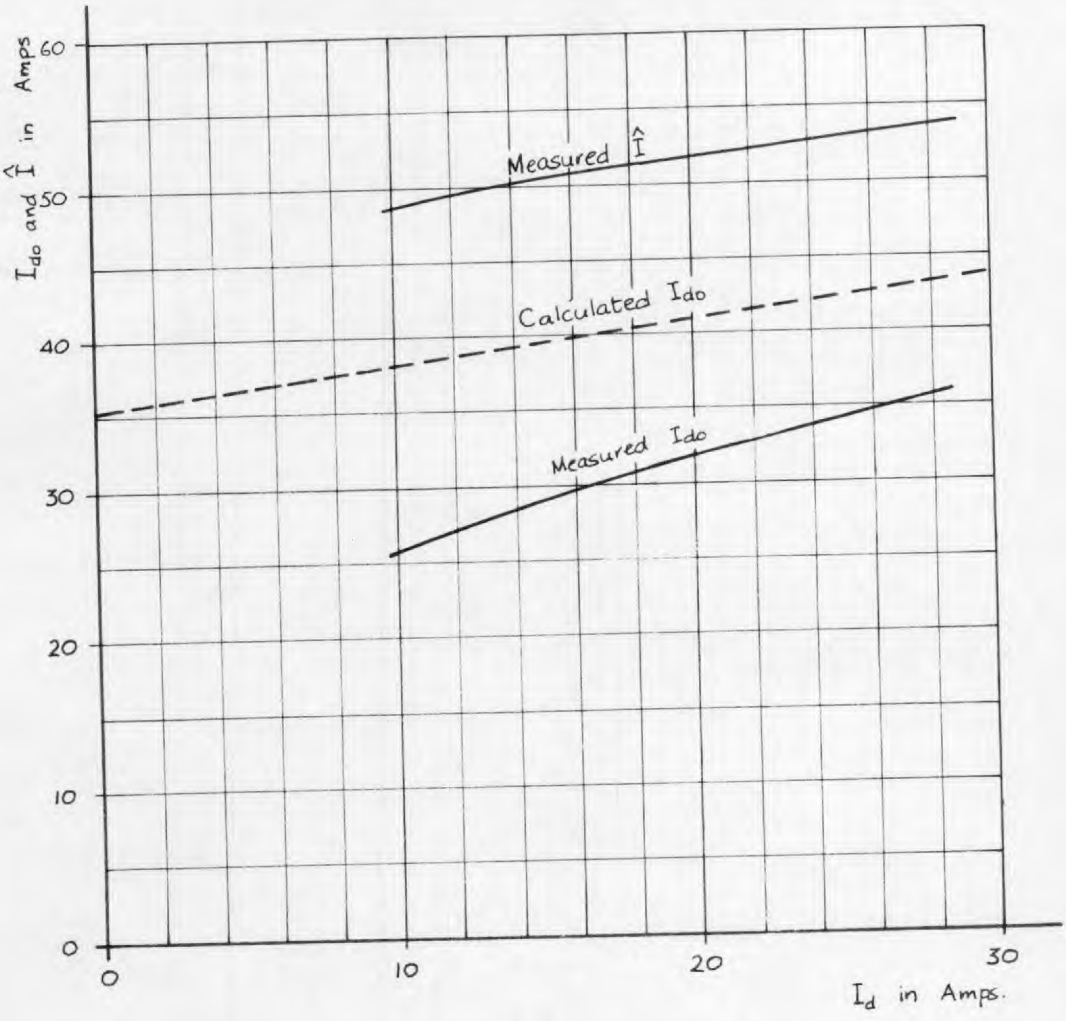


Fig. 6.7 : Typical variation of I_{do} with I_d at high inverter output frequency.

$V_d = 100v$, $V_a = 100v$, $V_{CR} = 230v$, $f = 40 c/s$

$C = 30 \mu F$, $L_d = 0.5 mH$, $L = 1.85 mH$.

$R_d = 0.06 \Omega$, $R_7 = 0.084 \Omega$, $R'_d = 0.16 \Omega$

The most important commutation circuit characteristics which must be taken into account are as follows:-

(a) the S C R reverse-bias time δ at turn-off is independent of the load power factor and this need not, therefore, be taken into account.

(b) δ varies in an inverse manner with the current I_{do} flowing in the d.c. choke prior to commutation. Hence it is essential that the highest load currents envisaged, even overload currents, should be taken into account,

(c) for a given value of I_{do}, δ is approximately proportional to the commutating capacitance C,

(d) δ is also approximately proportional to $(V_{CR} - V_d)$ where V_{CR} is the voltage on the commutating capacitor prior to commutation and V_d is the main supply voltage. Hence V_{CR} must be greater than V_d for commutation to be at all possible,

(e) when I_{do} is high, or the d.c. choke inductance is large, δ is approximately equal to $\frac{C(V_{CR} - V_d)}{I_{do}}$. This formula can be used with confidence to obtain values for C and V_{CR} at the first stage of designing the commutation circuit,

(f) when the inverter output frequency is increased a point is reached where I_{do} begins to rise independently of load current. Thereafter I_{do} becomes approximately proportional to the square root of frequency and δ falls accordingly. The frequency at which I_{do} starts to rise and the rate at which I_{do} rises depend upon the values of C and V_{CR} and the nature of the circuit forcing the d.c. choke current to decay between successive commutations. I_{do} becomes approximately proportional to $\sqrt{C}$

at a given frequency and δ in consequence becomes proportional to $\sqrt{C}$ at the same frequency.

(g) at high frequencies the value of I_{do} varies with the load current, but only to an extent determined by the relative magnitudes of the resistances, R_d, R_7 and R_8, concerned with the decay of current in the d.c. choke.

The results of the tests underline the necessity for keeping to a minimum the inductance distributed around the circuit and the capacitance used for limiting voltage surges. Some circuit inductance is necessary to reduce hole storage reverse recovery currents and to limit the rate of rise of current in each S C R at turn-on to a safe value. Protection against voltage surges, however, would be better carried out by some of the semiconductor devices now designed for this purpose.

6.3. Sample Calculations for R-L Load and Comparison with Measured Results.

6.3.1. Condition for the Calculation.

In this section the waveforms and mean values of voltage and current are found by calculation and compared with the corresponding measured results. A load and frequency were chosen so that diodes D_7 and D_8 conducted throughout each cycle except during the commutation periods.

The load and supply conditions were as follows :-

$V_d = 100\text{ V}$; $V_a = 100\text{ V}$; $V_{CR} = 230\text{ V}$

$L_d = 0.5\text{ mH}$; $C = 30\,\mu\text{F}$; $R'_d = 0.065\,\Omega$

$L = 3.85\text{ mH}$; $R = 2.3\,\Omega$; $f = 50\ ^c/\text{s}$.

6.3.2. Determination of I_{do}, $\hat{I}$, I_{LO}, I_{L1}, I_{L2}, T_1, T_2, T_3.

The condition of the circuit is such that I_{do} is higher than I_{LO}. I_{do} must therefore be calculated from the given data. From equation (5.98) a value I'_{do} can be obtained which is approximately half way between I and the true value of I_{do}.

$$\text{Thus}\quad I'_{do} \simeq \tfrac{1}{2}(V_d + V_{CR})\sqrt{\frac{6\,C\,f}{R'_d}}$$

$$\simeq \underline{\underline{61.5\text{ A}}}$$

From the definition of $\hat{I}$ (see equation (5.2))

$$\hat{I}^2 - I_{do}^2 = \frac{C(V_d + V_{CR})^2}{4\,L_d}$$

$$\text{i.e.}\quad (\hat{I} - I_{do})(\hat{I} + I_{do}) = 1635\ \text{A}^2$$

$$\text{Now}\quad \hat{I} + I_{do} \simeq 2I'_{do} = 123\text{ A}$$

$$\therefore\quad \hat{I} - I_{do} = \frac{1635}{123}$$

$$= 14.5\text{ A}$$

Hence $I_{do} \simeq I'_{do} - \frac{1}{8}(\hat{I} - I_{do})$

$$\simeq \underline{\underline{54\ A}}$$

Having calculated I_{do}, T_1 may now be found.

$$\omega = \sqrt{\frac{1}{4\ L_d C}}$$

$$= \underline{\underline{4.09 \times 10^3}}$$

$$\tan \phi = \frac{\omega\, C(V_d + V_{CR})}{I_{do}}$$

$$= \underline{\underline{0.75}}$$

$$\therefore \quad \phi = \underline{\underline{0.644}}$$

Then $T_1 = \frac{\phi}{\omega}$

$$= \underline{\underline{158\ \mu\ \text{Secs}}}$$

Take T_1 to be 160 μSecs.

I_{L0}, I_{L1}, I_{L2}, T_2, T_3 may now be found by the iterative process described in section 5.3.6.2. For this process the following values are required

$$\frac{V_d}{2R} = \frac{100}{2 \times 2.3} = \underline{\underline{21.75\ A}}$$

$$\frac{V_d}{3R} = \frac{100}{3 \times 2.3} = \underline{\underline{14.5\ A}}$$

$$\frac{2\,V_d}{3R} = \frac{200}{3 \times 2.3} = \underline{\underline{29.0\ A}}$$

First iteration.

I_{L0} must lie between $\frac{V_d}{3R}$ and $\frac{V_d}{2R}$. For the first iteration choose $I_{L0} = 18$ A.

$$\text{Then } I_{L1} = I_{L0} - (I_{L0} + \frac{V_d}{2R}) \cdot \frac{R\,T_1}{L}$$

$$= \underline{\underline{14.2\ A}}$$

$$\text{Then } I_{L2} = \frac{2V_d}{3R}\left(\frac{1}{1 + \frac{V_d}{3RI_{L1}}}\right)$$

$$= \underline{\underline{14.35\ A}}$$

$$\text{Also } T_2 = \frac{L}{R}\log_e\left(1 + \frac{3\,RI_{L1}}{V_d}\right)$$

$$= \underline{\underline{1.14\ \text{m Secs}}}$$

$$\text{Then } T_3 = \frac{1}{6f} - (T_1 + T_2)$$

$$= \underline{\underline{2.03\ \text{m Secs}}}$$

$$\text{Then } I_{L3} = \frac{V_d}{2R} - (\frac{V_d}{2R} - I_{L2})e^{-\frac{RT_3}{L}}$$

$$= \underline{\underline{19.54\ A}}$$

The value of I_{L3} at the end of the first iteration is not equal to the assumed value of I_{L0}. Hence the assumed value of I_{L0} was wrong and another value must be assumed for the second iteration.

Second and third iterations.

The results of the first, second and third iterations are summarised in Table 6.1 below. These iterations were carried out in exactly the same manner as the first. In the second iteration a value of I_{L0} was taken which was slightly smaller than the I_{L3} obtained from the first iteration. Because the new value of I_{L3} resulting was still larger than the I_{L0} taken for the second iteration a value of I_{L0} for the third iteration was chosen which was slightly greater than the preceding I_{L3}.

Value of ..	First Iteration	Second Iteration	Third Iteration
I_{L0}	18 A	19.5 A	19.66 A
I_{L1}	14.2 A	15.56 A	15.71 A
I_{L2}	14.35 A	15.00 A	15.07 A
T_2	1.14 mSecs	1.22 mSecs	1.229 mSecs
T_3	2.03 mSecs	1.953 mSecs	1.994 mSecs
I_{L3}	19.54 A	19.65 A	19.66 A

Table 6.1 Summary of results of first, second and third iterations.

After the third iteration the values of I_{L0} and I_{L3} are seen to be equal. Hence the correct value of I_{L0} is 19.66 A.

Then, to three significant figures, the other initial values are

I_{L0} = 19.7 A, I_{L1} = 15.7 A, I_{L2} = 15.1 A

T_1 = 0.16 mSecs, T_2 = 1.23 mSecs, T_3 = 1.94 mSecs.

6.3.3. Current Equations and Current and Voltage Waveforms.

Having obtained the initial values I_{L0}, I_{L1}, I_{L2} and the times T_1, T_2, T_3 the current equations can be found for each sixth of a cycle and the voltage and current waveforms constructed. The current equations and output voltage values will be given only for the sixth of a cycle between instant t_2 and t_3 since the equations for other sixths of a cycle can be obtained easily from them.

Period 1 (of duration T_1)

$$i_a = -i_b = -\frac{V_d}{2R} + \left(\frac{V_d}{2R} + I_{L0}\right)e^{-\frac{Rt}{L}} \quad \text{(from equation (5.1))}$$

$$= \underline{-21.7 + 41.4\, e^{-600\, t}\ \mathrm{A}} \quad \text{to 3 significant figures.}$$

$$\underline{i_c = 0}$$

$$\left.\begin{aligned} v_{ab} &= -V_d \\ v_{bc} &= \frac{V_d}{2} \\ v_{ca} &= \frac{V_d}{2} \end{aligned}\right\} \text{See section 5.3.5.}$$

Period 2 (of duration T_2)

$$i_a = \frac{V_d}{3R} + \left(I_{L1} - \frac{V_d}{3R}\right)e^{-\frac{Rt}{L}} \qquad \text{(from equation (5.14))}$$

$$= \underline{14.5 + 1.2\, e^{-600t}}$$

$$i_b = \frac{V_d}{3R} - (I_{L1} + \frac{V_d}{3R})e^{-\frac{Rt}{L}} \qquad \text{(from equation (5.16))}$$

$$= \underline{\underline{14.5 - 30.2\ e^{-600\ t}\ A}}$$

$$i_c = -\frac{2V_d}{3R}(1 - e^{-\frac{Rt}{L}}) \qquad \text{(from equation (5.18))}$$

$$= \underline{\underline{-\ 29\ (1 - e^{-600t})\ A}}$$

$$\left.\begin{aligned} v_{ab} &= 0 \\ v_{bc} &= V_d \\ v_{ca} &= -V_d \end{aligned}\right\} \text{ See section 5.3.5.}$$

<u>Period 3 (of duration t_3)</u>

$$i_a = -i_c = \frac{V_d}{2R} + (I_{L2} - \frac{V_d}{2R})e^{-\frac{Rt}{L}} \qquad \text{(from equation (5.32))}$$

$$= \underline{\underline{21.7 - 6.7e^{-600t}\ A}}$$

$$\underline{\underline{i_b = 0}}$$

$$\left.\begin{aligned} v_{ab} &= \frac{V_d}{2} \\ v_{bc} &= \frac{V_d}{2} \\ v_{ca} &= -V_d \end{aligned}\right\} \text{ See section 5.3.5}$$

In the sixth of a cycle between t_2 and t_3 i_a and v_{ab} are as given by the equations above. In the next sixth of a cycle i_a and v_{ab} are as given by the equations for $-i_b$ and $-v_{bc}$, in the next as for i_c and v_{ca}, next as for $-i_a$ and $-v_{ab}$, next as for i_b and v_{bc}, next as for $-i_c$ and $-v_{ca}$. Thus the complete load current and voltage waveforms can be drawn as in Figs. 6.8 and 6.9.

6.3.4. Mean and r.m.s. Values of Load and Supply Current and Voltage.

The r.m.s. value I_a of the current in phase A may be found by integration over half a cycle. Since in the half cycle starting at instant t_2 i_a is defined in turn by the equations given above for i_a, $-i_b$ and i_c. I_a may be found from

$$I_a = \sqrt{\frac{2}{T}\int_0^{\frac{T}{6}} (i_a^2 + i_b^2 + i_c^2)\,dt}$$

Then, using the current equations obtained in section 6.3.3,

$$\underline{\underline{I_a = 13.5\text{ A}}}$$

The r.m.s. value V_{ab} of the output line to line voltage v_{ab} may be found in a similar manner.

Hence

$$V_{ab} = \sqrt{\frac{2}{T}\int_0^{\frac{T}{6}} (v_{ab}^2 + v_{bc}^2 + v_{ca}^2)\,dt}$$

$= \underline{\underline{74.8\text{ V}}}$ using equations for v_{ab}, v_{ac}, v_{ca} derived in section 6.3.2.

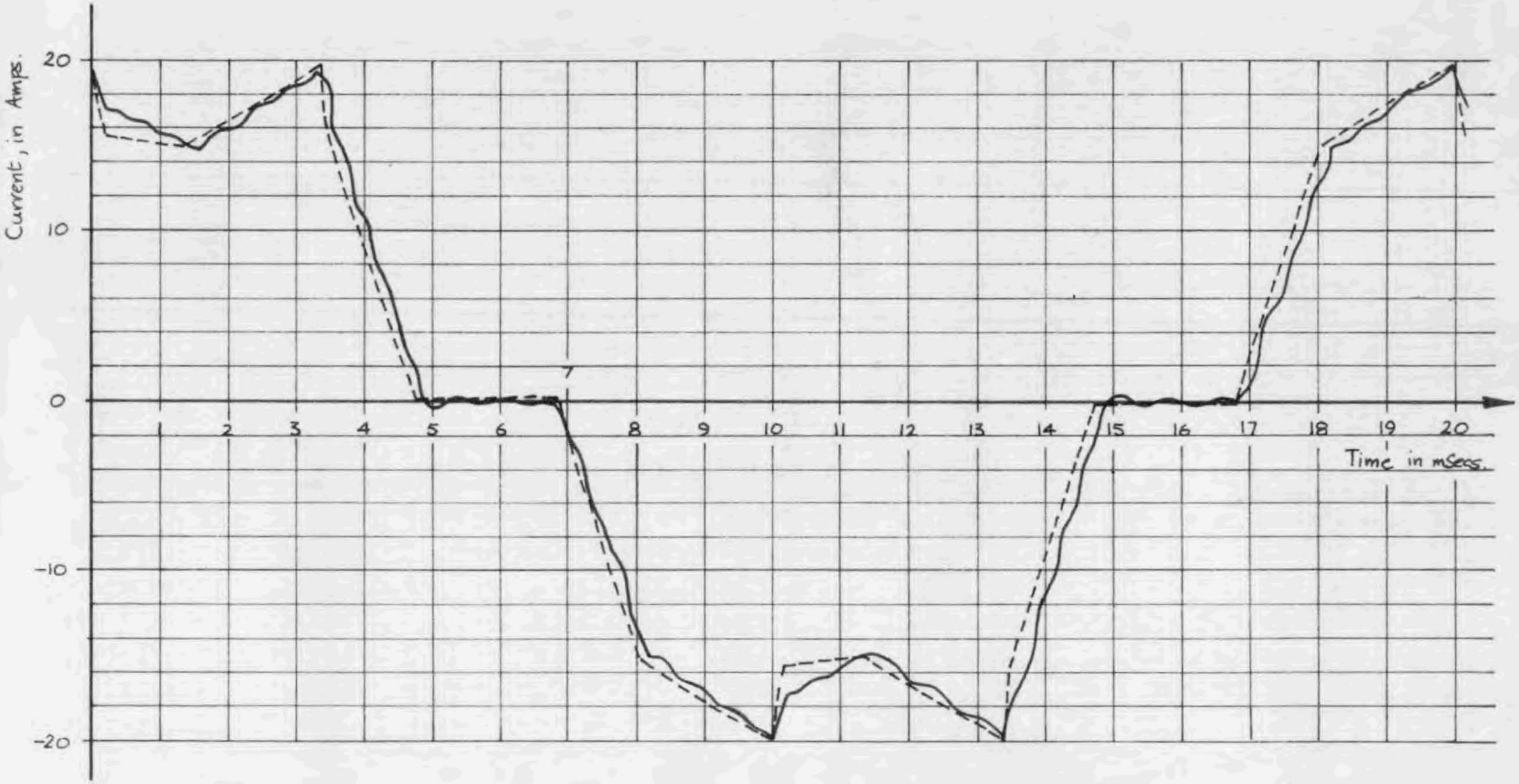


Fig. 6.8 : Measured (——) and predicted (- - -) inverter output phase currents waveforms.

(For circuit conditions see sample calculation in section 6.3.)

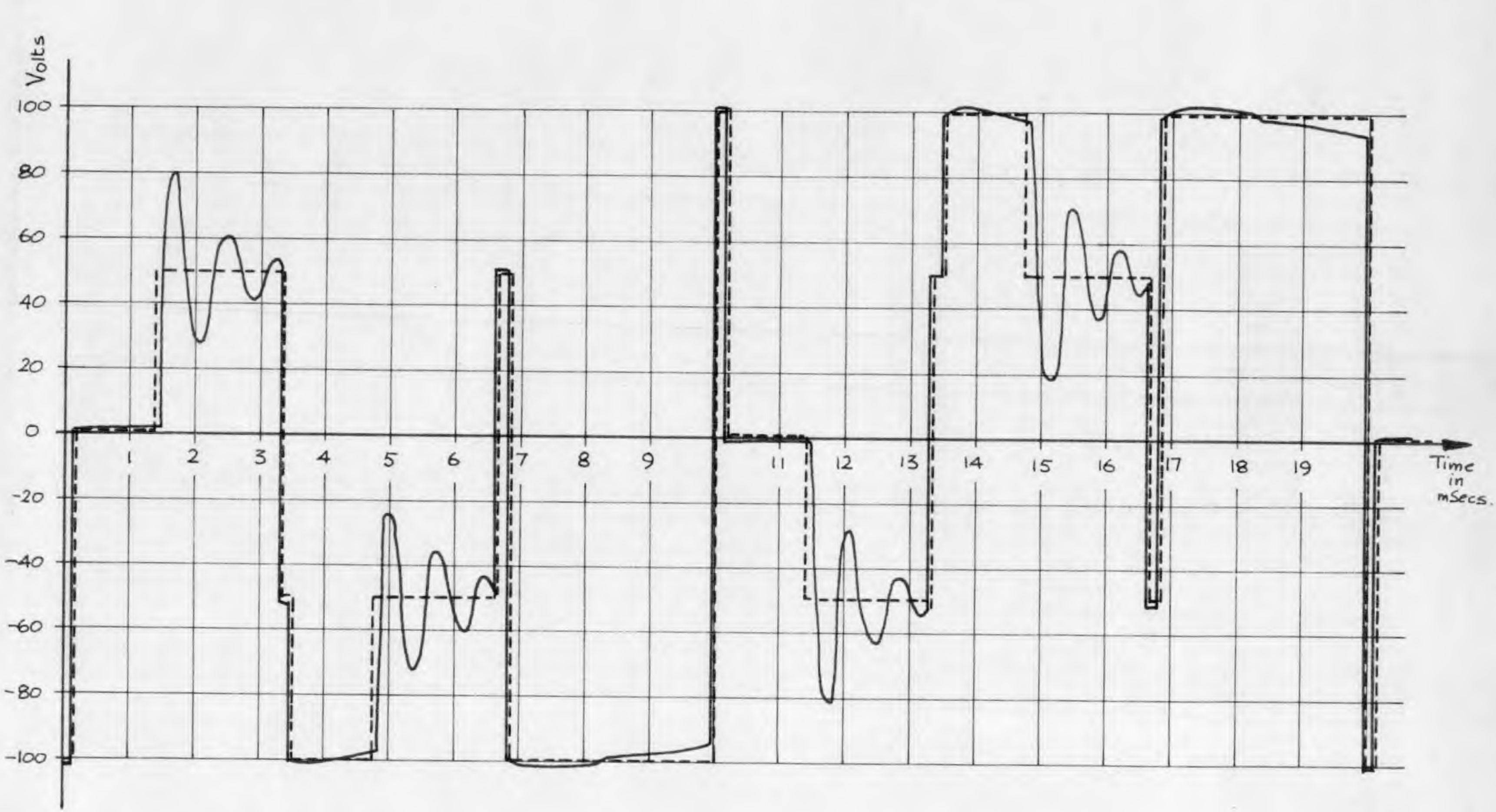


Fig. 6.9 : Measured (——) and predicted (- - -) inverter output line-to-line voltage waveforms.

(For circuit conditions see section 6.3 of text)

The waveform of i_d, the current taken from the main d.c. supply, consists mainly of the waveform for i_a between instants t_1 and t_2 repeated in every sixth of a cycle, (See Fig. 5.43), and is given by the equations ($- i_c$) derived in section 6.3.3. During the commutation period current is taken from the supply in charging the commutating capacitor from $- V_{CR}$ to $+ V_d$. The mean value of this contribution to the supply current is $6 C f (V_d + V_{CR})$ but is partially offset by the current returned to the supply through the reverse diode bridge. The latter current is given by the equation for i_a during period 1.

Hence the mean value I_d of the d.c. supply current is given by

$$I_d = \frac{6}{T} \int_0^{\frac{T}{6}} (-i_c)dt + 6\ C\ f(V_d + V_{CR}) - \frac{6}{T} \int_0^{T_1} i_a\ dt$$

Using the equations derived in section 6.3.3 for i_a and i_c

$$\underline{\underline{I_d = 15.6\ A}}$$

The current i_{gen} returned to the supply through the reverse diode bridge consists of a pulse during each commutation period given by the equation for i_a for period 1 followed in alternate sixths of a cycle by a decaying current given by the equation for $- i_b$ in period 2. The mean value I_{gen} of this current can therefore be found by integration over one third of a cycle.

$$\text{Hence } I_{gen} = \frac{3}{T}\left[2\int_{o}^{T_1} i_a dt + \int_{o\,(T_1)}^{T_2} (-i_b)dt\right]$$

$= \underline{\underline{2.20\text{ A}}}$ using equations for i_a and i_b from section 6.3.3.

The power, W_d, taken from the main d.c. supply may be found by multiplying together the d.c. supply voltage and the mean supply current

$$\text{i.e.}\quad W_d = V_d . I_d$$

$$= \underline{\underline{1560\text{ W}}}$$

The power W_L, consumed by the load may be found by adding the I^2R dissipations in the three load phases.

$$\text{i.e.}\quad W_L = 3 \times I_a^2 R$$

$$= \underline{\underline{1260\text{ W}}}$$

N.B. The difference between W_d and W_L is equal to the power taken from the main supply for charging the commutating capacitor from $- V_{CR}$ to $+ V_d$ six times per cycle, i.e. 297 W.

It should also be borne in mind that in each sixth of a cycle there are three equations to define each of the currents. Each of the current equations have their time zero at the beginning of the period for which they are valid. This simplifies the calculation of the integrals given above.

The output power factor, defined as $\text{P.F.} = \frac{W_L}{\sqrt{3}\, V_{ab} I_a}$, is found from the values of V_{ab} I_a and W_L calculated above.

Then $\underline{\underline{\text{P.F.} = 0.72}}$

6.3.5. Harmonic Content of Output Voltage and Current Waveforms.

In section 5.5 formulæ were devised for the several harmonic components of the output line-to-line voltage waveform. From the components of the total value of each voltage harmonic can be found and from these the current harmonics can be found. Table 6.2. shows the voltage components for the first five harmonics, the harmonic impedances per load phase, and the resulting current harmonics.

$\frac{1}{\sqrt{2}}\ a_n$ can be found from Table 5.1, putting $V_d = 100$ V.

To find $\frac{1}{\sqrt{2}}\ b_n$ and $\frac{1}{\sqrt{2}}\ c_n$ the value of u is required.

$$u = 2\pi f T_2 \text{ radians}$$

$$= 22.2^{\circ}$$

$\frac{1}{\sqrt{2}}\ b_n$ and $\frac{1}{\sqrt{2}}\ c_n$ can then be found from Fig. 5.36 or from Table 5.2 by putting $u = 22.2^{\circ}$.

Since the operating frequency is high enough for T_1 to form a significant part of each sixth of a cycle account must be taken of $\frac{1}{\sqrt{2}}\ b'_n$ and $\frac{1}{\sqrt{2}}\ c'_n$.

$$w = 2\pi f T_1 \text{ radians}$$

$$= 2.88^{\circ}$$

$\frac{1}{\sqrt{2}}\ b'_n$ and $\frac{1}{\sqrt{2}}\ c'_n$ can then be found from Table 5.3 by putting $w = 2.88^{\circ}$.

$V_n = \frac{1}{\sqrt{2}}\ d_n$ can then be found from equation (5.84).

The harmonic impedance Z_n per phase of the load is found from

$$Z_n = \sqrt{R^2 + (2\pi n f L)^2}$$

Then since V_n is the nth harmonic component of the load line-to-line voltage and Z_n is the nth harmonic impedance per phase of a star-connected load, the nth harmonic component I_n of the load current can be found from

$$I_n = \frac{V_n}{\sqrt{3}\, Z_n}$$

n	1	5	7	11	13
$\frac{1}{\sqrt{2}} a_n$	67.5 V	13.5 V	9.6 V	6.2 V	5.2 V
$\frac{1}{\sqrt{2}} b_n$	- 4.8 V	12.8 V	8.1 V	2.3 V	3.0 V
$\frac{1}{\sqrt{2}} c_n$	14.2 V	1.0 V	7.5 V	- 5.3 V	- 1.3 V
$\frac{1}{\sqrt{2}} b'_n$	- 5.8 V	5.8 V	- 5.7 V	5.6 V	- 5.5 V
$\frac{1}{\sqrt{2}} c'_n$	0.1 V	- 0.7 V	1.0 V	- 1.6 V	1.8 V
$V_n = \frac{1}{\sqrt{2}} d_n$	58.6 V	32.1 V	14.7 V	15.7 V	2.7 V
Z_n	2.59 Ω	6.48 Ω	8.77 Ω	13.51 Ω	15.90 Ω
I_n	13.1 A	2.86 A	0.97 A	0.67 A	0.098 A

Table 6.2 Calculations for harmonic content of load voltage and current waveforms.

$$\text{Power factor at fundamental frequency} = \frac{R}{Z_1}$$

$$= \underline{\underline{0.89}}$$

This is considerably higher than the total load power factor of 0.72 because of the harmonics which produce little power but add to the r.m.s. values of voltage and current.

6.3.6 Comparison between Measured and Predicted Results.

Measurements were taken from the inverter circuit of all the quantities predicted above. Mean and r.m.s. values were measured with meters, waveforms, time intervals and instantaneous current values on oscilloscopes, and harmonics were measured with a waveform analyser. The measured and predicted values are given together in the following table and discrepancies between values are expressed as percentages of the measured values.

Table 6.3: Comparison between measured results and results predicted in sample calculation

Quantity	Measured Value	Predicted Value	Discrepancy
I_{L0}	19.8 A	19.7 A	0.5%
I_{L1}	17.4 A	15.7 A	10%
I_{L2}	15.0 A	15.1 A	0.7%
T_1	0.16 mSec	0.16 mSec	0
T_2	1.35 mSec	1.23 mSec	8.9%
T_3	1.82 mSec	1.94 mSec	6.6%
I_d	17.2 A	15.6 A	9.3%
W_d	1720 W	1560 W	9.3%
I_{gen}	2.0 A	2.2 A	10%
I_ℓ	13.2 A	13.5 A	2.3%
V_ℓ	72.0 V	74.8 V	3.8%
W_L	1200 W	1260 W	5%
Total Power Factor	0.73	0.72	1.4%
V_1	60.0 V	58.6 V	2.3%
V_5	31.4 V	32.1 V	2.2%
V_7	15.7 V	14.7 V	6.4%
V_{11}	9.5 V	15.7 V	65%
V_{13}	6.2 V	2.7 V	56%
I_1	12.8 A	13.1 A	2.3%
I_5	2.71 A	2.86 A	5.5%
I_7	0.98 A	0.97 A	1%
I_{11}	0.39 A	0.67 A	72%
I_{13}	0.22 A	0.10 A	55%

Figs. 6.8 and 6.9 show how the measured inverter output current and voltage waveforms compare with those predicted. The oscillations visible on the measured waveforms are caused by interaction between the load inductance and the capacitors connected across the S C Rs in the inverter bridge.

From Table 6.2 and Figs. 6.8 and 6.9 it may be concluded that the theory developed in section 5.3 is capable of predicting the performance of the inverter to within 10%. The forward voltage drops of the rectifiers would account for about 2½% of the discrepancy between predicted and measured results and circuit resistance for a further 3%.

The measured value of I_{L1} is a mean value. In practice the instant in the cycle at which the bridge S C Rs resumed conduction after commutation fluctuated because of the pulsed control signal. Hence the value of I_{L1} given is higher than its lowest observed value which would compare better with the predicted value. For the same reason the measured value given for T_2 is higher than the predicted value.

The difference between W_d and W_L represents the power loss due to commutation and in the rectifier and circuit resistance. In the calculation only the commutation loss was taken into account and hence the measured power loss is larger than predicted.

There is seen to be a large discrepancy between the measured and predicted values for the 11th and 13th harmonics. The measured values are mean values since the reading of the wave analyser fluctuated. This again can be attributed mainly to the irregularity in the resumption of conduction by the S C Rs after commutation.

The voltage waveforms shown in Fig. 5.9 are line-to-line voltage waveforms and it is seen that oscillations take place where the voltage is nominally half of the supply voltage. This is when one of the output lines concerned is connected to the supply through an S C R and the other is effectively connected only to the S C R filter capacitors. The potential on the second line is therefore free to oscillate, interactions between the load inductance and the filter capacitance taking place where a steep voltage fall would theoretically have occurred. During commutation, however, the filter capacitor voltage changes so rapidly that the charging currents effectively swamp any load current which might flow. Hence no voltage oscillation is observed during commutation.

It is also seen that when the voltage between lines is nominally 100 V, i.e. when both lines are connected to the supply via S C Rs or diodes, the voltage waveform is in fact curved. This is because the main supply reservoir capacitor voltage fluctuates about its mean value as the current taken by the inverter varies during each sixth of a cycle. Hence the capacitor voltage falls during commutation periods and towards the end of each sixth of a cycle when the current drawn from it is greater than the mean current, and rises during the remainder of each sixth of a cycle.

6.4 Variation of Output Voltage Harmonics with Load.

Tests were carried out to determine how the inverter output voltage harmonic content changed with load. In this way the validity of the theory developed in section 5.5., which gave formulæ for the approximate harmonic content of the output voltage waveforms, was checked.

The procedure carried out in these tests was to keep constant the main d.c. supply voltage and to vary the load resistance and inductance to give a wide range of fundamental power factor. For each combination of load resistance and inductance the r.m.s. values of the first five harmonics in the output voltages were then measured with a waveform analyser. The total r.m.s. value of the output voltage was measured with a voltmeter and the duration of the various periods within each sixth of a cycle measured with an oscilloscope.

Results are given in Figs. 6.10, 6.11, 6.12 for a test carried out under the following conditions:-

$$V_d = 80\text{ V} ; \; V_a = 100\text{ V} ; \; V_{CR} = 210\text{ V}$$
$$L_d = 0.5\text{ mH} ; \; C = 30\,\mu\text{F} ; \quad f = 50\ {}^{c}/\text{s}.$$

The duration T_1 of the commutation period was found to change little during the test, remaining almost constant at about 200 μ Secs. This corresponds to a value for w of 3.6° which is the value used in the calculation of predicted results.

Fig. 6.10 shows the variation of the time T_2 with the load L/R ratio. This measured value of T_2 is compared with the approximate value of 0.7 L/R for T_2 suggested in section 5.5.6. It is seen that

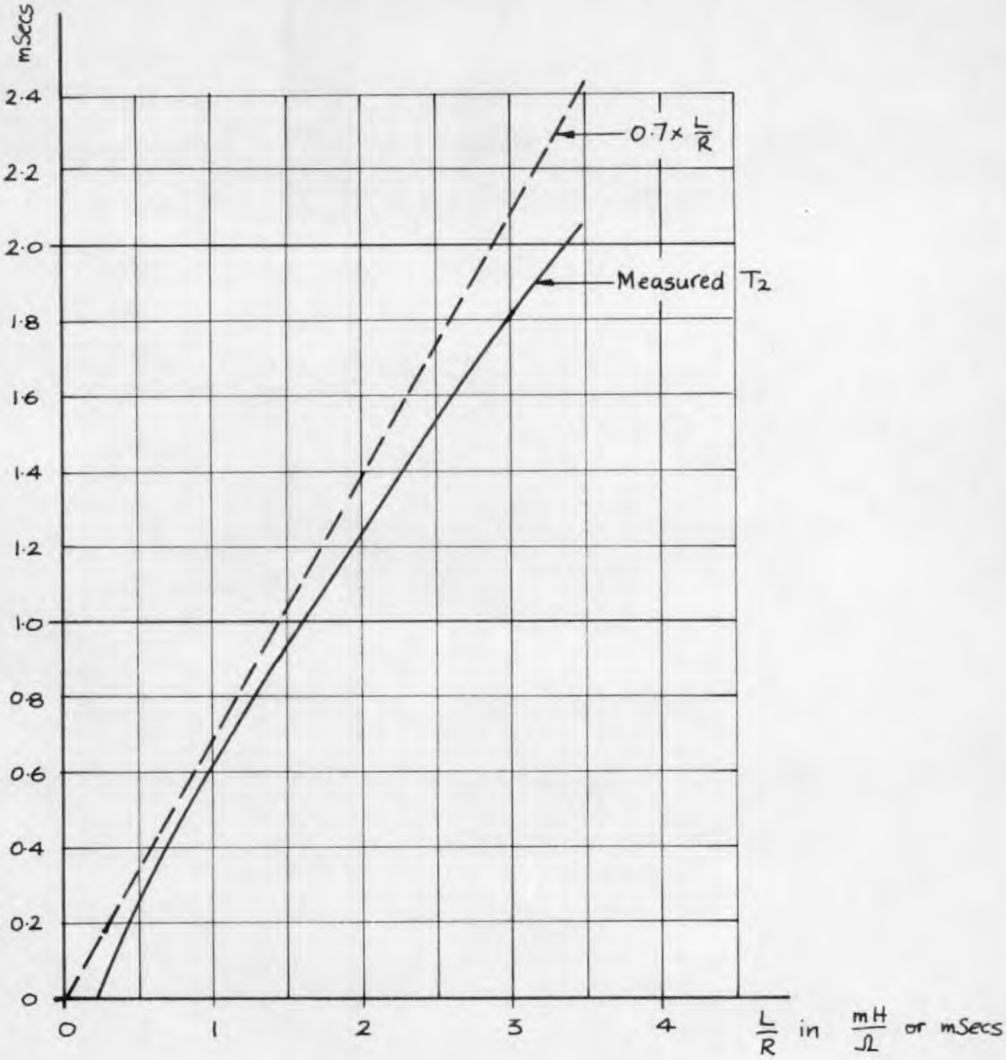


Fig. 6.10 : Variation of time T_2 with load $\frac{L}{R}$ ratio.

0.7 L/R is in fact a reasonable approximation for T_2, being within 10% of T_2 over most of the range covered in the test. At both ends of the range, however, the approximation is invalid for the following reasons:-

(a) when $\frac{L}{R}$ is smaller than, or comparable with, the time T_1 it is possible for the current in the load to be forced to zero in the commutation period. When this happens T_2 must be zero because the phase current being turned off is already zero. For this reason T_2 was seen to be zero until $\frac{L}{R}$ had been increased above about 250 μSecs.

(b) The approximate expression for T_2 is most accurate when I_{L2} is equal to $\frac{V_d}{3R}$. For a low power factor load, in which $\frac{L}{R}$ is long compared with a sixth of a cycle, the value of I_{L2} depends more upon the load inductance's contribution to the load impedance. Hence the greater the $\frac{L}{R}$ ratio the smaller I_{L2} and, consequently, T_2 become. A stage is reached eventually when the power factor is so low that period 2 extends from the end of the commutation period to the end of the sixth of a cycle. When $\frac{L}{R}$ is increased further T_2 remains constant at $(\frac{T}{6} - T_1)$. This is not shown in Fig. 6.10 because the $\frac{L}{R}$ was never made high enough.

Hence it may be concluded that 0.7 $\frac{L}{R}$ is a good approximation for the value of T_2 provided that this time is at least three or four times greater than T_1 and less than about two thirds of $\frac{T}{6}$ (i.e. u less than about 40°). These are arbitrary conditions based on the results shown in Fig. 6.10.

Fig. 6.11 shows the variation of the first five harmonics and the total r.m.s. line-to-line voltage with u, where u is found from the

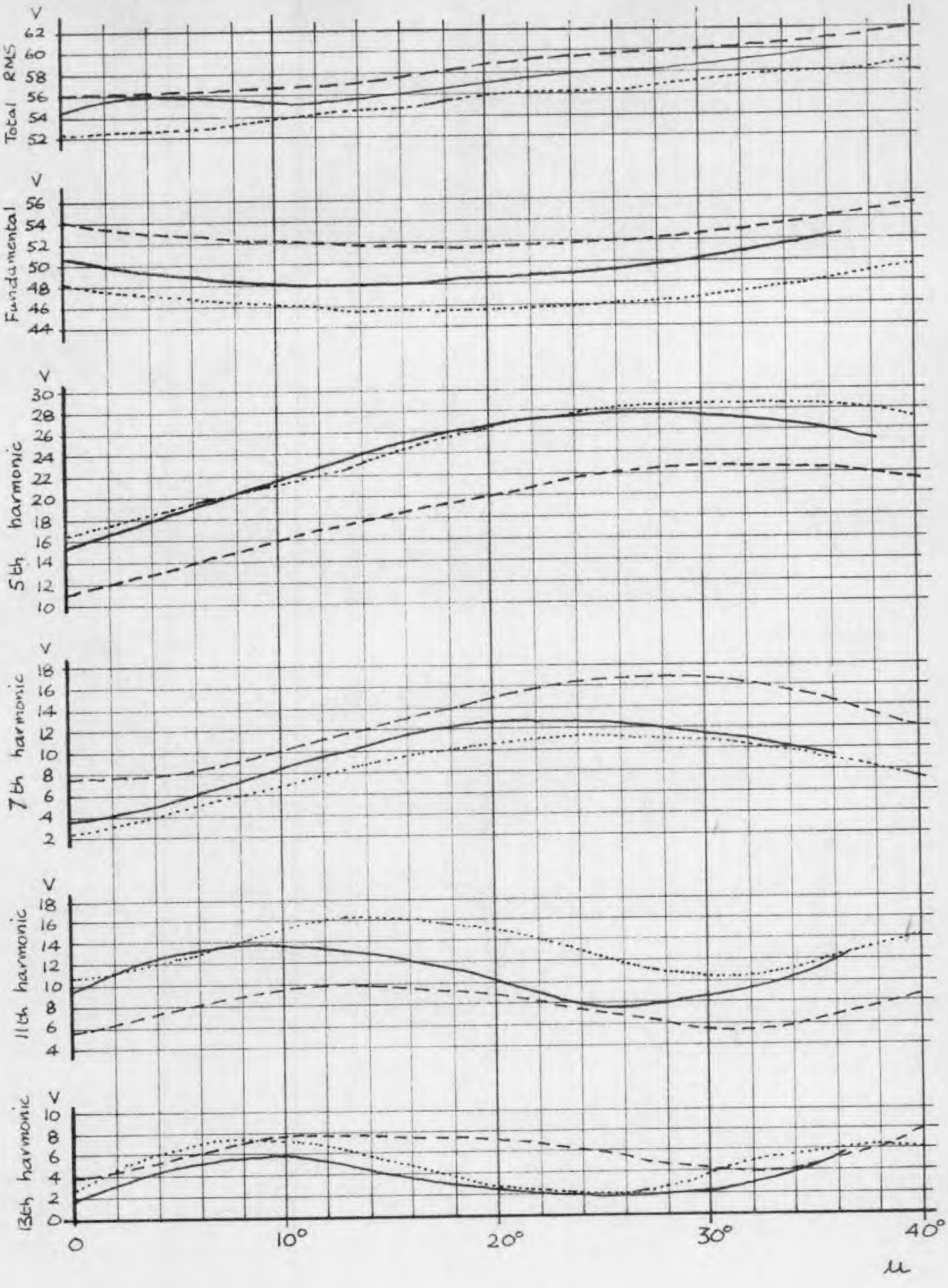


Fig. 6.11: Variation of harmonic content of output line-to-line voltage with u.

$V_d = 80v$, $\omega \simeq 3.6°$, $f = 50c/s$

——— Measured

– – – – Predicted, neglecting commutation

.... Predicted, including commutation.

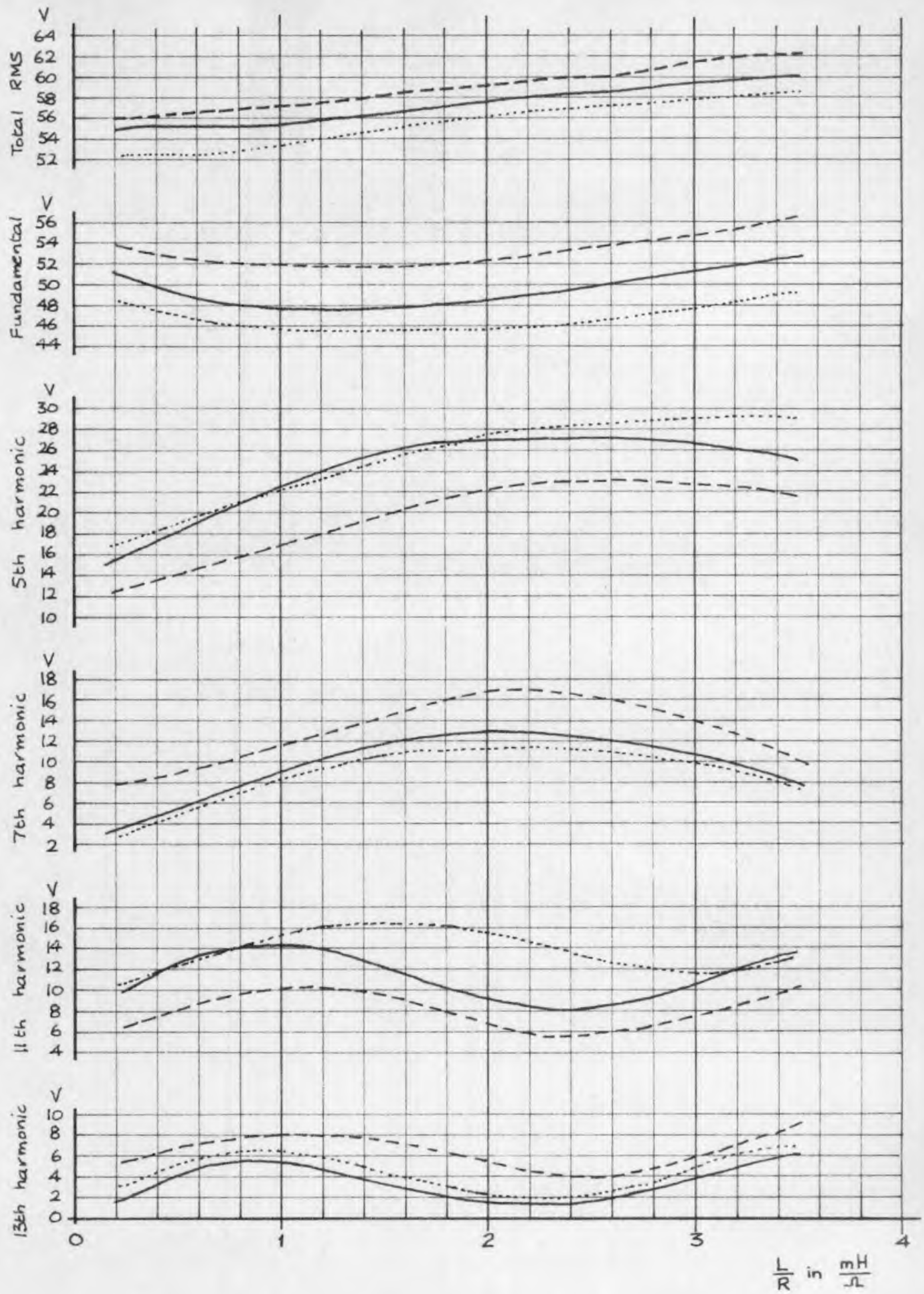


Fig. 6.12: Variation of harmonic content of output line-to-line voltage with load $^{L}/_{R}$ ratio.

$V_d = 80v$, $\omega \simeq 3.6°$, $f = 50c/s$

——— Measured.

– – – – Predicted, neglecting commutation.

··········· Predicted, including commutation.

measured values of T_2. Fig. 6.12 shows the same variation plotted against $\frac{L}{R}$ but in this case the predictions are based upon values of u found from $u \simeq 2\pi f \times 0.7 \frac{L}{R}$.

It is seen that in most cases better agreement between measured and predicted results is obtained by taking the commutation period into account. Good agreement between measured and predicted results is then observed for the total r.m.s. voltage and for the fundamental, fifth and seventh harmonics. For the eleventh and thirteenth harmonics, however, the predicted results are less reliable. In arriving at the predicted results five sine and cosine terms are added. An error in u or w is magnified by the harmonic number and would therefore result in a greater discrepancy at the higher harmonics than at the lower harmonics. The same applies to the assumption made to obtain the period 2 components, i.e. that the period starts at the beginning of each cycle. This would also account for the apparent horizontal shift between measured and predicted results which seems to increase for the higher harmonics.

The difference between the two sets of predicted results is due mainly to the b'_n component. Now $b'_n \propto \frac{\sin nw}{n}$ and hence when w is small b'_n is almost constant for the first few harmonics. In this case b'_n has numerical values falling from 5.9 V for the fundamental component to only 5.3 V for the thirteenth harmonic, being alternately negative and positive. For the first, fifth and eleventh harmonics the sum of the sine components is considerably greater than the sum of the cosine terms and hence the difference between the two sets of predicted results is almost constant. For the other harmonics, however, the cosine terms are of the same order as the sine terms and the difference is no longer constant.

This discrepancy between the two sets of predicted results would be less at lower frequencies where w and hence b'_n and c'_n would be smaller. Conversely at higher frequencies it would be even more necessary to take into account the harmonic content due to the commutation period.

Agreement between measured and predicted results is little worse in Fig. 5.45 than in Fig. 5.44 showing again that 0.7 L/R was a reasonable approximation for T_2 under the test conditions.

The final conclusion to be drawn from the results of this test is that although the eleventh and thirteenth harmonics have not been predicted to the same accuracy as the lower harmonics the predictions give a good indication of the order of magnitude of the harmonics likely to be encountered, i.e. the maximum predicted and measured harmonics are similar though occurring at differing values of u or L/R. The discrepancy between measured and predicted results is probably due to the resistance of the inverter circuit which has not been taken into account in the calculations.

6.5 Variation of Output Waveforms with Frequency.

To determine whether the output voltage and current waveforms were significantly affected by frequency a series of tests were carried out on the circuit using several combinations of circuit parameters. Fig. 6.13 and 6.14 include oscillograms of the output voltage and current taken at 10 $^c/s$. and $50^c/s$. for a single set of circuit parameters. The changes in the waveforms between the two frequencies for this set of parameters was found to be typical of all the waveforms encountered. The opportunity was taken once more for checking the validity of the theory of section 5.3 by comparing the measured results with predicted results.

6.5.1. Test Conditions.

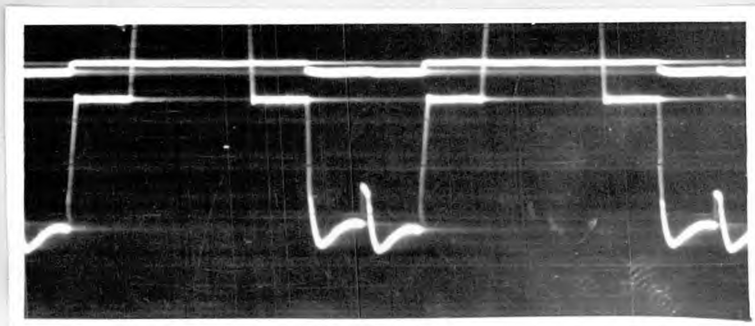
For these tests the following circuit parameters were used :-

V_d = 36 V, V_a = 96V, V_{CR} = 180V, L_d = 0.5 mH, C = 30μF,

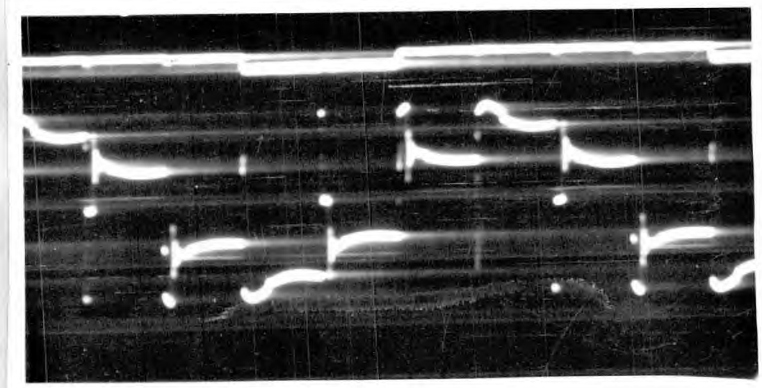
R = 0.8Ω, L = 1.85 mH.

Oscillograms of the output current and voltage were taken at frequencies of 10 $^c/s$. and 50 $^c/s$.

The value of L used is virtually the same as the leakage inductance of the induction motor tested later. The value of R was so chosen that at 10 $^c/s$. and a d.c. voltage of 36 V the load current had the same r.m.s. value as the motor current at about three quarters full load torque.



(a)



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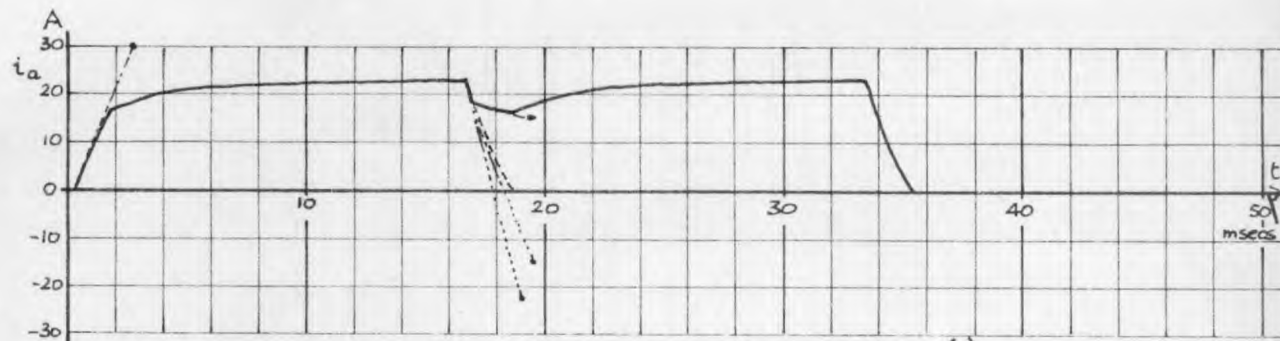

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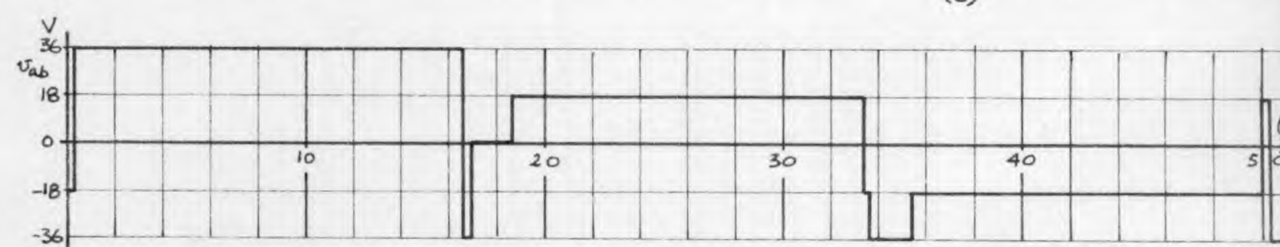


(d)

Fig. 6.13 : <u>Output current and voltage waveforms at 10c/s.</u>

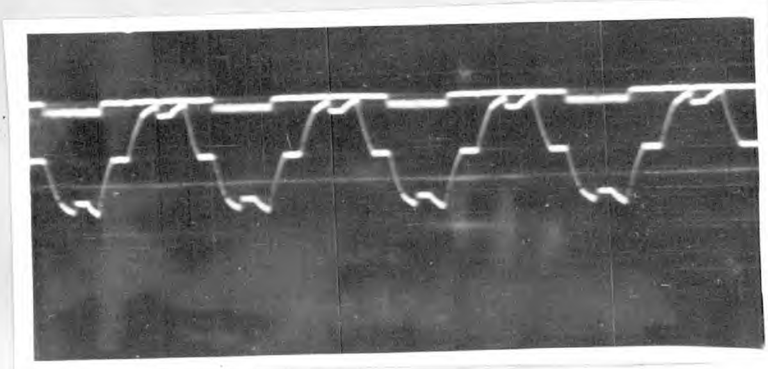
$V_d = 36v$, $R = 0.8\ \Omega$, $L = 1.85$ mH

(a) Oscillogram of output current waveform

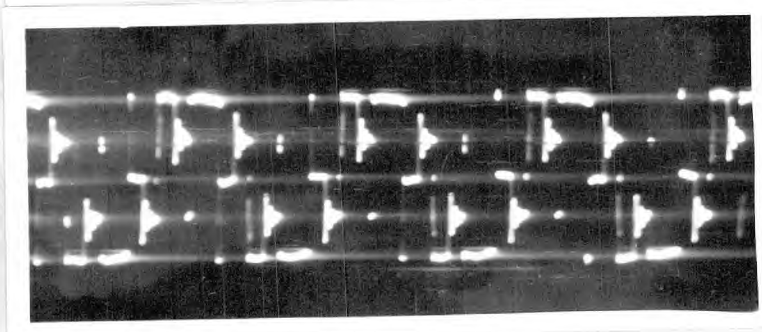
(b) " " " voltage "

(c) Predicted output current wave form } for a half-cycle

(d) " " voltage "



(a)



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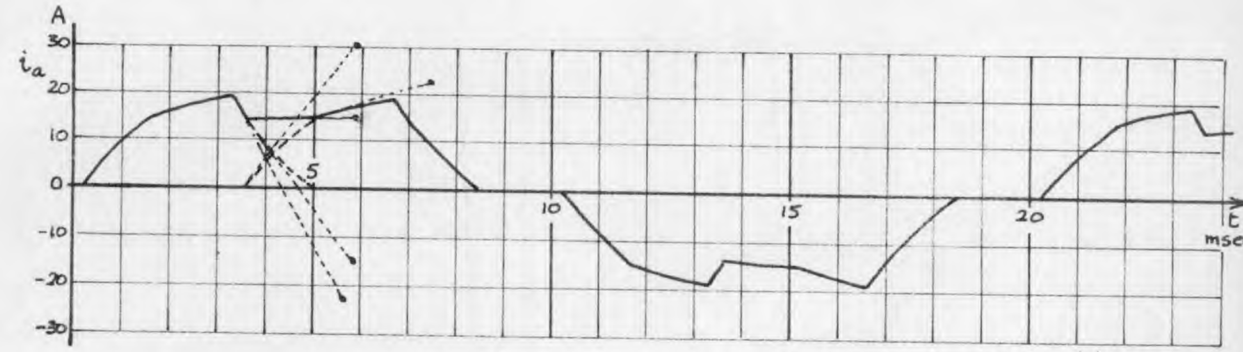

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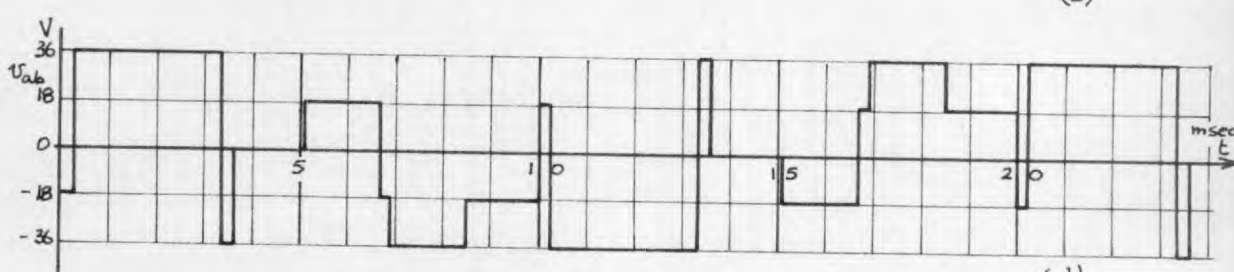


(d)

Fig. 6.14 : Output current and voltage waveforms at 50c/s.

V_d = 36v, R = 0.8 Ω , L = 1.85 mH.

(a) Oscillogram of output current waveform

(b) " " " voltage "

(c) Predicted output current waveform

(d) " " voltage "

6.5.2. Obtaining the Predicted Waveforms.

In figs. 6.13 and 6.14 predicted current and voltage waveforms, calculated for the parameters used, are shown. They have been constructed by the graphical method of section 5.3.6.2 and Fig. 5.26. The construction lines are shown. To construct the waveforms the value of T_1 must first be calculated. When f = 10 $^c/s$. it may be safely assumed that diodes D_7 and D_8 have ceased to conduct at the end of each sixth of a cycle. Since also the load time constant is much less than the duration of one sixth of a cycle it can be assumed that $I_{LO} = \frac{V_d}{2R} = I_{do}$.

Hence $\quad I_{do} = \frac{36}{1.6} = 22.5$ A

$$\omega = \frac{1}{\sqrt{4\, C\, L_d}} = 4.08 \times 10^3 \text{ rad/sec.}$$

Hence $\quad T_1 = \frac{1}{\omega} \tan^{-1} \frac{\omega C(V_d + V_{CR})}{I_{do}}$

$$= \underline{\underline{0.213 \text{ m Secs.}}}$$

At 50 $^c/s$. I_{LO} is lower than at 10 $^c/s$. but I_{do} is probably greater than I_{LO}. However T_1 would not be much smaller than at 10 $^c/s$. so assume that at 50 $^c/s$. $\underline{\underline{T_1 = 0.20 \text{ m Secs.}}}$

These values of T_1 have been used to obtain the constructed predicted waveforms. Only the correct waveforms are shown, i.e. the results of several iterations.

6.5.3. Comparison between Waveforms at 10 $^c/s.$ and 50 $^c/s.$ and between Measured and Predicted Results.

In Fig. 6.13(a) only the negative half cycles of current are shown but the positive and negative cycles are symmetrical. The waveforms of current and voltage do not at first sight appear to resemble those predicted. The main reason for the difference is the fluctuation of the main supply reservoir capacitor voltage. This voltage must fluctuate because of the ripple content of the current drawn from the supply. The fluctuations are most marked when the inverter switching frequency is low and the supply voltage is low. The result at 10 $^c/s.$ is a certain amount of overshoot in the load current waveform caused by the reservoir capacitor's oscillating with the load. It is also seen from the voltage waveform that when diodes D_7 and D_8 cease to conduct the d.c. choke causes a small voltage drop at the inverter d.c. terminals. This is observed on that part of the voltage waveform where the voltage should be $\pm V_d$ after the current has decayed to zero in one of the load phases. Apart from these differences the waveforms are in principle identical.

In Fig. 6.14 the capacitor voltage is much more smooth and diodes D_7 and D_8 appear to conduct continuously, except during commutation. As a result the measured and predicted waveforms agree very well, apart from the oscillation seen in the voltage oscillogram caused by ringing between the S C R filter circuit and the load inductance.

The increase in frequency did not appear to have any significant effect upon the load waveforms, the only real difference being that the exponentially rising and falling portions occupied a greater proportion of the waveform. In both cases the waveforms were essentially as predicted. It was shown in section 5.4 that it would be possible for the positive and negative half cycles of current to merge into a continuous current variation without a dwell at zero if the frequency were raised far enough for the load power factor to become very low.

Table 6.3, below, makes a comparison between the mean and r.m.s. values of voltage and current as measured and as predicted by a full analysis as in section 6.3. It is seen that the predicted and measured results agree to within 10% despite the obvious effect upon the waveforms at 10 $^{c}/s$ of the fluctuation of the reservoir capacitor voltage. It is also seen that in general better results would be obtained if the S C R voltage drop were allowed for by reducing the supply voltage by 2 to 3 volts for the calculations.

Quantity	$f = 10^{c}/s$		$f = 50^{c}/s$	
	Measured	Predicted	Measured	Predicted
I_d	17.7 A	19.3 A	13.2 A	13.1 A
I_{gen}	0.5 A	0.7 A	2.25 A	2.7 A
V_ℓ	23.5 V	25.9 V	25.4 V	27.4 V
I_ℓ	15.0 A	17.1 A	12.1 A	12.5 A

Table 6.3: Comparison between measured and predicted values of current and voltage.

The increase in the r.m.s. output voltage at the higher frequency should be noted. This is due to the change in shape of the output voltage waveform. The reduction in load current at the higher frequency was expected since the load impedance at 50 $^c/s$. was somewhat higher than at 10 $^c/s$.

CHAPTER 7.

TESTS ON THE "D.C. COMMUTATED THREE PHASE INVERTER" WITH INDUCTION MOTOR LOAD.

In this chapter a general study is made of the performance of the inverter-induction motor combination with special emphasis laid upon inverter efficiency and rectifier ratings. In the same laboratory a parallel study was being carried out into the effects of feeding the motor from a variable frequency inverter of a similar type. Hence a detailed study of the motor characteristics has not been attempted, this being a major task in itself.

7.1. Circuit and Test Procedure.

When the simple R-L load was replaced by an induction motor some modifications to the method of overcurrent protection were soon found to be necessary. Until this stage the S C Rs had been protected against current overloads by fuses in series with each of them. This was found to be unsatisfactory because of the rapidity with which the motor would stall when overloaded. The resulting high current drawn through the inverter from the d.c. supply often resulted in commutation failure which almost invariably caused one or more fuses to blow. Consequently a circuit breaker in conjunction with an electronic short-circuiting switch, described in section 7.2., was installed in the circuit as shown in Fig. 7.1 and relied upon for overcurrent protection, leaving a fuse in the d.c. supply line for ultimate protection and a fuse in series

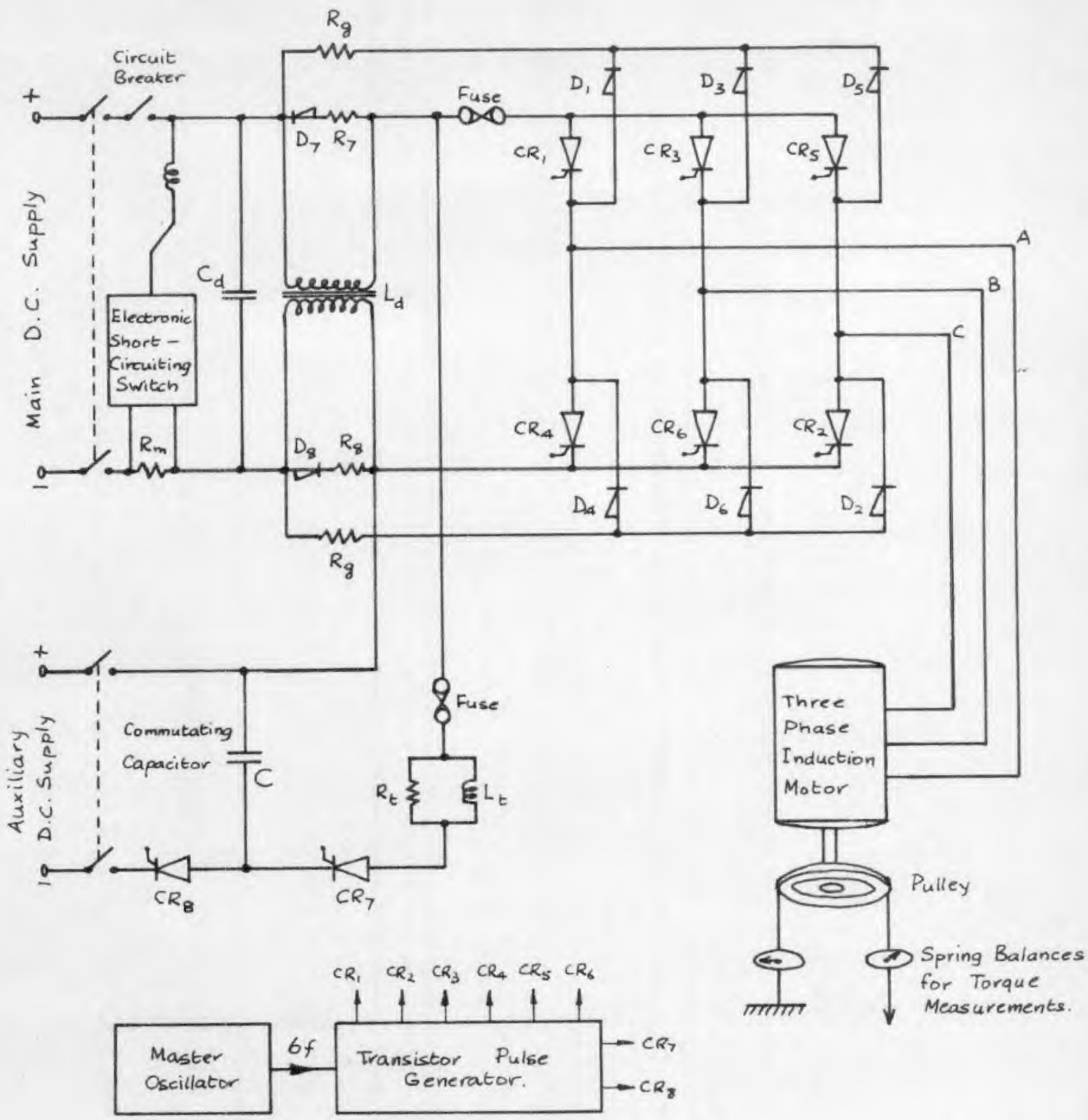


Fig. 7.1: Diagram of circuit used for tests on inverter with induction motor load.

with CR7 to cater for the rare faults in the auxiliary circuit.

The motor stalling problem was remedied to some extent by reducing the load regulation of the main d.c. supply as far as possible. This was done by adjusting the series field to the optimum value in the d.c. generator providing the main d.c. supply. Until this change was made the supply voltage fell considerably when the motor was loaded giving an unstable condition in which the motor stalling torque could fail to meet the applied torque. The even higher currents resulting caused very rapid stalling.

Apart from these changes the electrical circuit, as shown in Fig. 7.1 was much as described in sections 5.1 and 5.2.

The motor speed was measured by a hand tachometer and the motor was loaded by means of a friction belt on a pulley which was driven by the motor. The load was measured by means of spring balances which read the tensions in the two ends of the belt, the difference between the tensions giving the force exerted by the motor at the rim of the pulley. The pulley was so designed that the measured force in lb when multiplied by the motor speed in revs./minute and divided by 10^4 gave the motor output horse-power. The pulley diameter was 12.6 inches and the motor torque in lb-ft. was therefore given by $T = 0.525 \times$ measured force in lb at rim. Tension was applied to the friction belt by a form of screwjack and the pulley was cooled by pouring water inside its rim occasionally.

The motor was a three-phase induction wound rotor slipring motor made by B.T.H. Details of the motor are as follows:-

Type:- MZ 3519

Ratings:- 110 V, 28 A; 50 $^{c}/s$.

5 H.P. at 1420 r.p.m.

Efficiency:- 84% at 0.83 power factor.

Full load:- 35.2 lb at rim of pulley (Torque = 18.5 lb-ft.)

The motor was operated with its secondary (stator) windings short-circuited to simulate the characteristics of a squirrel cage induction motor.

The S C Rs used were Westinghouse Type CS 31 "Trinistors". These had a mean current rating of 24 A for 120° conduction and a voltage rating of 300 V. The S C Rs were mounted on the appropriate Westinghouse heat sinks.

7.2. Overcurrent Protection Circuit.

The circuit for the circuit breaker and short-circuiting switch is shown in Fig. 7.2. The requirements for this protection circuit were that it should detect an overload or fault current, quickly reduce the voltage at the inverter terminals to a safe value and trip the circuit breaker, and that it should be easily re-set. The philosophy behind the design of this circuit was that the d.c. supply would withstand an overload for the short operating time of the circuit breaker whereas the S C Rs in the inverter would not.

The circuit breaker used was a magnetically operated device which could be easily re-set by hand. It was modified to allow its contacts

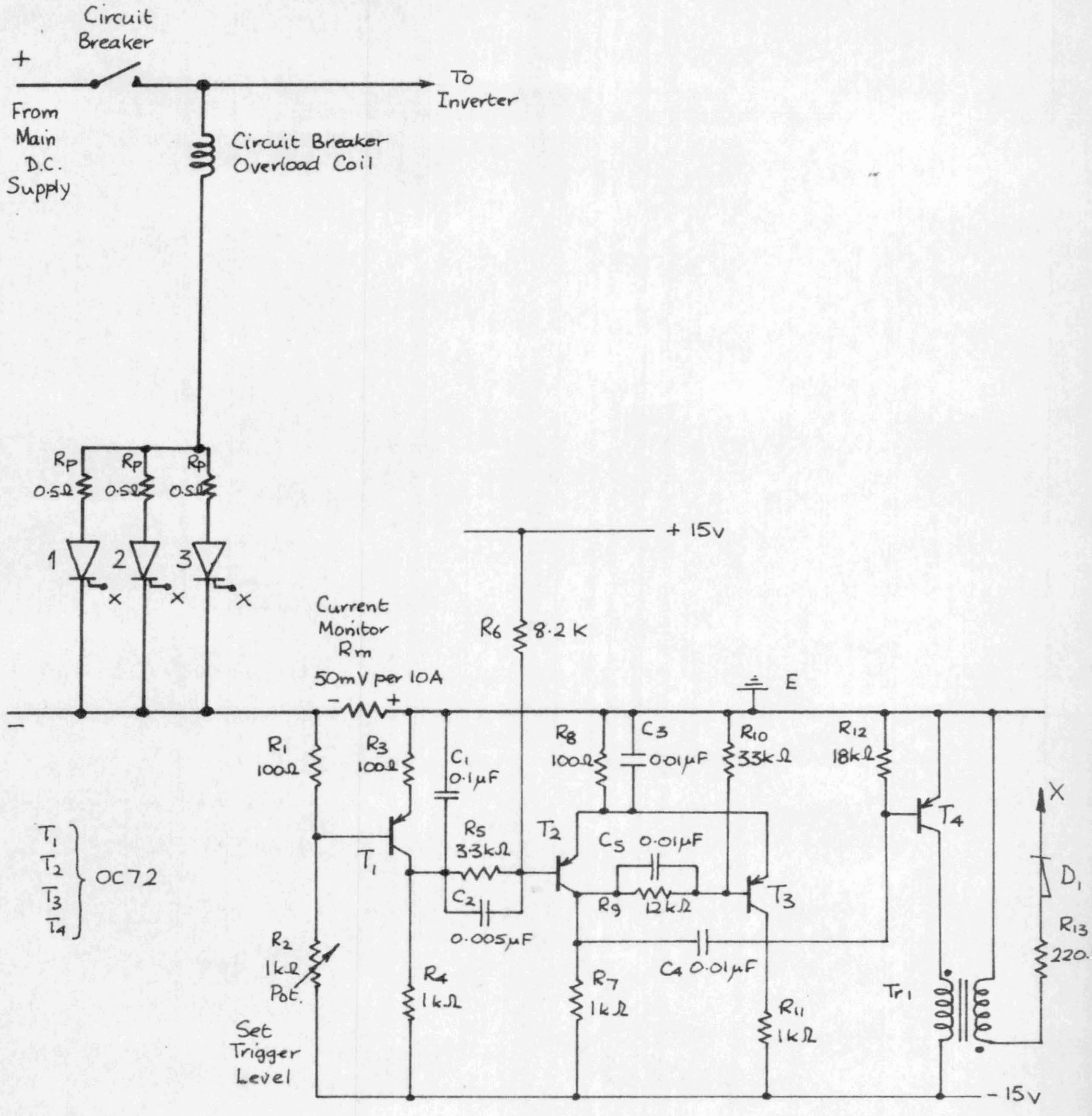


Fig. 7.2: Circuit diagram for the overload and fault protection circuit used with inverter.

to be connected in the positive d.c. line between the supply and the inverter while its operating coil was connected in series with the short-circuiting switch across the d.c. supply lines. In this way the circuit breaker could be set to its most sensitive tripping value, making it act more rapidly and at lower supply voltages than normal.

For the electronic short circuiting switch three S C Rs, labelled 1, 2, 3 in the diagram, were used in parallel. In series with each a 0.5 Ω resistor R_p was connected to limit the current in the S C Rs and to provide sufficient voltage for the slowest S C Rs to fire when one or two had already fired. The S C Rs were fired by a pulse generated by the transistor circuit when the current in resistor R_m exceeded a pre-set value. The transistor circuit consisted of three stages :-

(a) an amplifying stage, using transistor T_1, to amplify the voltage change across R_m,

(b) a monostable circuit, using transistors T_2 and T_3, which changed state very rapidly when the voltage across R_m reached a pre-set value,

(c) a pulse-forming circuit, using transistor T_4, which applied a pulse of voltage and current to the gates of S C Rs 1, 2, 3 via transformer Tr_1 when the monostable circuit changed from its normal state.

The triggering level of the circuit could be adjusted by means of the rheostat R_2 which determined the quiescent voltage on the base of T_1. Capacitor C_1 prevented the circuit from operating spuriously. Capacitors C_2, C_3 and C_5 speeded up the transition of the monostable circuit from one state to the other. Transistor T_4 was turned on by the negative going voltage transmitted by capacitor C_4 from T_2 when T_2 turned off.

The monostable circuit automatically returned to its normal state when the current in R_m fell after the S C Rs had fired and tripped out the circuit breaker. The circuit breaker could then be re-set by hand.

The operating time of the circuit was found to be about 10 μSecs from the moment when the monostable circuit switched over to the instant when S C Rs 1, 2 and 3 fired and reduced the inverter input voltage and current. The circuit breaker tripped out after a further delay of from 30 mSecs, depending upon the main d.c. supply voltage and the resulting short-circuit current in the operating coil.

The current-monitoring resistor R_m was connected between the supply and the reservoir capacitor C_d so that the large peaks of current taken from the capacitor C_d during commutation did not pass through R_m.

7.3. Standstill Impedance, Open-Circuit and No-Load Tests on Motor.

These tests were carried out on the motor to estimate the losses in the windings and iron, the friction and the windage losses, and to obtain an approximate equivalent circuit.

The standstill impedance tests were carried out at 50 $^c/s.$ and 10 $^c/s.$ using a three-phase sinusoidal supply from the mains and from a motor-alternator set. The rotor was locked and a low voltage supply applied to the motor; measurements of voltage and total power being taken at values of current up to and slightly above normal full-load current. From these measurements the values, referred to the primary side, of the total resistance of the motor and the leakage inductance were found. The results of the standstill impedance tests are given

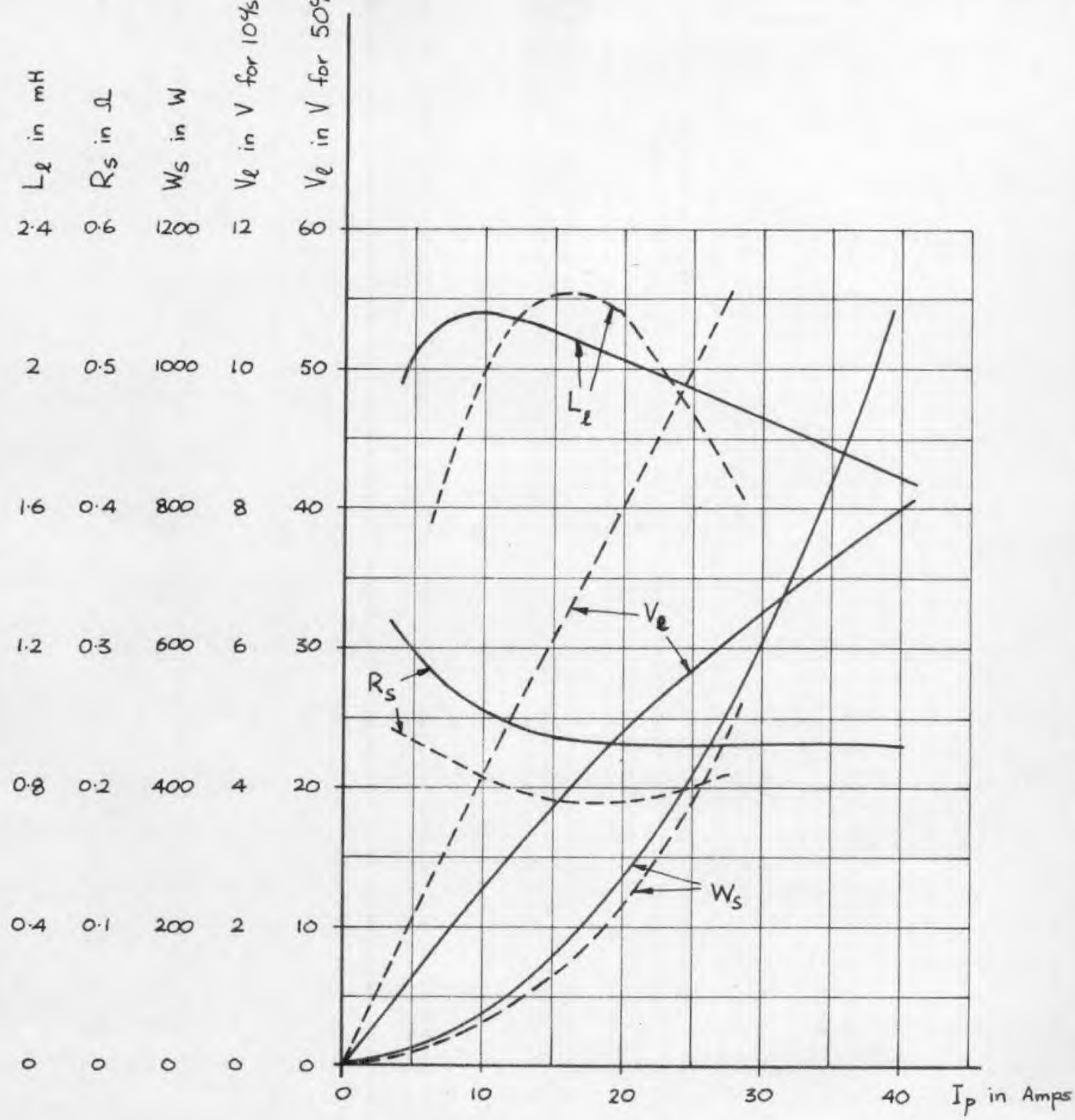


Fig. 7.3: Standstill impedance tests – variation of line-to-line voltage, V_ℓ, power consumption, W_S, resistance, R_S, per motor phase, leakage inductance, L_ℓ, per phase, with motor phase current.

——————— results at 50c/s

- - - - - - - results at 10c/s

in Fig. 7.3. It is seen that the value of the winding resistance referred to the primary side was practically the same at 10 $^c/s.$ as at 50 $^c/s.$ The initial high value in each case may be attributed to the change in brush resistance with current. The effective value of the total leakage inductance, L_ℓ, was also virtually the same at 10 $^c/s.$ as at 50 $^c/s.$ The variations of the total power loss, W_s, with current were also nearly identical at 10 $^c/s.$ and 50 $^c/s.$ The voltage required at 10 $^c/s.$ to produce a given current is seen to be rather more than a fifth of that required at 50 $^c/s.$ for the same current. This is due, of course, to the resistance's contributing more to the standstill impedance at 10 $^c/s.$ than at 50 $^c/s.$

The open-circuit test was carried out by open-circuitng the secondary winding of the machine, applying a voltage to the primary winding, and measuring the power consumed and current taken by the motor. The results of these tests are shown in Fig. 7.4. The variation in current with supply voltage was found to be typical of induction motors, the current rising sharply just before rated voltage. The effective value of the core-loss resistance R_c rose with voltage until the iron began to saturate, the hysteresis loss varying with voltage according to some law between a linear and a square law. When the iron saturated, however, the value of R_c is shown to fall but this does not properly indicate the core loss in the saturation region since much of the power loss measured then consisted of copper loss in the primary winding. The peak value of R_c has therefore been taken as representing the core loss at voltages producing maximum flux in the iron.

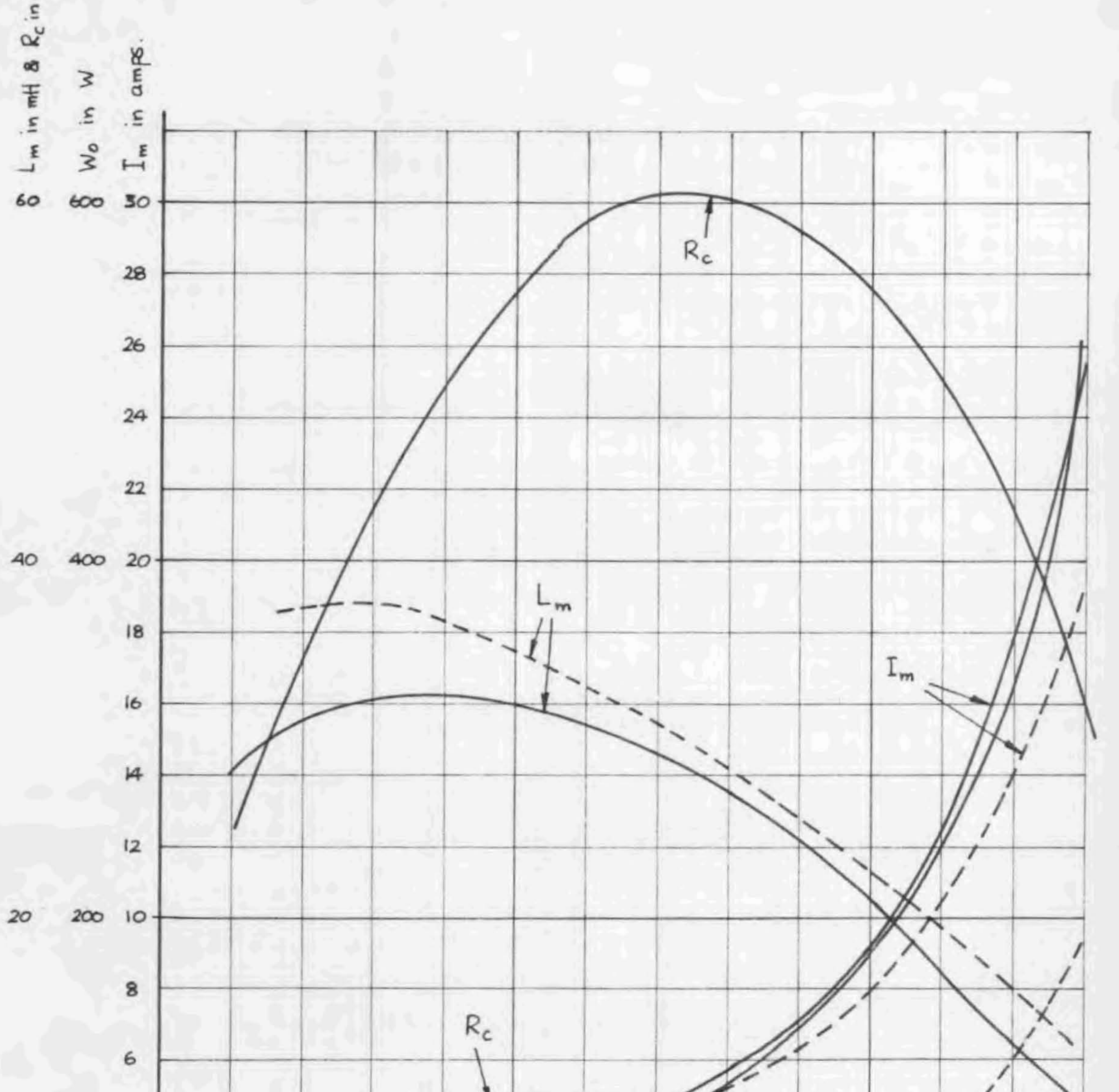


Fig. 7.4 : Open-circuit Tests, — variation with line voltage of motor phase current, I_m, open circuit power loss, W_o, core loss resistance R_c, and magnetising inductance, L_m.

———— 50c/s results ; – – – – – 10c/s results

The magnetising inductance L_m is seen to reach a maximum value corresponding to the point at which the iron has maximum permeability and to fall off at higher voltages as the iron saturated.

The magnetising inductances are seen to be very similar for voltages at 10 $^c/s.$ and 50 $^c/s.$ having the same voltage to frequency ratios. The power loss, W_o, and core loss resistance, R_c, were much smaller at 10 $^c/s.$ than at 50 $^c/s.$ The major portion of the core loss consists of hysteresis loss and for corresponding flux densities at 10 $^c/s.$ and 50 $^c/s.$ the hysteresis loss at 50 $^c/s.$ would be five times greater than at 10 $^c/s.$ Hence the value of R_c at 50 $^c/s.$ would be expected to be five times as great as at 10 $^c/s.$ since the supply voltage would itself be five times greater to produce the same flux density.

From d.c. measurements the primary winding resistance was found to be 0.095 Ω per phase. A figure of 0.21 Ω per phase for the combined primary and secondary resistance has been taken from the results of the standstill impedance test along with a figure of 2 mH for the combined leakage inductance per phase. From the open-circuit tests a figure of 30 mH per phase has been taken for the magnetising inductance per phase. The iron losses measured from the open-circuit tests included the secondary iron losses. Under normal running conditions the slip frequency and the resulting secondary iron losses would be very small. Hence the primary iron losses have been assumed to be one half of those measured from the open-circuit tests and a value of 2 Ω per phase per cycle per second has been taken for the core-loss resistance.

From a no-load test the friction and windage losses were found to be 280 W at 50 $^c/s$. By checking this value at several voltages at 50 $^c/s$. it was also possible to check that the core-loss resistance assumed was a good approximation.

Fig. 7.5 shows the equivalent circuit obtained from the above tests.

7.4. Torque-Speed Characteristics of Overall System.

Fig. 7.6 shows the torque-speed characteristics of the motor over a range of inverter output frequencies. At each frequency the characteristic of the motor was measured for a number of different constant inverter supply voltages. Instead of giving the actual supply voltage a number is given which indicates for each characteristic the ratio of the inverter d.c. supply voltage per output cycle per second to that which would produce an inverter r.m.s. output voltage of 110 V at 50 $^c/s$. on a resistive load.

For each frequency and supply voltage the characteristic of the motor was measured from no-load to stalling. This was done by increasing the tension in the friction belt whilst maintaining the d.c. supply voltage constant and observing the speed of the motor. When the motor speed began to fall very rapidly with an increase in load this was taken to be the stalling point. The torque and speed were extremely difficult to measure accurately at this point using the simple loading method described above and this accounts for the differences between the shapes of the characteristics near the stalling points.

The characteristics were measured for supply voltages which produced stalling torques only slightly greater than the full-load torque of the motor. When the supply voltage was increased beyond these values it

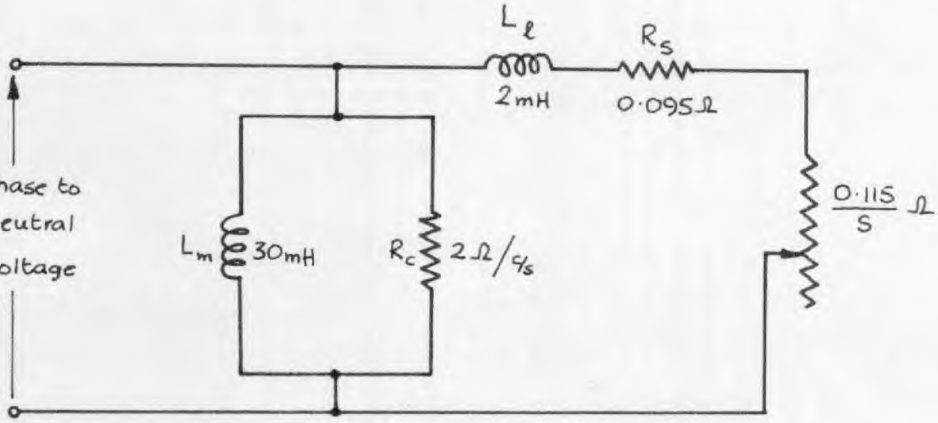


Fig. 7.5: Simple equivalent circuit of induction motor per phase

(S = per unit slip frequency)

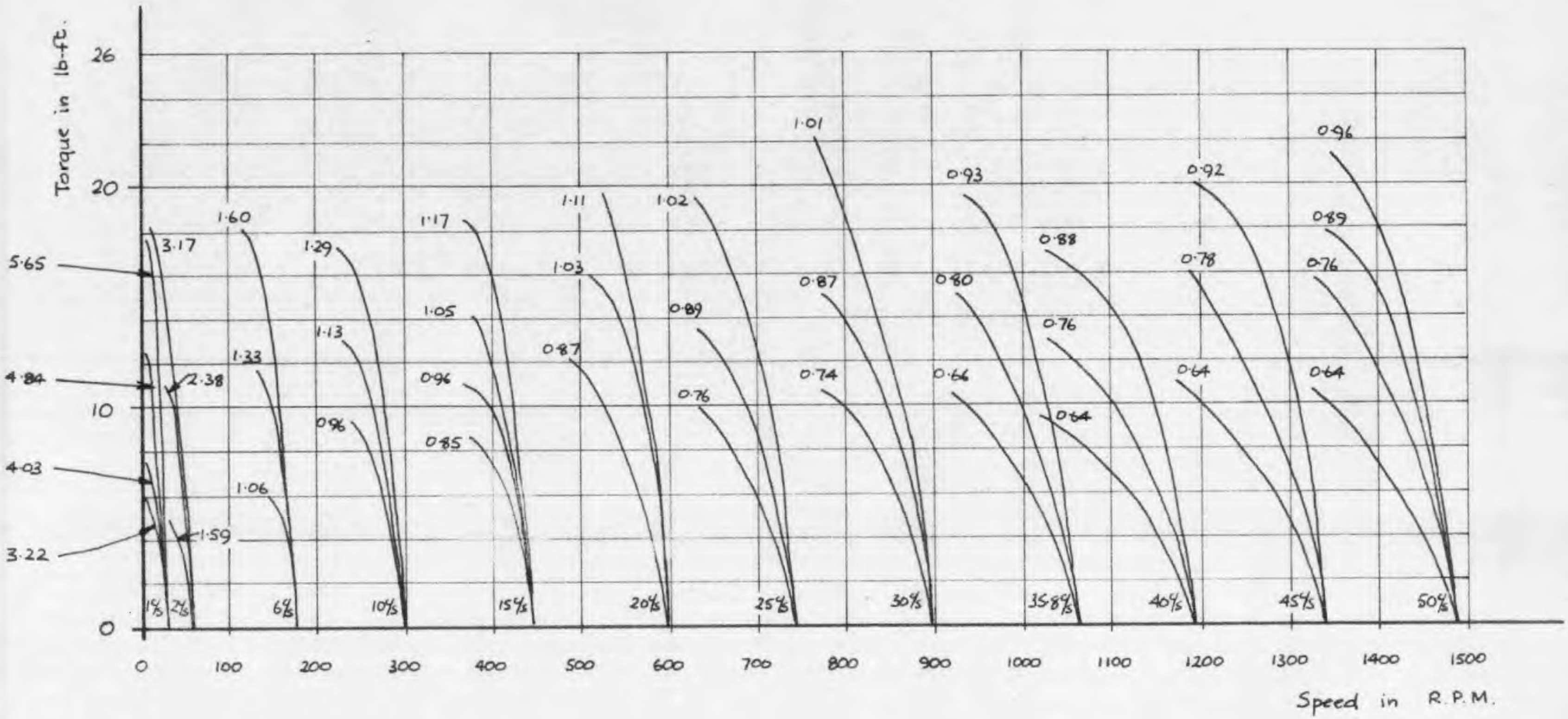


Fig. 7.6 : Torque - speed characteristics of inverter - motor combination for several inverter output frequencies and supply voltages.

was found that the motor drew very high peaky currents from the supply and sufficient commutating capacitance to cope with these currents had not been installed.

Although the motor was run lightly loaded on many occasions at speeds up to 2250 r.p.m. it was not found possible to take measurements up to full load torque at speeds higher than about 1500 r.p.m. This was because the high supply voltages required would have caused voltage transients high enough to cause damage to the S C Rs and also because the rated voltage of the main supply reservoir capacitor C_d was insufficient. At 50 $^c/s$, the supply voltage, V_d, required for full load torque was 150 V and the capacitor was rated at 175 V. Reverse voltage transients on the S C Rs at this stage had already reached 350 V.

From Fig. 7.6 it may be seen that to produce the same maximum torque for each speed the inverter supply voltage must be varied almost proportional to frequency except at the lowest frequencies. This is to be expected since the maximum torque obtainable from an induction motor is proportional to the square of the air gap flux. At the higher frequencies the motor winding resistance is much smaller than the magnetising reactance and hence the supply voltage required for constant flux is proportional to frequency. As the frequency is lowered, however, the motor resistance becomes more significant and a higher supply voltage, proportionally, is required to produce the same flux.

It may also be seen that at the lower frequencies the measured motor slip speed for a given torque was rather less than at the higher frequencies. If the inverter output voltage had been sinusoidal, this phenomenon would be surprising since it may be shown, using the simple equivalent circuit of the induction motor, that at any frequency the maximum torque is obtained when $s\omega = \frac{R_s}{L_\ell}$. It was found from the standstill impedance tests that R_s and L_ℓ were virtually the same at 10 $^c/s.$ as at 50 $^c/s.$ and hence $s\omega$, i.e. the slip frequency which is proportional to the actual slip speed, should be the same at all frequencies. It is possible that at the higher frequencies the harmonics present in the inverter waveforms would cause the effective value of R_s to increase due to eddy currents in the conductors and reduce the effective value of L_ℓ due to eddy currents in the iron. This explanation would seem to be most unlikely in a motor so small. If eddy currents were the cause of the higher slip at the higher frequencies, it would be expected that the motor would run slower at 50 $^c/s.$ when fed from the inverter than when fed from a sinusoidal supply. However, at 1420 r.p.m., the rated full-load speed of the motor, the torque when the inverter supply voltage was 150 V was 15.2 lb-ft. The supply voltage corresponded to 105 V r.m.s. motor voltage and 101 V fundamental 50 $^c/s.$ component (assuming basic square inverter output waveform). If the fundamental 50 $^c/s.$ component had been 110 V the motor would have produced a torque equivalent to $15.2 \times (\frac{110}{101})^2$, i.e. 18.0 lb-ft. This is marginally less than the rated full-load torque of 18.0 lb-ft. at 1420 r.p.m. Consequently it must be concluded that at the higher frequencies the motor slip was normal but at lower frequencies the slip was smaller than would be expected. It must also be concluded that this reduced slip is due to the voltage waveform of the inverter-motor combination or due to the characteristics of the braking system used.

The brake, as previously described, was simply a belt running over a pulley driven by the motor. Tension was applied to the belt by screwing up one end and extending it. At low frequencies, especially at 1 $^c/s.$, the motor torque was seen and felt to pulsate severely. On increasing the frequency, however, the pulsations decreased because of the effect of the motor's inertia and at the higher frequencies the motor inertia was sufficient to absorb practically all the pulsations, giving a smooth output torque. At the low frequencies it is possible that the belt might have stretched during the torque peaks and, because of its own inertia, remained relatively slack between these torque peaks. If this were the case, the rotor would have been allowed to accelerate more freely immediately after a torque peak than if a constant belt tension had been maintained. The measured mean motor speed and the measured mean torque would give unreliable results under these circumstances. The investigation was not carried far enough to confirm or disprove any of these theories but it did raise the question of whether the mean slip as measured with a tachometer has much meaning under conditions of pulsating motor speed and non-uniform rotation of air-gap flux.

The torque pulsations were undoubtedly caused by the uneven rotation of the air-gap flux. In each sixth of a cycle the flux rotated through sixty electrical degrees. Under ideal conditions with a three-phase sinusoidal supply the magnitude of the flux would be constant and its rotation uniform. However, in the inverter-fed motor at the lower frequencies the current in one phase falls to zero before the end of each sixth of a cycle and all the rotation of the flux would therefore take place in this time. During this part of the cycle the motor would operate as a three-phase induction motor with a high relative speed (the slip speed) between flux and the secondary circuit conductors. In the latter part of each sixth of a cycle the flux does not change position but does increase in magnitude. During this period the motor would behave as akind of single phase induction motor. At low frequencies, where the winding resistance of the motor becomes significant compared with the the magneticing reactance, it is possible for the flux to reach a steady value in the last part of each sixth of a cycle. In this case the motor would behave as an induction brake with reversed torque.

7.5. Variation of Inverter Efficiency and Losses with Frequency and Load.

In the course of measuring the torque-speed characteristics of the inverter-motor combination readings were taken of the current, voltage and power in various parts of the system. This enabled the inverter efficiency, motor efficiency, and overall system efficiency to be determined in order to find as far as possible where the power losses were dissipated.

In this section the inverter efficiency is considered.

7.5.1. Test Conditions.

Throughout the tests the commutating capacitance was constant at $32\mu F$ and the total inductance of the d.c. choke, i.e. $4\ L_d$, was constant at 2 mH. In series with diodes D_7 and D_8 resistances R_7 and R_8, each of 0.15Ω, were connected to reduce the rate of rise of I_{do} with frequency. It was decided to connect this resistance in series with diodes D_7 and D_8 rather than in series with the two halves of the d.c. choke in order not to increase the losses due to the current flowing into the S C R bridge, particularly at low frequencies. To overcome the tendency for the choke current to decay after commutation through the conducting bridge S C Rs and the reverse bridge diodes a resistance R_g of 0.3Ω was connected in each d.c. line from the reverse diode bridge. These values were chosen arbitrarily to give a good compromise between low I_{do} and low R_g at the higher frequencies.

Fig. 7.7 shows how the supply voltages V_d and V_a were increased with frequency. At each frequency a value of V_d was used which was sufficient for the motor to develop its rated full-load torque though not so great that the motor iron was driven into hard saturation. V_a was maintained at 100 V up to 15 $^c/s$. but it was found necessary to increase V_a as the main supply voltage was further increased.

In theory (see section 5.3.4.5., equation (5.37)) V_{CR} should have been equal to $(V_d + 2\ V_a)$. Had this been the case $(V_{CR} - V_d)$, i.e. the voltage through which the commutating capacitor can charge whilst reverse-biasing the bridge S C Rs, would have been equal to $2\ V_a$. Then for a constant maximum I_{do} a single value of V_a would have been

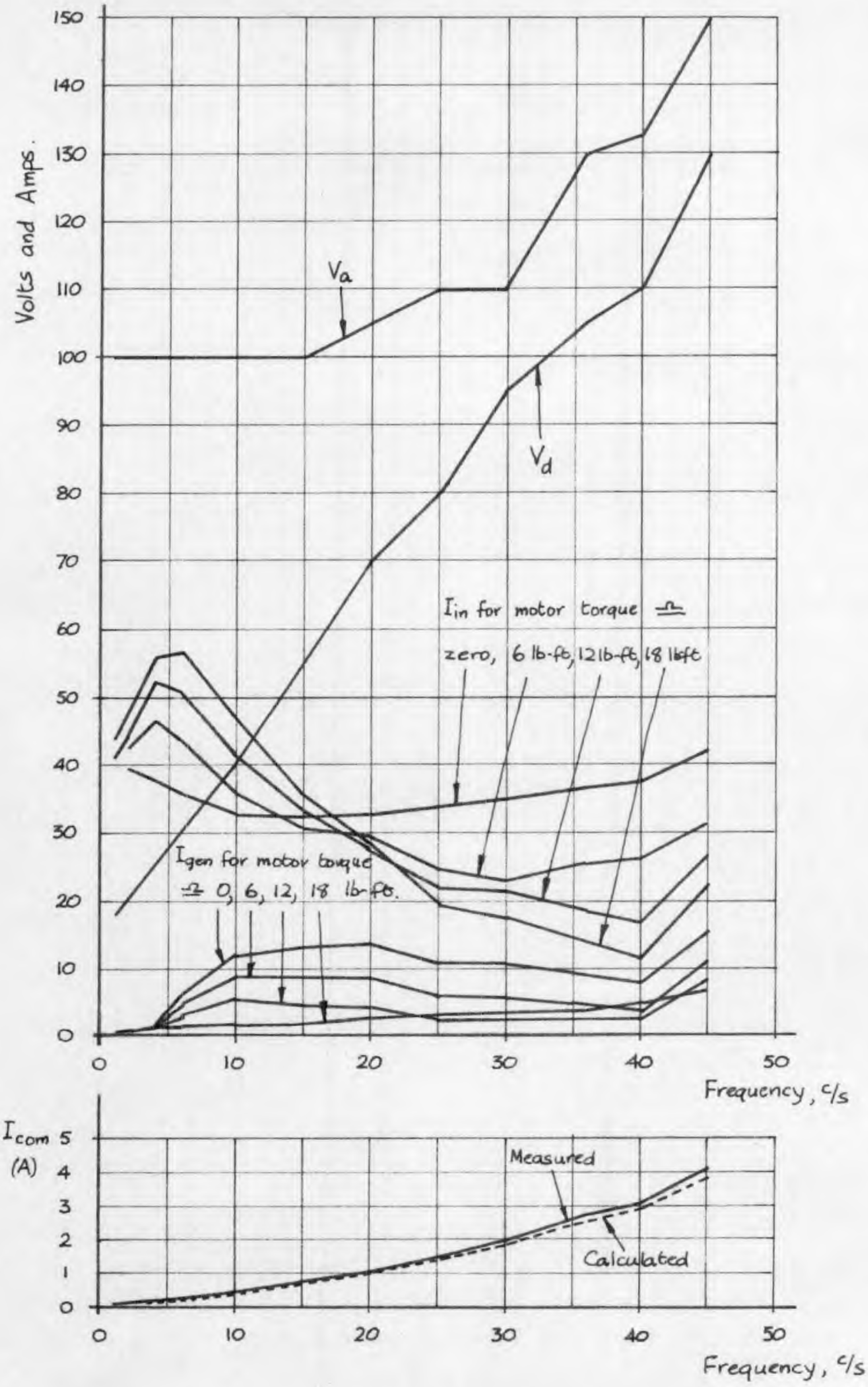


Fig. 7.7 : Variation with frequency of inverter supply voltages, V_d and V_a, converted current, I_{in}, current I_{gen} in reverse diode bridge, and commutation current I_{com}.

adequate throughout the entire frequency range. In practice the inductance of the auxiliary d.c. supply was relied upon to provide the desired capacitor voltage overshoot beyond V_a when re-charging. Unfortunately the resistance in this re-charging circuit reduced the value of V_{CR} from the maximum attainable and it was found that during the tests the value of V_{CR} was given approximately by

$$V_{CR} = V_a + 0.65\,(V_a + V_d)$$

$$= 1.65\,V_a + 0.65\,V_d$$

$(V_{CR} - V_d)$ was thus approximately equal to $(1.65\,V_a - 0.35\,V_d)$ and hence fell as V_d was increased, necessitating an increase in V_a to make up the deficit.

Fig. 7.7 also shows the variation with frequency of I_{in}, the current flowing into the S C R bridge, I_{gen}, the current returned to the supply through the reverse diode bridge, and I_{com}, the current flowing into the commutatingcapacitor from the main and auxiliary d.c. supplies. These are the mean values of these currents. The mean value I_d of the current taken from the main d.c. supply is equal to $(I_{in} + I_{com} - I_{gen})$ and is shown in Fig. 7.8. Both measured and calculated values of I_{com} are shown, the calculations being based on $V_{CR} = 1.65\,V_a + 0.65\,V_d$. The measured and calculated values are seen to be almost identical. Comment upon the other current variations will be made in section 7.7.

A typical value for the forward voltage drops for S C Rs was found to be 1.5 V and for diodes 1.0 V. The total effective value of

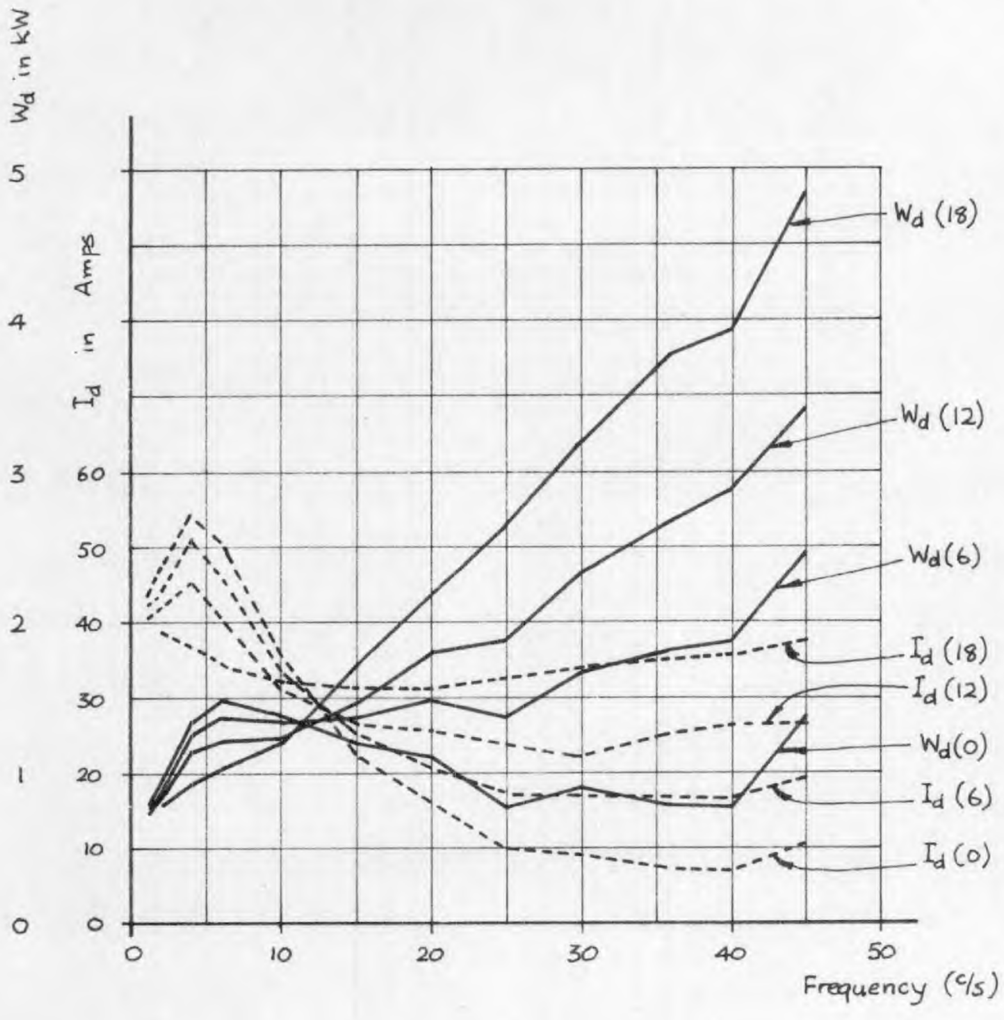


Fig 7.8: Variation with frequency of the current I_d and power W_d taken from the main d.c. supply for four motor load conditions.

Figures in brackets give approximate motor torque in lb-ft for each curve drawn.

lead resistance in the inverter circuit, not including the d.c. choke, was measured as 0.1 Ω. Each half of the choke had a resistance of 0.03 Ω.

7.5.2. Inverter Power Losses and Efficiency.

Fig. 7.8 shows how the power taken by the inverter from the main d.c. supply changed with frequency for the four motor loads used. Fig. 7.9 shows the power lost in the inverter as the difference between main d.c. supply power and inverter output power. No account is taken in this diagram of the power taken from the auxiliary supply which may be assumed to be an additional power loss in the circuit. Fig. 7.9 also shows the estimated major components of the inverter power loss together with their sum.

The components of the power loss have been estimated using the measured values of current and voltage as follows :-

(a) Commutation power loss, $P_{d\ com}$, found from $P_{d\ com} = V_d \cdot I_{com}$

(b) Bridge S C Rs conduction losses. Since two S C Rs conduct, effectively in series, at all times (except the commutation periods), the total S C R voltage drop is 3 V and the conduction losses are then given by $I_{in} \times 3$ V.

(c) Losses in the power leads. These have been calculated as $I_{in}^2 \times 0.1\ \Omega$

(d) Reverse bridge diode conduction losses. These have been calculated as $I_{gen} \times 2$ V since two diodes are involved which are effectively in series.

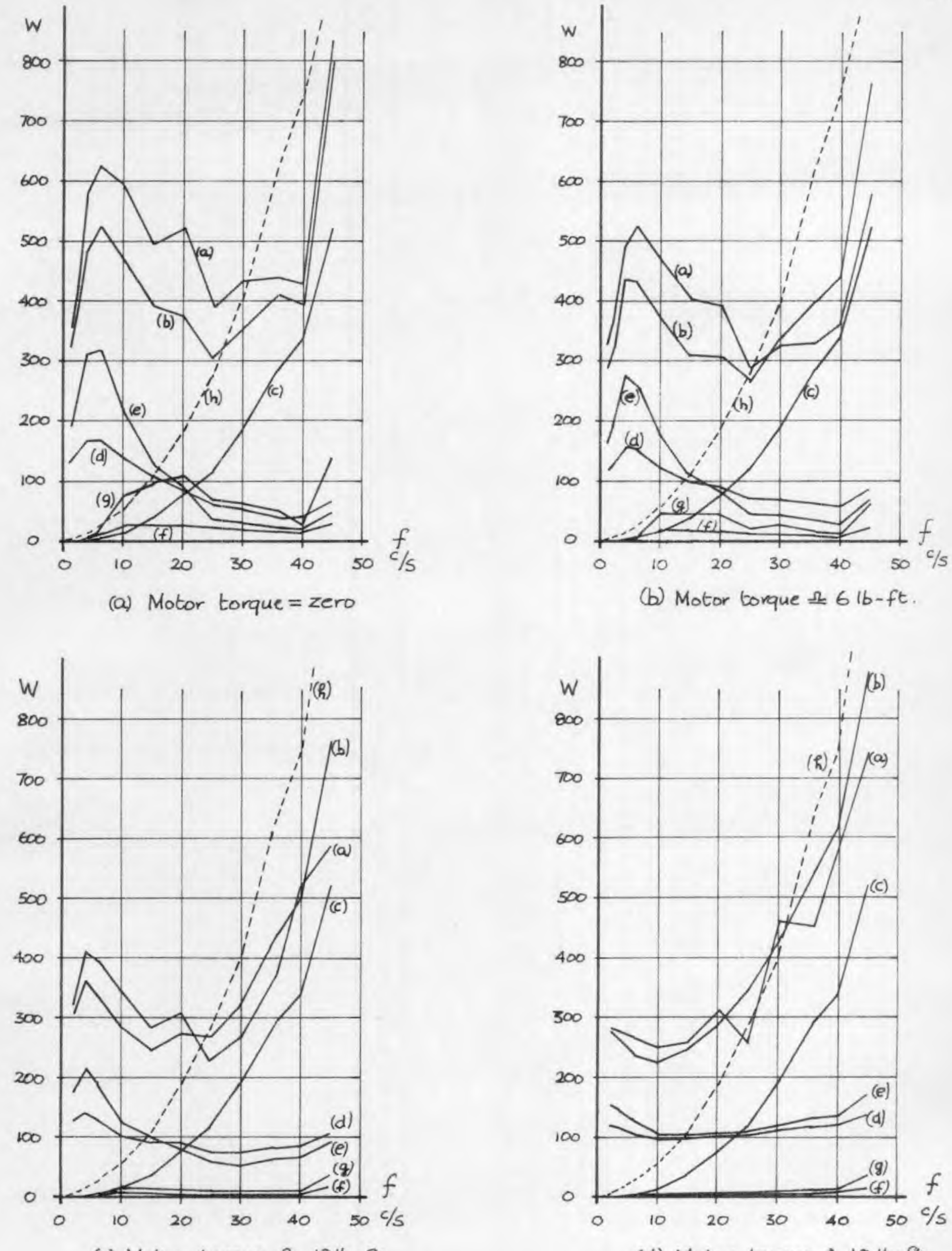


Fig. 7.9: Variation with frequency of inverter power loss and its components for several motor load conditions.

(a) Measured P_{cx}; (b) Estimated P_{cx}; (c) P_{dcom}; (d) $3 I_{in}$; (e) $0.1 I_{in}^2$; (f) $2 I_{gen}$; (g) $0.6 I_{gen}^2$; (h) Total P_{com}.

(e) <u>Losses in R_g</u>, calculated as $I_{gen}^{2} \times 0.6\Omega$.

The I^2R losses calculated as in (c) and (e) are approximate since the measured values used for I_{in} and I_{gen} were mean and not r.m.s. values. The true values of these losses would be a little higher, depending upon the form factor of the current waveforms, but the values given are sufficiently accurate to indicate the relative magnitudes of the several losses. At low frequencies where the d.c. choke current decays to the value of S C R current after each commutation the choke resistance would contribute to the losses in power leads and this component of loss would thus be greater than indicated. A further source of error is that despite the presence of R_g in the circuit some of the d.c. choke current decays through the S C R and reverse bridge diodes. Thus the measured values of I_{in} and I_{gen} were higher than their true values and this results in part of P_{com} being allowed for twice. This is most significant at high frequencies when the voltage across R_7 and R_8 is highest, due to the high P_{com} to be dissipated, and at low values of I_{gen} when the motor is loaded.

Referring to Fig. 7.9 once more it is seen that the estimated total power loss compares quite favourably with the measured power loss, agreement to within 15% being obtained in general. The errors in estimating the losses described in the previous paragraph account for some of the discrepancy and some random discrepancies can be attributed to drift in motor torque during the course of taking measurements, caused by changes in the brake belt coefficient of friction and tension under prolonged running conditions.

Of all the losses in the circuit it is seen that the commutation loss was by far the greatest single item above approximately 20 $^{c}/s$. If the total power required for commutation, taken from both main and auxiliary supplies, as shown by the dotted lines in Fig. 7.9., is compared with the other losses, it is seen that this became greater than any other single loss at about 15 $^{c}/s$. At very low frequencies the total commutation power loss was small but increased with frequency according to some law between a square and cubic law. (This is the reason why readings were taken only up to 45 $^{c}/s$. To obtain measurements at 50 $^{c}/s$. and above would have necessitated making several alterations to the circuit which would have changed the pattern of some of the readings.)

The losses due to the currents I_{gen} and I_{in} varied with the motor load as a direct result of the variation of the currents themselves with load. This will be discussed further in section 7.7.

Fig. 7.10 shows the variation of inverter efficiency with frequency for the four motor loads. Two types are indicated, the first being the main d.c. supply to inverter output efficiency ignoring the auxiliary power supplied, the second being the overall efficiency of the inverter with the auxiliary power taken into account. At low frequencies the efficiency was low because of the power losses in the rectifier and circuit resistance at the abnormally high currents flowing. The efficiency then increased as the power losses decreased and the converted power increased, but later decreased when the commutation power absorbed by the circuit began to become more and more significant compared with

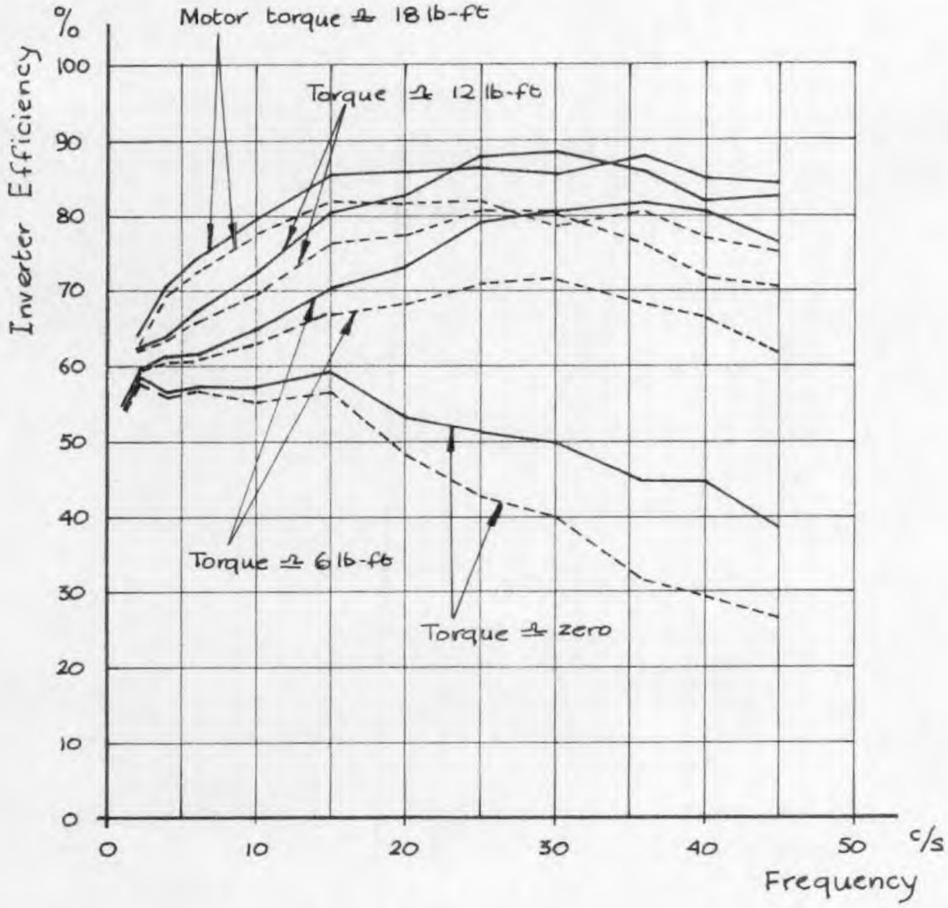


Fig. 7.10: Variation of inverter efficiency with frequency for several motor load conditions.

——— auxiliary supply power ignored

- - - - - - auxiliary supply power taken into account.

the converted power. Maximum efficiencies of 88% were recorded between 25 $^c/s$. and 35 $^c/s$, ignoring the auxiliary supply power, or an overall efficiency of 82% at 15 $^c/s$.

The efficiency was naturally lower at the lighter than at the heavier loads since the commutation loss and, to some extent, the converted current at low frequencies were independent of load.

At a motor torque of 18 lb-ft. the overall efficiency of the inverter was nearly constant at approximately 80% between 15 $^c/s$. and 35 $^c/s$. If it is assumed that the only circuit losses which could be reduced are the power load resistance losses and the losses in R_g and that when these resistances were made zero a corresponding increase in output power would result, the overall efficiency would be 88% at 15 $^c/s$. and would fall to 79% at 45 $^c/s$. It would seem, therefore, that the maximum efficiency attainable at 50 $^c/s$. would be of the order of 80%. This figure is still far short of the 94% suggested in section 5.7.3. for several reasons. Firstly the S C R and diode losses would account for a loss of efficiency of about 3%. Secondly the formula given in equation (5.96) assumes that the re-charging circuit is 100% efficient and that V_a is kept equal to V_d while C is varied. This was not the case in practice and some deviation from optimum must be expected for this reason. Thirdly equation (5.96) is based on the assumption that I_{do} is nearly equal to the mean value of I_d. Using equations (5.98) and (5.105) for the conditions of the test it would be found that I_{do} would be nearly twice the measured value of I_d at 45 $^c/s$. Consequently the loss in efficiency due to commutation power would be at least twice as great as that suggested by equation (5.96).

7.6. Variation of Motor Efficiency and Losses with Frequency and Load.

7.6.1. Test Conditions.

The test conditions were as described in section 7.4 for the torque-speed measurements. It should be emphasised once more that the d.c. supply voltage, not the motor terminal voltage, was kept constant at each frequency.

Fig. 7.11 shows how the motor terminal line-to-line voltage, V_ℓ, the motor line current, I_ℓ, and the motor input power, W_i, varied with frequency for the four motor loads between no-load and rated full-load output torque. The values of current and voltage are their r.m.s. values. The change in motor voltage with load was caused by the effective resistance drop in the inverter and by the change in voltage waveform with load. Some waveforms of motor current and voltage are shown and discussed in section 7.8.

7.6.2. Motor Power Losses and Efficiency.

Fig. 7.12 shows how the measured motor power loss, P_{mx}, varied with frequency for three loaded conditions of the motor. This power loss was the difference between the power supplied by the inverter to the motor and the power dissipated in the friction belt brake used for loading the motor. Also shown in Fig. 7.12 are the estimated values of the four main components of the motor losses together with their sum.

The estimated loss components were calculated as follows:-

(a) Primary copper losses. These have been calculated as $3 \times I_\ell^2 \times 0.1\Omega$ since the primary resistance was measured as 0.1Ω per phase.

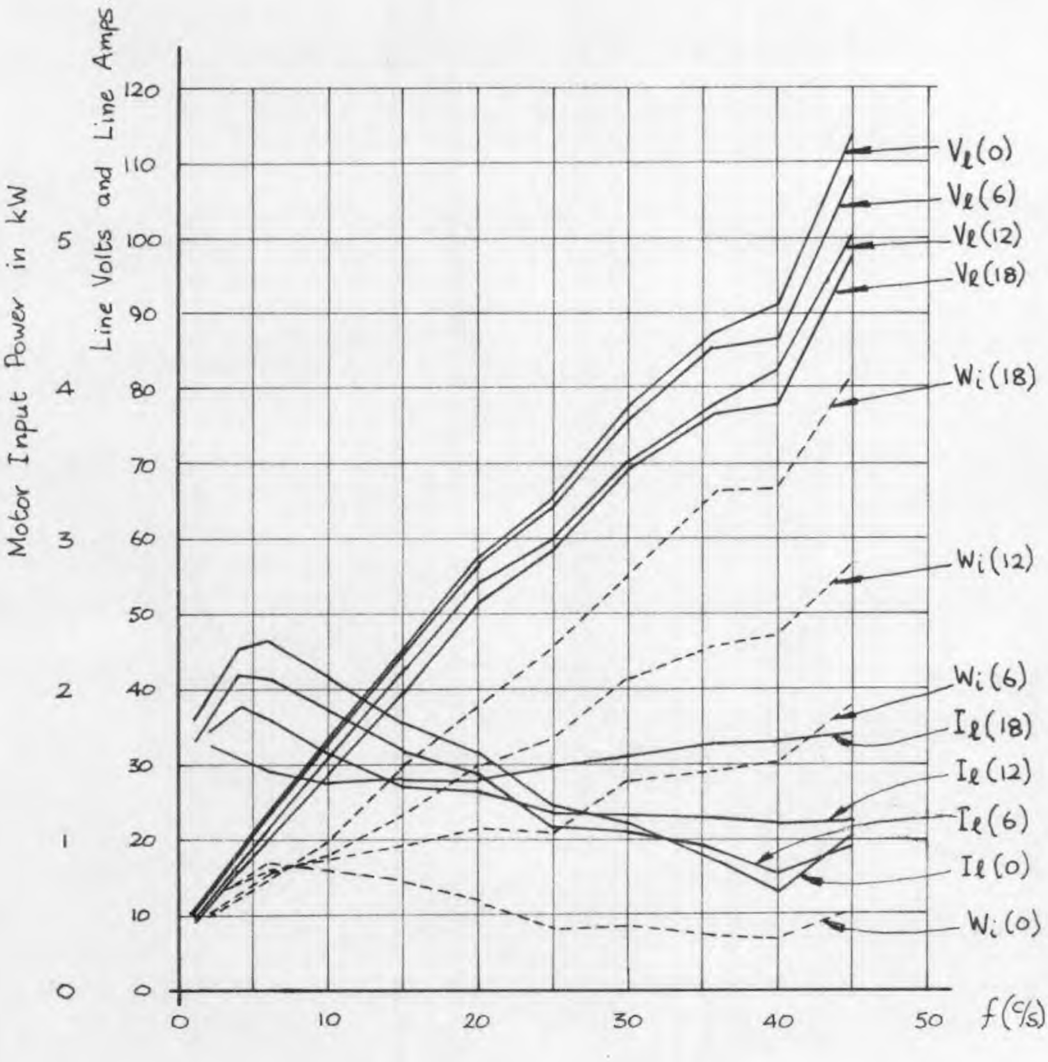
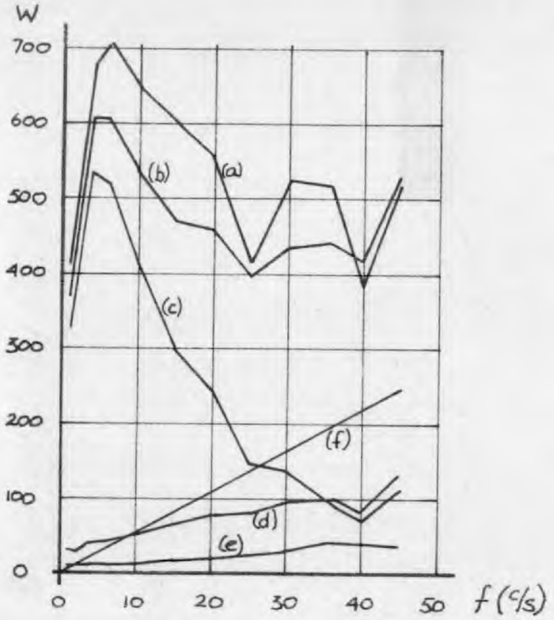
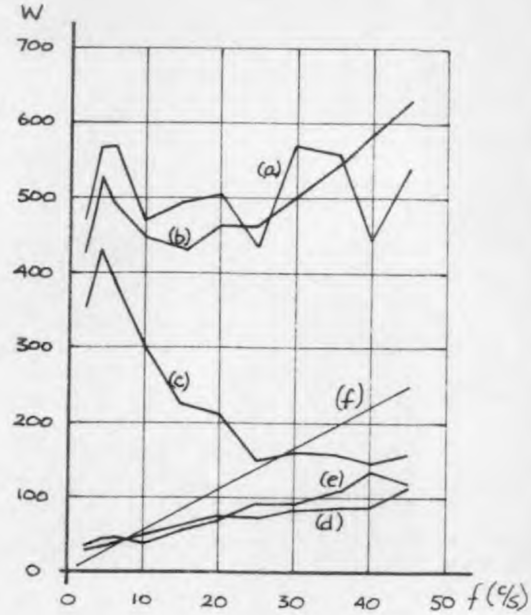


Fig. 7.11: Variation with frequency of rms line-to-line motor voltage, V_ℓ, motor line current, I_ℓ, and motor input power, W_i.

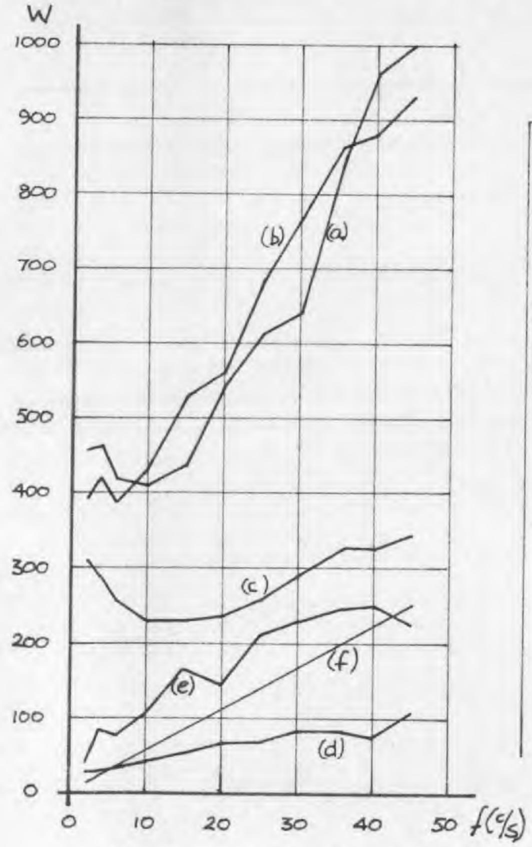
(Figures in brackets indicate approximate motor torque in lb-ft. for each curve.)



(a) Motor torque ≙ 6 lb-ft.



(b) Motor torque ≙ 12 lb-ft.



(c) Motor torque ≙ 18 lb-ft.

Fig. 7.12 : Variation with frequency of motor power loss and its components for several load conditions.

(a) Measured power loss P_{mx}
(b) Estimated power loss P_{mx}
(c) Estimated primary copper loss
(d) Estimated primary iron losses
(e) Estimated secondary copper losses
(f) Estimated friction and windage losses.

(b) Primary iron losses. These have been calculated as $\frac{V_\ell^2}{2f}$ since the core loss resistance in the motor equivalent circuit was found to be approximately $2\,\Omega$ per phase per cycle per second.

(c) Friction and windage losses. These have been assumed proportional to frequency and were measured as 280 W at 50 $^c/s$.

(d) Secondary copper losses. These have been assumed to be equal to the per-unit slip multiplied by the total mechanical output power, i.e. the sum of the estimated friction and windage losses and the power dissipated in the brake.

Losses in the leads to the motor have been neglected. In calculating the primary iron losses it has been assumed that the components due to the harmonics present in the voltage waveform can be allowed for by using the r.m.s. value of voltage instead of the fundamental component of the voltage. Secondary iron losses have been ignored since the per unit slip was small at all except very low frequencies with full-load torque. The effective slip would not be small for any harmonic components of air gap flux, however, and some harmonic components of secondary iron loss have, therefore, also been ignored. Similarly, in calculating only the fundamental component of secondary copper loss the effect of harmonics upon the secondary current has also been ignored.

The measured and estimated values of power loss, P_{mx}, in the motor are seen to agree to within about 15%, in general. With such a large discrepancy between measured and estimated total power loss it is difficult to estimate the magnitudes of the losses which have been ignored. In the diagram drawn for full-load torque, however, it is seen that the total of the estimated power losses is mostly greater than the measured power loss. This would suggest that the ignored losses would not be substantial.

Fig. 7.13 shows how the motor efficiency varied with frequency. At low frequencies the motor was very inefficient, delivering little output power compared with the power lost in the motor. As the frequency was increased the efficiency improved and in general the higher the output power the higher the motor efficiency. Above 35 $^c/s.$, however, it was found that the motor efficiency at full-load torque was less than that at two thirds of full-load torque. This was due to the doubling of the primary and secondary copper losses resulting from the expected 50% increases in primary current and slip above two thirds full load.

The efficiency of the motor at full-load torque was found to be of the order of 75% from 30 $^c/s.$ upwards. It was found that to produce full-load torque motor currents of approximately 34 A and slip speeds of about 110 r.p.m. were required. The equivalent ratings given for the motor were 28 A and 80 r.p.m. The reasons for the increase in current and slip are that the fundamental component of the motor voltage was lower than rated and that the motor current contained harmonics. The larger current would account for a 50% increase in primary copper losses above the rated value and the larger slip would account for a 40% increase in secondary copper losses above the rated value. Together, these increased copper losses account for most of the difference between the 84% rated efficiency and 75% measured efficiency.

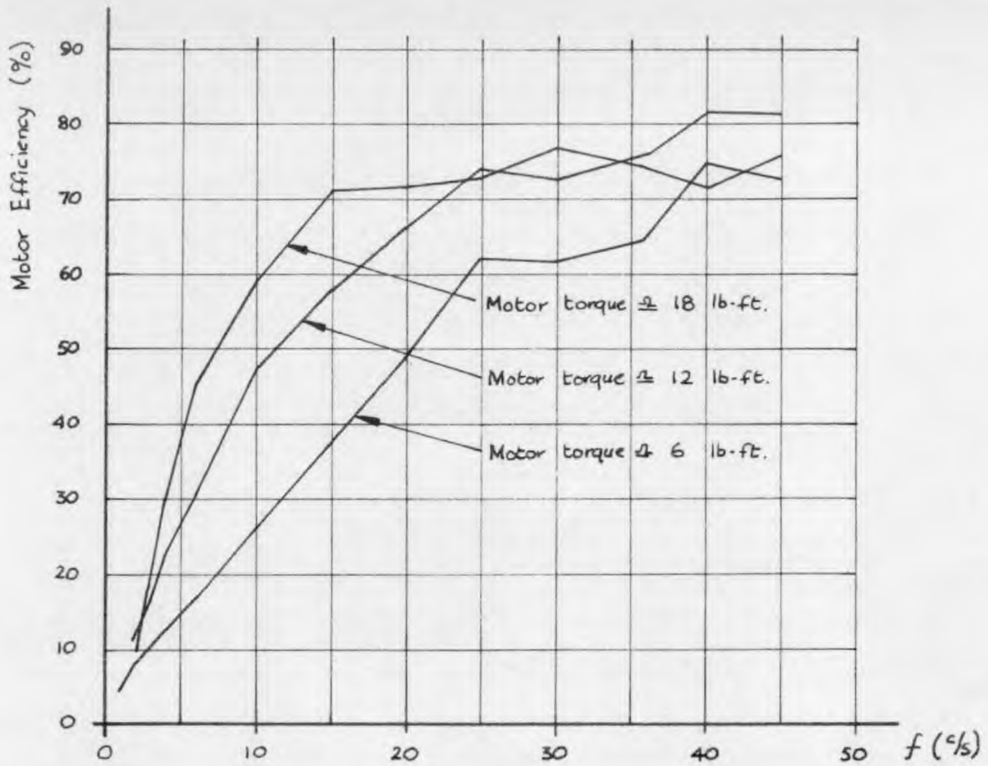


Fig. 7.13: Variation of motor efficiency with frequency for several load conditions.

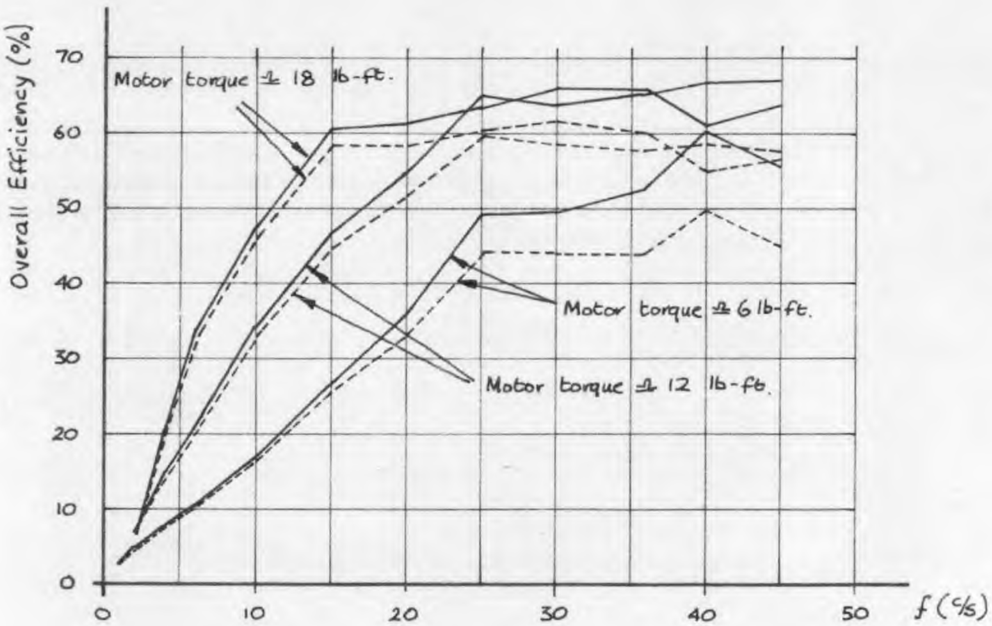


Fig. 7.14: Variation of overall inverter-motor efficiency with frequency for several motor load conditions.

——————— auxiliary supply power ignored

- - - - - - - - - - auxiliary supply power taken into account.

7.7. Variation with Frequency and Load of Efficiency of Inverter-Motor Combination.

Fig. 7.14 shows how the overall efficiency of the inverter-motor combination varied with frequency. One set of curves shows the efficiency when the auxiliary supply power is ignored, the other the true efficiency which takes into account all the power supplied to the circuit. The efficiency of the overall system is simply the product of the individual efficiencies of the inverter and motor and is seen to vary accordingly. The efficiency was very low at very low frequencies because of the low motor efficiency. On increasing the frequency the efficiency improved until a peak of about 61% was reached whereupon it began to fall off. The motor efficiency displayed a tendency to continue rising with frequency but this tendency was countered by the falling-off of inverter efficiency when the commutation power loss became serious above approximately 30 $^{c}/s$.

Both motor and inverter efficiencies suffered at frequencies lower than about 25 $^{c}/s$. from the high motor current, and hence inverter current, required to produce a given motor torque. Surprisingly, this current fell as the motor load was increased. It was suggested in section 7.4 that in each sixth of a cycle the motor would produce torque in three different ways. Firstly, at the beginning of each sixth of a cycle, immediately after commutation the air gap flux would rotate while the current in one phase decayed to zero. This would produce a positive torque in the rotor by virtue of relative speed between flux and rotor windings. Secondly, when the current in the one phase had fallen to zero the current in the other two phases would increase exponentially towards some final value which depends upon the resistance of the primary windings. This would produce an increasing but stationary air gap flux which would induce current in the secondary and produce another positive torque by the principle of the single phase induction motor. Then for the remainder of the sixth of a cycle the rotor would be turning relative to a stationary and constant or slowly increasing flux and a braking torque would be developed. The magnitudes of the first two torques would depend upon the rate at which flux could be increased in the air gap, the third would be constant for a given rotor speed. Hence to overcome the braking torque it would be possible to increase the first two torques by increasing the voltage applied to the motor and hence the rate of change of air gap flux. This would also result in a large motor current drawn from the supply.

The length of the first two periods would be a function of the motor's electrical time constant which would be lower than normal because of the additional resistance in the inverter circuit. The longer the time constant, compared with the duration of a sixth of a cycle, the shorter the time during which braking torque is developed. Hence as the frequency is increased the necessity for quickly saturating the motor iron eventually ceases and the resulting motor current falls. A similar effect can be obtained by increasing the motor time constant which occurs in effect when the slip increases on load and the effective secondary resistance is decreased. This is suggested as the reason for the fall in motor current with increase in load at low frequencies.

7.8. Waveforms and Harmonic Content of Motor Voltage and Current.

Figs. 7.15 and 7.16 are oscillograms of the motor voltage and current corresponding to no-load and approximately three quarters of full-load torque. The oscillograms were taken at an inverter output frequency of 25 $^c/s$. and a main d.c. supply voltage of 80 V but are typical of the waveforms observed at all except very low frequencies.

Table 7.1 gives the r.m.s. values of the harmonic components and total waveforms of current and voltage for both load conditions together with the harmonic impedance per phase.

Motor Torque	Harmonic	1	5	7	11	13	17	Total R.M.S. values
Zero	Voltage (V)	61	16.8	4.6	7.2	1.9	4.7	64
	Current (A)	17.9	8.95	2.69	2.5	0.81	0.98	20.4
	Impedance (Ω)	1.97	1.08	0.99	1.69	1.36	2.77	--
14 lb-ft Torque	Voltage (V)	53.8	13.2	7.95	9.3	4.5	5.6	57.3
	Current (A)	21.5	6.72	2.91	2.24	0.94	0.94	23.0
	Impedance (Ω)	1.45	1.13	1.57	2.4	2.76	3.44	--

Table 7.1 : Harmonic components of motor voltage and current and harmonic impedances for no-load and three quarters full-load torque

$f = 25\ ^c/s.\quad V_d = 80$ V.

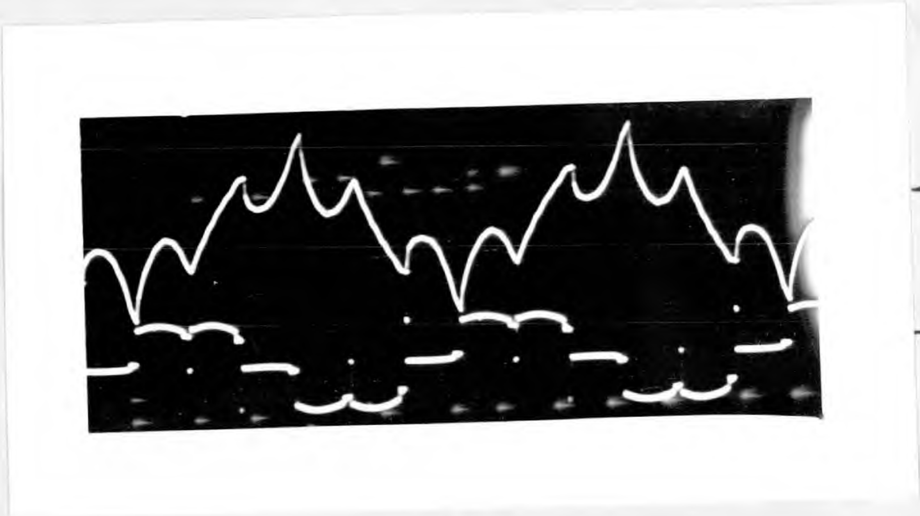


Fig. 7. 15 : Waveforms of motor current and line voltage at no-load.

V_d = 80v ; f = 25 c/s

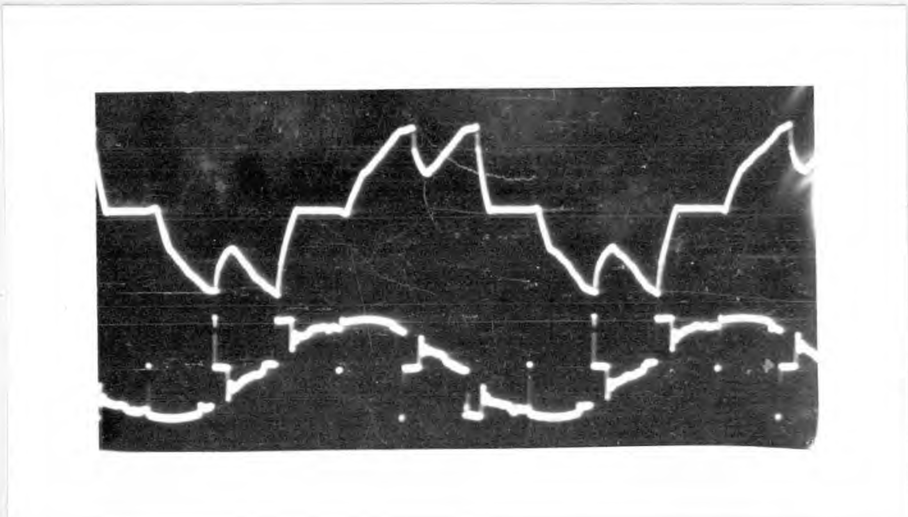


Fig. 7.16 : Waveforms of motor current and line voltage at approximately ¾ of full load torque.

V_d = 80v ; f = 25 c/s

It is seen from Fig. 7.15 that the motor current at no-load was quite unlike anything predicted or measured with a simple R-L load with passive elements. The peaky nature of the waveform is an indication that the motor iron was saturated and the concave outwards shape of the current waveform indicates mutual coupling between the motor phases and/or the effect of rotational voltages generated by the motor. It is also seen that the current reverses direction in the course of a sixth of a cycle at the end of each half cycle. It was shown in section 5.4 that this is quite normal when the load power factor is very low. From this waveform it must be concluded that it is not possible to predict the waveform of motor current and voltage by regarding the motor simply as a combination of resistance and inductance with no mutual coupling between the inductances in the three phases, and with no account being taken of the effect of the rotation of the machine or saturation of the iron.

The voltage waveform appears in Fig. 7.15 to be very similar to that which would be obtained with a highly inductive series R-L load. With such a load, as was shown in section 5.4., the voltage across the load must always be $\pm V_d$ or zero, even during the commutation periods, because the diode carrying the current in the phase not being fed from an S C R conducts throughout the whole of the sixth of a cycle. The small changes from $\pm V_d$ or zero towards the end of the sixth of a cycle are caused by the cessation of conduction of diodes D_7 and D_8 and the resulting voltage drop across the d.c. choke.

When the motor was loaded the voltage and current waveforms changed considerably. The current waveform became rather more like that observed for a simple R-L load but the voltage waveform became less so. In this case, after the reverse diode bridge had ceased condution, the voltage waveform approximated to a sine-wave due to the presence of a rotational voltage in each phase of the motor.

From Table 7.1 it is seen that the voltage harmonics were of the order that would be expected in an R-L load with a value of u of about 60° (see Fig. 5.37) when the motor was unloaded. The harmonic impedance per phase did not change with harmonic number in a uniform manner and neither, therefore, did the current harmonics. This was perhaps due to saturation of the motor iron. On load the magnitudes of the harmonics were quite different from their equivalents for no-load but in this case the harmonic impedances, apart from the fundamental, were nearly proportional to the harmonic number. For all the harmonics except the fundamental the slip was high and the effective value of secondary resistance in the motor equivalent circuit would therefore be nearly constant. The harmonic impedance would then depend mainly upon the reactive component which would be proportional to frequency. For the fundamental component of voltage and current the slip would be small and the impedance dependent mainly upon the effective value of secondary resistance and the magnetising inductance and core-loss resistance.

It should also be noted from Table 7.1 that the r.m.s. values of voltage and current were higher than the fundamental components because of the presence of harmonics. On no load the r.m.s. voltage was 5% and the r.m.s. current 14% higher than the fundamental components. With a motor torque of 14 lb-ft. the increases were 7% in each case. On load this would mean that the primary copper losses and iron losses would each be increased by 14%. Taken together, with the other losses in the motor these increased losses would cause a drop in motor efficiency of about 2%. This would mean, however, that the motor needs to dissipate nearly 10% more thermal energy than that for which it was designed and would therefore run hotter than normal.

It can be assumed that almost all the power produced by the motor is due to the fundamental components of voltage and current, the higher harmonics merely increasing the total r.m.s. values. Taking 7% as a typical ratio of r.m.s. to fundamental component, this would mean a fall of about 14% in power factor from sinusoidal supply condition.

7.9. Regenerative Braking Characteristics.

A three-phase induction motor is capable of acting as an induction generator if it is driven at supersynchronous speeds and the air gap flux is rotated at synchronous speed. Provision must be made in the supply system for accepting power from the motor. Any normal three-phase sinusoidal supply system meets these requirements but a three-phase inverter using rectifiers is a different proposition. However, one of the characteristics of the inverter under discussion here is that it is capable of passing power in both directions.

To find whether the inverter was capable of maintaining the motor air gap flux and also accept power generated by the motor some tests were carried out and are briefly described.

7.9.1. Method of Testing.

The induction motor and test rig of a fellow-postgraduate student were used for the tests. This motor was slightly larger than the one on which all the other tests described were carried out and had the following principal ratings :-

Maker:-	E.D.D.C. Ltd.	
Output:-	7 H.P. at 1440 r.p.m.	
Rated Voltage:-	190 V	) with motor connected as used
Rated F.L.Current:-	22 A	) for tests to be described.

In its test rig the motor was coupled to a separately-excited d.c. generator whose armature was fed from a variable voltage d.c. supply. In this way the motor-generator combination could be made to run at any desired speed. The torque was measured by the dynamometer principle.

To reduce the current drawn by the motor the tests were carried out at a much reduced voltage. A frequency of 25 $^{c}/s$. was used, giving a synchronous speed of 750 r.p.m. For the first test the inverter supply voltage was kept constant at 50 V and measurements were made of motor torque, current, voltage, and power in various parts of the circuit for motor speeds from 200 r.p.m. up to a little beyond synchronous speed. The results of this test are shown in Fig. 7.17. The transition from motoring to braking was made smoothly without any special measures being taken but it was found that in the braking region the motor torque increased rapidly with speed and showed little sign of reaching a maximum value. The motor current also increased rapidly, together with the current flowing in the reverse diode bridge, and the test was stopped

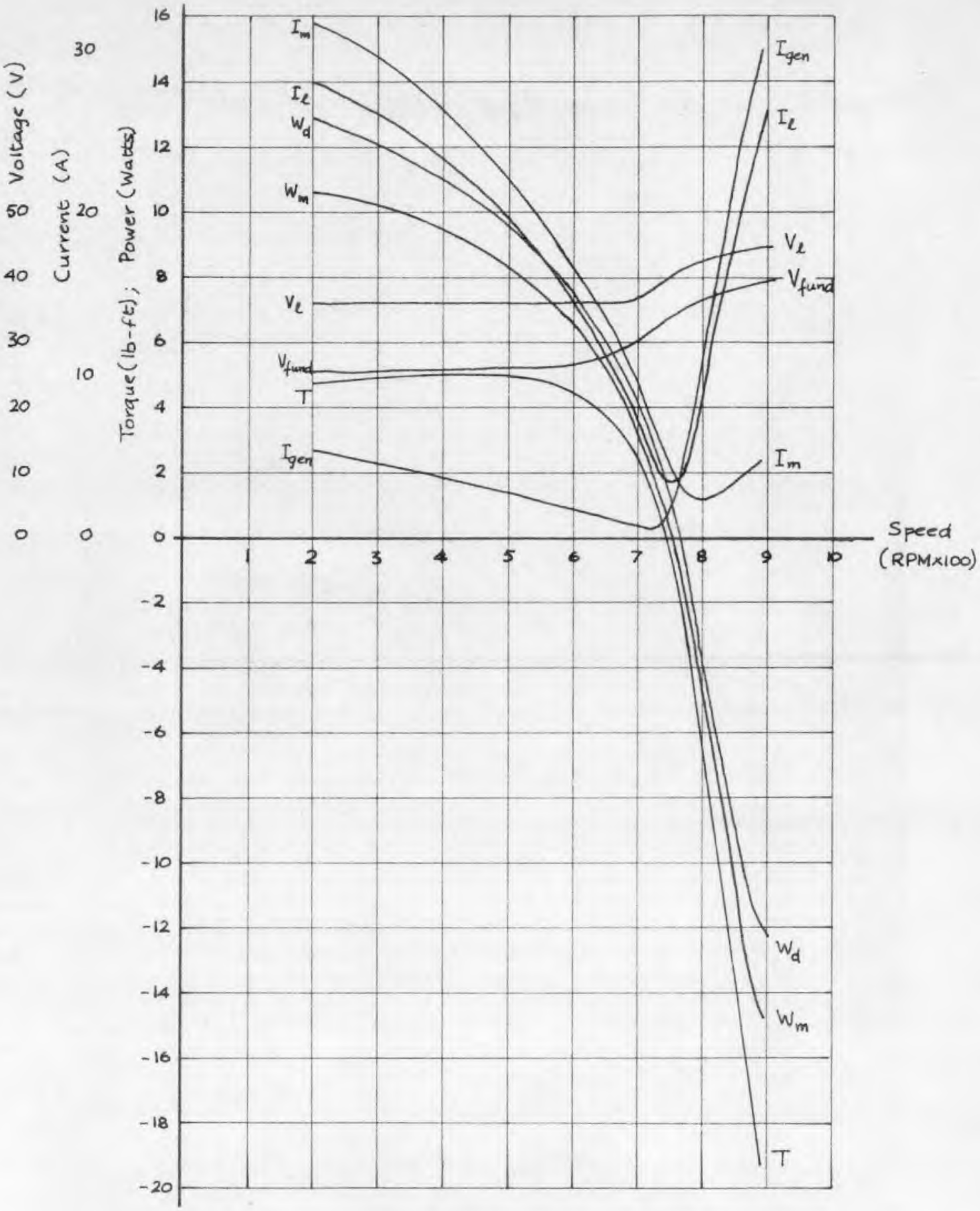


Fig. 7.17 : Variation with speed of motor torque T, and the currents, voltages and power in inverter and motor.

V_d constant at 50v; f = 25 c/s.

when the speed had been taken to 890 r.p.m.

The fact that the braking torque was much greater than the motoring peak torque was attributed to the higher values of motor voltage when braking and to the losses in the motor which at such low voltages were comparable with the mechanical power developed. A second test was therefore carried out in which the r.m.s. motor voltage was constant at 36 V. The results of this test are shown in Fig. 7.18. In this case the torque still increased rapidly with speed in the braking region but not as rapidly as when the motor voltage had been allowed to rise. However, the fundamental component of motor voltage still increased when the transition from motoring to braking was made and a third test was therefore carried out in which the fundamental component of motor line voltage was kept constant at 26 V. Fig. 7.19 shows the results of this test. The braking torque now showed a definite tendency to reach a maximum value but the test was stopped at a speed of 1100 rp.m. because the motor current had become excessive.

In all three tests the power, W_m, supplied to the motor during motoring was less than the power, W_d, taken from the d.c. supply, whilst in braking W_m was greater than W_d. This, of course, was because of the power loss incurred in the inverter. During motoring the S C R current, I_{in}, was greater than the reverse diode bridge current I_{gen} whilst in motoring I_{gen} was greater than I_{in}. This was because the total power passing through the inverter had reversed direction. It was, however, found that the value of I_{in} increased rapidly with speed in the braking region. This was attributed to the falling power factor and the

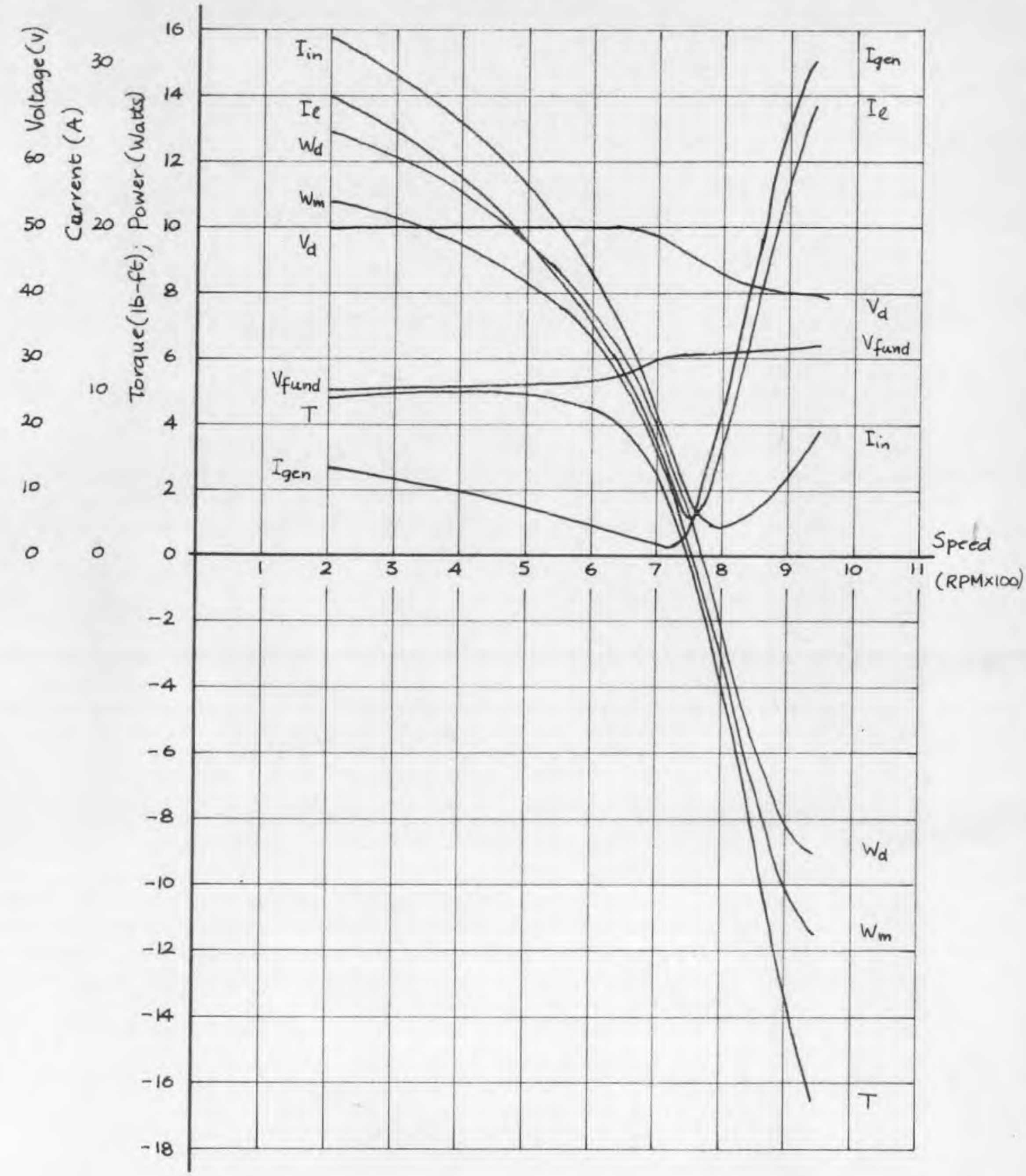


Fig. 7.18: Variation with speed of motor torque, T, and the currents, voltages and powers in the inverter and motor.

Inverter output line voltage's r.m.s. value kept constant at 36 V; $f = 25$ c/s.

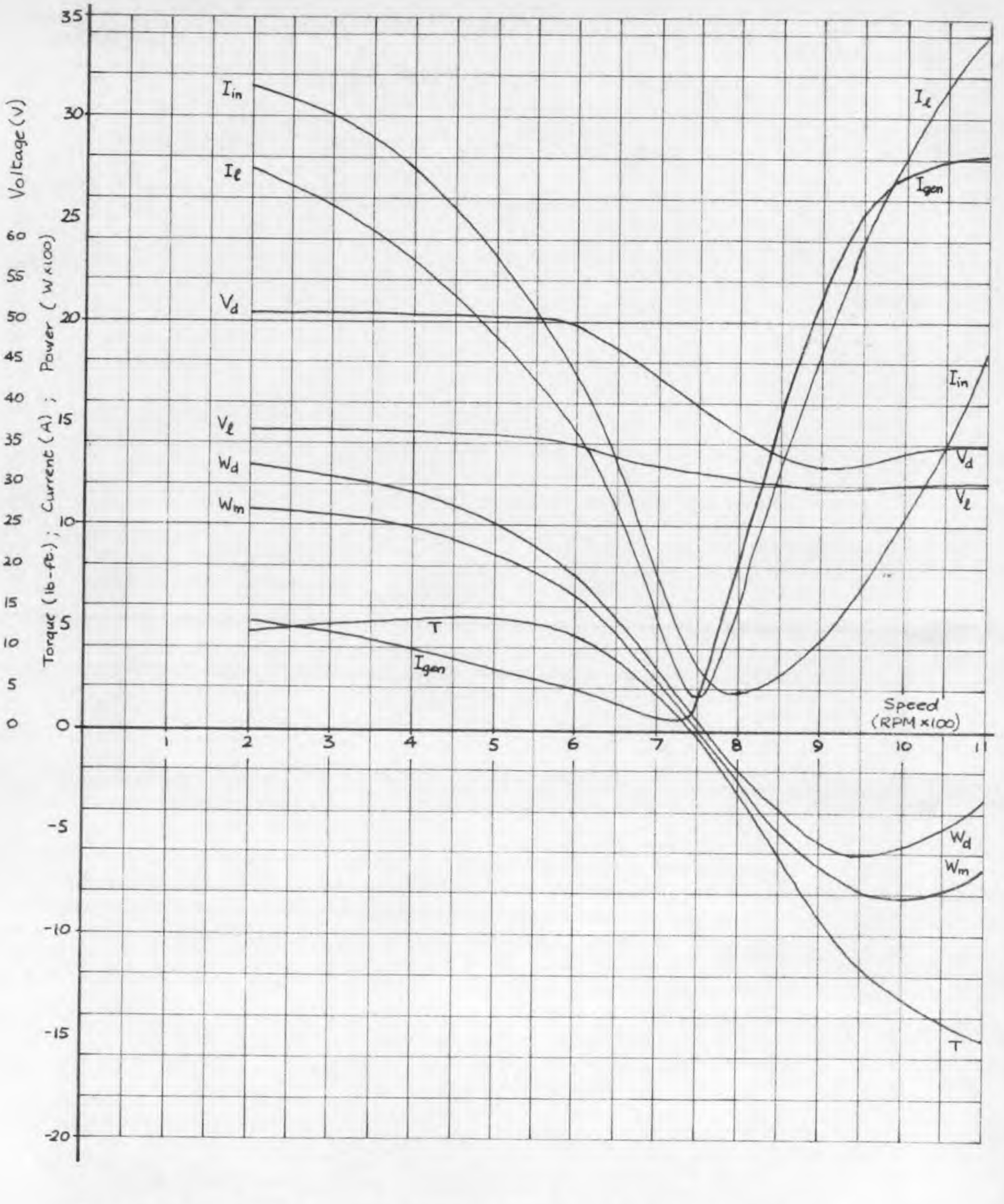


Fig: 7.19 : Variation with speed of motor torque, T, and the currents, voltages, and powers in the inverter and motor.

Fundamental component, V_{fund}, of inverter output line voltage kept constant at 26v ; $f = 25$ c/s.

resulting increase in the magnitude of power flowing in the direction opposite to that of the total power flow.

7.10. Variation with Load Power Factor of Supply Current and the Current in the S C R and Reverse Diode Bridges.

In section 5.8.1 approximate formulae were derived for estimating the current taken from the main d.c. supply and the mean current in the S C R and reverse diode bridges for a given load current and power factor. In Fig. 7.20 the accuracy of these formulae is checked by plotting adjusted measured values of I_d, I_{in}, and I_{gen} against load power factor. By "adjusted" is meant adding to the measured value of I_{gen_p} and subtracting from the measured values of I_d an amount equal to $\frac{cx}{V_d}$ for each set of values. The values were measured under widely varying load and frequency conditions with the induction motor as the inverter load.

It is seen in Fig. 7.20 that the general forms of the variations in I_d, I_{in} and I_{gen} conform quite well with those predicted shown by the dotted lines. Hence it may be assumed that the formulae given in equations (5.106), (5.107) and (5.108) give reasonable estimates of the distribution of current in the inverter circuit for any given load.

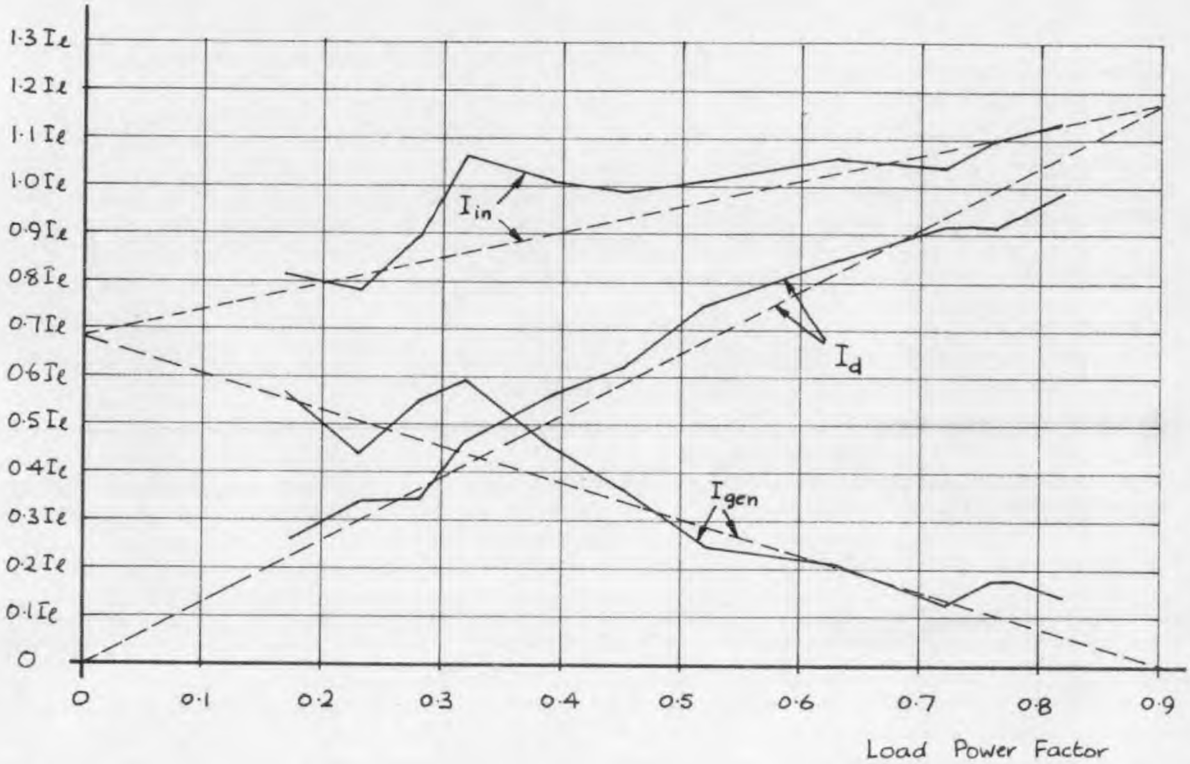


Fig. 7. 20 : Measured and predicted variations of I_{in}, I_{gen}, and I_d with the load power factor.

Measured values:- ————————

Predicted values:- – – – – – – – – – –

(The measured values have been adjusted to take account of the circuit losses P_{cx}.)

7.11. Ratings of Main Circuit Components.

One of the objects of the investigation was to derive a basis on which to assess the rating necessary for the system components to insure continuous reliable operation. The ratings suggested in the following sub-section have been based upon the various results obtained during the investigation.

7.11.1. The Induction Motor.

It was found that the harmonic content of the inverter output voltage and current waveforms increased the r.m.s. values of the motor voltage and current required to produce rated motor output. It was estimated that at full load the r.m.s. voltage and current would be about 5% to 7% higher than rated. The motor efficiency would therefore fall by some 2% or 3% but the elctrical losses in the conductors and iron of the motor would increase by 10% to 14%. It is imperative that the motor should be capable of dissipating these additional losses. The motor power factor would be reduced by about 10% to 14% below that obtained using a sinusoidal supply.

7.11.2. S C Rs for Inverter Bridge.

To obtain a suitable current rating for the bridge S C Rs some knowledge of the worst operating conditions would be necessary. When the maximum load current likely to flow for any prolonged period, i.e. more than a few seconds, has been determined the S C Rs should be chosen so that they can handle this current without overheating. Unless the motor overload is known to occur with a very low power factor the ratio of I_{in} to I_ℓ should be taken as 1.2. If the worst operating conditions are determined assuming a sinusoidal supply, about 7% should be added to the motor current value so obtained to allow for the inevitable harmonics caused by the inverter.

The mean current flowing in each bridge S C R is $\frac{I_{in}}{3}$ and this should be the basis for the S C R rating, i.e. an S C R mean current of 0.4 x maximum expected I_ℓ .

The voltage rating of the S C Rs depends upon the main and auxiliary d.c. supply voltages which in turn depend upon the required motor voltage. The r.m.s. motor voltage should be taken as 7% higher than that required when the supply is sinusoidal. Then the main d.c. supply voltage would be about 1.4 times the full load r.m.s. motor voltage. The maximum forward voltage on the S C Rs would then be little greater than the main d.c. supply voltage. During commutation the reverse voltage on the S C Rs is in theory a maximum of $\frac{1}{2}(V_d + V_{CR})$ but in practice the voltage would be about 50% greater, depending upon the measures taken (e.g. the use of selenium or other surge absorbing devices) to limit the voltage overshoots. V_{CR} would normally be at least twice as large as V_d and hence the voltage rating of the S C Rs would be at least 2.25 V_d allowing for 50% overshoot on reverse voltage.

7.11.3. Reverse Bridge Diodes.

The current I_{gen} has been shown to vary with the load power factor. On motoring, however, the maximum value of I_{gen} that was found to flow was about $0.6\ I_{\ell}$. Unless the maximum value of I_{ℓ} expected can be guaranteed at a high power factor the diodes should be rated on this basis. The mean current in each diode is one third of I_{gen} and hence for motoring only the diodes should be rated for $0.2 \times$ maximum I_{ℓ} expected.

If the motor is required to regenerate, the roles of the S C R bridge and diode bridge are to a large extent reversed, the diode bridge now carrying the bulk of the regenerated power. In this case the diodes should be rated as the S C Rs were, i.e. $0.4 \times$ maximum I_{ℓ} expected in regeneration.

The maximum voltage which should appear across the reverse bridge diodes is V_d but allowance must be made for some voltage overshoot.

7.11.4. Commutating Capacitor.

The value of C required depends upon V_d, V_{CR}, I_{do} and δ. For each value of V_d there would probably be a fixed value of V_{CR} and δ would remain almost constant. I_{do}, however, can itself vary with V_d, V_{CR}, C and f at the higher frequencies and hence a certain amount of trial and error is required using equations (5.98), (5.99) and (5.105). It should be remembered that these equations are simplified approximations and cannot be guaranteed accurate to better than about 10%.

Allowance should be made for the deviation in capacitor current from I_{do} during commutation (this depends on I_{do}, L_d, C, V_d and V_{CR}), for the effects of inductance in the circuits concerned in commutation, for the effects of hole storage in diodes (especially D_7 and D_8) and S C Rs, and for the dependence of the S C R turn off time on the current to be turned off, and on the reverse voltage applied to the S C R for turn off.

Care should be taken to ensure that the commutating capacitor is large enough to cope with the highest load currents anticipated. It is also important that the capacitor be designed to cope with the r.m.s. value of the current flowing into it during commutation and re-charging.

At low frequencies I_{do} may be assumed equal to the peak value of a sinewave having the same r.m.s. value as I_{ℓ}.

The voltage rating of the capacitor should be at least equal to the highest value of V_{CR} expected.

7.11.5. Choke Current Decay Diodes D_7 and D_8.

Equation (5.98) gives the current which can be expected to flow in these diodes at high frequency. The current depends upon V_d, V_{CR}, C and f and upon the effective resistance of the decay circuit. When load is taken from the inverter the current in the decay diodes falls but if no load operation at full circuit voltage is required, the diodes should be rated for the maximum current expected.

In theory the maximum reverse voltage which should appear across the decay diodes during commutation is $\frac{1}{2}(V_d + V_{CR})$ but voltage spikes must be allowed for and hence their voltage rating should be the same as the bridge S C R rating.

7.11.6. D.C. Series Choke.

The current rating of each half of the d.c. choke should be adequate for the highest expected I_{do}. The inductance of the choke is not critical provided that $\hat{I}$ is no more than 1.1 I_{do} to 1.2 I_{do} at the highest value of I_{do} to be catered for. If the inductance were too small, the capacitor current would increase significantly during the turn off period making necessary a larger commutating capacitor and increasing the commutation power loss.

7.11.7. S C R 7.

S C R 7 should be capable of passing the current which flows into the commutating capacitor during commutation. The mean value of this current is equal to 6 f $C(V_d + V_{CR})$ but it should be ensured that the S C R is capable of withstanding the r.m.s. value of this current.

S C R 7 should be rated for a voltage of $(V_d + V_{CR})$ plus overshoot.

7.11.8. S C R 8.

S C R 8 carries the same mean current as S C R 7 but the r.m.s. value of the current is different since S C R 7 passes rectangular pulses of current whereas S C R 8 passes a series of half sinewaves of current.

S C R 8 should be rated for a voltage of $(V_d + V_a)$ plus overshoot.

7.11.9. Inductance in Auxiliary Supply.

The commutating capacitor is re-charged between commutation periods. A definite time must be allowed after commutation for S C R 7 to recover its blocking properties, about 100 μSecs if the reverse voltage on S C R 7 is very small, before S C R 8 can be fired. The re-charging process must be complete and S C R 8 allowed time to recover before the next commutation can be allowed. Hence the re-charging half-sinewave should take no longer than about a twelfth of a cycle at the highest frequency of operation required. Thus $L_c < \frac{1}{144f^2\pi^2 C}$ for the maximum frequency f.

7.12. General Conclusions on the "D.C. Commutated Three Phase Inverter" with Simple R-L Load and Induction Motor Load.

Having studied theoretically and experimentally the three-phase inverter using auxiliary S C Rs and an auxiliary commutation supply some major conclusions may be reached.

The use of a diode bridge connected in opposite direction to the S C R bridge enabled the power supplied to the motor to flow in both directions through the inverter. The inductive stored energy was thus able to pass back to the main d.c. supply instead of being absorbed by the commutating capacitor as in the inverter circuit of Chapter 3. This also made it possible to use a single, relatively small, capacitor for commutation which could be charged to a fixed voltage prior to commutation and did not have to change for each new output frequency.

The commutation circuit was found to be very effective in turning off the bridge S C Rs and was independent of load power factor in its operation. It did, however, possess several very serious disadvantages. The energy absorbed by the capacitor during re-charging from the auxiliary supply was transferred during commutation, together with additional energy taken from the main supply, to the choke in the main d.c. lines. This energy had to be dissipated in the decay circuit connected to the choke between commutation periods. The resultant power loss increased with the supply voltage and with frequency and became very serious at frequencies above 25 $^{c}/s.$ or so when it became greater than all the other circuit losses. A secondary effect was that as the frequency was increased the current circulating in the choke and decay circuit increased, and hence the current flowing into the commutating capacitor at commutation was increased, reducing the time for which the S C Rs were reverse biased. It was found possible to reduce the rate of increase of I_{do} with frequency by increasing the choke resistance or adding resistance in the decay circuit but this was also found to introduce undesirable secondary effects. Some method of extracting the energy from the choke between commutation periods and returning it to one of the two d.c. supplies instead of dissipating it in the circuit would be a great step forward, and would increase the frequency up to which the circuit could be efficiently used. Some suggestions will be found in Chapter 9.

The methods developed for calculating the performance of the circuit on an R-L series load were found to give accurate results. The calculations were quite straightforward but laborious when many had to be carried out and would be better programmed on to a digital computer for which the calculation techniques were eminently suitable. The output voltage was found to change substantially with load but in a predictable manner and apart from resistance drops in the inverter circuit the change in output voltage was due entirely to change in waveform with load power factor.

The inverter was tested with an induction motor load but calculations of motor waveform were not attempted. It was found, however, that the harmonic content of the motor current and voltage waveforms increased the r.m.s. values by about 6% above the fundamental sinusoidal components on load. This caused the power factor to be about 12% lower than it would have been on a sinusoidal supply and reduced the motor efficiency by about 2%. The resulting 10% increase in the motor's electrical losses, however, meant that the motor would run hotter than normal unless specially designed for operation from the inverter or derated by about 10%.

At low frequencies the motor torque was found to pulsate severely but above 5 $^{c}/s$. the motor inertia damped out most of the torque pulsations.

Regenerative braking was found to take place automatically when the motor speed was made supersynchronous and power was then transferred from the motor to the supply through the reverse diode bridge, the S C R bridge merely maintaining the air gap flux and also coping with reverse power flow at low power factors.

Although no tests were carried out with any supply other than a pure d.c. supply taken from a generator there would appear to be no reason why the circuit would not function perfectly well from a rectified a.c. supply. Even a single phase rectified supply would be suitable provided that a reservoir capacitor were used to accept negative supply current for low power factors. V_{CR} would have to be large enough to cater for the fluctuation in V_d since $(V_{CR} - V_d)$ is the critical voltage for commutation. The harmonics introduced by the supply might have undesirable effects upon the motor but if the supply were taken through an L-C filter before the inverter input, such effects could no doubt be minimised. Regeneration would not be possible if the inverter were to be supplied by a rectifier unless provision could be made for inversion into the a.c. supply whenever necessary.

CHAPTER 8.

AN "A.C. COMMUTATED THREE PHASE INVERTER".

It was concluded that the"d.c. commutated inverter" had low efficiency at high frequency mainly as a result of the power losses caused by the commutation circuit used. All the energy taken by the commutating capacitor from the auxiliary supply and the energy taken from the main supply during commutation were transferred to the d.c. circuit choke and dissipated in the form of heat. These energies were high because it was necessary to charge the commutating capacitor to a voltage higher than that of the main d.c. supply to effect commutation. Another feature of the commutation circuit was that in the commutation period all S C Rs in the inverter bridge were reverse biased, not only the one S C R required to be turned off. As well as being unnecessary this forced the load current to fall when it should have been at its peak and resulted in an increased harmonic content of load current.

In an attempt to improve the performance of the inverter another form of cummutation circuit was developed and is described in this chapter, attention being concentrated upon the commutation process and the resulting power loss. It will be seen that the new commutation circuit is selective in that it turns off only the one S C R required and hence improves slightly the waveform and harmonic content of load current. More important, it will be seen that no auxiliary supply is required in this "a.c. commutated" inverter.

8.1. Circuit and Principle of Operation.

Fig. 8.1 shows the circuit of the inverter and the connections of the capacitors and S C Rs used for commutation. Each of the three identical capacitors is connected between a pair of output lines through a pair of S C Rs connected in inverse parallel. CR1, CR2,... CR6 form the inverter S C R bridge and D_1, D_2, .. D_6 the reverse diode bridge as before. CR1a, CR2a,...CR6a are so numbered because they are triggered by the same gate pulses as CR1, CR2,... CR6 respectively (though fed through separate isolating transformers). For this purpose the output circuits of the pulse generator were duplicated. The d.c. choke and diodes D_7 and D_8 are retained from the previous inverter circuit.

During operation each capacitor is charged to supply voltage in one direction or the other and this voltage is retained until one of the auxiliary S C Rs connected to it is fired. Fig. 8.2 shows the state of conduction of the circuit immediately after CR2 and CR2a have been fired at instant t_2. The capacitor connected between CR2 and CR6 was charged to supply voltage with the indicated polarity half a cycle earlier when CR5 and CR5a were fired. This time CR2 and CR2a are fired with the object of turning off CR6.

The L.H.S. of C cannot be at a lower potential than the negative supply terminal because diode D_6 conducts. Hence the distribution of potential around the circuit is as shown, with the positive and negative supply terminals taken to have potentials of +100 and -100 respectively. If a current I_{do} had been flowing in each half of the d.c. choke prior to instant t_2, a current, initially I_{ao}, now flows in the positive

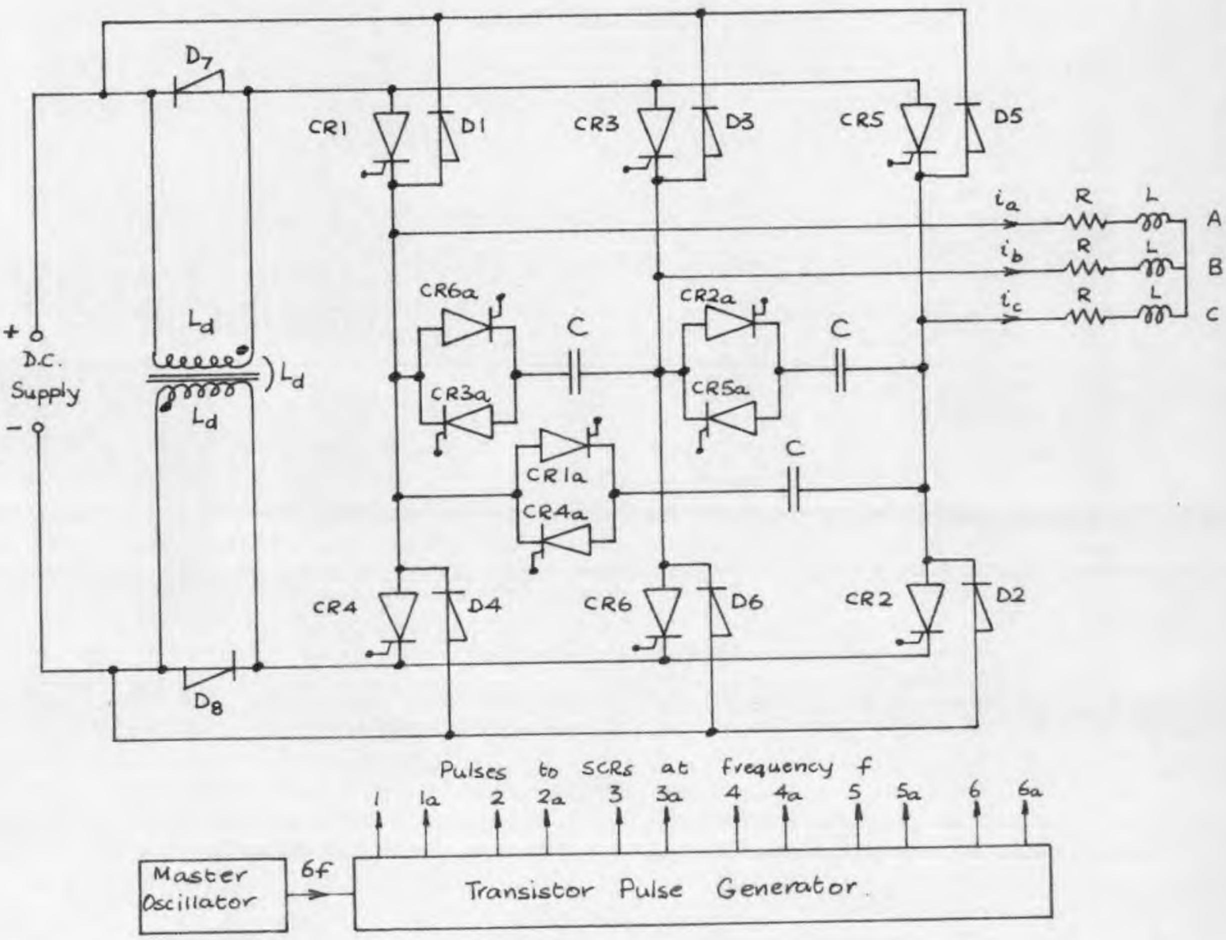


Fig. 8.1: Circuit for "a.c. commutated" three-phase inverter.

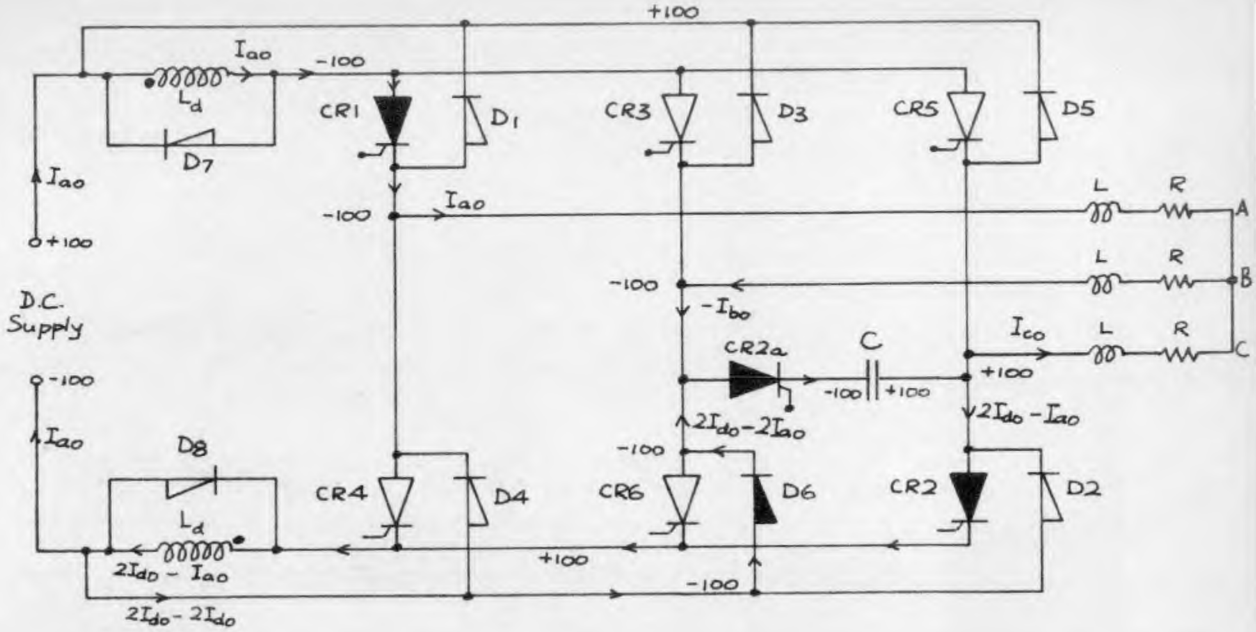
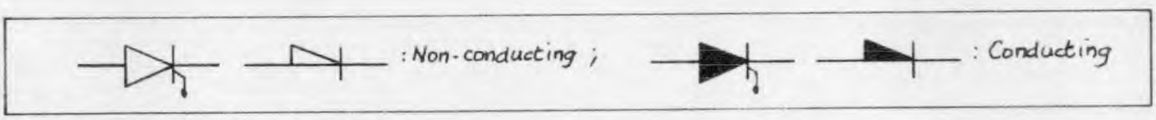


Fig. 8.2 : State of conduction of circuit immediately after the initiation of commutation at instant t_2.



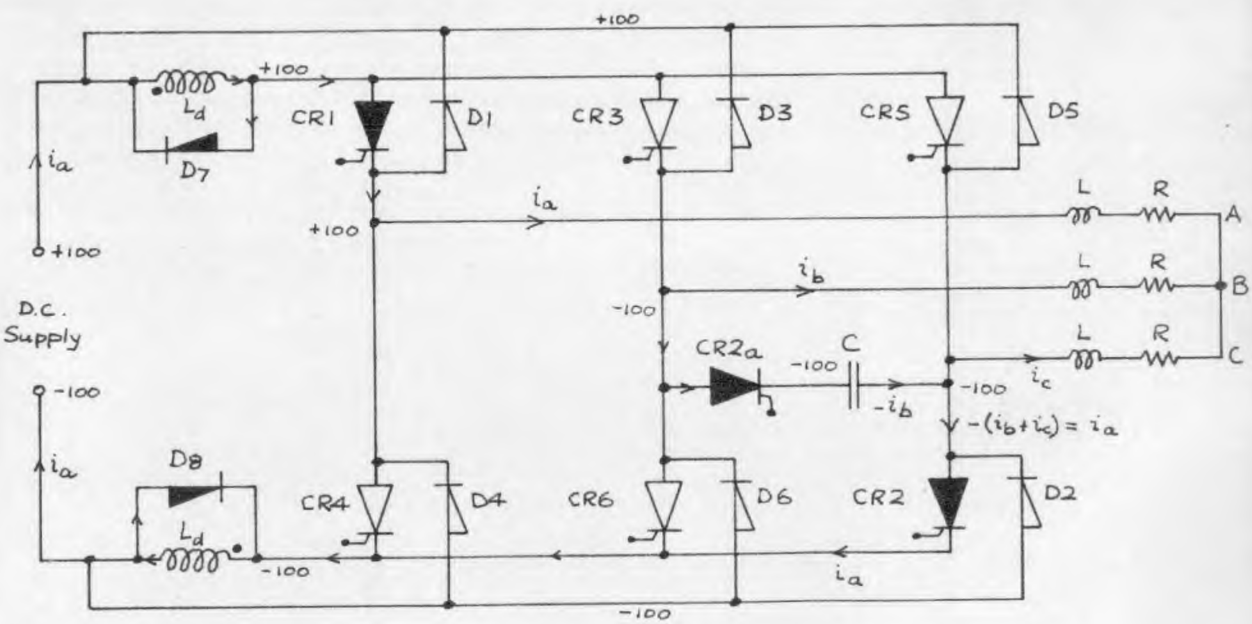


Fig. 8.3 : State of conduction of circuit immediately after the capacitor voltage reaches zero in the commutation period following instant t_2.

half and the remainder $2I_{do} - I_{ao}$ in the negative half. Since the supply current is I_{ao} initially a current $2I_{do} - 2I_{ao}$ must flow in diode D_6 and the current flowing into the capacitor must therefore be $2I_{do} - 2I_{ao} + I_{bo}$. The capacitor therefore charges with its L.H.S. becoming more positive with respect to its R.H.S. During the initial charging period it should be noted that the capacitor voltage appears across CR6, thus turning it off, and across the negative half of the d.c. choke, thus increasing the current and energy stored in the choke. By transformer action the same voltage appears across the positive half of the d.c. choke and this results in the voltage v_{ab} falling instantaneously to zero. However, the voltage v_{cb} is positive and causes an increase in i_c and $(-i_b)$ and hence the current flowing into the capacitor, both from the load and from the choke, increases during its initial charging.

When the capacitor voltage reaches zero the choke voltage also becomes zero and diodes D_7 and D_8 start to conduct. From this point the R.H.S. of the capacitor is held by CR2 at a potential of -100 and hence D_6 must cease conduction. This condition is shown in Fig. 8.3. The additional energy absorbed by the choke is now dissipated in diodes D_7 and D_8 and the choke plays no further part in the charging of the capacitor. The only current now flowing in the capacitor is that from phase B and hence the capacitor now charges at a slightly lower rate towards +100 on its L.H.S. CR6 now becomes forward biased but remains off provided that the time for which it was reverse biased by the capacitor was longer than its turn-off time.

Diode D_3 conducts when the capacitor voltage reaches supply voltage and thus prevents the capacitor from charging further. The capacitor current becomes zero, CR2a therefore turns off, and the current in phase B flows via D_3 to the supply. From this point to the end of the sixth of a cycle at instant t_3 the circuit behaves exactly as the d.c. commutated inverter, i.e. once commutation is complete both circuits are exactly the same. This is shown in Fig. 8.4. It should be noted that CR2 and D_2 have been shown as possibly conducting. Which of these two devices conducts depends upon the direction of current in phase C at the end of commutation. If i_c is +ve, according to the convention used, D_2 conducts. However, at some stage during the sixth of a cycle i_c must become negative, whereupon CR2 conducts for the remainder of the sixth of a cycle.

It should also be noted that the capacitor is now charged with the correct polarity for commutation at instant t_5 when CR5 and CR5a are fired to turn off CR3. Commutation takes place in exactly the same way at the beginning of every sixth of a cycle, one of the three capacitors being discharged through the appropriate auxiliary S C R and reversing its voltage ready for the commutation taking place half a cycle later.

8.2. Theory of Operation on R-L Load.

Unlike the d.c. commutated inverter the new inverter circuit is not very amenable to simple and accurate calculation during the period of discharge of the commutating capacitor. This is because the circuit cannot be split up into two distinct parts as before since the load is

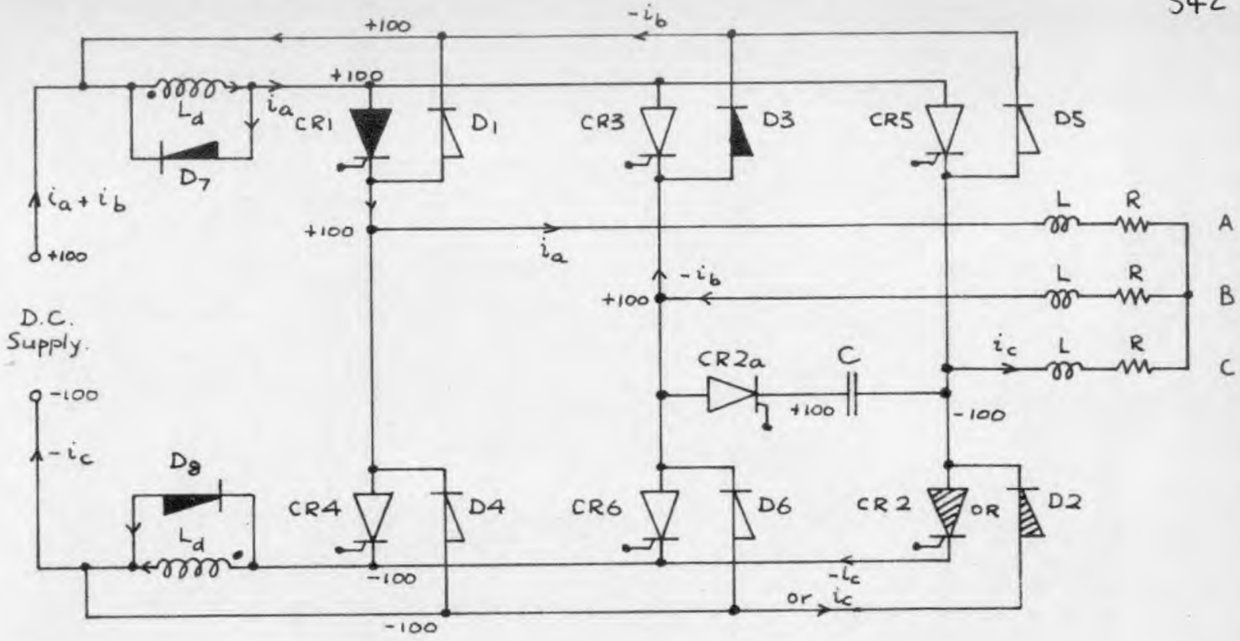


Fig. 8.4 : State of conduction of circuit after capacitor voltage has reached supply voltage in commutation period following instant t_2.

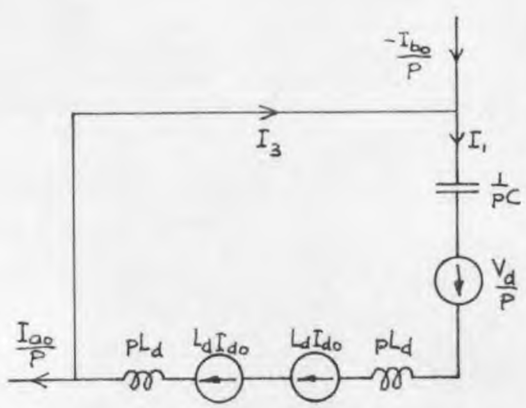


Fig. 8.5 : Operational circuit valid during period 1.

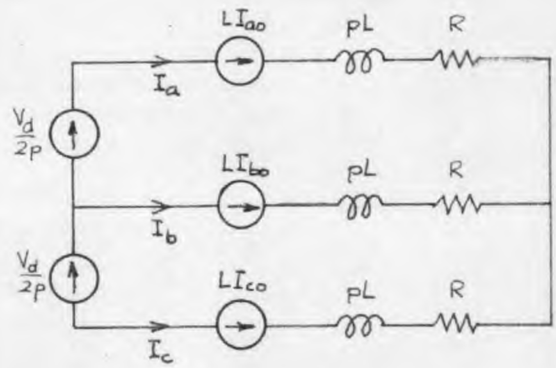


Fig. 8.6 : Operational circuit used for obtaining the current and voltage equations for period 2.

involved in the charging of the capacitor. An accurate calculation can certainly be carried out but this involves the solution of cubic equations in obtaining the solution of the differential equations and is therefore suitable only for numerical analysis and gives little indication of the general behaviour of the circuit. It is therefore proposed that some simplifying assumptions should be made in order to obtain relatively simple formulæ for the reverse-bias time δ for the turn off of S C Rs and for the increase in stored energy of the d.c. choke. These formulæ will in general give reasonably accurate results and it will be indicated how the assumptions made affect the accuracy.

8.2.1. Period 1 - Reverse Bias Time of S C R 6.

8.2.1.1. Assumptions made to simplify theory.

(a) S C Rs and diodes are considered ideal, i.e. zero forward voltage drop when conducting and infinite resistance when not conducting.

(b) All components inserted to limit voltage peaks, etc. are ignored.

(c) i_b remains constant at I_{bo}, i.e. its initial value at instant t_2.

(d) i_a is also assumed constant at I_{ao} and hence i_c at I_{co}.

(c) and (d) are valid assumptions provided that the changes in i_b and i_a are small compared with the actual values of I_{bo} and I_{ao}. The changes in i_a and i_b are small if the duration of period 1 is short compared with the load time constant. In fact, during period 1 i_a falls at first and then rises as the capacitor charges and the load voltage changes. i_c increases and then falls in a similar manner. The change in i_b is the sum of the changes in i_a and i_c and clearly these changes balance each other to some extent.

When i_a falls the current in the negative half of the choke must increase by the same amount. The effect of assuming i_a to remain constant, therefore, is that the calculated value of δ will be a little greater than it should be, the error depending upon the relative magnitudes of the change in i_a and the total current flowing into the capacitor. This error could be counteracted or enlarged by the assumption (c). However, the larger the values of I_{ao} and I_{bo} the more insignificant become the errors and it is when I_{ao} and I_{bo} are largest that an accurate calculation of δ becomes most important.

8.2.1.2. Current and voltage equations.

Fig. 8.5 shows the operational circuit which can be used to obtain the current and voltage equations during period 1. The values of i_a, i_b, i_c are shown as constants $\frac{I_{ao}}{p}$, $\frac{I_{bo}}{p}$, $\frac{I_{co}}{p}$. The initial values of current in the two halves of the d.c. choke are shown as I_{do}, If the load power factor is low, the currents in the two halves of the choke would probably not be equal at the end of each sixth of a cycle but if the mean is taken to be equal to I_{do} the same result will be obtained. I_1 is the current flowing into the capacitor, I_2 the current flowing in the negative half of the d.c. choke and I_3 the current in diode D_6. The initial voltage on the capacitor is V_d in the direction shown.

Considering the closed loop in the circuit

$$\frac{V_d}{p} + L_d I_{do} + MI_{do} = I_1 . pC + I_2 . pL_d + pMI_a \qquad (8.1)$$

Now $M = L_d$, I_a is assumed constant at $\frac{I_{ao}}{p}$, and $I_2 = I_1 - \frac{I_{co}}{p}$

$$\therefore \frac{V_d}{p} + L_d I_{do} + L_d I_{do} = I_1 . \frac{1}{pC} + (I_1 - \frac{I_{co}}{p}) pL_d + pM . \frac{I_{co}}{p}$$

$$\text{i.e. } I_1 = \frac{\frac{V_d}{L_d} + p(2I_{do} - 2I_{ao} - I_{bo})}{p^2 + \frac{1}{CL_d}} \quad \text{since } I_{co} = -(I_{ao} + I_{bo})$$

Inverting to obtain i_1 in terms of time, t,

where $\omega^2 = \frac{1}{CL_d}$,

$$\underline{\underline{i_1 = \hat{I} \cos(\omega t - \phi)}} \qquad \hat{I} = \sqrt{(2I_{do} - 2I_{ao} - I_{bo})^2 + (\frac{V_d}{\omega L_d})^2}$$

$$\text{and } \tan \phi = \frac{V_d}{\omega L_d (2I_{do} - 2I_{ao} - I_{bo})}$$

(8.2)

Hence v_c = voltage across capacitor

$$= - V_d + \frac{1}{C} \int_0^t \hat{I} \cos (\omega t - \phi)\, dt$$

$$\underline{\underline{= \frac{\hat{I}}{\omega C} \sin (\omega t - \phi)}} \qquad (8.3)$$

δ is the time for which the capacitor voltage is negative and hence

$$0 = \frac{\hat{I}}{C} \sin (\omega \delta - \phi)$$

i.e. $$\delta = \frac{1}{\omega} \tan^{-1} \frac{V_d}{\omega L_d(2I_{do} - 2I_{ao} - I_{bo})} \tag{8.4}$$

During period 1 the L.H.S. side of the capacitor is held by diode D_6 at a potential of $\frac{V_d}{2}$. Across each half of the d.c. choke appears the capacitor voltage.

Hence potential on output line A $= \frac{V_d}{2} + v_c$

" " " " B $= -\frac{V_d}{2}$ $\left[v_c \text{ being initially } - V_d . \right]$

" " " " C $= -\frac{V_d}{2} - v_c$

Hence $$v_{ab} = V_d + v_c = V_d + \frac{\hat{I}}{\omega C} \sin(\omega t - \phi) \tag{8.5}$$

$$v_{bc} = v_c = \frac{\hat{I}}{\omega C} \sin(\omega t - \phi) \tag{8.6}$$

$$v_{ca} = -V_d - 2v_c = -V_d - \frac{2\hat{I}}{\omega C} \sin(\omega t - \phi) \tag{8.7}$$

8.2.1.3. Approximate value of δ.

When I_{do}, I_{ao}, I_{bo} are large, $\tan \phi$ is small and ϕ is nearly equal to $\tan \phi$.

Then $\delta \simeq \frac{1}{\omega} \cdot \frac{V_d}{\omega L_d(2I_{do} - 2I_{ao} - I_{bo})}$

i.e. $$\delta \simeq \frac{CV_d}{2I_{do} - 2I_{ao} - I_{bo}} \quad \text{since } \omega^2 = \frac{1}{CL_d} \tag{8.8}$$

This expression is most accurate when the currents are high, which is the condition which must be allowed for in selecting the capacitor required.

Except at high frequencies, when the choke current becomes greater than the load current, the current in one half of the choke is I_{ao} and in the other half $(-I_{bo})$ immediately before commutation.

Hence $2I_{do} = I_{ao} - I_{bo}$ and then δ is given by

$$\delta \simeq \frac{CV_d}{-2I_{bo} - I_{ao}}$$

$$\simeq \frac{CV_d}{-I_{bo} + I_{co}} \quad \text{since } I_{co} = I_{ao} - I_{bo} \qquad (8.9)$$

At load power factors greater than about 0.5 I_{co} is zero. Then δ may be further simplified to

$$\delta \simeq \frac{CV_d}{-I_{bo}} \qquad (8.10)$$

All the above approximate formulae give values for δ which are higher than they should be. This is because it is assumed that the increase in current in the negative half of the d.c. choke is insignificant compared with the initial current flowing into the capacitor. When the currents are low the capacitor takes longer to charge, the volt-seconds applied to the choke are greater and the increase in choke current is therefore greater and more significant compared with the initial capacitor current.

8.2.1.4. Increase in stored energy of d.c. choke during period 1.

During period 1 the total current in the d.c.choke increases. At the end of period 1 diodes D_7 and D_8 conduct and the additional energy absorbed by the choke is then dissipated in the decay circuit formed by the choke and diodes. The additional energy absorbed by the choke is therefore lost.

An expression for the increase in choke stored energy can be obtained from the initial and final values of total choke current in period 1. The initial total current is $2I_{do}$, and the final total current is $(\hat{I} + I_{ao} - I_{co})$. The increase $\Delta\, EL_d$ in choke stored energy is therefore given by

$$\Delta\, EL_d = \tfrac{1}{2} L_d([\hat{I} + I_{ao} - I_{co}]^2 - 4\, I_{do}^{\;2}) \tag{8.11}$$

This expression can be simplified no further. An alternative expression for $\Delta\, EL_d$, offering more scope for simplification, may be obtained by finding the increase in stored energy from the instantaneous values of current in the choke and the voltage across it. During period 1 the total instantaneous current in the choke is $(\hat{I}\cos(\omega t-\phi)+I_{ao}-I_{co})$ and the voltage across the choke is $\frac{\hat{I}}{\omega C}\sin(\omega t-\phi)$. Then $\Delta\, EL_d$ is given by

$$\Delta\, EL_d = -\int_0^{\phi/\omega}\left[\hat{I}\cos(\omega t-\phi) + I_{ao} - I_{co}\right]\left[\frac{\hat{I}}{\omega C}\sin(\omega t-\phi)\right] dt$$

This reduces to

$$\Delta EL_d = \underline{\underline{\tfrac{1}{2} CV_d^2 + L_d(I_{ao} - I_{co})(2I_{do} - 2I_{ao} - I_{bo})(\sqrt{1 + \tan^2\phi} - 1)}}$$

$$\ldots(8.12)$$

If the currents in the circuit are large, $\tan\phi$ is small and then

$$\sqrt{1 + \tan^2\phi} \simeq 1 + \tfrac{1}{2}\tan^2\phi - \tfrac{1}{8}\tan^4\phi$$

Taking the first two terms only,

$$\Delta EL_d \simeq \tfrac{1}{2}CV_d^2 + L_d(I_{aO} - I_{co})(2I_{do} - 2I_{ao} - I_{bo})(\tfrac{1}{2}\tan^2\phi)$$

This simplifies to

$$\Delta EL_d \simeq \underline{\underline{\tfrac{1}{2}CV_d^2 \left(\frac{2I_{do}}{2I_{do}-2I_{ao}-I_{bo}}\right)}} \qquad (8.13)$$

At zero power factor $(-I_{bo})$ is equal to $2I_{ao}$ (see section 5.4.5).

Then $\Delta EL_d \simeq \tfrac{1}{2} CV_d^2 \cdot \dfrac{2I_{do}}{2I_{do}}$

i.e. $\underline{\underline{\Delta EL_d \simeq \tfrac{1}{2} CV_d^2}}$ (8.14)

At high power factors $(-I_{bo})$ is equal to I_{ao}.

$$\text{Then } \underline{\underline{\Delta EL_d \simeq \tfrac{1}{2} CV_d^2 \cdot \frac{2I_{do}}{2I_{do} - I_{ao}}}} \qquad (8.15)$$

In this case $2I_{do} = 2I_{ao}$ unless the commutation power loss is high enough to make I_{do} greater than I_{ao}.

Then $\Delta EL_d \triangleq \frac{1}{2} CV_d^{\,2} \cdot \frac{2I_{ao}}{I_{ao}}$

i.e. $\underline{\underline{\Delta EL_d \triangleq CV_d^{\,2}}}$ (8.16)

Hence the increase in stored energy of the choke depends upon the load and upon the frequency (if $2I_{do}$ is greater than the sum of I_{ao} and $(-I_{bo})$). The stored energy increase, however, varies only between $\frac{1}{2} CV_d^{\,2}$ and $CV_d^{\,2}$ and under most operating conditions would be nearer $CV_d^{\,2}$ than $\frac{1}{2} CV_d^{\,2}$.

8.2.1.5. Commutation power loss.

ΔEL_d is dissipated six times per cycle in the form of heat. The commutation power loss, P_{com}, is therefore given by

$$P_{com} = 6f\,\Delta EL_d$$

In worst case

$$\underline{\underline{P_{com} \triangleq 6f\,CV_d^{\,2}}} \qquad (8.17)$$

8.2.2. Period 2 - C charging from Zero Voltage to V_d.

During period 2 capacitor C charges from zero voltage with current flowing into it from phase B only. If the load inductance is small it is possible that the oscillatory charging of the capacitor reaches a peak voltage below the supply voltage. At this point the capacitor and phase B currents would become zero and CR2a would turn off. The capacitor would then remain at this voltage until the end of the sixth of a cycle when CR3 is fired. Since CR2a is triggered, like CR2, from instant t_2 to t_4, CR2a would conduct again at t_3 and the capacitor would complete its charging to supply voltage.

In general, provided that phase B has sufficient inductive energy for the capacitor to be charged to supply voltage in the first part of the prospective oscillation, the capacitor voltage would follow part of a damped oscillation. It would not be possible to find the duration of period 2 from the capacitor voltage equation except by numerical methods. It is proposed, therefore, that the capacitor voltage rise shall be assumed linear, which implies that i_b must be assumed constant at I_{bo} during period 2. However, by assuming that phase B is in effect connected to a potential mid-way between the potentials of the d.c. supply terminals the change in i_b during period 2 may be estimated.

These assumptions are only valid if the load inductive stored energy is high enough for C to charge to V_d during period 2 almost linearly. If the load is mainly resistive, the assumptions are not valid.

8.2.2.1. Current and voltage equations.

The duration, T_2, of period 2 is the time taken by capacitor C to charge from zero to supply voltage V_d with a current of I_{bo} flowing into it.

Hence $$T_2 \simeq \frac{CV_d}{I_{bo}} \tag{8.18}$$

Fig. 8.6 shows the operational circuit which it is assumed can be used to obtain the current and voltage equations during period 2. Phase B is shown connected to the mid-point of the supply so as to simulate the mean voltage across the capacitor during period 2.

From the closed loop including phases A and B,

$$\frac{V_d}{2p} + LI_{ao} - LI_{bo} = I_a(R + pL) - I_b(R + pL) \tag{8.19}$$

From the closed loop including phases A and C

$$\frac{V_d}{p} + LI_{ao} - LI_{co} = I_a(R + pL) - I_c(R + pL) \tag{8.20}$$

Putting $I_c = -(I_a + I_b)$ and $I_{co} = -(I_{ao} + I_{bo})$ in (8.20)

$$\frac{V_d}{p} + 2LI_{ao} + LI_{bo} = 2I_a(R + pL) + I_b(R + pL) \tag{8.21}$$

Eliminating I_a from (8.19) and (8.21)

$$I_b = \frac{I_{bo}}{p + \frac{R}{L}}$$

Hence

$$\underline{\underline{i_b = I_{bo}\, e^{-\frac{Rt}{L}}}} \tag{8.22}$$

Eliminating I_b from (8.19) and (8.21)

$$I_a = \frac{V_d}{2pL(p + \frac{R}{L})} + \frac{I_{ao}}{p + \frac{R}{L}}$$

Hence
$$\underline{i_a = \frac{V_d}{2R} - \left(\frac{V_d}{2R} - I_{ao}\right)e^{-\frac{Rt}{L}}} \qquad (8.23)$$

Hence
$$i_c = -(i_a + i_b)$$

i.e.
$$\underline{i_c = -\frac{V_d}{2R} + \left(I_{co} + \frac{V_d}{2R}\right)e^{-\frac{Rt}{L}}} \qquad (8.24)$$

The values I_{a2}, I_{b2}, I_{c2} of i_a, i_b, i_c at the end of period 2 may be found by putting $t = T_2$ in equations (8.23), (8.22) and (8.24) respectively.

A better approximation for T_2 may be obtained by equating the charges flowing into the capacitor and out of phase B during period 2, using equation (8.22) for i_b.

i.e.
$$CV_d = -\int_o^{T_2} i_b \, dt$$

$$= \frac{L}{R} I_{bo} \left(e^{-\frac{RT_2}{L}} - 1\right)$$

Hence
$$\underline{T_2 = -\frac{L}{R} \log_e \left(1 + \frac{CV_d R}{I_{bo} L}\right)} \qquad (8.25)$$

During period 2 phase A is connected by CR1 to the positive terminal of the d.c. supply and phase C by CR2 or D_2 to the negative terminal of the d.c. supply (D_7 and D_8 would be conducting during the period). Phase B is connected to the end of the capacitor which starts at the potential of the negative terminal and rises to the potential of the positive supply terminal in time T_2.

Hence

$$\underline{\underline{v_{ab} \doteq V_d\left(1 - \frac{t}{T_2}\right)}} \tag{8.26}$$

$$\underline{\underline{v_{bc} \doteq V_d \cdot \frac{t}{T_2}}} \tag{8.27}$$

$$\underline{\underline{v_{ca} = -V_d}} \tag{8.28}$$

8.2.3. Remainder of the Sixth of a Cycle.

At the end of period 2 the current in phase B decays through diode D_6 and the capacitor ceases to charge further, $CR2_a$ turning off. For the remainder of the sixth of a cycle ending at instant t_3, therefore, the currents and voltages vary in exactly the same way as in the d.c. commutated inverter, after the commutation period. The equations for current, voltage, etc. are therefore given in sections 5.3.4.2, 5.3.4.3 and 5.3.4.4. if I_{c2} is zero or section 5.4.2.2. if I_{c2} is not zero.

8.3. Tests with a Simple Series R-L Load.

8.3.1. Commutation.

Tests were carried out to find how the reverse-bias time δ of the turned off S.C.R. was dependent upon the supply voltage, size of commutating capacitor, the current being commutated, and the load.

8.3.1.1 Variation of δ with C and I_{bo}.

For this test the supply voltage was kept constant at 80 V and the load phase inductance constant at 1.85 m.H. The operating frequency was 25 $^{c}/s.$ and the inductance of the d.c. choke was constant at 0.5 m.H. per coil (self and mutual) throughout. Three values of commutating capacitor, C, were used and for each the current in the circuit was increased in steps by changing the load resistance. δ and I_{bo} were measured on an oscilloscope.

Fig. 8.7 shows the results of these tests. For each value of commutating capacitance two pairs of calculated curves are also shown. One pair is calculated using 80 V for the capacitor voltage at the start of commutation, the other pair is calculated for a "corrected" capacitor voltage. The "correction" takes account of the transfer of charge from the commutating capacitor at the start of commutation to 1μF capacitor connected across each S C R (to suppress troublesome voltage peaks) when the S C R voltages change abruptly.

At the operating frequency used it was found that the excess choke current had died away before commutation took place and that therefore $2I_{do}$ was equal to $I_{ao} + (-I_{bo})$. At the end of each sixth of a cycle current flowed in two phases only and it was also possible to take I_{ao} and $(-I_{bo})$ as being equal. The expressions for δ used in the calculation therefore simplified to

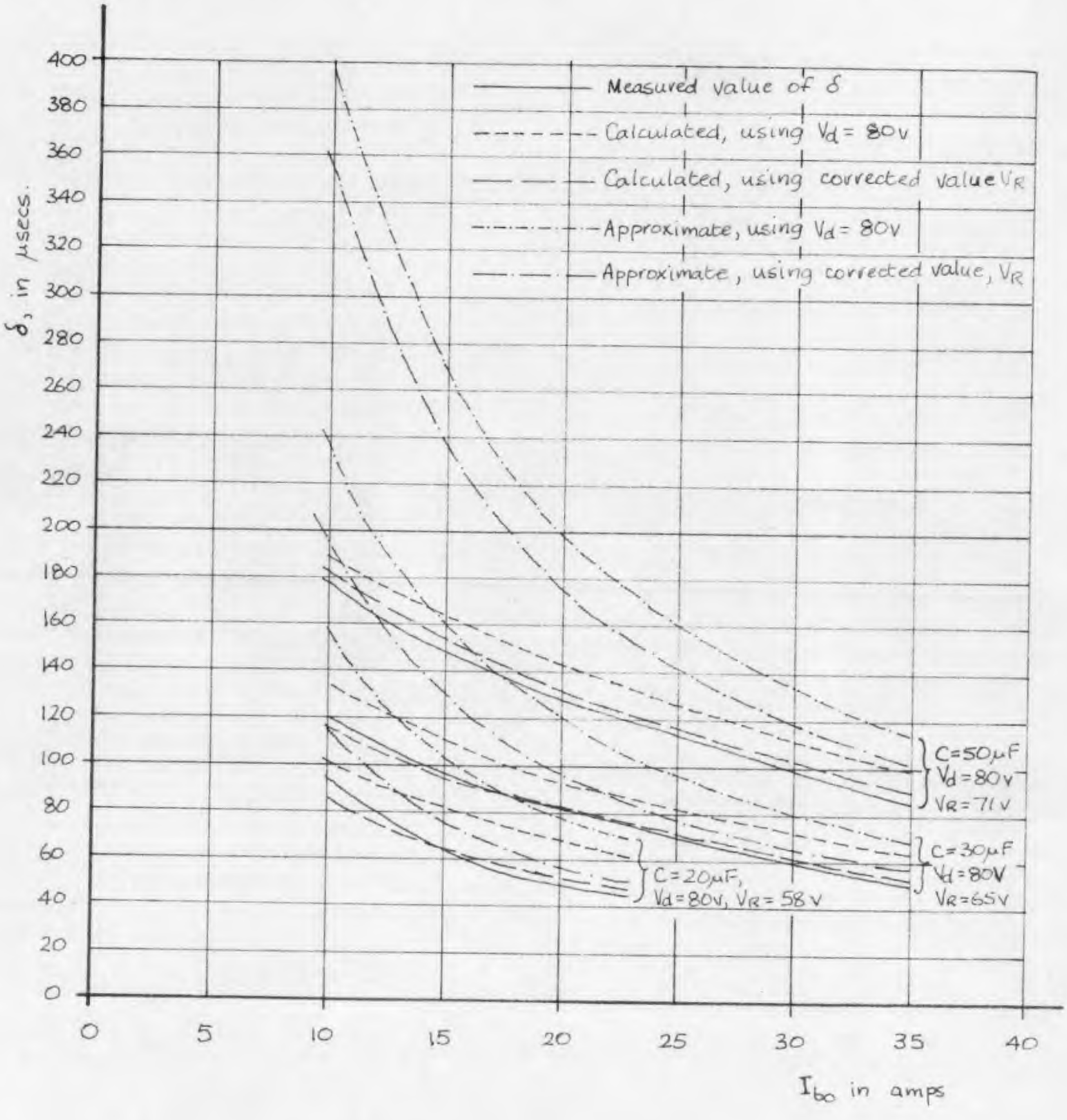


Fig. 8.7: Variation of δ with I_{bo} for several values of C.

$V_d = 80v$, $L_d = 0{\cdot}5$ mH, R varied, $L = 1{\cdot}85$ mH, $f = 25$ c/s

$$\delta = \frac{1}{\omega} \tan^{-1} \frac{V_d}{\omega L_d(-I_{bo})}$$

and $$\delta \simeq \frac{CV_d}{-I_{bo}}$$

The former equation has been used to obtain the results described as "calculated" in Fig.8.7, the latter used for the "approximate" results. The "corrected" voltage V_R appearing on the capacitor at the start of commutation is used by substituting it for V_d in the two equations.

It is seen that considerably better agreement between measured and calculated results was obtained when the "corrected" voltage was used. These results, however, would be expected to be still a little higher than measured because of S C R forward voltage drops , reverse current drawn from the turned-off S C R, etc.

The "approximate" results are seen to give useful predictions for δ at higher values of current, which is the condition for which the commutation circuit is designed. At lower currents, however, the approximate results are very far from accurate. This is because according to the approximate formula δ would vary inversely with I_{bo} whereas in practice even if I_{bo} were zero δ could be no greater than $\frac{\pi}{2\omega}$, i.e. $\frac{\pi}{2}\sqrt{C\ L_d}$.

It may be concluded from Fig. 8.7 that δ varies as predicted, approximately proportional to C at high currents and approximately proportional to $\sqrt{C}$ at low currents. It can also be concluded that δ becomes almost inversely proportional to I_{bo} when I_{bo} is large.

8.3.1.2. Effect upon δ of load inductance L.

To find what effect the load inductance had upon δ the inverter was operated with constant supply voltage and commutating capacitance at a frequency of 25 $^c/s$. For several different values of I_{bo} the load inductance was varied between 0.95 mH and 3.85 mH, adjusting the load resistance when necessary to keep I_{bo} constant.

Fig. 8.8 shows the results of this test. It is seen that L has virtually no effect upon δ which is to be expected as shown by the calculated results for each value of I_{bo}.

8.3.1.3. Variation of δ with supply voltage V_d.

For this test I_{bo} was kept constant at 20A by adjusting the load resistance with supply voltage. The load inductance, commutating capacitance and frequency were kept constant at 3.85 mH, 50 μF, and 25 $^c/s$. respectively.

Fig. 8.9 shows the results of this test. At low voltages the curves showing the calculated variation of δ with V_d tend towards becoming asymptotic with the lines showing the approximate variation of δ. This is because when V_d is small the capacitor energy is small and the increase in current flowing into the capacitor is small during the reverse voltage period. At large supply voltages, however, δ seems to tend towards a steady value. In this case the steady value should be $\frac{\pi}{2}\sqrt{L_dC}$ i.e. 248 μSecs since δ can never be greater than $\frac{1}{\omega}\tan^{-1}\infty$.

The predicted values agree favourably with the measured values of δ

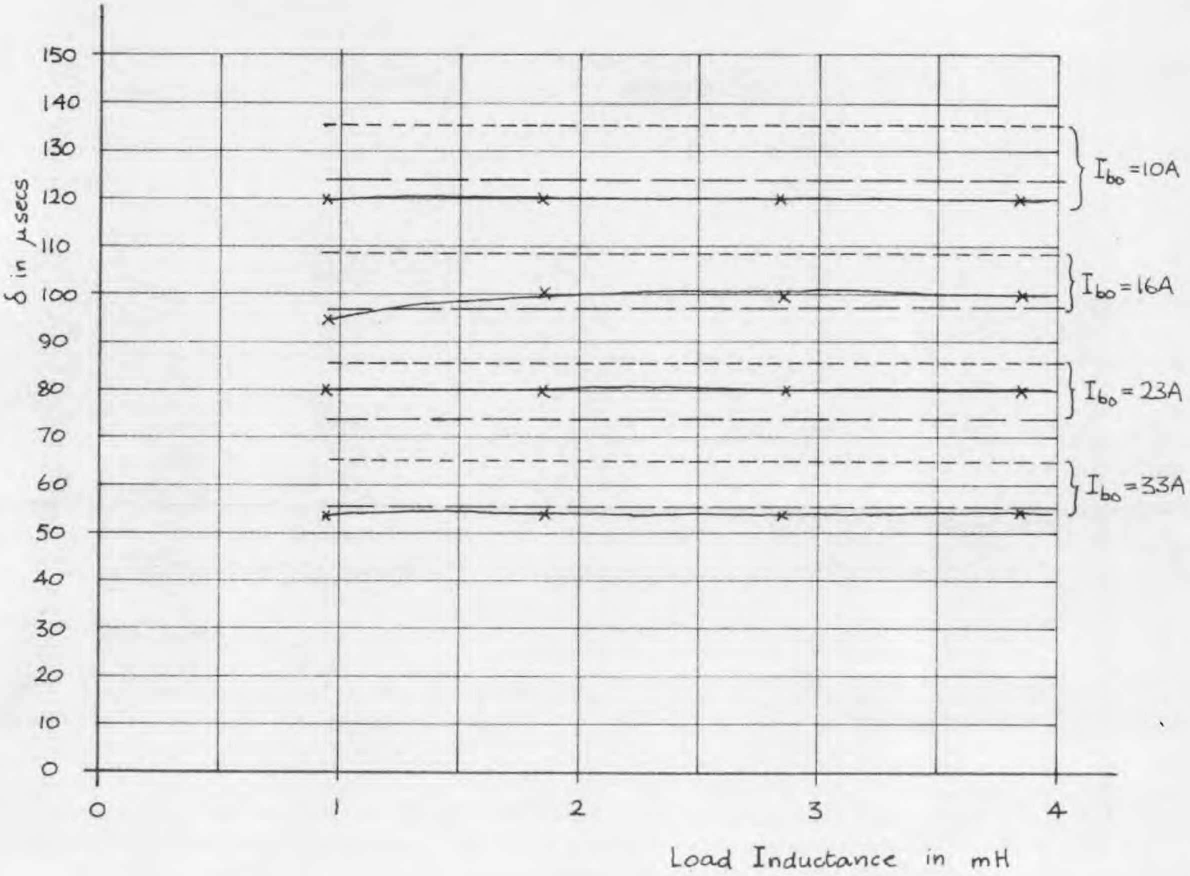


Fig. 8.8 : Variation of δ with load inductance for several values of I_{bo}.

$V_d = 80v$, $L_d = 0{\cdot}5mH$, $C = 30\mu F$, R varied, $f = 25$ c/s.

——————— Measured values of δ

- - - - - - - - - Calculated, using $V_d = 80v$

— — — Calculated, using $V_R = 65v$ ("corrected" value)

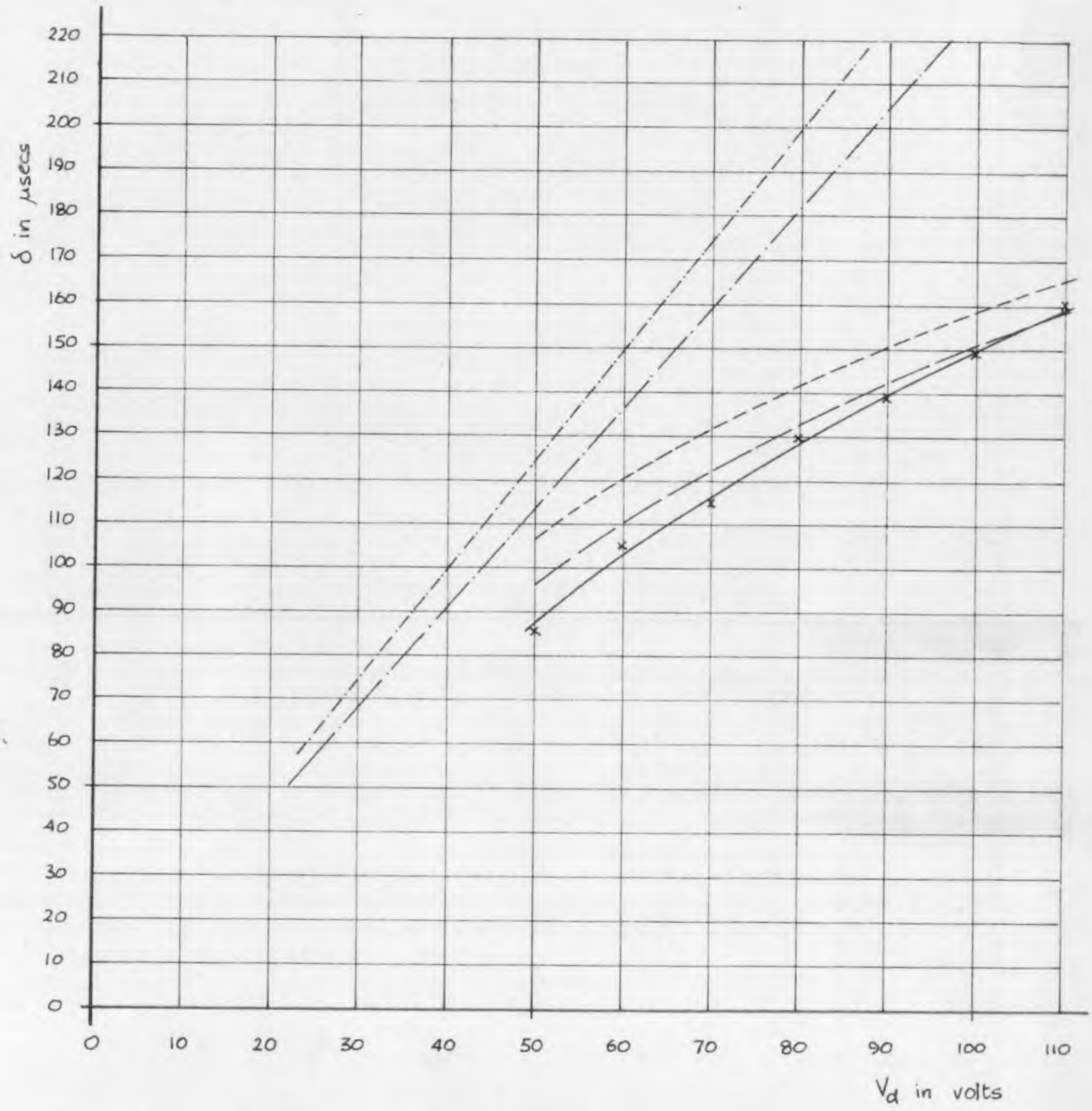


Fig. 8.9: Variation of δ with V_d.

$L_d = 0{\cdot}5\,mH$, $C = 50\,\mu F$, $L = 3{\cdot}85\,mH$, $I_{bo} = 20A$, $f = 25\,c/s$

———————— Measured values of δ

- - - - - - - - - - - Calculated, using V_d = value indicated

— — — — Calculated, using "corrected" value V_R

—·—·—·—·—·— Approximate, using indicated V_d

——·——·——·— Approximate, using "corrected" value V_R

especially those based on the "corrected" capacitor voltage. The remaining discrepancy between prediction and measurement can be attributed to the S C R reverse current at turn-off, circuit resistance, leakage of capacitor voltage through the auxiliary S C Rs during the half cycles between commutations, and to the assumptions made in deriving the expressions for δ.

8.3.2. Period 2 - charging of Capacitor to Supply Voltage.

For the reasons given in section 8.2.2 the duration of period 2 is difficult to predict with a high degree of precision. The tests to be described below were carried out to determine the validity of the rather limited theory developed in section 8.2.2.

8.3.2.1. Variation of T_2 with C and I_{bo}.

The test conditions were as described in section 8.3.1.1 and the results are shown in Fig. 8.10.

In general it is seen that the predicted values of T_2 are lower than those measured. This indicates that the fall in $(-i_b)$ during period 2 is, in general, greater than is allowed for in equations (8.18) and (8.25). It was observed, however, that the commutating capacitor did in fact charge to a voltage slightly higher than supply voltage, this being attributed to the inductance of the d.c. circuit of the reverse diode bridge. This would also account in part for the higher measured values of T_2.

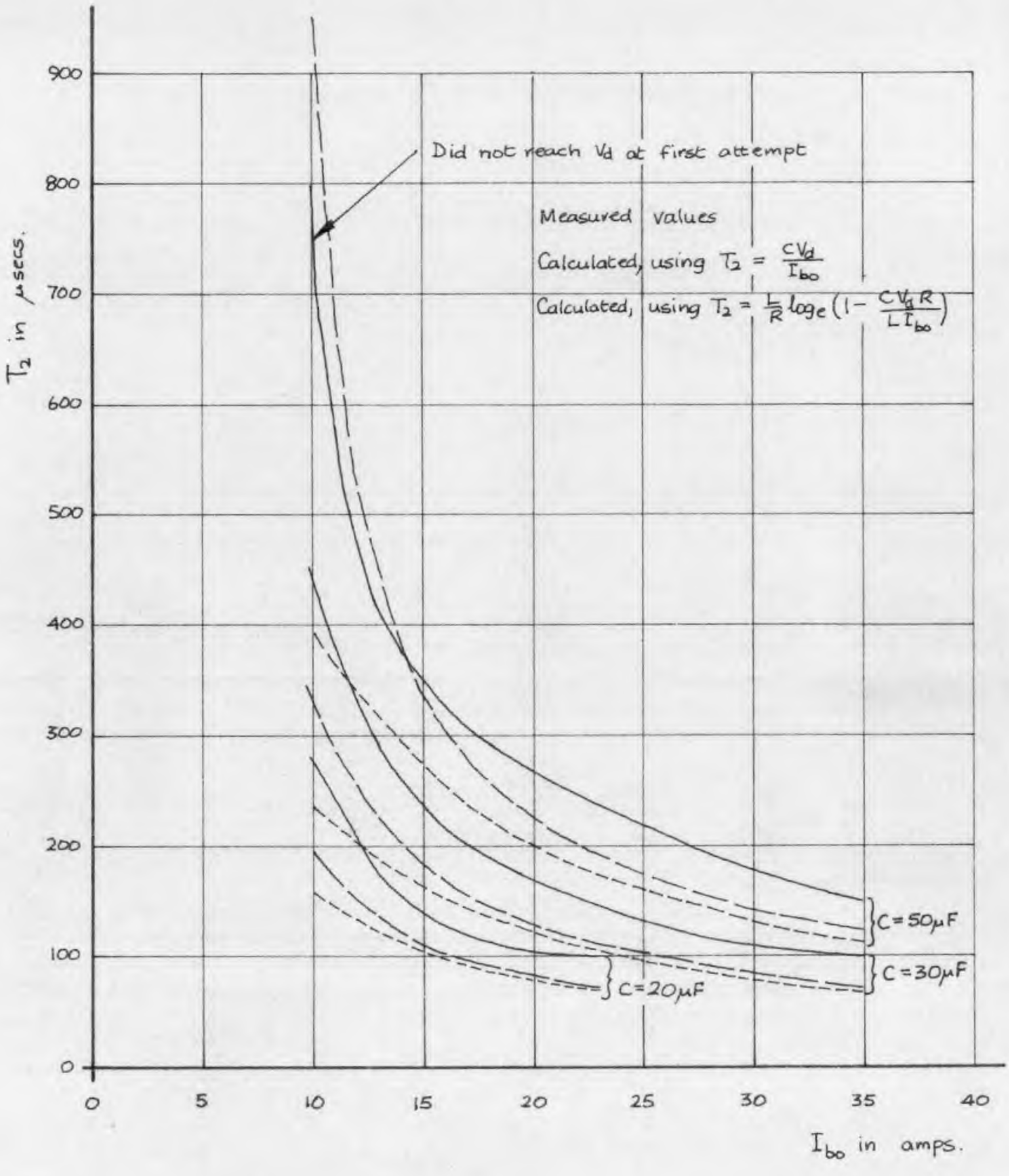


Fig. 8.10: Variation of T_2 with I_{bo} for several values of C.

$V_d = 80v$, $L_d = 0{\cdot}5$ mH, $L = 1{\cdot}85$ mH, R varied, $f = 25$ c/s.

The results predicted from equation (8.25) are seen to agree more closely with the measured results than with those based on equation (8.18). This is because the former partly take into account the fall in $(-i_b)$ whereas the latter are based on the assumption that i_b remains constant at I_{bo} throughout period 2. The difference between the two methods of prediction is most marked at low values of I_{bo} where i_b would be expected to change most severely.

With $C = 50\,\mu F$ and $I_{bo} = 10$ A it was found that the capacitor would not charge to supply voltage at the first attempt but completed the process one sixth of a cycle later. This was because the inductive stored energy of phase B was so low that the natural peak of the oscillation between C and the load was lower than the supply voltage. In all other cases encountered during this series of tests the load stored energy was greater or the required increase in capacitive stored energy less so that the capacitor charged to V_d in one step.

8.3.2.2. Variation of T_2 with L and I_{bo}.

The test procedure was as described in section 8.3.1.2 and the results are displayed in Fig. 8.11.

Once again it is seen that T_2 varied in an inverse manner with I_{bo}. The predicted results are again seen to be lower than the measured values of T_2, the discrepancy being nearly 30% in the worst cases. At all values of I_{bo} T_2 increased when the load inductance was decreased. This was because the fall in i_b from I_{bo} was greater when the inductance was

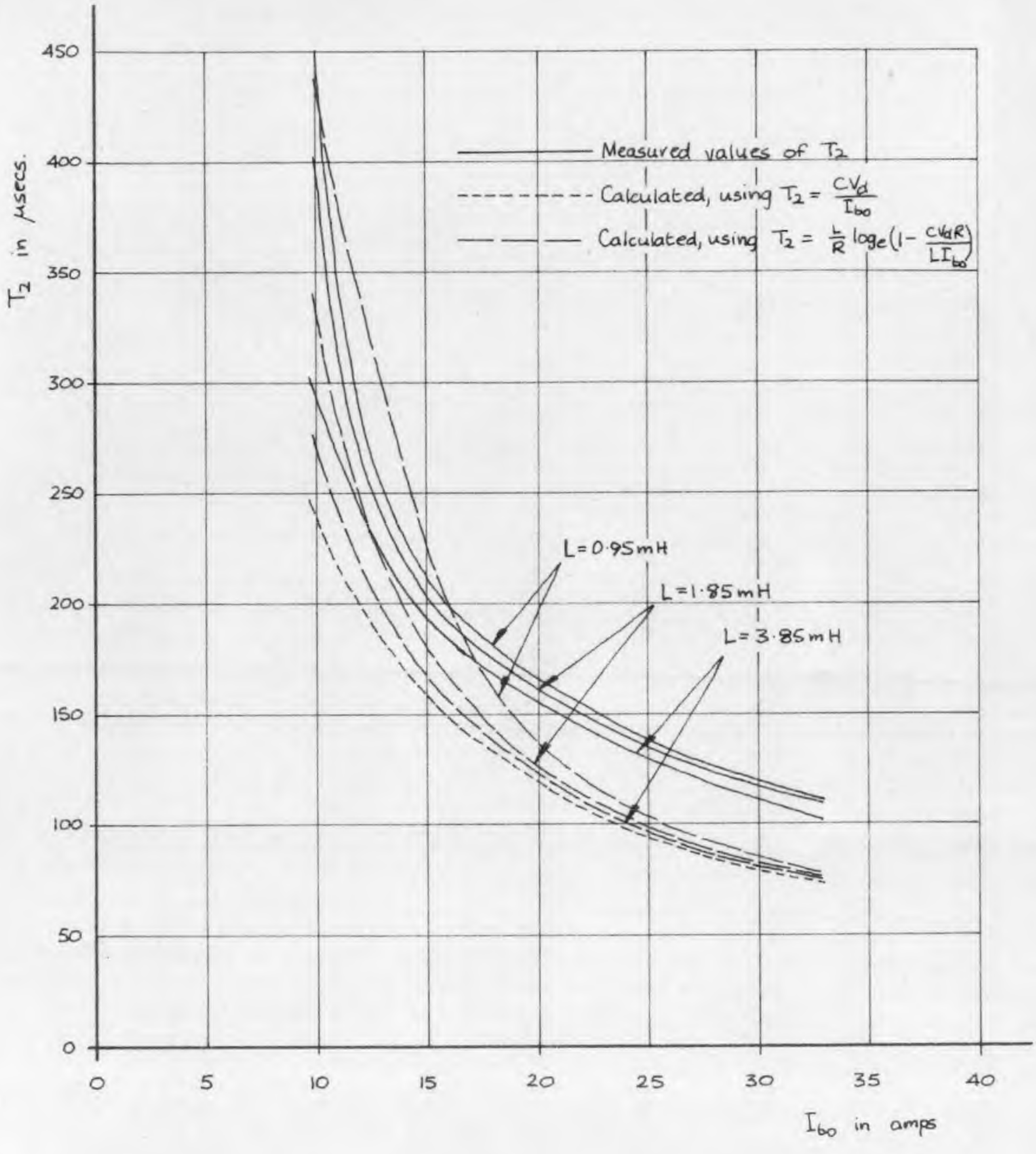


Fig. 8.11 : Variation of T_2 with I_{bo} for several values of L.

V_d = 80v, L_d = 0·5mH, C = 30μF, R varied, f = 25 c/s smaller and hence less current flowed into the capacitor which then took longer to charge through the same voltage range.

The results predicted from equation (8.25) gave more accurate predictions than those predicted from equation (8.18), particularly at the lower values of I_{bo}, because the fall in i_b was partly allowed for in this former equation.

8.3.2.3. Variation of T_2 with V_d.

This test was carried out as described in section 8.3.1.3 and the results are shown in Fig. 8.12.

T_2 was found to increase linearly with V_d, as predicted by equation (8.18). However, the results given by equation (8.18) were in general about 20% lower than those measured on the oscilloscope. The results given by equation (8.25) were also low, the discrepancy between measurement and prediction in this case being about 15%. Of the 15% discrepancy, 5% can be attributed to the capacitor's peak voltages being about 5% higher than supply voltage due to the inductance of the leads connecting the reverse diode bridge with the supply.

The linearity of the measured variation of T_2 with V_d indicates that i_b did not fall during period 2 or that the fall in i_b was constant at all values of V_d. Under the conditions of the test, with L = 3.85 mH, I_{bo} = 20A, and C = 50μF it can be seen that the inductive stored energy of phase B, even with V_d at 110 V was much greater than the increase in energy of C during period 2. If L or I_{bo} had been smaller, the curve

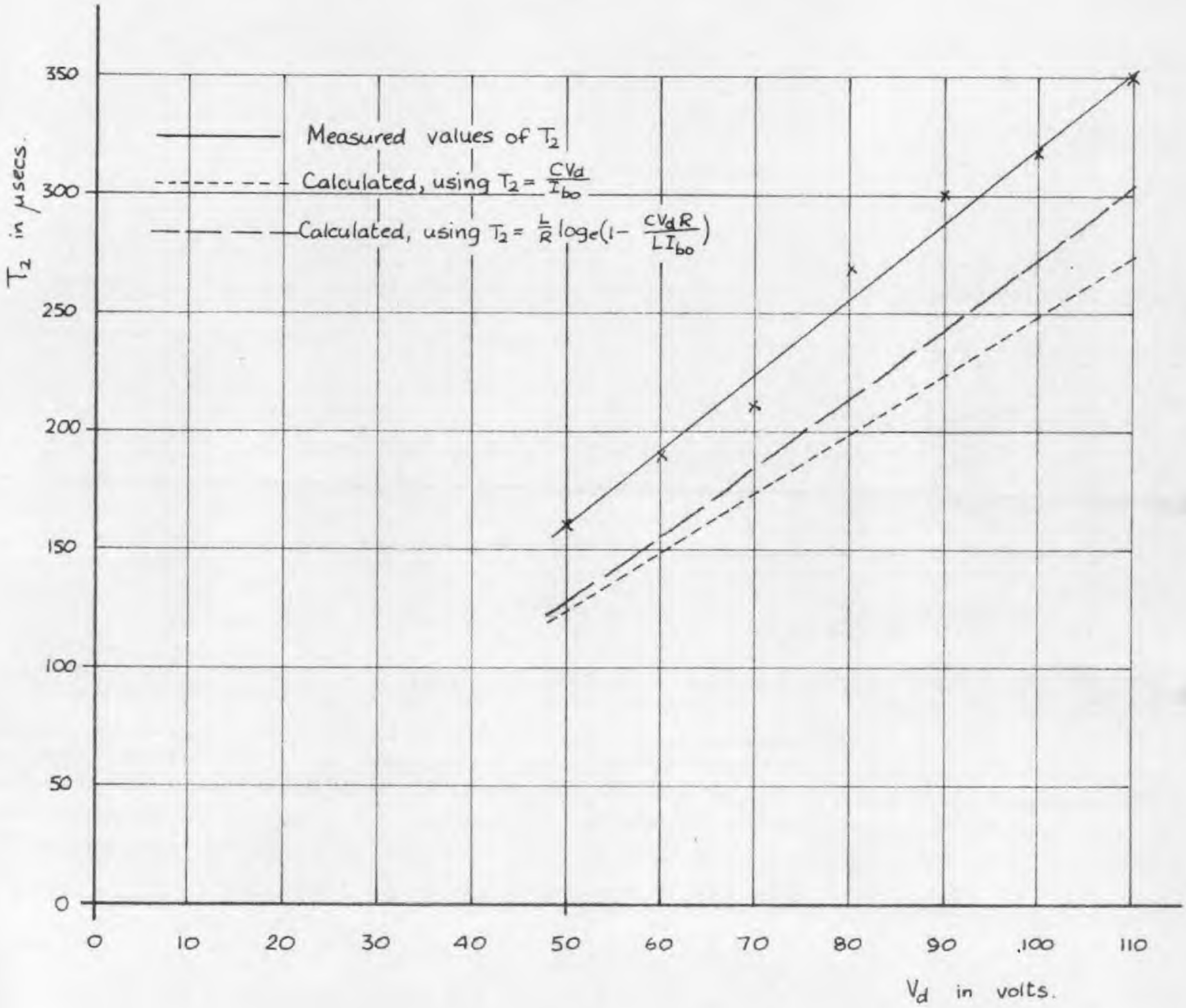


Fig. 8.12 : Variation of T_2 with V_d.

$L_d = 0.5$ mH, $C = 50\ \mu F$, $L = 3.85$ mH, $I_{bo} = 20A$, $f = 25$ c/s showing the variation of T_2 with V_d would be expected to be concave upwards, T_2 increasing more rapidly at higher values of V_d.

8.3.3. Approximate Calculation of Sample Load Waveforms.

8.3.3.1. Conditions for calculation.

Apart from the difference in commutation circuits the inverter and load were exactly as calculated for in section 6.3. The load and supply were :-

$$V_d = 100\text{ V},\quad L_d = 0.5\text{ mH},\quad C = 30\,\mu\text{F},\quad L = 3.85\text{ mH},$$
$$R = 2.3\,\Omega,\quad f = 50\ ^{c}/\text{s}.$$

In this case the current in one phase was zero at the end of each sixth of a cycle and hence for the calculations $I_{ao} = (-I_{bo})$ and $I_{co} = 0$. $2I_{do}$, the total current in the d.c. choke is assumed to be equal at $I_{ao} + (-I_{bo})$, i.e. $-2I_{bo}$.

8.3.3.2. Determination of boundary values of currents and the times T_1, T_2, T_3, T_4.

The iterative process which must be followed in determining the period durations and the current boundary values is not shown, only the final set of calculations being given.

$$\frac{V_d}{3R} = 14.5\text{ A},\quad \frac{V_d}{2R} = 21.75\text{ A},\quad \frac{2V_d}{3R} = 29.0\text{ A}.$$

Assume $I_{ao} = -I_{bo} = 20.05$ A and $I_{co} = 0$

$$\text{Then } \delta = T_1 \simeq \frac{CV_d}{-I_{do}} = \frac{30 \times 100 \times 10^{-6}}{20.05} = \underline{\underline{150\mu\,\text{Secs.}}}$$

i_a, i_b, i_c are assumed constant at 20.05 A, - 20.05 A and 0 during period 1.

$$\therefore\ T_2 \simeq \frac{CV_d}{-I_{bo}} = \underline{\underline{150\mu\,\text{Secs.}}}$$

The values of i_a, i_b, i_c at the end of period 2 are found from equations (8.23), (8.22), (8.24).

Hence

$$I_{a2} = 21.75 - (21.75 - 20.05)e^{-\frac{2.3}{3.85} \times .15}$$

$$= \underline{\underline{20.2\text{ A}}}$$

$$I_{b2} = -20.05e^{-\frac{2.3 \times .15}{3.85}}$$

$$= \underline{\underline{-18.33\text{ A}}}$$

$$I_{c2} = -(I_{a2} + I_{b2})$$

$$= \underline{\underline{-1.89\text{ A}}}$$

I_{c2} is not zero and hence the time T_3 taken for i_b to decay to zero and the values of i_a and i_c at the end of this period must be found from equations (5.58), (5.57) and (5.59).

Putting $i_b = 0$ and $t = T_3$ in equation (5.58)

$$0 = 14.5 + (-18.33 - 14.5)e^{-\frac{2.3 \times 10^3}{3.85}T_3}$$

Hence $T_3 = \underline{1.367 \text{ m Secs.}}$

Putting $t = 1.367$ m Secs in equation (5.57)

$$i_{a3} = \underline{17.1 \text{ A}}$$

Hence $I_{c3} = -I_{a3} = \underline{-17.1 \text{ A}}$

The remainder of the sixth of a cycle, T_4, is given by

$$T_4 = \frac{T}{6} - (T_1 + T_2 + T_3)$$

$$= \underline{1.666 \text{ m Secs.}}$$

Then I_{a4} and $(-I_{c4})$ can be found by putting $t = 1.666$ m Secs in equation (5.32)

$$\text{i.e.} \quad I_{a4} = -I_{c4} = 21.75 - (21.75 - 17.1)e^{-\frac{2.3 \times 1.666}{3.85}}$$

$$= \underline{20.04 \text{ A}}$$

This value is practically identical with the value assumed for I_{ao} and $(-I_{bo})$. Hence it can be assumed that the initial values chosen were correct. It has been assumed that diodes D_7 and D_8 conduct for the whole of the cycle apart from the periods of duration T_1 and that, therefore, the d.c. choke plays no part in the circuit except during commutation.

8.3.3.3. Current and voltage equations.

Having obtained the duration of the four periods in each sixth of a cycle and the boundary values of current, the current and voltage equations for each of the four periods may now be set out.

Period 1 (Of duration T_1 or δ = 150μ Secs.)

$$i_a = -i_b = 20.05 \text{ A (assumed constant)}$$

$$i_c = 0$$

$$\left.\begin{aligned} v_{ab} &= 100\frac{t}{T_1} \text{ V} \\ v_{bc} &= 100(1 - \frac{t}{T_1}) \text{ V} \\ v_{ca} &= 100(1 - \frac{2t}{T_1}) \text{ V} \end{aligned}\right\} \text{Derived from equations (8.5), (8.6) and (8.7) but assumed linear.}$$

Period 2 (Of duration T_2 = 150μ Secs.)

$$i_a = 21.75 - 1.7e^{-0.598\times10^{+3}t} \text{ A} \qquad \text{from equation (8.23)}$$

$$i_b = -20.05e^{-0.598\times10^{+3}t} \text{ A} \qquad \text{" " (8.22)}$$

$$i_c = -21.75(1 - e^{-0.598\times10^{+3}t}) \text{ A} \qquad \text{" " (8.24)}$$

$$v_{ab} = 100(1 - \frac{t}{T_2}) \text{ V} \qquad \text{from equation (8.26)}$$

$$v_{bc} = 100\frac{t}{T_2} \text{ V} \qquad \text{" " (8.27)}$$

$$v_{ca} = -100 \text{ V} \qquad \text{" " (8.28)}$$

Period 3 (Of duration T_3 = 1.367 m Secs.

$$i_a = 14.5 + 5.7e^{-0.598\times10^{+3}t} \text{ A} \qquad \text{from equation (5.57)}$$

$$i_b = 14.5 - 32.8e^{-0.598\times10^{+3}t} \text{ A} \qquad \text{" " (5.58)}$$

$$i_c = -29.0 + 27.1e^{-0.598\times10^{+3}t} \text{ A} \qquad \text{" " (5.60)}$$

$v_{ab} = 0$ from equation (5.64)

$v_{bc} = 100\ V$ " " (5.65)

$v_{ca} = -100\ V$ " " (5.66)

Period 4 (remainder of sixth of a cycle, of duration $T_4 = 1.666$ m Secs.)

$i_a = -i_c = 21.75 - 4.65e^{-0.598 \times 10^3 t}$ from equation (5.32)

$i_b = 0$

$v_{ab} = 50\ V$

$v_{bc} = 50\ V$

$v_{ca} = -100\ V$

8.3.3.4. Load current and voltage waveforms.

Using the equations set out in the previous sub-section the load current and voltage waveforms have been drawn in Fig. 8.13. For comparison the measured waveforms have been drawn on the same axes and to the same scale. Agreement is to within about 10% in general.

There are several discrepancies between the calculated and measured waveforms which are worthy of note. During the commutation periods it is seen that the load currents did not remain constant but nevertheless the changes were very small. In fact, the only significant change not predicted was the negative current which began to flow in the phase just about to be connected by an S C R to the supply. This is shown at 6.7 and 16.7 m Secs on thetime scale. The oscillations on the current

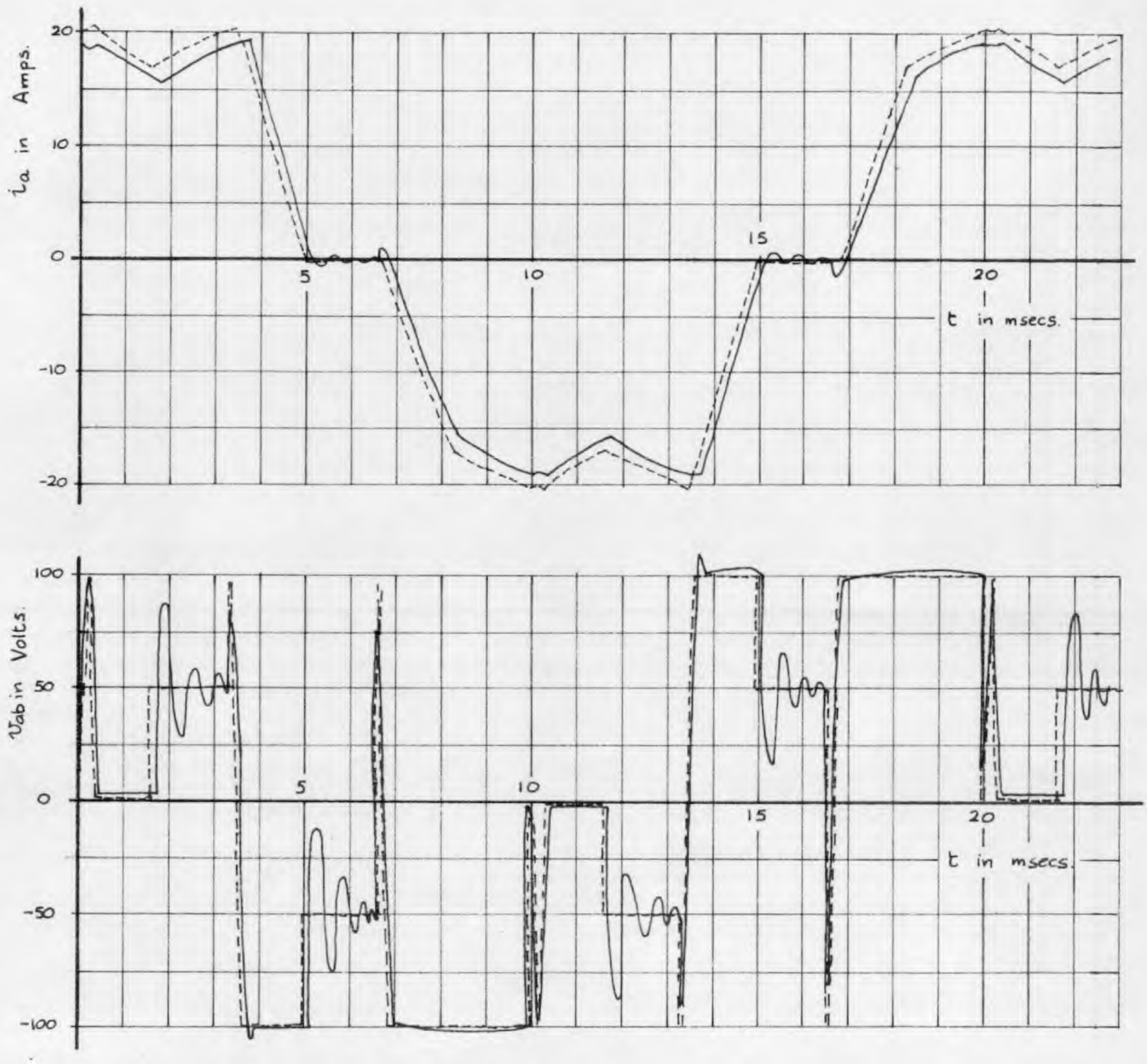


Fig. 8.13: Measured(——) and predicted (----) waveforms of load current i_a and line-to-line voltage v_{ab}.

$V_d = 100V$, $L_d = 0{\cdot}5mH$, $C = 30\mu F$, $R = 2{\cdot}3\Omega$, $L = 3{\cdot}85mH$, $f = 50c/s$.

and voltage waveform were caused by the filter capacitors connected across the load and have not, therefore, been predicted. The voltage excursions during commutation were not as large as predicted. This was because the commutating capacitors lost some of their charge to the filter capacitors during the initiation of commutation. A degree of overshoot beyond supply voltage was observed during the charging of the commutating capacitor after commutation and is shown at 3.33 and 13.33 m Secs. This was attributed to the inductance of the lines connecting the reverse diode bridge to the supply. At a nominal voltage of $\pm$ 100 V the load voltage waveform was seen to be curved. This was due to the ripple on the voltage of the supply reservoir capacitor caused by the fluctuation in the current drawn by the inverter.

8.3.4. <u>Comparison between Performances of d.c. Commutated and a.c. Commutated Inverters on Identical R-L Loads.</u>

The supply voltage, load and frequency were identical for the waveforms calculated in sections 6.3 and 8.3.3. and the measurements made under the same conditions for both circuits form a good basis for comparing their fundamental differences.

When the waveforms shown in Figs. 6.8 and 6.9 are compared with those of Fig. 8.13 it is seen that although the current waveforms are basically similar the distortion near the peaks is rather less in Fig. 8.13 than in 6.8. It would therefore be expected that the r.m.s. value of current would be higher and the harmonic content smaller in the current waveform of Fig. 8.13. In the voltage waveforms the effect of commutation is to add a large rectangular pulse to the basic waveform in Fig. 6.9 but a triangular pulse in Fig. 8.13 and the total excursions during commutation in the former waveform are rather greater than in the latter waveform. Hence although the r.m.s. voltages would be nearly equal it would be expected that the harmonic content would be smaller in the latter waveform.

Table 8.1 below shows the most important quantities compared side by side for the two circuits.

Quantity		D.C. Commutated Inverter		A.C. Commutated Inverter	
V_d	(Mean	100 V		100 V	
I_d	(Mean)	17.2 A		15.0 A	
W_d		1720 W		1500 W	
W_a		295 W		-	
$W_d + W_a$		2015 W		1500 W	
V_ℓ	(R.M.S.)	72.0 V		72.5 V	
I_ℓ	(R.M.S.)	13.2 A		13.7 A	
W_ℓ		1200 W		1360 W	
Efficiency (overall)		59.6%		90.7%	
Power Factor		0.73		0.79	
V_1	Actual values	60.0 V	83.3%	63.2 V	87.2%
V_5	of harmonics	31.4 V	43.6%	28.5 V	39.3%
V_7	are given in	15.7 V	21.8%	19.8 V	27.3%
V_{11}	the first	9.5 V	13.2%	8.1 V	11.1%
V_{13}	column and	6.2 V	8.6%	5.9 V	8.2%
I_1	their percentage	12.8 A	97.0%	13.5 A	98.5%
I_5	of V or I in	2.71 A	20.5%	2.5 A	18.0%
I_7	the second	0.98 A	7.4%	1.23 A	9.0%
I_{11}	column.	0.39 A	3.0%	0.33 A	2.4%
I_{13}		0.22 A	1.7%	0.20 A	1.4%

Table 8.1: Comparison between performances of d.c. commutated and a.c. commutated inverters.

The remarks made above about r.m.s. values and harmonic content are seen to be borne out in Table 8.1. The most significant difference between the two inverters, however, is seen to be the much improved efficiency of the a.c. commutated inverter. The higher power factor is the result of the lower harmonic content of voltage and current.

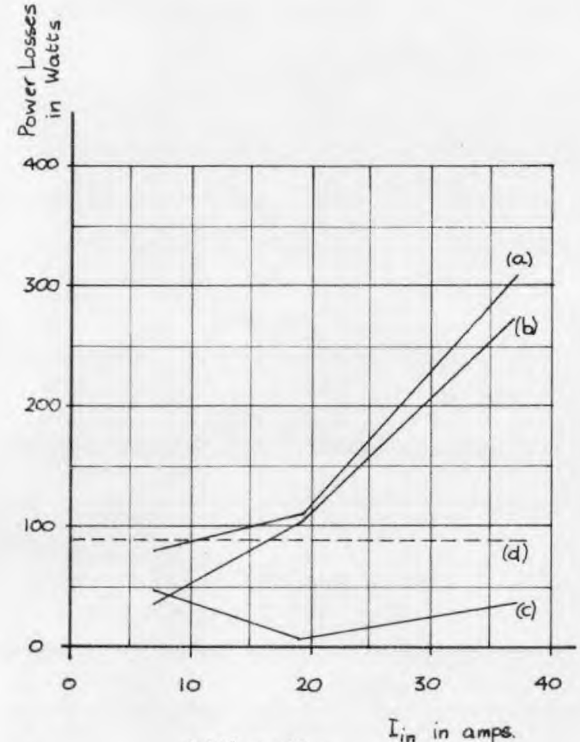
8.4. Commutation Power Loss and Inverter Efficiency.

A number of tests were carried out, using the motor as a load, to determine the efficiency of the inverter and to check the validity of the expression given for the commutation power loss.

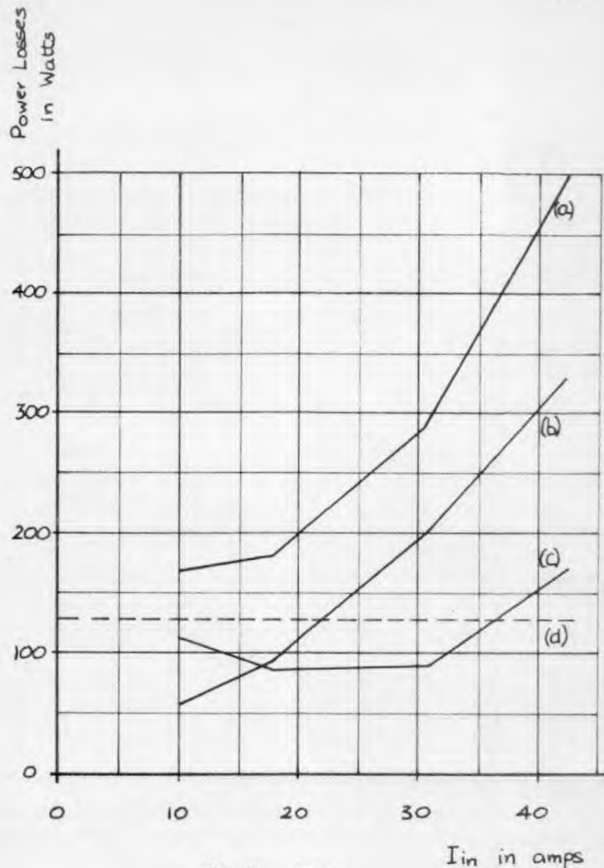
8.4.1. Commutation Power Loss.

At an operating frequency of 50 $^c/s$. the inverter was loaded by the motor to varying degrees and the input and output powers measured for the inverter. This was done for $C = 30\,\mu F$ and $C = 50\,\mu F$ and for several different supply voltages. The losses in the S C Rs and diodes and the I^2R losses in the circuit were estimated from the measured currents and the known forward voltage drops and circuit resistances and these losses were subtracted from the total power loss. The remaining losses should then have been the commutation losses.

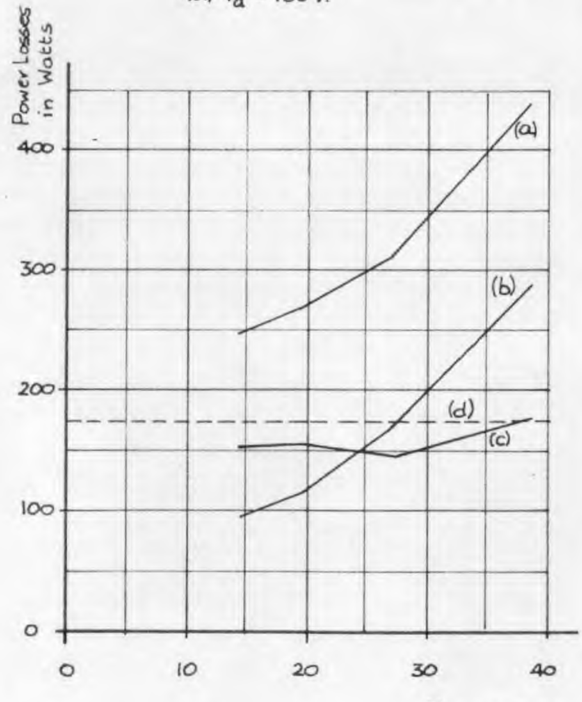
Figs. 8.14 and 8.15 show the results of these tests. The losses have been plotted against I_{in}, the mean current flowing into the S C R bridge. In determining the rectifier losses 1.5 V and 1.0 V have been taken to be the S C R and diode forward voltage drops. For the resistive losses 0.1 Ω has been taken as the effective resistance of



(a) $V_d = 100$v.



(b) $V_d = 120$v.



(c) $V_d = 140$v

Fig. 8.14: Variation of inverter power losses with I_{in}.

$C = 30\mu F$, $f = 50$c/s, $L_d = 0{\cdot}5$mH.

(a): Total power losses

(b): Estimated rectifier and I^2R losses

(c): Remainder, attributed to commutation.

(d): Predicted commutation loss = $6CfV_d^2$.

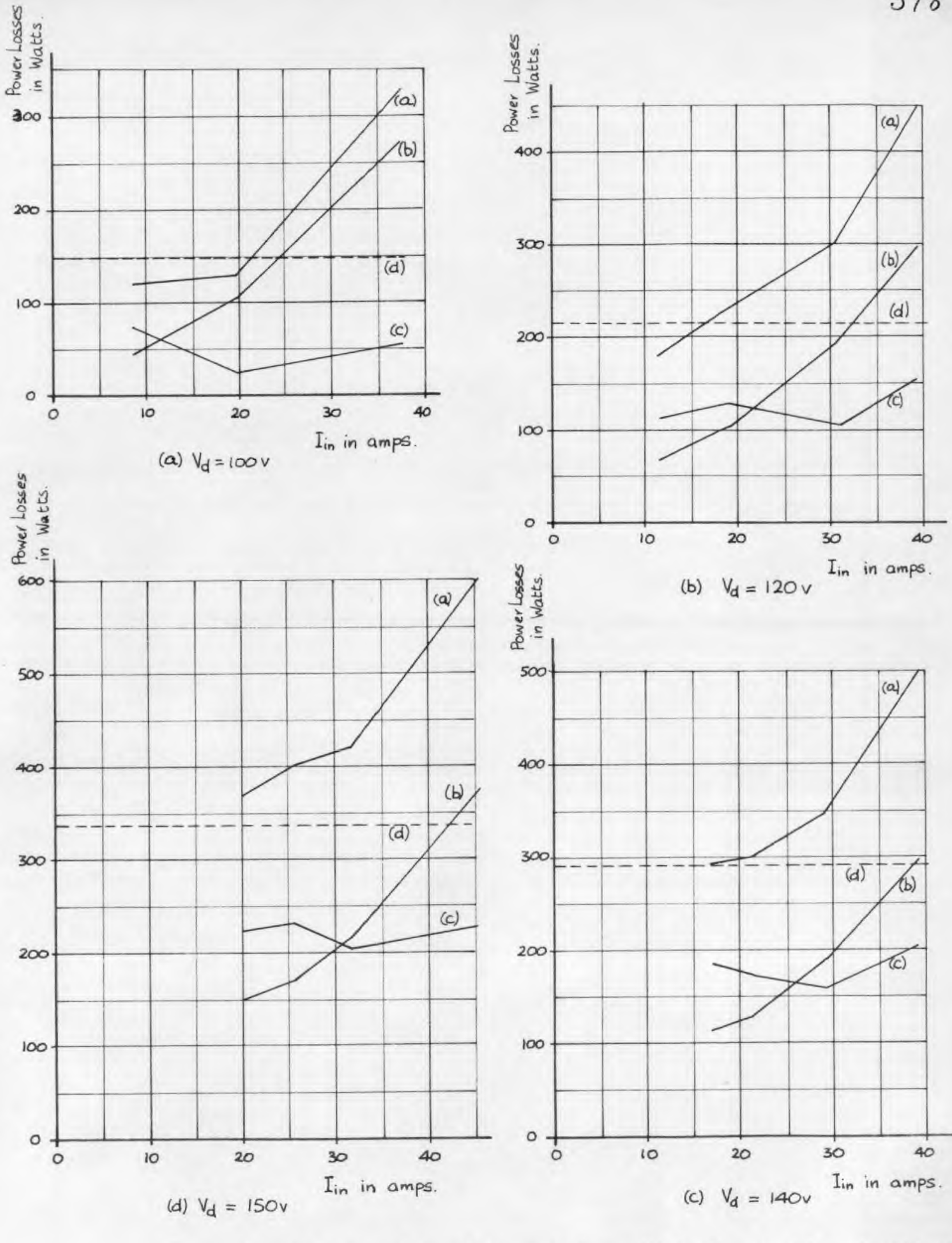


Fig. 8.15: Variation of inverter power loss with I_{in} for several supply voltages

$C = 50\,\mu F, \quad L_d = 0{\cdot}5\,mH, \quad f = 50\,c/s$

(a) : Total power loss ; (b) : Estimated rectifier and I^2R losses;

(c) : Remainder ; (d) : Predicted commutation loss $= 6CfV_d^2$.

the d.c. circuits of both S C R and diode bridges.

In each graph in both Fig. 8.14 and 8.15 the predicted commutation loss is shown as $6\ CfV_d^{\ 2}$. For $V_d = 100$ V in both cases the losses attributed to commutation are seen to be far less than predicted. Some of this discrepancy can be attributed to the errors involved in reading the wattmeters at low powers and some to the fact that a component of the commutation power loss is dissipated in the S C Rs and reverse bridge diodes. At higher voltages the losses attributed to commutation are nearer to prediction but, in general, are no more than about two thirds of the predicted values. In sections 8.2.1.4 and 8.2.1.5 it was predicted that the commutation loss would lie between $3\ CfV_d^{\ 2}$ and $6\ CfV_d^{\ 2}$ and so in general the commutation loss did fall between these limits.

8.4.2. Inverter Efficiency.

In Fig.8.16 the inverter input power required to produce a given output power and the inverter efficiency is shown. The values given are those which were measured in the course of the tests for commutation power loss. It is seen that at low output power the input power increased with supply voltage and commutating capacitance. This was due to the increase in commutation power loss and resulted in a corresponding decrease in inverter efficiency. The efficiency increased to a maximum value and then decreased as the output power was increased. Maximum efficiency corresponds to the point where the increasing I^2R and rectifier losses become equal to the virtually constant commutation

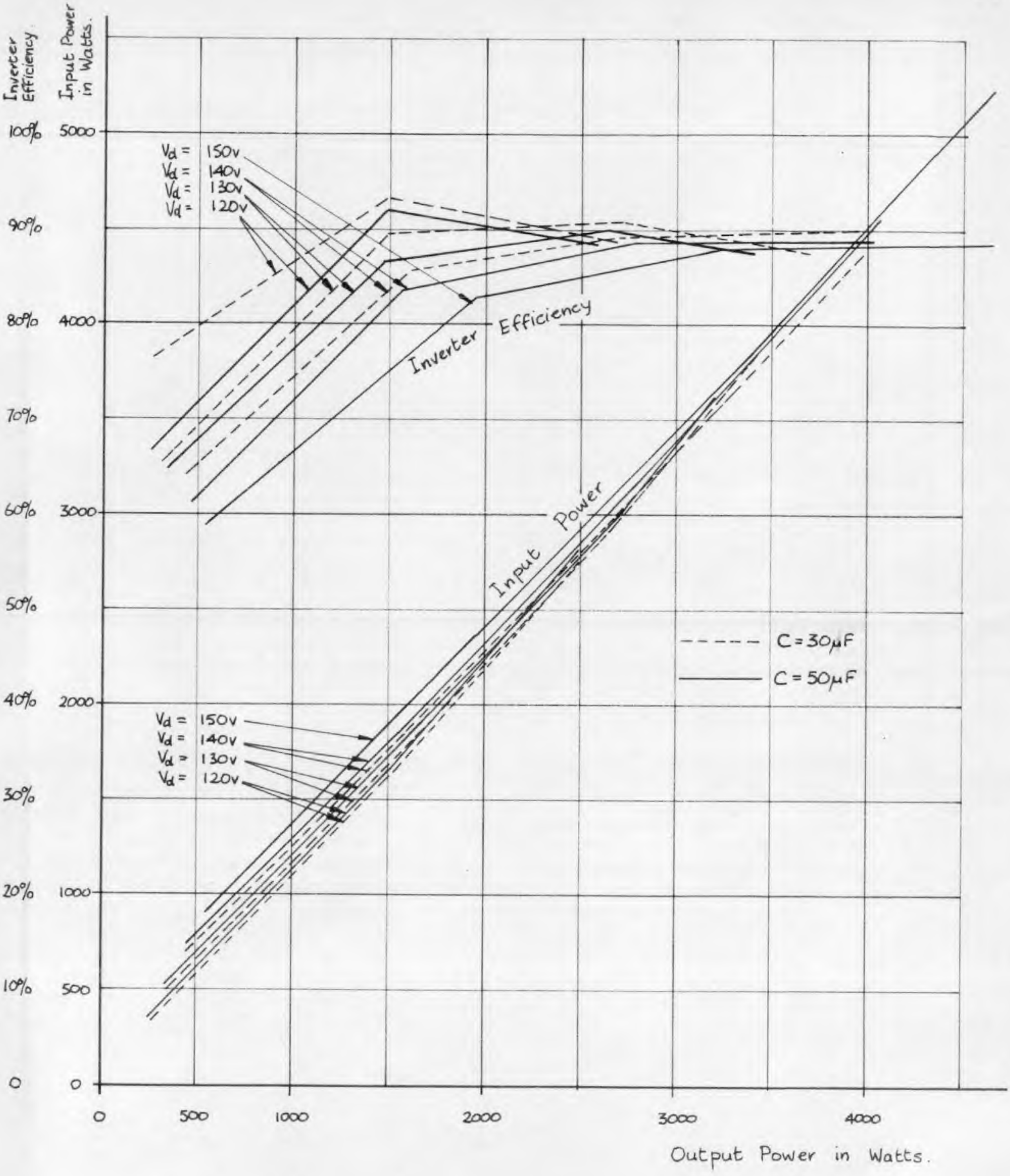


Fig. 8.16: Variation of input power required and inverter efficiency with inverter output power for several combinations of C and V_d.

$L_d = 0{\cdot}5\,mH$, $f = 50\,c/s$.

losses. Since the commutation losses increase with voltage and capacitance the power at which peak efficiency is obtained also increases with voltage and capacitance.

The peak inverter efficiency attained at 50 $^{c}/s$. was seen to be 93% and the efficiency was generally about 89% at powers above about 3 KW. This compares very favourably with the efficiency of the d.c. commutated inverter, which was about 80% under similar load conditions. It was seen in Figs. 8.14 and 8.15 that at high powers the rectifier and resistance losses constituted at least a half of the inverter losses. If the resistance losses could be reduced almost to zero, it would be expected that the efficiency of the circuit could be improved to a minimum of 95% at 50 $^{c}/s$. when giving a high power output.

8.5. Motor Efficiency and Typical Motor Waveforms.

8.5.1. Motor Efficiency.

Fig. 8.17 shows how the motor input power and efficiency varied with motor output power for the several combinations of supply voltage and commutating capacitance used in the tests of section 8.4. It is seen that the change of commutating capacitance made virtually no difference to the motor input power or efficiency. When the supply voltage was increased, however, the input power required was increased, and efficiency therefore decreased at low powers because of the higher iron losses. At higher powers, however, the input power was smaller and efficiency greater when the voltage was increased, partly because of the smaller currents required at higher voltages and partly because

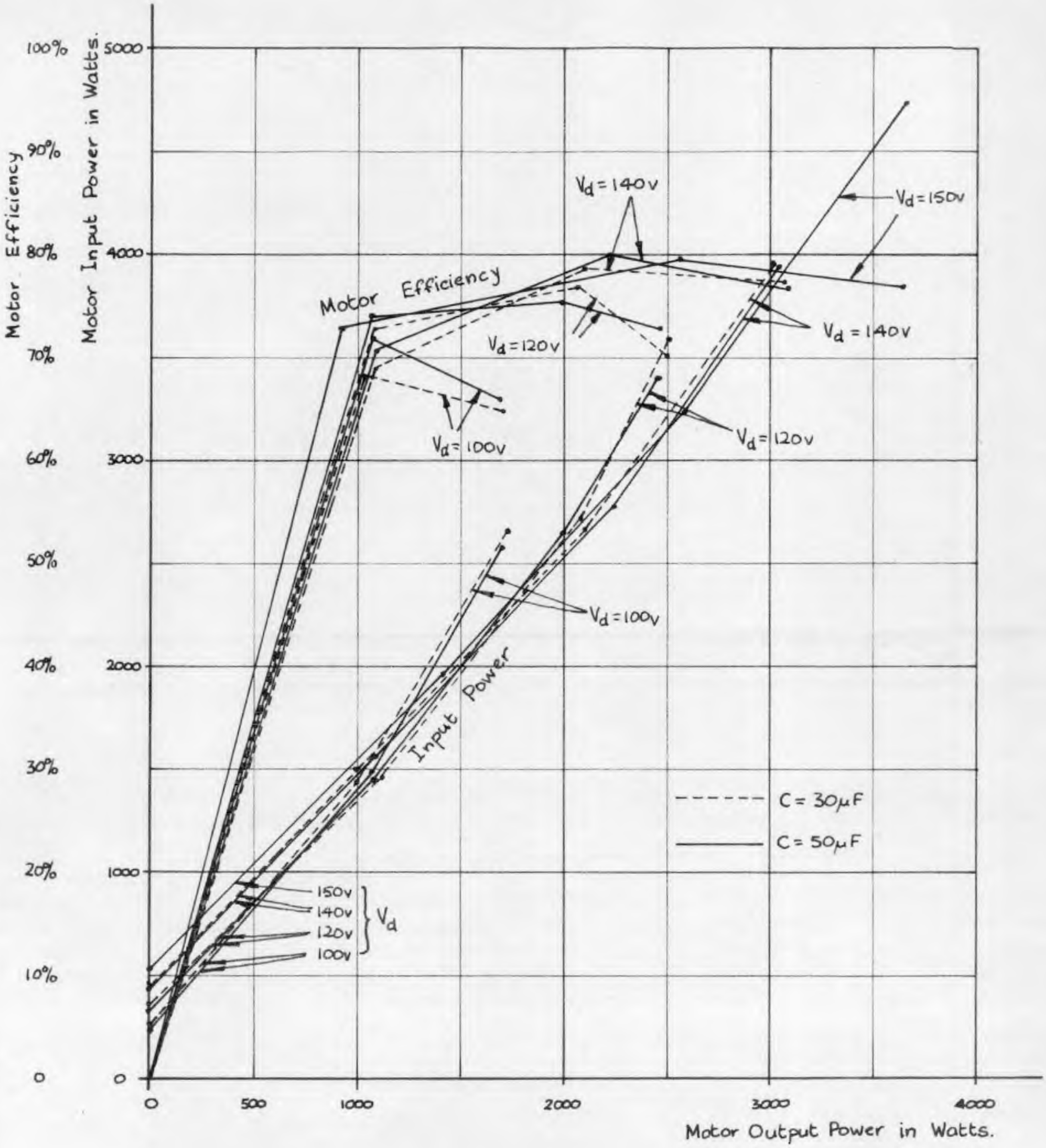


Fig. 8.17: Variation of motor input power and motor efficiency with motor output power for several combinations of commutating capacitance and inverter supply voltage.

$L_d = 0.5\,mH$, $f = 50\text{c/s}$.

of higher air gap flux and the resulting smaller rotor slip losses.

The motor efficiency was seen to be about 78% at about 3 KW output power. This efficiency was attained with a motor line r.m.s. voltage of about 109 V but the fundamental component of the motor line voltage was only about 104 V. Increasing the fundamental component to 110 V, the rated voltage of the motor would probably have improved the efficiency to about 80%. Thus the motor efficiency was marginally higher than when the motor was fed from the d.c. commutated inverter.

8.5.2. Typical Motor Voltage and Current Waveforms and Harmonic Content.

Figs. 8.18, 8.19 and 8.20 are oscillograms of the motor line-to-line voltage and line current for no-load, one third, and two thirds of full-load torque. The oscillograms were photographed at a d.c. supply voltage of 115 V, using commutating capacitors of 50 μF, and with a frequency of 40 $^{c}/s$. The waveforms were, however, typical of the waveforms observed at all frequencies, except low frequencies, under similar conditions.

Table 8.2 shows how the r.m.s. values of current and voltage and their harmonic content changed with load.

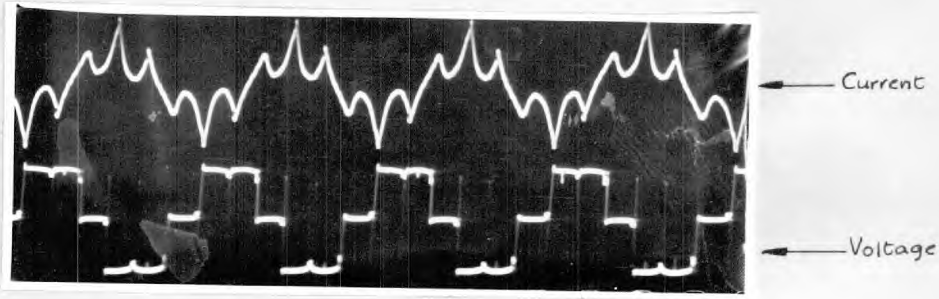


Fig. 8.18: Motor current and voltage waveforms at no-load.

$V_d = 115v$, $f = 40^c/s$

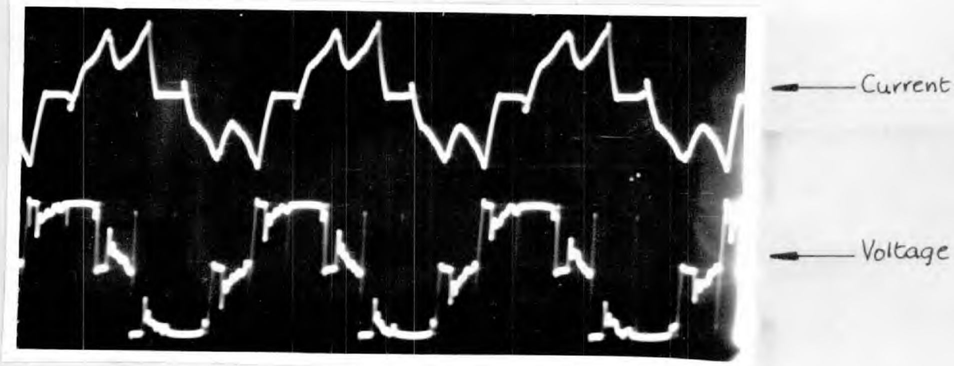


Fig. 8.19: Motor current and voltage waveforms for 1/3 full load torque.

$V_d = 115v$, $f = 40^c/s$

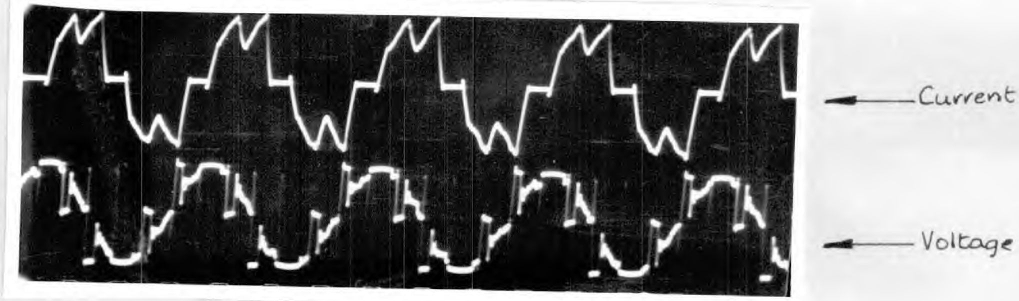


Fig. 8.20: Motor current and voltage waveforms for 2/3 full load torque.

$V_d = 115v$, $f = 40^c/s$

Motor Torque	Harmonic	1	5	7	11	13	17	Total r.m.s.
	Voltage (V)	89.5	20.5	9.5	9.5	4.2	6.0	92.0
Zero	Current (A)	11.4	6.4	2.34	1.67	0.72	0.72	13.4
	Impedance (Ω)	4.54	1.87	2.45	3.31	3.41	4.86	-
	Voltage (V)	84.0	17.9	11.2	12.5	6.1	5.2	87.8
7 lb-ft	Current (A)	14.8	5.4	2.46	1.84	0.72	0.58	16.2
	Impedance (Ω)	3.28	1.92	2.63	3.92	4.94	5.24	-
	Voltage (V)	78.5	20.1	14.0	13.4	9.2	6.05	83.5
13 lb-ft	Current (A)	22.4	5.91	2.82	1.84	0.98	0.63	23.4
	Impedance (Ω)	2.02	1.96	2.87	4.20	5.42	5.55	-

Table 8.2: Harmonic components of motor voltage and current and harmonic impedances for no-load, one third, and two thirds of full-load torque. V_d = 115V, f = 40 $^c/s$.

The oscillograms are very similar to those of Figs. 7.15 and 7.16 apart from the voltage excursions during commutation, the smaller distortion at the peak of the current waveform, and the reverse current peak just prior to a forward current half cycle. These differences have been discussed already in section 8.3.4. The general remarks about the motor waveforms in section 7.8 apply here with equal force, as do the remarks made about harmonic content and harmonic impedance.

As the load was increased the motor voltage waveform changed shape. On no load it consisted almost of a rectangular pulse, one third of a cycle long, in each half cycle such as would be obtained by putting

$u = 60^{\circ}$ (See Fig. 5.37 and section 5.5) At higher speeds u became smaller. It was because of the change in waveform with load that the r.m.s. value and the fundamental components of voltage decreased with load.

On no-load the total r.m.s. values of voltage and current were about 4% and 17% higher respectively than the fundamental components. For two thirds of full-load torque the corresponding increases were about 6.5% and 5% respectively. These increases on load were smaller than those encountered in section 7.8 but this is partly attributable to the increase in frequency from 25 $^{c}/s.$ to 40 $^{c}/s.$ It may be concluded, however, that the a.c. commutated inverter produces a slightly smaller harmonic content in the motor voltage and current than the d.c. commutated inverter but sufficient tests were not carried out to determine the precise improvement.

8.6. Limits of Operation of the "A.C. Commutated Inverter".

Because δ was approximately proportional to C V_d for a given load current the range of frequency over which the a.c. commutated inverter could function satisfactorily was somewhat restricted. For a given value of C the supply voltage hadto be greater than a certain minimum value to produce an adequate reverse bias time δ for reliable commutation. This minimum required value of V_d depended, of course, upon the size of the commutating capacitor.

When the motor formed the inverter load the supply voltage had to be varied proportional with the output frequency, and hence motor speed, to prevent saturation of the motor. Consequently the inverter could not be operated unaided below a certain inverter output frequency, this minimum frequency depending upon the value of C used.

For a given value of C and load current the time taken by the commutating capacitor to charge from $-V_d$ to $+V_d$ during the commutation process is almost proportional to V_d. Hence when the supply voltage and frequency increase, the commutation process takes up an increasing period in a decreasing sixth of a cycle. It is undesirable that commutation should take up a large proportion of the output cycle because of the distortion of the voltage and current waveforms that results. Hence if C is made large enough to provide an adequate value of δ at low frequency and supply voltage, it would be found that the output waveforms would not be satisfactory at high frequencies.

Because the a.c. commutated circuit had no auxiliary supply for commutation special measures were necessary to set it into operation and charge the capacitors with the correct polarity. For starting, the commutation circuit of the d.c. commutated circuit was used in addition to that of the a.c. commutated circuit. The a.c. commutation circuit could operate unaided only when the supply voltage had become high enough, in conjunction with the commutating capacitors used, to provide adequate reverse bias time for the S C Rs. To turn off the d.c. commutation circuit it was sufficient then to remove the gate pulses from CR7.

Another possible method of starting the circuit would have been to turn on all the auxiliary S C Rs (CR1a, CR2a, etc.) for the first few cycles of switching. The circuit would then have operated in the same way as that employing artificial commutation on the a.c. side (see Chapter 3), charging the capacitors in the correct directions. This method was not tried and it is clear that it would have been successful only if the supply voltage and the commutating capacitors had been high enough and the load current low enough in the first few cycles for artificial commutation to be sufficient.

Some success in improving commutation and extending the range of operation of the circuit was achieved by connecting a small choke of inductance L_x in each d.c. line of the reverse diode bridge as shown in Fig. 8.21. One effect of L_x was to increase the amount by which the capacitor voltage overshot the supply voltage after commutation. Fig.8.22 shows the opsrational circuit valid for the overshoot period. When the voltage on the capacitor reaches supply voltage after instant t_2 diode D_3 conducts. If L_x were zero, the current in D_3 would immediately become equal to the current flowing in phase B and the capacitor woubd stop charging, $CR2_a$ thereupon turning off. Because of the presence of L_x the current in D_3 takes time to become equal to i_b and the capacitor contiznues to charge until the equality occurs. If i_b were to remain constant at I_{bo} during the overshoot period, it could be found from the circuit shown in Fig. 8.22 that the peak voltage on the capacitor when it finally ceases charging would be given by

$$\underline{\underline{\hat{v}_c = V_d + I_{bo}\sqrt{\frac{L_x}{C}}}} \qquad (8.29)$$

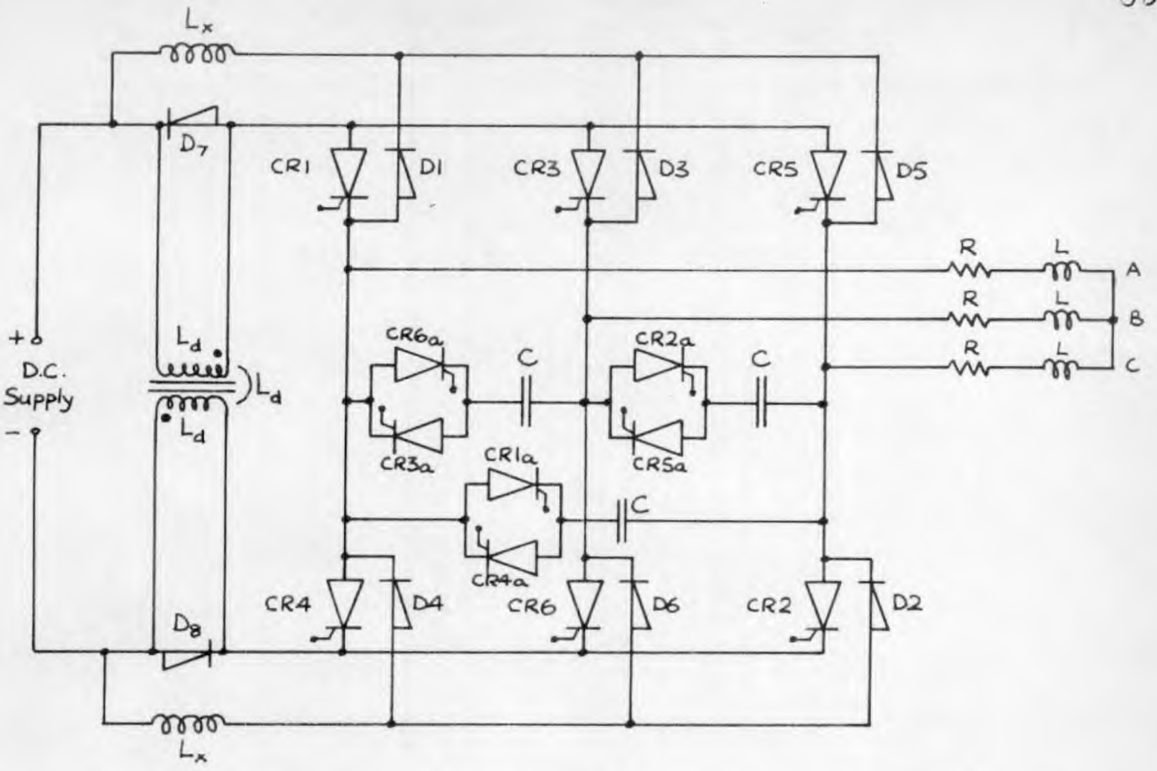


Fig. 8.21: A.C. commutated inverter with improved commutation and an extended range of operation.

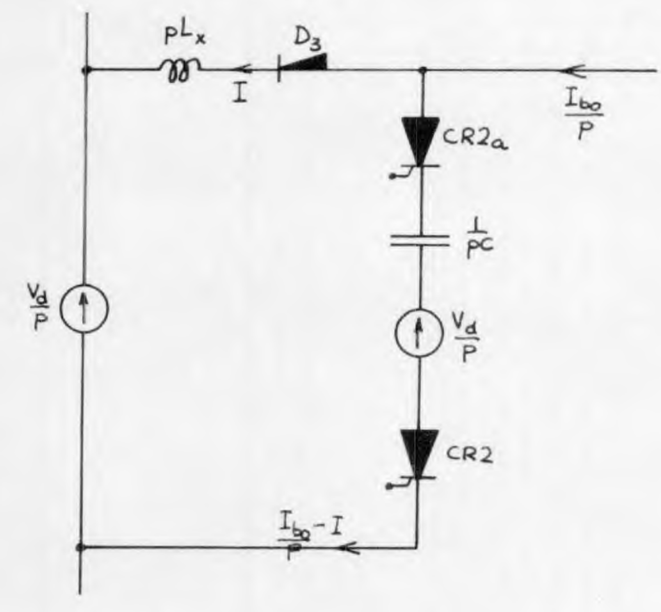


Fig. 8.22: Operational circuit valid during the period when the capacitor voltage overshoots supply voltage after commutation at instant t_2.

Equation (8.29) is of considerable significance because it shows that it is possible to charge the commutating capacitor to a voltage which is dependent upon the current to be commutated. It then becomes possible to make δ less dependent upon the current to be turned off than has been the case hitherto.

Fig. 8.23 shows the results of some tests for the effect of L_x upon commutation. It was found that when L_x was zero the circuit behaved in the manner described in section 8.3, $\hat{v}_c$ increasing slightly with current due to stray inductance and δ falling almost inversely proportional to current. When L_x was 170 μH and 360 μH in turn $\hat{v}_c$ was found to increase substantially with current. The increase in $\hat{v}_c$ was not as great as predicted from equation (8.29) probably because i_b did not remain constant during the overshoot period and because i_b had already fallen from I_{bo} before the overshoot period began. However, the effect of L_x upon δ was quite marked especially at the higher currents where δ showed a tendency to level off and become independent of current.

Unfortunately this effect of L_x was not appreciated until the end of the investigation and it was therefore not possible to carry the study very far. It is clear, however, that if the capacitor voltage can be made dependent upon load current, then the supply voltage becomes less important. It was found that if C was made large enough for the circuit to operate without L_x from 25 ^{c}/s. upwards, it was possible to operate down to about 10 ^{c}/s. with an L_x of about 170 μH.

Some disadvantages of this method of improving commutation became evident. It was more difficult to use the d.c. commutation method to

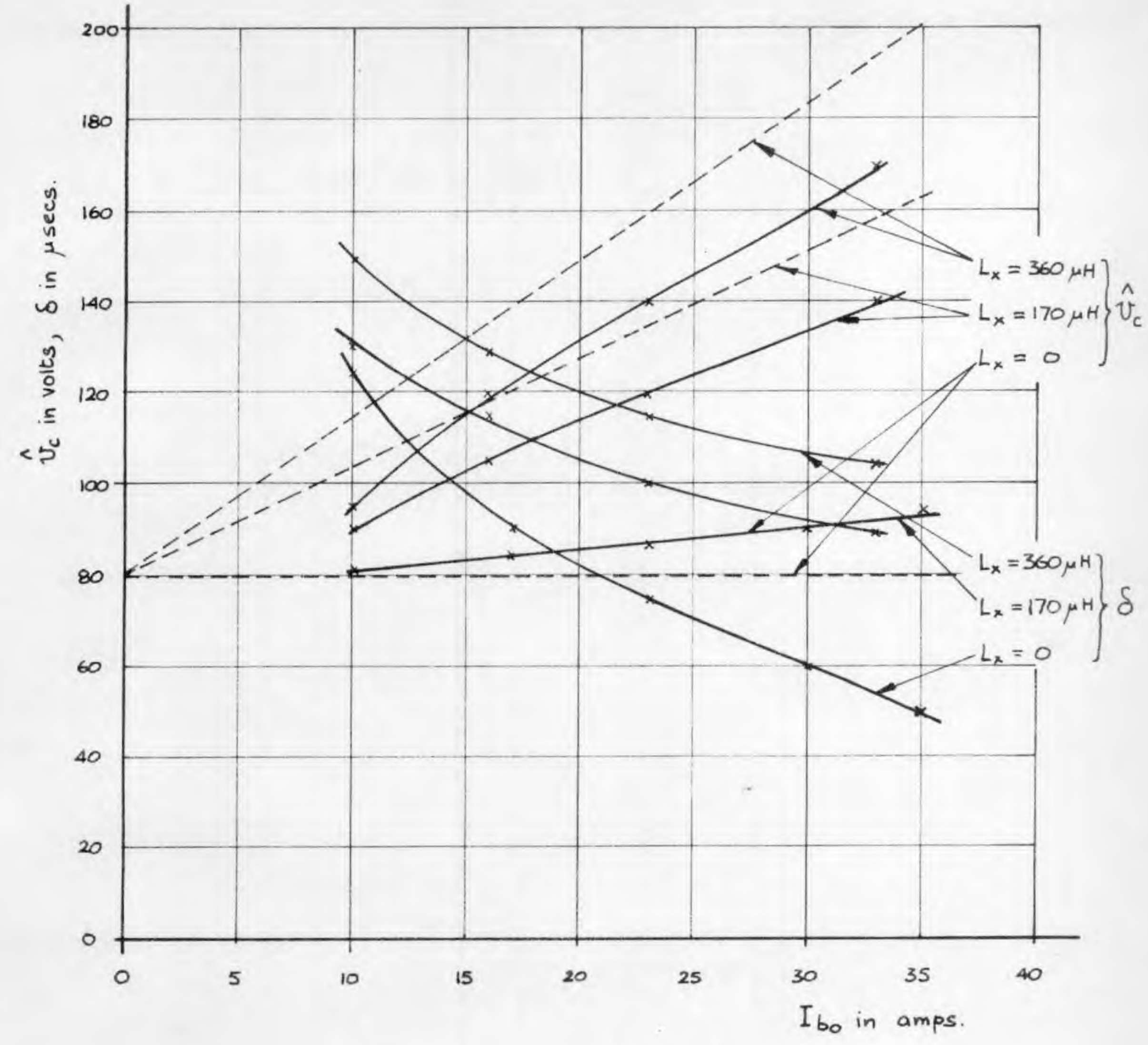


Fig. 8.23 : Variation of $\hat{v}_c$ and δ with I_{bo} for several values of L.

$V_d = 80V$, $C = 30\mu F$, $L_d = 0{\cdot}5\,mH$, $L = 1{\cdot}85\,mH$, R varied, $f = 25\,c/s$.

———— Measured values

- - - - - - - - Predicted values of $\hat{v}_c$

start the inverter because of the presence of L_x. The inclusion of L_x made the already difficult analysis of the a.c. commutated inverter even more complex. It was also found that the overshoot did not occur with purely resistive loads or with low load currents when the load inductance was low. It should also be noted that the capacitor voltage overshoot depends upon the current being commutated half a cycle before the capacitor is used again for commutation. The capacitor voltage is therefore adequate for the current to be commutated only if the current does not change greatly in half a cycle.

The effect of L_x upon the commutation power loss was not determined. During commutation, however, the capacitor voltage is shared between L_x and the d.c. choke and the increase in energy of the d.c. choke would clearly not be as great as if V_d were equal to $\hat{v}_c$ in the absence of L_x.

8.7. Ratings of Circuit Components.

The current ratings required for the bridge S C Rs and diodes are the same as those given for the d.c. commutated inverter. The maximum voltage which can appear on these devices is $\pm V_d$ plus transient overshoots, unless the inductance L_x is included. In this case the maximum voltage would be $\pm \hat{v}_c$ (which can be found from equation (8.29)) plus transient overshoots.

The same voltage rating applies to the auxiliary S C Rs. The mean current in each auxiliary S C R is equal to $2C f V_d$, i.e. the current required to charge the capacitor through a voltage $2V_d$ once per cycle. If L_x is included, the mean current becomes $2 C f \hat{v}_c$.

For this application the peak current is probably more important and this is approximately equal to the peak value of the load current. At high frequencies the peak current may be greater because of the building up of a circulating current in the d.c. choke and diodes D_7 and D_8.

The capacitor current consists of the same peaks as in the auxiliary S C Rs but twice per cycle. The capacitors should be rated for the r.m.s. value of this current.

8.8. <u>General Conclusions on the "A.C. Commutated Inverter"</u>.

The a.c. commutated inverter was found to be considerably more efficient than the d.c. commutated inverter. The power loss due to commutation was found in general to be about $4\ C\ f\ V_d^{\ 2}$ instead of $12\ C\ f(V_d + V_a)^2$. To give the same value of δ in both inverters with the same value of C, V_a would be about $0.5\ V_d$ and the commutation power loss would then be about 4.5 times less in the a.c. than in the d.c. commutated inverter.

It was also found that the harmonic content of the load waveforms was a little smaller in the a.c. than in the d.c. commutated inverter and that the motor efficiency, in consequence, was marginally higher.

Although no detailed tests were carried out regenerative braking of the motor was found to be possible. This could be demonstrated by reducing the inverter frequency when the motor was running, whereupon the motor speed quickly followed the setting of the frequency-defining oscillator.

The circuit was only tested on a d.c. supply but it is clear that if a rectified supply were to be used the ripple would need to be small. Because the commutating capacitors charge to supply voltage a single phase rectified supply could not be used without a great deal of smoothing being provided. A three phase rectified supply could be used since the minimum value of this supply voltage would be 0.9 of the mean value but only a limited amount of voltage control by means of delayed firing in the supply rectifier could be tolerated. The supply problem would, perhaps, be made a little easier by the use of the L_x chokes described above.

Despite its advantages over the d.c. commutated inverter the a.c. commutated inverter possessed some serious shortcomings. Its inability to start unaided and its limited range of operation have been discussed before but another feature was that should an S C R fail to turn off, the commutating capaitor would not charge to supply voltage and commutation would fail. In the d.c. commutated inverter, however, there would be a good chance that the fault could be corrected one sixth of a cycle later, since all S C Rs would be reverse biased, provided that the fault current had not risen too far in the meantime.

CHAPTER 9.

CONCLUSIONS.

9.1. General Conclusions.

In this thesis attention has been focussed upon the three-phase bridge inverter circuit, the basic circuit and three variations of it having been studied. The aim in each case was to determine the suitability of each circuit for controlling a three-phase motor, speed control being effected by changing the switching frequency of the inverter. The ultimate aim was to determine whether a scheme incorporating a variable frequency inverter and a conventional three-phase motor would be a feasible proposition.

The first scheme studied utilised thyratrons as the switching elements in the basic three-phase bridge circuit in its synchronous inverter form. For commutation a three-phase a.c. supply was required and so a synchronous motor was used with the inverter. The pulses which were made to fire the thyratrons at the appropriate instants were derived from the a.c. voltage generated by the motor and therefore coincided with certain rotor positions. Consequently the overall characteristics of this system were similar to those of a d.c. separately excited motor. The motor speed could be controlled by variations of the d.c. supply voltage, of the motor field current, and by varying the firing points of the thyratrons relative to the a.c. voltage waveforms. This was analogous to varying the supply voltage and field current and to changing the brush positions in a d.c. motor. The development of this scheme was abandoned because the motor could not be started from standstill and because the degree of advance of the firing pulses necessary to cope with commutation and with the thyratron turn off time introduced instability problems which could not be solved with the inverter circuit in its unsophisticated form.

The next scheme was embarked upon when S C Rs eventually became available and these were used in a three-phase bridge circuit with capacitors connected across the output lines to provide artificial commutation. When an inductive load was connected to the inverter it was found that the capacitor voltages oscillated severely with the load inductance and satisfactory waveforms were obtained only when capacitors large enough to correct the load power factor to unity were used. Since the inverter is a device which in its basic form can only transmit power in one direction this was to be expected. When smaller capacitors were used commutation could be achieved under some circumstances but it could never be guaranteed that the capacitor voltage would be in the correct direction and with sufficient magnitude to effect commutation at all frequencies. With an induction motor load, whose power factor changed with the load, the problem became more difficult. When a motor is operated with constant output torque and constant air gap flux over a range of speeds the motor current must stay constant. Since the turn-off capacity of the inverter (approximately the product of commutating capacitance and capacitor voltage just before commutation) fell with voltage, unless the capacitance was increased as the inverse of voltage, the motor could not be run at very low voltages and frequencies. For these reasons it was concluded that this form of inverter was of no use for induction motor control.

The efficiency of conversion in both circuits above was high since the only power losses occurred in the S C Rs (or thyratrons) during conduction and in the circuit wiring.

The studies into the first two inverter circuits indicated the basic requirements which would need to be satisfied by any inverter intended for supplying an inductive load over a range of frequency and voltage. Firstly provision must be made for power to flow in the reverse direction through the inverter. This simulates the sinusoidal condition in which power flows to and from the supply in different parts of each cycle. Such provision must be made unless power factor correction can be installed as part of the load so that no reverse power flow ever occurs. Secondly, if capacitors are to be used for turning off S C Rs for commutation, they should be charged by some means to a voltage which is independent of the main supply voltage or which increases in proportion to the current flowing in the S C R when it is turned off.

A study of the d.c. switching circuit of Chapter 4 formed a good introduction to the technique of using an auxiliary supply for charging the commutating capacitor and a diode to cope with the load stored energy.

The "d.c. commutated three-phase inverter" was then built using the commutation circuit of the d.c. switch and diodes connected from each load phase to the main supply terminals. These enabled power to flow in both directions between supply and load and, in effect, isolated the load from the commutating circuit. This circuit was proved capable of supplying a load of any power factor with a single value of commutating capacitor, the only provision being that the current was not greater than a certain amount. To cater for changing main supply voltage and frequency it was necessary only to vary the auxiliary supply voltage. This inverter was used to supply an induction motor and it was found that speed control from very low speeds could be achieved simply by varying the inverter switching frequency. The motor torque could be controlled by changing the supply voltage. The ability of the inverter to allow power flow in either direction enabled regenerative braking of the motor to be achieved.

The diodes used to provide a path for reverse power also prevented the voltage across the d.c. choke from reversing after commutation and as a result the energy absorbed by the choke during commutation had to be dissipated as a power loss, a decay circuit being provided to dissipate this power. At high frequencies this power loss became significant compared with the converted power and this resulted in low inverter efficiency. A secondary effect was that the current in the d.c. choke increased with frequency and supply voltages and this reduced the S C R reverse-bias time for turn-off.

Another inverter, the "a.c. commutated three-phase inverter" was then studied. In this circuit the commutation power loss was far smaller and, as a result, the conversion efficiency much higher than in the d.c. commutated inverter. This circuit could not, however, be used at low supply voltages and was not self-starting and could not therefore be used to drive the induction motor at low speeds. A small modification, consisting of a small choke connected in the d.c.

lines of the reverse diode bridge, extended the operating range and improved commutation in this circuit. This was achieved by giving to the commutating capacitor voltage the very desirable characteristic of increasing with load current.

The a.c. output waveforms from an inverter circuit which switches d.c. must inevitably have a high harmonic content. In the d.c. and a.c. commutated inverter circuit it was found that the r.m.s. values of motor current and voltage were about 5% or 6% higher than their fundamental frequency components under typical load conditions. The copper and iron losses in the motor were therefore about 10% or 12% higher than normal which meant that the total motor losses were about 7% or 8% higher than normal. This not only meant that the motor efficiency would be between 1% and 2% lower than normal at rated load and speed but that extra cooling facilities would be needed for the motor.

Harmonic suppression in the inverter output was not considered to be necessary because the drop in motor efficiency due to harmonics was small. It is also difficult to visualise a harmonic suppression circuit which could function over a range of frequencies extending from nearly d.c. to above 50 $^c/s$.

The change in output voltage waveforms with load power factor caused the r.m.s. voltage and its fundamental component to fall with load. Because induction motors are normally designed to operate just over the knee of the magnetisation curve this voltage change proved to be an embarrassment since the d.c. supply voltage which would produce enough a.c. voltage for full-load torque would also produce at light load sufficient voltage to saturate the motor iron. The resulting motor current peaks drawn from the inverter were high enough in many cases to cause difficulty with commutation.

At low speed the motor torque pulsated severely and it was concluded that this was probably caused by the air gap flux's reaching a steady value in a stationary position in each one sixth of a cycle. It was suggested that to overcome the pulsations a motor with very long time constants would be required.

The torque speed curves became steeper, i.e. smaller slip for a given torque, as the motor speed was reduced. It was suggested that this also might be due to the nature of the flux changes in the air gap.

A theoretical analysis developed for each of the three inverters employing either artificial or forced commutation was based on an inductive star-connected load consisting of resistance and inductance in series in each phase. When used on such a load the analyses proved capable of predicting the voltages currents etc. in the circuit to an accuracy of 10% in general, though the approximate formulae for the higher harmonics proved to be rather less accurate. Formulae were derived for determining the ratings of the circuit components and for predicting the efficiency of the inverter for any load at any frequency.

When the inverter was used to supply an induction motor the voltage and current equations given for the R-L load were no longer valid and some aspects of the load voltage and current waveforms could not be explained by treating the motor as as R-L load. However, the commutation circuits, being effectively isolated from the load in the d.c. and a.c. commutated inverters, still obeyed the theory derived for an R-L load and the formulae for S C R and diode ratings were still valid. Since the invertersfunction in excatly the same way whether the load consists of a simple R-L configuration or an induction motor there seems no reason why it should not be possible to calculate the performance of the complete system with an induction motor load. To do this the appropriate equivalent circuit of the motor, valid for such transient conditions as apply in such a case, would have to replace the simple R-L circuit and there is little doubt that a digital computer could be programmed for the purpose.

It can be concluded that a brushless variable speed motor system, using a variable frequency inverter with an inductive motor, is a feasible proposition. An inverter of a type similar to the d.c. commutated inverter would be the most versatile, capable of operating over a very wide speed range andfrom almost any form of d.c. supply. This inverter, in the form used for the investigations described above, would become inefficient at high frequencies unless some means were found for recovering the power lost as a result of the commutation process. It is doubtful whether an inverter efficiency higher than about 95% could be obtained and this, coupled with the 2% (approximate) drop in motor efficiency from normal, would make it difficult to justify the replacement of a single d.c. machine on economic grounds. When the choice is between a Ward Leonard type of control system, involving several machines for precise speed control of only one of them, and an inverter-motor system it is possible that the inverter-motor system would be cheaper and more efficient. Another case in which the inverter-motor system would be preferable to a d.c. machine system is where maintenance of the commutator and control gear might present a problem. Some system would still be needed for controlling the voltage applied to the motor through the inverter and for closely matching the inverter frequency to the motor speed.

9.2. Basic Control Scheme.

Fig. 9.1 shows in block diagram form the basic elements of a control scheme which would be suitable for the control of a squirrel cage induction motor by the d.c. commutated three-phase inverter. The primary supply is converted into suitable d.c. voltages, V_d and V_a, for the main and auxiliary supplies to the inverter. D.C. is converted into three phase a.c. at the required frequency by the inverter and supplied to the motor. The motor rotates at a certain speed and produces torque to drive its load. The control scheme as shown in Fig. 9.1 is intended for a traction application, or any other application where constant torque is required over a wide speed range.

The motor torque depends principally upon the air gap flux and the slip speed. To maintain the air gap flux constant at all speeds the motor voltage should be increased approximately proportionally with frequency. Hence the main d.c. supply voltage is shown to be controlled by a signal representing frequency. When the main d.c. supply voltage is increased the auxiliary supply voltage should also be increased to keep the S C R reverse bias time constant. Hence the auxiliary supply

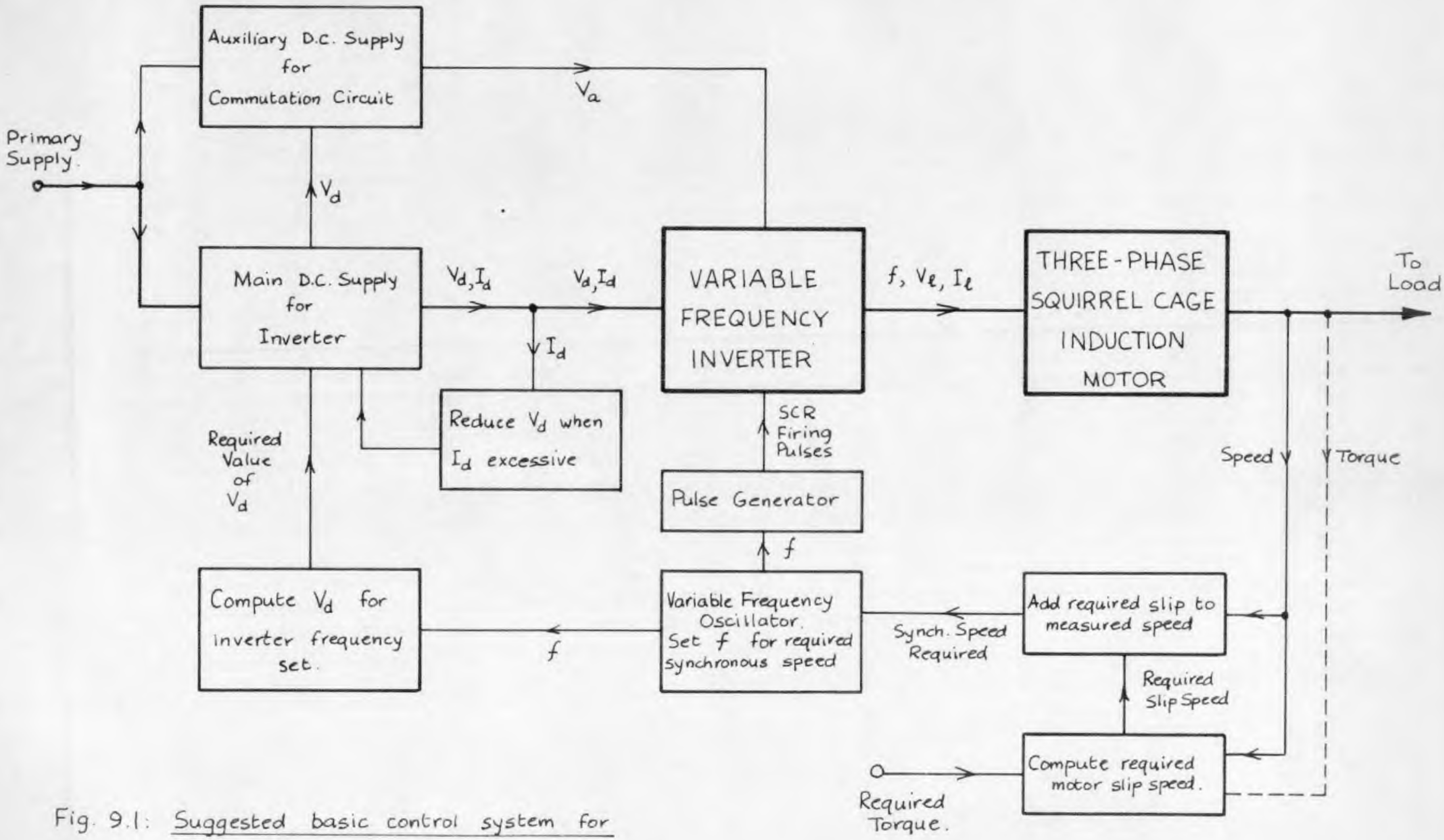


Fig. 9.1: Suggested basic control system for variable speed inverter-motor combination, motor torque being controlled in case shown.

voltage is shown to be controlled by a signal representing V_d. An overload protection circuit is also included which causes V_d to reduce when the inverter input current becomes excessive for any reason.

If constant torque is required, the inverter frequency must be closely controlled according to the actual motor speed. This can be done by measuring the motor speed, adding to it the appropriate required slip speed. The slip speed required for a given torque was found to vary with speed and should thrrefore be computed from the required torque and actual motor speed. The required inverter a.c. frequency is then proportional to the required synchronous speed. The frequency signal is then fed to the pulse generator which produces pulses to fire the inverter S C Rs at this frequency. An alternative method would be to compare the actual motor torque with that required and adjusting the slip speed until the discrepancy became zero. A signal representing actual torque could be derived from a torque measuring coupling or other suitable means. If this method were to be adopted, the control system would possess closed loop feedback and very close control of torque could be achieved.

When maximum supply voltage is attained it would be necessary to limit the slip speed to a certain value. At higher speeds the motor voltage to frequency ratio would fall and the air gap flux and hence the motor torque would fall away inversely proportional to speed and the square of speed respectively. This overall characteristic, i.e. constant torque up to a certain speed and torque varying inversely with speed thereafter, is that which is normally used for traction purposes. To obtain a further characteristic analogous with field weakening of d.c. series traction motors it would probably be necessary to tap the stator winding of the induction motor and operate with a smaller number of stator turns per phase.

If close speed control were required, as in rolling mill, paper mill drives, etc. it would be necessary to compare the motor speed, instead of torque, with that required and adjust the slip speed accordingly. The rest of the control system would still be required in the same form.

9.3. Application to Large System.

In a large system involving the conversion of many tens or hundreds of kilowatts several problems become severe whereas in the small scale system studied above they were hardly significant.

First there is the problem of electrical and magnetic interference between the power circuit and the electronic control circuit. The various types of interaction between the two circuits increase in severity as the currents being switched and the power circuit voltages increase. Careful layout of the power circuits, paying special attention to the avoidance of loops carrying rapidly changing currents and to the position of cables carrying rapdily changing voltages, and effective screening of the control circuits and control leads in the power circuit, become absolutely essential.

Next comes the problem of improving the efficiency of the inverter by reducing the power loss caused by commutation (see section 9.5). Unless some method can be found for reducing or recovering this power loss the inverter efficiency will be prohibitively low at high frequencies and the dissipation of the power will present a cooling problem.

In a large inverter the dissipation of the conduction power losses in S C Rs and diodes can also introduce difficulties. Natural convection cooling would probably be insufficient if there were many S C Rs and diodes and it would probably be necessary to resort to fan cooling or water cooling, using appropriate forms of heat sink.

The higher the inverter voltage and current the higher, in general, becomes the rate of change of current in S C Rs and diodes. This introduces problems both at the start of conduction for the S C Rs and at the end of conduction for S C Rs and diodes. Some means of limiting the rate of increase of current in the S C Rs at turn on becomes necessary, especially with the larger S C Rs. The rate of fall of current in S C Rs and diodes at turn off determines, to a large extent, the quantity of effective charge which must be removed from the junctions as a reverse current. The sudden cessation of this reverse current can cause transient voltages which are very difficult to suppress. A method which can be used for limiting the rate of change of currents for the crucial 10μ Secs or so after turn on and before turn off is to connect a saturating choke in a strategic part of the circuit. Great care should be exercised, of course, in choosing the location for such a choke and ensuring that the sudden cessations of current in the circuit are routed away from it.

At some stage it would be necessary to use S C Rs and diodes in series and in parallel. The problems associated with series operation are concerned with ensuring that all S C Rs and diodes share both steady and transient voltages equally. At turn-on it must be ensured that the slowest S C R to fire is not called upon to support full circuit voltages when all others in series with it have turned on. At turn-off it must be ensured that the first S C R or diode to cease passing reverse recovery current is not called upon to support full reverse voltage plus, in some cases, voltage transients caused by the sudden cessation of reverse current. Capacitors can be of great assistance for such transient voltage sharing in a chain of series diodes. In the case of series S C Rs, however, capacitors, except for very small ones, should not be used directly between anode and cathode because of the damage that can result at turn on. In the case of both S C Rs and diodes some reliable form of surge suppression device (e.g. selenium devices or non-linear resistors) can be made use of to assist in series sharing and voltage limiting. When S C Rs are used in parallel it must be ensured that the S C Rs share the current equally under all conditions. It must also be ensured that when one S C R fires first the voltage across the others does not fall to such a low level that they cannot start to conduct. Centre tapped chokes can be used to ensure reliable firing, and to share the current equally between S C Rs except at low frequencies.

Finally there remains the problem of ensuring that the failure of one device in the circuit does not cause a cascade failure of several others, that the circuit is protected against any possible overload or fault, and that the commutation circuit is thoroughly reliable.

9.4. Rough Outline of a Design for an Inverter to Feed a 200 H.P. Motor.

The following is a rough outline of a preliminary design for an inverter to supply a 200 H.P. three-phase induction motor. The intention is to show how to arrive at suitable ratings for the S C Rs, diodes, commutation circuit and d.c. supplies on the basis of the motor characteristics and the requirements demanded by the application for the system.

The application considered is for traction in which as much torque as possible is obtained from the motor during the acceleration of the train up to a certain speed, after which the torque is allowed to fall as the speed rises further.

9.4.1. Motor Characteristics.

The motor considered is an A.E.I. three-phase squirrel cage induction motor Type NC 7144 having the following characteristics (quoted for a sinusoidal supply):-

Output power :- 200 H.P.

Line voltage :- 440 V at 50 $^{c}/s$.

Line current :- 230 A at full load

Rated full load speed :- 1460 r.p.m.

Full load power factor :- 0.91

Full load efficiency :- 92.5%

Stalling torque :- 2.3 x full load torque

Current at stalling torque :- 3.5 x full load current (approx.)

Power factor at stalling torque :- 0.62 (approx.)

Full load losses in motor.

Stator iron losses :-	1.9 KW
" copper " :-	4.1 KW
Rotor losses :-	3.8 KW
Friction and windage :-	1 KW
Total	10.8 KW

9.4.2. Conditions to be catered for in Inverter Design.

Assume that the motor is operated just below stalling torque where the torque is twice full load torque and the line current is about 2.8 x full load current, i.e. current is about 650 A. Let this condition be sustained up to 50 $^c/s$. and afterwards let the slip be maintained at the same value so that the torque and current fall as the speed increases further.

The worst condition for the inverter is then at the point when the frequency reaches 50 $^c/s$. where the maximum voltage and current coincide.

9.4.3. Calculation of Ratings for Bridge S C Rs and Diodes.

Motor power factor under above conditions at 50 $^c/s$. $\triangleq$ 0.67 for a sinusoidal supply. Hence for inverter supply the power factor would be approximately 10% lower at 0.6.

From Fig. 5.42 the values of I_{in} and I_{gen} for a motor current of 650 A and power factor of 0.6 are

$$I_{in} = 1.02 \times 650 = 664 \text{ A}$$

$$I_{gen} = 0.24 \times 650 = 156 \text{ A}$$

At low speeds I_{in} can show an increase of about 50% to produce the same torque. Hence the maximum value of I_{in} should be taken as 664 x 1.5 i.e. 1000 A.

Hence each bridge S C R should be capable of passing a mean current of 330 A. Two 200 A S C Rs is parallel would suffice, allowing for a certain amount of derating for parallel operation.

If no regeneration is required, the maximum I_{gen} to be allowed for is 156 A. Each bridge diode would therefore require a mean current rating of 52 A. A 70 A diode should be sufficient, allowing for the peaky nature of the current flowing in it.

If regenerative braking is required, the bridge diodes should have the same current rating as the S C Rs and two 200 A diodes in parallel would then be required.

To produce a motor voltage fundamental component of 440 V at 50 $^{c}/s$. at a power factor of about 0.6 the main d.c. supply voltage required would be given by

$$V_d = \frac{440 \text{ V}}{0.65} = 675 \text{ V} \quad \text{(see Fig. 5.37)}$$

If the d.c. commutated inverter were used, V_a would be made equal to V_d to obtain optimum efficiency. Then the maximum reverse voltage applied to the S C Rs would in theory be 2 V_d. Allowing for 50% overshoot this maximum reverse voltage would be 2030 V. To give an additional safety margin the S C Rs should be rated for at least 2400 V. Hence three 800 V S C Rs in series would be required.

The diode ratings should cater for the main supply voltage plus about 50% overshoot plus a safety margin. Single 1500 V diodes should suffice for this purpose.

If the a.c. commutated inverter were used, the S C R voltage ratings could be reduced by about a half unless choke assisted commutation were employed, in which case the S C R voltage rating would be about the same as for the d.c. commutated inverter. The diode voltage rating would be the same in the a.c. commutated inverter as in the d.c. commutated inverter unless choke assisted commutation were to be employed in which case the diode voltage rating would need to be approximately doubled. This is based on the assumption that in the choke assisted commutation circuit the commutating capacitor voltage overshoot would be made equal to main d.c. supply voltage at 50 $^c/s$. at maximum current.

9.4.4. Commutation Circuit.

(a) D.C. commutation.

To determine the size of commutating capacitor required the maximum d.c. currentis required. The peak value of the d.c. current into the inverter is approximately equal to the peak load current, i.e. $650\sqrt{2}$ or 920 A. To allow for the increase in I_{do} with frequency I_{do} should be taken to be 50% larger than this in the first instance. Hence I_{do} should be assumed equal to about 1400 A.

The turn-off time of the S C Rs would probably be about 25 μ Secs but to allow for hole storage, the effects of inductance to be inserted in the circuit, and other contingencies δ should be made at least twice this figure. Hence assume δ to be 50μ Secs. δ is the time taken for the commutating capacitor to charge through $2\ V_a$ with a current of 1400 A flowing. The required value of C is therefore given by

$$C \simeq \frac{50 \times 1400}{1350} = 52\mu F. \quad \text{(see equation (5.5))}$$

For $\hat{I}$ to be no more than 10% greater than I_{do} at its maximum value $\tan^2\phi$ should be greater than 0.2 (see equation (5.2)). Hence the minimum value of L_d can be found from

$$\left(\frac{V_d + V_{CR}}{I_{do}}\right)^2 \times \frac{C}{4L_d} > 0.2$$

This gives $L_d = 250\mu H$ approximately.

The mean current in both auxiliary S C Rs depends upon the inverter frequency. At an assumed maximum frequency of 80 $^c/s$. the mean current in these S C Rs is given by $12\ C_f(V_d + V_a)$ i.e. 67.5 A. Allowing for the pulsed nature of this current S C Rs of 100 A rating should be used.

The voltage rating of CR7 should be $4\ V_d$ plus overshoot and a safety margin, i.e. at least 4500 V. Six 800 V S C Rs should be used in series.

The voltage rating of CR8 should be $2\ V_d$ plus overshoot and a safety margin, i.e. at least 2300 V. Three 800 V S C Rs should be used in series.

The voltage ratings of D_7 and D_8 should also be at least 2300 V and their current rating would need further investigation since this depends upon frequency, the resistance of the d.c. choke decay circuit and the commutation power loss.

The commutation power loss at 50 $^c/s$. as given by $12\ C_f(V_d + V_a)^2$ would be 57 KW. At a converted power of 400 H.P. this would make the inverter efficiency 84% discounting other losses. At higher frequencies the commutation power loss would be higher and the converted power smaller and the efficiency of the inverter would become even lower.

The capacitor should be rated for a voltage of $3\ V_d$, i.e. 2000 V and for a current consisting of 1400 A pulses of duration 100μ Secs twelve times per cycle at the maximum frequency assumed above to be 80 $^c/s$., i.e. a current of 350 A.

The inductance of the auxiliary supply should be such that the re-charging time of the commutating capacitor is substantially less than a twelfth of a cycle at maximum frequency. Hence at 80 $^c/s$. $\pi\sqrt{C\ L_c}$ should be less than about 0.8 m Secs. giving a maximum L_c of about 1.2 mH.

(b) A.C. commutation.

When a.c. commutation is used the frequency range to be covered must be decided upon and the commutating capacitor designed for the lower frequency and voltage.

Let the lowest frequency be 20 $^c/s$. In this case the lowest supply voltage for this commutation circuit to function at is 0.4 x 675 V, i.e. 270 V.

The current to be commutated at 20 $^c/s$. can be taken to be 920 A. The reverse bias time, δ, is the time taken for the commutating capacitor to charge through 270 V with approximately 920 A flowing in it. Hence the value of C required at 20 $^c/s$ to give δ = 50μ Secs. is given approximately by

$$C = \frac{50 \times 920}{270} = 170\mu F. \qquad \text{(see equation (8.10))}$$

At 50 $^{c}/s$. the commutation power loss would be approximately given by $4\, C_f\, V_d^{\,2} = 15.5$ KW. At a converted power of 400 H.P this would give a conversion efficiency of 95% discounting all other losses. At higher frequencies the efficiency would be even less.

The voltage rating of the auxiliary S C Rs should be V_d plus overshoot and safety margin. The current rating should permit 920 A pulses of duration 250μ Secs. (at V_d = 675 V at 50 $^{c}/s$. and above) once per cycle at the highest frequency. Two 30 A, 600 V S C Rs in series should suffice.

The capacitor should be rated for supply voltage, i.e. 675 V, and for a current consisting of 920 A pulses of duration 250μ Secs. twice per cycle at the highest frequency, i.e. an r.m.s. current of about 180 A.

It should be noted that the total V A rating of the auxiliary S C Rs in the d.c. commutated circuit is 9 x 800 V x 100 A, i.e. 720 KVA, whereas in the a.c. commutated circuit the auxiliary S C R VA rating is 12 x 600 V x 30 A, i.e. 216 KVA. The commutating capacitor VA rating in the d.c. commutated circuit is 2000 V x 350 A, i.e. 700 KVA, whereas in the a.c. commutated circuit its total VA rating is 3 x 675 V x 180 A, i.e. 365 KVA. This shows that the a.c. commutated circuit, apart from being more efficient, is more economical in its use of auxiliary S C Rs and commutating capacitance.

9.4.5. Motor Efficiency at 50 $^{c}/s$.

In obtaining twice full-load torque from the motor the losses must be greater than at full-load torque. In addition to these losses the harmonic content of the motor current and voltage must be allowed for.

The friction and windage losses would be the same as at full load for a sinusoidal supply.

The stator iron losses would be about 10% higher than for a sinusoidal supply.

The stator copper loss, because the motor current at twice full-load torque would be about 2.8 times full load current, would be $(2.8)^2$ times that at full load. An additional 10% should be added because of the current harmonic content.

The slip would be about twice full-load motor slip and hence the rotor loss would be approximately four times that at full load.

Hence the motor losses would be as follows:-

Friction and windage :-	1.0 KW
Stator iron losses :-	2.1 KW
Stator copper losses :-	35.5 KW
Rotor losses :-	15.2 KW
Total	53.8 KW

Hence for a motor output power of approximately 400 H.P. the motor efficiency would be 85%.

9.4.6. Overall System Efficiency.

At 50 $^c/s$. a.c. frequency and twice full-load torque the motor efficiency would be about 85%, the efficiency of the d.c. commutated inverter would be 84%, and of the a.c. commutated inverter would be 95%. The overall system efficiency would therefore be 71% and 81% for the d.c. and for the a.c. commutated inverter respectively, taking into account only commutation power losses in assessing inverter efficiency.

9.4.7. Comparison between Inverter-motor Combination and a conventional d.c. Motor Control System of similar Power Rating.

The inverter-motor combination would perform the same function in a variable speed drive as the d.c. motor alone in a conventional system. Under similar load and speed conditions at twice full-load torque a d.c. series motor of similar horse power(the A.E.I. Type 253 traction motor has been taken for comparison) would have an efficiency of about 91%, as opposed to 81% for the induction motor fed from the a.c. commutated inverter. At corresponding full load conditions the induction motor itself would have an efficiency of about 91% while the d.c. motor efficiency would be about 90% but while the induction motor would be more efficient than the d.c. motor the inverter combination would be less efficient.

The calculation of motor efficiency showed that the induction motor is not amenable to running at more than full-load torque because the motor current increase and slip increase are proportionally greater than the increase in torque. This results in substantially greater motor losses and lower motor efficiency.

A comparison between the weight of the induction and the d.c. motor would be hardly fair since the Type 253 motor is a self ventilated traction motor whereas the Type VC 7144 motor is an industrial motor designed for fan cooling. It is nevertheless interesting to note that the weights are 1750 lb for the induction motor and 3720 lb for the d.c. motor. Both motors have similar overall dimensions.

9.5. Suggestions for Further Work.

The analyses carried out on the inverter described in this thesis were based on a simple R-L load. For the analysis of the operation of an induction motor with the inverter it would be necessary to determine the motor's equivalent circuit which would be valid under the transient conditions met in this method of operation. Having established some such equivalent circuit or set of equations to represent the motor faithfully it should then be possible to apply methods of analysis similar to those developed above to the complete system. It would undoubtedly be necessary to use a computer in this analysis.

A particularly worthwhile subject for study would be the improvement of the commutation process in the inverter. Some method of reducing the power loss due to commutation will need to be found before the inverter-induction motor scheme can be seriously considered as a viable proposition. A method, suggested to the author by a colleague, for recovering part of the power loss due to commutation in the d.c. commutated inverter is shown in Fig. 9.2.

In Fig. 9.2. should be noted the rearrangement of the d.c. choke decay circuit, to make excess choke current and reverse bridge diode current flow through resistor R_x, and the inclusion of another coil on the same core as the d.c. choke but with N times a s many turns as each half of the d.c. choke. The additional coil is connected through diodes D_x between the main supply terminals in such a sense that when commutation takes place D_x is reverse biased. Many diodes in series would be required for D_x since the turns ratio N is large. After commutation the excess choke current and reverse diode bridge current flow in R_x. If the voltage drop in R_x reaches $\frac{1}{N} V_d$ diodes D_x conduct and current is returned to the supply. The turns ratio N should be so chosen that at the highest voltage and frequency the mean voltage applied to the choke by virtue of the conduction of D_x should equal the mean voltage applied during commutation, both mean values being taken over a sixth of a cycle. A substantial recovery of commutation power loss has been claimed for this circuit.

It would still be preferable, however, that a reliable but loss-free commutation circuit with some means incorporated to increase the turn off capacity in proportion to current should be developed. A possible method was indicated by the choke assisted a.c. commutation circuit of section 8.6.

For high power drives many more than six S C Rs and diodes would be required in the inverter bridge circuits. It would be useful if a study could be made of the various ways in which the multiplicity of

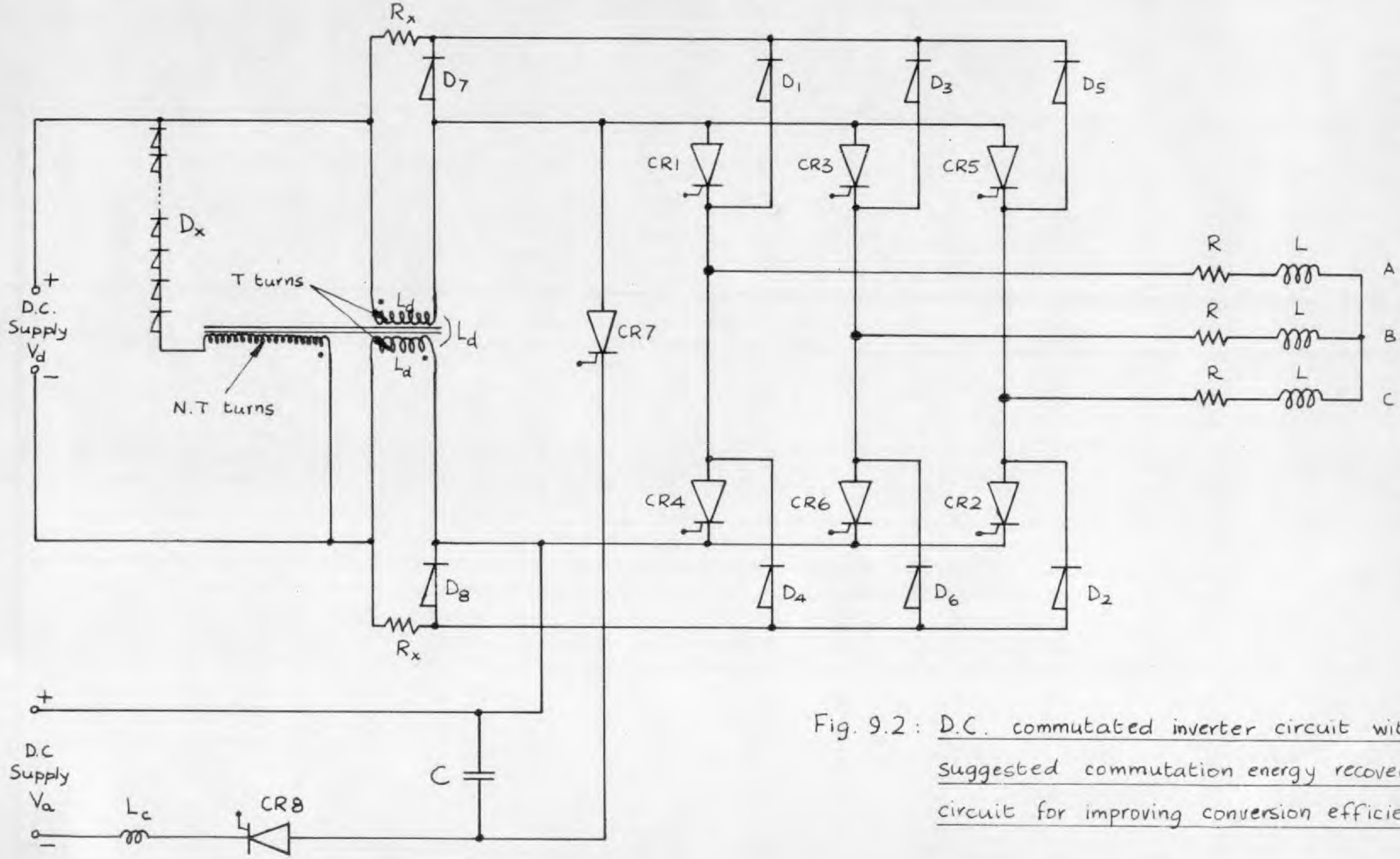


Fig. 9.2 : D.C. commutated inverter circuit with suggested commutation energy recovery circuit for improving conversion efficiency.

rectifiers could be employed. It is possible that instead of one large inverter bridge it would be desirable to use several smaller bridges. If the smaller bridges were operated out of phase with each other, it might be found that the alternating current produced would contain a smaller harmonic content than would be the case if a single bridge were to be used.

APPENDIX A.

THEORY OF OPERATION OF THREE PHASE INVERTER OF CHAPTER 3 ON RESISTANCE LOAD.

A.1. Derivation of Current and Voltage Equations for the Sixth of a Cycle between Instants t_2 and t_3.

Fig. A.1 shows the state of the circuit, in its Laplace operational form, between instants t_2 and t_3. Current is being commutated from phase B to phase C. CR1 and CR2 are conducting and hence phases A and C are connected directly to the inverter input terminals while phase B is connected via two commutating capacitors.

E_1, E_2 and E_3 are the values of V_{ab}, V_{cb} and V_{ac} immediately before and after instant t_2 and I_o is the initial value of the current I_1 in the d.c. circuit. pL_d and $\frac{1}{pC}$ are the operational impedances of the choke L_d and each commutating capacitor. The small resistors and capacitors used for transient voltage suppression have been omitted from Fig. A.1 and their effect neglected.

It is assumed that when CR2 is triggered it at once becomes a short circuit between anode and cathode, at the same time causing CR6 to turn off and become an open circuit between anode and cathode. Consequently all the S C Rs in the inverter circuit have been omitted from Fig. A.1., being replaced by solid connections or open circuits.

I_a, I_b, I_c are the currents in load phases A, B and C. I_1, I_2, I_3 and I_4 are as indicated in Fig. A.1.

The circuit may now be analysed by the method shown below.

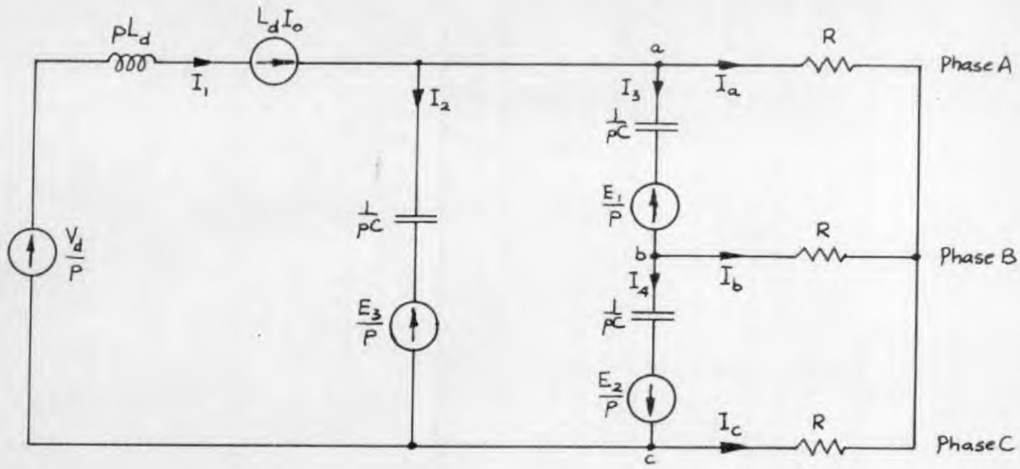


Fig. A.1: Operational form of inverter circuit valid between instants t_2 and t_3.

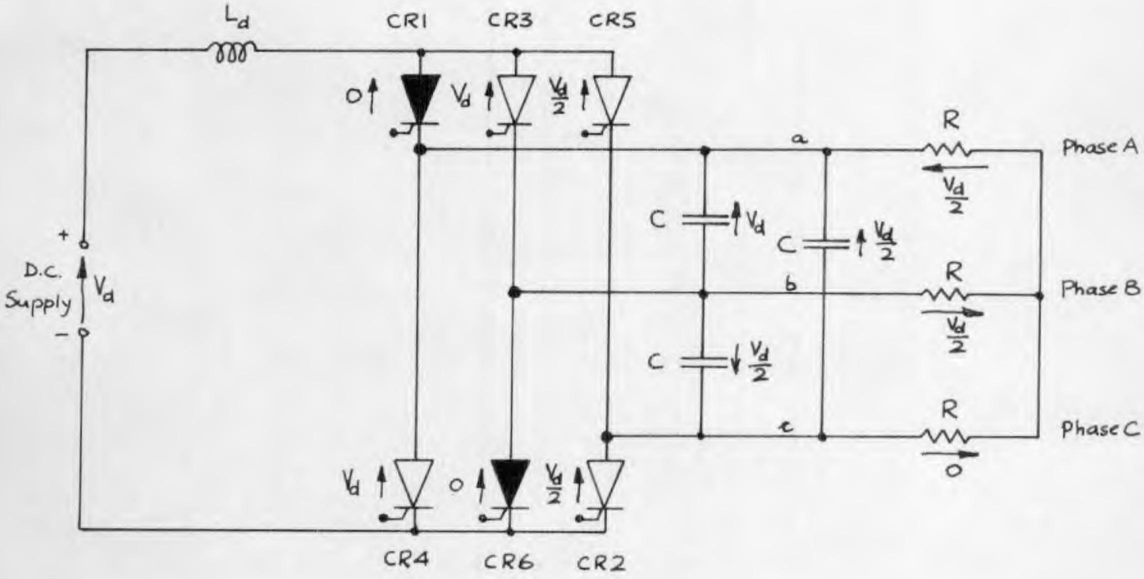


Fig. A.2: State of circuit immediately before instant t_2 in low frequency case.


conducting SCR


non-conducting SCR

Since E_1, E_2 and E_3 are the initial values of V_{ab}, V_{cb} and V_{ac},

$$E_1 - E_2 - E_3 = 0 \tag{A.1}$$

Applying Kirchhoff's Law to the nodes and meshes of the circuit,

$$I_a = I_1 - I_2 - I_3 \tag{A.2}$$

$$I_b = I_3 - I_a \tag{A.3}$$

$$I_c = -I_1 + I_2 + I_4 \tag{A.4}$$

$$(I_2 - I_3 - I_4).\frac{1}{pC} = \frac{1}{p}(E_1 - E_2 - E_3)$$

$$\text{i.e.} \quad I_2 - I_3 - I_4 = 0 \tag{A.5}$$

$$(I_a - I_b)R - I_3.\frac{1}{pC} = \frac{E_1}{p} \tag{A.6}$$

$$I_4.\frac{1}{pC} + (I_c - I_b)R = \frac{E_2}{p} \tag{A.7}$$

$$I_1.pL_d + (I_a - I_c)R = \frac{V_d}{p} + L_d I_o \tag{A.8}$$

$$I_2.\frac{1}{pC} + (I_c - I_a)R = -\frac{E_3}{p} \tag{A.9}$$

Substituting for I_a, I_b, I_c, dividing by R, and re-arranging, equations (A.6), (A.7), (A.8), (A.9) become

$$I_1 - I_2 - I_3\left(\frac{1}{pRC} + 2\right) + I_4 = \frac{E_1}{pR} \tag{A.6}$$

$$I_1 - I_2 + I_3 - I_4\left(\frac{1}{pRC} + 2\right) = -\frac{E_3}{pR} \tag{A.7}$$

$$I_1\left(\frac{pL_d}{R} + 2\right) - 2I_2 - I_3 - I_4 = \frac{V_d}{pR} + \frac{L_d I_o}{R} \tag{A.8}$$

$$2I_1 - I_2\left(\frac{1}{pRC} + 2\right) - I_3 - I_4 = \frac{E_3}{pR} \tag{A.9}$$

Subtracting equation (A.6) from equation (A.7),

$$I_3 - I_4 = -\frac{C(E_1 + E_2)}{3pRC + 1} \tag{A.10}$$

Eliminating I_1 from equations (A.8) and (A.9) and substituting $I_2 = I_3 + I_4$ from equation (A.5),

$$I_2 = I_3 + I_4 = \frac{pCL_d(2RI_o - E_3) + 2RC(V_d - E_3)}{3p^2 RCL_d + pL_d + 2R} \tag{A.11}$$

Then from equation (A.9),

$$I_1 = \frac{E_3}{2pR} + \frac{(3pRC + 1)(pL_d\left[2RI_o - E_3\right] + 2R\left[V_d - E_3\right])}{2pR(3p^2RCL_d + pL_d + 2R)} \tag{A.12}$$

From equations (A.10) and (A.11)

$$I_3 = \frac{pCL_d(2RI_o - E_3) + 2RC(V_d - E_3)}{2(3p^2RCL_d + pL_d + 2R)} - \frac{C(E_1 + E_2)}{2(3pRC + 1)} \tag{A.13}$$

$$I_4 = \frac{pCL_d(2RI_o - E_3) + 2RC(V_d - E_3)}{2(3p^2RCL_d + pL_d + 2R)} + \frac{C(E_1 + E_2)}{2(3pRC + 1)} \tag{A.14}$$

Then,

$$V_{ab} = \frac{E_1}{p} + I_3 \cdot \frac{1}{pC}$$

$$= \frac{E_1}{p} + \frac{pL_d(2RI_o - E_3) + 2R(V_d - E_3)}{2p(3p^2RCL_d + pL_d + 2R)} - \frac{E_1 + E_2}{2p(3pRC + 1)} \tag{A.15}$$

$$V_{ac} = \frac{E_3}{p} + I_2 \cdot \frac{1}{pC}$$

$$= \frac{E_3}{p} + \frac{pL_d(2RI_o - E_3) + 2R(V_d - E_3)}{2p(3p^2RCL_d + pL_d + 2R)} \tag{A.16}$$

and $V_{bc} = -\frac{E_2}{p} + I_4 \cdot \frac{1}{pC}$

$$= -\frac{E_2}{p} + \frac{pL_d(2RI_o - E_3) + 2R(V_d - E_3)}{2p(3p^2RCL_d + pL_d + 2R)} + \frac{E_1 + E_2}{2p(3pRC + 1)} \qquad (A.17)$$

Inverting these operational equations to obtain the instantaneous time dependent values of current and voltage, the following equations may be obtained:-

$$i_1 = \frac{V_d}{2R} - \frac{(\alpha-\beta)[(\alpha+\beta)K_2 - K_1]}{K_3\beta(\alpha+\beta)} e^{-(\alpha+\beta)t} + \frac{(\alpha+\beta)[(\alpha-\beta)K_2 - K_1]}{K_3\beta(\alpha-\beta)} e^{-(\alpha-\beta)t} \qquad (A.18)$$

$$i_2 = \frac{(\alpha+\beta)K_2 - K_1}{K_5\beta} e^{-(\alpha+\beta)t} - \frac{(\alpha-\beta)K_2 - K_1}{K_5\beta} e^{-(\alpha-\beta)t} \qquad (A.19)$$

$$i_3 = \frac{(\alpha+\beta)K_2 - K_1}{2K_5\beta} e^{-(\alpha+\beta)t} - \frac{(\alpha-\beta)K_2 - K_1}{2K_5\beta} e^{-(\alpha-\beta)t} - \frac{E_1+E_2}{K_6} e^{-2\alpha t} \qquad (A.20)$$

$$i_4 = \frac{(\alpha+\beta)K_2 - K_1}{2K_5\beta} e^{-(\alpha+\beta)t} - \frac{(\alpha-\beta)K_2 - K_1}{2K_5\beta} e^{-(\alpha-\beta)t} + \frac{E_1+E_2}{K_6} e^{-2\alpha t} \qquad (A.21)$$

$$v_{ac} = V_d - \frac{(\alpha+\beta)K_2 - K_1}{K_4\beta(\alpha+\beta)} e^{-(\alpha+\beta)t} + \frac{(\alpha-\beta)K_2 - K_1}{K_4\beta(\alpha-\beta)} e^{-(\alpha-\beta)t} \qquad (A.22)$$

$$v_{bc} = \frac{V_d}{2} - \frac{2E_1 - E_3}{2} e^{-2\alpha t} - \frac{(\alpha+\beta)K_2 - K_1}{2K_4\beta(\alpha+\beta)} e^{-(\alpha+\beta)t} - \frac{(\alpha-\beta)K_2 - K_1}{2K_4\beta(\alpha-\beta)} e^{-(\alpha-\beta)t} \qquad (A.23)$$

and

$$v_{ab} = v_{ac} - v_{bc} \qquad (A.24)$$

where
$$K_1 = 2R(V_d - E_3)$$
$$K_2 = L_d(2RI_o - E_3)$$
$$K_3 = 4RL_d$$
$$K_4 = 6RCL_d$$
$$K_5 = 6RL_d$$
$$K_6 = 6R$$
$$\alpha = \frac{1}{6RC}$$
$$\beta = \sqrt{\frac{1}{36R^2C^2} - \frac{2}{3C\,L_d}}$$

i_a, i_b, i_c may then be found by substituting for i_1, i_2, i_3, i_4 in

$$i_a = i_1 - i_2 - i_3 \tag{A.25}$$
$$i_b = i_3 - i_4 \tag{A.26}$$
$$i_c = -i_1 + i_2 + i_4 \tag{A.27}$$

A.2. Determination of I_o, E_1, E_2 and E_3.

Before the equations for the currents and voltages in the circuit can be obtained the values of I_o, E_1, E_2 and E_3 must be found. When the inverter frequency is low these values can be readily obtained but at higher frequencies their determination is a little more involved.

A.2.1. Low Inverter Output Frequencies.

At low inverter output frequencies the state of the circuit just before instant t_2 is as shown in Fig. A.2. The capacitor currents have become negligible and the other circuit currents have reached steady values. The current in the choke and the capacitor voltages shown in Fig. A.2 are therefore the required values of I_o, E_1, E_2 and E_3.

i.e. $I_o = \frac{V_d}{2R}$, $E_1 = V_d$, $E_2 = \frac{V_d}{2}$, $E_3 = \frac{V_d}{2}$.

Hence $K_1 = R\,V_d$ and $K_2 = \frac{1}{2} L_d V_d$

The current and voltage equations may now be found for the sixth of a cycle between t_2 and t_3 by straightforward substitution of the circuit parameters in equations (A.18) to (A.27).

A.2.2. Higher Inverter Output Frequencies.

At higher inverter output frequencies the state of the circuit just before instant t_2 is not as shown in Fig. A.2. It cannot be assumed that any current or voltage has attained a steady value and it is therefore necessary to calculate the initial values I_o, E_1, E_2 and E_3. This calculation can be based on equations (A.18), (A.22) and (A.23).

In equations (A.18), (A.22) and (A.23) K_1 and K_2 are functions of I_o and E_3. The equations may therefore be written as

$$i_1 = F_1(I_o, E_3, t) \qquad (A.28)$$

$$v_{ac} = F_2(I_o, E_3, t) \qquad (A.29)$$

$$v_{bc} = F_3(I_o, E_1, E_3, t) \qquad (A.30)$$

The d.c. choke has the same initial current I_o at the end of every sixth of a cycle. The initial capacitor voltages E_1, E_2 and E_3 are also the same at the end of every sixth of a cycle, though appearing across the individual capacitors in a set sequence. If t is put equal to $\frac{T}{6}$, where T is the duration of a whole cycle, the value of i_1 given given by equation (A.28) must be equal to I_o and the values of v_{ac} and v_{bc} given by equations (A.29) and (A.30) must be equal to E_1 and E_3 respectively.

Hence

$$I_o = F_1(I_o, E_3, \tfrac{T}{6}) \qquad (A.31)$$

$$E_1 = F_2(I_o, E_3, \tfrac{T}{6}) \qquad (A.32)$$

and

$$E_3 = F_3(I_o, E_1, E_3, \tfrac{T}{6}) \qquad (A.33)$$

Equations (A.31), (A.32), (A.33) reduce to linear simultaneous equations from which I_o, E_1, E_3 and hence E_2 can be readily obtained.

The current and voltage equations may then be found for the sixth of a cycle between instants t_2 and t_3 by substitution of these initial current and voltage values and the circuit parameters in equations (A.18) to (A.27).

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