THE ELECTRICAL PROPERTIES OF POLYCRYSTALLINE SEMICONDUCTOR FILMS

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ABSTRACT

The nucleation and structural details of evaporated layers of the compound semiconductors InSb and PbTe have been studied.

To evaluate the electrical behaviour of these polycrystalline films as grown on amorphous substrates both resistivity and Hall voltage have been measured both as a function of deposition conditions and of temperature.

Dynamic measurement of the high frequency differential capacitance associated with the surface space charge region on these materials when in contact with anodically formed Al_2O_3 has enabled the trapping behaviour of the surface region of these semiconductors to be determined across essentially the entire band gap. When combined with the results of field effect measurements a measure of the specularity to current carriers of these interfaces has also been obtained.

Theoretical analysis of the surface measurements has required, for these narrow band gap materials, the use of degenerate statistics and in the case of InSb the inclusion of terms to account for the large non-parabolicity of its conduction band. Because of the complexity of the resulting expressions their evaluation has been carried out on an IBM 7090 computer.

Correlation between the surface and Hall results has been obtained and in the case of PbTe, as a result of its inordinately large value of permittivity, it is believed that the apparent intrinsic behaviour results from compensation of the bulk dopant by surface states.

Thin film field-effect transistors have been fabricated from both InSb and PbTe. Both materials have proved reasonably successful in this respect but in the case of PbTe its large temperature sensitivity has indicated the inapplicability of its commercial exploitation. Dielectric trapping, the degrading effects of high resistance channel contacts and minority carrier conduction have been studied, the last apparently setting a fundamental limit on the device application of InSb.

ACKNOWLEDGEMENTS

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No group can work successfully in isolation and contact with the Plessey Organisation, English Electric and the Associated Electrical Industries is gratefully acknowledged.

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TABLE OF CONTENTS

to SYLVIA and KARIN

CHAPTER ONE

INTRODUCTION

1.1 Field Effect Transistor Development

In 1928 Lilienfeld (L1) filed a patent for a semiconductor active device employing a thin layer of CuS whose electrical conductivity was modulated by the application of a normal electric field. This device, later to be called the field effect transistor (FET), marked a turning point in the development of electronics. Until that time amplification of electric signals had relied on the modulation of electron trajectories within a gaseous medium. This device relied upon their modulation within a solid.

Predictably, the expected behaviour of this early solid state device did not emerge in practice and it was while attempts were being made to remedy this that bipolar transistor action, namely minority carrier injection, was discovered by Bardeen and Brattain at the Bell Laboratories (B7). Developments in this field rapidly overshadowed work on the surface controlled device and it was not until the 1950's that the early interest in the FET was again revived.

The FET is essentially a capacitor, one plate of which is replaced by a material whose carrier concentration is sufficiently low to enable an appreciable percentage change in carrier density to be capacitatively induced. A semiconductor can satisfy this requirement but in addition, transistor action requires the modulation of the conductance of the layer. This can only occur if the induced charges are mobile. In the early field effect devices this was not so. Much of the induced charge became virtually immobilized in defects associated with the surface region of the semiconductor. These traps, which will be considered later, can arise for a number of reasons but en masse are referred to as 'surface states'.

Attempts to reduce the density of these defects met with little success and in an effort to circumvent rather than overcome the problem Shockley, in 1952 (S1) ingeniously proposed a device in which the capacitive properties of a p-n junction, rather than a dielectric, were exploited. In this case the charge would be modulated in a region remote from the semiconductor surface and as a result the effect of surface trapping would become unimportant.

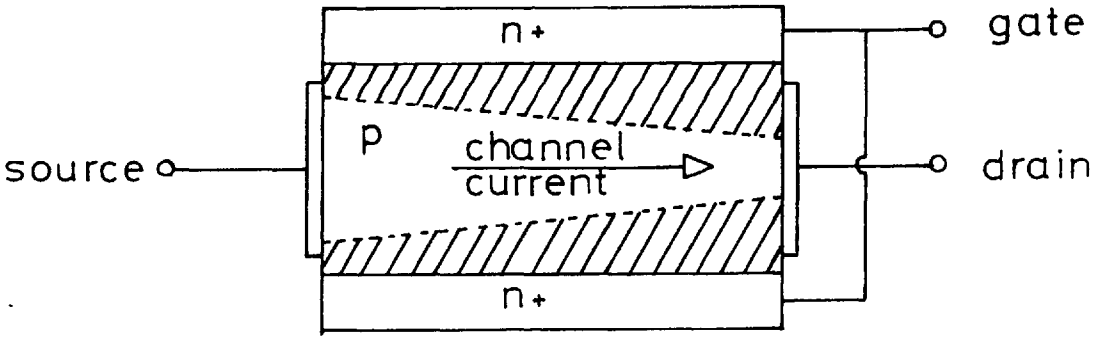
The form of this junction device as proposed by Shockley, together with that of the surface channel FET, is shown in figure (1).

Successful junction devices were subsequently fabricated in Ge (D1) and Si (P1) and once again interest in a surface controlled FET diminished.

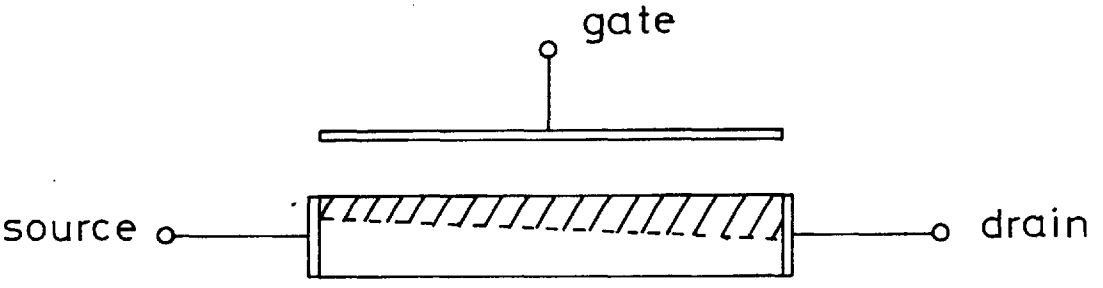
However, in 1961 Weimer (W1) succeeded, in an evaporated layer of CdS, in producing sufficient conductivity modulation at last to warrant the claim to a truly surface controlled FET. Following on this success a large number of workers (S2, W2, K1, S3) obtained appreciable transistor action in a variety of semiconductors, the majority of which were prepared by vacuum evaporation. This method of fabrication has not as yet however resulted in a commercially viable device owing to irreproducibility and instability of the characteristics but an alternative method of fabrication, termed the planar technique (K10), has had considerable success. This method, which relies upon the high stability of a thermally grown oxide on single crystal Si has resulted in a commercial device termed the MOST (Metal - Oxide - Silicon Transistor (H1)).

These MOSTs, like bipolar and junction FETs, are compatible with current integrated circuit technology and are at present employed in commercial microcircuits. The complementary technique of thin film fabrication

Figure 1



(a) The Junction Field-Effect Transistor



(b) The Surface Channel or Insulated Gate Field-Effect Transistor

Space charge regions are shown cross-hatched

however still has to rely, for its active components, on hybrid techniques whereby transistors and diodes prepared by alternative methods are bonded on to the passive thin film patterns. The desirability of a compatible thin film transistor has resulted in a vast effort (summarized in table (i)) being expended over the last seven years on thin film transistor (TFT) research. Notable successes have been achieved (W3, B1, W4, S4) but even though the field effect transistor, of all TFT*, offers most promise of success, to date no viable device has emerged.

From the vast literature on this thin film device it appears somewhat surprising that very few measurements of an unambiguous nature have been made of the relevant electrical parameters (W5, W6). The present work is in the nature of an attempt to remedy this situation for the two semiconductors PbTe and InSb. These materials have been chosen because of their inherent high mobility and hence suitability (section 3.2) for device application and also because of the relatively large amount of bulk data already available.

Before proceeding to consider the FET in further detail in chapter III it will be advantageous to review briefly the relevant properties of these two materials, additional basic concepts being treated separately in chapter II.

1.2 The III - V Compound InSb

The intermetallic compound InSb is perhaps the most extensively studied of all compound semiconductors. This is largely due to the fact that it can be prepared rather easily and partly due to its high value of electron

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* As a result of the low minority carrier lifetime observed in evaporated layers devices relying upon minority carrier effects are essentially unsuitable. In addition to the FET, devices employing majority carrier conduction include (L2) the metal base transistor, the dielectric triode and the tunnel emission amplifier.

Table (i)

Surface Channel Field-Effect Transistor Developements

Year	Active Material	Reference	Comment
1962	CdS	Weimer. Proc.IRE	TFT on amorphous substrate
1963	Si	Hofstein & Heiman Proc.IEEE	Single crystal Si (MOST) device
	CdSe	Shallcross Proc.IEEE	
1964	Te	Weimer. Proc.IEEE	
	SnO & In_2O_3	Klasens & Koelmans SSE	Gate electrode used to mask source to drain gap
1965	PbS	Pennebaker SSE	Poorly saturating characteristics
	InSb	Frantz. Proc.IEEE	Non saturating behaviour
	PbTe	Skalski. Proc.IEEE	Epitaxial growth on cleaved NaCl giving poor characteristics
	Si	Salama & Young Proc.IEEE	Si evaporated onto sapphire by electron beam heating
	GaAs	Becke, Hall & White SSE	Single crystal GaAs device
1966	CdS	Conragan & Muller SSE	Single crystal CdS device
	GaAs	Mead. Proc.IEEE	Schottky barrier for gate isolation
	CdS	Zuleeg & Wieder SSE	Fabricated on ferroelectric TGS giving bistable device
	CdS	Witt et.al. Proc.IEEE	Silk screened CdS
	Te	Heyman & Heilmeier Proc.IEEE	Bistable device on TGS
	InAs	Brody & Kunig Appl. Phys. Letters	Three temperature evaporation giving $\mu_{fe} \sim$ 1800 $cms^2/v\text{-}sec.$
1967	ZnTe & InSb	Spinulescu-Carnaru Electronics Letters	μ_{fe} values as large as 18000 $cms^2/v\text{-}sec.$ in InSb
	GaAs	Becke & White Electronics	Single crystal GaAs devices superior to Si MOSTs
	CdS	Heime. SSE	Chemically sprayed semi - conductor

mobility. These properties remain largely true for the material in thin film form also.

1.2.1 Crystal Structure

InSb crystallizes with the Zinc Blende structure, namely interpenetrating face centered cubes of In and Sb displaced relative to each other by $\frac{1}{4}$ the body diagonal along the diagonal.

The bonding, as in all III - V compounds, is essentially covalent in nature (H11).

1.2.2 Band Structure

Of all the III - V compounds InSb has the smallest band gap. The most recent data on which gives (M6):

$$E_g = 0.25 - 2.8 \times 10^{-4} T \text{ eV}$$

the transition being a direct one at k = 0.

The valence band consists of a light and heavy hole component almost degenerate at k = 0. The former is symmetrical about k = 0 and hence is represented in k space by spherical constant energy surfaces. Its E - k relationship is however non-parabolic. The heavy hole maxima occur at small values of k along the $\langle 111 \rangle$ crystal directions being only $\sim 10^{-3}$ eV above the zero k value. This heavy hole band may be taken, to a good approximation, to be parabolic but unlike the light component does not have spherical constant energy surfaces.

The conduction band of InSb is its most distinguishing feature. The band is spherical but highly non-parabolic with a remarkably small effective mass. Its value of course is energy dependent but at $k \cong 0$ it has a value of $0.013\ m_o$. This exceptionally small value of electron effective mass has

three important consequences:

(i) For temperatures greater than ~ 200°K even intrinsic material has a degenerate electron distribution.

(ii) The resulting low density of states in the conduction band requires the non-parabolicity of the band to be taken into account for all cases where $n \gtrsim 5 \times 10^{15}$ cms^{-3} if large errors are to be avoided (S5).

(iii) The possibility exists of a very large value of electron mobility which is in fact observed in practice. Values of 77,000 cms^2/v - sec. at 300°K for $N_d \sim 10^{16}$ cms^{-3} and 620,000 cms^2/v - sec. at 78°K for $N_d = 1.7 \times 10^{14}$ cms^{-3} have been measured (M6) with a temperature dependence of the form

$$\mu_e \propto T^{-1.66}$$

being obeyed in most cases.

This temperature behaviour is believed to be a result of scattering by polar lattice modes at temperatures above 200°K whereas at lower temperatures a combination of acoustic phonons and ionized impurity scattering seems more likely (M6).

The hole mobility at 300°K is typically ~ 700 cms^2/v - sec.

1.2.3 Evaporated Layers

Preparation of evaporated layers of compounds so as to retain their bulk stoichiometry is difficult in the case where the component elements have widely differing values of vapour pressure. This is a result of the fact that preferential evaporation of the more volatile component is likely to occur from either the source or the substrate leading to a deposit rich in the other element. Current techniques to overcome this problem include

(i) Evaporation to completion of the source charge (P11).

(ii) Evaporation of the elemental components from separate sources (3 temperature method) (G6).

(iii) Flash evaporation (M1).

A vast improvement in both carrier concentration and mobility seems possible however in films prepared by any of the above methods if, subsequent to deposition, the film is protected by an evaporated layer of dielectric or by a self formed oxide and then annealed to a temperature approaching its melting point (C1, J1)*. In this way InSb films with electron mobilities as large as 5×10^4 cms^2/v - sec. have been prepared.

An even more successful technique was recently reported by Teede. By locally melting evaporated layers of InSb by means of electron bombardement he succeeded, on amorphous substrates, in achieving galvanomagnetic properties within 5% of their bulk value (T1).

Apart from two reports of p-type films (D2, P2) which can be ascribed to Cu doping, films of InSb evaporated in reasonably clean conditions, are invariably n-type, even at low temperatures.

1.3 The IV - VI Compound PbTe

Interest in InSb thin films arose out of a desire to reproduce in this form a material exhibiting the high purity (second only to Si and Ge) and mobility which was attainable in the bulk.

In the case of the lead salts however it became apparent that in thin film form they possessed a property which was essentially masked in the bulk

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* This high temperature is necessary in the case of InSb as a result of the small rates of self diffusion of In and Sb (H2). The encapsulant in this case prevents re-evaporation of the Sb.

This was their pronounced photoconductive efficiency.

As early as 1904 Bose (B2) had observed photovoltaic effects in natural PbS crystals (Galena) and in 1917 Case (C5) reported on photoconductive phenomena in the same material. These effects, however, were not so pronounced as those observed in the 1930's in evaporated polycrystalline layers of the lead salts (A1). These layers, as evaporated, were generally n-type and to maximize the photoconductive response it was found necessary to subject them to a subsequent oxygen treatment. Oxygen, acting as an acceptor, drives these films p-type and the maximum photoresponse was found to occur near the intrinsic condition where the dark resistance is a maximum (B6, H9).

The mechanism of photoconductivity (B3, B4) in these layers is still open to question. Opinion seems to be divided between a mobility modulating mechanism associated with internal barriers such as p-n junctions or oxide intergrain layers and a carrier density effect. The latter model rests on the fact that oxygen, acting as an acceptor, can increase the photoexcited hole lifetime by trapping electrons in a non-recombinative state. Because of the narrow band gap of these materials the photoresponse extends to low frequencies in the infra-red region of the spectrum.

1.3.1 Crystal Structure

The lead salts crystallize with a NaCl structure i.e. two interpenetrating face centered cubes displaced $\frac{1}{2}$ a cube edge relative to each other along the cube side.

Because of this structure the bonding has generally been assumed to be predominantly ionic. Results reported by a number of workers (D5, Z8, J4) have however thrown some doubt upon the validity of this assumption.

In contrast with InSb it has proved remarkably difficult to produce

stoichiometric crystals of the lead salts owing to the incompatible conditions required for crystal growth and stoichiometric composition. Component deficiencies in the form of lattice vacancies typically lead to carrier densities $\sim 10^{17}$ cms^{-3}. (InSb can be prepared with impurity concentrations in the range of $\sim 10^{14}$ cms^{-3}) Pb and Te deficiencies lead respectively to p and n-type conduction.

1.3.2 Band Structure

From a large amount of experimental (S6, D3, M2, C2) as well as theoretical data (P3, P4, K2) it appears that both the conduction and valence band of PbTe consist principally of 4* prolate ellipsoids of revolution located at the zone boundaries along the $\langle 111 \rangle$ crystal directions together with secondary spherical extrema at k = 0. In the case of the valence band both of these extrema are believed to be highly non-parabolic, the effective mass of the spherical k = 0 band being much larger than that of the ellipsoids.

Measurements of the minimum energy gap by Tauber et. al. (T1) indicate it to increase linearly with temperature up to approximately 350°K with a variation given by

$$E_g = 0.19 + 4.1 \times 10^{-4} T \text{ eV}$$

Above 400°K it remains essentially constant at 0.36 eV.

This behaviour has been interpreted (T2, A2, C3) in terms of a temperature dependent positioning of the valence band ellipsoids with respect to the conduction band edge. At low temperatures the holes are predominantly in the ellipsoids whereas above $\sim$ 400°K most are located in the spherical extremum. This model, depicted schematically in figure (2), is consistent with

* Although there are 8 axes in the $\langle 111 \rangle$ set, diagonally opposed locations at the zone boundary are equivalent. This equivalence will result in 4 rather than 8 band extrema when these occur at the zone boundary.

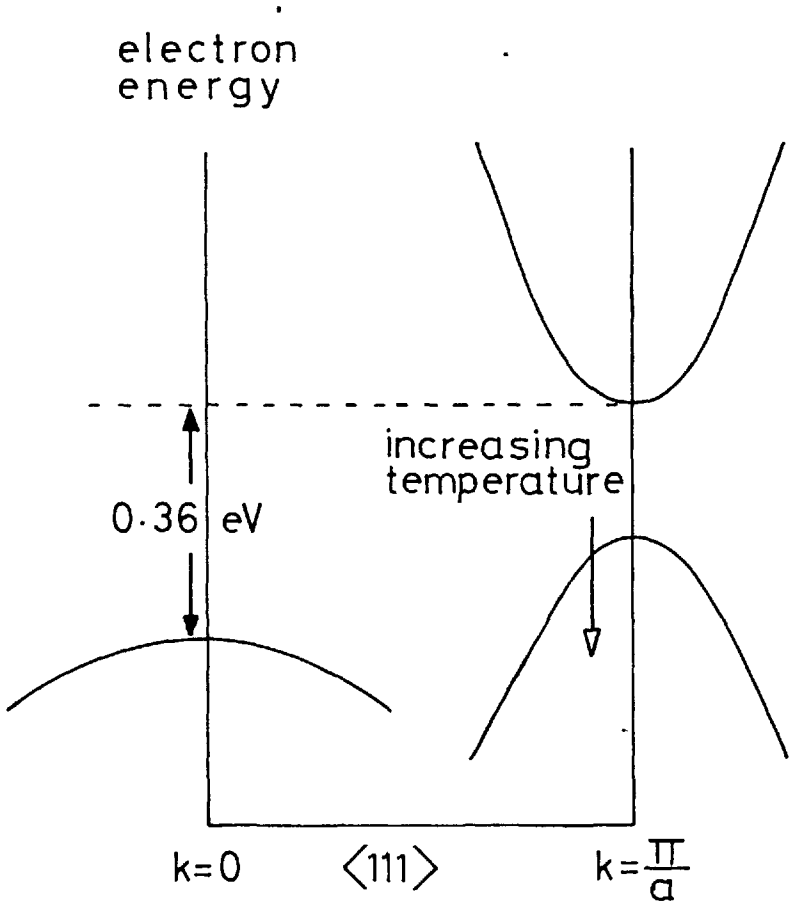

Figure 2

Schematic Representation of the Band Structure of PbTe

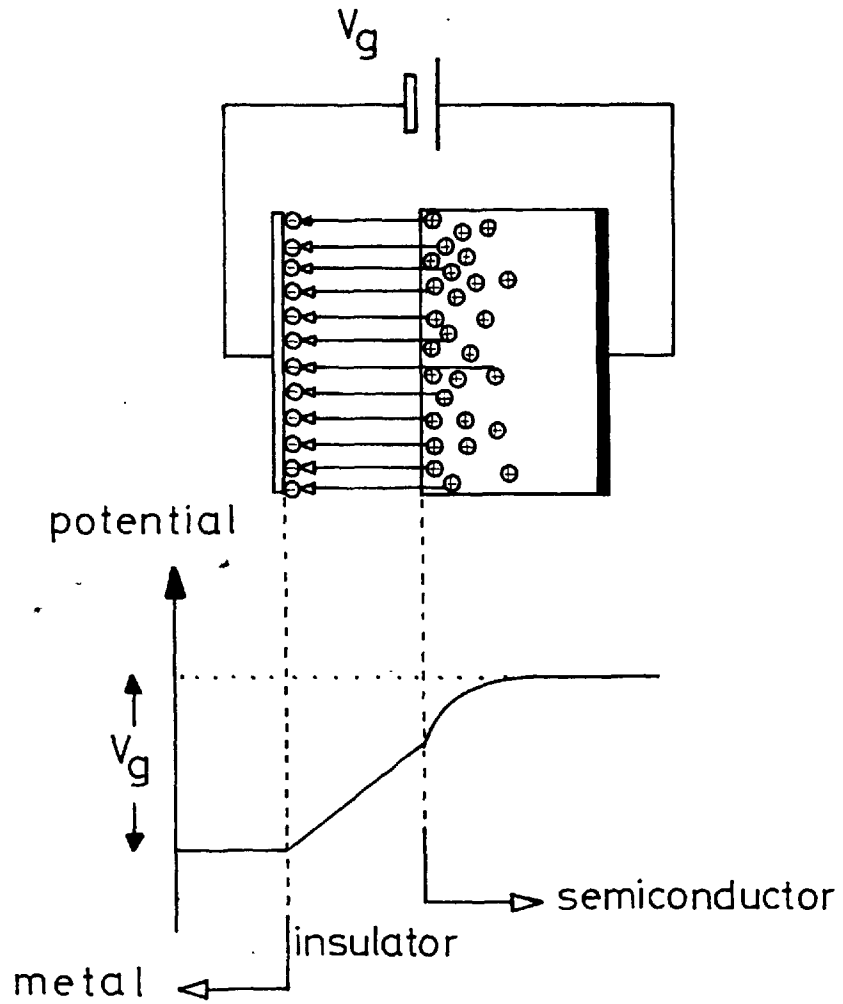

Figure 3

Geometry and Potential Distribution of a Biased MIS Diode

the observed increase in hole effective mass with temperature and carrier concentration as reported by Cuff et. al. (C2).

1.3.3 Carrier Mobility

The mobility of both electrons and holes in PbTe, as in the other lead salts, varies essentially as $T^{-5/2}$ over a wide temperature range and for electrons values as high as 750,000 cms^2/v - sec. are usual at 4.2^oK. This 5/2 dependence together with the apparent absence of mobility reduction associated with ionized impurity scattering at low temperature remained for many years largely unexplained.

An anomolously large value of dielectric constant estimated at several hundreds was proposed by a number of authors (A3, K3, A4) to account for the small scattering cross section implied by the high value of low temperature mobility but it was not until 1963 that Kanai and Shohno (K4), using the results of junction capacitance measurements, deduced a permittivity value of 400 for both p and n-type material. Subsequent measurements by Burstein et. al. (Z1) using magneto-optical techniques at microwave frequencies led to a value of 3200 in a p-type sample containing 10^{17} carriers/cms^3. They concluded that this higher value was a result of the fact that the earlier measurements were made for a carrier free region and that the permittivity was an increasing function of carrier density.

Because of the assumed ionic nature of the lead salts optical phonons were originally believed to dominate the scattering process. However, above the Debye temperature, which is approximately 150^oK in the lead salts (P5), optical phonon scattering predicts a $T^{-\frac{1}{2}}$ mobility variation which agrees rather poorly with the $T^{-5/2}$ variation observed experimentally.

In an attempt to improve the theoretical model Petritz and Scanlon

(P6) proposed a combination of acoustical and optical phonon scattering. This led to better agreement with experiment but only for temperatures below $\sim 250^{\circ}K$.

Subsequent to this Talpygo and Fedorchenko (T3) modified the theory of optical phonon scattering to include the effect of lattice deformation resulting from the presence of the mobile species and in this way obtained a 5/2 temperature dependence at high temperatures.

All these previous attempts to explain the distinctive temperature dependence of mobility in the lead salts had however been based on the assumption of a temperature independent value of effective mass. Smirnov et. al., (S7) by comparing theoretical and experimental values of thermoelectric power, showed that the electron and hole effective masses in PbSe in fact varied as $T^{0.35}$ and $T^{0.45}$. This variation when combined with acoustical lattice scattering alone led to a temperature dependence of mobility which was in good agreement with experiment. The mobility is given in this case by

$$\frac{1}{m^{5/2}\, T^{3/2}} \quad \text{and} \quad \frac{1}{m^{2}.\, T}$$

for classical and degenerate statistics respectively (S16).

More recently this same model has been successfully applied to PbTe by Allgaier and Houston (A4) with agreement not only being obtained for the dependence of mobility upon temperature but also for its dependence upon doping density.

It therefore seems likely that in the lead salts acoustical phonons dominate carrier transport over a large temperature range and that the experimentally observed variation of mobility with temperature is partly a result of the temperature dependence of effective mass in these materials.

Table (ii)

Relevant Semiconductor Properties

	Lead Telluride		Indium Antimonide		
Relative dielectric constant (i)	400		16		
Minimum band gap at $77^{\circ}K$	0.222 eV		0.228 eV		
Efective masses	electron	hole	electron	hole	
	0.17 m_o	0.21 m_o	0.013 m_o	0.41 m_o	
Carrier mobilities (cms^2/ v-sec.) (ii)	1600 35000	750 20000	77000 620000	700 8000	@ $300^{\circ}K$ @ $77^{\circ}K$
Non parabolicity coefficient B	conduction	valence	conduction	valence	
	zero	zero	0.0001	zero	
Lattice constant	6.34 A		6.479 A		

(i) Although in some doubt these values seem most appropriate at the 1 Mc/s of interest here.

(ii) These represent in general the highest values to be expected.

1.3.4 Evaporated Layers

Evaporated layers of the lead salts, like bulk material, tend to be highly non-stoichiometric. Doping densities are typically greater than 10^{17} cms^{-3} for both p and n-type films and the pronounced interaction of these layers with oxygen, which acts as an acceptor, increases further the initial likelihood that doping in these films is highly non-uniform.

Layers grown epitaxially on substrates such as Mica and NaCl have exhibited large mobilities. The 5/2 temperature dependence is maintained and in many cases values of mobility within a factor of three of those in the bulk have been achieved.

Polycrystalline layers grown on amorphous substrates are not so good, the mobility in these cases being rarely greater than 200 cms^2/v - sec. For photoconductive applications however they do appear far superior to the high mobility single crystal films.

A summary of the basic electrical properties of InSb and PbTe, which are relevant to the present work, is given in table (ii). These data refer to bulk single crystal specimens and are average values taken from a large number of reported results.

CHAPTER TWO

SURFACE PROPERTIES

2.1 Surface Space Charge

Application of a voltage across a metal-insulator-semiconductor (MIS) sandwich of the construction shown in figure (3) results in the build up of a space charge on both the metal and semiconductor surfaces. The quantity of charge on each is equal and the distribution in both cases is given by a solution of Poisson's equation. In the case of the semiconductor however, with its much lower carrier density, the space charge will penetrate a much greater distance into the bulk than is the case with a metal; the latter being typically as small as one percent of an atomic layer.

The main consequence of this quantitative difference is that, in the case of the semiconductor particularly when in the form of a thin layer, it is possible appreciably to alter the average value of its carrier concentration by the application of an electric field normal to its surface. On a band diagram this space charge requires that, in the surface region, the allowed energy levels be drawn with a finite slope.*

With reference to figure (4) the qualitative behaviour of this space charge is as follows:

(i) For voltages on the field plate such that majority carriers are attracted to the surface a so-called enhancement or accumulation layer is formed with the charge lying close to the semiconductor-insulator interface.

(ii) For voltages such that majority carriers are repelled from the surface, a region essentially devoid of carriers is set up and this,

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* In such a band diagram the band edges are representative of electron potential and hence the slope gives the electric intensity i.e. $E_x = -\frac{dV}{dx}$

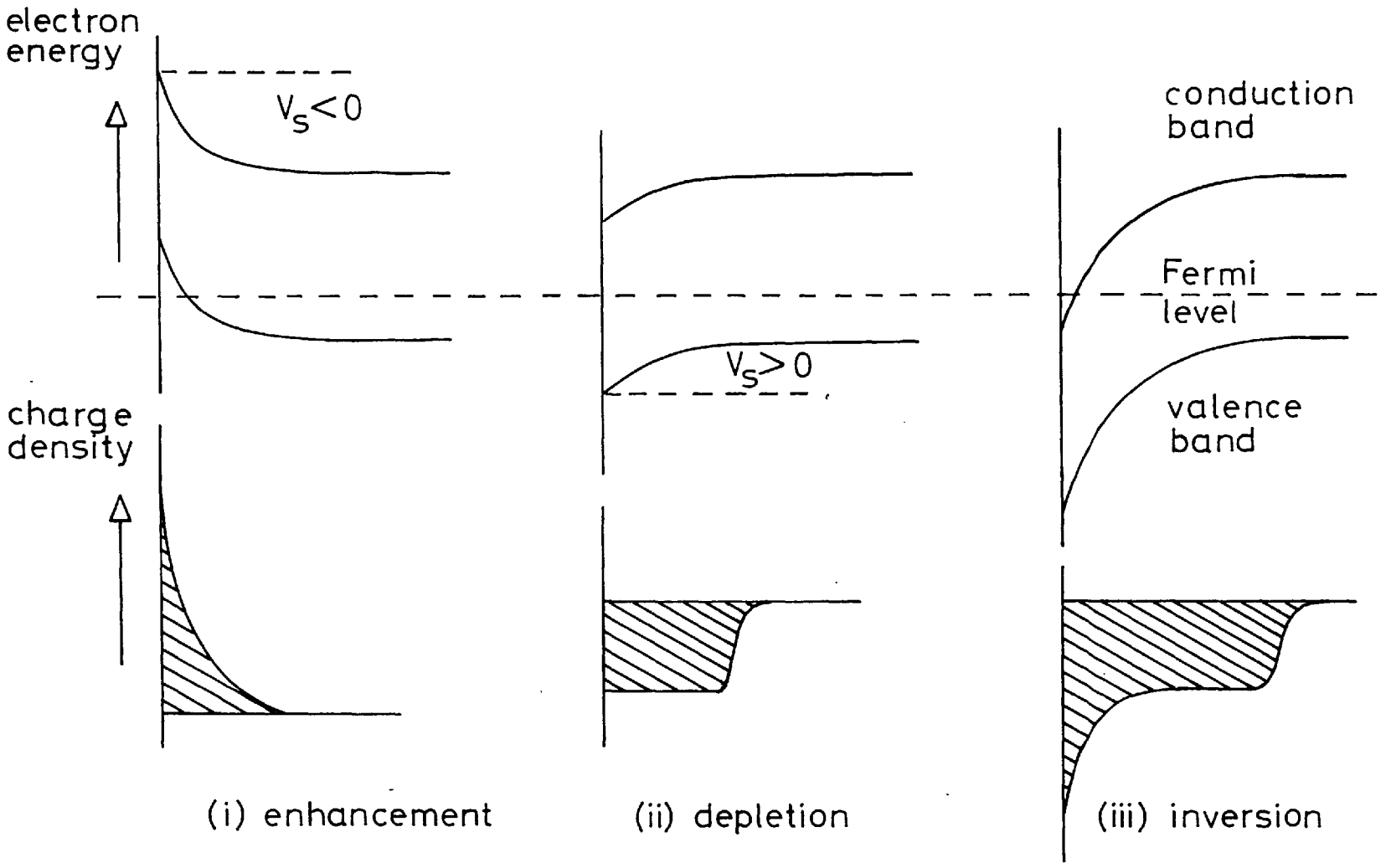

Figure 4 The Energy Level and Charge Distribution in the Surface Region of a Semiconductor in the presence of a Surface Space Charge

termed a depletion region, can extend far into the semiconductor.

(iii) For increasing voltages this depletion region will penetrate even further into the semiconductor until a point is reached when further voltage increase will be essentially accommodated by a build up of minority carriers close to the interface. When this inversion region forms, further changes in voltage result in only small changes in the majority carrier depletion region component of the space charge.

Quantitatively the above behaviour follows from a solution of Poisson's equation (G1), in essentially the same way that the space charge distribution at a p-n junction is determined. The difference is that in the latter case Poisson's equation is applicable to both sides of the junction whereas in this case the charge free Laplace equation must be applied in the insulator.

Approximations to the exact solution are obviously possible. Perhaps the most well known of these being that developed by Schottky in 1939 (S8). In this treatment the depletion region is considered to be completely devoid of free carriers. The space charge density is then given solely by the, assumed uniform, concentration of ionized impurities N. This assumption leads to a depletion depth d given by

$$d = \left[\frac{2 \epsilon \epsilon_o V_s}{qN}\right]^{\frac{1}{2}}$$

where V_s is the potential drop across the space charge region.

The potential distribution resulting from this approximate analysis is generally termed a Schottky barrier.

2.2 Definition of Terms

Flat Band: This refers to the situation where the space charge is zero and on

a band diagram the energy levels continue flat up to the surface.

Surface Potential: In the presence of a surface space charge the potential at the semiconductor surface will be different from its value in the bulk. The difference is termed the surface potential V_s (see fig. (4)) and is positive for a negative space charge (downward band bending).

As is shown in appendix A, all the properties of the space charge region are uniquely determined by the surface potential.

Carrier Excess: The surface space charge region is composed of holes, electrons and ionized impurities. The contribution to this space charge of the mobile carriers measured as the number present relative to flat band is termed the hole/electron excess and is given by

$$\Delta P = \int_{\text{surface}}^{\text{bulk}} (p - p_b)\, dx \qquad \text{for holes}$$

and

$$\Delta N = \int_{\text{surface}}^{\text{bulk}} (n - n_b)\, dx \qquad \text{for electrons}$$

n_b and p_b are the bulk values of electron and hole density and the excesses are measured in carriers/unit area.

The total surface space charge Q_{sc} is given by the sum of $q\,\Delta P$, $q\,\Delta N$ and the contribution of the ionized impurities.

2.3 Surface States

The solution of Schrödinger's equation for a potential energy distribution which is periodic leads to the well known band picture of allowed electron energy levels grouped in bands which are separated by forbidden energy intervals. These energy levels correspond to real values of the electron

wave vector k, i.e. unattenuated electron waves if an infinite periodic model is assumed.

Just as defects within the bulk of a real crystal modify the solution to allow complex (localized) values of k so the termination of the lattice introduces at the surface, the mathematical possibility of levels lying in the 'forbidden' gap. This was originally realised by Tamm (T4) and subsequently reworked by Shockley (S9) using a different potential distribution. Physically interpreted (H3) the Shockley states can be associated with the lattice termination whereas the Tamm states results from the strain induced in the surface region. These additional states at the surface are intrinsic; they occur solely as a result of the deviation from periodicity of the crystal potential near the surface.

On a real surface contamination must invariably occur and this will lead to a modification of the above energy diagram at the surface. These 'extrinsic states' associated with the presence of electrically active impurities on the surface together with the intrinsic states constitute what are termed 'fast surface states'. Because of their immediate juxtaposition to the carrier bands of the semiconductor rapid charge transfer between these bands and the states can occur.

In contrast 'slow surface states', which in practice are associated with defects in the adjacent dielectric or mobile charge on the far surface of the dielectric, by definition are states which, because of their poor electrical contact with the surface carriers, require times measured in seconds or more to reach equilibrium.

As will be shown later, it is the fast states which degrade the performance of FETs and the slow states which lead to time dependent variations

in their characteristics.

2.3.1 Surface State Equilibrium

Consider a semiconductor surface initially free of surface states as shown in figure (5a). In this case, in the absence of an externally applied field, there can be no surface space charge and the bands will continue flat up to the surface.

Surface states can be divided into two types: Acceptor states are states which are normally neutral but which can accept one or more electrons to become negatively charged. Donor states are those which can loose one or more electrons thereby becoming positively charged.

If states of both these types are now introduced on to the semiconductor surface of figure (5a) a state of disequilibrium will exist as shown in figure (5b). Donor states lying above the Fermi level and acceptors lying below it must respectively loose and accept electrons.* This charge transfer will occur between the carrier bands, the bulk impurity levels near the surface and the surface states until an equilibrium is reached as shown in figure (5c). At this point the energy of the system is a minimum and this equilibrium is termed the quiescent surface condition. It corresponds to the surface potential which exists in the absence of an externally applied field.

For a surface state distribution which is reasonably symmetric about the middle of the band gap and which has an approximately equal number of donors and acceptors, then the quiescent condition for extrinsic materials must always be one of depletion.

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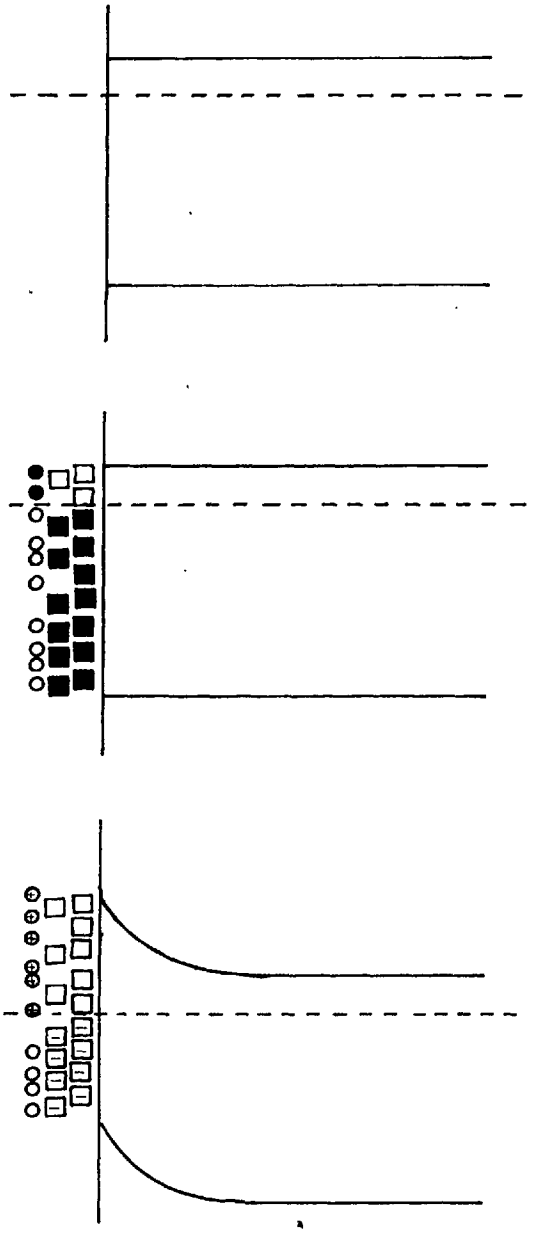
* In general terms surface states, like bulk states, obey Fermi Dirac statistics. For a large density of states however the interaction between them may become appreciable, leading to a situation in which Fermi statistics are not wholly valid. This has been proposed by Haneman (H3) to account for the smaller than expected number of surface states observed on clean semiconductor surfaces.

Figure 5



(a) energy levels at the surface of an n-type semiconductor in the absence of surface states

(b) donor and acceptor surface states in disequilibrium with the semiconductor

(c) thermal equilibrium with a net negative charge in the surface states and an equal positive charge in the surface space charge region

Legend: o donors, □ acceptors — in equilibrium; ● donors, ■ acceptors — in disequilibrium

It will be shown in chapter VI that this is in fact the case on the surfaces of both InSb and PbTe.

2.4 Surface Space Charge Capacitance

It will be shown later that it is advantageous to define a quantity termed the differential surface space charge capacitance

$$C_{sc} = - \frac{dQ_{sc}}{dV_s}$$

Where Q_{sc} is the net surface space charge/unit area and V_s is the surface potential. Qualitatively the form of C_{sc} as a function of V_s is as shown in figure (6) and this may be understood in general terms as follows:

For an enhanced surface (i.e. $V_s < 0$ for the p-type semiconductor shown) the space charge lies close to the surface and a given change in V_s will result in a large change in electric field E within the space charge region ($E \sim V_s/d$ where d is the thickness of the space charge). Now by Gauss' law the induced charge is proportional to the electric field and thus C_{sc} is large. In depletion ($V_s > 0$) the space charge is spread over a much larger distance and for the same change in V_s a much smaller change in majority carrier density will occur at the edge of the space charge remote from the surface, i.e. C_{sc} is small. In the case of inversion ($V_s \gg 0$) the space charge is once again confined close to the surface and C_{sc} rises leading to the 'V' shaped curve of figure (6).

Gauss' law gives

$$\Delta Q = \Delta D = \epsilon\epsilon_o \Delta E \sim \frac{\epsilon\epsilon_o \Delta V_s}{d}$$

where D is the electric displacement

therefore $C_{sc} \sim \frac{\epsilon\epsilon_o}{d}$

hence large semiconductor permittivity leads to a large value of surface

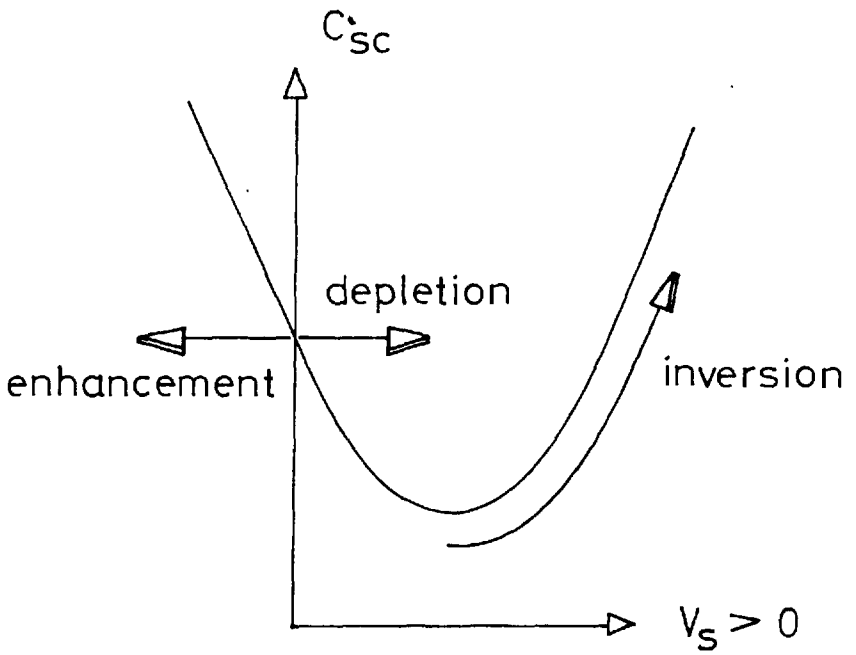


Figure 6 Variation of Differential Surface Space Charge Capacitance with Surface Potential for a p-type Semiconductor

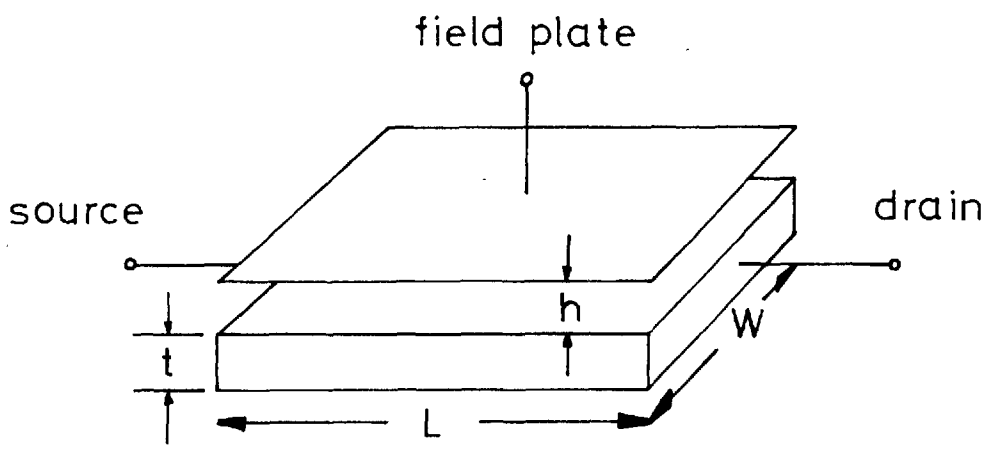


Figure 7 Idealised Geometry of the FET

capacitance

2.5 Surface Transport

As was mentioned in section 1.1, carriers induced into the surface region of a semiconductor which do not become trapped, can modify the conductivity of the semiconductor by altering the carrier concentration at the surface. This effect, the modulation of conductivity by an applied normal field, is termed the field effect and was first studied by Shockley and Pearson in 1948 (S10).

For an applied normal field the induced surface charge/unit area which is numerically equal to Q_g the charge on the field plate, can be divided into that charge which lies in the surface space charge region and that which enters any active surface states i.e.

$$- Q_g = Q_{sc} + Q_{ss}$$

The part of Q_g which can contribute to conductivity modulation is given by that part of Q_{sc} which is mobile, namely ΔN and ΔP. The remainder of Q_{sc} consists of immobile ionized impurities. Thus we may write

$$\Delta\sigma = q\,(\mu_{ns}\Delta N + \mu_{ps}\,\Delta P)$$

where $\Delta\sigma$ is the change in the semiconductor sheet conductivity and μ_{ns} and μ_{ps} are defined as the surface mobility of electrons and holes respectively, these being a function of surface potential.

2.6 Surface Mobility

In bulk material a carrier's mobility is determined by its effective mass, which determines how rapidly it can draw energy from the applied field, and by the extent of its interaction with the environment within which it moves.

In an ideal periodic lattice with no thermal motion this interaction is zero and the mobility is infinite. Deviations from this situation such as thermal vibration of the lattice (phonon waves) and impurity inclusions (neutral and ionized impurity scattering) reduce the carrier's mobility to a finite value. This value being the lower the greater the deviation from the ideal. As we have seen, external surfaces present a gross departure from this periodicity but for bulk samples the probability of a carrier suffering a collision with a surface subsequent to a bulk interaction is negligible. For thin films or for carriers drawn into a surface space charge region however this probability can be large. For a surface interaction to contribute to mobility reduction it is necessary for the interaction to result in a decrease in the component of carrier momentum in the plane parallel to the surface. A surface which results in a zero net carrier momentum parallel to itself subsequent to collision is termed diffuse. For no net reduction in this component of momentum the surface is termed specular. The specularity of a given surface is not solely a function of the surface however. As the carrier crystal momentum decreases the specularity would be expected to increase owing to the increased value of electron wavelength.

The subject of surface scattering was initially studied by Thomson in 1901 (T5) for the case of conduction in thin metal films. This was later extended by Fuchs (F1) and Sondheimer (S11) who treated the problem by means of the Boltzmann transport equation. In these analyses however concern was with conduction in thin metallic films where space charge effects could be neglected. The theoretical extension to the case where the distribution function is a function of distance from the surface was carried out by Schrieffer in 1955 (S12). This being subsequently extended to include the effects of a magnetic field by Zemel in 1958 (Z2).

In both these treatments the contribution of bulk carriers was suppressed. Inclusion of this bulk contribution was later carried out by Greene et. al. (G2) and the expression they arrived at for electron current was

$$I_x \Big|_{\text{electrons}} = qE_x \left(n_b \mu_n (d - \lambda_n) + \mu_{ns} \Delta N \right)$$

where E_x is the longitudinal electric field, d is the half thickness of the layer, n_b is the bulk carrier density and λ_n is the electron's thermal mean free path.

The second term on the right accounts for the effect of the, assumed diffuse, surface on the excess electrons and the first term includes the mobility reducing effect of the surface on those electrons which, although near the surface and hence in the space charge region, have enough energy normal to the surface to surmount the barrier presented by the space charge and hence move freely into the bulk.

In all these treatments non-degeneracy of the carrier populations was assumed. In the case of the narrow band gap materials, however, especially when in thin film form where carrier densities may be very large, this assumption is rarely valid. Recently this deficiency has been remedied by Juhasz (J2) who extended the Boltzmann solution to the case where complete Fermi Dirac distributions were assumed. In addition, this treatment included the effects of band non-parabolicity which had hitherto been neglected.

2.7 Field Effect Mobility

The way in which the sheet conductance varies with applied normal field is a function of both surface trapping and surface scattering. It is thus not possible, from a field effect measurement alone, to differentiate between these two effects. Nevertheless it is possible by this means to assess

the total net effect of the surface on the induced charges and this is usually done by measuring what is termed the field effect mobility μ_{fe}. This quantity is defined by

$$\mu_{fe} = - \frac{d\sigma}{d Q_g}$$

where σ- sheet conductance of the semiconductor

and Q_g - charge/unit area on the field plate.

μ_{fe} has the dimensions of a mobility. It is simply the slope of the field effect curve (see chapter (VI)) and in the absence of surface trapping becomes equal to the differential surface mobility (see section 4.5).

In physical terms μ_{fe} is simply the average effective conductivity mobility of those carriers induced incrementally into the surface region. The average being taken over all those induced charges irrespective of whether they are trapped or not.

CHAPTER THREE

THE SURFACE CHANNEL FET

3.1 Theory of Operation

We consider initially a first order theory based on the device geometry shown in figure (7), namely a slab of semiconductor of width W and length L to the ends of which are attached low resistance contacts and above which, separated by a distance h from the semiconductor surface lies the metal field plate termed the gate.*

By definition (see section 2.7)

$$\mu_{fe}\Big|_x = \frac{d\sigma_x}{dQ_x} \tag{1}$$

where σ_x is the sheet conductivity of the semiconductor slab a distance x from the source and Q_x is the charge density/unit area at that point.

If C is the capacitance/unit area between the gate and the semiconductor then we may write

$$\mu_{fe}\Big|_x = - \frac{d\sigma_x}{C\, d(V_g - V_x)} \tag{2}$$

Where V_g is the voltage on the gate and V_x is the potential of the semiconductor at a distance x from the source.

Integration of (2) gives

$$\sigma_o - \sigma_x = \mu_{fe}\, C\, (V_g - V_x) \tag{3}$$

---

* The terms source, drain and gate which have come to be generally accepted in device terminology were initially coined by Shockley (S1) for the junction FET. Although geometrically interchangeable the source and drain strictly refer respectively to the electrodes at which carrier injection and collection occur irrespective of carrier sign.

where σ_o is the sheet conductivity at $V_x = V_g$.

The current along the slab is

$$I = W \sigma_x E_x \qquad (4)$$

where E_x is the x component of the electric field in the semiconductor.

Substitution for σ_x from (3) in (4) and integration over the length of the semiconductor leads to (taking voltages with respect to the source)

$$I = \frac{W \mu_{fe} C}{L} \left[(V_g - V_o) V_d - \frac{V_d^2}{2} \right] \qquad (5)$$

where $V_o = \frac{\sigma_o}{\mu_{fe} C}$ and V_d is the potential at the drain electrode.

Equation (5) represents the output characteristics for the FET and is plotted in figure (0). The assumptions on which it is based, implicit in the above, are

(i) that the gate to semiconductor capacitance is constant i.e. independent of $(V_g - V_x)$ so that (2) follows from (1)

(ii) that μ_{fe} is independent of $(V_g - V_x)$ so that (3) follows from (2)

(iii) that the normal component of electric field in the insulator is much larger than its longitudinal component so that we have approximately the one dimensional field distribution of a parallel plane capacitor and $Q_x = C (V_g - V_x)$.

The first assumption, termed the 'shallow channel approximation' is valid for insulators thick compared to the extent of the surface space charge region. In most cases this is a valid approximation but, as will be shown later, deviations from it can provide a powerful means of probing the trapping behaviour of the surface.

The second assumption holds only for a surface trap distribution such that the trapped charge increases linearly with gate voltage. For the

case where surface scattering is constant and finally, but perhaps most important of all, for a system in which only one carrier is present. As will be shown in section 3.4, this last limitation can be severe in narrow band gap materials.

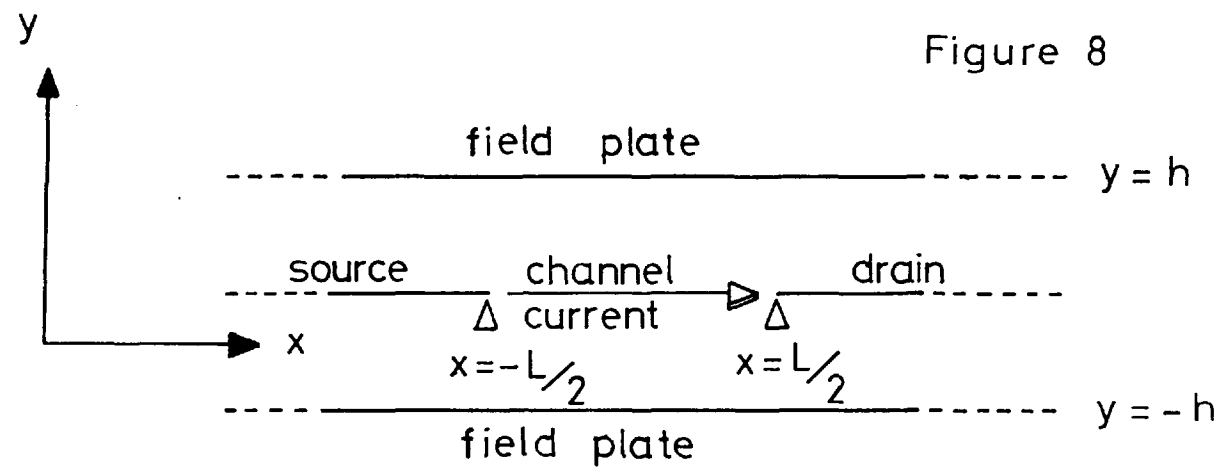
The final assumption, termed the 'gradual approximation' was introduced by Shockley (S1) to reduce the field equation to a soluble form. Using this approximation he showed that the longitudinal component of electric field tended to infinity as $V_d \rightarrow (V_g - V_o)$. This value of drain voltage must thus represent the limit of validity of (5). Shockley (S18) originally expected that beyond this point the current would show a sharp drop owing to the complete depletion of carriers from the drain end of the semiconductor. Further reasoning convinced him however that this would represent an unstable situation and instead he proposed in a qualitative fashion that the current should in fact remain constant as V_d was increased beyond this 'pinch-off' value (S1, P7).

This linear extrapolation was subsequently observed in practice although the slope resistance in this saturation region was observed to vary somewhat from device to device.

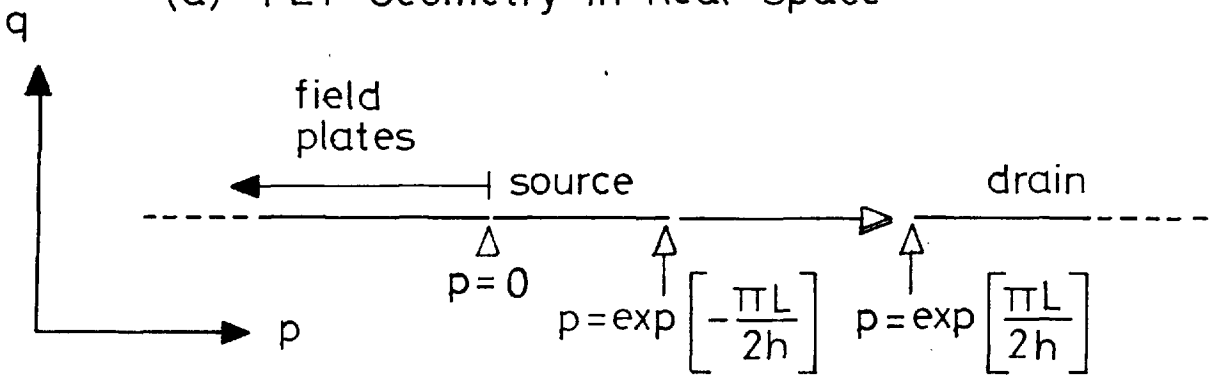
Despite many attempts (G3, H4, R1, L3) to improve the theoretical treatment of this saturation region by including such effects as the field dependence of carrier mobility, no real advance was made until as recently as 1966 when Geurst (G4), treating the problem in an entirely different way, arrived at a solution which was valid for all values of drain voltage.

The geometry which Geurst chose to analyse is shown in figure (8a). The structure is symmetric about the semiconductor channel, which is assumed infinitely thin (i.e. shallow channel approximation retained) and all elec-

Figure 8



(a) FET Geometry in Real Space



(b) FET Transform of Geometry (a)

where $p = \exp\left[\frac{\pi x}{h}\right].\cos\left[\frac{\pi y}{h}\right]$

and $q = \exp\left[\frac{\pi x}{h}\right].\sin\left[\frac{\pi y}{h}\right]$

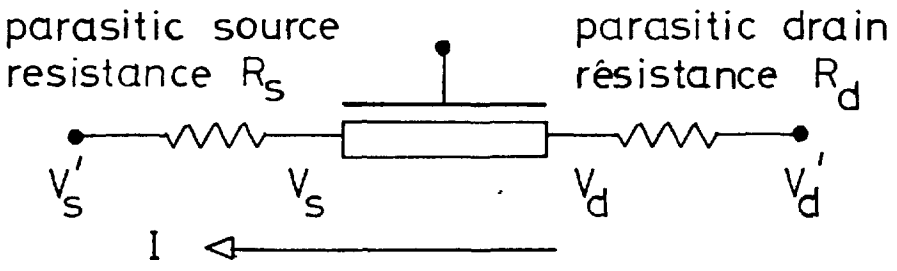


Figure 9 Linear Contact Resistance Model

trodes are assumed infinite in extent.

To derive the electrical behaviour of the FET essentially requires the solution of Poisson's equation in two dimensions for the semiconductor channel. Shockley overcame this problem by means of his gradual approximation which reduced the problem to a one dimensional form (as in a p-n junction) leading, as we have seen, to equation (5).

Geurst however, instead of solving for current explicitly, included it as a boundary condition on a solution of the more tractable Laplace's equation for the dielectric.

In this case a conformal transformation of the problem from the x, y plane of figure (8a) into the w plane where

$$w = p + i\,q$$

$$z = x + i\,y$$

and for the transform $w = \exp \frac{\pi z}{h}$

leads to the geometry of figure (8b) for which a solution to the transformed field equation became possible.

Although the details of this analysis will not be reproduced here the results of importance in the present work, will be considered:

For $^{h}/_{L} \to 0$ a closed form asymptotic solution is arrived at, namely

$$j = (1 - v^2)\left[1 - \frac{h}{\pi L} \exp A + \ldots\ldots\ldots\ldots\ldots\ldots\right. \qquad (6)$$

for $V_d < (V_g - V_o)$ and

$$j = 1 + \frac{h}{\pi L} \log v^2 + \ldots\ldots\ldots\ldots\ldots\ldots\ldots \qquad (7)$$

for $V_d > (V_g - V_o)$

j and v being respectively dimensionless current and voltage variables.

The first term of (6) reduces to (5) indicating that deviations from the gradual solution are exponentially small in the geometric ratio $^{h}/_{L}$ before saturation.

From (7) it can likewise be seen that for small values of $^{h}/_{L}$ little error is involved in the linear extrapolation of the gradual solution beyond its range of validity. Geurst further showed that for small values of the ratio $^{h}/_{L}$ a single gate device can, to good approximation, be considered as one half of a symmetrical structure.

Subsequent work by Rittner and Neumark (R2) using an analogue technique, led to the conclusion that, for a device of finite dimensions, the above still holds true providing that the gate overlaps the channel contacts by more than an amount h. In addition they showed that finite contact thickness had no great effect on the results.

It thus appears that the results obtained by Geurst for a highly idealized geometry do in fact apply to devices fabricated in a more realistic form (figure(27)) and further that the qualitatively introduced extrapolation of the gradual theory can in fact be supported theoretically.

3.2 Device Performance

The device transconductance follows immediately from equation (5) viz:

$$g_m = \left.\frac{dI_d}{dV_g}\right|_{V_d \text{ constant}} = \frac{W \mu_{fe} C V_{d^*}}{L} \text{ mhos (for } V_d < (V_g - V_o)\text{)} \qquad (8)$$

An oft quoted figure of merit for active systems is the gain-bandwidth product

---

* For $V_d > (V_g - V_o)$, g_m and the gain-bandwidth product (GBW) are constant in the ideal case at

$\frac{W \mu_{fe} C (V_g - V_o)}{L}$ and $\frac{W \mu_{fe} (V_g - V_o)}{2\pi L^2}$ respectively.

(GBW). This parameter follows most simply from the equivalent circuit of the device (B8) and is given by

$$GBW = \frac{W \mu_{fe} V_d}{2\pi L^2} \text{ c/s* (for } V_d < (V_g - V_o)) \qquad (9)$$

from (8) and (9) it can be seen that optimization of device performance involves increasing μ_{fe} and decreasing L. At present the technological limit of L lies in the range $1 \rightarrow 10\mu$. The field effect mobility is, as was seen in section 2.7, a function of bulk mobility, surface trapping and surface scattering. For commercially available MOSTs it has a value typically in the region of 550 cms^2/v - sec. (L4) leading to a cut-off at ~ 500 Mc/s. As shown by Page however (P8), (9) can be rewritten in terms of power dissipation leading to

$$GBW \propto \left[\frac{\mu_{fe}}{L^2}\right]^{2/3} P^{1/3}$$

and thus for constant power dissipation P the frequency response increases as the 2/3 power of μ_{fe} rather than as the more rapid linear dependence indicated by equation (9).

The frequency response of the FET is limited by the rate at which carriers can be transported into the surface space charge region, just as in a bipolar device it is invariably the charging of the emitter-base junction which dominates the frequency behaviour. In the latter case however an alternative mechanism can dominate, namely minority carrier transport to the collector. By making the base sufficiently thin the capacitive charging of the emitter junction becomes the limiting mechanism but in the FET source to drain transport is completely unimportant in that carriers in an FET drift rather than diffuse along the channel. The GBW given by equation (9) can in fact be rewritten as proportional to the reciprocal of the source drain transit time,

---

* see footnote on foregoing page.

but this is solely a result of the fact that decreasing this time reduces the time constant of the channel.

Just as in other active devices, voltage and power gain are increasing functions of slope resistance so in the FET the desirability of good saturating characteristics is evident.

3.3 The Effect of Contact Resistance

In his review article, Weimer (W7) noted the importance of the statement made in section 3.1 namely 'to the ends of which (the semiconductor) are attached low resistance contacts'. Qualitatively he pointed out that the effect of a poorly injecting contact for majority carriers would result in a 'crowding' of the output characteristics for increasing conductivity enhancement as a result of the increasing inability of the source to supply the required number of carriers.

Subsequent to this Hofstein (H5) treated the problem mathematically but only for the saturation régime of operation.

Owing to the fact that in the presence of large contact resistance saturation may not be attained, we will develop here the theory which is applicable to the pre-saturation region and in section 3.3.2 correlate this with experimental results as obtained on devices fabricated from InSb and PbTe.

3.3.1 Theoretical

For this analysis we will assume the contact resistance to be current-independent. It will subsequently be shown that this is not strictly valid but as the non-linearities are small they can be treated as perturbations on the first order theory to be developed here.

The situation is represented by the equivalent circuit of figure (9) from which it is readily evident that

$$\left.\begin{aligned} V_s &= V_s' + IR_s \\ \text{and}\quad V_d &= V_d' - IR_d \end{aligned}\right\} \qquad (10)$$

where V_s and V_d are the actual voltages at the ends of the channel and V_s' and V_d' are those applied to the contacts.

It was shown in section 3.1 that, before saturation, the output characteristics are given to good approximation by equation (5) namely

$$I = A\left[(V_g - V_s - V_o)(V_d - V_s) - \frac{(V_d - V_s)^2}{2}\right] \text{where } A = \frac{W \mu_{fe} C}{L} \qquad (5a)$$

where a finite value of the source electrode potential is included.

Substituting for V_s and V_d from (10) and putting $V_s' = 0$ leads to a quadratic equation in I

$$a I^2 + bI + c = 0$$

$$\left.\begin{aligned} \text{where}\quad a &= \tfrac{1}{2}(R_s^2 - R_d^2) \\ b &= (V_d' R_d - (V_g - V_o)(R_s + R_d) - \tfrac{1}{A}) \\ \text{and}\quad c &= (V_d'(V_g - V_o) - \frac{V_d'^2}{2}) \end{aligned}\right\} \qquad (11)$$

the root of which follows directly. In the symmetric case however where $R_s = R_d = R$, 'a' is zero and

$$I = \frac{V_d'(V_g - V_o) - \frac{V_d'^2}{2}}{2(V_g - V_o)R - V_d' R + \frac{1}{A}} \qquad (12)$$

Equations (11) and (12) represent the output characteristics of the device in the presence of contact resistance. Both equations reduce to (5) for $R = 0$.

Differentiation of (11) with respect to V_g leads to the device

transconductance viz:

$$g_m^* = \frac{I\,(R_s + R_d) - V_d'}{b + I\,(R_s^2 - R_d^2)} \tag{13}$$

Now the transconductance of the actual device for which g_m^* is that observed at the external terminals is simply

$$g_m = A\,(V_d - V_s) \tag{8a}$$

$$= A\,(V_d' - I\,(R_s + R_d))$$

$$\therefore \frac{g_m^*}{g_m} = \frac{1}{A}\left[I\,(R_d^2 - R_s^2) - V_d'\,R_d + (V_g - V_o)\,(R_d + R_s) + \frac{1}{A}\right]^{-1} \tag{14}$$

For $R_s = R_d = R$ this becomes

$$\frac{g_m^*}{g_m} = \frac{1}{A}\left[2(V_g - V_o)\,R - V_d'\,R + \frac{1}{A}\right]^{-1} \tag{15}$$

or alternatively using (12)

$$\frac{g_m^*}{g_m} = \frac{I}{A\left[V_d'\,(V_g - V_o) - \frac{V_d'^2}{2}\right]} \tag{16}$$

where the denominator is just the current which would flow in the absence of contact resistance, g_m being thus reduced in the same ratio as I.

The limit on these expressions as set by the gradual approximation occurs when

$$V_d' = (V_g - V_o) + IR_d \tag{17}$$

and although the equations in saturation may be generated by direct substitution of (17) in the previous results it in fact proves more straightforward to work directly from the simple expression for current in saturation,

i.e.

$$I_{sat} = \frac{A}{2}(V_g - V_o - V_s)^2 \tag{18}$$

this reducing direct from equation (5a) with $V_d = (V_g - V_o)$

Substituting for $V_s = V_s' + IR_s$ in (18) gives

$$I_{sat} = \frac{1}{R_s^2}\left[R_s(V_g - V_o) + \frac{1}{A} - \left\{\frac{1}{A^2} + \frac{2R_s(V_g - V_o)}{A}\right\}^{\frac{1}{2}}\right] \tag{19}$$

where the extraneous root has been discarded.

Differentiation of (19) gives

$$g_m^*\Big|_{sat} = \frac{A((V_g - V_o) - IR_s)}{1 + AR_s((V_g - V_o) - IR_s)} \tag{20}$$

where the numerator is simply $g_m\Big|_{sat}$ i.e. $A((V_g - V_o) - V_s)$

$$\therefore \quad \frac{g_m^*}{g_m}\Big|_{sat} = (1 + AR_s(V_g - V_o - IR_s))^{-1}$$

$$= (1 + g_m R_s)^{-1} \tag{21}$$

Using (5) and (12) the output characteristics of a typical transistor in the absence and presence of R are plotted in figure (10).

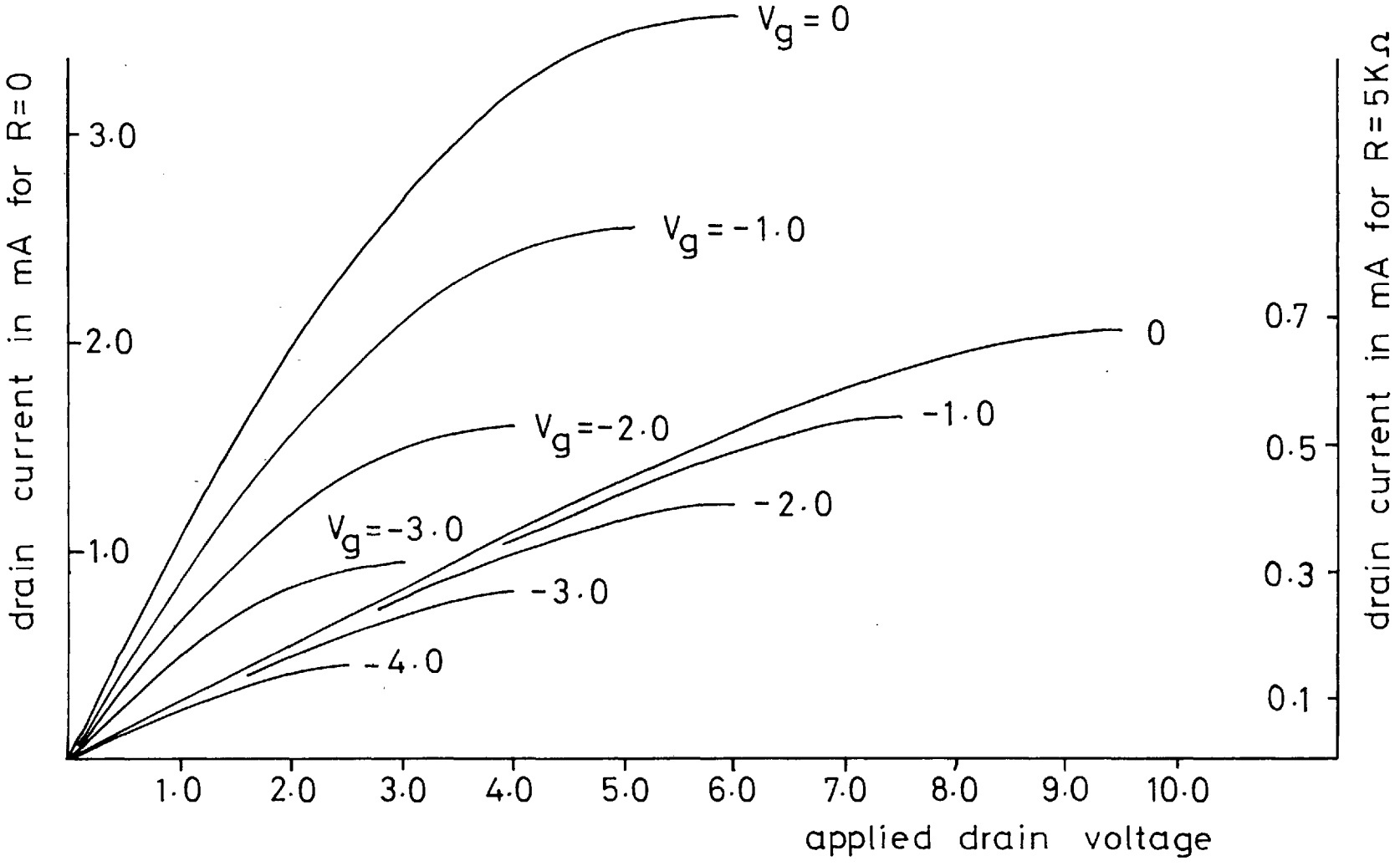
A value of A of 2×10^{-4} amps/v^2 was used corresponding to a typical geometry and a μ_{fe} of 50 cms^2/v sec. and, assumed symmetric, the contact resistance was set at 5 KΩ . The general effect of the poor contacts is thus to reduce the saturation effect, decrease the modulation and decrease the absolute value of current.

Perhaps a more illuminating demonstration of the degradation produced by high contact resistance is given in figure (11). Here g_m^*, calculated from equation (13), is plotted versus applied drain voltage for various values of

Figure 10

Variation of Drain Current with Drain Voltage for an Insulated Gate FET in the presence and absence of Contact Resistance

(n-type device in depletion with $A = 0.0002$ and $V_o = -6.0$ volt)



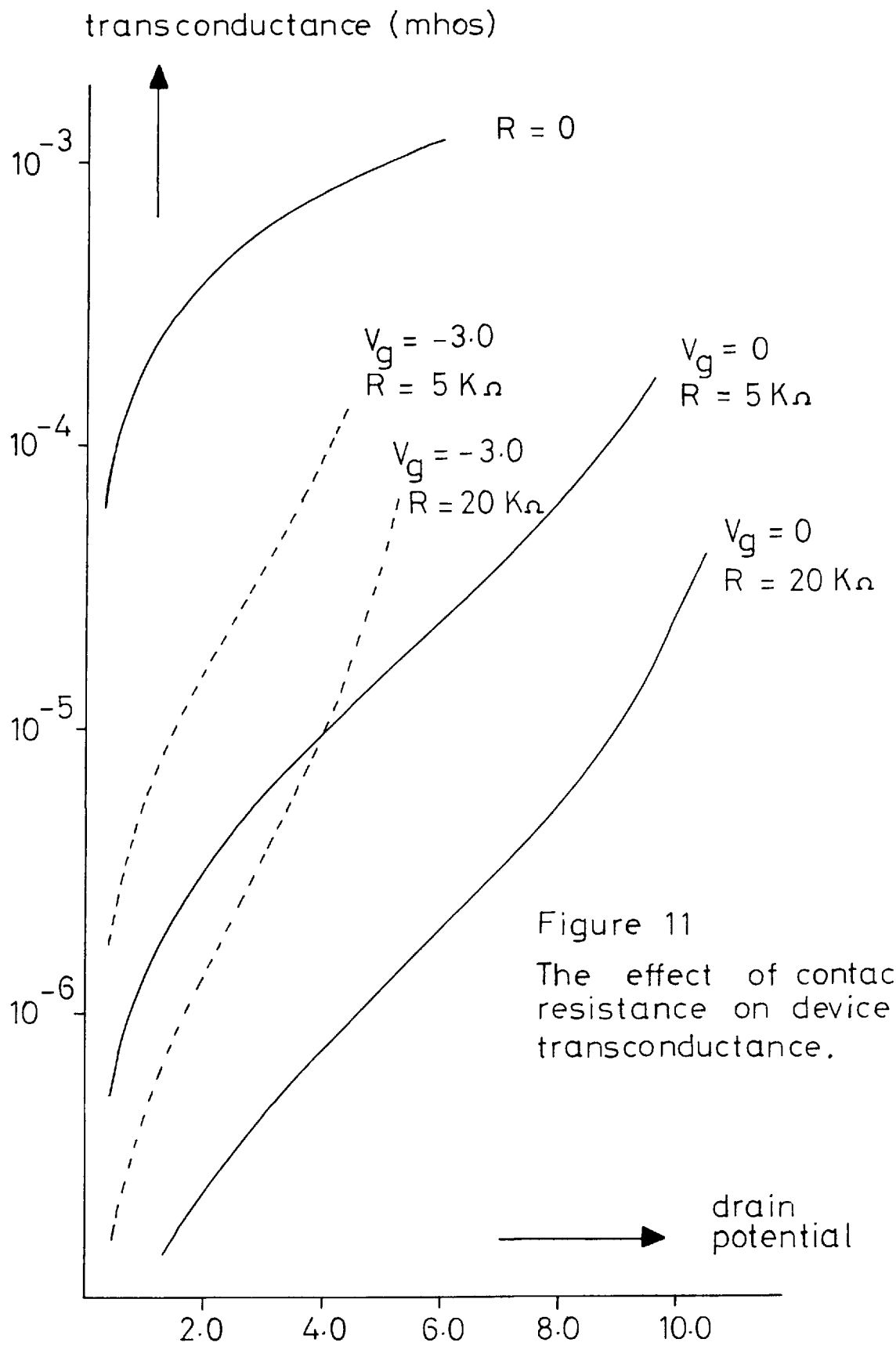


Figure 11

The effect of contact resistance on device transconductance.

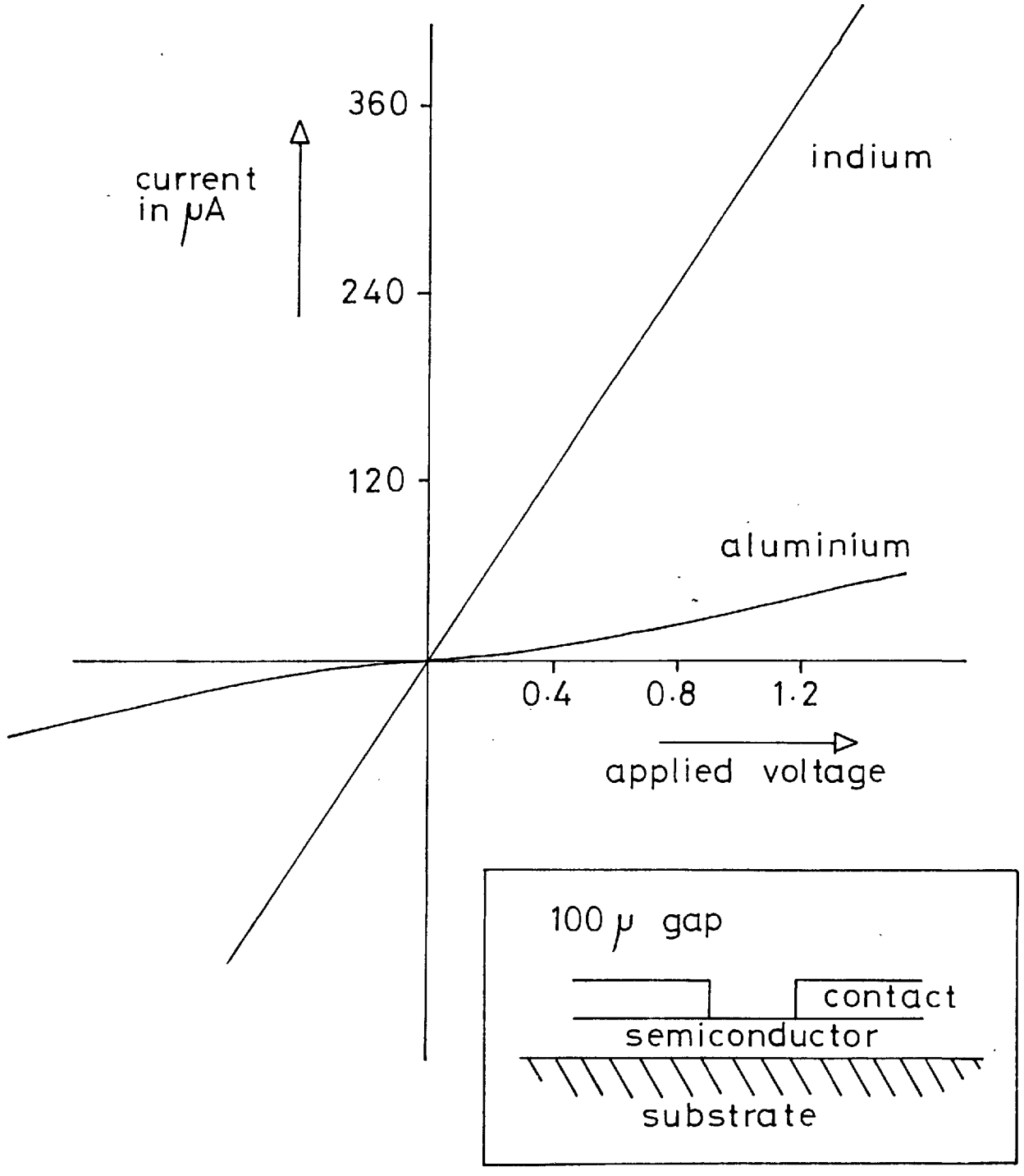


Figure 12

I-V Characteristics for an Al-PbTe and In-PbTe Planar Diode of the Geometry shown in the inset

contact resistance and voltage on the gate. From this figure it can be seen that finite values of R both reduce g_m by many orders of magnitude and in addition make it a function of gate voltage.

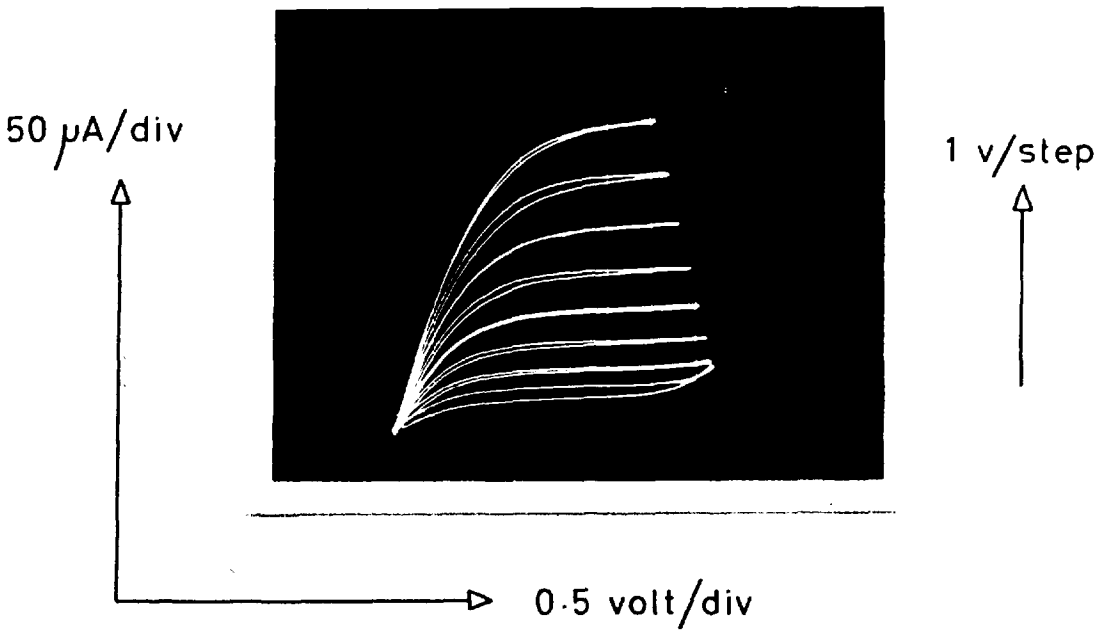
3.3.2 Experimental

Thin film field effect transistors have been successfully fabricated from the two narrow band gap semiconductors PbTe and InSb. The method of fabrication of these devices will be considered in chapter V . In the following only that section of the work which is pertinent to the contact problem is discussed.

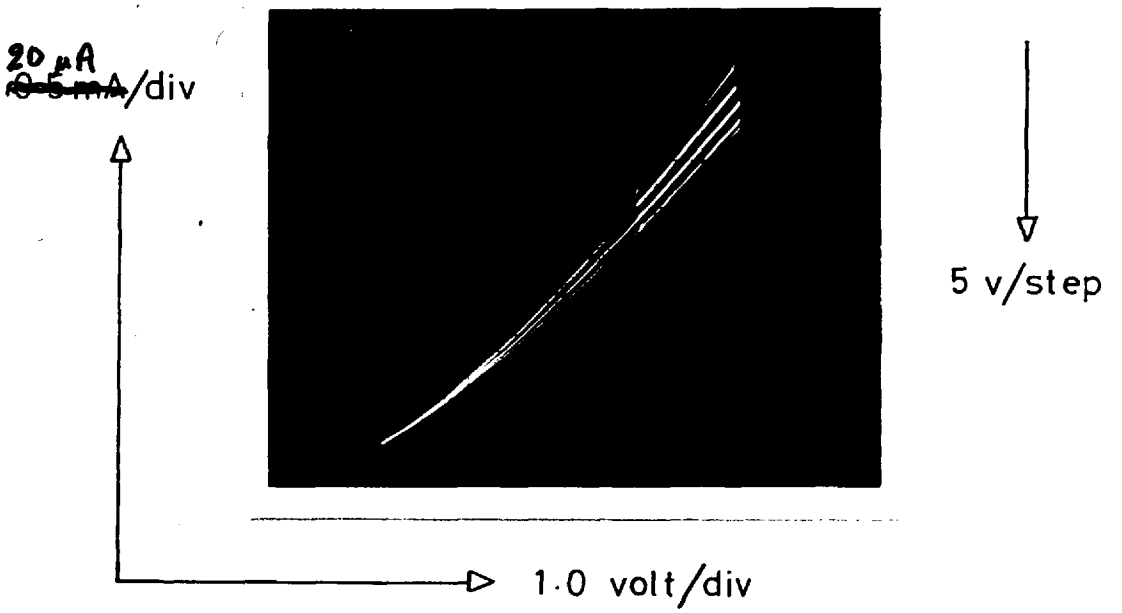
During the course of the work two types of contact material were encountered. One, typified by Al, made poor non-ohmic high resistance contact to the evaporated layers this being quite independent of whether the metal was evaporated prior or subsequent to the semiconductor layer. The second type of material made good contact. In and Sn characterize this group and figure (12) shows the I/V characteristics for these two types of material. The semiconductor in this case is PbTe and the contacts are evaporated on top of the semiconductor with a geometry as shown in the insert. Qualitatively identical behaviour is observed on InSb. Comparison of the semiconductor resistance measured by this means and that predicted from Hall measurements showed that both In and Sn make an essentially zero resistance contact to these semiconductors. From figure (12) it is readily calculated that in the case of Al each contact presents a resistance of ~ 7 KΩ. In addition it is not independent of current but initially decreases as current is increased.

Typical output characteristics of transistors fabricated in essentially the same manner save for the source and drain material are shown in figure (13). Figure (13a) represents an InSb device employing In for the channel

Figure 13



(a) Output characteristics of an InSb FET



(b) The effect of poor channel contacts

contacts whereas (13b) is for a PbTe device on Al. The behaviour of this latter device varies little between the two semiconductors used.

It will be observed that the general conclusions of section 3.3.1 are exhibited by these characteristics. The current level in the case of the Al contacts is lower, the g_m is very small and saturation is absent. The slight upward bending reflects the non-ohmic behaviour evident in figure (12). It should be pointed out however (and this will be considered in more detail later) that even in the presence of good injecting contacts the devices fabricated from PbTe are somewhat inferior to those on InSb owing to the presence of a larger density of fast states on the PbTe surface (see chapter VI).

The results of previous workers* using similar narrow band gap materials seem to indicate that the contact problem is generally encountered but until now the critical dependence of performance on this aspect of fabrication does not appear to have been fully appreciated. The earliest report of this kind was on devices fabricated from layers of PbS. Au was used for the contacts and some of the results seem explicable in terms of contact limited conduction.

Results by Frantz on InSb with gold contacts are similar although Al in this case appears to have been successful.

Subsequent work on PbTe, again using Au, led to similarly poor modulation and it was not until the more recent work of Brody and Kunig working with InAs and Spinulescu-Carnaru using ZnTe and InSb that real success was obtained.

The contact material in the former case was not reported but in the

---

* For references to these see table (i).

latter Al was employed. Although insufficient data were provided to draw unequivocal conclusions it seems possible that even in this case Al may not have been an ideal material for ZnTe.

A recent report by Kunig (K5) seems to indicate that at least for InAs, ion bombardment of the semiconductor surface prior to the evaporation of the contacts leads to a lower resistance connection to the semiconductor.

3.4 The Effect of Minority Carriers

In section 3.1 a parameter σ_o was introduced to signify the semiconductor sheet conductance when the semiconductor to gate voltage was zero.

From equation (1), for constant μ_{fe}, we may write

$$\Delta\sigma = \mu_{fe} Q_x$$

i.e. $$\Delta\sigma = - \mu_{fe} C (V_g - V_x)$$

Thus to reduce the semiconductor conductance to zero requires

$$(V_g - V_x) = \frac{\sigma_o}{\mu_{fe} C}$$

which is simply V_o as defined in section 3.1. Hence V_o represents the voltage necessary to reduce the semiconductor conductance to zero. In the transistor structure this occurs initially at the drain end of the channel and in fact represents the limit of the gradual theory as discussed in 3.1.

i.e. $$(V_g - V_d) = V_o$$

The above assumes however that the field effect mobility is constant.

As we have seen (section 3.1) this can be true for enhancement and depletion of the surface but for voltages such that depletion occurs a point will be reached when majority carriers will no longer be repelled from the

surface but, instead, minority carriers will accumulate in an inversion layer. This inversion has been discussed in section 2.1 and corresponds to a change in sign of μ_{fe} i.e. the conductance at inversion begins to increase rather than continue to decrease.

This inversion will always occur in the presence of an adequate source of minority carriers but only in narrow band gap materials it is usually possible to induce sufficient band bending to attain this condition.*

This minority carrier conduction can manifest itself in essentially two ways:

(i) For a semiconductor layer which is thicker than the extent of the depletion region at inversion, saturation of the transistor characteristic will not occur. Instead the characteristics will tend to a slope given by the 'bulk' component of current flowing beneath the depletion region and beyond this point the current will further increase as a result of the additional minority carrier current in the inversion layer. This is illustrated in figure (14a).

(ii) For a semiconductor in which complete depletion occurs at the drain good saturation is possible. Further increases in drain voltage can however lead to inversion and at this point the current will rise. This sets a limit on the range of operating voltages possible because:

(a) This gross departure from linearity would result in severe distortion for signal voltages entering the inversion régime.

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* Exceptions do occur; the most notable is the inversion layer formed on p-type Si following oxidation in wet oxygen. This however is a result of the presence of positive ions in the oxide near the oxide-Si interface rather than an externally applied field (K6).

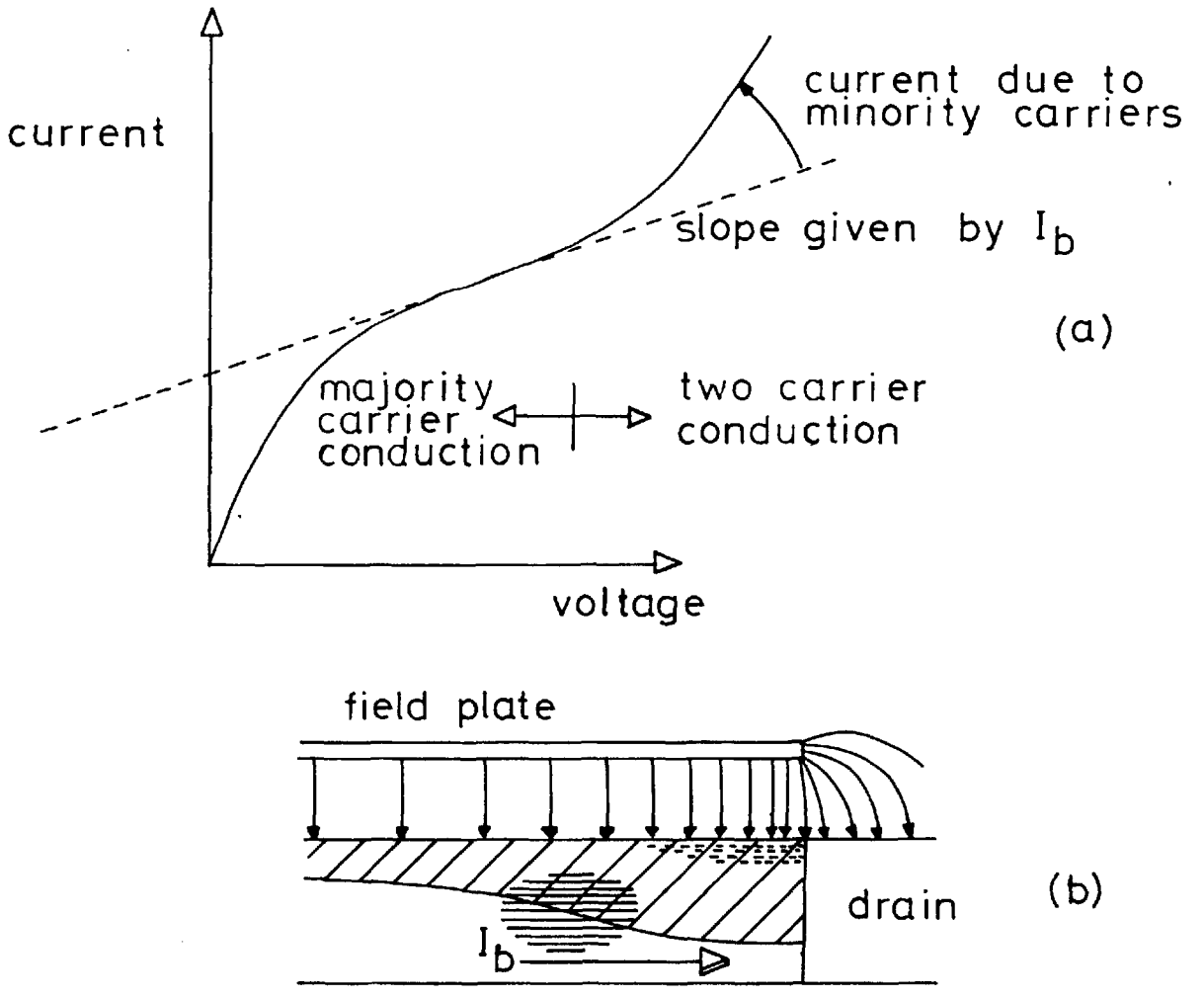
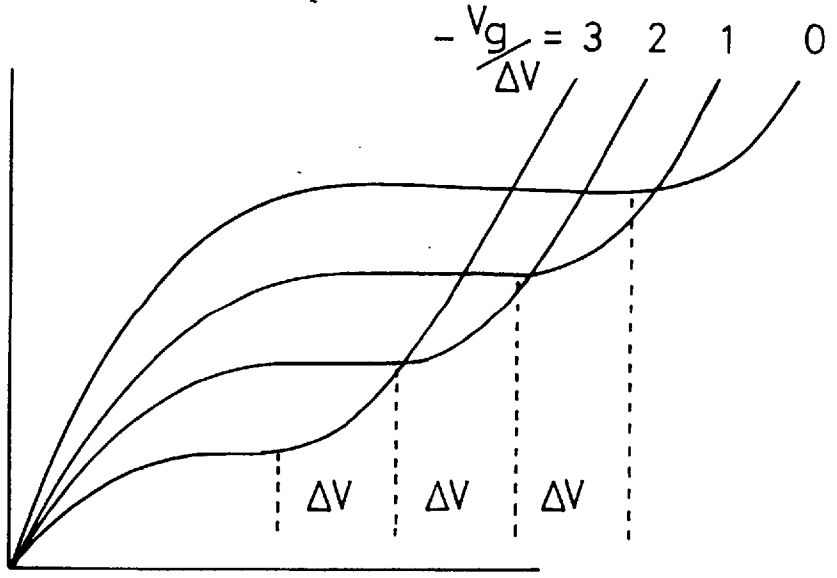


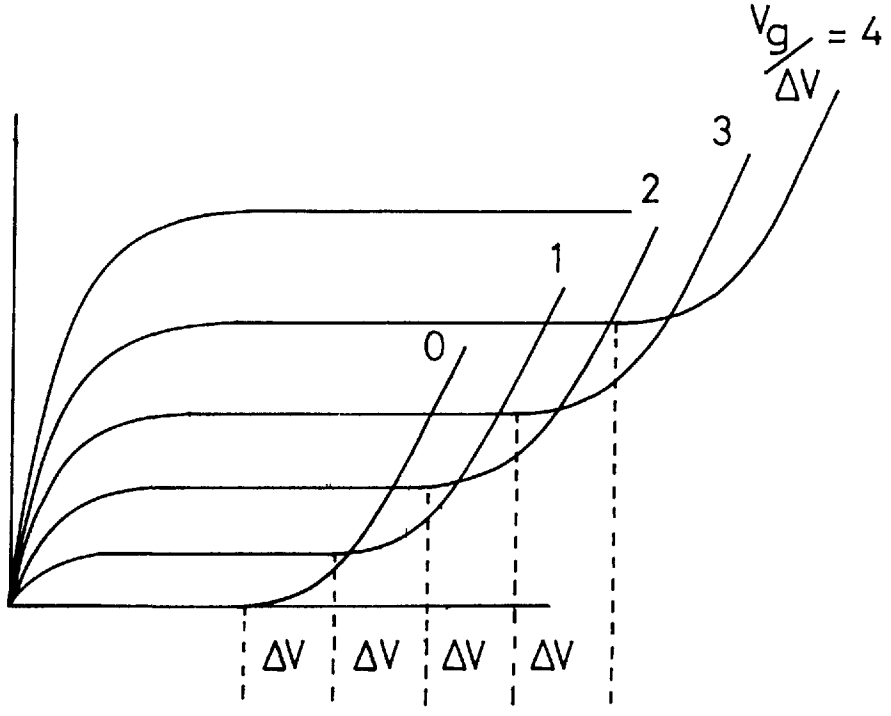
Figure 14 (a) Output Characteristics in the presence of Inversion

(b) Field, Charge and Current Distribution near the Drain of an FET in the Inversion Regime

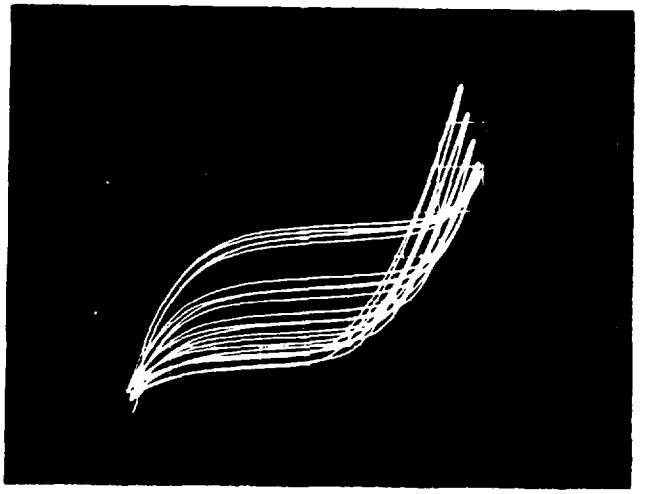
Figure 15a



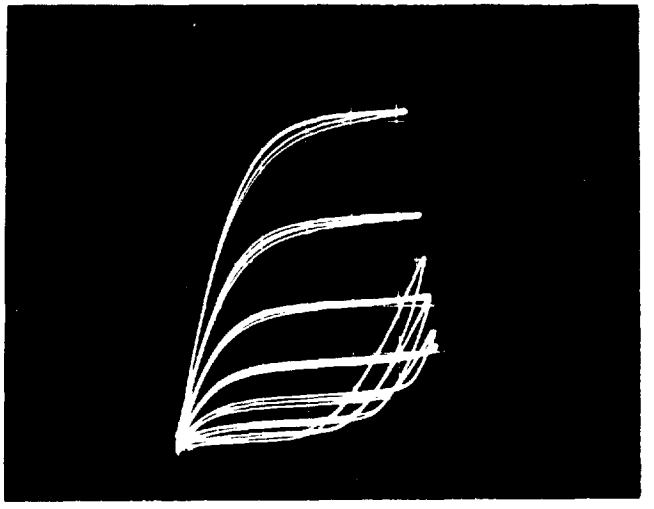
Output characteristics of an n-type FET operating in depletion and exhibiting minority carrier effects



The effect of minority carriers in the enhancement mode of operation



(i) The effect of minority carriers on an n-type InSb transistor operating in depletion



(ii) The effect of minority carrier conduction in the enhancement mode

[The hysteresis present in these characteristics is mainly due to the curve tracer used for their measurement]

(b) In inversion the current near the drain is being carried by minority carriers whereas near the source the conduction is by majority carriers. This will therefore result in a region near the pinch-off point* in which minority carrier recombination is occurring at a rate (see figure (14b)) dependent on current. The random nature of this process is of course a source of noise and will reduce appreciably the inherent low noise properties of the FET (J3).

A schematic representation of this inversion effect together with the result as observed on InSb devices is shown in figures (15a and b). The occurrence of inversion on InSb is a result of the relative high purity of these layers together with the favourable condition of the surface of this material, (i.e. low surface state density and quiescent depletion as will be discussed in chapter VI).

As can be seen from the oscillographs of figure (15b) large hysteresis is present in the inversion region of operation. The reason for this is not clear but it has also been observed on the field effect and differential capacitance curves to be considered in chapters VI and VII and for this reason further discussion will be deferred until then.

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* Shockley (S1) coined the term 'expop' to represent this point. It is an acronym for 'extrapolated pinch-off point' and indicates the necessary extension of his gradual theory into this region.

CHAPTER FOUR

SURFACE ANALYSIS

4.1 Introduction

It has been shown in chapters I and II that the electrical properties associated with a semiconductor surface region differ from those of the bulk. The effect of these differences on an induced space charge is generally described in terms of surface traps, which reduce the effective carrier density and surface scattering which reduces the carrier mobility.*

It is therefore necessary, to characterize a surface electrically, to specify both the number and distribution of the surface traps and the scattering behaviour of the surface. In the last 20 years a considerable effort has been devoted to achieving this for a number of semiconductors and in particular for Si and Ge (M3).

The main difficulty encountered in measuring surface parameters results from the fact that bulk processes remote from the surface essentially dominate any measurement that is made. This bulk contribution can be reduced by working with thin samples but it cannot be completely eliminated owing to the fact that surface parameters must be measured relative to the bulk.

This problem is generally overcome by measuring some property as the surface condition is varied. In this way changes can be ascribed solely to the surface region, the constant bulk contribution being suppressed. An additional advantage of this, of course, is that the surface parameters can then be determined as a function of surface potential.

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* Field emission from impurities within the space charge region as discussed by Abraham and Poehler (A5) can increase μ_{fe} above μ_b but as this is a second order effect it will not be considered further.

This variation of surface potential is usually achieved by means of an applied field as in the field effect transistor, but an alternative technique introduced by Bardeen and Brattain (B10) involves modifying the surface state distribution, and hence occupation, by means of ambient gas variations. Using this technique they were able to swing the surface of Ge over ~ 0.5 eV but by the nature of the method it is not possible to evaluate a unique surface state distribution by this means.

Of the various methods of surface analysis which have evolved perhaps the most popular, because of its essential simplicity, is the field effect measurement. In this the conductance of a slab of semiconductor is measured as the surface potential is varied and by comparison with the expected behaviour a measure of the surface properties can be obtained (M4).

One important consideration however is that both surface scattering and trapping are in general operative and the field effect measurement alone cannot separate these. Assumptions can and have been made (S10, G5, M4) concerning one or other of these mechanisms so as to reduce the problem to one which can be solved by means of a single measurement alone, but the assumptions are generally rather arbitrary and a better approach would appear to consist of measuring two properties simultaneously. Suitable alternatives (M3) to conductance include Hall voltage, surface recombination velocity, surface photovoltage and surface capacitance.

The merits of any particular method will depend on the particular system under investigation but in the case of disordered materials, as employed in the present study, the influence of their structure is the overriding consideration in the choice of a measurement technique. This results from the fact that carrier transport, even when remote from the surface, is

little understood in these materials. Methods not involving longitudinal transport thus seem preferable in this situation and because of this the measurement of differential surface capacitance has been employed in the present work.

As will be apparent later, both surface state density and distribution in energy can be obtained by this method which, when subsequently combined with the results of a conductance measurement, can lead to information on surface mobility.

4.2 Differential Surface Capacitance

Although it is the surface capacitance which is of interest it is not in practice possible to make contact with the surface directly. A blocking contact to current flow is required and this is in general accomplished by means of a dielectric spacer as in the field effect experiment.

The form of this structure is shown in figure (3) and for a voltage V_g applied between the field plate and a low resistance contact to the semiconductor we may write

$$V_g = V_s + V_{ox}$$

where V_{ox} is the voltage dropped across the dielectric and negligible voltage drop is assumed to occur in the metal electrode.*

In terms of charge/unit area $\frac{dV_g}{dQ_g} = \frac{dV_s}{dQ_g} + \frac{dV_{ox}}{dQ_g}$

Now $\frac{dQ_g}{dV_g}$ is the total differential capacitance C_t/unit area measured between

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* The capacitance associated with the space charge in the surface of a metal has been evaluated by Ku and Ullman (K7) and for our purposes can be neglected i.e. $C_{metal} \gg C_{sc}$

the field plate and the semiconductor bulk and $\frac{dQ_g}{dV_{ox}}$ is equal to the dielectric capacitance C_{ox}

$$\therefore \frac{1}{C_t} = \frac{1}{\frac{dQ_g}{dV_s}} + \frac{1}{C_{ox}}$$

and since

$$- Q_g = Q_{sc} + Q_{ss}$$

$$\frac{dQ_g}{dV_s} = C_{sc} + C_{ss}$$

where we define the differential capacitance associated with the space charge and that associated with surface states by

$$C_{sc} = - \frac{dQ_{sc}}{dV_s}$$

and $$C_{ss} = - \frac{dQ_{ss}}{dV_s}$$

$$\therefore \frac{1}{C_t} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{ss}} \qquad (22)$$

The total differential capacitance of the metal - insulator - semiconductor (MIS) structure of figure (3) is thus given by the sum of the geometrically determined and constant dielectric capacitance in series with the parallel combination of the surface state and space charge capacitances as shown in figure (16a).

The surface space charge capacitance is a function of surface potential and the manner in which it varies has been schematically depicted in figure (6). The total differential MIS capacitance is thus of the form shown in figure (17) curve (a). In heavy enhancement and inversion where C_{sc}, and hence the total semiconductor surface capacitance C_s, is large

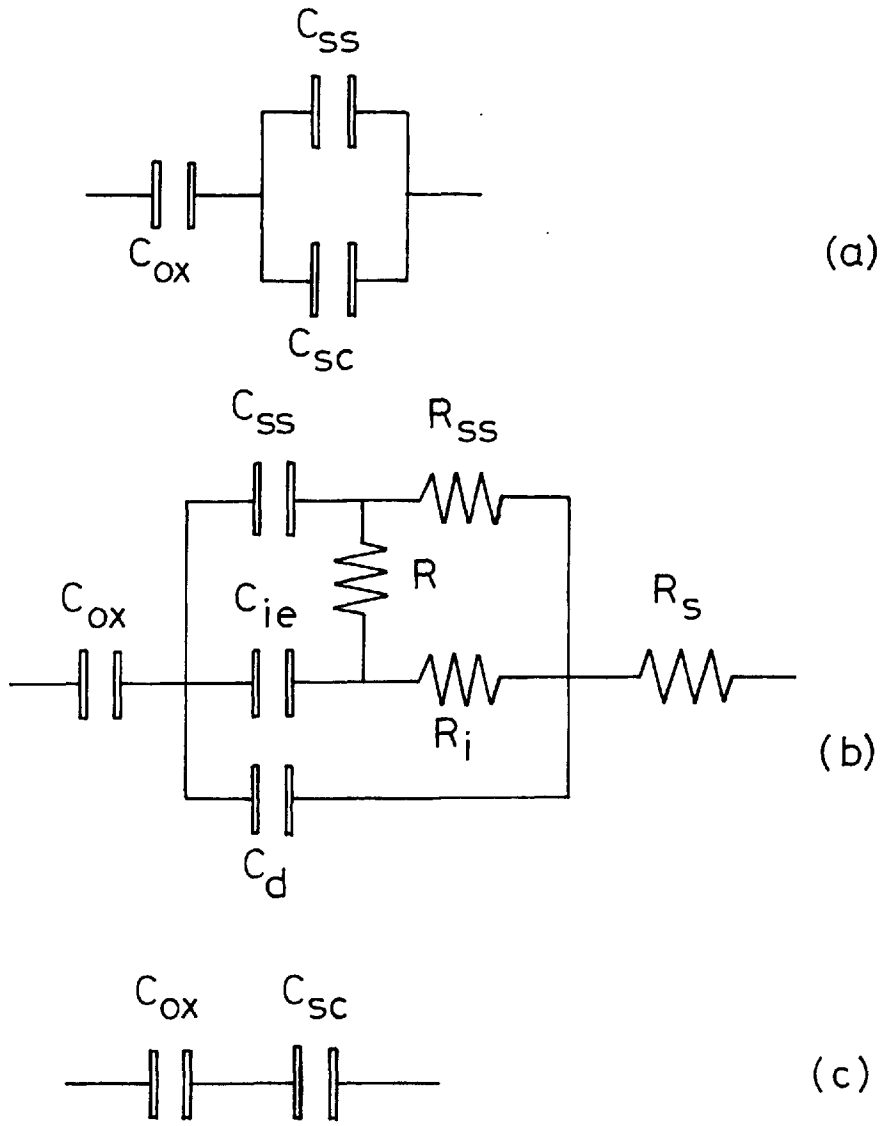

Figure 16

Equivalent Circuits for an MIS Diode

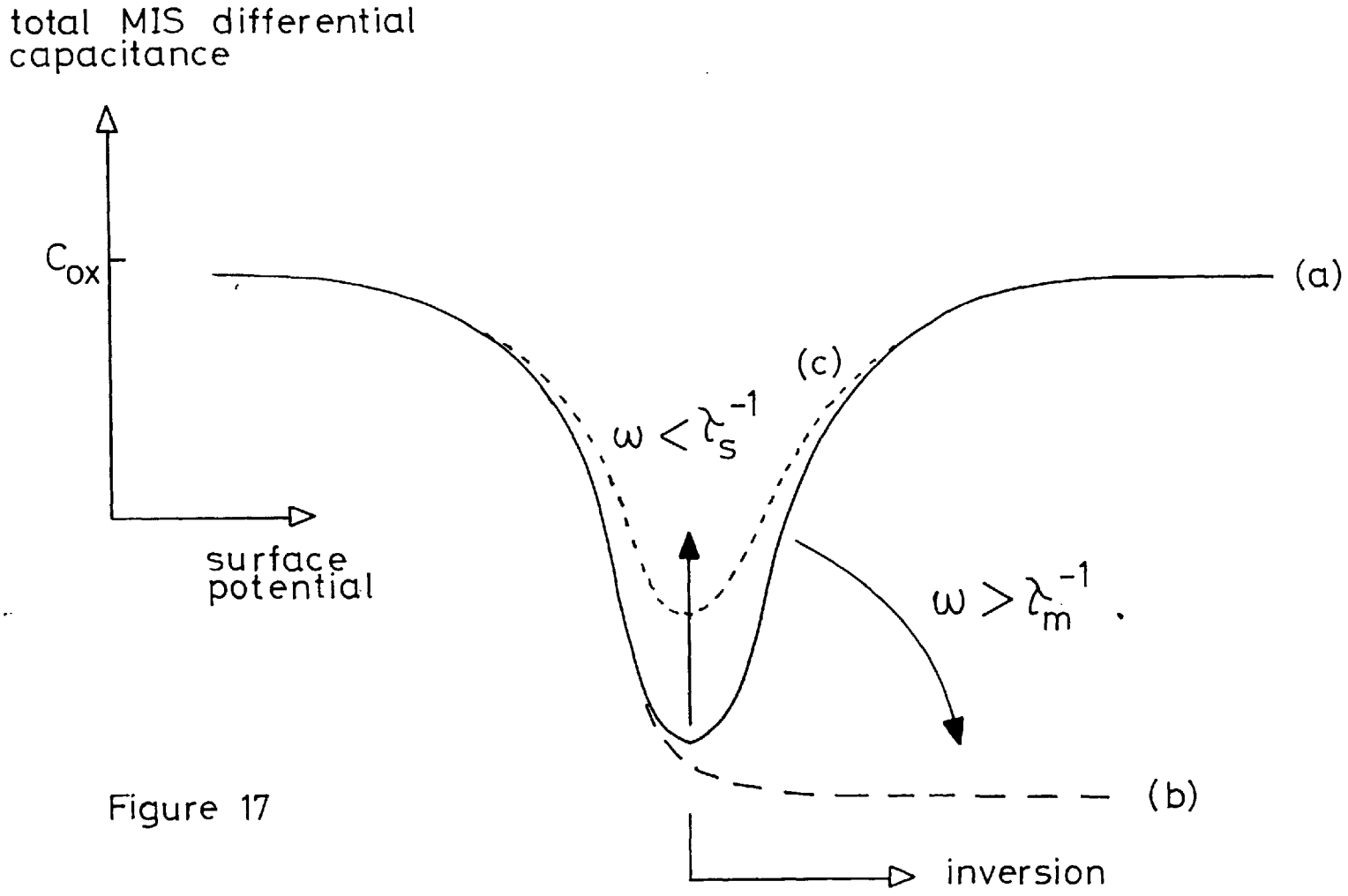
total MIS differential capacitance
C_{ox}
surface potential
(a)
(b)
(c)
$\omega < \tau_s^{-1}$
$\omega > \tau_m^{-1}$.
inversion

Figure 17

$C_t \rightarrow C_{ox}$ in accord with equation (22).

The extent to which C_t varies from C_{ox} depends on both the value of dielectric capacitance and the minimum value of surface capacitance. The larger C_{ox} and the smaller $C_s|_{min}$ the more C_t will deviate from C_{ox}. It will be shown later that $C_{sc}|_{min}$ increases with doping density and for a given semiconductor at a fixed temperature is solely a function of this.

In certain cases it is possible considerably to increase C_{ox} by using a liquid electrolyte (B5) instead of the dielectric spacer of figure (3). This is only possible however if the electrolyte-semiconductor interface is blocking to current flow, but if that condition is satisfied then values of series capacitance as large as $\sim 100\ \mu F/cms^2$ are possible.

As will be seen in chapter VI, to obtain meaningful variations in measured capacitance it is necessary, for the materials under study here, to use very thin dielectric layers, these being typically ~ 200 Å thick.

4.3 Equilibrium Considerations

The way in which charge in the surface region of a semiconductor varies in response to a changing field at the surface is most easily understood in terms of charge relaxation to equilibrium following an abrupt change in the normally applied field. For such a change, which may for example be generated by a step function increment in the voltage applied across the MIS structure of figure (3), the subsequent relaxation to thermal equilibrium may be considered under the following headings:

(i) Surface space charge response in enhancement and depletion

(ii) Surface space charge response in inversion

(iii) Surface state response.

(i) Following the change in applied voltage an immediate change will occur

in the electric field in both the dielectric and the semiconductor. This situation is unstable however and as a result charge flow will occur in that region of the semiconductor in which carriers are present. Both minority and majority carriers will respond but owing to their larger number the contribution of the latter will be greater. This enables modulation of enhancement and depletion layers, which depends on majority carrier flow, to occur rapidly and equilibrium occurs in the order of the semiconductor dielectric relaxation time τ_d, this being typically $\sim 10^{-13}$ secs.

This relaxation is approximately exponential (section 6.1 of M3) and hence in the equivalent circuit of figure (16a) the dynamic response can be accounted for by the inclusion of a resistor R_{sc} in series with C_{sc} where

$$\tau_d = R_{sc}C_{sc}$$

In the frequency domain, where we consider a sinusoid of angular frequency w to replace the step function considered so far, equilibrium essentially requires all the signal to fall across C_{sc}.

At an angular frequency w_o such that

$$w_o = \frac{1}{\tau_d}$$

one half of the applied voltage appears across C_{sc} and the remainder across R_{sc}. This frequency can therefore be taken as that below which equilibrium is maintained, this in the present case being strictly valid.

(ii) In inversion, however, the situation is somewhat different and for a field increment such as to modify an inversion layer the initial charge rearrangement occurs at the back of the depletion layer as a result of the much larger flow of majority carriers in that region as compared with that in the depletion region itself.

This is exactly the same process as initially occurs during minority carrier injection. The space charge is neutralized by majority carriers. (The case of enchancement and depletion corresponding to majority carrier injection). Following this initial charge rearrangement which occurs within $\sim 10^{-13}$ secs. minority carrier generation in the space charge region and within a diffusion length of it results in a relaxation of the inversion and depletion regions to their equilibrium values. The time involved in this process is simply the minority carrier generation time τ_m and for equilibrium of the inversion layer

$$w < \frac{1}{\tau_m}$$

For Si, for which most data is available, it appears that equilibrium in the inversion layer is lost for a frequency $\gtrsim$ 100 c/s (G5). Longitudinal charging of the inversion layer extends this to $\sim$ 1 Mc/s but this is a second order effect which does not apply in our case and will thus not be considered further (N1).

(iii) The problem of charge transfer into and out of surface states is highly complex. It is complicated by surface state and surface space charge interaction which results in the surface state response being dependent on τ_m and τ_d and vice versa.

This problem has been treated by Lehovec and Slobodskoy (L5) and subsequently by Hofstein and Warfield (H6) who analysed it in terms of the equivalent circuit of figure (16b). This circuit is arrived at in quite a straightforward manner by considering the various mechanisms by which charge transfer into the components of surface capacitance can occur. As discussed previously an exponential process is represented in such an equivalent circuit by a simple series RC network.

For this circuit

C_{ss} represents the capacitance associated with surface states.

R_{ss} characterizes the charging of the surface states from the bulk.

C_{ie} accounts for the capacitance associated with the inversion or enhancement layer (this going to zero in depletion).

R_i characterizes the supply of carriers into the inversion layer from the depletion region and from the bulk within a diffusion length of it.

R accounts for the surface state - space charge interaction.

C_d is the depletion capacitance which is absent in enhancement.

R_s is the bulk resistance of the semiconductor and includes any resistance which may be present at the metal - semiconductor contact.

In terms of the parameters of this equivalent circuit;

(a) Inversion layer equilibrium is maintained for

$$w < \frac{1}{\tau_m}$$

where $\tau_m = R_1 C_{ie}$ and $R_1 = \frac{R_i (R + R_{ss})}{R + R_i + R_{ss}}$

(b) Surface state equilibrium is maintained for

$$w < \frac{1}{\tau_s}$$

where $\tau_s = R_2 C_{ss}$ and $R_2 = \frac{R_{ss} (R + R_i)}{R + R_i + R_{ss}}$

All the components of the equivalent circuit are functions of surface potential but for

$$\frac{1}{R_2 C_{ss}} < w < \frac{1}{R_1 C_{ie}} \qquad (23)$$

and $$R_s << \frac{1}{wC_t}$$

the MIS equivalent circuit of figure (16b) reduces to the simple form shown in figure (16c).

All the above has been based on the assumption that the dielectric is lossless. The presence of loss can be accounted for by means of a resistive path in parallel with C_{ox} but for the dielectric used in the present study this is not necessary (see chapter V).

For a frequency such that the conditions of equation (23) are satisfied then the inversion layer will be in equilibrium and the surface states inoperative. For this situation the circuit of figure (16c) is applicable and as has been shown the variation of C_t with V_s is as in figure (17) curve (a).

For increasing frequency the form of the curve in inversion reduces to that of curve (b) where the inversion layer cannot equilibriate and C_s is just C_d.

For decreasing frequency so as to allow surface states to follow the signal the behaviour shifts to curve (c), C_s increases above C_{sc} by an amount given by C_{ss} and C_t tends to a value closer to C_{ox}; this effect being greatest where C_{sc} is smallest.

4.4 The High Frequency Differential Capacitance Method of Surface Analysis

4.4.1 Theory

We shall now assume that the frequency of the capacitance measuring signal satisfies equation (23) i.e. that at the frequency of measurement the inversion layer is in equilibrium and that the surface states are inoperative. In this case the MIS structure of figure (3) can be represented by the equivalent circuit of figure (16c) and C_{sc} is given by equilibrium statistics.

The derivation of C_{sc} as a function of V_s is carried out in appendix

A. Fermi-Dirac distributions, partial impurity ionization and non-parabolicity of the carrier bands are included. These being essential complications when dealing with narrow band gap materials.

As is shown in appendix A

$$C_{sc}(v_s) = \frac{\epsilon\epsilon_o}{2L_o F(v_s)} \left[\frac{N_a}{\alpha} \left\{ 1 + 2 \exp(-v_s - w_{f,a}) \right\}^{-1} - \frac{N_d}{\alpha} \left\{ 1 + 2 \exp(v_s - w_{d,f}) \right\}^{-1} \right.$$

$$- A_v F_{\frac{1}{2}}(-v_s - w_{f,v}) - B_v F_{\frac{3}{2}}(-v_s - w_{f,v}) + A_c F_{\frac{1}{2}}(v_s - w_{c,f})$$

$$\left. + B_c F_{\frac{3}{2}}(v_s - w_{c,f}) \right] \qquad (24)$$

where the F function is given by

$$F(v) = \left[\frac{N_d}{\alpha} \ln \left[\frac{1 + \frac{1}{2} \exp(w_{d,f} - v)}{1 + \frac{1}{2} \exp(w_{d,f})} \right] + \frac{N_a}{\alpha} \ln \left[\frac{1 + \frac{1}{2} \exp(w_{f,a} + v)}{1 + \frac{1}{2} \exp(w_{f,a})} \right] \right.$$

$$+ \frac{2}{3} A_v \left[F_{\frac{3}{2}}(-v - w_{f,v}) - F_{\frac{3}{2}}(-w_{f,v}) \right]$$

$$+ \frac{2}{5} B_v \left[F_{\frac{5}{2}}(-v - w_{f,v}) - F_{\frac{5}{2}}(-w_{f,v}) \right]$$

$$+ \frac{2}{3} A_c \left[F_{\frac{3}{2}}(v - w_{c,f}) - F_{\frac{3}{2}}(-w_{c,f}) \right]$$

$$\left. + \frac{2}{5} B_c \left[F_{\frac{5}{2}}(v - w_{c,f}) - F_{\frac{5}{2}}(-w_{c,f}) \right] \right]^{\frac{1}{2}} \qquad (25)$$

v is the reduced potential given by $\frac{qV}{kT}$, all other terms being defined in appendix A.

Owing to the complexity of this expression its evaluation has been programmed * and carried out on an IBM 7090 computer.

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* This program is an extension of that written by Juhasz (J2) to include the calculation of differential surface capacitance. A brief outline of the method of computation is given in appendix C.

Figure (18) shows a typical set of results. In that figure

$$\frac{C_t}{C_{ox}} = \frac{C_{sc}}{C_{sc} + C_{ox}} \tag{26}$$

is plotted versus surface potential for InSb at 77°K. The insulator capacitance is taken as 0.4 $\mu F/cms^2$ and the running parameter is doping density (donor impurities assumed).

It has been pointed out in section 4.2 and is shown in appendix A that the overall change in C_t from C_{ox}, for a given value of dielectric capacitance and a fixed temperature, is solely a function of doping density. The way in which $C_{sc}|_{min}$ varies with doping for p-type PbTe and n-type InSb is shown in figure (19). The materials parameters used in this evaluation are listed in table (i) and discussed in chapter VII but what should be noticed from figure (19) is that for PbTe with its large value of dielectric constant the surface capacitance at the minimum can be as large as 3 $\mu F/cms^2$ at a doping density of $5 \times 10^{17}/cms^3$. This corresponds to less than a 5% overall change in C_t for a dielectric of 400 Å thickness with an assumed relative permittivity of 6. It will be seen in chapter VI that these figures are typically realized in practice and for that reason a capacitance measuring technique of high sensitivity is required.

From figure (18) it can be seen that for $N_d \gtrsim 10^{16}$ cms^{-3} C_t exhibits a subsidiary maxima. This is solely due to the fact that deionization of impurities has been included in the theoretical analysis. The maximum is a result of charge transfer into those impurity levels lying within the space charge region. This however should not be confused with surface state charging. The theoretical analysis does not include the effect of surface states in accord with the assumption of high frequency of measurement and the corres-

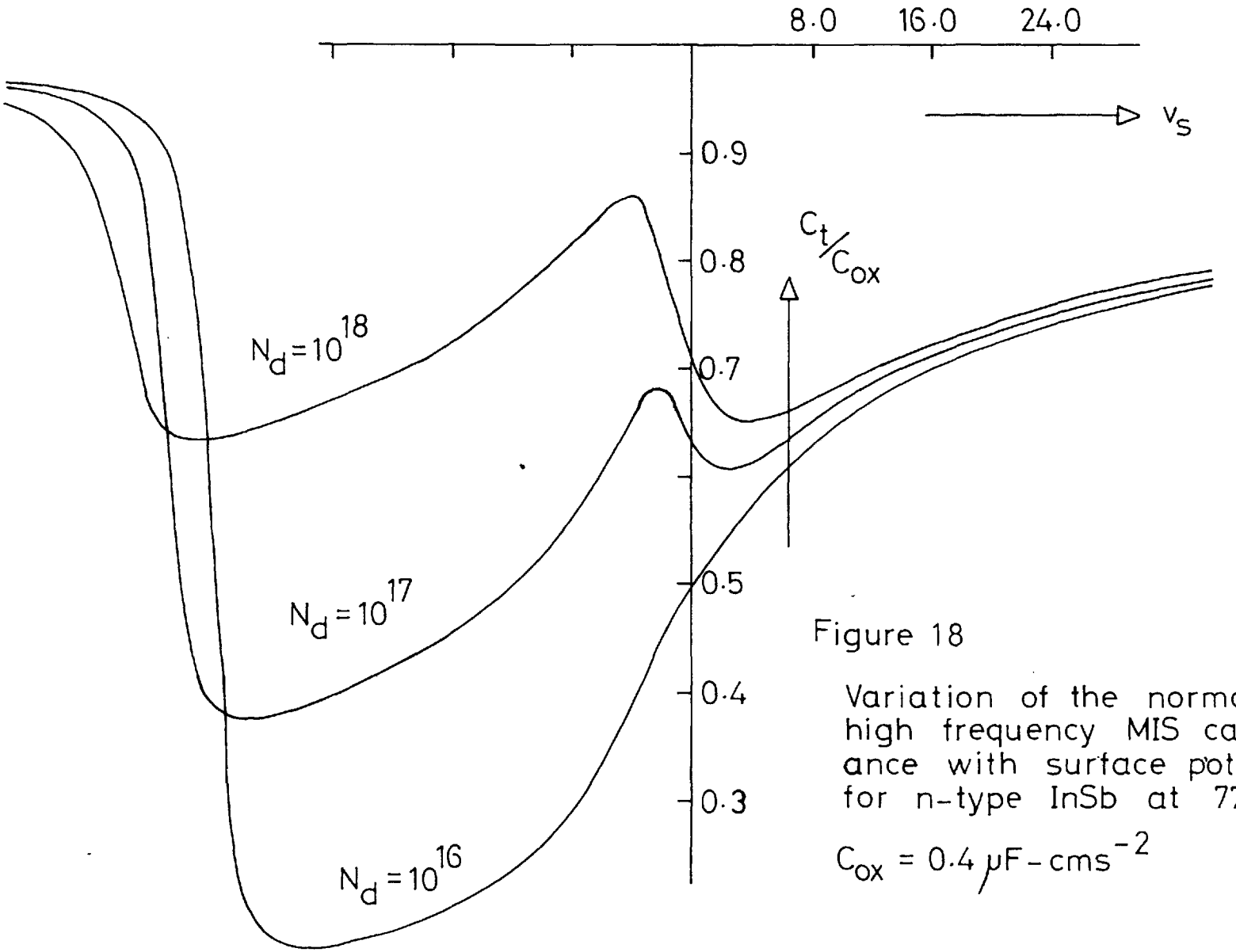


Figure 18

Variation of the normalized high frequency MIS capacitance with surface potential for n-type InSb at 77°K

$C_{ox} = 0.4\ \mu F - cms^{-2}$

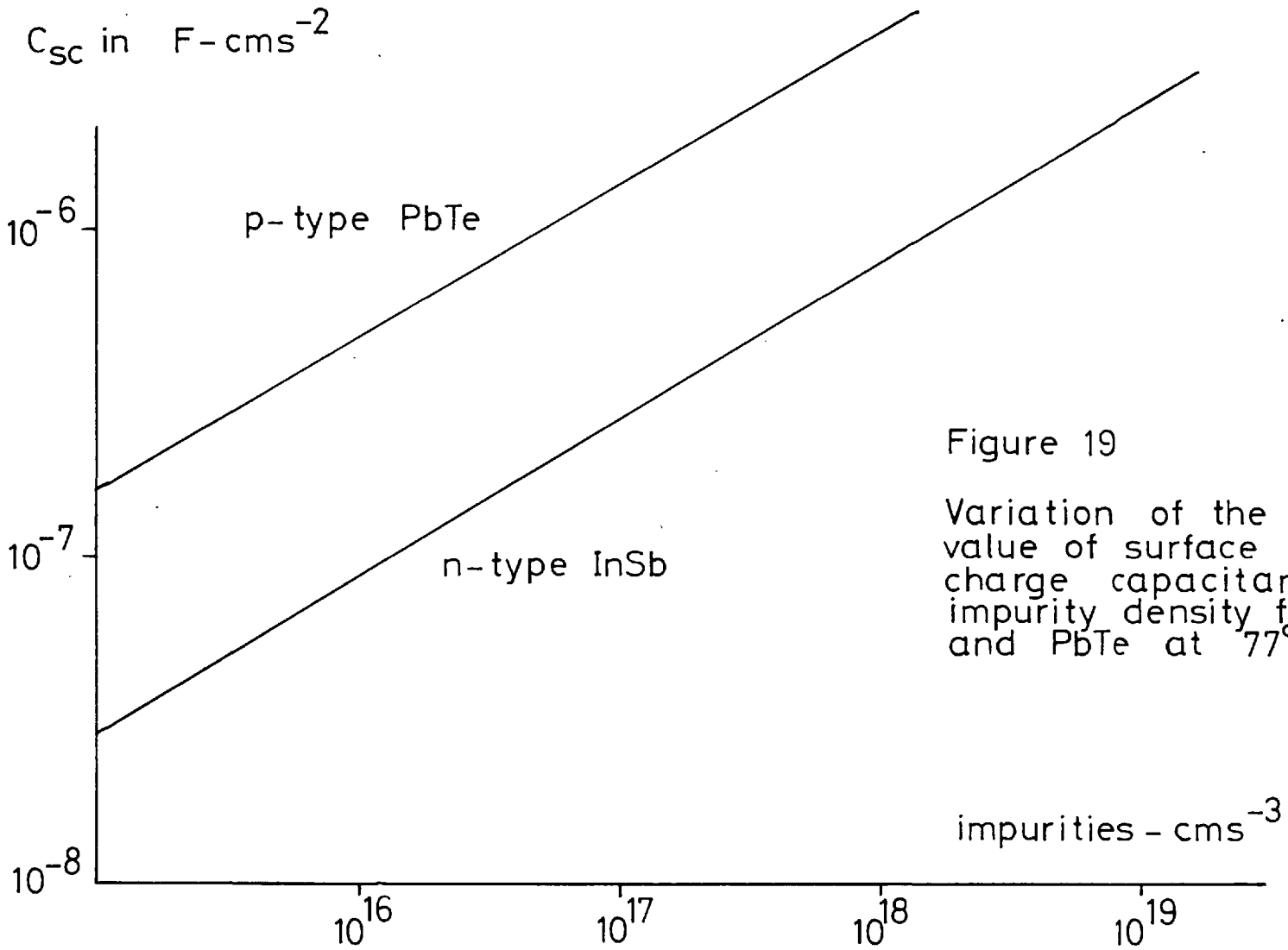


Figure 19

Variation of the minimum value of surface space charge capacitance with impurity density for InSb and PbTe at 77°K

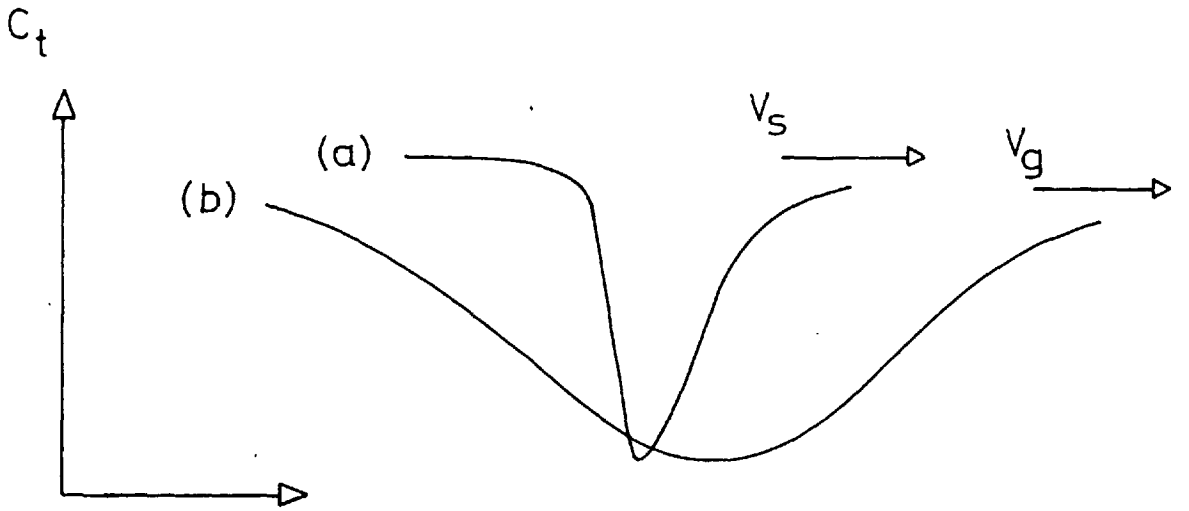
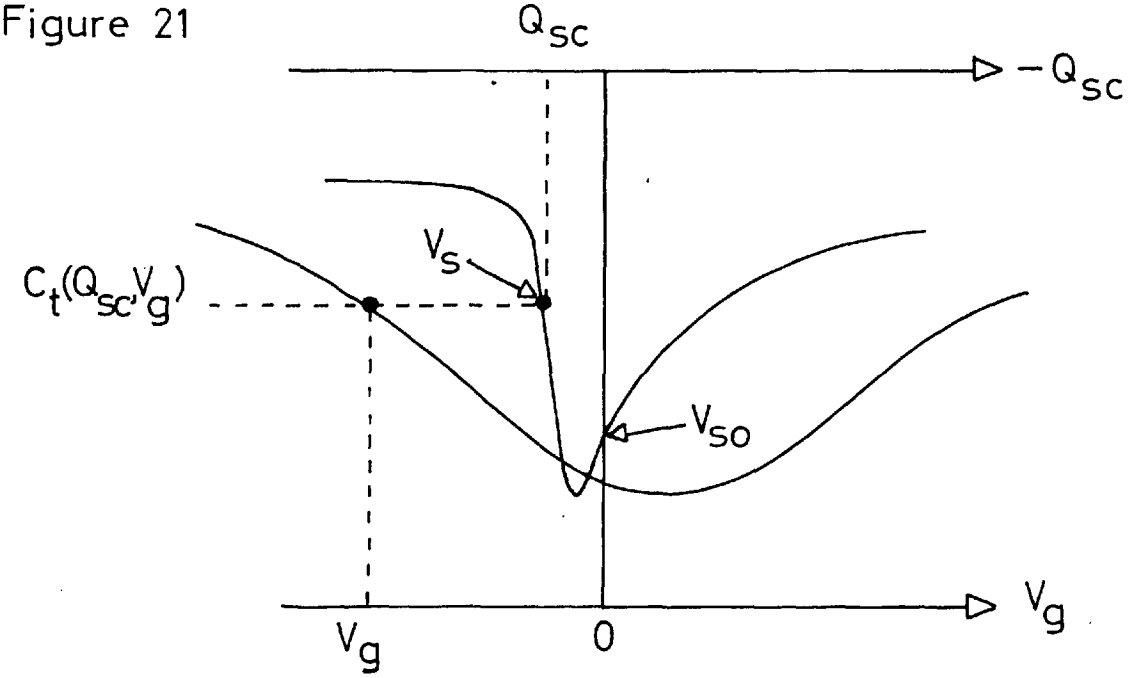


Figure 20 Schematic representation of the experimental and theoretical variation of MIS capacitance with potential

Figure 21



$$Q_{ss} = C_{ox}(V_s^o - V_g) - Q_{sc}$$

where $V_s^o = (V_s - V_{so})$

ponding validity of the high frequency equivalent circuit of figure (16c).

Practically all* previously reported work on this capacitive method of surface analysis has been carried out on wide band gap materials and in particular on the Si surface (T6, L6, H7, I1). Non-degenerate statistics have been used and in such cases it is usual to assume complete impurity ionization. As a result this fine detail has not been reported previously. The consequences of this are probably small in the case of the wide band gap materials but for narrow band gap semiconductors where much of the band gap can be investigated its omission can lead to large errors.

4.4.2 Experimental

The surface space charge capacitance C_{sc} is a unique function of surface potential and knowing C_{sc} thus enables the corresponding value of V_s to be found.

Experimentally, as will be described in chapter V, the total MIS differential capacitance C_t is measured as the surface potential is varied by means of a slowly varying bias voltage applied between the field plate and the semiconductor of figure (3). Surface states are assumed inoperative at the high frequency of measurement but they will follow the slowly changing bias and the result will be as shown in figure (20). Curve (a) is simply the same as figure (18), i.e. a plot of C_t versus V_s in the absence of effective surface states and curve (b) represents the form of the experimentally measured high frequency differential capacitance variation.

A given value of C_t on either curve must correspond to the same value of V_s as in both, surface states are excluded as far as the capacitance

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* see reference (C4) for the only exception of which the present author is aware

is concerned.

In the experimental case, however, the value of V_g at which this chosen value of C_t occurs will depend on the surface state density. V_g is varying relatively slowly and as a result the fast surface states will remain in equilibrium with it.

Consider that the experimental C_t versus V_g curve is available having a shape of the general form of curve (b) of figure (20). It is first necessary to chose C_{ox}. This is done by drawing the asymptote to the experimental curve but as will be seen in chapter VI this cannot always be done unequivocally. Once C_{ox} is known it is then possible to derive C_{sc} at the minimum using equation (26). For a given material and temperature $C_{sc}|_{min}$ defines uniquely the doping density in the space charge region of the semiconductor. For InSb and PbTe the relationship is as shown in figure (19). If the material is non-stoichiometric then this average doping density will admittedly vary with the extent of the space charge i.e. surface potential, but effective doping as evaluated by this means is probably more meaningful than an average over the entire thickness of the sample as would be found by a Hall measurement.

Knowing C_{ox} and the doping density enables the theoretical C_t versus V_s curve to be derived by means of equation (24) and (25). At each value of C_t it is then possible to equate corresponding values of V_g and V_s, the former from the experimental and the latter from the theoretical curve.

It is shown in appendix A that in addition to C_{sc} the values of Q_{sc}, ΔN and ΔP are all uniquely defined by V_s. Q_{sc} is therefore known as a function of V_g.

Furthermore the total induced surface charge Q_g can be calculated

from

$$Q_g = C^o V_g \tag{27}$$

where C^o is the total MIS capacitance.

C^o is the large signal capacitance and is related to the differential capacitance C_t by

$$C_t = C^o + V_g \frac{dC^o}{dV_g} \quad * \tag{28}$$

Alternatively, Q_t may be calculated from

$$Q_g = C_{ox} (V_g - V_s^o) \tag{29}$$

where V_s^o is the change in surface potential from its quiescent zero gate voltage value.

Knowing both Q_{sc} and Q_g as a function of V_s and V_g the charge in surface states Q_{ss} may be evaluated as a function of surface potential from

$$Q_t = - Q_g = Q_{sc} + Q_{ss}$$

In summary the technique therefore requires the experimenter to:

(1) Experimentally derive the high frequency differential capacitance versus gate voltage curve.

(2) Choose C_{ox} from the asymptote.

(3) Calculate $C_{sc}\big|_{min}$ from

$$C_{sc} = \frac{C_t C_{ox}}{C_{ox} - C_t}$$

(4) Find doping density from figure (19) in the case of InSb or PbTe at 77^oK

---

* $C^o = \frac{Q_t}{V_g}$

$\therefore \frac{dC^o}{dV_g} = \frac{1}{V_g} \frac{dQ_t}{dV_g} - \frac{Q_t}{V_g^2}$ i.e. $C_t = \frac{dQ_t}{dV_g} = C^o + V_g \frac{dC^o}{dV_g}$

(5) Calculate the theoretical C_t versus Q_{sc} curve using these values of C_{ox} and effective doping density.

(6) At each value of V_s calculate Q_t from

$$Q_t = C_{ox} (V_s^o - V_g)$$

(7) Calculate Q_{ss} at each value of V_s using

$$Q_{ss} = Q_t - Q_{sc}$$

This is depicted graphically in figure (21).

From this measurement it is therefore possible to derive the way in which the total net charge trapped in surface states varies with surface potential.

Once this distribution is known it is a simple matter to derive the effective density of surface states.* At low temperature the electron distribution function is to good approximation a step function. As surface states move past the Fermi level at the surface their occupancy must change in accordance with the discussion of section 2.3.1. The rate at which the occupancy changes, i.e. the rate of change of the net trapped charge, is simply given by the number of surface states at the Fermi level as shown in figure (22).

The effective density of surface states N_{ss} at a particular value of surface potential is therefore given by the derivative of the total trapped charge curve with respect to surface potential at that value of surface potential; the usual units for N_{ss} being / cms^2 - eV.

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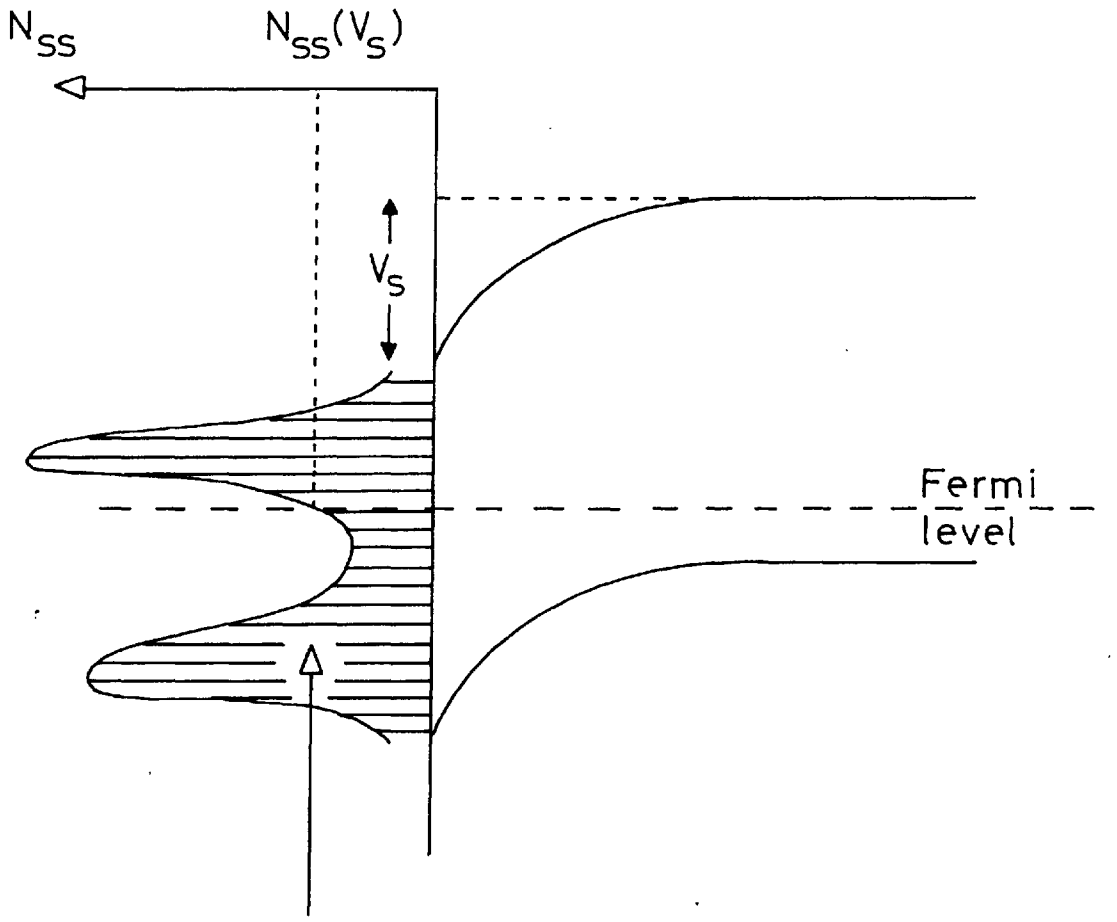
* This method, as with most surface investigation techniques, determines only the difference between a measured and a theoretically expected variation. This difference is then attributed to 'surface states'. What these states might be physically will be discussed in chapter VII.

Figure 22



TOTAL NET TRAPPED CHARGE $Q_{SS}(V_S)$

EFFECTIVE DENSITY OF SURFACE STATES

$$N_{SS}(V_S) = \frac{dQ_{SS}(V_S)}{q.dV_S}$$

4.5 The Evaluation of Surface Mobility

It has been shown in section 4.4 that a differential capacitance measurement can lead to a knowledge of sample doping and also to a relationship between V_g and V_s. Just as Q_{sc} and C_{sc} are uniquely defined by V_s so are the carrier excesses ΔN and ΔP. The differential capacitance method thus enables a unique relationship between V_g and ΔN and ΔP to be found.

This knowledge coupled with the results of a field effect measurement therefore enables a plot of sample sheet conductance σ versus carrier excess to be made.

From section 2.5 we have by definition

$$\Delta\sigma = q\,(\mu_{ns}\Delta N + \mu_{ps}\Delta P)$$

For a one carrier system, for example enhancement or depletion of n-type material,

$$\Delta\sigma \cong q\mu_{ns}\Delta N$$

and $$\mu_{ns} = \frac{\Delta\sigma}{q\Delta N}$$

Similarly for p-type operation i.e. n-type material in inversion or p-type material in enhancement or depletion

$$\mu_{ps} = \frac{\Delta\sigma}{q\Delta P}$$

thus by replotting the field effect curve of σ versus V_g as σ versus ΔN (or ΔP) and taking the origin at flat band ($V_s = 0$) it is possible to derive the surface mobility of carriers as a function of surface potential by taking the slope of chords to the curve from the origin.

Surface mobility is an average mobility of carriers in the space charge region where the average is taken over all the carriers in that region.

An alternative mobility can be defined by

$$\mu_s\Big|_{diff} = \frac{1}{q}\frac{d\Delta\sigma}{d\Delta N}$$

where this differential surface mobility, which is an average taken only over those carriers incrementally induced into the space charge region, is given by the slope of the $\Delta\sigma$ versus ΔN curve.

This differential mobility, which reduces to the field effect mobility of section 2.7 in the absence of trapping, is related to the surface mobility in the following way

By definition $\mu_{ns} = \frac{\Delta\sigma}{q\Delta N}$ for electrons

$$\therefore \quad \frac{d\mu_{ns}}{d\Delta N} = \frac{q\Delta N\frac{d\Delta\sigma}{d\Delta N} - q\Delta\sigma}{(q\Delta N)^2}$$

$$= \frac{\mu_{ns}\Big|_{diff}}{\Delta N} - \frac{\Delta\sigma}{q\,(\Delta N)^2}$$

$$\therefore \quad \mu_{ns}\Big|_{diff} = \mu_{ns} + \Delta N\frac{d\mu_{ns}}{d\Delta N}$$

and $\mu_{ns}\Big|_{diff} \longrightarrow \mu_{ns}$ at flat band or for constant surface mobility.

In the foregoing analysis no mention has been made of the effect of work function difference between the metal and the semiconductor.

In a system free from surface states a difference in work function would result in a built in surface space charge this being the larger the smaller the physical separation between the semiconductor and the metal. In the presence of surface states however some of the work function difference is taken up by charge in surface states (B9). Although in the present investigation the fast states are not so numerous as to completely eliminate the effect, the slow states are (see section 5.4).

As a result of this the quiescent surface potential is essentially independent of the work function of the metal and will therefore be neglected.

CHAPTER FIVE

EXPERIMENTAL TECHNIQUES

5.1 The Evaporation System

The evaporator in which the semiconductor layers were prepared is shown in figure (23). The chamber was oil pumped by means of an Edwards 6" diffusion pump type 6M3A containing type 704 silicone fluid*; backing being provided by a single stage Edwards rotary pump type 1SC 450B.

The system was baffled and liquid nitrogen trapped and was capable of an ultimate base pressure, following a mild bake, of $\sim 6 \times 10^{-8}$ torr, this pressure being measured by an ionization gauge situated at the bottom of the chamber.

The interior of the vacuum chamber is shown in figure (24). The substrate heater was wound from 40 thou. tantalum wire and could accommodate substrates of up to a maximum size of $2\frac{1}{2}$" x 2". The substrates were heated radiantly from the back, their temperature being measured by means of a chromel-alumel thermocouple. This was embedded in a layer of colloidal graphite which was painted onto the backs of the substrates prior to their being mounted in the vacuum system.

The evaporation rate and film thickness were measured by means of an Edwards thickness monitor which was calibrated interferometrically for each material using a Varian Å-scope. The associated quartz crystal was thermally baffled to minimize the effects of radiant heating.

The films of PbTe were prepared by thermal evaporation of the compound, at a rate of ~ 5 Å/sec, from a tantalum wire wound silica furnace.

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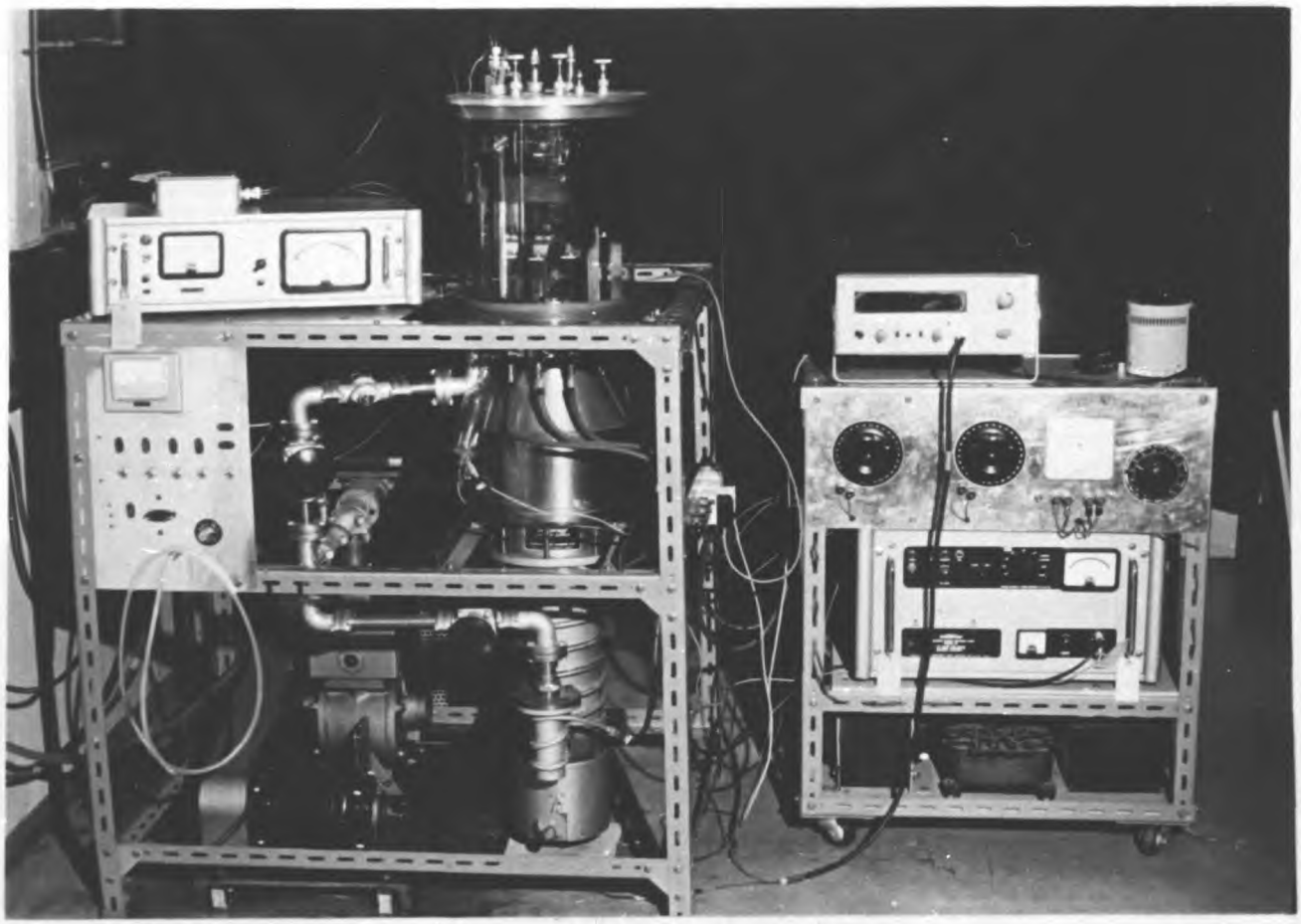
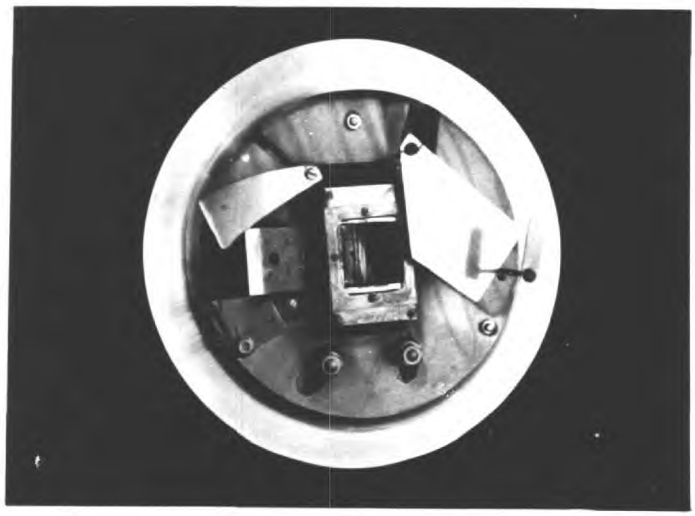
* A Midland Silicones product.

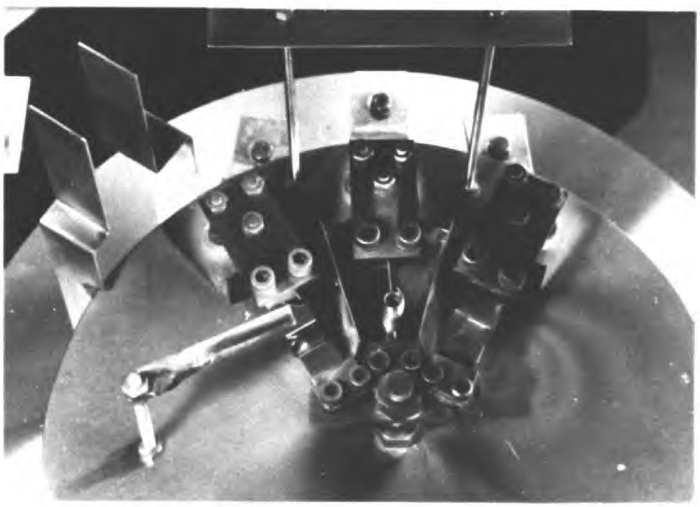
Figure 23



The evaporation system together with ancillary control and monitoring equipment



The chamber top plate supporting the substrate enclosure and quartz monitor crystal



From left to right the InSb, PbTe and SiO_x source assemblies

The source material employed was obtained both at 5N purity from Koch Light Laboratories and at ~ 10^{18} impurities - cms^{-3} from the Zenith Corporation. In both cases the material was p-type.

As no significant difference was observed in the physical or electrical properties of films prepared from these two materials the Koch Light material was used more extensively owing to its easier availability.

The PbTe was finely ground in a silica crucible before being loaded into the source and before deposition was pre-heated to drive off any excess free Te, which in the Koch Light material was observed to be appreciable. The chamber pressure during the PbTe evaporation was typically better than 1×10^{-6} torr owing to the low source temperature at which sublimation occurred.

Flash evaporation was employed for the InSb deposition. The InSb, in power form, was loaded into a molybdenum shute and, following outgassing of the V-shaped molybdenum source, was dispensed from the feed shute by mechanical agitation from outside the chamber. It was not possible by this means to control the evaporation rate very closely. However, previous work on the evaporation of InSb (W8, J2) has indicated that rate is relatively unimportant, the electrical properties being more a function of the post deposition annealing temperature. During the evaporation of the InSb the pressure generally rose to ~ 7×10^{-6} torr as a result of the high source temperatures employed (~ 1400°C).

SiO_2 supplied by the Kemet Company was used to encapsulate some of the semiconductor layers. This was evaporated from a molybdenum boat which was covered with a screen of 60 mesh tantalum gauze to prevent spitting of the source charge.

5.2 Device Fabrication

It has been shown in chapter IV that to achieve meaningful variations of MIS differential capacitance when using such evaporated semiconductors as PbTe and InSb it is necessary to go to large values of dielectric capacitance.

Evaporated insulators such as SiO_x and MgF_2 are invariably of poor quality when thinner than ~ 1000 Å due to the presence of pin holes.

Anodically formed oxides of various metals have however been shown to improve electrically as their thickness is decreased (K9) and this fact, for the requirements of the present study, seemed to indicate their superior suitability.

5.2.1 Anodization (Y1)

Anodization involves the oxidation of a conductor by ionic transport in an electrolyte under the action of an applied electric field.

The mechanism of oxide growth at the anode is not completely understood and whether metal or oxygen ion transport is involved in the process is believed to depend on the particular metal used. In the case of Al and Ta however (A6) it seems likely that oxide growth is in fact a result of metal transport through the oxide to the growing oxide-electrolyte interface.

Depending upon the rate at which the electrolyte dissolves the oxide, either porous or continuous oxide films will be formed (H8). The former, occurring in high etch rate electrolytes, have poor electrical properties and are mainly employed for decorative purposes. The oxide in this case can grow to be many microns thick.

For good electrical insulation non-porous layers are required and in this case, for a given voltage applied between the anodizing surface and a cathode, a fixed oxide thickness will result, this being essentially time

independent after the initial growth period has passed. For such non-porous layers it is in fact possible, for a given electrolyte-metal system, to ascribe a figure to the thickness of oxide to be expected for a given voltage applied; this being typically ~ 12 Å/volt.

Because of its ease of evaporation aluminium was used for the field plate electrode. Throughout the course of this work all metallization was carried out in an Edwards 12E6 evaporator. To have prepared the metal layers in the same system as was used for the semiconductor evaporation would have introduced an unnecessary source of contamination for the latter.

Wet anodization of the Al was carried out in a system schematically illustrated in figure (25). The cathode was of spec. pure Al and three different electrolytes were employed:

(a) A 4% by weight aqueous solution of boric acid adjusted to a pH of ~ 6.0 by the addition of a small amount of sodium tetraborate.
(b) A 10% by weight solution of ammonium pentaborate in glycol.
(c) An ammonium - glycol - borate electrolyte supplied by the Plessey Company.

The last of these proved to be the most successful and was used exclusively throughout the final stages of the study. Both of the other electrolytes suffered from the fact that attack of the Al invariably occurred leading to pin hole formation in the Al film. Worse however was the fact that, for the aqueous based electrolyte especially, severe etching occurred at that region of the Al where it passed through the liquid surface. This was observed to be the result of boric acid dissociating from solution and crystallizing out along the electrolyte-film interface. Although this could be reduced by stirring and keeping the current at a low level during anodization it was

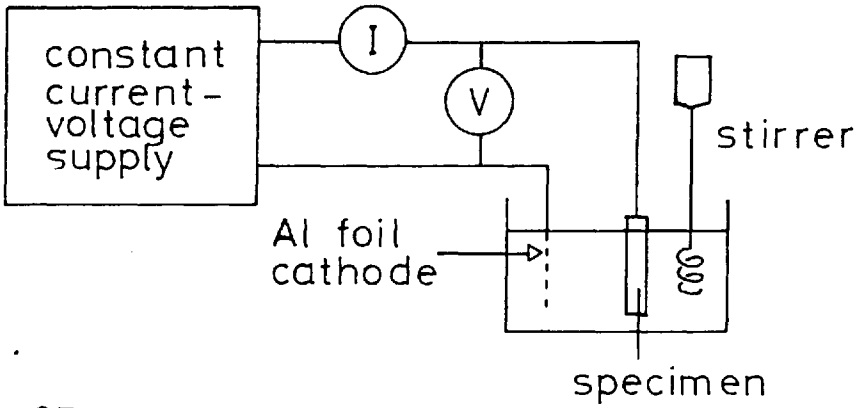


Figure 25
Schematic of the anodization apparatus

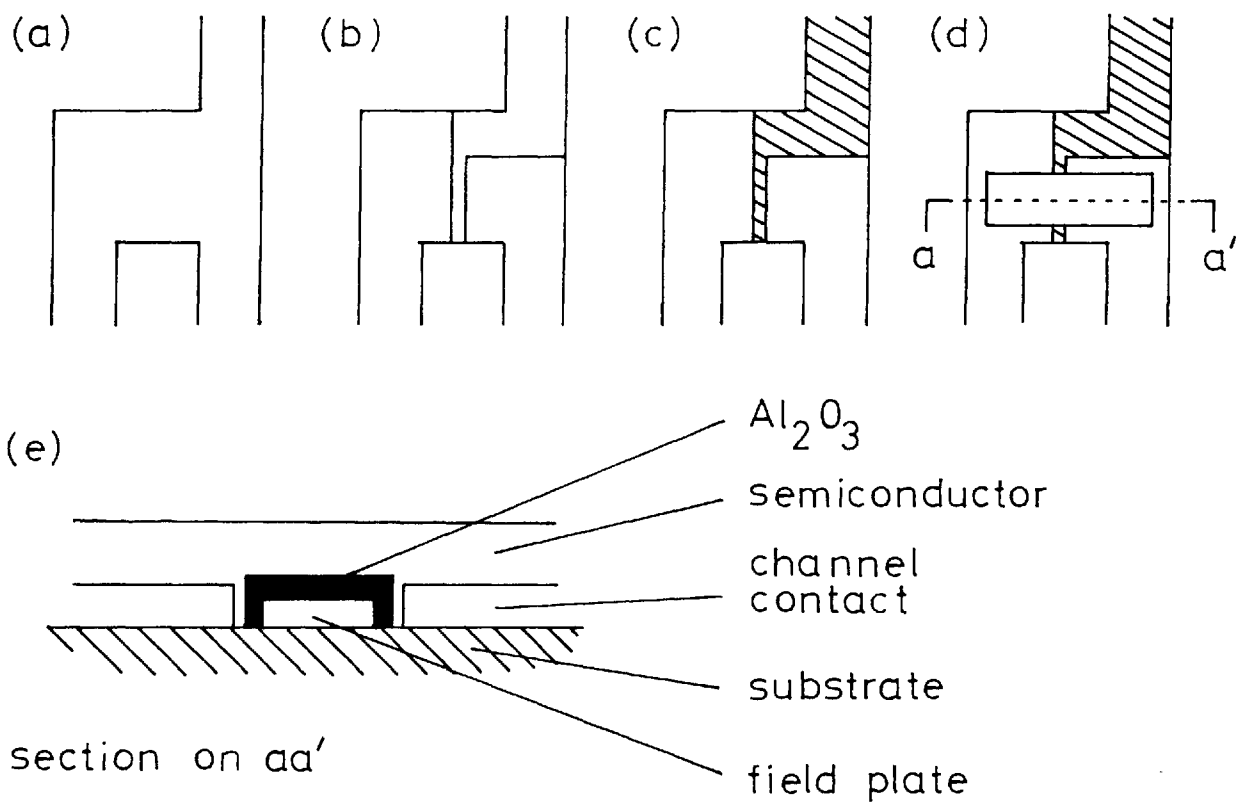


Figure 26 Device structure A

not possible completely to eliminate the effect, and in many cases complete open circuiting of the Al film occurred as a result of it.

Apart from this, if the oxides formed successfuly they were of similar quality quite irrespective of the particular electrolyte used.

An initial feasibility study on Al - Al_2O_3 - Al capacitors at 300°K indicated a loss tangent for this dielectric of $< 1\%$ at 1592 c/s and a breakdown field of $\sim 1 \times 10^6$ v/cms at thicknesses $\gtrsim 500$ Å, this increasing to as much as 5×10^6 v/cms for thicknesses ~ 150 Å. This form of thickness-dependent behaviour has been observed by Kawamura and Azuma (K9) who attributed it to the fact that avalanche breakdown cannot occur for dielectric thicknesses less than the electronic mean free path.

At 77°K, the temperature at which all surface measurements were made, the electric field strength appeared to be even larger than its room temperature value.

5.2.2 Device Structure A

During the course of this work two different MIS structures were developed. The first of these, intended particularly to fulfil the needs of a high frequency transistor, was fabricated as follows:

Al was evaporated onto a vapour degreased and thermally baked glass* substrate to the pattern shown in figure (26a). The pattern shown in figure (26b) was then scribed and the shaded area in figure (26c) was then selectively anodized to form the gate insulator. The semiconductor was subsequently evaporated as shown in figure (26d) leading to the completed transistor structure shown in cross section in figure (26e). Electrically this structure

* Corning 7059 glass was used throughout this study.

is equivalent to that of figure (1b). It can be seen that overlap of the gate, source and drain is completely and automatically eliminated by this technique of 'coplanar delineation' and hence the degrading effects of parasitic inter-electrode capacitance are minimised.

Although a minimum source to drain spacing of ~ 100μ was all that was possible with the crude techniques employed, this method of fabrication would be ideally suited to electron or laser beam machining. Using these refined methods of pattern delineation it should be at present possible to achieve source-drain spacings of ~ 10μ which is comparable with those currently attained by more conventional photo-lithographic methods. The advantage of the mechanical machining method however lies in its high speed and simplicity of operation.

One major limitation of this method and one which in fact prevented its successful exploitation in the present work, is the fact that the source and drain are necessarily of Al. As has been shown in section 3.3.2, Al does not make a good contact to the semiconductors of interest here and as a result, for the present purpose, this structure proved to be of no further value.

Alternative metals such as tantalum or hafnium could be used or alternatively the Al source and drain could be electroplated with a more suitable contact material. Because of the development time required however, these possibilities were not investigated.

5.2.3 Device Structure B

The second structure was developed to overcome the problems encountered with the earlier device. In addition however it was required to satisfy the need for a low value of series resistance (R_s of section 4.3).

As will become evident in section 5.4.1, owing to the method of

capacitance measurement chosen a very small value of loss tangent is required. The presence of series resistance manifests itself in this respect by raising the apparent loss above that associated with the dielectric i.e. (W10)

$$\text{Measured loss tangent} = \text{Actual loss tangent} + R_s\left[wC + \frac{1}{wR^2C}\right]$$

where C and R are the parallel components of dielectric impedance. R_s must, as will become evident, be below $\sim 0.5\,\Omega/\text{cms}^2$ in the present case.

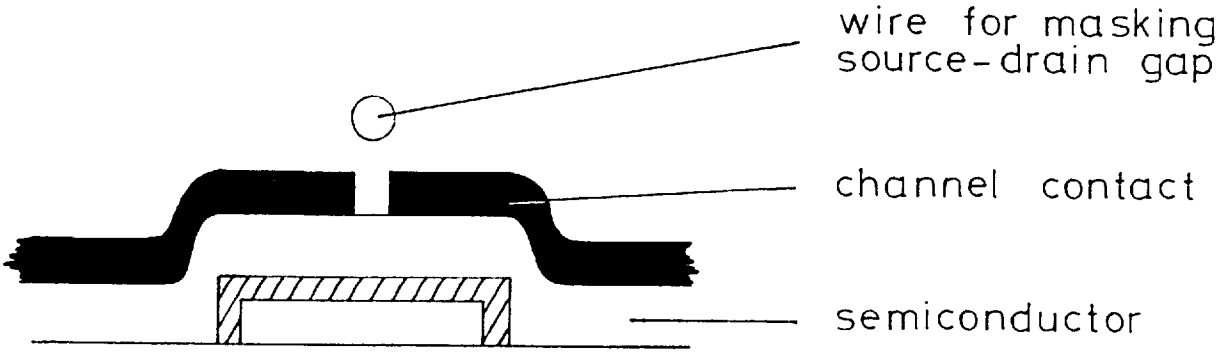
Both these requirements are satisfied by the geometry shown in cross section in figure (27a). The Al gate is initially evaporated as a strip of $\sim 500\mu$ width, this being then anodized to form the gate insulation. Following this the semiconductor is evaporated across the gate strip, it being possible on a 2" x 1" substrate to fabricate 6 of these devices together with 6 Hall samples simultaneously as shown in figure (27b). Subsequent to, and overlying the semiconductor the source and drain electrodes of In or Sn are deposited; the source-drain spacing being defined by means of a wire spot welded across a molybdenum aperture mask. By this means spacings of less than 50μ are readily achieved.

It can be seen from figure (27a) that this structure is essentially that of a plane parallel capacitor, the series resistance being simply that presented by the semiconductor film which is only $\sim$ 2000 Å thick together with any contact resistance which may be present. These in practice proved so small that loss tangents at 1 Mc/s were invariably $<$ 15%, this corresponding to a value of $R_s < 0.25\,\Omega/\text{cms}^2$.

5.3 Hall and Resistivity Measurements

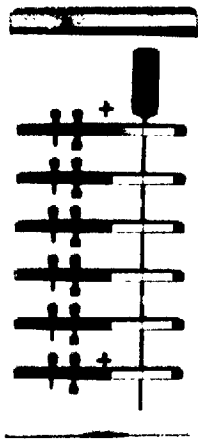
Hall voltage and resistivity measurements were carried out by standard dc techniques (P10) using an evaporated sample geometry as shown in figure (27c).

Figure 27

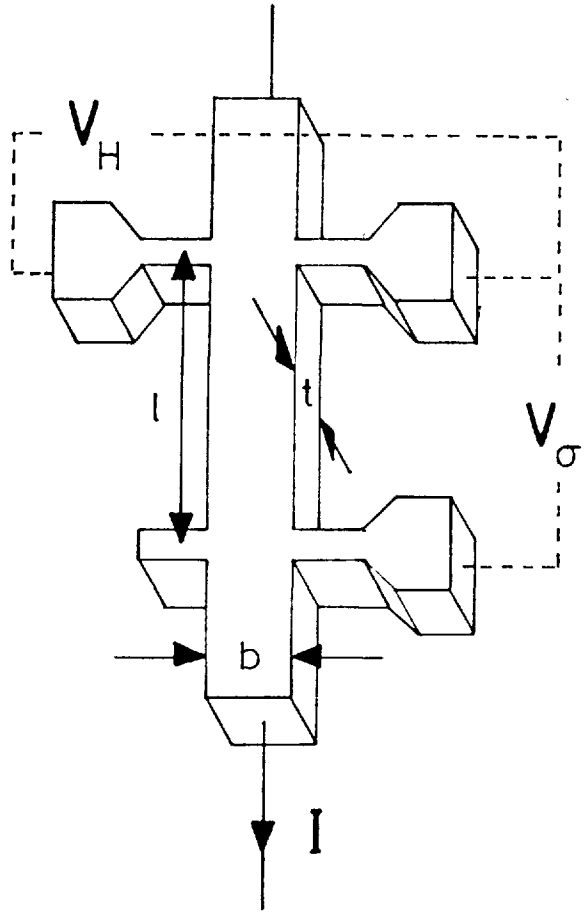


(a) Device structure B in cross section

(b)



Physical realisation (actual size) of structures 'a' and 'c' showing the gate electrode common to all six devices.



(c) Hall sample geometry

Indium soldered contacts were employed and Hall and conductivity voltages were measured using a digital voltmeter whose maximum input impedance was > 5000MΩ. Nevertheless at low temperatures the impedance of the PbTe samples invariably rose to such a high value as to lead to serious sample loading. This set the low temperature limit on the measuring technique in the case of PbTe. For InSb the measurements were possible to 77°K, these being carried out in a liquid nitrogen cooled cryostat of simple construction. The sample temperature was measured by means of a copper-constanton thermocouple.

The Hall coefficient R_H which is defined by $E_H/B.J$ and the Hall mobility μ_H given by (σR_H) are calculated for the sample geometry of figure (27c) by means of the expressions

$$R_H = \frac{t\ V_H}{I\ B} \quad \text{cms}^3/\text{coulomb}$$

and $$\mu_H = \frac{V_H}{V}\frac{l}{Bb} \quad \text{cms}^2/\text{volt-sec.}$$

where E_H is the transverse Hall field

V_H is the Hall voltage

V is the conductivity voltage

B is the normal component of magnetic flux

J is the longitudinal current density

I is the total longitudinal current

and l, b and t are the geometric parameters of figure (27c).

A permanent magnet giving approximately a 0.2 webers/cms^2 magnetic flux was employed for these measurements.

The Hall coefficient and mobility as defined above can be readily shown (P10) to be related to the material parameters by the following expressions:

$$R_H = \frac{r\ (p\mu_p^{\ 2} - n\mu_n^{\ 2})}{q\ (p\mu_p + n\mu_n)^2}$$

and $$\mu_H = \frac{r\,(p\mu_p^2 - n\mu_n^2)}{(p\mu_p + n\mu_n)}$$

These are the simplified relationships in the case where $\mu_n B \ll 1$ and the surface recombination velocity is large (L7).

The Hall factor r, with a value generally between 0.5 and 2, is a function of the band structure, the carrier statistics applicable and the scattering mechanisms operative (p.117 of S19). In the absence of more precise information we shall take r = 1.

For a one carrier system these expressions reduce to the more simple form of

$$R_H = -\frac{r}{nq} \quad \text{and} \quad \mu_H = -r\mu_n$$

for $n\mu_n \gg p\mu_p$

and $$R_H = \frac{r}{pq} \quad \text{and} \quad \mu_H = r\mu_p$$

for $p\mu_p \gg n\mu_n$

5.4 High Frequency Capacitance Measurement

The high frequency MIS differential capacitance method was applied initially to the thermally oxidized Si system (T6).

For this surface, because of its low density of surface states, it was possible to measure the high frequency capacitance versus voltage curve by standard bridge techniques. The bias in this case being applied in steps, at each of which the capacitance was measured.

Although perfectly adequate for the Si system the method proved in practice to be rather time consuming and so, to decrease the time required, Schlickman (S14) in 1966 proposed a method whereby the capacitance was measured as a continually varying function of bias. This method, although

inherently simple, suffered from limitations both in frequency of measurement possible and in accuracy.

Following this Schewchun and Waxman (S15) proposed a much refined method which measured dynamically both the differential capacitance and conductance variation with bias. This technique however required the use of elaborate and expensive instrumentation.

More recently Zaininger (Z3) presented a technique employing relatively simple circuitry which would enable plots of capacitance versus bias to be made dynamically up to a measuring frequency of ~ 1 Mc/s.

These techniques were developed to speed up the measurement of capacitance versus bias on Si surfaces. In the present study, although the fast state density is reasonably small, there is a very large density of slow states; and in an attempt to measure the C/V variation by means of a stepped gate bias these slow states were observed effectively to pin the surface to the quiescent value of surface potential, all induced charge relaxing in a matter of a few seconds into the traps in the insulator. (cf. the final paragraph of chapter IV).

For this reason, rather than the desirability of a short measuring time, a dynamic measuring technique was employed. For bias sweep frequencies greater than a few cycles/sec. all slow states were observed to be effectively eliminated, the surface potential swing being limited only by the fast state distribution.

5.4.1 Method of Measurement

The measuring circuit, shown in detail in appendix B, is based on that of Zaininger. It varies from his in that the larger values of capacitance encountered in the present work can be measured and, because of the much

smaller variations in C_t to be expected in the case of PbTe and InSb (see section 4.4.1), a simpler detector is possible.

The basic measuring circuit is shown in figure (28a) together with a photograph of the experimental apparatus in figure (29).

Neglecting for the moment the biasing circuit and C_2, for

$$R \gg \frac{1}{w\, C_t} \gg \frac{1}{w\, C_1}$$

$$v_x \propto \frac{1}{v_{in}\, C_t} \tag{30}$$

C_t is the capacitance of the MIS device and is assumed to dominate the impedance of the structure.

As has been shown by Zaininger (Z4), this assumption that the device reactance and impedance are equal results in an error given by

$$\frac{\Delta C_t}{C_t} = (\tan^2 \delta + 1)^{\frac{1}{2}} - 1 \tag{31}$$

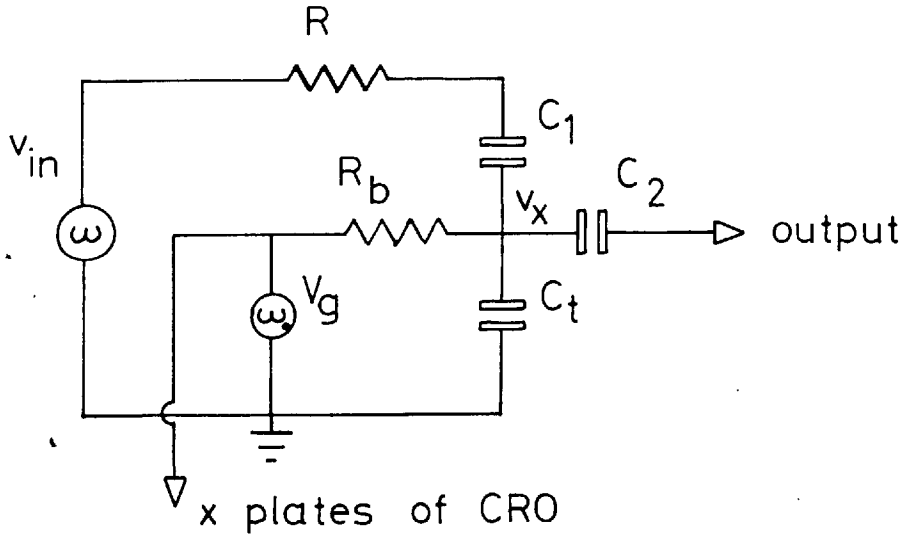
A loss tangent of 30% results in an error of $< 5\%$. In practice, with a good dielectric, this loss tangent is invariably dominated at high frequency by series resistance and in the present study has been reduced to such a level that $\tan \delta$ is usually $< 15\%$ at 1 Mc/s.

The bias is applied at a frequency w_o via a blocking resistor R_b which is chosen so that

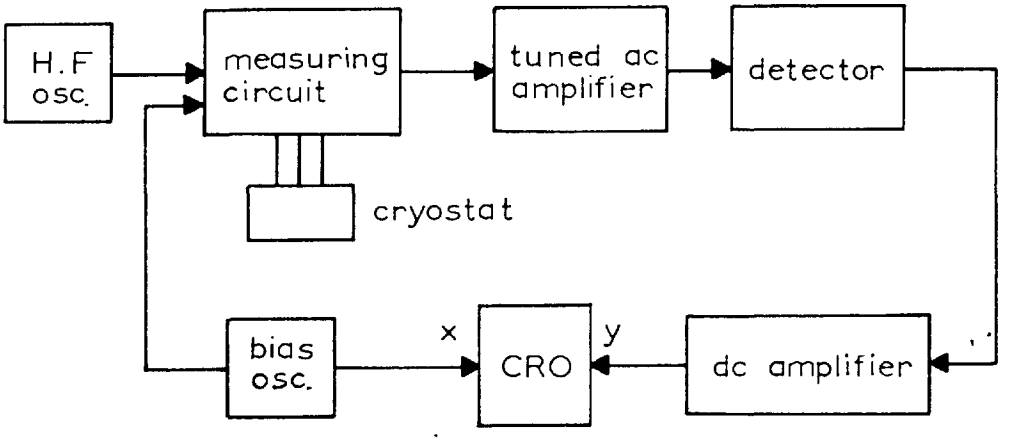
$$\frac{1}{w\, C_t} \ll R_b \ll \left[\frac{1}{w_o C_t} \text{ and } (R + \frac{1}{w_o C_1})\right]$$

This ensures that the high frequency circuit is not loaded by the bias network and that the bias voltage appears entirely across the capacitor.

Figure 28

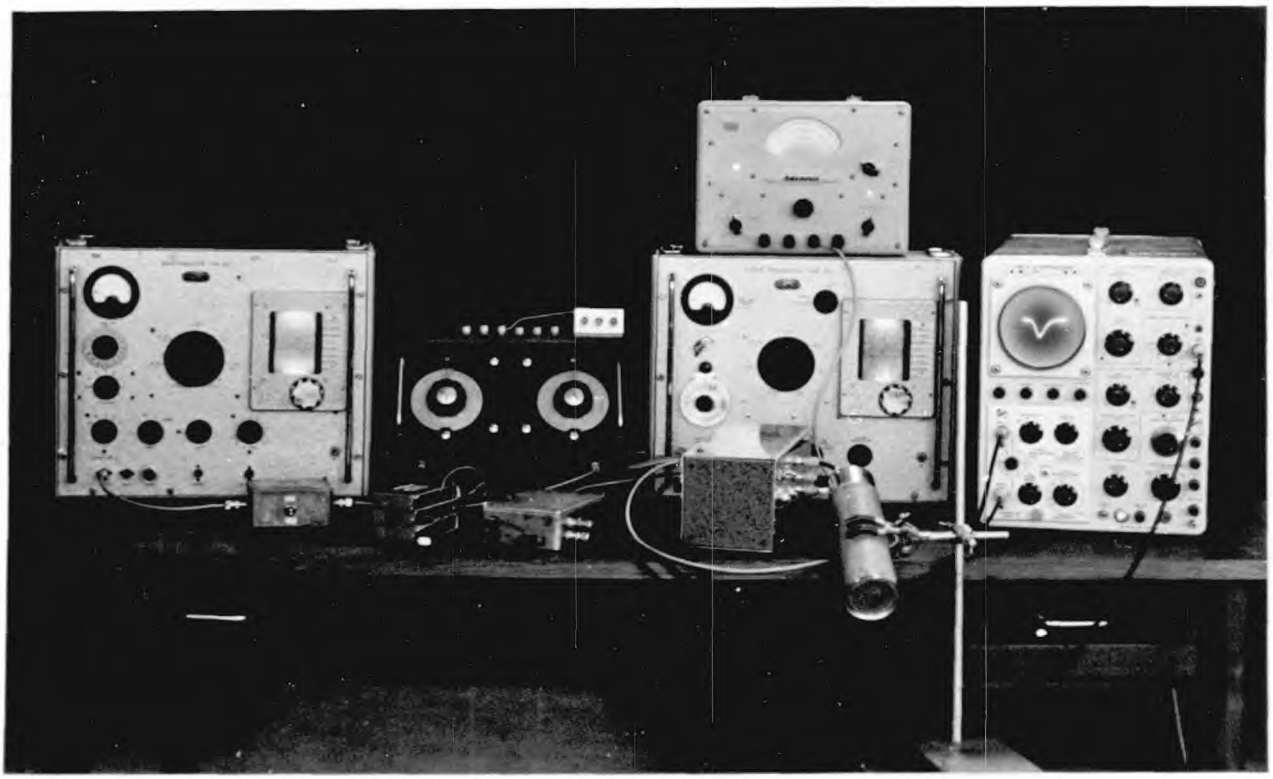


(a) The basic capacitance measuring circuit



(b) Schematic of the dynamic differential capacitance measuring system

Figure 29



The differential capacitance and field effect measuring apparatus displaying the MIS differential capacitance of InSb at 1 Mc/s and 77 °K

Moreover the input impedance to the first amplification stage Z_{in} is chosen large compared with $^{1}/wC_t$ to prevent an additional path for circuit loading.

The capacitor C_2, chosen so as not to attenuate the high frequency signal significantly is included to block off the bias signal at the frequency w_o i.e.

$$\frac{1}{w_o C_2} \gg Z_{in}\Big|_{w_o} \tag{32}$$

Because it is the differential capacitance we are interested in, v_x must be much smaller than the bias voltage V_g, typically 1/100 th. of it. This means that, in the absence of C_2, the high frequency signal containing the required information through equation (30) would be swamped by the low frequency bias signal. Tuning of the first amplification stage is provided to improve further this situation but an upper frequency limit of ~ 100 c/s is set on w_o as a result of the breakdown of inequality (32) at higher frequencies.

The output voltage v_x is amplitude modulated in C_t^{-1} and is typically set at ~ 40 mV peak to peak. As is shown schematically in figure (28b), this voltage is initially amplified by an ac coupled and tuned first stage and passed at ~ 2V peak to peak to a detector and dc amplifier. The output is displayed on a Tektronix oscilloscope type 545A via a differential input; the horizontal deflection of this being driven from the bias oscillator.

The display, of C_t^{-1} versus V_g, is photographed and inverted to give C_t versus V_g in the following way:

The circuit is calibrated by inserting in parallel with C_t a standard capacitor of known value and noting the display deflection at zero V_g.

If ΔV corresponds to this deflection and ΔC is the capacitance

change, then from equation (30)

$$\Delta V \propto \left[\frac{1}{C_o + \Delta C} - \frac{1}{C_o}\right]$$

i.e. $$\Delta V \propto \frac{\Delta C}{C_o(C_o + \Delta C)} \qquad (33)$$

where C_o is the capacitance value at zero V_g as measured at the same frequency and temperature on a bridge.*

If A is the constant of proportionality in equation (33) then

$$A = C_o \frac{\Delta V}{\Delta C} (C_o + \Delta C) \qquad (34)$$

and can be evaluated in terms of ΔV and ΔC corresponding to the standard capacitor.

Then for any other value of ΔV as measured off the oscilloscope display photograph the corresponding value of ΔC_t and hence C_t can be calculated using (33), i.e.

$$C_t = \frac{C_o^2 \Delta V}{A - C_o \Delta V} \qquad (35)$$

As has been described in chapter IV, the frequency of measurement w must be large enough to eliminate the fast surface states. The upper frequency limit on the circuit employed here is ~ 5 Mc/s. and at this frequency all states with relaxation times $\geq$ 50 nanosec. are inoperative. It is of course not possible to say anything about states with relaxation times less than this because they are beyond the resolution of the system but from previously reported work on the lead salts (Z5, P9) and InSb (D4, C4) it appears that at 1 Mc/s at least one set of fast states has been eliminated.

---

* Wayne Kerr bridge type B601 using a Wayne Kerr radio frequency oscillator type 201 and detector type 853

The effect of states remaining in equilibrium is to increase the measured value of $C_{sc}\dagger_{min}$ above its true value leading to an overestimate of the doping density. Moreover some distortion of the measured surface state density near the minimum will occur but as has been shown by Heiman and Warfield (H10) this error should not be too large for all reasonable values of surface state density.

Over the frequency range of 100 Kc/s to 5 Mc/s, as covered in the present work, no appreciable difference in the C_t/V_g curve has been observed and as a result of this all measurements have been carried out at ~ 1 Mc/s.

The devices were also maintained at ~ 77°K during the measurements both to increase the time constant of the surface states and also to increase the measured capacitance change as a result of the decreased surface state density at the lower temperature.

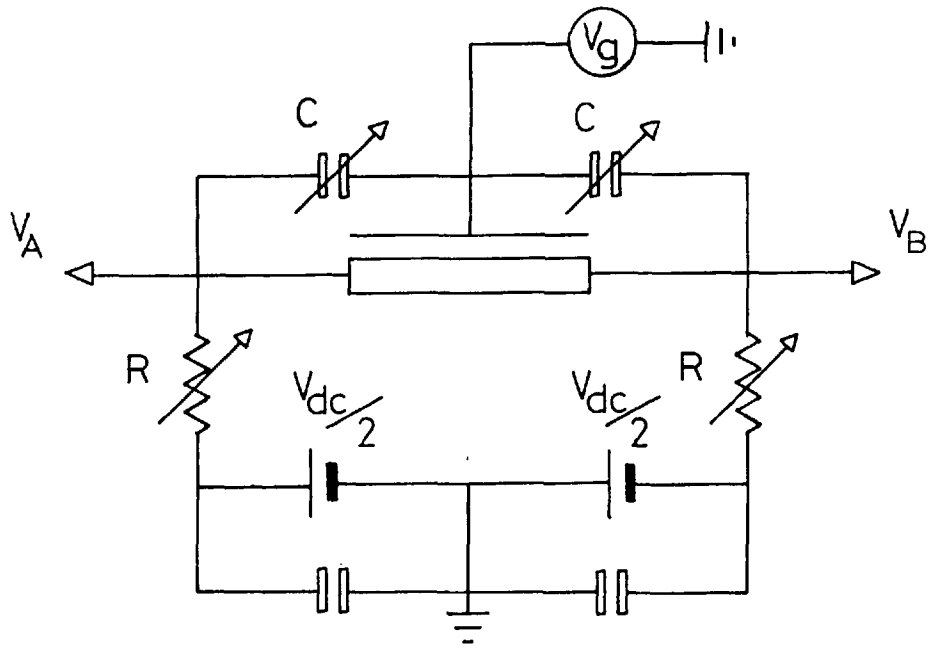
At 1 Mc/s the space charge has also been observed to remain in equilibrium in inversion, satisfying the second requirement of inequality (23) and indicating a minority carrier lifetime in these films of < 100 nanosec. At this frequency therefore the equilibrium analysis of appendix A is valid over the entire range of surface potential investigated.

5.5 Conductance Measurement

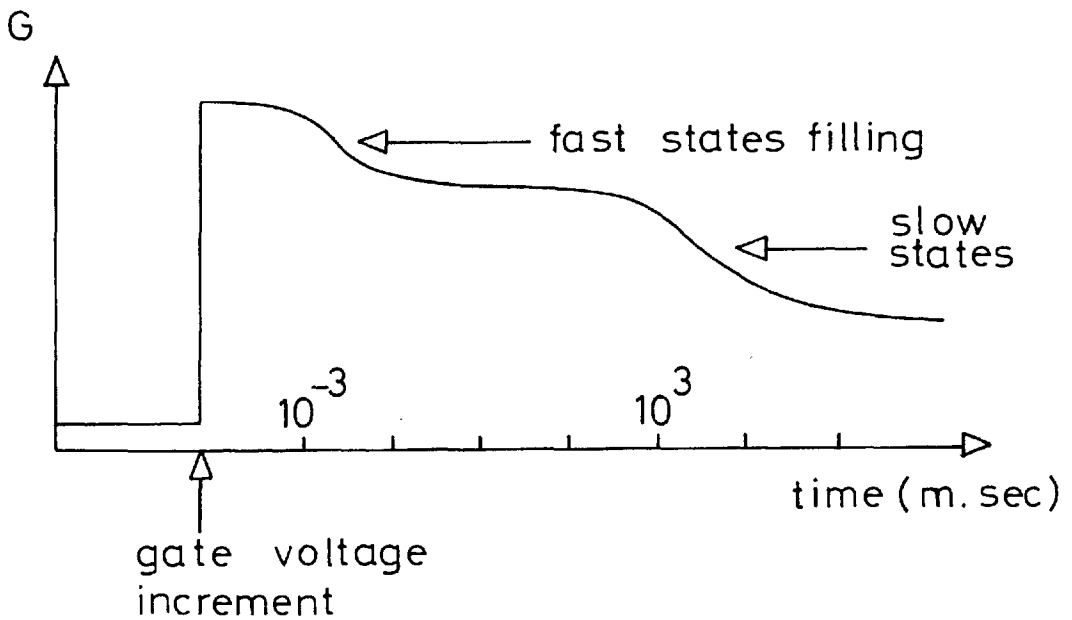
The way in which the semiconductor conductance varies with gate bias was measured in the present study by means of the simple bridge network depicted schematically in figure (30a).

The voltage V_{AB} is displayed on a Tektronix oscilloscope via a high gain differential input, the capacitive charging current being initially balanced out by means of the resistors R and capacitors C with $V_{dc} = 0$.

Figure 30



(a) Bridge circuit for measuring the field-effect



(b) A typical dc field-effect curve

On application of V_{dc} the variation of V_{AB} is then solely a function of G, the conductance of the sample, and for $2R \gg G$ is given by

$$\Delta V_{AB} = \frac{V_{dc}}{2R}\left[\frac{1}{G_o + \Delta G} - \frac{1}{G_o}\right]$$

where G_o is the zero V_g value of semiconductor conductance.

For $\Delta G \ll G_o$ this reduces to the simple relationship:

$$\Delta V_{AB} = -\frac{V_{dc}\Delta G}{2 R G_o^2} \qquad (36)$$

Knowing V_{dc}, R and G_o therefore enables the G/V_g variation to be plotted from the $\Delta V_{AB}/V_g$ display.

To ensure that the surface potential is approximately constant along the whole length of the sample, so that we have essentially a one dimensional problem, it is necessary to chose V_{AB} small with respect to V_g.

This method of measurement enables the conductance versus gate voltage variation to be obtained from dc to greater than 50 Kc/s if care is taken with the setting up of the circuit. The measurement at dc involves applying a step voltage to the gate and observing the way in which the semiconductor conductance varies with time. As the initially induced charge relaxes from the semiconductor surface into trapping levels the initial conductance change is observed to decrease. The ideal form of this is as depicted in figure (30b) where it is assumed that the resolution is good enough (20 μ sec. for a 50 Kc/s frequency limit) to enable the filling of the fast states to be observed in addition to the more easily detected slow states.

CHAPTER SIX

EXPERIMENTAL RESULTS

6.1 Film Structure

Materials evaporated onto amorphous surfaces generally grow in a disordered fashion. For low substrate temperatures during deposition a practically amorphous structure generally results where all long range order for distances greater than ~ 100 Å is lost. For higher substrate temperatures a polycrystalline structure forms where over regions usually > 1000 Å crystal order is maintained. The crystallites do not however normally orientate themselves with respect to their neighbours.

The way in which such a polycrystalline layer grows is shown in the electron micrograph* sequence (31a) to (e) for a film of PbTe evaporated onto a glass substrate at ~ 150° C. The initially formed nucleii with a density ~ 4×10^{11} cms^{-2}, residing in low energy sites on the substrate, grow by material addition from the vapour stream until they are large enough to touch. At this point coalescence occurs with some of the crystallites increasing in size at the expense of others. This process continues until, at an average thickness of ~ 450 Å, a continuous film results. This final stage is shown in figure (31f). This process is typical of most materials and is similar at all temperatures of deposition. For PbTe at low temperatures the crystallites have a final diameter of ~ 100 Å whereas at the highest temperatures of deposition their average size may be greater than 1500 Å.

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* A JEM 7 electron microscope was used for the microscopy on these films. Specimens were removed from the glass substrates by exposing them to hydrofluoric acid vapour and then floating them off onto a water surface, from which they could be readily mounted on copper microscope grids. For the nucleation studies carbon replication and platinum shadowing were employed to improve contrast and structural rigidity.

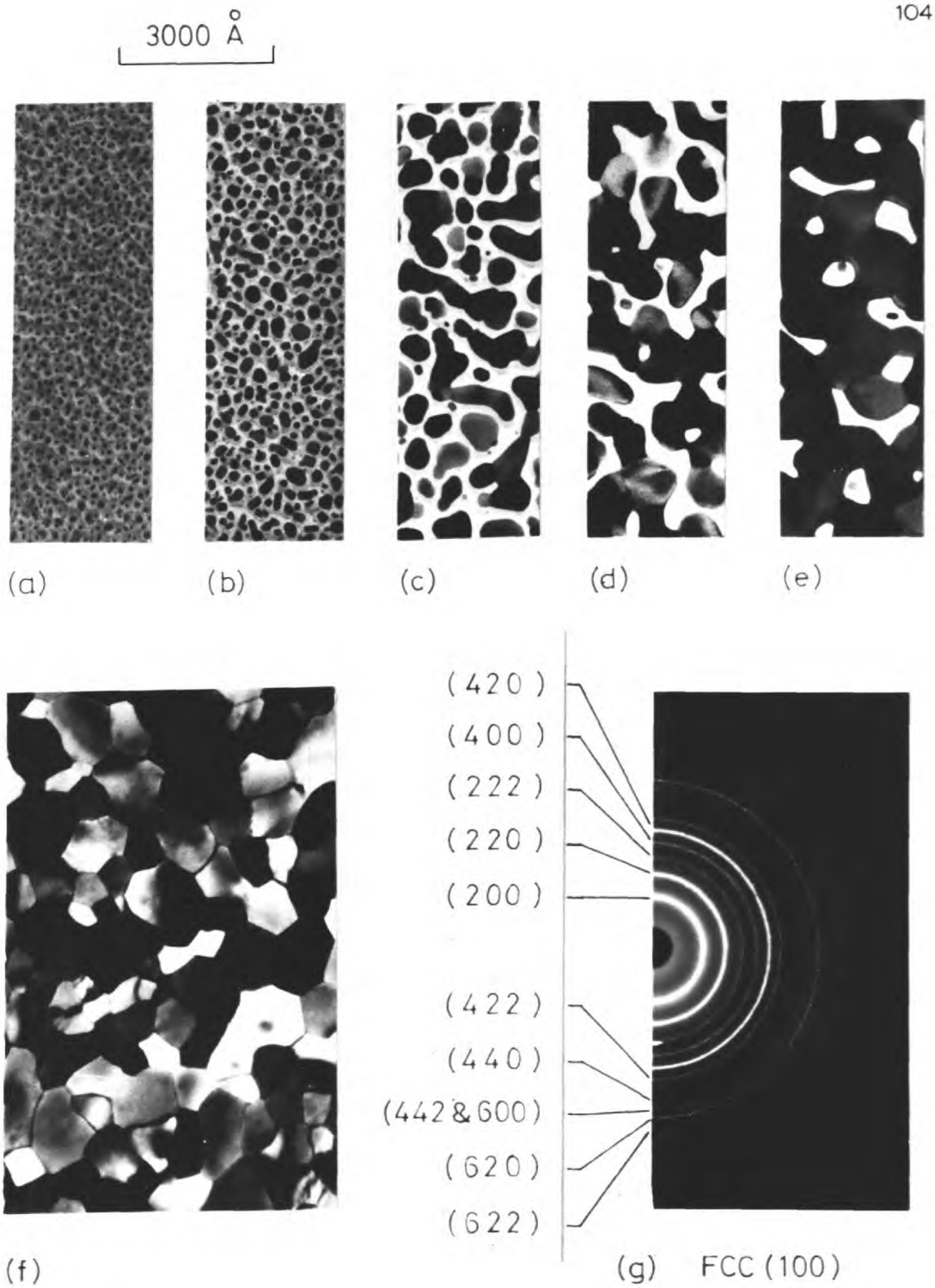

Figure 31
Growth sequence and structure of PbTe on glass

Selected area electron diffraction on such a layer will lead to a diffraction pattern as shown in figure (31g). This particular pattern is for PbTe and is essentially the same for all temperatures of growth. It can be seen that about an axis normal to the film there is no detectable preferential direction of orientation whereas the pattern does show that the film grows with each grain presenting a (100) crystal plane parallel to the surface of the substrate. At the very highest temperatures of deposition (~ 450° C) the diffraction pattern does include additional rings to those of the (100) system but these are always relatively weak in intensity. By calibrating the diffraction camera against an Al film the lattice constant of the evaporated PbTe layers was measured to be ~ 6.3 Å, which is in agreement with values reported for bulk material (A7).

Although each grain is essentially a single crystal as deduced from selected area electron diffraction on single grains, it does contain a large density of defects. In addition, for the film as a whole, each grain boundary consists of a two dimensional array of dislocation lines (M7) corresponding to the crystal mismatch between the individual crystallites. The structure is thus highly disordered and, as will be shown in chapter VII these gross crystal discontinuities can effectively dominate the electrical properties of such layers.

Such disordered polycrystalline growth is always observed on amorphous substrates but subsequent to deposition extensive annealing has been reported to result in a certain degree of ordering with a resulting marked increase in carrier mobility (T1, J2). Because of the desire to employ these films in a transistor structure (section 5.2.3) preparation conditions which are compatible with this have been employed throughout. As a result of this the largest mobilities possible have not been achieved but as will be seen

in section 6.5 reasonable device performance is nevertheless possible.

6.2 Bulk Film Properties

6.2.1 The Dependence on Temperature of Deposition

Evaporated layers of InSb do not change appreciably on exposure to air. They are n-type over large ranges of temperature quite irrespective of their temperature of deposition. As was stated in chapter I, PbTe reacts with oxygen and the manner in which the resistivity of a freshly deposited layer of PbTe varies on exposure to O_2 is shown in figure (32). The influence of dried N_2 and H_2 on the films was also investigated, but these were observed to have practically no effect. This behaviour is observed for all temperatures of growth but is most pronounced at lower temperatures. Measurement of the resistivity and Hall voltage of such films at atmospheric pressure showed them to be of p-type conductivity, which together with the form of the resistivity versus time curve of figure (32) results in the conclusion that, as first deposited, at least a part of the films must be n-type. This type of behaviour is not new and has been observed previously in all of the lead salts (H9, B6, P12).

If the semiconductor is covered with an evaporated layer of SiO_x prior to the admission of O_2 then the effect of the oxygen is reduced. This can be concluded from the curves of figure (33a) where Hall coefficient is plotted at atmospheric pressure and room temperature for a series of films* evaporated onto substrates ranging in temperature from ~ 22° C to the critical temperature of ~ 450°C (at 5 Å/sec).

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* Except for the transistor work reported in section 6.5 all semiconductor films used in this study were of thicknesses ranging from 1000 to 3000 Å.

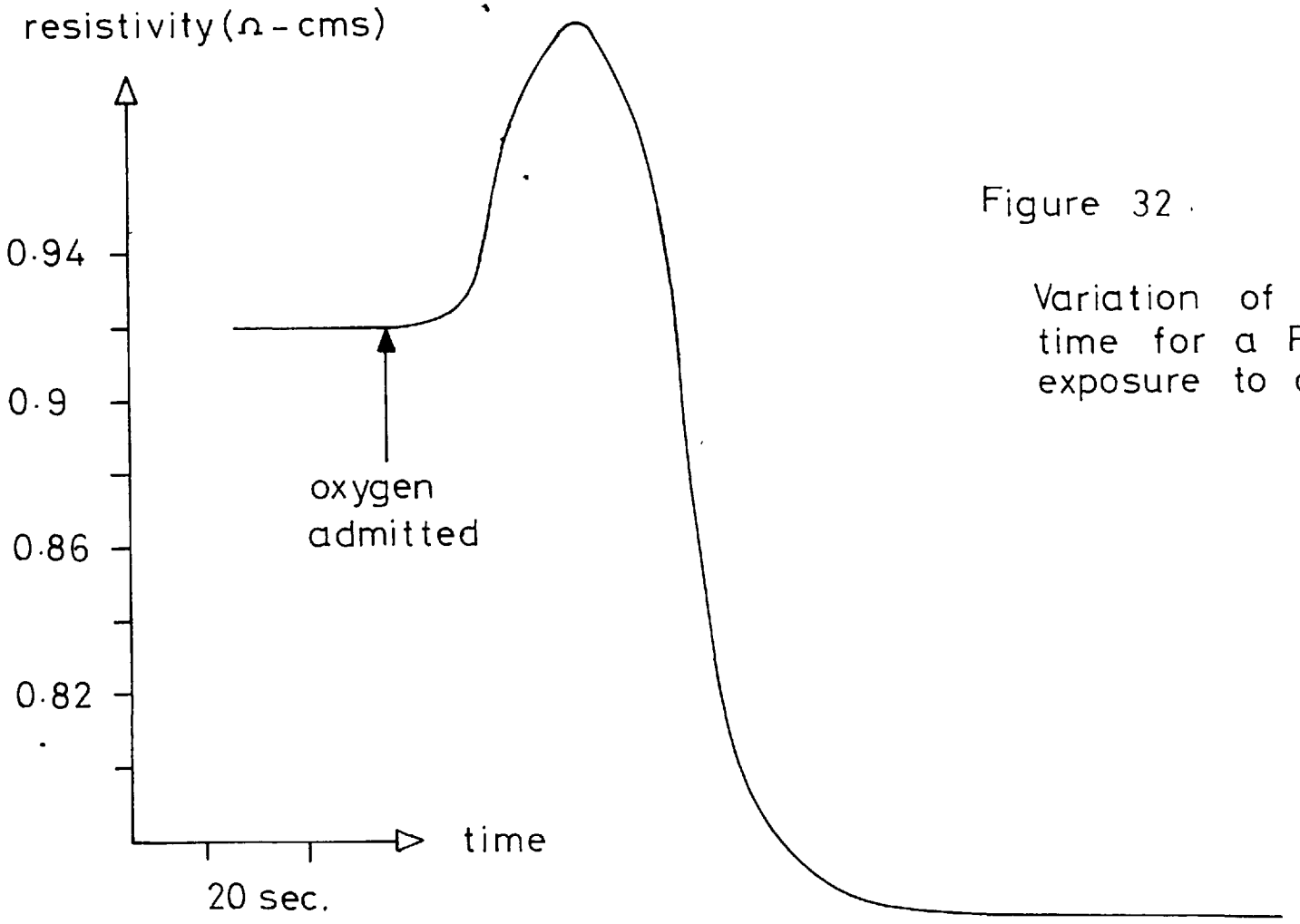
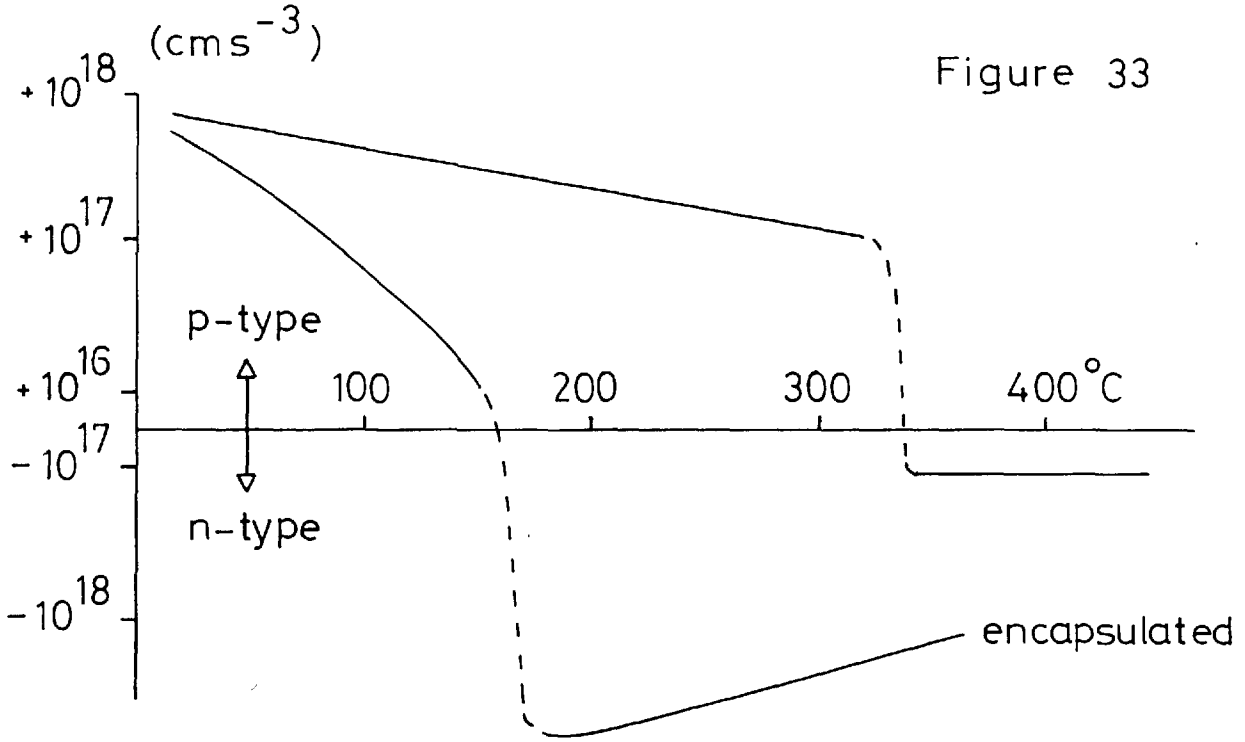


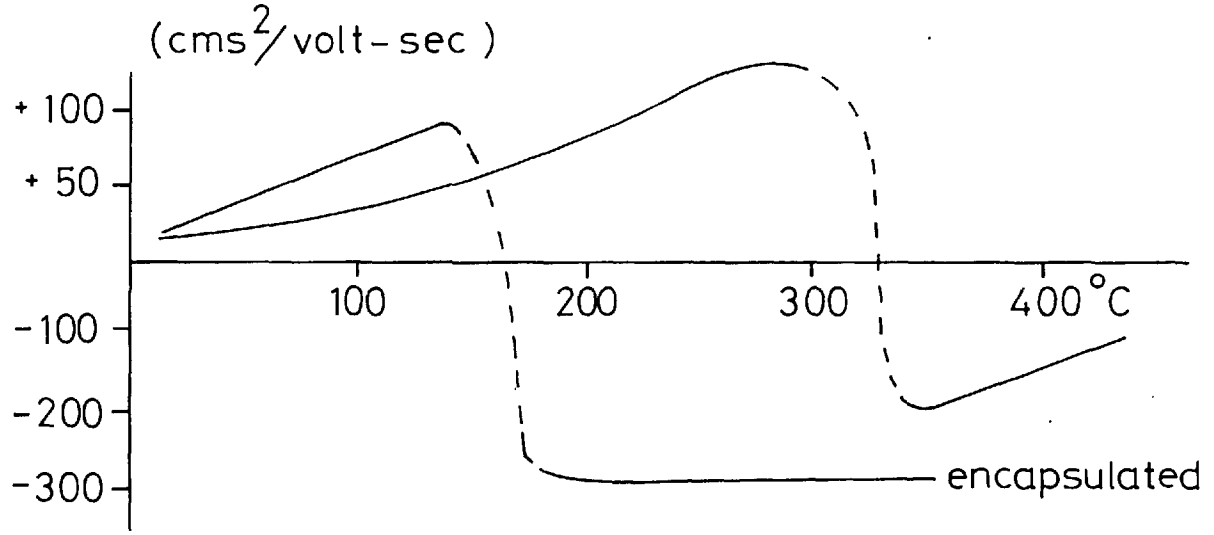
Figure 32.

Variation of resistivity with time for a PbTe film during exposure to oxygen

Figure 33



(a) Variation of $(qR_H)^{-1}$ with deposition temperature for films of PbTe measured at ~300 °K



(b) Variation of Hall mobility with deposition temperature

[These curves are based on the results of measurements on ~50 separate films]

The effect of oxygen is to drive an initially n-type film p-type, the effect of SiO_x being to maintain the film n-type to lower temperatures of deposition. This behaviour of Hall coefficient with temperature is explicable in terms of the following phenomena:

(a) The starting material is p-type (section 5.1) but during the pre-deposition anneal a large amount of the excess Te is driven off. In addition Te, being the more volatile component, will re-evaporate from the substrate during deposition, this being the more pronounced the higher the temperature of the substrate. Both these effects can account for the initially n-type deposit consisted with figure (32), the donor density being an increasing function of growth temperature.

(b) Subsequent oxygen incorporation will drive the film p-type and for a certain temperature of growth this acceptor density will be exactly compensated by the Te deficit of (a). Below this temperature the oxygen acceptors will predominate and the film will be p-type; above it the film will be n-type.

(c) SiO_x encapsulation prior to the admission of oxygen will reduce the acceptor density and therefore move the temperature of deposition corresponding to exact compensation to a lower value.

The way in which the Hall mobility of these layers, again measured at room temperature and atmospheric pressure, varies with temperature of deposition is shown in figure (33b). It can be seen from these curves that the mobility of both holes and electrons in these polycrystalline layers is much below that to be expected for single crystals as discussed in section 1.3.3. The reason for this will be considered in chapter VII.

It was found that by depositing the films of PbTe at a low

temperature and then subjecting them to an anneal essentially the same results were obtained as for films initially deposited at the annealing temperature. Because the latter proved more controllable it was used exclusively throughout the subsequent stages of the work.

6.2.2 The Variation of R_H and μ_H with Temperature

Figure (34) indicates the way in which the Hall coefficient for a number of PbTe films and one typical InSb film varies with temperature. The constant behaviour of R_H for the InSb sample is consistent with a film in which the carrier concentration is degenerate and hence little affected by temperature. The exponential behaviour exhibited by all the PbTe films measured, quite independent of their temperature of deposition, is however rather puzzling. The average activation energy exhibited by these samples is ~ 0.11 eV which is practically one half the band gap of PbTe at $0^{o}K$ (E_g (T = 0) = 0.19 eV from section 1.3.2) and is in fact what would be expected for an intrinsic material. That evaporated and highly disordered films of PbTe could be intrinsic seems rather unlikely. The best bulk samples and epitaxial single crystal films of this material all exhibit (A3, Z6) the constant R_H behaviour to be expected of this highly non-stoichiometric compound and why a more imperfect material should appear more pure is not immediately apparent.

All of the samples of both PbTe and InSb which were studied exhibited a Hall mobility which decreased with decreasing temperature. In many samples, particularly of PbTe, a maximum was in fact observed to occur near room temperature with a subsequent decrease at higher temperatures. The extent of this maximum was more or less pronounced, varying from an almost complete absence in some InSb samples to a very marked form for some of the films of PbTe.

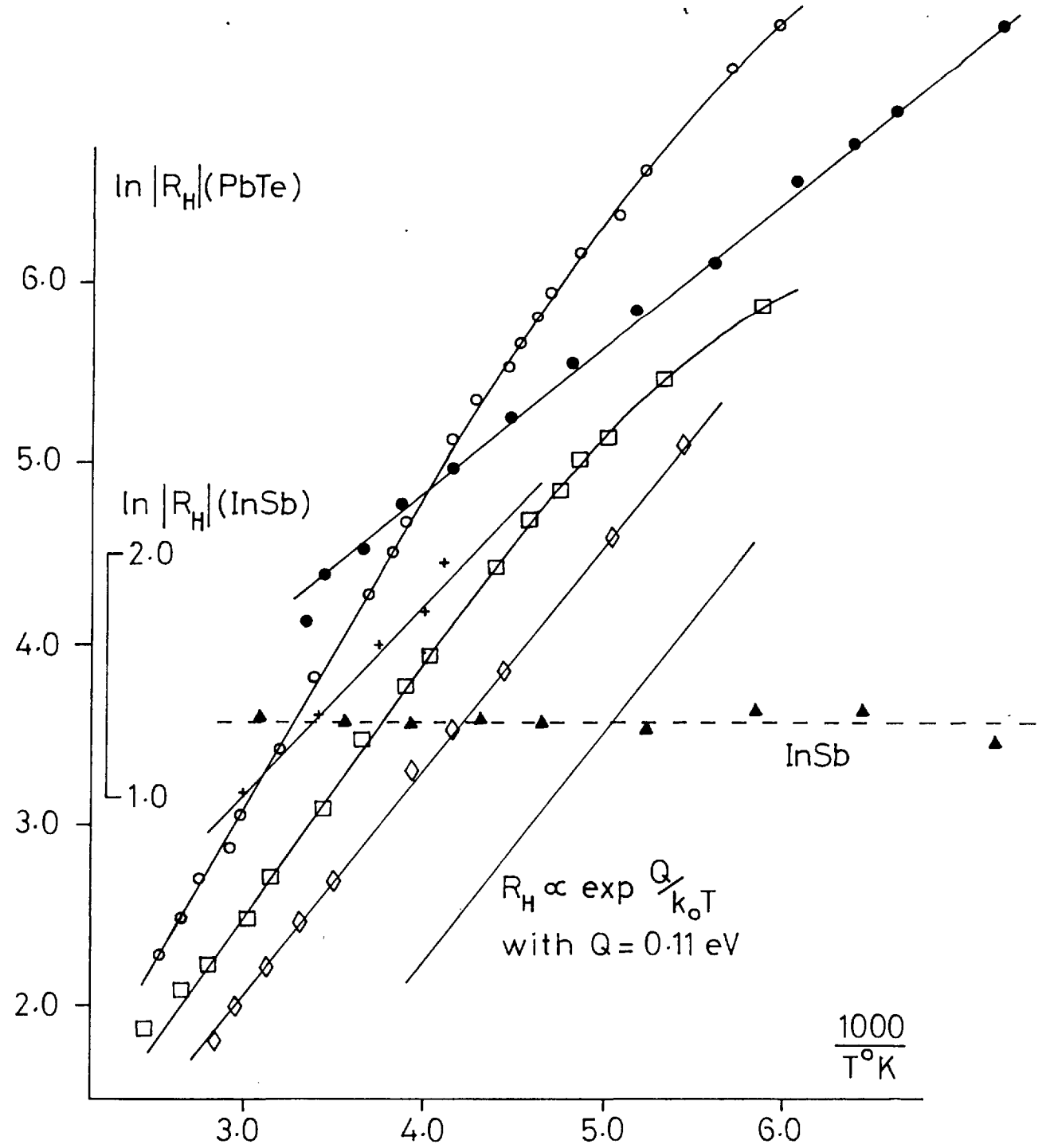


Figure 34

Variation of Hall coefficient with temperature for a number of PbTe samples and one typical film of InSb

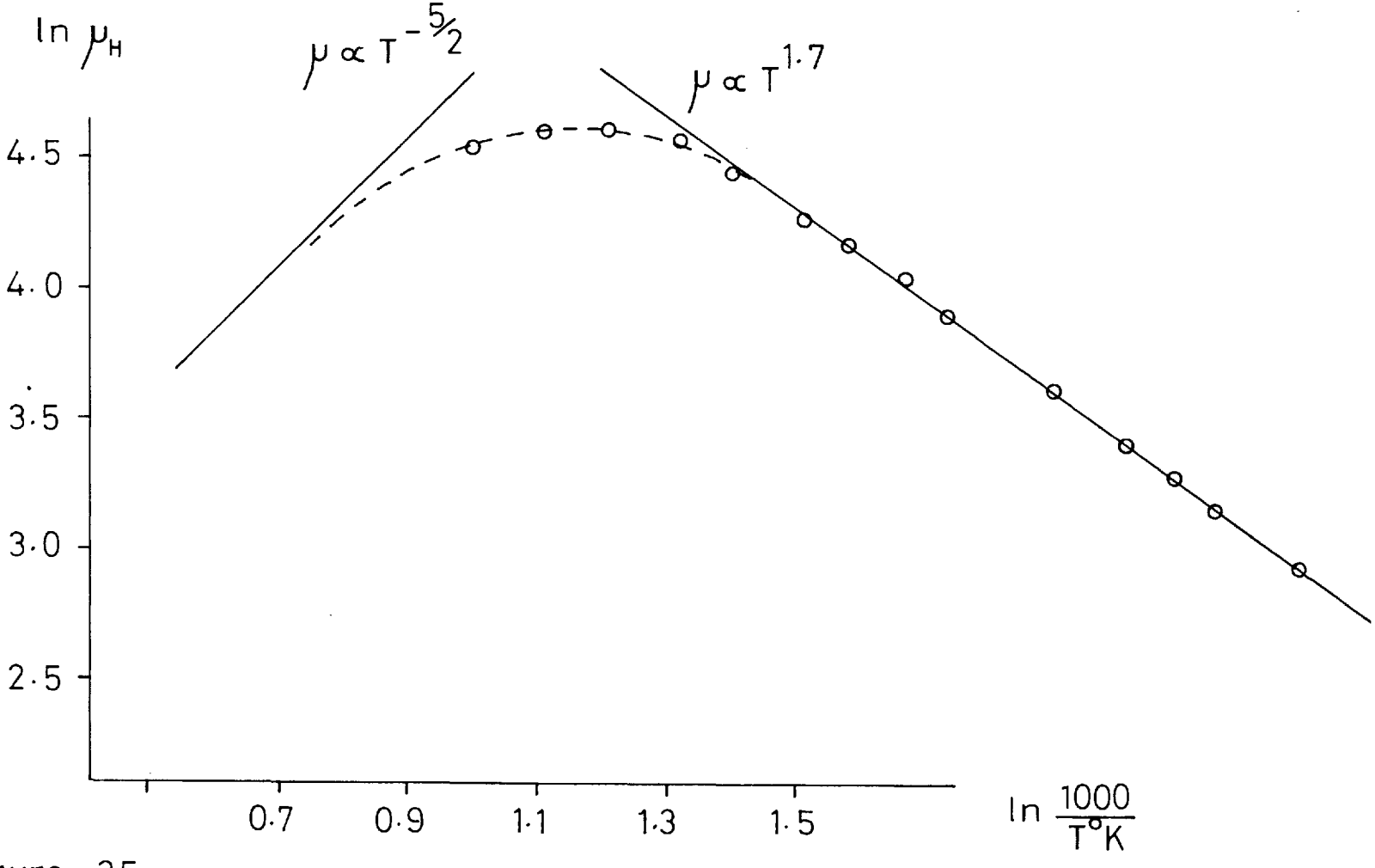


Figure 35

Variation of Hall mobility with temperature for a p-type sample of PbTe

This behaviour for one of the samples of PbTe is shown in figure (35). Here a plot of ln μ_H versus ln $\frac{1000}{T^{\circ}K}$ is shown and it can be seen that below the temperature at the maximum a dependence given by

$$\mu_H \propto T^{1.7}$$

is strictly obeyed. Above room temperature the curve can be extrapolated to fit a $T^{-5/2}$ behaviour, reminiscent of the dependence of μ_H upon temperature in single crystal material.

6.3 The Density and Distribution of Surface States

The oscillographs shown in figure (36) are of the differential surface capacitance versus bias for typical samples of p-type PbTe and n-type InSb. The measurement was made at 1 Mc/s and 77°K using device geometry B of figure (27).

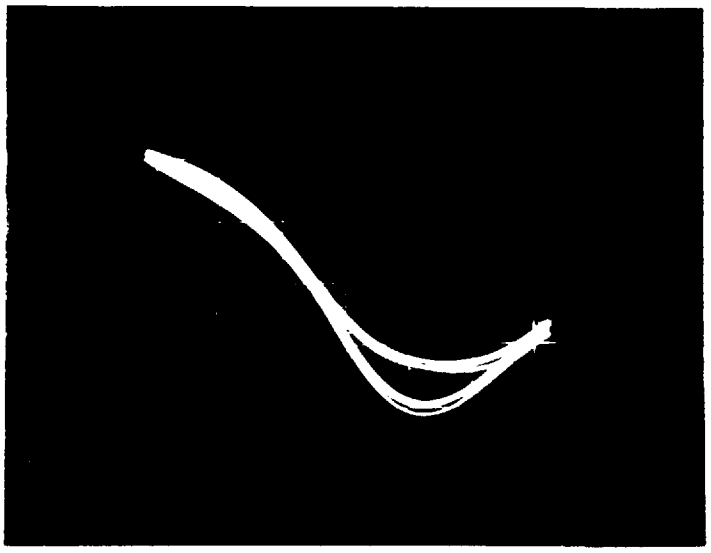
It can be seen that in both cases the inversion layer is following the high frequency measuring signal and that in the case of InSb the asymptote to which C_t tends is fairly clearly defined. These oscillographs are in fact of C_t^{-1} and when redrawn as C_t, in accord with the method of section 5.4.1, are as shown in figures (37) and (38). It can be seen from figure (37) that a large extrapolation is required to determine the asymptotic value of dielectric capacitance to which C_t tends in the case of the PbTe sample.

The overall capacitance change is ~ 10% for the PbTe and ~ 24% for the InSb. Using the value of C_{sc} deduced at the minimum from the relationship

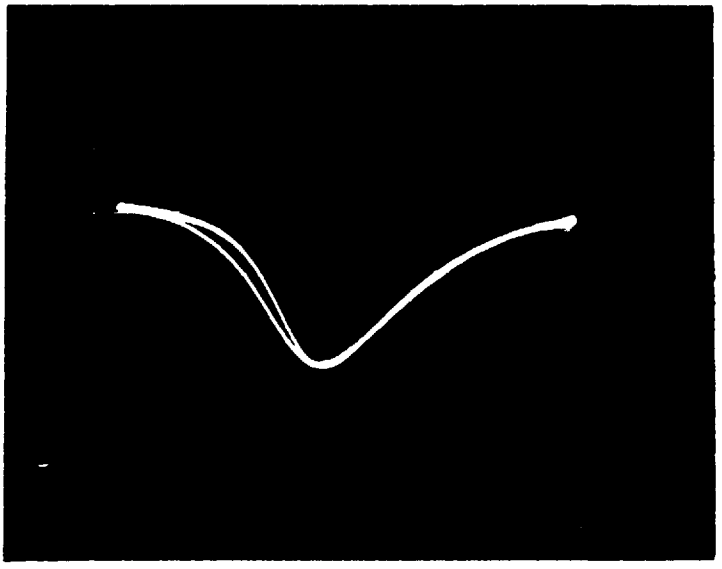
$$C_{sc} = \frac{C_t\, C_{ox}}{C_{ox} - C_t}$$

doping densities of 4×10^{17} cms^{-3} for the PbTe and 5.6×10^{16} cms^{-3} for InSb are determined using the curves of figure (19). This information, together

Figure 36



The variation of differential capacitance with bias for PbTe at 77°K



The variation of differential capacitance with bias for InSb at 77°K

Figure 37

Theoretical and experimental curves of capacitance versus applied charge and bias respectively for PbTe at 77°K

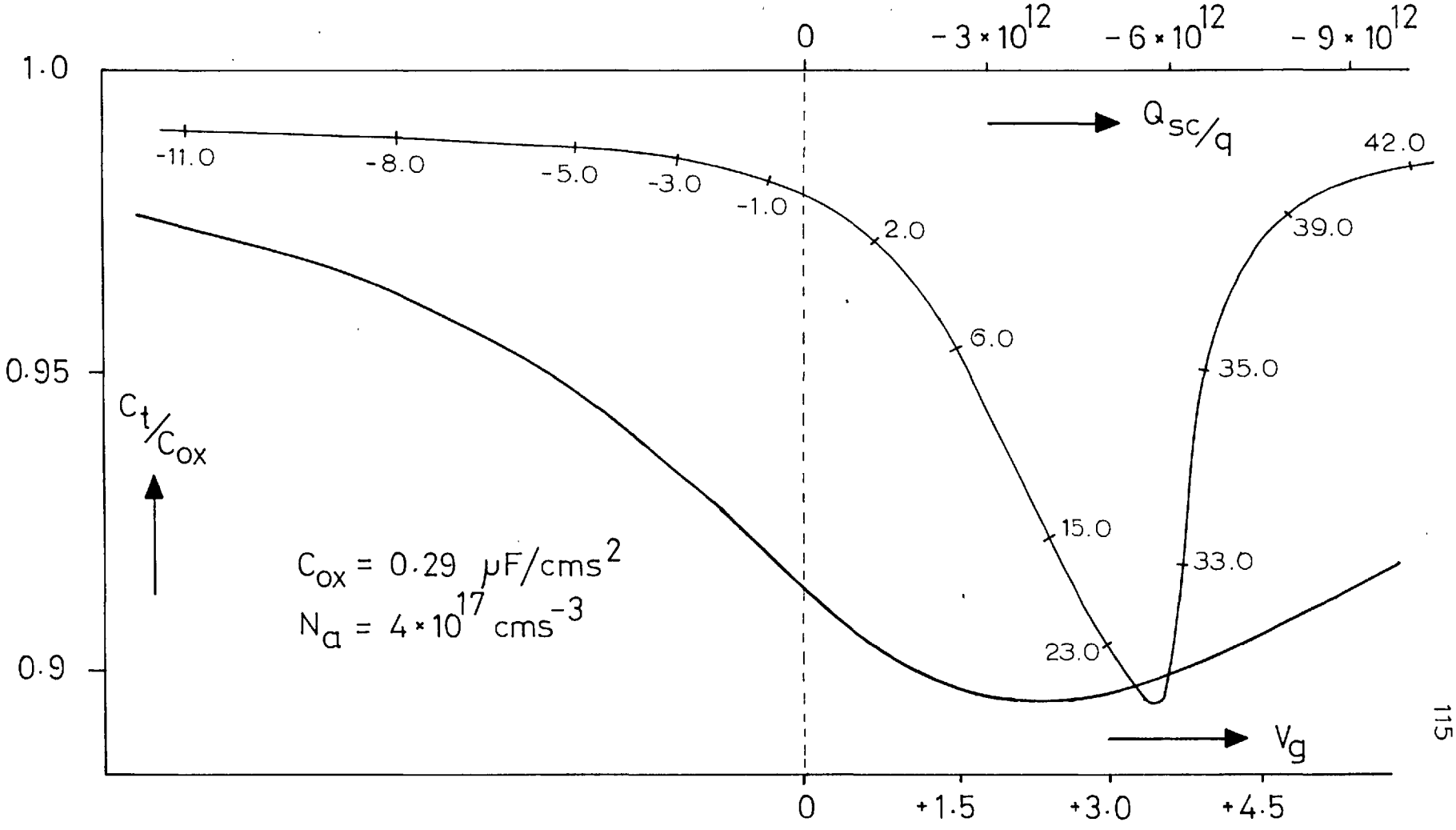
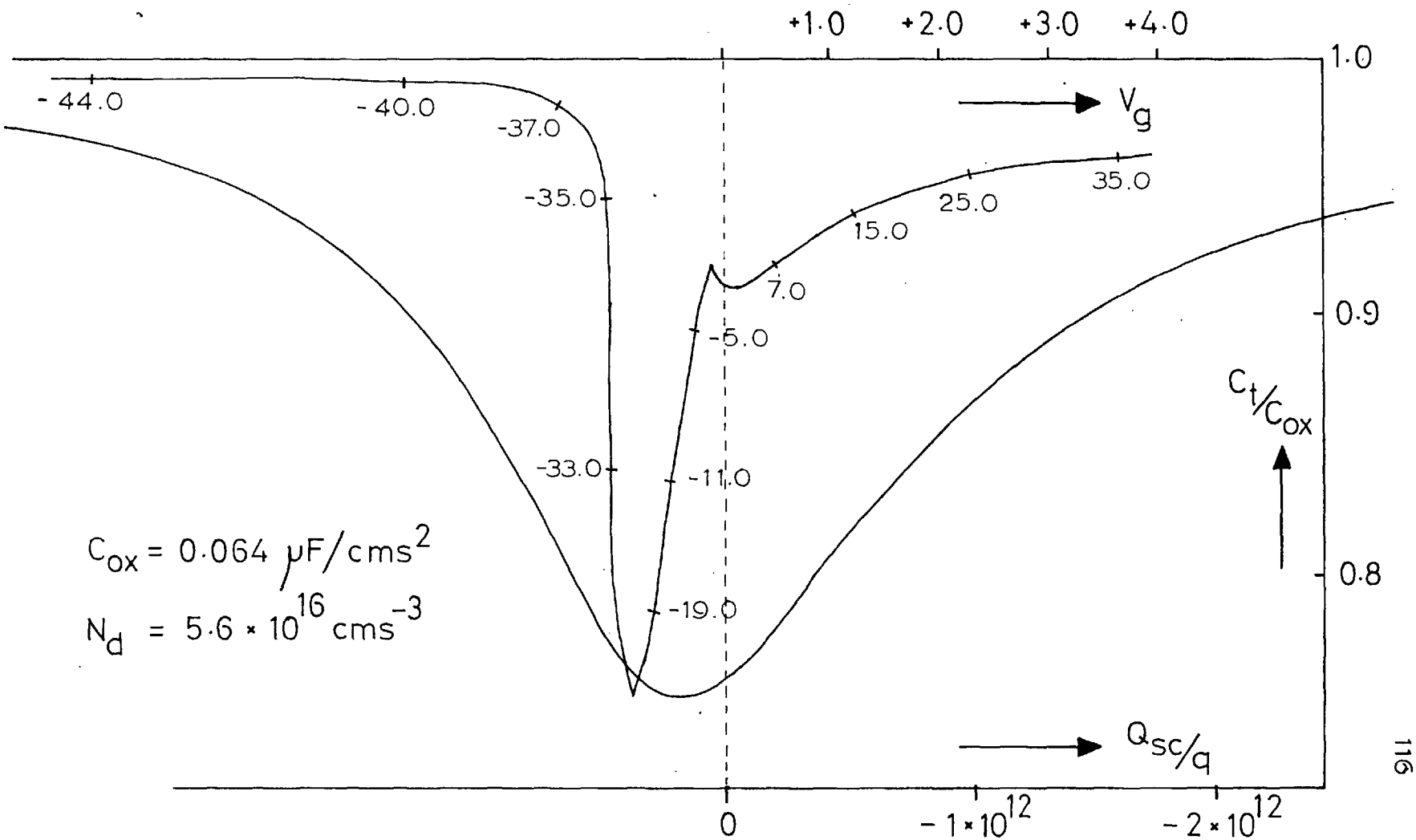


Figure 38

Theoretical and experimental curves of capacitance versus applied charge and bias respectively for InSb at 77°K



with the values of C_{ox}, then enable the theoretical curve to be computed as described in appendix C. These curves are shown in figures (37) and (38) and for InSb the slow rise of capacitance in enhancement for both the experimental and theoretical curves should be noted. This is a result of the low density of electron states in the conduction band of InSb and is some verification of the non-parabolic treatment of appendix A.

Between the theoretical and experimental curves the total net trapped charge as a function of surface potential is calculated as described in section 4.4 leading to the distributions given in figures (39) and (40). The derivative of these curves then leads to the effective surface state distributions of figures (41) and (42). From these it can be seen that for both InSb and PbTe the surface state density increases asympotically to the band edges, being of the order of one order of magnitude larger in the case of PbTe than in InSb.

In both cases it is possible to swing the surface to such an extent that essentially the entire band gap is covered. Moreover, for InSb, because of its low value of electron effective mass and its lower value of surface state density, it is in fact possible to push the Fermi level at the surface well into the conduction band as can be seen from figure (40). In this region the trapped charge settles down to a constant value indicating an absence of surface states beyond the conduction band edge*. Because of this the distribution shown in figure (42) has been confined to that range of surface potential corresponding to the band gap.

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* The peak in Q_{ss} near the conduction band edge is believed to result solely from the inadequacy of the theoretical model in assigning the bulk impurities to a discrete energy level rather than to a more credible impurity band.

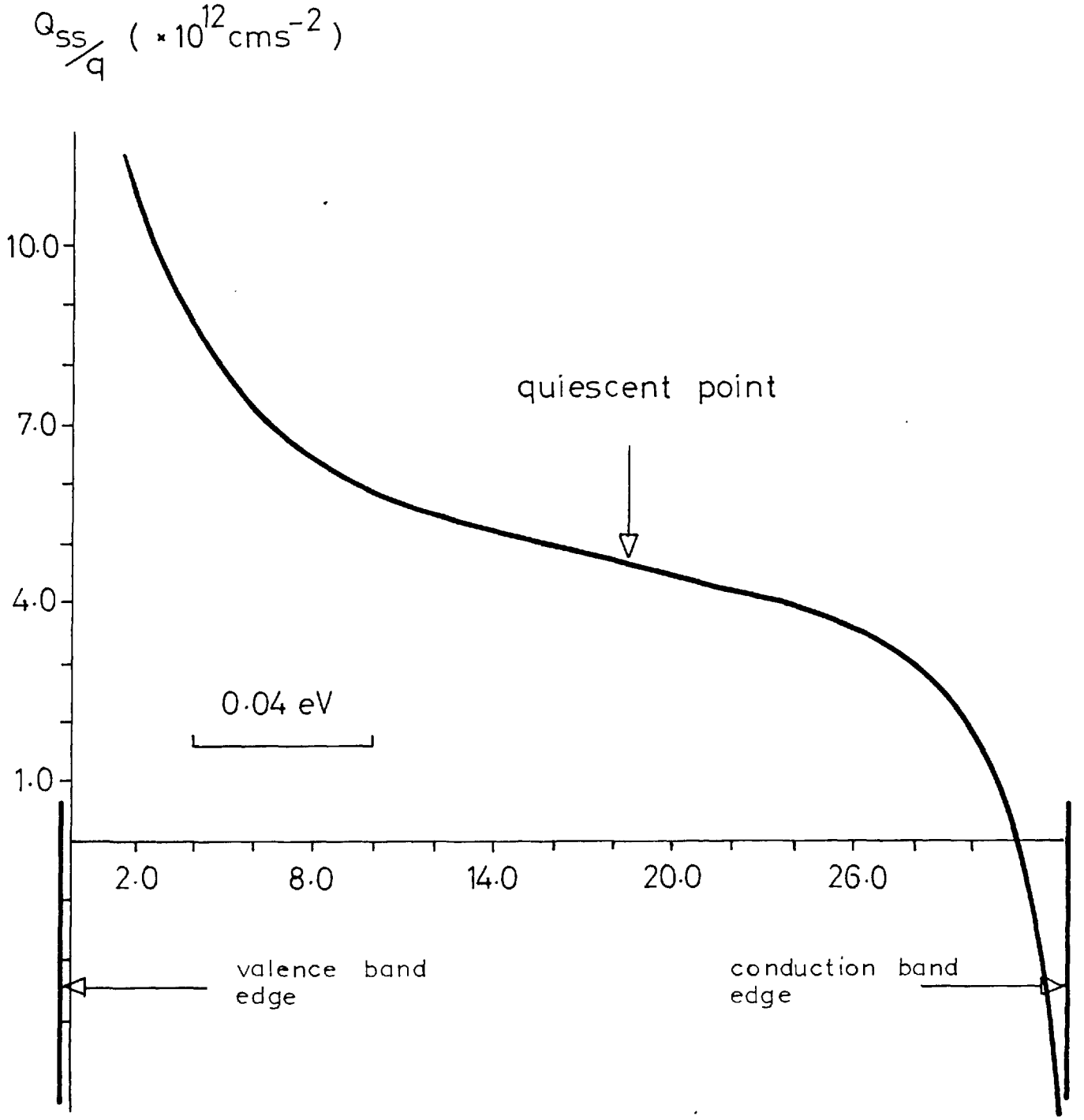


Figure 39

Variation of net total trapped charge with surface potential for PbTe at 77 °K

Figure 40

Variation of total net trapped charge with surface potential for InSb at 77°K.

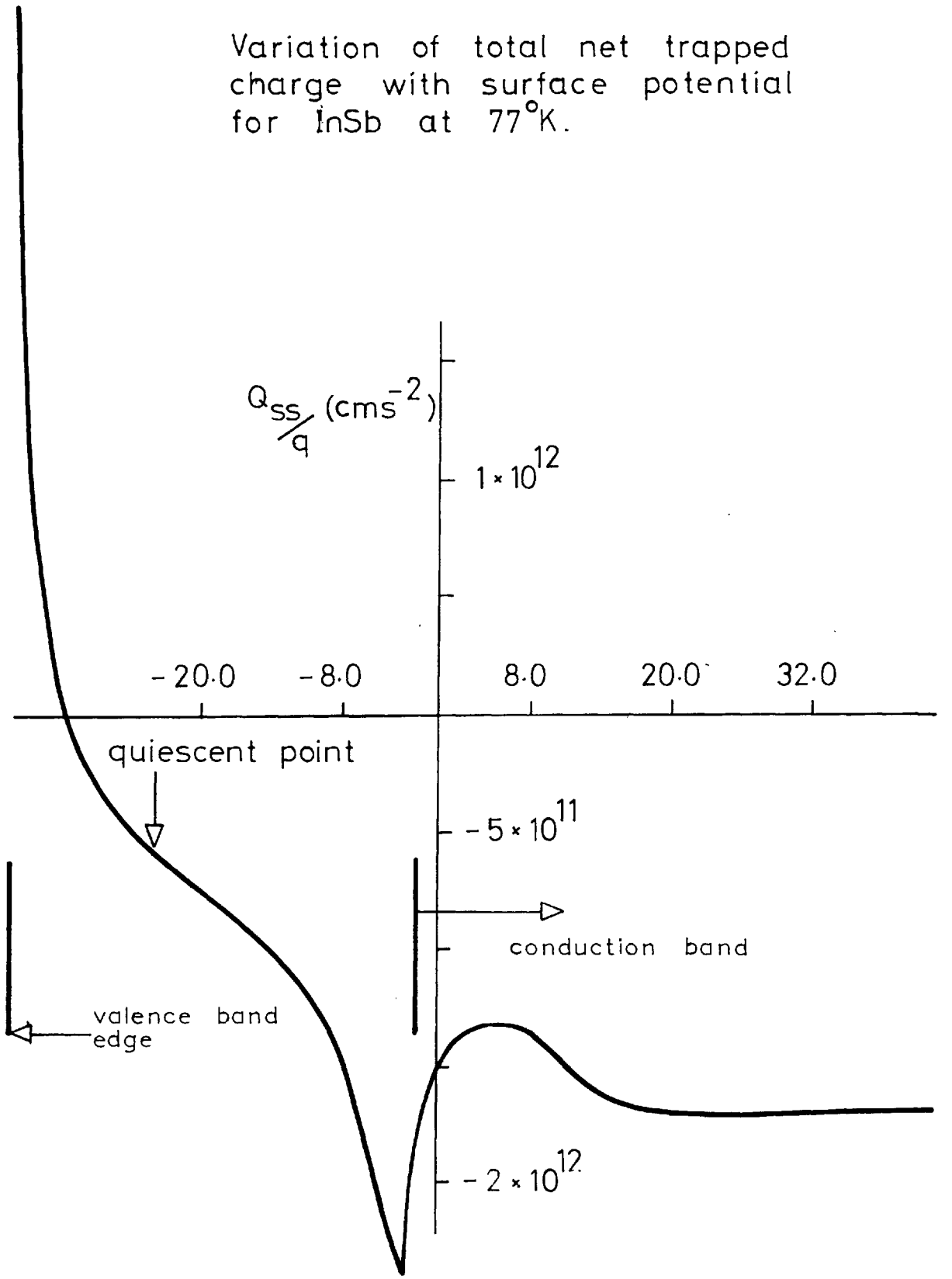
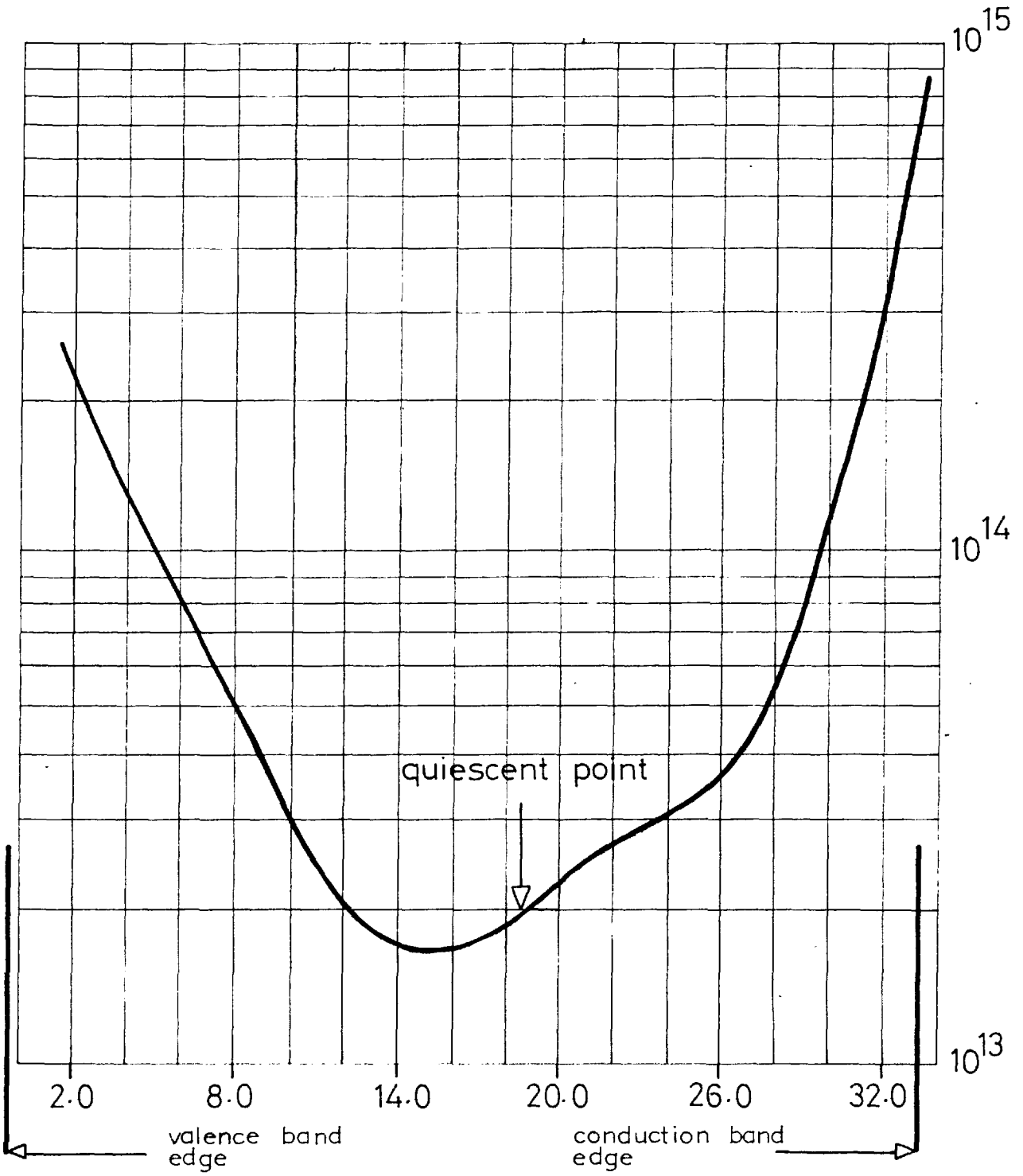


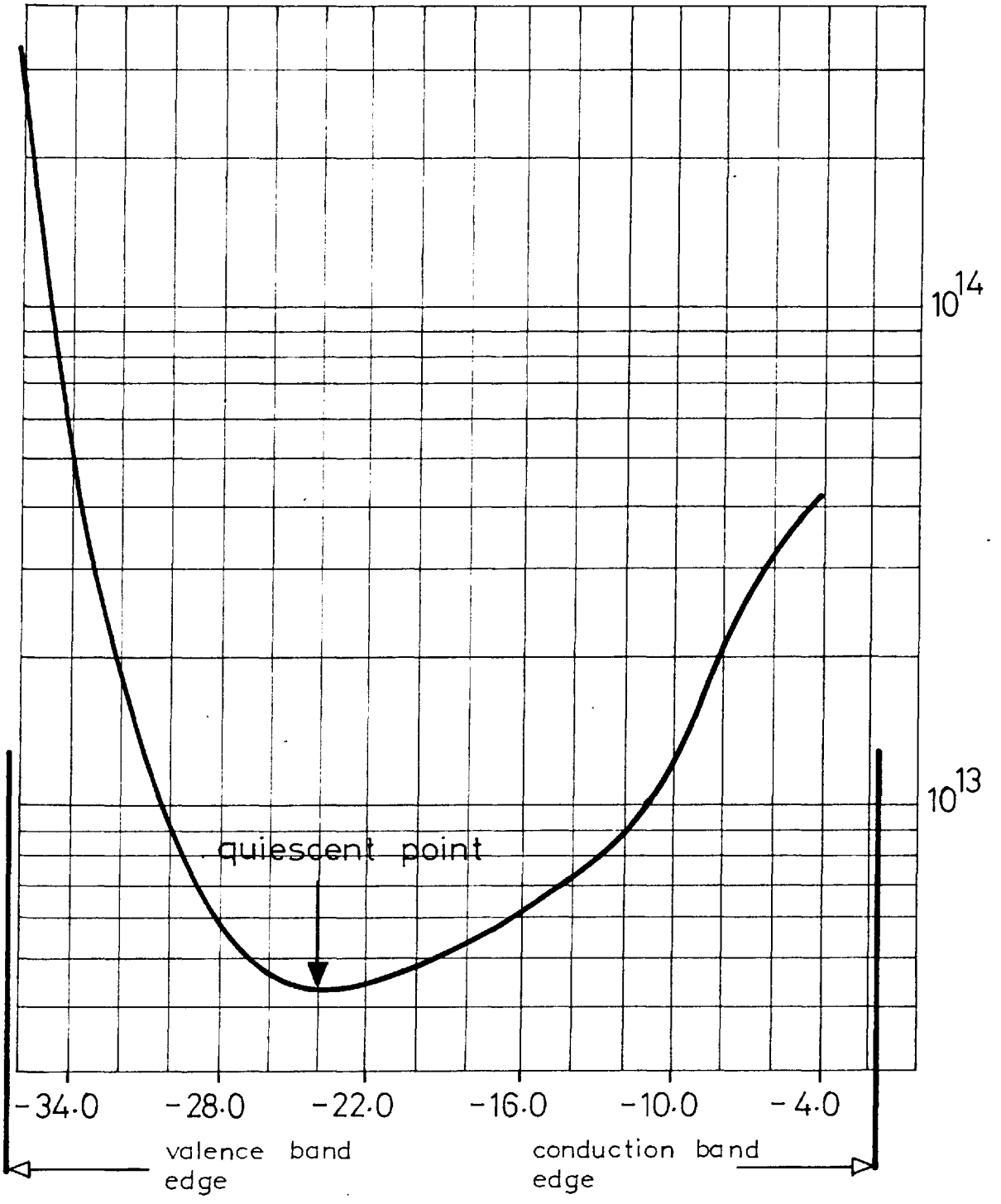
Figure 41



Variation of net effective surface state density with surface potential (in units of k_oT/q) for PbTe at 77°K

N_{ss} is measured in traps/cms^2 - eV

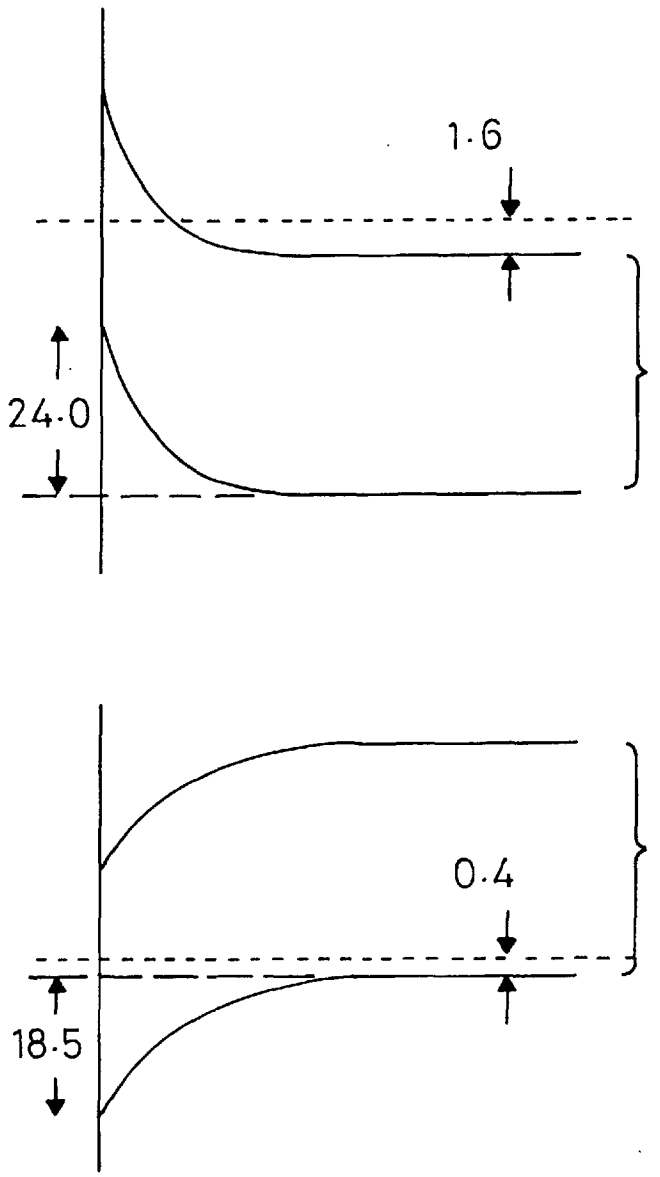
Figure 42



Variation of net effective surface state density with surface potential (in units of k_oT/q) for InSb at 77°K

N_{ss} is measured in traps/cms^2-eV

Figure 43



Quiescent surface condition of InSb and PbTe at 77 °K.

Energy is given in units of k_oT

The quiescent surface condition ($V_g = 0$) corresponds to depletion in both cases with 6×10^{11} trapped charges cms^{-2} on the InSb surface and 4.6×10^{12} cms^{-2} on the surface of the PbTe. This quiescent condition is shown for both materials in figure (43). It can be seen that because of the low value of density of states in the conduction band of InSb the Fermi level in the bulk is actually within the conduction band, indicating the necessity of using degenerate statistics to describe the carrier populations in these materials.

Of prime importance in both cases is the fact that in the absence of an applied external field the Fermi level at the surface passes practically through the center of the band gap. As will be seen in chapter VII this has important consequences particularly in the case of PbTe.

At $300^{o}K$ the change in differential capacitance was observed to be appreciably smaller than that at $77^{o}K$ and in fact it was not possible at this higher temperature to swing the surface potential to a sufficient extent to enable the asymptotic value of capacitance to be determined. Consequently it was not possible to analyse the high temperature state distribution although from the general form of the capacitance curve it is nevertheless possible to qualitatively conclude that :

(i) the quiescent value of surface potential varies little with temperature

and (ii) the surface state density at room temperature is larger than that at $77^{o}K$ in agreement with the results of Rzhanov et. al (R4) on the surface of Ge. A tentative estimate would place its value at $300^{o}K$ at somewhere between two and three times its value at $77^{o}K$.

6.4 Surface Mobility

Using the circuit of figure (30a) a number of conductance versus gate voltage curves have been obtained at liquid nitrogen temperature for samples which have had their surface state densities evaluated as in the previous section. Knowledge of the latter then enables the field effect curve of $\Delta\sigma$ versus V_g to be replotted as $\Delta\sigma$ versus ΔN (or ΔP) leading to values of surface mobility as discussed in section 4.5.

This has not been possible for films of PbTe however owing to their very large resistance at $77^{o}K$. This is not so for InSb and in this case it has proved possible to evaluate the variation of μ_s, $\mu_{s_{diff}}$ and μ_{fe} for electrons as a function of surface potential leading to the behaviour shown in figure (44).

Although the surface state results are remarkably consistent from one device to another a large quantitative variation has been observed in the surface mobility results. The general features of figure (44) are however typical, namely that for increasing surface potential the surface mobility decreases.

6.5 Transistor Application

Using device structure B it has proved possible to fabricate field effect transistors from both InSb and PbTe. The transistors were fabricated in exactly the same way as were the devices used for the surface measurements save for the thinner layer of semiconductor required in the former application.

For the capacitance measurement the semiconductor must be thick enough to prevent the space charge from penetrating through to the ohmic contact so that the boundary condition, $\frac{dv}{dz} = 0$ as $z \rightarrow \infty$, of appendix A is satisfied. Saturation of the transistor characteristics however requires

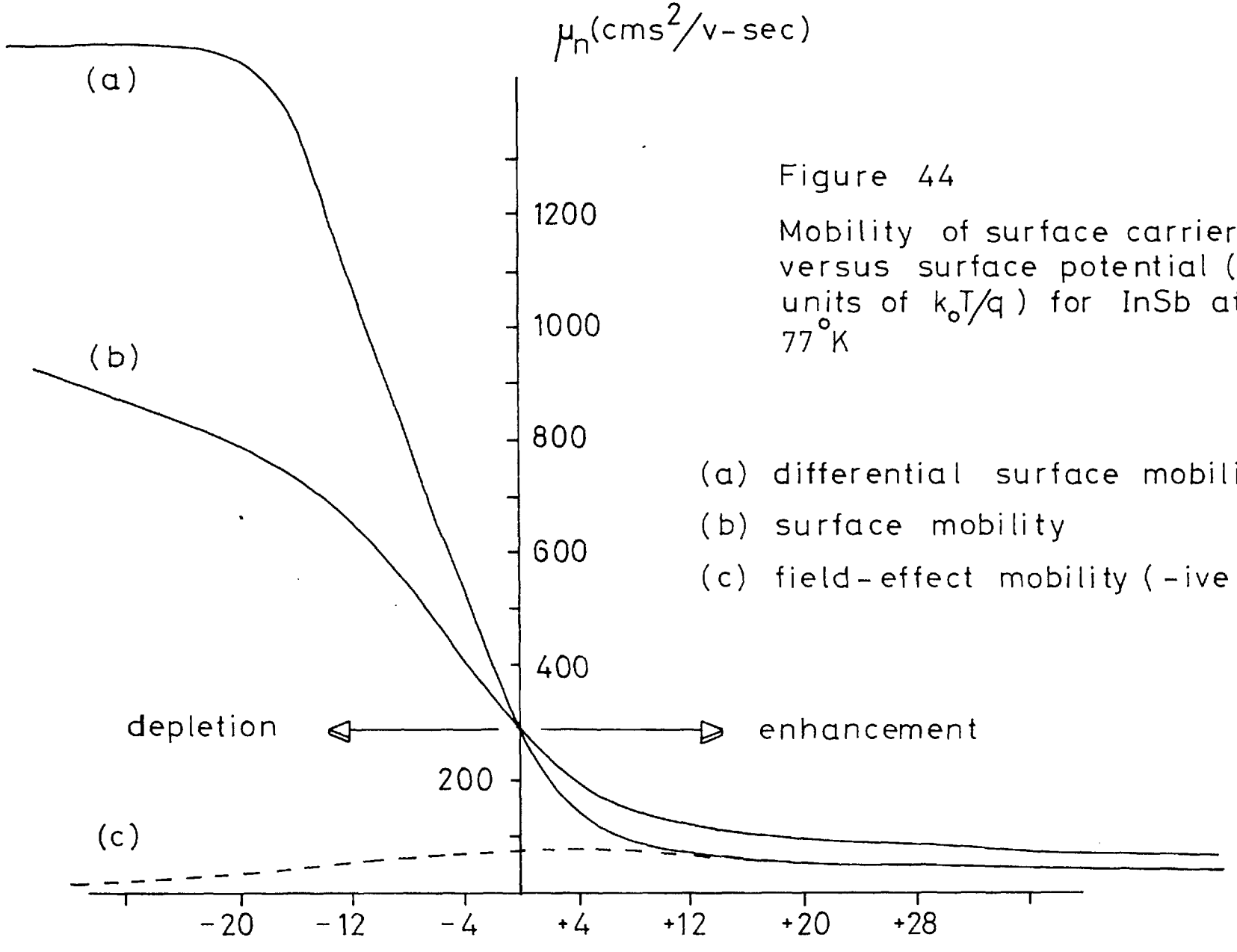


Figure 44

Mobility of surface carriers versus surface potential (in units of k_oT/q) for InSb at 77°K

(a) differential surface mobility

(b) surface mobility

(c) field-effect mobility (-ive)

that the drain end of the semiconductor does completely deplete as was discussed in section 3.4. Semiconductor layers of InSb with a thickness of ~ 1000 Å were found to be sufficiently thin to enable such saturation to occur as is evident in the oscillographs of chapter III.

In the case of PbTe it was not possible to achieve good saturating characteristics at room temperature even for semiconductor layers on the limit of continuity at ~ 450 Å thickness. Such a device was typically observed to behave as shown in figure (45a) and from this oscillograph the poor saturation is evident.

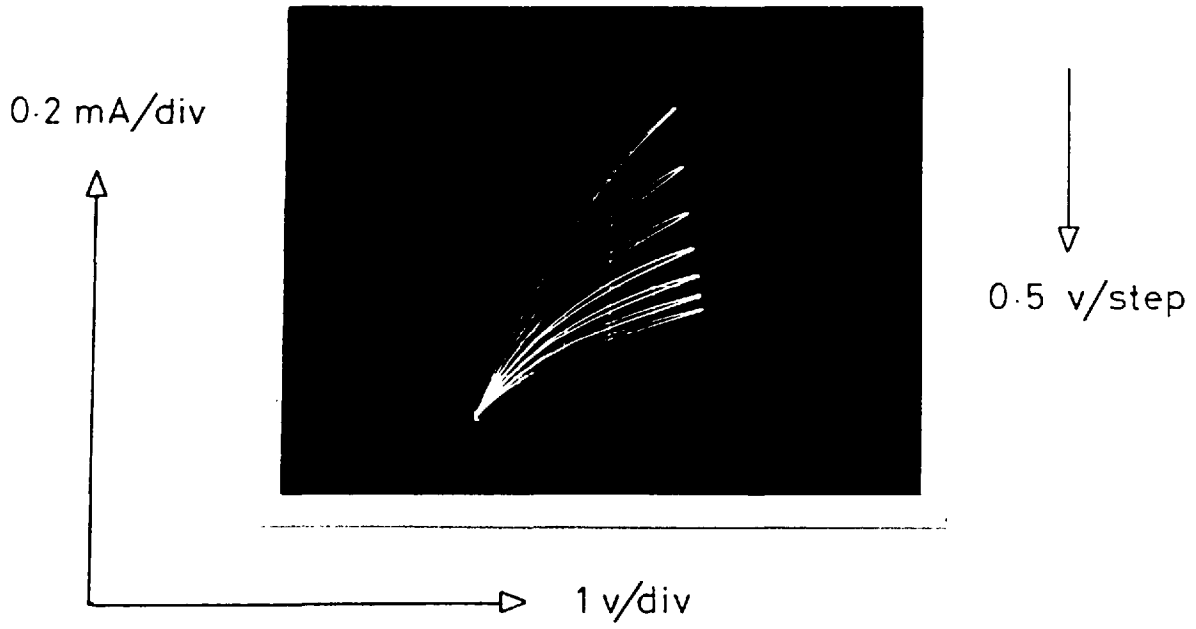
The reason for such behaviour is at the present time little understood. It has previously been observed on a number of materials (P14, F3, A5) but as yet no satisfactory explanation has been forthcoming. A fuller discussion of this point will be given in chapter VII.

On cooling such a device a rapid variation was observed to occur in both the magnitude of the current flowing and in the form of the characteristics. Figure (45b) indicates the form of output characteristics obtained at ~-60°C and by comparison with the room temperature behaviour of figure (45a) the large temperature sensitivity of the PbTe transistor can be appreciated.

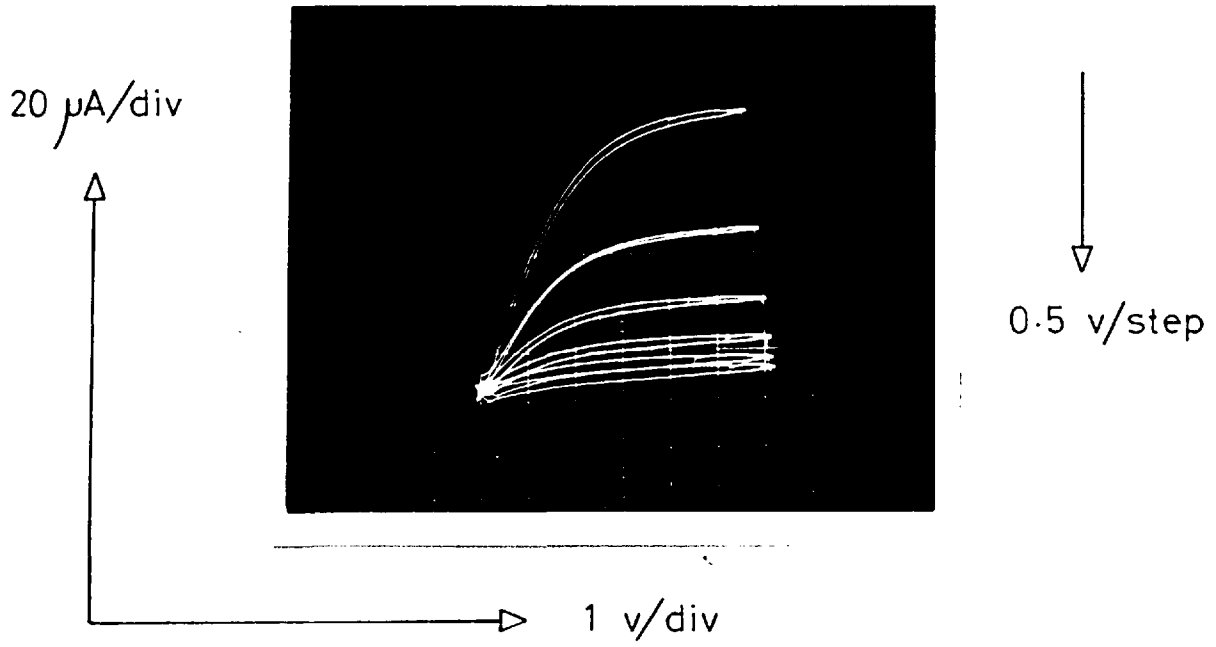
This rapid variation with temperature is consistent with the exponential temperature dependence of R_H, and hence of carrier density, evident in figure (34). The relative temperature insensitivity of the InSb devices is again supported by the Hall coefficient behaviour of figure (34) and indicates, in the present study, the superior properties of this latter material.

It was not possible to obtain mobilities in the films of PbTe

Figure 45



(a) Output characteristics of a PbTe transistor at 20°C



(b) Output characteristics of a PbTe transistor at ~-50°C

significantly greater than those shown in figure (33). For InSb previous workers have shown that by annealing beneath a protective insulator layer very large values of mobility can be achieved (J1, C1), and this was found to be the case in the present work. However the necessity of using evaporated contacts of the low melting points materials In and Sn has precluded the use of such annealing treatments on the present active devices. A mild anneal to ~ 400°C in the absence of an encapsulant has instead been used but by this means it has not proved possible to achieve mobility values greater than ~ 450 $cms^2/v\text{-}sec$.

Prepared in this way field effect mobilities of between 10 and 100 $cms^2/v\text{-}sec$. are typical in these semiconductor films, those of InSb being in general the larger.

6.5.1 Time Dependent Variations

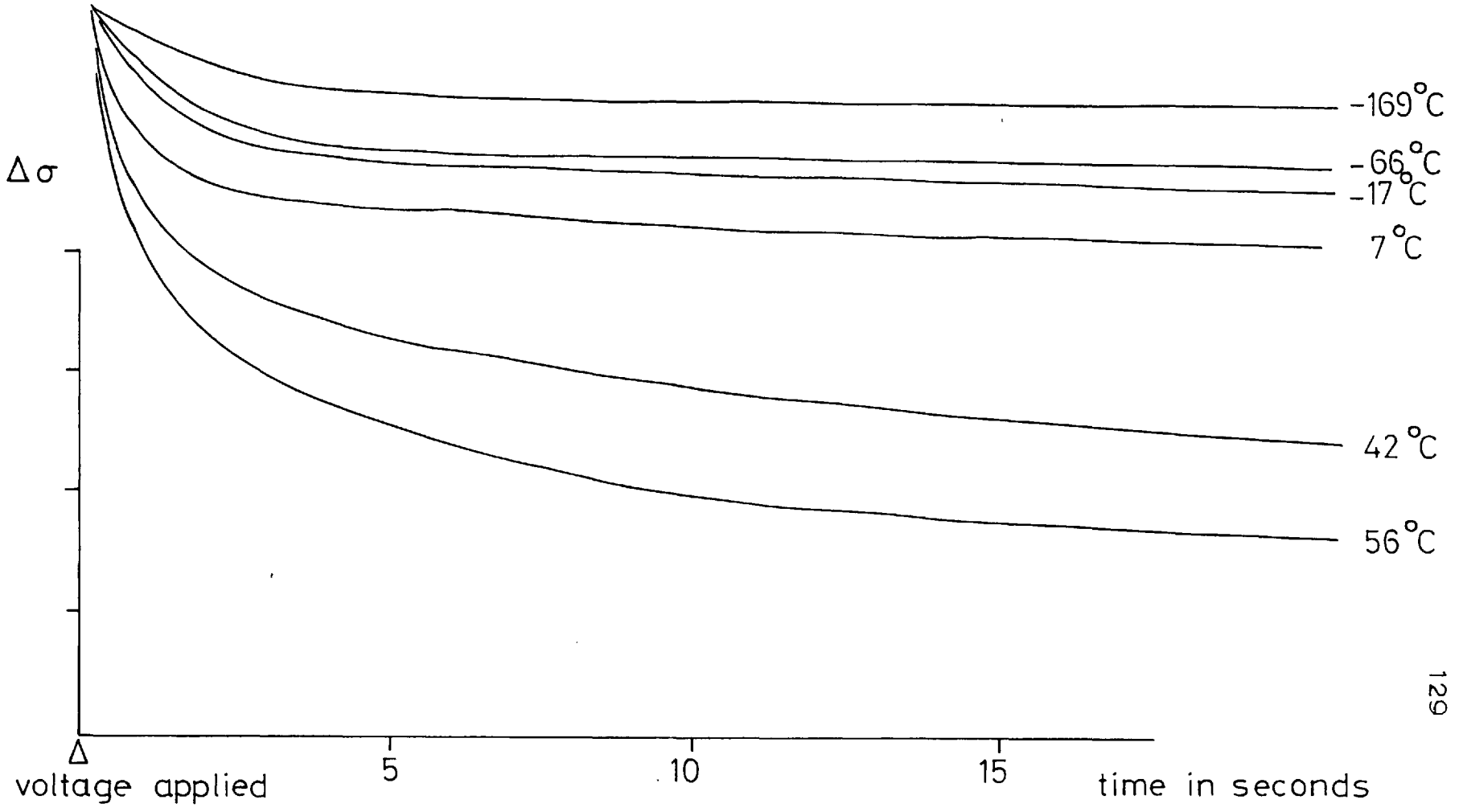
The variation of transistor characteristics with time, commonly termed 'drift' is believed to be mainly the result of charge transfer into the slow states associated with defects in or on the dielectric. The resulting relaxation in the induced conductivity can be conveniently studied by means of the dc field effect described in section 5.5.

Such a study was made on the Al_2O_3/PbTe and InSb interfaces and a typical set of results is shown in figure (46). It is evident that after ~ 10 secs. all charge transfer is essentially complete and that by reducing the temperature of the system the overall effect of the trapping centers can be appreciably reduced.

These slow states are generally believed to fill by one of two mechanisms namely:

Figure 46

The change of semiconductor conductance with time following the application of a 1·5v pulse to an $Al-Al_2O_3-PbTe$ diode. The PbTe was n-type, the surface was enhanced by the pulse and the curves have been normalized to coincide at t = 0·2 secs.



(i) Tunnelling from the semiconductor surface into available trapping sites in the insulator.

(ii) Thermal activation into these sites over the potential barrier resulting from the differences in electron affinity of the semiconductor and dielectric.

Because of the generally observed large temperature dependence of this decay process the thermal activation mechanism has gained wider acceptance. Heiman and Warfield (H10) have shown however that the tunnelling process can be expected to vary with temperature through its dependence on the carrier densities at the semiconductor surface. The tunnelling current is proportional to the product of the tunnelling probability and the available carrier density, the latter in the present situation being an exponentially temperature dependent quantity through the temperature dependence of the carrier distribution function.

From the limited extent of the present investigation no conclusions can be drawn regarding the actual mechanism of filling responsible for the behaviour shown in figure (46). What is apparent however is that, after an initial rapid change, very little long term drift is present in the Al_2O_3/PbTe and InSb system and that by cooling the overall change can be made reasonably small.

The results which have been presented in this chapter represent the principal outcome of this work and in the next (and final) chapter an attempt is made to explain these results in the light of previously reported work.

CHAPTER SEVEN

DISCUSSION AND CONCLUSIONS

7.1 Transistor Saturation

In the discussion of chapter III it was shown that saturating transistor characteristics could be expected for a semiconductor film sufficiently thin to enable complete depletion to be achieved at the drain end of the channel. Empirically it became evident in section 6.5 that although the desired conditions could be met for InSb, for PbTe saturation was poor unless the film was cooled.

This problem of poorly saturating characteristics has for long been treated rather superficially. Hofstein and Warfield (H4) analysed the problem in terms of capacitive channel to drain coupling via the substrate and Geurst's rigorous analysis (G4) led to the conclusion that saturation was solely a function of device geometry, thin dielectric layers and large source to drain spacings leading to large values of slope resistance.

It will be worthwhile to develop here, in terms of quantities which are measurable, a simple model based on the first order concept of 'pinch-off' introduced by Shockley (S1) for the junction transistor.

For these narrow band gap, high impurity density, films the Fermi level well away from the surface can, to good approximation, be assumed to lie at one or other of the band edges (see figure (43)).

At inversion the surface potential is given by* (p.212 of M3)

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* This expression is strictly valid only for non-degenerate conditions but will be sufficiently accurate for our present needs.

$$v_s\Big|_{min} = -2u_b - \ln \frac{\mu_n}{\mu_p}$$

If we assume $\mu_n \sim \mu_p$ and $E_i \sim E_g/2$ then the point of maximum depletion occurs when $qV_s \sim \pm E_g$ (positive for p-type conduction and negative for n-type material).

In terms of the depletion approximation as outlined in section 2.1 the depth of the depletion region is given by

$$d = \left[\frac{2\epsilon\epsilon_o V_s}{qN}\right]^{\frac{1}{2}}$$

and therefore

$$d_{max} = \left[\frac{2\epsilon\epsilon_o E_g}{q^2 N}\right]^{\frac{1}{2}} \qquad (37)$$

The amount of charge/unit area in this depletion region is given by qNd_{max} i.e.

$$Q_{sc}^{max} = (2\epsilon\epsilon_o E_g N)^{\frac{1}{2}}$$

If Q_{ss}^{max} denotes the amount of charge in surface states/unit area at $V_s = \pm \frac{E_g}{q}$ then the two conditions which must be satisfied for complete depletion are:

$$\left.\begin{array}{l} \text{(a) } Q_{induced} \geq Q_{ss}^{max} + (2\epsilon\epsilon_o E_g N)^{\frac{1}{2}} \\ \\ \text{(b) film thickness } t \leq \left[\dfrac{2\epsilon\epsilon_o E_g}{q^2 N}\right]^{\frac{1}{2}} \end{array}\right\} \qquad (38)$$

Inserting typical values for these evaporated layers into the second of these two conditions indicates that for complete depletion of the film its thickness must be less than $\sim$ 1200 Å. This condition is readily satisfied in practice and as a result condition (a) evidently represents the dominant limitation.

From equation (38a) it can be seen that the smaller the band gap the more likely is it that inversion can be reached as was pointed out in section 3.4. However, a large surface state density, a large impurity density and a large value of permittivity all reduce the likelihood that complete depletion can be reached before the electric strength of the dielectric is exceeded. From the results of chapter VI together with the knowledge that the permittivity is inordinately large in PbTe it thus appears that in this respect PbTe is less likely to exhibit saturation than is InSb.

For the anodically formed oxide used in the present work it is possible to induce more than 10^{13} carriers/cms^2 into the semiconductor surface. For PbTe the second term on the RHS of equation (38a) corresponds typically to $\sim 6 \times 10^{12}$ carriers/cms^2 and for InSb the value of this term is less. It is therefore evident that satisfaction of condition (a) depends essentially upon the density of surface states present on the semiconductor surface. A large density, as occurs on the PbTe layers, reduces the expectation of good saturation.

As has been proposed by Grosvalet et. al. (G3), if the electric field along the channel exceeds that value at which the carrier mobility varies as E^{-1}* the current will saturate as a result of this mechanism quite independently of whether the drain is 'pinched-off' or not. Nevertheless once the semiconductor has been completely depleted at the drain end of the channel current flow near the drain will consist of the passage of carriers

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* Ohm's law is strictly valid only for vanishingly small values of electric field and hence carrier velocity for which the average value of carrier energy is essentially that of the lattice. At higher velocities the carriers can acquire an energy appreciably above that of the lattice in which they move and when this occurs carrier mobility will fall. This will continue with increasing electric field until a point is reached at which $\mu \propto E^{-1}$. When this occurs current becomes constant and quite independent of changes in applied field.

through a region in which a very high electric field exists (section 3.1). In this region the carriers are constrained to move at high velocity along the surface of the film remote from the insulator interface and as a result of this large velocity are in a condition to undergo ionizing collisions with both the lattice atoms (L3) and the interfacial defects associated with the substrate-semiconductor interface (H5). If such secondary carrier generation does occur then the slope resistance in the saturation region will be reduced. Avalanche breakdown in this region will be unlikely owing to the limited extent of the high field region (P7) but quite apart from breakdown the presence of excess carriers in this region will reduce saturation and increase the noise level of the transistor in the same way as an inversion layer can degrade performance (see section 3.4).

Because of the smaller activation energy associated with surface state ionization this would seem to be the more likely mechanism by which a secondary generation effect could occur, especially on a surface where this trap density is large.

This brief discussion of the saturation process in the insulated gate transistor is not intended to represent a rigorous analysis. The complete process is inevitably complex and at the present time is only superficially understood. What has been attempted here is a correlation of expected transistor behaviour with the electrical parameters of the semiconductor employed. In this way it has been shown that the poor saturation in PbTe as compared with InSb can be ascribed to its larger surface state and doping density together with its large value of permittivity.

The temperature dependence of the characteristics, which as has been shown is so pronounced in PbTe, is implicitly included in the above through the temperature dependence of N, the charge density in the depletion region.

7.2 The MIS Measurement

7.2.1 The Inherent Error

As has been shown in previous chapters, the differential capacitance curve tends asymptotically to the dielectric capacitance on either side of the minimum and in these regions comparison of the theoretical and experimental curves can involve large inaccuracies.

In a thoroughgoing and critical discussion of the differential capacitance method Zaininger and Warfield (Z7) considered the error associated with the determination of the surface capacitance containing the required information from the total measured capacitance. Perhaps as a result of a mistake in presentation an incorrect impression was given in that paper which has been corrected by the present author (L8) and is reprinted in appendix D.

From this appendix it can be seen that the deduction of C_s from C_t can be accomplished with acceptable accuracy providing that the major part of the error of measurement is systematic in nature. With a dynamic measurement technique as employed in the present study this is in fact the case. The error involved in circuit calibration and that involved in deducing the C_{ox} asymptote are both systematic in that they are single quantities which apply to all points on the measured capacitance curve. Circuit non-linearity is similarly systematic for the near unity values of C_n which occur in the present case as a result of the high material doping densities.

The main random component of error is that associated with noise in the measuring circuit. This can be minimized however by integrating the output photographically by means of a relatively long exposure time (typically $\sim$ 0.2 secs). As a result of this it is estimated that the final error in C_t from this source is as low as $\sim \pm$ 0.1%.

For such random errors it is necessary to consider mean values and thus from equation (4) of appendix D we have*

$$\left[\frac{dC_s}{C_s}\right]^2 = \frac{1}{(1-C_n)^2}\left[\frac{dC_t}{C_t}\right]^2 + \frac{C_n^2}{(1-C_n)^2}\left[\frac{dC_{ox}}{C_{ox}}\right]^2 - \frac{2C_n}{(1-C_n)^2}\frac{dC_t}{C_t}\cdot\frac{dC_{ox}}{C_{ox}}$$

which, for near unity values of C_n such that

$$\left[\frac{dC_t}{C_t}\right]^2 \simeq \left[\frac{dC_{ox}}{C_{ox}}\right]^2$$

reduces to

$$\left[\frac{dC_s}{C_s}\right]^2 = \frac{(1+C_n^2)}{(1-C_n)^2}\left[\frac{dC_t}{C_t}\right]^2 - \frac{2C_n}{(1-C_n)^2}\frac{dC_t}{C_t}\cdot\frac{dC_{ox}}{C_{ox}}$$

Taking the square root of the mean of this expression gives

$$\frac{dC_s}{C_s} = \frac{(1+C_n^2)^{\frac{1}{2}}}{(1-C_n)}\cdot\frac{dC_t}{C_t} \qquad (39)$$

This expression indicates that the error in deducing C_s from C_t diverges rapidly for $C_n \longrightarrow 1$. In fact for the estimated random error in the present case of 0.1% equation (39) indicates that C_n must be less than 0.99 to keep the error in C_s below 14%. As can be seen from figures (37) and (38) this is so in the present case and this fact, combined with an estimated 10% systematic error in the method, results in the conclusion that the present capacitance measurement is accurate to within $\leq \pm$ 15%.

7.2.2 Dielectric Leakage

One of the outstanding features of the surface channel FET is its large input impedance, associated with the high resistivity dielectric layer in the input circuit of the device.

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* C_t in the text replaces C of appendix D.

Dielectric conduction has been the subject of a great deal of work (for a review see L9) and in general it is possible to describe such conduction in terms of bulk and contact limited processes.

For very thin layers an additional mechanism can contribute to dielectric leakage. Carriers tunneling between the metal electrodes can reduce the apparent resistivity of the insulator by orders of magnitude below that value which would be predicted from bulk data. This quantum mechanical conduction process sets an upper limit on the value of C_{ox} which may be employed in the MIS structure of figure (3). As has been shown in chapter IV as large as possible a value of dielectric capacitance is desirable so as to maximize the deviation of the measured capacitance from that of the dielectric. Dielectric layers as thin as ~ 150 Å have been employed in the present study and even with the large values of capacitance associated with such thin layers deviations of no more than 10% are obtained with PbTe (see figure(37)).

Tunneling will manifest itself as an enhanced value of leakage and hence loss tangent and although there is no indication of this occurring in the case of the thin Al_2O_3 layers employed in the present study it will be instructive to consider the limit set on loss tangent by dielectric leakage.

Transport of carriers through the insulator will result in a deviation from thermal equilibrium in the surface of the semiconductor. The limit on this leakage is set by the level of disequilibrium which is tolerable.

For a given rate of dielectric transport the disequilibrium in the space charge region will be much less in enhancement and depletion than in inversion as a result of the much lower rate of carrier supply in the latter case as discussed in section 4.3. Considering this worse case with reference to figure (47), for zero leakage thermal equilibrium must prevail with the

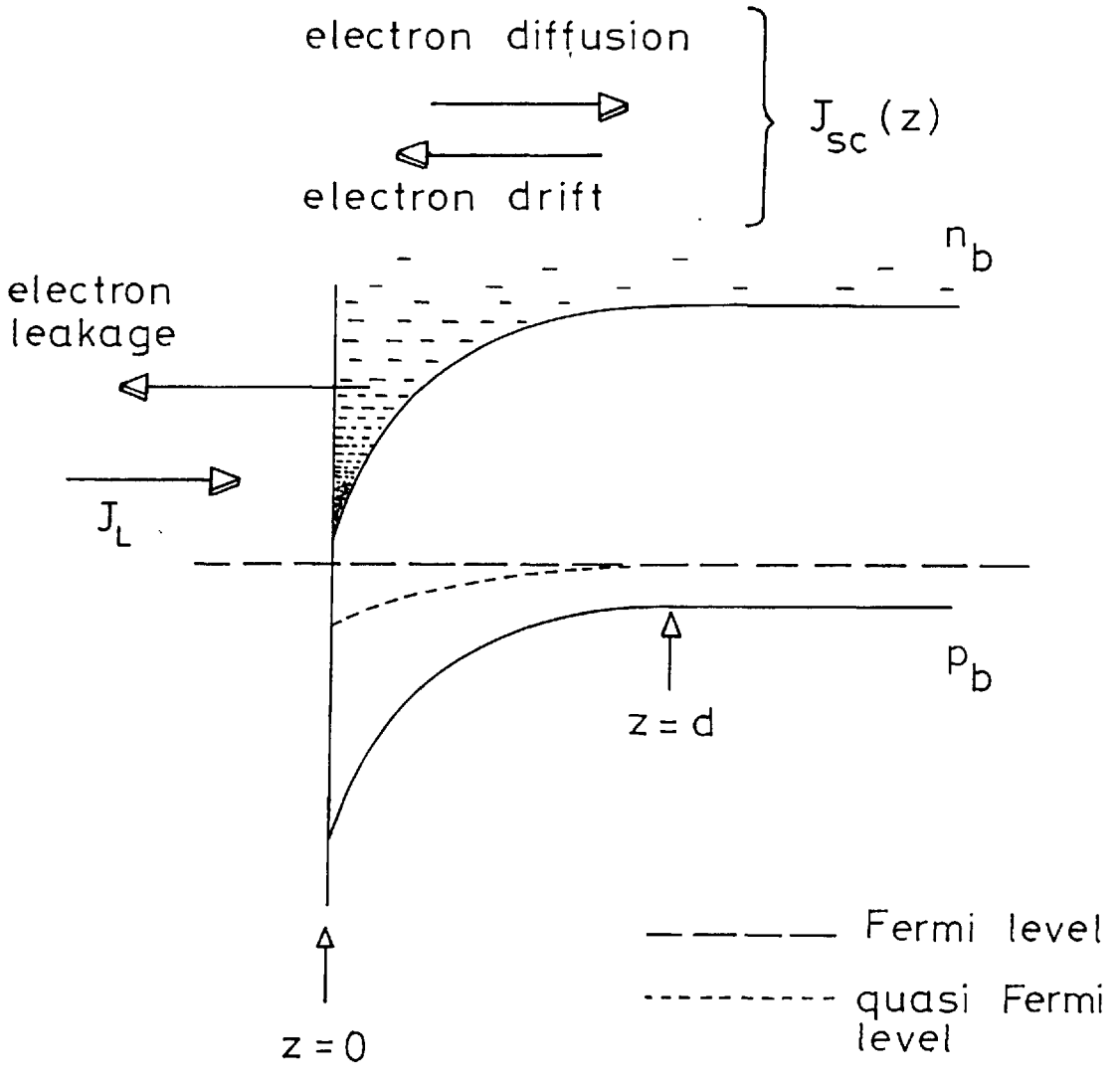

Figure 47

An inversion layer in the presence of leakage

diffusion and drift currents in the inversion layer exactly balancing for both holes and electrons. In this case the Fermi level continues flat up to the surface and the analysis of appendix A is strictly valid.

For a finite value of dielectric leakage current J_l/unit area current flow will occur normal to the surface in the semiconductor, being given by

$$J_{sc}(z) = (n \mu_n + p \mu_p) \frac{dE_f}{dz}$$

where E_f is the quasi Fermi energy.

For the n-type inversion layer shown we may write to good approximation

$$J_{sc}(z) = n \mu_n \frac{dE_f}{dz}$$

and for small deviations from equilibrium so that generation and recombination rates may be equated at all values of z then

$$J_l = n \mu_n \frac{dE_f}{dz}$$

$$\text{i.e.} \quad \Delta E_f = \frac{J_l}{\mu_n} \int_o^d \frac{1}{n} \, dz$$

where ΔE_f is the change in Fermi energy across the space charge region of depth d.

If V, at frequency w, is the voltage across the MIS diode then

$$\text{Tan } \delta = \frac{J_l}{wV C_{ox}}$$

$$= \mu_n \Delta E_f \left[wV C_{ox} \int_o^d \frac{1}{n} \, dz \right]^{-1}$$

For a given tan δ a liberal estimate of ΔE_f, the deviation from equilibrium,

may be obtained by taking $n = n_b$. As n_b, the bulk electron density, is the smallest value of n in the space charge region this overestimates the above integral and leads to a maximum estimate for ΔE_f i.e.

$$\Delta E_f\Big|_{max} = \frac{wVd\ C_{ox}}{\mu_n\ n_b} \cdot \mathrm{Tan}\ \delta \qquad (40)$$

7.2.3 Hysteresis

The field effect mobility defined in section 2.7 is in general a complex quantity, the phase relationship between the induced conductance change and the applied voltage being a function of frequency and the relaxation times of any surface states which may be present (p.244 of M3).

At angular frequencies well below and well above the reciprocal relaxation time of the surface states the phase angle of μ_{fe} becomes zero as a result of the states being completely in and out of equilibrium respectively. For frequencies near to the characteristic frequency of the states a phase displacement occurs between the induced charge and the resultant change in conduction as a result of charge interaction between the states and the induced surface space charge.

In an FET such a displacement will result in a phase shift between channel current and gate voltage leading to hysteresis in the characteristics of such a device.

Hysteresis of device characteristics together with drift and irreproducibility have been the main reasons why thin film FET have not as yet reached the production stage. It should however be borne in mind that hysteresis is a function of frequency of measurement and although a device may exhibit large phase shifts at the 120 c/s which is the most popular frequency

of characterisation*, it does not preclude its hysteresis free operation at higher frequencies.

Hysteresis has been observed in the present work on both the conductance and differential capacitance curves for both InSb and PbTe. The effect has been less at low temperature and has been further reduced by choosing the bias frequency so as to minimise the effect.

7.3 Surface States

7.3.1 The Physical Interpretation of Q_{ss}

The variation of trapped surface state charge with surface potential shown in figures (39) and (40) is obtained, as was described in chapter IV, by comparing theoretically and experimentally derived curves. Q_{ss}, defined in this way is thus solely a measure of the difference between an experimental quantity and a value based on an arbitrary theoretical model; the model (analysed in appendix A) chosen in the present case being based on three as yet unverified assumptions namely

(i) that the semiconductor is a single crystal;

(ii) that the band structure is that appropriate to a single crystal;

(iii) that the sample is sufficiently thick to enable the boundary condition

$$\frac{dv}{dz} \longrightarrow 0 \text{ as } z \longrightarrow \infty$$

to be applied.

The last two of these assumptions will be discussed in subsequent sections but for the moment consider the consequences of assuming the film to be crystalline.

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* The widely used Tektronix transistor curve tracer operates at this frequency

As was shown in section 6.1, the materials employed here are polycrystalline. Electrically this is equivalent to a single crystal structure permeated by a three dimensional grid of edge dislocations corresponding to the crystallite boundaries evident in micrograph (31f).

The measured capacitance is only affected by that region of the semiconductor lying within the space charge and as a result Q_{ss} as measured will only include the effects of the grain boundaries in the surface space charge region, those outside it being of no consequence.

Grain boundaries are planes of crystal mismatch and as a result are electrically analogous to the external surfaces of the material. These internal surfaces were first studied for n-type Ge in 1954 by Read (R3). The conclusion in that case was that the mismatch resulted in a distribution of acceptor states across the forbidden gap.

Lacking evidence to the contrary it seems likely that the behaviour of these internal surfaces is similar to that of the true surfaces as discussed in section 2.3, namely that for extrinsic material the surface states will result in the formation of a depletion region.

The intergrain states are of course distributed in space, as well as energy, along a direction normal to the external surface of the semiconductor and any measurement of surface states will evaluate not only those on the external surface, which might well be the same as those on a single crystal sample, but in addition those on the grain boundaries within the space charge region.

As will become evident in section 7.5 a great deal of effort has gone into the study of the mobility degrading effects of grain boundaries whereas their influence on surface state densities has not apparently been

appreciated. Indeed to the present author's knowledge no measurements whatsoever have been previously reported on the distribution of surface states on polycrystalline surfaces.

The contribution of these grain boundaries to an enhanced value of surface state density can in part explain the relatively poor values of field effect mobility reported for such disordered structures; the other main contribution will be discussed in section 7.5.

An additional contribution to Q_{ss} can arise from states in the dielectric being in good electrical contact with the semiconductor. This has been discussed by Heiman (H10) who demonstrated how severely a distribution of traps in space can distort their measured distribution in energy.

Although from what has been said it should be evident that little can be concluded from curves of Q_{ss} versus V_s regarding their physical location, nevertheless this detracts nothing from the usefulness or validity of such a measurement. Surface states and surface trapping are defined in terms of deviations of practice from theory and whether or not these surface states are truly associated with the external surface is really of no consequence. Curves such as those of figures (39) and (40) show how much of the induced charge does not lie in the conduction, valence and impurity levels of the material and must be interpreted with this in mind. It is apparent therefore why N_{ss} of figures (41) and (42) was termed the 'effective' surface state density.

Many authors have gone to some trouble to associate trapped surface charge with traps lying at discrete energy levels. As was pointed out by Montgomery and Brown (M4) this can only be accomplished unambigiously if the variation in trapped charge is known for an infinite range of surface

potential, but nevertheless, even assuming that it is possible the distinction between a discrete and a continuous distribution is somewhat obscure.

Consider an unfilled set of levels at an energy E^o capable of accepting N_s electrons. If one electron is trapped the remaining (N_s-1) levels will lie at a new energy $(E^o+ \delta E^o)$ where δE^o, the interaction energy, corresponds to the increased energy associated with a subsequent charging of an initially ionized set. This continues for each additional electron supplied and as a result the initially assumed discrete set of levels will appear on a Q_{ss} versus V_s plot as a distributed quasi-continuum.

This is exactly analogous to the discussion of appendix A regarding bulk trapping levels and because of the large densities typical of surface state distributions the spreading in energy can be large corresponding in the bulk to the spreading of impurity levels into bands.

For this reason as well as the suspected inapplicability of Fermi statistics to surface state populations (see section 2.3.1) no attempt has been made in the present work to associate measured trapped surface charge with actual surface trap levels. The curves of N_{ss} in figures (41) and (42) depict the net effect of these trapping levels and are considered sufficiently informative in themselves.

7.3.2 Comparison with previous Results

As was mentioned in the preceding section no results have been previously reported for surface state distributions on polycrystalline solids and in addition no theoretical analysis, even for the single crystal case, has been performed for a realistic surface model.

These two deficiencies in the literature of this subject make it difficult to discuss the validity or otherwise of the present surface results

in the light of previous work. What can be done however is to compare the results in a qualitative fashion with those which have been reported on single crystal surfaces.

The earliest work on surface states was carried out in the main on Ge and Si and from these results, which were obtained by a variety of experimental techniques on both clean* and real surfaces, it became evident that on Ge surfaces there were ~ 10^{11} states/cms^2 and for Si ~ 10^{12} states/cms^2. Even though these measured distributions showed rather a large spread a general trend was observed which is typified by the results of Many and Gerlich (M8) reproduced in figure (48).

On these large band gap materials it was usually only possible to investigate perhaps less than one third of the band gap but nevertheless, as the results of figure (48) show, surface state densities were invariably observed to increase near the band edges.

Qualitatively it therefore appears that the present results are in general agreement with earlier work on Si and Ge which perhaps lends support to the results shown in figures (39) and (40).

To the present author's knowledge the only previous reports of a rigorous nature on the surface state distributions on either PbTe or InSb are those of Davis (D4) on single crystal InSb and Egerton (E2) and Juhasz (J2) on epitaxial PbTe and InSb respectively. The results of Juhasz and Davis were in reasonable agreement and are typified by the distribution shown in figure (49) which is reproduced from reference D4. It can be seen that although the distribution on this single crystal surface is in general agreement with the

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* A clean surface is one on which there are no impurities. As might be expected this condition is only partially attainable in practice.

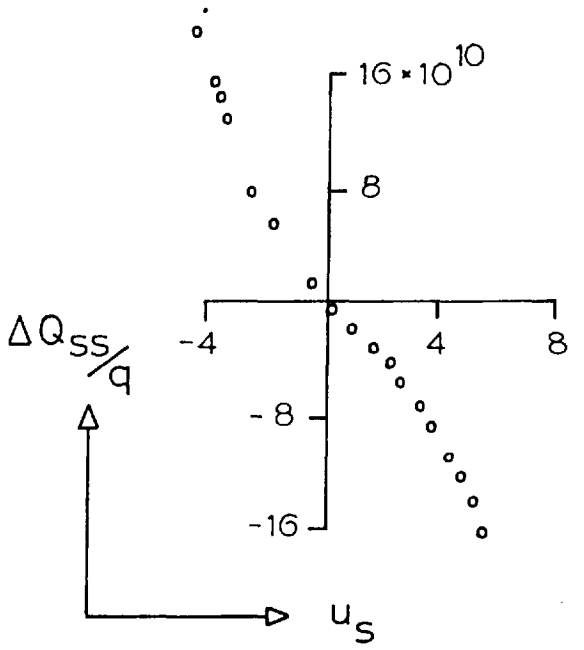

Figure 48

Variation with surface potential of the trapped surface charge (cms^{-2}) on n-type Ge at 289°K

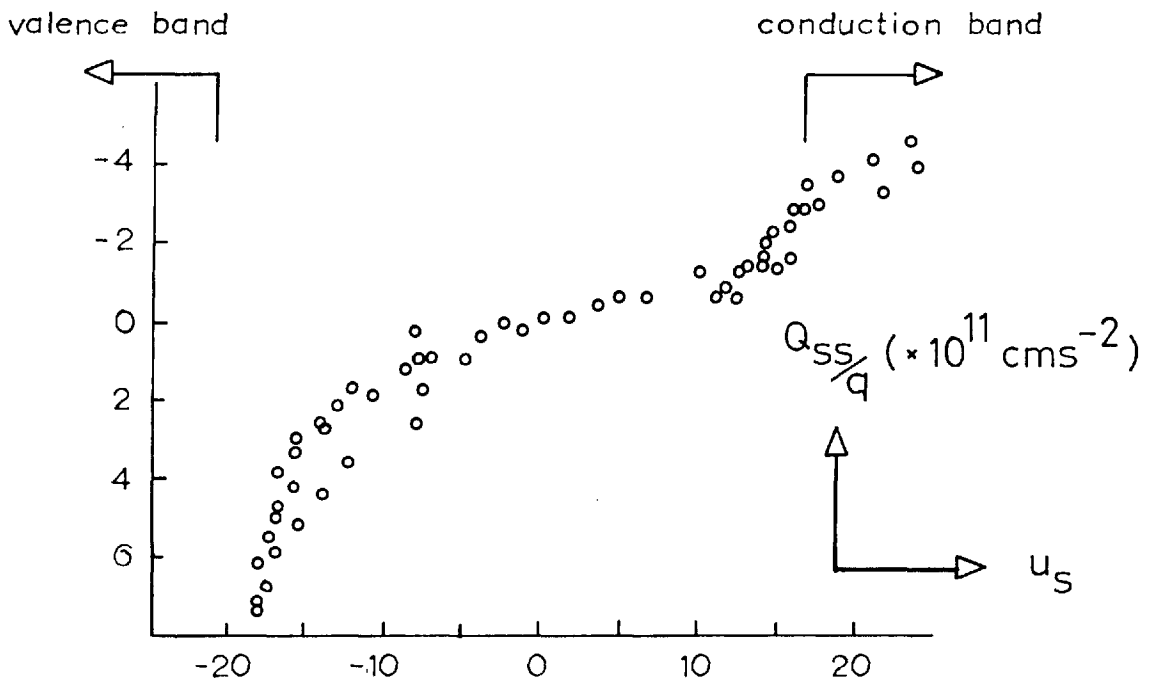

Figure 49

Variation of the trapped electronic charge with surface potential for the $(\bar{1}\bar{1}\bar{1})$ surface of n-type InSb at 77°K

present work the actual magnitudes are smaller. This is also the case with the results of Egerton on PbTe where a uniform distribution of $\sim 1.7 \times 10^{13}$ states/cms^2-eV was observed at room temperature.

The similar distribution although larger density observed on the polycrystalline films compared with the earlier results on single crystals substantiates the discussion of section 7.3.1, and further support perhaps lies in the larger density observed in the present study on the PbTe surface as compared with that on the surface of InSb (cf. figures (41) and (42)). As was proposed in section 7.3.1, the larger density of surface states on polycrystalline layers compared with single crystals can be associated with the intergrain states lying within the surface space charge region. The larger the extent of the space charge the larger will therefore be the contribution of the intergrain states and as can be seen from equation (37) the space charge region penetrates further in PbTe than in InSb owing to the larger permittivity of the former.

One final point is that, if in fact the surface state density is larger on polycrystalline layers as a result of the internal surface contribution then in general the state distribution should be similar on single crystal and polycrystalline surfaces provided that the intergrain state distribution is not too different from that on the external surface. Comparison of figures (40) and (49) indicates that in fact this may be so.

Following the success of the MOST a vast effort has been devoted to measurements on the thermally oxidized Si surface. Densities of states measured on this system have varied widely but considering the very low density ($\sim 10^{10}$ cms^{-2}) of states present, resulting in a critical dependence on contamination, this is perhaps not surprising.

Potentially any impurity can act as a surface state but from the small amount of data available at the present time (D4, B13, B5) it appears that metal ions are perhaps the most effective in this respect. It was the recognition that Na contamination was degrading MOST performance (H12) that led to the present low value of surface states on such devices.

7.3.3 Band Structure of Polycrystals

We shall now briefly consider the second of those assumptions listed in section 7.3.1 namely, what are the consequences to be expected from employing single crystal band data to a polycrystalline structure.

Polycrystals in terms of their structure essentially lie midway between single crystal and amorphous materials. The theory of amorphous structures is at the present time in an early stage of development but nevertheless, from the work which has been done, it is possible to estimate the general effects on band structure of a loss in long range periodicity.

It appears (M9) that if each atom of a periodic lattice is displaced by a factor γ so that all long range order is lost at a distance of $\frac{a}{\gamma^2}$, where 'a' is the lattice constant, then the effect on the allowed electron levels of the single crystal form is to raise them by an amount

$$\gamma^2\left(\frac{3\hbar^2}{2m}\right)\left[\frac{3}{a^2} + k^2\right] \qquad (41)$$

where k is the electron wave vector. k varies from zero at the bottom of a band to π/a at the top and hence equation (41) indicates that disordering of an initially periodic lattice leads to a narrowing of the forbidden energy range by an amount

$$\gamma^2\left(\frac{3\hbar^2}{2m}\right)\frac{\pi^2}{a^2} \qquad (42)$$

Furthermore a distortion of the density of states function near the band edges is believed to occur together with a certain amount of localization

of these levels (G7, B11).

If we consider a polycrystal to be analogous to an amorphous structure with a value of half the crystallite size for the distance over which long range order is lost, then for crystallites of 1000 Å diameter and using parameters appropriate to the materials of interest here, equation (42) indicates that the forbidden gap should decrease by ~ 0.025 eV below its single crystal value, this corresponding to ~ 10% of the band gap employed in the surface state evaluation at $77^{o}K$ (see table (ii)).

Any error in the assumed band model employed in the theoretical analysis will manifest itself as a contribution to the measured surface state density in accord with the discussion of section 7.3.1 and further, this spurious contribution will decrease from the band edges due to the smearing out of the density of states function resulting from the structural disorder. The effect will also be the less the smaller the value of the density of allowed states and as can be seen from figure (42) the measured surface state density near the conduction band of InSb is relatively low.

The 10% change in band gap which results from the first order theory of equation (42) is an overestimate owing to the fact that we have assumed the material to be amorphous rather than polycrystalline. The shift appropriate to the discrete disordering of a multi-crystallite structure is unknown at the present time as is the form of the density of states function for such a material.

Because of all these uncertainties it seems inappropriate to pursue this topic further but nevertheless it should be borne in mind that some contribution to N_{ss} may result from band edge spreading although as can be seen from figure (49) similar behaviour to that of the present results has been observed on single crystal material.

7.4 Interpretation of the Hall Coefficient of PbTe

Epitaxial single crystal films of both InSb (J2) and PbTe (Z6) like bulk samples (M6, A3) exhibit essentially temperature independent values of R_H over large ranges of temperature. This behaviour is an indication of a practically constant value of carrier density consistent with a degenerate carrier distribution and implies a high density of fairly shallow*, and electrically active impurities.

In an intrinsic semiconductor which is non-degenerate the electron and hole densities, being equal, are given by (see any standard text on semiconductors)

$$n_i = p_i = 2\left[\frac{2\pi k_o T}{h^2}\right]^{3/2} (m_e\, m_h)^{3/4} \exp\left[-\frac{E_g}{2k_o T}\right] \qquad (43)$$

From section 5.3

$$R_H\Big|_i = \frac{r}{qn_i}\left[\frac{\mu_p - \mu_n}{\mu_p + \mu_n}\right] = N_i \exp\left[\frac{E_g}{2k_o T}\right] \qquad (44)$$

where $$N_i = \frac{r}{2q}\left[\frac{2\pi k_o T}{h^2}\right]^{-3/2} (m_e\, m_h)^{-3/4}\left[\frac{\mu_p - \mu_n}{\mu_p + \mu_n}\right]$$

this being in general only slightly temperature sensitive compared with the exponential term of equation (43).

From equation (44) it is therefore to be expected that an intrinsic material will exhibit an exponential dependence of R_H upon temperature which is what is in fact observed in the present case of polycrystalline PbTe.

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* Shallow in this context refers to the distance in energy of donors from the conduction band edge and acceptors from the valence band edge. Impurity centers located at a large energy from their relevant bands are termed 'deep'.

As was stated in sections 1.3.1 and 1.3.4 it has not been possible to grow intrinsic PbTe in either bulk single crystal or epitaxial film form and thus the apparent intrinsic behaviour in the present case is rather surprising.

As far as carrier density is concerned of course compensation of one impurity type by the other can result in a material appearing intrinsic and, although bulk compensation would not be expected in polycrystalline materials when it is not observed in the single crystal case, compensation at the surface would be more effective owing to the larger surface area for a given volume of the former structure.

As can be seen from the results shown in figure (43), the quiescent surface condition of PbTe is such that, at the surface, the Fermi level passes practically through the centre of the forbidden gap. The surface is thus essentially intrinsic, held so by the surface states which act to compensate the heavy bulk doping.

The depth to which the effect of this surface compensation will be felt can be estimated to first order by means of the depletion approximation outlined in section 2.1. By this means, taking typical values for the parameters of PbTe together with the measured value of quiescent surface potential leads to a depletion depth of ~ 1200 Å. Although the Fermi level will move away from the mid band gap position as the distance from the surface increases this 1200 Å can be taken as a first order approximation to the depth of semiconductor dominated by the surface.

Because of the large thermal mismatch between PbTe and the glass substrates* employed in the present work irreversible cracking of the semi-

* The linear coefficient of thermal expansion of PbTe is ~ 19.0 x 10^{-6}/°C (N2) whereas that of Corning 7059 glass is ~ 4.5 x 10^{-6}/°C.

conductor occurred for films thicker than ~ 2500 Å and hence for all thicknesses employed here it can be seen that the majority of the film is dominated by the space charge associated with the surfaces of the film. In addition, if the internal surfaces behave in the same way as the external ones, as the crystallites are in general always less than ~ 1500 Å in diameter, surface dominated behaviour can be expected even for films much thicker than 2400 Å.

Exponential R_H behaviour has been reported previously for polycrystalline films of both wide band gap (MIO) and narrow gap materials, the behaviour in the former case being attributed to deep impurity levels. Working with polycrystalline PbS Zemel and Varela (Z5) and Petritz et. al. (P9) have observed intrinsic behaviour similar to that observed in the present case and have also attributed it to compensation, the active species being believed to be oxygen. It was in fact proposed that these compensating centers may, in addition, be responsible for the enhanced photoconductivity by acting as minority carrier traps, in agreement with a proposal by Harada and Minden (H9), and that these centers may well be located at the semiconductor surfaces rather than in the bulk.

Although at the time these inferences were rather tentative in nature they can be seen to be in complete agreement with the present results.

The above interpretation of the Hall data, namely that in the case of polycrystalline films of PbTe as prepared here the film is dominated by the surface states, does to some extent invalidate the analysis on which the conclusions are based. As is shown in appendix A, it is necessary to assume that the semiconductor is sufficiently extensive in a direction normal to the surface to enable the assumption to be made that

$$\frac{dv}{dz} \longrightarrow 0 \quad \text{as} \quad z \longrightarrow \infty$$

In PbTe films of the thicknesses employed here this apparently does not hold and the results of figure (41) must in consequence be viewed with this in mind.

In contrast to the quasi-intrinsic appearance of the PbTe samples, the films of InSb appear well behaved. This is, however, hardly surprising considering the much lower surface charge present on this material (see figure (43)). Again using the depletion approximation the depth of semiconductor affected by the surface works out at less than 400 Å which is sufficiently small to exert only a secondary effect on the measured Hall coefficient compared with the underlying low resistance extrinsic region.

7.5 Carrier Transport in Polycrystalline Layers

The theoretical analysis of carrier transport in bulk crystalline materials has been extensively studied for a great many years and experimental results can, in general, be successfully accounted for in terms of carrier interactions with either the lattice, defects or impurities.

The theoretical extension to thin films was undertaken as early as 1901 by Thomson (T5) who considered the surface contribution to carrier scattering in metal films. As was described in section 2.5, this treatment has been extended and modified to include the effects of surface space charges and at the present time a fairly extensive volume of literature is available on this aspect of thin film transport.

In the case of the polycrystalline films studied here however an additional scattering mechanism would seem to be important. Although each crystallite may to good approximation be considered single crystal the region

between the crystallites, the intergrain regions, are far from ordered. As was discussed by Mataré (M7) these regions may be considered as planes of dislocations and as such might be expected to be electrically charged. The polycrystal thus contains a large density of defects which, unlike the usual situation in bulk crystals, are to some extent ordered. They lie on a three dimensional intersecting grid defined by the crystallites.

Carrier transport in such a structure would thus seem to be far from simple and in fact at the present time very little theoretical work has been undertaken on this problem.

In contrast a fairly large amount of experimental data has been reported and from this it is possible to conclude that, in general, polycrystalline layers exhibit a positive temperature coefficient of mobility over large ranges of temperature with a maximum sometimes being observed at around 300°K. In addition, the absolute magnitude of the mobility is invariably well below that of the bulk; the general form of behaviour being typified by the present results shown in figure (35).

Lattice scattering always predicts a negative temperature coefficient of mobility and thus the dominant mechanism would seem to be other than this for these layers. Even for relatively well ordered polycrystals the above behaviour still seems to exist, this being typified by the results of Wieder (W9) where even for films with mobilities greater than half of their bulk values at 300°K a decrease of mobility with decreasing temperature was observed.

Once it is accepted that mobility limitation is set by defects or impurity inclusions it would seem reasonable to expect these to be associated in large part with the highly disordered intergrain regions. This in fact has

been the conclusion of all authors since this mechanism was initially proposed by Gunther (G6) in 1962. Correlation has in fact been obtained between mobility and crystallite size in such films although the spread of results in such cases is invariably large (J2).

More rigorous studies of the effects of grain boundaries in thin films do not at this time seem possible, as a result of the lack of understanding and control of the parameters which control the growth behaviour in such layers. A more reasonable approach would seem to be that of introducing one grain boundary into an otherwise single crystal during growth. Such bicrystals have been studied by Mataré (M7) who concluded that such a grain boundary will contain interfacial states which will result not only in adjacent depletion regions but perhaps also in an inversion layer close to the boundary, along which the conductivity is high. Perpendicular to the interface however little conduction will occur owing to the potential barrier existing in that direction (see figure (50)).

Transport in polycrystals will involve movement of carriers through such regions which indicates perhaps why such low values of mobility are invariably encountered in these structures.

Although at present at a somewhat unsatisfactory stage of development, we shall for completeness briefly review here the two theories existing at present for transport in such polycrystals

(i) The barrier theory - In this model, which was developed initially to account for the phenomenon of photoconductivity (P13), the film is assumed to be composed of a number of high resistance intercrystalline barriers connected in series by low resistance grains.

In this case each barrier has a band diagram of the form shown in

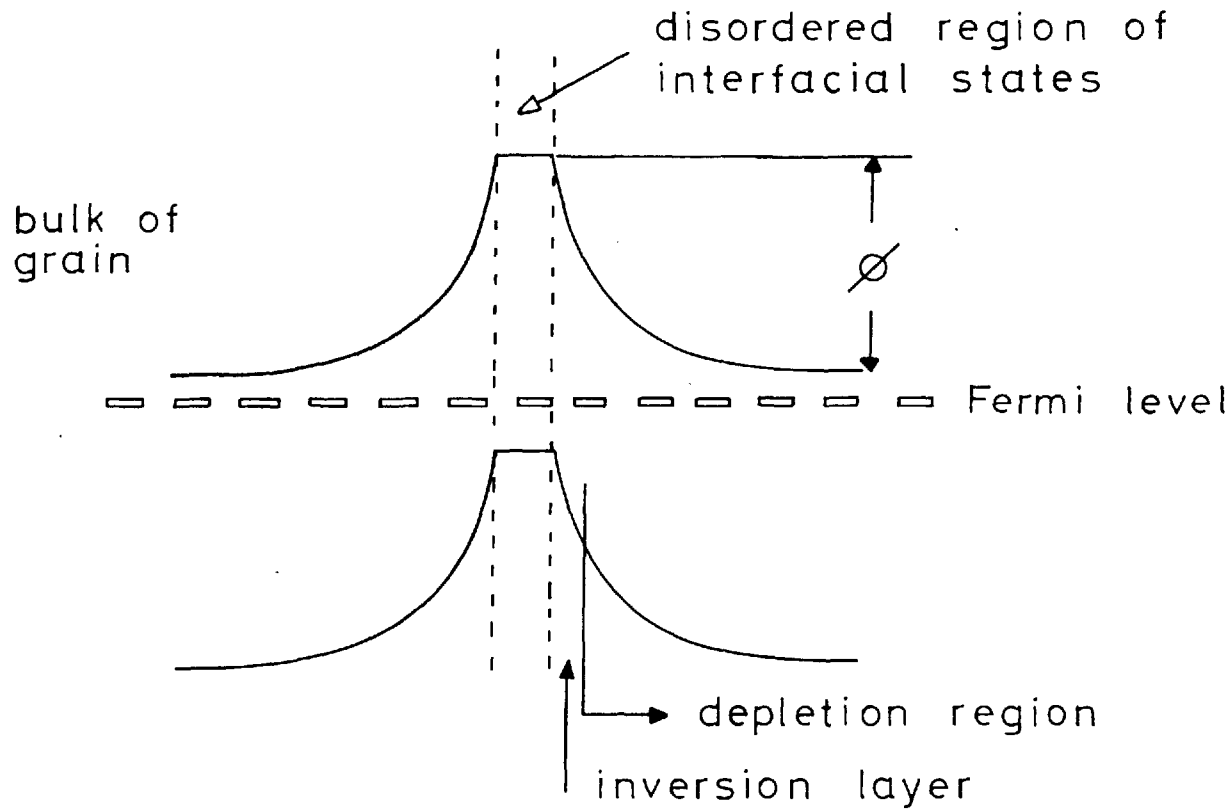

Figure 50

Band diagram for grain boundary in n-type material

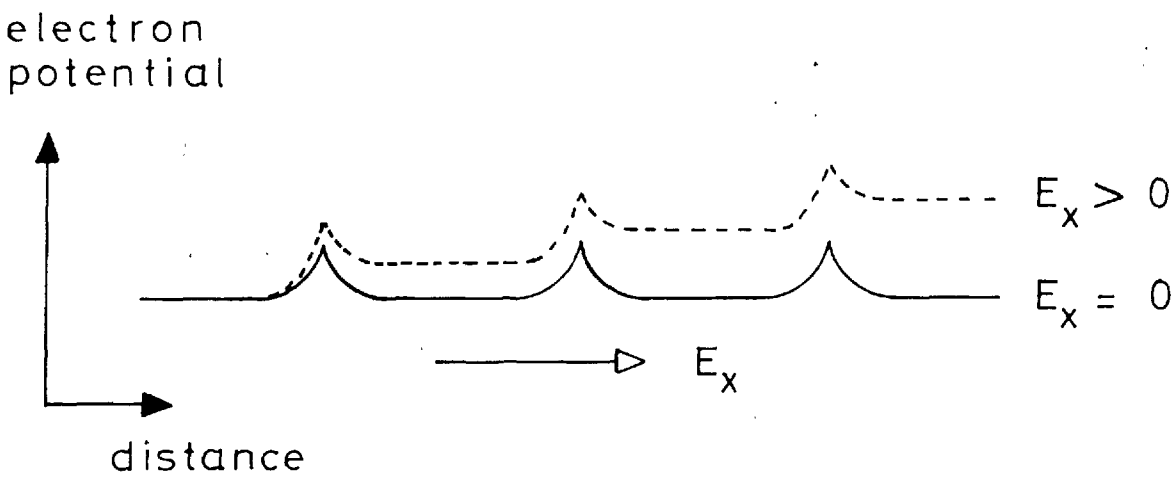

Figure 51

Potential distribution along polycrystal in absence and presence of an applied field

figure (50) leading to an overall potential distribution along the film as shown in figure (51).

Because of the assumed disparity between the grain and barrier resistances essentially all the applied voltage appears across the barriers and the externally measured conductivity is dominated by them.

By means of the classical diode theory (T7) the current-voltage relationship for such a barrier can be shown to be of the form

$$I = AV \exp - \frac{q\phi}{k_o T}$$

leading to $$\mu_H = B \exp - \frac{q\phi}{k_o T} \qquad (45)$$

where ϕ is the barrier height.

(ii) The grain boundary as a defect - Whereas the barrier model localizes the grain boundary interaction to the exclusion of all other processes, the dislocation lines comprising the grain boundary are in this treatment assumed uniformly distributed through the film so that in accord with the usual assumptions*

$$\frac{1}{\mu} = \frac{1}{\mu_l} + A_i T^{-3/2} + A_d T^{-1} \qquad (46)$$

where the first term on the right accounts for the effect of the lattice phonons, the second the ionized grain boundaries and the last the deformation associated with these boundaries (D6). Equation (46) indicates that at low temperatures the mobility will vary as T^x where

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* Derived from the addition of reciprocal relaxation times this relationship assumes mutual independence of the scattering processes together with similar variations of their respective relaxation times with energy. (J5, page 114 of S19, section 13c of B14)

$$1.0 < x < 1.5$$

whereas at higher temperatures it will pass through a maximum to approach asymptotically the pure bulk behaviour with its associated negative temperature coefficient.

Experimentally determined Hall mobilities in polycrystalline semiconductors have been observed both to vary exponentially (W5, Z5) and as a power law (M10) with temperature substantiating to some extent both models. The reason for these different forms of behaviour is not, at present, understood.

As can be seen from figure (35) and equation (46), in the present work a better fit is obtained with the second model although as was stated in section 6.2.2, irreproducibility between samples makes such a conclusion tentative.

An alternative factor to the dominance of lattice scattering and one which has not apparently been discussed in the literature to date (W9, C1), can account for the often observed drop in Hall mobility at higher temperatures.

As was shown in section 5.3, the two carrier expression for Hall mobility is

$$\mu_H = \frac{r\,(p\mu_p^2 - n\mu_n^2)}{(p\mu_p + n\mu_n)}$$

which reduces for intrinsic material to

$$\mu_H = r\,(\mu_p - \mu_n)$$

Thus at high temperatures where the intrinsic conductivity begins to dominate, and we may take $p = n$, the Hall mobility will indicate the difference of the individual carrier conductivity mobilities and for this reason alone might

be expected to fall in value.

Knowledge of the mobility ratio would still enable the values of μ_n and μ_p to be extracted from the measured mobility in this range but in the case of polycrystalline layers the value of this ratio is debatable.

7.5.1 The Mobility Ratio

The field effect method was discounted in section 4.1 as unsuitable in the case of polycrystals because of the lack of knowledge as to the ratio of electron to hole mobilities in such structures.

The results of Juhasz (J2) on well ordered polycrystalline InSb have indicated a value of 10 for this ratio whereas by extending the results of figure (44) into the inversion régime a value of ~ 2.0 for this same ratio has been obtained in the present study. These figures are in contrast with the bulk value which is generally accepted to be ~ 30 (M6).

From this admittedly limited amount of data it thus appears that in polycrystalline InSb electrons are scattered more effectively than holes and a quite simple treatment indicates that this should perhaps be so.

As we have seen, scattering in polycrystals would seem to be dominated by the grain boundaries and with reference to the band diagram of such a region shown in figure (50) this interaction can be considered as follows:

An electron approaching a barrier with a kinetic energy η will experience initially a retarding field which will slow the electron at the expense of an increase in its potential energy. If $\eta > \emptyset$, where $\emptyset$ is the barrier height, then the electron will have lost an amount of kinetic energy $\emptyset$ on reaching the center of the barrier, which it will recoup on being

accelerated out on the other side by the oppositely directed field.

If, however, $\eta < \emptyset$ then the electron will not penetrate the barrier save for those with energy near $\emptyset$ which will be able to tunnel through.

For holes the situation is somewhat different. They will experience forces oppositely directed to those on the electrons and will in consequence be first accelerated and then retarded by such a potential distribution as is shown in figure (50). The net result of this is that all holes will pass through such a region being relatively unaffected by its presence.

For p-type material, however, following the discussions of sections 2.3.1 and 7.3, the intergrain barriers might be expected to consist of regions of hole depletion. In such a situation the potential distribution will be the inverse of that shown in figure (50) and the exact opposite of the above argument will hold.

Although naive, this model thus suggests that grain boundaries will be more effective in scattering the majority species; the argument relying on the proposal that intergrain states always act to deplete the host material.

7.5.2 Transport of Carriers in the Surface Space Charge Region

The theoretical treatment has been carried out rather extensively (see section 2.6) for carriers drawn into a space charge region on single crystal material where completely diffuse scattering is assumed.

The added problem of polycrystallinity and the actual mechanism by which surface scattering takes place have received very little attention and, as with bulk polycrystalline transport, we will confine ourselves here to a brief qualitative discussion.

Carriers drawn into the surface region of a polycrystal will move

in a structure which is not only dislocated as is the underlying bulk but whose degree of electrical disturbance is also a function of the normal applied field. The barrier height in figure (51) is a function of the carrier density in the grains (see section 2.1) and by changing this carrier density by the application of a normal field the height of the intercrystalline barrier will be affected (M11, W5), this being in addition to the scattering effects of the surface itself which were discussed in section 2.6. The sign of this effect will be such as to decrease the barrier height and hence increase the mobility in enhancement layers. At some point however the increased interaction with the surface will offset this effect leading to a maximum in the surface mobility.

Although not observed in the present work Waxman (W5) and Juhasz (J2) have reported such behaviour although in the latter case an alternative explanation, based on the results of the degenerate surface analysis, was proposed.

Concerning the mechanism of surface scattering a possible explanation, suggested by Frankl (F2), is that a diffuse scattering event corresponds to the random emission of a carrier from a surface trap promoted by an incident carrier which itself subsequently becomes trapped. This would then lead to the expectation that surface specularity is accompanied by a low density of surface states and vice versa.

Although there is very little experimental evidence to substantiate this proposal it should be noted that:

(i) The surfaces of the lead salts are thought to scatter specularly (B12) and also to support a small surface state density (E2).

(ii) The present large change in surface mobility (figure (44)) is accompanied by a relatively large surface state density (figure (42)).

In addition of course if this suggestion is correct, then the variation of diffuseness with surface potential will bear some relation to the distribution of surface states present.

7.6 Conclusions

From the results of a high frequency differential capacitance measurement it has proved possible to evaluate the surface state distributions across the entire band gaps of both polycrystalline InSb and PbTe when in contact with anodically formed Al_2O_3.

These distributions, which are qualitatively similar on both materials, show a minimum near mid-gap and a sharp rise towards each band edge and indicate that the quiescent condition for both surfaces is such that the Fermi level at the surface passes practically through the middle of the band gap, in the absence of an externally applied field.

Because the density of trapped surface charge is larger than that in the bulk it seems likely that the intrinsic behaviour exhibited by the PbTe Hall data is a result of compensation of the bulk states by traps at the surface.

The application of these materials to a field effect transistor has been successfully accomplished and useful characteristics have been demonstrated. However, the large surface state density, leading to its intrinsic type behaviour and hence high temperature sensitivity, indicate that PbTe in this respect offers little hope of commercial success; the InSb being quite temperature insensitive appears much more suitable.

The device structure chosen was such as to enable device characteristics and surface properties to be determined by the aforementioned technique on the same sample, rather than requiring extrapolation of the data obtained on one structure to the device itself.

Initial fabrication difficulties were traced to poor channel contacts, perhaps due to an oxide of aluminium forming between the semiconductor and the Al proper. In and Sn were found to be much more suitable and this practical demonstration of the critical effect of this aspect of device fabrication was subsequently verified theoretically.

The surface results together with the successful fabrication of a PbTe FET are new. No reports have previously appeared of the surface state distribution on any polycrystalline material. Neither have they been measured on any form of PbTe.

The differential capacitance method has previously been applied to Ge (B13), Si (L6), GaAs (H7), CdS (I1), CdSe (I1), and InSb (C4, C6) although only in the case of Si and Ge was a rigorous analysis of the results carried out. The present work extends this powerful technique both experimentally and theoretically to the study of the narrow band gap material PbTe and also to the polycrystalline thin film form of InSb.

It is to be hoped that future work on surface structure will be directed towards a correlation of theory with experiment leading to some degree of control over the parameter 'surface state density'. Until that time however it appears that low state densities, with their associated promise of high field effect mobilities and stability of performance, will only be found by the necessarily slow technique of trial and error as is evidenced by the singular success of Si after some 40 years of experimental investigation.

APPENDIX A

The Theoretical Analysis of the Surface Space Charge Region

The first treatment of the surface space charge region was carried out by Kingston & Neustadter (K8) in 1955. Their analysis was based on the simplifying assumptions of non degenerate carrier distributions and parabolic bands.

This work was subsequently extended by Seiwatz & Green (S13) to include the effects of carrier degeneracy and partial impurity ionization and more recently Juhasz (J2) has included a first order correction to account for non-parabolicity.

The analysis to be presented here includes the effects of non-parabolicity, partial impurity ionization and degeneracy of the carrier populations. It is an extension of the earlier treatments to include the expressions for differential surface capacitance of relevance to the present work.

Definitions

We assume a semi-infinite, isotropic, homogeneous semiconductor having no surface states, to the surface of which is applied a normal electric field.

For thermal equilibrium the surface energy distribution is as shown in figure A.1. The z axis being taken normal to the surface as shown, electron energy E_o being measured upwards.

Referring to this figure:

E_c represents the conduction band edge

E_v represents the valence band edge

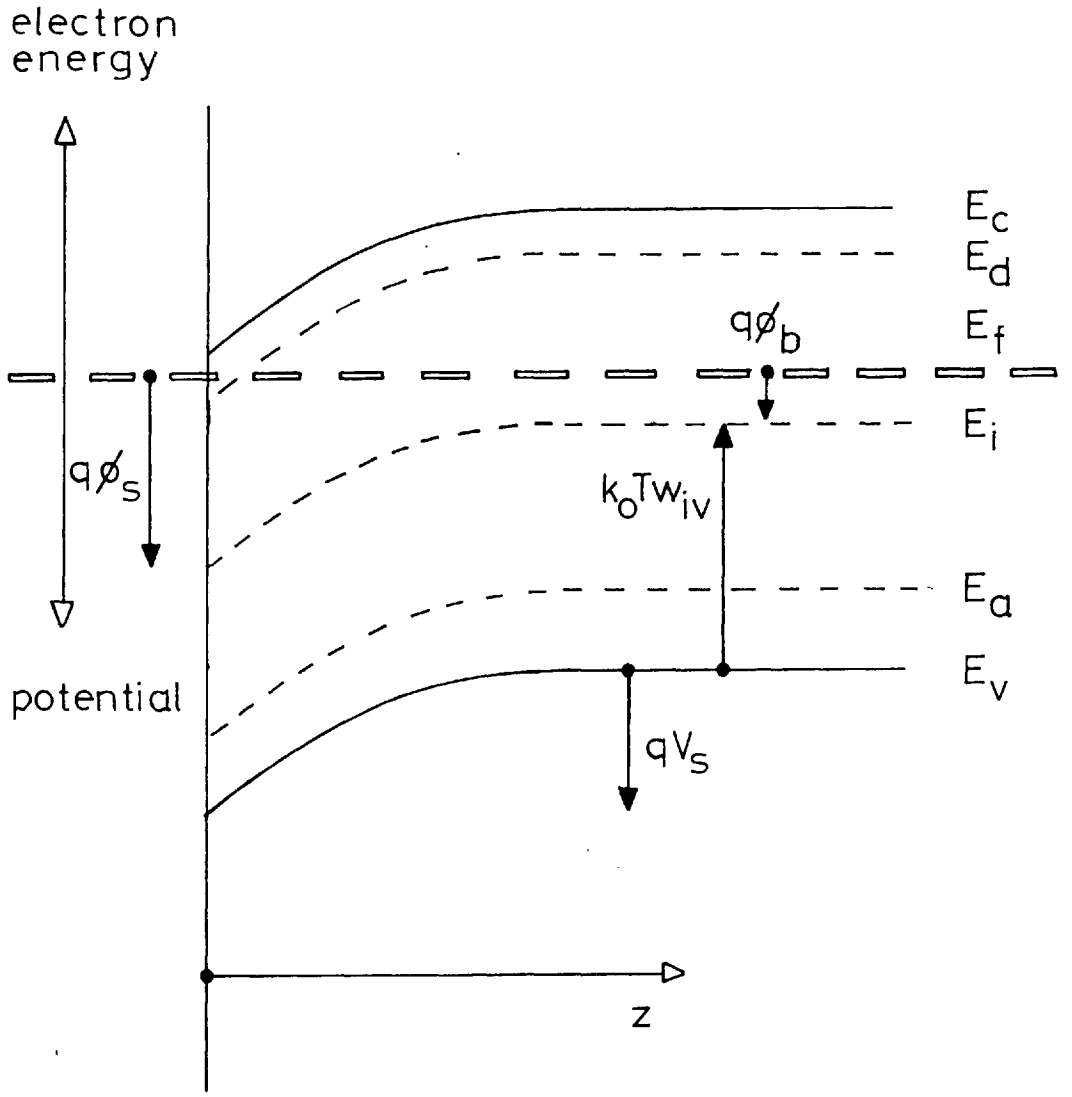


Figure A1

Band model of the surface region of an n-type semiconductor in the presence of a negative surface space charge

E_f is the Fermi level which is constant throughout the system at thermal equilibrium i.e. no net current flow normal to the surface.

E_i is drawn parallel with the band edges to coincide in the bulk with the intrinsic value of Fermi energy.

We define parameters η, ϕ, u, v, w by

$$\eta = E_o/k_oT$$

$$q\phi = (E_f - E_i)$$

$$u = \frac{q\phi}{k_oT} = \eta_f - \eta_i$$

$$v = (u - u_b) = (\eta_{ib} - \eta_i)$$

and $$w_{pq} = \frac{E_p - E_q}{k_oT} = (\eta_p - \eta_q)$$

ϕ, u and v are functions of z but w_{pq}, as defined, refers to the separation of the energy levels p and q well away from the surface.

The subscript b is used to denote values remote from the surface and s is used for values at the surface.

It should be noted that:

u_s is zero for an intrinsic surface

and v_s is zero at flat band i.e. in the absence of a surface space charge.

u_s and v_s are both positive for increasing electron concentrations at the surface which on a band diagram is represented by further downward band bending.

Density of States

For a carrier band of arbitrary shape save for the maintenance of symmetry about the extremum at k = 0 we may write

$$E_o = Ak^2 + Bk^4 + Ck^6 + \ldots\ldots\ldots\ldots\ldots \qquad A.1$$

where k is the electron wave vector and the energy E_o is measured positive into the band from the band edge.

Alternatively the E_o- k relationship may be written:

$$Ak^2 = E_o + aE_o^2 + bE_o^4 + \ldots\ldots\ldots\ldots\ldots \qquad A.2$$

Near the band extremum for $E \longrightarrow 0$ equation A.2 must reduce to the standard parabolic form

$$E_o = \frac{\hbar^2 k^2}{2m^*}$$

where $\hbar$ is the reduced form of Planck's constant and m* is the carrier effective mass appropriate to the band edge

$$\therefore \quad \frac{\hbar^2 k^2}{2m^*} = E_o + aE_o^2 + bE_o^4 + \ldots\ldots\ldots\ldots \qquad A.3$$

Taking only the first two terms on the R.H.S. i.e. first order correction for non-parabolicity, Ehrenrich (E1) has shown that A.3 may be re-written

$$\frac{\hbar^2 k^2}{2m^*} = E_o + \frac{E_o^2}{E_{gp}} \qquad A.4$$

where E_{gp} is the so called 'density of states' band gap.

Now in general the density of electron states $g(E_o)$ is given by (S19)

$$g(E_o)\, dE_o = \frac{k^2}{\pi^2}\, dk \qquad A.5$$

where each energy level can be occupied by only one electron.

From A.4 $\quad k^2 = \frac{2m^*}{\hbar^2}\left(E_o + \frac{E_o^2}{E_{gp}}\right)$

and $\quad dk = \frac{m^*}{\hbar^2 k}\left(1 + \frac{2E_o}{E_{gp}}\right) dE_o$

using these relationships in A.5 gives

$$g(E_o)\, dE_o = 4\pi\left(\frac{2m^*}{h^2}\right)^{3/2}\left(1 + \frac{2E_o}{E_{gp}}\right)\left[1 + \frac{E_o}{E_{gp}}\right]^{\frac{1}{2}} E_o^{\frac{1}{2}}\, dE_o \qquad \text{A.6}$$

Expanding the square root term in a Taylor series and taking the first two terms leads to

$$g(E_o)\, dE_o = 4\pi\left(\frac{2m^*}{h^2}\right)^{3/2}\left[1 + \frac{5}{2}\frac{E_o}{E_{gp}}\right] E_o^{\frac{1}{2}}\, dE_o \qquad \text{A.7}$$

or in reduced energy units

$$g(\eta)\, d\eta = 4\pi\left(\frac{2m^* k_o T}{h^2}\right)^{3/2}\left[1 + \frac{5}{2}\frac{k_o T}{E_{gp}}\eta\right]\eta^{\frac{1}{2}}\, d\eta \qquad \text{A.8}$$

i.e. $g_{v,c}(\eta) = \alpha\left(A_{v,c}\,\eta^{\frac{1}{2}} + B_{v,c}\,\eta^{3/2}\right)$ A.9

where $\alpha = 4\pi\left[\frac{2m_o k_o T}{h^2}\right]^{3/2}$, m_o = electron mass

$$A = \left(\frac{m^*}{m_o}\right)^{3/2}$$

and $\quad B = \frac{5}{2}\frac{k_o T}{E_{gp}} \cdot A$

For B = 0 equation A.8 reduces to that appropriate to a parabolic band,

namely $g(\eta) = 4\pi\left(\frac{2m^* k_o T}{h^2}\right)^{3/2}\eta^{\frac{1}{2}}$

The subscripts c and v in equation A.9 refer to the values appropriate to the conduction and valence bands respectively.

The Field Equation

The number of electrons/unit volume in the conduction band is given by the integral over the conduction band of the product of the electron distribution function and the density of states i.e.

$$n_c(z) = \int_0^\infty \frac{g_c(\eta)}{1 + \exp(\eta + w_{cf} - v(z))}\, d\eta \qquad \text{A.10}$$

Similarly for holes in the valence band

$$p_v(z) = \int_0^\infty \frac{g_v(\eta)}{1 + \exp(\eta + w_{fv} + v(z))}\, d\eta \qquad \text{A.11}$$

If we denote the Fermi integral $\int_0^\infty \frac{x^r}{1 + \exp(x - \beta)}\, dx$

by $F_r(\beta)$ then A.10 becomes

$$n_c(z) = \alpha\left[A_c F_{\frac{1}{2}}(v - w_{cf}) + B_c F_{\frac{3}{2}}(v - w_{cf})\right] \qquad \text{A.12}$$

and from A.11

$$p_v(z) = \left[A_v F_{\frac{1}{2}}(- v - w_{fv}) + B_v F_{\frac{3}{2}}(- v - w_{fv})\right]\alpha \qquad \text{A.13}$$

where $g(\eta)$ has been substituted for from A.9.

For N_d donor impurities situated at an energy η_d a fraction

$$\left[1 + \tfrac{1}{2}\exp(w_{df} - v)\right]^{-1} \qquad \text{A.14}$$

will be full of electrons and hence the positive charge density associated with these donors is given by

$$\rho_d = qN_d\left[1 - (1 + \tfrac{1}{2}\exp(w_{df} - v))^{-1}\right]$$

$$= qN_d\left[1 + 2\exp(v - w_{df})\right]^{-1} \qquad \text{A.15}$$

The negative charge density associated with N_a acceptors located at an energy η_a is similarly given by

$$\rho_a = qN_a \left[1 + 2 \exp(- w_{fa} - v) \right]^{-1} \qquad \text{A.16}$$

The factor of $\frac{1}{2}$ which appears in the Fermi function of equation A.14 can be understood from the following:

In general an impurity center can capture more than one electron and in each condition of charge there can be several energy levels associated with it. In addition to this each state may be degenerate such as when the center can capture two electrons, one of either spin.

For the simple case of a center which has only one possible energy associated with each of its two possible conditions of charge, and which exhibits g_o and g_1 degenerate states when empty and when occupied by an electron respectively, Shockley and Last (S17) have shown, by maximizing the occupation probability of the various possible states that the center will exhibit an effective energy given by

$$E_t^f = E_t + k_o T \ln \left(\frac{g_o}{g_1}\right) \qquad \text{A.17}$$

where E_t is its energy when unoccupied.

Its probability of occupation is given by the Fermi function viz:

$$f\left(E_t^f\right) = \left[1 + \exp\left(\frac{E_t^f - E_f}{k_o T}\right) \right]^{-1}$$

$$\text{which from A.17} = \left[1 + \frac{g_o}{g_1} \exp\left(\frac{E_t - E_f}{k_o T}\right) \right]^{-1} \qquad \text{A.18}$$

Because of its possibility of accepting an electron of either spin $g_1 = 2$ and $g_o = 1$ for donors and under these conditions A.18 leads to equation A.14.

The total net charge density at any value of z is given by

$$\rho(z) = q(p_v(z) - n_c(z) + \frac{(\rho_d - \rho_a)}{q}) \qquad A.19$$

and the potential distribution in the space charge region, satisfying Poisson's equation, is given by

$$\frac{d^2V}{dz^2} = -\frac{\rho(z)}{\epsilon\epsilon_o}$$

$$\therefore \frac{d^2v}{dz^2} = -\frac{1}{2L_o^2}\left[\frac{N_d}{\alpha}\left[1 + 2\exp(v - w_{df})\right]^{-1} - \frac{N_a}{\alpha}\left[1 + 2\exp(-w_{fa} - v)\right]^{-1}\right.$$

$$+ A_v F_{\frac{1}{2}}(-v - w_{fv}) + B_v F_{\frac{3}{2}}(-v - w_{fv})$$

$$\left. - A_c F_{\frac{1}{2}}(v - w_{cf}) - B_c F_{\frac{3}{2}}(v - w_{cf})\right] \qquad A.20$$

$$\text{where } L_o = \left[\frac{\epsilon\epsilon_o k_o T}{2q^2\alpha}\right]^{\frac{1}{2}}$$

Solution of the Field Equation

If equation A.20 is multiplied throughout by $\frac{dv}{dz}$ and integrated from $z = \infty$, then the L.H.S. becomes equal to $\frac{1}{2}(\frac{dv}{dz})^2$ as $\frac{dv}{dz} = 0$ in the bulk. A.21

The first two terms on the R.H.S. are readily integrated using the relation

$$\int\left[1 + 2\exp(\mp x + y)\right]^{-1} dx = \ln\left[1 + \tfrac{1}{2}\exp(\pm x - y)\right] \qquad A.22$$

whereas the Fermi integrals are related by (M5)

$$r\,F_{r-1}(\beta) = \frac{dF_r(\beta)}{d\beta} \qquad A.23$$

Using the relationships given by equations A.21, A.22 and A.23 it can be shown that integration of A.19 leads to

$$\left[\frac{dv}{dz}\right]^2 = \pm \frac{1}{L_o^2}\left[\frac{N_d}{\alpha} \ln\left[\frac{1 + \frac{1}{2}\exp(w_{df} - v)}{1 + \frac{1}{2}\exp(w_{df})}\right] + \frac{N_a}{\alpha} \ln\left[\frac{1 + \frac{1}{2}\exp(w_{fa} + v)}{1 + \frac{1}{2}\exp(w_{fa})}\right]\right.$$

$$+ \frac{2}{3} A_v \left[F_{\frac{3}{2}}(-v - w_{fv}) - F_{\frac{3}{2}}(-w_{fv})\right]$$

$$+ \frac{2}{5} B_v \left[F_{\frac{5}{2}}(-v - w_{fv}) - F_{\frac{5}{2}}(-w_{fv})\right]$$

$$+ \frac{2}{3} A_c \left[F_{\frac{3}{2}}(v - w_{cf}) - F_{\frac{3}{2}}(-w_{cf})\right]$$

$$\left. + \frac{2}{5} B_c \left[F_{\frac{5}{2}}(v - w_{cf}) - F_{\frac{5}{2}}(-w_{cf})\right]\right] \qquad \text{A.24}$$

This equation reduces to equation (25) of reference S13 for $B_v = B_c = 0$ i.e. the parabolic case.

We may write

$$\frac{dv}{dz} = \pm \frac{F(v)}{L_o}$$

where F(v) is called the 'F function' and is for the degenerate, non-parabolic case given by the square root of the bracketed term on the R.H.S. of equation A.24.

Surface Space Charge

The surface space charge/unit area of surface is given by Gauss' law as equal to the electric flux density at the surface, i.e.

$$Q_{sc} = -\epsilon\epsilon_o E_s = \epsilon\epsilon_o \frac{dv}{dz}\bigg|_s = \frac{\epsilon\epsilon_o k_o T}{q} \frac{dv}{dz}\bigg|_s$$

$$\therefore \quad Q_{sc} = \pm \frac{\epsilon \epsilon_o k_o T}{q L_o} F(v_s) \qquad \text{A.25}$$

Surface Excesses

The electron and hole contributions to the space charge, measured relative to flat band are given / unit area by

$$\Delta N = \int_{z=o}^{z=\infty} (n_c(z) - n_c(\infty)) \, dz$$

$$= L_o \int_{v=o}^{v=v_s} \frac{1}{F(v)} (n_c(z) - n_c(\infty)) \, dv \qquad \text{A.26}$$

which gives, by substituting for n_c from A.12

$$\Delta N = \alpha L_o \int_{v=o}^{v=v_s} \frac{1}{F(v)} \left[A_c \left[F_{\frac{1}{2}}(v - w_{cf}) - F_{\frac{1}{2}}(- w_{cf}) \right] + B_c \left[F_{\frac{3}{2}}(v - w_{cf}) - F_{\frac{3}{2}}(- w_{cf}) \right] \right] dv \qquad \text{A.27}$$

similarly for holes

$$\Delta P = \int_{z=o}^{z=\infty} (p_v(z) - p_v(\infty)) \, dz$$

$$= \alpha L_o \int_{v=o}^{v=v_s} \frac{1}{F(v)} \left[A_v \left[F_{\frac{1}{2}}(- v - w_{fv}) - F_{\frac{1}{2}}(- w_{fv}) \right] + B_v \left[F_{\frac{3}{2}}(- v - w_{fv}) - F_{\frac{3}{2}}(- w_{fv}) \right] \right] dv \qquad \text{A.28}$$

Differential Surface Capacitance

It has been shown that

$$Q_{sc} = \pm \frac{\epsilon \epsilon_o k_o T}{q L_o} F(v_s) \qquad \text{A.25}$$

Now $C_{sc}(v_s) = \frac{dQ_{sc}}{dV_s} = \frac{q}{k_o T} \frac{dQ_{sc}}{dv_s}$

i.e. $C_{sc}(v_s) = \pm \frac{\epsilon \epsilon_o}{L_o} \frac{dF(v_s)}{dv_s}$ A.29

$\frac{dF(v_s)}{dv_s}$ is obtained by differentiation of A.24 and leads to the expression for C_{sc} viz:

$$C_{sc}(v_s) = \frac{\epsilon \epsilon_o}{2 L_o F(v_s)} \left[\frac{N_a}{\alpha} \left[1+2 \exp(-v_s - w_{fa}) \right]^{-1} - \frac{N_d}{\alpha} \left[1+2 \exp(v_s - w_{df}) \right]^{-1} \right.$$

$$- A_v . F_{\frac{1}{2}} (-v_s - w_{fv}) - B_v . F_{\frac{3}{2}} (-v_s - w_{fv})$$

$$\left. + A_c . F_{\frac{1}{2}} (v_s - w_{cf}) + B_c . F_{\frac{3}{2}} (v_s - w_{cf}) \right] \qquad \text{A.30}$$

For a given material at a fixed value of surface potential the differential surface capacitance is solely a function of doping, i.e. N_a and N_d. This is used to advantage in the differential capacitance method of surface analysis as a unique relationship exists between the minimum value of C_{sc} and doping density. This enables the effective doping in the space charge region to be determined once the relationship has been evaluated.

Taking the derivative with respect to v_s of equation A.30 and equating to zero, following some algebra, leads to

$$C_{sc}\Big|_{min} = \frac{\epsilon \epsilon_o}{L_o \sqrt{2}} \cdot F_o \qquad \text{A.31}$$

$$\text{where } F_o = \left[\frac{N_a}{\propto} \left[\frac{2 \exp(-v_s - w_{fa})}{(1 + 2 \exp(-v_s - w_{fa}))^2} \right] + \frac{N_d}{\propto} \left[\frac{2 \exp(v_s - w_{df})}{(1 + 2 \exp(v_s - w_{df}))^2} \right] \right.$$

$$- \tfrac{1}{2} A_v . F_{-\frac{1}{2}} (-v_s - w_{fv}) - \tfrac{3}{2} B_v . F_{\frac{1}{2}} (-v_s - w_{fv})$$

$$\left. + \tfrac{1}{2} A_c . F_{-\frac{1}{2}} (v_s - w_{cf}) + \tfrac{3}{2} B_c . F_{\frac{1}{2}} (v_s - w_{cf}) \right] \qquad \text{A.32}$$

and is evaluated for v_s corresponding to the capacitance minimum.

An iterative technique can be employed to evaluate $C_{sc}\Big|_{min}$ from equations A.31 and A.32 but a shorter method is to evaluate it by inspection of the C_{sc} versus v_s relation as obtained from equation A.30.

APPENDIX B

The Differential Capacitance Measuring Circuit

The circuit employed in the present study, which has been schematically outlined in section 5.4, is shown in figure (B1).

A signal with an amplitude of ~ 20 mV is required at the device and because of the circuit condition

$$R \gg (w\, C_t)^{-1}$$

it is necessary that the high frequency signal generator should be capable, at the frequency of interest, of supplying a voltage of ~ 8 volts p-p.

C_t in the present study was typically ~ 2000 pF requiring at 1 Mc/s a value of R of ~ 12 KΩ. A lower limit on the value of capacitance which may be measured with this circuit is set by the necessity of satisfying the condition

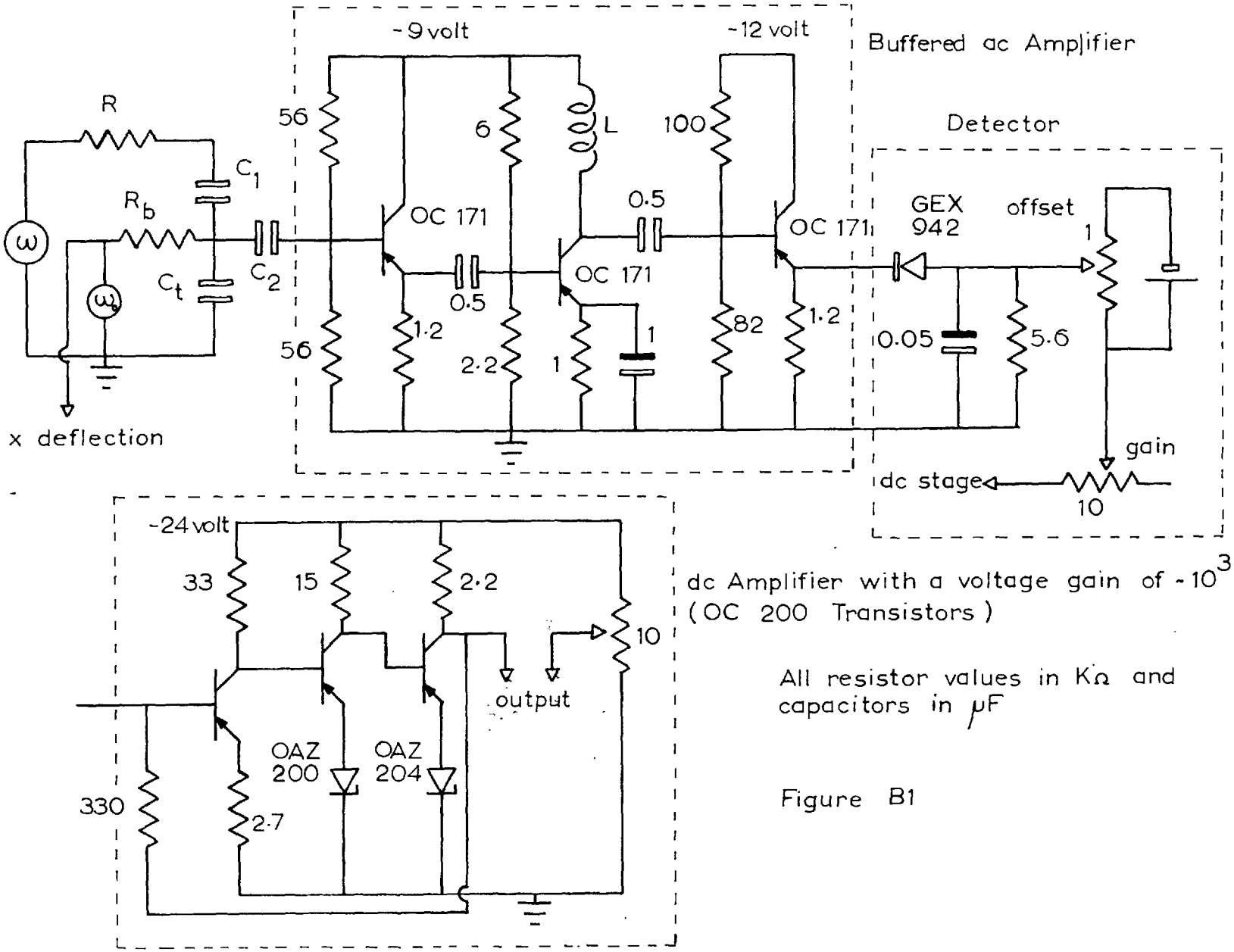
$$(w\, C_t)^{-1} \ll |Z_{in}|_w$$

The inductor L is chosen to maximise the stage gain at the frequency of measurement and in the present case, at 1 Mc/s, must have a value of ~ 150 μH.

The upper frequency limit with this circuit occurs at ~ 5 Mc/s if care is taken with circuit layout. The limit on detection, set by circuit noise, corresponds to an estimated change in C_t of ~ 0.1%.

The use of the simple diode detector employed here is reasonable for overall capacitance changes of $\lesssim$ 30%. For larger variations non-linearity of the detector characteristics may prove excessive but in the present work this problem did not arise (chapter VI).

The device, which was maintained at a low temperature in a liquid nitrogen cooled cryostat, is coupled into the system via coaxial leads; these being kept as short as possible to minimise spurious effects.



dc Amplifier with a voltage gain of -10^3
(OC 200 Transistors)

All resistor values in KΩ and capacitors in μF

Figure B1

APPENDIX C

Computer Program (written in Fortran IV)

DATA REQUIRED

Dielectric capacitance/unit area C_{ox}
Semiconductor permittivity ϵ
Band gap E_g
Doping densities N_a and N_d
Dopant energy levels E_a and E_d
Temperature T in ^oK
Hole and electron effective masses m_h and m_e
Band parameters A and B

In addition the range of surface potential and potential increments required must be stated.

COMPUTATION

In the semiconductor bulk the charge density is zero and the charge neutrality equation which must be satisfied is:
(from equation A19)

$$\frac{N_d}{\alpha}\left[1 + 2\exp(\eta_f - \eta_d)\right]^{-1} - \frac{N_a}{\alpha}\left[1 + 2\exp(\eta_a - \eta_f)\right]^{-1}$$

$$+ A_v . F_{\frac{1}{2}}(\eta_v - \eta_f) + B_v . F_{\frac{3}{2}}(\eta_v - \eta_f)$$

$$- A_c . F_{\frac{1}{2}}(\eta_f - \eta_c) - B_c . F_{\frac{3}{2}}(\eta_f - \eta_c) = 0$$

By varying η_f this equation is solved iteratively for $N_d = N_a = 0$ to give η_{ib}, and with doping densities included to give η_{fb}.

Knowing these two energy levels the bulk carrier densities and intrinsic carrier density can be evaluated using equations A.12 and A.13. The carrier excesses/unit area of surface are then calculated from equations A.27 and A.28 by numerical integration. The integration is begun at the specified value of surface potential and continued until v approaches zero

The differential surface capacitance and total surface space charge/unit area follow directly from equations A.30 and A.25 respectively.

Although these computations are quite straightforward the length of the process can be appreciated when it is considered that each increment in the integrand of equation A.27 for example involves the evaluation of the F function from equation A.24 where each of the Fermi integrals within these equations is itself an integral*. This has then to be repeated for each value of v to complete the evaluation of ΔN for each value of surface potential.

PRINT OUT

The information calculated is:

Intrinsic Fermi energy
Intrinsic carrier density
Extrinsic Fermi energy
Bulk electron density
Bulk hole density

and for each specified value of surface potential

Surface space charge/unit area
Electron excess/unit area
Hole excess/unit area
Differential surface capacitance/unit area
C_t/unit area for the specified values of C_{ox}

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* Although series expansions of the Fermi integrals have been presented by McDougall and Stoner (M5) it proved advantageous in the present case to compute their values by numerical integration.

APPENDIX D

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pp. 189-190

On the Error Associated with the MIS Method of Capacitance Measurement of Surface State Density

Abstract—**The inherent error associated with the deduction of surface capacitance from measured MIS capacitance is considered. It is shown that the systematic component of the experimental error does not restrict the range of application of the technique whereas any random contribution can invalidate the measurement in certain cases.**

Surface transport[1] in semiconductors has, in recent years, received ever increasing attention mainly as a result of its importance to device physics. Both the MOST[2] and thin-film FET[3] depend for their action upon the free transport of carriers along a semiconductor-dielectric interface and for device optimization a knowledge of the electrical parameters of this interface is essential.

One means by which this information may be obtained requires a measurement of the differential capacitance associated with the semiconductor surface space-charge layer as the surface potential is varied. This technique, termed the MIS capacitance method,[4] allows an estimate of surface state density and frequency response to be made. Coupled with a field-effect measurement it also leads to information on surface mobility and hence allows deductions to be made as to the specularity of the interface.

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In practice it is not possible to make contact to the interface directly and instead the series combination of the surface capacitance and the geometric dielectric capacitance is measured.

From this measured capacitance C it is then necessary to calculate the surface capacitance C_s using

$$C_n = C_s/(C_s + C_{ox}) \tag{1}$$

where C_{ox} is the dielectric capacitance and

$$C_n = \frac{C}{C_{ox}}.$$

Taking the partial derivatives of (1), viz.,

$$\frac{\partial C_n}{\partial C_s} \quad \text{and} \quad \frac{\partial C_n}{\partial C_{nx}},$$

leads to the complete differential of C_n

$$dC_n = \frac{1}{(C_s + C_{ox})^2}\left[C_{ox}dC_s - C_s dC_{ox}\right]$$

which when rearranged in terms of C_n gives

$$\frac{dC_s}{C_s} = \frac{dC_{ox}}{C_{ox}} + \frac{1}{(1 - C_n)}\frac{dC_n}{C_n}. \tag{2}$$

As in general $C_{ox} \ll C_s$, $C_n \sim 1$ and the coefficient of the last term in (2) is very large, implying a large error in deducing C_s from C_n and C_{ox}. However, C_n is a quotient of two measured capacitance values and hence the error in its measurement, viz., dC_n/C_n is given by

$$\frac{dC_n}{C_n} = \frac{dC}{C} - \frac{dC_{ox}}{C_{ox}}. \tag{3}$$

Substitution of (3) in (2) gives

$$\frac{dC_s}{C_s} = \frac{1}{(1 - C_n)}\frac{dC}{C} - \frac{C_n}{(1 - C_n)}\frac{dC_{ox}}{C_{ox}}. \tag{4}$$

If we now neglect personal errors and assume the method of measurement to be limited by systematic errors we may, for $C_n \sim 1$, write

$$dC \cong dC_{ox},$$

i.e.,

$$\frac{dC_s}{C_s} = (1 + C_n)\frac{dC}{C}. \tag{5}$$

Hence the relative error in deducing C_s from C can never exceed twice the error set by the method of measurement however small the deviation of C from the oxide capacitance C_{ox}.

It should be appreciated, however, that for a measurement dominated by random errors then

$$\frac{dC_s}{C_s} \to \infty \text{ as } C_n \to 1.$$

The result as given by (5) should be contrasted with that of Zaininger and Warfield [5, equations (22)–(24)] where it is concluded, incorrectly, that the error is given by

$$\frac{dC_s}{C_s} = -\frac{dC_{ox}}{C_{ox}} + \frac{1}{(1 - C_n)}\frac{dC}{C}$$

which leads for $dC_{ox} \cong dC$ to

$$\frac{dC_s}{C_s} = \left[\frac{C_n}{1 - C_n}\right]\frac{dC}{C}. \tag{6}$$

From (6) it can be seen that the error diverges rapidly for $C_n \to 1$ and it is concluded that it becomes meaningless to investigate that region of the surface corresponding to $0.8 < C_n < 1.0$. This is not a severe limitation on the method when applied to such large-bandgap materials as Si in the highly developed Si/SiO_2 system[6] but in narrow-bandgap semiconductors, especially in polycrystalline thin-film form, the carrier concentration can be so high as to confine C_n to the "forbidden range" for all values of surface potential.

The correct result, as given in (5), thus has particular relevance to studies on thin-film surfaces.

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