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THE ANALOGUE AND DIGITAL CONTROL OF HIGH VOLTAGE D.C. TRANSMISSION SYSTEMS UNDER FAULT CONDITIONS

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ABSTRACT

H.V.D.C. transmission is now established for point to point high power transmission over long distances. The extension of d.c. techniques to more complex system inter-connections is predicated on cheaper terminal equipment, the feasibility of the multiterminal connection and the development of d.c. circuit breakers or other fault control methods. In the work described here an h.v.d.c. simulator has been used in conjunction with a process control type computer to investigate the control and behaviour of multiterminal h.v.d.c. systems under fault conditions.

The simulator in the Imperial College Power Systems Laboratory was equipped with reliable thyristor pulsing units and a complete set of converter controls. These controls included an entirely new method of c.e.a. control having many advantages over the conventional 'consecutive control' techniques. A three terminal teed system was successfully operated.

A PDP.8 computer programmed to function as a central fault controller was linked through D/A and direct-digital channels to the simulator; a group of electronic fault control circuits was installed at each converter terminal. The study has, in the main, been confined to d.c. transmission network and converter faults. The purpose of the central fault control is to obtain good fault discrimination ensuring minimum outage subsequent to fault. The programme is adaptive in that control is ensured as the network configuration alters subsequent to fault isolation. Results of the fault control tests on the simulator are included.

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List of Principal Symbols.

A	Amplifier gain constant.
$A(s)$	Amplifier operational transfer function
$A_{1,2\,...}$	Logic information from RE to central controller.
$B_{1,2\,...}$	Logic information from IN1 to central controller.
$C_{1,2\,...}$	Logic information from IN2 to central controller.
C	Capacitance.
$e_{1,2\,...}$	Voltage signals.
f	Frequency.
F_y^x	Logic fault indication between conductors x and y
G	Amplifier gain.
H	Inertia constant.
I, $I_{1,2\,...}$	Current (a.c. or d.c.)
I_d	d.c. current.
i_c	Commutation loop circulating current.
IN1, IN2	Inverter designations
$k_{1,2\,...}$	Amplifier gain constants.
L, l	Inductance.
L_c	Commutating inductance/phase
Lx, y	Choke inductance.
$M_{1,2\,...}$	Logic information from node to central controller.
n	Harmonic order
	number of bridges per converter
	pulse number.
P	Power flow
R	Resistance
R_G	Inverter apparent negative resistance
r_t	Commutating loop resistance/phase

RE	Rectifier designation.
R_{sc}	C.C. control slope resistance.
S, s	Laplace operator.
$T_{1,2\ldots}$	Amplifier time constants.
u	Commutation overlap angle.
v	velocity of propogation
V_{do}	Converter d.c. voltage at zero delay ang.
$v_{r,y,b.}$	Phase to neutral voltages.
v_{dc}	Instantaneous d.c. voltage.
V_L	a.c. r.m.s. line volts.
V_m	Peak a.c. voltage.
V_{th}	Thyristor drop.
X	Reactance
X_c	Commutating reactance/phase.
Y(S)	Operational admittance.
z	z - transform operator.
α	Rectifier delay angle
β	Inverter angle of advance
γ	Inverter extinction angle
δ	Prefix to indicate incremental value
$\delta I_{1,2\ldots}$	Current margins
ω	2π x frequency

In the circuit diagrams unless otherwise indicated;

All npn transistors are type 2N2926

All pnp transistors are type 2N3702

All diodes are type OA91

CHAPTER 1

H.V.D.C. in the A.C. Power System

1.1. Preamble

If it is true that the consumption of electricty is a reliable index of the progress of any part of the world it is, dialectically, no less true that the diversification of materials, techniques and processes is the essence of growth. Examples of the related nature of growth and diversification abound in nature and in every aspect of man's culture, while the history of technology has been one of continual diversification.

In the field of Electric Power Engineering high voltage d.c. transmission is becoming established as a reliable method of power transmission with many functions complementary to more conventional a.c. transmission techniques. This renewed interest in d.c. transmission is on the one hand the result of improved techniques, especially the development of the high voltage mercury arc valve, and on the other is a response to certain problems in the a.c. power system. Heavy demands for power have made the transmission of bulk power over long distances unavoidable and here the use of d.c. transmission is no longer novel. Only more recently however has it come to be appreciated that h.v.d.c. can be usefully employed for limiting short-circuit levels on heavily inter-connected a.c. systems, for inter-connecting large geographically dispersed systems, for the supply of massive conurbations and as a method of containing the growth of complex urban distribution systems.

1.2. H.V.D.C. and the British Grid

The decision to construct the 275 kv supergrid in Britain(1) stemmed from the need for much larger inter-connection capacity to meet the increased load and generation and from an awareness that some regions of the country would be permanent areas of power deficit while others have considerable export capability. The 275 kv supergrid was projected to meet these requirements and concurrently new generation was rapidly installed. The philosophy of the 400 kv supergrid[2, 3, 4] while taking over the tasks of inter-connection and bulk power movement introduces a third concept, High Power Distribution, which has largely determined its structure. A large part of the new generation capability in Britain is fairly evenly deployed around the principal load centres and a significant part of the national load is sparsely distributed throughout the country. For these reasons some 20 GW of the estimated 35 GW to be moved in the supergrid will be short distance bulk power transmission. This taken together with the rapid increase of 2 GW stations that must necessarily feed into a widely inter-connected network has dictated that the 400 kv grid function not only as an inter-connector and a bulk power transmitter but also as a supply "main" for local loads.

It can be appreciated from this sketch of the evolution of the grid why d.c. links were never a serious alternative to any part of the a.c. supergrid network. D.C. transmission techniques have not been proved in multiterminal connections and consequently cannot be integrated into a grid, one of whose principal functions is high power distribution.

Further system growth when the 400 kv supergrid is saturated in the 1980's is being studied and h.v.d.c. techniques may be usefully employed. The rapidly rising short circuit level of the supergrid is causing anxiety and when the 35 GVa limit is exceeded either a higher voltage grid will be laid over the present supergrid or the system subdivided and suitably intertied. It is by no means clear that a higher voltage will be required in Britain[3, 5]. Demographic and other studies have indicated that London and the South Eastern load will continue to grow rapidly and will remain a major deficit area. Hence any subdivision of the national grid will need to be supplemented by a few bulk power transfer lines from centres of generation to load. H.V.D.C. can be used both to link together the separate parts of a subdivided network or to function as a bulk transmission line with multiple outlets in the South East.

1.3. Scope for Multi-terminal D.C. in A.C. Grids

For reasons briefly outlined below the British grid does not mirror the future evolution of power systems in other countries. Because a large evenly distributed load is not often encountered outside Europe and because the geographical overlap of the coalfields and industrial regions of England, the heritage of the Industrial Revolution, is not repeated in this classic form elsewhere, high power distribution is not a dominant feature of grid planning in other countries(6). The paucity of hydro resources, the short transmission distances and the maturing of the grid while d.c. transmission was in its infancy are also peculiar to Britain. The main areas of interest in h.v.d.c. in other parts of the world are in system inter-connection, especially in the United States, the U.S.S.R., and the European Continent, and in multiple power feeds to massive conurbations.

The Federal Power Commission of the U.S.Government recommended in 1964(7) that the economics arising from inter-connection and the importance of secure power system operation were overriding motives for the inter-connection of the United States into a single integrated system. Investigations undertaken in connection with the North Eastern blackout of November 9th, 1965, have shown(8) that seventeen of the twenty major failures that occurred since that date have also been cascading failures resulting from inter-connections which were too weak to cope with the disturbance. It can be reasonably anticipated that a strong cohesive countryside e.h.v. grid overlaying the existing h.v. systems, quite apart from a mere strengthening of the present inter-area commercial ties, will be constructed in the U.S. over the next decade. Plans for the inter-connection of the Central part of the United States with North West Pacific coast are also being examined(9). Seasonal and time zone dependant load diversity permits the exchange of 3 GW of power over transmission distances of the order of 2000 miles. The need to inter-connect to and integrate the numerous power networks of the intermediate regions dictates the use of e.h.v. a.c. or multiterminal d.c. Many a.c. and d.c. plans have been considered and more detailed studies are now being undertaken.

The present five year plan of the U.S.S.R. envisages the creation of a single grid for European Russia. Extensive studies for the best use, in this process, of both a.c. and d.c. techniques are under way(10) and no doubt multiterminal h.v.d.c. systems will be considered. Another reason for interest in h.v.d.c. arises from the fact that the bulk of the new fossilfuel deposits and untapped hydro resources of the U.S.S.R. lie in Siberia, Kazakhstan and Central Asia while 75% of the population and industry is concentrated in European Russia. By 1975 these regions will be connected to the centre and to the Urals by two 1500 kv d.c. lines with a single circuit capacity of 6000 MW(11). However the two systems thus interconnected will not remain asynchronous for long as the fast growing a.c. systems are also to be inter-connected. Since this implies the need for support at intermediate points and also because of the desirability of multiple power infeeds to the receiving European grid the development of multiterminal h.v.d.c. needs to be emphasised. A not dissimilar situation has arisen in Canada where interest has been shown in tapping the Nelson river line to inverters in Saskatchewan.

The characteristic feature of the situation as regards the inter-connection of the European countries is the existence of three large inter-connected grids, one in the East, one in the West and one in Scandinavia. The term interconnected grid as applied to any of these systems is, as yet, a misnomer, because in general - the exceptions being Switzerland, Luxembourg, Denmark and Czechoslovakia - they are national grids with weak inter-connections and minimal international power exchange. For example, excepting one W. Germany - Switzerland/Austria, one France - Switzerland and one U.S.S.R. - Hungary interconnection, there are no links at voltages above 220 kv. There is therefore considerable scope for inter-connection both within and between these systems and planning and organisation is well under way(12). There is plenty of scope for h.v.d.c. transmission but interest in the multiterminal aspect appears, at present, to be absent.

Another aspect of d.c. transmission of truly international significance is its potential application as a method to contain the expansion of urban a.c. distribution networks. Both direct economic advantages and great simplification of the already overcomplex distribution system can be shown to accrue[13 - 17]. Casson, East and Huddart[13] have after extensive investigation shown that the incooperation of direct d.c. infeed from the super-grid to the a.c. distribution network can sometimes be substantially cheaper than the conventional expansion of the supporting primary and secondary high voltage a.c. networks.

An important conclusion arising from the foregoing discussions is that the extensive use of h.v.d.c. will be predicated on cheaper terminal equipment and the feasibility of the multiterminal connection.

1.4. Automatic Control of A.C. and D.C. Systems

The fault control of a multiterminal h.v.d.c. system as envisaged in this thesis relies on a digital computer, but it would be difficult to justify computer access for handling the fault problem alone. Furthermore the future of h.v.d.c. will be influenced by the methods adopted to control the world's electricty networks and therefore the recent trend towards the automatic control of power systems is briefly surveyed.

Computers are an essential in Nuclear power station control and are becoming well established in thermal stations for automatic start-up and shut down, boiler control and auxiliary supervision[18 - 23]. Optimisation of plant and fault programming will be the next steps in this field.

The automatic control of power systems using digital computers is being developed viz: the South West region experiment[24-27] of the CEGB and error adaptive computer control and load dispatch in the U.S.[28, 29].

At present computers are usually employed off-line to predict demand and prepare minimum cost generation schedules compatible with system security, plant availability, spinning reserve and transmission loading[22, 30 - 34]. The future being problematic the computer serves the operations engineer burdened with forecast errors and outages by making security checks and computing short time generation schedules. During emergencies it is a means of quickly assessing the effect of alternative actions. The trend is towards on-line security assessment, on-line economic surveys, fault adaptive controllability, and dynamic scanning with selective display availability.

In the United States where the emphasis is on the load frequency control concept and the minimisation of area control error every area of an inter-connected network relies on independent control computers[22, 28, 33, 35]. Complete automatic control where machine controllers at the generators and area switching stations are automatically controlled from a 'nerve' centre is in the process of development but it is as yet uncertain whether wholesale automation of the power system is economic or desirable. At the present time the degree of automation varies as do the methods of control which range from complete digital to various analogue-digital techniques.

It is against this background that Ito and Sekine's emphatic remarks[36] that "when considering the economic automatic operation of inter-connected h.v.d.c. power systems within a.c. systems the most economic and efficient operation cannot be expected without the use of an on-line digital computer control-protection system" should be read. Noting that the digital computer is fast becoming an indispensable element in power system control they recommend automatic control from one, or a hierarchy of, digital computers, and estimate that, a computer developed exclusively for this purpose with comprehensive control-protection facilities will so simplify instrumentation as to make it comparable in cost with the complex circuitry of conventional control-protection equipment. The Electrotechnical Laboratory in Tokyo is developing such equipment for use in conjunction with a simulator model[36 - 39].

The d.c. system has no inherent response of its own and can be made to respond rapidly to control. This can be usefully exploited either to achieve rapid changes in a healthy power system or during emergencies. The control of a d.c. terminal to alleviate a.c. system emergencies remains to be studied and the associated problem of collecting and processing the right intelligence must be solved.

Digital computer control can therefore be justified in h.v.d.c. inter-connections handling large amounts of power and in ref. (36) a scheme using a central control computer and three local computers at the terminals is proposed.

In contrast if d.c. links are employed nearer the distribution level[13, 14, 16] where from a single rectifier on the primary or secondary h.v. a.c. grid multiple inverter injections are made to the distribution network, the use of a computer will be uneconomical.

One of the principal difficulties associated with multi-terminal h.v.d.c. schemes is the complex control required to clear faults. The fault problem cannot be handled in a manner compatible with the demands of maximum security and discrimination without a system control computer.

1.5. Transmission Faults on Multiterminal H.V.D.C. Systems

A short circuit on an inter-connected a.c. system collapses the system voltage only at the point of fault. Elsewhere due to the transmission reactances and the large reactive current flow towards the fault the a.c. voltage is depressed only partially. Power transmission is completely disrupted only in the immediate vicinity of the fault and power flow in remote networks is unaffected. During a d.c. transmission line fault however the voltage short circuited at the fault point disappears throughout the system since current flows cannot be allowed to increase for reasons of valve safety and the only impedance between the fault point and the more remote sections of the network are the small line resistances. All power exchanges associated with the voltage that has been short circuited are terminated. (These remarks do not, of course, apply to the 25 to 50 ms immediately after fault i.e. to the transient settling into the faulted condition).

It is clear that to limit the disturbance to the entire grid a fault on a heavily connected high power multiterminal h.v.d.c. system must be isolated with the greatest possible speed. Dr. Lamm's statement that "we cannot see the advantage of a d.c. breaker .... it is possible that a d.c. breaker would be useful at a further stage." [40] is not comprehensible as a circuit breaker allows fast isolation of the faulty line only, while other methods involve the slower co-ordinated control or de-energisation of one or both poles of the whole system. Even with circuit breakers post fault operation depends on fast re-setting of controlled orders at all operational converters and would still need extensive communication and automatic control facilities. Despite much research in Germany, the U.S.S.R. and Switzerland and some promising research reported in a paper at CIGRE 1968, d.c. circuit breakers are not likely to be available in the near future.

For the two terminal link Uhlmann[41] proposes that the low voltage portion of rectifier and inverter characteristics be arranged such that under fault conditions both converters move sharply towards $\alpha = 90^{\circ}$ and the inverter move less steeply than the rectifier, making the transmission unstable and leading to system extinction. The time from the application of the fault to extinction is about 150 ms. This is rather large as the system is allowed to extinguish itself and the converters are not deliberately pushed into continuous inversion. Also the author does not give the size of smoothing inductor used in these analogue computer studies. Furthermore an unrealistic fault resistance value of 100 ohms has been used.

Lamm et al[42] propose that fast de-energisation of a multiterminal system be achieved by forcing converters to invert, that the faulty line be opened by fast acting low current isolators and the system be quickly restarted. Total time from fault to restart is estimated as 200 ms but the contention that larger outage times are permissible with d.c. systems because greater divergence of phase and frequency at the terminals are no impediment to restart is questionable. D.C. system restart capability is not a sufficient criterion of permissible a.c. system instability.

High speed reclosing of the a.c. side of an inverter subsequent to a.c. system faults leads to transient commutation failure of the inverter during the re-starting process. T. Machida discusses(43) the origins of these failures and suggests methods of co-ordinating a.c. system switching with d.c. system restart to eliminate this. High speed controls of the type investigated in this thesis achieve satisfactory restart without the need for special controls and in any case Machida's proposals involve communication problems as inverter a.c. side switching has to be co-ordinated with the rectifier bridge controls.

1.6. Converter Faults in Multiterminal H.V.D.C. Systems

The external causes of commutation failure of a converter bridge valve are either sudden excessive drops of a.c. voltage or control and grid pulsing circuit malfunctioning. The internal causes of valve failure are rectifier arc-back, rectifier or inverter arc-through and arc-quenching. The failure of one bridge at any converter of an 'N' bridges per terminal system will result in a loss of $\frac{1}{N}$ of transmission capability everywhere in a multiterminal system.

Present protective practice relies on the comparison of currents in the a.c. and d.c. sides of the converter and/or the detection of unusual harmonics. More precise information of the nature of the failure or identification of the faulty valve are not sought and if the fault is repetitive the bridge is bypassed for about 200 ms and a re-start attempted(44, 45). The exception is rectifier arc-back where the severity of the fault demands immediate shut down and precludes restart.

Reeve(46, 47) enumerates the shortcomings of the conventional techniques especially with regard to multiterminal connections, the trend to higher ratings with automatic control and the desirability of detailed data logging. Ref. (46) lays out a set of tables in which time is divided into a sequence of discrete intervals separated by grid pulsing and by a.c. voltage zeros. In any interval only certain faults can occur, these and their progressive development are derived. A wired logic set-up using 108 NOR gates is designed in ref. (47). The inputs to this circuit are the logic states of valve currents, grid firings and voltage zeros and the output is an unambiguous indication of every type of valve fault and the faulty valve. Fail safe reliability is unfortunately interpreted to mean that the failure of any logic component results in a repetitive indication of commutation failure. This is not suitable if the detector is coupled to automatic bridge controls.

Where digital computers are available at converter stations the wired logic scheme proposed by Reeve can be replaced by direct digital processing. The converter information can be monitored by simple supervisors and the computer need be called only when an unusual sequence is detected.

The on-line digital supervisory instruments of the Universal control-protection unit of the E.T.L. works on a similar principle by generating logic states for valve currents, commutation voltages and permissible pulsing periods. These logic states are combined to form binary numbers and are processed in a control computer to define the operating condition of the converter[36].

1.7. Perspectives and Scope of this work

1.7.1. Perspectives

The prospects of h.v.d.c. transmission have been assessed and the importance of multiterminal links has been emphasised. The trend towards automatic control in power systems has been surveyed for its relevance to a highly controllable device like the converter and also because of the need for co-ordination and integral control when clearing faults. This thesis considers the control of a three terminal h.v.d.c. system from a digital computer and makes comprehensive records with a simulator of the behaviour of the system while clearing numerous types of converter and bridge faults.

In preparing the fault control program it has been necessary to make the assumption that adequate fault information in logic form will be available to the computer. Very little has been published on fault detectors for d.c. transmission systems and indeed this aspect of d.c. system protection remains a wide open field for investigation. An effort has nevertheless been made to ensure that the type of fault information expected is eminently reasonable. The development of moderately priced d.c. circuit breakers will radically alter the duties of detecting devices and fault control procedures.

Above all, automatic control in large systems will integrate protection and control together and the results of fault investigations must be complemented by system control studies and feasible adaptive control methods.

1.7.2. The h.v.d.c. Simulator

An h.v.d.c. simulator has been in use in the Imperial College Power Systems Laboratories for some time but lacked controls adequate for a study of this nature. Entirely new controls have been built for three 6-pulse bridges including conventional constant current control, a new type of constant extinction angle controller, bypass valve controls and reliable thyristor pulsing units. In addition an analogue interface from the digital computer to the converter controls has been installed.

The controls have been designed for fast stable operation with the connected a.c. system realistically weakened. The limiting of commutation failures in the period immediately following a fault is one of the features of these controls. The speed and controlability of the simulator are displayed in a series of preliminary tests presented in Chapter 3.

1.7.3. The PDP.8 Computer

This is a small process control computer that has been programmed for the centralised fault control of the simulator. The computer has a twelve bit word, a 4k core memory, a cyclic time of 1.6μs and the input output facilities include twelve direct digital channels each way, three D/A channels and six A/D channels.

The computer is linked to the simulator by a 100 ft. 30-way cable. A computer/simulator interface whose principle functions are the starting and stopping of the converter, the control of line isolators and by-pass values and the setting of current orders has been built.

1.7.4. The fault control program

The objectives of any fault program must be

i) To discriminate between transmission and converter faults as the latter do not always need central control intervention.

ii) On available logic information to ascertain with maximum discrimination the nature and location of any fault.

iii) To make up and transmit suitable commands to individual converter controls to de-energise the minimum necessary section of the network, then isolate the fault and restart. Also bypass valve operation under certain circumstances is initiated by the fault control program.

iv) To attempt a single restart of the faulted section before locking out if this is desirable.

v) Where the network configuration has been altered by iii) above, to automatically update the program and ensure continued control.

vi) To ensure that occasional single misfiring of converter valves does not trigger protective equipment.

1.7.5. The Multiterminal System Investigated

To make the control program illustrative of general techniques it has been written for the typical three terminal, two bridges per terminal teed connection. Fig (1.1) shows the system including the positions of line isolators. The figure indicates system inter-connection when all lines and converters are operational but under conditions of temporary outage of portions of the network it may be working in one of a large number of possible configurations. Topologically there are forty eight feasible configurations of the transmission lines and bridges that avoid electrically nonsensical open circuits. Usually however numerous additional constraints are imposed by the power system, for example: restrictions on cable polarity, restrictions on the use of earth path etc. Realistic constraints have been introduced and the number of inter-connections, i.e. operating modes, in which the system will be allowed to work are limited to fifteen.

As only three bridges of the simulator have been as yet equipped with the new controls each terminal is represented by a single converter bridge. For this reason only some sections of the fault control program could be proved by on-line control tests in conjunction with the simulator.

It would appear reasonable to except the behaviour of the three bridge connection on pole to 'neutral' faults to be the same as that of a six bridge connection on pole to pole faults, as the only essential difference is in the twelve pulse and six pulse nature of the d.c. voltages and currents. A short analytical comparison using sampled data techniques at two different sampling rates has been made to throw light on this aspect.

1.7.6. Enumeration of the Tests Conducted

The following faults were put on the d.c. system and the behaviour of simulator with on-line computer control was recorded.

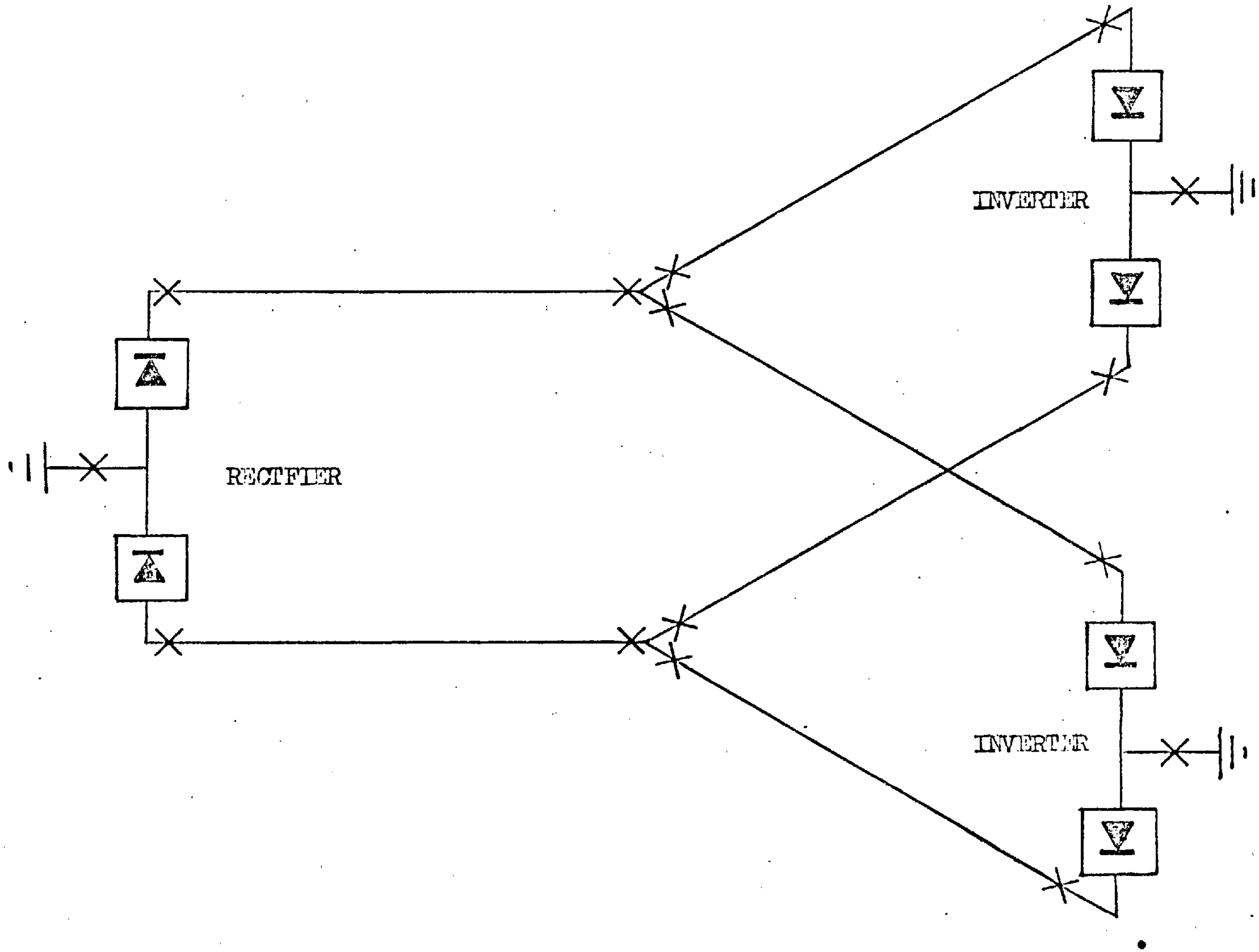


Fig 1.1 The Three Terminal System.

i) Transient faults on the rectifier and inverter lines

ii) Permanent faults on the rectifier line leading to system shut down

iii) Permanent faults on the inverter line leading to isolation of the faulty branch

iv) Repetitive commutation failure of the rectifier and of the inverters cleared by block-bypass - deblock sequence at the faulty station.

The method proposed by Lamm et al[33] for the removal of both rectifier and inverter stations by co-ordinated control with minimum disturbance to the system and without firing the by-pass valve have also been applied with promising results.

The recovery of the system subsequent to the following short time a.c. system faults

i) Rectifier a.c. system 3 phase short circuit

ii) Inverter a.c. system balanced and unbalanced faults

iii) Loss of inverter a.c. voltage

has also been recorded and is presented in Chapter 4.

CHAPTER 2

Simulation and the Simulator

2.1. The Scope of H.V.D.C. Model Studies

Analytical techniques have been developed[48 - 55] for the solution of some aspects of the two terminal h.v.d.c. link operation. These methods can be extended to the three terminal system but with increased computational complexity. The results presented by Norton and Cory[52, 53] can as yet be viewed only as a first step towards a satisfactory mathematical analysis of h.v.d.c. system stability and performance. Increasing computational complexity, difficulties in finding a precise mathematical model and the large number of high order non-linear differential equations involved defeat the analytical solution of the general multiterminal system. While the analysis of the normal system for stability etc. is itself formidable, the analytical study of the system during emergencies is even more difficult as events like commutation failures cannot be regarded as small disturbances and are not amenable to linearisation. The need for model study and simulation is generally understood and accepted[57 - 62]. The simulator is free from the linearisation often demanded by analytical methods, does not overlook or approximate many factors as the analyst must do, permits the monitoring at will of voltage, current or any waveform in any part of a complex inter-connected network and is convincing to the practical engineer by the directness of its display. A preliminary simulation of a problem will usually indicate its salient features and be a guide to the choice of a mathematical model and in this sense the simulator is complementary to more abstract techniques like digital computers. At the present stage of knowledge a good deal of emphasis needs to be laid on simulation techniques, sometimes even as a stepping stone to computational methods.

2.2. Limitations of Modelling

An h.v.d.c. simulator is relatively inflexible of control if the labour of building a new control loop is contrasted with the changing of a few cards in a computer program. Full organisational and technical support is needed if a reliable and realistic simulator is to be maintained[58]. The best d.c. simulators are backed by a technical team and are much more costly than digital computer studies.

The three principal sources of error in a model are

i) the thyristor drop of 1^V to 2^V is a much larger ratio of the model voltage of 100^V than the 40^V to 60^V arc drop in say a 100 kv mercury arc valve.

ii) the spurious effects encountered in the laboratory, for example mains disturbance and stray capacitances are in no way identifiable with the spurious disturbances encountered in valve houses and transmission networks.

iii) the resistance to inductance ratio of all laboratory equipment, particularly transformers transmission lines and connecting leads will invariable be higher than in power systems; Ref. (60) suggests ten times higher. This contributes to reducing the model rectifier d.c. voltage and raising the inverter voltage in comparison with an h.v.d.c. bridge.

Another difference relevant to fault studies is that if due to control failure or during rapid transients the inverter extinction angle falls below, say 5^o (250 microsec) commutation failure is almost certain to occur in mercury arc valves. Thyristors however require a de-ionisation time of only a few microseconds.

2.3. Effect of error in $^R/L$ on extinction angle of Inverters

It has been noted that the $^R/L$ ratio of a laboratory converter transformer is about ten times that of a power transformer. The equation for circulating current during commutation is written from figs. (2.1) and (2.2) which show the two commutating transformer phases and valves.

$$2L_c \cdot \frac{di_c}{dt} = (v_y - v_r) - (V_{th1} - V_{th2}) - 2i_c\, r_t + I \cdot r_t \quad - (2.1)$$

where V_{th1} and V_{th2} are the drops in the thyristors. If V_{th1} and V_{th2} are assumed equal and written V_{th} the d.c. terminal voltage during commutation is given by

$$v_{dc} = \frac{v_r + v_y}{2} - V_{th} - \frac{I.r_t}{2}$$

Before and after commutation the d.c. voltages are given by

$$v_{dc} = v_r - V_{th} - 1.r_t$$

and $v_{dc} = v_y - V_{th} - i.r_t$ respectively.

It is to be noted that the voltage during commutation is not the mean of these two values being $\frac{I.r_t}{2}$ less than the mean as indicated in fig 2.3. From this figure it is also clear that the effect of this is to reduce the available extinction angle by an amount given approximately by

$$\delta\gamma = \frac{I.r_t}{V_{max}}$$

For the simulator r_t is conservatively estimated at 0.5 ohms so that under full load conditions and $V_m = 60\sqrt{2}$ $\delta\gamma = 2^o$.

V_{th} however is not a constant, though non-linear and if it is assumed that $V_{th} = 0$

i) for the thyristor beginning to conduct at the start of conduction

ii) for the thyristor ending conduction near the instant of extinction.

At the beginning and end of the commutation period

$$v_{dc} = \left(\frac{v_r + v_y}{2}\right) - \left(\frac{I.r_t + V_{th}}{2}\right)$$

and the displacement on the mean is now $\left(\frac{I.r_t + V_{th}}{2}\right)$ at

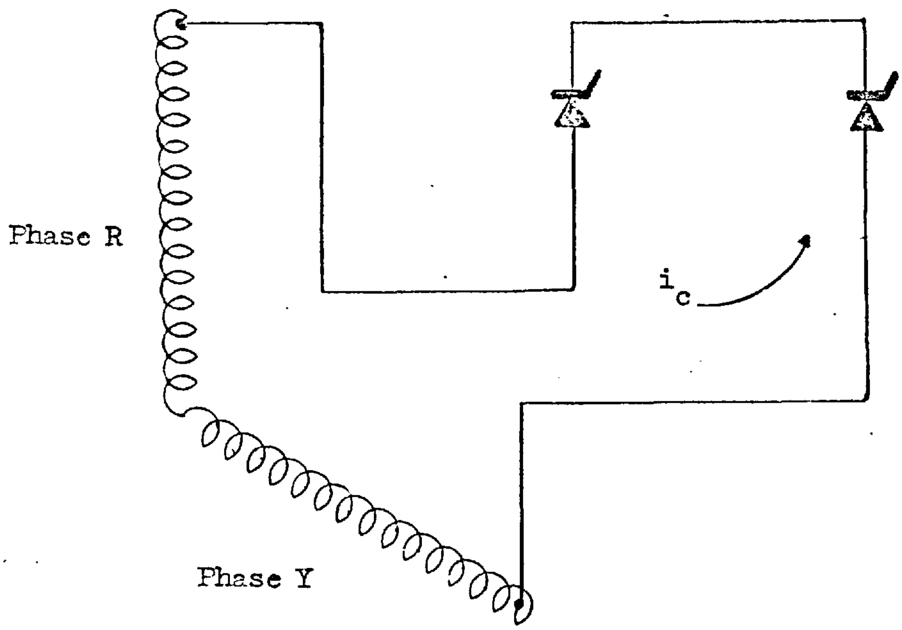


Fig 2.1 Commutating Circuit.

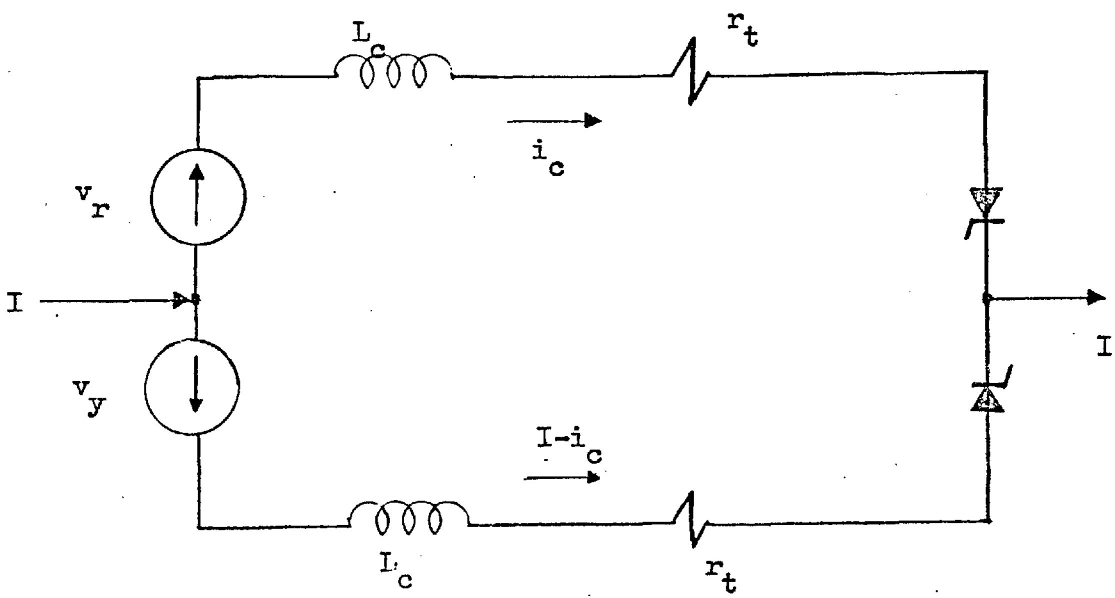


Fig 2.2 Simplified Commutating Circuit.

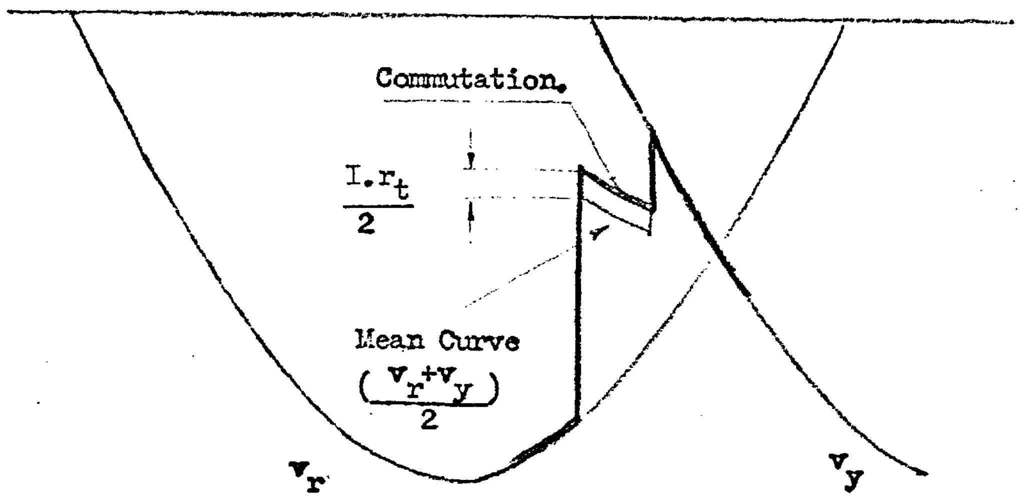


Fig 2.3 Commutating Waveform when $R/L \neq 0$

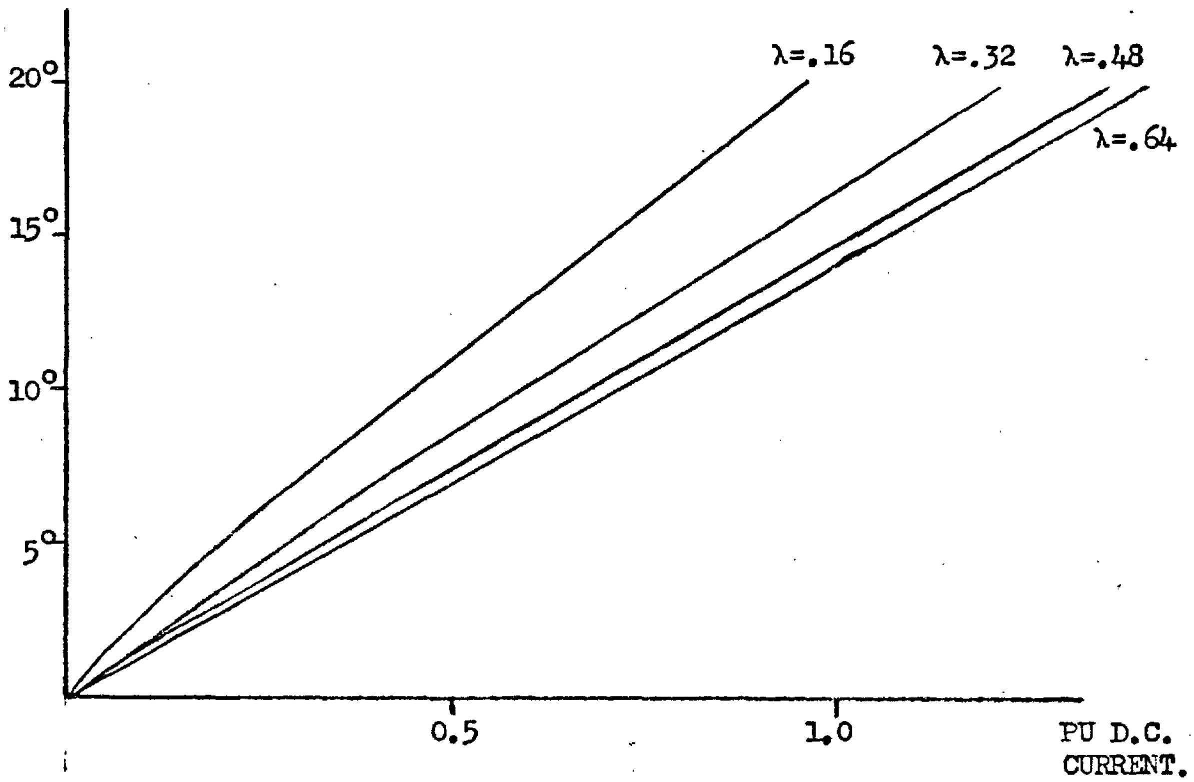


Fig 2.4 Variation of Commutation Overlap Angle with Current when (R/L) is not negligible.

Graphs obtained by increasing R at fixed L to increase λ.

these instants but remains $\frac{I.r_t}{2}$ during the remainder of the commutation period. An additional loss of 1° to 2° in the effective extinction angle is to be expected.

The overlap angle (u) is no longer given by the conventional equation

$$\cos(\beta - u) - \cos\beta = \frac{2\omega LcI}{Vm}$$

and is now given by the solution of equation (2.1)

$$\frac{\cos(\beta + \theta - u) - \cos(\beta + \theta) \cdot e^{-\lambda u}}{1 + e^{-\lambda u}} = \frac{I.\omega L_c}{E_m} \cdot \sqrt{1 + \lambda^2}$$

where $\lambda = \frac{R}{\omega L_c}$ and $\theta = \tan^{-1}(\lambda)$.

These results are plotted in fig. 2.4.

The effects of the resistance in the commutating circuit are

i) the commutation overlap angle is increased

ii) the d.c. voltage during commutation is less than the mean voltage of the commutating phases and the effective available extinction angle is reduced

iii) the valve inverse voltages and step inverse voltages are not accurately modelled.

Inclusion of the nonlinear thyristor drop enhances these effects. It must also be pointed out that once successful commutation occurs the de-ionisation angle is not affected.

2.4. General description of the H.V.D.C. System Model

The simulator is a three terminal scheme with provision for a total of six three-phase Gratz bridges. The bridge and by-pass values are modelled by silicon controlled rectifiers rated at 16^A and 400^V p.i.v. Each bridge is nominally rated at 5^A and 100^V and a two bridge converter at 2 kVA. The high current rating of the thyristor permits the use of cheap glass fuses during control development and system tests achieving considerable overall economy in simulators for research purposes.

2.4.1. The Bridge Transformer and d.c. Smoothing Inductor

Each converter is supplied from two independent three winding transformers, star/star/delta and delta/star/delta both rated at $220^V/80^V/110^V$. The primary is tapped to $\pm$ 10% in 1% steps, the tertiary is provided for filter or reactive compensation connection. The transformer is designed for minimum leakage inductance to allow a wide range of a.c. system reactance simulation using external reactors. Table 2.1. gives the losses in the transformer and fig 2.5 is a plot of magnetising current, both are reproduced from ref. (63).

The smoothing inductor used on the d.c. side has eight separate sections each of which has a self-inductance of 0.0464H and a mutual inductance of 0.065 H to any other section. The resistance of each section is 0.2 ohms. A wide variety of inductances values between 0.46 H and 4.0 H can be obtained by suitable series parallel conections provided they are compatible with coil current rating.

Tests on the inductor are described in ref. (63) from which the test circuit of fig 2.6 and the results in fig 2.7 have been reproduced. The a.c. source of fig. 2.6 is a 40^V, 300 c/s oscillator.

2.4.2. The Thyristor pulsing units

The thyristor and the pulse transformer are mounted on a single panel, fig. 2.9. Unidirectional pulses of current pass through the thyristor gate-cathode junction and the transformer secondary during pulsing. This current is compensated by variable resistor VR and the d.c. magnetisation of the

TABLE 2.1 LOSSES IN THE TRANSFORMERS.

	STAR/STAR	STAR/DELTA
Effective shunt resistance (core loss)	1010 ohms	1058 ohms
Effective shunt reactance (magnetising)	554 ohms	505 ohms
Lumped series resistance	1.33 ohms	1.25 ohms
Lumped series reactance	Negligible	Negligible

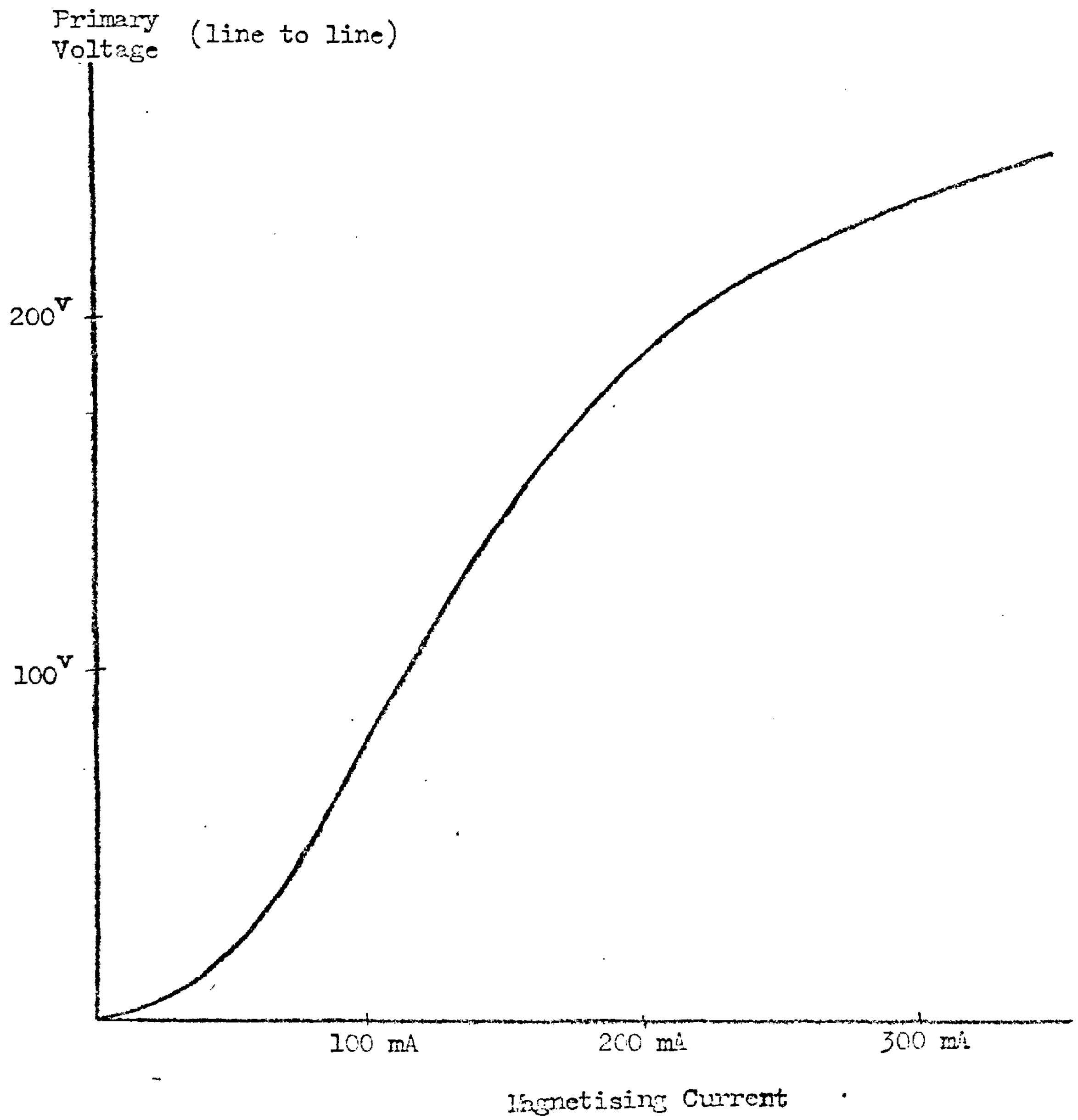


Fig 2.5 Magnetising Current of Converter Transformer.

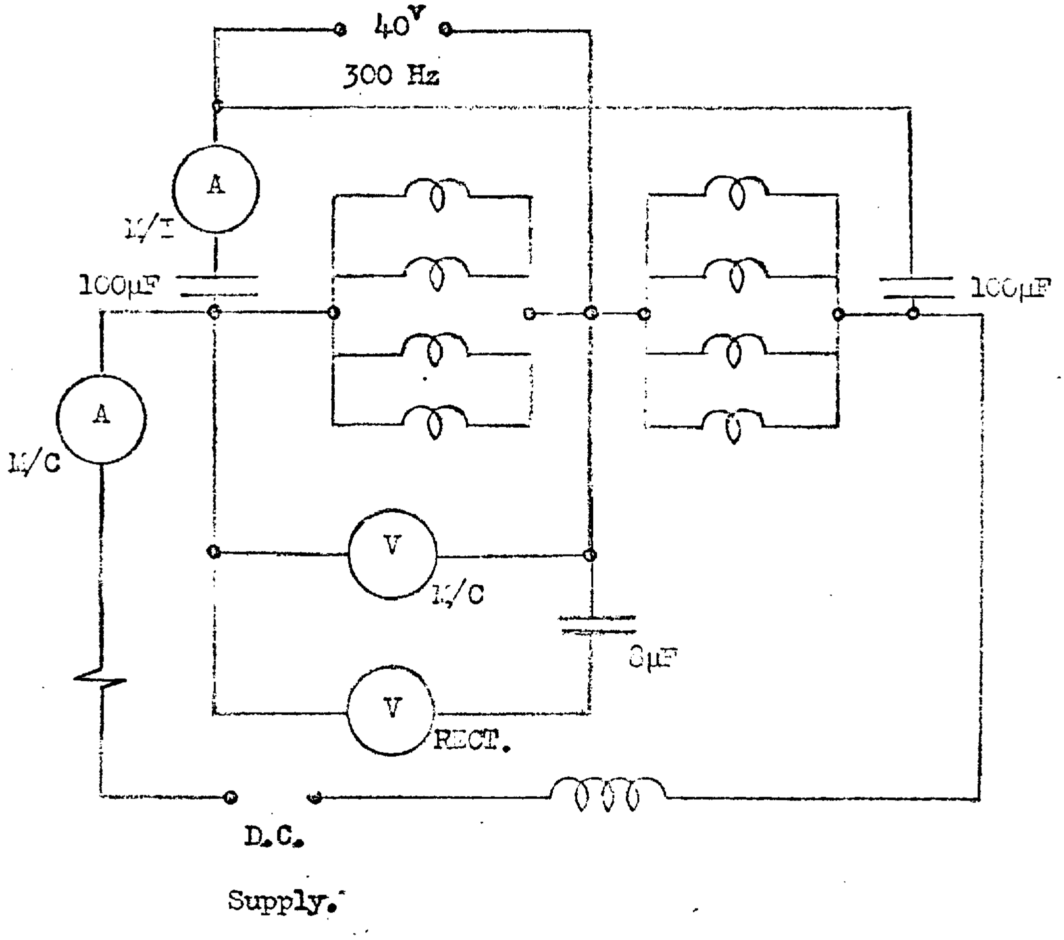


Fig 2.6 Smoothing Inductor Test Circuit. (Results fig 2.7)

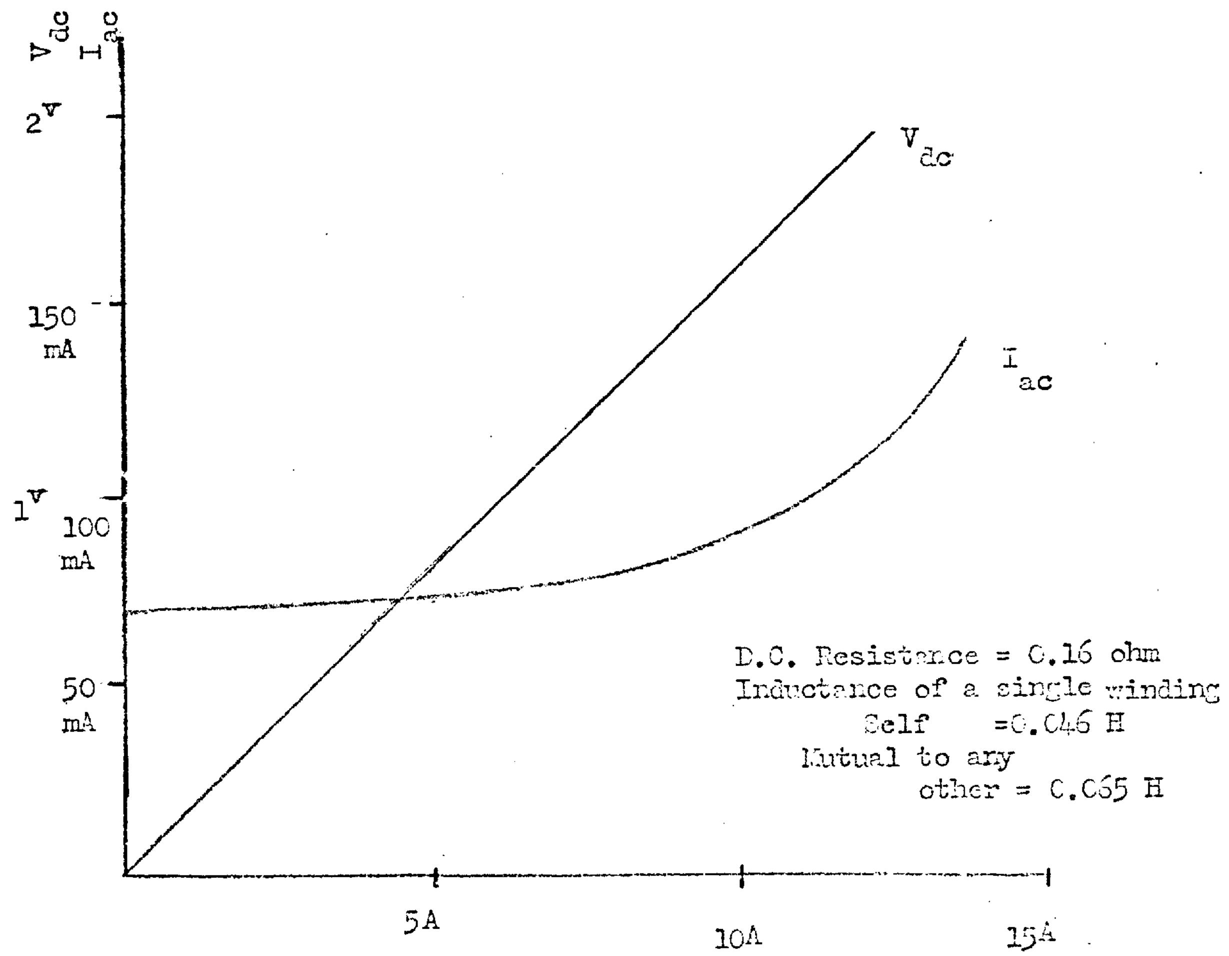


Fig 2.7 Results of Tests on Choke.

core is offset by a bias current of 40 mA in the tertiary winding. Sustained and unusual pulse distortion accentuated by the "bootstrapping" across the pulse generator output stage can arise if these precautions are not observed.

Fig. 2.8 is a circuit diagram of the pulse generating unit, one of which is required for each thyristor. The circuits were designed and tested in the laboratory and commercially etched to order on fibre glass printed circuit cards. The circuit is controlled by a d.c. firing angle control signal and the phase of the output pulse is linearly proportional to the magnitude of this signal.

Transistors T1 - T2 form a level detector pair sensitive to an input sinusoidal supply and generating a square-wave fixed in phase with respect to it.

Transistor T3 is switched by this square wave and when in the off state permits capacitor C1 to charge through VR1. C2 provides positive feedback or bootstrapping to ensure a linear ramp signal which in turn is applied to a second level detector pair T5 - T6 to generate positive going pulses each time the ramp voltage exceeds the reference signal. The output is differentiated and used to trigger a 150° monostable T9 - T10 and is fed via output stage T11 - T12 (provided with bootstrapping for fast pulse rise) to the pulse transformer primary. The circuit is automatically reset each time T3 turns on and discharges C1. The method of pulse terminating and pulse blocking are evident from the circuit diagram. A pulse of 150° is advantageous during transients but is terminated at 120° by the next pulsing unit during steady state operation.

The triggering pulse rise time on open circuit is 0.5 microsec and the ramp linearity is better than 0.5%.

Ainsworth(64) has shown that harmonic instability can arise with weak a.c. systems due to the distortion of the a.c. terminal voltage and therefore the pulsing unit reference sinusoid. An oscillator generating true sine waves and locked in frequency and phase to the a.c. system is proposed as a means

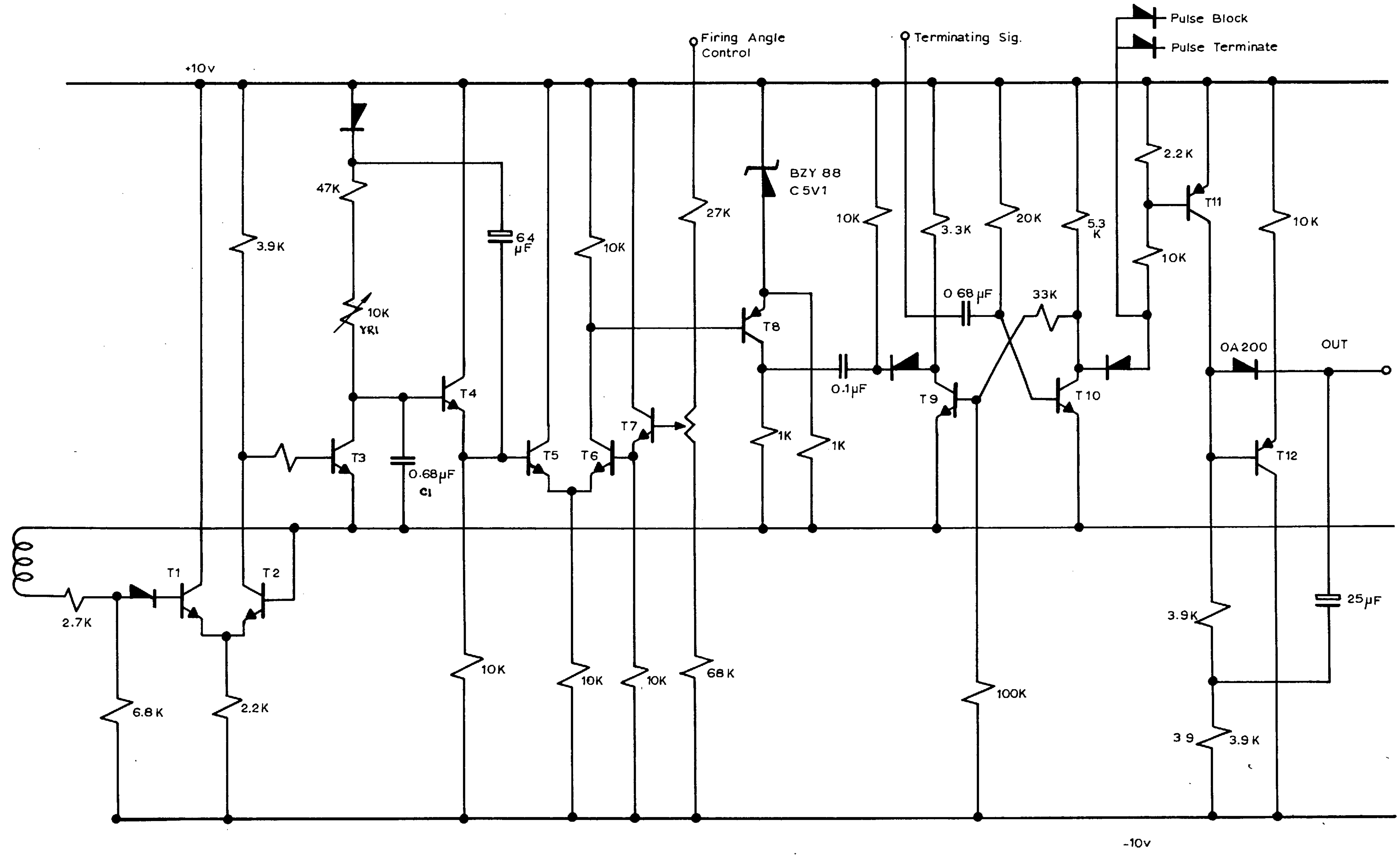


Fig. 2.8. Pulse Generating Unit.

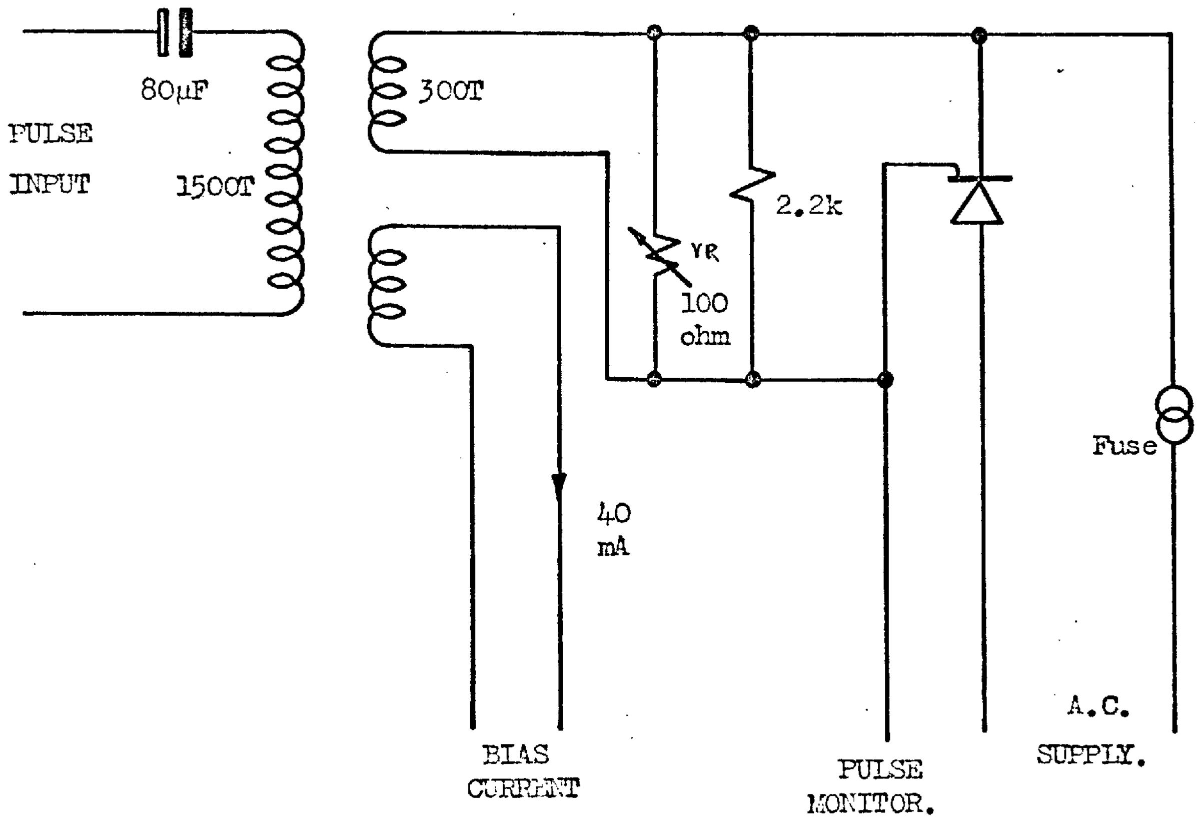


Fig. 2.9 Thyristor and Pulse Transformer Panel Diagram.

of eliminating harmonic instability. In the laboratory the a.c. infinite busbars may be used as a substitute provided the phase locked oscillator transient response will not be significant in the type of faults investigated. This procedure has usually been adopted and some further aspects of this are discussed in section 4.2.

2.5. Elementary considerations of Three Terminal System Stability.

An exhaustive analysis of the stability of the two terminal system has been made by Reider[49] where it is shown that

i) A two terminal system with rectifier constant current control and an uncontrolled inverter is always stable

ii) An uncontrolled rectifier with inverter c.e.a control is unstable

iii) An inverter on c.e.a control working against a rectifier on constant current control is normally stable but possesses a region of instability which can be reduced by confining the rectifier controller gain within certain upper and lower bounds.

The method of solution was to obtain expressions for the two terminal voltages in operational form using the discrete-Laplace transform and investigate the locus of the denominator of these expressions. As a complicated operator is obtained an exhaustive investigation requires a family of curves corresponding to three parameters, rectifier angle α, inverter angle β , and the phase difference between the two systems. An investigation of the three terminal system by this method would involve a more complicated operator having five parameters. The method of investigation by Norton[65] for the three terminal link is limited in usefulness by the assumption of an infinite bus on the a.c. side. Clade and Lacoste[55] again assume an infinite system at the inverter and are also compelled to neglect line and cable capacitance in order to arrive at a third order operational equation.

A simple analysis providing approximate stability criteria will suffice as a starting point for design as the final adjustments are always made on the model. The following elementary analysis serves this purpose.

A converter on constant current control may be represented by a constant current source Isc in parallel with a resistance R_s where

$$R_s = \frac{3\sqrt{2}}{\pi} . A.V.\text{Sin}\,\alpha + \frac{X_R(I.X_R + V(A.I.\tan\phi.\text{Sin}\,\alpha + X_R.\text{Sin}\,\phi\,)}{V + I.X_R.\,\text{Sin}\,\phi}$$

where V, I, ϕ are the a.c. system voltage, current and phase angle X_R is the a.c. system reactance.

The second term is to make allowance for changes in a.c. system voltage as current changes.

An inverter on constant extinction angle control may similarly be represented by a voltage source in series with a resistance $-R_G$ where

$$-R_G = -\frac{3X_c}{\pi} + \frac{X_c\,(X_c.I - V.X_c.\text{Sin}\,\phi\,)}{V - I.X_c.\text{Sin}\,\phi}$$

where V, I, ϕ are the a.c. system voltage, current and power factor angle and X_c is the nett commutation reactance.

The mathematical model employed is shown in fig. 2.10 (a) where I_{sc}.RE and I_{sc}.INI are the short circuit currents of the converters or constant current control and R_{s1}, R_{s2} are the linearised slope resistances determined as indicated above. Line and smoothing inductor parameters are lumped and the effective negative resistance $-R_G$ is modified to

$-R_G = -R_G$ (defined above) + inverter line resistance.

For stability considerations the simplified circuit of fig. 2.10b is derived where v_d is a disturbing signal and i_d is the

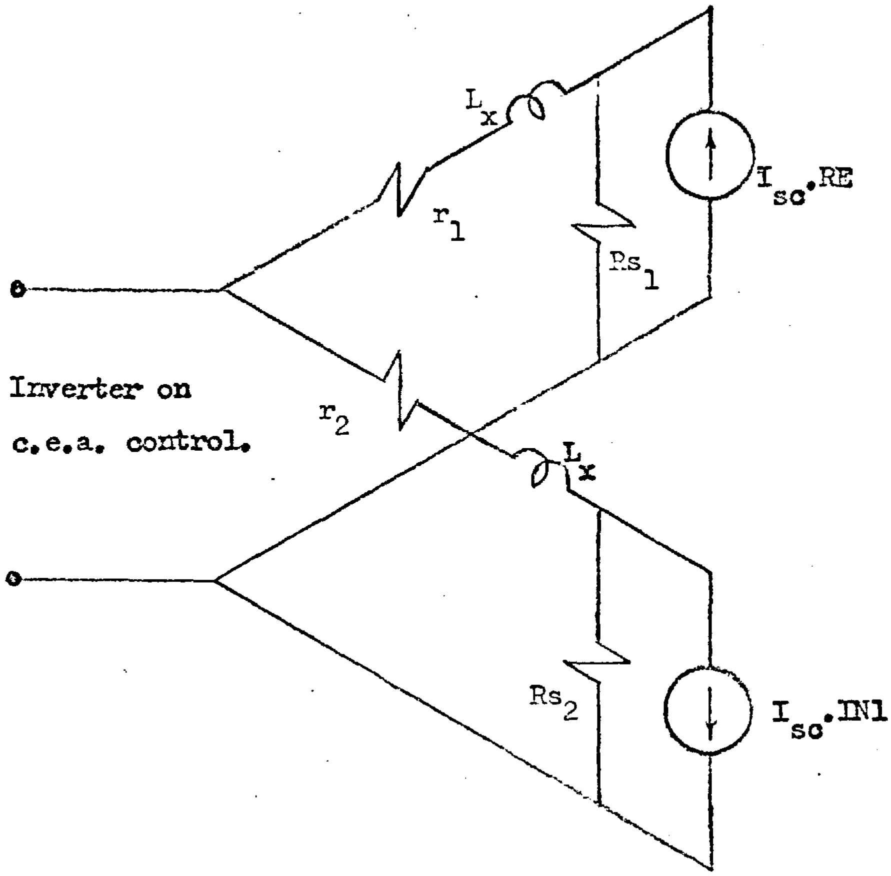


Fig 2.10a Mathematical Model for Three Terminal System Elementary Stability Analysis.

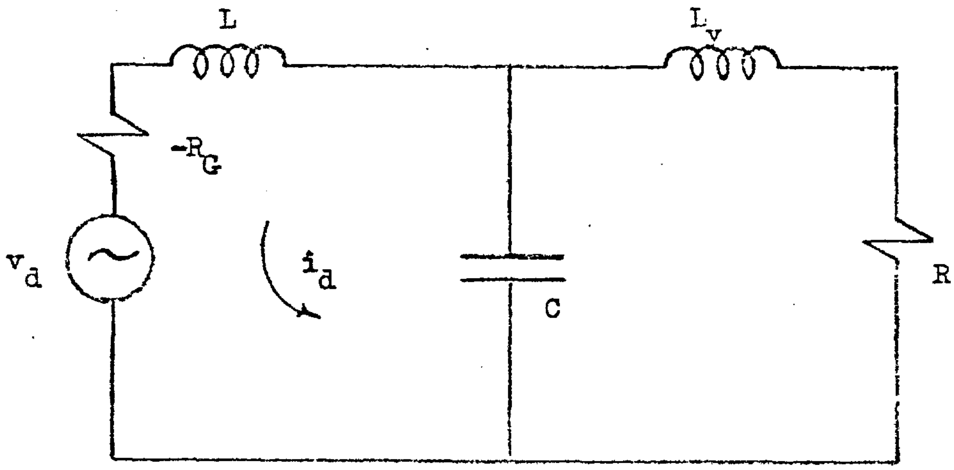


Fig 2.10b Simplified Form of Mathematical Model of fig. 2.10a.

disturbed current related by the operational equation

$$i_d\ (p) = v_d\ (p)\ .\ L\ (p)$$

where

$$L_y = \tfrac{1}{2}\ L_x$$

$$R\ = 1/((\frac{1}{R_{s1} + v_1}) + (\frac{1}{R_{s2} + v_2}))$$

and the operator L (p) is

$$L\ (p) = \frac{p^2.\ CL_y + p.RC + 1}{p^3.\ C^2LL_y + p^2.C^2(LR - L_yR_G) + p.C(L + L_y - RR_GC) + C.\ (R - R_G)}$$

If for convenience the assumption $L_y = \tfrac{1}{2}\ L_x = \tfrac{1}{2}\ L$ is made the conditions for stability are given by

i) $R > R_G$

ii) $R < \dfrac{3L}{2C.R_G}$

iii) $R^2 - R\ (\dfrac{R_G}{2} + \dfrac{L}{C.R_G}) + \dfrac{L}{4C} < 0$

From i) and ii) the system cannot be stabilised if

$$R_G > \sqrt{(3L/2C)}$$

In practise the critical value of R_G is never exceeded but the limitations this places on the bounds of R may be unsuitable from constant current control considerations.

The function of criterion (iii) is sketched in fig. 2.11 and the stable region bounded by an upper and a lower limit of R is shown.

The stability limits indicated by this method both for typical and extreme parameter values have been collected in table 2.2 for a single bridge converter. Only the upper limit of R is usually of any significance.

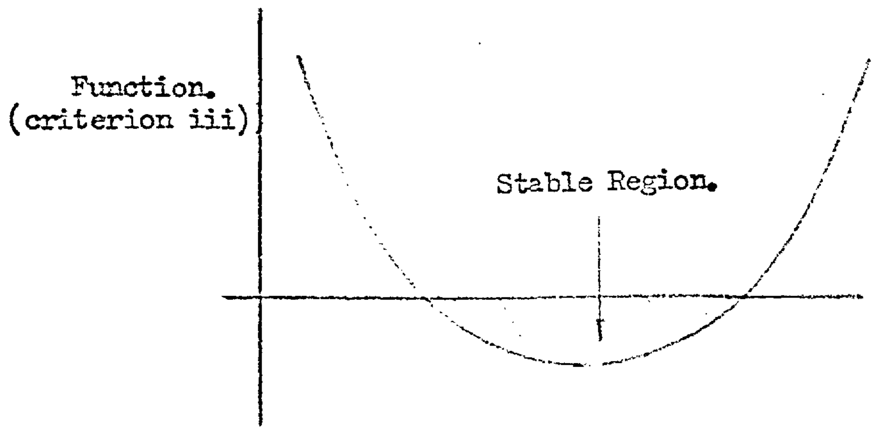


Fig 2.11 Sketch of function derived in Section 2.5 and associated Stability boundary.

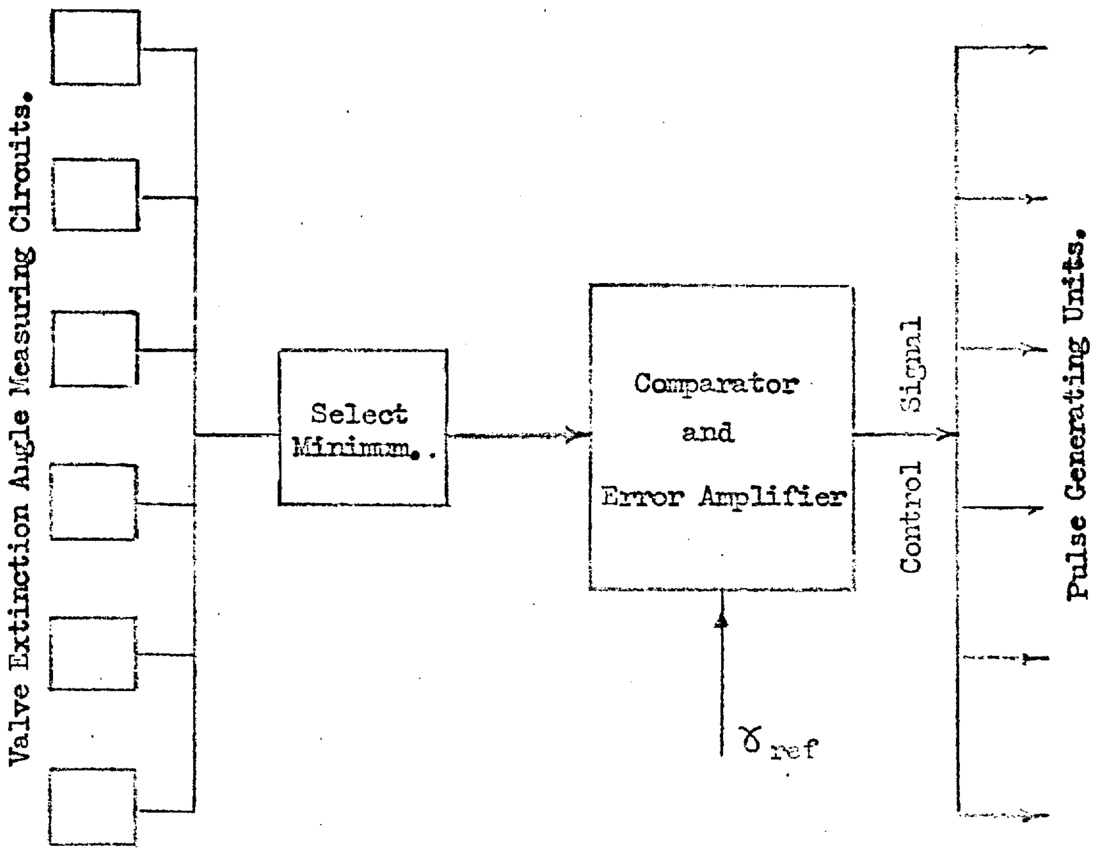


Fig 2.12 Principle of the new C.E.A. Control Scheme.

TABLE 2.2

Transformer secondary kV a.c.	Inverter rating MVA	Inverter a.c. SCR	L Hen	C µF	R.upper limit approx. ohms	R.lower limit approx. ohms
80	200	2	0.5	100	330	15.0
80	200	5	0.5	100	820	6.5
80	200	5	1.0	25	6.5k	6.5
160	200	2	1.0	25	370	75

The principal error in this analysis is that the finite transient response of the controllers have been neglected.

2.6. The Constant Extinction Angle Controller

2.6.1. Conventional Method of Control

The only system of constant extinction angle (c.e.a) control in use at the present time is called consecutive control(66 - 68). In this method certain equations are assumed to describe the process of commutation. Peak a.c. voltage, direct current magnitude and the instantaneous cyclic time are continuously monitored and operated on until the requirements of the equations are met when minimum firing angle for successful commutation is assumed to occur and the subsequent valve is fired. Reactive power consumption is minimised at every individual valve firing. Consecutive control suffers from a number of defects.

1. The assumption of balanced sinusoidal 3-phase supply is implicit, with the result that where harmonic or other waveform distortions reduce the area under the commutating voltage-time curve the danger of commutation failure arises.

2. Phase unbalance can cause the true voltage cross over point to shift so that the angle available for extinction is reduced but this is not detected by this method of control.

3. The firing of the six valves is independently controlled so that successive firing intervals can differ from 60° resulting in the generation of extra harmonics including sizeable even harmonics. The harmonic instability discussed by Ainsworth(64) is aggravated.

2.6.2. The Principle of the new Control Scheme

In the new scheme the firing of the six thyristors is not independent. The method of control ensures that the firing interval is always maintained at 60° despite small disturbances. The extinction angle of every valve is measured and stored, each store being updated once a cycle. The smallest value in store is continuously selected, compared with the reference minimum extinction angle and the amplified error signal applied to all the pulse control units to complete a closed loop control. The extinction angles of all valves are equal to or greater than the selected minimum. The scheme is illustrated in fig. 2.12.

Waveform harmonic distortion, supply voltage phase and magnitude unbalance or any other factors which influence commutation but are not accounted for in the conventional equations employed in consecutive control do not lower control effectiveness in this method as the actual extinction angles are measured. Overall control stability is improved because accurate 60° phase separation between successive firings is ensured. The concept is one of extreme simplicity involving merely the measurement of an angle and the use of a closed loop to hold it at an optimum value. Analogue computers are not required as the system is easily fabricated from standard electronic circuitry. Very small settings of extinction angle, down to 6° have been successfully used. Commutation failure is detected as zero degrees extinction angle and the bridge firing angle is rapidly advanced by the large error signal.

The main limitation of this method is that a time delay of up to 60° (30° in twelve pulse operation) may be introduced between the occurrence of some system transient and an awareness of it reaching the controller. No control action is taken to compensate for a disturbance until it is detected in the variation of the extinction angle itself.

It must be pointed out however that consecutive control corrects for a voltage disturbance only if it occurs before the voltage peak. Variations of d.c. current are taken into account up to the instant of valve firing but the large smoothing inductor ensures that these changes between successive firings is not fast. In any event if inverter $(\gamma + u) > 30^{o}$ consecutive control has no advantage even in these respects.

The name 'comprehensive control' is proposed for this method of c.e.a. control to contrast this concept to the consecutive control principle.
The term C.E.A. Control when used in the following Sections refers to this new method of control.

2.6.3. Circuit details of Angle Measuring and Storing device

Each bridge requires six separate angle measuring and storing circuits together with one output comparator amplifier. The measuring and storing units were designed in the laboratory and commercially etched to order on fibre glass printed circuit cards.

The functioning of circuit fig. 2.13 may broadly be divided into five sections, the input bistable, the ramp generator with buffer, the sample and hold circuit with buffer, the Schmidt trigger and the cascaded twin monostables. A voltage ramp commencing at the valve current zero is generated, this is sampled and stored at the corresponding commutation voltage zero. The stored signal is therefore a measure of the valve extinction angle.

The voltage across a thyristor, that is one of the six a.c. line to line voltage combinations, is supplied to the Schmidt trigger which has a snap action and rapidly changes state when the nett volt voltage passes an adjustable level near zero.

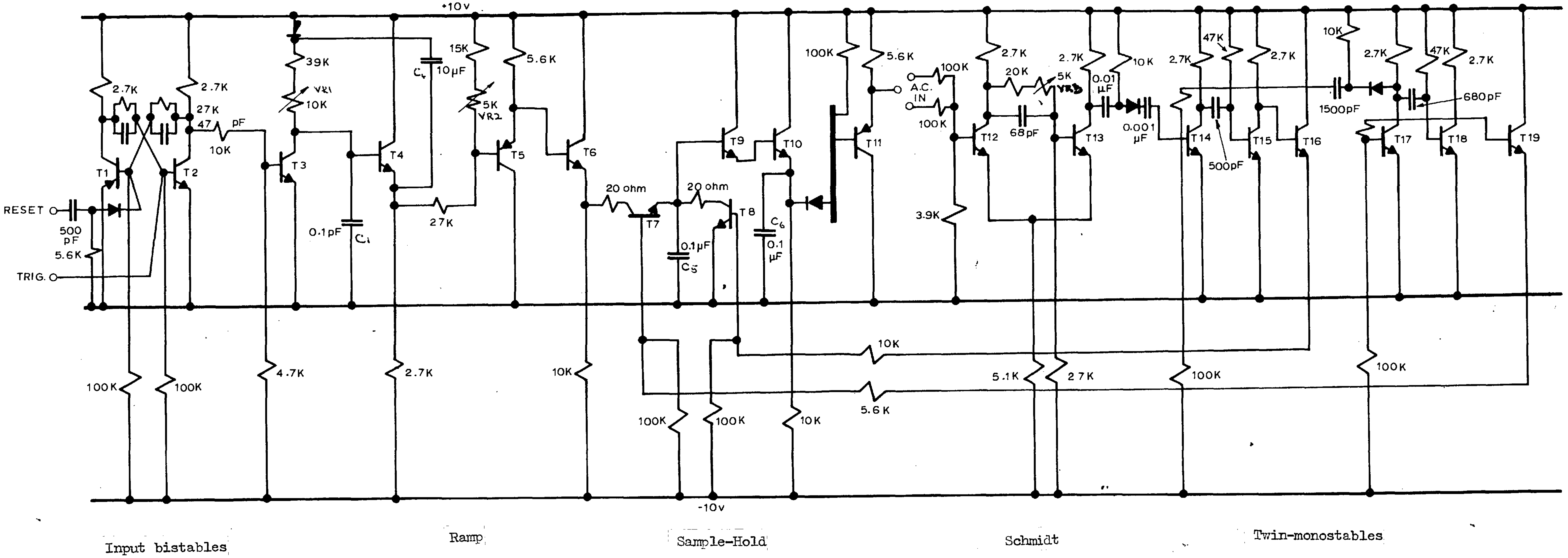


Fig. 2.13. C.E.A. Control Angle Measuring Circuit.

VR3 is the adjustment potentiometer. The Schmidt resets at the next voltage cross over, i.e. 180^o later. The Schmidt output is differentiated and triggers the first monostable which generates a 20 µs positive going pulse. This pulse is used to discharge the capacitor on which the measured extinction angle signal is stored in readiness to store a new sample. The negative going edge of this monostable triggers a second identical monostable whose pulse is used to operate the sample action. The phase of the Schmidt output can be controlled by VR3 and the whole circuit is carefully aligned to ensure that the second monostable pulse coincides with the commutation voltage zero.

The input bistable changes state in response to a pulse generated by a circuit (section 2.6.4) detecting the instant of valve current zero. The bistable is reset only at the beginning of the valve conducting period so as to be insensitive to spurious impulses during the valve non-conducting period. The bistable switches the ramp generator, a ramp linearity better than 1% is obtained by bootstrapping via capacitor C4. Ramp excursion is approximately, 0^V to 8^V for α going from 0^o to 90^o, and the slope can be aligned at VR1. The buffer has a potential divider added to reduce the ramp size as necessary and also to allow the ramp origin to be offset accurately away from zero volts, say to 1^V, for measurement precision at small extinction angles.

The sample and hold circuit receives a 20 µs discharge pulse at the base of T9 followed immediately by a 20 µs sample pulse at the base of T7 at the valve commutating voltage cross over. The time constant of the sampling path is 2 µs allowing ten time constants for the charging action. The sampled value is stored on C5, 0.1 µF, and as the signal must be stored for 20 m s stringent measures have to be taken to minimise leakage of stored analogue signal. The output buffer is a Darlington-pair of selected high gain transistors. The capacitor C6 supresses the impulse dip in the stored signal arising from cyclic discharging, the associated time constant of 0.1 m s is not significant from the power system point of view. The linearity of the sample and hold

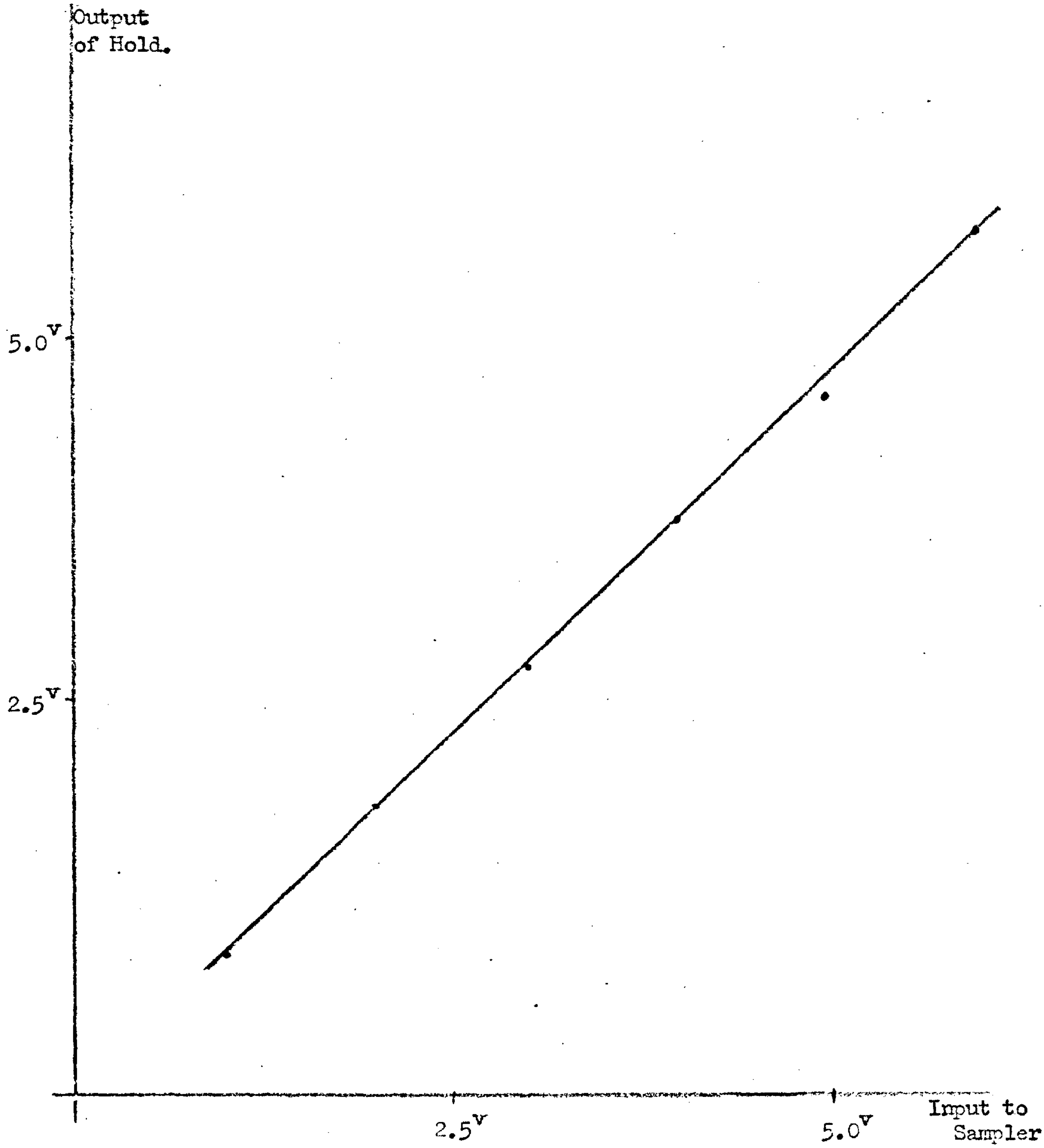
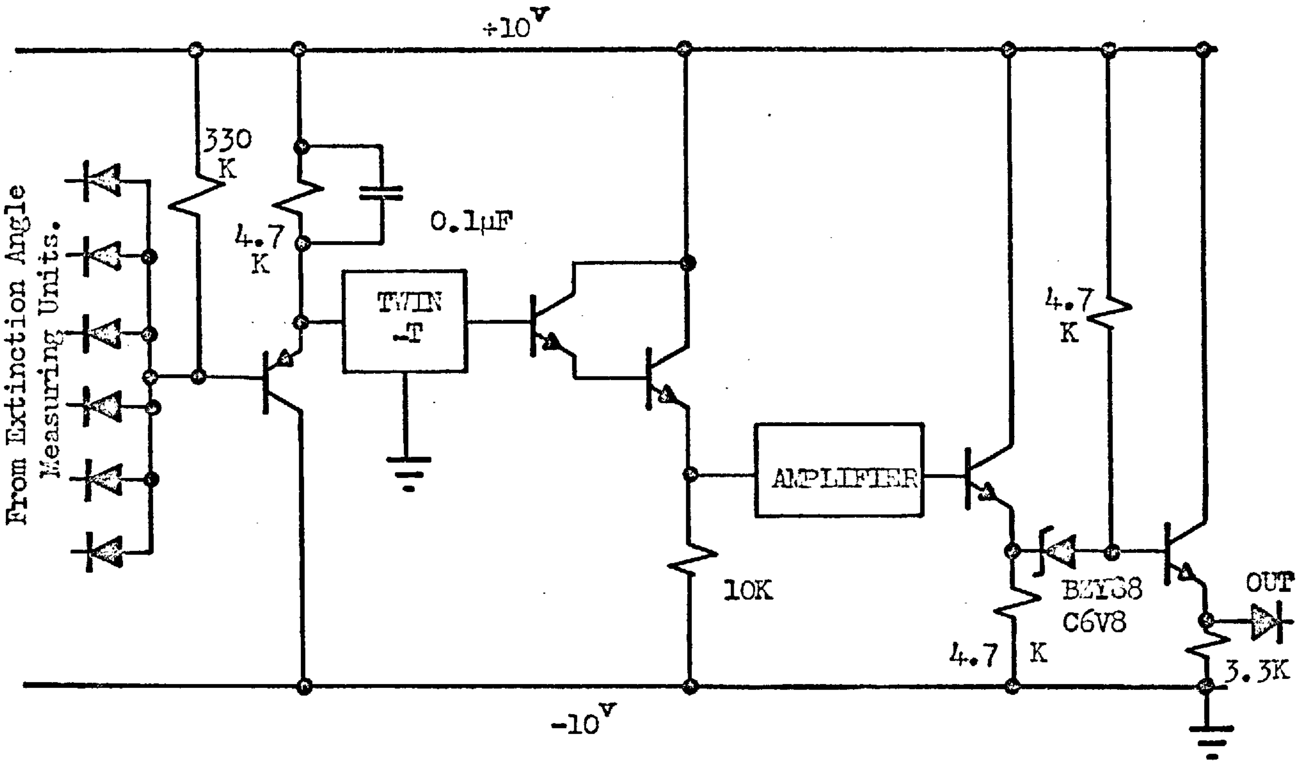
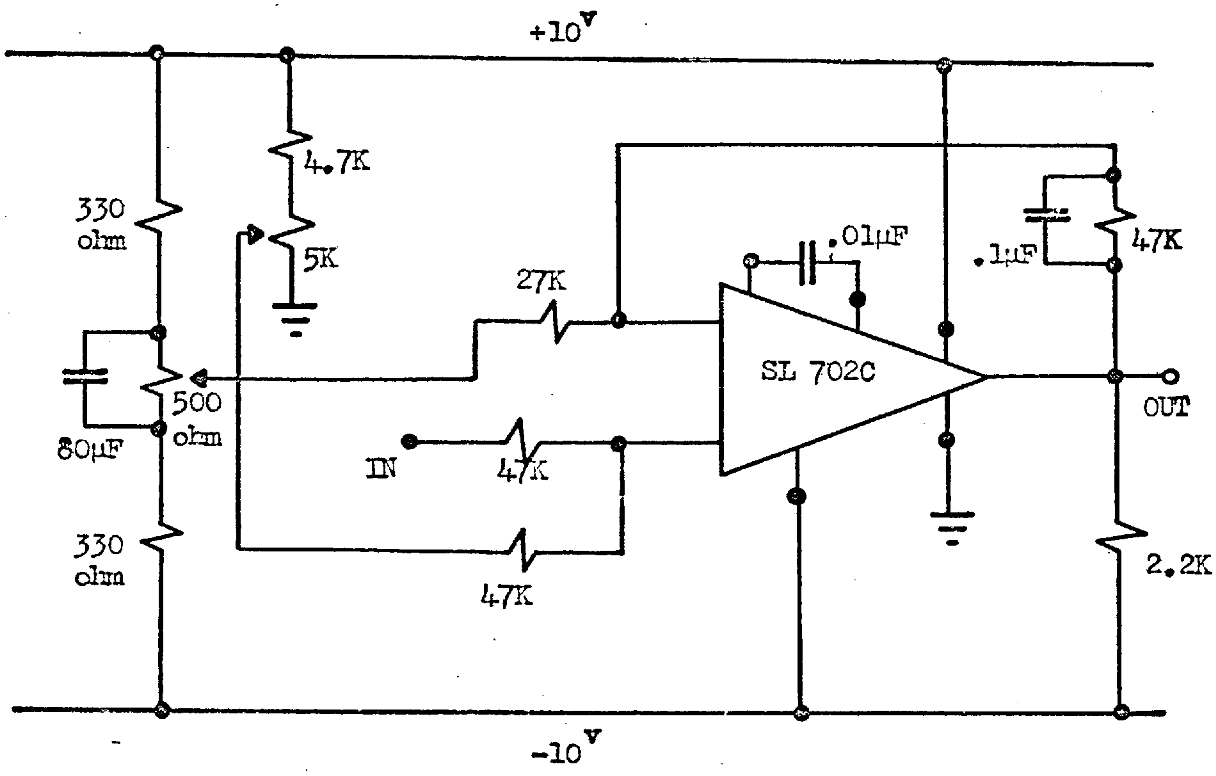


Fig 2.14 Linearity Check on Sample and Hold Section of C.E.A. Controller.



(a) Feedback Circuit.



(b) Amplifier Details.

Fig. 2.15 CFA Feedback Circuit and Amplifier Circuit Details.

circuit is shown in the results of fig. 2.14.

2.6.4. The Comparator Amplifier

The amplifier gain and time constants must be chosen for high gain, that is negligible variation of extinction angle over a wide range of overlap angles, and fast response to eliminate commutation failure. The most difficult design considerations arise with weak a.c. systems but it is found that performance is sensitive to smoothing inductor, transmission line and far-end characteristics as well. The parameters of the control amplifier for best performance are therefore individually tuned for any power system.

The amplifier circuit diagram is shown fig. 2.15(a) and (b) from which the transfer function of the operational amplifier section alone is written

$$\text{Vout} = V_g \quad k_1 \frac{1 + ST_1}{1 + ST_2} + V_{R1} \quad k_2 \frac{1 + ST_1}{1 + ST_2} - V_{R2} \quad k_3 \frac{1}{1 + ST_2}$$

V_g is the fed-back γ-minimum signal
V_{R1}, V_{R2} are reference level, i.e. angle, settings.

More accurately V_g above should be replaced by

$$V_g \quad \frac{1}{(1 + ST_3)(1 + ST_4)} \qquad \text{where } T_3 = 0.47 \text{ m s. } T_4 = 0.1 \text{ m s}$$

to take delays in other parts of the circuit into account; the twin-T transient response being neglected.

A typical set of values of the above parameters corresponding to the c.e.a. controller at the weak a.c. system of the three terminal system exhaustively investigated in this thesis are set out below:-

$k_1 = 1.37 \quad k_2 = 1.37 \quad k_3 = 1.74 \quad T_1 = 1.7\text{m s} \quad T_2 + 4.7\text{m s}$

2.6.5. The twin-T filter

A fast control with high gain has a tendency to 25 c/s auto-oscillations round the closed loop including the converter. These oscillations were eliminated by a sharply tuned (47 db peak, 20 db $\pm$ 5 c/s) twin-T 25 c/s band stop filter.

A rigorous analysis of 'comprehensive' control is very difficult due to its numerous non-linearities, a particularly intractable one is the minimum angle selection. The response of this device is sensitive to $\frac{d\gamma}{dt}$ in that the effective sampling rate is 20 m s and $\frac{20}{6}$ m s for positive and negative values of this quantity. Fig. 2.16 illustrates its response to monotonic increasing and monotonic decreasing values of γ. A second obstacle to conventional sampled data theory is that the response of the various elements is fast in comparison with the sampling frequency. For these reasons a brief description of how the oscillations arise is given in place of an analysis. The 25 c/s oscillation arises when only one valve is controlling the system throughout as may arise with unbalanced line voltages, controller maladjustment or current zero detector jitter. The signal fed back to the amplifier is of a square wave nature being alternately above and below the set value. The cyclic time of this square wave is 25 c/s, shown in fig. 2.17 (a).

Writing the amplifier transfer function in simplified form as

$$A(S) = \left(\frac{1 + ST_1}{1 + ST_2}\right) \cdot A$$

and the peak to peak value of the square wave input function as $\delta\gamma$ the operation equation for the firing angle oscillation is

$$\delta\beta(S) = \frac{A.\,\delta\gamma}{2} \cdot \frac{1 + ST_1}{(1 + ST_2)} \cdot \tanh\left(\frac{3T}{4}\right)$$

where T is the periodic time.

Selecting only the sustained oscillatory component of the

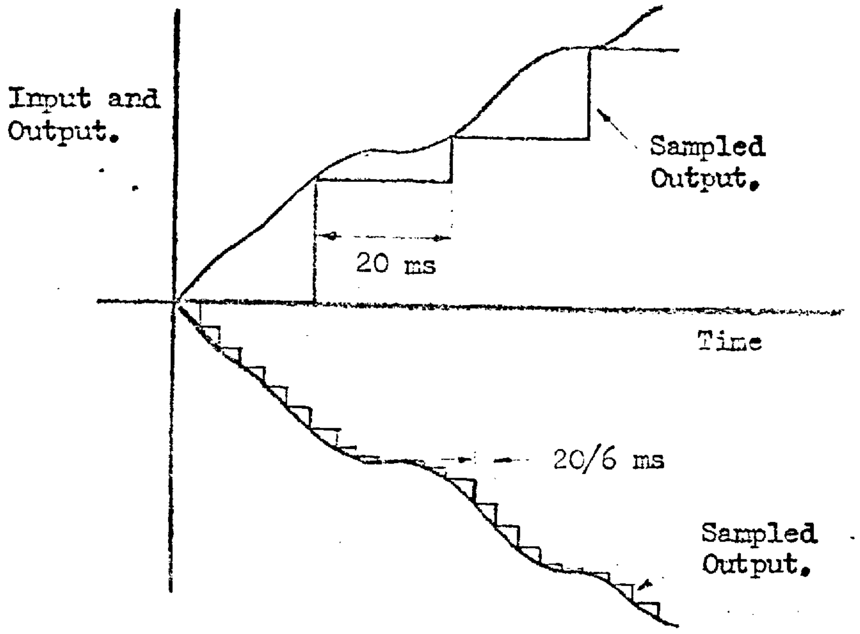


Fig 2.16 Diagram to illustrate the dependence of the Sampler/Selector apparent frequency on the sign of the time derivative of the input. The output for monotonic increasing and decreasing input signals is shown.

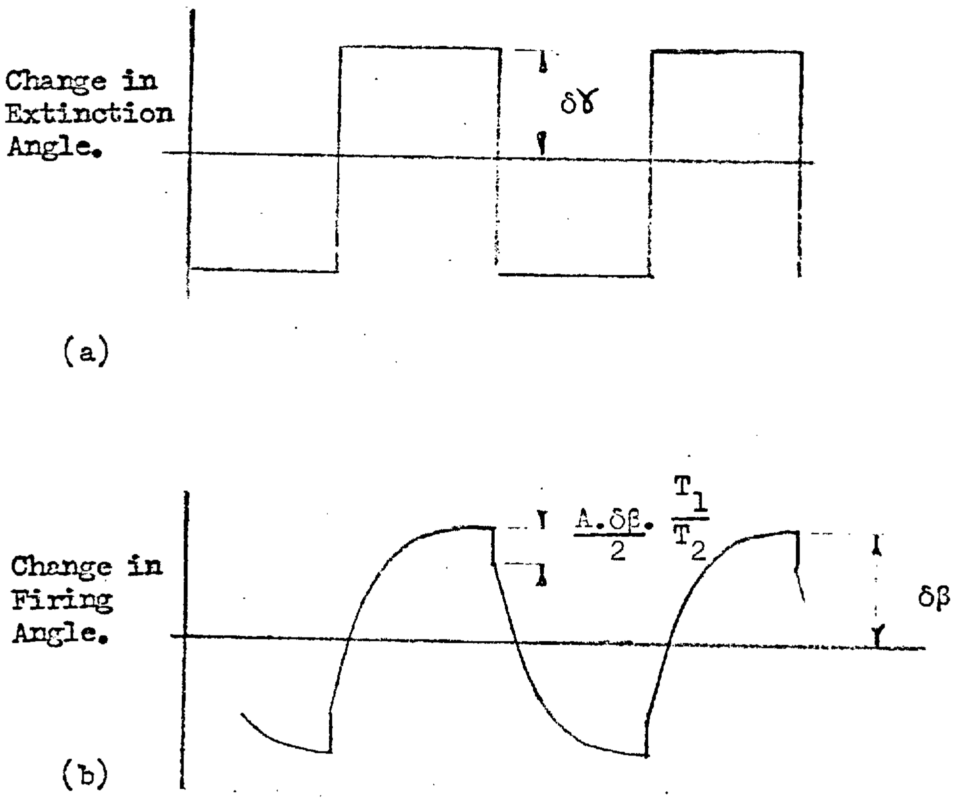


Fig 2.17 Diagram illustrating Oscillations.

inverse transform

$$\delta\beta(t) = \frac{A\ \delta\gamma}{2}\left(k_1 + k_2 + \left(1 + \frac{T_1 - T_2}{2}\right) e^{-\frac{t}{T_2}} \right)$$

where

$$k_1 = 0 \qquad nT < t < \frac{2n+1}{2} T$$

$$k_1 = -2\left(1 + \left(\frac{T_1 - T_2}{T_2}\right) \cdot e^{\frac{-(t - nT)}{T_2}}\right.$$

$$\frac{2n+1}{2} T < t \leq (n+1) T$$

$$k_2 = 0 \qquad t < nT$$

$$k_2 = 1 + \frac{T_1 - T_2}{T_2} \cdot e^{\frac{-(t - nT)}{T_2}} \qquad t > nT$$

This is plotted in fig. 2.17 (b) and corresponds closely to the firing angle signal observed on test.

Typical numerical values give

$$(\delta\beta) \text{ peak to peak} = 10 \text{ to } 15 \times (\delta\gamma) \text{ peak to peak} \qquad - (2.2)$$

Also the commutation equation

$$\cos\gamma = \frac{2XcI}{Vm} + \cos\beta \quad \text{yields}$$

$$\delta\gamma = \delta\beta \sqrt{1 - \left(\frac{4XcId}{Vm}\right.} \cot\gamma \cdot \operatorname{cosec}\gamma - \left(\frac{2XcI}{Vm}\right)^2 \operatorname{cosec}^2\gamma - \left(\frac{2Xc}{Vm\sin\gamma}\right).\delta I$$

Again with typical numerical values, $\gamma = 15^{o}$, $Xc = 3.14$
$Vm = 80^{V}$, $I = 5^{A}$

$$\delta\gamma = 3.2\,\delta\beta - 17.7\,\delta I \quad , \quad \delta\beta, \delta\gamma \text{ in degrees} \qquad - (2.3)$$

From equation (2.2) and (2.3) the possibility of sustained oscillations if δI is small enough are evident.

Similar effects are conceivable at 50 c/s and 150 c/s when two valves only control the firing angle or when all six valves oscillate on alternate firings. However after careful alignment neither of these effects caused any serious disturbance. This is explained by a well known property of sampled data systems; a stable sampled data system can become increasingly unstable as the sampling rate is decreased, that is, sampled data system may stabilise at higher sampling rates because in the limit, a continuous system possesses one pole less than the corresponding sampled data system. Time constants and gains in all parts of the loop have been 'optimised' by trial and error adjustments.

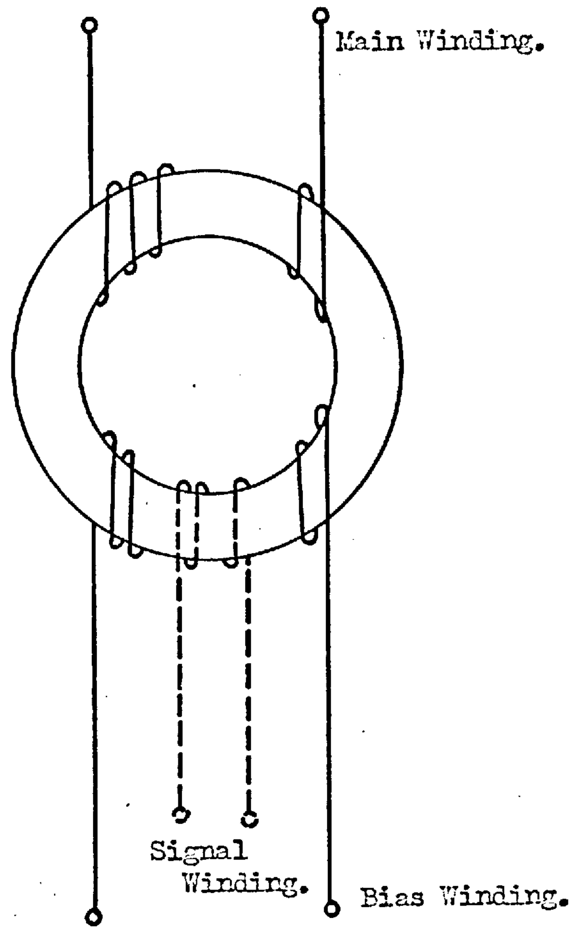
2.6.6. Monitoring of the valve current zero

A magnetic method is used to detect the valve current zero. A saturating toroid of HCR, a material with a narrow rectangular Hystereses loop,(69) carries three windings fig. 2.18(a). Bias current in one winding magnetises the core to point A, fig. 2.18 (b), but valve current in a second winding moves the magnetisation level to B. When valve current falls below 10 mA (0.3%) the magnetisation level is returned to A and the flux change is detected on the third signal winding. The smallest value of valve current whose zero can be accurately detected is approximately 0.3^{A} (10%) though this varies somewhat with bias current value.

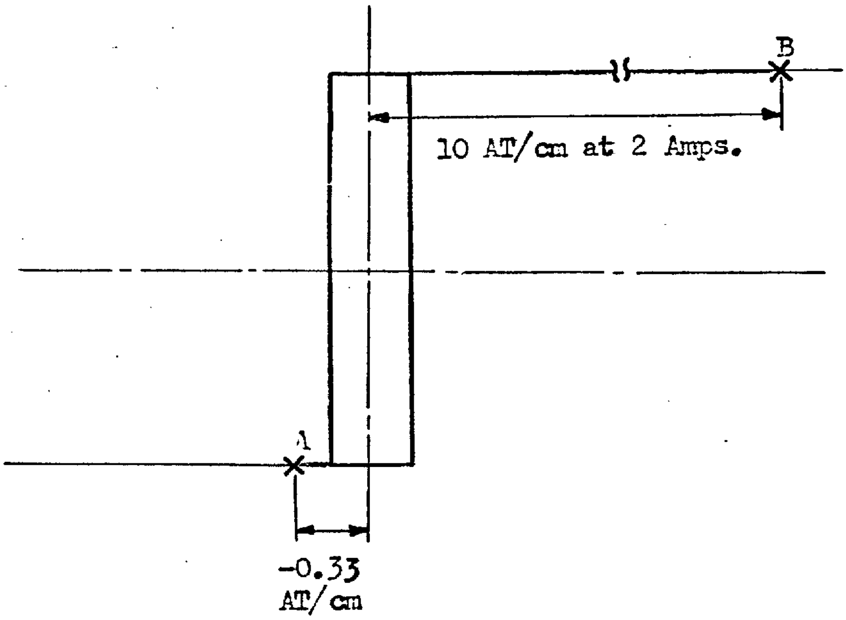
2.7. Constant Current Control (c.c.c.)

2.7.1. Particular considerations under fault conditions

Some questions relating to c.c.c. gain to preserve system



(a) Winding Arrangements.



(b) Magnetic Characteristics.

Fig. 2.18 Diagrams Relating to Valve Current Zero Detection.

stability have been considered in section 2.5 and here stability under fault conditions is briefly discussed as it is desirable that on line fault the converter should 'settle in' quickly with the minimum of commutation failure or transient oscillations. In faulted transmission systems the three converters can be regarded as three non-interacting units; an assumption exactly true for faults near the node but liable to some error if the fault position is at the terminal end of a capacitive inverter cable.

Any converter may now be taken separately as in fig. 2.19 a where r_1, depends on fault position. If the c.c.c. transfer function is approximately written

$$A(S) = \frac{A}{1 + ST}$$

the open loop system transfer function is

$$\frac{k \cdot (S + z)}{(1 + ST)(S - S_1)(S - \bar{S}_1)}$$

with

$$k = \frac{A \cdot V_{do} \cdot \sin\alpha}{L}$$

$$S_1, \bar{S}_1 = -\lambda \pm \partial$$

$$\lambda = \tfrac{1}{2}\left(\frac{1}{r_1 C} + \frac{r}{L}\right)$$

$$\partial = \sqrt{\left(\lambda^2 - \frac{r_1 + r}{LC\, r_1}\right)}$$

The pole zero pattern and 180° lines are sketched in fig. 2.19b where $p = -\left(\frac{1}{T} + \frac{r}{L}\right)$. Apparently the system is always stable, however the discrete nature of the converter control may be represented approximately by an additional pole at $S = -2/(\text{sampling rate})$, and a further cluster of distant poles arise from filtering etc. (D(S)). This will cause the 180° lines to move right as shown dotted but a small amount of phase advance will pro-

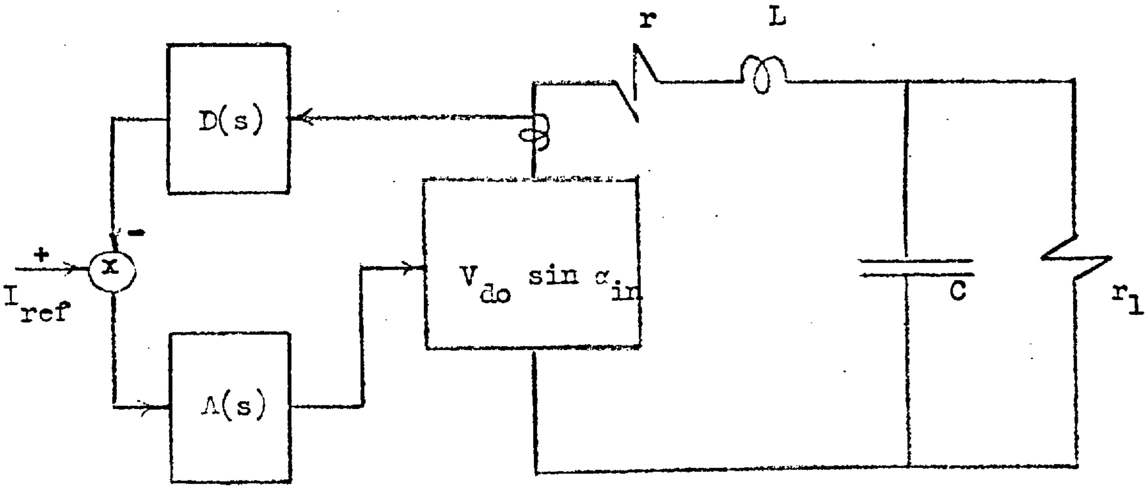


Fig 2.19a Mathematical Model for Stability Analysis of Converter on Fault.

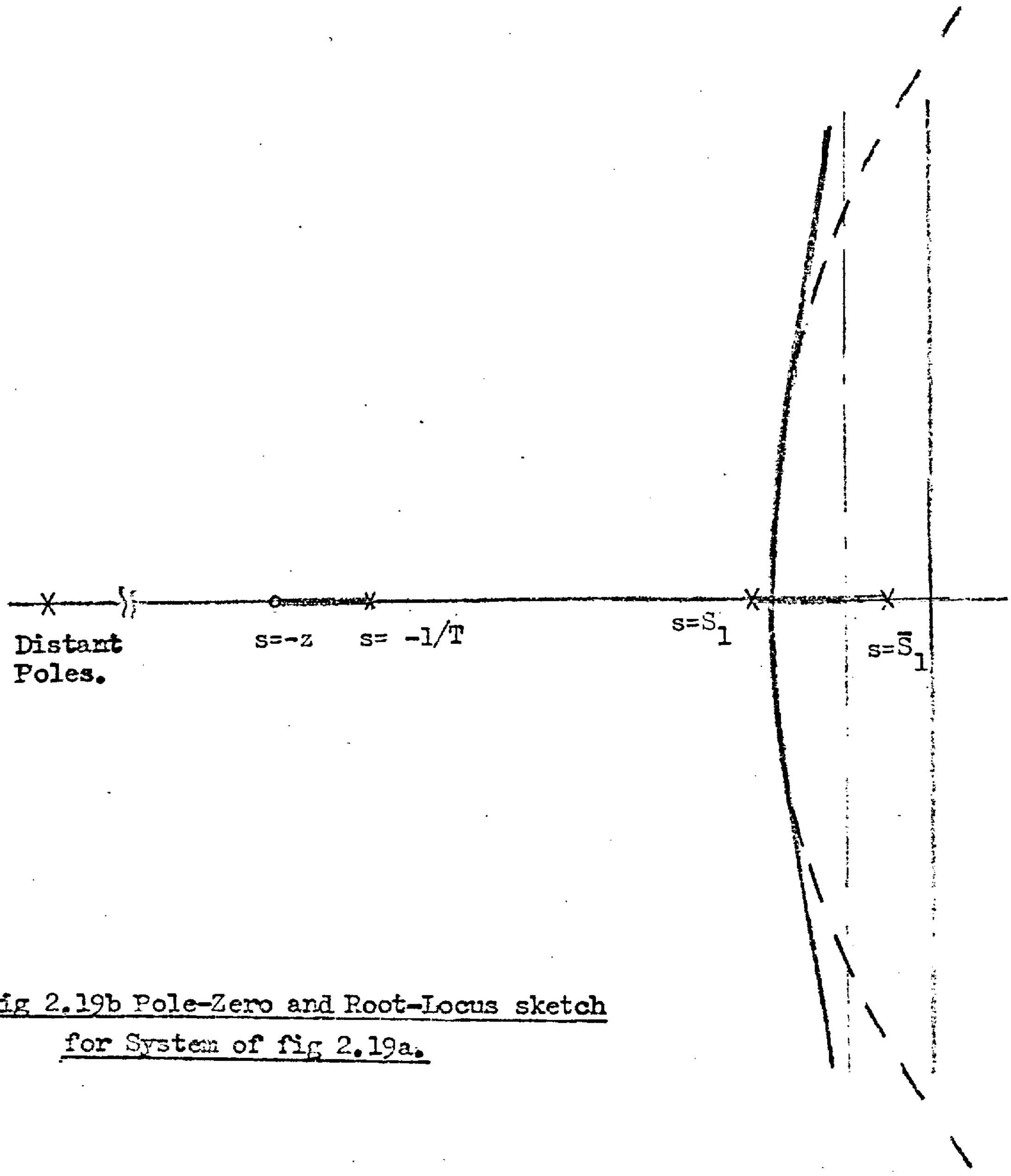


Fig 2.19b Pole-Zero and Root-Locus sketch for System of fig 2.19a.

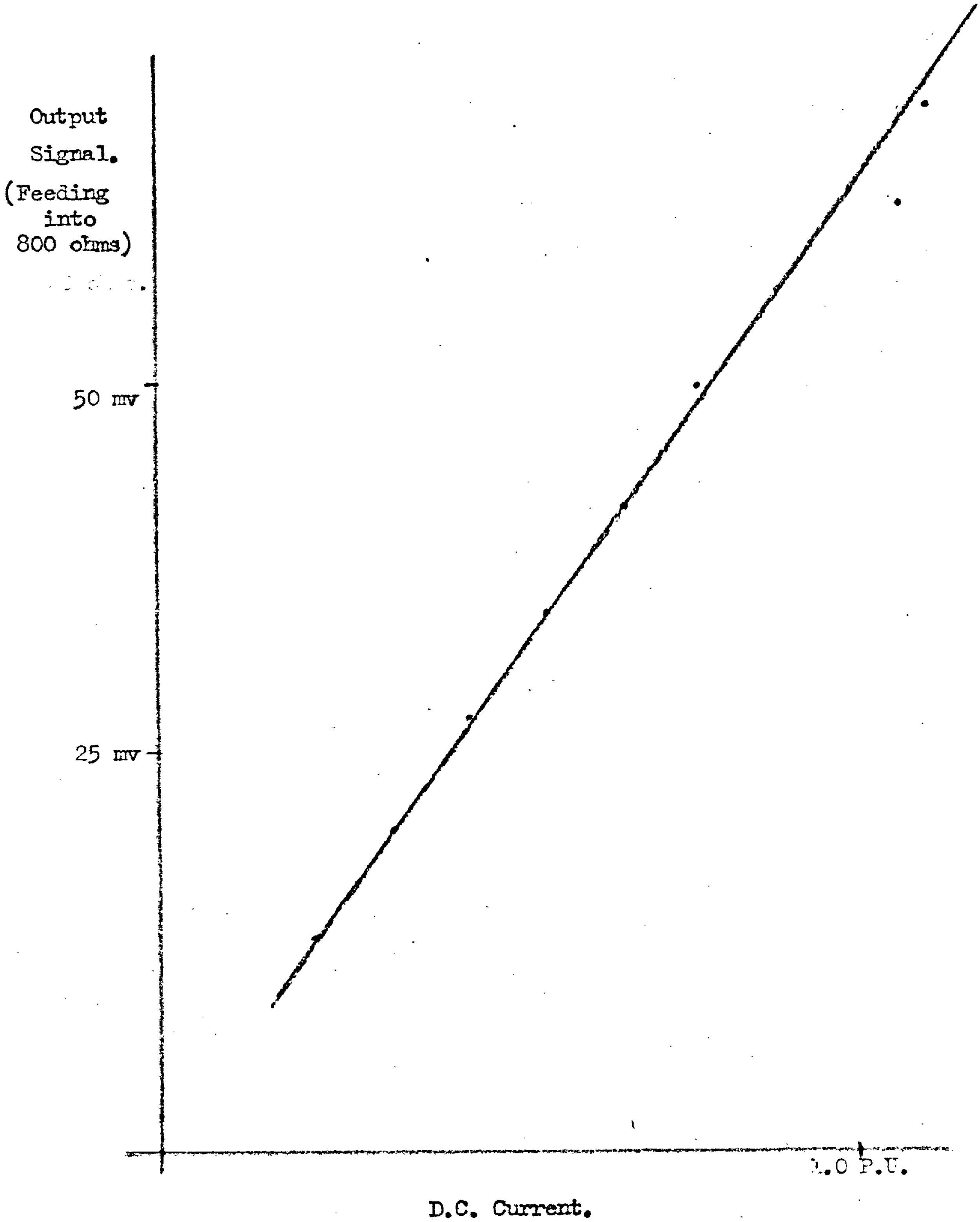


Fig 2.20 Hall Effect Device Characteristic.

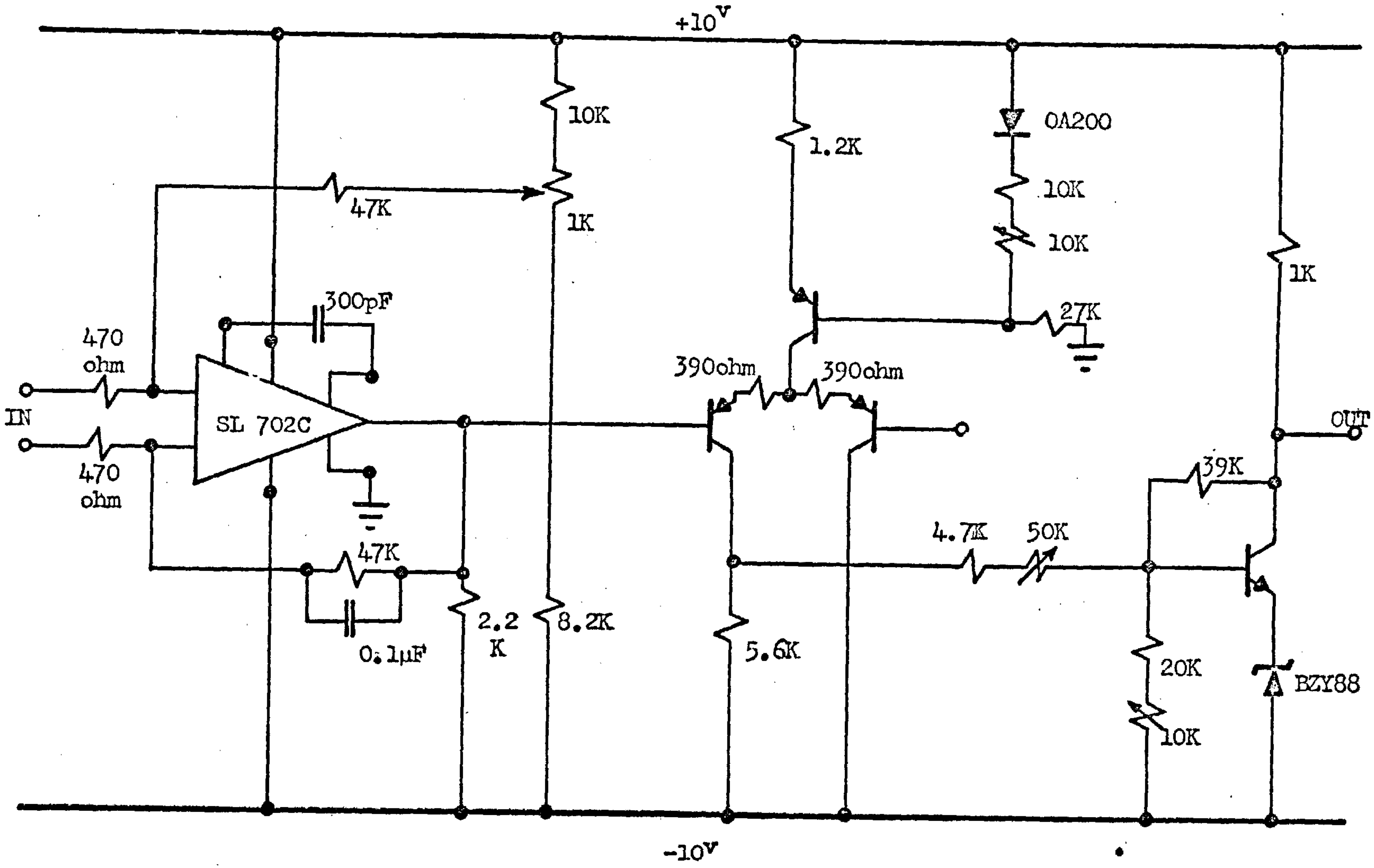


Fig. 2.21 Constant Current Control Amplifier.

duce a compensating distant zero. The c.c.c. transfer function was modified to

$$A(S) = \frac{A\ (1 + ST_2)}{(1 + ST_1)}$$

and this resulted in greatly improved performance during both normal operation and faults.

2.7.2. The d.c. current transformer

A current transformer is an essential element in a flexible simulator as it enables current measurement at voltages removed from earth. The saturating reactor type[70 - 71] was built but abandoned in favour of a Hall device[72] (AEI Mark IIIA Hall Field Probe). Fig. 2.20 is a plot of its characteristic when feeding an 800 ohm load with 75 m A in the constant current leads. The slope is 11 V/amp and the linearity is adequate ($\pm$0.5%) over the working range of 0-5^A. The effect of laboratory temperature drift is not significant being below 0.1% per $^\circ$C.

2.7.3. The C.C.C. Amplifier

The basic component of the amplifier is a Plessy SL702C integrated circuit module. An integrated circuit was chosen for its low drift and ease of circuit construction. The Hall device output is fed to the integrated circuit, the output is compared with a reference setting in a standard design difference amplifier and the control signal taken to the thyristor grid pulsing units via buffers. See fig. 2.21.

The principal time constant is chosen for fast response and with special reference to d.c. harmonic suppression. Clearly the control should be insensitive to the 300 c/s ripple but fast in comparison with the a.c. frequency of 50 c/s. The variation in gain is under the control of the operator at VR3.

Low gain has adverse effects on system controllability while higher gain creates dangers of instability as previously discussed.

There are also limitations to the phase advance that can be used as the system must not be responsive to spurious signals.

The transfer function of the operational amplifier element of fig. 2.21 is

$$\text{Vout} = -100 \left(\frac{1 + ST_1}{1 + ST_2} e_1 - \frac{1}{1 + ST_2} e_2 \right)$$

where e_1 and e_2 are the double ended output voltages from the Hall effect current transformer and typically

$T_2 = 4.7$ m s

$T_1 = 0.5$ m s

The output stage transfer function is

$$\text{Control voltage} = G. \left(\frac{1}{1 + ST} \right) \text{ x signal from comparator}$$

where T = 0.4m s
G = variable gain setting. Set at VR3

2.8. Other Control Circuits

2.8.1. The bypass valve control circuit

This is in principle the same as the original circuit developed in ref. (63); circuit diagram fig. 2.22. A free running 30 kc/s square-wave oscillator is continuously running and its output pulses are either gated to the bypass valve grid transformer or held suppressed by a bistable gate which is switched on and off as required by external control signals.

The largest possible operating delay is equal to one mark-time of the oscillator i.e. 15 μs.

2.8.2. The Inverter Recovery Unit

This is a simple monostable which when triggered injects a voltage pulse to the inverter pulsing units to transiently move the advance angle β beyond 60^{o} for one or two firing periods. In the unexcited state the circuit output voltage is at the ceiling value of 10^{V} and is therefore ignored by the control selection panel. Circuit diagram: fig. 2.23.

2.8.3. The Control Selection Unit

This panel, fig. 2.24, selects from all the controllers the appropriate control signal to be transmitted to the pulsing units. A second function of this circuit is to impose a minimum β limit on the inverter firing angle as suggested in[36, 39]. These authors have, as would be done on an h.v.d.c. converter, made β minimum equal to the minimum extinction angle on the ETL simulator in Japan. However a thyristor bridge with $\beta = 10^{o}$ to 20^{o} is a good deal more reliable than a mercury arc rectifier and for this reason the minimum β setting has been reduced to between 5^{o} and 10^{o}. Also see last paragraph of section 2.2.

2.9. Valve Damping Circuits

Valve damping series R - C circuits are connected in parallel with H.V.D.C. converter valves to limit the rate of rise of voltage and the voltage overshoot at the instant of valve current extinction when the anode-cathode space is still ionised. Busemann[73] attempted to formulate design criteria by breaking down the circuit into simple oscillatory networks each defining a normal mode of system oscillation. The method however suffers from many approximations and an over emphasis of the effects of stray capacity, and from the design point of view, the limiting of the rate of rise of recovery voltage is also

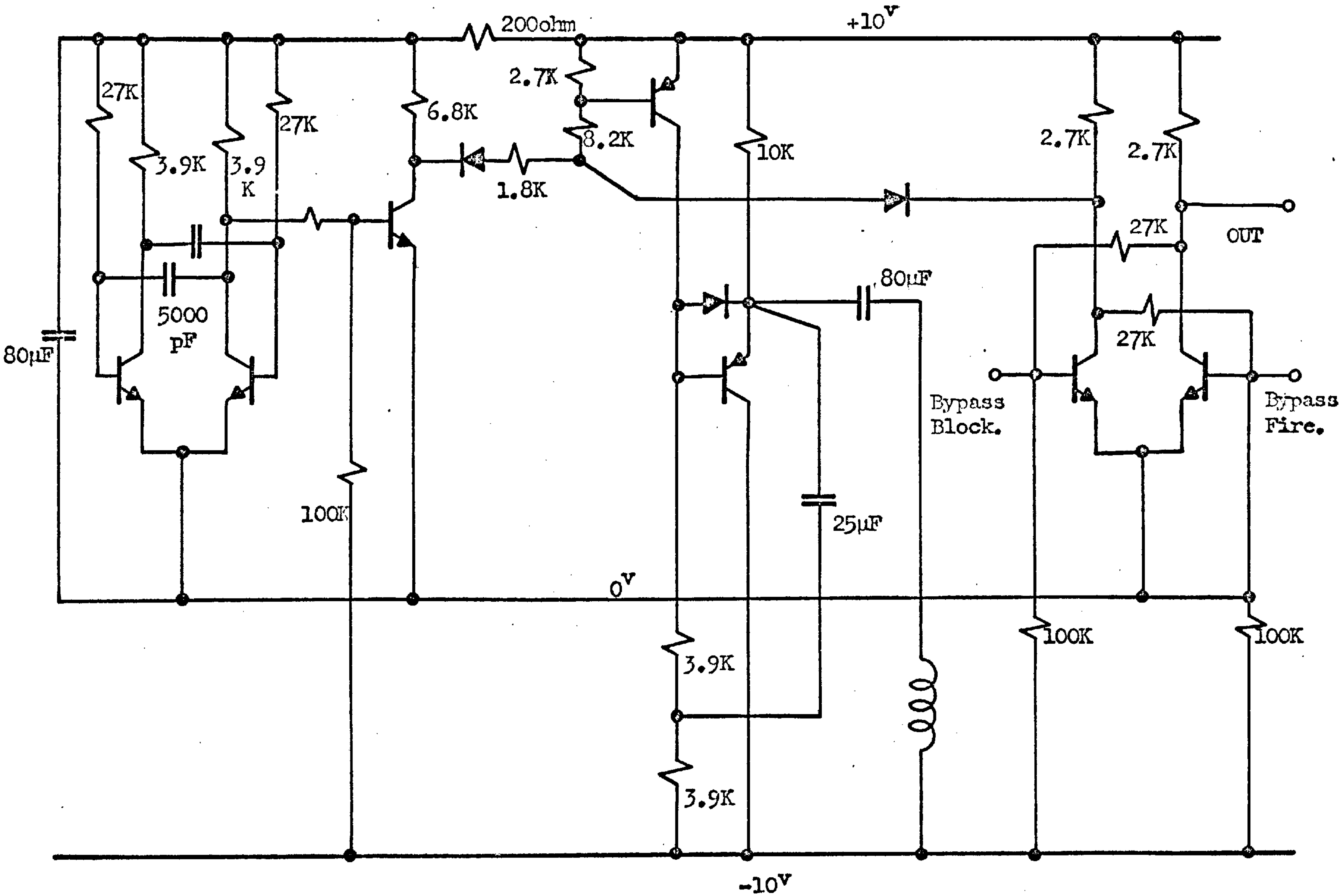


Fig. 2.22 Bypass Valve Control Circuit.

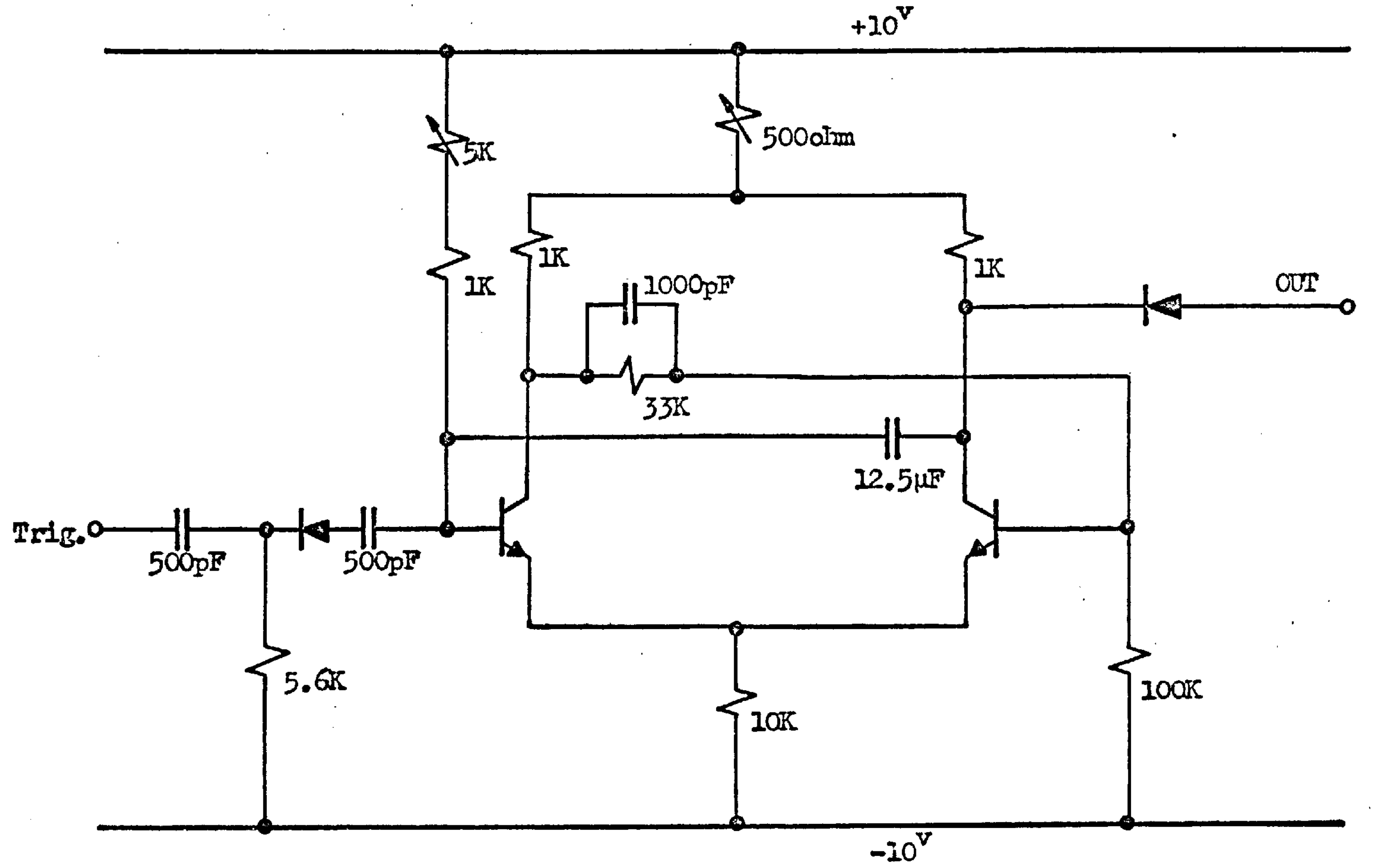


Fig. 2.23 Inverter Recovery Unit.

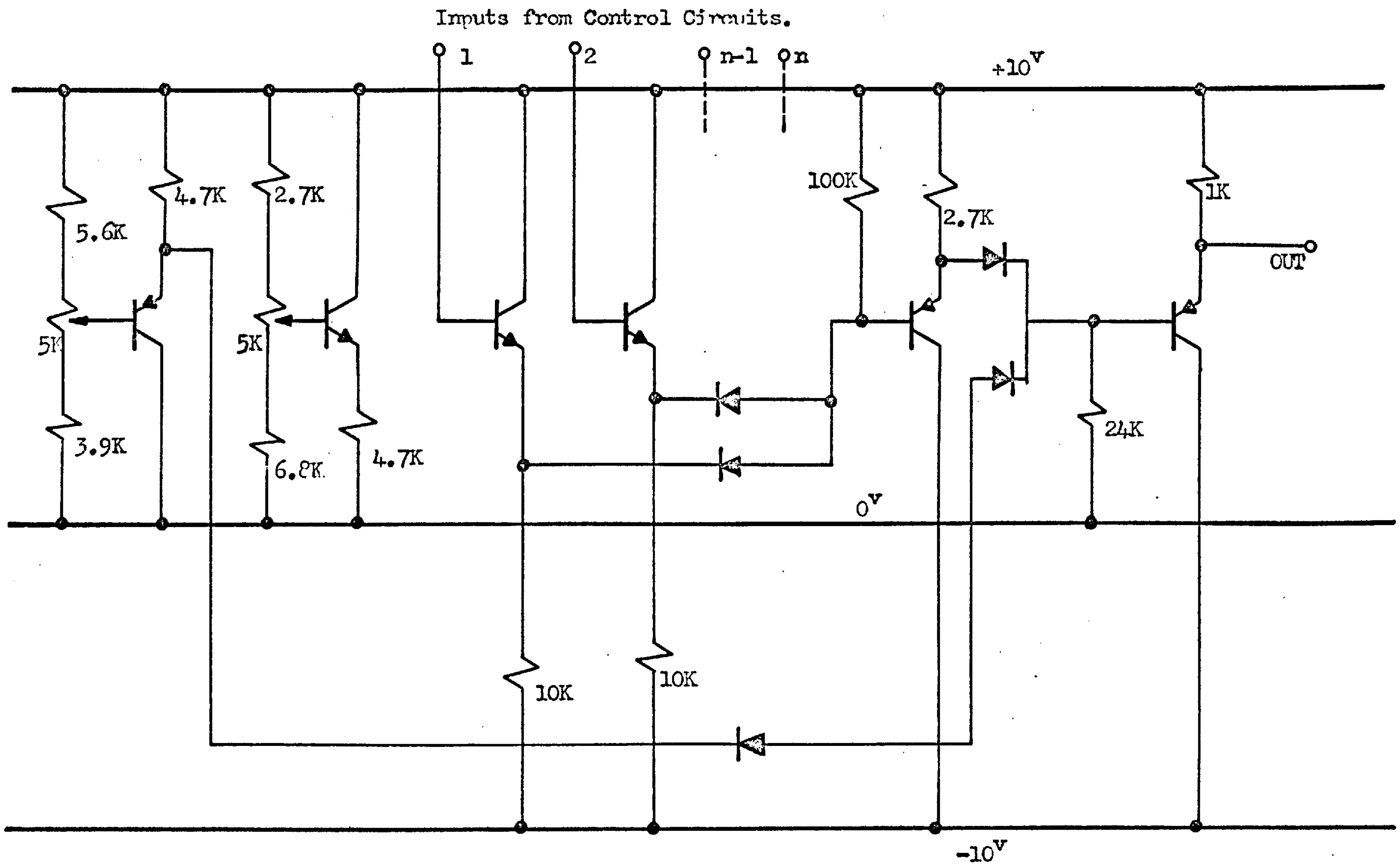


Fig. 2.24 Control Selection Unit.

neglected. The design criteria proposed by Ainsworth[74] can be used to give satisfactory results.

2.9.1. Analysis of damping effects

The bridge circuit immediately after the current zero in valve 1, that is with valves 2 and 3 conducting is as in fig. 2.25.a and is re-arranged in fig. 2.25.b in a form suitable for analysis. Stray capacitance is neglected. V_j is the commutation jump voltage across the valve and is represented by two equal parts one in each phase. The operational equation for the voltage across the valve is given by

$$V(S) = \frac{(1 + SRC)\,(2 + 2SRC + 9S^2LC)}{(1 + SRC + S^2 \,.\, 3\,LC)} \cdot \frac{V_j}{2S} \cdot \frac{1}{(1+SRC+S^2 \cdot 5LC)}$$

and the time solution is

$$v(t) = -\sqrt{2}\;V_L \sin(\alpha + u)\Big\{\tfrac{3}{4}\Big(1 + e^{\frac{-\pi x_1}{\sqrt{M_1}}}\Big(\frac{\sin \pi x_1 \sqrt{4 - \frac{1}{M_1}}}{\sqrt{4M_1 - 1}} - \cos \pi x_1 \sqrt{4 - \frac{1}{M_1}}\Big)\Big)$$

$$+ \tfrac{1}{4}\Big(1 + e^{\frac{-\pi x_2}{\sqrt{M_2}}}\Big(\frac{\sin \pi x_2 \sqrt{4 - \frac{1}{M_2}}}{\sqrt{(4M_2 - 1)}}$$

$$- \cos \pi x_2 \sqrt{4 - \frac{1}{M_2}}\Big)\Big)\Big\}$$

where

$$V_j = -\sqrt{2}\,V_L \sin(\alpha + u)$$
$x_1, x_2 = {}^{t}/_{2\sqrt{3LC}}$ and ${}^{t}/_{2\sqrt{5LC}}$ resp.

M_1, M_2 = 3M and 5M resp.

M = L/R^2C

t = time after current zero

L = commutating inductance per phase

This solution is obtained from an equivalent circuit that is more straightforward than that used by Ainsworth(74). Both solutions however should be identical, but the latter has suffered at the hands of the printer.

The conditions for critical damping apparently are $R = \sqrt{\left(\frac{20L}{C}\right)}$ and $R = \sqrt{\left(\frac{12L}{C}\right)}$ but Ainsworth(26) rightly points out that since the values of C required for limiting the rate of rise of recovery voltage are much larger than stray capacitances critical damping in the sense of no overshoot cannot be achieved.

2.9.2. Inverter damping circuit design

An acceptable rate of rise of recovery voltage across the valve after current extinction is 2kv/ μs or on the model scale, $R_v = 2v/\mu s$. The commutating reactance L calculated from a.c. system conditions for the weak a.c. system = 9.1 mH.

Taking inverter operation at $\gamma = 15^o$
and a transformer secondary voltage of 80^v

$$0.4 \times 2\pi\sqrt{LC} = \frac{V_L \cdot \sin\gamma}{Rv}$$

$$C = 0.007\ \mu F \quad \text{use} \quad 0.01\ \mu F$$

From the critical damping conditions of $R = \sqrt{\left(\frac{20L}{C}\right)}$ and $\sqrt{\left(\frac{12L}{C}\right)}$

R = 3 to 4k approximately

A value of 2.7k was found to give best results on the simulator.

The valve damping circuits at the other converters were similarly designed.

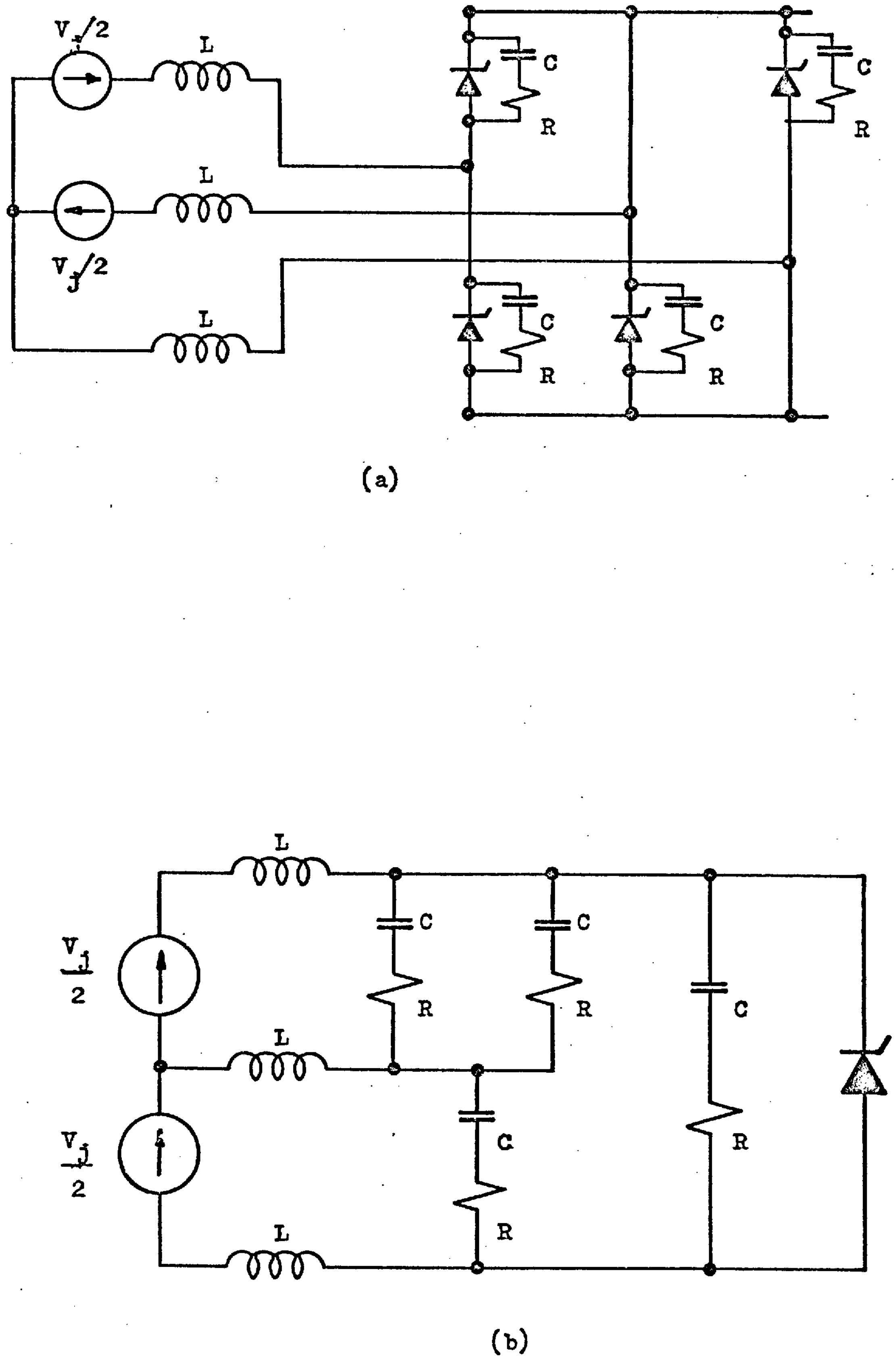


Fig. 2.25 Circuits for Analysing Valve Damping Effects.

Converter	R	C
Rectifier	1K	0.1 μF
Inverter 1	2.2K	0.05 μF
Inverter 2	2.7K	0.01 μF

In no case could the oscillation overshoot be completely removed.

2.10. Conclusions

The design and synthesis of the controls necessary for a flexible h.v.d.c. system model suitable for multiterminal studies has been described and the final circuits shown. The analytical considerations used as an aid to design are indicated but the final adjustments have been made on the model. The control details are to a high degree dependent on the characteristics of the a.c. systems and on the transmission line parameters, with the result that h.v.d.c. system controls are in a sense tailor made. The objective at all times was to build a fast, closely controllable simulator free from system instability and commutation faults during transients.

CHAPTER 3

Performance of the Simulator

3.1. Introduction

In this chapter the performance of the simulator will be described in some detail. As outlined below the emphasis in these tests is on transient response; the steady state characteristics of h.v.d.c. systems has been fully discussed in the literature in the form of voltage-current characteristics[42, 48, 67, 75]. The response of the individual controls are shown by a series of tests on a single bridge where the output signals of the constant current controller and the constant extinction angle controller together with the firing angle control signal and the measured extinction angle are recorded. The response of the three terminal inter-connected system is obtained from a second set of tests where step changes of order are communicated to the system controllers. The three converter voltages and currents and the voltage at the d.c. transmission line node point are recorded on these tests.

It is necessary to investigate the extent to which the single pole 3-bridge studies conducted here can be extended to 2-pole 6-bridge operation. In particular it would appear reasonable to assume that the behaviour of a 3-bridge system during pole to neutral faults can be identified with that of a 6-bridge system during pole to pole faults. The only essential difference between these two conditions is the 6-pulse and 12-pulse nature of the converter output d.c. voltage and the corresponding difference in the frequency of the discrete control exercised by the converter control circuits. A mathematical model suitable for a comparison of this nature is proposed and the 6-pulse and 12-pulse converter characteristics are compared.

3.2. The proposed Mathematical Model

The d.c. converter is inherently a discretely controlled device in that control action is effective only at six (or twelve) instants in the a.c. cycle. In the interval between the instants of selection of firing angles the control signal exercises no influence on the converter. With sampled data theory in view the mathematical model of fig. 3.1 is proposed. S is on position 1 for an investigation of constant current control and in position 2 for constant extinction angle control. Linearised parameters are used throughout and therefore this discussion is strictly applicable to small disturbances only; it will be seen later that this restriction is not as serious as it appears.

The converter is represented by an amplitude term $V_{do} \sin \alpha_{in}$ a sampler of frequency 1/T and a zero order hold circuit. The input to this converter 'box' is $\delta\alpha$ the change of firing angle from its quiescent value α_{in}. T = 20/6 MS and 20/12 MS for six and twelve pulse converter operation respectively. In addition

A(S) is the constant current controller amplifier transfer function

G(S) is the transfer function of extinction angle determining process

H(S) is the transfer function of c.e.a. amplifier

Y(S) represents the operational admittance of transmission line

The transmission line is represented by the lumped parameter equivalent circuit of fig. 3.2 where the far end resistance r_3 can be positive or negative depending on the terminal equipment. l_1, l_2 are predominantly due to the smoothing inductors.

The z transform operational equation of the converter is given by

$$i(z) = k. \frac{(1 - z^{-1}) \cdot Z_t \left(\frac{Y(S)}{S}\right) \cdot Z_t \left(A(S) \cdot \delta I(S)\right)}{1 - (1 - z^{-1}) \cdot Z_t \left(k.A(S) \cdot \frac{Y(S)}{S}\right)} \qquad - (3.1)$$

- for constant current control

and

$$i(z) = k. \frac{(1 - z^{-1}) \cdot Z_t \left(\frac{Y(S)}{S}\right) : Z_t \left(H(S) \cdot \delta Y(S)\right)}{1 + (1 - z^{-1}) \cdot Z_t \left(k. H(S) \cdot \frac{Y(S)}{S} \cdot G(S)\right)} \qquad - (3.2)$$

- for c.e.a. control

Where $k = V_{do} \cdot \sin \alpha_{in}$

$\delta I(S)$, $\delta Y(S)$ are the operational input disturbing functions

Z_t $\equiv$ z transform of

$$Z_t(F(S)) = \frac{1}{2\pi j} \int_{\lambda_1 - j\infty}^{\lambda_1 + j\infty} \frac{F(p)}{1 - e^{-T(S-p)}} \cdot dp$$

Equations 3.1,3.2 may be derived by an extinsion of results in ref(76)

p is a dummy variable of integration and λ_1 lies within the abscissa of convergence

$z = e^{ST}$

Equations (3.1) (3.2) show that in sampled data systems it is not always possible to write equations of the form

Operational Output Quantity = transfer function x operational input quantity

In order to form an equation of this type where the response function of the converter alone may be separated and examined the disturbing function $\delta\alpha(S)$ is introduced into the grid control signal as shown in fig. 3.3.

The system operational equations with c.c. and c.e.a. control now become respectively

$$i(z) = (-k) \frac{Z_t\left(\frac{Y(S)}{S}\right)}{1 - (1 - z^{-1}) \cdot Z_t\left(k.A(S) \cdot \frac{Y(S)}{S}\right)} \cdot Z_t(\delta\alpha(S)) \qquad - (3.3)$$

and

$$i(z) = (-k) \frac{Z_t\left(\frac{Y(S)}{S}\right)}{1 - (1 - z^{-1}) \cdot Z_t\left(k.\, H(S).\, G(S). \frac{Y(S)}{S}\right)} \cdot Z_t(\delta\alpha(S)) \qquad - (3.4)$$

It is now possible to postulate two closed loop system transfer functions,

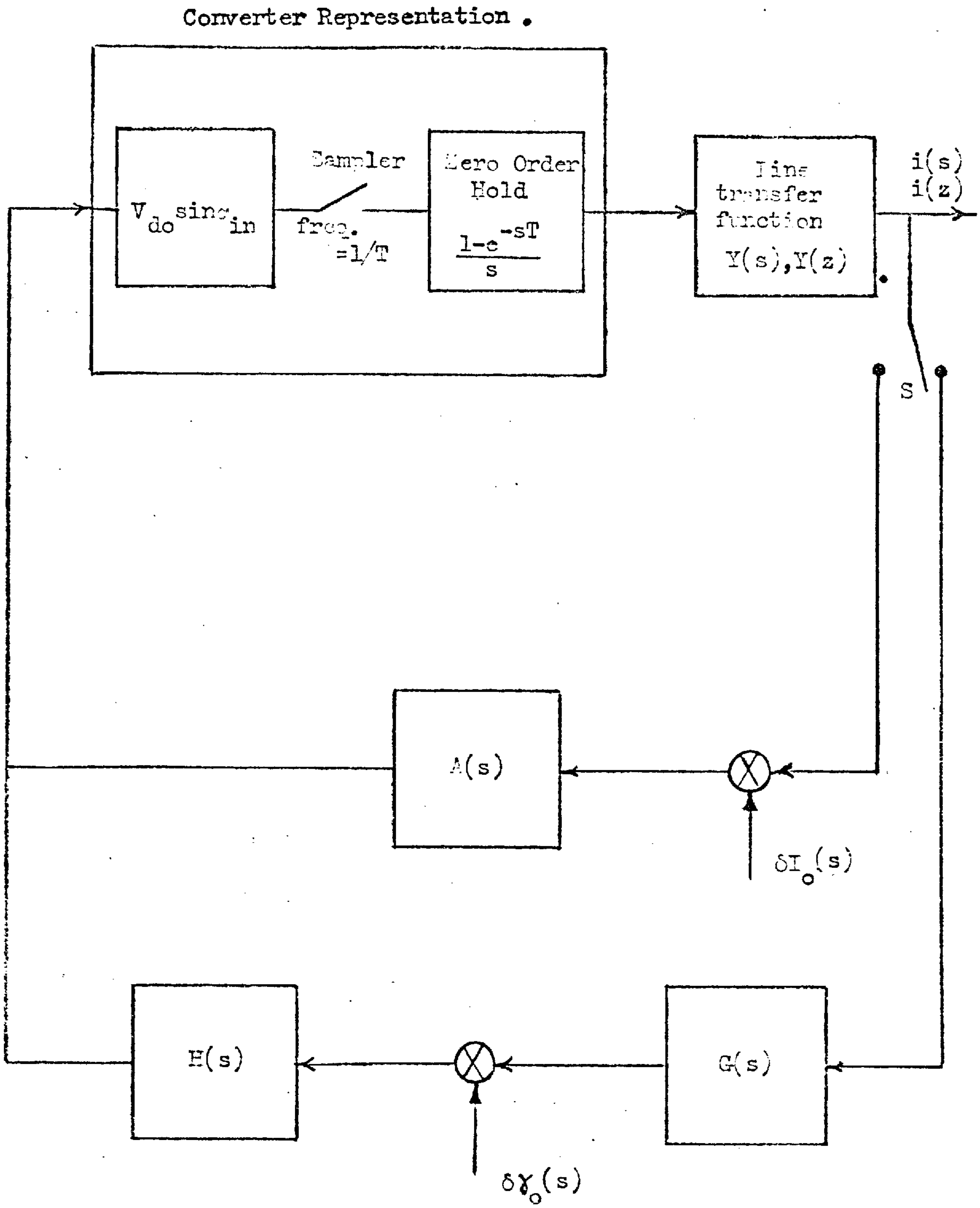


Fig 3.1 Mathematical Model for the comparison of 6 and 12-Pulse Systems.

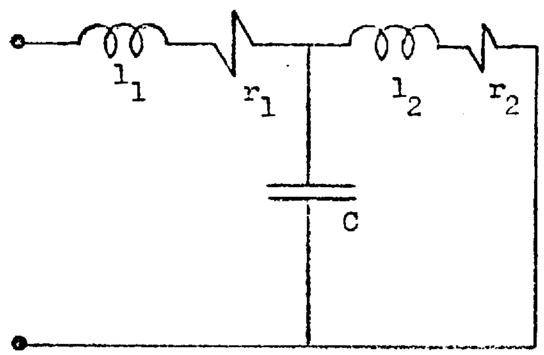


Fig 3.2 Circuit for determination of Y(s),Y(z).

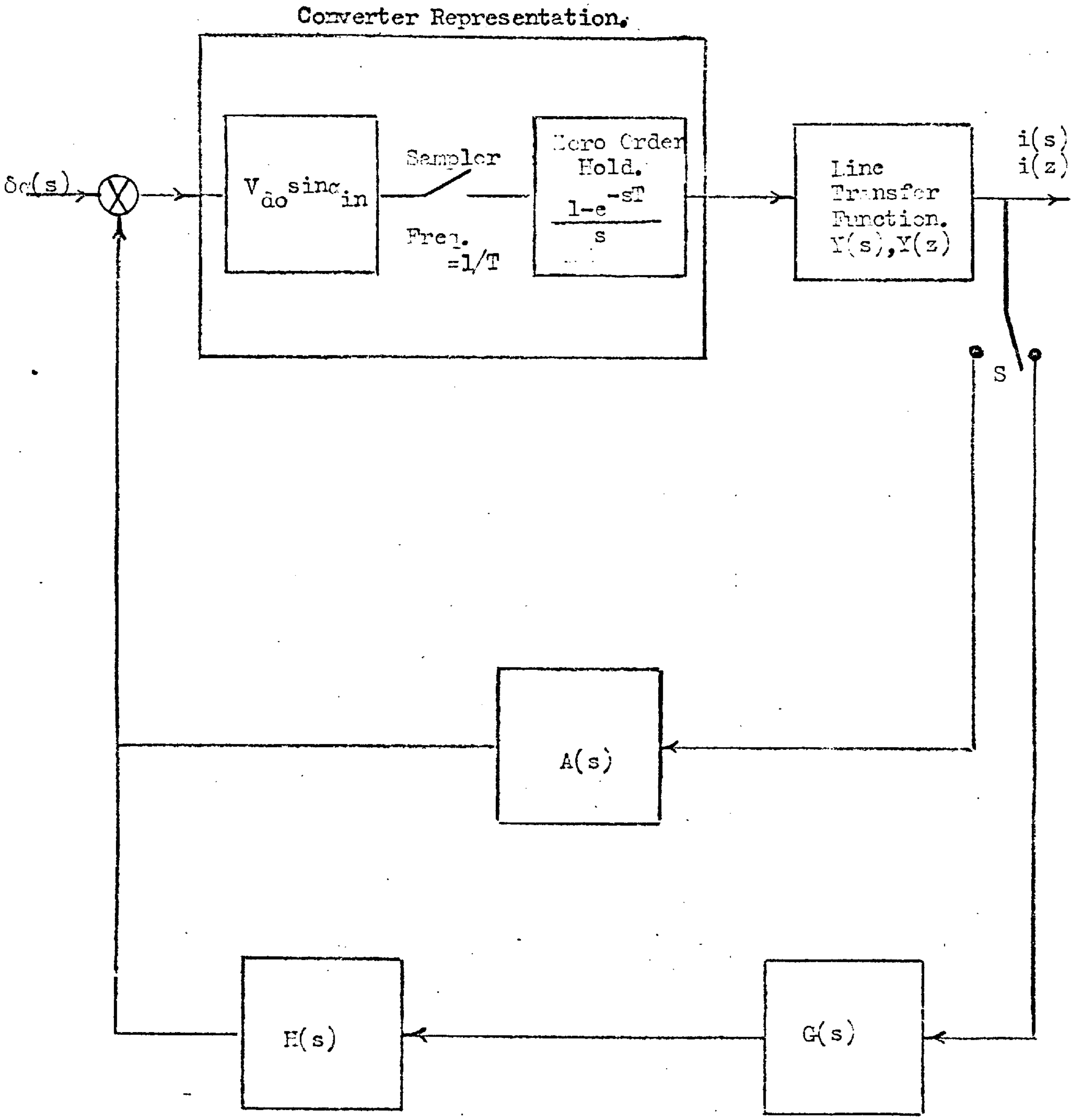


Fig 3.3 Modified Mathematical Model

$$\frac{Z_t \left(\frac{Y(S)}{S} \right)}{1 - (1 - z^{-1}) \cdot Z_t \left(k.A(S). \frac{Y(S)}{S}\right)} \qquad - (3.5)$$

- for c.c. control

and

$$\frac{Z_t \left(\frac{Y(S)}{S} \right)}{1 - (1 - z^{-1}) \cdot Z_t \left(k.\ H(S).\ G(S). \frac{Y(S)}{S}\right)} \qquad - (3.6)$$

- for c.e.a. control

and investigate the behaviour of both for sampling rates corresponding to 6-pulse and 12-pulse operation. The constant current control is examined in detail in the next section.

3.3. 6-Pulse and 12-Pulse System Comparison

Inserting numerical values the z-transforms of expression (3.5) are readily determined by conventional methods and thereafter alternative methods for comparing 6-pulse and 12-pulse operation are employed.

In the first method the frequency response of the transfer function is determined and plotted on a Bode diagram. A large number of diagrams were obtained for various parameter values and two typical sets corresponding to c.c. control principal time constant value of 5ms and 20ms are shown fig.3.5. a, and fig. 3.5. b respectively.

In order to obtain these diagrams for 6-pulse and 12-pulse operation the following substitutions require to be made.

$z = e^{ST}$

$S = 0 + j\ 2\ \pi\ f$; f = frequency

$T = 20/6$ ms for 6-pulse and

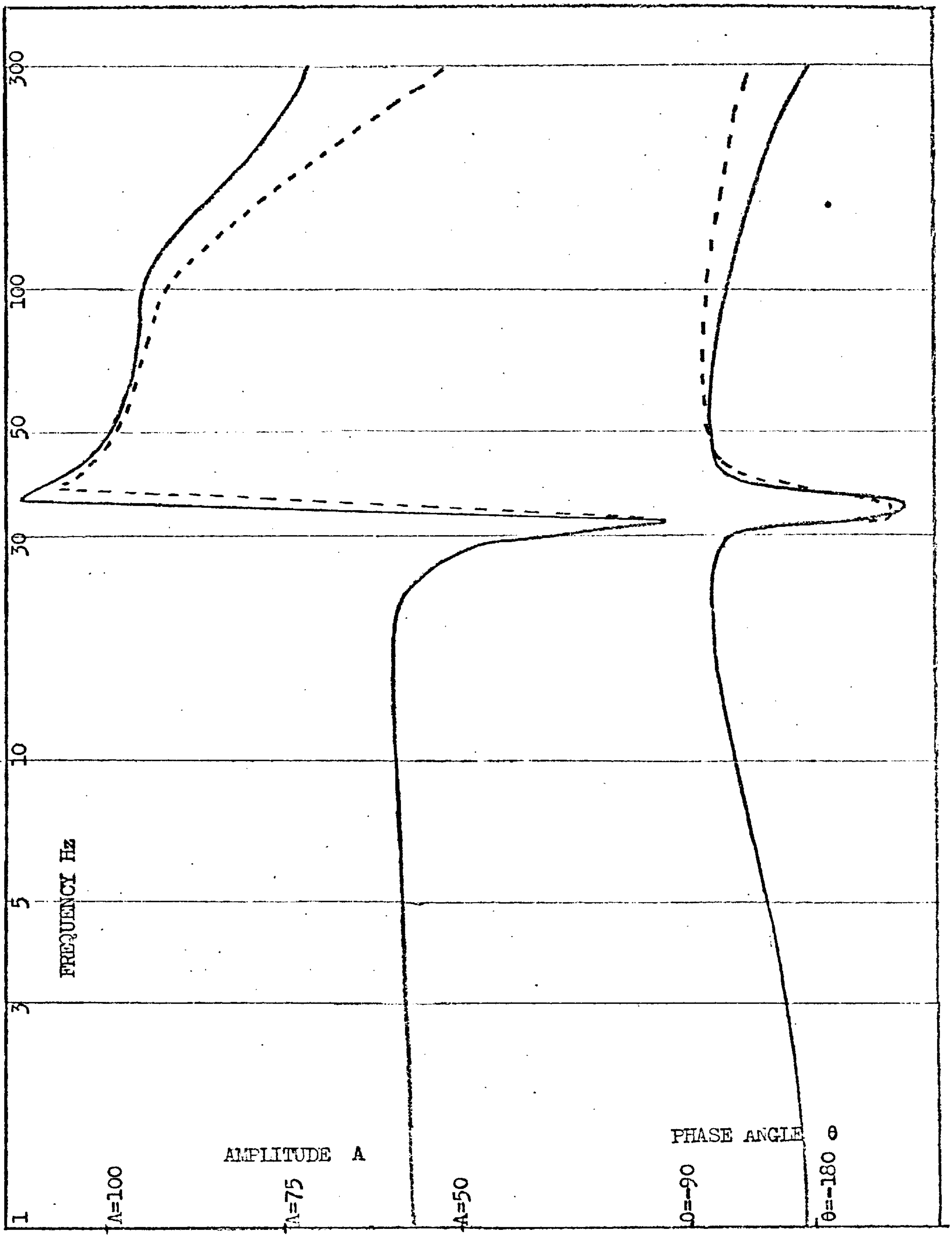
$20/12$ ms for 12-pulse working

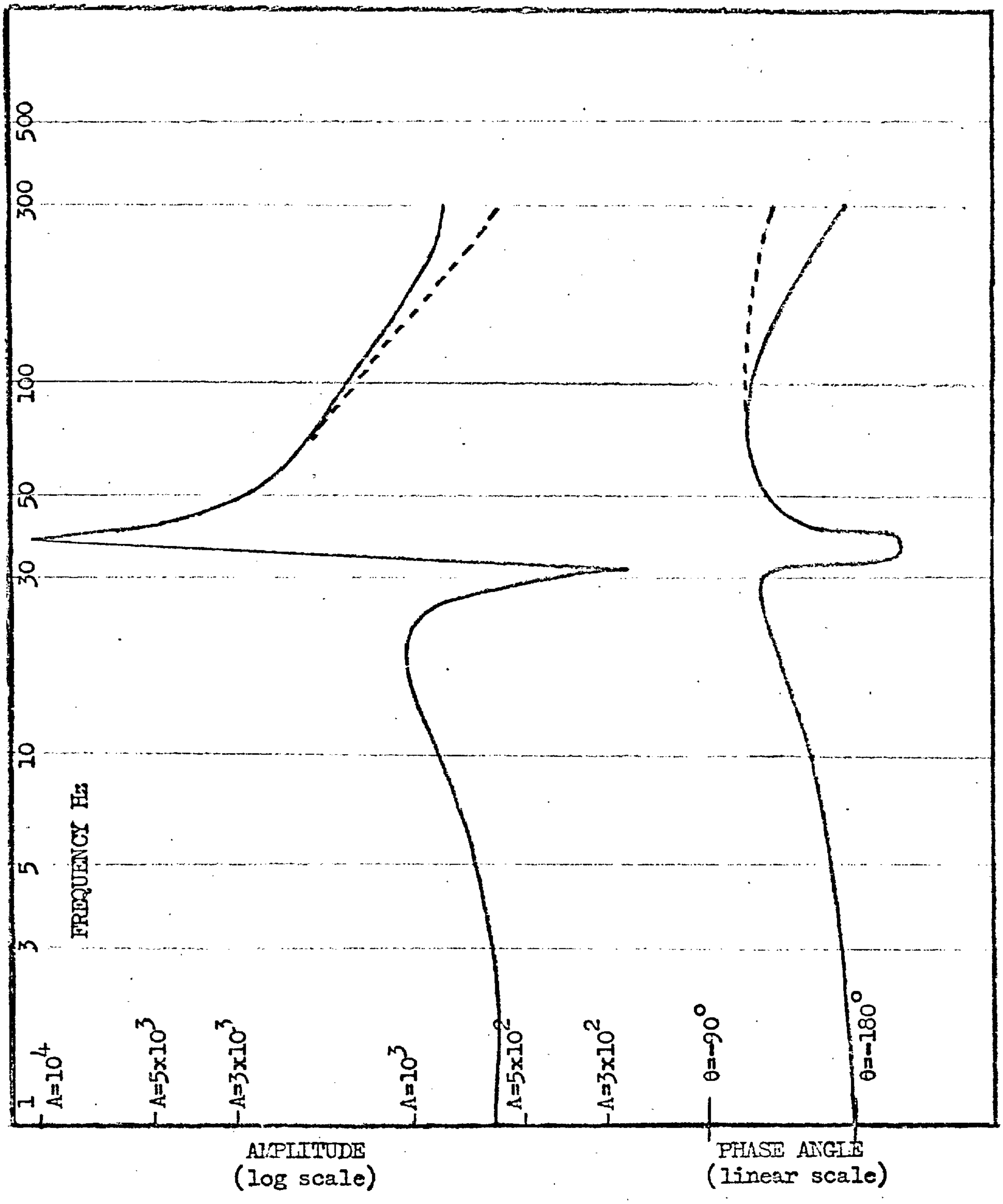
The general conclusion that can be made is that there is negligible difference between 6 and 12 pulse working for

Fig. 3.5a Bode Diagrams for the comparison of 6 and 12-Pulse Systems.

(c.c. control principal time constant value = 5 mS)

——————— 6-Pulse.   – – – 12-Pulse.





———— 6-Pulse.   – – – – 12-Pulse.

(c.c.control principal time constant value = 20 mS)

Fig. 3.5b Bode Diagrams for the comparison of 6 and 12-Pulse Systems.

frequencies less than 100 c/s. It is also found that increasing line capacitance further reduces these differences as can be anticipated from the increased electrical inertia of the system. Consequently the 6-pulse and 12-pulse system behaviour are closer to each other for cable networks than overhead lines.

The second method of comparison, used as a check on the above results is to re-write equations 3.3, 3.4 in the alternative form

$$i(s) = \frac{\left(\frac{1 - e^{-ST}}{ST}\right) . Y(S)}{1 + \frac{1}{T} \sum_{-\infty}^{+\infty} F(S + jn\,\omega_r)} \cdot \sum_{-\infty}^{+\infty} (S + jn\,\omega_r)$$

where n = 1, 2 ...

$\omega_r = 2\pi$ x sampling frequency

$$F(S) = -k\left(\frac{1 - e^{-ST}}{S}\right) . Y(S) . A(S) \text{ for c.c. control}$$

$$F(S) = -k\left(\frac{1 - e^{-ST}}{S}\right) . Y(S) . G(S) . H(S) \text{ for c.e.a. control}$$

Neglecting all values of $n > 1$ and approximating $\left(\frac{1 - e^{-ST}}{ST}\right)$ to $(1 - \frac{ST}{2})$ the transfer function of c.c. control can be written

$$\frac{Y_N(S).A_D(S).(1 - \frac{ST}{2})}{\begin{array}{l}\left(Y_D(S).A_D(S) - k(1 - \frac{ST}{2}).Y_N(S).A_N(S)\right) + \left(Y_D(S+\omega_r).A_D(S+\omega_r)\right. \\ \left. - k\left(1 - \frac{(S+\omega_r)T}{2}\right) . Y_N(S+\omega_r).A_N(S+\omega_r)\right) \\ + \left(Y_D(S-\omega_r).A_D(S-\omega_r) - k\left(1 - \frac{(S-\omega_r)T}{2}\right).Y_N(S-\omega_r).A_N(S-\omega_r)\right)\end{array}}$$

where subscripts N, D refer to the individual numerator and denominator polynomials of Y(S) and A(S).

It is now possible to obtain the poles and residues of this function for $T = \frac{20}{6}$ ms and $T = \frac{20}{12}$ ms and thus compare the characteristic modes of the 6-pulse and 12-pulse systems.

The fifth order polynomial has one pole on the real axis, near S = -1 and the difference in residue value and pole position at this pole is less than 1% between 6-pulse and 12-pulse operation. A pair of poles are located near the imaginary axis between 20 c/s and 40 c/s for normal parameter range. The residue at this pole is negligibly small and its influence can be neglected. A second pair of poles is located near the imaginary axis between 30 c/s and 45 c/s. The difference in pole positions and residue values between 6-pulse and 12-pulse operation at this pole does not usually exceed 5 - 10%.

3.4. Steady state characteristics

The frequency response plots for the c.c. control amplifier and the c.e.a. control amplifier are plotted in fig. 3.6. and 3.7 respectively. In the latter case the influence of the 25 c/s filter is easily discernible.

The Hall device current transformer has a frequency response better than 50 kc/s and a temperature co-efficient less than 0.1% /^{o}C.

The constant current control characteristics are variable between a slope of 50 p.u. d.c. impedance base and 5 p.u. d.c. impedance base on the potentiometer VR.3 fig. 2.21. Fig. 3. is a plot of the typical constant current characteristics of the rectifier in the system used in the majority of tests discussed in the following chapters.

The droop of the voltage-current characteristic of an inverter depends on the a.c. system reactance and this negative resistance is an important factor in system stability discussions. The characteristics of fig. 3.9 correspond to the weak a.c. system of the subsequent three terminal studies. The disproportionally large a.c. side resistance drop of model systems has been discussed previously and the characteristics of fig. 3.9 have been corrected for this effect. The thyristor drops have been ignored and may be regarded as a constant value

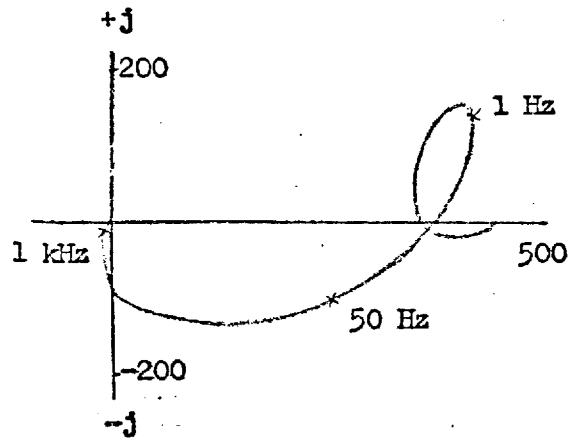


Fig. 3.6 Gain Characteristic of Constant Current Control Amplifier with Phase-Advance.

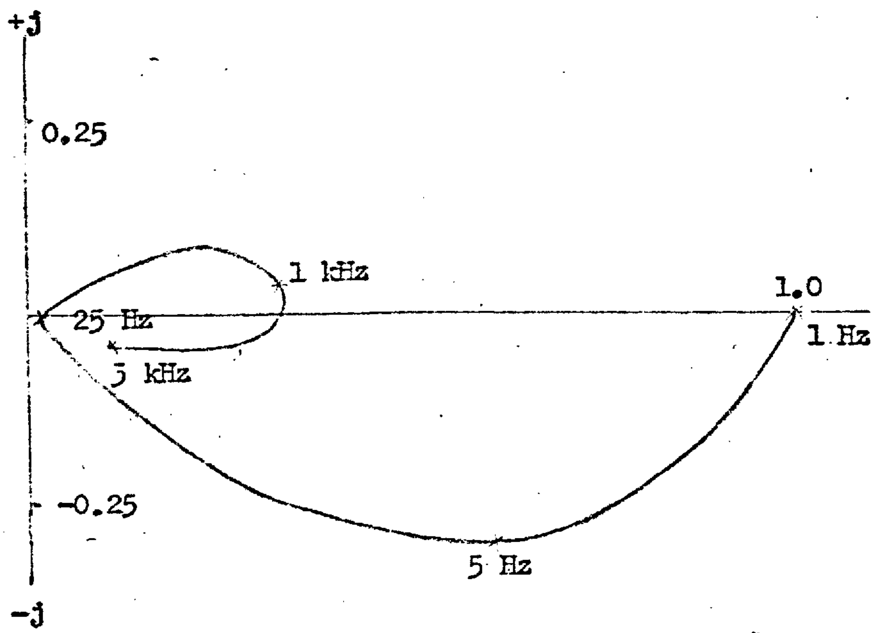


Fig. 3.7 Gain Characteristic of CEA Control Amplifier with Phase-Advance and Twin-T Filter.

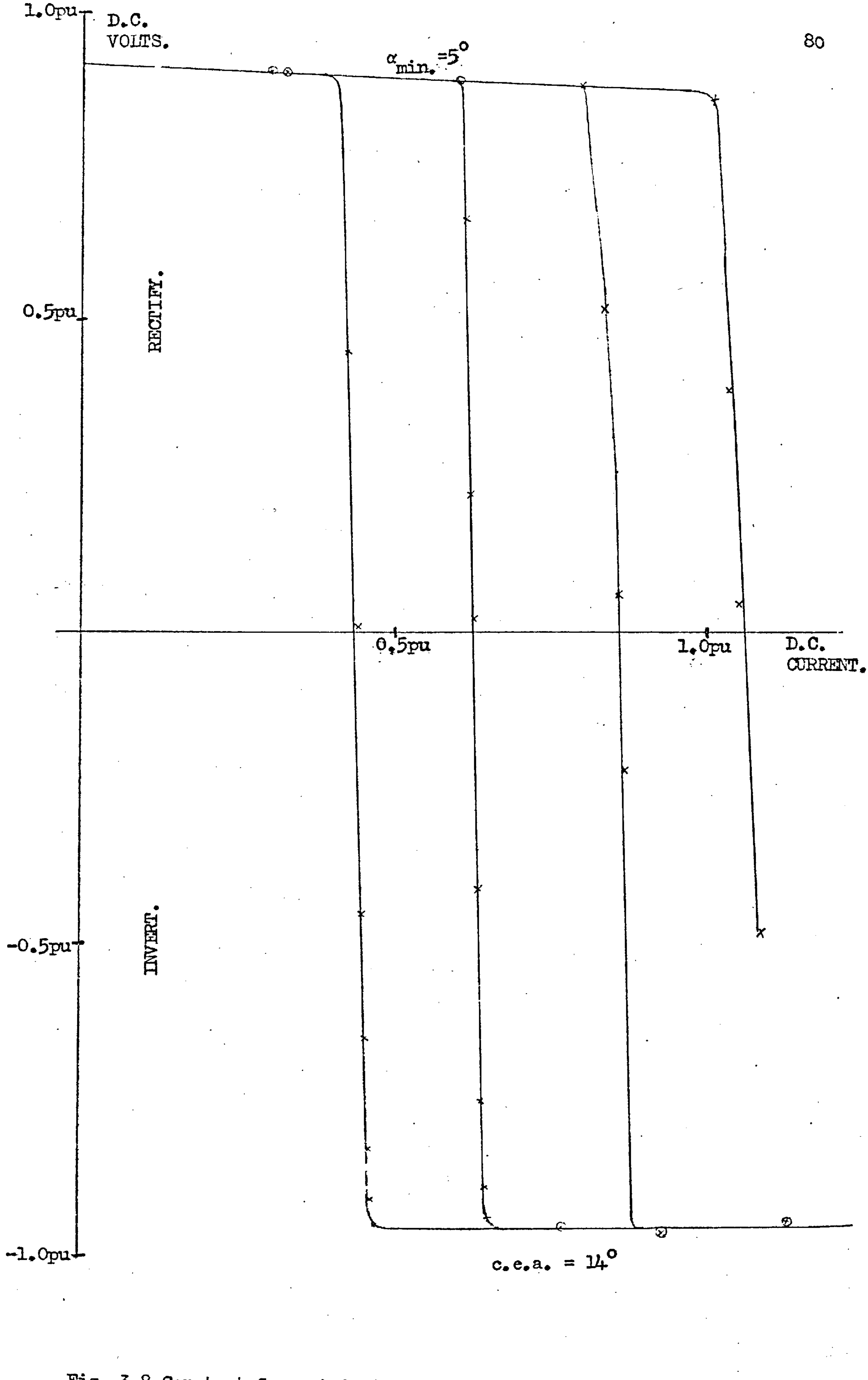
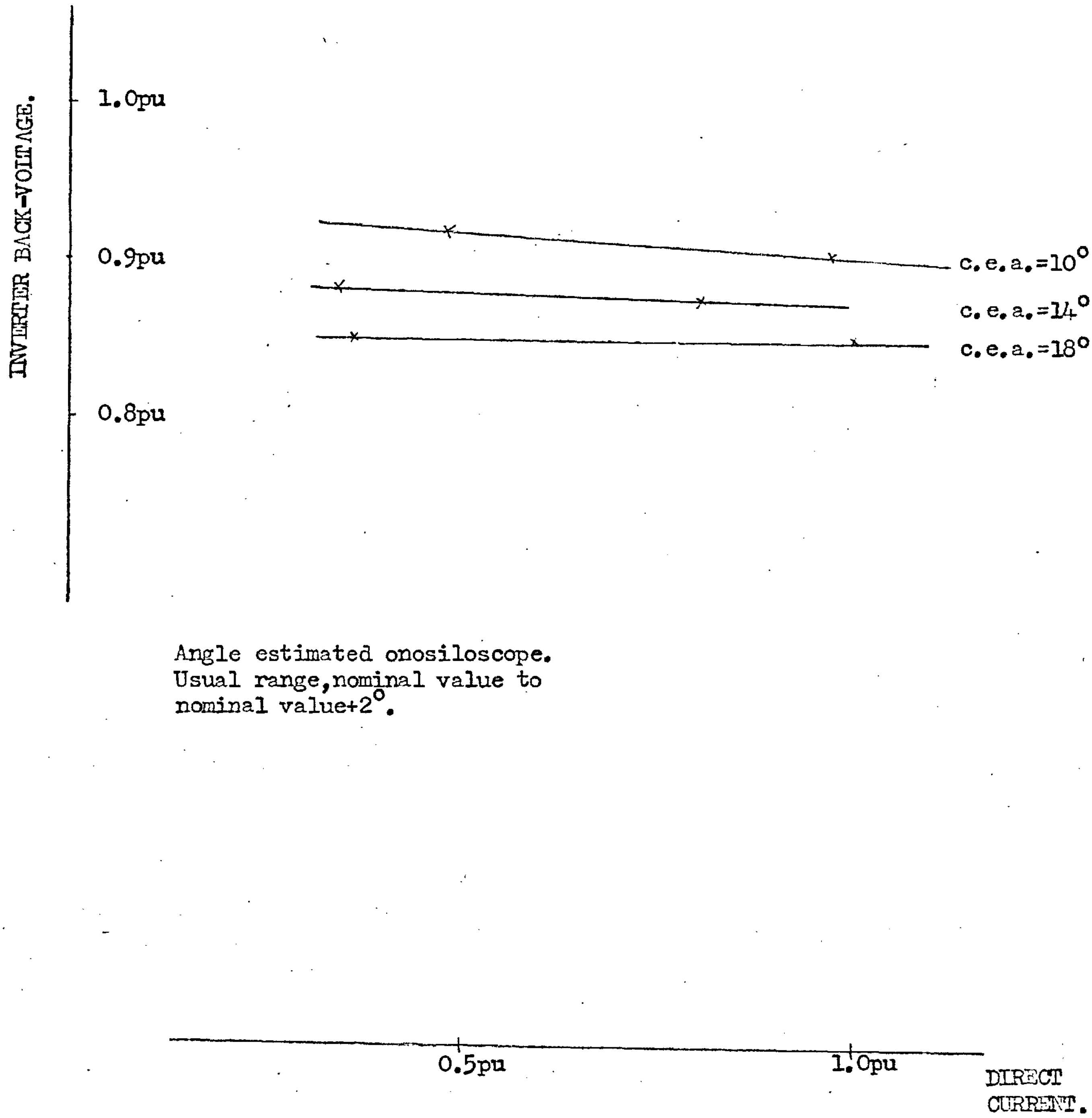


Fig. 3.8 Constant Current Control Characteristics at various Current Settings



Angle estimated onosiloscope.
Usual range,nominal value to
nominal value+2°.

Fig. 3.9 CEA Control Characteristics.

of about 3^V adding to the inverter back voltage. The pulsing units were carefully aligned to give an accurate 60^o firing interval between thyristors over the range $\alpha = 0^o$ to near 180^o; an accuracy of about 0.5% being obtained.

Due to phase voltage unbalance in the laboratory mains supply and the resulting shift of line voltage zeros a difference of about 2^o has always been observed among the six extinction angles. The shift of line voltage zero per 1% magnitude unbalance in phase voltage is about 0.32^o and the change of commutation angle of a typical $\beta = 30^o, \gamma = 15^o$ inverter per 1% magnitude change in the commutating voltage is about 0.22 degrees. A phase voltage phase angle unbalance introduces an angular error of half its value into the effective extinction angle.

3.5. Single Bridge Tests

The purpose of these tests was to monitor the input and output signals of the individual converter controls and their interactions, for step changes of control input signal and for transition from one controller to another. In order to eliminate completely the effects of the interaction of the controls at different terminals of a multiterminal system the tests were made with one converter only connected on the d.c. side through the smoothing inductor either to a resistive load or to a constant d.c. source in series with a resistance.

In interpreting the grid control signal and the control amplifier output signals it is to be noted that an increase of control voltage linearly increases the firing angle α over the range $4.2^V/\alpha = 0^o$ to $7.3^V/\alpha = 180^o$.

3.5.1. Step Changes of Current Order

A step increase was applied to the reference current signal of the c.c. control unit and waveform recording fig. 3.10 was obtained. The grid control signal increases rapidly until

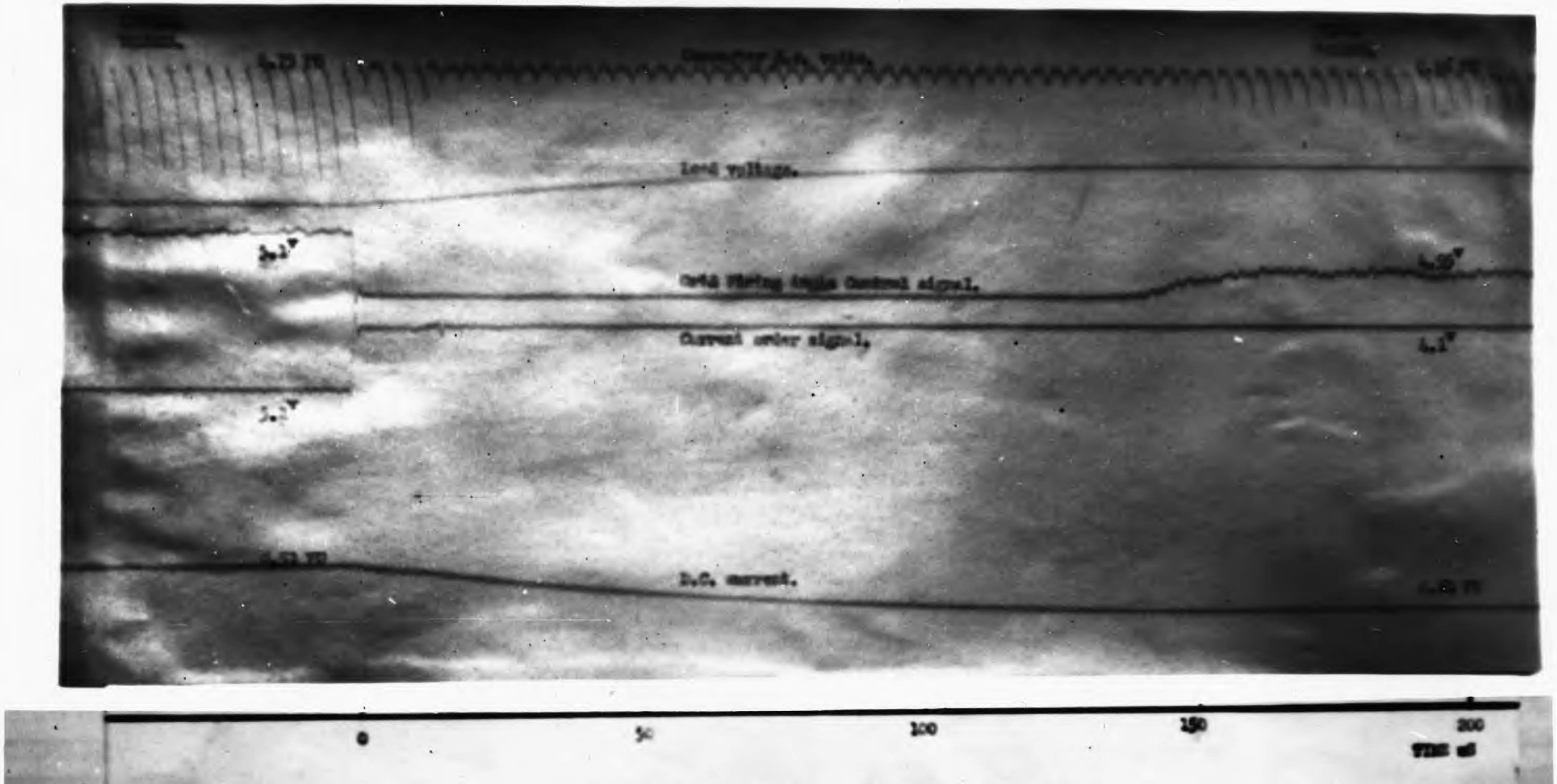


FIG 3.10 STEP INCREASE OF ORDER TO CONSTANT CURRENT CONTROLLER.
SINGLE BRIDGE TEST. RECTIFIER IN SERIES WITH CHOKE AND RESISTIVE LOAD.

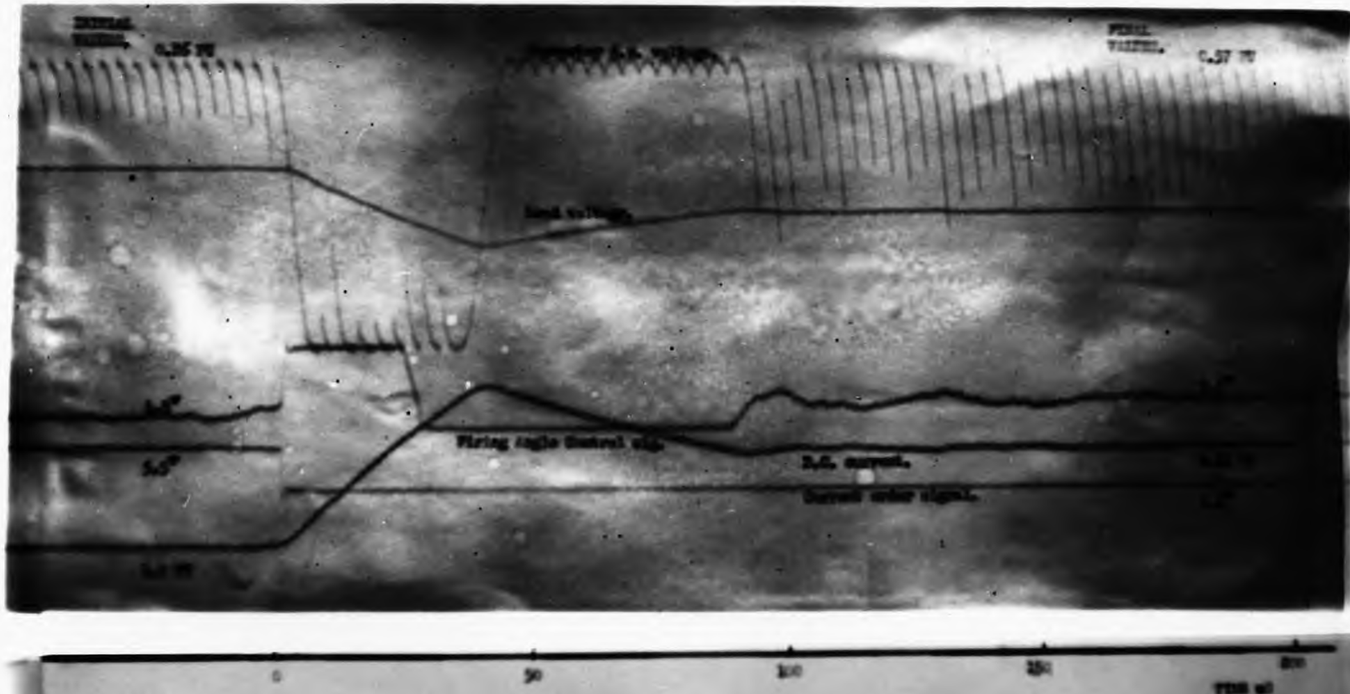


FIG 3.11 STEP INCREASE OF ORDER TO CONSTANT CURRENT CONTROLLER.
SINGLE BRIDGE TEST, RECTIFIER IN SERIES WITH CHOKE AND RESISTIVE LOAD.

further increase is prevented by the α minimum limit circuits and the bridge remains in this condition for $3\frac{1}{2}$ a.c. cycles. The c.c. amplifier output - not directly recorded here - would in this period be in the saturated condition. The rate of increase of current is limited by the d.c. inductor and when it approaches the new demanded value the c.c. control amplifier comes out of saturation and increases the firing angle to control current to this value. The final steady state voltage and current are 132% of the initial values. Changing the size of the current step has the effect of changing the duration of α minimum control and introduces no qualitative changes in the recording.

Fig. 3.11 is a recording of waveforms subsequent to a step decrease of current order such that the final voltage and current are 66.7% of the initial values. The fast high gain current control rapidly moves the bridge into inversion until further increase of the firing angle is limited by the β minimum stop. The bridge remains in this state for about 1 a.c. cycle when d.c. current overshoot brings the c.c. control out of negative saturation forcing the bridge on α minimum control for over two cycles before c.c. control comes out of positive saturation settling the system into its new operating condition. If the size of the negative current order step is less than about 15% the overshoot is limited and the secondary α minimum operating period is absent.

3.5.2. Step changes of reference Extinction Angle Setting

Rapid changes of extinction angle are not required in any form of h.v.d.c. converter control envisaged at present. The tests discussed in this section therefore have no practical relevance and are included only as a record of the transient characteristics of the c.e.a. control unit. The tests were made on an inverter working on the d.c. side in series with a resistance of about 5 ohm and a 0.56H choke against a 100^{V} d.c. mains. The a.c. system short circuit level was reduced by inserting a reactance of 12 mh/phase on the 220^{V} side to give a commutation overlap angle of 12^{o} to 15^{o} at full load. Fig.3.12

relates to a step increase of bridge extinction angle from 10° to 15° as estimated on the oscilloscope at rated current. Fig. 3.13 and 3.14 show the effects of a step decrease of extinction angle from 16° to 11° for bridge currents of 100% and 120% respectively of rated value. The sharp pips in the control amplifier output transferred to the grid control signal arise from the phase advance, i.e. $\frac{d\gamma}{dt}$ component of the fed back control signal. The measured minimum extinction angle signals clearly show the discrete nature of the control and the peculiar non-linearity discussed in section 2.6.5. The waveform of fig. 3.12 settles down after a single overshoot of $\beta > 30^{\circ}$ and the converter does not show any significant transient effects after 3 to 4 a.c. cycles.

A number of interesting aspects of 'comprehensive' c.e.a. control are illustrated in fig. 3.13 and 3.14 which deserve to be examined in some detail. Referring to fig. 3.14, on applying the step change of reference signal demanding a reduction of extinction angle from 16° to 11° the c.e.a. control amplifier begins to reduce the angle of advance and due to the large operating current (120%) commutation failure occurs at the second commutation after the step change. At this point the angle measuring unit reads zero extinction angle and the amplifier responding to the large step error signal produces immediate corrective action in the form of the sharp pip of control voltage induced by the phase advance, i.e. $\frac{d\gamma}{dt}$, control. This ensures an immediate large increase, 25°, of delay angle at the subsequent commutation and the prevention of any further commutation failure. This is an important feature of the new control scheme. Furthermore the c.e.a. control permits the bridge to resume normal operation only slowly as evidenced by the increased values of β for a further two a.c. cycles. Finally the bridge settles down to its new operating state at a reduced extinction angle of 11°. The waveform of fig. 3.13 shows the same test conducted at 100% rated current when no commutation failure takes place but the excessively small value of the extinction angle immediately offer step application is again corrected as described above but the action is less drastic.

One of the drawbacks of 'comprehensive' control when com-

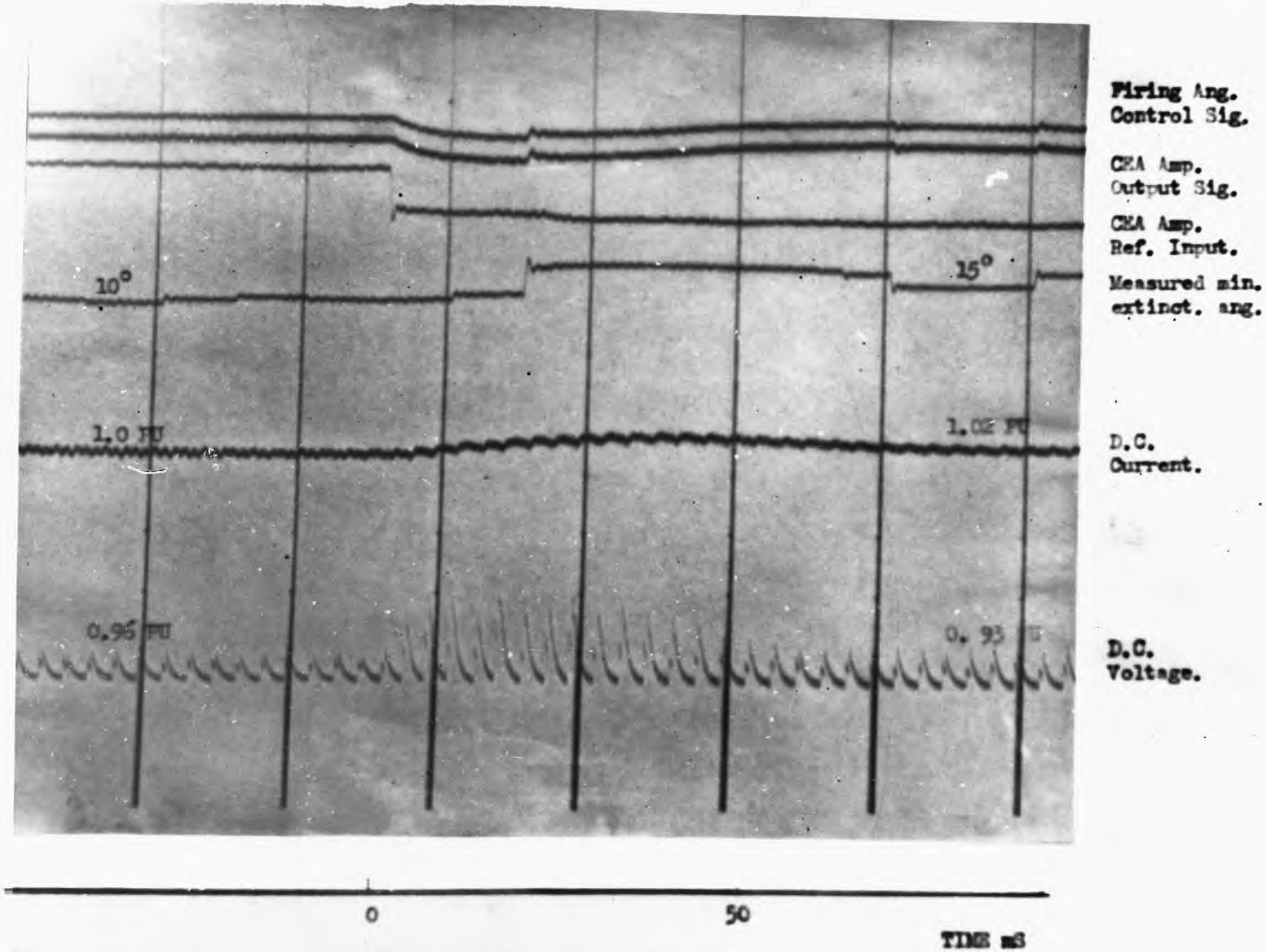


FIG 3.12 STEP INCREASE OF INVERTER MINIMUM EXTINCTION ANGLE REFERENCE SETTING, SINGLE BRIDGE TEST. INVERTER IN SERIES WITH CHOKE, RESISTANCE AND D.C. SOURCE.

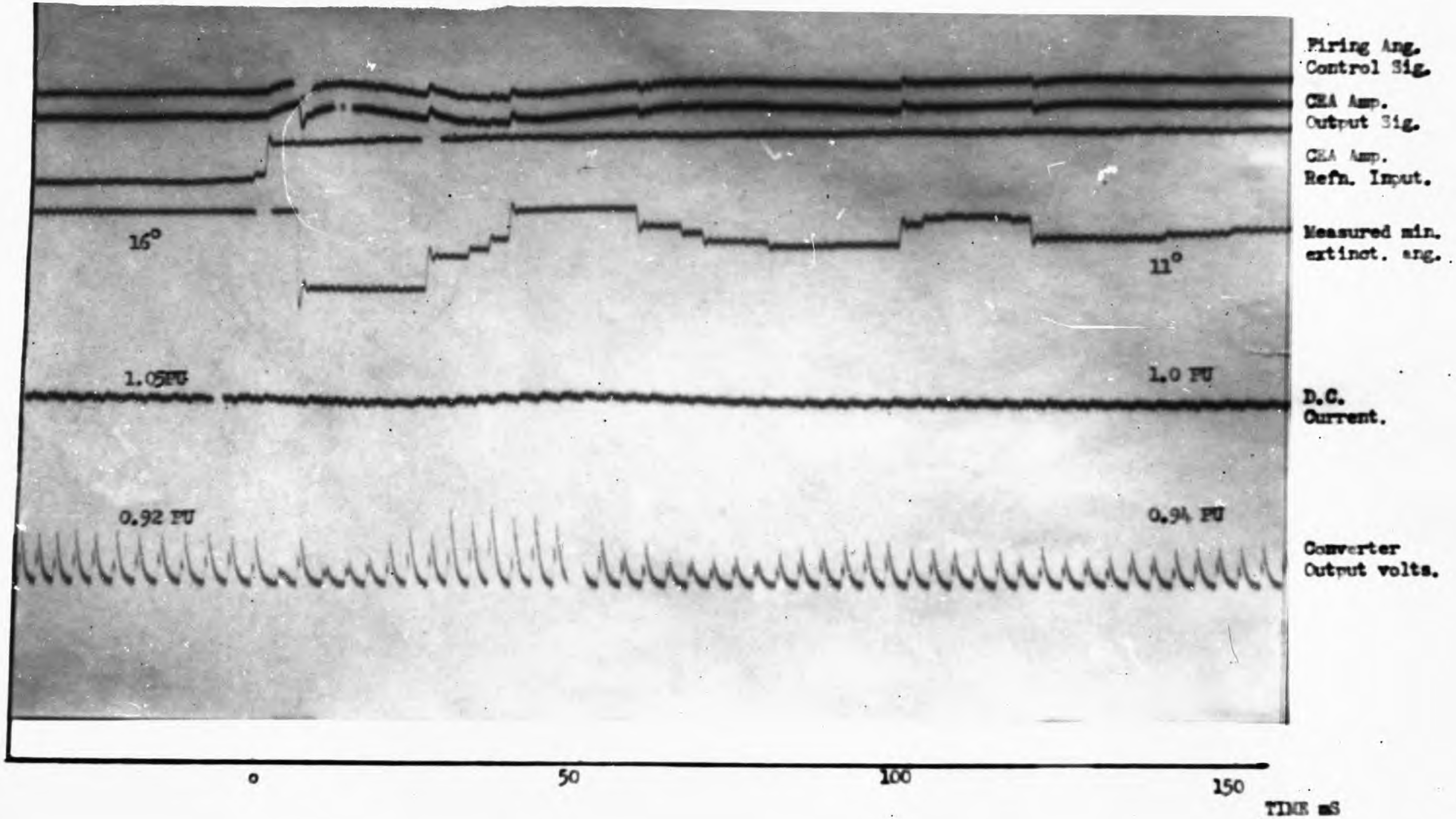


FIG 3.13 STEP DECREASE OF INVERTER MINIMUM EXTINCTION ANGLE REFERENCE SETTING. SINGLE BRIDGE TEST, INVERTER IN SERIES WITH CHOKE, RESISTANCE AND D.C. SOURCE.

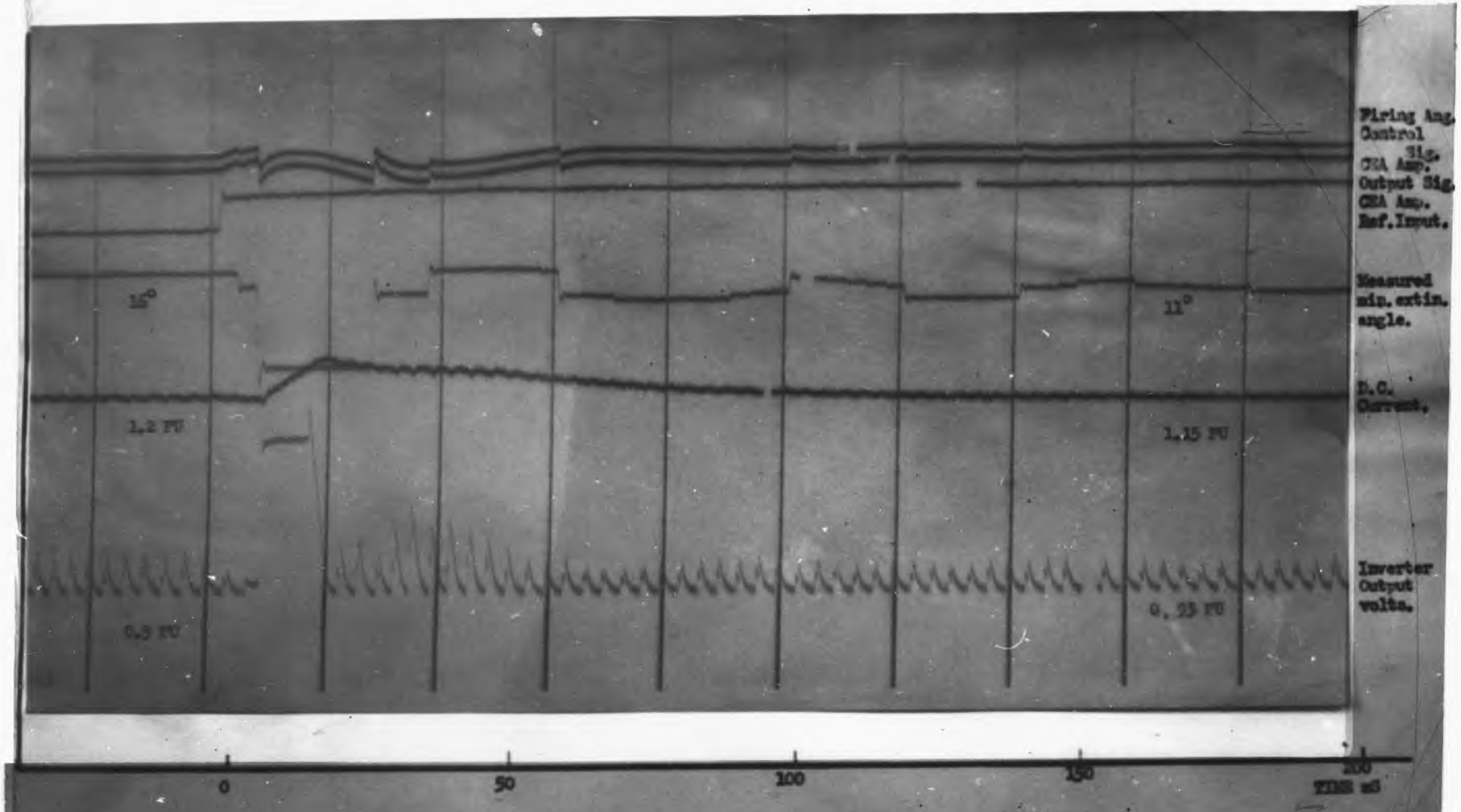


FIG 3.14 STEP DECREASE OF INVERTER MINIMUM EXTINCTION ANGLE REFERENCE SETTING.
SINGLE BRIDGE TESTS. INVERTER IN SERIES WITH CHOKE, RESISTANCE AND D.C. SOURCE.

pared to consecutive control that was pointed out in section 2.6.2 is the inability to produce a correction until a change of extinction angle is sensed. However the excellent automatic corrective action to commutation failures exhibited by 'comprehensive' control, especially when $\frac{d\gamma}{dt}$ feedback is used is a marked advantage of this method.

If the $\frac{d\gamma}{dt}$ component of the control signal was sensitive to the small random variations of extinction angle that continuously occur in power systems, normal system operation would be adversely effected. The waveforms corresponding to the steady state region in these figures however show that for these small disturbances the control voltage pips produced by the phase advance action have completely disappeared by the time of the next valve firing. The $\frac{d\gamma}{dt}$ control component gain is low enough to ensure that it is effective only for large disturbances and commutation failures.

3.5.3. Transition of the converter between c.e.a. and c.c. controls

A transition of inverter operation from c.e.a. controlled operation to c.c. controlled operation is brought about by collapsing the d.c. source voltage to 75% of its initial value. The c.c. control setting is 18% below the initial operating current. The waveform of fig. 3.15 shows the c.c. controller output changing rapidly and beginning to take over bridge control in less than half an a.c. cycle.

The reverse pehnomenon due to a 25% rise in d.c. source voltage is recorded in fig. 3.16. In this case the final operating current is only 5% higher than the initial value and the transient extinction angle is only slightly lower than the final value on c.e.a. control. The c.e.a. control amplifier therefore corrects more gradually than in fig. 3.13 or 3.14.

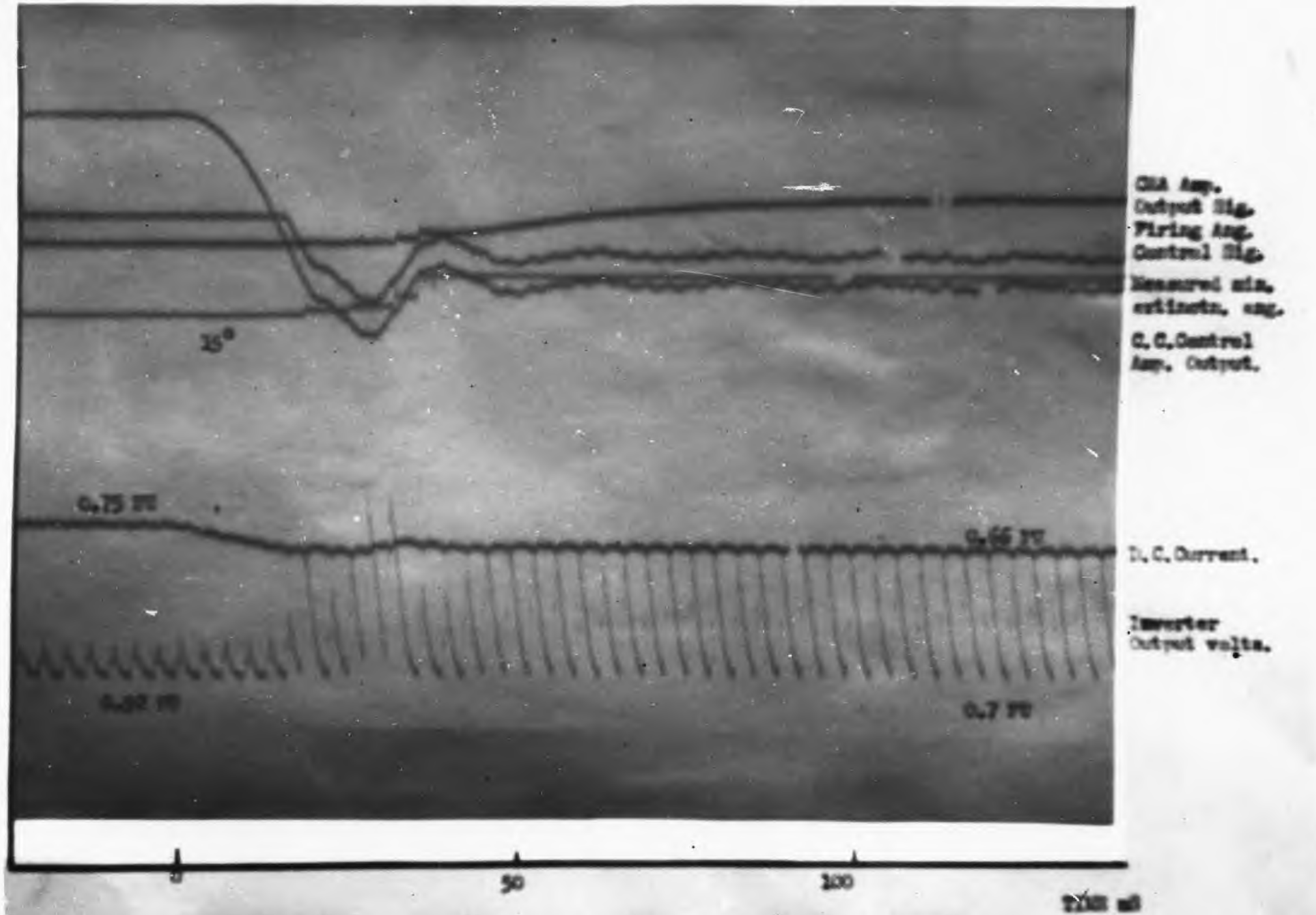


FIG 3.15 TRANSITION OF AN INVERTER FROM C.E.A.CONTROL TO C.C.CONTROL SUBSEQUENT TO A 25% STEP REDUCTION OF D.C.SOURCE VOLTAGE.

SINGLE BRIDGE TEST,INVERTER IN SERIES WITH CHOKE,RESISTANCE AND D.C. SOURCE.

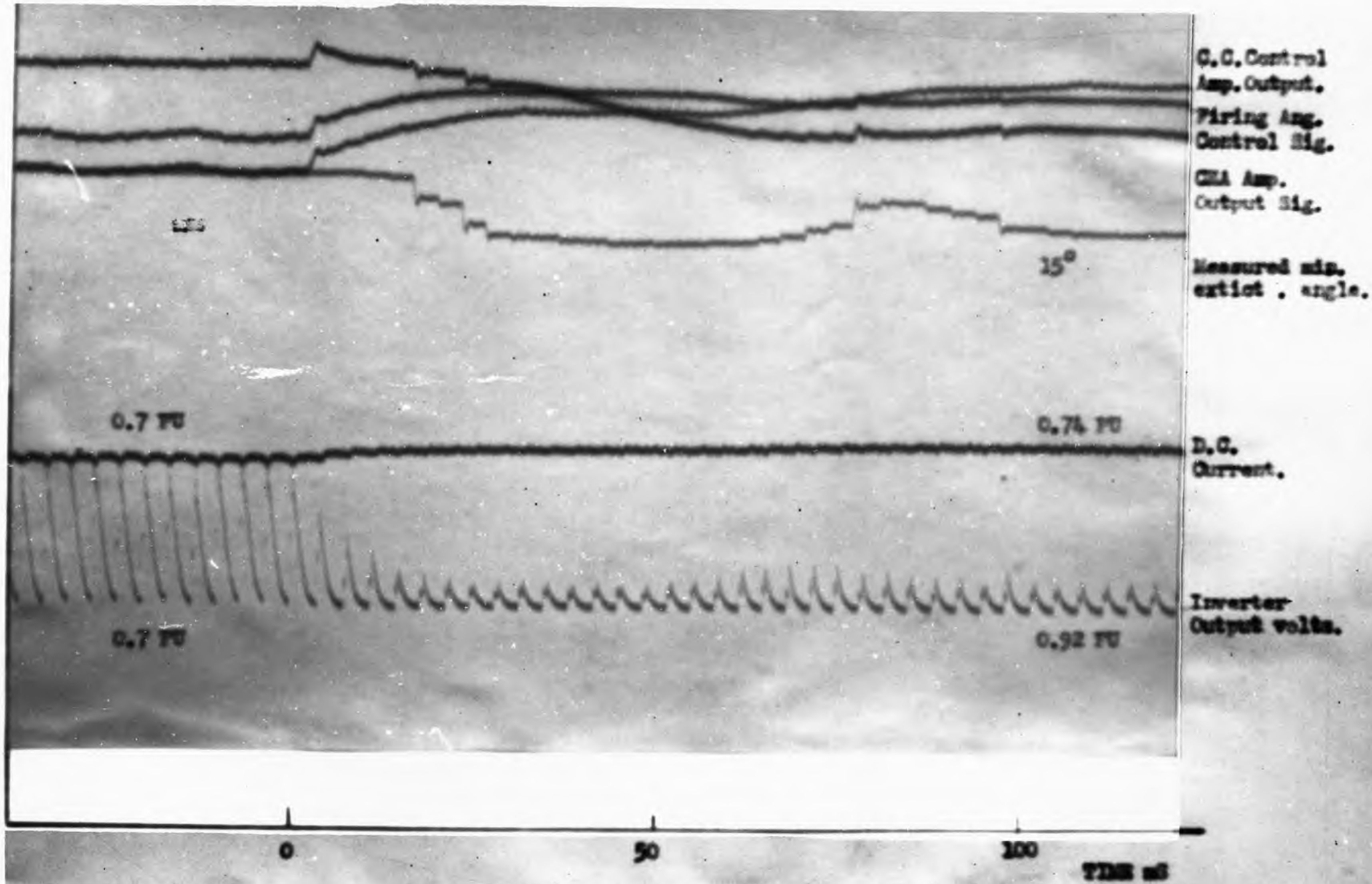


FIG 3.16 TRANSITION OF AN INVERTER FROM C.C. CONTROL TO CEA CONTROL SUBSEQUENT TO A 25% STEP INCREASE OF D.C. SOURCE VOLTAGE.

SINGLE BRIDGE TEST, INVERTER, CHOKE, RESISTANCE AND D.C. SOURCE IN SERIES.

3.6. Three Terminal System Performance

3.6.1. Converter Commutation Failure

Small disturbance analysis of h.v.d.c. transmission system stability using linearised equations is not acceptable because the typical system disturbance, a single isolated converter commutation failure, is excluded. In tuning the gains and other characteristics of the controls at the three terminals of the h.v.d.c. simulator, particular attention was paid not only to obtaining fast, close control, but also to the ability of the system to ride through rectifier and inverter single commutation failures. The following figures illustrate the effect of commutation failures,

Figure	Failure at	Type	Current margin
3.17	Rectifier	Single	8%
3.18	Inverter connected to weak a.c. system	Single	8%

These tests were conducted with the rectifier on normal volts and at full load current . 60% of which was delivered to the inverter on c.e.a. control by constant current controlling the other inverter to accept the remaining 40%. The inverter IN2 connected to the weak a.c. system is on c.e.a. control for both tests and the converter voltage waveform immediately after failure clearly shows the corrective action discussed at some length in section 3.5.2.

The node voltage oscillations are representative of the predominant natural frequency of the transmission network and in the case of fig. 3.17 is easily measured as 30 c/s. This is much lower than the conventional natural frequency of transmission lines and cables of the same length due to the large lumped smoothing inductor at line terminations.

3.6.2. Step changes of Rectifier Current Order

One of the principal advantages of h.v.d.c. transmission is the ability to rapidly alter power flow in different parts of

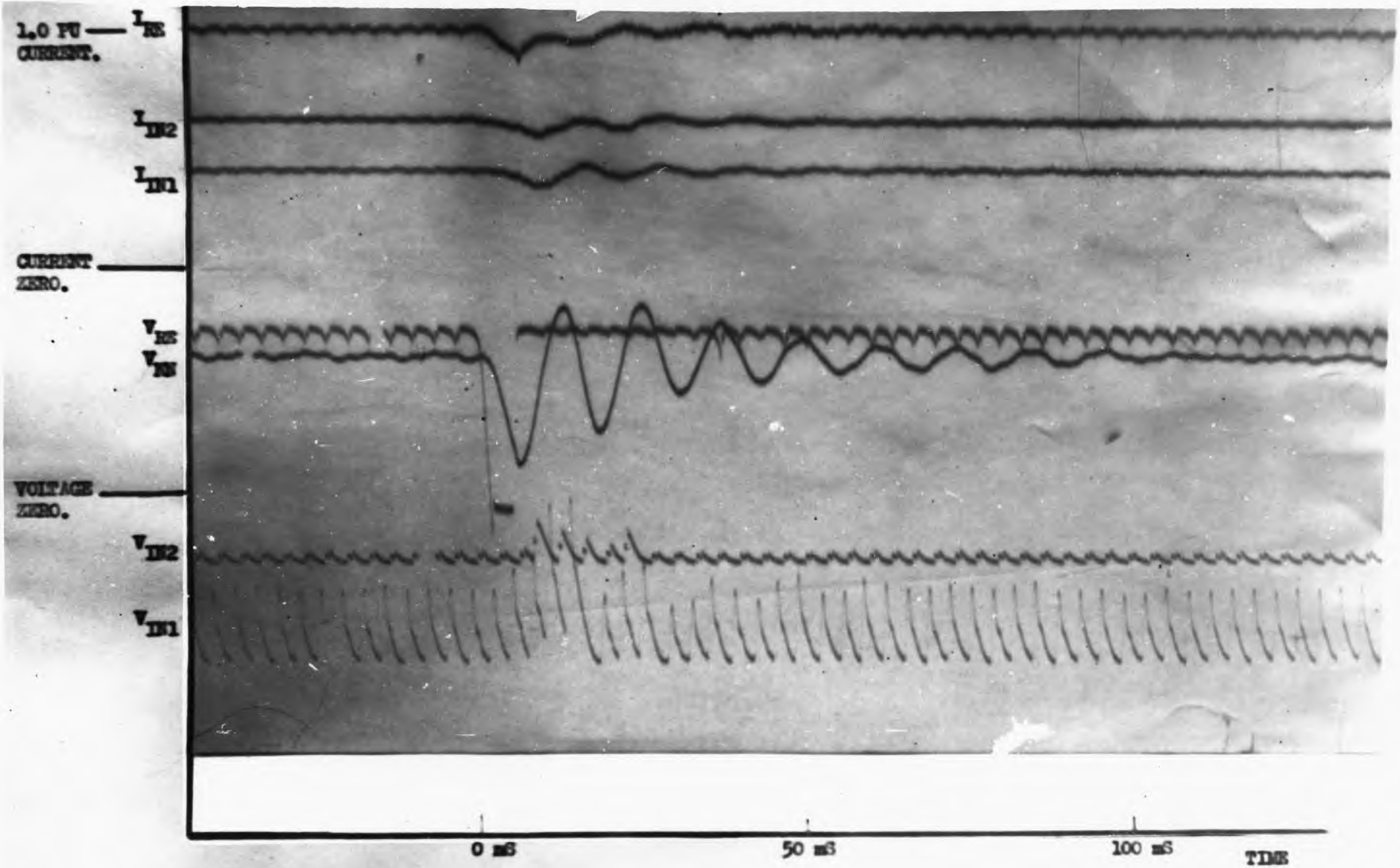


FIG 3.17 SYSTEM DISTURBANCE AND SETTLING SUBSEQUENT TO ISOLATED RECTIFIER COMMUTATION FAILURE.

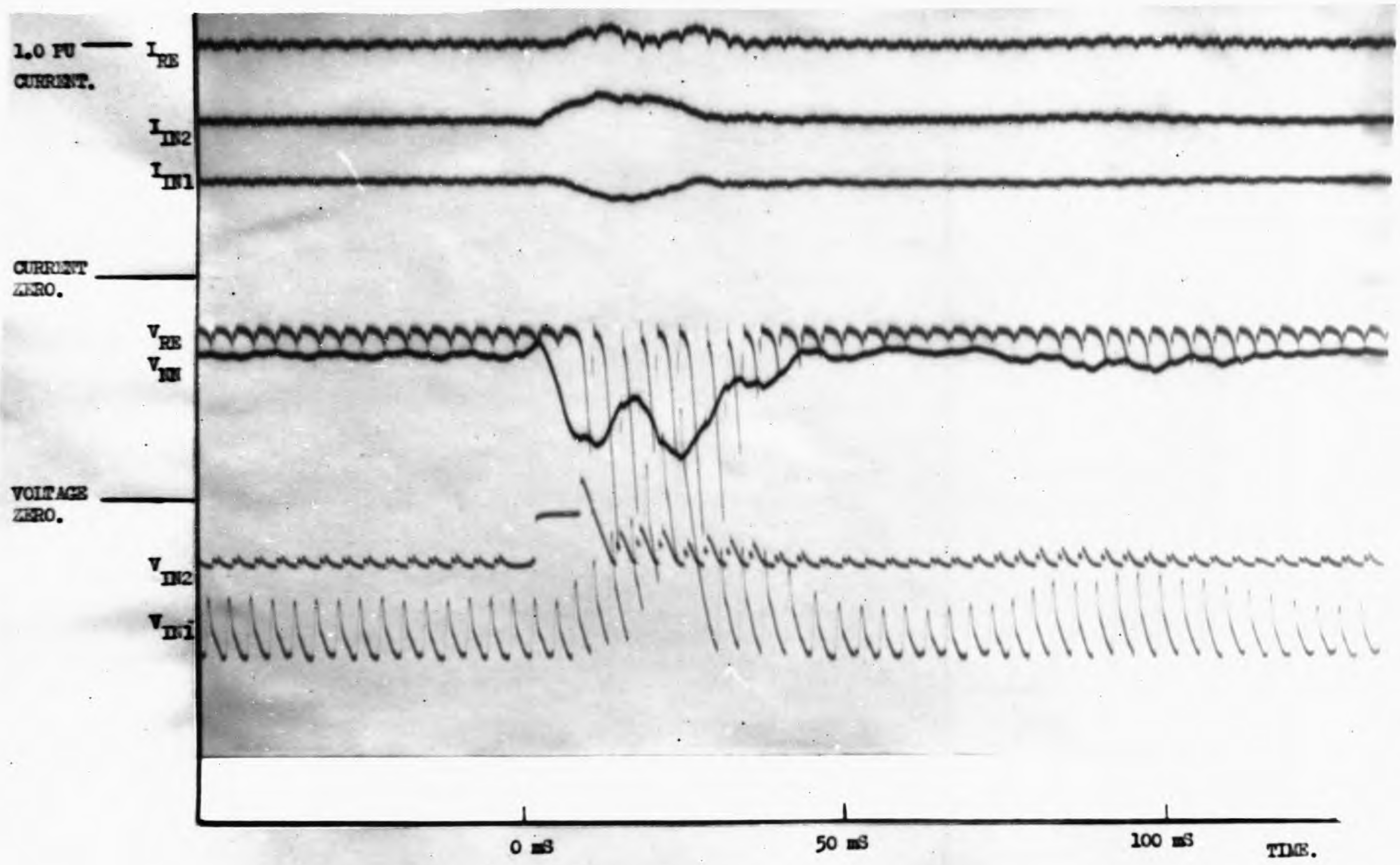


FIG 3.18 SYSTEM DISTURBANCE AND SETTLING SUBSEQUENT TO AN ISOLATED INVERTER COMMUTATION FAILURE.

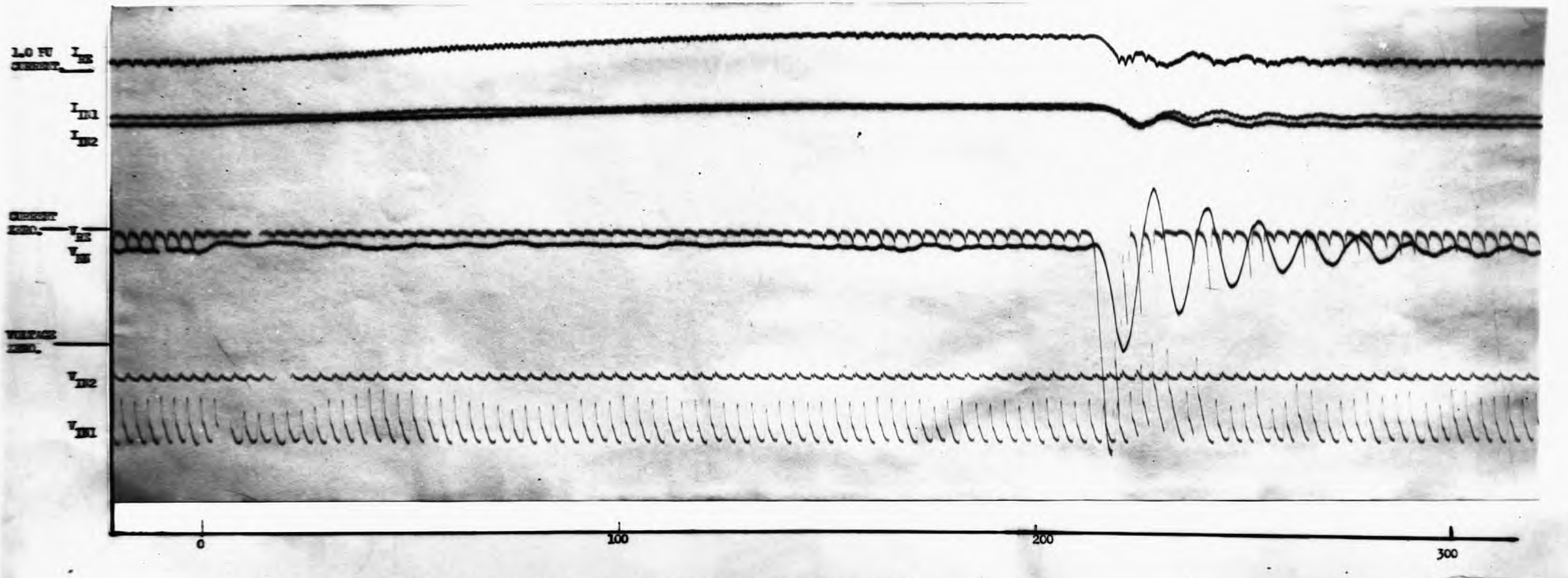


FIG 3.19 STEP INCREASE AND SUBSEQUENT STEP DECREASE OF RECTIFIER CURRENT ORDER.

the network. This is illustrated in fig. 3.19 where rectifier current is increased from 90% to 110% of rated value by a step change of control signal. Soon after the system settles down the current is reduced to its original value by a second step change of control signal. The second transient shows one double commutation failure of the rectifier arising from rapid control change but system recovery is excellent. The transient is much less severe than the corresponding effect in fig. 3.11 for a single bridge working against a resistive load because the other two controlled converters contribute favourably to the stability of the disturbed converter.

3.6.3. Fast Power-flow Reversal

Cautious experiments[78] have been conducted on the cross channel link to reverse the direction of flow of d.c. power between the systems. The method used was to decrease both rectifier and inverter current orders to zero and restart the system with the rectifier/inverter functions and therefore the cable polarity reversed. The entire change over took 600 ms of which 500 ms was due to delay in the communication systems.

Much faster power reversal can be achieved by altering converter control signals to make the operating current margin negative, if the rapid change of cable polarity is acceptable. In the most arduous case where step changes were applied (fig. 3.20) to the model the rapid transient includes one double commutation failure of inverter IN1 but control oscillations cease in two a.c. cycles. The converter which was initially on c.e.a. control transits to the α minimum limit control and continues the function of regulating system voltage. This converter exhibits a single excursion out of α min. Control to c.c. control and a return to α min. control, in this case about 7 a.c. cycles after the step input, but the resulting system disturbance is small. If the transmission is to be maintained in the reverse direction for more than a few seconds it is desirable that the transformer top-changers are operated to lower the large firing angles that necessarily arise at the two converters on c.c. control.

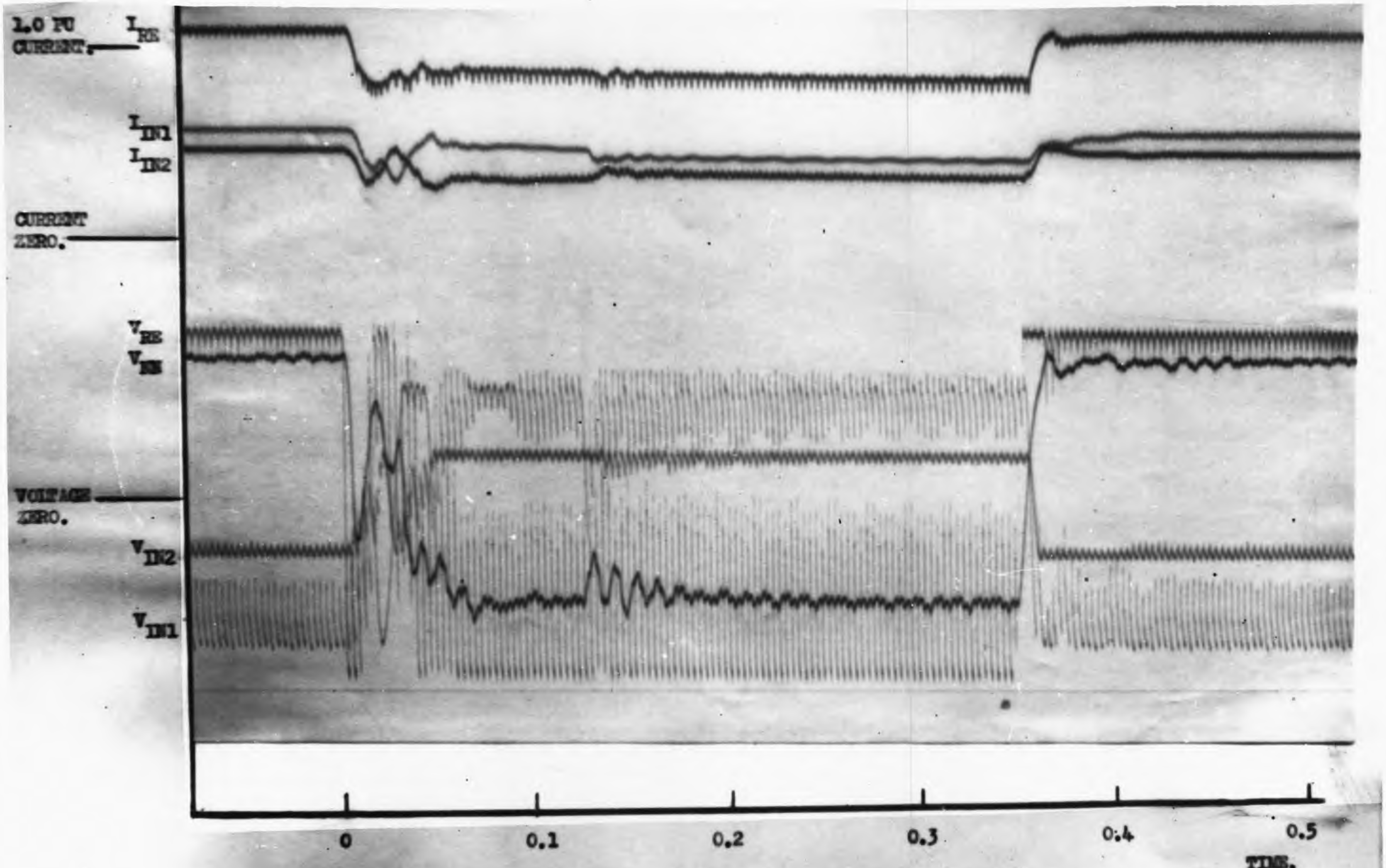


FIG 3.20 STEP DECREASE OF RECTFIER CURRENT ORDER CAUSING POWER FLOW REVERSAL FOLLOWED BY A STEP INCREASE TO RETURN TO THE INITIAL STATE.

The transmission was returned to its original operating state by a second step change. The reversal of the system is now much more rapid and smooth, though minor oscillations of control persist for 2 to 3 a.c. cycles.

The two operating conditions are described by the table below.

	Normal power transfer	Reversed power transfer
Rectifier		
	current 106%	88%
	voltage 90%	– 53%
	c.c. control	c.c. control
Inverter 1		
	current 55%	48%
	voltage 74%	– 69%
	c.c. control	c.c. control
Inverter 2		
(weak a.c. system)	current 51%	40%
	voltage 74%	– 69%
	c.e.a. control $\gamma = 13^{\circ}$	α min control
Node	voltage 81%	– 61%

Voltage and current everywhere are given as % of Rectifier rated values.

CHAPTER 4

A Discussion of the Power System Representation

4.1. A.C. system representation

The behaviour of a d.c. converter is to a large extent determined by the characteristics of the a.c. system to which it is connected. The a.c. system characteristics were taken into account when designing and synthesising the converter control circuits and here the discussion of these characteristics is extended. Generation and load connection, network interconnection and outages, continually cause modification to the characteristics of an a.c. power system.

4.1.1. Impedance Characteristics of A.C. Power Systems

The 50 c/s impedance of a.c. power systems is usually determined with sufficient accuracy from an estimation of system short circuit level. An impedance angle of between 80° and 90° is also assumed. Where the interest is in fast changes the system transient reactance together with transient damping effect have to be considered. When the rectifier is connected to an isolated machine the great complexity of adequate modelling with static components is best overcome by using micro-machines.

The harmonic impedance of power systems however poses a much more complex problem than power frequency effects. An approximation that is sometimes used is: harmonic impedance = harmonic order x power frequency impedance. The converter filter bank can resonate with the a.c. system at a harmonic of order n, where $n \doteq$ (short circuit level of a.c. system/capacitor power frequency VA_r supply).

Network analyser/computer studies have been made to determine the variation of system impedance with frequency and the principal conclusions arrived at include (79)

1. fault level is not a guide to harmonic impedance except under maximum load conditions when resonance tends to be

damped out. The lowest harmonic impedances at high harmonic frequency were, surprisingly, encountered under minimum plant conditions.

2. the main resonance peak occurs between the 5th and the 10th harmonic. Many more subsidiary resonance frequencies than were theoretically anticipated occurred and resonances were more frequent on the higher voltage networks.

3. the high frequency impedance drops off more markedly in cable systems than in overhead line networks.

Network analyser/computer calculations by Horigome et al[(80)] on a simplified but typical power network however shows the resonance peak in the region of the 19th harmonic.

Field tests have been conducted[(79)] on the Lydd converter equipment to obtain the a.c. system harmonic impedance at the frequencies present in the converter a.c. line currents. The resonances were found to be both more frequent and more pronounced than in network analyser tests and the magnitude of the high frequency (above 20th harmonic) impedance was much higher. No reliance can be placed on the harmonic damping resistance value indicated by network analyser studies. Impedance angles as low as 40° to 60° are sometimes used in transient studies on h.v.d.c. simulators.

Filter groups tuned to series resonance at odd harmonic frequencies can show parallel resonance in pairs at intermediate harmonics of even number. Small even harmonic currents arising from a.c. voltage, network commutating reactance, or firing angle unbalances can give rise to high even harmonic voltages at the converter transformer terminals.

It is known that simulator tests have been carried out at the English Electric Co. where, with the bridge blocked, the converter station terminals have been suddenly energised by closing the main a.c. side circuit breaker. The a.c. waveform is heavily distorted and shows numerous high frequency spikes. It is believed that these phenomena arise from filter ringing and are influenced by transformer inrush currents.

Gardner[82] has also pointed out that the impedance presented to harmonics by synchronous machines is dependant on magnetic saturation, and therefore on load magnitude and power factor. The harmonic impedance decreases at higher saturation and usually lies in the range (harmonic order) x (transient or sub-transient reactance).

No high pass filter was originally planned for the New Zealand scheme but telephone interference dictated installation. The English end of the cross channel link is subject to harmonic instability under certain network configurations without the third harmonic filter bank[81, 83]. It is known that quite large odd and even harmonics flow in transmission networks near h.v.d.c. converter installations. In contrast no filters are used on the island of Gotland and this substantiates the statement that the severity of the harmonic problem depends entirely on the terminal a.c. system.

4.1.2. A.C. system Inertia

The a.c. networks at the two (or more) terminals of an h.v.d.c. system may bear one of the following three relationships to each other.

1. Closely integrated by other synchronous ties. Frequency deviations and phase swinging between the terminals is not significant.

2. Loosely coupled by synchronous ties. The possibility of loss of synchronism following faults needs to be investigated.

3. Asynchronously coupled.

The second and third cases require further consideration during fault studies so that either synchronism or frequency instability respectively of the two a.c. networks, may be taken into account[84].

$H_{1,2}$ are suitably dimensioned inertia constants for the two systems and $\delta f_{1,2}$ are system frequency deviations due to a disturbance, subscripts 1,2 refer to the two systems. Suppose a power imbalance δP occurs in either system, then

$$s.\ \delta f_{1,2} = \left(\frac{\delta P}{H_{1,2}}\right) \qquad - (4.1)$$

s = the Laplacian operator

If the d.c. system power transfer is sensitive to phase or frequency deviation we can write an approximate transfer equation connecting incremental power exchange and frequency deviation.

$$\delta P = DC(s)\ .\ \ \delta f \qquad - (4.2)$$

and under the same conditions a sensible relationship for incremental power exchange through the synchronous links is

$$\delta P = AC\ .\ \left(\frac{\delta f}{s}\right) \qquad - (4.3)$$

where AC is a constant; for a single line we have the well known expression $AC = 2\ \pi .\ \frac{E_1 E_2}{X}\ .\ \cos \partial$ and for case 3 above AC = 0.

Suppose that the power exchange required between two networks coupled in the general manner indicated above changes by an amount δP, from 4.1, 4.2 and 4.3.

$$\delta f_{1,2} = \frac{1}{s}\left\{ \delta P - \left(DC(s) + \frac{AC}{s}\right) . \delta f \right\} \frac{1}{H_{1,2}}$$

since

$\delta f_1 + \delta f_2 = \delta f$ the nett frequency deviation,

$$\delta f = \left(\frac{\delta P}{H}\right) \left(\frac{s}{s^2 + s.\left(\frac{DC(s)}{H}\right) + \frac{AC}{H}} \right)$$

$$H = \frac{H_1 \cdot H_2}{H_1 + H_2}$$

The damping due to losses and frequency dependant loads has been tacitly neglected, these may be approximately accounted for by the inclusion of a factor 'k' to give

$$\delta f = \left(\frac{\delta P}{H}\right) \left(\frac{s}{s^2 + s\left(\frac{DC(s)}{H} + k\right) + \frac{AC}{H}} \right)$$

This general expression represents a damped sinusoidal oscillation where the d.c. link contributes to the system damping. The importance of accurately modelling the combined system inertia and the damping can be appreciated.

It is not intended to demonstrate here that a d.c. link can be used to stabilise a.c. networks. Stabilisation is in certain cases frustrated by the nonlinearity of DC(s) arising from the inability to overload the converter valves for any worthwhile length of time.

4.1.3. The A.C. system as represented on the simulator

From the foregoing discussion it is clear that adequate a.c. system representation is of prime importance if comprehensive simulator studies are to be undertaken. At the same time the complexity of the problem defeats straightforward solutions and at the time of writing no published research is available on simulation techniques suitable for this purpose though it is arousing interest. At the present time it is usual to connect the converter transformers of simulators to the laboratory mains through inductances and resistors to give correct short circuit level and transient damping only.

A compromise also needs to be struck between the requirements imposed by the use of one bridge only per converter terminal and accurate modelling of system short circuit ratios. If X_c is the commutating reactance referred to the primary at an n-bridge inverter on c.e.a. control the apparent d.c. side negative resistance arising from commutation overlap is $\frac{3.X_c}{n.\pi}$ The result of employing the correct value of X_c (from short circuit level considerations) when a single bridge of n-times higher rating replaces n bridges is to magnify the commutation overlap angle and increase this negative resistance n-fold; correspondingly lowering transmission stability and limiting rectifier c.c. control gains. Throughout this thesis an ambivalent attitude is adopted towards the three bridge system as numerous transients investigated are considered typical of a two bridges per converter system. Hence it is necessary to compromise between modelling the correct short circuit level or twice the correct short circuit level. The construction of filters has not been undertaken at any terminal and hence the benefits of VA_r supply and reduced waveform harmonic distortion have to be foregone. For these reasons the higher value of short circuit level is invariably employed.

A range of a.c. systems has been obtained by connecting one inverter to a weak a.c. system of short circuit ration 5.5 and the other to a considerably stronger a.c. system. The short circuit ratio at the rectifier is of the order of 7.5. The connections to the a.c. mains are made through reactance coils having a 50 H_z $^X/R$ ratio of about 20. It has been noted previously that a considerable resistive component is to be expected in simulators. No additional damping has been provided as it is estimated that the existing series resistances alone (giving rise to an impedance angle of 60° to 70°) makes sufficient if not excessive allowance for transient damping.

4.2. Recovery after A.C. side faults

The purpose of these tests is to show the d.c. transmission system recovering from a number of different faults on the sending and receiving end a.c. networks. The shortcomings in the representation of the a.c. network discussed above make these results optimistic but the absence of filters in the model provide a measure of compensation.

Test details are as follows.

<table>
<tr><th>Figure</th><th>type of fault</th><th>location</th></tr>
<tr><td>4.1</td><td>unsymmetrical Y to B phase to earth short on transformer primary terminals</td><td rowspan="3">Inverter IN2 connected to weak a.c. system</td></tr>
<tr><td>4.2</td><td>3-ph open circuit on transformer primary terminals</td></tr>
<tr><td>4.3</td><td>symmetrical collapse of a.c. volts to 40%</td></tr>
<tr><td>4.4</td><td>symmetrical collapse of a.c. volts to 55%</td><td>Rectifier</td></tr>
</table>

Also, the system initial and final operating conditions which are identical are as follows:-

	Rectifier	Inverter IN1	Inverter IN2	Node
voltage %	96	82	80	85
current %	100	40	60	
control	c.c.	c.c.	c.c.a. ($\gamma = 15^{\circ}$)	

All %ages on rectifier rated values.

Brief reference was made in section 2.4.2. to the fact that the pulsing unit reference sinusoid was derived from the laboratory mains rather than the transformer primary voltage in order to simulate a true-sinewave oscillator locked in frequency and phase to the a.c. power system. This representation will give accurate results only for disturbances where the transient response of the oscillator is not relevant, that is only for disturbances that do not materially alter the frequency or phase of the a.c. system. Where these quantities do change the error is limited to the first a.c. cycle; the 'phase-locked' oscillator developed

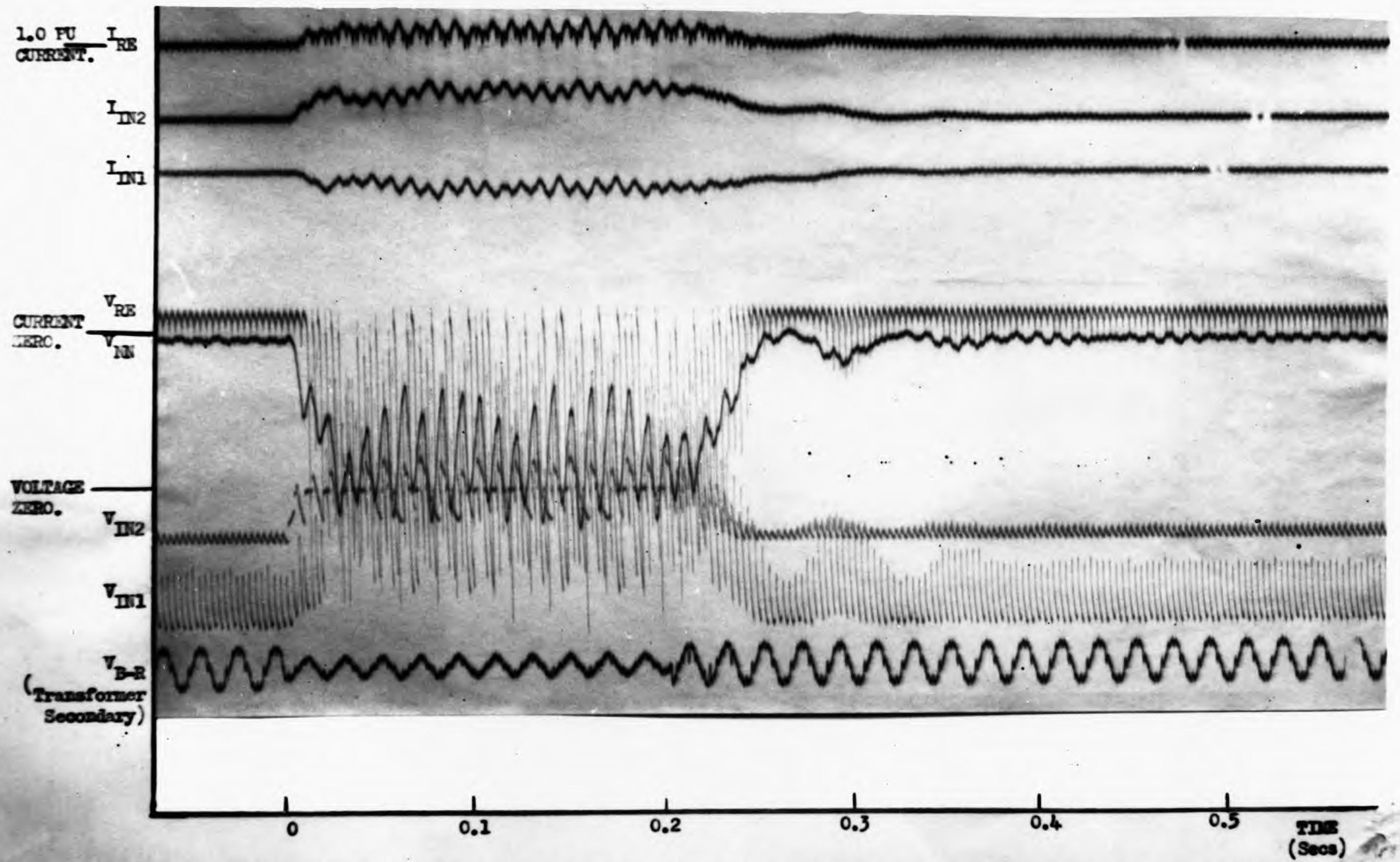


FIG 4.1 TRANSIENT UNSYMMETRICAL Y-PHASE TO B-PHASE TO EARTH SHORT CIRCUIT ON INVERTER IN2 TRANSFORMER PRIMARY TERMINALS.

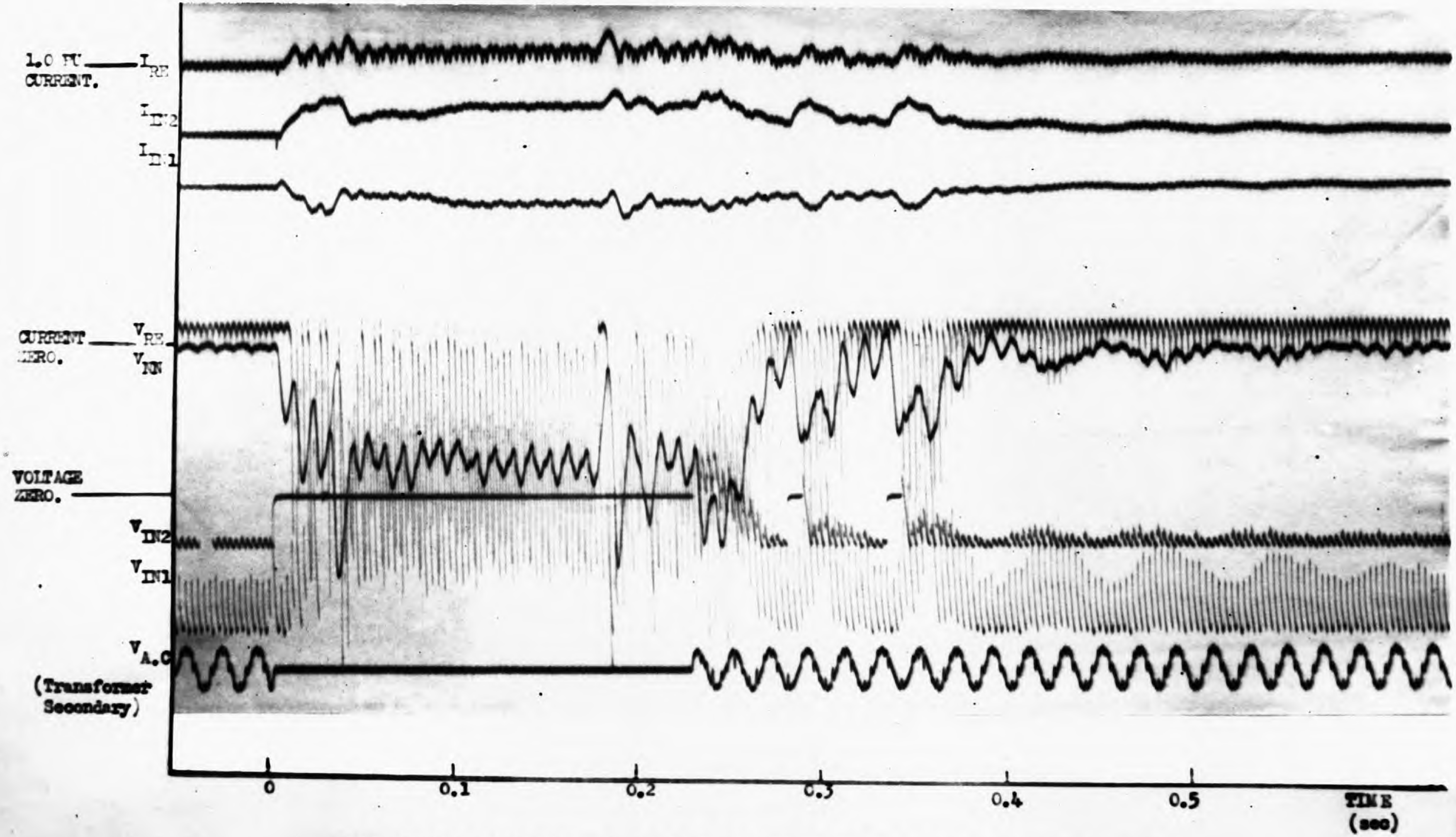


FIG 4.2 TRANSIENT 3-PHASE OPEN CIRCUIT ON INVERTER IN2 TRANSFORMER PRIMARY TERMINALS.

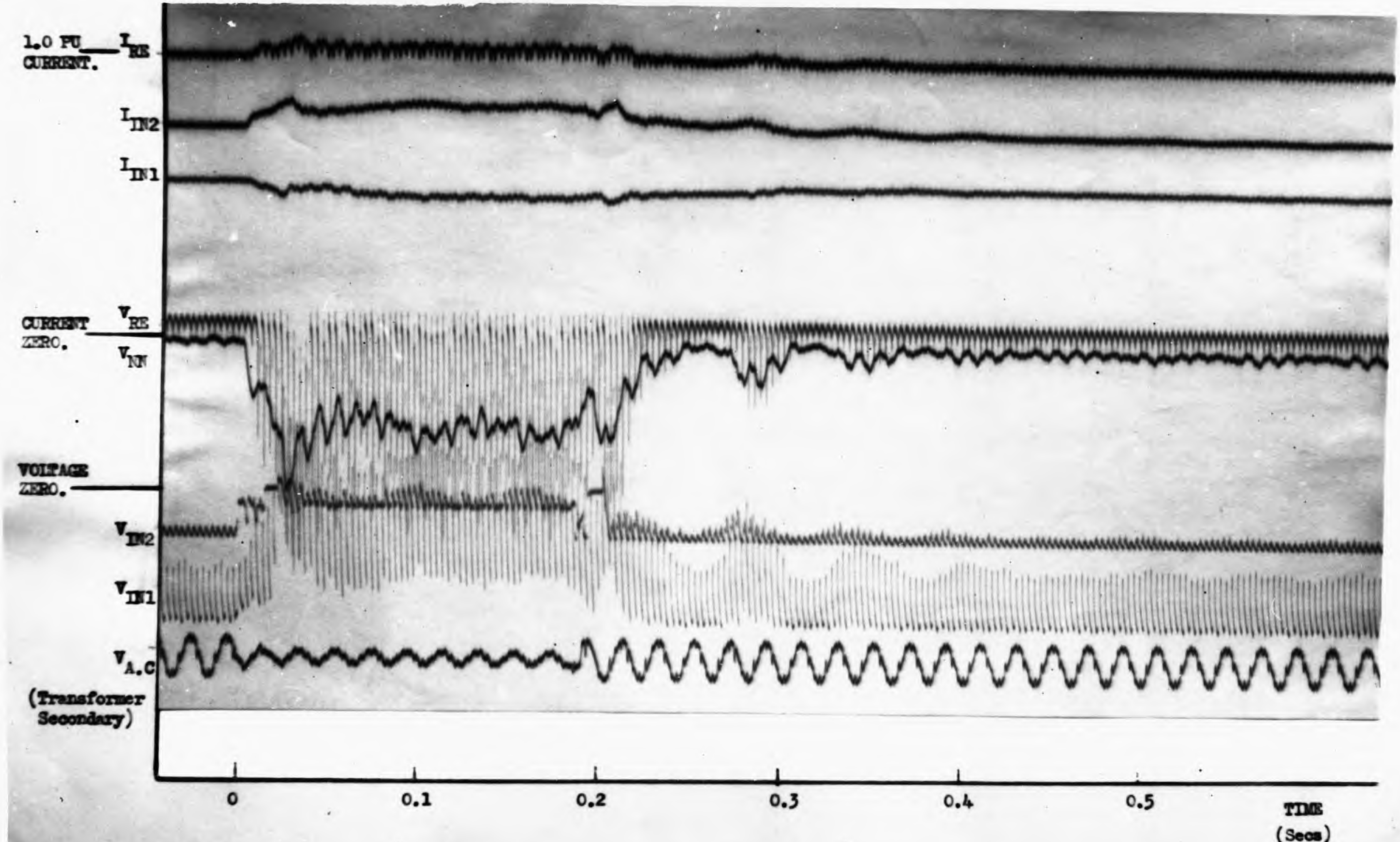


FIG 4.3 TRANSIENT SYMMETRICAL COLLAPSE OF INVERTER IN2 A.C. SIDE VOLTAGE TO 40% OF NOMINAL VALUE.

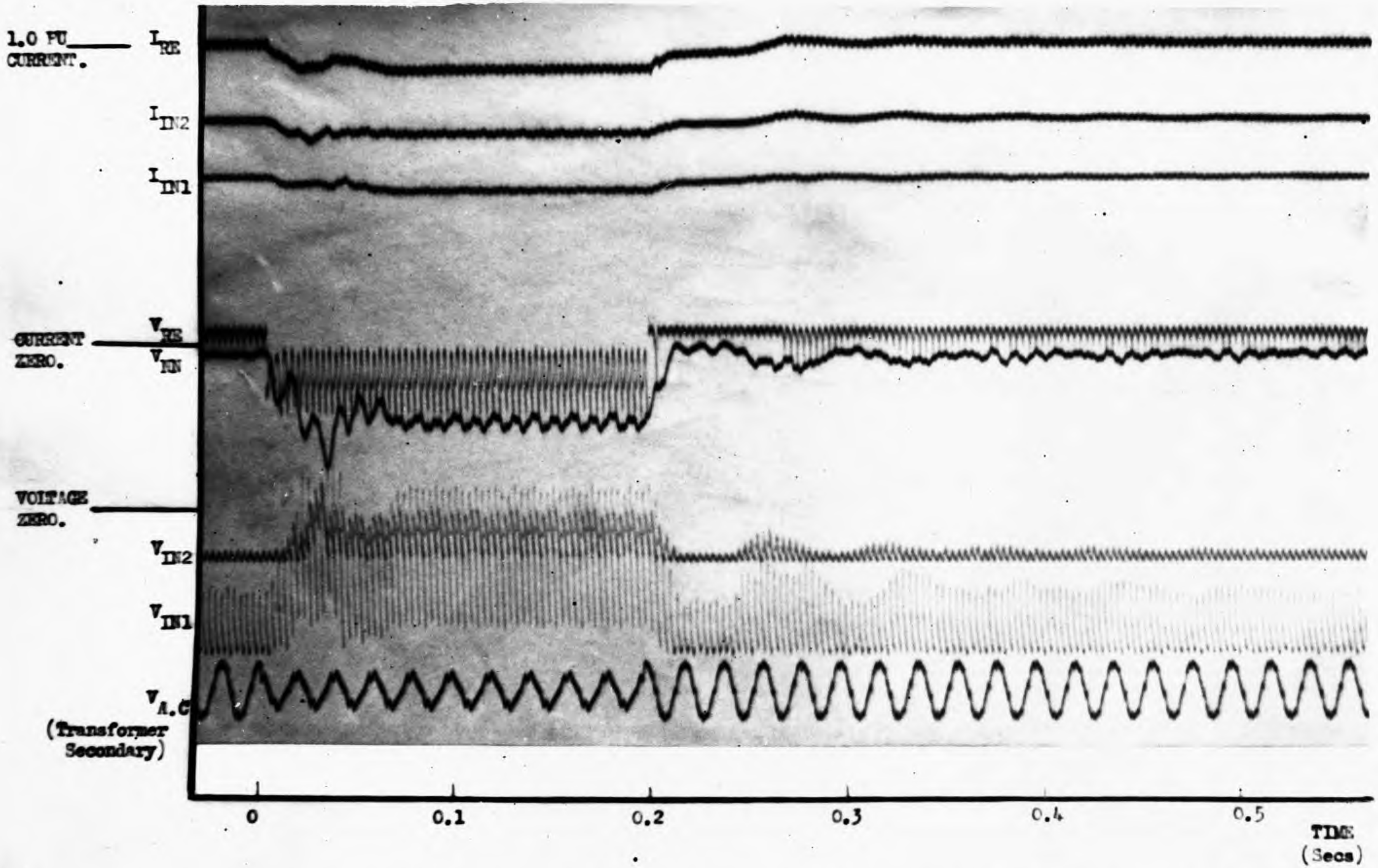


FIG 4.4 TRANSIENT SYMMETRICAL COLLAPSE OF RECTIFIER RE A.C. SIDE VOLTAGE TO 55% OF NOMINAL VALUE.

by the English Electric Co. is capable of correcting for step changes of phase in about one cycle. In the test of fig. 4.2 to 4.4 the phase of the a.c. supply initially and finally is identical. Furthermore in fig. 4.3 and 4.4 the phase position for the duration of the fault is not permitted to vary significantly from the initial state. Fig. 4.1 however gives rise to a more complex condition arising from the unsymmetrical nature of the fault and the approximate representation considered above is less valid.

The most severe conditions occur in the case of an a.c. system open circuit on the inverter transformer terminals, fig. 4.2. On sudden re-energisation two commutation failures and severe transient oscillations occur before the system settles down.

The transients in all the tests have been applied for 200 ms to 250 ms for ease of record reading. In practice the converters would have to be blocked after some 5 a.c. cycles to limit valve stress though the system itself is capable of recovering after an indefinitely long fault period.

4.3. Representation of D.C. Transmission Lines

The transmission system simulated in these studies consist of a 100 mile overhead line from the rectifier to the T-point from where two 20 mile cables lead to the two inverters. The lines have been modelled on the nominal-π representation. The equivalent-π representation, sometimes used in a.c. transmission studies, has no meaning here and in fact tends as a limiting case to the nominal π for d.c. voltages and currents. Lumped parameter circuits are of limited accuracy for transient investigations as the accuracy of connecting a number of π-sections in series to represent a distributed parameter line is dependent on frequency.

By manipulation of the equations of conventional transmission line theory[85] it can be shown that

$$z_{\pi} = z\left(1 - \frac{1}{2!}\left(\frac{\mu\cdot\delta 1}{2}\right)^2 + \frac{1}{4!}\left(\frac{\mu\delta 1}{2}\right)^4 - \ldots\right.$$

$$\mu_{\pi} = \mu\left(1 - \frac{1}{3!}\left(\frac{\mu\cdot\delta 1}{2}\right)^2 + \frac{1.3}{2.4.5}\left(\frac{\mu.\ \delta 1}{2}\right)^4 - \ldots\right.$$

where

z_{π} = characteristic impedance of nominal-π
z = characteristic impedance of line
μ_{π} = propagation coefficient of nominal-π (per unit length)
μ = propagation coefficient of line
$\delta 1$ = line length represented per π section

In order to assess the error, simplification to the lossless line case of $\mu = j\,\frac{2\pi.f.\ \delta 1}{v}$ is made, where f and v are the frequency and velocity of propagation respectively. The following expressions for approximate percentage errors can be obtained,

$$\text{error in } z_{\pi} = \frac{\pi^2 f^2.\delta 1^2}{2v^2} \times 100\%$$

$$\text{error in } \mu_{\pi} = \frac{\pi^2 f^2.\delta 1^2}{6v^2} \times 100\%$$

The fastest voltage changes arising in a converter are at the beginning and end of commutation and may be approximated by a wavefront of some 10 to 100 μsec rise time. However the large smoothing inductors limit high frequency effects and a sensible upper limit to the values of frequency that need be considered in the error analysis above is in the range 300 Hz to 1kHz. Using the numerical values derived in the latter part of this section the above formulae yield

		At 1 kHz	At 300 Hz
% error in z	o.h. line	4.45	0.4
% error in μ	o.h. line	1.5	0.14
% error in z	cable	1.2	0.11
% error in μ	cable	0.4	0.03

At 300 Hz the error is small and is much less significant than the errors in the values of the model transmission line components.

A second source of error that is unavoidable in lumped parameter models is that the finite propagation time arising from the large physical length of transmission lines is neglected. This effect cannot be reproduced in the laboratory by simply using a larger number of sections so long as the physical length of the simulation remains small, nor by using delay lines as the R, L, C parameters are too divergent. These times for the o.h. line and cable modelled here are 0.6 ms and 0.31 ms respectively.

The parameters assumed for the transmission lines are as follows:-

o.h. line

length	100 mls
resistance	0.125 ohms/ml
inductance	3.0 mH/ml
capacitance	0.012 μF/ml

cable

length	20 mls each
resistance	0.3 ohms/ml
inductance	0.5 mH/ml
capacitance	0.07 μF/ml

The propagation velocities of the o.h. line and cable as determined from these constants are 165,000 ml/sec and 80,000 ml/sec respectively.

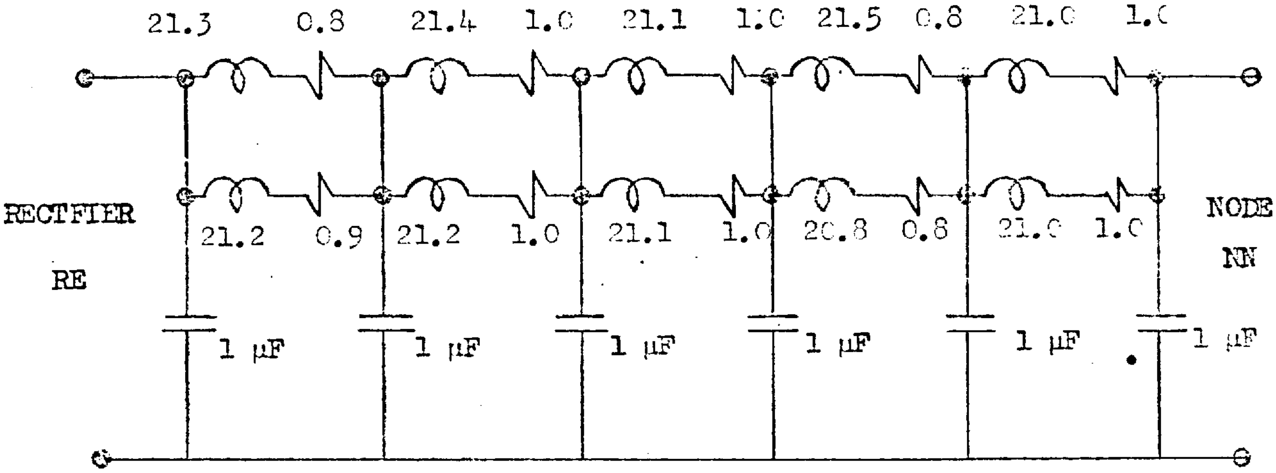


Fig 4.5 Overhead Line Simulation Details.

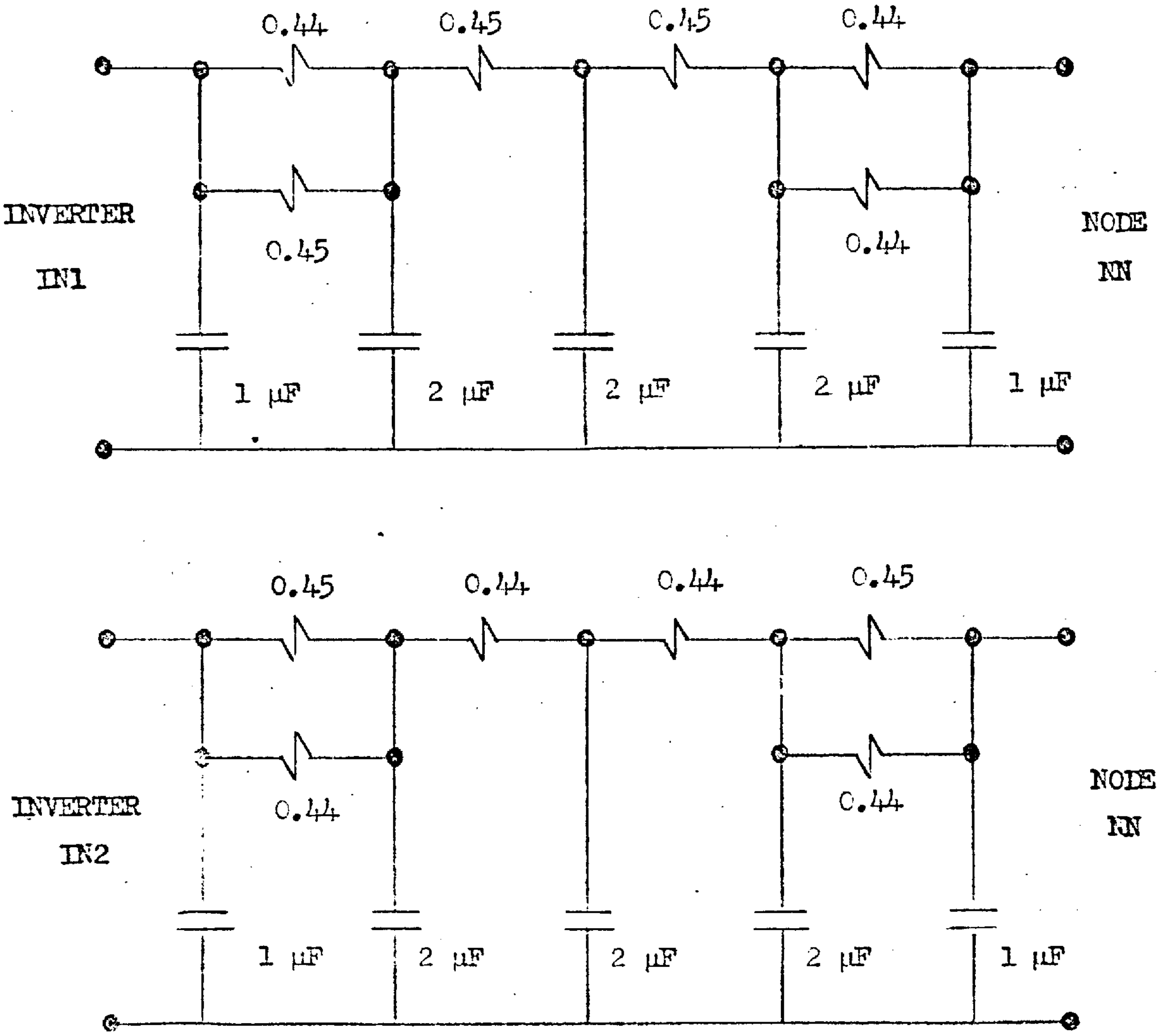


Fig 4.6 Cable Line Simulation Details.

In above figs. Resistance and Inductance values in Ohms and mHen. resp.

The detail transmission system circuit constructed after reducing the above constants to model scale and neglecting cable inductance together with measured component values is given in fig. 4.5 and 4.6. The cable is modelled by 4-sections and the o.h. line by 5-sections. All capacitors are $\pm$ 5% tolerance and the best combinations that could be obtained from the air cored inductors available in the laboratory had to be used. The most serious component error is that the total o.h. line series inductance is 52 mH while 60 mH is theoretically required. The error cannot be avoided as the correct $^R/L$ ratio cannot be reproduced, however inductance errors are not serious because of the presence of a large, 0.56H, smoothing inductor in series with each line.

4.4. Interconnections of the D.C. Transmission System

The system control program, the interpretation of fault signals and the fault control procedure are all dependant on the operational configuration of the system and the need therefore arises to make a systematic classification of the numerous configurations in which a given d.c. system may work. The arrangement used here is especially suitable for adaptive fault programming and can be extended well beyond the three terminal case.

4.4.1. Three terminal system configurations

The fault control program is written for a three terminal, two bridges per converter system, so as to be illustrative of general methods. The availability of isolators and the identification of transmission lines by assigning numerals to their end points is indicated in fig. 4.7. Topologically there are forty eight electrically feasible configurations (or modes) of the lines and bridges with at least one earth isolator closed. However constraints imposed by power system considerations, for example restrictions on cable polarity and earth return restrictions, reduce this number considerably.

For the purpose of this study a number of reasonable and typical power system constraints are postulated and included in the general description of the system below.

Number of converters	Three
Network type	Nodal
Normal rectifiers	Converter RE (200 kv/2000A)
Normal inverters	Converters IN1 and IN2
Normal operation	Full system Earthed at RE only
Earth (neutral) paths	Allowed on all sections To be used only when essential.
Other restraints not implied above.	Unstable modes (see 4.3.3) excluded. Power exchange between inverters is not required.

These constraints reduce the permissible operating modes to fifteen, which have been sketched in fig. 4.8 Apart from problems of interpreting fault signals and building up the best commands for transmission to the individual converter controls, the need for a fully adaptive central control program dictates that these modes be arranged in a systematic manner. A systematic treatment has been achieved by classifying the various operating modes into groups and tiers as in the chart of Table 4.1, from an examination of which the method can be understood. The method is readily extended to the n-terminal case.

This classification achieves the following:-

1. Subsequent to any line to line fault from any initial mode and the isolation of the faulted line, the end mode is at the same tier level of the next lower group.
2. Subsequent to any line to earth fault from any initial mode and isolation of the faulted conductor, the system moves downward from tier to tier within the same group. There is however one set of well defined exceptions to this rule.

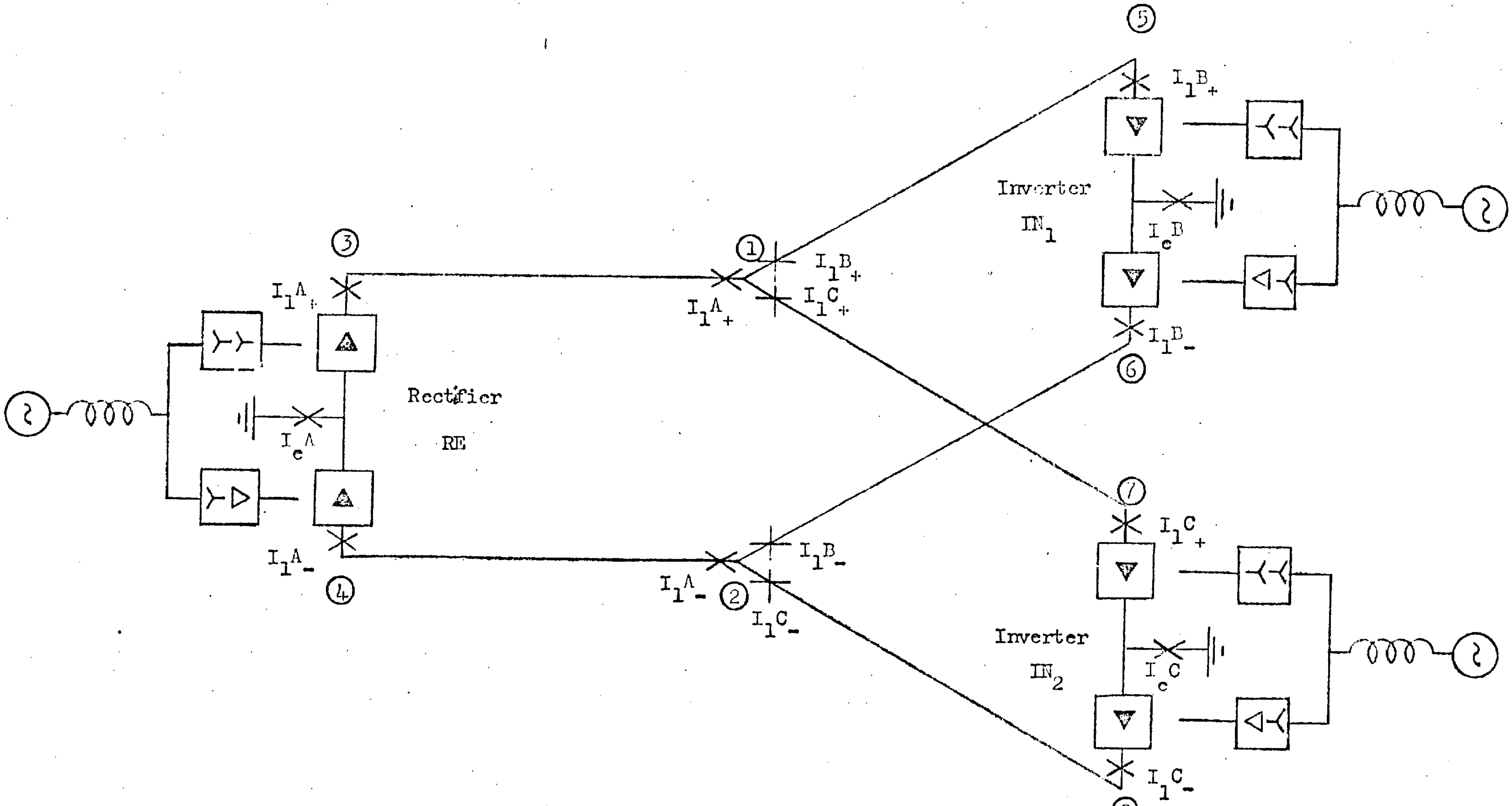


Fig 4.7 The Three Terminal System Investigated.

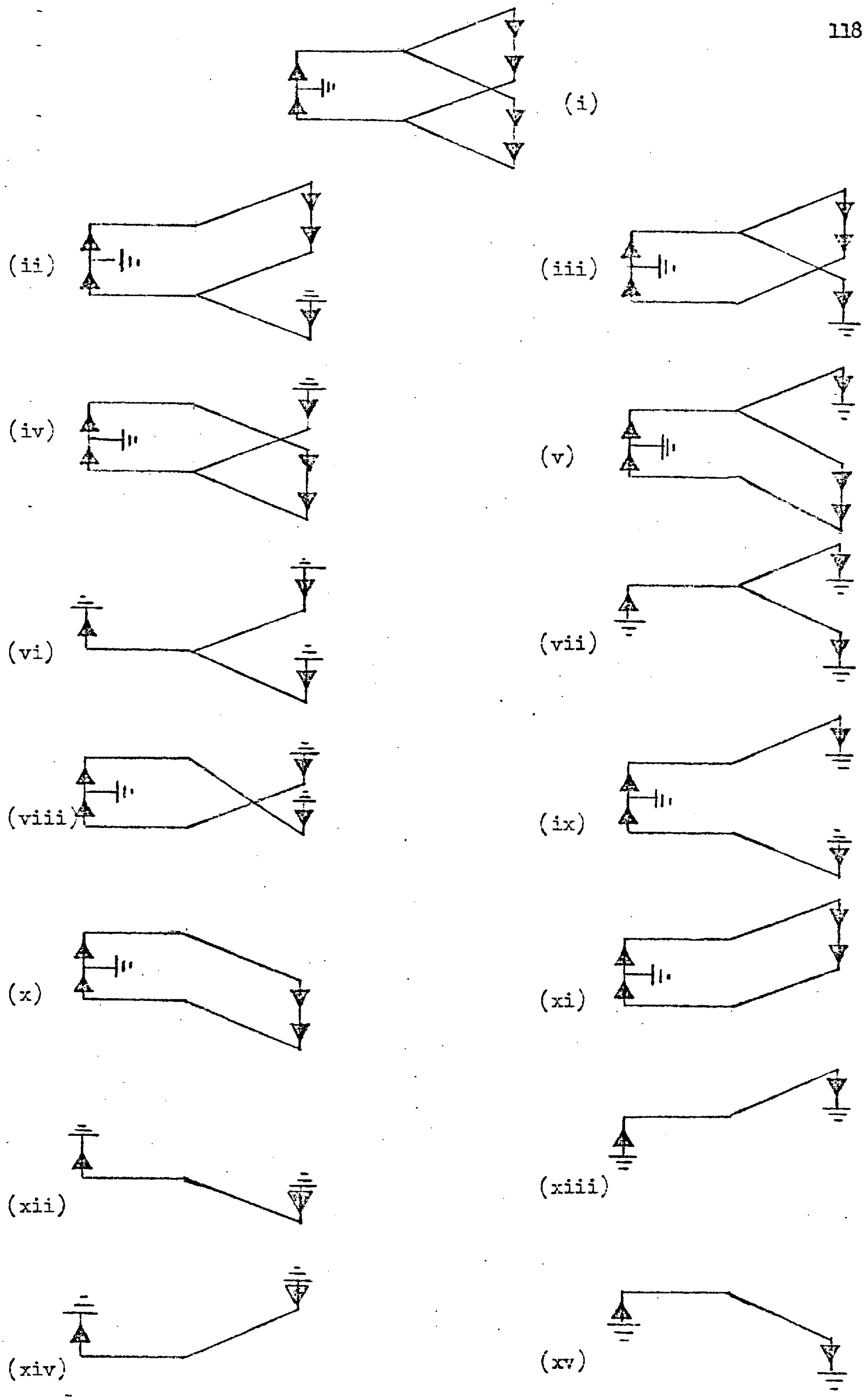


Fig 4.8 System Operating Modes.

TABLE 4.1

CHART DESCRIBING SYSTEM OPERATING MODES.

INTERPRET BLANK SPACES AS 1.

GROUP I

(3 terminal)

TIER		Bridges.						Isolators.								
		A^+	A^-	B^+	B^-	C^+	C^-	IA_e	IB_e	IC_e	I_1A^+	I_1A^-	I_1B^+	I_1B^-	I_1C^+	I_1C^-
1st	1(a)							0		0						
2nd	2(a)					0			0						0	
	2(b)						0		0							0
	2(c)			0						0			0			
	2(d)				0					0				0		
3rd	3(a)	0		0		0					0		0		0	
	3(b)		0		0		0					0		0		0
	3(c)			0			0						0			0
	3(d)				0	0								0	0	

GROUP II

(2 terminal)

TIER		Bridges.						Isolators.								
		A^+	A^-	B^+	B^-	C^+	C^-	IA_e	IB_e	IC_e	I_1A^+	I_1A^-	I_1B^+	I_1B^-	I_1C^+	I_1C^-
1st	1(a)			0	0			0	0				0	0		
	1(b)					0	0	0		0					0	0
2nd	2(a)	0		0	0	0			0		0		0	0	0	
	2(b)		0	0	0		0		0			0	0	0		0
	2(c)	0		0		0	0			0	0		0		0	0
	2(d)		0		0	0	0			0	0			0	0	0

3. The system cannot move between the operating modes represented in the same group and tier.
4. The system cannot move to a higher group or tier.

In the chart of table 4.1 the positions of all isolators (line I_1A +, I_1A −, etc; earth I_eA, I_eB, etc.) and the condition of all six bridges are indicated. The entry '0' is interpreted as a bridge not operating or as an isolator open and a blank space is interpreted as "1" the logical complement of '0'.

The extension of this method to systems with any number of converters, $n > 3$, connected at a single node is straightforward, though from a practical point of view such connections are of trivial importance. Nonetheless when dealing with any general network, whether branch, delta or ring etc., it is necessary and possible to derive a general classification if the writing of an on-line adaptive control program is to be reduced to a systematic and repetitive task. The complexity increases in systems that may divide into two or more discrete sub-systems subsequent to fault isolation.

4.4.2. Operating diagrams of an unconventional configuration

In the modes (ii) to (v) of fig. 4.8 the current settings at the positive and negative poles of the rectifier will in general be different. In order to evolve a convenient diagramatic basis for their representation, fig. 4.8 (iii) is chosen, three concepts are defined and some diagrams sketched.

Through current: This is the component of d.c. current passing in series through both bridges at a converter.

Through current characteristic: This is the operating diagram when all current passes through both positive and negative poles, that is no current in the neutral path.

Neutral current characteristic: This is the operating diagram when non-zero current flows in the neutral path. The shape of the diagram varies with this current.

Let $I_1 + I_2$ and I_2 be the current orders at the positive and negative poles of the rectifier, fig. 4.9. In fig. 4.10 the rectifier positive and negative pole characteristics are sketched separately in (i), (ii) is the through current characteristic obtained by assuming zero neutral current and hence derived as the difference ordinate between the characteristics of (i). The neutral current characteristics for $I_N = I_2/2$; I_2; and $3I_{2/2}$ are sketched in (iii), (iv), (v) respectively with through current as the abscisa. In general the positive pole characteristic of (i) is moved left by an amount I_N and the difference ordinate is plotted to obtain these neutral current characteristics.

The method developed is used to draw diagrams that clearly illustrate the normal operation of the system. Later on these ideas will be used to provide useful insights into system operation during bridge faults. As can be appreciated from the foregoing discussion the system of fig. 4.9 has two degrees of voltage freedom in that the positive pole to earth and the pole to pole voltages can be set independently and at separate stations. Four operating conditions can normally arise and in every case two diagrams have to be drawn as in fig. 4.11, one for pole to pole voltage (against through current) and the other for positive pole to earth voltage (against positive pole current).

The neutral currents in fig. 4.11 (i) to (iv) are given by:-

(i) I_2

(ii) $I_2 - \delta I_2$ where δI_2 is the nett negative pole margin

(iii) $I_2 + \delta I_1$ where δI_1 is the nett positive pole margin

(iv) $I_2 - \delta I_2$

Only the unusual looking second diagram of 4.11(iii) where both rectifier and inverter appear to be on constant current control needs explanation. This is clarified by the third diagram of (iii) which shows the positive and negative poles of RE separately. The operating points are marked and the transmission is quite stable.

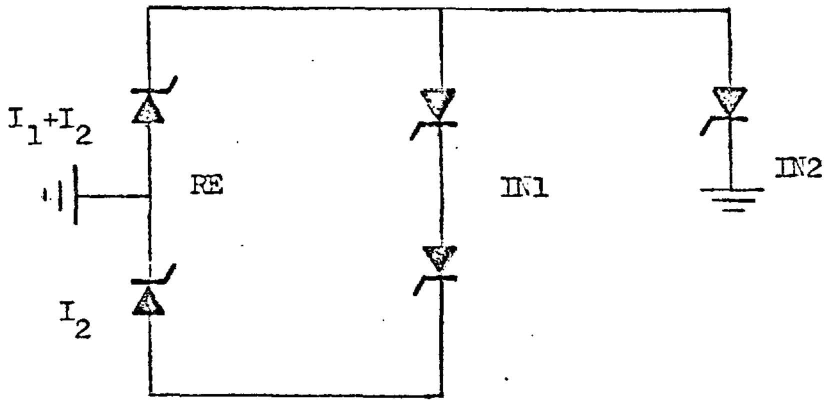


FIG 4.9 An unconventional Operating Mode.

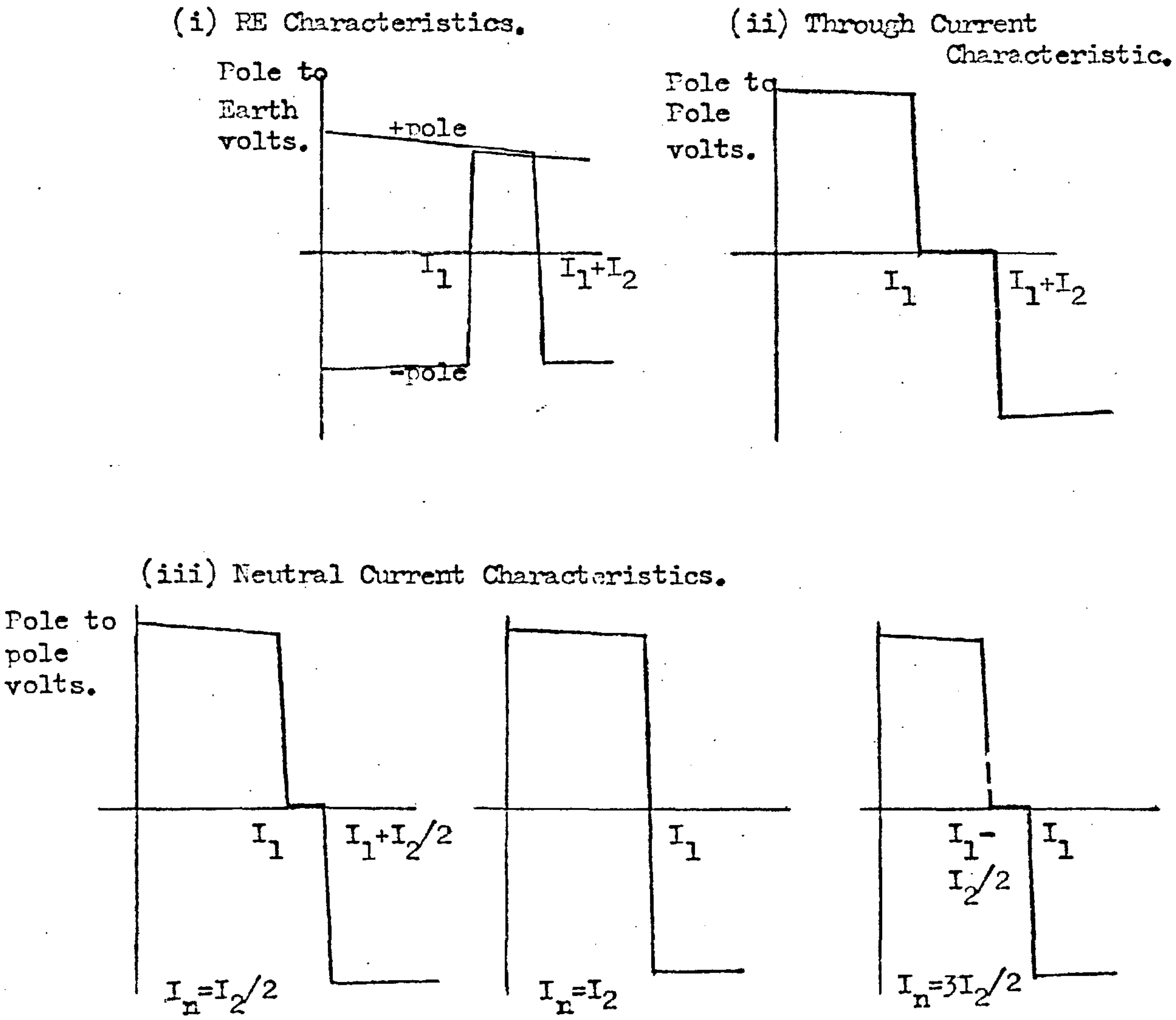
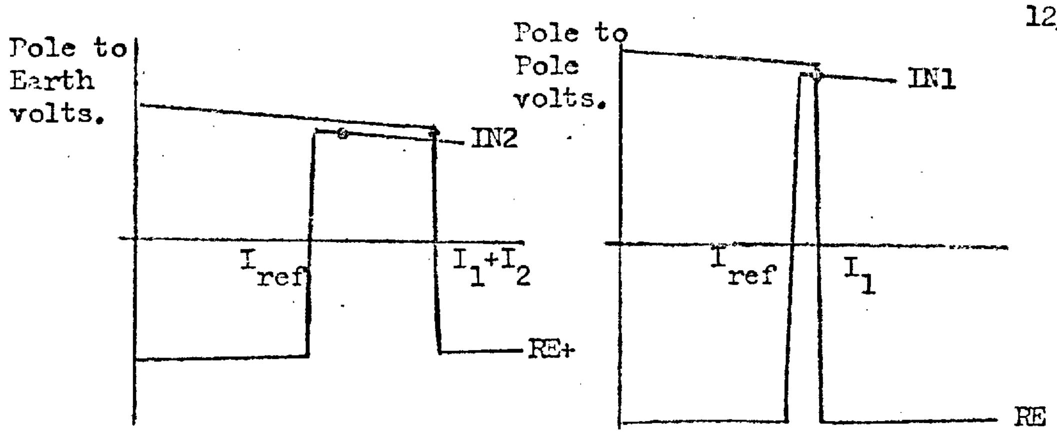
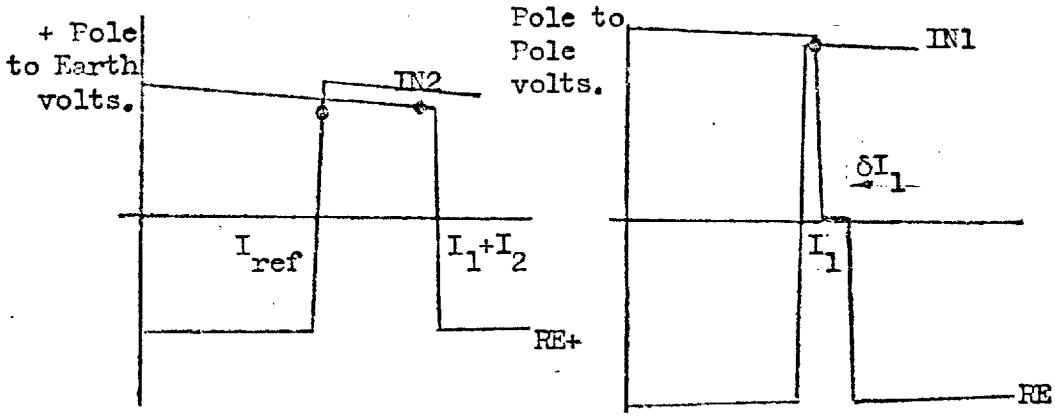


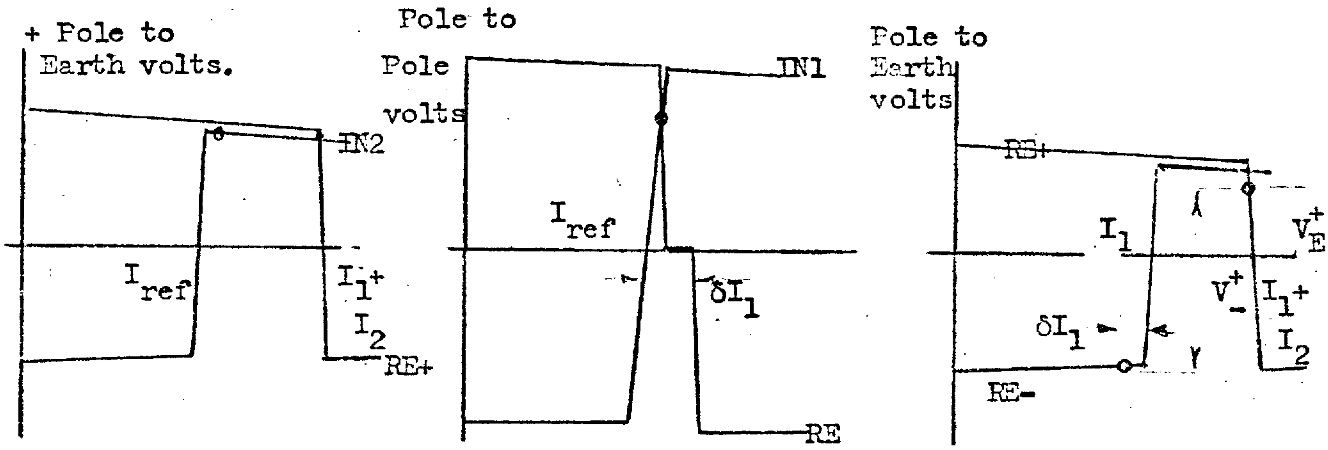
Fig. 4.10 Diagram illustrating Characteristics defined in Section 4.4.2.



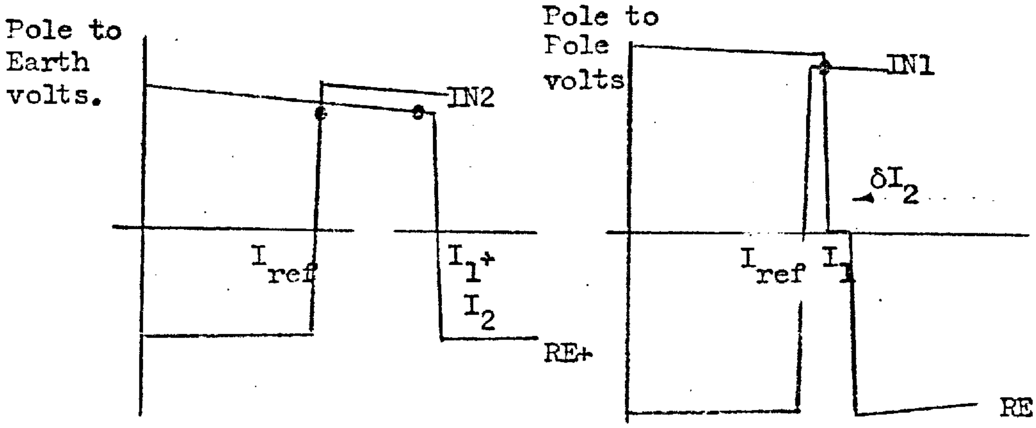
(i) Voltage levels fixed by IN1(both bridges) and IN2.



(ii) Voltage levels fixed by IN1(both bridges) and RE+ bridge.



(iii) Voltage levels fixed by IN2 and RE- bridge.



(iv) Voltage levels fixed by the two RE bridges.

Fig.4.11 Operating Characteristics for Mode of fig. 4.9.

4.4.3. An unstable operating mode

The configuration sketched in fig. 4.12(i) in which the bridge groups are numbered, has been excluded as it is unstable except in the trivial (though in practice the most probable) case where positive and negative pole settings are identical, that is except when unit control is exercised over the bridges at RE and IN1.

In the general case when these settings are different the system voltage can be controlled in one of several ways by the bridge groups as follows:-

EITHER	Bridge group (1. or 5.)	AND	Bridge group (2. or 6.)
OR	(1. or 5.)	AND	(3. and 4.)
OR	(2. or 6.)	AND	(3. and 4.)

All combinations on the first line are stable.

Considering the operating condition where the voltage is set at bridge 1. and bridges 3./4., and writing I_1 to I_6 for bridge currents. I_{01} to I_{06} for bridge current orders and δI_1, δI_2 for positive and negative pole nett current margins,

$$I_{01} = I_{03} + I_{05} + \delta I_1$$

$$I_{02} = I_{04} + I_{06} + \delta I_2$$

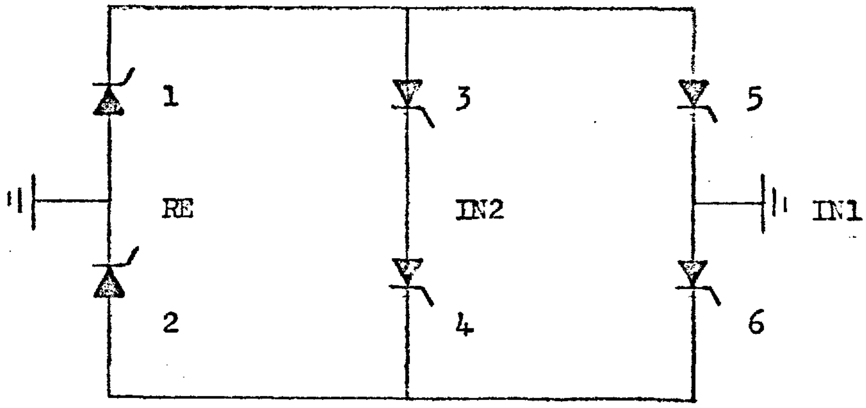
$$I_{03} = I_{04}$$

and since bridges 2, 5 and 6 are necessarily on c.c. control

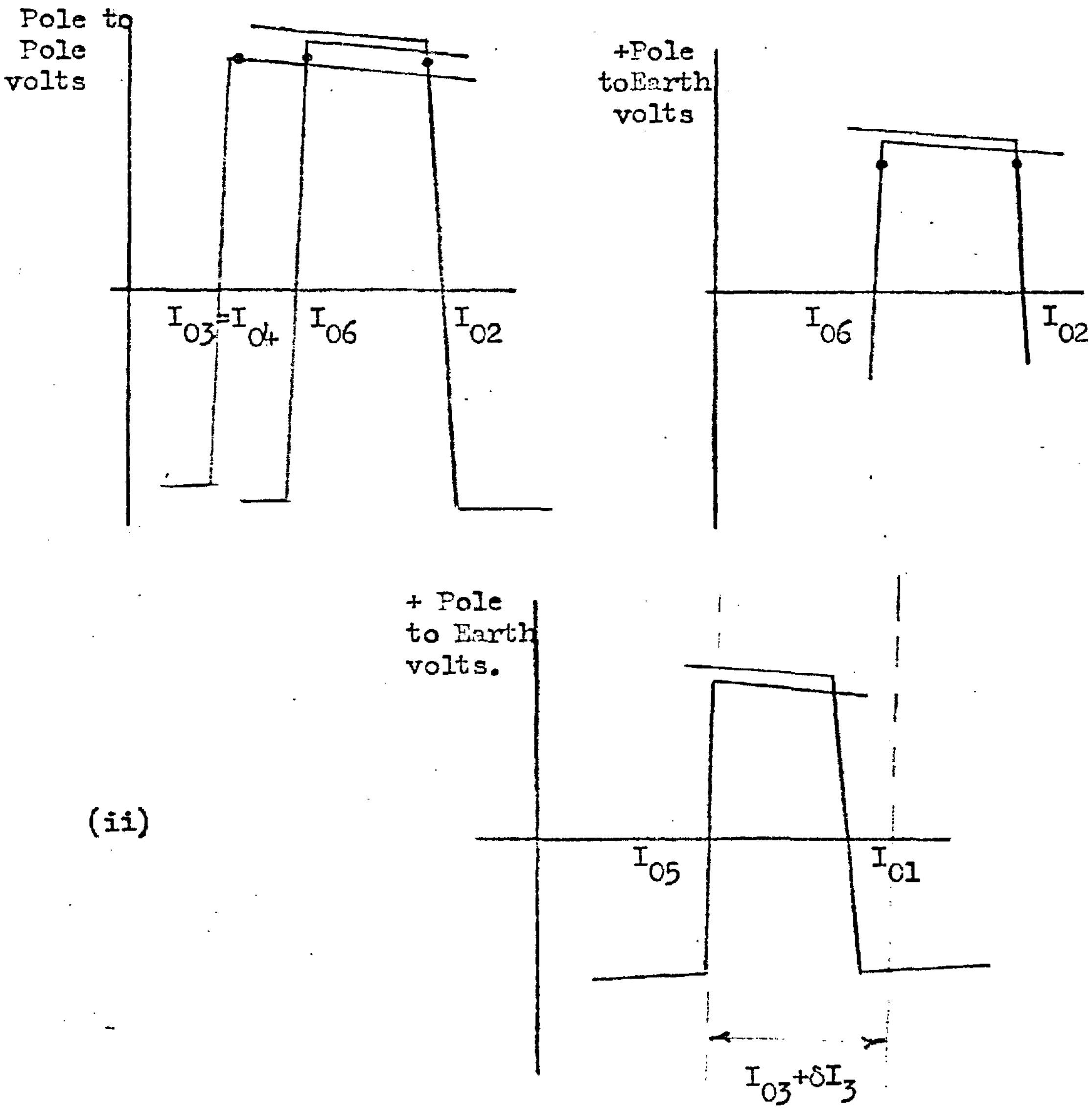
$$I_2 = I_{02}$$

$$I_5 = I_{05}$$

$$I_6 = I_{06}$$



(i)



(ii)

Fig. 4.12 An Unstable Operating Mode and Characteristics.

$$I_3 = I_4 = I_2 - I_6 = I_{04} + \delta I_2$$
$$= I_{03} + \delta I_2$$
$$I_1 = I_3 + I_5 = I_{01} - (\delta I_1 - \delta I_2)$$

Since bridge 1 is a rectifier it is stable in operation only if $\delta I_1 > \delta I_2$. However it follows immediately that should voltage control pass from bridge 1 and bridges 3/4 to bridge 2 and bridges 3/4 the condition for an operating condition to exist is that $\delta I_2 > \delta I_1$. As a result of these conflicting requirements the system is not always stable.

This instability is also illustrated in fig. 4.12(ii) for the case where $\delta I_2 > \delta I_1$ and system voltage levels demand that bridges 1 and bridges 3/4 control the d.c. voltage. Since the line distant $I_{03} + \delta I_2$ from the bridge 5 constant current line has no intersection with the constant α line of bridge 1 no operating state exists and either the entire system or converter 3/4 will extinguish.

4.5 Conclusion.

This chapter has been devoted to a discussion of some extensions of the simulator, that is, the connection of the convertor to the a.c. power system and the representation of the d.c. transmission network. The different operating modes of the d.c. three terminal system also been presented and classified in a chart. The chapter as a whole is intended to serve as a bridge from the description of the simulator design and performance of chapters 2 and 3 to an investigation of the control of the d.c. system under fault conditions.

CHAPTER 5

Fault Control Programmes

5.1. Digital Computer Control-Protection of A.C.- D.C. Systems

The functions of a digital computer in power system operation may be divided into off-line planning and on-line control. The planning of system operation includes long term forecasting, generation and economic dispatch schedule preparation, ensuring security and satisfying reactive power flow and voltage level constraints. The d.c. system and associated filter capacitor banks are easily included in these studies[37]. The constant current or constant power controlled d.c. link presents no problems in economic transmission determinations and it has also been suggested that in load flow analysis of the inter-connected a.c. system the d.c. converters may be treated as current sources and sinks.

On a more long term basis the digital computer is also becoming an indispensable aid to the planning of system extension[34], the collection and processing of power system and energy statistics and the general investigation of system operating techniques.

The computers used for these studies are large conventional calculating machines while the on-line controls discussed below feature smaller process-control type computers fitted with specially designed interface connections.

5.1.1. On-line digital control

On-line digital computer aided control of inter-connected a.c. - d.c. systems includes the control of the system both during normal operation and under emergency conditions. The starting point of normal system control is to achieve the preplanned generation/transmission targets. Unforeseen outages and errors between predicted and true loads make continuous amendment of system operating conditions necessary. In inter-connected a.c. - d.c. systems regulation of power flow and, less flexibly, control of VAr loading in the d.c. ties provide determinate and direct methods of adjusting system operation and must be fully exploited in the control programme. Assessment of the possibility or desirability of d.c. converter operation during balanced and unbalanced faults at various points on the a.c. system and a policy for overload elimination by load rejection are further aspects of power system operation that devolve on the normal control programme. Once the power and VAr loadings of the d.c. links have been defined from these general perspectives the basic operating mode of the d.c. converters have to be chosen. A converter can operate with constant power control, constant current control, constant extinction angle control, frequency sensitive control, etc. The control methods chosen for the stations must be compatible with each other and satisfy the specified loading condition.

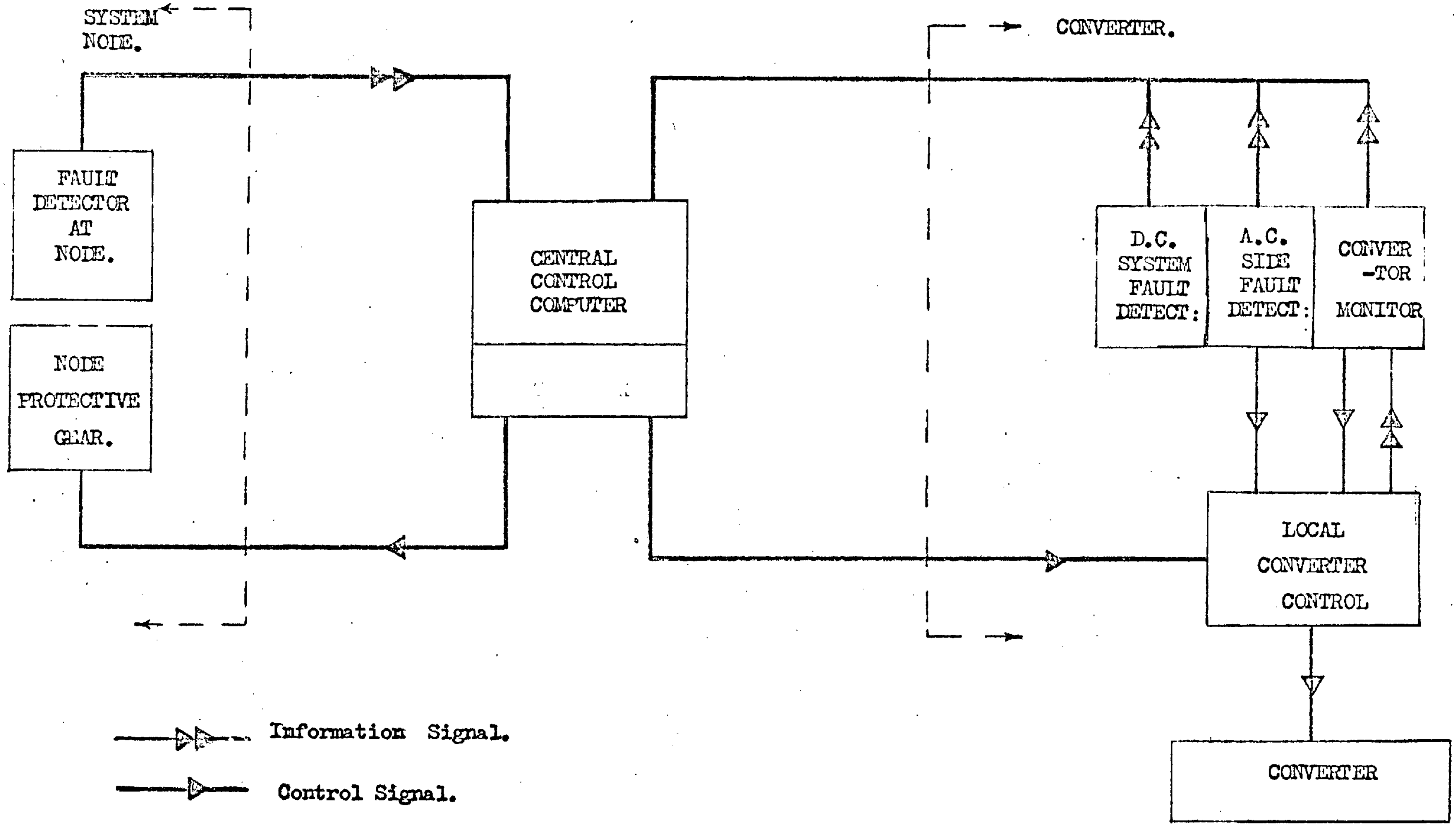
5.1.2. Converter Control

The method of implementing the controls will depend entirely on the structure of the converter controls. It has been suggested[37] that a digital computer pre-programmed for the different methods of control enumerated above may replace the conventional circuits that have been used in the past. Fallside and Jackson[88] have programmed a PDP.8 computer to control the output voltage of a bridge to follow a given reference input signal. The control proposed is of the open loop type where the input signal is sampled at bridge repetition frequency, the sample processed, and then compared with a look up table at 100 μs intervals to determine the instant of valve firing. Ambiguity at starting or due to loss of a firing pulse are avoided by a simple addressing system which identifies pulse-valve pairs. This method of control is wasteful of computer time as the actual time lost per cycle in simply 'looking up the table' is the equivalent of $(n \times \alpha)$ electrical degrees for an n-pulse bridge, firing angle α^{o}.

Digital computer control of a converter can be economically justified only where the computer can be used for other aspects of converter control than as a glorified pulse generator. However, while as at most times the converter is working steadily in an undisturbed system the proposed control scheme requires the computer to cycle wastefully. Clearly, for h.v.d.c. applications, other methods of pulsing and of selecting pre-calculated firing angles must be found.

Horigome et. al.[37] derive a series of equations for calculating the rectifier and inverter firing angles at every firing once the control modes at the terminals are defined. If however this result implies that due to changes in the system any absolute constraint (e.g. valve current rating, inverter minimum extinction angle) is violated an alternative control loop is chosen and fresh calculations have to be performed before the next valve firing so that acceptable firing instants can be re-determined. It can be appreciated that with computer control the alternative control modes have to be checked out in series during system transients, and two or more control loops may have to be obtained in the time between successive valve firings. This however is not the case with conventional bridge control equipment where all the control loops are continuously operating in parallel and one is electronically selected. Proper estimates of the considerable analogue digital conversion equipment required for complete closed loop control when made, may prejudice the economics of computer control.

For these reasons it is believed that for some time to come the immediate bridge and converter control circuits will remain of the analogue static-electric type. The reference inputs, emergency injections and conceivably certain parameters of these control circuits can however be supervised by a digital computer. The computer can either be common to a number of terminals to which it is linked by telecommunication channels or the converter equipment, a.c. system protection and power station controls at the same place may have access to a common computer. Under emergency conditions the affected section will have immediate access to the computer on a priority basis.



Note 1. Only one node and converter shown for simplicity..

Note 2. Monitors and detectors not installed on Simulator.

Fig.5.1 Diagram illustrating Fault Control of Multiterminal HVDC system.

The fault control methods investigated in this chapter and simulated by the on-line control tests are of the type where a central control computer is associated with various analogue fault control circuits at each converter terminal. Before proceeding to describe the programmes that have been developed it is necessary to summarise briefly the under-lying hierarchy of control.

5.2. Local Fault Control

"Local equipment" is that equipment physically located at a converter station, as contrasted to "central" or "nodal" equipment. "Fault control" is the control of an h.v.d.c. system during either transmission or valve faults as distinct from "normal control" which refers to a healthy system.

The philosophy of fault control (fig. 5.1) that underlies the subsequent programmes is summarised as follows:-

1. A central control computer that supervises local control equipment at each converter and receives information from all fault detectors.

2. Whether local control is computerised or static electronic depends on the size and requirements of any particular system and terminal.

3. Converter and valve faults are handled locally whenever possible.

4. For maximum discrimination, and therefore minimum outage on faults, directionally sensitive fault detectors at every node are assumed.

5. Local control is allowed independent action when central control or the communication channel fail.

5.2.1. An assessment of the choice between static-electronic circuitry and a small digital computer for local control

In this section interest is centred on fault control only and a summary of the capabilities of the two alternative methods is given.

(i) Static Electronic Circuits

These controls are built around the normal operating characteristics so as to ensure safe operation of the converters until emergency control instructions have been received from the central controller. Specifically, an overriding constant current limiter and circuits to rapidly reduce bridge currents to a low value when compelled to operate with α near 90^{o} (87) are designed as an integral part of the normal control circuits.

The capability of normal static-electronic controls are summarised below.

a) De-energise and re-start one or both poles with or without simple changes in current/power order in response to central control commands.

b) Fixed rate of shut down and restart.

c) Block-bypass and deblock/remove single bridge units or entire converter without central control intervention in case of valve or a.c. side faults.

d) Back-up protection in case of communication failure.

(ii) Computer Control

A digital computer at the local control level is capable of entering into a conversation with the central control permitting the transfer of large amounts of information when required by the central control. This facility, however, is of no great value under fault conditions as fast control is necessary and the programme relies only on simple logic information from special d.c. fault detecting equipment.

The advantages of computerised local fault controls are summarised below.

a) Start, de-energise or control to any pre-programmed method one or both poles of a converter in response to central control instructions.

b) Rate of shut down and start up are fully controllable and may be programmed to be sensitive to a.c. system voltage and frequency.

c) Block-bypass and deblock/remove single bridge units or whole converter without central control intervention in case of valve faults and automatic "fault development control"[86].

d) Flexible control programmes can be written to aid the recovery of the a.c. system following a.c. faults. However, gathering and processing the correct intelligence is an important problem that awaits study.

e) Flexible control programmes in the event of communication failure.

f) Programmes are easily modified or extended.

g) Simple interfacing with the central control computer. Logic decoding replaced by programmed decoding.

By comparison of (i) and (ii) above and bearing in mind the discussion of Section 5.1.1. it is concluded that the use of a digital computer for local fault control is not justified unless it can be combined with a.c. side fault detection and protection and also made available for general extended programming for normal control and optimisation studies.

5.3. The Transmission Fault Control Programme

5.3.1. Why Logic?

It is very desirable that the information channels be limited to cheap simple types, preferably using ordinary telecommunication equipment. Information will be required to be transmitted to the central control from (i) fault detecting equipment at the system nodes; (ii) transmission system protective equipment at the converter terminals;and (iii) converter/bridge monitoring equipment. High speed of protection and the transmission of data from many points in the system to ensure adequate discrimination are essential. The commands from the control centre to the local converter controls and the transmission node will begin a sequence of de-energising and re-starting operations together with the opening or closing of isolators. It is evident that with these limitations information can and should be binary, i.e. logic (YES/NO) form. Apart from the logic type of information if in some cases a small amount of binary coded analogue information is transmitted, only marginal changes in the main control programme need to be made.

5.3.2. Information transmitted on faults

It is assumed that the information from the terminal fault sensing equipment will contain the following items:-

(i) Whether a line to line or line to earth voltage collapse has been detected at the converter terminal.

(ii) If line to earth the polarity of the fault.

(iii) The state of the converter bridges.

(iv) If a commutation failure or an a.c. side disturbance has caused bridge failure, the polarity of the bridge that has failed. The types of bridge failure or a.c.

disturbance that can cause spurious fault detection are communicated to the centre.

A minimum of four information bits is required to carry this information. The nature of the information is such that high reliability in transmission is indispensable and an error correcting code will have to be employed. Hammings' error correcting code is suitable requiring three or four error correcting bits to be added to the transmitted word. In general with Hammings' code the word length is $2^k - 1$ where k is the number of error correcting bits. This will ensure that any single error is detected and corrected while a twin error will be detected but not corrected. Two additional leading bits are added for differentiating between normal system information and emergency fault information and for the purpose of identifying the information source.

The information from the system node points must identify the fault as line to line or as line to earth and in the latter case the fault polarity. Whenever possible the node must further discriminate directionally, that is,carry information that the fault detected is towards converter stations RE, IN1 or IN2. Here too the minimum number of information bits required is four and leading bits and error correcting bits will be added as suggested earlier.

Hence,in either case a ten bit word length will adequately convey sufficient information for emergency fault control.

The incoming information is decoded by the fault control program and stored in the computer memory as five bits in the case of terminal end information and twelve bits in the case of node point information. Symbols A, B, C and M are used for information originating at the three converter stations and the node respectively and subscripts 1 to 5 and 1 to 12 are attached to these symbols with the meaning given below. The symbols are explained by posing questions, such that if the answer is a YES its value is a binary 1 and if the answer is NO its value a binary 0.

A_1	B_1	C_1	Has a collapse of line to line voltage been detected?
A_2	B_2	C_2	Has a collapse of positive line to earth voltage been detected?
A_3	B_3	C_3	Has a collapse of negative line to earth voltage been detected?
A_4	B_4	C_4	Has the converter positive bridge failed?
A_5	B_5	C_5	Has the converter negative bridge failed?
M_1			Has a line to line fault towards RE been detected?
M_2			Has a positive line to earth fault towards RE been detected?
M_3			Has a negative line to earth fault towards RE been detected?
M_4			Has a line to line fault towards IN1 been detected?
M_5			Has a positive line to earth fault towards IN1 been detected?
M_6			Has a negative line to earth fault towards IN1 been detected?
M_7			Has a line to line fault towards IN2 been detected?
M_8			Has a positive line to earth fault towards IN2 been detected?
M_9			Has a negative line to earth fault towards IN2 been detected?
M_{10}			Has a collapse of line to line voltage been detected?
M_{11}			Has a collapse of positive line to earth voltage been detected?
M_{12}			Has a collapse of negative line to earth voltage been detected?

These last three information bits are to be used in cases where the fault sensors at the node detect a fault,but it is not possible to discriminate accurately the direction from the node in which the fault has occurred.

5.3.3. Formulation of Boolean Equations

It is now possible to formulate Boolean equations to test for every type of fault from any initial mode (see Sect. 4.4.2) of the system and to suggest the order of priority in which these tests should be made. The equations are solved on the basis of the available information and the derived values of any words not received are set to zero in the above list.

The symbol F is used to indicate the presence or absence of transmission line faults, F = 1 if a positive fault indication results from carrying out the Boolean expression that F is equated to, if not F = 0. F always appears with superscripts and subscripts indicating the line elements between which a fault is searched for. For example F_{24}^{13} is used in connection with a fault between conductors 13 and 24 of the system, i.e. a line to line fault on the line section between the node and converter station RE . F_{17}^{E} similarly refers to a line to earth fault on positive conductor 17 between node and station IN2. The line section nomenclature follows fig. 4.7.

The Boolean equations written in terms of the previously defined Boolean variables for every fault from all fifteen permissible operating modes of the d.c. system are given in Appendix 1. The operating modes and their naming was treated in Section 4.4.1.

In every mode the equations are solved in the order in which they are written, which is to say the equations are written in their order of priority. Hence in mode G1/T1(a) the information is checked first for a line to line fault between 13 and 24 (F_{24}^{13}) and thereafter for line to line faults between 15 and 26 (F_{26}^{15}) and between 17 and 28 (F_{28}^{17}). If these three tests do not give positive fault indication a check is made for a line to line fault between the positive and negative conductors whose position cannot be localised (F_{-}^{+}) to account for cases where sufficient intelligence to satisfy the first three tests is lacking. In the absence of line to line faults the computer program proceeds to check for faults on the positive or negative lines to earth in a very similar fashion.

The nature of the Boolean equations is best understood by examining one of the longer equations in some detail. Selecting for example the equation that checks for a +line to earth fault anywhere in the system of initial mode G1/T1(a).

$$
\begin{aligned}
F_{+}^{E} = \; & M_{11}.(A_4'.B_4'.C_4') \\
& + A_2.(B_4'.C_4') + B_2.(C_4'.A_4'.) + C_2.(A_4'.B_4') \\
& + M_{10}.(A_4'.A_5 + B_4'.B_5 + C_4'.C_5) \\
& + A_1.(B_4'.B_5 + C_4'.C_5) + B_1.(C_4'.C_5 + A_4'.A_5) \\
& \qquad + C_1.(A_4'.A_5 + B_4'.B_5)
\end{aligned}
$$

The first term will provide a positive fault indication (1 or YES) if the node point detector has seen a positive line to earth fault ($M_{11} = 1$) AND none of the positive side converter bridges have failed ($A_4 = B_4 = C_4 = 0$).

The next three terms on the second line of the equation will provide positive fault indication if any one or more of the terminal fault detectors have sensed a positive line to earth fault (A_2 OR B_2 OR $C_2 = 1$) AND the positive bridges of none of the other stations have failed.

The term on the third line of the equation will provide positive indication if a line to line fault has already NOT been detected - since the above equation is solved after F_{-}^{+} has been checked - AND the node detector has indicated a line to line fault ($M_{10} = 1$) AND the negative side bridge but NOT the positive bridge at some converter station has failed (e.g. $A_4 = 0$, $A_5 = 1$).

The three terms on the fourth line of the equation will indicate fault presence if the protective equipment at one or more terminals has sensed a line to line voltage collapse (A_1 OR B_1 OR $C_1 = 1$) AND the negative bridge but NOT the positive bridge at EITHER of the other two stations has failed (e.g. $A_4 = 0$, $A_5 = 1$).

A closer examination of the sixty eight equations in Appendix A shows that all of them can be built up by merging two or more of twenty two basic full length equations. In certain cases selected irrelevant terms in the basis equations have to be simultaneously suppressed, as for example in two terminal operating modes all references to the third non operating converter must be deleted from the basic equations. This is easily arranged by putting the information bits corresponding to irrelevant terms equal to 0 prior to solving the equations. Hence the computer programme carries twenty two sub-routines, being the stated equations in the Appendix, in some of which provision is made for suppressing computation of selected terms if desired. On apparent fault indication from some part of the system the on line control calls such sub-routines as are appropriate to the initial mode that the system is operating in.

The actual equations themselves and the method of solution via twenty two independent sub-routines is specific to the three terminal system and to the type of information postulated. This in turn depends on the type of fault sensors or detectors installed in the h.v.d.c. network. It follows then that if the characteristics of the fault sensors installed in a system or the structure of the network itself differs, the equations suggested above will need to be modified to accommodate the changed character of the information. However it is anticipated that in any control scheme that relies on logic methods the approach to the problem of accurate fault detection and the broader lines of the fault control programme will be similar to that proposed.

5.3.4. The Commands from Central Fault Control

Any instruction to the node point will open one or more of the six line isolators at current extinction and include a reset instruction to fault detectors. The minimum number of information bits required for this command is four and with the addition of Hammings' error correcting codes and the leading transmission bits a ten bit word is used.

The fault control signal to the converter stations will either request no action - i.e. reset - or the de-energisation of one or both poles and, when required, the restarting of one or both poles. Whenever both poles are to remain operational in the post fault mode the instruction must specify whether the earth isolator is to be open or closed. A minimum of four binary bits is required to contain this basic set of instructions. Usually further instructions specifying restart at reduced or increased current settings or for variable rates of shut down require to be transmitted and hence two or more information bits require to be added depending on the flexibility required. Together with identification and transmission synchronisation binary elements and error correcting codes the word length reaches thirteen bits. It is preferable in this case to transmit two independent and successive ten bit words, one with de-energise and/or shut down instructions together with the rate of de-energisation, the second with restart instructions and the new current settings. In this way a ten bit word has been standardised for all information flows in the system. Where the receiving station controls are of the static electronic type with no computational facilities compressed coding is avoided and instructions transmitted on the basis of one specific instruction per bit.

5.3.5. Programming

The on-line control programme is illustrated in the flow diagram of fig. 5.2. The programme is capable of finding the location and type (line to line, line to earth positive or negative pole) of fault to the greatest degree of accuracy possible with the information available at the time of execution. Thereafter the minimum necessary section of the system is de-energised and a single system re-start is attempted. In the event of a second and immediate failure of the same transmission line the minimum number of lines and bridges compatible with the constraints of the network is isolated. For example an earth fault on the positive conductor between the node and inverter IN2 will entail the permanent disconnection of this conductor and the positive bridge at IN2. However if the positive conductor to the rectifier station RE is faulted the entire positive pole is shut down as power exchange between the inverters is excluded; the negative pole remains fully operational.

Receipt of fault information on any input channel interrupts the computer which begins to scan all incoming channels for further signals. Since the utilisation of the discriminating capacity of the on-line control programme depends on the amount of data collected, a compromise must be struck between flexibility and scan time limiting. If at least a single signal word is received from every converter and node the scan is terminated, otherwise the scan is terminated by a clock whose setting is variable between one and five a.c. cycles (20 to 100 m sec). In laboratory tests the setting has been raised to a very large value as all simulated fault information has to be set up manually on the computer input channel. In the event of a clock out from the scan routine it is assumed that the converters at all stations from which no signal is received are healthy and the transmission fault detectors unexcited. The effect of this is that a voltage collapse arising from converter faults will be treated as a transmission line fault and therefore the method fails to safety.

At the end of the scan the available information is decoded and stored and the programme is then routed to one of fifteen parallel sections corresponding to the initial mode of operation of the d.c. system. The appropriate Boolean equations are selected and solved in their order of priority. In the event of a positive fault indication from any Boolean expression the programme moves out to classify the fault by type and location simultaneously with the preparation of the commands to be transmitted. In the absence of a fault 'no fault' and 'reset' commands as necessary may be loaded into the transmit routine. In the laboratory a dummy Ø Ø Ø Ø signal is successively loaded.

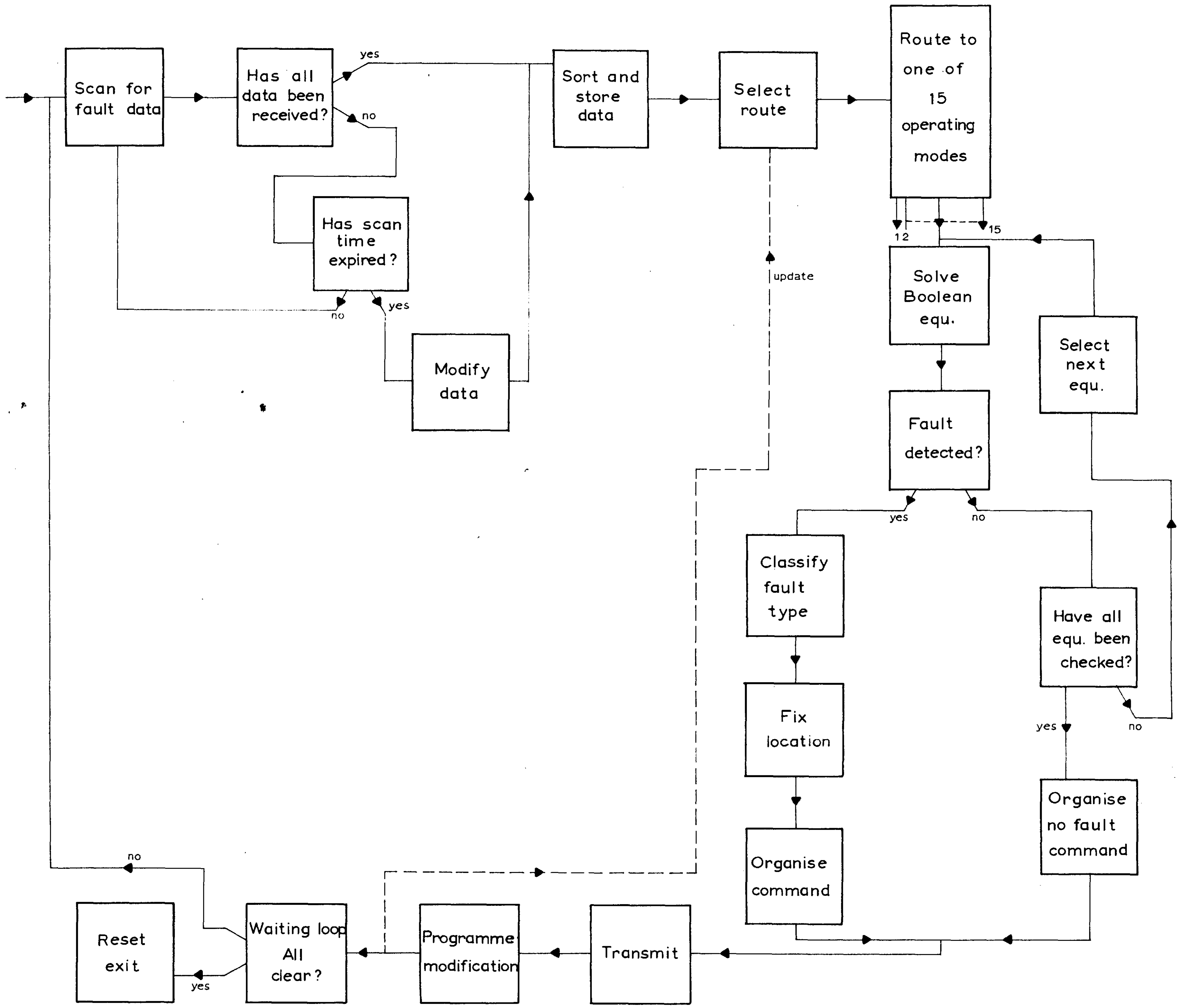


Fig. 5.2. Fault Control Programme - Flow diagram.

A transmit routine is next called to transmit these commands. In a realistic system the computer would interface with telecommunication transmitting equipment; in the laboratory tests these commands are passed on to a separate programme which successively loads the direct digital and digital to analogue channels of the PDP-8 computer with a decoded version of these signals together with an address to identify the stations for which the signal is intended. When the new mode of system operation resulting from the execution of these commands by local control equipment is different from the initial operating mode, the Routing section of the programme is updated accordingly. The programme finally enters a waiting loop to ensure that the power system restart is successful.

The Basic Control Programme takes up approximately two thousand five hundred locations of PDP-8 core memory, that is about two thirds of available computer core store. The programme, as written, has been simplified at certain points not significant from a laboratory testing point of view, for example the error correcting coding and de-coding procedure has been dropped. The PDP-8 is a twelve bit word, 1.6 μs per memory cycle computer. The word length is the most serious limitation of this computer as the number of memory reference instructions are limited to six, and from any one memory location all but 128 of the other locations have to be addressed by an indirect addressing technique which wastes an additional memory location for each distant location addressed. The execution time of the fault control programme varies with the type of fault and the initial mode of d.c. system operation. Line to line faults will be detected in a shorter time than line to earth faults and naturally faults whose location in the network is determinate from the available intelligence will be detected in less time than a fault of unknown location. The maximum and minimum execution times, excluding the scan time and the final waiting loop, both of which can be set by the operator, varies from 25 m sec to 5 m sec respectively.

5.3.6. Modifications to Programme

The simple entry routine into the fault control programme suggested above will need to be modified and refined considerably in any practical application. Some of these requirements are discussed here and the first of these has been programmed and tested separately. It has not however been attached to the prepared main programme as it will not be required in the envisaged laboratory simulation usage.

1. The Fault control programme as written is not capable of handling simultaneous or overlapping multiple faults or of utilising data arriving after execution has commenced. Information signals received between the exit from the SCAN routine and the final return is completely neglected. Fig. 5.2. is a simple flow diagram of a partial solution to this problem. All incoming information is recorded on registers which are cleared when the programme exits from the SCAN routine to the next stage of the fault control programme. Information arriving during execution is stored on these registers up to maximum of one signal word per channel. The main programme exit routine checks these registers and if non-zero the information is further checked for equivalence with the fault currently attended. If a new fault is indicated the programme returns to the fault routine after up-dating stored information.

2. Information about self-correcting converter failures and local block-deblock sequences requiring no central control intervention is transmitted to prevent spurious system tripping. This must not initiate the SCAN routine but data is directed to a temporary store for a pre-determined time interval after which it is erased. From observations of the simulator behaviour it appears that this time interval should be about four times the line natural oscillation frequency plus the block-deblock or commutation failure period.

3. Intelligence arriving during execution, if used via data-break facilities on the computer, will enhance the reliability of control.

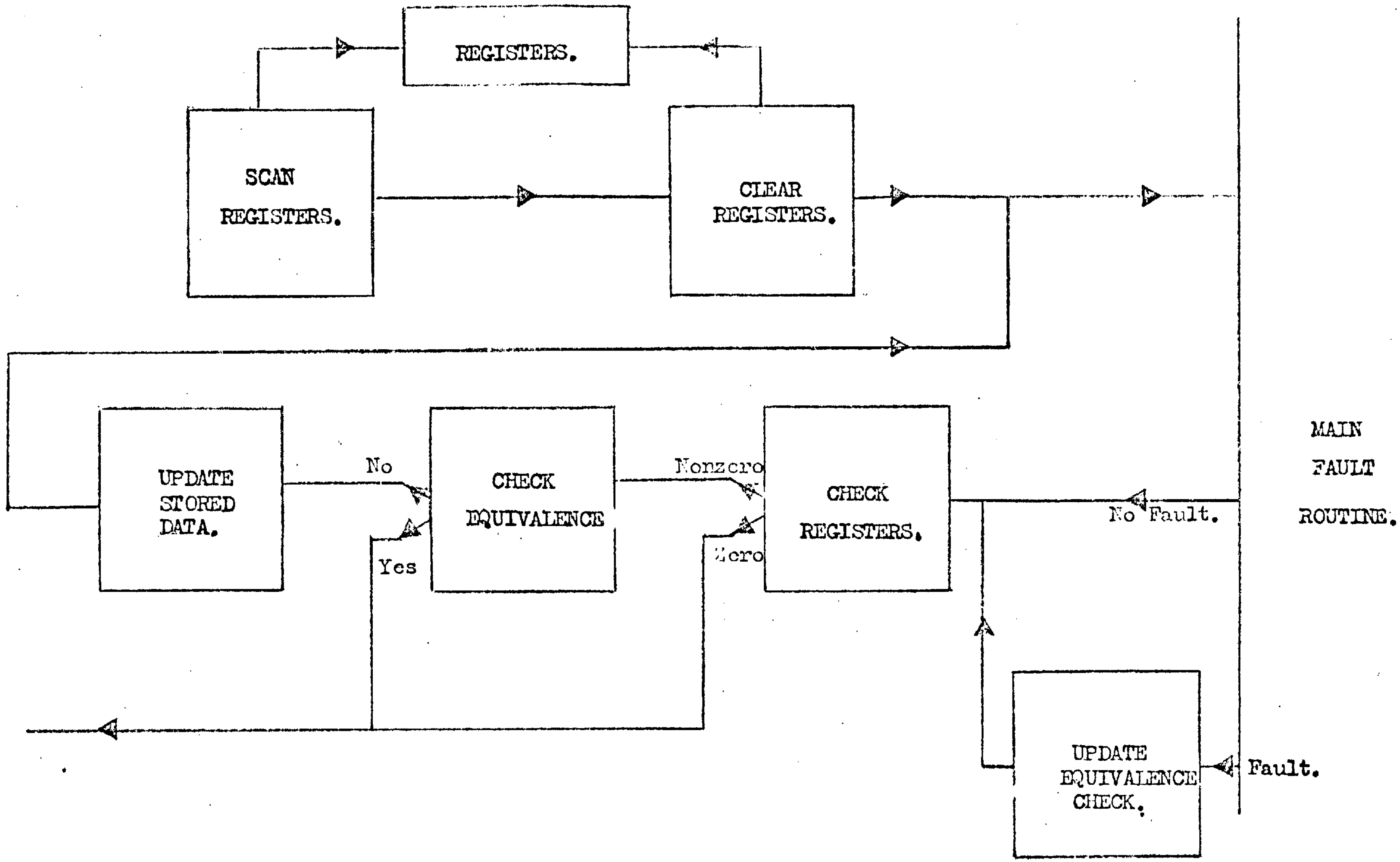


FIG. 5.3 Modifications to Control Programme.

4. Much work remains to be done on peripheral regions of the fault control programme to obtain the best co-ordination with the adjacent normal control programmes.

5.4. Converter and Bridge Failures

Commutation failures occurring occasionally in converter valves are usually self-correcting and require no control action. Their occurence must however be reported to the central controller when the possibility of spurious fault detection elsewhere in the system arises. It is advisable to log random commutation failures for statistical analysis.

5.4.1. Clearing of repetitive faults by local control

When valve faults are not self-correcting one or more attempts are made by the local controller to clear the fault without reference to central control, which is merely warned. Often the effects of a block-bypass-deblock sequence at a converter bridge are of some importance to the connected a.c. systems, as for example in the case of a d.c. link connected to isolated generators or where the a.c. system voltages can change excessively after current rejection. A simplified analysis of the steady state features after by-pass valve operation can be made in terms of conventional voltage-current characteristics. It is easy to show that in any stable operating configuration of the system, (e.g. fig. 4.8 (i) to (xv)) with conventional control characteristics a single-bridge block-bypass operation at any converter cannot cause power flow reversal at the faulted or any other converter, though partial or total load rejection is unavoidable.

The number of times a bridge may be blocked and de-blocked to clear a valve fault will depend on both the a.c. system and on valve properties. The conservative restrictions now imposed by valve makers can be only removed after long experience, as yet lacking, with h.v.d.c. schemes.

5.4.2. Direct-local removal of a bridge

Under certain circumstances a bridge may be disconnected by the local control circuits, and sometimes the removal is directly under central control supervision. When one of many bridges per pole is faulted the healthy bridges continue to operate in series with the bypass valve of the faulted bridge. Whether the station is a rectifier or an inverter the faulty bridge is invariably blocked and bypassed locally but subsequently normal (not fault) control has to choose between disconnecting the terminal or operating the pole at reduced voltage.

In converters with only one bridge per pole a faulty bridge can be blocked without bypassing only if it is initially rectifying. Central control may then have to alter the current order settings throughout the system and this may be done before or while blocking the rectifier. In the former case the voltage controlling inverter is transiently overloaded and in the latter case transient power fluctuations and reversals occur on one or both poles. The method of revising current orders must follow a simple standardised procedure to avoid softwave complications not necessary in a fault routine. Rectifier loadings are increased in proportion to their ratings, while still observing ceiling current constraints, and a residual error is disposed of by reducing inverter loads preferably in proportion to their individual ratings.

5.4.3. Disconnection of a faulty bridge under central control supervision

A temporary de-energisation of one or both poles of the system prior to bridge disconnection is sometimes unavoidable for the following purposes:-

1. Removal of an inverter bridge not in series with any other bridges on the same pole.
2. Removal of a rectifier bridge.

a) Where direct local by-pass operation implies working with half voltage between poles and it is desirable to change to single pole operation via neutral.

b) Direct local blocking leaves the d.c. system in an unstable or otherwise unacceptable mode and therefore a new mode must be switched into.

c) Local control fails to block the bridge and fire the valve e.g. for two valve failures or a control circuit failure.

Under these circumstances the central control programme is required to send complete restarting instructions and the system classification chart, table 4.1, must be used as in the transmission fault control programme.

The speed at which the system has to be run down varies with the nature of the fault. Line and cable faults require very fast de-energisation and the same applies to rectifier back fires not successfully bypassed. Commutation failures not successfully bypassed are less serious. Consequent to a failure that has been successfully bypassed but requires both poles to be de-energised before restart, a slow shut down is acceptable. Current/power orders to the system are slowly and evenly reduced chiefly to minimise disturvance to the a.c. system and to achieve co-ordination with compensating changes that may be made elsewhere in the system.

5.4.4. Automatic extinction of an inverter

The method of bridge disconnection under central control supervision discussed above requires the initial de-energis - ation of the system. This is a serious limitation. An alternative[42] method, that is suitable for certain rectifiers and inverters in some inter-connection modes, is to initially revise voltage levels throughout the system to ensure that the faulty bridge takes over the function of voltage control. Thereafter all system current orders are revised gradually to reduce the current in this bridge to zero, or in the case of an inverter to the margin value above zero. A low current isolator can now open the circuit at the bridge to be disconnected. The method is slow but the rate of shut down is variable and it also has the advantage that the participation of local controls at the faulty station are not required.

5.4.5. Summary of methods for handling single bridge failures

The following table summarises the types of single bridge faults that can be encountered and the methods of protection. All those methods that can be tested on a three bridges simulator have been programmed and checked as separate routines, but a composite programme, as in the case of transmission faults, has not been prepared.

Converter type	Fault type	Method of protection
Rectifier	Single valve permanent failure	1. Local removal 2. Central control when local removal violates system constraints.
Inverter	Single valve permanent failure	Central Control a) De-energise restart b) Auto-extinction
Rectifier and Inverter	Failure of one bridge when more than one bridge in series on each pole	Local bypass. Followed by removal of all bridges if reduced voltage operation is undesirable.
Rectifier and Inverter	One pole in by-passed condition	De-energise one or both poles as necessary and restart
Rectifier and Inverter	Local control failure a) Failure to extinguish bridge b) Failure of control circuits	De-energise and restart. Auto-extinction depending on extent of control circuit failure.

Converter type	Fault type	Method of protection
Rectifier	Failure of communication channel	Local removal
Inverter	Failure of communication channel	Bypass locally. Operate a.c. breaker when necessary.

CHAPTER 6

Fault Control Tests on the Simulator

The performance of the h.v.d.c. simulator, controlled under fault conditions by the PDP.8 computer, has been investigated when clearing numerous types of transmission and convertor and faults. These tests are described in this chapter and a selection of the waveform recordings that were made are presented.

6.1. Converter Fault Control Circuits

Analogue fault control circuits have been constructed for the fast shut-down and start-up of the simulator bridges in response to instructions from the central control computer. The method of emergency control used is to inject signals into the firing angle control circuits and to avoid changing any of the settings of the normal control circuits except when the post-fault and pre-fault operating conditions differ. Each terminal is provided with a complete group of these emergency controls. The immediate interface at the computer is the direct digital output channels and the digital to analogue (D/A) converter output channels. The direct digital input is used to enter fault information into the programme. The D/A outputs from the computer may be plugged into the constant current controller reference inputs to reset the converter current orders after de-energisation and before re-starting, or to alter the operating conditions of the energised system. The direct digital output takes the place of the telecommunication channels that would be used in a power system. Monolithic diode-transistor logic silicon integrated circuit devices are wired to function as de-coders for the direct digital signals. The output of the decoding circuits pulse control the analogue fault control circuits whose functions are discussed below.

1. Fast de-energising circuits.

The circuit diagram of the converter rapid de-energising circuits and the variation of the converter controlled firing angle, which corresponds to the control circuit output voltage waveform, are illustrated in fig. 6.1(a) and (b) respectively. The function of this circuit is to rapidly move the converter into the inverting region by increasing the firing angle to a preset value and drain energy out of the transmission system. However, very large values of firing angle (i.e. in excess of 160°) are not approached to avoid transient commutation failures that can occur despite the protection afforded by the constant extinction angle control circuit. The rate of change of firing angle is also limited to less than 30° change between successive firings to minimise stress on the valves. The circuit is triggered on and off by negative going pulses at the corresponding inputs. Usually, the converter is blocked at current zero and the de-energising signal may, thereafter, be turned off.

The points a, b and the time interval α of fig. 6.1.b are defined as follows:-

	Rectifier	Inverter
a - delay angle (degrees)	35	90
b - delay angle (degrees)	150 to 160	150 to 160
c - m sec	10	20

When the converter is to be run down more slowly the current order to the constant current control circuits may be reduced at the appropriate rate, under programme control.

2. Fast re-starting circuits

The rectifier and inverter circuits for the quick restarting of a converter, e.g. subsequent to fault isolation, together with the firing angle output waveforms of these circuits are illustrated in fig. 6.2 (a,b) and 6.3 (a,b) respectively. The inverter restart circuit performs the function of not permitting the inverter firing angle to become less than a preset value of 120° in this instance. This is necessary in order to prevent the reversal of power flows which would otherwise occur at the inverter when deblocked due to the normal action of the constant current control circuit in attempting rectification to build up current. The rectifier re-start circuit builds up the rectifier full forward voltage in about two a.c. cycles and precludes the sudden energisation of the line at full voltage when the rectifier is deblocked.

3. Converter blocking circuit.

This is a simple bistable followed by a drive stage and triggered by negative going pulses at its inputs. The output is normally, with the converter operating, at 10^V and when triggered on it is grounded, thus cutting off the valve firing pulses. The output is connected to the pin marked 'Pulse Block' of the pulse generating units in fig. 2.9.

4. By-pass valve control circuit.

This circuit has been described in Section 2.8.1, fig. 2.22. The output of the computer signal decoding unit is coupled to the trigger inputs of this circuit.

5. Low voltage current rejection circuit[87]

When the converter terminal voltage falls to a low value, say below 0.2 pu, the current order is decreased to prevent operation at full load current and firing angles of approximatly 90 degrees, a condition of high valve stress. It is desirable that this circuit has sufficient delay to prevent spurious operation for commutation failures or fast transients and has been designed with a lag exceeding one a.c. cycle. A straightforward low voltage relay has been employed on the simulator.

At delay angles near 90^o a converter appears as a reactive load to the a.c. system and the need to limit its effects on the voltages of the neighbouring portions of the a.c. network is an additional reason for using these circuits especially if this system is weak.

6. Isolator controls.

Relays, driven from bistables, are used to represent the low current line isolators[42] of the simulator. The operating times are not significant in comparison to the normal dead time, de-energisation and restart of the system.

6.2. Description of Waveform recording procedure

The waveforms have been recorded on an ultra-violet recorder on direct print paper. Normal photographic development and fixing has been used in preference to development by exposure to an ultra-violet source and spray fixing as a much better image contrast is obtained.

The following table summarises the waveforms recorded and provides some details of the galvanometers employed.

Waveform	Galvo. natural frequency	Remarks
Rectifier RE current	600 c/s	sensitivity (cm/amp) equalised
Inverter IN1 current	600 c/s	
Inverter IN2 current	600 c/s	
Rectifier RE voltage	3 kc/s	sensitivity (cm/volt) approx. equalised
Node point voltage	600 c/s	
Inverter IN1 voltage	700 c/s*	
Inverter IN2 voltage	6 kc/s*	sensitivity less than above 3. Galvo. rating limitations

* These two galvos are sometimes interchanged.

An assortment of galvanometers have been used for the voltage recordings as sufficient high frequency devices capable of reproducing details of converter output voltage waveform were not available. The frequency sensitivity of the 3 kc/s and 6 kc/s galvanometers is adequate, but as the sensitivity of the latter is low, one of the four voltage traces is recorded to a sensitivity of approximately 0.23 times that of the other three. The natural frequency of 700 c/s for the galvanometer recording node voltage and 600 c/s for those recording currents is adequate. The

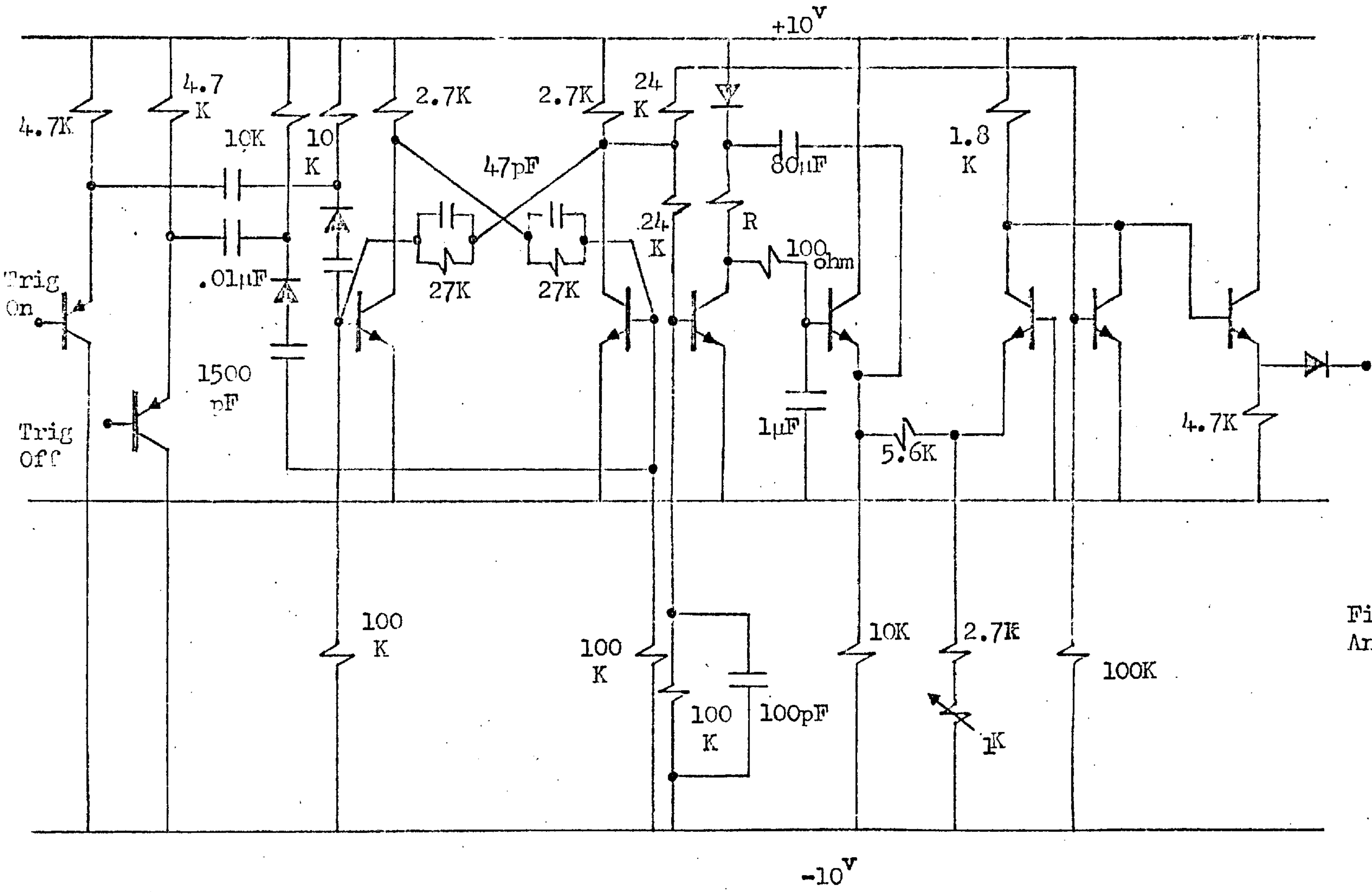


Fig 6.1a Converter De-Energising Circuit.

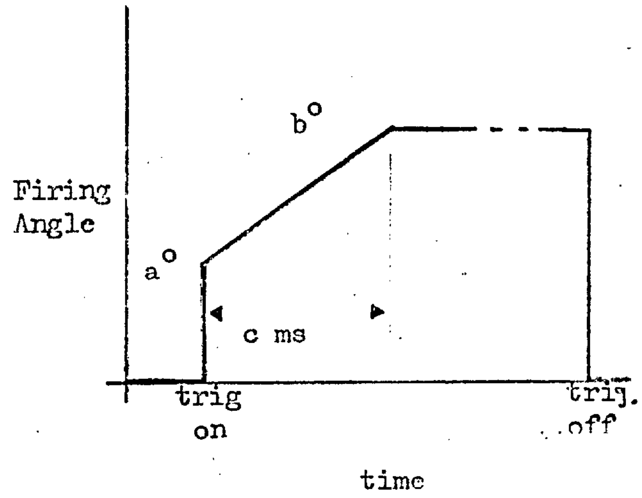


Fig 6.1b Output Waveform.

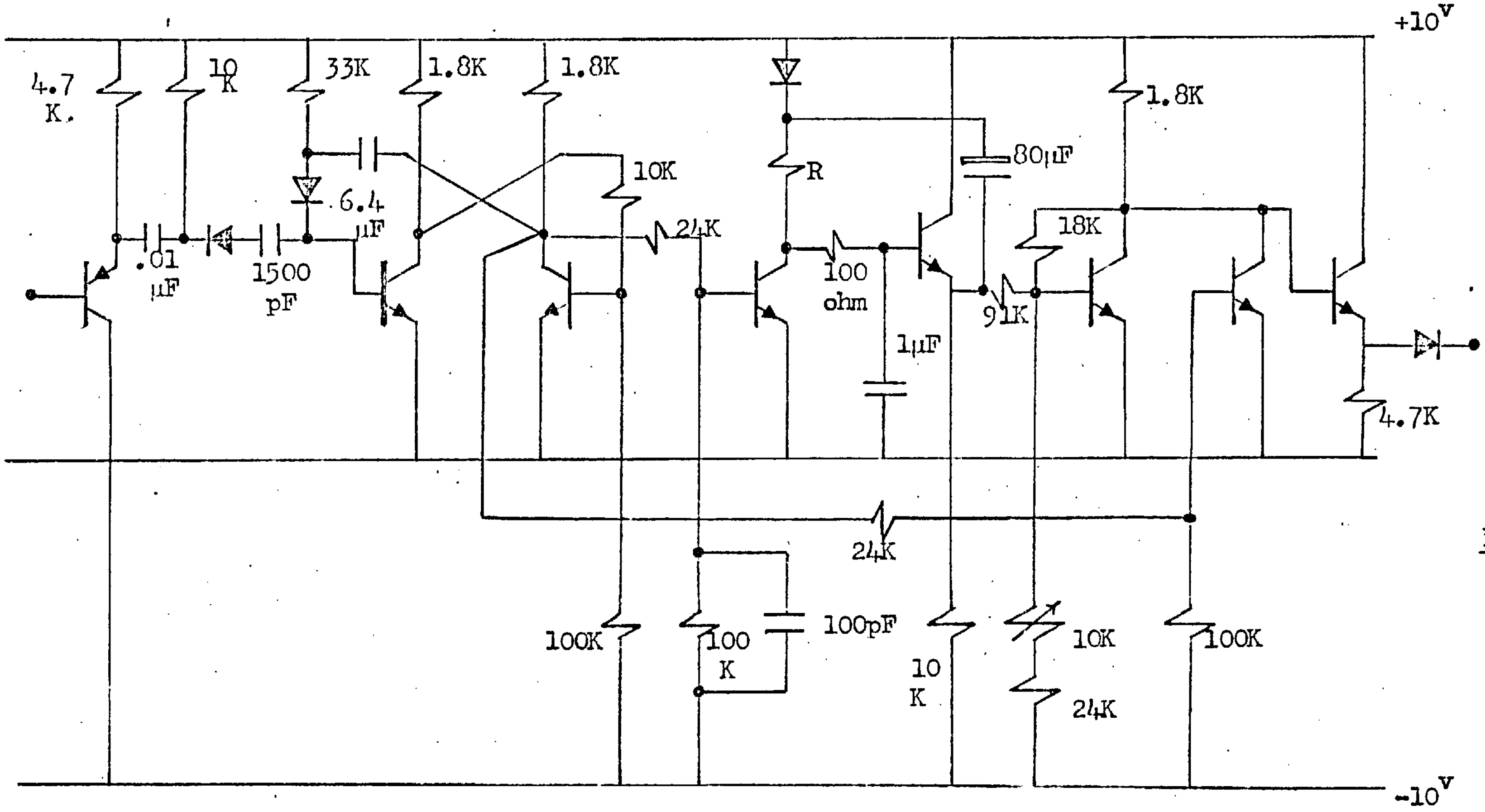


Fig 6.2a Rectfier Starting Circuit.

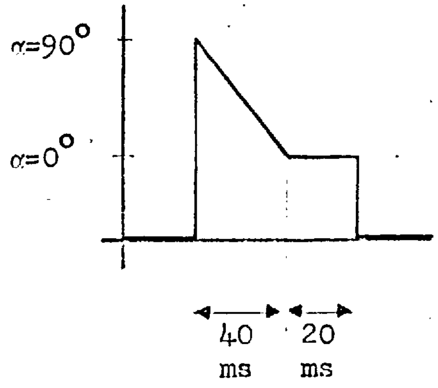


Fig 6.2b Output Waveform.

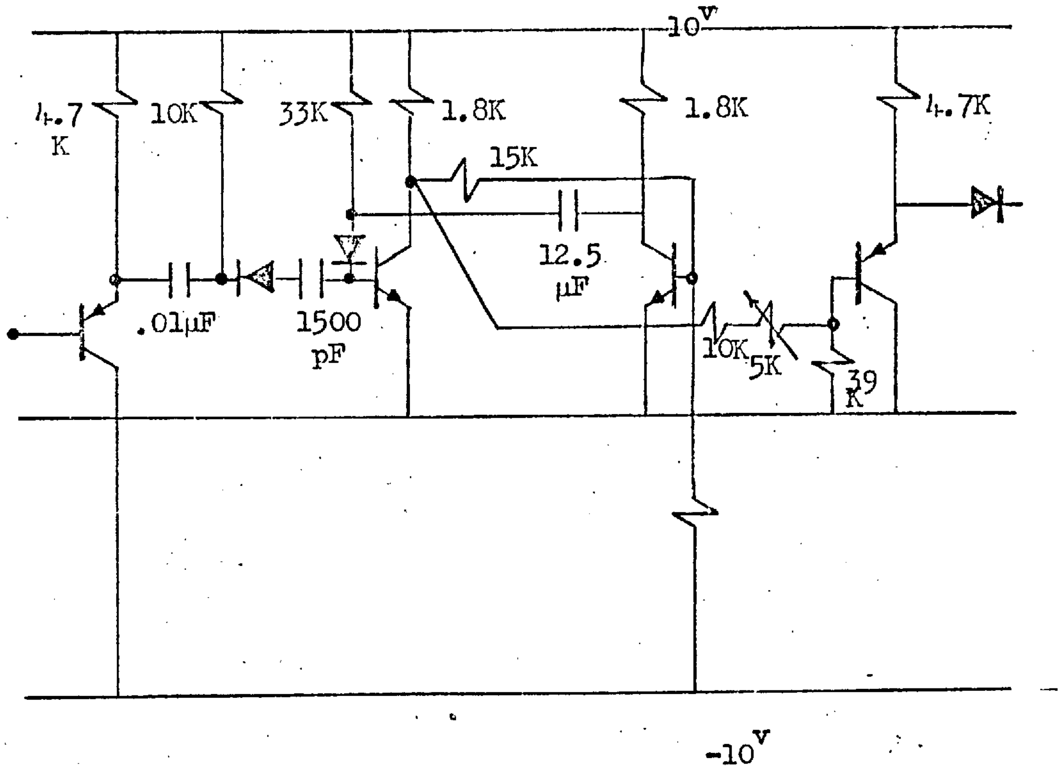


Fig 6.3a Inverter Starting Circuit.

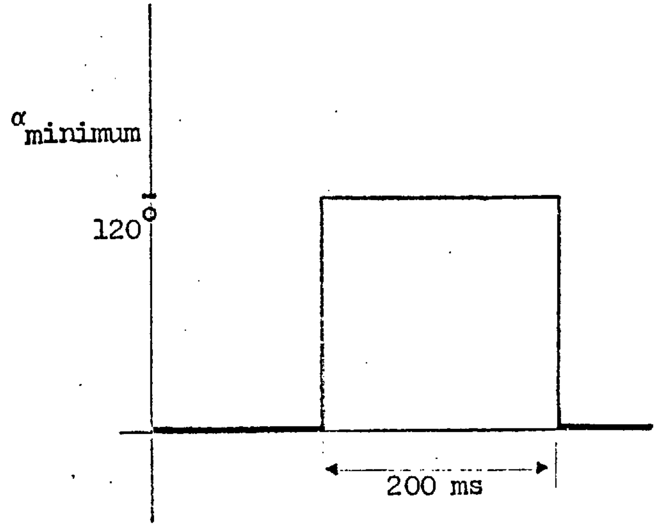


Fig 6.3b Output Waveform.

converter terminal voltage and not the voltage on the line side of the choke has been recorded at each terminal as a great deal more information of converter performance is obtained at this point.

6.3. Transmission System Faults

Numerous tests of faults at various locations in the d.c. transmission circuit and over a wide range of system load conditions have been conducted. The realistic a.c. system connections discussed in Section 4.1.3 have invariably been used but a few tests were conducted with strong a.c. systems connected to all three terminals. In these latter tests, the response of the h.v.d.c. simulator was optimistic and therefore confirms the importance of proper a.c. system representation. The system behaviour at light loads is, as anticipated, better than the performance under full load conditions. The heavily loaded system is more prone to commutation failure, shows greater perturbation and settles down more slowly after faults or other disturbances.

The location of the fault on the d.c. transmission circuit does not have much influence on the extent to which the converters are disturbed before settling into the faulted operating condition, except when the fault is on the station terminals themselves, in which case, the near converter shows more pronounced oscillations of control and a tendency to transient commutation failure. The behaviour of the converters was found to be sensitive to the alignment of the control circuits, since especially careful alignment of the pulse generating units to ensure correct 60° pulse intervals and accurate measurement of the six extinction angles was found to improve transient performance.

Transient Faults

A transient short circuit on the d.c. transmission circuit is cleared by shutting down and re-starting, fig. 6.4. The operating conditions of the system are as follows:-

TABLE 6.1

	D.C.			A.C.
	Current	Voltage	Control	Transformer secondary volts
Rectifier RE	100%	99%	c.c.c.	107%
Inverter IN1	40%	86%	c.c.c.	88%
Inverter IN2	60%	84%	c.e.a. $\gamma = 13^{\circ}$	86.5%
Node	-	88%	-	-

Smoothing Inductors 0.55 H/terminal

Location of fault : Transmission system node

The a.c. system representation of section 4.1.3. is used.

In this and the following tables all percentage values refer to rectifier rated values as base. The base a.c. voltage is that voltage at the transformer secondary terminals to give 100% d.c. voltage on open circuit for a firing angle of 0°.

Fig. 6.4 shows that immediately after fault application, oscillations of control occur, attempting to sustain ordered current in the converters. This causes transient excursion of the inverters into the region of rectification before the system settles down. These oscillations completely disappear in about 60 m sec. The rectifier and inverter IN2 current are examples of the ability of the constant current controllers to intervene quickly and sustain ordered current. Inverter IN1 current however shows a larger current overshoot arising from a double commutation failure and consequent transient loss of control.

The time interval between the occurence of the fault and the start of system de-energisation is, in the main, determined by the delays in protective equipment and telecommunication channels - the processing time of the computer being small - and therefore an arbitrary value of 120 ms has been used to represent this in this recording. The time from the commence-

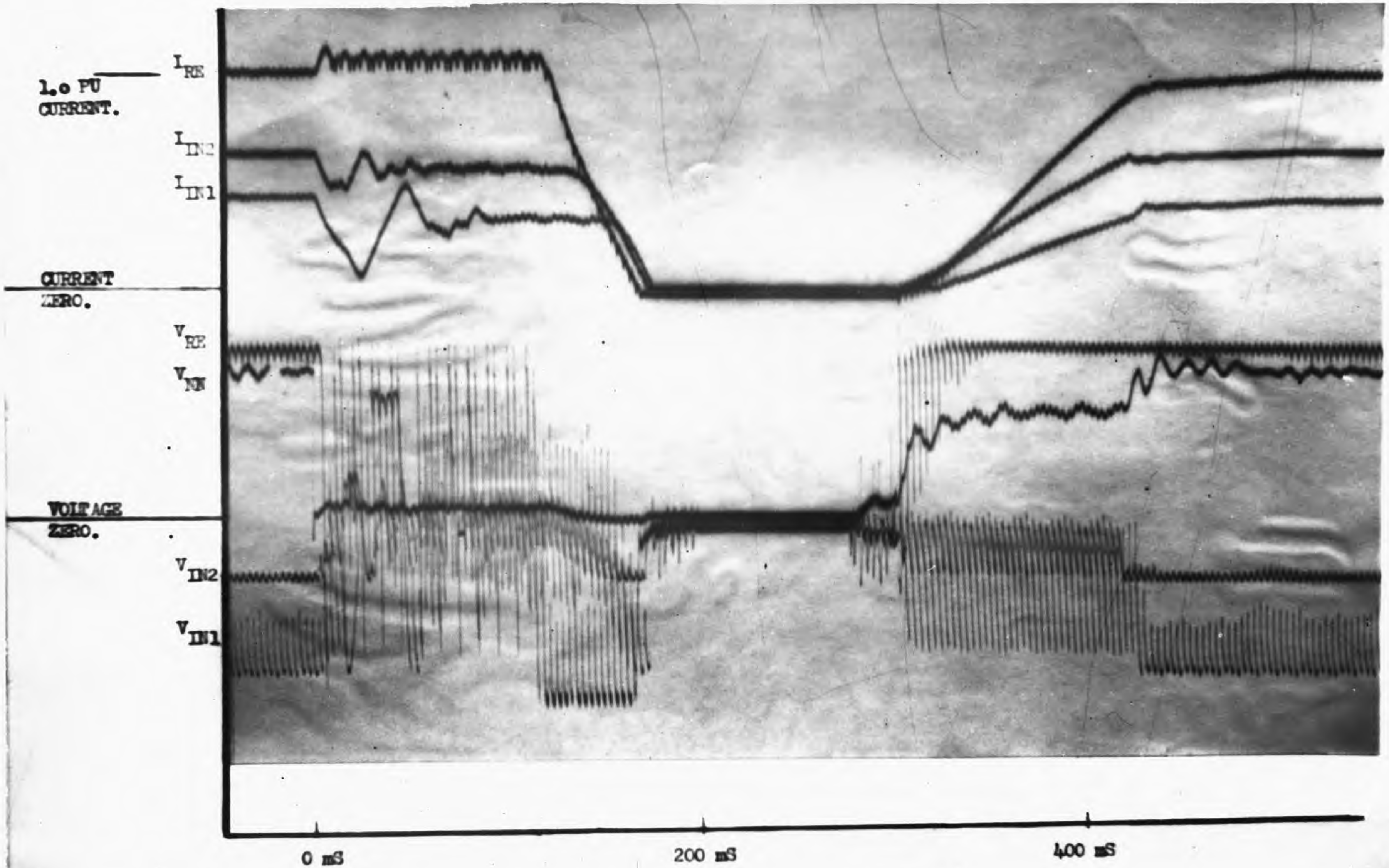


FIG 6.4 CLEARING A TRANSIENT FAULT NEAR SYSTEM NODE.

ment of de-energisation to current extinction depends on the size of the smoothing reactor and the initial currents. At the rectifier, when pushed to inversion at a delay angle of 155°, this de-energisation time is 55 m sec for 1.0 p.u. current, as in fig. 6.4. The system dead time before restart must be sufficient to ensure de-ionisation of the d.c. arc path and a reasonable value of 130 ms is allowed in this test, during which time the fault relay is opened.

The following points should be noted with regard to the restart period. The controlled build up of rectifier forward voltage limits overshoot of line voltage, the largest overshoot of node voltage does not exceed 5% over the entire restart period. Both inverters are prevented from reducing their firing angles below 120° during the re-start period to prevent power flow reversal at these terminals. When inverter current exceeds the constant current controller setting this controller intervenes, taking over control from the restart circuits and increasing the firing angle to full inversion. The inverters return to their normal controlled operation some 125 m sec after the rectifier is deblocked but a further 90 m sec is required for the rectifier to build up the additional margin current.

The overall time from the instant of fault to restitution of completely normal operation is approximately 0.5 sec.

Fig. 6.5. shows in detail the initial part of the fault control. A test carried out under entirely different conditions from that recorded in fig. 6.4 has been chosen to illustrate a number of additional features.

The a.c. systems connected to the three terminals are now very strong, having short circuit ratios in excess of 15, and the time between fault and the beginning of shut down has been reduced to 80 m sec to limit the record length. The detail figure shows the inability of the galvanometer, natural frequency 700 c/s, recording IN1 voltage wave shape to adequately follow the converter ripple.

The system operating conditions are given below:-

TABLE 6.2

	D.C.			A.C.
	Current	Voltage	Control	Transformer secondary voltage
Rectifier RE	102%	103%	c.c.c.	110%
Inverter IN1	61%	88%	c.c.c.	91%
Inverter IN2	41%	89%	c.e.a. $\gamma = 16^{\circ}$	91%
Node	-	92%	-	-

smoothing inductance 0.55 H per terminal

Fault location : On rectifier line at a distance of 0.4 x line length from the node.

The transient rectification of the inverters to sustain ordered current and the ensuing oscillations arising from current overshoot leading to steady working offer some 60 m sec are all features that can now be seen in detail. The disturbance to the converters is smaller than that encountered with the weakened a.c. systems at the terminal.

In this test the de-energising circuits at all three terminals have been triggered simultaneously whereas in the previous test, fig. 6.4, the beginning of de-energisation at the three terminals was staggered to obtain a near simultaneous current extinction in the system. Clearly, the former procedure, that is fig. 6.5, is not desirable as large currents flow into the fault path during the latter part of the de-energisation period.

The node voltage does not collapse immediately but decays to zero in 1.5 a.c. cycles in the form of damped sinusoidal oscillations at the relatively high frequency of 450 c/s.

Permanent Faults.

The control of the system during a permanent fault on the line between node and inverter IN1 is shown in fig. 6.6. The

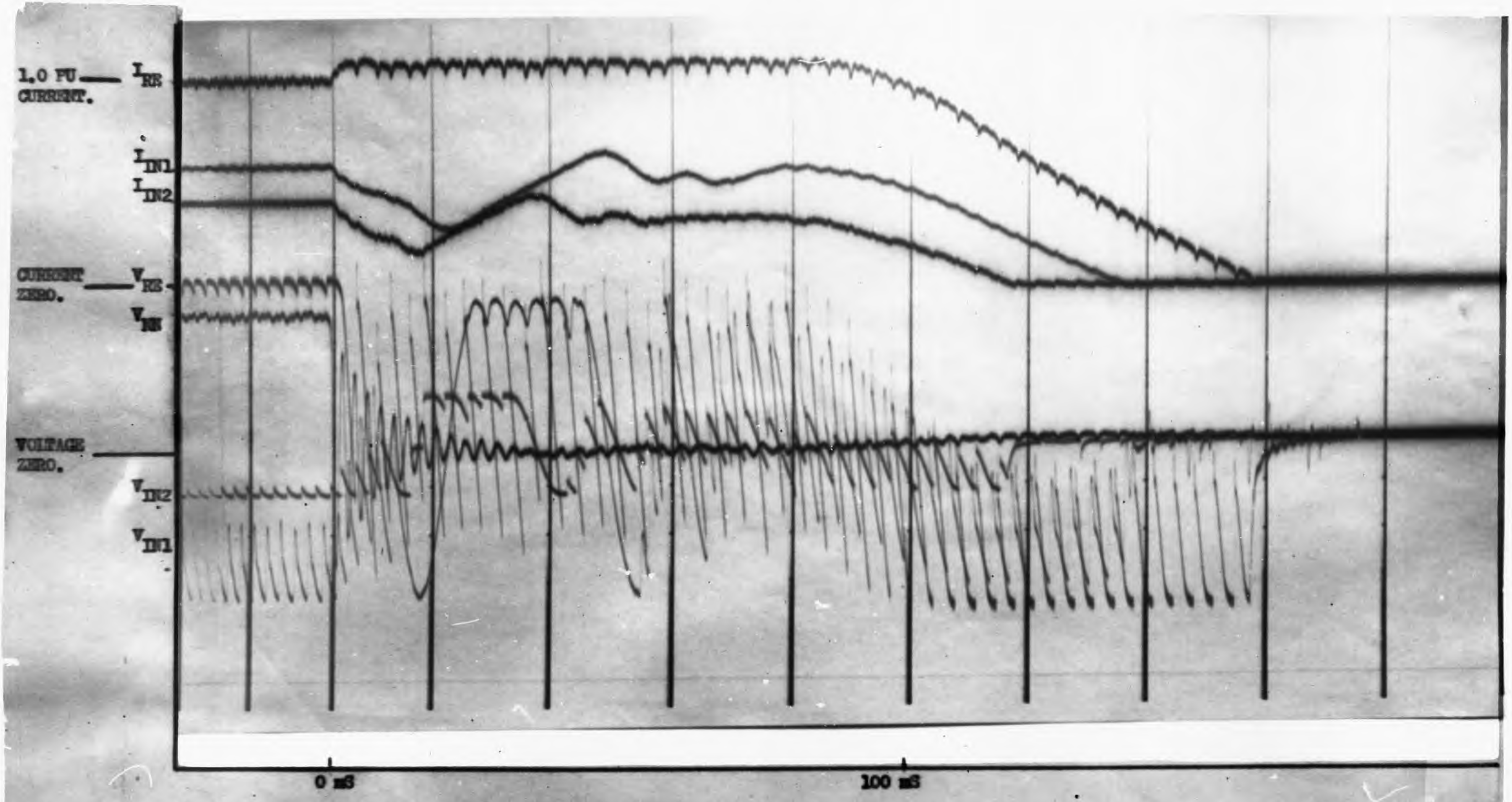


FIG 6.5 DETAIL OF FAULT AND SYSTEM DE-ENERGISATION.

system is de-energised, a single unsuccessful re-start attempted, thereafter the faulted line is locked out and the healthy portion re-started.

Pre-fault and post-fault operating conditions are summarised below:-

TABLE 6.3.

	D.C. pre-fault			D.C. post-fault		
	Current	voltage	control	current	voltage	control
Rectifier RE	100%	99%	c.c.c.	66%	97%	c.c.c.
Inverter IN1	40%	86%	c.c.c.	-	-	-
Inverter IN2	60%	84%	c.e.a. $\gamma = 18^{\circ}$	66%	84%	c.e.a. $\gamma = 18^{\circ}$
Node	-	88%	-	-	90%	

Smoothing inductance : 0.55 H./terminal
Fault location : Midpoint of line between node and IN1
The a.c. system representation of section 4.1.3. was used.

The system is re-started with the rectifier current order reduced to supply one inverter only, but 100% rectifier current may be supplied to this inverter should this be desirable.

The other feature of this test that requires comment is the attempted unsuccessful re-start. When inverters are deblocked on to a faulted line they neither inject current nor build up voltage since the firing angle is held greater than 90° by the re-start circuits. Subsequently, when the rectifier is deblocked, the current, limited by circuit impedance only, rises rapidly. Rate of rise of current detectors will detect the deblocking of the converter on a faulted line immediately; in the laboratory fault information is artificially set up at the computer input. De-energising circuits are turned on a second time to drain energy from the system.

Fault and de-energisation of a system when the constant current controllers are provided with low voltage current rejection circuits is illustrated in fig. 6.7. The operating conditions of the system are tabulated below:-

TABLE 6.4

	D.C.			A.C.
	Current	Voltage	Control	Transformer secondary volts
Rectifier RE	104%	100%	c.c.c.	108%
Inverter IN1	38%	87%	c.c.c.	89%
Inverter IN2	66%	85%	c.e.a. $\gamma = 14^{\circ}$	87%
Node	-	89%	-	-

Smoothing inductance 0.55H/ terminal
Fault location : D.C. transmission circuit node
The a.c. system representation of section 4.1.3. was used.

Approximately 30 m sec after the fault the current orders at the three converter stations are decreased to a low value as operation at firing angles near 90° and large currents presents valve stress problems. The current order is reduced rapidly, the circuit time constant being 6.5 m sec, and this accounts for the more pronounced transient oscillations of control; these can however be entirely eliminated by increasing this time constant to about 50 m sec.

The complete de-energisation of the system is carried out only in response to instructions from the central control computer. The de-energisation time is considerably reduced as the system is now working at reduced current, and in the case shown, where the rectifier current is reduced to 27%, extinction time is about 20 m sec.

Certain objections exist to the inclusion of this controller

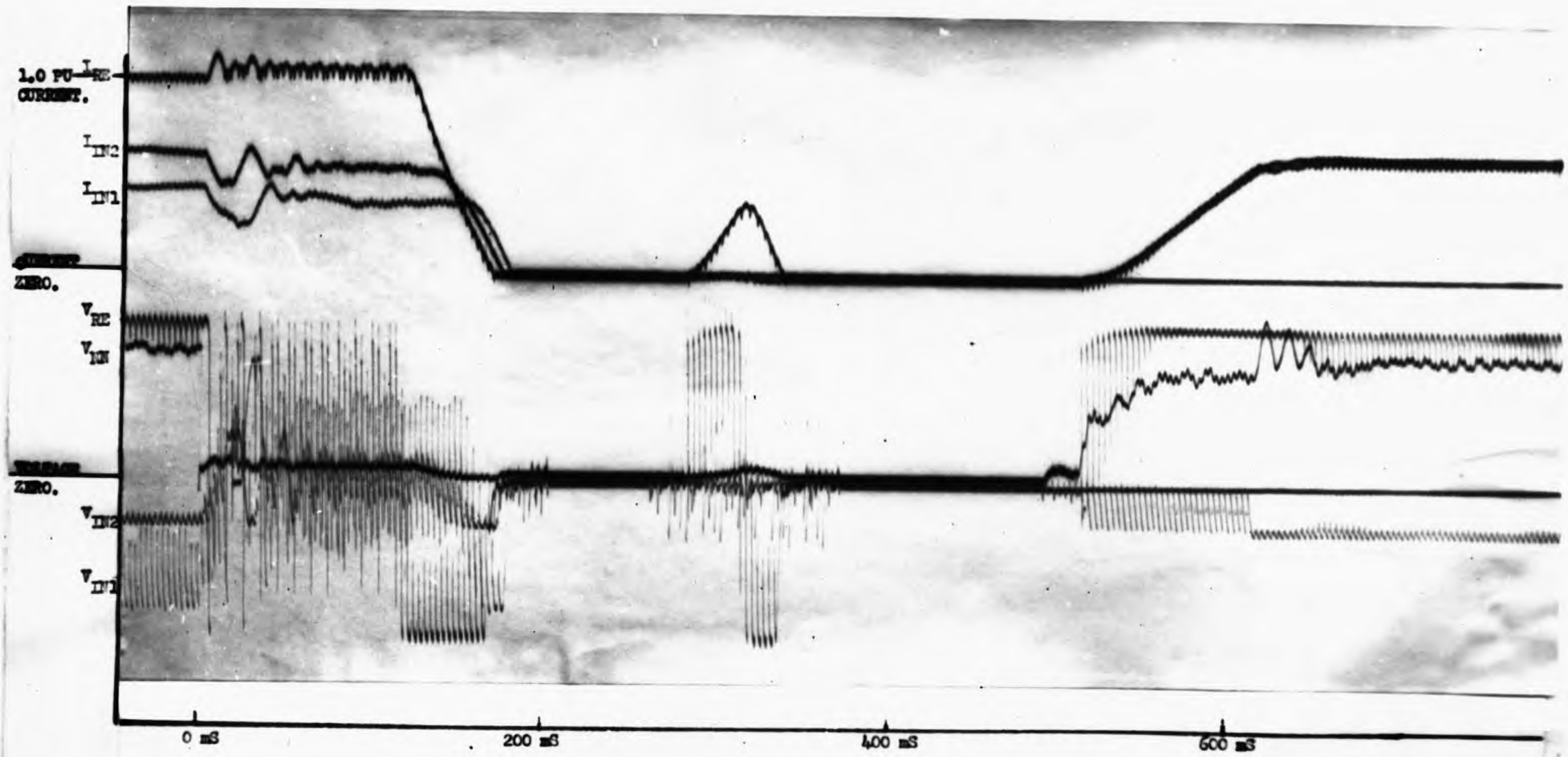


FIG 6.6 CLEARING A PERMANENT FAULT ON AN INVERTER LINE.

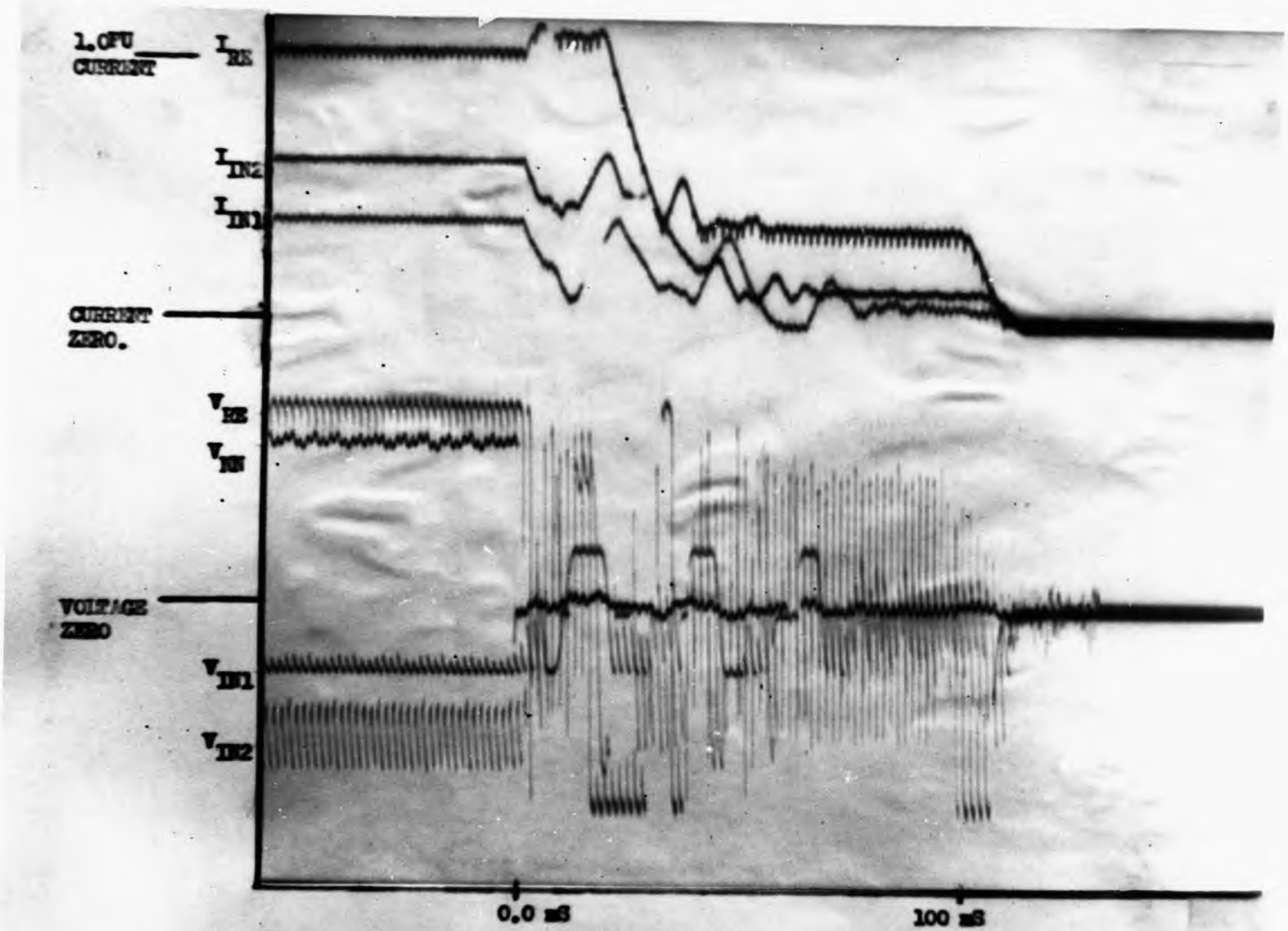


FIG 6.7 FAULT AND DE-ENERGISE WHEN CIRCUITS CAUSING CURRENT INJECTION AT LOW VOLTAGES ARE USED.

in converter systems having one bridge per pole per terminal. Repetitive commutation failure is usually cleared by by-passing the bridge for a short time and then deblocking. When these controls are included this would lead to current rejection in the relevant pole and it would be some time after deblocking before normal current, and therefore power transmission, is built up again. Co-relation with fig. 6.4, 6.8, 6.9, indicates that if current rejection to nearly zero is used, the time between de-blocking and steady normal operation would require over 200 m sec as against 25 to 50 m sec when these controls are not included. Commutation faults in valves are encountered far more frequently than transmission system faults in h.v.d.c. systems.

6.4. Converter Faults

The control of the h.v.d.c. system during bridge failures is presented in two parts, faults that are cleared by local control circuits at the converter and faults that require the intervention of the central control computer.

Converter Faults cleared by Local Control

The two following tests relate to the discussion of section 5.4.1.

Fig 6.8: Repetitive rectifier commutation failure cleared by a block bypass, deblock sequence at the rectifier.

Fig. 6.9: Repetitive inverter commutation failure cleared by a block-bypass, deblock-recover sequence at the inverter. The fault is applied on the inverter IN2 which is connected to the weakened a.c. system, section 4.1.3.

The operating conditions of the system was the same as that tabulated for Table 6.1, except that in fig 6.9 the currents in IN1 and IN2 are 45% and 55% respectively.

In these two tests the central control programme plays no positive part, its role being to identify the disturbance as one that does not require system de-energisation. The

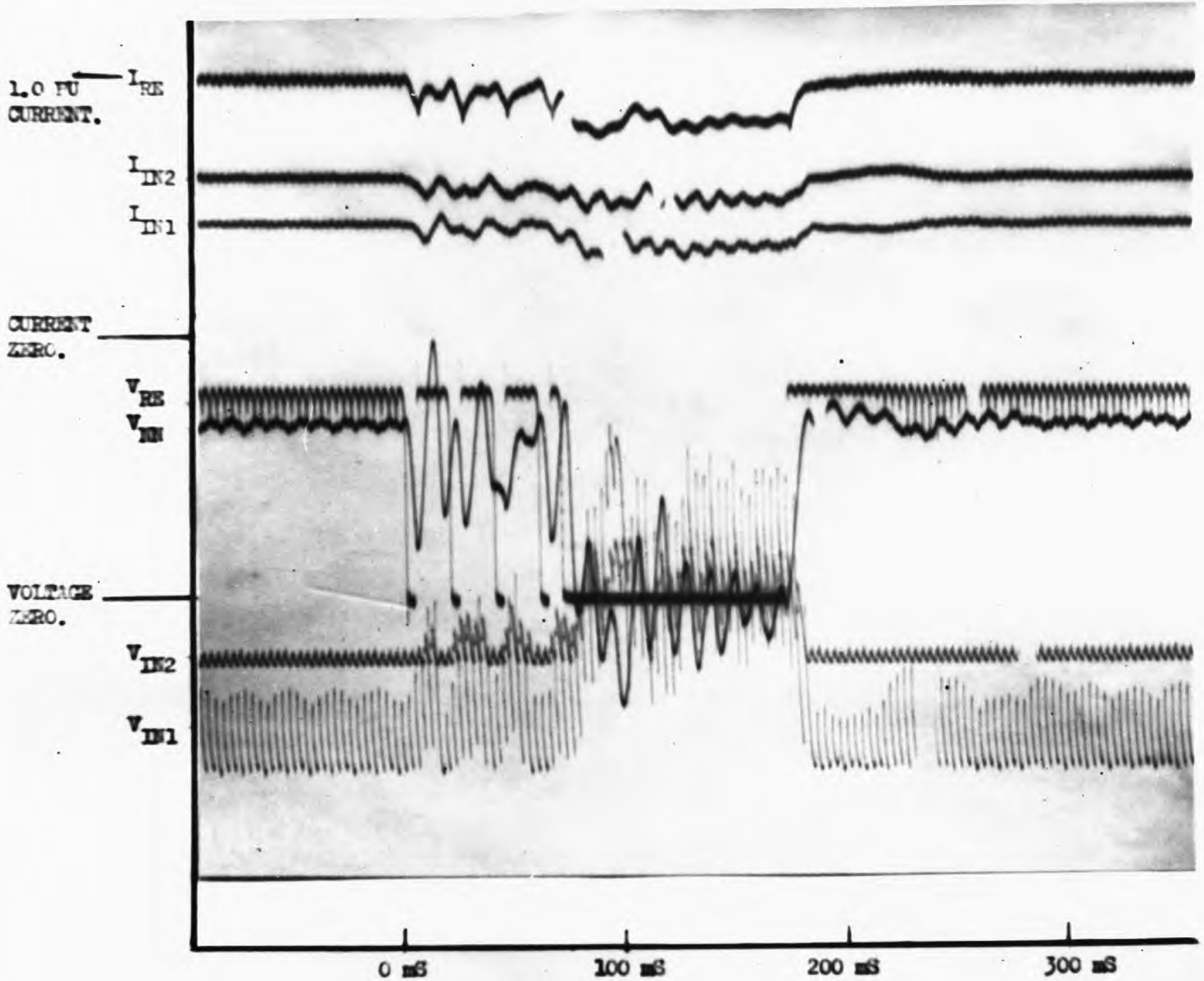


FIG 6.8 RECTIFIER REPETITIVE COMMUTATION FAILURE CLEARED BY LOCAL CONTROL.

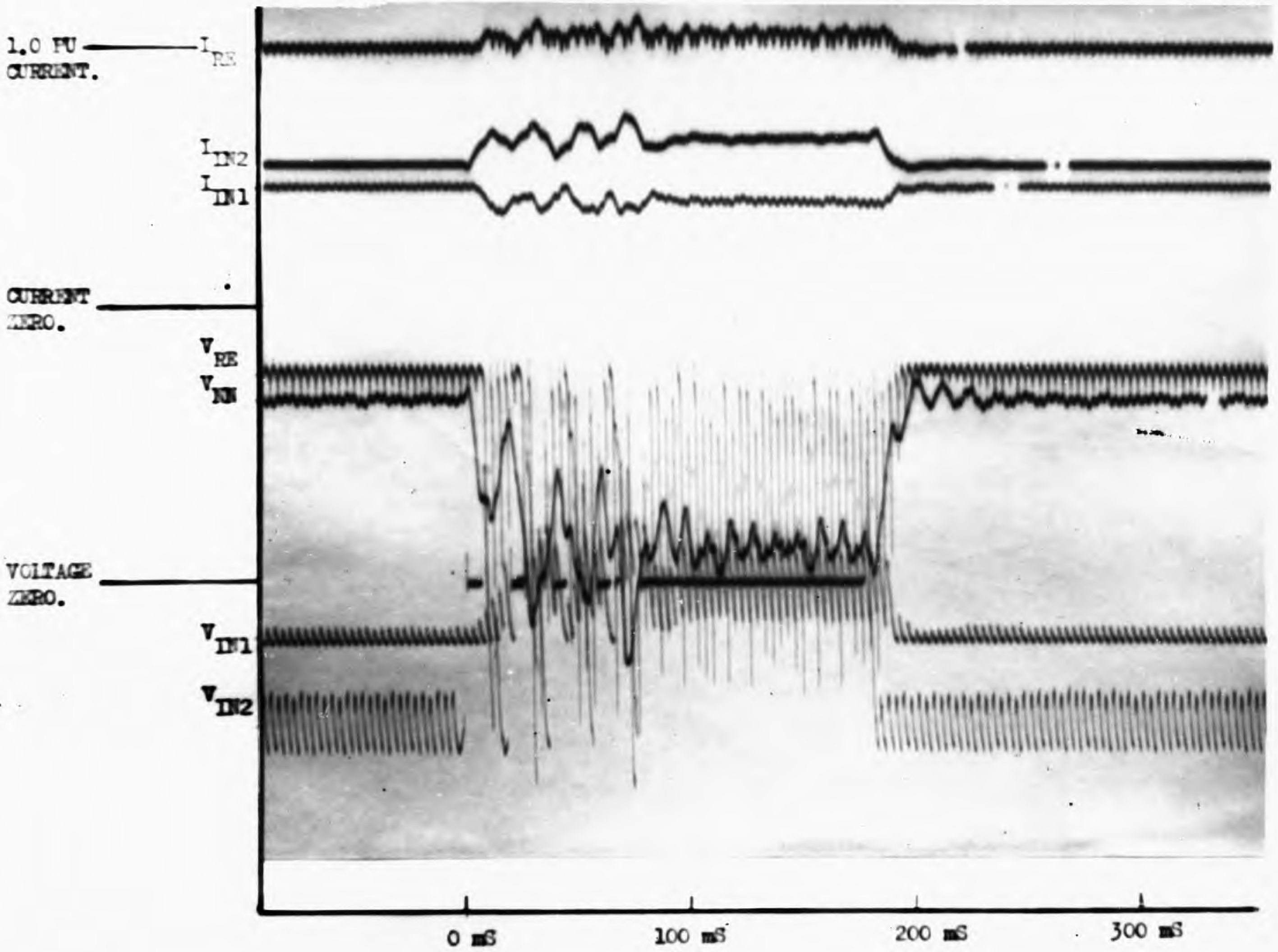


FIG 6.9 INVERTER REPETETIVE COMMUTATION FAILURE CLEARED BY LOCAL CONTROL.

system resumes normal operation when the converter is deblocked with the fault cleared, the initial transient associated with the restart disappears in less than 50 ms and in any event it is hardly perceptible in these recordings after the first 20 msec. The inverter recovery unit, described in section 2.8.2. and fig. 2.23, is used to obtain current pick up in the inverter in the first firing period after deblocking. The period for which the faulty converter needs to be bypassed depends on mercury arc valve recovery characteristics, a value of 100 m sec being used in these tests.

Converter Faults cleared by Central Control

Fig. 6 10 shows a test, related to the discussion of section 5.4.3 where subsequent to the failure of two valves in series on the same arm of an inverter bridge the system was rapidly run down by the central control. Either a local control failure or the inability of the values to de-ionise is hypothesised but this aspect is not relevant here. The fault was removed before restarting the system.

A failure of two valves in series was induced prior to the commencement of the recording and a d.c. short circuit results. Firing the bypass valve causes a sharing of the d.c. current between these two parallel paths but fails to ensure current extinction in the bridge valves. This test may also be considered as describing the protection sequence required subsequent to the following converter faults.

1. Failure of bypass valve hold off properties.
2. Failure of an inverter to pick up current in a block-bypass-deblock operation; e.g. due to recovery unit failure.

The automatic removal of an inverter from a live system under central control supervision, discussed in section 5.4.4, is illustrated in fig. 6.11 and 6.2.

The conventional method[44] of disconnecting an inverter from an h.v.d.c. system is to run the system down transiently, or in the case of a faulty inverter, to bypass before de-energisation. For a period transmission is interrupted over the whole d.c. network or on one pole The disconnection of an inverter may be necessary for a number of reasons, for example, for maintenance work on the converter equipment or some essential component of the a.c. system, or where one of a number of bridges in series has failed and has been bypassed and disconnection of this terminal is preferred to operating all the converters in the system at reduced voltage, or to effect the isolation of a faulty converter, or to reverse the direction of power flow at the inverter only.

It was suggested in section 5.4.4 that in a centrally controlled multiterminal system rapid disconnection of an inverter without the need to bypass which interrupts transmission elsewhere, may be achieved in three stages, as follows:-

1. Ensure that the inverter to be disconnected is on c.e.a. control, that is, that all other converters are on constant current control. This will certainly occur automatically in the second and third examples suggested above, in general tap changers have to be operated.

2. Bring the current order of the inverter to zero and then alter the current orders of the other converters in a co-ordinated manner to bring down the current in this inverter to margin value. The rate at which this change may be implemented depends on the permissible transient disturbance to the system. The quickest method is to make current order step changes but this is also the most severe. (see fig. 3. 19).

3. When the current into the inverter has fallen to a low value (equal to the system current margin) a low current isolator is opened. Another converter will then take on the function of voltage control and the system continues to operate normally.

The operating conditions of the system are as follows:-

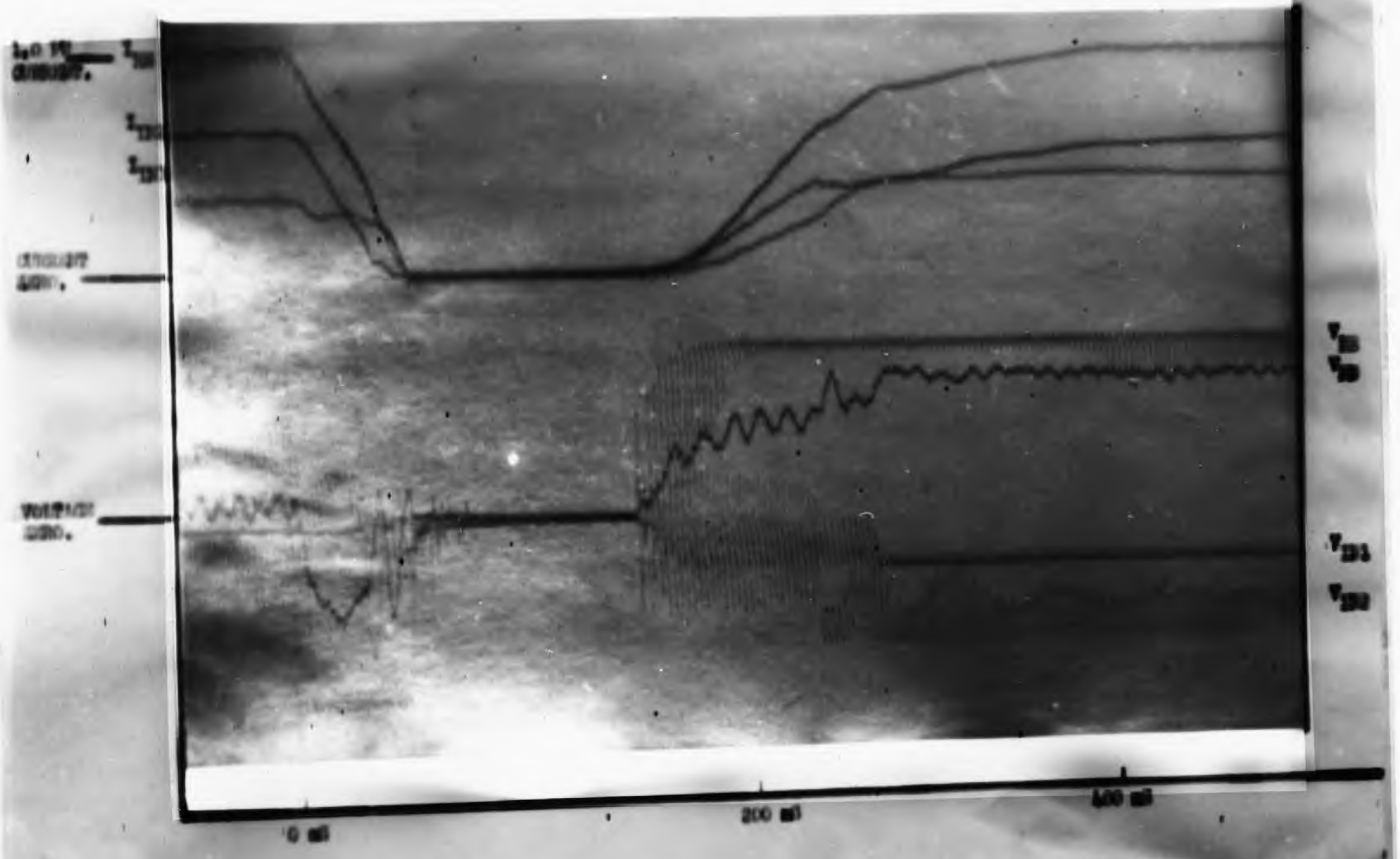


FIG 6.10 CLEARING OF A BRIDGE VALVE FAILURE AT AN INVERTER BY CENTRAL CONTROL.

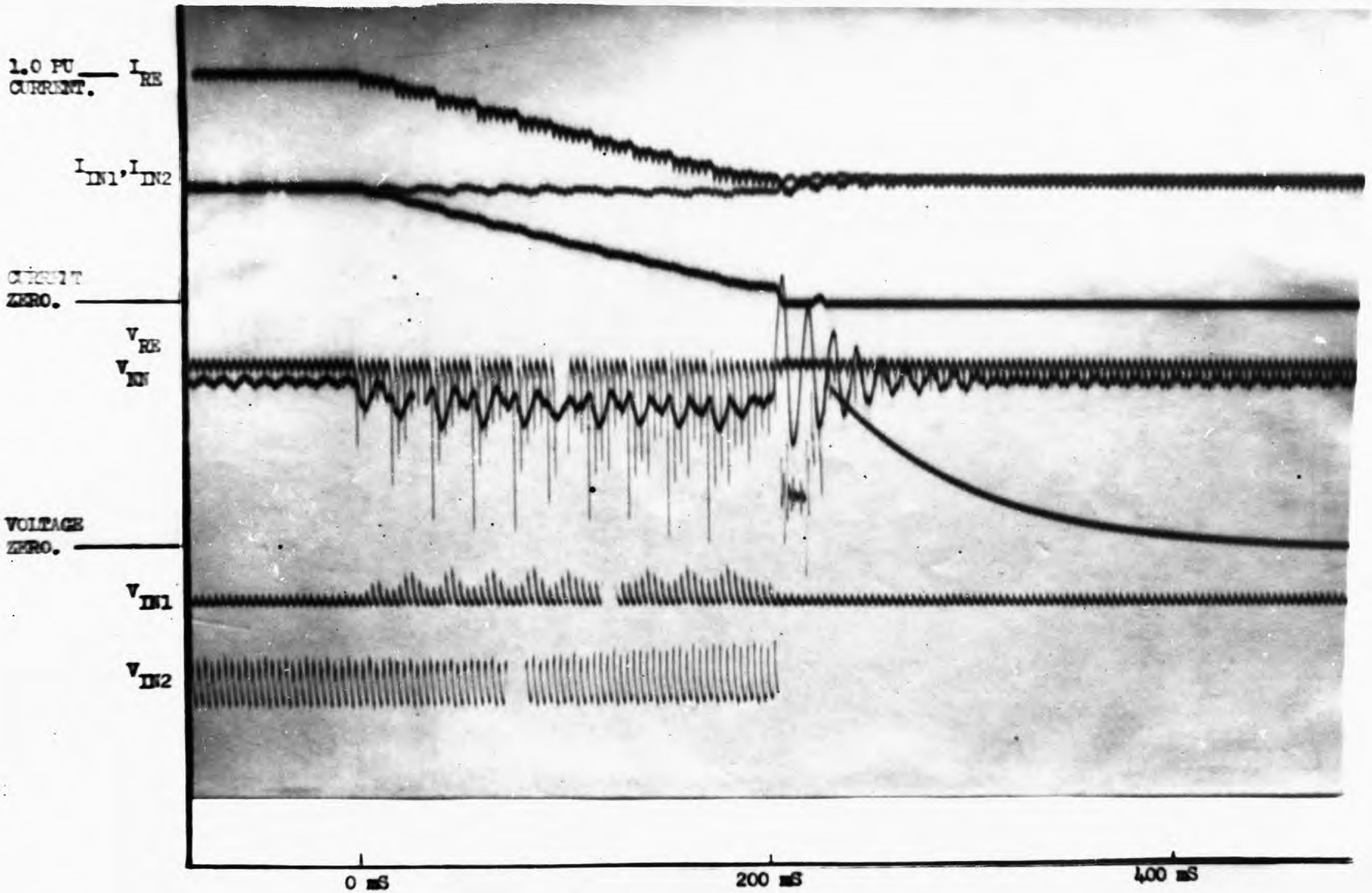


FIG 6.11 AUTOMATIC REMOVAL OF AN INVERTER BY THE CENTRAL CONTROL COMPUTER.

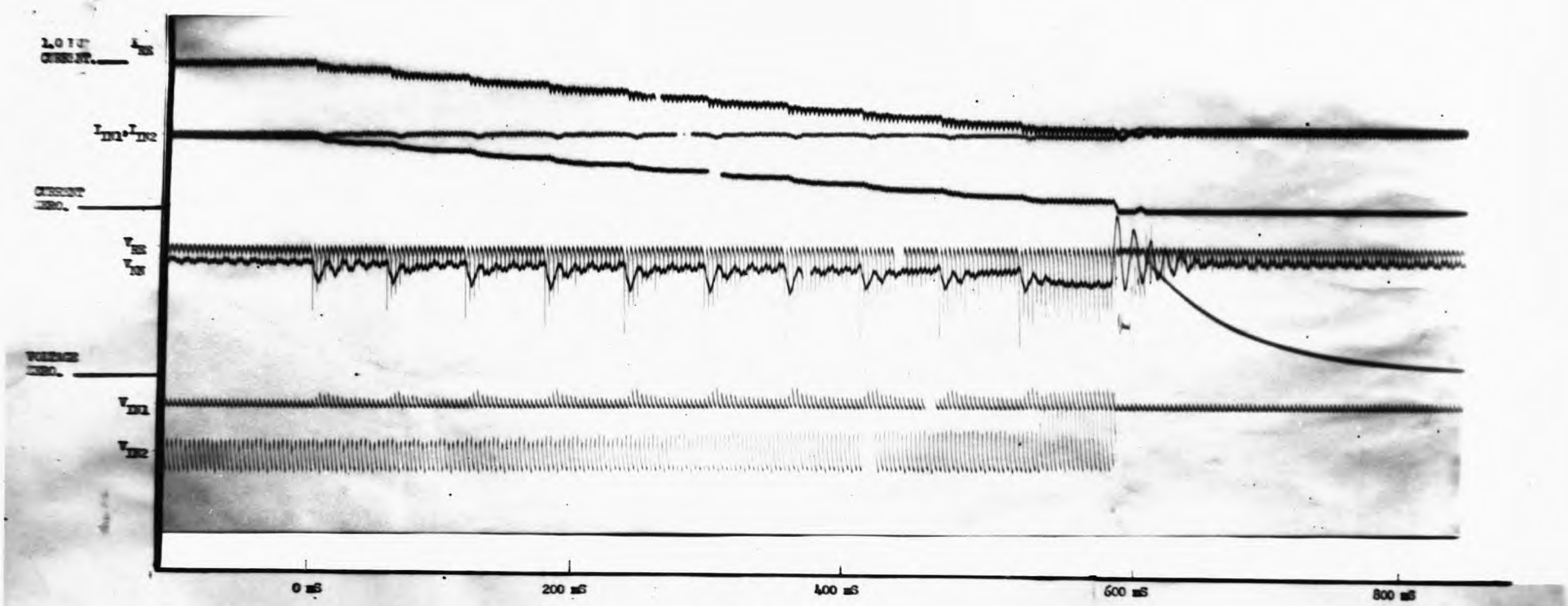


FIG 6.12 AUTOMATIC REMOVAL OF AN INVERTER BY THE CENTRAL CONTROL COMPUTER.

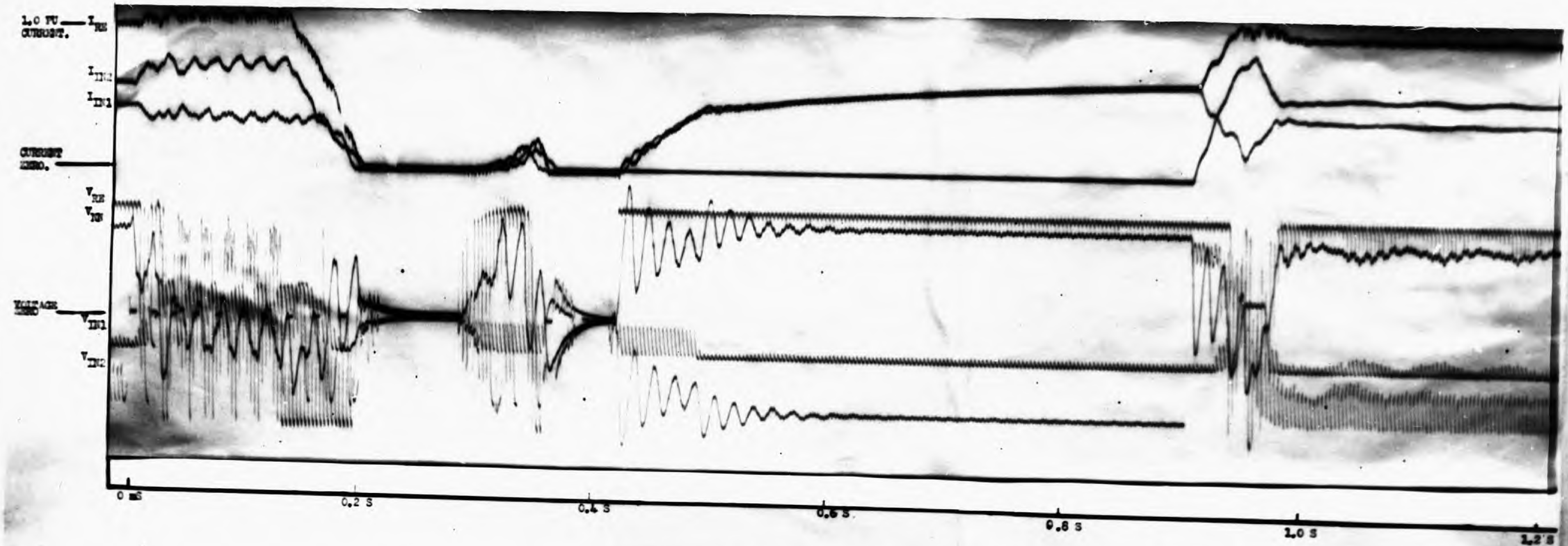


FIG 6.13 ISOLATION OF A FAULTY INVERTER BY THE CENTRAL CONTROL. SUDDEN RECONNECTION SUBSEQUENTLY.

TABLE 6.5

	Initial			Final		
	Current	Voltage	Control	Current	Voltage	Control
Rectifier RE	100%	99%	c.c.c.	54%	96%	c.c.c.
Inverter IN1	50%	85%	c.c.c.	54%	86%	c.e.a. $\gamma = 16^{\circ}$
Inverter IN2	50%	85%	c.e.a. $\gamma = 16^{\circ}$	-	-	-
Node NN	-	88%	-	-	89%	-

The a.c. system representation of section 4.1.3. was used.
Smoothing inductance = 0.55 H/terminal.

The rectifier current order is reduced in ten equal steps over a total time of 200 m sec in the case of fig. 6.11 and 600 m sec in fig 6.12. The former represents the fastest possible without instantaneous voltage reversal at the rectifier.

Fig. 6.13: Shut down of a faulty inverter by central control.

If for any reason it is not desirable or not possible to block-bypass a faulty inverter station locally the system must be rapidly de-energised by central control. In the test shown the fault was of a permanent nature and commutation failure persists when a restart was attempted. The system was de-energised for a second time and the healthy converters only restarted. The isolators on the line to the faulty inverter are not opened at either the node or the terminal, the inverter only being blocked. In practice this should permit a quick restart.

The rectifier starter has not been operated during restart when the rectifier was deblocked. This has been done for purposes of comparison with the normal re-start procedure, see previous figures, 6.4 and 6.6. The switching transient shows the over-voltage at the node to be of the order of 40% to 50%

as against the small value of 5% when the rectifier starter is used.

The initial operating conditions are approximately the same as for fig. 6.4, section 6.3. The system is re-started with the two terminal system current order arbitrarily reset to 75% of rectifier rated value. Any value consistent with converter ratings and optimum a.c. system performance could be substituted.

The final section of fig. 6.13 shows an additional switching action; the current orders were suddenly modified to their original values and the inverter IN2 deblocked. The system returns to its original operating state after a transient of duration 75 m sec to 100 m sec that includes a period of reversed power flow at all the converters. This is presented here as a pointer to future extensions of the control studies discussed up to now. The sudden switching in and out of converters, and the opening of live line sections as a circuit breaker would, have been tentatively simulated. Here is scope for an extensive study with a view to obtaining results of practical value in the development of ultra-fast control and protection.

CHAPTER 7

Conclusions

The first part of this thesis describes the construction of an h.v.d.c. simulator, equipped with fast reliable controls, that can be used for the investigation of h.v.d.c. system operation with some measure of confidence. The model was however, more than a simulation of known h.v.d.c. techniques as the investigation and installation of an entirely new method of constant extinction angle control has also been undertaken. These controls have been successfully incorporated into a three bridge system and the test results of Chapter 3 are evidence of excellent operational characteristics achieved after some problems of instability and oscillation, not previously anticipated, had been overcome. This method of c.e.a. control is of great interest in view of the fact that at least two major manufacturers of h.v.d.c. equipment are developing it for use in future installations. This report however is the first complete description, including circuit details and performance characteristics, of the new method of c.e.a. control.

Reliable thyristor pulse generating units responding rapidly and accurately to the new controls are an indispensable component of the control structure. The new pulsing units that have been incorporated in the simulator have been good enough for all the tests conducted. Constant current control, by-pass valve control, an inverter recovery unit and a circuit incorporating α-minimum and β-minimum stops together with the function of selecting the control loop have also been included and a three terminal system satisfactorily operated with realistic a.c. systems and d.c. transmission networks. However the simulator suffers from two defects, firstly the inflexibility imposed by the use of only one bridge per station and secondly the absence of a.c. side filters and therefore the inability to model very weak a.c. systems. The additional construction work of installing controls on three more bridges and building a.c. filter banks could not be undertaken.

The construction and proving trials on the simulator were followed, as recorded in the second part of the thesis, by an investigation of some aspects of the control of an h.v.d.c. system under fault conditions. The study has, in the main, been confined to d.c. transmission system faults and converter faults. A few tests have, however, been conducted to demonstrate the ability of the h.v.d.c. system to recover automatically from severe a.c. system faults. However this resiliance refers to the system aspect alone; other limitations arising from the properties of the mercury arc valve not being represented in a simulator of this type.

The purpose of the control programme discussed in Chapter 5, and to some extent the justification for the use of a digital computer as a central control, is to obtain high fault discrimination and therefore de-energise the smallest and restart the largest feasible portion of the system. The full versatility of the control programme in this respect cannot be appreciated from three bridge system tests. Normal system operation, that is power and VAr control, optimisation and possibly a.c. system sensitive controls, must however be the economic justification for the inclusion of a control computer in the first place. The concept of emergency control proposed here consists of a digital computer programmed to receive logic fault information from system detectors and converter monitors, ensuring high speed and discrimination in protection, associated with straightforward analogue control circuits at the terminals functioning as slaves, in the hierarchical sense, of the centre. As converter faults can often be cleared by blocking and deblocking locally, provision is made for this. The emergency local control functions by superimposing emergency fault control signals on the thyristor firing circuits, that is, interference with the settings of normal control equipment are avoided.

The results of fault control tests conducted on the simulator and controlled by the PDP.8 computer are presented in a series of waveform recordings in Chapter 6. Control is lost, that is control oscillates or commutation fails, only for a short period usually not exceeding two a.c cycles, and the convertors can be de-energised, shut down or re-started in a fully controlled fashion. The principle time delays are the allowances made for telecommunication and minimum fault path de-ionisation time. It is argued that these tests show that the division of functions as between central and local control and also between emergency converter control and normal converter control provides a satisfactory basis for the protection of h.v.d.c. systems. No doubt a practical central control programme will be more thorough, less fragmentary, carry numerous refinements pertaining to correlation with associated normal system control programmes and interfacing with communication receiving and transmitting equipment and include fail safe and back-up protective facilities. Programmes of the type developed here, therefore, form the necessary and basic skeleton only. The investigation of the automatic/computer control of an h.v.d.c. system is a new field and few publications of note have appeared as yet. The contents of Chapters 5 and 6 are the first systematic treatment of the fault control of a multiterminal h.v.d.c. system.

Suggestions for future work

The h.v.d.c. simulator provides a means for the investigation of almost every system aspect of d.c. transmission. The two most immediate fields of interest are the investigation of a wide range of control techniques and the study of the interaction, on each other, of different a.c. and d.c. systems and inter-connections. The former must aim on the one hand at deriving additional modes of control that are practically useful and on the other at obtaining criteria for the stability and interaction of the various controls of a multiterminal system. The importance of the characteristics of the a.c. system on h.v.d.c. converter operation is now well appreciated. The simulator provides perhaps the most reliable method for the investigation of such problems as operation under conditions of a.c. system imbalance, con nection to weak a.c. systems of both cable and o.h. line networks, the connection of a converter to isolated generation and the connection of a converter at the end of a long a.c. transmission line.

More specifically, with regard to the simulator at Imperial College, the following extensions are urged. The installation of a.c. side filters, whose components have already been designed and purchased, and the further weakening of the a.c. system at one of the inverters, the construction of constant power control circuits at a rectifier and an inverter and, if connection of a micro-machine to the simulator is undertaken, frequency sensitive controls need to be investigated. It is considered desirable to develop for the simulator actual analogue models of analogue type h.v.d.c. control circuits. If a number of analogue type control loops are installed at each terminal of a multiterminal h.v.d.c. system, the simultaneous digital simulation of the controls at all the terminals as a technique of laboratory modelling to be used in conjunction with a basic simulator is not likely to be a feasible method of system investigation.

Although the construction of fault detectors and converter monitors will facilitate the extension and improvement of fault control programmes it is premature to equip a research simulator of this type with a complete set of detecting and monitoring units in the immediate future. The design of various types of detectors, in conjunction with a multi-terminal simulator, should however be profitable.

The fault control programme can be extended to develop more sophisticated techniques for use in connection with a.c. system faults and a.c. switching, e.g. loss of one of many machines feeding a rectifier, fall of inverter a.c. system short circuit level due to switching, partial loss of a.c. voltage for longer than about 100 ms, co-ordination with a.c. protection etc. Criteria for altering the power/current order and for shutting down a converter need to be investigated - these rapid changes are not to be confused with changes that "national control" may request from considerations of the power system as a whole.

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APPENDIX A

This appendix contains the Boolean equations of the basic fault control program for detecting transmission system faults. Each fault is identified by superscripts and subscripts denoting the elements between which the fault occurs. For example F^{15}_{26} refers to a line to line fault between line 15 and 26 of Converter station B. F^{E}_{+}, F^{E}_{-}, F^{+}_{-} refer to earth to positive pole, negative pole and positive to negative pole faults in any part of the system. The other symbols have been defined previously.

The equations are written for every one of the fifteen operating modes of the system sketched previously and classified in the chart of Table 4.1. They are identified by headings of the form G.n/T.m where n = group number, m = tier number and an addition identifying alphabetic. The fifteen sketches of fig. 4.8 are drawn in the same order as the equations here.

Line sections are numbered in fig. 4.7.

$+$ = Boolean OR operation

$\cdot$ = Boolean AND operation

$'$ = Complement; NOT operation

MODE G1/T1(a)

$$F^{13}_{24} = A_1 \cdot M_1 + M_1 \cdot A_4' \cdot A_5' \quad *$$

$$F^{15}_{26} = B_1 \cdot M_4 + M_4 \cdot B_4' \cdot B_5' \quad *$$

$$F^{17}_{28} = C_1 \cdot M_7 + M_7 \cdot C_4' \cdot C_5' \quad *$$

$$\begin{aligned} F^{+}_{-} = {} & M_{10}\cdot(A_4'\cdot A_5'\cdot B_4'\cdot B_5'\cdot C_4'\cdot C_5') \\ & + A_1\cdot(B_4'\cdot B_5'\cdot C_4'\cdot C_5') + B_1\cdot(C_4'\cdot C_5'\cdot A_4'\cdot A_5') \\ & + C_1\cdot(A_4'\cdot A_5'\cdot B_4'\cdot B_5') \end{aligned} \qquad \ast$$

$$F^{E}_{13} = A_2\cdot M_2 + M_2\cdot A_4' + M_1\cdot A_4'\cdot A_5 \qquad \ast$$

$$F^{E}_{15} = B_2\cdot M_5 + M_5\cdot B_4' + M_4\cdot B_4'\cdot B_5 \qquad \ast$$

$$F^{E}_{17} = C_2\cdot M_8 + M_8\cdot C_4' + M_7\cdot C_4' + M_7\cdot C_4'\cdot C_5 \qquad \ast$$

$$\begin{aligned} F^{E}_{+} = {} & M_{11}\cdot(A_4'\cdot B_4'\cdot C_4') \\ & + A_2\cdot(B_4'\cdot C_4') + B_2\cdot(C_4'\cdot A_4'\cdot) + C_2\cdot(A_4'\cdot B_4') \\ & + M_{10}\cdot(A_4'\cdot A_5 + B_4'\cdot B_5 + C_4'\cdot C_5) \\ & + A_1\cdot(B_4'\cdot B_5 + C_4'\cdot C_5) + B_1\cdot(C_4'\cdot C_5 + A_4'\cdot A_5) \\ & + C_1\cdot(A_4'\cdot A_5 + B_4'\cdot B_5) \end{aligned} \qquad \ast$$

$$F^{E}_{24} = A_3\cdot M_3 + M_3\cdot A_5' + M_1\cdot A_4\cdot A_5' \qquad \ast$$

$$F^{E}_{26} = B_3\cdot M_6 + M_6\cdot B_5' + M_4\cdot B_4'\cdot B_5 \qquad \ast$$

$$F^{E}_{28} = C_3\cdot M_9 + M_9\cdot C_5' + M_7\cdot C_4\cdot C_5' \qquad \ast$$

$$\begin{aligned} F^{E}_{-} = {} & M_{12}\cdot(A_5'\cdot B_5'\cdot C_5') \\ & + A_3\cdot(B_5'\cdot C_5') + B_3\cdot(C_5'\cdot A_5') + C_3(A_5'\cdot B_5') \\ & + M_{10}\cdot(A_4\cdot A_5' + B_4\cdot B_5' + C_4\cdot C_5') \\ & + A_1\cdot(B_4\cdot B_5' + C_4\cdot C_5') + B_1(C_4\cdot C_5' + A_4\cdot A_5') \\ & + C_1\cdot(A_4\cdot A_5' + B_4\cdot B_5') \end{aligned} \qquad \ast$$

MODE G1/T2(a)

$$F^{13}_{24} = A_1.M_1 + M_1.A_4'.A_5'$$

$$F^{15}_{26} = B_1.M_4 + M_4.B_4'.B_5'$$

$$F^{+}_{-} = M_{10}.(A_4'.A_5'.B_4'.B_5') + A_1.(B_4'.B_5') + B_1.(A_4'.A_5')$$

$$F^{E}_{+} = M_{11}.(A_4'.B_4') + A_2.B_4' + B_2.A_4'$$

$$+ A_2.M_2 + M_2.A_4' + M_1.A_4'.A_5$$

$$+ B_2.M_5 + M_5.B_4' + M_4.B_4'.B_5$$ *

$$+ M_{10}.(A_4'.A_5 + B_4'.B_5 + C_5)$$

$$+ A_1.(B_4'.B_5 + C_5) + B_1.(A_4'.A_5 + C_5)$$

$$F^{E}_{24} = A_3.M_3 + M_3.A_5' + M_1.A_4.A_5'$$

$$F^{E}_{26} = B_3.M_6 + M_6.B_5' + M_4.B_4.B_5'$$

$$F^{E}_{28} = C_3.M_9 + M_9.C_5'$$

$$F^{E}_{-} = M_{12}.(A_5'.B_5'.C_5')$$

$$+ A_3.(B_5'.C_5) + B_3.(C_5'.A_5') + C_3.(A_5'.B_5')$$

$$+ M_{10}.(A_4.A_5' + B_4.B_5')$$

$$+ A_1.(B_4.B_5') + B_1.(A_4.A_5')$$

MODE G1/T2(b)

$$F^{13}_{24} = A_1.M_1 + M_1.A_4'.A_5'$$

$$F^{15}_{26} = B_1.M_4 + M_4.B_4'.B_5'$$

$F^{+}_{-} = M_{10}.(A_4'.A_5'.B_4'.B_5') + A_1.(B_4'.B_5') + B_1.(A_4'.A_5')$

$F^{E}_{13} = A_2.M_2 + M_2.A_4' + M_1.A_4'.A_5$

$F^{E}_{17} = C_2.M_8 + M_8.C_4'$

$F^{E}_{+} = M_{11}.(A_4'.B_4'.C_4')$

$+ A_2.(B_4'.C_4') + B_2.(C_4'.A_4') + C_2.(A_4'.B_4')$

$+ M_{10}.(A_4'.A_5 + B_4'.B_5)$

$+ A_1.(B_4'.B_5) + B_1.(A_4'.A_5)$

$F^{E}_{-} = M_{12}.(A_5'.B_5') + A_3.B_5' + B_3.A_5'$

$+ A_3.M_3 + M_3.A_5' + M_1.A_4.A_5'$

$+ B_3.M_6 + M_6.B_5' + M_4.B_4.B_5'$ ＊

$+ M_{10}.(A_4.A_5' + B_4.B_5' + C_4)$

$+ A_1.(B_4.B_5' + C_4) + B_1.(A_4.A_5' + C_4)$

MODE G1/T2(c)

$F^{13}_{24} = A_1.M_1 + M_1.A_4'.A_5$

$F^{17}_{28} = C_1.M_7 + M_7.C_4'.C_5$

$F^{+}_{-} = M_{10}.(A_4'.A_5'.C_4'.C_5') + A_1.(C_4'.C_5') + C_1.(A_4'.A_5')$ ＊

$$F_{+}^{E} = M_{11}.(A_4'.C_4') + A_2.C_4' + C_2.A_4'$$

$$+ A_2.M_2 + M_2.A_4' + M_1.A_4'.A_5$$

*

$$+ C_2.M_8 + M_8.C_4' + M_7.C_4'.C_5$$

$$+ A_1(B_5 + C_4'.C_5) + C_1.(A_4'.A_5 + B_5)$$

$$F_{24}^{E} = A_3.M_3 + M_3.A_5' + M_1.A_4.A_5'$$

$$F_{26}^{E} = B_3.M_6 + M_6.B_5'$$

$$F_{28}^{E} = C_3.M_9 + M_9.C_5' + M_7.C_4'.C_5$$

$$F_{-}^{E} = M_{12}.(A_5'.B_5'.C_5')$$

$$+ A_3.(B_5'.C_5') + B_3.(C_5'.A_5') + C_3.(A_5'.B_5')$$

$$+ M_{10}.(A_4.A_5' + C_4.C_5')$$

$$+ A_1.(C_4.C_5'). + C_1(A_4.A_5')$$

MODE G1/T2(d)

$$F_{24}^{13} = A_1.M_1 + M_1.A_4'.A_5'$$

$$F_{28}^{17} = C_1.M_7 + M_7.C_4'.C_5'$$

$$F_{-}^{+} = M_{10}.(A_4'.A_5'.C_4'.C_5') + A_1.(C_4'.C_5') + C_1.(A_4'.A_5)$$

$$F_{13}^{E} = A_2.M_2 + M_2.A_4' + M_1.A_4'.A_5$$

$$F_{15}^{E} = B_2.M_5 + M_5.B_4'$$

$$F_{17}^{E} = C_2.M_8 + M_8.C_4' + M_7.C_4'.C_5$$

$$F^E_+ = M_{11}.(A_4'.B_4'.C_4')$$

$$+ A_2.(B_4'.C_4') + B_2.(C_4'.A_4') + C_2.(A_4'.B_4')$$

$$+ M_{10}.(A_4'.A_5 + C_4'.C_5)$$

$$+ A_1.(C_4'.C_5) + C_1.(A_4'.A_5)$$

$$F^E_- = M_{12}.(A_5'.C_5') + A_3.C_5' + C_3.A_5'$$

$$+ A_3.M_3 + M_3.A_5' + M_1.A_4.A_5'$$

$$+ C_3.M_9 + M_9.C_5' + M_7.C_4.C_5' \qquad *$$

$$+ M_{10}.(A_4.A_5' + B_4 + C_4.C_5')$$

$$+ A_1.(B_4 + C_4.C_5') + C_1.(A_4.A_5' + B_4)$$

MODE G1/T3(a)

$$F^E_{24} = A_3.M_3 + M_3.A_5'$$

$$F^E_{26} = B_3.M_6 + M_6.B_5'$$

$$F^E_{28} = C_3.M_9 + M_9.C_5'$$

$$F^E_- = M_{12}.(A_5'.B_5'.C_5')$$

$$+ A_3.(B_5'.C_5') + B_3.(C_5'.A_5') + C_3.(A_5'.B_5')$$

MODE G1/T3(b)

$$F^E_{13} = A_2.M_2 + M_2.A_4'$$

$$F^E_{15} = B_2.M_5 + M_5.B_4'$$

$$F^{E}_{17} = C_2.M_8 + M_8.C_4'$$

$$F^{E}_{+} = M_{11}.(A_4'.B_4'.C_4')$$

$$+ A_2.(B_4'.C_4') + B_2.(C_4'.A_4') + C_2.(A_4'.B_4')$$

MODE G1/T3(c)

$$F^{+}_{-} = M_{10}.(A_4'.A_5') + A_1.(B_5'.C_4')$$

$$+ A_1.M_1 + M_1.A_4'.A_5$$ ✱

$$F^{E}_{+} = M_{11}.(A_4'.C_4') + A_2.C_4' + C_2.A_4'$$

$$+ A_2.M_2 + M_2.A_4' + C_2.M_8 + M_8.C_4'$$

$$+ M_{10}.(A_4'.A_5 + B_5) + A_1.B_5.$$

$$F^{E}_{-} = M_{12}.(A_5'.B_5') + A_3.B_5' + B_3.A_5'$$

$$+ A_3.M_3 + M_3.A_5' + B_3.M_6 + M_6.B_5'$$

$$+ M_{10}.(A_4.A_5' + C_4) + A_1.C_4$$

MODE G1/T3(d)

$$F^{+}_{-} = M_{10}.(A_4'.A_5) + A_1.(B_4'.B_5')$$

$$+ A_1.M_1 + M_1.A_4'.A_5'$$ ✱

$$F_{+}^{E} = M_{11}.(A_4'.B_4') + A_2.B_4' + B_2.A_4'$$
$$+ A_2.M_2 + M_2.A_4' + B_2.M_5 + M_5.B_4'$$
$$+ M_{10}.(A_4'.A_5 + C_5) + A_1.C_5$$

$$F_{-}^{E} = M_{12}.(A_5'.C_5') + A_3.C_5' + C_3.A_5'$$
$$+ A_3.M_3 + M_3.A_5' + C_3.M_9 + M_9.C_5'$$
$$+ M_{10}.(A_4.A_5' + B_4) + A_1.B_4$$

MODE G2/T1(a)

$$F_{-}^{+} = M_{10}.(A_4'.A_5'.C_4'.C_5')$$
$$+ A_1.(C_4'.C_5') + C_1.(A_4'.A_5')$$
$$+ A_1.M_1 + M_1.A_4'.A_5' \qquad *$$
$$+ C_1.M_7 + M_7.C_4'.C_5'$$

$$F_{+}^{E} = M_{11}.(A_4'.C_4') + A_2.C_4' + C_2.A_4'$$
$$+ A_2.M_2 + M_2.A_4'$$
$$+ C_2.M_8 + M_8.C_4'$$
$$+ A_1.(C_4'.C_5) + C_1.(A_4'.A_5)$$
$$+ M_{10}.(A_4'.A_5 + C_4'.C_5)$$

$$F_{-}^{E} = M_{12}.(A_5'.C_5') + A_3.C_5' + C_3.A_5'$$

$$+ A_3.M_3 + M_3.A_5'$$

$$+ C_3.M_9 + M_9 . C_5'$$

$$+ M_{10}.(A_4.A_5'. + C_4.C_5')$$

$$+ A_1.(C_4.C_5') + C_1.(A_4.A_5')$$

MODE G2/T1(b)

$$F_{-}^{+} = M_{10}.(A_4'.A_5'.B_4'{,}B_5')$$

$$+ A_1.(B_4'.B_5') + B_1.(A_4'.A_5') \qquad \ast$$

$$+ A_1.M_1 + M_1.A_4'.A_5'$$

$$+ B_1.M_4 + M_4.B_4'.B_5'$$

$$F_{+}^{E} = M_{11}.(A_4'.B_4') + A_2.B_4' + B_2.A_4'$$

$$+ A_2.M_2 + M_2.A_4'$$

$$+ B_2.M_5 + M_5.B_4'$$

$$+ M_{10}.(A_4'.A_5 + B_4'{,}B_5)$$

$$+ A_1.(B_4'.B_5) + B_1.(A_4'.A_5)$$

$$F_{-}^{E} = M_{12}.(A_5'.B_5') + A_3.B_5' + B_3.A_5'$$

$$+ A_3.M_3 + M_3.A_5' + B_3.M_6 + M_6.B_5'$$

$$+ M_{10}.(A_4.A_5' + B_4.B_5')$$

$$+ A_1.(B_4.B_5') + B_1.(A_4.A_5')$$

MODE G2/T2(a)

$$F_{-}^{E} = M_{12}.(A_5'.C_5') + A_3.C_5' + C_3.A_5' + A_3.M_3 + M_3.A_5' + C_3.M_9 + M_9.C_5'$$

MODE G2/T2(b)

$$F_{+}^{E} = M_{11}.(A_4'.C_4') + A_2.C_4' + C_2.A_4' + A_2.M_2 + M_2.A_4' + C_2.M_8 + M_8.C_4'$$

MODE G2/T2(c)

$$F_{-}^{E} = M_{12}.(A_5'.B_5') + A_3.B_5' + B_3.A_5' + A_3.M_3 + M_3.A_5' + B_3.M_6 + M_6.B_5'$$

MODE G2/T2(d)

$$F_{+}^{E} = M_{11}.(A_4'.B_4') + A_2.B_4' + B_2.A_4' + A_2.M_2 + M_2.A_4' + B_2.M_5 + M_5.B_4'$$