Reduced Dynamic Model of the Alternate Arm Converter

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***Abstract*—The Alternate Arm Converter (AAC) is a hybrid HVDC converter that maintains low power losses while protecting against DC-side faults. This paper shows the development of a Reduced Dynamic Model (RDM) of the AAC which enables time efficient system level modelling of multi-converter HVDC systems. The methodology and equations to develop the RDM are described. The RDM is then compared directly to a full switching model of the AAC, where the accuracy and the computation times are measured. The RDM is observed to simulate almost 20 times faster than the full dynamic model. The RDM is then evaluated under normal and abnormal operating conditions using a point to point HVDC model while maintaining a good level of accuracy.**

***Index Terms*—HVDC, AC/DC Converters, Voltage Source Converters**

I. Introduction

In recent years the Voltage Source Converter (VSC) has become the preferred HVDC technology for connecting remote renewable generation. The VSC has several advantages over Current Source Converters (CSC). The main benefits of the VSC being that it does not require a connection to a stronng AC source and it can provide flexible control of both real and reactive power. It also allows black start of an islanded network, such as an offshore wind farm. VSCs have been identified as the HVDC technology for use with Mutli-Terminal DC (MTDC) grids, this is thanks to the ease of power flow reversal which is achieved by reversing current polarity rather than voltage polarity with CSCs [1]. The first MTDC which uses VSCs in the world is in operation in Nan'ao, China, operating at ± 160 kV [2].

The first VSC that was developed was the two-level converters as it switches between two voltage levels to create the AC waveforms and the first VSC was built in . These two-level VSCs suffer from high switching losses as the converter switches rapidly between the positive and negative DC rails to produce a simple AC waveform, using low frequency pulse-width modulation resulting in high harmonic content which requires significant filtering [3]. This high switching frequency of the two-level converter gives rise to their loss figure of approximately 1.8 % [4]. To achieve very high voltages a high number of devices must be placed in series which causes issues with switching them simultaneously [5]. Multi-level converters use additional DC voltage levels to create the AC waveform. The two-level VSC cannot protect itself in the case of a DC-side fault because the diode connected in parallel with the IGBT allows the DC fault current to flow through the converter. A higher number of levels implies less filtering and lower switching losses [6], however as the number of levels increase so too does the complexity of the converter.

In the early 2000's a new VSC circuit was proposed in [7] termed the Modular Multi-level Converter (MMC). The MMC has six arms and each arm comprises a high number of cells. These cells are composed of two IGBTs and a DC capacitor. Each cell represents a DC voltage level that is used to create a staircase AC waveform with numerous voltage steps. This results in very low harmonic content in the waveform and hence the elimination of AC filters [6]. Another advantage of the MMC is the lower switching frequency of the IGBTs when compared to the two-level and three-level VSCs, leading to a reduction in the switching losses. The first built MMC was the Trans Bay Cable Project in the USA by Siemens [6].

However, the half-bridge MMC is still susceptible to DC side faults. At present a DC side fault is cleared by opening the circuit breakers on the AC side. This may not be practical in a large meshed HVDC network. At present a DC circuit breaker is not commercially available. If full-bridge cells were used in the MMC, it would be able to manage the DC side faults with the sacrifice of almost 70% of additional losses during normal operation [8]. Several options have been proposed, instead of using the full-bridge MMC, which offer protection against DC side faults while maintaining lower losses including the use of double clamp submodules in [9] which limits DC fault currents and alternative converter circuits have been proposed in [10]–[12]. The Alternate Arm Converter (AAC) in [12] is a hybrid VSC which is modular in structure like the MMC and switches between upper and lower arms like a two-level VSC. The AAC uses full-bridge cells and thus can protect against DC faults. The AAC is introduced in full in Section 2.

A full scale multi-level VSC for high voltage applications (e.g. ± 320 kV) can have hundreds of levels. In order to accurately simulate the converter each cell must explicitly modelled. These converter models can takes several hours to simulate. These long computation times are not practical for system studies, which would have several converters. Reduced dynamic models of power electronic converters can be used for high level system studies because they are less computationally intensive as each switching device is not explicitly modelled. However, these reduced models cannot be used for high frequency transient events and detailed converter analysis. Reduced models have been developed for the MMC

in [13]–[15]. In [13] a combination of current and voltage sources are used to represent the MMC. The AC side and the DC side of the converter are represented separately. It was observed to be significantly more efficient in computation time when compared to full dynamic switching model. This model was assessed for different fault conditions in [16] and it showed that the reduced model was capable of accurately representing AC-side faults but not DC-side faults. The second is a continuous state space mathematical representation of the MMC [14]. It is based on time variable capacitors and knowing the number of cells that are inserted at each instance. This continuous model was compared with an experimental MMC, it was observed that the continuous model closely matched the experimental set up and provided smoother waveforms. In [15] another continuous model is presented and it also uses the insertion indices, being the number of cells inserted at a given time relative to the total number of cells, to determine the arm voltage. A blocking and deblocking feature was also implemented in this model to improve the accuracy of the model during abnormal operation, such as start up and protective actions.

This paper describes the operation of the AAC and explains the importance of energy balancing in the converter. This is followed by a description of the methodology used for developing the reduced dynamic model (RDM). The RDM is then compared to the full switch model for several scenarios including normal and abnormal operation using a point to point link.

II. Alternate Arm Converter

The AAC is a hybrid VSC which was first introduced in [12] and elaborated upon in [17]. The circuit diagram of the AAC is shown in Figure 1.

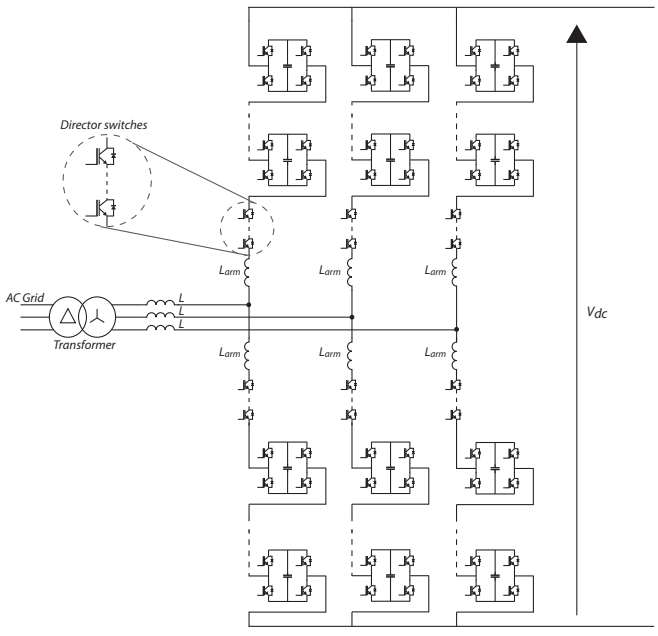


Figure 1. Circuit diagram of the alternate arm converter

There are six converter arms and each arm contains a stack of cells, a director switch and an arm inductor. The cells in the stack are full H-bridge cells and are capable of producing positive and negative voltage. The director switch is used to alternate the current path between the upper and lower arm, similar to the two-level VSC. The upper arm is used during the positive half cycle and the lower arm during the negative half cycle. The director switch comprises several series connected IGBTs. By alternating between the upper and lower arm the maximum voltage the cells need to produce, during normal operation, is half the DC bus voltage. This implies fewer cells in the stack compared to the full bridge MMC. During the transition from one arm to the other there is a short overlap period when both arms are in conduction. This overlap period can be used to circulate currents within the converter to balance the energy stored in the cells. The director switches are soft-switched thanks to the stack of cells which actively control the current to zero before switching.

The AAC is capable of blocking DC side faults as full-bridge cells are used and the converter can be designed to produce a voltage that can equal the AC grid voltage. Should a DC fault occur the converter is still able to oppose the AC side voltage and maintain control of the internal converter currents [17]. During a DC fault the AAC is able to act as a STATCOM and provide reactive power support to the AC grid. The AAC is able to maintain low power losses as the stack has fewer cells than the full-bridge MMC. This converter also has better temperature distribution between the IGBT submodules when compared to the full-bridge and half-bridge MMC [18]. The AAC has also been used in a DC/DC converter design for low conversion ratios [19]. In [17] a 20 MW AAC was observed to be near 99 % efficient.

A. Energy Balancing in the AAC

The charge of the cell capacitors will vary over time due to the AC current running through the stack. It is important that the energy in the cells is balanced to ensure the capacitor voltages do not drastically drift away from there nominal voltage. To balance energy between individual cells in the stack a cell rotation algorithm is used. This algorithm determines which capacitor is to be inserted next depending on the capacitor voltage. The cell with the highest voltage is inserted before a cell with a lower voltage. The energy of the entire stack also requires balancing and this is achieved by running a DC current through both the upper and lower arms during the overlap period when both arm are in conduction. This allows an exchange of energy between the stacks ensuring the energy is balanced [17].

III. Reduced Dynamic Model

A RDM is used to decrease simulation time while maintaining accurate external converter characteristics. It should be noted that the proposed RDM does not model the high frequency effects or harmonic content which is inherent to the switching occurrences from the individual IGBTs as they are

not modelled. It is assumed that a good cell rotation algorithm is in place that balances the individual cells within the arm. The RDM of the ACC was developed in MATLAB Simulink.

A. Methodology

The first step taken is to determine how to represent the stack without using IGBT switches. The cells in the stack collectively act as a controllable voltage source with a maximum voltage determined by the number of cells times the cell capacitor voltage. The stack of cells also has an associated resistance which comes from the IGBT devices on resistance. Figure 2 shows the representation used for the RDM, which is a controllable voltage source with a series resistance and an ideal switch represents the director switch.

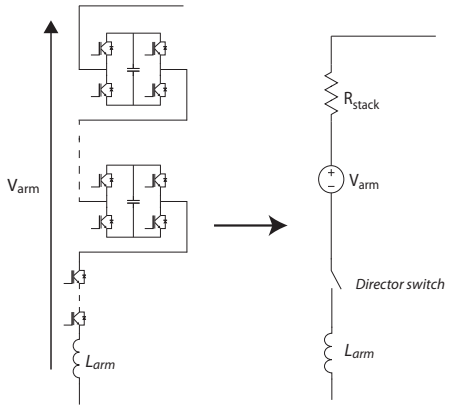


Figure 2. RDM arm representation

As with the MMC, it is important to monitor and balance the energy in the arms of the AAC. In the full model each cell capacitor voltage is measured to evaluate the energy deviation in the stack using Equation 1. Where $\triangle E$ is the energy deviation, C_{cell} is the cell capacitance, $V_{cell_{nom}}$ is the nominal cell voltage, V_{cell_i} is the measured cell voltage, and N is the number of cells in one arm.

$$\triangle E = N\frac{C_{cell}}{2}V_{cell_{nom}}^2 - \frac{C_{cell}}{2}\sum_{i=1}^{N}V_{cell_i}^2 \tag{1}$$

However, in the RDM the measurement of individual cell voltages is not available, so the stack energy is estimated using the integral of the current times the voltage through the arm, shown in Equation 2. Where R_{stack} is the equivalent resistance of the stack, assuming at least two IGBTs in each cell are always conducting, $\triangle E_{RDM}$ is the energy deviation of the RDM, V_{stack} is the stack voltage, and I_{arm} is the arm current.

$$\triangle E_{RDM} = \int V_{stack}(t)I_{arm}(t) + R_{stack}I_{arm}^2(t)\,dt \tag{2}$$

The controllable voltage source must be constrained to the maximum voltage which is determined by the number of cells times the cell capacitor voltage. The energy deviation calculated in Equation 2 is used to estimate the average cell voltage of the stack shown in Equation 3.

$$V_{cell_{average}} = \sqrt{V_{cell_{nom}}^2 - \left(2\frac{\triangle E_{RDM}}{NC_{cell}}\right)} \tag{3}$$

Using this average cell voltage, a limit can be placed on the control command for the stack voltage ensuring that the voltage generated by the stacks does not exceed the maximum voltage, which is N times the cell voltage. Figure 3 shows how the voltage is limited.

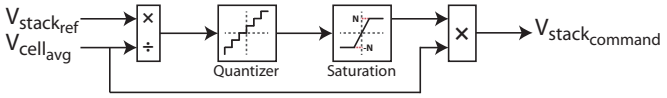


Figure 3. Block diagram of voltage constraint control

The full RDM circuit is shown in Figure 4

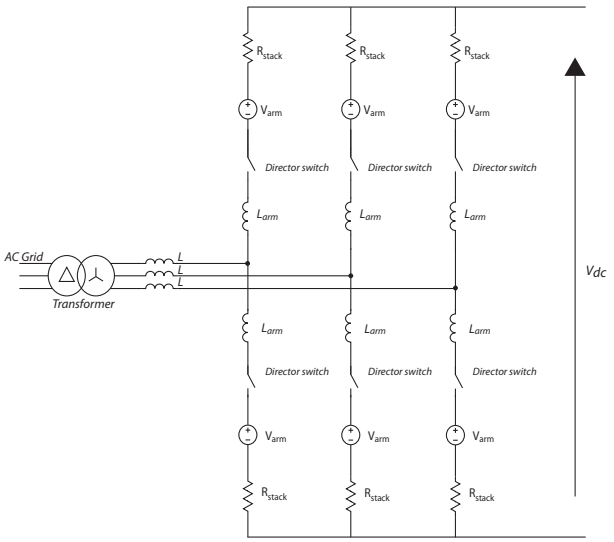


Figure 4. AAC RDM circuit

IV. Simulations

The full switching model (FSM) and the RDM were modelled using the SimPowerSystems toolbox in MATLAB Simulink on a Intel Xeon 2.4 GHz PC with 12 GB of installed memory.

A. Converter Simulations

Table I show the converter parameters that were used in the FSM and the RDM. The converter is connected to a ideal voltage sources on both the AC and DC side. A scaled down model was used for all simulations to allow direct comparison between the FSM and the RDM.

Table I
AAC MODEL PARAMETERS

Rated Power	20 MW
DC Voltage	±10 kV
Line - Line Grid AC Voltage	11 kV
Line - Line Converter AC Voltage	16 kV
Operating Frequency	50 Hz
Number of Cells per Arm	9
Number of series IGBTS in Director Switch	5
Cell Voltage	1.5 kV
Cell Capacitor	4 mF
Phase Inductor	4.1 mH
Arm Inductor	100 µH

Figure 5 shows the comparison between the FSM and the RDM. It can be seen from Figure 5c that the RDM and the FSM are very closely matched, including start up and power flow reversal. The models were simulated with different time steps and the results are shown in Table II. The relationship between between simulation timestep and the computation difference is shown in Figure 6, and it can be seen that as the timestep is increased that the computation time for both models reduces, and that the RDM becomes significantly quicker for higher timesteps.

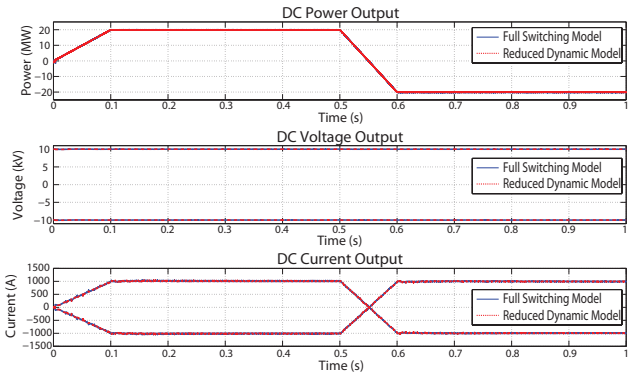
Table II
MODEL COMPUTATION TIMES FOR 1 SECOND OF DATA

Timestep (μs)	FSM (s)	RDM (s)	FSM/RDM
1	398.28	88.16	4.52
5	153.16	15.22	10.07
10	91.11	8.98	10.14
20	70.02	5.86	11.95
50	72.97	4.07	17.93

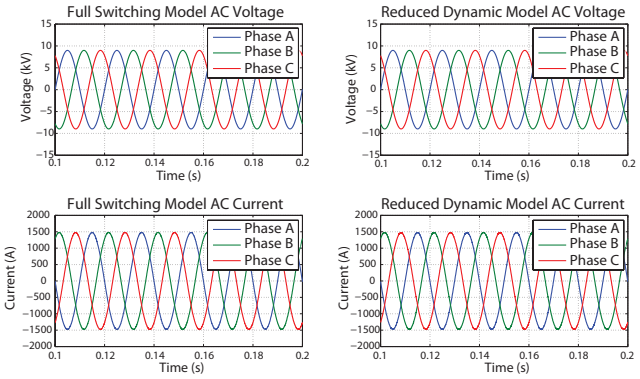
To determine the accuracy of the RDM the waveforms of the AC and DC current were compared directly to the AC and DC FSM current waveforms. The average percentage difference was determined using Equation 4. To ensure that there were no divide by zero errors, a limit was placed on the current that was used in the difference equation. The calculation was performed for current above the value of 0.1 pu.

$$\overline{Difference}(\%) = \left(\sqrt{\left(\frac{I_{FM} - I_{RDM}}{I_{FM}} \right)^2} \right) \times 100 \quad (4)$$

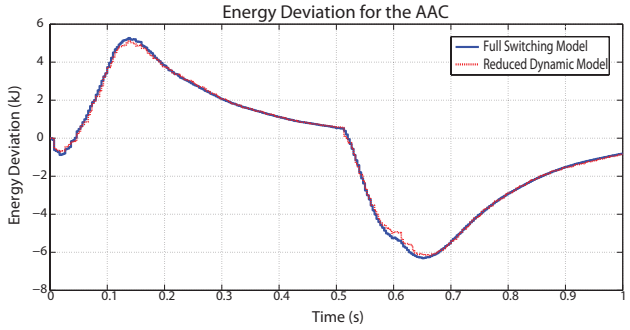
Figure 7 shows the accuracy results for the RDM for different time steps compared to the FSM with a time step of 1 μs, for the AC and DC currents. It can be seen from this figure that the accuracy of RDM reduces, approximately linearly, as the time step is increased but it matches closely. This increase in error may be linked to the harmonic content in the FSM associated with the switching occurrences of the IGBTs.



(a) DC graphs



(b) AC graphs



(c) Energy deviation

Figure 5. Comparison plots for AAC

B. System Simulations

A point to point HVDC scheme, shown in Figure 8, was modelled to allow effective testing of the RDM under normal and abnormal operating conditions. These were directly compared to a full power electronic model using the same point to point model. The same converter parameters given in Table I and the cable data in Table III were used for all scenarios. A simple voltage droop controller was used to control the point to point link.

1) Normal Operation: The real benefit of using a RDM is clear when it comes to simulating several converters at time

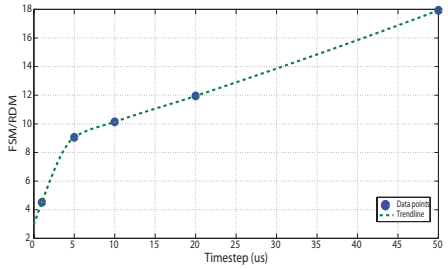


Figure 6. Computation time versus time step

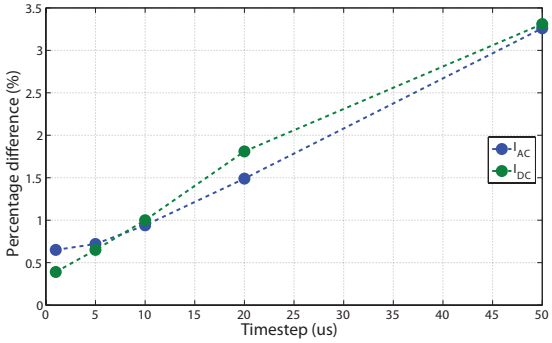


Figure 7. Percentage difference between FSM and RDM versus time step

in a single model. For the system shown in Figure 8 it was observed that the RDM ran more than six times quicker than the FSM equivalent for a time step of 1 μs obtaining 1 second of data. Figure 9 shows the DC cable voltage, measured on the DC side of AAC 1 and the DC power of AAC 1 and AAC 2.

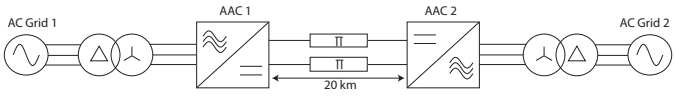


Figure 8. Point to point model block diagram

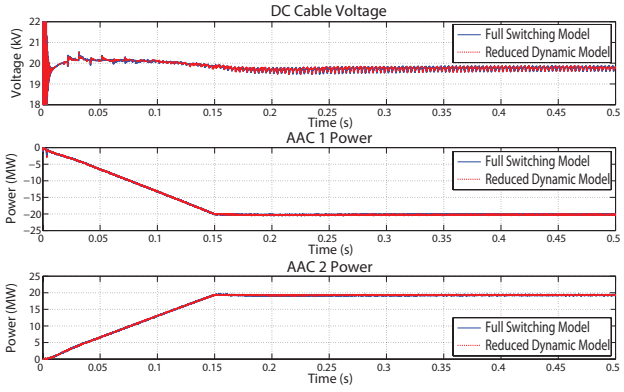


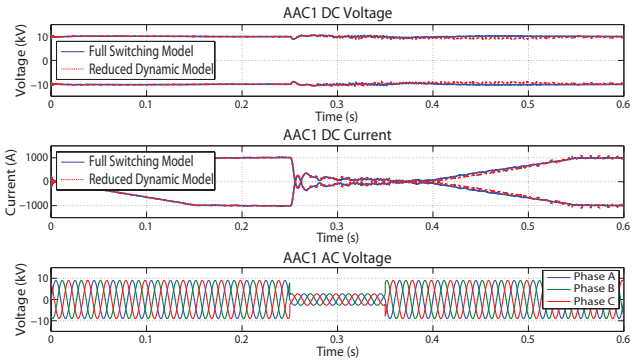
Figure 9. Normal operating voltage and power for point to point system

Table III
CABLE PARAMETERS

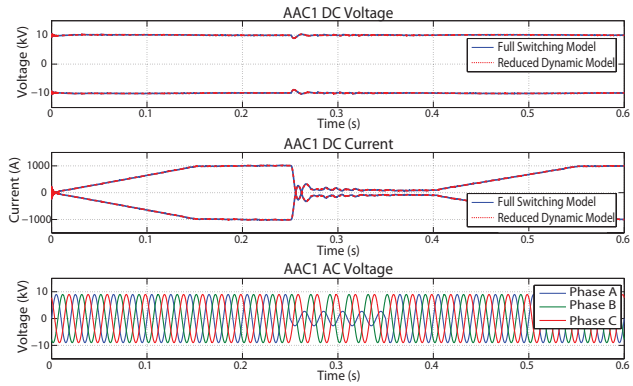
Parameter	Value	Unit
Resistance	11.3	mΩ/km
Capacitance	0.212	μF/km
Inductor	0.362	mH/km
Length	20	km

2) Abnormal Operation: Three fault conditions were placed on the system in Figure 8. Two AC faults were applied on AC Grid 1, a three-phase symmetrical fault and a phase to ground fault. A line to gournd DC fault was placed half way along the cable, at 10 km. For all fault scenarios the fault are applied for 100 milliseconds at 0.25 seconds.

Figure 10 show the simulation results of the FSM and the RDM for a three-phase symmetrical AC fault and a phase to ground AC fault on phase A. The power is reduced to 2 MW after 1 ms and the power references ramps back to full power at 0.4 seconds.



(a) Three-phase AC fault



(b) Phase to ground AC fault

Figure 10. Simulation results for AC fault scenarios

It can be seen that the RDM matches the FSM closely for the three-phase AC fault apart from oscillations on the DC voltage and current. For the phase to ground AC fault the reduced model matches very closely to the FSM.

The simulation results for a DC line to ground fault is shown in Figure 11. For this fault case the power reference is reduced

to zero after 1 ms and after the fault has cleared the converter returns to full power after 0.4 seconds. It can be seen that the DC line to ground that the RDM matches quite closely.

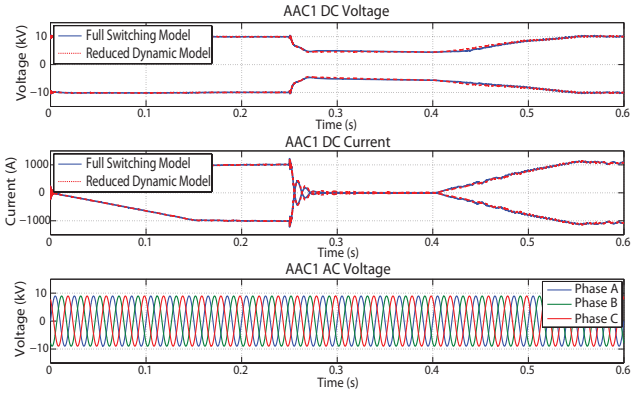


Figure 11. DC line to ground fault

Table IV shows the computation time for the different cases simulated, where A is the three phase AC fault, B is the AC line to ground fault, and C is the DC line to ground fault. The percentage difference between the RDM and FSM current waveforms, for 0.6 seconds of data at a timestep of 1 μs is also given in Table IV. The accuracy was determined using the same method outlined in Section 3. It can be seen that for all scenarios that the RDM has a faster computation time and maintains a high level of accuracy for the three fault cases simulated.

Table IV
NORMAL AND ABNORMAL COMPUTATION TIMES AND PERCENTAGE DIFFERENCE FOR 1 μs TIMESTEP

Fault case	FSM (s)	RDM (s)	FSM/RDM	$I_{ac}(\%)$	$I_{dc}(\%)$
No fault	952.02	142.33	6.69	0.61	0.13
A	856.72	111.86	7.66	6.34	5.24
B	848.96	114.07	7.44	1.07	0.96
C	882.37	115.69	7.63	1.71	1.86

V. CONCLUSIONS

A RDM of the AAC was presented. The methodology to create the model was described and the importance of limiting the voltage sources was outlined. The RDM was compared to a FSM in MATLAB and was observed to match the current and voltage waveforms of the converter closely and ran up to 17 times faster than the FSM. The RDM was then tested in a point to point system for different DC and AC faults scenarios. It was observed that the RDM closely matched the FSM for the AC faults conditions and for a DC line to ground fault.

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