Novel Solution Processable Dielectrics for Organic and Graphene Transistors

by

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This thesis describes the work carried out from November 2008 to November 2011 within the Experimental Solid State Physics group at Imperial College London under the supervision of Professor Thomas D. Anthopoulos. The material in this thesis has not been submitted for a degree at any other university and except where explicitly stated is the product of my own work.

Florian A. J-M. Colléaux

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Abstract

In this thesis we report the development of a range of high-performance thin-film transistors utilising different solution processable organic dielectrics grown at temperatures compatible with inexpensive substrate materials such as plastic. Firstly, we study the dielectric properties and application of a novel low-k fluoropolymer dielectric, named Hyflon AD (Solvay). The orthogonal nature of the Hyflon formulation, to most conventional organic semiconductors, allows fabrication of top-gate transistors with optimised semiconductor/dielectric interface. When used as the gate dielectric in organic transistors, this transparent and highly water-repellent polymer yields high-performance devices with excellent operating stability. In the case of top-gate organic transistors, hole and electron mobility values close to or higher than 1 cm^2/Vs, are obtained. These results suggest that Hyflon AD is a promising candidate for use as dielectric in organic and potentially hybrid electronics. By taking advantage of the non-reactive nature of the Hyflon AD dielectric, the p-doping process of an organic blend semiconductor using a molybdenum based organometallic complex as the molecular dopant, has also been investigated for the first time.

Although the much promising properties of Hyflon AD were demonstrated, the resulting transistors need, however, to be operated at high voltages typically in the range of 50-100 V. The latter results to a high power consumption by the discrete transistors as well as the resulting integrated circuits. Therefore, reduction in the operating voltage of these devices is crucial for the implementation of the technology in portable battery-operated devices. Our approach towards the development of low-voltage organic transistors and circuits explored in this work focused on the use of self-assembled monolayer (SAM) organics as ultra-thin gate dielectrics. Only few nanometres thick (2-5 nm), these SAM dielectrics are highly insulating and yield high geometrical capacitances in the range 0.5 - 1 $\mu F/cm^2$. The latter has enabled the design and development of organic transistors with operating voltages down to a few volts. Using these SAM nanodielectrics high performance transistors with ambipolar transport characteristics have also been realised and combined to form low-voltage integrated circuits for the first time.

In the final part of this thesis the potential of Hyflon AD and SAM dielectrics for application in the emerging area of graphene electronics, has been explored. To this end we have employed chemical vapour deposited (CVD) graphene layers that

can be processed from solution onto the surface of the organic dielectric (Hyflon AD, SAM). By careful engineering of the graphene/dielectric interface we were able to demonstrate transistors with improved operating characteristics that include; high charge carrier mobility (~1400 cm^2/Vs), hysteresis free operation, negligible unintentional doping and improved reliability as compared to bare SiO_2 based devices. Importantly, the use of SAM nanodielectrics has enabled the demonstration of low voltage ($<|1.5|$ V) graphene transistors that have been processed from solution at low temperature onto flexible plastic substrates. Graphene transistors with tuneable doping characteristics were also demonstrated by taking advantage of the SAM's flexible chemistry and more specifically the type of the chemical SAM end-group employed.

Overall, the work described in this thesis represents a significant step towards flexible carbon-based electronics where large-volume and low-temperature processing are required.

Contents

List of publications

Journal articles

1. Cecilia Mattevi, Florian Colléaux, HoKwon Kim, Yen-Hung Lin, Kyung T. Park, Manish Chhowalla and Thomas D. Anthopoulos. Solution-processable organic dielectrics for graphene electronics. Nanotechnology, 23 (34):344017, 2012.

2. Florian Colleaux and James M. Ball and Paul H. Wobkenberg and Peter J. Hotchkiss and Seth R. Marder and Thomas D. Anthopoulos. Bias-stress effects in organic field-effect transistors based on self-assembled monolayer nanodielectrics. *Physical Chemistry Chemical Physics*, 13(32):14387-14393, 2011.

3. Mohammed Al-Hashimi, Mohammed A. Baklar, Florian Colléaux, Scott E. Watkins, Thomas D. Anthopoulos, Natalie Stingelin and Martin Heeney. Synthesis, Characterization, and Field Effect Transistor Properties of Regioregular Poly(3-alkyl-2,5-selenylenevinylene). *Macromolecules*, 44(13):5194-5199, 2011.

4. James Ball, Paul H. Wöbkenberg, Florian Colléaux, Floris B. Kooistra, Jan C. Hummelen, Donald D.C. Bradley and Thomas D. Anthopoulos. Solution processed self-assembled monolayer gate dielectrics for low-voltage organic transistors. *Materials Research Society*, 1114, 2008.

5. James M. Ball, Paul H. Wöbkenberg, Florian Colléaux, Martin Heeney, John E. Anthony, Iain McCulloch, Donal D.C. Bradley and Thomas D. Anthopoulos. Solution processed low-voltage organic transistors and complementary inverters. *Applied Physics Letters*, 95(10):103310, 2009.

Conference presentations

1. Florian Colléaux, James Ball, Paul H. Wöbkenberg, Donal D.C. Bradley, and Thomas D. Anthopoulos. Threshold Voltage Instabilities in Low-Voltage Organic Transistors (talk). *Materials Research Society Fall Meeting*, Boston, USA, 2009.

2. Florian Colléaux, James Ball, Paul H. Wöbkenberg, Donal D.C. Bradley, and Thomas D. Anthopoulos. Electrical Stability of Organic Field-Effect Transistors based on Self-Assembled Monolayers (poster). *Society for Information Display*, London, UK, 2010.

3. Florian Colléaux, Jeremy Smith, Donal D.C. Bradley, and Thomas D. Anthopoulos. Novel fluoropolymer gate dielectrics for organic transistor applications (poster). *European Materials Research Society Spring Meeting*, Nice, France, 2011.

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As physics matters in sport, nothing is better than to carry on after work our experimental skills and quantify our energy level by playing squash with tipsy ginger mate (his name is kept secret for health and safety issues), humble Huang with his sly passing shots and Alex with his terrific backend. After experiencing four years of one day weather, I have learnt that, when it is tipping with rain on a stormy day, nothing is better than to keep going for a long run in the parks. For these, I am grateful to Hyde Park Relay Committee, XC Society for introducing to the events and all for the happy running. Nothing is better than playing some fantastic football. To these, I want to switch on, to keep in and chambrê the 5 a side football squad: Antonio, Warren, Sam, James, Stuart, Will, Peach, Jez, Liam, Rob. Nothing is more surprising than developing a mechanical wave on a ski lift. For that, i am grateful to Nathalie and Sophie for organizing the ski school. Finally following one of my office mate, I write, at the end of the day, giving a description of nature, banters and random debates, this what physics is all about !??!!!! and on and on and on. To all the people a massive thanks for the living science.

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Chapter 1

Introduction

1.1 Motivations and Applications

Invented 65 years ago, the transistor is a key building block of today's digital world. Invisible to the naked eye, transistors are virtually everywhere; they can be found in many devices from computers, tablets and mobile phones to automotive systems, household appliances and credit cards. Although today's integrated circuits contain several million transistors, if not few billions for the most advanced microprocessors, they don't cost more than a dollar per square millimetre. This has been possible only thanks to the fast pacing and constant development of the semiconductor industry. In 1965, Intel co-founder Gordon Moore predicted that the number of transistors on a chip would double about every 18 months. Since then, the number of transistors integrated into microprocessors has increased exponentially offering greater performance and energy efficiency. As Moore's Law continues to hold true today, microprocessors become even more highly integrated and computationally powerful with billions of calculation every seconds. Today the metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used device in digital electronics for microprocessors or memories and in analogue electronics for amplification as a power device. The association of single-crystal silicon and thermally grown silicon dioxide is still the most widespread combination of materials used in commercial applications. Scaling down of microelectronic devices goes on. The manufacturing technology is now 32 nm while the research focuses already on 22 nm and even smaller technologies. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the strategic document for the semiconductor industry, the conventional Si-based technology is, however, expected to encounter fundamental limitations at the spacial scale below 10 nm, thus calling for novel materials that could substitute or complement silicon. Possible candidates for the next generation electronics are carbon based materials: organic semiconductors, carbon nanotube and graphene.

For the past 30 years, organic materials such as polymers and small molecules have emerged as a practicable and economically viable technology for large area flexible

optical displays, low-cost low-end electronic circuits such as printable radio-frequency identification tags, and chemical sensors. Since the discovery of the conducting [2] and electroluminescent [3] properties of carbon-based molecules, organic semiconductors have been the subject of intense research and great progress has been made in the area of solar cells (OSCs) [4, 5], light emitting diodes (OLEDs) [6, 7, 8] and thin-film transistors (OTFTs) [9, 10, 11]. Already demonstrated in prototypes and manufactured in small portable devices such as mobile phones and digital cameras, this attractive technology is about to be widely commercialized in large-area OLED optical displays and flexible plastic e-readers. For example, Samsung announced the release of the first 55 inches super OLED TV set for the end of this year. And other innovative applications are yet to come on the market.

In terms of performance, organic semiconductors do not attempt to compete with inorganic single-crystal materials for high current driven or high frequency applications, such as microprocessors, which requires extremely high charge carrier mobility. Today the field-effect mobility of organic transistors is comparable to amorphous silicon (a-Si), which is still the most used semiconductor in commercial flat-panel displays. In order to be competitive, organic transistors should provide with the same performance and reliability, at a reduced cost and/or with easier fabrication techniques. Field-effect mobility values greater than 1 cm^2/Vs have already been achieved with not only evaporated semiconductors [12, 13] but also solution-processed semiconductors [14, 15]. The demonstration of such mobility for both type of carriers, hole and electron, opens up the possibility for complementary logic applications [16, 17] since integration of both p and n type conduction are necessary for logic circuits.

Organic semiconductors are an alternative solution to silicon for electronic applications that require low-cost manufacturing, large-area coverage, mechanical flexibility and low temperature processing. Easily processed from solution using techniques such as as inkjet printing, gravure printing or spray coating, organic semiconductors offer the possibility of large scale fabrication at a much lower cost than inorganic materials [9]. As only low temperatures are necessary to anneal the film and remove the solvent, the semiconductor film can be deposited on a wide variety of substrates including flexible plastic substrates. This contrasts with the Si based technology, which requires lithographic patterning techniques and high vacuum high temperature processes, thus increasing considerably the cost of manufacturing. Moreover the electrical and optical properties of organic semiconductors can be finely tuned by adjusting their chemical structure. For example it is possible to alter the emission wavelength in OLEDs, maximise the orbital overlap to improve the charge carrier mobility or change surface energies to enhance solution processability.

Current research in the field of organic electronics focuses on increasing charge carrier mobility, tuning optical properties, and improving processability of semiconductor films. Understanding of the microstructural properties and control of the morphology in organic thin-films are crucial to further improve individual device and overall integrated circuit performances. For further developments in thin-film tran-

sistor applications, several critical issues including environmental stability, charge trapping at the interfaces, device reliability and device-to-device variability needs to be addressed. Reduction of the device operating voltage and power consumption in organic circuits are also crucial for successful implementation of the technology in portable battery-powered applications. Given the critical role of the gate dielectric for the device performance, much efforts are also dedicated to the development of new dielectrics that are compatible with low temperature processing and flexible applications. Understanding the charge transport at the interface and control of the threshold voltage in devices are of paramount importance to design electronic circuits and improve their reliability. Several of these issues will be discussed in this thesis.

Graphene is a promising material for the next generation technologies in both logic and radiofrequency applications. It continues to attract tremendous interest because of its remarkable optical and electronics properties, such as high mobility, optical transparency, mechanical robustness, environmental stability and flexibility [18, 19]. Graphene is a unique two dimensional material, consisting of a single layer of carbon atoms arranged in a hexagonal structure. This bidimensional material has a distinctive band structure with a zero bandgap and cone-shaped valence and conduction bands. Its specific charge transport, which is characteristic of massless Dirac fermions, make it a potential material for nanoelectronic, especially for high-frequency applications. The low sheet resistance and high transparency make graphene an ideal candidate for optoelectronic applications [20] such as displays [21], touch screens [22], solar cells [23], photodetectors [24, 25], frequency converters [26], and smart windows. In light-emitting diodes, it can be used as the transparent anode electrode in replacement of the traditional indium-tin oxide material. Besides cost issues, ITO is brittle and limited as a flexible substrate whereas, graphene exhibit the same performance with respect to conductivity, work function, and transparency while providing better operational lifetime and flexibility at a much lower cost. In photodetectors, graphene offers a much broader spectral bandwidth and faster response. Graphene can fulfill multiple functions in photovoltaic devices as the transparent conductor, photoactive material, or catalyst.

According to the ITRS [1], graphene is considered as a promising candidate for post-silicon electronics, as it combines high electron mobility and atomic thickness. Graphene is technologically interesting as it offers the possibility of reduced power consumption and enhanced performance in field-effect transistors. Electric field-effect was observed for the first time in October 2004 by the group in Manchester [27]. The sample was produced by mechanical exfoliation of graphite. This technique still produce the highest quality films in terms of purity, defects and mobility [18]. Several approaches including chemical vapor deposition (CVD) [28], liquid-phase exfoliation (LPE) [29], and carbon segregation from silicon carbide (SiC) [30] have been developed for large-area deposition. CVD deposition of graphene on polycrystalline Ni films or Cu foils is certainly one of the more viable and practical approach for large-area high-throughput applications.

The performance of graphene transistors overcome those of silicon-based MOSFETs. One of the main advantage of graphene is its high carrier mobility. Mobility of 10000-70000 cm^2/Vs are frequently reported for exfoliated graphene [31, 32]. Large-area CVD-grown graphene exhibit mobility as high as 16 000 cm^2/Vs for CVD graphene [33]. And there is still more room for progress as mobility up to 10^6 cm^2/Vs is reported for suspended graphene [34]. Although the low on-off ratio demonstrated so far hamper their use in logic devices, graphene transistors hold great potential for radio-frequency devices, as they benefit from high carrier mobility and switch-off is not required. A cut-off frequency as high as 150 GHz was reported with a 40 nm gate graphene transistors [35], exceeding the performance of the best silicon MOSFETs (f_T ~ 40-50 GHz with similar gate length). However the radiofrequency performance of graphene are limited by the absence of saturation and the contact resistance. Finally integrated circuits with graphene interconnects can also be envisioned. With current density greater than 10^8 A/cm^2 [36] and thermal conductivity of 50 W $cm^{-1}K^{-1}$ [37], graphene overcomes the performance of copper.

Current research in the area of graphene focuses on developing deposition techniques for large areas with controlled grain size, thickness, and orientation. Characterization techniques to control the thickness and purity of graphene over these large areas are also required [38]. Graphene could be made electroluminescent by opening a bandgap. The latter can be created by cutting graphene into nanoribbons [39, 40], apply a back gate bias to a bilayer graphene [41], plasma O_2 treatment [42], hydrogen surface treatment [43] or through particular interactions with the substrates *[44]*. Development of flexible substrates and gate dielectrics with high quality passivated interface are necessary to further improve the device performance and reduce the operating voltage in graphene TFTs. Finally further developments in logic applications require the integration of p-type and n-type material through the doping of the channel region. Emergence of viable techniques to overcome these issues will make graphene a serious candidate for the next generations of optoelectronic applications.

1.2 Thesis Outline

In this thesis, we report the fabrication of high performance solution processed organic and graphene transistors employing unconventional organic gate dielectrics that can be processed at temperatures below 150°C. The role of the gate dielectric in high performance organic field-effect transistors (OFETs) is as important as the semiconductor itself, since it affects both the morphology of the semiconductor and the charge carrier transport at the semiconductor-dielectric interface [45]. The dielectric materials investigated in this work are a fluoropolymer thin-film and various organic self-assembled monolayer (SAM) nanodielectrics. Charge transport in organic thin-film transistors based on these gate dielectrics are explored through the study of their electrical characteristics, device performance, surface properties, and thin-film morphology. Several issues encountered in OFETs related to device reliability, charge

trapping at interfaces, contact resistance and environmental stability are discussed. Fabrication of devices and simple circuits using these gate dielectrics and high performance semiconductors, that can also be processed from solution, are demonstrated to show their potential for portable and large-area applications.

Chapter 2 reviews the charge transport in state-of-the-art materials (relevant to our study), the device physics, while chapter 3 will give an overview of the different fabrication, processing and characterization techniques used to carry out this work.

Following, chapter 4 reports on the use of a novel amorphous fluoropolymer with a low-k, namely Hyflon AD (SOLVAY), as the gate dielectric in organic transistors. Our surface and electrical measurements show that this transparent highly water-repellent insulating polymer is an ideal candidate as gate dielectric for use in organic transistors and potentially inorganic and/or hybrid electronics. Hyflon AD has the advantage of being orthogonal to most organic solvents, therefore it can be easily implemented from solution-based deposition techniques in low-cost organic field-effect transistors. High-performance transistors with hole mobility greater than 1 cm^2/Vs are reported. When used as gate dielectric it yields high performance transistors with excellent operating stability. Tested in different TFTs architecture, the performance and reliability of Hyflon-based OTFTs are comparable, if not better, than those obtained with the widely used Cytop fluoropolymer. Doping effects in organic semiconductor film is also investigated employing small molecular complexes as the dopant compound.

To date the majority of organic transistors operate at high operating voltage, typically 40-80 Volts, resulting in high power consumption. This is problematic especially in battery-powered applications, where low power dissipation is required. Therefore reduction in the operating voltage is crucial for the implementation of the technology in portable devices. Lowering the operating voltage while keeping a high output current can be achieved by using high-k dielectrics as the gate insulator or through the use of ultra-thin gate dielectrics. Our approach, as described in chapter 5, towards low-voltage organic circuits is the use of ultra-thin self-assembled monolayer (SAM) gate dielectrics [46, 47]. The latter are composed of densely packed organic molecular monolayers that suppress carrier tunneling thanks to highly ordered aliphatic chains. Despite the fact that they are only few nanometers thick (2-5 nm), optimized SAMs can be highly insulating with low leakage current densities (10^{-7}- 10^{-8} A/cm^2) and yield high geometrical capacitance ($C = 500\ nF - 1\ \mu F$). Use of such SAMs enables reduction of the transistor operating voltages to below 2 Volts. High-performance transistors with mobility greater than unity are reported using these nanodielectrics. Bias stress-induced threshold voltage shift and electrical behaviour as a function of temperature were investigated to determine the different origin of charge trapping in these devices. This approach offers the possibility to tune the threshold voltage by chemical tailoring of the SAM molecules. Demonstration of both p-type and n-type, and even ambipolar, low-power transistors and basic circuits such as inverters is important to show their potential for complementary logic circuits [48].

Flexible displays, radio-frequency identification tags and large-surface sensor net-

works are example of some macro-electronic devices that would benefit from the use of high mobility graphene as the channel material. The chemical vapour deposition (CVD) of graphene on copper provides high quality material over large areas that can be readily transferred onto a variety of substrates and implemented into devices [28]. The choice of the substrate is of paramount importance to optimize the device performance of graphene transistors. Up till now conventional inorganic dielectrics such as SiO_2, HfO_2, Al_2O_3 have been used in majority of graphene-based devices. However these dielectrics have shown undesired effects like unintentional doping, carrier mobility degradation, Dirac voltage hysteresis and shift [31, 49]. Besides in air ambient atmosphere, a strong hole doping behavior is observed due to absorption of water on the graphene layer. This leads to electrical instabilities of the device. In order to reduce these undesired effects and instabilities, graphene/dielectric interface engineering with suitable polymer layers [50, 51] or self-assembled monolayer [52, 53, 54] can be considered as a promising solution, as it is explained in chapter 6.

In our work reported in chapter 6, CVD graphene is processed from solution onto Hyflon gate dielectric, the amorphous fluoropolymer studied in chapter 4, as well as onto various self-assembled monolayer (SAM) nanodielectrics functionalized directly onto the gate electrodes, similarly to what was done for organic semiconductors in chapter 5. In the first case, due to its highly repellent properties, the interface engineering of Hyflon polymer in graphene transistors leads to improved performance as compared to bare SiO_2 based devices. Hysteresis-free ambipolar characteristics with carrier mobility up to 1400 cm^2/Vs are observed. Measurements in air over several weeks show also better environmental stability. Imaging of the film morphology allow to understand the charge trapping mechanisms that can occur at the interface. This study shows that interface engineering with a polymer is a suitable approach for high-performance large-area flexible electronics.

Although the use of lightweight substrates and flexible active materials are useful towards making large area electronics technology portable, it is also necessary to develop devices that provide minimal power dissipation that can be powered by small batteries or by near-field radio-frequency coupling. With that prospect, our graphene transistors based on SAM nanodielectrics have the significant advantages of operating at ultra-low voltages ($<|1.5|$ V) and exhibiting highly controllable doping characteristics. The improved transistor performance is attributed to the very thin nature of the highly compatible interface formed between the graphene and the organic monolayer dielectrics. These CVD graphene transistors exhibit hole and electron mobility as high as 600 cm^2/Vs and 300 cm^2/Vs, respectively. A number of phosphonic acid SAM molecules have been employed as dielectrics and the influence of their terminal group as dopant on the graphene layer is discussed. The simplicity, the low-temperature processing and the scalability of this approach pave the way towards flexible graphene electronics as well as providing a simple method for controlling the graphene/dielectric interactions at the nanometre scale.

Chapter 2

Background

Organic materials have attracted tremendous interests over the last decade for large area flexible applications. This chapter will review the recent progress that has been made in the development of organic materials in transistors, differentiating electron, hole and ambipolar transporting materials. Their properties, advantages and disadvantages of each material will be discussed. Given the importance of the gate dielectrics in device performance, the insulating properties of different dielectrics and their influence on the charge transport are reviewed. The main requirements that are discussed for TFT applications include low leakage current, high capacitance, high dielectric strength, easy processability, good chemical and thermal stability, and minimized trap state density. While results for inorganic dielectrics will be presented, more emphasis will be given to polymer dielectrics and self-assembled monolayer dielectrics.

Compared to inorganic materials, organic semiconductors are characterized by a more disordered structure and weak intermolecular interactions, implying that the conduction mechanisms that occur in organic semiconductors may be different. The charge transport in organic semiconductors is strongly related to the molecular order of films. In amorphous organic films, the charge transport is explained by hopping of carriers between localized states whereas, in highly ordered molecular films, the charge transport is described as activation of carriers from localized states to a transport level. In a second section, several charge transport models will be discussed.

Graphene is considered as an ideal candidates for post silicon electronics because of its high mobility and the possibility of scaling to shorter channel lengths and higher speeds without encountering the issues related to short-channel effects. Among the numerous advantages offered by graphene are: transparency, flexibility, robustness, and environmental stability. We will review the electronic properties of graphene that are relevant to electronic devices, the different fabrication techniques used to grow and transfer graphene and the current state-of-the-art in terms of transistor performance. A great deal will focus on the surface treatments employed to improve the performance of graphene transistors.

Finally, despite having different charge transport mechanisms than their inorganic counterparts, organic transistor operation can be described by the same thin-film transistor models. After depicting the four possible transistor architectures that can be fabricated and their attributes, the different operating regimes of a field-effect transistor will be described. Having derived the current-voltage characteristics of a transistor, we will explicate how the different device parameter are extracted and their physical meaning. Lastly we will explain the operation of inverters and ring oscillators following the design rules of both unipolar and complementary logic. Fabrication of simple electronic building blocks represents the first step towards the development of electronic circuits.

2.1 Organic materials in field-effect transistors

2.1.1 Organic semiconductors

Organic semiconductors are envisioned as an alternative solution to more traditional inorganic materials because of their unique processing characteristics. Despite the great progress that has been achieved over the last ten years, the mobility of organic semiconductors are not likely to match those of inorganic single-crystals such as Si, Ge, and GaAs, which have charge carrier mobility of three orders of magnitude higher. However the field-effect mobility of organic transistors is comparable to, if not greater than, the value of 1 cm^2/Vs observed in amorphous silicon (a-Si), which is still the most used semiconductor in commercial flat-panel displays. Both hole and electron mobility up to 10 cm^2/Vs have already been reported from not only vacuum-sublimed organic materials but also solution-processed semiconductors, allowing their implementation in complementary logic applications. Much of the current research focuses on solution-processed organic materials since the latter offer easier fabrication techniques at reduced costs for large area electronic applications.

2.1.1.1 Hole transporting organic semiconductors

Hole transporting organic field-effect transistors (p-channel) can be made of either small conjugated molecules or polymers. Compared to polymers, small molecules show higher degree of crystallinity, hence higher mobilities. However small molecules, often deposited by vacuum sublimation, are not as easy processed from solutions as polymers. Here we summarize some of the most important classes of small conjugated molecules and polymers that have been used as hole transporting materials in field-effect transistors. Their molecular structures are shown in figure 2.1.

The first OFET made with a small conjugated molecules was reported by Horowitz et al. employing α-sexithiophene molecules [11]. A hole mobility of $10^{-3}cm^2/Vs$ was measured in air. Oligothiophene molecules can be either non-substituted or alkyl-substituted at both ends. Dimethyl- and dihexyl- substituted oligothiophenes showed high ordered films, resulting in significant increase of the mobility. Mobilities up to

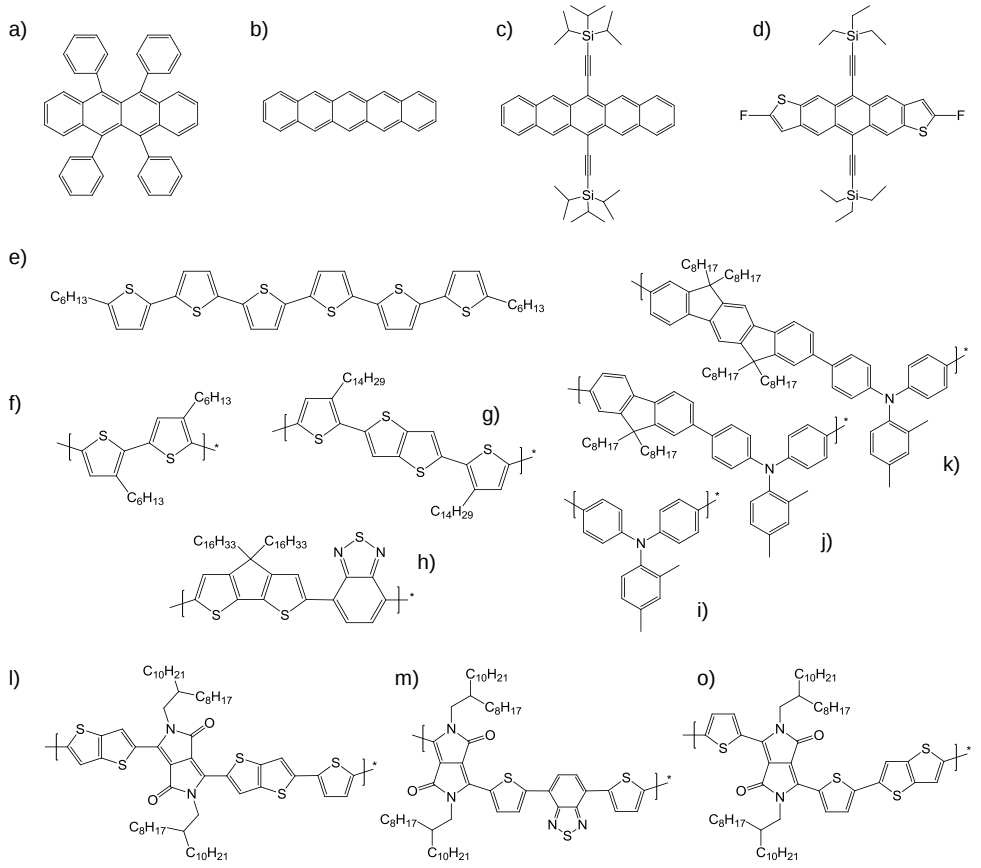

Figure 2.1: Chemical structures of some hole p-type organic semiconductors: rubrene (a), pentacene (b), bis-(triisopropylsilylethynyl)-pentacene (TIPS-pentacene) (c), 2,8-difluoro 5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) (d), $\alpha,\omega-$dihexyl-hexathienylene (DH6T) (e), regioregular poly(3-hexyl thiophene) (P3HT) (f), poly(2,5-bis(3-alkylthiophene-2-yl) thieno[3,2-b]thiophene) (PBTTT) (g), cyclopentadithiophene-co-benzothiadiazole (CDT-BTZ) (h), poly(dimethyl triarylamine) (PTAA) (i), poly(dioctyl fluorene-co-dimethyl triaryl amine) (PFTAA) (j), poly(dioctyl indenofluorene-co-dimethyl triaryl amine) (PIFTAA) (k), 2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-thiophene-co-thieno[3,2-b]thiophene (DPPT-TT) (l), 2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-co-thiophene-benzothiadiazole-thiophene (DPP-TBT) (m), 2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-1,4-(2H,5H)-dione-co-3,6-bis(thieno[3,2-b]thiophene) (DPP-TT) (n).

0.13 cm^2/Vs were obtained for molecular beam deposited α,ω-dihexyl-hexathienylene (DH6T) [55]. The mobility in oligothiophenes was observed to be independent of the length of the structure (from 4T to 8T) and the presence or absence of alkyl end substitution [56].

Pentacene and rubrene small molecules are certainly among the most well-know and widely studied p-type organic semiconductors. High single crystal hole mobility of 6 and 20 cm^2/Vs were reported, respectively [57, 13]. Pentacene, whose molecular structure is shown on figure 2.1, is a polycyclic aromatic hydrocarbon consisting of five aligned fused benzene rings. Pentacene small molecules are de-

posited by vacuum-sublimation, since the molecule is not soluble, and yield to highly ordered microstructures [58, 59]. High hole mobilities up to 5-6 cm^2/Vs were observed using an alumina dielectric treated with a self-assembled monolayer [59] or with a poly(α-methyl styrene) polymer layer [57]. Despite the high-performance, solution-processing pentacene is not possible. To solve this processing issue, an alternative approach is to use soluble pentacene precursor [60, 61]. The precursor can be spin-coated on the substrate before being thermally converted into pentacene. Hole mobility of 0.02 cm^2/Vs was measured in devices based on precursor molecules, which is much lower than values obtained in vacuum-sublimed thin-films. Functionalisation of pentacene with side groups has also proved to be a successful solution to increase the solubility. A solution-processed pentacene derivatives, such as bis-(triisopropylsilylethynyl)-pentacene (TIPS-pentacene), showed a good π-stacked structure and exhibited a hole mobility as high as 1 cm^2/Vs [62, 63]. Similarly using a functionalized anthradithiophene, 2,8-difluoro 5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT), solution-processed TFTs with a hole mobility of 1.5 cm^2/Vs were demonstrated employing gold electrode treated with pentafluorobenzenethiol (PFBT) SAM [64]. Grown as single crystal from the vapor phase, diF-TESADT transistors exhibited high performances with an intrinsic hole mobility up to 6 cm^2/Vs and a current on/off ratio of 10^8 [65].

On the other hand, amorphous p-type polymers are more easily processed from solutions than small molecules and present less defects in the bulk and at the interface than polycrystalline films. Amorphous polymers, such as polyacetylene and polythiophene, usually lead to disordered films and low field-effect mobilities in the range of 10^{-5}-10^{-3} cm^2/Vs. A class of amorphous triarylamine polymers have attracted much attention due to their good hole mobility, uniform and smooth (<1 nm) film formation from solution and excellent stability in air. A hole mobility of 0.004 cm^2/Vs was obtained for poly(dimethyl triaryl amine) (PTAA, figure 2.1) TFTs [45]. Addition of a fluorene or indenofluorene unit to the polymer structure was found lead to a significant improvement of hole mobility and current on/off ratio (by two orders of magnitude). Mobility of 0.02 cm^2/Vs and 0.04 cm^2/Vs were measured in poly(dioctyl fluorene-co-dimethyl triaryl amine) (PF-TAA) and poly(dioctyl indenofluorene-co-dimethyl triaryl amine) (PIF-TAA) thin-films. This mobility enhancement was attributed to the improved intermolecular π-orbital overlap and structural ordering resulting from the additional planar conjugated units while the triarylamine unit maintain the air stability and amorphous microstructure. Combining acene molecules with these amorphous polymers, Smith et al. demonstrated high hole mobility in top-gate transistors [66, 67, 68, 69]. This was explained by accumulation of the small molecules at the top interface due to the vertical phase separation that occurs in the blends during film formation. Blending TIPS-pentacene and diF-TESADT small molecules with the amorphous PTAA polymer yielded hole mobilities of 1.1 cm^2/Vs and 2.4 cm^2/Vs, respectively [66]. When substituting the PTAA polymer matrix by PF-TAA or PIF-TAA polymers (with higher mobility in single component devices), mobility as high

as 4.6 and 2.6 cm^2/Vs, respectively were reported for diF-TESADT:polymer blend devices [14]. This approach associates the high mobility of small molecules and the processability of polymers. When using highly crystalline polymers as polymer matrix in blends, crystallization of acenes molecules is inhibited and no vertical phase separation occurs, resulting in mobilities equal or lower to the values obtained with the polymer itself.

For single component polymers, higher mobilities were achieved with polymers showing a higher degree of crystallinity. Mobility up to 0.1 cm^2/Vs was reported in semi-crystalline regioregular poly(3-hexyl thiophene) (RR-P3HT) polymer thin films [70, 71]. High regioregularity of the material leads to improved molecular ordering and thus higher crystallinity. Processing conditions (high boiling point solvent) and molecular weight of the polymer were observed to play also an important role in device performances. The mobility increases with increasing molecular weight. This is ascribed to an increase of the conjugation length and reduction of the chain end effects. However, with a low ionization potential of 4.8 eV, P3HT films are sensitive to oxygen and show poor device performance in ambient atmosphere. In the same class of materials, poly(2,5-bis(3-alkylthiophene-2-yl) thieno[3,2-b]thiophene) (PBTTT) exhibit a highly organized microstructure with interdigitation of the alkyl side chains upon annealing from a liquid-crystal phase. High charge carrier mobility, equivalent to amorphous silicon (1 cm^2/Vs), were obtained from this polymer. In comparison with P3HT, PBTTT thin-films are environmentally stable in air over several days due to a high ionization potential (of 5.2 eV). High crystallinity and good hole transport was also reported in cyclopentadithiophene-benzothiadiazole copolymer (CDT-BTZ) thin films [72]. Hole mobility up to 1.4 cm^2/Vs was observed by dip-coating the copolymer [73]. This processing method was used to improve the long-range order and thus obtain high mobility. However CDT-BTZ thin-films are not really stable in air. After exposure to ambient atmosphere, the current on/off ratio is reduced by three orders of magnitude, probably due to doping of the film through oxidation and the mobility is reduced to half its initial value after 2 days.

Recently a group of copolymers based on diketopyrrolopyrrole (DPP) unit have shown great promise as p-type material [74, 75, 76]. These single-component polymers are solution-processable, air stable and presents a low-bandgap (possibility for ambipolar transport). For this copolymers, DPP is used a core building block which acts as a strong electron accepting moiety. DPP can be easily connected to various donor moiety blocks at the 2- and 5- position of the DPP moiety. Alkyl chains can be added to the lactam N atoms to improve the solubility of the polymer. The strong $\pi - \pi$ intermolecular interactions between molecules result in high order molecular organization and high hole mobility. Combining the DPP moiety with the thiophene-benzothiadiazole-thiophene building block, forming a copolymer with a DPP-TBT repeat unit (shown on figure 2.1), a mobility value of 0.35 cm^2/Vs was reported in TFTs based on OTS SAM treated SiO_2 dielectric (after annealing at 200°C) [74]. Electron transport was also observed for this copolymer. Using a similar FET struc-

ture, Li et al. reported after annealing at 200°C a hole mobility approaching 1 cm^2/Vs in DPP–thiophene polymer (DPPT–TT) thin films [76]. The repeat unit, shown on figure 2.1, was composed of alternating (DPP) thieno[3,2-b]thiophene TT and two thiophene moieties. Copolymerization with thieno[3,2-b]thiophene resulted in DPP–TT with a rare mobility of 1.94 cm^2/Vs [75], the highest mobility reported to date for a single-component polymer-based FET.

2.1.1.2 Electron transporting organic semiconductors

For n-channel transistors, the current in the channel is attributed to the conduction of electrons that are injected from the electrodes to the LUMO level of the semiconductor. The main challenges for n-channel transistors are the injection of carriers, due to the high injection barrier between the work function of electrodes and the LUMO level, and the reactivity to water and oxygen in ambient conditions. For the development of new transporting materials, different characteristics are taken into account: high mobility, ease of synthesis, ease of processing and stability under ambient and operational conditions. Electron transporting, also called n-type, materials must be electron deficient. Materials with a low-energy LUMO are readily reduced and thus favor charge injection at the electrodes. They are also more stable to oxygen and water. Their ambient stability can be improved by attaching strong electron withdrawing group, e.g. fluoroalkyl, cyano, diimide, carbonyl groups, which lower the LUMO level of a system. To get high mobility, a strong electronic coupling, in space and phase [77], between the π-systems on adjacent molecules is necessary. Three classes of molecules have a high electron affinity and were shown to yield good n-channel transistors: fullerenes, acenes and rylene diimides. The molecular structures of some n-type materials are shown on figure 2.2.

Fullerenes and their derivatives have attracted much attention as n-type material since the discovery of the fullerene C_{60} that far in 1985. They have high electron affinity and yield n-channel transistors with very high electron mobility. However they degrade rapidly upon exposure to ambient air [78]. Fullerenes are hollow spherical molecules composed entirely of carbon atoms. In the first report of a C_{60} transistor, Haddon et al. had observed an electron mobility of $8 \cdot 10^{-2}$ cm^2/Vs by vacuum-sublimation of the semiconductor film on a bottom gate Si/SiO_2 substrate and using bottom contact gold electrodes [79]. A high electron mobility of 6 cm^2/Vs was obtained by hot wall epitaxy (at 250°C) of C_{60}on a crosslinked divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) gate dielectric [12]. Top contact low work function LiF/Al electrodes were evaporated to ensure good electron injection. The mobility was observed to depend significantly on the temperature of the substrate during the growing process, as the grain size increases with increasing temperature. Mobility in the range of 2-5 cm^2/Vs also achieved by physical vapor deposition at room temperature on BCB layer on top of SiO_2 dielectric [80, 81] or by vacuum sublimation onto octadecyltrichlorosilane (OTS) monolayers [82]. In both cases,

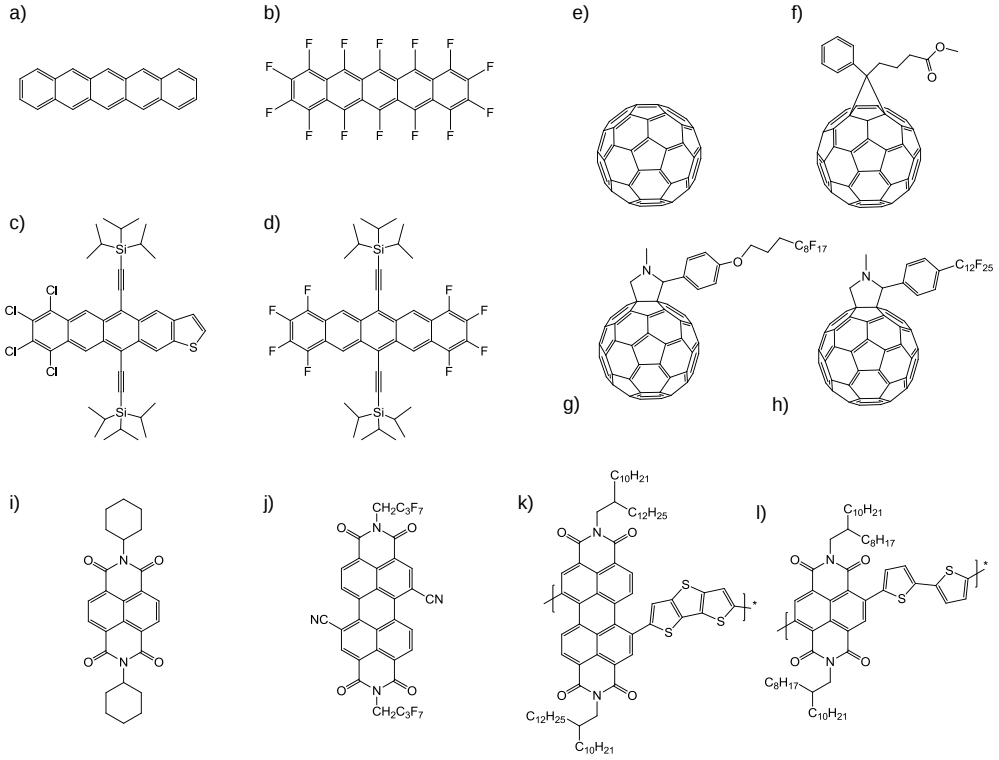

Figure 2.2: Chemical structure of some n-type semiconductors: pentacene (a), perfluoropentacene (b), 7,8,9,10- tetrachloro-5,12-bis(TIPSethynyl)tetraceno-[2,3-b]thiophene (tCl-TIPS-TC-T) (c), octafluoro-5,12-bis(TIPSethynyl)-pentacene (oF-TIPS-pentacene) (d), C_{60} fullerene (e), [6,6]-phenyl-C_{61}-butyric acid methyl ester ($PC_{61}BM$) (f), fullerene derivatives F17-DOPF (g)-(h), N,N´-bis(cyclohexyl) naphthalene-1,4,5,8-bis(dicarboximide) (i), N,N´-bis(n-octyl)-(1,7&1,6)-dicyanoperylene-3,4:9,10-bis(dicarboximide) (PDI-8CN_2) (j), N,N´-dialkyl-1,7-perylene-diimide-co-dithienothiophene (PDI-dTT) (k), and N,N´-dialkyl-1,7-naphtalene-diimide-co-dithiophene (NDI-dT) (l).

the thin layer of BCB or the self-assembled monolayer passivates the SiO_2dielectric from any electron traps, thus leading to higher carrier mobility. Recently, Li et al. demonstrated an electron mobility of 11 cm^2/Vs, the highest electron mobility for organic semiconductors, in well-aligned C_{60} needle shaped single-crystals prepared by simple droplet-pinned crystallization (DPC) [15]. According to this method, an organic semiconductor droplet is pinned by a silicon wafer; while drying, the crystals nucleate near the contact line of the droplet and grow along the receding directions. With in situ growth on cross-linked BCB-treated SiO_2 gate dielectric, crystals with length up to 200 μm (and thin $\sim 9\mu m$) were obtained guaranteeing excellent electrical contacts with electrodes. This single crystal deposition method has the major advantages of being solution-processable and scalable to large area substrate. Electron transport transistors was also reported with fullerenes with higher number of carbon atoms, such as C_{70} [83], C_{76} [84] and C_{84} [85]. In all cases the electron mobility was found to be lower than C_{60}. For example, a mobility of $7 \cdot 10^{-2}$ cm^2/Vs was

reported for gradient zone vacuum-sublimed C_{70} film [86]. The main disadvantages of unsubstituted fullerenes are their low availability, their need for high purification and low solubility in most common organic solvents.

To tune their electrical properties, fullerenes can be functionalized by an addition reaction of a side chain to one double bond of the fullerene. Two isomers can be formed from this reaction. [5,6] fulleroid derivatives are isoelectronic with their parent fullerene, but are rather thermally and photochemically unstable. For that reason, only few studies report the use of fulleroid derivatives in transistor [87]. On the other hand, [6,6] methanofullerene derivatives have two less delocalized electrons compared to their parent fullerene, resulting in a decrease of the electron accepting properties by 50-100 mV. A large number of these fullerene derivatives have shown a decent electron transport in transistors, with mobilities in the range of 10^{-3}-$10^{-1}$$cm^2$/Vs [88, 89, 90, 91, 92, 93, 94]. These fullerene derivatives are solution-processable, simplifying considerably the device fabrication. One of the first and maybe most well-known soluble fullerene derivative is [6,6]-phenyl-C_{61}-butyric acid methyl ester ($PC_{61}BM$). This material is synthesized by substituting a 4-phenyl butyric methyl ester group to the C_{60} ring via a bridging cyclopropane group. A very good electron mobility up to 0.21 cm^2/Vs, a threshold voltage of 7 V, a currrent on/off ratio of 10^4were observed in solution-processed methano fullerene PCBM transistors, using cross-linked BCB gate dielectric in combination with top contact Ca/Al electrodes [88]. Ambipolar transport behavior with hole and electron mobilities of $8 \cdot 10^{-3}$ and $1 \cdot 10^{-2}$ cm^2/Vs, respectively was also reported in $PC_{61}BM$ transistors employing Au electrodes [95]. The main drawback of PCBM (and other hydrogenated fullerene derivatives) is its (their) high sensitivity to oxygen and water, resulting in a drop of device performance once exposed to air. Inclusion of fluorine containing groups to fullerene was found to enhance electron mobility and stability under ambient conditions [96, 97]. An electron mobility of 0.25 cm^2/Vs was observed employing the solution-processable fluoroalkyl-substituted C_{60} derivative ($C_{60}PC_{12}F_{25}$). Its molecular structure is shown on figure 2.2. Transistors based on these fluorinated fullerene derivatives could be operated in air for several days. This stability was attributed to the water repellent property of the fluor atoms and high packing density of fluorine containing derivatives, that prevent diffusion of oxygen and water in the semiconductor film. Soluble derivatives of higher fullerenes can also be synthesized. Prepared as a mixture of three inseparable isomers, the C_{70} [88] and C_{84} [98] analog of $PC_{60}BM$ yield electron mobility of 0.1 and $5 \cdot 10^{-4}$ cm^2/Vs, respectively in FETs. Due to the higher electron affinity of C_{84} over C_{60}, devices based on $PC_{84}BM$ are stable in ambient atmosphere and can be operated over long period of time (a week) [98].

Acene small molecules are well-known as p-type semiconductors. However hole transport as well as electron transport should be observable in these materials since the dispersion is similar in both conduction and valence bands. In transistors, the main causes that limit electron transport in acene small molecules are charge injection into the LUMO level and charge trapping at the dielectric interface. These issues

can be addressed by selection of suitable dielectric materials, employing low work function electrodes, passivation of oxide dielectrics by deprotonation. For instance, electron transport was demonstrated in pentacene films using an inert PMMA dielectric and top-contact calcium electrodes, yielding electron mobility of 0.1 cm^2/Vs [99]. Devices with an electron mobility of 0.2 cm^2/Vs were reported in pentacene thin-films by passivating the silicon dioxide dielectric by an ultra-thin (0.6 nm) layer of calcium [100]. The calcium prevents the formation of trapping sites at the dielectric interface by reacting with the hydroxyl residues. Electron transport was also observed in single-crystal rubrene by passivating the SiO_2 dielectric with a thin PMMA layer (using a PMMA dielectric) and Ag paste electrodes [101]. These devices exhibited a saturation electron mobility of $1.1 \cdot 10^{-2}$ cm^2/Vs under vacuum. Perfluorination of acene molecules is considered as an attractive solution to improve the device stability. Indeed addition of electron-withdrawing fluorine stabilize the semiconductor anion without significantly changing the crystal packing of the material. This stabilization allow untreated oxide surface to be used as gate dielectric, thus simplifying considerably device fabrication. On untreated SiO_2dielectric, vacuum-sublimed perfluoropentacene transistors with an electron mobility of 0.05 cm^2/Vs were reported in vacuum [102]. The mobility can be increased up to 0.11 cm^2/Vs by treating the SiO_2 dielectric with an OTS SAM [103]. Complementary inverters with pentacene/fluoropentacene transistors were demonstrated with a gain of 57 (at 100 V) [104]. On a similar approach, the group of Zhenan Bao developped series of silylethyne acenes and silylethyne thienoacenes small molecules with electron-withdrawing halogen atoms [105, 106, 107, 108] and showed how the electrical transport in transistors can be changed by tuning the LUMO and HOMO levels of these materials. They found for example that materials with LUMO $<$ -3.15 eV and HOMO $<$ -5.6 eV exhibited only n-type transport in transistor applications [108]. In that case sufficiently low barrier injection for electrons and large barrier for hole injection enable electron transport. Tested with top-contact gold electrodes and on OTS-SAM treated SiO_2 dielectric, these halogenated acene small molecules yield electron mobility in the range of 0.1-0.6 cm^2/Vs, good current on/off ratio of 10^5-10^6 but high threshold voltages (50-70 V) [107, 105]. The highest electron mobility were reported for 7,8,9,10-tetrachloro-5,12-bis(TIPSethynyl)tetraceno-[2,3-b]thiophene (0.56 cm^2/Vs) and octafluoro-5,12-bis(TIPSethynyl)-pentacene: 0.41 cm^2/Vs small molecules [106], whose molecular structures are shown on figure 2.2.

Rylene diimides are synthesized by substituting an aromatic core with two sets of π-accepting imides groups. They have high electron affinities and excellent chemical, thermal and photochemical stabilities. Naphtalene diimide (NDI) and perylene diimide (PDI) small molecules yield n-channel transistors with very high electron mobility. Shuckla et al. reported an electron mobility of 6.2 cm^2/Vs in inert atmosphere for FET based on OTS-treated silicon dioxide dielectric using top-contact gold electrodes [109]. This is the highest mobility reported for NDIs. An electron mobility up to 6 and 3 cm^2/Vs in vacuum and in air, respectively, were also reported for pery-

lene diimide devices using poly(methyl methacrylate) (PMMA) as the gate dielectric and gold electrodes [110]. The best performances were obtained by depositing these rylene diimides small molecules by vacuum-evaporation. Alternatively Zhan et al. were the first to synthesize a soluble rylene-based fully conjugated polymer [111]. This PDI-dithienotiophene copolymer showed a saturation electron mobility of 1.10^{-2} cm^2/Vs . In these polymers the rylene core are bridged by other π-conjugating units, instead of linked through the imide groups. Besides these PDI polymers were highly unstable under ambient conditions. Far from it Fachetti and coworkers synthesized a NDI bithiophene co-polymer and demonstrated transistors with an electron mobility as high as 0.85 cm^2/Vs and an on/off ratio of 10^5 under ambient conditions [112].

2.1.1.3 Ambipolar organic semiconductors

Ambipolar semiconductors are materials that allow conduction of hole and electron under certain bias conditions. Ambipolar transistors are of great interest in applications such as complementary-like logic circuits [113, 114, 115, 116] and light-emitting field-effect transistors [117, 118]. To fabricate high-performance circuits high and well-balanced hole and electron mobility are required, since the mobility is the main limiting factor in the operating frequency of logic circuits. Explanations on the operation regimes and characteristics of ambipolar transistors are provided in section 2.4.2.3. Ambipolar transistors have been realized by three different approaches: bilayer transistors, blend transistors and single-component transistors.

The first approach to obtain ambipolar transistor is the fabrication of a bilayer structure composed of n-channel film and a p-channel film. To obtain a well-defined smooth bilayer structure, thin-films are very often deposited by vacuum sublimation [119, 120, 121, 122, 123]. Balanced hole and electron mobility values as high as 0.04 cm^2/Vs were reported in transistors based on vacuum-sublimed fluorinated copper phthalocyanines (FCuPc, electron transporting layer) and 2,5-bis(4-biphenylyl)-bithiophene (BP2T, hole transporting layer) [123]. Solution-processing is not the most suitable technique for bilayer structure since spin-coating the second layer from solution is difficult without dissolving the first one. Ambipolar transport was nonetheless demonstrated in solution-processed P3HT or PCBM bilayer structures either by inserting a TiO_x separating layer [124] or by contact transfer of the second layer [125].

For blend transistors, the p-type and n-type materials are blended and can be deposited as a single layer either by vacuum-sublimation or solution-processing techniques. For evaporated blend, among the system that result in ambipolar transport are α-quinquethiophene/PTCDI-$C_{13}H_{27}$ [126, 127], pentacene/PTCDI-$C_{13}H_{27}$ [128], pentacene/fluorinated pentacene [104]. Mobilities were found to be smaller than those for the pure material and depends on the relative fraction of each material component in the system [127]. Transistors based on solution-processed small molecule-polymer blend offer the attractive processing properties of polymers and simplifies the device fabrication. With only one layer to deposit, blend films are suitable for integrated

circuits. Ambipolar transport with hole and electron mobilities in the range of 10^{-5}-10^{-3} cm^2/Vs were reported with these blend films [129, 130, 131, 132]. The device performance with these blend films were observed to depend strongly on the nature of the dielectric and the morphology of the films.

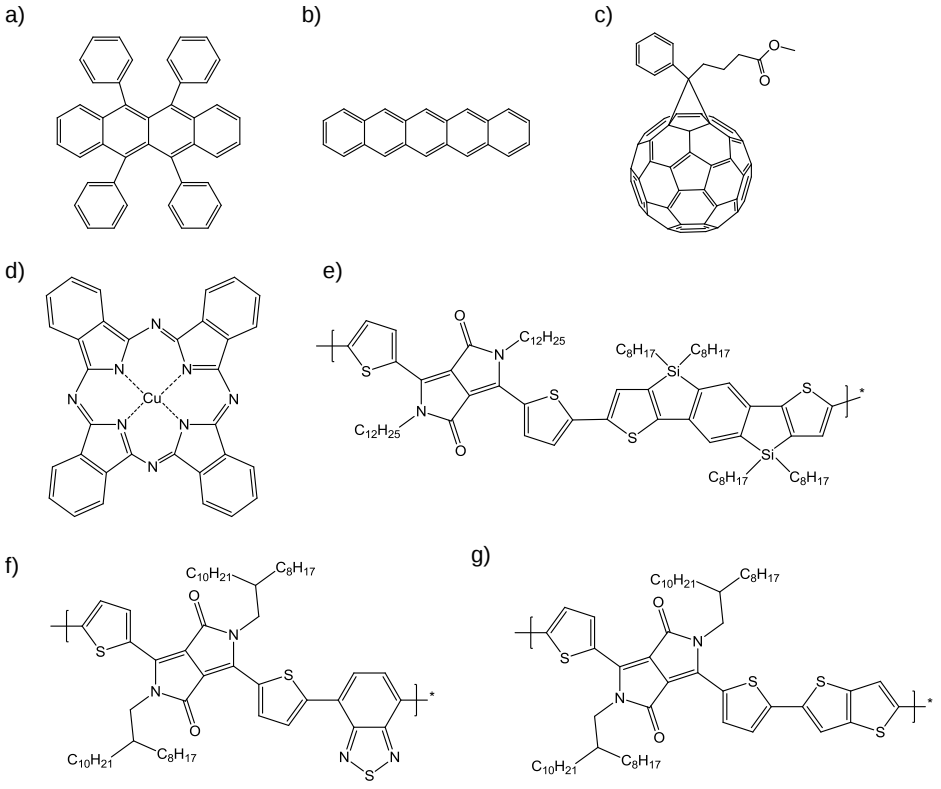

Figure 2.3: Chemical structure of single component ambipolar materials: rubrene (a), pentacene (b), $PC_{60}BM$ (c), copperphthalocyanine (d), 2,5-bis(dodecyl)pyrrolo[3,4-c]pyrrole-co-silaindacenodithiophene (e), 2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-thiophene-co-thieno[3,2-b]thiophene (DPPT-TT) (f), 2,5-bis(2-octyl-1-dodecyl)pyrrolo[3,4-c]pyrrole-co-thiophene-benzothiadiazole-thiophene (DPP-TBT) (g).

The last class of ambipolar materials is the single component ambipolar material. Contrary to the preceding two groups, where a p-type material and a n-type material are combined, either in a bilayer or in a blend, to achieve ambipolar transport, the following materials are intrinsically ambipolar (figure 2.3).

Transistors based on single-crystal material, like rubrene [133, 13] or pentacene [57], show extremely high hole mobility as high as 20 and 6 cm^2/Vs, respectively. Ambipolar transport can also be achieved in these crystals. For example, an electron mobility of 0.01 cm^2/Vs (compared to 1 cm^2/Vs for holes) was measured in vacuum for rubrene single crystal transistor using poly(methyl methacrylate) (PMMA) as a dielectric [101]. Despite depositing silver electrodes to improve the electron injection, high contact resistance was observed and could be one reason for the low electron mobility. Ambipolar behaviour was also demonstrated in pentacene films. High hole

and electron mobility of 0.5 cm^2/Vs and 0.2 cm^2/Vs, respectively were reported for pentacene films on poly(vinyl alcohol) (PVA) as gate dielectrics and with gold electrodes [134]. Ambipolar transport were also demonstrated in other single crystals, such as copper phthalocyanine (CuPc) and iron phthalocyanine (FePc) single crystals [135]. In all these single-crystal materials, the hole transport is dominant and the electron transport is observed by selecting a suitable dielectric that prevents charge trapping at the semiconductor-dielectric interface.

Well-known for their n-type transport, some fullerene derivatives can also show ambipolar characteristics [95, 136, 137]. The additional side chain attached to the fullerene acts as a π-electron donor and allow for hole transport. Balanced hole and electron mobility as high as 0.01 cm^2/Vs was reported for the solution-processable $PC_{60}BM$ on HMDS SAM treated SiO_2 dielectric and with gold electrodes [95, 113]. Complementary-like voltage inverter fabricated with two identical PCBM OFETs were demonstrated and exhibited a gain of 18. For PCBM small molecules, when the C_{60}fullerene is substituted with the C_{70} or C_{84} versions, the transistors are more stable in air [16].

Towards low-cost and flexible complementary logic circuits, transistors based on low-bandgap ambipolar polymers with symmetric electrodes are promising candidates since this strategy makes full use of the easy-processing and mechanical properties of polymers. In low-bandgap polymers, the ambipolar transport is determined by the position of the energy levels and particularly of the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), the device architecture, material processing (choice of dielectric and metal electrodes) and ambient conditions. To improve the charge carrier injection in ambipolar transistors, the energy levels of copolymers can be tuned by selecting appropriate donor-acceptor building blocks. Recently, a class of donor-acceptor (D-A) alternating copolymers based on diketopyrrolopyrrole (DPP) has attracted great interest due to their promising performances in TFTs [118, 74, 76, 75, 138, 139, 140]. Ambipolar transport was first demonstrated in these DPP-based copolymer by Burgi et al. using poly[3,6-bis-(4'-dodecyl-[2,2']bithiophenyl-5-yl)-2,5-bis-(2-hexyl-decyl)-2,5-dihydro-pyrrolo[3,4-c]pyrrole-1,4-dione]. Transistors based on this donor-acceptor copolymer film exhibited a hole and electron mobility of 0.1 cm^2/Vs [118]. Using different diketopyrrolopyrrole-based copolymers, ambipolar transport with a balanced hole and electron mobility on the order of 0.1 cm^2/Vs were also achieved [139, 138]. Combining the DPP moiety with the donor-acceptor-donor (D-A-D) thiophene-benzothiadiazole-thiophene (TBT) building block in the same polymer unit (DPP-TBT), ambipolar transport with a hole and electron mobility up to 0.35 cm^2/Vs and 0.4 cm^2/Vs were demonstrated in top-contact transistors using OTS treated SiO_2 dielectric and gold electrodes after annealing at 200°C [74]. The efficient ambipolar transport in these polymer films were explained to result from the formation of interconnected networks between domains of bundled nanofibers (with increasing annealing temperature). Li et al. had reported a hole mobility of 1 cm^2/Vs in TFTs based on DPPT-TT copolymer, composed of DPP,

two thiophene units and thieno[3,2-b]thiophene in the polymer unit [76]. However, at that time, insignificant electron transport was reported in this low-bandgap polymer (1.2 eV). This year high performance ambipolar OFETs exhibiting well-balanced hole and electron mobility up to 1.4 cm^2/Vs and 1.6 cm^2/Vs were demonstrated using the DPPT-TT copolymer and poly(methyl methacrylate) as a dielectric [140]. These are the best performance reported for ambipolar transistors to date. This was possible by optimisation of the device fabrication and material processing. A top-gate/bottom-contact device architecture was preferred to the bottom-gate/top contact electrodes used in the work by Li et al. To improve charge injection of electrons, the work function of the gold electrodes was reduced to 4.7-4.9 eV by solvent cleaning. A significant improvement of the transport was observed upon annealing the DPPT-TT films. This was attributed to a better crystallinity of the polymer film. The planar skeleton of the core DPP allows highly ordered films lying "edge-on" relative to their substrates. Combining two identical DPPT-TT transistors, inverters were demonstrated with a gain of 35.

2.1.2 Gate dielectrics in organic transistors

If much effort has been dedicated to develop high mobility, stable and solution-processable semiconductor materials for organic electronics, the organic semiconductor is not the only crucial component in OFETs. The gate dielectric plays also an important role in transistor operation. The gate dielectric insulates the conducting channel from the gate electrode and determines the amount of charges that can accumulate in the channel region for a given voltage through its capacitance effect ($Q_{channel} = C_I V_G$). Moreover the charge transport in a transistor depends strongly on the quality of the semiconductor-dielectric interface.

To date the majority of organic transistors operates at high voltages, often exceeding 20V. This leads to high power consumption in organic electronic circuits. However in battery powered mobile applications, low consumption and hence low operating voltage is required. Therefore reduction in the operating voltage of OFETs is a major motivation so as to implement this technology into portable devices. Lowering the operating voltage while keeping a high output drive current can be achieved by using a gate dielectric with a high capacitance. The geometric capacitance is given by: $C_I = \epsilon_r \epsilon_0 / t$, where ϵ_r and t are the permittivity and the thickness of the gate dielectric. Thus the operating voltage can be scaled down either by choosing an insulating material with a high permittivity or by decreasing the dielectric thickness.

To ensure a good transistor operation, the key requirements that the gate dielectric should satisfy are a high dielectric strength, a low roughness, a trap-free surface and absence of impurities and defects. When developing new dielectric materials for transistor applications, few other properties are sought, the gate dielectrics should be low-cost manufacturing, compatible with flexible substrates, solution processable and orthogonal (insoluble in the solvent used for the deposition of the organic semicon-

ductor).

2.1.2.1 Inorganic dielectric materials

Already abundantly employed for years in the inorganic technology and manufacturing, silicon oxide (SiO_2) dielectric on Si wafer is also employed as a gate insulator in organic electronics for research purpose. Despite its low dielectric constant ($\varepsilon_r = 3.9$), it provides an ultra-smooth interface and makes device fabrication easy. In order to evaluate and compare different organic semiconductors in TFTs, the use of an insulator which is identical to each substrate allow to draw relevant conclusions. However the presence of hydroxyl groups at the surface that can act as trapping sites alter the device performance [141]. Therefore the interface is often passivated by applying a self-assembled monolayer [141, 142, 143] or depositing a thin polymeric layer on the surface [144, 80, 145].

To reduce the operating voltage in TFTs, one possible approach is to use high-k dielectric materials. With a high dielectric constant, dielectrics based on these materials yield high capacitance and thus can induce the same amount of charge in the channel for a lower voltage. The first high-k materials that were used as gate dielectrics in OTFTs were sputtered amorphous barium zirconate titanate ($\varepsilon_r = 17$), barium strontium titanate ($\varepsilon_r = 16$) and Si_3N_4($\varepsilon_r = 6$) [146]. Pentacene TFTs with a mobility in the range 0.3-0.6 cm^2/Vs were demonstrated. These transistors operate at a voltage of 5V. Titanate oxide $Ta_2O_5$was often chosen as a high-k material (ε_r = 21-27). It could be deposited by electrochemical anodization [147, 148], electron beam evaporation [149], reactive magnetron sputtering [150]. Deposition of the dielectric film was carried out on various substrates such as silicon wafer [147], glass [149], poly(methyl methacrylate) [149] and polycarbonate [148] substrates. Capacitance as high as 250 nF/cm^2 were reported for a 86 nm thick film [148]. Using pentacene as the active layer, TFTs with a mobility of 0.36 cm^2/Vs were demonstrated on flexible substrates. Aluminium oxide Al_2O_3films (ε_r = 7-11) are also used as gate insulators in transistors. Al_2O_3 films were deposited by radiofrequency magnetron sputtering on Si substrate [151], indium tin oxide [151] or flexible plastic sheet [152, 153]. Capacitance ranging from 60 to 600 nF/cm^2 were obtained, corresponding to film thickness of 7-120nm. Using P3HT [154], pentacene [155, 151, 154] or PTAA [152, 153], TFTs with operating voltage below 5V were reported. Other high-k dielectrics includes silicon nitride (Si_3N_4, ε_r = 6-7) [156], Gd_2O_3 oxide (ε_r = 10-11) [157], titanium oxide (TiO_2, ε_r = 41) [158**?**] and hafnium oxide (HfO_x, ε_r = 16-25) [159]. The surface of high-k dielectric oxides is sometimes modified by application of a self-assembled monolayer [154, 159] or a thin polymeric layer such as poly(α-methylstyrene) (PαMS) [154**?**] or poly(methylmethacrylate) (PMMA) [150] to passivate the surface or reduce the leakage current. Using an anodized TiO_2 oxide capped with a thin layer of PαMS (7-8 nm) as a gate dielectric, Majewski et al. reported a one-volt pentacene transistor with a hole mobility of 0.8 cm^2/Vs [**?**]. However processing of inorganic

dielectric materials often requires high temperature, which is incompatible to plastic substrates. Acton et al. reported a low-temperature vacuum-free hybrid dielectric composed of an octadecylphosphonic acid (ODPA) self-assembled monolayer (~2-3 nm) on a cured sol-gel hafnium oxide (4.8 nm) [159]. Compatible with plastic substrates, this ODPA/HfO_xhybrid dielectric provides with high capacitance 410 nF/cm^2 and a low leakage current density $5 \cdot 10^{-8}$ A/cm^2. Operating at 2V, OFETs with a hole mobility of 0.1 cm^2/Vs were demonstrated using a solution processed thiophene-thiazolothiazole copolymer as the semiconductor.

2.1.2.2 Polymer dielectric materials

Polymer dielectric materials are very attractive for applications in electronics because of their solubility with most common solvents, ease of processing at room temperature and their compatibility with patterning techniques. Their properties can be tuned by the design of the monomer and polymerization conditions. As a gate dielectric in TFTs, they should produce smooth uniform pin-hole free thin films with good insulating properties. Insulating polymers that have been used in transistors include polystyrene (PS, $\varepsilon_r = 2.6$), poly(vinylalcohol) (PVA, $\varepsilon_r = 7.8$), poly(methylmethacrylate) (PMMA, $\varepsilon_r = 3.5$), poly(α-methylstyrene) (PαMS), polyvinylphenol (PVP, $\varepsilon_r = 4.5$).

TFTs based on polyvinylphenol (PVP) gate dielectric, in particular those using pentacene as the semiconductor, exhibit the greatest mobility among devices based on a polymer gate dielectric. Using a cross-linked PVP gate dielectric (280 nm thick), carrier mobilities as high as 3 cm^2/Vs were reported in vacuum-sublimed pentacene TFTs, which is much larger than OTS-SAM treated SiO_2gate dielectric TFTs ($\mu \sim 1$ cm^2/Vs) [58]. These results show that polymer gate dielectrics may not only lead to simpler processing than inorganic gate dielectrics, but may also provide with better electrical performance. However TFTs based on high polar polymer insulators such as poly(vinylphenol) (PVP) or poly(vinylalcohol) (PVA) show large hysteresis in their I-V characteristics, with threshold voltage shift as large as 10 V upon operation. This is probably the result of charge trapping due to due to the presence of hydroxyl group or adsorbed water at the interfaces. To reduce this hysteresis, Park et al. used a double layer gate dielectric, which is composed of a thick polymer layer with good dielectric properties and a thin polymer layer in contact with the semiconductor that can induce good charge transport [160]. By combining a thick (1 μm) less-polar poly(vinyl acetate) layer and a thin (20 nm) poly(vinylphenol) layer on top, the undesirable hysteresis was suppressed while maintaining the high mobility (of 0.1 cm^2/Vs) observed in single-layer PVP dielectric TFTs.

Charge trapping can be reduced by employing hydroxyl-free polymers as gate dielectric. Divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) polymer, whose chemical structure is shown on figure 2.4, is a good example of hydroxyl-free and cross-linkable polymer. When cured by UV-lamp or heating process, BCB is or-

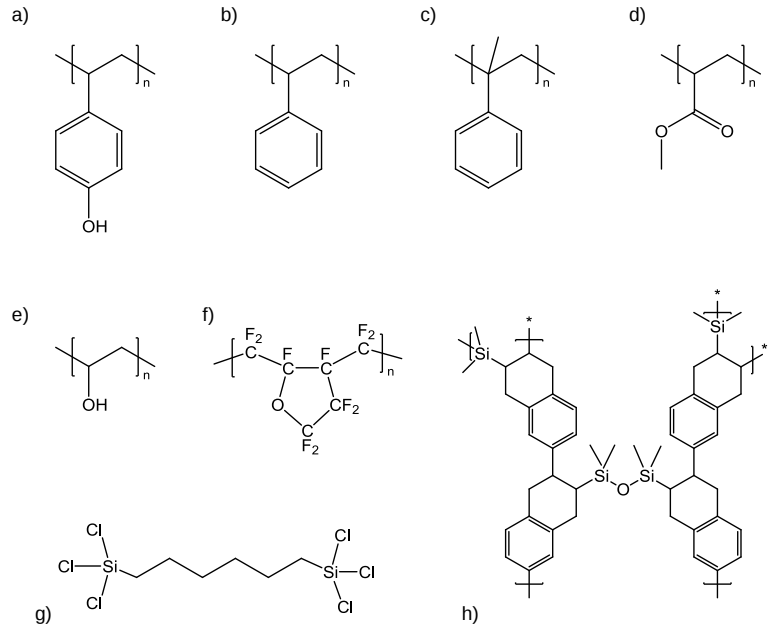

Figure 2.4: Chemical structure of some polymers used as gate dielectrics in transistors: poly(vinylphenol) (PVP), polystyrene (PS), poly(α-methylstyrene) (PαMS), poly(methylmethacrylate) (PMMA), poly(vinylalcohol) (PVA), poly(perfluorobutenylvinylether) (Cytop) and divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB). Molecular structure of 1,6-bis(trichlorosilyl)hexane (C_6-Si) crosslinking agent.

thogonal to most common solvent. Therefore the semiconductor can be solution-processed on top without dissolving the dielectric layer. Uniform and pin-hole free layers can be deposited down to few nanometers (10-25 nm) and yield excellent insulating properties [161]. A dielectric breakdown strength of 3 MV/cm and leakage current below 10^{-8}A were reported for these thin films. Low-voltage top-gate TFTs with a hole mobility of 10^{-4} cm^2/Vs were demonstrated using a 50 nm thick BCB gate dielectric in combination with poly[(9,9-dioctylfluorene-2,7-diyl)-alt-(phenylene[N-(p-2-butylphenyl)iminophenylene])] (TFB) as the semiconductor. The dielectric film was cured at 290°C for 9s under N_2. BCB polymer can also be employed as a passivation layer on top of silicon oxide to improve the performance in n-channel transistors. Mobilities up to 3 cm^2/Vs were reported for C_{60} devices, which is much higher than the value obtained for OTS-SAM treated SiO_2 dielectric TFTs [80].

Amorphous fluoropolymer dielectrics such as poly(perfluorobutenylvinylether) [45], commercially known as Cytop (Asahi Glass Co.), exhibit good insulating properties and provide with excellent TFT operational stability. This hydroxyl-free fluoropolymer is highly transparent, has a low permittivity ($\varepsilon_r = 2.1$) and is highly water repellent. Cytop has a water contact angle of 112° [162]. Easily-processed from solution, it can be spin-cast onto many organic layers without dissolving the underlying semiconductor layer because of its orthogonality with most common organic solvent.

This is useful for the fabrication of transistors in a top-gate architecture. Cytop is an excellent insulator. A dielectric strength of 9.8 MV/cm and a leakage current of 3.10^{-6} A/cm^2 at this field were reported for thick (460 nm) films [162]. Excellent insulating properties were also demonstrated for thinner films. Measured for different thicknesses ranging from 15 nm to 200 nm, breakdown strength of 5-6 MV/cm^2 and a low leakage current density of 10^{-8} A/cm^2 were reported [163, 164]. Cytop polymer was first used as a gate dielectric with polymer semiconductors such as P3HT ($\mu = 2 \cdot 10^{-2}$ cm^2/Vs), F8T2 ($\mu = 1 \cdot 10^{-3}$ cm^2/Vs) and PTAA ($\mu = 5 \cdot 10^{-3}$cm^2/Vs) in top-gate transistors [45]. Kalb et al. reported single-crystal rubrene and pentacene TFTs with very steep subthreshold swing (0.3 V/dec) and mobilities as high as 5.7 and 1.4 cm^2/Vs, respectively [162]. Negligible hysteresis and threshold shift on gate bias were observed, showing the quality of the interface. Both p-channel and n-channel transistors employing pentacene and perylene diimide (PTCDI-C_{13}) as semiconductors were demonstrated on a standard SiO_2dielectric coated with an ultrathin layer of Cytop [144]. With ultrathin CYTOP film (20 nm), high capacitances (~100 nF/cm^2) were achieved, allowing operations of PTCDI-C_{13} TFTs within 3 V [164]. TFTs exhibited the same performance and electrical stability as TFTs with much thicker films.

To fabricate low-operating TFTs, one of the major challenge for polymer gate dielectric is the reduction of the film thickness, while preserving good insulating properties. It has been found difficult to deposit polymer films less than 100 nm thick without pin-holes due to their large free volume [161]. Cross-linking agents were added to polymer systems to achieve ultrathin (<50 nm) film with high capacitance and high dielectric breakdown strength [165, 166, 167]. Adding organosilane cross-linking agent to PVP and PS polymers, Yoon et al. were able to spin-coat ultrathin (10-20 nm) smooth pin-hole-free polymer gate dielectric [165]. By creating a strong 3D network in the polymer system, the leakage current densities (10^{-8}-10^{-7} A/cm^2 at 2 MV/cm) were reduced by one or two orders of magnitude compared to neat PVP or PS films (120-130 nm). TFTs fabricated on n^+-Si substrate were demonstrated employing various p-type and n-type semiconductors such as pentacene (0.1 cm^2/Vs), DH6T (0.1 cm^2/Vs), P3HT ($4 \cdot 10^{-3}$ cm^2/Vs) or CuFPc ($5 \cdot 10^{-3}$ cm^2/Vs). These transistors operate at very low voltages (< 2 V) due to the large capacitance (200-300 nF/cm^2). Pentacene TFTs with cross-linked PVP insulating layer were also fabricated on many different substrate including ITO-glass, ITO-mylar, and Al foil.

However application of cross-linked polymer in top-gate transistors is often challenging because of the high curing temperature that can damage the semiconductor film, the difficulty to find orthogonal solvents and the roughness of the underlying semiconductor layer that may lead to an increase of the leakage current. The main advantage of employing organosilane as cross-linking agents is that the cross-linking takes place at room temperature spontaneously in presence of moisture and is therefore compatible with top-gate architecture. Blending 1,6-bis(trichlorosilyl)hexane with PMMA and PVP polymer dielectrics, top-gate polymer TFTs with ultra-thin (30-50 nm) gate dielectric were demonstrated [166]. High mobilities of 0.2 cm^2/Vs

and on/off current ratio of 10^4 were obtained with pBTTT semiconducting polymer. Cheng et al. extended this approach to amorphous fluoropolymer gate dielectric and realized cross-linked Cytop films as thin as 50 nm with excellent yield (100%) [167]. Dielectric breakdown strength of 2 MV/cm and low leakage current densities below 10-100 nA/mm^2 were reported. The orthogonality of the Cytop fluorinated solvent to most organic semiconductors allow fabrication of transistors on both polymeric (F8T2) and soluble small molecule (PDI N1400) semiconductors. Furthermore these low-voltage (< 5 V) transistors based on cross-linked Cytop exhibit reduced bias stress and better air stability compared to cross-linked PMMA devices due to their perfluorinated chemical structure.

2.1.2.3 Self-assembled monolayer dielectrics

Self-assembled monolayers are densely packed and self-ordered molecular assemblies of small molecules. They can be deposited on metals, on oxides or on passivated Si surfaces by spontaneous absorption or vapor deposition. The anchor group of the molecule, also named active precursor, is chemisorbed to the surface and the molecular chain stands perpendicular or with a small tilt angle to the surface. They can be used as passivation/injection layer over electrodes, also as a passivation layer over thick dielectrics (e.g. Silicon oxide) or as a dielectric itself.

In electronic applications, SAM functionalization of metal electrodes was shown to improve charge injection between the semiconductor and the electrodes by altering the work functions of electrodes. On metal surfaces, among the most commonly used and well characterized SAMs (especially on gold electrodes) are alkanethiols [168, 169, 170] and thiol-derivatives [171, 69].

Surface modification of dielectric oxides with self-assembled monolayers was found to be useful to improve device performances and to passivate the surface from hydroxyl groups that can act as charge trapping sites. Organosilane molecules, such as octyltrichlorosilane (OTS), octyldecyltrichlorosilane (ODTS) or hexamethyldisilazane (HMDS) (shown on figure 2.5), can be deposited on hydroxilated surfaces such as SiO_2, Al_2O_3 and ITO surfaces by vapor deposition. Two other class of molecules, alkanoic acids and phosphonic acids, can bind on metal oxide surfaces, such as Al_20_3, ITO and AgO by vapor or solution depositions. SAM surface treatments on the gate dielectric surface were observed to increase the charge carrier mobility, reduce the current hysteresis, reduce the subthreshold slope, increase the current on/off ratio and shift the threshold voltage. These performance enhancements can be explained by a change in the semiconductor film growth morphology (crystallinity and grain size) and/or the dielectric-semiconductor interface properties (passivation of trap sites, surface energy or chemical structure of the SAMs).

When using octadecyltrichlorosilane (ODTS) treated gate dielectrics in pentacene TFTs, the carrier mobility was increased up to 1.6 cm^2/Vs compared to 0.1 cm^2/Vs on bare SiO_2 and the current on/off ratio was improved by three orders of magnitude

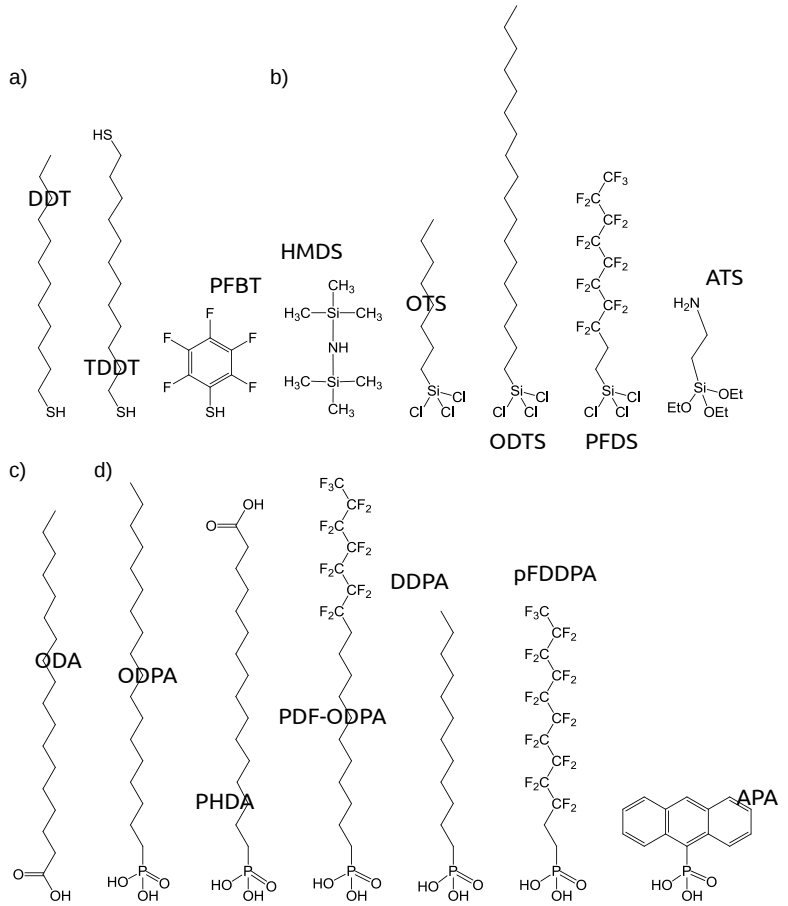

Figure 2.5: Chemical structures of some self-assembled molecules, used on metal: dodecylthiol (DDT), thioldodecylthiol (TDDT), pentafluorobenzenethiol (PFBT) (a); silanes used on oxides: hexamethyldisilazane (HMDS), octatrichlorosilane (OTS), octadecatrichlorosilane (ODTS), , $10F_3$-perfluorodecylsilane (PFDS), aminotricylsilane (ATS) (b); n-alkanoic acid used on oxides: octadecanoïc acid (ODA) (c), phosphonic acids: octadecylphosphonic acid (ODPA), phosphonohexadecanoïc acid (PHDA), 12-18F-pentadecylfluorooctadecylphosphonic acid (PDF-ODPA), dodecylphosphonic acid (DDPA), $1H_2$,$2H_2$-perfluorododecylphosphonic acid (pFDDPA), anthracene-phosphonic acid (APA) (d).

[143]. The self-assembled monolayer plays an important role as a nucleation site. For instance, favorable growth of pentacene islands were obtained on anthracene-phosphonic acid (compared to octadecylphosphonic acid or quaterthiophene phosphonic acid) due to structural similarities between pentacene and the SAM terminal group [172]. Pentacene films grown on highly ordered ODTS SAMs (alignement and packing of the alkyl chain) show a higher crystallinity and a better connectivity between domains, than disordered SAMs [172]. On HMDS-treated SiO_2 surface, Yang et al. reported a hole mobility of 3.4 cm^2/Vs in pentacene films and observed that the crystalline structure of the first semiconductor layers depends strongly on the dielectric surface properties and affects directly the structure and mobility of the bulk pentacene film [173]. Mobility of 5 cm^2/Vs in pentacene films were reported on

eicosanoic acid-treated Al_2O_3 and was ascribed to the regular small grains [59].

The presence of -OH group on dielectric oxide surfaces act as carrier traps for electrons, resulting in a decrease of the carrier mobility in TFTs. Surface treatment with SAM reduce significantly charge trapping at the interface and lead to an improvement in carrier mobility and a decrease in current hysteresis, especially in n-channel devices [141, 174, 142]. Using alkylsilane SAMs (HMDS, DTS, ODTS) on SiO_2 gate dielectric, Chua et al. showed that electron transport was enhanced with increasing alkyl SAM chain length, while no field-effect could be observed with unpassivated SiO_2 surface [141].

To reduce the TFT operating voltage, a promising solution is to develop OFET based on self-assembled monolayer (SAM) gate dielectrics. With densely packed monolayer, SAM dielectrics can suppress carrier tunneling thanks to highly ordered aliphatic chains [175, 176, 9]. These molecules can be functionalized on a native dielectric oxide. Even though they are only few nanometers thick (2-5 nm), they yield to high capacitances (500 nF - 1 μF) and low leakage current densities ($\sim 10^{-7} - 10^{-8}$ A/cm^2). Thus the operating voltage is reduced to few volts (below 2-3 V).

OFETs based on SAM gate dielectric have been demonstrated and reported by several research groups. Collet et al. were the first to pioneer in 2000 the use of SAM as a gate insulator in transistor. Functionalizing a carboxyl terminated n-alkyltrichlorosilane SAM gate dielectric on a Si wafer, they reported α-sexithiophene transistors with an operating voltage below 2 V, a hole mobility of $3.6 \cdot 10^{-4}$ cm^2/Vs and gate leakage current of 10^{-6} A/cm^2 [177]. Using an aromatic terminated alkylsilane, 18-phenoxyoctadecyltrichlorosilane, as SAM gate dielectric, Halik et al. demonstrated low-voltage (<2 V) high performance pentacene TFTs with a hole mobility of 1 cm^2/Vs, a current on/off ratio of 10^6 and subthreshold slope of 100 mV/dec. The SAM dielectric showed low leakage current (10^{-7} A/cm^2 at 2 V) and large dielectric breakdown strength (14 MV/cm^{-1}) [47].

Later the same group realized the self-assembly of octadecylphosphonic acids on patterned aluminium gate electrode and showed that the leakage current through SAM on aluminium oxide (10^{-8} A/cm^2 at 2 V) was no larger than leakage through SAMs on silicon [48]. With this phosphonic acid SAM gate dielectric, they demonstrated both p-type and n-type low-voltage transistors employing vacuum-sublimed small molecules and the first low-voltage (3 V) organic complementary inverters on glass or flexible substrates. Similarly, Ma et al. functionalized anthryl-alkyl phosphonic acid SAM on *AlOx/Al* and reported pentacene transistors with an operating voltage of 3 V and a leakage current of 10^{-8} A/cm^2 at 2 V [178]. By employing alkylphosphonic acids with five different chain lengths (from 2 to 18 carbon atoms), Jedaa et al. studied the impact of the chain length of the SAMs on the insulating properties of the AlOx/SAM dielectrics and on the performances in TFTs [179]. The breakdown voltage was the same for dielectrics with short SAM (C_6-PA, C_2-PA) and without SAM, and increases for longer SAM chain (up to 5 MV/cm for C_{18}-PA). An increase in leakage current was observed as the chain length is reduced. Low-voltage

pentacene transistors with mobility greater than 0.1 cm^2/Vs and current on/off ratio of 10^6 were reported for SAMs with a chain length longer or equal to C_{10} on plasma grown AlOx, the best performance being obtained with C_{14}-PA ($\mu \sim 0.3$ cm^2/Vs). This work showed that alkyl chain as short as C_{10} are adequate as insulating layers.

Using solution-processable fullerene derivative semiconductors and octadecylphosphonic acid SAM dielectric, Wöbkenberg et al. demonstrated low-voltage solution-processed n-type transistors. Operating below 2V, these transistors exhibited an electron mobility of 0.01-0.04 cm^2/Vs [180]. However the problem associated with methyl terminated SAM dielectrics is that they have low and dispersive surface energy. Therefore a major challenge with low-voltage TFTs based on SAM dielectric is to find semiconductors with good wetting behavior on the dielectric surface in order to form good quality semiconductor-dielectric interface. Ball et al. have demonstrated both hole and electron transporting low-voltage solution-processed transistors based on a phosphonohexadecanoic acid (PHDA) SAM dielectric [181]. Compared to methyl terminated alkylphosphonic acids, carboxylic terminated SAMs, such as PHDA, exhibit increased surface energy, enabling the solution process of a wide range of organic semiconductor onto the hybrid dielectric.

The use of SAM gate dielectrics provide with a powerful method to control and tune the threshold voltage in organic transistors. The threshold voltage can be adjusted in TFTs by choosing judiciously the molecular structure of the SAM employed in the structure. Kobayashi et al. showed that the threshold voltage can be controlled by functionalizing the surface of the SiO_2gate dielectric with a silane-based SAM having more or less electronegative substituents [182]. In pentacene and C_{60} TFTs, surface treatment of SiO_2gate insulator with perfluoroalkylsilane and aminoalkylsilane induce a threshold voltage shift towards more positive and negative voltages, respectively, compared to unsubstituted alkylsilane SAM and untreated devices. These shifts were ascribed to the built-in potentials created by the SAM dipole moments. To control the threshold voltage in low-voltage (<3 V) transistors, Kraft et al. functionalized fluoroalkyl phosphonic acid SAM on patterned plasma-oxidized aluminium gate electrode [183]. Compared with alkyl phosphonic acid SAM, the use of fluoroalkyl phosphonic acid SAM led to a significant positive threshold voltage shift of more than 1 V in both pentacene (p-type) and F_{16}CuPc (n-type) OFETs. The strong electron withdrawing character of the fluorinated alkyl chain implies that an additional potential is required to accumulate electrons (deplete hole) in n-channel (p-channel) OFETs. Zschieschang et al. were able to tune continuously the threshold voltage of low-voltage p-type and n-type TFTs over a wide range (from -0.3 V to 1.1 V) as a linear function (40 mV/%) of the fluorine concentration in a mixed self-assembled monolayer gate dielectric composed of alkyl and fluoroalkyl phosphonic acid molecules [184]. This change in threshold voltage can be explained by the reduction of the electron density in the transistor channel due to the electron-withdrawing property of the fluoroalkyl SAMs. As the switching voltage of an inverter is determined by the threshold voltages of the transistors, its ideal value (half the supply voltage) can

be set by setting a suitable SAM mixing ratio so that it provides maximum signal noise immunity and lower operating voltage to the circuit [184]. Based simply on a solution process technic, chemical tayloring of the SAM and concentration ratio calibration are two powerful methods to control the threshold voltage in low-power organic transistors and circuits.

2.2 Charge transport in organic semiconductors

2.2.1 Electronic properties of conjugated materials

Organic small molecules or polymers are mainly composed of carbon atoms. The atomic number of carbon is Z = 6 and the electronic configuration of an isolated carbon atom is $1s^2\ 2s^2\ 2p_x^1\ 2p_y^1$. The $1s^2$ electrons are core electrons and are not involved in bonding. The carbon's tetravalence cannot be explained only by the valence bond theory but is made possible thanks to the promotion of one electron [185]. Indeed as the energy gap between the $2s$ and $2p$ orbitals is small, an electron of the $2s$ orbital is promoted to the empty $2p_z$ orbital which leads to the configuration $1s^2\ 2s^1\ 2p_x^1\ 2p_y^1\ 2p_z^1$ with four unpaired electrons (on figure 2.6 a.) The spins are all parallel according to Hund's rule. The energy needed for the electron promotion is largely compensated by the energy released when bonds are formed. Thus the system is more stable. Electrons from one $2s$ and two $2p$ orbitals are reorganized to form a sp^2 hybrid: 3 sp orbitals lie in a plane pointing to the corners of an equilateral triangle and one pure p orbital (p_z), which is not involved in the hybridization, is perpendicular to the plane formed by the three sp hybrid orbitals (figure 2.6 a) [185]. Like in ethene molecule $H_2C = CH_2$, each sp^2 hybridized carbon atom can form three σ bonds in the same plane while electrons from the unhybridized p orbitals of two carbon atoms are paired and form a π bond (figure 2.6 b-d). The latter lock any rotations between the two CH_2 groups. The σ and π bonds between the two carbon atoms form a double bond. The π bond is relatively weak because the bond is accessible from above and below the plane.

Small conjugated molecules and conjugated polymers are made of an alternation of single and double bonds. The π electrons are delocalized along the molecule, resulting in conduction of electrons. When π orbitals of two carbon atoms interfere constructively, it leads to a π bonding orbital whereas when π orbitals interfere destructively, π antibonding orbital are formed. If occupied, the first one increases the cohesion between the two carbon atoms while the second one tend to separate the two atoms. The molecular orbital energy level diagram of conjugated molecules can be constructed using Hückel approximation and filled according to Pauli's principle. Similarly to ethene's molecular orbitals, a diagram of which is shown in figure 2.6 (b), it is found that the highest occupied molecular orbital (HOMO) is the π-bonding orbital and the lowest unoccupied molecular orbital (LUMO) is the π^*-antibonding orbital. In organic semiconductor, the LUMO and HOMO, jointly called the frontier

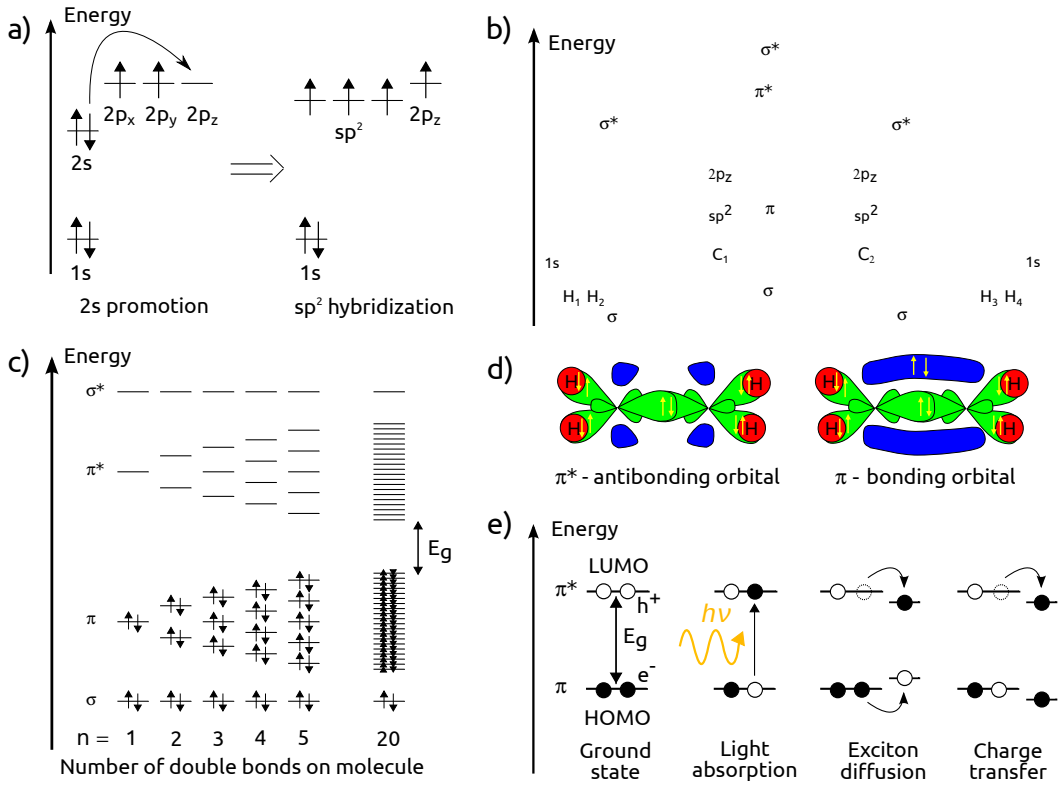

Figure 2.6: Electronic configuration diagrams of carbon atom: promotion of an electron from the 2s orbital to a 2p orbital and sp^2hybridization of atomic orbitals (a). Molecular orbital energy level diagram of ethene (b). Inset (b): molecular structure of ethene. Molecular orbital energy level diagram of conjugated molecules as function of the length of the molecule (c). Diagram representing the formation of σ-bonding, π-bonding and π*-antibonding orbitals in ethene molecule (d). Diagram illustrating the different optoelectronic processes that occur in organic semiconductors: light absorption, diffusion of an exciton and charge transfer (e).

orbitals, are respectively the equivalent to the conduction band and the valence band in inorganic semiconductors. The energy difference between the two levels is the band gap energy (Eg).

While the length of molecules increases, the number of π states increases. Therefore the number of energy levels increases and the band gap energy decreases. In long conjugated polymers, the number of states increases so much that the dense energy of states can be considered as a continuous energy band (figure 2.6 c). In the ground state, the HOMO level is filled with electrons and the LUMO remains empty. When a photon with sufficient energy ($h\nu > E_g$) is absorbed or a bias ($eV > E_g$) is applied to the electrodes, an electron can be optically or electrically excited leaving a hole in the HOMO orbital (figure 2.6 e). Due to proximity and Coulomb interaction, the pair hole-electron relax into a localized bound excited state, called an exciton. The binding energy of an exciton in molecular solids is typically 0.1-0.5 eV.

2.2.2 Band-like transport

In high conductivity materials such as metals and crystalline semiconductors, charges are delocalized and the transport is limited by phonon scattering. At zero temperature the valence band is completely filled, whereas there are no electrons in the conduction band. By thermal excitation or through doping, charge carriers can be transferred to the conduction band, where they are ideally delocalized over the whole crystal. As temperature increases, the mobility first increases ($\mu \sim T^{3/2}$) due to impurities scattering then decreases ($\mu \sim T^{-3/2}$) due to phonon scattering induced by the lattice vibrations.

In inorganic semiconductors, crystals are covalently bonded and coupling between atoms is strong. Whereas in molecular crystals coupling between molecules is weaker and rely on Van-der-Walls forces and π-π interactions. The larger effective mass and lattice disorder of organic crystals leads to higher density of localized states and lower charge carrier mobility.

An increase of mobility with decreasing temperature is an indicator of band-like transport and this trend was observed in high-purity defect-free single-crystals such as pentacene [186] or rubrene [187]. However most organic semiconductors show a high degree of disorder, grain boundaries, impurities, which prevent band-like transport.

2.2.3 Polaronic transport

In many organic systems with a high degree of crystallinity and mobility values greater than 0.1 cm^2/Vs, conduction of current can be of polaronic nature. Due to the energetic and positional disorder and strong electron-phonon interactions that occurs in these systems, charge carriers can form localized polarons and their energy levels are lowered compared to their extended states [77, 9]. A polaron, which is the combination of a charge and the induced distortion of the surrounding lattice, is considered as a quasi-particle. When the electron move into the lattice, it carries the lattice polarization with it, and thus the surrounding molecular distortion. Charge transport is characterized by carrier hopping between neighbouring sites and polaronic relaxation. Optical transitions below the absorption edge of the neutral molecule are characteristic of the polaronic transport and can be observed by charge modulation spectroscopy. At high temperatures, charge transport of polaronic carriers is thermally activated. Following the physics of electron-transfer process developed by Marcus [188], the mobility is found to be:

$$\mu = \frac{ea^2}{k_B T} \frac{\sqrt{\pi} J^2}{\hbar \sqrt{2 E_p k_B T}} \exp\left(-\frac{E_p}{2 k_B T}\right) \tag{2.1}$$

where a is the hopping distance, J is the nearest-neighbor interaction energy, E_p the polaron binding energy that can be estimated to be on the order of 30-60 meV, e is the electronic charge, k_B is the Boltzmann's constant, $\hbar$ is the Planck's constant, T is the temperature.

2.2.4 Variable Range Hopping transport model

In low conductivity materials ($\mu < 0.1$ cm^2/Vs) such as amorphous and polycrystalline semiconductors, the transport is explained by hopping of charges between localized states. Contrary to delocalized transport, localized transport is phonon assisted: the carrier mobility increases with increasing temperature. Mott developed the variable range hopping (VRH) concept, in which a carrier may either hop over a small distance with a high activation energy or hop over a large distance with a low activation energy [189]. In this model, the temperature dependence of the mobility is described as:

$$\mu = \mu_0 exp\big[-(T_0/T)^{\frac{1}{n+1}}\big] \tag{2.2}$$

where T_0 is inversely proportional to the density of states at the Fermi level, μ_0 is the mobility at low temperatures and n = 1, 2 or 3 is the dimensionality of the system.

2.2.5 Vissenberg and Matters model

Vissenberg and Matter developed a model to explain the temperature and gate voltage dependence of the FET mobility of amorphous organic semiconductors [190]. In their model, the charge transport is dominated by thermally activated tunneling of carriers between localized states. Following the VRH concept developed by Mott, they suggested that the carrier transport depend not only on the hopping distance but also on the energy distribution of the localized states. Indeed, when applying a gate voltage to a FET, accumulated charge carriers at the interface fill first the lower-lying states of the organic semiconductor and any additional charges will occupy states with higher energies. Hence the additional charges require less activation energy to jump to a neighboring localized site. Therefore the mobility increases with increasing gate voltage. Contrary to Mott who used a constant density of states, this model is based on the concept of hopping in an exponential density of localized states as:

$$g(E) = \frac{N_t}{k_B T_0} \exp(\frac{E}{k_B T_0}) \tag{2.3}$$

where N_t is the number of states per unit volume, T_0 is the width of the exponential distribution, k_B is the Boltzmann's constant and E is the energy level. By using this concept and the percolation theory, the FET mobility was derived as:

$$\mu_{V_{GS}} = \frac{\sigma_0}{e}\left[\frac{(T_0/T)^4 \ sin(\pi\frac{T}{T_0})}{(2\alpha)^3 B_c}\right]^{\frac{T_0}{T}}\left[\frac{(C_i V_{GS})^2}{2k_B T_0 \varepsilon_s}\right]^{\frac{T_0}{T}-1} \tag{2.4}$$

where σ_0 is a pre-exponential factor, T_0 is the width of the exponential distribution, T is the temperature, α is the effective overlap parameter between the wave functions of localized states, B_c is the critical number of bonds for the onset of percolation ($B_c = 2.7$ for 3D amorphous systems) in networks, ε_s is the dielectric constant of the semiconductor, C_i is the geometrical capacitance of the gate dielectric and V_{GS}

is the gate voltage. Hence the temperature dependence of the field-effect mobility follows an Arrhenius behavior $\mu_{FE} \sim exp[-E_a/kT]$. The activation energy (E_a) is logarithmically temperature dependent and decreases with increasing gate voltage. This model was confirmed experimentally in disordered semiconductors [191, 192].

2.2.6 Field dependent charge carrier mobility

According to Poole-Frenkel mechanism [56], high electric fields (above $\sim 10^5$ V/cm) can modify significantly the coulombic potential of the local states. This induces a change in mobility in transistors and its dependence on the magnitude of the electric field (F) is given by:

$$\mu(F) = \mu(0)exp(\frac{e}{k_B T}\beta\sqrt{F}) \tag{2.5}$$

where $\mu(0)$ is the mobility at zero field and $\beta = (\frac{e}{\pi\epsilon_r\epsilon_0})^{\frac{1}{2}}$ is the Poole-Frenkel factor.

2.2.7 Multiple Trapping and Release model

The Multiple Trapping and Release (MTR) model was developed to describe electronic transport in amorphous silicon [193] and now is also used to explain the electronic transport in organic semiconductors. This model takes into account the interactions between the delocalized band and localized states, that are separated by a certain energy level called the transport level. Above this transport level, the density of states is sufficiently high so that the electronic states are extended and form a band whereas below this level, electronic states are localized. While drifting in the delocalized states closed to the transport level, carriers get trapped in the localized states and then are thermally released. Assuming that the total time a carrier spends in trap states is significantly shorter than the transit time and the release of trap carriers (which is thermally activated), the drift mobility (μ_D) is found to be:

$$\mu_D(E_t, N_t) = \alpha\mu_0 exp\left[-\frac{E_c - E_t}{kT}\right] \tag{2.6}$$

where μ_0 is the mobility in the delocalized band, E_c is the energy of the delocalized conduction band edge (for n-channel materials), E_t is the energy of the trap state and α is a parameter that depends on the distribution of traps. For a single trap level, α is the ratio of the density of states N_c at the delocalized band edge to the density of traps N_t: $\alpha = \frac{N_c}{N_t}$. In other cases, the values for N_t and α have to be calculated.

2.3 Graphene for transistor applications

2.3.1 Electronic properties of graphene

Graphene has attracted great interest due to its distinctive band structure and unique electronic properties. Graphene is a zero-gap semiconductor and its band structure has a linear relation between energy and momentum. Charge carriers in graphene are massless Dirac fermions and are described by a Dirac-like equation [18, 194, 19].

Graphene is a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice. Each carbon atom is sp^2 hybridized (see subsection 2.2.1) and has one conduction electron ($2p_z$) per atom, which can be treated independently from the other valence electrons (filling the low-lying σ-band) in the $\pi - \pi^\star$ model. In the hexagonal lattice of graphene, the distance between two adjacent carbon atoms is 1.42 Å and the fundamental displacements of the unit cell have magnitude a = $1.42\times\sqrt{3}$. Its first Brillouin zone, a zone containing one electron per atom, is an hexagon whose sides are distant $1/\sqrt{3}$a from its center. The electronic structure of single-layer graphene can be described using a "tight-binding Hamiltonian" to obtain the dispersion relation restricted to the first nearest-neighbour interactions as [194]:

$$E(k_x, k_y) = \pm\gamma_0\sqrt{1 + 4\cos(k_y a/2) + 4\cos(\sqrt{3}k_x a/2)\cos(k_y a/2)} \tag{2.7}$$

where γ_0 is the transfer integral between first-neighbour π-orbitals (~ 2.9-3.1 eV) and $\mathbf{k} = (k_x, k_y)$ are the ensemble of electronic vectors in the first Brillouin zone.

Electrons propagating through the bidimensional structure of graphene are massless Dirac fermions, a gas of charged particles with zero rest mass and an effective "speed of light" of around 10^6 m/s. Charge carriers in graphene are described by a 2D analog of the relativistic Dirac equation, rather than the non-relativistic Schrödinger equation with an effective mass ($m^\star$), as[19]:

$$\hat{\mathcal{H}} = \nu_F \vec{\sigma}\cdot\hat{p} \tag{2.8}$$

where $\nu_F = \sqrt{3}\gamma_0 a/(2\hbar) \approx 10^6$ m/s is the Fermi velocity playing the role of the speed of light, $\vec{\sigma}$ is a 2D pseudospin matrix describing two sublattices of the honeycomb lattice and $\hat{p}$ is the momentum operator. The pseudospin is an index that indicates on which of the two sublattices a quasi-particle is located. Applying this Dirac-like Hamiltonian near the Fermi level (E_F) leads to the linear spectrum of graphene $E = \hbar\nu_F k$. The band structure is composed of two branches that are cone-shaped (for low-energy values, |E|< 1 eV) and meet at the K point. The positive energy branch is fully occupied whereas the negative branch is totally empty.

Moreover, graphene exhibits near-ballistic transport at room temperature. Its electrons can cover submicrometer distances without scattering, even in samples places on an atomically rough substrates or covered with adsorbates. Noteworthy, it has also a minimum conductivity of ~ $4e^2/h$ at zero field when the carrier density

tends to zero near the Dirac point [18].

2.3.2 Transparent conductor

Because of its low sheet resistance and high transparency, graphene is a promising material for optoelectronic applications [195] such as displays, solar cells, and photodetectors. Graphene has several advantages over more widespread transparent conductors like indium tin oxide (ITO). Graphene is flexible and has a high transparency over a wide wavelength range, whereas ITO is brittle, expensive (due to indium scarcity) and difficult to pattern. From Fresnel equations, the transmittance of single-layer graphene is derived as [196]:

$$T = \frac{1}{(1 + 0.5\pi\alpha)^2} \sim 1 - \pi\alpha \simeq 97.7\% \tag{2.9}$$

where $\alpha = e^2/(4\pi\varepsilon_0\hbar c) \simeq 1/137$ is the fine-structure constant [197]. The absorption spectrum is quite flat over a wide range of spectrum from 300 nm to 2500 nm and a peak in the ultraviolet region (~270 nm) [22]. Few layers graphene is equivalent to a superposition of almost non interacting single-layer graphene. In FLG, other absorption peaks can be observed at lower energies due to interband transitions.

In a thin-film of thickness (t) and resistivity (ρ), the resistance of a rectangle of length (L) and width (W) is:

$$R = \frac{\rho}{t} \cdot \frac{L}{W} = R_S \cdot \frac{L}{W} \tag{2.10}$$

Even though the sheet resistance R_s has units of ohms, it is often quoted in "ohms per square" ($\Omega/\square$). The transconductance (T) can also be expressed as function of the optical conductivity (G_0) [20]:

$$T = (1 + \frac{Z_0}{2R_s}\frac{G_0}{\sigma_{2D}}) \tag{2.11}$$

where $Z_0 = 1/\varepsilon_0 c = 377\,\Omega$ is the free-space impedance, ε_0 is the free-space dielectric constant, c is the speed of light and $\sigma_{2D} = n\mu e$ is the bidimensional conductivity. When the number of charge carriers (n) is equal to 0, the bidimensional conductivity is not equal to zero and take a minimal value of $4e^2/h$, resulting in an ideal sheet resistance of 6 $k\Omega/\square$ for single-layer graphene with $T \simeq 97.7\%$. Commercial ITO has a transconductance of 80% and a low sheet resistance of 10 $\Omega/\square$ on glass [198] and 60-300 $\Omega/\square$ on polyethylene terephtalate[199]. Therefore intrinsic single-layer graphene compete with ITO in terms of transparency, but not sheet resistance. For real graphene film, $T \simeq 90\%$ and $R_s = 20\ \Omega/\square$ can be estimated when taking the number of charge carriers and mobility of typical CVD grown graphene films ($n = 3{\cdot}10^{12}$ cm^{-2} and $\mu \sim 2 \cdot 10^4$ cm^2/Vs).

Blake et al. were able to fabricate transparent conductive films with $T \simeq 90\%$ and $R_s = 5\ k\Omega/\square$ by liquid phase exfoliation of graphite, followed by vacuum filtration and

annealing [200]. They also showed that the properties of transparent conducting films can be improved by chemical doping. They used a film of polyvinyl alcohol to induce n-type doping in mechanically exfoliated graphene and obtained a transparency of 98% and a low sheet resistance of 400 Ω/□. Bae et al. reduced the sheet resistance by one order of magnitude down to 30 Ω/□ while maintaining a transparency of 90% by nitric acid treatment of CVD grown graphene conductive layer [22].

2.3.3 Production of graphene

Current graphene deposition techniques include mechanical exfoliation, liquid-phase (or solvent) exfoliation, chemical vapour deposition, epitaxy on metal substrates, chemical oxidation, and sublimation of silicon from SiC.

When the electrical field-effect was first observed in 2004 [27], graphene was prepared by mechanical exfoliation (ME) of graphite. This method consists in peeling off a piece of graphite with an adhesive tape. It still produces high quality single layer graphene up to millemetres in size, which is suitable for research purpose. However it's incompatible with large scale applications, which require high yield and throughput.

Liquid phase exfoliation (LPE) provide with a scalable method to produce high-quality unoxidized graphene layer. This approach consists in exfoliating graphene flakes from powdered graphite by chemical wet dispersion followed by sonication and/or centrifugation (to remove any aggregates) [29]. These dispersed flakes can be then deposited by spray coating, vacuum filtration or drop casting on substrates. Dispersion of graphite in solvent can only occur if the net energy cost is very small. This energy balanced can be expressed as the enthalpy of mixing (per unit volume):

$$\frac{\Delta H_{mix}}{V_{mix}} \approx \frac{2 \cdot \phi}{T_{flake}} (\sqrt{E_{Gr}} - \sqrt{E_{Sol}})^2 \tag{2.12}$$

where E_{Gr} and E_{Sol} are the surface energy of graphite and the solvent, respectively, T_{flake} is the thickness of a graphene flake and ϕ is the graphene volume fraction. For graphite, the surface energy is defined as the energy per unit area required to overcome the van der Waals forces when peeling two sheets apart. The dispersed concentration reaches peak values for solvent with a surface energy very close to the graphene surface energy (70-80 mJ/m^2). Solvents with a surface tensions in the region of 40-50 mJ/m^{2}are found to be more suitable for exfoliation of graphene. Monolayer graphene at yields (mass of monolayers/ starting graphite mass) of 1 wt % were reported [29].

Single layer graphene can be grown by chemical vapour deposition (CVD) of hydrocarbons on metal substrates at a suitable temperature. Graphene can be grown on various substrates from single-crystal Ni [201], Ir [202], Pt [203] to polycrystalline Ni thin films [204, 205] and Cu foil [28]. With respect to deposition on Ni film, growth on copper film lead to larger grain size and large coverage of monolayer flakes (>95%) [28]. After being grown on metals, these graphene films are transfered to SiO_2/Si substrate or other device structures. Transfer of graphene from SiO_2/Si substrate

[206] or Cu foils [28] was reported by coating an intermediate poly(methyl methacrylate) (PMMA) polymer layer, followed by etching of the initial metal substrate. The PMMA/graphene membrane is transferred to the target substrate and PMMA is disolved in acetone. CVD growing technique on polycrystalline substrates and thin film transfer provide with a cost effective approach for large area deposition of graphene.

Graphene, or rather called chemically derived graphene, can be prepared by reducing graphene oxide films (GO)[207]. Graphite oxide is first synthesized by placing graphite in acids in the presence of an oxidizing agent. Graphene oxide flakes are then produced by sonication of graphite oxide, following the 55-year-old Hummers method [208], and finally transferred on a substrate surface. The presence of functional groups on both sides of the plane (hydroxyl or epoxide) and around the edges (carboxylic or carbonyl) makes graphene oxide sheets readily dispersible in water to form a suspension of individual sheets. Although large flakes can be deposited, graphene oxide is electrically insulating due to the presence of the chemical moities that disrupt the sp^2 network. Once reduced, graphene oxide does not fully regain the electrical properties of pristine graphene. Due to its processing advantages, mechanical stability and optoelectronic tunability, reduced graphine oxide is an attractive approach for flexible thin-film applications [209].

Ordered graphene layers can also be grown by sublimation of silicon from hexagonal silicon carbide (SiC). The thermal degradation of SiC has the benefit that the graphene is grown directly on a silicon surface. However it requires process with high temperatures of 1000-1200°C or above. Riedl et al. explained that after thermal annealing (700°C), hydrogen intercalation between the silicon surface and carbon layers does the interfacial layer, the zero-layer, electronically inactive, while leading to a free-standing-monolayer on top, which is decoupled from the substrate [210]. This method is compatible with large surface and envisioned for epitaxial graphene .

2.3.4 Identification of graphene monolayer

To accompany the techniques used for the deposition of large-area graphene, characterization techniques must be developed to control the thickness and the quality of graphene layers. The techniques available at the moment include optical microscopy, electron diffraction, and raman spectroscopy. Identification techniques should ideally be nondestructive and ensure high throughput.

2.3.4.1 Optical microscopy

As a result of interference, optical microscopy can be used to identify graphene on top of Si/SiO_2 substrate. When the oxide layer thickness (eg. to 300 nm) and the light wavelength are finely tuned, the monolayer add to the optical path of the reflected light and become visible with a change of color with respect to the empty substrate [27]. However this method can only be used as observation as it's not precise enough.

2.3.4.2 Electron diffraction

Monolayer graphene can be identified by analysis of electron diffraction patterns. The normal-incidence diffraction pattern of a monolayer flake shows a typical sixfold symmetry [211, 212]. The peaks can be labeled with the Miller-Bravais (hkil) indices. In case of multilayer graphene, the (2110) spots appear more intense relative to the (1100) spots. This is characteristic of multilayers with Bernal (AB) stacking. The intensity ratio is $I_{(1100)}/I_{(2110)} < 1$, whereas it is superior to unity for a graphene monolayer. This allows us to differentiate monolayer graphene from multilayer graphene by inspection of the intensity ratio. On the diffraction pattern a line section is plotted through the (1-210)-(0-110)-(-1010)-(-2110) axis. If the inner peaks, (0-110) and (-1010), are more intense than the outer ones, (1-210) and (-2110), this indicates that the flake is a monolayer. Conversely, if the outer peaks are more intense than the inner ones, this corresponds to multilayer graphene. Experimental studies showed that the intensity ratios of $I_{(1100)}/I_{(2110)}$ are close to 1.4 for monolayer graphene and to 0.4 for bilayer graphene.

2.3.4.3 Raman spectroscopy

Raman spectroscopy provides with a non destructive and high throughput technique to control the number of layers of graphene since it has a clear signature in Raman spectroscopy and its spectrum evolves with the number of layers [38]. The Raman spectra at 514 nm is characterized by two distinctive features, the G peak at 1580 cm^{-1} and a 2D (also called G') band at 2700 cm^{-1}. The G peak is due to the doubly degenerate zone center E_{2g} and the 2D peak can be explained by the second order of zone-boundary phonons. There is a difference of shape and intensity of the peaks between graphene and bulk graphite. In bulk graphite the G peak is the most intense compared to the 2D band. The latter is actually the superposition of two components $2D_1$ and $2D_2$with an intensity of 1/4 and 1/2 the height of the G peak, respectively. Whereas single layer graphene present a single sharp 2D peak, which is 4 times more intense than the G peak. If the intensity of the G peak is comparable in both cases, an upshift of 3-5 $cm^{-1}$is observable in single layer graphene compared to bulk graphite. Observation of a D peak at 1350 cm^{-1}resulting from phonons indicates the presence of a number of defects. Absent in the center of graphene layers, this D peak can be observed at the sample edge. The splitting in two of the 2D band is confirmed in this D band. In comparison to single layer graphene, a bilayer has a broader and up-shifted 2D band, which is actually composed of 4 components: $2D_{1B}$, $2D_{1A}$, $2D_{2A}$ and $2D_{2B}$. $2D_{1A}$ and $2D_{2A}$ are more intense than the other two peaks. The intensity of the lower frequency $2D_1$ peaks decrease with increasing number of layers. For more than 5-10 layers, the spectrum is hardly distinguishable from that of bulk graphite.

2.3.5 Graphene properties in transistors

In graphene devices, both electron and hole transports can be induced by applying an electric field. This ambipolar transport is characterized by a "V" shaped transfer characteristic in transistors. The neutrality point or Dirac voltage (V_{Dirac}) is defined as the voltage at which the channel conductance reaches minimum and the on/off ratio (G_{max}/G_{min}) is the ratio between the maximum to minimum conductance [207].

2.3.5.1 Mobility

For transistor applications, one of the main advantage of graphene is its high carrier mobility at room temperature. Mobility of 70 000 cm^2/Vs was measured for mechanically exfoliated graphene on SiO_2 substrate using dielectric screening with a solvent dielectric ($\varepsilon_r \sim 47$) [32]. For large area graphene grown by CVD on Cu foil and transfered to SiO_2 substrates, a mobility up to 16 000 cm^2/Vs was reported and was attributed to the large domain size obtained by the two-step CVD process [33]. Epitaxial graphene on silicon carbide exhibit carrier mobilities as high as 15 000 cm^2/Vs [213]. This reported value corresponds to the mobility of graphene grown on the carbon face of SiC and is an order of magnitude higher than the value of epitaxial graphene grown on the silicon face. For epitaxial graphene, the mobility depends on the face on which the graphene is grown. Although the mobility of graphene grown on the carbon face was found to be higher, it is easier to grow single-layer or bilayer graphene on the silicon face.

For top-gate graphene transistors, mobility of around 23 000 cm^2/Vs was demonstrated using high-κ oxide nanoribbons as gate dielectrics [214]. The mobility was not even affected by the nucleation of the oxide dielectric on the pristine graphene. Previous efforts to fabricate top-gate graphene devices often resulted in significant degradation in carrier mobility.

Mobilities of 200 000 cm^2/Vs have been predicted [215] and a mobility of 10^6 cm^2/Vs was reported for suspended graphene [34], leaving room for improvement.

2.3.5.2 Bandgap

Large-area single-layer graphene is a semimetal with zero bandgap. Its valence and conduction bands are cone-shaped and meet at the K point of the Brillouin zone. Because of its zero bandgap, transistors with channel made of large-area graphene cannot be switched off. To be used in CMOS logic applications, transistors must have excellent switching properties: a small off current to reduce the static power dissipation and a large on-off ratio of 10^4-10^7. To be suitable for logic applications, transistors must have a semiconducting channel with a sizeable bandgap (> 0.4 eV). The use of graphene as the channel material in logic applications requires the generation and control of a bandgap. Opening of a bandgap in graphene can be realized following several techniques including cutting graphene into nanoribbons [39, 40], apply a back gate bias to a bilayer graphene [41], plasma O_2 treatment [42], hydrogen

surface treatment [43] or through particular interactions with the substrates [44].

For graphene nanoribbons (GNRs), the bandgap (E_g) is inversely proportional to the width (w) of the nanoribbon and was approximated as [40]:

$$E_g\,(eV) = \frac{0.8}{w\,(nm)} \tag{2.13}$$

Nanoribbons with width down to 1 nm and bandgap exceeding 200 meV were fabricated [40, 39, 216]. Li et al. prepared from solution-phase well-defined ribbon structures with ultrasmooth edges [40]. Using sub-10 nm graphene nanoribbons, p-type devices were demonstrated with a mobility of 200 cm^2/Vs and a on/off ratio of 10^6. The on/off ratio increases exponentially with the bandgap energy. Jiao et al. reported a mobility of 1500 cm^2/Vs for a nanoribbon 14 nm wide, which is the highest mobility so far for a nanoribbon [216]. Similarly to conventional semiconductors, the mobility of graphene nanoribbons tend to decrease with increasing bandgap. This means that for a bandgap similar to that of silicon (1.1 eV), the mobility of graphene nanoribbons would be lower than that of silicon in conventional MOSFETs. Therefore opening a bandgap in graphene come at the expense of reducing the high mobility offered by graphene, and thus its speed of device. Development of processing methods to produce narrow nanoribbons with well-defined smooth edges is crucial to implement GNRs in conventional FETs. The electronic properties of nanoribbons are very sensitive to a change in width along their lengths, edge geometry [217], and/or edge functionalization [218].

Bilayer graphene is gapless and its valence and conduction bands have a parabolic shape near the K point. When applying an electric field perpendicular to the bilayer, a bandgap opens and the bands take on the so-called Mexican-hat shape. The bandgap depends on the strength of the electrical field. Bandgap energy of 200-250 meV and on-off ratio of 5-10 were achieved with bilayer graphene [219, 220].

A bandgap can also be generated by surface treatment. Nourbakhsh et al. reported a bandgap of 2 eV for graphene treated with O_2plasma [42]. The opening of the bandgap, which increases with increasing oxygen density, can be tuned carefully by the plasma duration time. Upon functionalization of single-layer graphene with oxygen, devices exhibit a unipolar p-type behaviour with a current modulation of $I_{on}/I_{off} \sim 3$. Balog et al. showed that the patterned absorption of hydrogen on graphene resulted in a gap opening of 450 meV [43].

2.3.5.3 Frequency

Owing to its high carrier mobility, graphene shows great promise for radiofrequency (RF) applications. Cut-off frequencies as high as 100-300 GHz were demonstrated. However the radiofrequency performance of graphene are limited by two factors: the weak saturation of the drain current and the high contact resistance.

For RF applications, switching off devices is not so crucial. In small-signal amplifiers, the transistor operate in the on state and small radiofrequency signals are

superimposed onto the dc gate-source voltage. For radiofrequency devices, the figure of merit is the cut-off frequency (f_T), defined as the frequency at which the magnitude of the small-signal current gain ($|h_{21}|$) rolls off to unity. This is the highest frequency at which the signal is propagated. The cut-off frequency can be expressed as:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})[1 + g_{ds}(R_S + R_D)] + C_{GD} g_m (R_S + R_D)} \tag{2.14}$$

where $g_m = \left(\frac{dI_D}{dV_{GS}}\right)_{V_{DS}=cste}$ is the transconductance, $g_{ds} = \left(\frac{dI_D}{dV_{DS}}\right)_{V_{GS}=cste}$ is the drain conductance, C_{GS} is the gate-source capacitance, C_{GD} the gate-drain capacitance, R_S and R_D are the source and drain series resistance, respectively. The cut-off frequency can be maximized by making the transconductance as large as possible and making the drain conductance, all the capacitances and resistances as small as possible. This requires short gates, fast carriers and lower series resistance. Beyond the high mobility offered by graphene, one of its most attractive feature is the possibility of having channel that are only one atomic layer thick. Graphene is therefore an ideal solution to minimize short-channel effects at short gate lengths. For short channel devices, the cut-off frequency has a 1/L dependence, where L is the gate length, indicating that the transport is contact limited. Whereas a $1/L^2$ scaling trend is observed for graphene FETs with long gate length where the transport is rather channel-resistance limited. Besides the cut-off frequency, the maximum oscillation frequency (f_{MAX}), which is the frequency at which the power gain is equal to one, is an other important parameter for radiofrequency devices. It depends significantly on the design of the device and interconnects.

With very high carrier mobility, graphene transistors have the capacity to operate at very high frequencies, up to hundreds of gigahertz. The cut-off frequencies of high-speed graphene transistors reported in the litterature are summarized in table 2.1. Lin et al. demonstrated a cut-off frequency of 100 GHz for a gate length of 240 nm for devices based on epitaxial graphene grown on silicon carbide [221]. Wu et al. reported a cut-off frequency of 155 GHz for a CVD graphene transistors with a

Table 2.1: Summary of performance parameters reported in the literature for high frequency graphene transistors.

Fabrication	L (nm)	μ (cm^2/Vs)	f_T (GHz)	f_{MAX} (GHz)	V_{DS} (V)	Ref.
Epitaxy on SiC	240	1500	100	10	2.5	[221]
Epitaxy on SiC	550	1500	50	14	2.5	[221]
CVD on Cu foil	40		155	20		[35]
CVD on Cu foil	140		70	13		[35]
CVD on Cu foil	550		26			[35]
Mechanical Exfoliation	144		300	2.4	1	[222]
Mechanical Exfoliation	182		168	1.9	0.3	[222]
Mechanical Exfoliation	210		125	1.6	1.1	[222]

gate length scaled down to 40 nm [35]. A 1/L dependence of the cut-off frequency was observed for devices with channel length ranging from 40 nm to 550 nm. The fastest graphene transistor is a mechanically exfoliated graphene transistor with a self-aligned nanowire gate [222]. A cut-off frequency of 300 GHz was reported for a 140 nm device. The channel length is defined by the diameter of the nanowire. This self-alignement process ensure that the edges of the source, drain and gate electrodes are precisely positioned so that no overlapping or gap exist between these electrodes, thus minimizing the contact resistance. These results overcome the performance of the best silicon MOSFETs for similar gate length (~ 40 GHz at 240 nm).

2.3.6 Interface engineering of graphene

Graphene FETs based on SiO_2 dielectric have shown undesired effects like unintentional doping, Dirac voltage hysteresis, carrier mobility degradation and/or Dirac voltage shift under operation over long period times. These electrical instabilities hamper the operation of the device. In order to reduce these undesired effects and instabilities, graphene/dielectric interface engineering was reported using self-assembled monolayer [54, 53, 52, 223] or polymer layers [224][1, 7-8]. Table 2.2 summarizes the carrier mobilities and threshold voltages reported in the literature for graphene transistors based on bare SiO_2 and SAM treated SiO_2 as the gate dielectric.

p-doping is frequently observed in graphene transistors based on bare SiO_2 dielectric. Various chemical absorbates can attach to the SiO_2 surface due to the formation of hydrophilic silanol (SiOH) groups [225]. Dipolar molecules such as water are absorbed to the surface and contribute to charge transfer, resulting in doping of the graphene layer (p-doping in the case of water molecules) [226]. The hysteresis effect can also be explained by the presence of the silanol groups and absorbates.

Interface engineering of graphene transistors by self-assembling a molecular monolayer onto the SiO_2 surface is a key strategy to reduce these undesired effects. Liu et al. improved the performance and reliability of CVD graphene transistors employing 4-phenylbutyl trichlorosilane (PBTS) as the self-assembled monolayer [54]. The mobility was enhanced up to 2500 cm^2/Vs with the phenyl-terminated organosilane SAM, in contrast with the value of 1000 cm^2/Vs obtained without SAM. This improvement was attributed to the ultra smooth SAM surface, which reduces interface impurities and interfacial polar phonon coupling. For bare SiO_2substrate, large hysteresis (>25 V) were observed to be clockwise on the electron branch and anticlockwise on the hole branch. The negligible hysteresis of the phenyl-SAM engineered graphene FETs suggests that the charge injection from graphene to the dielectric interface was mostly suppressed by the SAM interface engineering. CVD graphene FETs with the phenyl-SAM exhibit also better reliability under bias stress. The Dirac point shift can be described by a stretched exponential model and is more pronounced in devices without the SAM interface engineering. After a stressing time of 1000 s, the Dirac point shift is reduced to 5 V with the SAM interface engineering, compared to more

Table 2.2: Summary of performance parameters reported in the literature for graphene transistors based on bare SiO_2 and on SiO_2 treated with different SAMs.

Reference	Substrate	Carrier mobility (cm^2/Vs)	Dirac point (V)
[54]	SiO_2-PBTS	2 500	40
[54]	SiO_2	1 000	40
[52]	SiO_2-HMDS	12 000	<10
[52]	SiO_2	4 000	>50
[53]	SiO_2-OTMS	47 000	5
[53]	SiO_2	5000	50
[223]	SiO_2-H_2N	661	-18
[223]	SiO_2-CH_3	460	-8
[223]	SiO_2	449	4
[223]	SiO_2-H_3N^-	363	20
[223]	SiO_2-CF_3	450	30

than 8 V on bare SiO_2. This suggests that SAM interface engineering improves the quality of the interface by reducing significantly the number of trapping sites.

Lafkioti et al. employed hexamethyldisilazane (HMDS) SAM as the surface passivating layer in their mechanically exfoliated graphene transistors [52]. The use of hydrophobic self-assembled monolayer on top of the SiO_2 prevents the formation of silanol groups and the absorption of dipolar substances. Large hysteresis effect (>20 V) and high p-doping level (~ $4.2{\cdot}10^{12}$ cm^{-2}) had been observed on bare SiO_2. With the hydrophobic self-assembled monolayer on top of SiO_2, the hysteresis effect vanishes and the doping level was dropped drastically below $0.7{\cdot}10^{12}$ cm^{-2}. The HMDS treatment resulted also in an increase of mobility from 4000 cm^2/Vs to 12 000 cm^2/Vs. Similarly, Wang et al. modified the SiO_2surface with an octadecyltrimethoxysilane (OTMS) and obtained high-quality exfoliated graphene devices with a low intrinsic doping level (V_{Dirac} ~ 5 V) and a mobility of 47 000 cm^2/Vs, which is almost one order of magnitude higher than that of devices on bare SiO_2 [53]. The hysteresis was suppressed with the SAM treatment. These enhancements were explained by the reduction of the density of charged impurities and remote interface phonon scattering.

Interface engineering with self-assembled monolayer provide with an efficient method to modulate the electronic properties of graphene. Controllable doping of graphene FETs, either p-type or n-type, can be realized by functionalizing the SiO_2 substrate with different SAMs. Using SAMs with different end groups, Yan et al. were able to tune the Dirac point over a wide range, from -18 V (n-doping) to 30 V (p-doping), without affecting the mobility of the graphene layer [223]. This doping arises from built-in electric dipoles and charge transfer between SAMs and the graphene channel. Compared to other doping techniques such as boron or nitrogen substitution and physical or chemical absorption of small molecules, this approach has the advantage of being stable and having limited effect on the mobility.

The surface of SiO_2 dielectric can also be modified by using passivating polymer

layer. Levesque et al. deposited a hydrophobic parylene-C (170 nm thick) layer on top of the SiO_2 dielectric to reduce the p-doping effect of graphene in ambient air [224]. Mechanically exfoliated graphene FETs based on bare SiO_2 dielectric showed large Dirac point shift by 15 V towards more positive gate voltage when exposed to ambient atmosphere, whereas no visible doping effect by air was observed for parylene-treated devices. The presence of molecular absorbates or difference of metal work function were excluded to explain this doping effect. To understand the underlying mechanisms that lead to this tunable doping, the FETs were exposed to the main atmospheric constituents. For bare SiO_2, they observed no shift when exposed to O_2 or N_2, a negative shift in presence of water (only) and a shift similar to that of air when exposed to both O_2 and H_2O. Negligible shift were reported in the case of parylene-treated FET. These shifts were attributed to the charge transfer between the graphene layer and the water/oxygen redox system, following the Marcus-Gerischer model [227]. The local electrochemical potential can be probed through the measurements of the Dirac point. This study shows also that graphene is a sensitive surface probe that can be used as a gas sensor.

2.4 Field-effect transistors and electronic circuits

The invention of the transistor 65 years ago triggered the digital revolution that we live today. Many applications and devices powered by transistors have impacted the way we work, we live and we play over the past 60 years. As the building block of computer chips, transistors can be found in computers, mobile phones, cars, household appliances, smart cards, etc. Transistors are mainly used in digital electronics for microprocessors or memories as well as analogue electronics for signal amplification and/or power device. A field-effect transistor is a voltage-driven device. It is composed of three electrodes: the source, the drain and the gate. The current between the first two contacts is modulated by the potential applied at the latest one.

The first transistor, a germanium point-contact transistor, was invented by John Bardeen, William Shockley and Walter Brattain in 1947 at Bell labs. All three were awarded the Nobel prize in Physics in 1956. However the idea of the field-effect transistors dates back to 1926 when Julius Lilienfeld proposed a method to control the magnitude of an electrical by applying an external electrical field. Although a patent was granted, no functioning transistors was demonstrated at that time. The metal-oxide-semiconductor field-effect transistor (MOSFET) based on single-crystal silicon, still the most used nowadays in digital electronics for the complementary (CMOS) logic, was first fabricated in 1959.

Since the fabrication of the first integrated circuit (IC) in the 1960 by Jack Kilby and Robert Noyce, the device features have scaled down (32 nm manufacturing technology) and the density of transistors on a chip has increased exponentially fueled by Moore's Law, a prediction made by Intel co-founder Gordon Moore in 1965, which states that the number of transistors on a chip would double about every 18 months.

As this prediction about the semiconductor industry still holds true today, microprocessors are more highly integrated, computationally powerful and interconnected. However, for inorganic materials such as silicon and germanium, manufacturing techniques used to fabricate such circuits become more and more complex and expensive when large areas need to be covered.

In 2000, Jack Kilby and Robert Noyce were awarded the Nobel Prize in Physics for “the invention of the integrated circuit” while Alan Heeger, Alan MacDiarmid and Hideki Shirakawa received the Nobel Prize in Chemistry for “the discovery and development of conductive polymers". The occurrence of these two events the same year could well suggest the transition underway in the semiconductor industry. Organic semiconductors have been studied for almost 50 years. In 1963, Pope and Kallman discovered the electro luminescent properties of small molecules [3, 228]. Fourteen years later Chiang and Shirakawa reported the electrical conductivity of polymers [2]. However it's only in the last 25 years that organic materials have attracted great interest for their potential in optoelectronic applications. The initial demonstration of OLEDs in 1987 [6, 7] and OFETs in 1983 [229, 230, 10]. Based on either conjugated polymers [229] or small molecules [11], both hole and electron transporting transistors can be fabricated. Great progress has been achieved over the last ten years and field-effect mobility up to 10 cm^2/Vs have been reported with not only evaporated semiconductors [12, 13] but also solution-processed semiconductors [14, 15]. Their high performance and easy fabrication techniques make OFETs a viable and practical technology and opens up a wide range of novel applications.

Electrical field-effect in graphene was first observed in October 2004 by Andre Geim and Konstantin Novoselov [27]. Even though this two-dimensional material had been studied theoretically since the 50's [194], it was presumed not to exist for some thermodynamically stability reasons [231], until the group in Manchester prepared a graphene layer from mechanical exfoliation. Only six years later, they were awarded the Nobel prize in Physics "for groundbreaking experiments regarding the two-dimensional material graphene". Graphene hold great promises in logic and radiofrequency applications due to its high carrier mobility. With a mobility of 70 000 cm^2/Vs [32] and a cut-off frequency of 150 GHz [35], the performance of graphene transistors overcome those of the best silicon MOSFETs. This makes graphene a promising candidate for the next generations of optoelectronic applications.

2.4.1 Thin-film transistor architectures

An organic field-effect transistor consists of a semiconducting layer, a dielectric and three electrodes: the gate (G), the drain (D) and the source (S). The source and drain electrodes are separated by the semiconducting layer. The distance between the two electrodes is called the channel length (L) and the width of the electrodes is termed the channel width (W). Insulated from the semiconducting layer by a dielectric film, the gate electrode is used to modulate the conductivity of the source-drain channel.

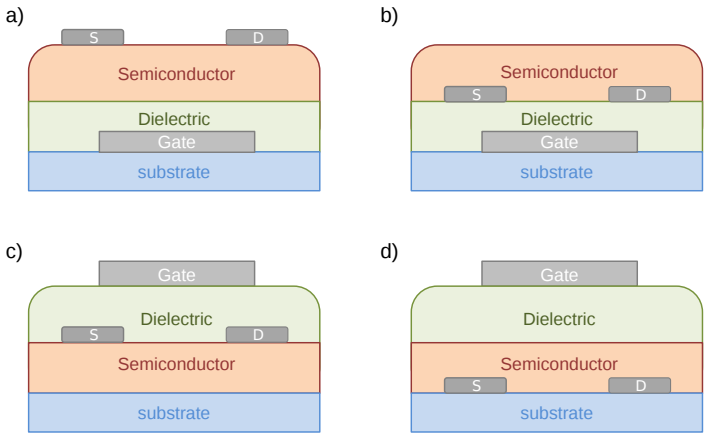

Figure 2.7: Bottom-gate top-contact (a), bottom-gate bottom-contacts (b), top-gate top-contacts (c) and top-gate bottom-contacts (d) transistor architectures.

As shown on figure (2.4.1), four main architectures are reported: bottom-gate top-contact (BG/TC), bottom-gate bottom-contacts (BC/BG), top-gate top-contacts (TG/TC) and top-gate bottom-contacts (TG/BC). The performance of the devices, fabricated with the same materials, can change from one architecture to another. Several reasons can explain these differences, such as: charge injection efficiency into the conducting channel. BC/BG and TG/TC devices are coplanar devices, therefore charges are directly injected into the channel whereas, the other two (TC/BG and BC/TG) are staggered and charges have to go through the semiconductor layer before reaching the channel [232]; morphology of the semiconductor-dielectric interface and the semiconductor-electrode interface [233]; formation of trap states during metal evaporation on organic semiconductor for top contact devices [232].

2.4.2 Operating principle of thin-film transistors

2.4.2.1 Operating regimes

The field-effect transistor is a voltage device in which the current in a conducting channel between the source and the drain is controlled by a voltage applied to the gate. Like in a metal insulator semiconductor (MIS) structure, a voltage is applied to the gate electrode while the source and drain are grounded. For a positive (negative) gate voltage, electrons (holes) are injected from the source into the semiconductor and accumulate at the semiconductor-insulator interface. To form an homogeneous channel at the interface, the gate voltage must reach a critical threshold voltage (V_T). The latter takes into account the difference of work function between the gate electrode and the semiconductor, the trapped carriers in localized states and the free charges due to impurities [56], leading to the following equation:

$$V_T = \phi_M - \phi_S - \frac{Q_i}{C_i} \tag{2.15}$$

where ϕ_M and ϕ_S are respectively the work functions of the metal electrode and the semiconductor, Q_i represents the trapped charges at the interface and C_i is the insulator capacitance per unit area.

Let us consider a n-type transistor whose source electrode is grounded. Note that a p-type transistor would behave in pretty much the same way but with voltage polarity reversed. Below the threshold voltage, the device is said to be operating in *the cutoff* regime: the device is turned off and there is no mobile charge that can migrate. When the gate voltage is greater than the threshold voltage ($V_G > V_T$; for V_G and V_D when not mentioned the potential is referred to the source), the device is switched on and a conductive channel forms between the source and drain. When a small drain voltage V_D is applied, charges are injected from the source, migrate along the channel and are absorbed into the drain. The channel current flow I_D is proportional to the drain voltage V_D and the transistor acts as a linear resistance. That is why this mode of operation is called *linear*. The drain current I_D is also proportional to the gate voltage V_G since the accumulated carriers at the semiconductor-insulator interface is proportional to the gate voltage. In the channel, the charge density decrease linearly from the source to the drain as the local voltage distribution decrease ($V_G > V_{GD}$). If V_D becomes sufficiently large such that $V_{GD} < V_T$, the channel is *pinch off*: the region near the drain electrode is depleted. Beyond this drain voltage $V_{D(sat)} = V_G - V_T$, as the charges reach the end of the channel, they are accelerated through the depleted region toward the drain thanks to the additional electric field ($V_D - V_{D(sat)}$) applied between the pinch off point and the drain. The drain current I_D is now independent of the drain voltage V_D and is controlled only by the gate voltage V_G. This mode of operation is called *saturation* regime.

2.4.2.2 Current-voltage characteristics

The current-voltage characteristics of the field-effect transistors is derived by using the gradual channel approximation [56, 232]. According to the latter theory, the electric charge density is more sensitive to a variation of the electric field across the channel ((Oy) direction) than a variation along the channel ((Ox) direction). In other words, the transport along the (Ox) direction does not influence the charge distribution along (Oy) distribution and (Ox) and (Oy) directions are dealt separately. The drain current is the total amount of mobile charge ($Q_{channel}$) accelerated to a velocity v, which is proportional to the lateral electric field $F = -\frac{dV}{dx}$, and is given by:

$$I_D = -Q_{channel}.\mu.W\frac{dV}{dx} \tag{2.16}$$

where μ is the mobility of carriers that is assumed to be constant and W is the channel width. The total amount of charge in the channel is:

$$Q_{channel} = -C_i[V_G - V_T - V(x)] \tag{2.17}$$

where $V(x)$ is the local voltage at the dielectric-semiconductor interface. By using equations (2.16) and (2.17) and integrating over the channel length, the drain current is given by:

$$I_D = \mu\ C_i \frac{W}{L}(V_G - V_T - \frac{V_D}{2})V_D \tag{2.18}$$

The I-V characteristic can be simplified in the three regimes of operation as:

$$I_D = \begin{cases} 0 & \text{if} \quad V_G < V_T, & & & \text{cutoff;} \\ \mu C_i \frac{W}{L}(V_G - V_T)V_D & \text{if} \quad V_G > V_T & \text{and} & V_D < V_{D(sat)}, & \text{linear;} \\ \mu C_i \frac{W}{2L}(V_G - V_T)^2 & \text{if} \quad V_G > V_T & \text{and} & V_D > V_{D(sat)}, & \text{saturation.} \end{cases} \tag{2.19}$$

At a given linear drain voltage, the linear mobility can be deduced from the transconductance as:

$$\mu_{lin} = \frac{L}{WC_iV_D} \cdot \left(\frac{\partial I_D}{\partial V_G}\right)_{V_{D_{lin}}} \tag{2.20}$$

At a given saturation drain voltage, the saturation mobility is calculated as:

$$\mu_{sat} = \frac{L}{WC_i} \cdot \left(\frac{\partial^2 I_D}{\partial V_G^2}\right)_{V_{D_{sat}}} = \frac{2L}{WC_i} \cdot \left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2_{V_{D_{sat}}} \tag{2.21}$$

Finally the threshold voltage can be extracted from the plot of the square root of the drain current ($I_D{}^{1/2}$) versus the gate voltage (V_G) for a saturation drain voltage as the drain current depends quadratically on the gate voltage in the saturation regime.

The density of traps can be estimated using two methods, the first one being based on the threshold voltage and the other on the subthreshold slope. As mentioned before (see equation 2.15), the threshold voltage (V_{ON}) corresponds ideally to the difference of work function between the semiconductor and the gate electrode (also called flat-band potential). However, in a real transistor, the presence of localized trap states that can donate or accept carriers leads to a shift of the threshold voltage (compared to the flat-band value). If these trap states need to be filled before the transistor channel reaches its on state, a positive (negative) shift is observed for n-type (p-type) channels. On the contrary if at $V_G = V_{FB}$ additional free charges must be depleted from the channel so that the device is turned off, this would correspond to a negative (positive) shift for n-channel (p-channel) transistors. Considering that the voltage shift between the onset voltage (V_{ON}) and the real threshold voltage (V_T) is induced by charge trapping, the areal concentration of filled traps (N_{tr}) can be estimated as:

$$N_{tr} = \frac{C_i \mid V_T - V_{ON} \mid}{e} \tag{2.22}$$

With decreasing temperature, the Fermi level shifts towards the transport level, meaning that a higher concentration of traps needs to be filled before thermal acti-

vation to the transport level. The density of trap states (D_{tr}) is then expressed as a variation of threshold voltage with temperature [133]:

$$D_{tr} = \frac{\partial Ntr}{\partial E} = \frac{C_i}{ek}\frac{\partial V_T}{\partial T} \tag{2.23}$$

Another method to estimate the trap density is based on the subthreshold slope (SS) of a transistor, which is defined as the gate voltage required to increase the drain voltage by a factor of ten (calculated at voltages below the threshold voltage).

$$SS = \frac{\partial V_G}{\partial(logI_D)} \tag{2.24}$$

This parameter indicates how quickly the device changes from the off state to the on state. The minimal value (no charge trapping) at room temperature is 60 mV/dec. The maximum value for the density of interface traps is given by [234]:

$$D_{tr}^S = \frac{C_i}{e^2}\left(\frac{e\,SS}{kTln(10)} - 1\right) \tag{2.25}$$

Noteworthy this estimation is only valid for transistors with a high current on/off ratio. On the other hand, for transistors with a high off current (high film conductivity), trap states from the bulk contributes also to the subthreshold slope.

2.4.2.3 Ambipolar transport regimes

Ambipolar transistor are able to accumulate and conduct both electrons and holes. The type of carriers accumulated in the channel depends on the bias conditions. These different operating regimes observed in ambipolar transistors are illustrated on figure 2.8. When $V_{GS} > V_{T,e}$ and $V_{GS} > V_{DS} + V_{T,h}$ (the subscript h and e refer to holes and electrons, respectively), the current is carried by electrons in the channel (1). Similarly, when $V_{GS} < V_{T,h}$ and $V_{GS} < V_{DS} + V_{T,e}$, only holes are injected from the source electrode into the channel (4). When $V_{GS} > V_{T,e}$ and $V_{DS} < 0$, the effective gate potential is positive throughout the whole channel, the transistor operates as a unipolar n-type transistor where the source and drain are inverted (6). Similarly, when $V_{GS} < V_{T,h}$ and $V_{DS} > 0$, the effective gate potential is negative and the transistor is operating in a unipolar reversed p-type regime (3). Finally, when $V_{GS} > V_{T,e}$ and $V_{GS} < V_{DS} + V_{T,h}$ (2) and when $V_{GS} < V_{T,h}$ and $V_{GS} > V_{DS} + V_{T,e}$ (5), holes and electrons accumulate at opposite sides and contribute to the channel conductivity. Under these circumstances, the transistor operates in the *ambipolar regime*. Hole- and electron accumulated layers are both pinched off (saturation regime). At the position where the effective gate potential changes sign (called the pinch off point), a p-n junction is formed separating the two accumulation regions.

According to the different models developed for ambipolar transistors [235, 117, 232], the transistor channel is considered as an electron channel of length L_e and a hole channel of length L_p in series. Thus the total channel length is assumed to be the sum of the channel lengths of the two layers ($L = L_e + L_h$) and the total current

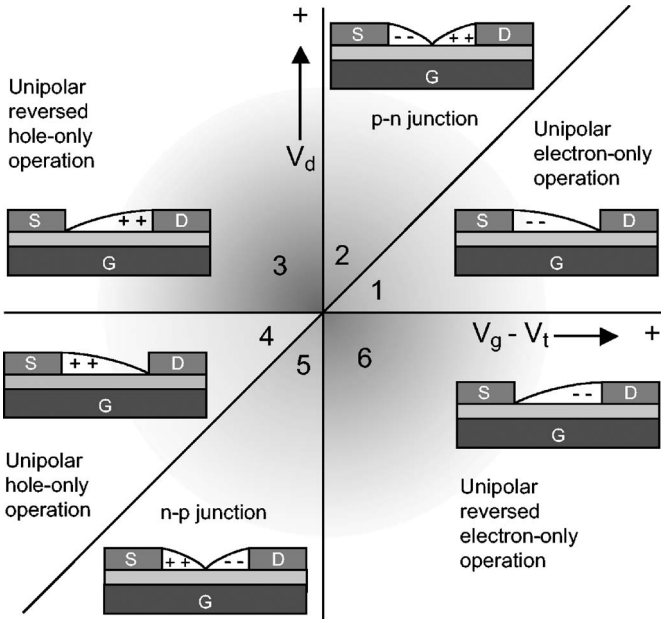

Figure 2.8: Schematic of all operating regimes for an ambipolar transistor as a function of drain and gate biasing [235].

is equal to the electron or the hole currents ($I = I_e = I_h$). The current-voltage characteristics of an ambipolar organic transistors can described as:

$$\mid I_{DS} \mid = \frac{WC_I}{2L}[\mu_e(V_{GS} - V_{T,e})^2 + \mu_h(V_{DS} - (V_{GS} - V_{T,h}))^2] \tag{2.26}$$

To obtain this expression, voltage-dependent mobility and non-ideal contacts are discarded in the model.

In the vicinity of the pinch off point, where the two accumulation layers meet, electron and hole recombine, resulting in light emission in electroluminescent materials. The recombination point depends on the applied gate and drain voltages, the threshold voltages and mobility ratio. Its coordinate along the channel is found to be:

$$x_0 = \frac{L(V_{GS} - V_{T,e})^2}{(V_{GS} - V_{T,e})^2 + \frac{\mu_h}{\mu_e}(V_{DS} - (V_{GS} - V_{T,h}))^2} \tag{2.27}$$

The assumption of an infinite recombination rate at the meeting point is rather unrealistic. This implies a charge density of zero at the meeting point and non overlap of the two layers. However it would make more sense to model a finite recombination over a certain region width. That means that holes and electrons penetrate into each other's accumulation layers before recombining.

The transfer curve of ambipolar transistors has a V-shape with the right arm corresponding to the electron transport and the left to the hole transport. For positive drain, an increase of the drain current is observed on the hole branch with increasing drain voltage. Similarly, a current increase is noticeable on the electron branch

when decreasing the source-drain voltage towards more negative voltages. The output curves are composed of the standard saturation flat-plateau behavior at high gate voltages (injection of one carrier) and the superlinear current increase at low gate voltages and high drain voltages (injection of the other carrier at the other electrodes).

In ambipolar transistor, a major issue is to get efficient injection of both charge carriers [232]. Optimal electron injection is obtained when the work function of the metal electrode lines up with the LUMO level and optimal hole injection occurs when the work function is aligned with the HOMO level. However these two conditions cannot be fulfilled in the meantime since the band gap in organic semiconductors is typically 2-3 eV. Hence for any given electrode material, the injection is limited for at least one carrier. An alternative is to select an electrode material whose work function is around the mid gap but the injection is not yet optimal because the injection is limited at both ends. Hence only narrow band gap materials can demonstrate efficient ambipolar injection in transistors.

2.4.3 Electrical stability of organic field-effect transistors

If much effort has been devoted to developing organic transistors with high field effect mobility, the good environment stability of these devices over time is also of paramount importance for the successful implementation of the technology. The stability of devices after extended operation is also crucial for the good use and reliability of the electronic devices and circuits. Therefore a good understanding of the origin of any instability is important to counteract this possible flaw. So far the literature related to electrical stability of OTFTs has been rather limited [236, 237, 238].

When studying the reliability of transistors, one of the main instability is certainly the shift of the threshold voltage when applying a prolonged gate bias, known as the bias stress effect. When applying a negative gate voltage to p-type transistor, the threshold voltage shifts toward more negative values whereas application of a positive voltage to a n-type transistor leads to a threshold voltage shift toward more positive values. Device degradation is also characterized by an increase of the subthreshold slope, an increase of the OFF current, a reduction of the mobility and/or increased hysteresis. In most cases, the effect is reversible, in other words the threshold voltage shift back toward its initial value while grounding the gate electrode. It is also possible to bias stress the device into the off-state, that is to say applying a positive voltage to a p-type transistors or a negative voltage to a n-type transistors, leading to a shift of the threshold voltage towards the applied gate voltage.

Among the origins of electrical instability are charge trapping in the semiconductor or at the interfaces, ionic displacements in the dielectric as well as structural changes. Assuming that the threshold voltage shift results from charge trapping, the threshold voltage shift $\Delta V_T(t)$ is given by:

$$\Delta V_T(t) = \frac{eN_{tr}(t)}{C_i} \tag{2.28}$$

where $N_{tr}(t)$ is the charge surface density, C_i is the capacitance of the gate dielectric and e the elementary charge. The rate at which the charges are trapped depends on the free-carrier density N_f. For an exponential distribution of trap states, the trap state is expressed as [238]:

$$\frac{dV_T}{dt} \propto \frac{dN_{tr}}{dt} \propto N_f(t)\frac{t^{\beta-1}}{\tau^{\beta}} \tag{2.29}$$

where τ is a characteristic time constant, the dispersion coefficient $\beta = \frac{T}{T_0}$ and T_0 the characteristic temperature of the trap states. By solving 2.29, the threshold voltage shift is found to be a stretched exponential function[238, 236]:

$$\Delta V_T(t) = \big[V_T(t=\infty) - V_T(t=0)\big]\big[1 - e^{(-\frac{t}{\tau})^{\beta}}\big] \tag{2.30}$$

where $V_T(t=0)$ is the threshold voltage in the initial state, $V_T(t=\infty)$ is the threshold voltage at equilibrium, τ is the time constant and β is the stretching parameter ($0 < \beta \leq 1$). First introduced by Rudolph Kohlrausch in 1854 to describe the time-dependent discharge of capacitors [239], this stretched exponential function is also useful to explain the reliability in amorphous silicon and organic [238, 240] thin film transistors. This empirical function describes time-dependent processes that are not completely exponential but depends exponentially on a distribution of time constants. Due to this distribution of time constants, the response is faster-than-exponential in the first part of the process (for times up to the time constant) and slower-than-exponential in the later part (for times beyond the time constant). The stretching parameter β corresponds to the diversion from the exponential function. A stretching parameter β close to 1 indicates a narrow distribution of time constants, while a stretching parameter smaller than 1 implies a broader distribution of time constants. The relaxation time is thermally activated as:

$$\tau = \nu^{-1} exp(\frac{E_a}{k_B T}) \tag{2.31}$$

where E_a is the mean activation energy for trapping and ν is a frequency prefactor.

The bias stress effect is often explained by charge trapping into localized states in the semiconductor, in the dielectric or at the semiconductor/dielectric interface. By applying a gate voltage, carriers that were initially mobile in the conduction channel are trapped into localized state and thus do not contribute to the drain current, resulting in a shift of the threshold voltage. In organic transistors, trapped carriers are usually released more or less rapidly into mobile states after removing the gate voltage. If they remain trapped, the bias stress induced threshold voltage shift can possibly be reversed by applying a bias into the off-state, by thermal annealing or/and by shining some light. For example, Salleo et al. suggested that the bias stress observed in the polymer poly-9,9' dioctyl-fluorene-co-bithiophene (F8T2) is due to hole charge trapping in the semiconductor. The formation of hole bipolarons was proposed as a

mechanism. The effect could be reversed by shining band gap radiation on the device [241]. Zschieschang et al. ascribed threshold voltage shift in low voltage pentacene transistor based on octadecylphosphonic acid (ODPA) self-assembled monolayer to charge trapping in the semiconductor due to the presence of water [240]. In the latter study the workers have shown that when applying a drain potential during gate bias stress, the equilibrium threshold voltage shift and the time constant τ were reduced with increasing drain-source voltage, suggesting that the drain potential does not only counteract the gate field near the drain electrode, and thus reduce the number of charge carriers available for trapping, but also creates a pathway for the fast release of carriers.

Based on the threshold voltage shift observed in their polytriarylamine (PTAA) transistors [238, 242], Sharma et al. suggested that the bias stress effect occurring in p-type transistors with SiO_2 dielectric is due to the migration of protons into the dielectric [242]. Protons are produced by electrolysis at the surface of the gate dielectric in presence of water and holes and diffuse into the gate dielectric while applying a continuous bias. According to this mechanism, the recovery process can also be explained by the reverse process, i.e. diffusion of protons back to the interface and conversion into holes.

2.4.4 Charge injection and contact resistance in organic field-effect transistors

The electrical performance of organic transistors usually suffers from large contact resistance. Several groups have shown that the contact resistance is typically greater than the channel resistance [243, 244]. This suggests that the bottleneck in the performance of OFETs may not be the intrinsic carrier mobility of the organic semiconductor, but rather the contact resistance of the transistor. That's why estimating the parasitic resistance is important to understand the effects of contacts.

In a transistor, the total resistance R_{ON} consists of the channel resistance and the parasitic resistance, $R_p = R_s + R_d$. At the source and drain, the contacts are assumed to be ohmic and independent of the channel length.

$$R_{ON}(L) = \left(\frac{\partial V_{DS}}{\partial I_{DS}}\right)_{V_{DS}\to 0} = R_{ch}(L) + R_p \tag{2.32}$$

The contact resistance in the current-voltage characteristics can be taken into account by substituting V_D with $V_D - R_p I_D$ in equation 2.18 and assuming that the term $V_D/2$ can be neglected. Thus the I-V characteristic can be rewritten as:

$$I_D = \frac{V_D}{R_p + \frac{L}{W\mu C_i(V_{GS}-V_T)}} \tag{2.33}$$

Therefore, in the linear regime, the channel resistance is found to be:

$$R_{ch}(L) = \frac{L}{W\mu_i C_i(V_{GS} - V_{T,i})} \tag{2.34}$$

where μ_i and $V_{T,i}$ are the intrinsic mobility and threshold voltage, respectively. The channel resistance is proportional to the channel length while the parasitic contact resistance is assumed to be independent of the channel length. Therefore the relative influence of the contact resistance increases as the channel length is reduced. Thus studying the channel length dependence of the linear and saturation mobility gives some clues about the contact effects. Indeed an increase of mobility with increasing channel length is characteristic of contact resistance in a transistor whereas a decrease of mobility with increasing channel length implies that the charge transport is limited by defects [245].

From the linear region of the output characteristic, the total resistance R_{ON} is first computed, then the width-normalized resistance $R_{ON}W$ is plotted as a function of the channel length L for different gate voltages. The reciprocal slope $\left[\frac{\Delta(R_{ON}W)}{\Delta L}\right]^{-1}$, which is named the channel sheet conductivity, contains only intrinsic device parameters independent of the channel length.

$$\left[\frac{\Delta(R_{ON}W)}{\Delta L}\right]^{-1} = \mu_i C_i(V_{GS} - V_{T,i}) \tag{2.35}$$

In the linear fit of the channel sheet conductivity versus the gate voltage, the intrinsic mobility is obtained from the slope while the intrinsic threshold voltage corresponds to the x-axis intercept.

The parasitic resistance R_pW at the source and drain contacts can be estimated as the y-axis intercepts of the extrapolated linear fit of $R_{ON}W$ versus L since this point corresponds to the resistance at a channel length of zero (where the channel resistance disappears). This parasitic resistance depends on the gate voltage. All fitted lines meet at a single point which defines a characteristic length l_0 and a characterized normalized resistance $(R_pW)_0$. Luan et Neudeck explain, in their empirical model developed for amorphous silicon transistor [246], that the parasitic resistance can be regarded as a minimum effective contact resistance $(R_pW)_0$ in series with an accumulation channel of length l_0 under the source/drain electrodes.

$$R_pW = \frac{l_0}{\mu_C C_i(V_{GS} - V_{T,c})} + (R_pW)_0 \tag{2.36}$$

Thus the mobility and threshold voltage for the contact region can be extracted by fitting the R_pW versus V_G plot and using equation 2.36.

2.4.5 Logic circuits

Once the device is optimized and modeled, transistors can be implemented in electronic circuits. At the research level, when a novel material or a new processing technique is implemented in a transistor, it is important to demonstrate simple building blocks of electronic circuit such as logic gates (e.g. inverter, NAND gate, NOR gate and/or ring oscillator), to show its potential and compatibility with the development of integrated circuits.

2.4.5.1 The NOT gate

The NOT gate, also called voltage inverter, is the key element for logic operation that converts a high output voltage into a low output voltage and vice versa. The symbol and the truth table of an inverter are shown on figure 2.4.5.1 (a). Inverters can be used either as an amplifier in analog circuits, where the input voltage is set near the inverter threshold voltage V_{inv} for voltage amplification, or as a building block in digital circuits, in which the input voltage is switched between low and high levels (voltages). The performance of an inverter will depend greatly on the circuit logic. The two main logic are unipolar or complementary logics. The assembly of inverters according to these circuit logics are depicted in figure 2.4.5.1.

An inverter can be characterized through analysis of its DC transfer function, which presents the variation of the output voltage (V_{out}) as a function of the input voltage (V_{in}). This characteristic shows the transient step of the inverter from a low level to a high level and vice versa. The slope of the curve $\mid dV_{out}/dV_{in} \mid$ is defined as the gain. The crossover point where $V_{in} = V_{out}$ corresponds to the input threshold voltage V_{inv}.

The noise margin are a quantitative measure of the immunity of a logic circuit against electronic noise [247, 184]. It corresponds to the maximum noise voltage on the input of a gate so that the output will not be corrupted. The effective noise margin is the smallest value between the low noise margin (NM_L) and the high noise margin (NM_H) and is often compared to the maximal value it can be, which is half the supply voltage. The low noise margin (NM_L) is defined as the difference between the maximum low input voltage (V_{IL}) recognized by the receiving gate and the maximum low output voltage (V_{OL}) produced by the driving gate. The high noise margin (NM_H) is the difference between the minimum high output voltage (V_{OH}) produced by the driving gate and the minimum high input voltage (V_{IH}) recognized by the receiving gate. Any value between V_{IL} and V_{IH} is in the forbidden zone and does not represent a logic level. The noise margins are calculated by defining the logic levels at the unity gain point (slope is -1) in the transfer characteristic of the inverter. In order to get high noise margins, the transfer characteristic should be symmetric and present a high gain.

Switching short circuit currents and leakage currents through the transistors are sources of power dissipation in inverters. The latter depends on the loading capaci-

tance C_L, the supply voltage V_{DD} and the operating frequency f and can be given by [247]:

$$P_{diss} = C_L * V_{DD}^2 * f \tag{2.37}$$

As the power dissipation depends quadratically on the operating voltage, reduction of the latter in OFETs is important to decrease the overall power dissipation in organic circuits.

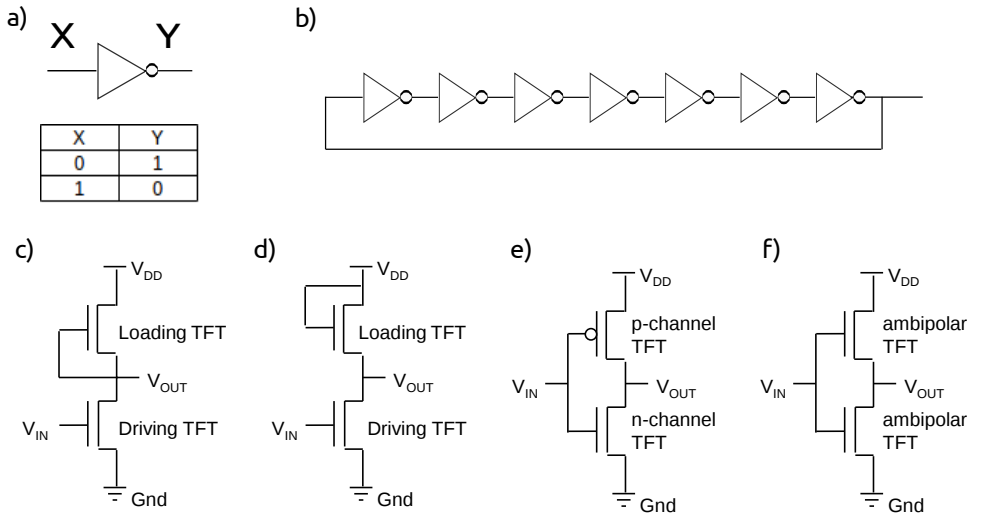

Figure 2.9: Inverter symbol and truth table (a). 7-stage ring oscillator (b). Unipolar "V_G= 0 V" inverter (c), unipolar diode load inverter (d), complementary inverter (e) and ambipolar complementary-like (f) inverter schematics.

2.4.5.2 Unipolar logic

A unipolar inverter is made of two transistors with the same charge carrier, either two p-type TFTs or two n-type TFTs. The two transistors can be associated either in unipolar V_G=0 V logic (a) or unipolar diode load logic (b), as shown on figure 2.4.5.1. In the first case the gate of the load transistors is connected to the output while in the second case the gate of the load transistors is railed to the supply voltage (V_{DD}). When the gate of the drive transistor (input of the inverter) is set to high, the drive transistor is on and overpower (the loaded transistor) and the output is pulled down to a low level. When the input is low, the drive transistor is off and the load transistor rules the output to a high level. A difference in on current or threshold voltage between the drive transistor and load transistor is necessary so that the inverter works properly. The main advantage of unipolar circuits is that both transistors can be easily fabricated on the same substrate since only one material is required for processing. However it has several problems in terms of operation such as low noise margins, low gain and high power dissipation.

2.4.5.3 Complementary logic

A complementary inverter is composed of a n-type transistor and a p-type transistor. Similarly to a complementary metal oxide semiconductor (CMOS) inverter, when the input X is low, the n-type transistor is off, the p-type transistor is on and thus the output is pulled up to high. Conversely, when the input is high, the n-type is on, the p-type is off and the output is pulled down to low.

Power dissipation in complementary inverters is dynamic and is due to charging and discharging the load capacitor. In steady state, only one of the transistor is on and the other one is off. But, when V_{inv} switches between ground and V_{DD}, both transistors are momentarily on, resulting in a pulse of current between power rails.

Both p-type and n-type transistors have a β coefficient defined as $\beta = \mu C \frac{W}{L}$. The *beta ratio* $\frac{\beta_p}{\beta_n}$ is an important feature for an inverter. If $\beta_p = \beta_n$, the inverter is said to be unskewed: the input threshold is $V_T^{in} = \frac{V_{DD}}{2}$, the noise margins is maximum and the times required to charge or uncharge a capacitive load are the same [247]. If $\frac{\beta_p}{\beta_n} > 1$, the inverter is HI-skewed: it has a stronger p-type transistor, its input threshold is higher than $\frac{V_{DD}}{2}$, whereas if $\frac{\beta_p}{\beta_n} < 1$, the inverter is LO-skewed: it has a stronger n-type transistor and a lower input threshold. Therefore the input threshold can be tuned by adjusting the beta ratio, hence the widths of transistors.

Complementary circuits are more challenging to fabricate as they require two different materials, one for the p-type pull-up network and one for the n-type pull-down network. Contrary to inorganic electronics, where the two networks are placed side by side by implantation of a n-well region into the p-substrate wafer, local deposition of both n-type and p-type organic semiconductors on the same substrates is difficult and results in parameter spreading and transconductance mismatch between the two materials. One alternative solution is the realization of complementary logic using two ambipolar transistors, as shown on figure 2.4.5.1 (f). This approach has the main advantage of simplifying the fabrication process by depositing a single semiconducting film and single type of electrode. Complementary circuits demonstrate also higher gains, wider noise margins and low power consumption. Despite few processing issues that still needs to be overcome, the organic electronic roadmap is definitely heading toward complementary logic circuit due to their promising performances.

2.4.5.4 The ring oscillator

The oscillation frequency and the propagation delay of transistors is obtained by testing ring oscillators. A ring oscillator is composed of an odd number of inverters in series. The output of each inverter is connected to the output of the following inverter and the output of the last stage is looped back to the input of the first one. Thus at any stage of the ring the logic state oscillates between the high and the low levels. The frequency (f_{osc}) of a n-stage ring oscillator depends on the stage delay (τ_d) as:

$$f_{osc} = \frac{1}{2n\tau_d} \tag{2.38}$$

Chapter 3

Experimental techniques

In this chapter, we review the different processing and characterization techniques that were employed to carry out this study. Processing of a material into a thin film is crucial for the device performance. Deposition of the semiconductor layer is all the more important in the fabrication of OFETs since the electronic transport, and hence the device performance, depends strongly on the degree of crystallinity and morphology of the semiconductor thin-film. Although thermal evaporation technique yield to higher degree of crystallinity and higher device performance, solution-processed deposition techniques such as spin-coating, inkjet printing or spray coating are promising for low-cost large-area applications. However solution-processing of small molecules is more challenging. The dielectric plays also a major role as it affects not only the charge transport at the semiconductor-dielectric interface through charge trapping and/or carrier scattering but also the morphology of the semiconductor film when the later is deposited on top. Furthermore deposition of metal contacts can not be neglected as injection of carriers from the source-drain electrodes to the semiconductor can hamper transistor characteristics if the energy barriers are too high. Therefore control of the surface roughness, surface energy and interface traps are of paramount importance for improving device performance.

This chapter describes the different deposition techniques used in this study, from thermal evaporation and spin-coating of organic semiconductor to functionalisation of self-assembled monolayer and chemical vapor deposition of graphene. Understanding the relationship between the charge transport and chemical or microstructural properties will be explored via electrical measurements, surface energy measurements, optical microscopy, and atomic force microscopy. Control of the grain size and thickness of graphene will be assessed through Raman spectroscopy. Finally transistors are implemented in basic integrated circuit to show their potential for practical applications.

3.1 Material and device processing

3.1.1 Deposition of thin-film by spin-coating

Spin-coating is processing method often used to deposit polymers or small molecules that are soluble in suitable solvents. The substrate is hold on the swivel of the spin-coater thanks to a vacuum pressure. Once the solution (100 μL) is poured on the sample surface, the turntable is set in motion. The speed, the acceleration and duration of the spin-coating are previously set on the instrument. While spinning, the solvent evaporates, leaving a thin semiconductor film on the substrate. [60]PCBM small molecules and P3HT polymer were diluted in chlorobenzene (at 20 mg/mL and 10 mg/mL, respectively) and spin-cast at a spin speed of 2000 rpm for 60 s. In the case of acene:polymer blend, the solution was spin-coated in a two-stage process: 500 rpm for 10 s followed by 2000 rpm for 20 s. The first low rotation stage allows for uniform crystallisation and better phase separation. For thick polymer films, like Cytop or Hyflon AD, the solutions were spin-coated at 2000 rpm for 60 s. The main advantages of spin-coating are the production of homogeneous film, the good control of the thickness and its low-cost process. The thickness of the layer depends on the viscosity of the solution, the spin speed, the boiling temperature of the solvent and the surface energy of the substrate. Unfortunately, not all organic molecules are soluble.

An alternative process to spin-coating is drop-casting. This is also a solution-based deposition processed. The solution is deposited on the substrate. The latter is lying on a hotplate, resulting in the evaporation of the solvent. However the deposited films obtained by drop casting are not as thin and homogeneous as with spin-coating process.

3.1.2 Evaporation of small molecules

Molecular vacuum evaporation is a deposition technique more suitable for small molecules. The problem with polymers is that they are likely to decompose at high temperature. Like for metal evaporation, under very high vacuum, the material is heated by Joule effect, evaporates and then condense and deposit onto the substrates. The main advantages of vacuum evaporation are the purity of the films and the good control of the thickness. The crystalline order of the film can be controlled by the deposition rate (typically 1 Å/s) and the substrate temperature. Even if this technique leads to devices with really high mobility, evaporation is a more expensive technique than spin-coating.

3.1.3 Evaporation of metal contacts

Vacuum evaporation of metals is a technique that is often used to make the electrical contacts. It is performed under high vacuum (10^{-6} mBar) in a bell jar. The samples and the shadow masks are placed in the upper part of the evaporation chamber. A metal wire is fastened to a coil or deposited in a boat. The temperature of the crucible

is of course higher than the boiling temperature of the metal. The metal is heated by Joule effect until it evaporates. The metal particles then condense onto the cold surfaces of the substrates.

According to the patterns defined by the shadow masks, a thin metal film is formed. In order to make sure that the metal starts to be deposited onto the substrates only once constant evaporation is reached and to avoid any contaminations from impurities, whose boiling temperature may be lower than the metal one, the substrates are momentarily protected from ballistic evaporation from the metal source using shutters. The latter are removed once the deposition rate is constant. The thickness and the speed of the deposition are controlled by a piezoelectric quartz, located at a position similar to the position of the substrates. The oscillation frequency of the quartz depend on the thickness of the deposited metal. The thickness of the metal films used were typically in the range 20-50 nm.

For diode fabrication, metal evaporation is used twice to deposit the two metal electrodes of the device. In case of organic transistors, metal evaporation occurs twice in the process to pattern the gate electrode and the source-drain contacts. A different set of shadow masks is employed for each evaporation. For source-drain contacts, the choice of the evaporated metal (e.g. aluminium, gold, calcium, etc.) depends on the semiconductor material. For example, gold (Au) is usually chosen when the semiconductor layer is a p-type material whereas aluminium (Al) is often selected for n-type semiconductor materials. The work function of the chosen electrode metal is adjusted to the HOMO or LUMO level of the semiconductor to reduce the barrier height energy and optimize the injection at the electrodes.

3.1.4 Deposition of self-assembled monolayers

Self-assembled monolayer were employed in our TFTs as the molecular dielectric on aluminium gate electrode or injection layer over conductive electrodes. In the first case, phosphonic acid SAMs such as octadecylphosphonic acid (ODPA), phosphonohexanoic acid (PHDA) or benzyloxyundecylphosphonic acid (BOUDPA) and fluorinated derivatives (the full range of molecules studied are described in chapter 5) were chosen for self-assembly on aluminium electrode. To realize bottom-gate TFTs, a 50 nm thick gate electrode is thermally evaporated on a pre-cleaned glass substrate. This electrode was then oxidized by exposure to oxygen plasma (30 s, 80W) to form a thin alumina layer ($\sim$ 5-10 nm thick). The monolayer is functionalized by submerging the substrate in a 5 mM solution of SAM in isopropanol and then rinsing with pure isopropanol. At this step, the molecules are spontaneously chemisorbed to the alumina surface and form a densely packed monolayer. The substrate are finally annealed overnight at 140°C under N2 atmosphere.

In the second case, fluorinated thiol SAMs were functionalized on gold source-drain electrodes to reduce the contact resistance. The molecules chosen for that purpose were pentafluorobenzene thiol (PFBT) or 3-fluorobenzene thiol (3-FBT).

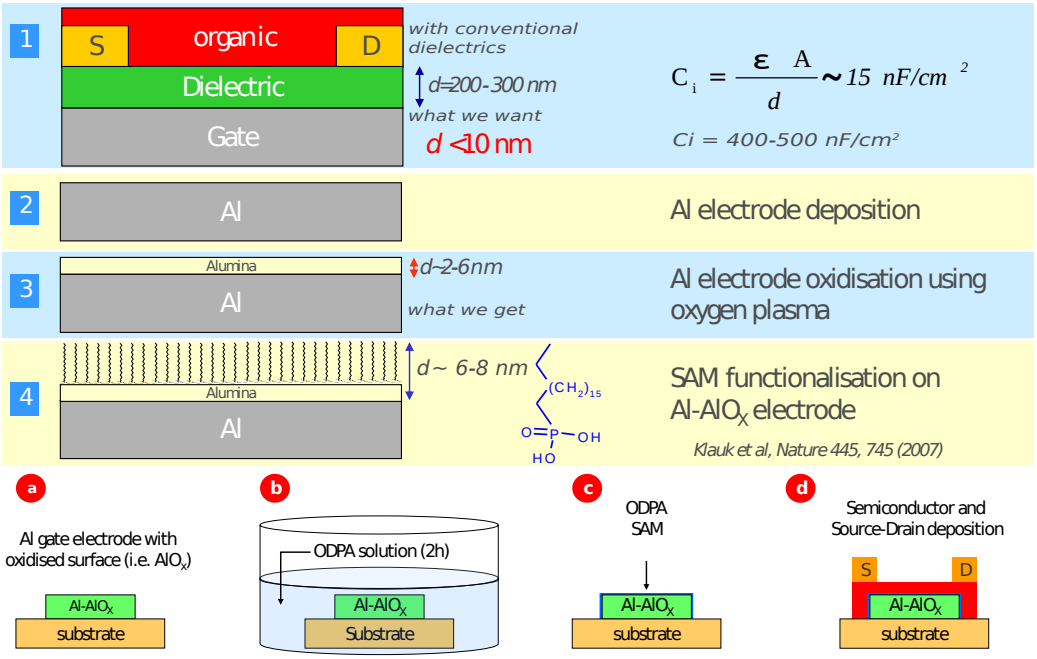

Figure 3.1: Steps of self-assembled monolayer functionalisation as gate dielectrics in bottom-gate transistors.

Diluted in isopropanol with a concentration of 5 mM, the SAM solutions is drop-casted on the freshly evaporated source-drain electrodes (30 nm). In order to facilitate the adsorption of the molecules, the substrate can be made more reactive by exposure to an oxygen plasma treatment (1 min, 80 W).

3.1.5 Chemical Vapor Deposition growth of graphene

In this section, the chemical vapor deposition (CVD) growth of graphene layer and its transfer to a substrate are described. This technique has been developed by Hok-Won Kim and Cecillia Mattevi in the Materials Department at Imperial College.

In our experiment, graphene layer is grown by low pressure (LP) chemical vapour deposition of carbon on polycrystalline 25 μm thick (99.8% purity) copper foils at a temperature of 1000°C using a mixture of methane and hydrogen [28, 35]. A PMMA polymer film is then deposited by spin-coating on one (the front) side of the graphene/Cu foil, the purpose being of avoiding any rolling or tearing of the graphene layer once floating in the solution. The graphene layer, also present on the rear side of the Cu foil, is removed with a cotton buds soaked with diluted nitric acid. At that stage, the Cu\graphene\PMMA layer is dropped in a iron chloride solution ($FeCl_3$, 3.5 g in 10 mL of HCl and 100 mL of DI water) and the copper is etched after 1 hour. The membrane graphene\PMMA is first rinsed with deionized water to

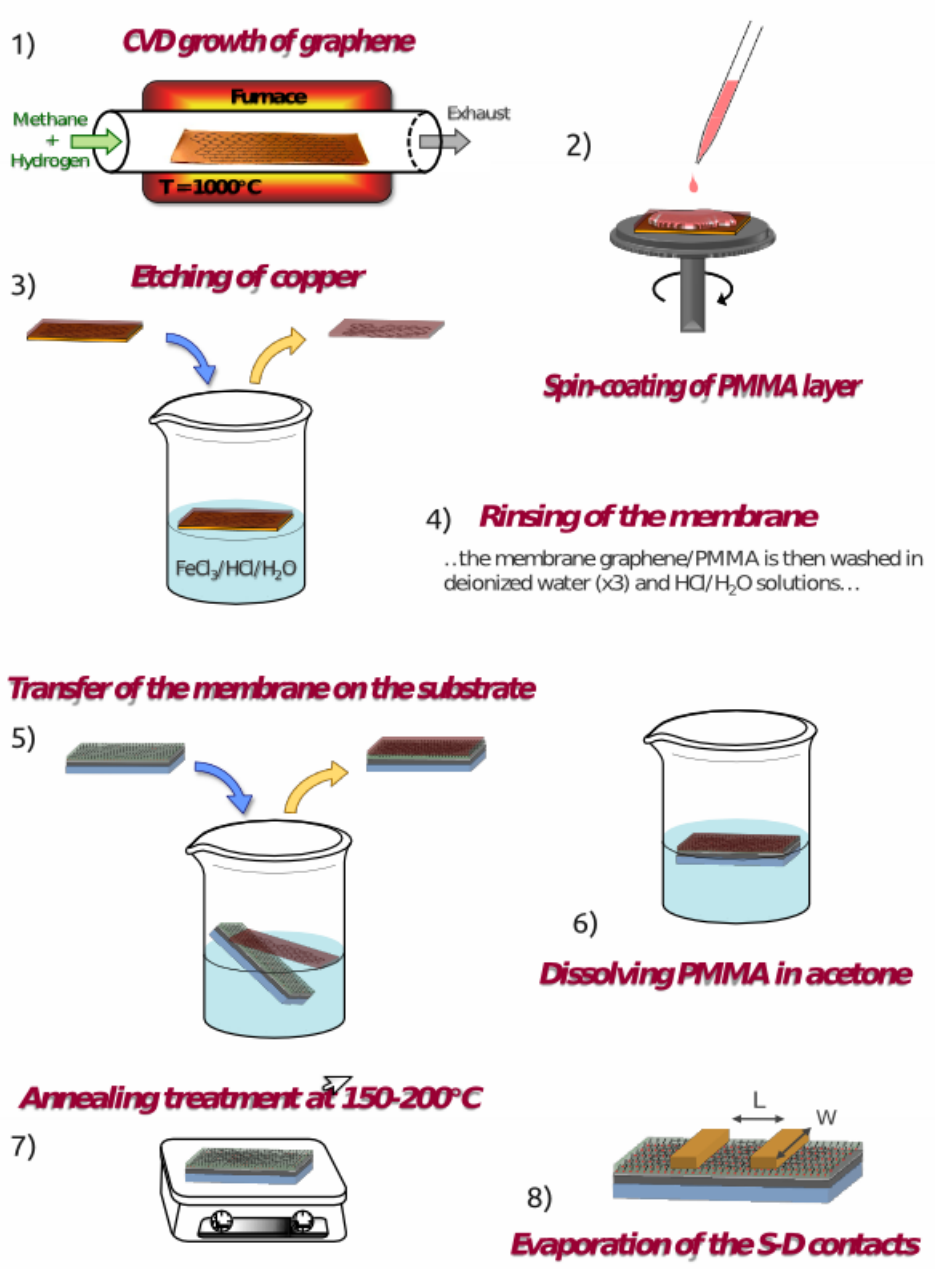

Figure 3.2: Steps of the CVD graphene growth and transfer to the substrate.

remove any iron or chloride ions and eventually in chloride acid solution (10%). The graphene/polymer membrane, which is floating at the air/water interface is scooped using the desired substrate. Once the floating membrane is transferred onto the substrate, the top PMMA film is dissolved in an acetone bath at 55°C for 15 min. The sample is then annealed at 150-200°C.

The graphene layer can be deposited onto different substrates (given appropriate surface energy). In our experiment, the goal was to develop graphene ambipolar tran-

sistors using a bottom-gate top-contacts architecture. For that purpose, the graphene layer was transferred onto self-assembled monolayer dielectrics for low-voltage applications, on fluoropolymer dielectrics for highly stable device applications and on SiO_2 dielectric as the reference samples. After transfer of the graphene layer, metal contacts are simply evaporated through shadow masks in high vacuum to define the transistor channel.

3.2 Material characterization techniques

3.2.1 Contact angle measurements

Contact angle measurement is a technique used to determine the wettability of a solution on a solid surface. In this work, this technique was used to study the surface energy characteristics of self-assembled monolayer or polymer dielectrics and then to evaluate how well the semiconductor solution is likely to wet on the SAM dielectric. This analysis method was reported by Wöbkenberg et al. [180] and is described in this section. Contact angle measurements were performed using a Krüss DSA100 drop shape analysis system. A pendant drop is deposited on a solid surface. Then the contact angle (θ), which corresponds to the angle between the solid-liquid interface and the liquid-gas interface, is measured.

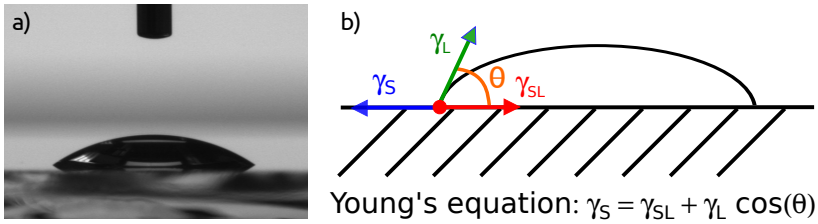

Figure 3.3: Contact angle measurement image of a water droplet on PHDA SAM layer (a) and schematic illustrating Young's equation of a drop of liquid on a solid interface (b).

First, the surface energy of the dielectric layer is studied. The equilibrium contact angle of three different liquids, whose polar and dispersive components are known, are measured on the solid surface. The three liquids used are: water, diiodo methane and ethylene glycol. Equation (3.1) is derived from the Owens-Wendt-Kaeble method [248]. The superscripts D and P stand for dispersive and polar parts, respectively. The subscripts S and L refer to solid and liquid, respectively.

$$\gamma_{SL} = \gamma_S + \gamma_P - 2(\gamma_L^P \gamma_S^P)^{1/2} - 2(\gamma_L^D \gamma_S^D)^{1/2} \tag{3.1}$$

As shown in figure (3.3), Young's equation applied to a drop of liquid in equilibrium on a solid interface is given by:

$$\gamma_S = \gamma_{SL} + \gamma_L \cos(\theta) \tag{3.2}$$

By using equations (3.1) and (3.2), the dispersive and polar components of the solid layer are related to the liquid's ones according to the following relation:

$$\frac{\gamma_L(\cos\theta+1)}{2(\gamma_L^D)^{1/2}} = (\gamma_S^P)^{1/2}\left(\frac{\gamma_L^P}{\gamma_L^D}\right)^{1/2} + (\gamma_S^D)^{1/2} \tag{3.3}$$

Once the contact angle θ is measured with each liquid solution, the dispersive and polar components can be extracted from a linear fit to equation (3.3). Secondly, the surface energy of the organic semiconductor is studied. For that, the contact angle of the semiconducting solution is measured on two different solid surfaces, for instance the studied dielectric layer and silicon oxide treated with HMDS. Using equations (3.4) and (3.5), the polar and dispersive components of the organic semiconductor can be deduced.

$$\frac{(\gamma_L^D)^{1/2}}{2\gamma_L} = \frac{(\cos\theta_1+1)(\gamma_{S2}^P)^{1/2} - (\cos\theta_2+1)(\gamma_{S1}^P)^{1/2}}{(\gamma_{S1}^D\gamma_{S2}^P)^{1/2} - (\gamma_{S2}^D\gamma_{S1}^P)^{1/2}} \tag{3.4}$$

$$\gamma_L = \gamma_L^P + \gamma_L^D \tag{3.5}$$

where the subscripts 1 and 2 refer to the two different solids.

The wettability of each solution on the dielectric is quantified by the spreading coefficient δW defined as the difference between the work of adhesion and the work of cohesion. The work of adhesion W_{SL} is the work required to separate a unit area of the solid-liquid interface whereas the work of cohesion is the work required to separate a unit area of the liquid-liquid interface. They are respectively given by:

$$\Delta W = \gamma_L(\cos\theta - 1) \tag{3.6}$$

$$W_{SL} = \gamma_L(\cos\theta + 1) \tag{3.7}$$

$$W_{LL} = 2\gamma_L \tag{3.8}$$

The spreading coefficient indicate the ability of the liquid drop to stick to the solid surface. A small contact angle indicates a good wetting of the semiconductor liquid on the SAM layer. If $\theta = 0°$, $\Delta W = 0$, this corresponds to complete wetting: the liquid adhere equally well to the solid surface as it would do to itself.

Another way to evaluate the wettability of the organic semiconductor on the SAM layer is to plot the wetting envelopes of the SAM layer and place the surface energy co-ordinates of different organic liquids on this plot. The wetting envelopes are lines of constant contact angle on a plot of the polar component γ_L^P versus the dispersive

part γ_L^D, the equation of which is given by:

$$\gamma_L^P = \left[\frac{2(\gamma_S^P)^{1/2} + \sqrt{4\gamma_S^P - 4[\cos\theta + 1][\gamma_L^D(\cos\theta + 1) - 2(\gamma_L^D\gamma_S^D)^{1/2}]}}{2(\cos\theta + 1)}\right]^2 \tag{3.9}$$

Then the liquid can be placed on the wetting envelope diagram of the SAM solid according to its dispersive and polar coordinates (γ_L^D, γ_L^P). Solutions whose surface energy components lie within the wetting envelope should show good wetting behavior. A semiconductor solution with a good wetting on the SAM is more likely to demonstrate good film formation by spin-coating and hence functional OFETs.

3.2.2 Optical microscopy

Optical microscopy is a technique used to assess the quality of the films at a mesoscopic scale (μm). In transistors, this could be used to check the device features or the grain size within organic semiconducting film. The microscope used in our labs was a Nikon LV100 integrated with a DS-Fi1 CCD camera. The microscope could be operated in transmission or reflection mode with objectives ranging from 5x to 50x.

3.2.3 Atomic Force Microscopy

Atomic Force Microscopy is an experimental technique used to study the morphology of surfaces [249]. This proximity technique is based on the physical measurement of short (r < 0.3 nm) and long range forces between the surface and the tip. Repulsive forces can be described by the Lennard-Jones potential and are due to electronic orbital ((non) entanglement) while attractive interactions results from first dipolar forces (VdW), then adhesion forces and capillarity forces.

The interaction between the cantilever and the surface is done by using the short distance interaction. The tip (20 μm, 10 nm„ 40º) is held at the extremity of the beam and scan the surface. The beam of the cantilever is (74 N/m, 129x37x4.0 $(\mu m)^3$) moved (bent) in a vertical direction using a piezoelectric ceramic while the scan is done on the surface along the two horizontal directions. The light of a laser diode is shined on a metallic film coated on the beam and after reflection is detected with a charge coupled device. The signal is transformed (two times), compared to the desired physical value and fed back. The signal could also be derivable and fed back with the Op-Amp without any transformation. This would just require a very accurate Op-Amp. The difference between the received signal and setting value would be finely amplified. A small adjustment in the controller and feeback loop so that the integration of the light of the photoddiode is taken into account in the loop. A small tip, due to its nature and profile, is particularly fragile and requires much attention when approached to the surface. Found in the middle, between the beam and the surface, it undergoes both strong elastic forces and interaction forces at the contact of the surface and has a weak spring constant. Two profiles are basically used in

AFM techniques: pyramidal tip and conic one. The tips are particularly precious for the quality of the images, and they are largely responsible for various artefacts. The larger is the radius of the tip compared to the roughness of the surface, the less subtle details of the surface topography are obtained. The resolution of the image is then reduced, and the image ends up completely fuzzy. The force of the cantilever depends on its mechanical characteristics, i.e. its bending and the sensitivity to the surface. To appreciate and adapt the force exerted on the cantilever, the string constant can be "derived" from the model of a beam embedded in the wall and, when the bending is at his peak, is presented as:

$$\varepsilon = \frac{Wh^3e}{4L^3} \tag{3.10}$$

where ε is the spring constant, W, L and h are the width, length and height of the beam and e its young modulus (N/m).

The AFM can work in two modes: contact and AC. In the first case, the cantilever is in contact with the surface and using the repulsive mode with the sample. This gives resolution up (or down) to the limitation of the piezoelectric ceramic (vertically) and the artefacts of the tip (laterally). This mode is characterized by large shear force. In the second case, attractive (and repulsive) forces are used and the tip is not in contact with the sample surface. The cantilever vibrates at his own frequency (~kHz) and at weak or stronger amplitudes depending on the displacement (<1 or >10 nm). With weak amplitude, the attractive forces modify the frequency when close to the surface. The signal is obtained by trying to assert the displacement and just keep the frequency constant. While with high amplitude, both attractive and repulsive forces play a role and the cantilever come in contact with the sample surface.

3.2.4 Raman spectroscopy

Raman technique is a method to detect the vibrational and rotational state of a material. Light is scattered on the sample, the first is then dispersed with different modes. After filtering and analysis, the composition of the signal is separated in its different frequencies and the intensity of each is presented.

3.3 Device and circuit characterization

3.3.1 Electrical measurements

Transfer and output characteristic measurements were performed using a semiconductor parameter analyzer (Keithley 4200 or Agilent 4156C). The analyzer can apply or measure simultaneously voltages and currents thanks to source-measurement units (SMUs). In the case of transistors, three probe tips are connected to the source, drain and gate electrodes. The parameter analyzer applied a drain and gate voltage while measuring the source, drain and gate currents. The gate current is recorded

to observe if there is any substantial leakage through the dielectric. The transfer curve corresponds to the (semilogarithmic) plots of the drain current (I_{DS}) versus the gate voltage (V_{GS}) measured at different drain voltages (V_{DS}). The output curve shows the plots of the drain current (I_{DS}) versus the drain voltage (V_{DS}) for different gate voltages (V_{GS}). These measurements were carried out under nitrogen atmosphere in the glove box, in a vacuum probe station (10^{-6} mBar) or in ambient air. Despite the fact that the Keithley 4200 analyser can provide a resolution as low as 0.1 fA with the preamplifier, the cables and probes are large sources of noise in the measurements, making currents below pA level difficult to measure accurately due to background noise. These measurements allow the extraction of device parameters such as the charge carrier mobility, the threshold voltage, the current on/off ratio and the subthreshold slope. Temperature dependence measurements were performed with a liquid nitrogen cooled cryostat in vacuum atmosphere.

Current-voltage measurements on metal-insulator-metal (MIM) structures allow evaluation of the leakage current density through the dielectric. Leakage current densities are measured by applying a bias voltage across the MIM structure. In the case of the study of hybrid SAM/AlOx dielectrics, the leakage current measurements on diodes indicate the presence and the quality of the self assembled monolayer, as a significant reduction of the leakage current is observed upon functionalization of alumina with a SAM. For the study of fluoropolymer dielectrics, the leakage current density measurements indicate the uniformity and good insulating property of the film, or the presence of pin-holes. When measuring the electrical characteristics of transistors, an additional step delay (~0.1 s) is set up on the analyser in order to take into account the time necessary to charge the semiconductor channel of the MIS diode. This is particularly true for gate dielectrics with high geometric capacitance (C ~ 1 μF/cm^2) such as SAM nanodielectrics.

3.3.2 Impedance spectroscopy measurements

Impedance measurements were performed using Solatron 1260A Impedance/Gain-Phase analyzer with a probe station under ambient or nitrogen atmosphere. An alternative voltage is applied to this capacitor, the DC voltage remaining zero. The impedance of the capacitor is then measured from 10 Hz to 1 kHz. The imaginary part of the impedance is assumed to be $Im(Z) = -1/(C\omega)$. Thus the capacitance of the dielectric can be extracted from the plot of the imaginary part versus the frequency and then divided by the overlap area ($A = 2.5 \times 10^{-3} cm^2$) between the two electrodes so as to obtain the geometric capacitance. Experimental determination of this geometric capacitance was used to calculate the field-effect charge carrier mobility from the electrical characteristics of the transistor.

3.3.3 Bias stress measurements

In the case of OFETs there isn't a unique stressing protocol. For this reason two experiments were designed and are described in this section.

A continuous bias stress $V_{G,ext}$ is applied on the gate electrode over a certain period of time and is interrupted at specific times (a log scale preferably) with a gate sweep to measure the transfer curve. The measurements should be completed within a short time, i.e. a time shorter than the smaller stress time, otherwise the device could undergo bias stress. The threshold voltage can be extracted as the intercept of the linear fit of the square drain current with the (Ox) axis. The threshold voltage shift can then be plotted as a function of time. The time-dependence of the threshold voltage shift is often described by a stretched exponential function: $\Delta V_T(t) = \big[V_T(t=\infty) - V_T(t=0)\big]\big[1 - e^{(-\frac{t}{\tau})^\beta}\big]$ where $V_T(t=0)$ is the threshold voltage in the initial state, $V_T(t=\infty)$ is the threshold voltage at equilibrium, τ is the time constant and β is the stretching parameter ($0 < \beta \leq 1$).

Electrical stability can also be observed by measuring the decay of the saturation drain current over time under a DC bias stress. Based on the equation of the saturation drain current and the stretched exponential function for the threshold voltage, the ratio of the saturation drain current I_{DS} between time t and the initial time can be derived as [250]: $\frac{I_{DS}(t)}{I_{DS}(0)} = exp\big[-2(\frac{t}{\tau})^\beta\big]$. Using the decay of I_{DS} instead of the threshold voltage shift to estimate stability avoid the error and inaccuracy due to the measurement and extraction of threshold voltage.

In order to further investigate the origin of the bias stress effect, stress measurements can be performed at different temperatures. If the threshold voltage shift can be fitted with a stretched exponential for each temperature and the graph of the relaxation time versus the reciprocal temperature is a straight line, then this would indicate that the relaxation is thermally activated [251].

3.3.4 Logic circuits measurements

To demonstrate the potential of our OFETs for application in basic electronic circuits, inverters were tested by combining two transistors and using four units of the semiconductor parameter analyser: input, output, supply voltage and ground. The configuration of the connections differs depending on the logic. The voltage at the output node is measured while sweeping the input node from ground to the supply voltage. Inverters must operate in the first or third quadrant of the DC transfer characteristic to show their relevance as a building block in circuits. These measurements were carried out in the vacuum probe station. The switching voltage, the gain and noise margins can be determined from these measurements.

Chapter 4

Organic transistors based on fluoropolymer dielectrics

The role of the gate dielectric in high performance organic field-effect transistors is as important as the semiconductor itself, since it affects both the morphology of the semiconductor and the charge carrier transport at the semiconductor-dielectric interface. Hence, the device performance and stability can be affected by imperfections, and/or contaminants or by the very chemistry of the dielectric surface.

Here we report on the use of an alternative amorphous fluoropolymer namely Hyflon® AD as the gate dielectric in organic transistors. Hyflon® AD is often used for the realization of membranes for gas separation. The copolymer Hyflon® AD 40 (referred often as Hyflon for simplicity in our study) was provided by Solvay and tested in transistors. The molecular structure of this fluoropolymer is shown on figure 4.1 (c). This copolymer is composed of 2,2,4-trifluoromethoxy-1,3-dioxole $(C_4F_6O_3)_m$ monomer and tetrafluoroethene $(C_2F_4)_n$ monomer. This polymer is highly transparent, it has a refractive index of 1.33 (similar to water), a glass-transition temperature of $95°C$, and a low relative permittivity of 2.0. The high solubility in perfluorinated solvent and its low solution viscosity allow solution-processing of this material. This distinctive features enabled the formation of uniform and thin films (down to submicron) by spin-casting. In our study, the surface and insulating properties of this polymer film are first investigated. Hyflon AD has the main advantage of being solution-processable, therefore it can be easily implemented as gate dielectric in low-cost organic field-effect transistors. The performance and reliability of the fluoropolymer Hyflon AD as a gate dielectric are utilized in different transistor architectures. High-performance transistors with hole mobility greater than 1 cm^2/Vs are demonstrated.

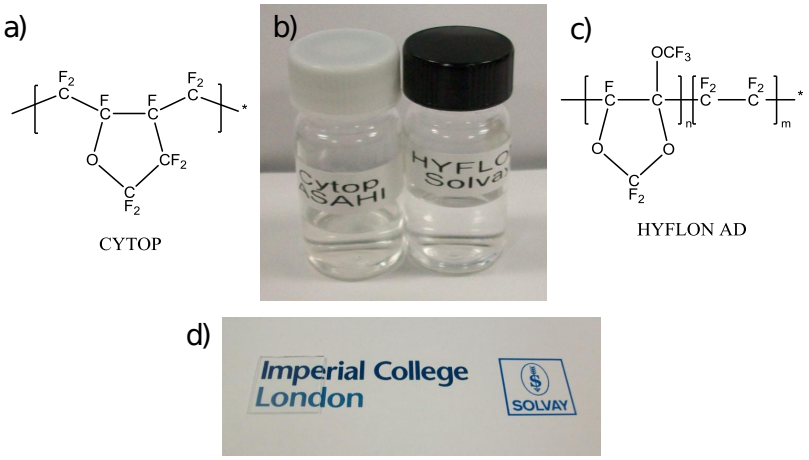

Figure 4.1: Molecular structure of poly(2,2,4-trifluoromethoxy-1,3-dioxole-co-tetrafluoroethene) (Hyflon® AD, MDO-TFE) (c) and poly(perfluorobutenylvinylether) (CYTOP) fluoropolymers (a). Transparent CYTOP and Hyflon AD solutions (b). Hyflon AD polymer film (thickness $\sim$ 500 nm) deposited on corning eagle glass substrate (d).

4.1 Thin film characterization of Hyflon AD polymer

4.1.1 Dielectric properties

Different weight concentration of HYFLON polymer and solvents were provided and tested: HYFLON 3.6 %, HYFLON 5 % and Hyflon 6.6 %. The performance of these gate dielectrics as insulators in organic transistors were systematically compared to those based on CYTOP dielectric (9 %). The latter, developed by Asahi Glass Corporation, is widely used and well characterized. Therefore samples based on CYTOP gate dielectric were used as reference samples in this study.

The insulating properties of the amorphous fluoropolymer thin films were tested with parallel plate metal-insulator-metal (MIM) structures. Polymer solutions were spin-cast onto patterned aluminium electrodes on glass substrates at 2000 rpm for 60 seconds and dried for 1 hour at $120°C$. Top electrodes were then deposited by vacuum sublimation through a shadow mask. The film thicknesses were measured with a Dektak step profiler. Figure 4.2 (a) displays the current density of these amorphous fluoropolymer when applying a bias across the MIM structure. Hyflon AD films (500 nm thick) exhibit excellent insulating properties with a low leakage current density of 10^{-8} A/cm^2 at 60 V (a value below 10^{-6} A/cm^{2}is required for gate dielectrics) and a dielectric breakdown strength exceeding 4 MV/cm. The current density of Hyflon AD at 1.2 MV/cm^2 is slightly higher than the value of 10^{-9}A/cm^2 found in our study and reported in literature for CYTOP film [163, 164, 167]. However this is lower than the current density obtained for polyimide (PI) [252], cross-linked poly 4-vinylphenol

(C-PVP) [58, 252, 166] and coss-linked polymethyl methacrylate (C-PMMA) [166] polymer dielectrics and also Aluminium oxide dielectric with a phosphonic acid-based self-assembled monolayer [47, 180, 177]. Table 4.1 reports the current density, the dielectric breakdown strength and dielectric constant of Hyflon and Cytop polymer but also the values of other polymer dielectric found in the literature. The geometrical capacitances were obtained by impedance measurements in air. Figure 4.2 (b) shows the geometric capacitance as a function of the frequency of Hyflon and Cytop polymer films sandwiched between two aluminium electrodes. The measured geometric capacitance were found to be 3.8 nF/cm^2 for 500 nm thick Hyflon AD (3.6%) film and 2.0 nF/cm^2 for 900 nm thick Hyflon AD (5%), compared to 2.9 nF/cm^2 for 750 nm thick Cytop film (9%). This results are in good agreement with the expected values when using the dielectric constant of 2.0 and 2.1 for Hyflon AD and Cytop, respectively. Walser *et al.* were able to deposit ultra-thin uniform and pin-hole free Cytop dielectric layer (down to 20 nm) by diluting the polymer in fluorinated solvent (1:10, CT-solvent 180) [164]. This reduction of the polymer dielectric thickness yields to significant increase of the geometric capacitance (100 nF/cm^2), and thus leads to a decrease of the operating voltage in transistors down to few volts (1-2 V). In our study, deposition of thin Hyflon layers was compromised by non-uniform films below 50 nm and formation of high concentration of pin-holes. Cheng *et al.* added the 1,6-bis(trichlorosilyl)hexane (Si-C_6) coss-linking agent to Cytop to prepare uniform thin dielectric film (50 nm) [167]. This cross-linked fluoropolymer exhibit low leakage current density (< 1 μA/cm^2) and high dielectric breakdown strength (> 2 MV/cm). This approach enable the fabrication of low-voltage bottom-gate transistors with a good device yield and a reduced bias stress.

4.1.2 Surface energy characteristics

Contact angle measurements were performed in order to determine the surface energy characteristics of Hyflon AD and Cytop polymer surfaces. Surface energy analysis will lead to a good understanding of the wettability of any semiconductor on these surfaces, an indication which is of tremendous importance in a bottom gate/ top contact configuration.

The dispersive (γ_D) and polar (γ_P) solid surface energy components of the dielectrics were determined by measuring the contact angles of three different liquids, whose polar and dispersive components were known, on the solid surface. The liquids used to do these measurements were water, ethylene glycol and diiodo methane. The solid surface energy components can then be extracted using the Owens-Wendt-Kaelble method [248]. These measurements are summarized in table 4.1.

Figure 4.3 shows the droplets of water (a) on top of Hyflon and CYTOP surfaces and their wetting envelopes for $\theta = 0°$ (b). Hyflon AD polymer is highly water repellent. It has a high contact angle with water of 117°, similar to the highly hydrophobic Cytop (~114°). Veres *et al.* observed an increase of the mobility with

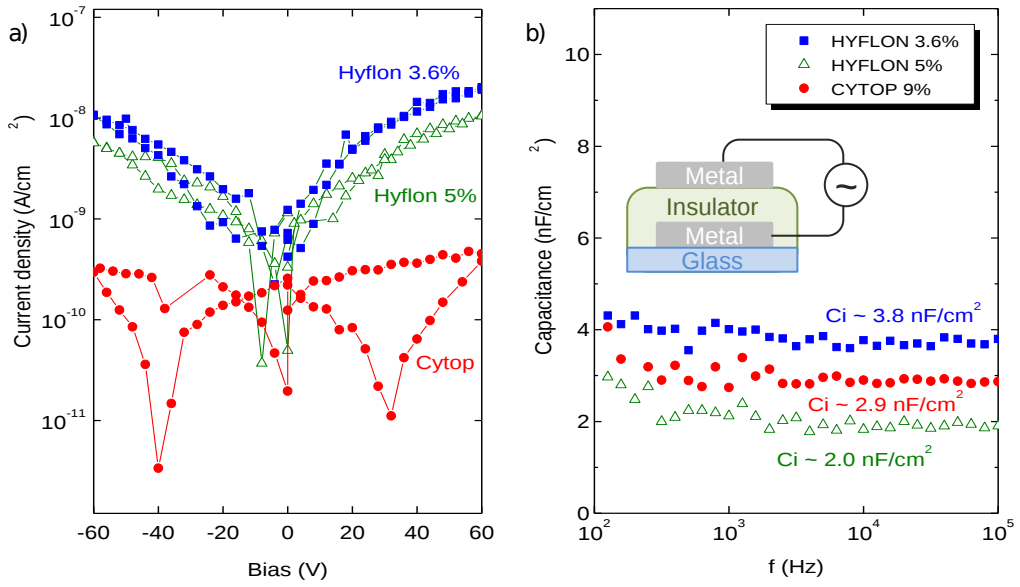

Figure 4.2: Leakage current density of Hyflon AD and Cytop films measured in a metal-insulator-metal structure (a). Capacitance versus frequency of theses polymer dielectrics over a range going from 1kHz to 100 kHz (b).

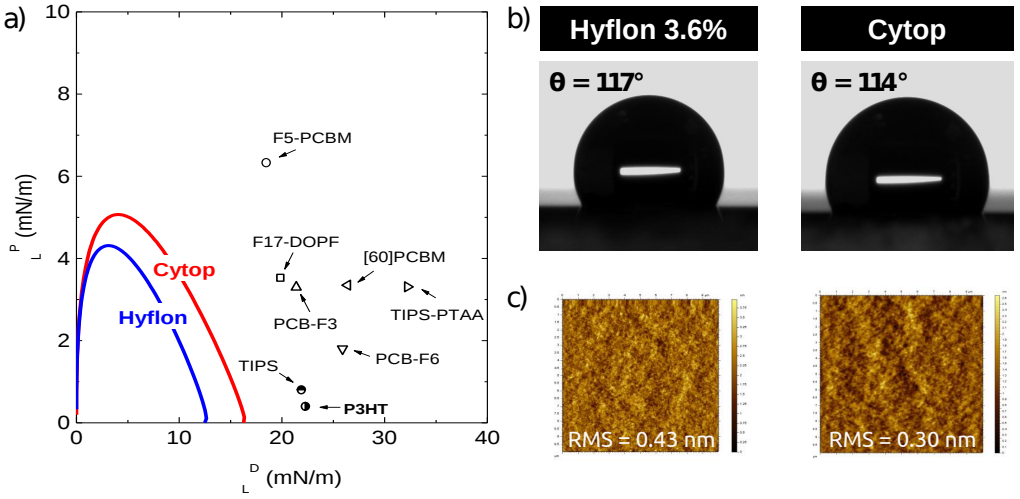

Figure 4.3: Wetting envelope of Hyflon AD and Cytop surfaces (a). The surface energy components of few semiconductor solutions are also plotted. Water droplet on the two fluoropolymer surfaces (b). Atomic force microscopy images ($2\,\mu m \times 2\,\mu m$) of Hyflon and CYTOP thin-films on glass substrates (c).

increasing contact angle on the gate insulator [45]. The presence of hydroxyl groups and absorbed water at the interface between the insulator and the semiconductor increases the density of traps and leads to threshold voltage instabilities in transistors. Compared to other polymer films like PVP, these hydroxyl-free and hydrophobic flu-

oropolymers forms good interface with the semiconductor and yield to high quality OFETs with good resistance against gate bias stress. However these fluoropolymers have a low wettability since small contact angles are associated with increased wettabilty. As shown on figure 4.3, these dielectrics exhibit small wetting envelopes with low polar component. Details of the surface energy components are summarized in table 4.1. The coordinates of different organic semiconductor solutions are also represented to assess the possibility of spin-coating solutions on the dielectric surfaces. Any liquid whose surface energy components lie within the wetting envelope will demonstrate good wettability on this surface. Given the low surface energy of Hyflon AD, solution-processing of any semiconductor on top of the insulator is very difficult. The morphology of the amorphous fluoropolymers was measured by atomic force microscopy in tapping mode. The roughness of Hyflon AD film was found to be ~ 0.43 nm, compared to ~ 0.30 nm for Cytop. Because of their low surface roughness Hyflon AD can be used in bottom-gate transistors. In that case, organic semiconductors are thermally evaporated on top of the polymer layer due to its low surface energy.

Table 4.1: Summary of the surface and electrical properties of Hyflon AD and Cytop polymer thin-film dielectrics. Geometrical capacitances (C_i), leakage current densities (J) and dielectric breakdown strengths (E_B) are measured in parallel plate M-I-M structures. Thicknesses (t) were measured with a dektak step profiler. θ_{water} is the contact angle of the water droplet on the polymer surface. γ_D and γ_P corresponds to the dispersive and polar surface energies extracted from contact angle measurements on polymer films. Litterature values for other polymer films are included for comparison.

Polymer	θ_{H_2O}	γ_D	γ_P	$J\,(at\,E_{MIM})$	E_B	C_i	t	ε_r	Ref.
	°	mN/m		A/cm^2(MV/cm)	MV/cm	nF/cm^2	nm		
Hyflon AD	117	16.3	0.2	$10^{-8}-10^{-7}$(1.2)	4	3.8	500		this work
Cytop	114	12.5	0.4	10^{-10}–10^{-9}(0.8)	4	2.9	750		this work
Cytop				10^{-8} (5)	5		15-200	2.1	[163]
Cytop				$5\cdot10^{-7}$ (4)	6	98	19	2.1	[164]
Cytop	112			$3\cdot10^{-6}$ (9.8)		4.4-2.7	430-700		[162]
C-Cytop		(19)		$5\cdot10^{-6}$	2	45-28	50-150		[167]
C-Cytop				10^{-9}	5	10	250		[167]
Cytop				10^{-9}	5	5	450		[167]
C-PMMA				10^{-5} (3)	3	103	30	3.5	[166]
C-PVP				10^{-5}(3)	3	180	30	6.4	[166]
PI				10^{-6}(2)	2.5	260	9	2.6	[252]
PI				10^{-6}(2)	2.1		13-240	3.4	[252]
C-PVP				10^{-7}(2)	3	254	12	3.3	[252]
C-PVP				10^{-7}(2)	2.5		22-293	3.8	[252]
C-PVP	50			$2.5\cdot10^{-7}$(0.7)	2.4	11.3	260-280	3.6	[58]
PVP-OEMA	50			$2.5\cdot10^{-7}$(0.6)	1.8	11.4	310-380	4.0	[58]

4.2 High-performance hole and electron transporting organic transistors

4.2.1 Top-gate solution-processed organic transistors

Having shown the good insulating properties of Hyflon AD polymer dielectric, solution-processed p-channel diFTESADT:PTAA and n-channel $PC_{61}BM$ transistors were fabricated in top-gate bottom-contact architecture. In this configuration, the presence of the fluoropolymer gate dielectric on top of the semiconductor provides a protection against environmental exposure. The top-gate architecture takes also advantage of the vertical phase separation that occurs in diFTESADT:PTAA blend [69]. The highest performance were observed at the top interface of the semiconductor film. However fabrication of top-gate transistors based on polymer gate dielectric presents few difficulties: the solvent should not dissolve the underlying semiconductor layer, high curing temperature of the polymer can damage the layer underneath, the roughness of the underlying layer may lead to higher leakage current through the dielectric. In our study, Hyflon AD was dissolved in fluorinated polyether solvents (Galden DO2 TS (3.6 %, 5 %) and Galden LS165 (6.6 %)), orthogonal to most organic semiconductor, including small molecule semiconductors.

Standard top-gate bottom-contact transistors were fabricated on glass substrates (Corning Eagle 2000). 50 nm thick metalic source-drain (S-D) electrodes were thermally evaporated through shadow masks. Aluminium electrodes were chosen for n-type PCBM semiconductor (EA = 3.7 eV) and gold for p-type diFTESADT:PTAA blend (IP = 5.11 eV). The work function of gold electrodes was altered by self-assembled monolayer treatment with pentafluorobenzene thiol (PFBT) to reduce the injection barrier between the metal electrodes and the semiconductor [69]. A solution of diFTESADT:PTAA (1:1 wt%) in tetralin was spin-coated at 500 rpm for 10 s and 2000 rpm for 20 s. The spun film was dried at 100°C for 15 min in nitrogen atmosphere. The Hyflon AD and Cytop were spin-coated at 2000 rpm for 60 s and was followed by drying at 120°C for 30 min to remove the solvent. Top-gate transistors were complete by evaporating 50 nm thick aluminium gate electrode.

Figure 4.5 shows the typical transfer and output characteristics of diFTESADT:PTAA blend transistors with Cytop (a-b) and Hyflon AD (a-c) gate dielectrics. Unless otherwise stated all transistor measurements were carried out under nitrogen atmosphere in a glove box. These transistors operate at large voltages (~60 V) because the thicknesses of the dielectric polymer films are typically 500-750 nm. The device performances are summarized in table 4.2. The transistor based on HYFLON AD (3.6 %) exhibit a good hole mobility up to 1.2-1.7 cm^2/Vs, a low threshold voltage (V_T = -2.5 V), a current on-off ratio of $2 \cdot 10^4$ and a low subthreshold slope of 3.5 V/dec. The hole mobility measured is higher than the saturation mobility of 1 cm^2/Vs (0.9 cm^2/Vs in linear regime) obtained with CYTOP based devices. The threshold voltage (V_T ~ -11.5 V) and subthreshold swing (SS = 10V/dec) for Cytop based device

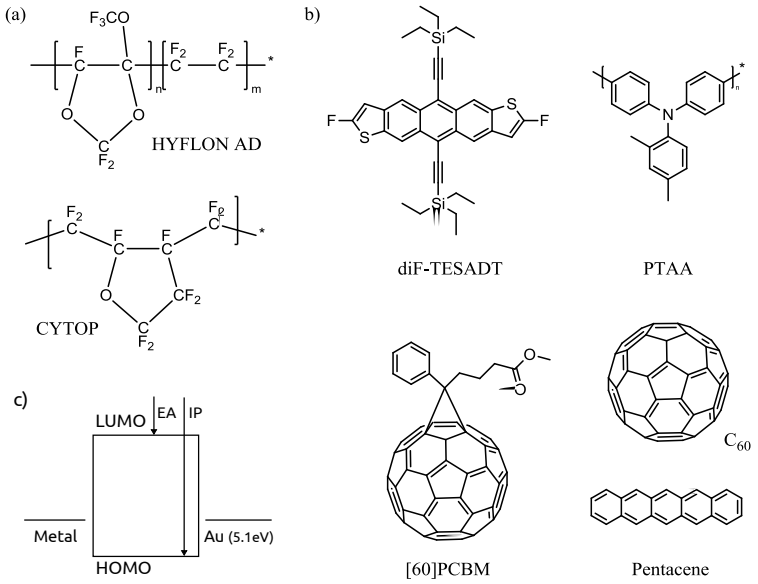

Figure 4.4: Molecular structures of Hyflon AD and Cytop fluoropolymer dielectrics (a). Chemical structures of 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diFTESADT, purity 99%, electron affinity EA = 2.79 eV, ionization potential IP = 5.04 eV, M_W = 566.97 g/mol), pentacene (99%, EA = 3.2 eV, IP = 5.0 eV, M_W = 278.35 g/mol), $PC_{61}BM$ (99.9%, EA = 3.7 eV, IP = 6.1 eV, M_W = 910.88 g/mol) and C_{60}(99.9%, EA = 3.6 eV, IP = 6.8 eV, M_W = 720.64 g/mol) small molecules and poly(triarylamine) (PTAA, IP = 5.1 eV, M_n = 7000-10000, M_W/M_n = 2.0-2.2) polymer (b). Energy band diagram for metal-semiconductor interfaces (c).

were relatively higher compared to transistors with Hyflon AD gate dielectric. This suggests that Hyflon AD provides an excellent (even better than Cytop dielectric) interface with low density of traps when in contact with the semiconductor. A lower mobility (0.6 cm^2/Vs) but better ohmic contact were observed with a 900 nm thick layer of Hyflon AD (5 %), suggesting a change in morphology at the semiconductor-dielectric interface. The mobility extracted with both fluoropolymer dielectrics are comparable to the value found in amorphous silicon and higher than the mobility that is extracted in most solution-processed transistors based on polymer dielectrics [253, 45, 166, 167]. For p-channel solution-processed semiconductors, 0.2 cm^2/Vs was reported in top-gate pBTTT transistors based on cross-linked PMMA [166] and 0.005 cm^2/Vs in top-gate F8T2 transistors based on C-PMMA [166], C-PVP [166] or C-Cytop [167] gate dielectrics.

N-channel solution-processed transistors were also demonstrated employing the amorphous methanofullerene [60]PCBM as the semiconductor. Figure 4.5 illustrates the typical transfer (d) and output (e-f) characteristics of solution-processed $PC_{61}BM$ transistors with a 500 nm thick Hyflon AD dielectric (e) and one device with a 750 nm thick Cytop dielectric (b) for comparison. Both devices have a channel width and length of 1000 μm and 40 μm, respectively. Transistors based on HYFLON AD (3.6

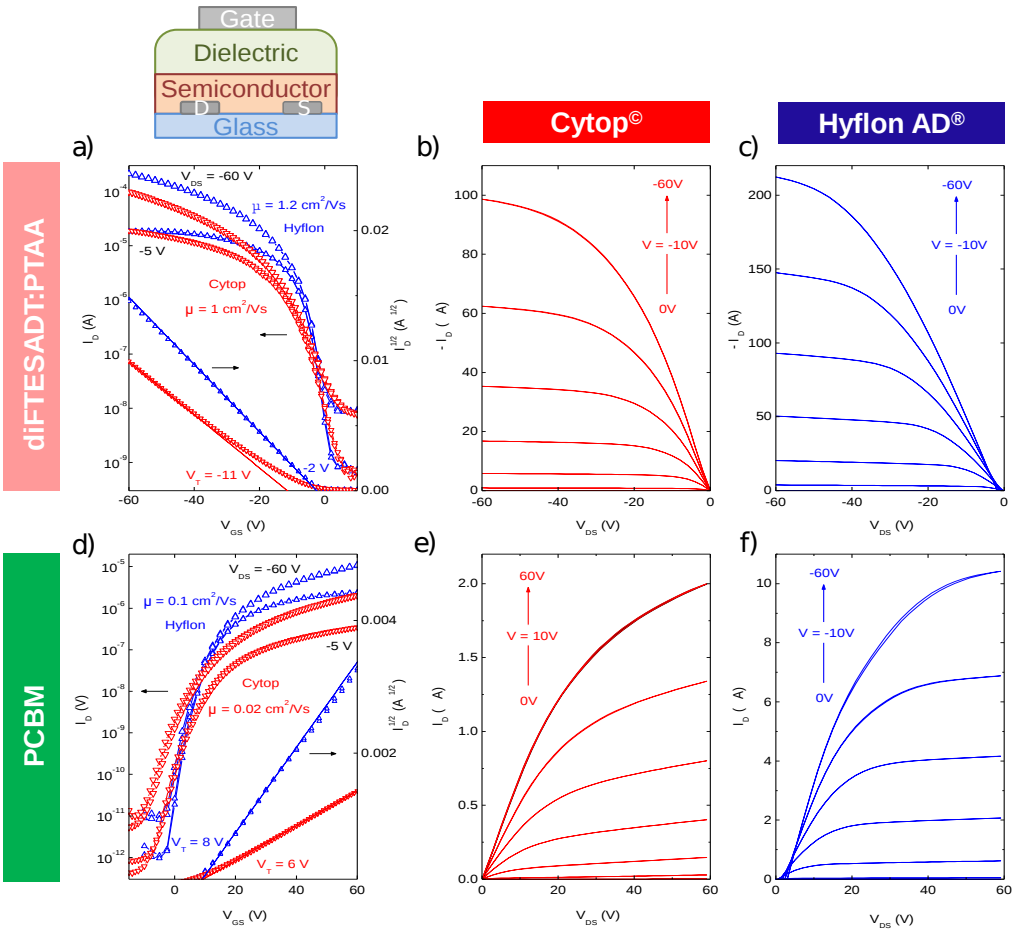

Figure 4.5: Transfer (a) and output (b,c) characteristics of solution-processed p-channel diFTESADT:PTAA (1:1) blend transistors based on Cytop (b) and Hyflon AD (c) polymer gate dielectrics. TFTs have a channel width of 1000 μm and a channel length of 30 μm. Transfer (d) and output (e,f) characteristics of solution-processed n-channel $PC_{61}BM$ transistors using Cytop (e) and Hyflon AD (f) polymers as gate dielectrics. Both TFTs have a channel width and length of 1000 μm and 40 μm, respectively. All these devices were fabricated in a top-gate bottom-contact architecture.

%) exhibit excellent transfer and output characteristics with electron mobility up to 0.1 cm^2/Vs, a current on/off ratio of 10^6, a low threshold voltage (V_T~ 8.1 V) and a low subthreshold slope of 2.7 V/dec. The electron mobility extracted is five times higher than the mobility (0.02 cm^2/Vs) obtained with CYTOP based device. The latter had a threshold voltage of 5.6 V and a subthreshold slope of 3.9 V/dec. These differences can be attributed to the dielectric since both devices have the same semiconductor and only the dielectric differs between the two devices. However devices based on HYFLON AD (3.6 %) gate dielectric show higher leakage current ($<10^{-6}$A at 60 V) than devices based on Cytop dielectric ($<10^{-8}$ A). This observation could be explained by a thinner or/and poorer film formation. Performances of Hyflon

AD-based transistors obtained with different concentrations or solvents are summarized in table 4.2. The output curve of devices based on Hyflon AD films (3.6 % or 5 %) presented non-perfect ohmic contact, in contrast with nice ohmic contact observed with devices based on CYTOP dielectric. Based on the cross-linked Cytop fluoropolymer gate dielectric, Chen et al. reported a mobility of 0.01 cm^2/Vs with solution-processed N1400 transistors.

4.2.2 Transistors fabricated by vacuum-sublimation

Having demonstrated that Hyflon AD can be successfully employed as a gate dielectric in top-gate transistors based on solution-processed semiconductors, we will show now that Hyflon AD can also be implemented as a dielectric in a bottom-gate architecture, in which the semiconductor lies on top of the dielectric. The study of the surface energy of the different dielectrics has shown that solution-processing of any semiconductor, especially small molecules, on fluoropolymers is really difficult (see section 4.1). That is why thermal evaporation was considered as a more appropriate technic to fabricate BG-TC transistors using Hyflon AD as the dielectric. Previous reports on bottom-gate transistors based on polymer gate dielectrics also reported vacuum-sublimation as the deposition technique for the semiconductor [164, 252, 58, 162, 163].

In our study, vacuum-sublimed p-channel pentacene and n-channel C_{60} bottom-gate transistors were fabricated as follows: a 50 nm thick aluminium (Al) gate electrode was deposited on a clean glass substrate. The insulating polymer, Hyflon AD or Cytop, was spin-coated at 2000 rpm for 60 s. The samples were subject to a thermal annealing process at 100°C for 30 min. Pentacene and C_{60} semiconductors were evaporated on top of the fluoropolymers in high vacuum (10^{-8} mbar) to obtain ~20 nm thick films. Devices were finally completed by evaporating gold (pentacene) or aluminium (C_{60}) source-drain contacts. In order to compare the performance of transistors based on different architectures with the same dielectric and semiconductor materials, vacuum-sublimed C_{60} transistors were also fabricated using top-gate bottom-contact structure on glass substrates employing Al S/D electrodes (the fabrication procedure corresponds to the one explained in the previous section, only the deposition technic of the semiconductor differs).

Figure 4.6 displays the transfer (a) and output (d) characteristics of a pentacene transistor based on a 900 nm thick Hyflon AD (5%) dielectric in a bottom gate–top contacts configuration. This device has a hole mobility of 0.05 cm^2/Vs. The threshold voltage is however rather high -39 V and the current on/off ratio is $5 \cdot 10^2$. The mobility value for pentacene transistors is much lower than the values (0.4-1.4 cm^2/Vs) that were reported for transistors based on Cytop gate dielectric [163, 162]. Bottom-gate top-contact C_{60} transistors were also successfully demonstrated with Hyflon AD and Cytop gate dielectrics. The electrical characteristics of the bottom-gate (b,e,g) and top-gate (c,f,h) C_{60} transistors are presented on figure 4.6. The electron mobility was found to be 0.16 cm^2/Vs with both Hyflon AD and Cytop dielectrics in bottom-gate

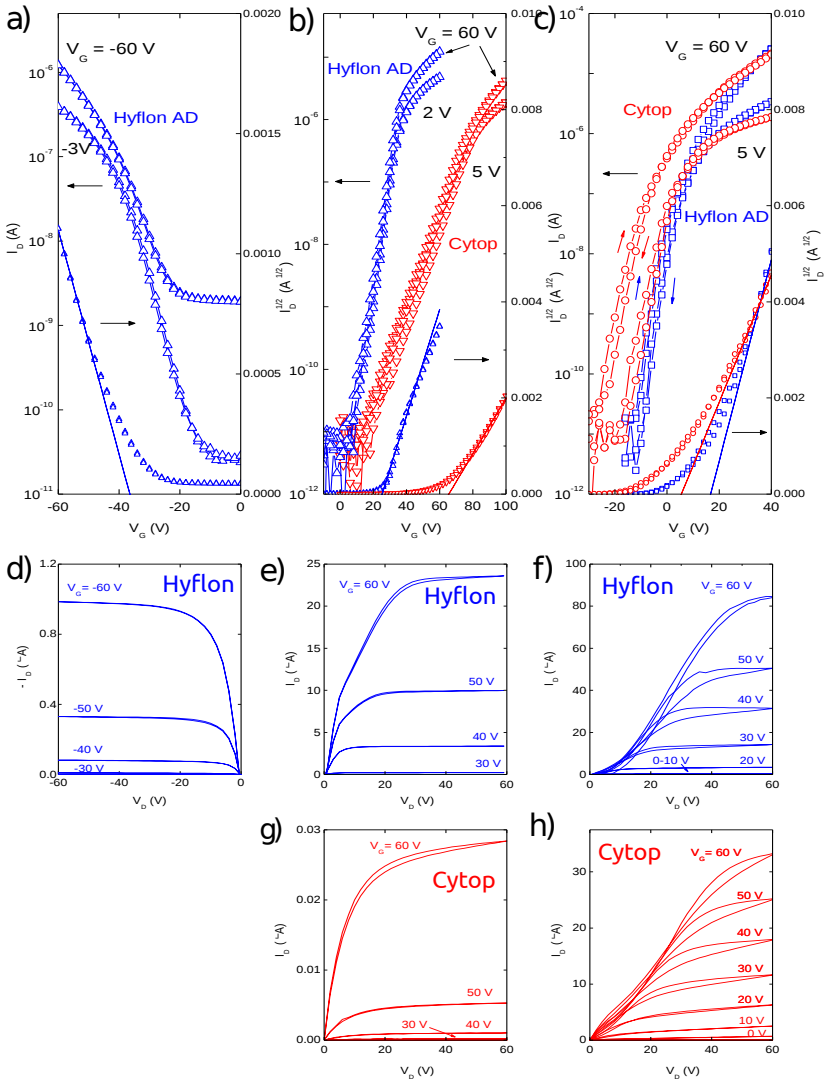

Figure 4.6: Transfer (a) and output (b) characteristics of top-gate pentacene transistors based on Hyflon AD (t ∼ 900 nm) gate dielectric. Transfer (b) and output (e-g) characteristics of top-gate C_{60}transistors with 500 nm thick Hyflon AD (e) and 750 nm thick Cytop (g) dielectrics. Electrical characteristics (c-f,c-h) of bottom-gate top-contact C_{60} transistors with the two fluoropolymers are given for comparison.

devices. Mobility values as high as 0.8 cm^2/Vs with Hyflon AD and 0.5 cm^2/Vs with Cytop in top-gate devices. Threshold voltages of 28 V for Hyflon AD and 70 V for Cytop were observed in bottom-gate TFTs, in contrast with the low values (17 V for Hyflon and 5 V for Cytop) found in top-gate devices, suggesting that charge trapping at the top semiconductor-dielectric interface is more important than at the bottom interface. Hysteresis of 2.5-3 V for Cytop and 0.8 V for Hyflon dielectrics in top-gated devices were observed between the forward and backward sweep, suggesting also charge trapping at the interface. Important non-ohmic contact was observed in devices fabricated in a top-gate bottom-contact structure. More details on the

Table 4.2: Summary of electrical performances of organic transistors based on Hyflon AD and Cytop gate dielectrics. Semiconductors employed in this study are the solution-processed diFTESADT:PTAA blend (p-type) and PCBM (n-type) small molecules, the vacuum sublimed pentacene (p-type) and C_{60} (n-type) small molecules. Parameters were obtained assuming a geometric capacitance of 3.5 nF/cm^2 for Hyflon (3.6 %, 500 nm), 2.0 nF/cm^2 for Hyflon (5 %, 900 nm), 4.0 nF/cm^2 for Hyflon (6.6 %, 450 nm) and 2.5 nF/cm^2 for Cytop (9 %, 750 nm). As a deposition technique, the semiconductor mentioned with the symbol $\star$ were solution-processed and those with the symbol ‡ were vacuum-sublimed. Literature values for transistors based on polymer gate dielectrics are also reported here for comparison. † The cross-linking reagent 1,6-bis(trichlorosilyl)hexane (C_6-Si) is used in this study.

Dielectric	Semiconductor	Struct.	C_i	W/L	μ_{sat}	$V_T(V_{ON})$	$I_{ON/OFF}$	SS	Reference
			nF/cm^2	μm/μm	cm^2/Vs	V (V)		V/dec	
Cytop	TESADT:PTAA*	TG|BC	2.1	1000/60	2.5	-5	10^4		[66, 69]
Cytop	TIPS5P:PTAA*	TG|BC	2.1	1000/60	1.1	-5	10^5		[66]
Cytop	TIPS5P:PαMS*	TG|BC	2.1	1000/60	0.7	-2	10^5		[66]
Hyflon 3.6%	TESADT:PTAA*	TG|BC	3.5	1000/30	1.2	-2.5	2.10^4	3.5	this work
Cytop	TESADT:PTAA*	TG|BC	2.5	1000/30	1.0	-11.5	10^4	10	this work
Cytop	TESADT:PFTAA*	TG|BC	1.2	1500/50	2.7	-16.9	10^5	11	this work
Hyflon 3.6%	PCBM*	TG|BC	3.5	1000/40	0.1	8.1 (2.5)	10^6	2.7	this work
Cytop	PCBM*	TG|BC	2.5	1000/40	0.027	5.6 (4.5)	2.10^5	3.9	this work
Hyflon 5%	TESADT:PTAA*	TG|BC	2	2000/50	0.84	1.5		18	this work
Hyflon 5%	PCBM*	TG|BC	2	1000/40	0.071	17.4		4.4	this work
Hyflon 6.6%	PCBM*	TG|BC	4	1000/20	0.078	7.7		4.7	this work
Cytop	P3HT*	TG|BC	2		0.02				[45]
PMMA	P3HT*	TG|BC	2		0.007				[45]
Cytop	F8T2*	TG|BC			0.0015				[253]
PMMA	F8T2*	TG|BC			3.10^{-4}				[253]
C-Cytop	F8T2*	TG|BC	45	1000/20	0.005	-1.1	10^4-10^5		[167]
C-Cytop	N1400*	TG|BC	45	1000/20	0.01	0.5	10^5-10^6		[167]
C-PMMA†	pBTTT*	TG|BC	103	1000/5	0.2	-4	10^2-10^4		[166]
C-PMMA†	F8T2*	TG|BC	103	1000/20	0.005	-1.5	10^3		[166]
C-PMMA†	P3HT*	TG|BC	103	1000/10	0.01	-2	10^2-10^3		[166]
C-PVP†	F8T2*	TG|BC	108	1000/20	0.005	-2	10^3		[166]
Hyflon 5%	pentacene‡	BG|TC	2	1500/20	0.05	-39	5.10^2	12.9	this work
Hyflon 3.6%	$C_{60}{}^\ddagger$	BG|TC	3.5	1000/30	0.80	17.3	10^6	3.7	this work
Cytop	$C_{60}{}^\ddagger$	BG|TC	1.2	1500/30	0.55	5.1	7.10^5	4.5	this work
Hyflon 3.6%	$C_{60}{}^\ddagger$	TG|BC	3.5	1500/20	0.16	27.8	10^6	4.2	this work
Cytop	$C_{60}{}^\ddagger$	TG|BC	1.2	1000/20	0.16	70.4	3.10^5	4.1	this work
Cytop	pentacene‡	BG|TC	46.5	1000/50	0.45	-6.3	3.10^7	0.56	[163]
Cytop	PTCDI-$C_{13}{}^\ddagger$	BG|TC	103	450/250	0.16	0.2	10^4	0.15	[164]
Cytop	pentacene‡	BG|TC	4.4-		1.4	(1)	10^7	0.3	[162]
Cytop	rubrene‡	BG|TC	2.7		5.7	(3)	10^8	0.5	[162]
PI	pentacene‡	BG|TC	260	700/70	0.38	-0.8	10^4		[252]
C-PVP	pentacene‡	BG|TC	254	700/70	0.50	-1.4	10^5	0.17	[252]
C-PVP	pentacene‡	BG|TC	12.2	170/130	3.0	-5	10^5	1.2	[58]
PVP-OEMA	pentacene‡	BG|TC	9.3	170/130	2.9	-8	10^5	1.3	[58]

device performances are summarized in table 4.2. Similarly to what was observed in pentacene device based on Hyflon AD, C_{60} devices based on Hyflon AD dielectric suffered from relatively high leakage current (~10^{-7}A at 1 MV/cm), compared to ~

10^{-9} A measured in Cytop-based devices.

4.2.3 Dual layer Hyflon/SiO_2 gate dielectrics

Finally, bottom-gate top-contact C_{60} transistors were demonstrated employing a dual layer dielectric composed of a thin layer of Hyflon on top of the silicon oxide. These devices exhibit similar performance to that obtained from Hyflon based transistors with maximum electron mobility 0.2-0.3 cm^2/Vs.

C_{60} transistors were fabricated in a bottom-gate top-contact configuration using Al electrodes and hybrid Hyflon/SiO_2 gate dielectric. A thin layer (200 nm) of Hyflon AD is deposited by spin-coating (6000 rpm for 60 s) on the atomically flat silicon oxide (SiO_2), the Si/SiO_2 substrate being used as bottom gate. The C_{60} semiconductor is evaporated on top of the fluoropolymer at a rate of 1 Å/s. Transistors were completed by thermal evaporation of Al source-drain contacts through shadow masks.

These devices exhibited good field behavior with a maximum electron mobility of 0.34 cm^2/Vs, a threshold voltage of 30 V, a high current on/off ratio of 10^6 and a subthreshold slope of 5.6 V/dec. The device performances are summarized in table 4.3. The extracted mobility is comparable to the values obtained with a single layer Hyflon AD as dielectric. The mobility is also higher than PTCDI-C_8 TFTs based SiO_2 dielectric treated with PVP or PMMA polymers [145]. Due to the addition of the silicon oxide layer, these transistors exhibit low leakage current (10^{-10}-10^{-9}A at 1 MV/cm). This corresponds to a reduction of three orders of magnitude compared to devices based on a single layer of Hyflon. In their study, Walser *et al.* demonstrated both p-type pentacene and n-type PTCDI-C_{13} transistors using SiO_2 dielectric passivated with a thin fluoropolymer layer on top [144]. An ultrathin layer of CYTOP (7-9 nm) was deposited by spin-coating at 1000 rpm for 40 s a diluted solution of CYTOP (1:30). Mobility of ~0.2 cm^2/Vs was reported for both p-type and n-type conducting transistors. The very low threshold voltage (7 V) and subthreshold swing (0.6 V/dec) shows the low trap density for n-type material at the dielectric interface. Both studies illustrate that fluoropolymers, like Hyflon AD or Cytop, provide with a good interface for n-type transport in transistors because these hydroxyl-free polymers passivate the siloxyl group on the SiO_2 surfacee. This leads to an improvement of the electrical stability in n-type OFETs, as it will be discussed in the next section.

4.3 Electrical stability of organic transistors

Bias stress effects of diF-TESADT:PTAA blend and $PC_{61}BM$ transistors based on Hyflon AD and Cytop gate dielectrics were studied over time at various temperatures ranging from 200 K to 400 K. Electrical stability measurements in transistors were performed by continuously applying a gate bias (V_{ext}) for 12-24 hours and measuring periodically (on a logarithmic scale) the transfer curve. The gate electrode potential

Table 4.3: Summary of electrical performances obtained for bottom-gate top-contact OFETs based on SiO_2 dielectric modified with a thin polymer dielectric layer. Hyflon AD and CYTOP polymer dielectrics were investigated in our study employing the vacuum-sublimed C_{60} as the semiconductor.

Dielectric	Semiconductor	Struct.	C_i (nF/cm^2)	μ (cm^2/Vs)	V_T (V_{ON}) (V)	$I_{ON/OFF}$	SS (V/dec)	Ref.
Hyflon/SiO_2	C_{60}	BG|TC	4.3	0.34	29.9(20.7)	10^6	5.6	this work
Cytop/SiO_2	pentacene	BG|TC	11.2	0.28	-20(-7.7)	10^5	2.6	[144]
Cytop/SiO_2	PTCDI-C_{13}	BG|TC	11.2	0.18	7(2.4)	10^5	0.6	[144]
SiO_2	PTCDI-C_8			0.13	...	$1.7{\cdot}10^5$		[145]
PαMS /SiO_2	PTCDI-C_8			0.33	15.0	$2.4{\cdot}10^5$		[145]
PVP/SiO_2	PTCDI-C_8			0.17	46.3	$4.0{\cdot}10^5$		[145]
PMMA/SiO_2	PTCDI-C_8			0.14	10.7	$4.8{\cdot}10^5$		[145]
PVA/SiO_2	PTCDI-C_8			0.056	20.2	$4.3{\cdot}10^4$		[145]

was released for the recovering. The change in threshold voltage and mobility over time can be observed from these measurements.

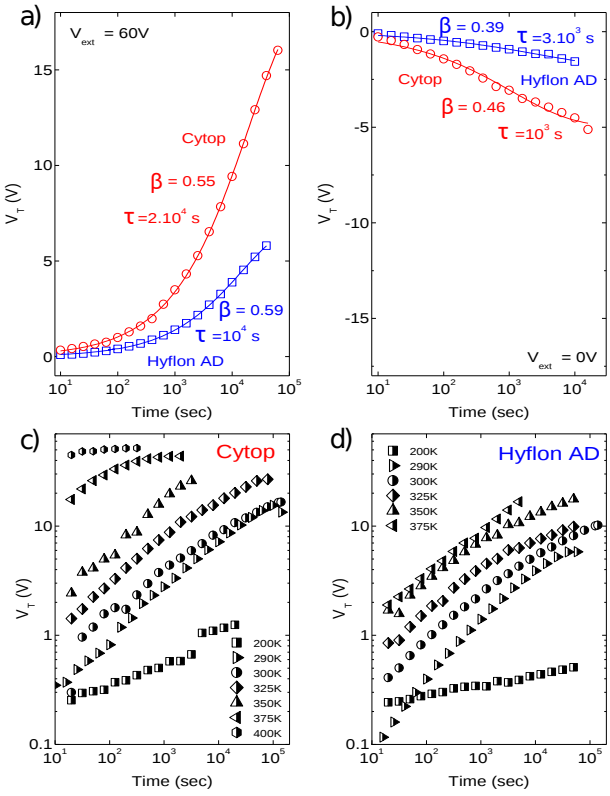

Figure 4.7: Threshold voltage shift as a function of time for top-gate PCBM transistors using Hyflon AD and Cytop dielectrics under a gate bias of 60 V (a), and while recovering (b). For both dielectrics: Cytop (c) and Hyflon (d), the stability measurements were also performed with different devices at various temperatures: 200 K, 290 K, 300 K, 325 K, 350 K, 375 K and 400 K.

Figure 4.7 shows the threshold voltage shift of PCBM transistor at room temperature in N_2 atmosphere under a gate bias of 60 V (a) and while recovering (b). Under gate bias in amorphous PCBM systems, the threshold voltage shifts toward more positive voltages. After a period of time of 16 hours, it has shifted by 6 V with Hyflon AD dielectric and by 16 V with Cytop dielectric. The mobility have decreased by only 5% and 10% over this period of time for Hyflon and Cytop dielectrics, respectively. However these threshold voltage shifts correspond to a decrease in drain current by 40% and 65% of its initial value for Hyflon and Cytop dielectrics, respectively.

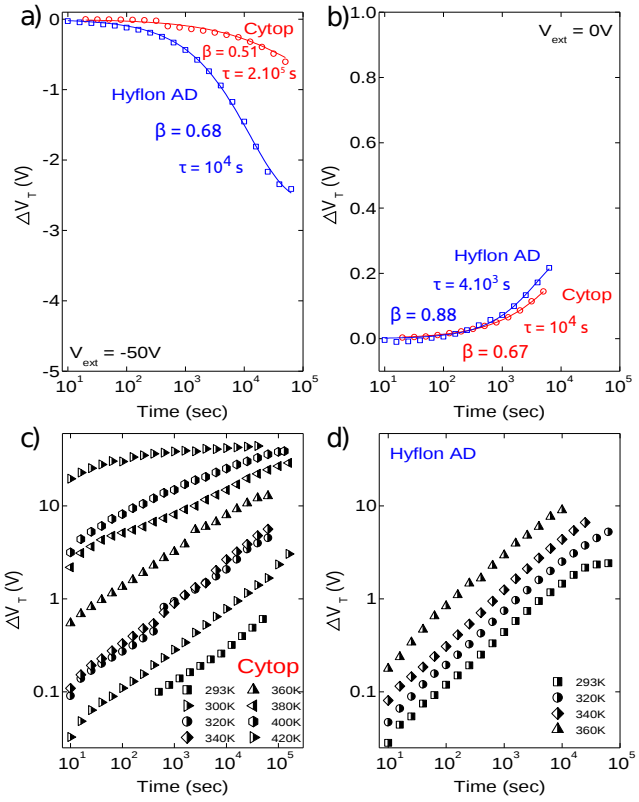

Figure 4.8: Threshold voltage shifts over time under electrical bias for diFTESADT:PTAA blend transistors with Hyflon AD and Cytop dielectrics. The gate electrode was held at -50 V during bias stressing (a) and released to 0 V for the recovering period (b). These measurements were carried out at various temperatures ranging from 293 K to 420 K.

In p-type transistors, a negative threshold voltage shift is induced under gate bias. Figure 4.8 displays the threshold voltage shift of diFTESADT:PTAA blend transistors under a gate bias of -60 V (a). These transistors exhibit excellent electrical stability under bias stress with both fluoropolymers. After 3 hours, the threshold has shifted by less than 1.5 V with Hyflon dielectric and 0.4 V with Cytop dielectric. The mobility remained constant over this period of time. These shifts can be explained by charge trapping due to defects, impurities or absorbed molecules at the interface. For Hyflon AD (900 nm) and Cytop (750 nm) dielectrics, the corresponding trapping density are found to be $2 \cdot 10^{10} \text{cm}^{-2}$ and $6 \cdot 10^{9} \text{cm}^{-2}$. During the recovery time, the trapped charge

carriers are released and contribute to the transport in the channel. The threshold voltage shifts back towards its initial value, as shown on figure 4.8 (b).

For diFTESADT:PTAA and PCBM devices, the threshold voltage shifts can be described by a stretched exponential [238]. For diFTESADT:PTAA devices, the extracted relaxation time is $\tau \sim 10^4$ s and the stretching parameter β is 0.68 with Hyflon AD, compared to $\tau \sim 2 \cdot 10^5$ s and $\beta = 0.51$ for Cytop dielectric. The threshold voltage shift at equilibrium was -2.6 V and -1.5 V with Hyflon AD and Cytop dielectric, respectively. During the recovery process, the stretching parameter was found to be higher in both cases ($\beta_{Hyflon} = 0.88$, $\beta_{Cytop} = 0.67$), suggesting that only part of the carriers are released. Summary of the bias stress parameters obtained for [60]PCBM transistors at room temperature are summarized in table 4.4.

To further investigate the trapping dynamics, electrical stability measurements were performed on these devices at various temperatures ranging from 200 K to 400 K. The measurements were performed in vacuum in the dark. Figure 4.8 and figure 4.7 illustrate the threshold voltage shifts of diFTESADT:PTAA and PCBM transistors over time at these temperatures. As it can be seen, the threshold voltage shifts faster with increasing temperature, indicating that the trapping process is thermally activated. The relaxation process was observed to be faster with higher temperature as well.

Similar results were obtained with top-gate C_{60} transistors. Other studies reported also low trap densities using Cytop as gate dielectric in transistors [163, 144]. This demonstrates that these hydrophobic fluoropolymers are ideal candidates as gate dielectrics to fabricate highly stable transistors with low-trap densities.

Table 4.4: Summary of the bias stress parameters obtained for diFTESADT:PTAA blend transistors, $PC_{61}BM$ transistors and C_{60}transistors. The parameters are extracted by fitting the threshold voltage shift over time to a stretched-exponential function.

Sc	Dielect.	W/L ($\mu m/\mu m$)	V_{ext} (V)	$\Delta V(10^4 s)$ (V)	$\Delta V(\infty)$ (V)	β	τ (s)	R^2
PCBM	Hyflon	1000/40	60	3.9	6.4±0.1	0.59±0.01	10^4	0.9992
			0	-1.6	-1.9±0.2	0.39±0.03	$3 \cdot 10^3$	0.991
	Cytop	1000/40	60	9.4	18.8±0.2	0.548±0.005	$2 \cdot 10^4$	0.99986
			0	-4.5	-5.0±0.2	0.46±0.03	10^3	0.989
TESADT	Hyflon	2000/30	-60	-1.45	-2.59±0.05	0.68±0.02	10^4	0.998
+PTAA			0	0.21	0.27±0.04	0.88±0.08	$4 \cdot 10^3$	0.990
	Cytop	1000/30	-60	-0.32	-1.5±1.2	0.51±0.06	$2 \cdot 10^5$	0.985
			0	0.14	0.36±0.08	0.67±0.02	10^4	0.9990

4.4 Molecular doping in blend organic transistors

Small molecules-polymer blends offer great promise towards high-performance solution-processed organic electronics. These blends associate the high mobility of the small molecules and the processability of polymers. Combining acene small molecules

with amorphous polymers, Jeremy et al. demonstrated high-performance transistors with hole mobility greater than 2 cm^2/Vs [67, 66, 69] and fast operating solution-processed code generator circuits [68], paving the way towards fast organic electronic circuits. The excellent electronic properties of these semiconductors films were related to the microstructure of the films. Vertical phase separation in the films was explained to result in high mobility in top-gate transistors since the small acene molecules accumulates to the top interface [66]. Two acene materials were widely investigated: 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) in the amorphous poly(dimethyl triaryl amine) (PTAA). In this study, we investigate the electronic properties of diF-TESADT small molecules in the amorphous poly(dioctyltrifluorene-co-triarylamine) (PFTAA) copolymer and the effect of p-type bulk doping in these blends.

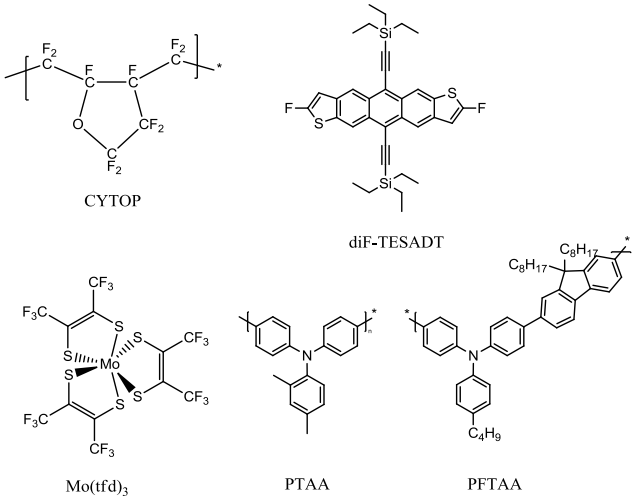

Figure 4.9: Molecular structures of Cytop insulating polymer, $Mo(tfd)_3$ dopant, diFTESADT small molecules, PTAA and PFTAA polymers.

4.4.1 Small molecule diF-TESADT and PFTAA polymer blend thin-film transistor

When used as single components, solution-processing of small diF-TESADT molecules leads to the formation of polycrystalline film with small grain size ($\sim 5\,\mu$m) and high surface roughness ($\sim$ 100 nm) [254]. Mobilities of 0.7 cm^2/Vs and 10^{-4} cm^2/Vs were reported using these films in top-gate and bottom-gate transistors. These low mobilities can be explained by the high trap density that results from the large number of grain boundaries and high surface roughness. On the other hand, amorphous polymer forms uniform and smooth films ($\sim$ 0.5 nm) but exhibit low mobility (~ 0.004 cm^2/Vs) in transistors [254]. By blending these acenes molecules in the amorphous polymer, uniform film with large-size well-ordered grains could be deposited. The solution-

processing conditions: high boiling solvent and low spin-coating rotation speed plays a major role to optimize the crystallisation and vertical phase separation. With high concentration of small molecules at the top interface, the surface roughness can however be reduced by a factor of 10 or 20, compared to pristine diFTESADT films. Saturation hole mobility as high as 2.4 cm^2/Vs were obtained using diFTESADT:PTAA blend semiconductor in top-gate bottom-gate architecture (in contrast to 0.1 cm^2/Vs in bottom-gate configuration) [66]. Now the polymer matrix PTAA is replaced with poly(dioctylfluorene-co-triarylamine) PFTAA shown in figure 4.9. Intensively studied in OLEDs, this amorphous polymer provides with suitable ohmic contact for hole injections from gold electrodes and has a higher mobility (0.02 cm^2/Vs) than PTAA. Therefore the aim of this study is increasing the conduction in top-gate transistors thanks to better transport through the polymer matrix.

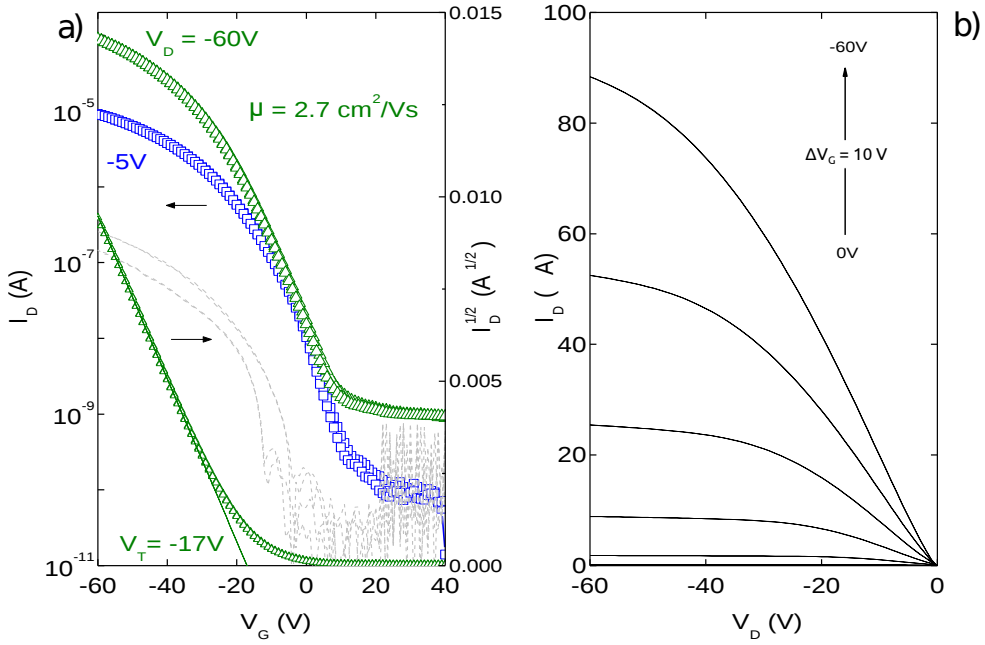

Figure 4.10: Transfer (a) and output (b) characteristics of top-gate diFTESADT:PFTAA blend TFTs. The channel width and length of the device are 1000 μm and 50 μm.

Top-gate bottom-contact diFTESADT:PFTAA blend transistors were fabricated employing the fluoropolymer Cytop dielectric and using gold source-drain contacts. The 40 nm thick gold electrodes were treated with the pentafluorobenzene thiol (PFBT) self-assembled monolayer to improve charge injection to the polymer. A solution of diFTESADT:PFTAA in tetralin was spun first at 500 rpm for 10 s, followed by a step at 2000 rpm for 20 s. The first slow stage of spin-coating offers more time for good crystallization and vertical phase separation of the blend. The film was then dried at 100 for 15 min to obtain a thickness of 50-70 nm. The fluoropolymer Cytop was spun at 2000 rpm for 60 sec and dried at $100°C$ for 15 min. Further post-annealing process was observed not to affect the electronic performances. Devices

were completed by evaporation of 50 nm thick aluminium electrodes.

Figure 4.10 shows the typical transfer and output characteristics of top-gate diF-TESADT:PFTAA blend TFTs (the channel width and length are 1500 μm and 50 μm, respectively) measured in N_2 atmosphere. This transistor exhibit excellent characteristics with negligeable hysteresis, a high current on/off ratio of 10^5, a threshold voltage of -17 V and a subthreshold slope of 11 V/dec. The maximum hole mobility was found to be 2.7 cm^2/Vs in saturation regime. However the significantly lower mobility value (1.5 cm^2/Vs) extracted in linear regime and the non-perfect linear output curves at small drain voltages suggest that charge injections from the electrodes to the polymer are not completely optimized, but leave the door open for even higher mobility values. Over the different samples measured (~15), excellent characteristics were observed with good reproducibility and device yield (>80 %). 8 devices exhibited a mobility greater than 1 cm^2/Vs. These mobility found for diF-TESADT molecules in PFTAA copolymer are comparable, if not higher, to those obtained for acene molecules in PTAA polymer [66]. The current on/off ratio is slightly increased due to a decrease of the off current, compared to the diFTESADT:PTAA blend.

4.4.2 Molecular bulk doping of blend semiconductors

Having demonstrated high-performance transistors employing diF-TESADT molecules blended in PTAA and PFTAA polymers, the effects of p-type doping is investigated in these blends. Smith *and al.* observed that the trap concentration and energetic distribution is related to the morphology of the blend film [69]. The aim of p-type doping is to enhance the mobility, by screening the hole traps that are located at the grain boundaries, and to reduce the contact resistance. The dopant compound used in our study is the organometallic complex molybdenum tris-[1,2-bis(trifluoromethyl)]ethane-1,2-dithiolene] ($Mo(tfd)_3$), shown in figure 4.9. This molecule was synthesized and provided by Professor Marder from Georgia Tech, USA. Kahn *et al.* reported the use of this molybdenum dithiolene complex in semiconductor films [255, 256].

In our experiment, in order to prepare the doped semiconductor film, the complex was first dissolved in chlorobenzene and then mixed at various concentration (0.1 %, 0.5 %, 1.0 % wt) to the blend (1:1) solution in tetralin. After few hours stirring on a hot plate, the film was deposited by spin-coating and dried for 5 min at 100°C. Devices were completed by following the standard procedure used for our top-gate transistors (see previous section).

The transfer characteristics in saturation of undoped and doped diFTESADT:PFTAA blend transistors are presented in figure 4.11. For each device, the same features (channel width W = 1500 μm and channel length L = 100 μm) were chosen for more relevant comparison. For the different dopant concentrations, the transistor performances for these blend films, as well as those obtained in diFTESADT:PTAA blends (results reported from the work done by Jeremy Smith), are displayed in table 4.5.

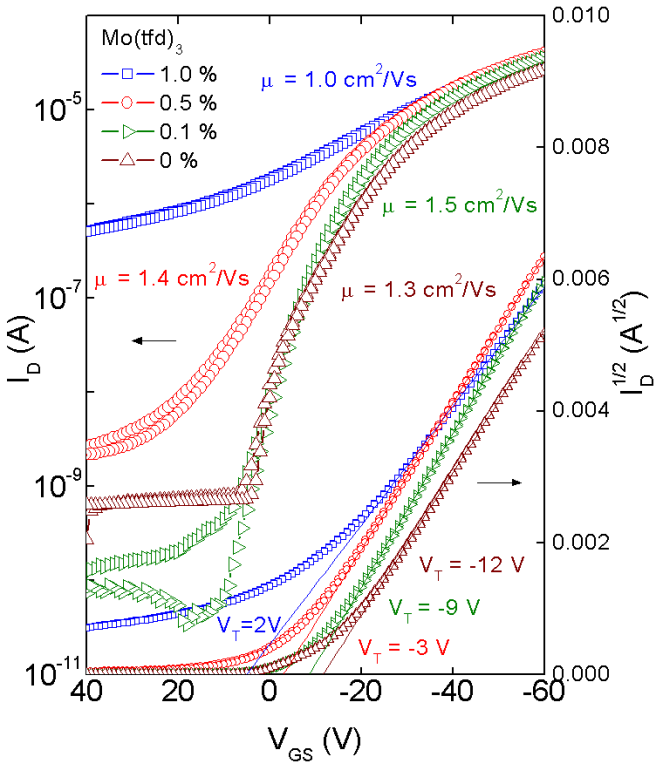

Figure 4.11: Transfer (a) and output (b) characteristics of a diF-TESADT:PFTAA blend transistors doped with $Mo(tfd)_3$. The concentrations of the p-type doping in the semiconductor film are 1 wt%, 0.5 wt%, 0.1 wt% and 0 wt%.

In both studies, doping of the semiconductor films leads to an increase of the mobility, a reduction of the threshold voltage and contact resistance. By doping the diFTESADT:PFTAA blend with a concentration of 0.1 %, an increase in saturation mobility from 1.36 cm^2/Vs to 1.56 cm^2/Vs is observed. The current on-off ratio was also improved by one order of magnitude and the subthreshold swing reduced to 8 V/dec. However, above a certain concentration, with increasing concentration, the mobility decreased (down to 1 cm^2/Vs at 1 %) and the subthreshold slope increased (above 39 V/dec at 1 %). The additional dopant may not act as deactivation trapping sites but rather as an impurity. For acene molecules blended in PTAA polymer matrix, the highest hole mobility was reached at a doping concentration of 1%. The threshold voltage can be reduced by increasing the dopant concentration. The threshold voltage decreased from -12 V for undoped transistors, to -9 V at a concentration of 0.1 wt% and down to -3 V at a concentration of 0.5 wt%. These improvements are attributed to the deactivation of traps. To further understand this doping effect, temperature mobility dependent measurements were carried out on diFTESADT:PTAA blend semiconductors. The change from double activation energy to single activation energy in the mobility characteristics when doping (1%) the blend confirmed this explanation.

Table 4.5: Summary of the electrical parameters obtained for the diF-TESADT:PFTAA blend transistor doped with $Mo(tfd)_3$ molecules at various concentrations (1.0 wt%, 0.5 wt%, 0.1 wt% and 0 wt%). Parameters obtained assuming a geometric capacitance of 1.2 nF/cm^2. The device features (W=1.5 mm, L = 100 μm) are the same for the different devices.

TESADT+ polymer:	$Mo(tfd)_3$ (wt%)	μ_{lin} (cm^2/Vs)	μ_{sat} (cm^2/Vs)	V_T (V)	I_{on}/I_{off} (A/A)	SS (V/dec)	μ_i (cm^2/Vs)	$V_{T,i}$ (V)	R_c ($G\Omega/\square$)
PTAA	0		2.03	-5.0	10^4		1.16	-3.8	140
	0.1		2.06	-4.7	$10^{3.3}$				23
	1		2.60	-2.2	$10^{2.3}$				1.2
	2	no gate modulation was observed at this concentration							
PFTAA	0	0.89	1.36	-12.3	$10^{4.5}$	11.9	0.68	-6.0	
	0.1	1.05	1.56	-9.1	$10^{5.3}$	8.3	1.01	-11.8	
	0.5	1.10	1.41	-3.4	10^4	12.0	1.51	-7.7	
	1	1.00	1.01	2.2	10^2	38.7	1.62	-8.4	

However, p-doping in the semiconductor blends is also accompanied by an increase in the off current in transistors and consequently by a significant reduction in the current on/off ratio. In doped diFTESADT:PFTAA blend (1 %), the current on/off ratio was reduced by three orders of magnitude compared to undoped transistors. At higher doping concentration the transistors show no gate field modulation. In that case the channel current become independent of the gate voltage and typically of high magnitude. For each blend system, estimation of the appropriate amount of dopant in the semiconductor film (by a dichotomy approach) is important to balance between the different device performances: enhancement of the mobility, reduction of the threshold voltage while keeping a descent current on/off ratio.

One of the main effect of p-type doping was the reduction of the contact resistance in the doped transistors. In undoped films, the output curves showed non-ideal ohmic contacts. Previous studies showed that in these blends the vertical phase separation within the semiconductor film results in a preferential crystallization of the diFTESADT small molecules at the top interface. Given that the polymer matrix is deposited at the bottom, the position of its HOMO level is crucial for efficient injections of holes from the gold electrodes to the semiconductor film. The barrier height between the bottom PFBT-treated Au S-D contacts (-5.8 eV) and the PFTAA polymer matrix (-5.4 eV) whereas the HOMO level (-5.2 eV) of the PTAA polymer matrix is closer to the gold electrodes (energy levels were obtained by combining UPS He and IPES measurements) [69]. However the potential energy barrier for hole injection may not be the only reason for lower contact resistance, the fluorine-fluorine interaction between diFTESADT and the SAM molecules may also results in better crystallization of the blend on the Au-SAM electrodes. When $Mo(tfd)_3$ dopant is added to the semiconductor blend, the injection from the electrodes to the semiconductor is clearly improved as a much better linearity of the output curves at low drain voltages (not shown in this work) was observed for higher dopant concentrations. Reduction in the difference between the mobility values extracted in the saturation regime and linear

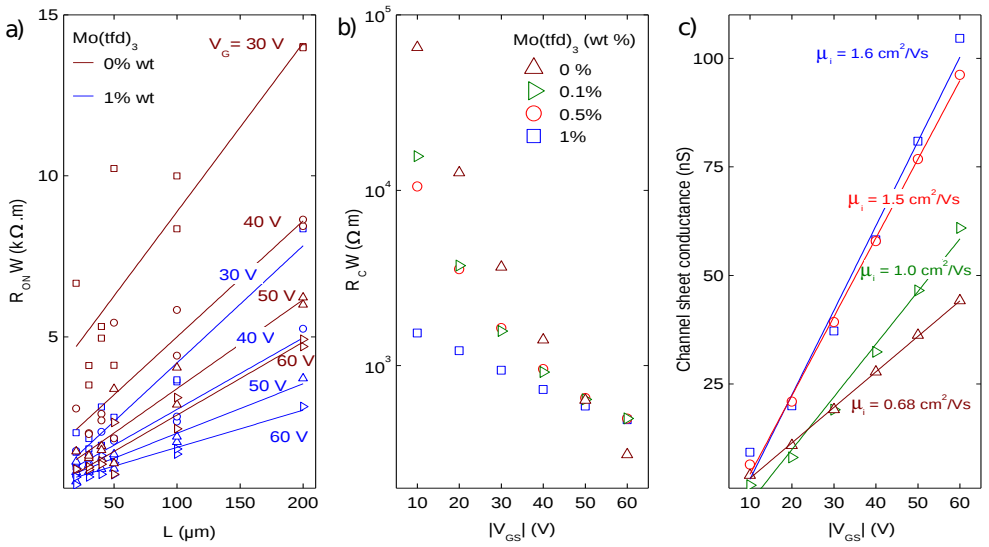

Figure 4.12: Width-normalized total ON resistance of undoped and doped (1%) diFTESADT:PFTAA blend transistors as a function of channel length (ranging from 20 μm to 200 μm) for different gate voltages (from 30 V to 60 V) (a). Width-normalised parasitic contact resistance as a function of gate voltage in transistors for the different doping concentration (0%, 0.1%, 0.5% and 1%) (b). Channel sheet conductance as a function of gate voltage for the different doping concentrations (c).

regime is also characteristic of more efficient carrier injection from the electrodes to the polymer matrix. A difference of 33 % in mobility was observed between the linear and saturation regimes for undoped or low concentration dopant (0.1 %) while the mobility was identical in both regimes for a doping concentration of 1 %. The increase in hole mobility with increasing channel length suggested the presence of high parasitic contact resistance in these devices, especially in the undoped ones.

To quantify this reduction in contact resistance with increasing doping concentration, charge injections at the electrodes was studied using the scaling law method. Figure 4.12 (a) shows the total device resistance (R_{ON}) of undoped and doped (1% wt) diFTESADT:PFTAA TFTs at small drain voltages. The total device resistance (R_{ON}) consists of the channel resistance (R_{ch}) in series with the contact resistance at the electrodes (R_c). We observe that for each gate voltages the total resistance is significantly lower in transistors with doped blend semiconductors, compared to undoped ones. Using the transmission line method, the contact resistance (corresponding to the extrapolation of the total device resistance at L = 0 μm) and the channel sheet conductance ($\left[\frac{\triangle(R_{ON}W)}{\triangle L}\right]^{-1}$) were extracted for each gate voltage and for the different doping concentrations. Figure 4.12 (b) presents the contact resistance as a function of gate voltages for the different doping concentrations. The contact resistance is relatively important compared to the channel resistance and depends strongly on the gate voltage. Worth mentioning is the significant decrease in contact resistance with increasing doping concentration. The contact resistance is reduced

by 35 % with a doping concentration of 0.1 % and 50 % with a concentration of 1 %, compared to undoped semiconductor films, at a gate voltage of 40 V. For the highest concentration (1 %), a reduction by one order of magnitude is observed at V_G = 20 V. As can be seen from figure 4.12 (c), the sheet conductance is linear with gate voltages and is significantly improved with increasing doping concentration, indicating better charge transport in the conducting channel. From the gate bias linear dependence of the channel sheet conductance, intrinsic device parameters independent of the channel length can be extracted The intrinsic linear mobility (μ_i) and threshold voltage ($V_{T,i}$) were found to be 0.68 cm^2/Vs and 6 V, respectively, in undoped diFTESADT:PFTAA blend TFTs. The intrinsic linear mobility increases with increasing doping concentration. Parameters obtained for the different doping concentrations are reported in table 4.5. An intrinsic hole mobility as high as 1.6 cm^2/Vs was obtained for a doping concentration of 1 % (the highest in this study). This value is higher than the intrinsic mobility reported for diFTESADT:PTAA transistors with pentafluorobenzene thiol (PFBT) treated gold electrodes (1.2 cm^2/Vs), but lower to the devices with 3-fluorobenzene thiol (3-PBT) treated gold electrodes (2.8 cm^2/Vs) [66].

Addition of the organometallic complex $Mo(tfd)_3$to acene:polymer blends has shown efficient p-doping effect in these semiconductor films. This approach leads to enhanced carrier mobility, reduction of the contact resistances and better charge transport. This results from the deactivation of traps in the presence of the doping molecules. In order to leap ahead towards high-mobility solution-processed semiconductors, our plan is to expand this molecular doping technique to systems with high hole mobility and see whether, and how much more, the doping effect can improve the performance. The aim would be to demonstrate solution-processed organic transistors with hole mobility in the range 5-10 cm^2/Vs. Further investigations would benefit from vertical profiling of the film by dynamic secondary ion mass spectrometry (DSIMS) to determine the distribution of the dopant in the blend film.

Conclusion

In summary, we have demonstrated both p- and n-type high-performance solution-processed organic transistors using Hyflon AD as gate dielectrics. This amorphous fluoropolymer exhibits excellent insulating properties with a low leakage current (10^{-8} A/cm^2) and a high dielectric strength (4 MV/cm). The orthogonality of Hyflon fluorinated solvents, to most conventional organic semiconductors, allows fabrication of top-gate transistors employing both polymer and small molecule semiconductors. This optically-transparent water-repellent polymer yield organic transistors with excellent high charge carrier mobility, hysteresis-free operation and high stability under electrical stress. Its transparency, excellent insulation and water repellent properties make Hyflon AD fluoropolymer an ideal candidate for solution-processable gate dielectrics for OTFT applications.

Chapter 5

Low-voltage organic transistors based on self-assembled monolayer dielectrics

The large power consumption in conventional organic electronics is problematic and reduction in the operating voltage of organic transistors is crucial for successful implementation in battery-powered applications. Self-assembled monolayer (SAM) gate dielectrics are a promising approach toward high-performance low-voltage organic transistors. Such molecular nanodielectrics provide the high geometric capacitance ($C_i \sim 500$ nF/cm^2) necessary for low-voltage transistor operation.

In this study, we investigate the surface and electrical properties of several alkyl phosphonic acid self-assembled monolayers and their potential as ultra-thin dielectric in OTFTs. Phosphonic acid molecules were chosen because of their superior stability compared to silane SAMs. High-quality monolayer dielectrics with low leakage current were formed onto evaporated patterned aluminium gate electrodes at room temperature. The surface properties of these monolayers were assessed by surface energy measurements and AFM measurements. The electrical properties of the hybrid SAM-alumina dielectric were investigated using metal-insulator-metal (M-I-M) structure. Given the good insulating properties of these SAMs, low-voltage solution-processed organic transistors were demonstrated in bottom-gate top-contacts architecture. The threshold voltage in these devices can be tuned by chemical tayloring of the SAM molecule. Electrical stability measurements, investigated for a wide range of semiconductors and SAM dielectrics based OTFTs, showed that bias-stress induced threshold voltage shift follows a stretched exponential time dependence with a time constant in the range 10^3-10^5 s. With the prospect of demonstrating their potential

in logic circuits, low-power unipolar and complementary inverters were demonstrated employing transistors based on these SAM gate dielectrics.

5.1 SAM functionalization and characterization

Self-assembled monolayers are densely packed and self-ordered molecular assemblies of small molecules. Deposited on metals, on oxides or on passivated Si surfaces by spontaneous absorption or vapor deposition, they can be used as passivation/injection layer over electrodes, as a passivation layer over thick dielectrics or as the dielectric itself. In our study, we will focus mainly on phosphonic acids SAM and their use as molecular gate dielectric on evaporated aluminium electrode in OTFTs. The molecular structures of the SAM molecules used in this study are depicted on figure 5.1.

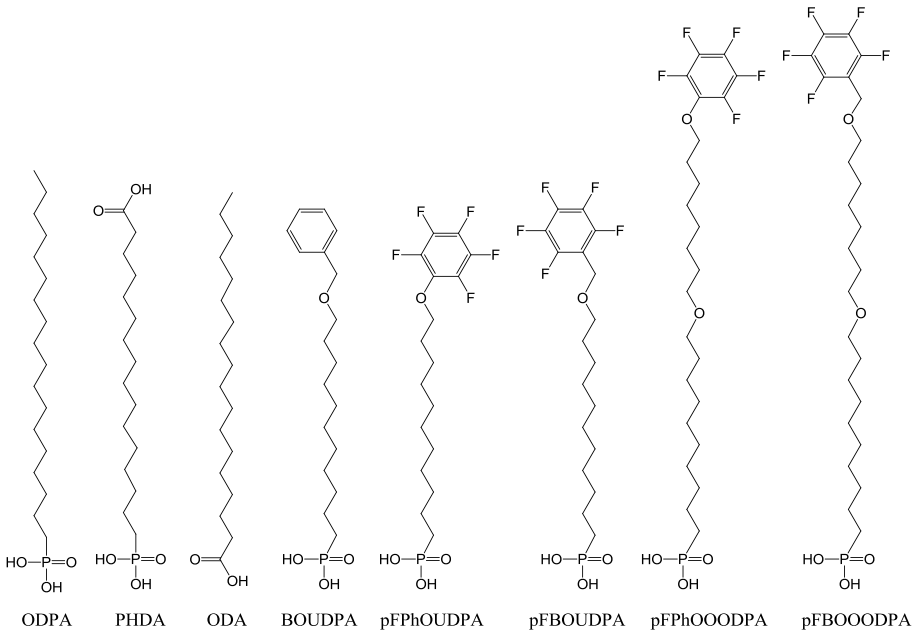

Figure 5.1: Molecular structures of the various self-assembling monolayer molecules that have been studied in this work: from left to right, octadecylphosphonic acid (ODPA), phosphonohexadecanoic acid (PHDA), octadecanoic acid (ODA), 11-(benzyloxy)undecylphosphonic acid (BOUDPA), perfluorophenoxyundecylphosphonic acid (pFPhOUDPA), perfluorobenzyloxyundecylphosphonic acid (pFBOUPA), perfluorophenoxyoctaoxydecylphosphonic acid (pFPhOOODPA) and perfluorobenzyloxyoctaoxydecylphosphonic acid (pFBOO ODPA).

One of the most commonly used and well studied SAM molecule is the octadecylphosphonic acid (ODPA, from Sigma-Aldrich). The phosphonic end-group reacts with the alumina surface to form P-O-Al bond while the long alkyl chain ensure the insulating properties of the layer. More details on the SAM functionalization technique is provided in section 3.1.4. The other studied molecular chains have also a phosphonic acid as an anchoring group but incorporate a different end group and/or

oxygen atoms are inserted in the alkyl chain. Our primary interest was to demonstrate their potential as a dielectric and secondly to investigate the effect of different terminal groups on the morphology of the semiconductor layer and their influence on the performance of the OTFTs.

The other two SAMs, phosphonohexanoic acid (PHA) and phosphonohexadecanoic acid (PHDA)(from Sigma-Aldrich), have a carboxylic acid as a end group, the first one having only 6 atoms on its carbon chain while the second has 16. As a carboxylic acid can also act as the anchoring for alumina, the orientation of these molecules was studied by James Ball and is summarized in this work. Benzyloxyundecylphosphonic acid (BOUDPA, from Solvay) has a benzyl end group and was chosen for its potential to favour nucleation of semiconductors on its surface.

Experimentally it was found more tricky to fabricate and obtain high performance p-type OFETs based on SAMs dielectrics than n-type ones. One way to tackle this could be to promote hole transport by adding suitable chemical groups or atoms at the end of the SAM molecule. In general, one can imagine engineering the SAM molecule to tune the electronic properties (for instance the threshold voltage) of organic transistors. For that purpose, a full range of phosphonic acid SAMs with perfluorinated benzyl ring were synthesized by Solvay and tested in our OTFTs structures. The molecules are perfluorophenoxyundecylphosphonic acid (pFPhOUDPA), perfluorobenzyloxyundecylphosphonic acid (pFBOUDPA), perfluorophenoxyoctyloxydecylphosphonic acid (pFPhOOODPA) and perfluorobenzyloxyoctyloxydecylphosphonic acid (pFBOOODPA). They differ by the length of the chain and the presence of the methyl group next to the phenyl ring.

5.1.1 Contact angle measurements

Contact angle measurements are performed on the SAMs surfaces in order to confirm the presence of the monolayer on the Al-AlO_x surface and assess the wetting behaviour of the semiconductor on the SAM surface. In the presence of a SAM, the surface is more hydrophobic than aluminium oxide because of the long alkyl chain (i.e. in the case of ODPA). In addition to that the hydrophilicity of the end group has to be considered. Upon functionalization, a change in the contact angle between the two surfaces indicates the presence of the monolayer. For each SAM surface, the contact angles with the different liquids are summarized in table 5.1 and figure 5.2 shows the water droplet on these surfaces. As explained in section , the surface energies of the Al-AlOx-SAM structures were analysed following the Owens-Wendt-Kaelble method.

Exhibiting a water contact angle of 110°, ODPA SAM is considered to be highly hydrophilic. It exhibits low surface energy ($\gamma_T = 28.2$ mN/m) dominated by non-polar interactions ($\gamma_D = 27.3$ mN/m) [180, 181]. This can be explained by its long alkyl chain (and its methyl group at the end). If this highly hydrophobic property prevents the absorption of water molecules on the surface, its low surface energy makes also solution-processing of any semiconductor solution much more challenging.

Compared to ODPA, PHDA has much higher polar component ($\gamma_P = 17.2$ mN/m). This can be attributed to the carboxylic group at the end of the alkyl chain. These higher surface energy allow organic polymer or even small molecules to be spin-cast onto the SAM surface. With the deposition of PHDA on alumina, the question of which end group functionalize on the AlO_x remains open since both phosphonic acid and carboxylic acid precursor can bond to the AlO_x surface. In order to determine the orientation of PHDA molecule on alumina, James Ball et al. compared the wetting behaviour and leakage current density of ODPA and PHDA to a third SAM molecule, octadecyl carboxylic acid (ODA) [181]. The latter has 18 carbon atoms incorporating one carboxylic anchoring group. When functionalized, ODA presents a lower contact angle than ODPA despite having the same methyl end group, most likely suggesting the formation of a lower density monolayer. This is partially confirmed by the much higher leakage current density. Because the phosphonic acid group has a higher affinity towards AlO_x than the carboxylic acid, this suggests that the majority of active anchoring groups in PHDA SAM is the phosphonic acid.

For the four perfluorinated SAMs, the water contact angle was measured above 90° and the surface energy analysis showed highly dispersive component and low polar component. This confirms the highly hydrophobic properties of these fluorinated SAM molecules.

From the dispersive and polar surface energy value, the $\theta = 0°$ wetting envelopes can be calculated and plotted (as shown on figure 5.2). Any solution whose surface energy lies within the wetting envelope are more likely to wet the surface and form good homogeneous film by solution-processing. Except for PHDA that presents large wetting envelopes, solution-processing of semiconductor solutions was found problematic for most SAMs studied. Experiences showed that good film formation was possible on PHDA SAM dielectric with P3HT polymer, diFTESAFT and [60]PCBM small molecules. Wöbkenberg et al. reported the fabrication of solution-processed SAM-based OTFTs employing the small molecule fullerene derivative F17-DOPF, and demonstrate mobility up to 0.4 cm^2/Vs. To demonstrate the potential of SAM dielectric in OTFTs, vacuum-sublimation technique was employed for deposition of the organic semiconductor [48, 178, 183, 184].

5.1.2 Morphology of the SAM surface

AFM measurements of the SAM surfaces were performed in tapping mode. Despite the high resolution that the contact mode provides, the AC mode was thought more appropriate as the first one could have raised issues with the SAM surface due to the possible capillar forces (in the case of water on the SAM surface) and/or to the electrostatic charges associated with the SAM end group. Figure 5.2 (b) displays the surface topography of Al-AlO_x/ODPA. Compared to silicon dioxide dielectric (RMS ~ 0.1-0.2 nm) [54], our SAM nanodielectrics present a high surface roughness with a root-mean-square value of 3.3 nm. This topography corresponds to the surface

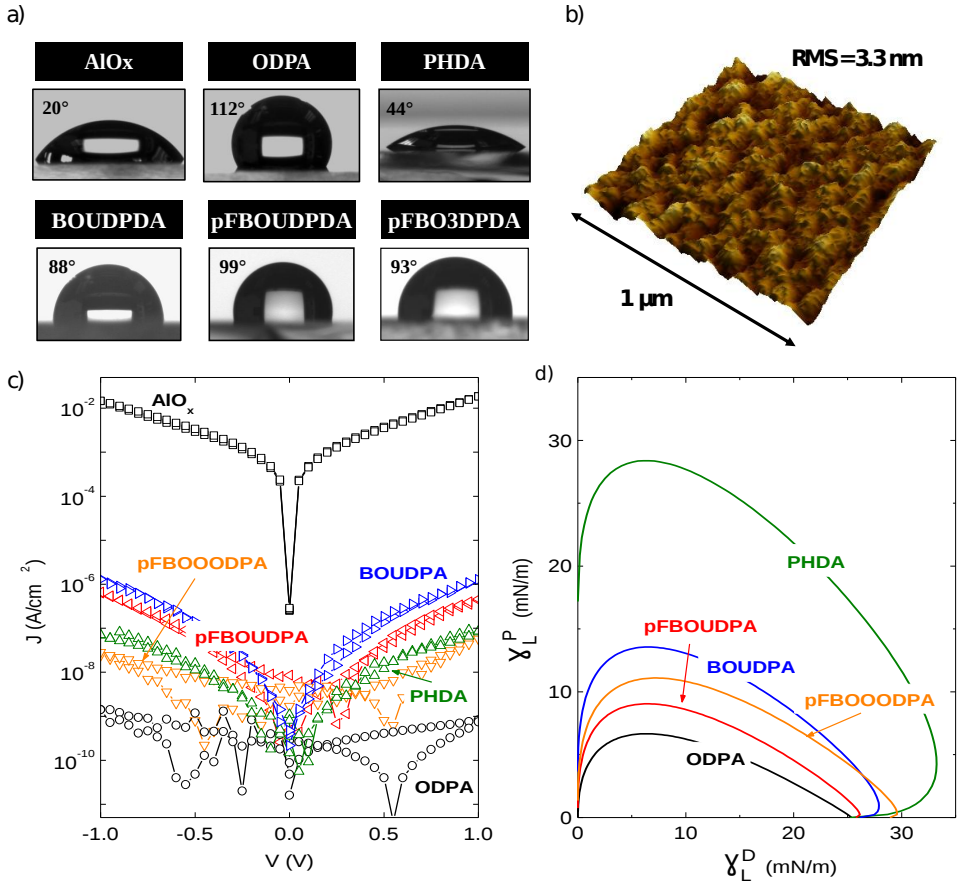

Figure 5.2: (a) Water droplets on AlOx, ODPA, PHDA, BOUDPA, pFBOUDPA and pFBOOODPA SAM surfaces. (b) AFM tapping mode image of the surface topography of Al-AlO_x/ODPA. (c) Leakage current densities measured in parallel plate M-I-M structures of area $A = 2.5 \cdot 10^{-3} cm^2$. d) Wetting enveloppes ($\theta = 0°$) of SAM surfaces and surface energy values of few semiconductors solutions.

roughness of the aluminium oxide as similar RMS values were measured after oxidation of the electrode and before SAM functionalisation.

5.1.3 Capacitance measurements

The dielectric properties of self-assembled monolayers were evaluated using the parallel plate metal-insulator-metal (M-I-M) structure. In this structure, the SAM, sandwiched between two metalic electrodes, plays the role of a capacitor due to its long aliphatic chain. In our study, Aluminium electrodes (40 nm) were evaporated through shadow mask and oxidized by plasma ashing. The self-assembled monolayers were then functionalized on the aluminium oxide (more details on the functionalization can be found in section 3.1.4). A second top electrode (40 nm) was evaporated through a shadow mask. The resulting dielectric is hybrid as it's composed of the alumina (5-10 nm) and self-assembled monolayer (2-5 nm). Geometrical capacitances were measured

as a function of AC frequency (f) with the Solatron 1260A Impedance/Gain-Phase analyser or Keithley 4200 parameter analyser. Nine diodes with area $A = 2.5 \cdot 10^{-3}$ cm^2 were tested for each SAM dielectrics. For each SAM dielectrics, the geometrical capacitance value obtained is used to extract the field-effect mobility from the transistor characteristics and is summed up in table 5.1. The capacitance of these dielectrics ranges between 200 nF/cm^2 and 1 μF/cm^2, close to supercapacitance. Compared to SiO_2 dielectric (8.6 nF/cm^2 with $t_{SiO2} = 400$ nm), these ultrathin dielectrics allow the accumulation of the same amount of charge in transistors channel while operating at much lower voltages.

The geometrical capacitance obtained for ODPA SAM on AlOx (C_i ~ 250-450 nF/cm^2) is slighty lower than the value reported by Klauk et al. [47, 48]. This could be explained by a different thickness in the alumina as accurate control over the oxide thickness is difficult (it can vary from 5 to 10 nm). Compared to ODPA and PHDA SAMs (C_i ~ 300-500 nF/cm^2), these SAMs exhibit high capacitance values (C_i ~ 600-800 nF/cm^2). When comparing between PFBOUDPA and BOUDPA SAMs (they have the same molecular structure except the F atoms instead of H atoms on the phenyl ring), the PFBOUDPA SAM (800 nF/cm^2) dielectric has a higher geometrical capacitance than BOUDPA dielectric (600 nF/cm^2). A significant reduction of geometrical capacitance from 800 nF/cm^2 to 600 nF/cm^2 is observed when the short chain length SAM molecules (PFPhOUDPA and PFBOUDPA SAM) are replaced with long chain length SAMs (PFPhOOODPA and PFBOOODPA).

5.1.4 Current versus voltage measurements

The current density (J) between the two metal electrodes as a function of voltage is shown on 5.2 (c). Values of the current density at ±1 V are summarized in table 5.1. The current density through the alumina AlOx layer was measured to be $10^{-3} - 10^{-2}$ A/cm^2. The presence of the SAM monolayer allows the reduction of the current density by several orders of magnitudes. The current density value found for ODPA are as low as 10^{-9} A/cm^2, show that its long alkyl chain is an excellent insulator and that can be used as gate dielectric. The other SAM dielectrics presented leakage current densities, ranging from $10^{-8} - 10^{-7}\, A/cm^2$ for PHDA or pFBOOODPA SAMs to $10^{-6} - 10^{-5}$ A/cm^2 for pFPhOUDPA and pFPhOOODPA SAMs. Only dielectrics presenting low leakage density, below $\sim 10^{-6}$ A/cm^2, could be implemented as gate dielectrics in transistors. As an example, field-effect couldn't be demonstrated using pFPhOUDPA and pFPhOOODPA SAMs. Similar to ODPA SAM, pFBOOODPA SAM present excellent insulating properties ($J \sim 10^{-8}$ A/cm^2).

In order to evaluate the dielectric breakdown, higher voltages (2-5 V) were applied across the MIM structure. For the four different SAMs, the breakdown was observed to be around 2.5-3 V, which corresponds to an electric field of $2.5 - 3.0 \times 10^8$ V/cm.

C-V measurements and leakage current measurements indicate which SAM are likely to be successfully implemented as gate dielectric in transistors. The following

section will present the performance of organic transistors based on these suitable SAMs. If ODPA SAM is still the phosphonic SAM which offers the best insulating properties as a dielectric, a broader range of phosphonic acid SAMs could potentially provide a better insight into the effect of end-group on transistor performances.

Table 5.1: Summary of the surface and electrical properties of SAM functionalized on AlOx/Al. Geometrical capacitances and leakage currents are measured using parallel plate M-I-M structures of area $A = 2.5 \cdot 10^{-3}$ cm^2. Litterature values for different SAM dielectrics are also included for comparison [48, 180, 178, 181, 184, 183].

SAM	θ_{water} (°)	γ_D (mN/m)	γ_P (mN/m)	J (at V_{MIM}) (A/cm^2)	C_i (nF/cm^2)	Ref.
AlO_x	20	21.6	42.0	10^{-3}–10^{-2}(1V)		
ODPA	112	27.3	0.9	10^{-9}–10^{-7}(1V)	450	[180]
ODA		25.2	7.6	$10^{-5} - 10^{-4}$		[181]
PHA					900	
PHDA	44	25.2	17.2	10^{-8}–10^{-6}(1V)	550	[181]
BOUDPA	88	26.1	3.7	1.10^{-6}(1V)	600	
pFPhOUDPA	96	18	2.9	6.10^{-6}(1V)	850	
pFBOUDPA	99	25.8	0.8	5.10^{-7}(1V)	800	
pFPhOOODPA	99	25.6	0.7	2.10^{-6}(1V)	625	
pFBOOODPA	93	28.9	1.3	6.10^{-8}(1V)	600	
AlO_x				$5 \cdot 10^{-5}$(2V)		[48]
ODPA	108	19.9	0.11	$5 \cdot 10^{-8}$(2V)	700	[48, 184]
PDF-ODPA	118	11.9	0.05			[184]
DDPA	110	18.8	0.2	10^{-5}(3V)	750	[183]
pFDDPA	121	8.5	0.5	$5 \cdot 10^{-6}$(3V)	750	[183]
AlO_x	<10			$2 \cdot 10^{-6}$(2V)	950	[178]
ODPA	107			$8 \cdot 10^{-8}$(2V)	600	[178]
π-σ-PA1	83			$5 \cdot 10^{-8}$(2V)	760	[178]
π-σ-PA2	84			$5 \cdot 10^{-8}$(2V)	700	[178]

5.2 Hole and electron transporting SAM-based transistors

Electrical measurements of SAMs showed that those ultrathin dielectric offer the much sought-after properties required for gate dielectrics in transistors: good insulating property, good thermal stability and high geometrical capacitance. However, few further properties need to be investigated before they can be utilized in low-power low-cost electronic circuits: compatibility with both hole and electron (and possibly ambipolar) semiconductors, good electrical stability and easy fabrication via solution-processing. To date low-voltage transistors based on phosphonic acid SAMs have been reported by several groups [47, 178]. The deposition technique used in these studies is usually vacuum sublimation. In the present study, both hole and electron transporting transistors are demonstrated using vacuum sublimation as well as spin-coating as the deposition techniques.

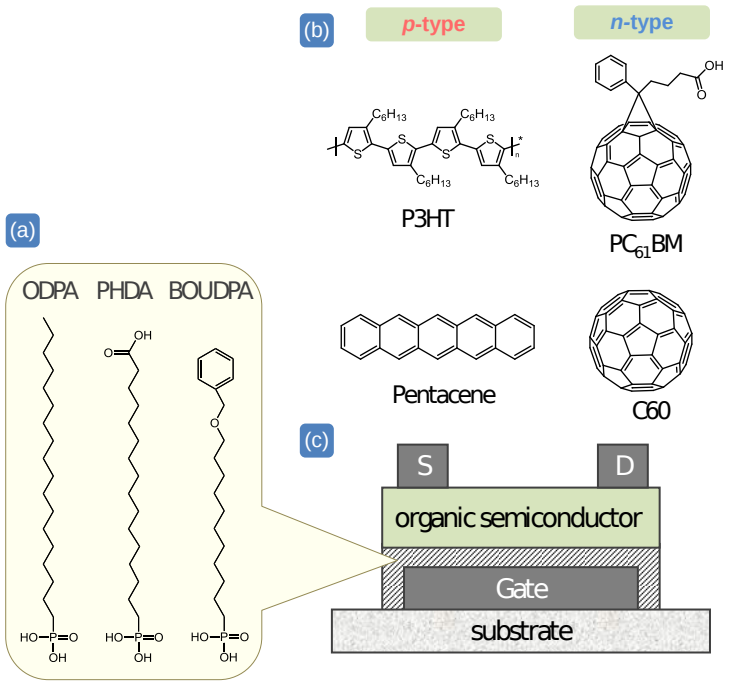

Figure 5.3: (a) Molecular structures of the self-assembling monolayer molecules used herein: octadecylphosphonic acid (ODPA), phosphonohexadecanoic acid (PHDA) and 11-(benzyloxy)undecylphosphonic acid (BOUDPA). (b) Molecular structures of the different organic semiconductors used in this study: P3HT (p-type, spin-coated), [60]PCBM (n-type, spin-coated), pentacene (p-type, evaporated) and C_{60} (n-type, evaporated). (c) Schematic of the bottom-gate top-contact architecture used in low-voltage organic transistors based on self-assembled monolayer dielectrics.

These SAM-based organic field-effect transistors are fabricated in a bottom gate - top contacts (BG/TC) configuration (figure 5.3(c)). After Al surface oxidation, the self-assembled monolayer is functionalized on top of the AlO_x gate electrode by submersion of the substrate in solution (see section 3.1.4). The substrates were then annealed overnight at 140°C under N2 atmosphere followed by the semiconductor deposition. The molecular structures of the different SAM molecules and semiconductors used in this study are depicted in figure 5.1. [60]PCBM and P3HT were spin-coated at 1000 rpm for 60 s from chlorobenzene solutions, at concentrations of 20 mg/mL and 10 mg/mL, respectively. C_{60} and pentacene were deposited by thermal sublimation at a rate of 1 $\AA s^{-1}$ under high vacuum (10^{-9} bar). Finally, 50 nm thick source and drain contacts were evaporated through a shadow mask to define the transistor channel. Aluminium was chosen as the S/D electrodes for n-type materials (i.e. [60]PCBM and C_{60}) and gold for p-type materials (i.e. P3HT and pentacene). P3HT devices were first annealed at 110 °C (1 hour) and then at 150 °C (1 hour) before electrical characterization in order to improve carrier transport. Electrical characterization was performed using a Keithley 4200 semiconductor parameter analyser in nitrogen, except for pentacene devices for which characterization was carried out in

vacuum after a short exposure (~ 5 min) to ambient air.

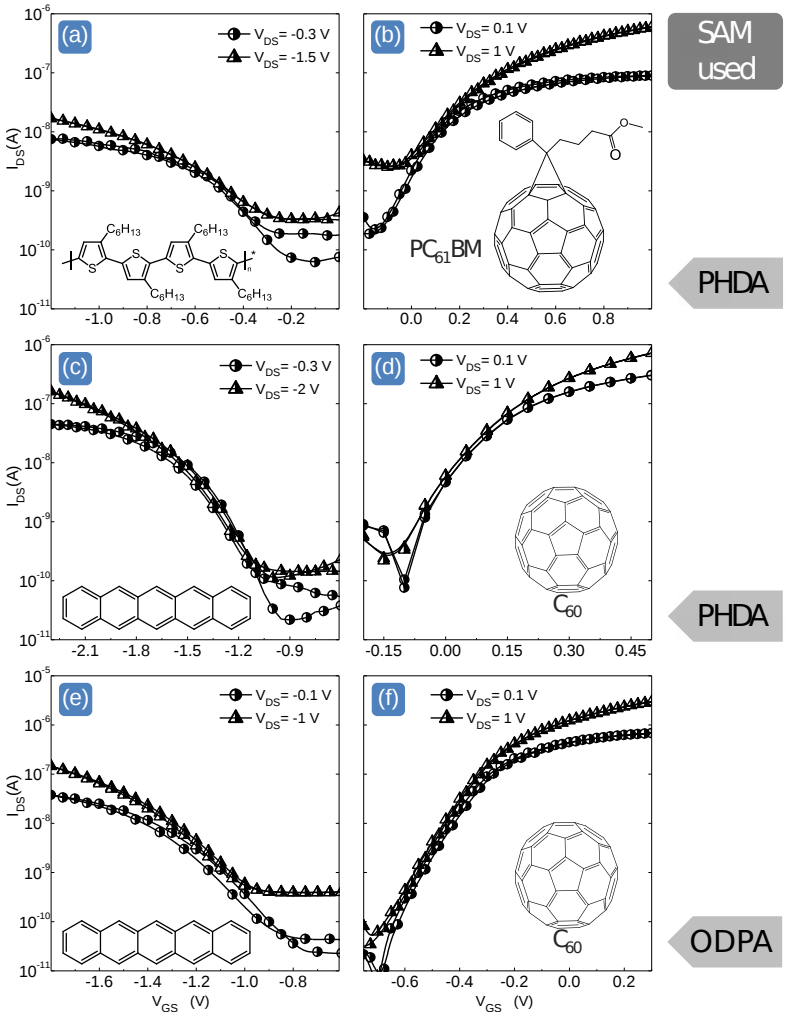

Figure 5.4: Transfer characteristics obtained from organic transistors based on different semiconductors and SAM nanodielectrics. P3HT and [60]PCBM layers were solution processed while pentacene and C_{60} have been deposited by vacuum sublimation.

Figure 5.4 a-b shows the transfer characteristics for solution-processed [60]PCBM and P3HT transistors based on PHDA SAM dielectrics. Figure 5.4 c-f displays the transfer characteristics for vacuum sublimed pentacene and C_{60} OFETs based on PHDA and ODPA SAM dielectrics. It should be noted that spin casting of [60]PCBM and low-viscosity P3HT solutions, used here, onto ODPA functionalised Al-AlOx electrodes was not possible due to the low surface energy of ODPA [180]. Gate electrodes functionalised with PHDA exhibited much higher surface energy allowing for processing of a wider range of semiconductor solutions [181]. The surface energy characteristics of ODPA and PHDA SAMs were reported in our earlier work [180, 181]. These ultrathin hybrid AlO_x-SAM dielectrics yield high geometrical capacitance (400-600 nF/cm^2) and low leakage current (10^{-9}-10^{-7} A/cm^2). Using these nanodielectrics,

OFETs with operating voltages below <|2| V can be obtained. This ultra-low operating voltage qualifies these transistors for battery-powered applications since this will reduce significantly the power dissipation when used in circuits. To be noted that no functional transistors could be obtained using gate electrodes based on the native AlO_x oxide alone. This is attributed to the large leakage current flowing between the gate terminal and the organic semiconducting channel [180]. The problem of high leakage current in these structures could in principle be partially circumvented by employing higher mobility semiconducting layers based on inorganic materials. This could result in a much higher channel current as compared to the leakage current of the Al-AlO_X structure. Testing such structures, however, was beyond the scope of this work.

The performances of all the SAM based OFETs fabricated in this work are summarized in Table 5.2. Low-voltage vacuum-sublimed C_{60} transistors based on BOUDPA SAM dielectric (employing Aluminium as source-drain electrodes) exhibit really high performances with a mobility up to 1.2 cm^2/Vs, a threshold voltage of 0 V and low subthreshold swing of 80 mV/dec. To our knowledge this is the highest electron mobility reported for low-voltage n-channel transistors based on SAM dielectric to date. Using a 100 nm thick Al_2O_3 dielectric passivated by a thin BCB layer, Zhang et al. demonstrated bottom-gate top-contact C_{60} transistors with an operating voltage of 5 V and reported a mobility of 2.3 cm^2/Vs for C_{60} as the semiconductor [257]. These devices presented an on/off current ratio of 10^6, a threshold voltage of 0.1 V and subthreshold swing of 100 mV. For high voltage transistors (> 60 V), the highest mobility for C_{60} semiconductor was reported to be 6 cm^2/Vs [12]. Good performances were also obtained for C_{60} FETs based on ODPA and PHDA SAM dielectrics with mobilities of 0.6 cm^2/Vs and 0.3 cm^2/Vs, repectively. For pentacene devices, good transfer and output characteristics were obtained. However the mobility values were in the range 0.01-0.03 cm^2/Vs, an order of magnitude lower to the one reported by Klauk et al. for ODPA-based transistors [48]. The threshold voltage was found to vary from -1.1 V to -1.5 V, which is quite substantial when considering an operating voltage of 2 V, and could suggest that SAM dielectric promote electron transport compared to hole transport. It has been found difficult to identify p-type solution processed semiconductors that show good film formation and field-effect behaviour.

If high performance transistors were fabricated by vacuum sublimation of the semiconductor, solution-processing of the semiconductor represent a potentially better technologic option for low-cost low-temperature manufacturing. In our study, both p-type and n-type transport were demonstrated employing diFTESADT small molecules or P3HT polymer for p-channel FETs and the fullerene derivatives PCBM or F17-DOPF for n-channel FETs [180, 181]. Mobility values as high as 0.06 cm^2/Vs for PCBM transistors based on BOUDPA SAM dielectric or 0.005 cm^2/Vs for diFTESADT transistors based on PHDA SAM dielectric were measured. Being able to demonstrate good charge transport in both solution-processed p-channel and n-channel field-effect transistors is crucial for successful implementation in complementary logic

circuits for low-cost organic electronics as we will see later in section (5.7). A summary of the performance of these low-voltage SAM transistors can be found in table 5.2.

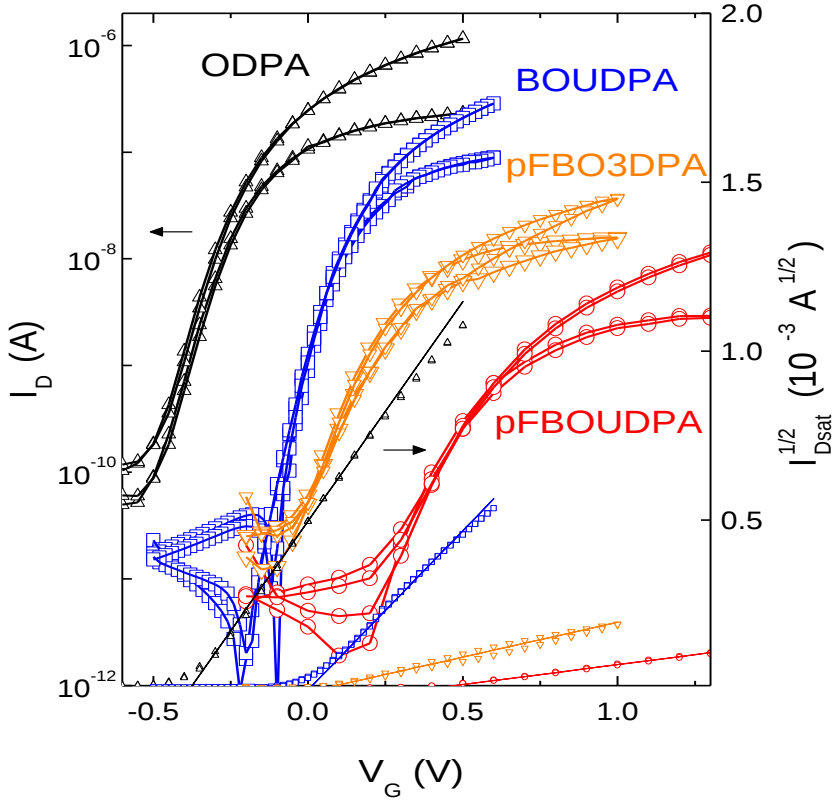

Figure 5.5: Transfer characteristics of low-voltage C_{60} transistors based on four different SAM dielectrics. The self-assembled monolayers compared in this study are octadecylphosphonic acid (ODPA), benzyloxyundecylphosphonic acid (BOUDPA), perfluorobenzyloxyundecylphosphonic acid (pFBOUDPA) and perfluorobenzyloxyoctooxyundecylphosphonic acid (pFBOOODPA).

Given the unfavorable surface wetting properties of the fluorinated SAMs, vacuum sublimed C_{60} as the semiconductor was chosen to fabricate bottom-gate, top-contacts OFETs using Al source and drain electrodes. Figure 5.5 show the transfer characteristics of C_{60} transistors based on fluorinated-end group SAM dielectrics. For comparison the operating characteristics of ODPA- and BOUDPA-SAM based devices are also shown. Transistors based on pFBOUDPA and pFBOOODPA exhibited a field-effect with a mobility of $1 \cdot 10^{-3}$ cm^2/Vs and $2 \cdot 10^{-3}$ cm^2/Vs, respectively. This relatively low mobility value (compared to 1.2 cm^2/Vs or 0.6 cm^2/Vs value obtained with C_{60} OFETs based on BOUDPA and ODPA SAM dielectrics, repectively) could be attributed to the electron withdrawing property of the perfluorinated end group that prevents efficient charge transport at the dielectric-semiconductor interface. Similarly Kraft et al. observed a mobility decrease from 1 cm^2/Vs to 0.2 cm^2/Vs in pentacene p-channel OFETs and from 0.3 cm^2/Vs to 0.006 cm^2/Vs in $F_{16}CuPc$ n-

channel OFETs when functionalising 1H,1H,2H,2H-perfluorododecylphosphonic acid (pFDDPA) SAM instead of the equivalent hydrogenated SAM (DDPA) on alumina [183]. For n-type C_{60} semiconductor, this effect was also reported by Kobayashi et al. when substituting octyltrichlorosilane SAM ($\mu \sim 0.07$ cm^2/Vs) with perfluorodecyltrichlorosilane SAM ($\mu \sim 0.005$ cm^2/Vs) on SiO_2 gate dielectric [182]. In their study, Kraft et al. also noticed a significant positive shift in the threshold voltage when replacing the alkyl chain by the fluoroalkyl SAM [183]. This was illustrated by a difference in threshold voltage of 1.2 V for pentacene TFTs and 1 V for F_{16}CuPc TFTs when replacing the DDPA SAM with a pFDDPA SAM. The strong withdrawing character of the fluorinated alkyl chain implies that an additional potential is required to accumulate electrons (deplete hole) in n-channel (p-channel) FETs. This observation correlates well with our study. When comparing pFBOUDPA and pFBOOODPA to ODPA, the threshold voltage in C_{60} transistors is changed by 0.8 V and 0.4 V, respectively, toward more positive voltages. When substituing BOUDPA by its perfluorinated equivalent pFBOUDPA, the threshold voltage is 0.4 V more positive. The difference in the threshold voltages (obtained in both studies) possibly suggests that perfluorinated alkyk chain has a stronger electron withdrawing effect than perfluorinated phenyl end groups.

Controlling the threshold voltage in TFTs is of paramount importance to ensure a proper switching behaviour of inverters at a first stage and thus the immunity of large-scale integrated circuits. The threshold voltage can be tuned in these low-voltage OFETs by choosing the appropriate self-assembled monolayer. For instance, employing C_{60} as a semiconductor in our TFTs, the threshold voltage of these low-voltage (< 2 V) transistors could be tuned from -0.5 V with ODPA SAM dielectric, to 0 V with PHDA, up to 0.4 V using pFBOUDPA. Zschieschang et al. were able to tune continuously the threshold voltage (40 mV/%) of low-voltage p-type and n-type OFETs over a wide range (from -0.3 V to 1.1 V) by increasing the fluorine concentration in the mixed self-assembled monolayer gate dielectric (composed of alkyl and fluoroalkyl phosphonic acid) [184]. This change in threshold voltage was explained by the reduction of the electron density in the transistor channel due to the electron-withdrawing property of the fluoroalkyl SAMs. Chemical tayloring of the SAMs and concentration ratio tuning are two powerful and simple methods to control the threshold voltage in low-power organic transistors.

5.3 Ambipolar transporting SAM-based organic transistors

We have demonstrated that low-voltage, low-cost organic transistors were made possible by solution-processing of the semiconductor and the use of self-assembled monolayer dielectrics. Fabrication of both p-channel and n-channel devices using this technic demonstrated the possibility to build complementary logic circuits. However pat-

Table 5.2: Summary of the device parameters obtained from the low-voltage SAM-based OFETs. Charge carrier mobilities were extracted using a channel geometrical capacitance of 550 nF/cm^2 for AlOx\PHDA, 450 nF/cm^2 for the AlOx\ODPA dielectric, 600 nF/cm^2 for BOUDPA/AlOx dielectric, 800 nF/cm^2 for pFBOUDPA dielectric and 600 nF/cm^2 for pFBOOODPA/AlOx dielectric. W and L are the channel width and length, respectively, of the specific transistors used in this study. The threshold voltage (V_T), the switch-on voltage (V_{ON}) and the subthreshold slope (SS) for each device were calculated from the transfer characteristics using standard procedures explained in section 2.4.2.2. Litterature values obtained for low-voltage organic transistors are also reported for comparison.

SC	SAM	W/L (μm/μm)	μ_{sat} (cm^2/Vs)	V_T (V_{ON}) (V)	$I_{ON/OFF}$	SS (mV/dec)	Reference
diFTESADT	PHDA	2000/20	0.005	-0.5			[181]
P3HT	PHDA	1500/40	0.002	-0.35(-0.55)	$2 \cdot 10^2$	270?	this work
PCBM	PHDA	2000/20	0.036	-0.49	10^3	250	this work
PCBM	BOUDPA	1000/20	0.061	0.15 (0.1)	10^4	100	this work
F_{17}DOPF	ODPA	1000/60	0.04	0.35	10^4	110	[180]
PBCF3	ODPA		0.01	0.13	10^3	200	[180]
Pentacene	ODPA	1000/20	0.035	-1.19 (-1.1)	10^3	180	this work
	PHDA	1500/30	0.015	-1.43 (-1.2)	10^3	150	this work
	BOUDPA	1000/20	0.011	-1.33 (-1.0)	$5 \cdot 10^3$	155	this work
C_{60}	ODPA	1000/70	0.62	-0.36 (-0.4)	10^4	100	this work
	PHDA	1500/40	0.25	0.0 (-0.1)	$5 \cdot 10^2$	130	this work
	BOUDPA	500/200	1.2	0.0 (0.0)	$2 \cdot 10^4$	85	this work
	pFBOUDPA	500/10	$7 \cdot 10^{-4}$	0.39 (0.7)	10^3	130	this work
	pFBOOODPA	1500/20	$2 \cdot 10^{-3}$	0.04 (0.2)	10^3	120	this work
Pentacene	ODPA	100/30	0.75	-1.1	10^6-10^7	100	[48]
	ODPA:PDFODPA	100/30	0.68	-0.7	10^7	120	[184]
	PDF-ODPA	100/30	0.25	0.5	10^5	250	[184]
	DDPA	100/30	1	-1.2	10^6		[183]
	pFDDPA	100/30	0.2	-0.05	10^5		[183]
F_{16}CuPc	ODPA	1000/30	0.028	-0.3	10^5	160	[48, 184]
	ODPA:PDFODPA	1000/30	0.027	0.6	10^5	180	[184]
	PDF-ODPA	1000/30	0.011	1.1	10^5	220	[184]
	DDPA	100/30	0.3	0.6	10^4		[183]
	pFDDPA	100/30	0.006	1.55	10^4		[183]
C_{10}DNTT	ODPA	100/30	4.3	-0.4	10^8	68	[258]
Pentacene	π-σ-PA1	9000/90	0.18	-1.3	10^5	85	[178]
Pentacene	π-σ-PA2	9000/90	0.14	-1.4	10^5	85	[178]
Pentacene	ODPA	9000/90	0.30	-1.5	10^5	110	[178]
α-6T	TSTDA/Si	20/0.2	$3.6 \cdot 10^{-4}$	-1.3	10^4	0.35	[177]
Pentacene	PhO-OTS/Si	170/130	1	-1.3	10^6	100	[47]
C_{60}	Al_2O_3/BCB	2000/25	2.3	0.1	$4 \cdot 10^6$	300	[257]

terning of the two different semiconductors is an issue that needs to be addressed. CMOS-like complementary logic based on ambipolar OFETs offer an alternative approach by simplifying the fabrication, since a single semiconductor layer needs to be deposited [129, 113]. For this purpose, intense research efforts have focused into developping solution-processed ambipolar materials and transistors.

In this section, we report the ambipolar charge transport of MS23-DPP and MS25-DPP polymers. These two ambipolar polymers belong to the group of low-bandgap donor-acceptor (D-A) copolymers based on diketopyrrolopyrrole (DPP). The polymers were synthesized in the chemistry department at Imperial College. Their molecular structures are presented in figure 5.6 a-b.

Those two polymers were tested in N_2 atmosphere using a bottom-gate, top-contact transistor architecture employing gold as source-drain electrodes. The polymer was disolved in chlorobenzene solution at 10 mg/mL and spin-cast at 2000 rpm for 60 sec on BOUDPA SAM surface. The samples were tested, then annealed, and retested at various temperatures from $100°C$ to $250°C$ with a step of $50°C$ to observe if any microstructural phase transitions occur in the polymer film.

As prepared transistor based on MS23-DPP polymer showed a hole and electron

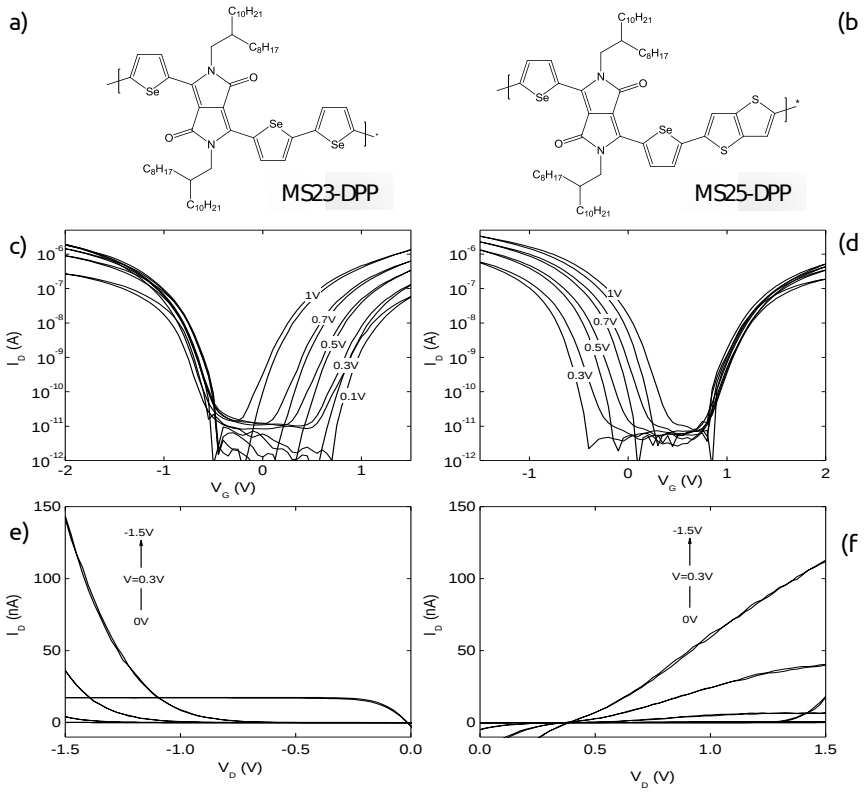

Figure 5.6: Transfer and output characteristics of low-voltage MS23-DPP (a,c,e) and MS25-DPP (b,d,f) transistors based on BOUDPA SAM dielectric after annealing at $200°C$. The channel width and length of the device tested here are 1500 μm and 50 μm, respectively.

Table 5.3: Summary of the device parameters obtained from the low-voltage ambipolar OFETs based on BOUDPA SAM dielectric. W and L are the channel width and length, respectively, of the specific transistors used in this study.

SC	Annealing conditions	W/L (mm/μm)	μ_h (cm^2/Vs)	μ_e	$V_{T,h}$ (V)	$V_{T,e}$ (V)	$I_{ON/OFF}$
MS23-DPP	as-spun	1.5/50	0.001	0.006	-0.99	0.81	
	200°C		0.18	0.07	-0.88	1.15	10^5
MS25-DPP	200°C	1/30	0.026	0.002	-1.48	0.54	10^2
	250°C		0.021	0.003	-1.56	0.60	

mobility of only 0.001 cm^2/Vs and 0.006 cm^2/Vs, respectively. For MS23-DPP transistors, the hole mobility gradually increased with increasing annealing temperature, reaching up to 0.18 cm^2/Vs when annealed at 200°C, while the electron mobility showed a significant improvement to 0.07 cm^2/Vs at 200°C . As shown in Figure 5.6, this low-voltage MS23-DPP transistors based on BOUDPA SAM dielectric (upon annealing at 200°C) show good ambipolar behaviour with a current On/Off ratio of 10^5. The relatively low mobility value obtained for electrons compared to holes could be explained by the non-ohmic contacts as observed in the output curves. Indeed the large barrier between the work function of gold and the LUMO level (~ 4 eV) can prevent efficient injection of electrons in the polymer film and thus increase the contact resistance.

However, almost no filed effect behaviour was observable for the as-spun MS25-DPP semiconductor. For this reason, the sample was annealed at 200°C and 250°C for 30 min. Ambipolar charge-transport characteristics was then observed exhibiting a maximun hole mobility of 0.026 cm^2/Vs (at 200°C) and a maximum electron mobility of 0.0028 cm^2/Vs (at 250°C). Severe non-ohmic contacts were observed for both carriers.

Previous studies, that were carried out in our group (work performed by John Labram), investigated the charge transport properties of these polymers in high-voltage bottom-gate, top-contact transistors using OTS functionalized SiO_2 as the dielectric. The mobility values obtained for MS23-DPP in our SAM-based OTFTs represents a really good results as compared to the 0.12 cm^2/Vs hole mobility and 0.01 cm^2/Vs extracted in high-voltage transistors. However the values extracted for the MS25-DPP polymer are found to be relatively low, since hole and electron mobility of 1.13 cm^2/Vs and 0.15 cm^2/Vs were reported for transistors based on SiO_2\OTS dielectric. If charge injection is still an issue, like often in ambipolar transistors, this preliminary study demonstrates ambipolar charge transport in transistors with an operating voltage of only 2 V. To the best of our knowledge, this is the first report of an ambipolar polymer OTFT.

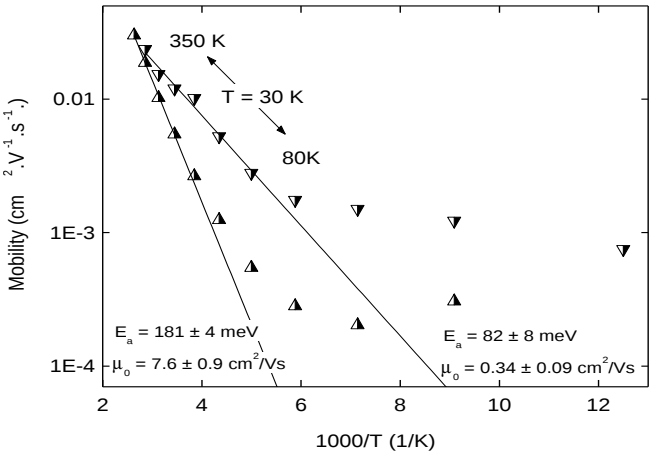

Figure 5.7: Electron mobility as a function of temperature for [60]PCBM transistors based on PHDA SAM dielectric. The temperature ranges from 80 K to 350 K.

5.4 Temperature dependence I-V measurements

In order to better understand charge transport in organic transistors, the temperature dependance of the electron mobility was investigated for [60]PCBM transistors based on PHDA SAM dielectrics. Because of device degradation in air, the substrate was encapsulated by spin-coating a layer of CYTOP (9%) polymer and then transferred to the cryogenic vacuum probe station (10^{-6} mBar). In vacuum, at room temperature, the electron mobility is 0.01 cm^2/Vs, the threshold voltage of ~0 V and the current on/off ratio on the order of $5 \cdot 10^3$. Electrical measurements were performed on a range of temperatures from 80 K to 350 K with a step of 30 K. As shown in figure 5.7, the mobility increases with increasing temperature. This indicates clearly that charge transport in PCBM film is thermally activated. The data were fitted in both regimes using the arrhenius law : $\mu_{FET} = \mu_0 exp(-E_a/kT)$. When decreasing the temperature from 350 K to 80 K, the activation energy was found to be 82±8 meV and the infinitely high temperature mobility was 0.34±0.09 cm^2/Vs, while for the increasing temperature regime they were of 181±4 meV and 7.6±0.9 cm^2/Vs, respectively. Variations of the threshold voltage were also observed with temperatures. In particular, the threshold voltage increases by 0.15 V when the temperature decreases from 290 K to 80 K and decreases by 0.1 V from 80 K to 350 K. These trends are in agreement with the presence of thermally activated transport sites.

5.5 Electrical stability of SAM based organic transistors

The electrical stability of low-voltage organic transistors based on phosphonic acid self-assembled monolayer (SAM) dielectrics was investigated using four different semiconductors. The threshold voltage shift in these devices show a stretched-exponential

time dependence under continuous gate bias with a relaxation time in the range of 10^3-10^5 s, at room temperature. Differences in the bias instability of transistors based on different self-assembled monolayers and organic semiconductors suggest that charge trapping into localized states in the semiconductor is not the only mechanism responsible for the observed instability. By applying 1-5 s long programming voltage pulses of 2-3 V in amplitude, a large reversible threshold voltage shift can be produced. The retention time of the programmed state was measured to be on the order of 30 hours. The combination of low voltage operation and relatively long retention times make these devices interesting for ultra-low power memory applications.

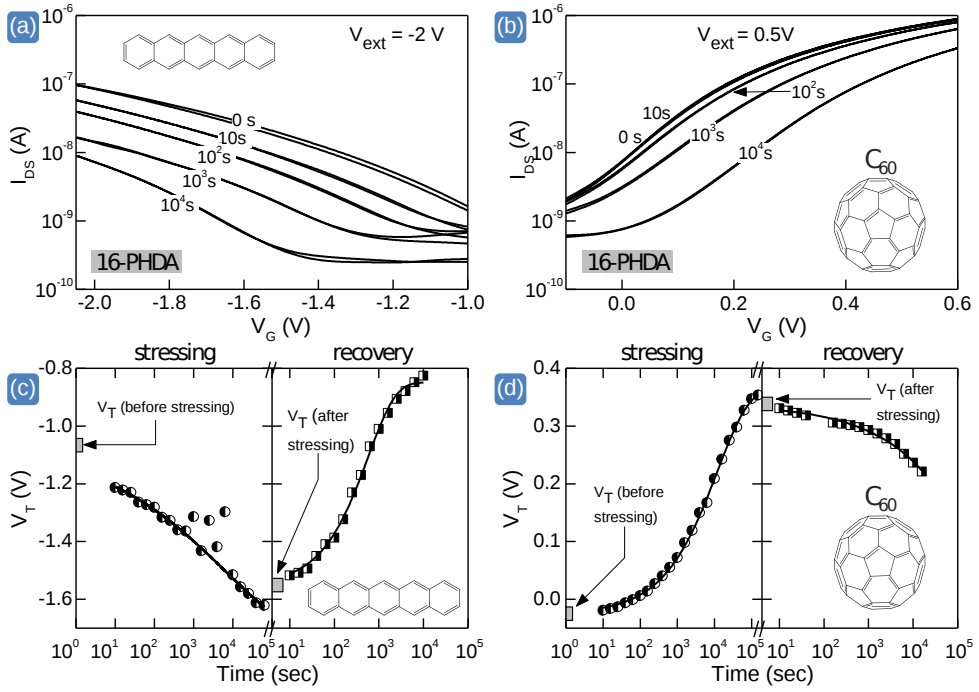

Figure 5.8: (a, b) Transfer characteristics for pentacene and C_{60} TFTs under gate bias stress and (c, d) threshold voltage shift as a function of time over a period of time of 100 000 s for low-voltage pentacene (a-c) and C_{60} (b-d) transistors based on PHDA SAM dielectrics. The gate voltage was held at -2 V for the pentacene device and 0.5 V for the C_{60} device, while the drain and the source were grounded. Figures c and d depict both the stress and recovery phases. The measured data (symbols) are fitted with the stretched exponential function (solid lines).

Bias stress and relaxation measurements were performed as a function of time for different gate voltages on as-prepared SAM OTFTs. The transistors were continuously stressed at a fixed gate bias (V_{ext}) while the drain and the source were grounded. As a criteria of comparison between the different devices, an applied gate bias was chosen corresponding to $V_{ext} \sim V_T + 1$ (n-type) or $V_{ext} \sim V_T - 1$ (p-type). The bias stress was briefly interrupted (4 to 6 s) to allow fast transistor measurements to be performed. Transfer characteristics were obtained at different periods of stressing time on a logarithmic scale (10 to 10^5 s). The duration of each gate sweep was kept

constant (5 s). The threshold voltage (V_T) was extracted as the intercept of the linear fit to the square-root of the drain current, measured in saturation, with the gate voltage (V_G) axis. After bias stressing, the recovery phase was monitored (i.e. by periodically measuring the transfer characteristic of the transistor in saturation and extracting the V_T following the procedure outlined earlier) by grounding the gate terminal.

Figure 5.8 displays the shifts in the transfer characteristics for low-voltage pentacene and C_{60} transistors, respectively, based on PHDA SAM dielectrics after bias stressing for 10^4 s. The threshold voltages (V_T) were extracted directly from these curves, using the procedure described earlier, and plotted as a function of time on a logarithmic scale in Figure 5.8 c-d. In Figures 5.8 a-b, the 0 s curves denote the non bias stressed device characteristics (i.e. the first ever measurement obtained from these specific transistor(s)). For n-type transistors, the V_T shifts toward more positive values with the application of a positive gate voltage and for p-type transistors towards more negative voltages with the application of negative gate voltage. During the recovery process, the transfer curves shift back to their initial positions.

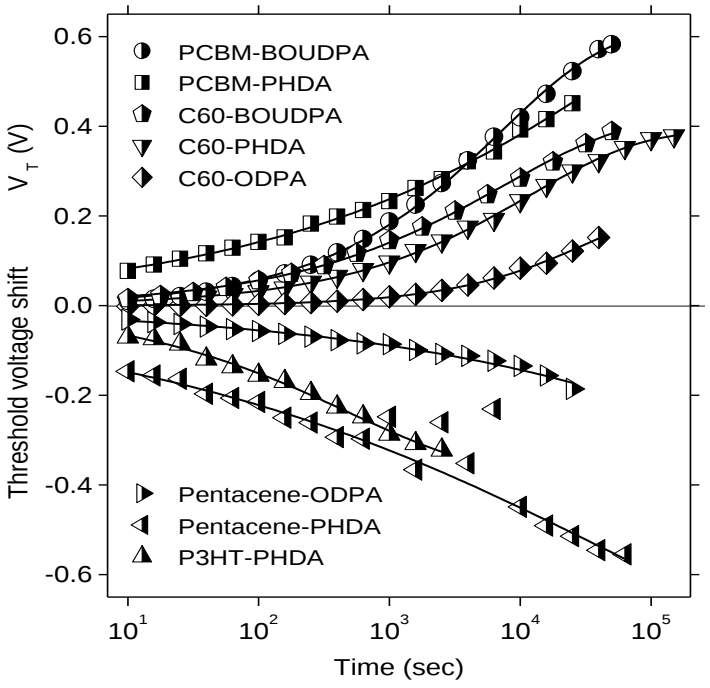

Figure 5.9: Threshold voltage shift (ΔV_T) of organic transistors based on BOUDPA, PHDA and ODPA SAM dielectrics measured under electrical bias stress as a function of stressing time. Semiconductors tested include [60]PCBM, P3HT, C_{60} and pentacene.

Similar threshold voltage shifts are observed for transistors based on different SAMs and semiconductors. For example, transistors based on PHDA SAMs exhibit bias instabilities that depend on the specific semiconductor used. Specifically, PHDA OTFTs subjected to 2.8 hours (10^4 s) bias stress exhibit threshold voltage shifts of

0.39 V for [60]PCBM, -0.45 V for pentacene and 0.23 V for C_{60}. The different stressing characteristics observed between these PHDA SAM OTFTs based on different semiconductors suggest that the bias-induced instabilities originate, at least in part, from trapping of charge carriers into localized states within the semiconductor. In order to assess the influence of the SAM on the bias stress effects in these devices, different monolayer nanodielectrics, namely ODPA, PHDA and BOUDPA, were tested in bottom-gate, top-contact transistor structures. For the three SAM molecules studied, significant differences between the V_T shifts were observed. Figure 5.9 displays representative characteristics of the evolution of V_T as a function of bias stress time for the different SAM based transistors studied. We emphasize that these characteristics are representative for each type of SAM-semiconductor system studied and have been reproduced for several different batches (>5) prepared during identical experimental procedures. From figure 5.9 it appears that the bias stress effect is less pronounced in ODPA-based OTFTs as compared to devices based on PHDA (for both pentacene and C_{60} based transistors). This difference is pronounced for all batches (>5 for each material system) studied. This can be tentatively attributed to the difference in the chemistry of the terminal group or its effect on the semiconductor microstructure at the interface with the SAM dielectric. However, studying the exact origin of this effect and/or the nanostructure of the SAM-organic interface was found to be very challenging due to the complexity of the system and the non ideal properties of the SAM-semiconductor interface (i.e. a very rough interfacial region making microstructural analysis extremely difficult). In order to obtain further insights into the origin of the bias stress effects in these OTFTs we have fitted the stress time dependence of the V_T shift using a stretched exponential function given as:

$$\Delta V_T(t) = \Delta V_T(\infty)\left[1 - \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right] \tag{5.1}$$

where $\Delta V_T(\infty)$ is the threshold voltage shift between the equilibrium state and the initial state, τ is the time constant and β is the stretching parameter ($0 < \beta \leq 1$). The quality of each fit was assessed by its coefficient of determination (R^2), where a R^2 value closer to 1 represents a better fit. The extracted bias stress parameters for each transistor studied are summarized in Table 5.4. The relaxation time (τ) is found to be in the order of 10^3-10^5 s, extracted from several devices of each type, at room temperature. This is relatively small when compared to the value of 10^7 sec measured for pentacene transistors [240] and $2{\cdot}10^4$ s for PTAA transistors [238], meaning that the relaxation process is relatively fast. The stretching parameters of β between 0.20 - 0.26 extracted for pentacene devices are slightly lower than the values obtained by Zschieschang et al. of $\beta = 0.29$-0.42 [240]. Noteworthy are the high values for β (between 0.47 for BOUDPA, 0.509 for PHDA and 0.69 for ODPA) obtained for C_{60} based transistors, indicating a rather narrow distribution of time constants. The latter also reflects the improved quality of the semiconducting film i.e. the structural and hence electronic properties of C_{60}. Finally, the coefficient of determination (R^2)

for all fits is high with the lowest one being the pentacene-PHDA system.

Table 5.4: Summary of bias stress parameters obtained for the low-voltage OTFTs using equation 5.1. Bias stress parameters include the threshold voltage shift $\Delta V_T(\infty)$ between the equilibrium state and the initial state, τ the time constant and β the stretching parameter (0). The quality of each fit using Eq. 5.1 was assessed by its coefficient of determination (R^2), where a value closer to 1 represents a better fit. The threshold voltage shift at t = 10 000 s is also quoted as a marker. W and L are the channel width and length, respectively, of the specific transistors used in this study.

Devices	W/L	V_{ext}	$\Delta V(10^4$s)	ΔV_T	β	τ	R^2
	(mm/μm)	(V)	(V)	(V)		(s)	
PCBM-BOUDPA	1.5/30	1	0.42	0.61±0.01	0.54±0.01	$7 \cdot 10^3$	0.9991
PCBM-PHDA	1/50	1	0.39	0.98±0.20	0.25±0.01	$2 \cdot 10^5$	0.998
C60-BOUDPA	0.5/30	1	0.35	0.401±0.001	0.465±0.002	$2 \cdot 10^3$	0.9999
C60-PHDA	1.5/40	0.5	0.23	0.389±0.004	0.507±0.008	10^4	0.999
C60-ODPA	2/30	0.5	0.08	0.22±0.01	0.69±0.04	$3 \cdot 10^4$	0.997
pentacene-ODPA	2/30	-2	-0.14	-0.20±0.02	0.26±0.02	$7 \cdot 10^3$	0.997
pentacene-PHDA	1.5/20	-2	-0.45	-0.86±0.21	0.20±0.02	$5 \cdot 10^4$	0.991
P3HT-PHDA	1/20	-1	...	-0.38±0.02	0.42±0.03	$5 \cdot 10^2$	0.996

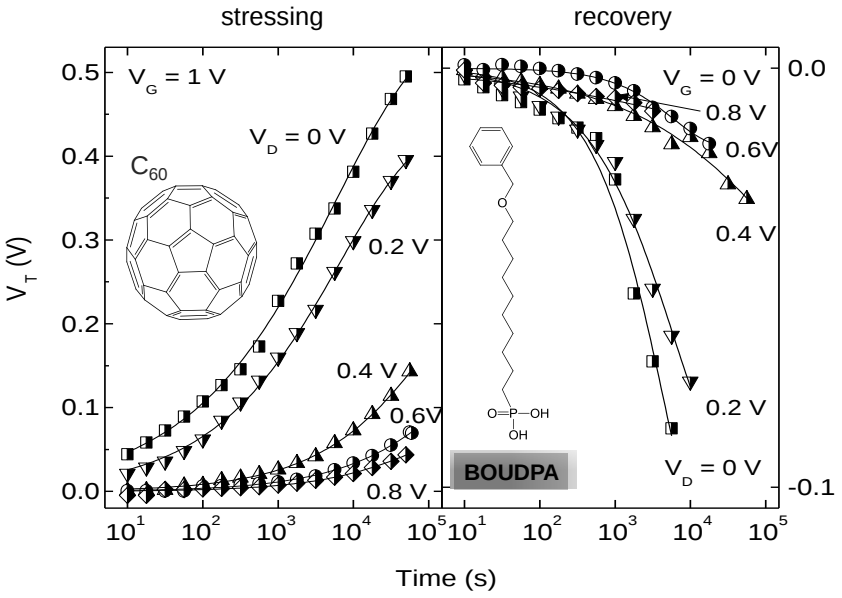

Figure 5.10: Threshold voltage shift (ΔV_T) of low-voltage C_{60} OTFTs based on BOUDPA SAM dielectric as a function of time. A different potential (from 0 V to 0.8 V with a voltage step of 0.2 V) was applied to the drain electrode during electrical bias stress. Both stressing and recovery regimes are presented.

For C_{60} devices based on BOUDPA SAM dielectric, threshold voltage shifts were measured by applying different drain-source voltages 0 V, 0.2 V, 0.4 V 0.6 V and 0.8 V on different devices while keeping a constant gate voltage of 1 V. As it can be seen on figure 5.10, applying a drain-source voltage during the gate bias stress reduces the threshold voltage shift. At 10 000 s, the threshold voltage shift decreases from 0.38 V

Table 5.5: Summary of bias stress parameters obtained for low-voltage C_{60} OTFTs based on BOUDPA SAM dielectric under different bias stress condictions. The drain voltage was varied from 0 V to 0.8 V.

V_{ext} (V)	W (mm)	L (μm)	$\Delta V(10^4$s) (V)	ΔV_T (V)	β	τ (s)	R^2
0	500	30	0.38	0.57±0.02	0.36±0.01	$6{\cdot}10^3$	0.998
			...	-0.12±0.04	0.78±0.13	$4{\cdot}10^3$	0.98
0.2	500	50	0.30	0.43±0.01	0.43±0.01	$7{\cdot}10^3$	0.9991
			-0.08	-0.10±0.02	0.65±0.06	$6{\cdot}10^3$	0.993
0.4	500	20	0.07	0.29±0.05	0.49±0.02	$1{\cdot}10^5$	0.998
			-0.02	-0.07±0.04	0.37±0.05	$2{\cdot}10^5$	0.98
0.6	1000	30	0.03	0.2±0.1	0.49±0.03	$3{\cdot}10^5$	0.997
			-0.01	-0.019±0.001	0.88±0.08	$6{\cdot}10^3$	0.990
0.8	500	10	0.02	0.08±0.06	0.54±0.09	9·104	0.97
			-0.02	...	...	...	...

when the bias applied to the drain is 0 V, to 0.07 V and 0.03 V when the drain voltage is 0.4 V and 0.6 V, respectively. When fitting the results obtained with a stretched exponential function, we observe that with increasing drain voltage the stretching parameter increases from 0.36 for V_D = 0 V to 0.54 at V_D = 0.8 V. For each drain voltage, the fitting parameters of the bias stress measurements are summarized in table 5.5. These results obtained for C_{60} are in fair agreement with those obtained by Zschieschang et al. with p-channel pentacene transistors. In their case, they had also observed a reduction of the time constant when V_D increases and concluded that the lateral field between the source and drain creates a detrapping pathway for carriers. As described by the Poole-Frenkel mechanism, the charge carriers trapped into localized states are released more easily and faster into the channel due to the tilting of the band edge. For C_{60} transistors, the time constants were found to increase with increasing drain bias. This most likely suggests that the drain voltage couteracts locally the gate bias.

In their study, Zschieschang et al. proposed that the bias stress effect in a low-voltage ODPA based pentacene transistor results mainly from charge trapping in the semiconductor and at the SAM/semiconductor interface [240]. From the results presented herein, it can also be concluded that charge trapping into localized states in the semiconductor and/or at the active interface is most likely responsible for the observed bias stress effect. The same measurements, however, suggest that the nature of a SAM's end group also plays an important role and can lead to enhanced bias-stress effect, as evident from the case of PHDA OTFTs based on pentacene and C_{60}. The exact mechanism responsible for this observation is not known and is the subject of ongoing investigation. Recently, Sharma et al. suggested that the bias stress effect occurring in p-type organic transistors using SiO_2 as the gate dielectric originates from the formation of protons at the surface of the gate dielectric by electrolysis in presence of water and holes, followed by the diffusion of these protons into

the dielectric when applying an electric field [242]. Based on a similar mechanism, we propose that the bias stress effect observed in our low-voltage transistors could perhaps result from ionic dissociation of the phosphonic acid under gate bias. A similar deprotonation process has been observed in the copolymer of vinyl phosphonic acid and acrylic acid P(VPA-AA) [238]. In the present case, however, bias stressing is also observed in OTFTs based on n-type semiconductors. Under these biasing conditions the mobile proton would move toward the semiconductor. If the protons do penetrate the semiconductor then relaxation is expected to be slower since they have to travel a longer distance. This could explain why the recovery process is slower and not always complete. Another possible mechanism is the formation of excess hydroxyl ions HO^- in the presence of water and electrons, followed by the ion diffusion into the dielectric, leading to a bias stress induced V_T shift. Each of these mechanisms could in principle be studied independently by developing appropriate device architectures utilising suitable materials systems (e.g. different types of semiconductor, different semiconductor film thicknesses, etc) and combining these with accurate control of the ambient atmosphere composition. In summary, the present results indicate that the nature/chemistry of the specific SAM dielectric employed appears to have an influence on the bias stress characteristics of SAM transistors. However, in order to distinguish between effects attributed to ionic dissociation of the phosphonic acid and/or to a change in the morphology of the semiconductor at the interface with the SAM, further work is needed.

5.6 Low-power memory devices based on SAM OFETs

The potential of using these low-voltage, bias "stress-able" SAM based OFETs as non-volatile memory elements has also been investigated. Low-voltage OFETs based on solution processed electron transporting molecule [60]PCBM as the semiconductor and PHDA as the SAM dielectric were used as model devices since they were found to exhibit strong bias stressing characteristics (see Figure 5.9). The different memory states (i.e. ON and OFF) were then programmed by controlling the V_T shift through the application of an appropriate (i.e. positive or negative) voltage at the gate terminal (V_{ext}). The channel current at each memory state was then monitored at a fixed reading drain voltage ($V_{DS} = 0.1\ V$) and gate voltage ($V_{read} = 0.18\ V$). These voltage levels are intentionally chosen to be low so they do not induce any significant bias stress effect to the device during the reading cycle.

Figure 5.11 (a) displays a typical set of transfer characteristics for a low-voltage PHDA based [60]PCBM transistor before (solid line) and after the programming cycle (circles) has been performed (i.e. $V_{ext} = 2.5\ V$). Upon application of a "writing" cycle of $V_{ext} = 2.5\,V$ for 5 s, the threshold voltage of the transistor shifts towards a more positive gate voltage value by approximately 0.34 V (i.e. by a third of the initial operating voltage range). Under these circumstances the channel current, measured at $V_{DS} = 0.1\,V$ and $V_{ext} = 0.18\,V$, is found to decrease by more than two orders of

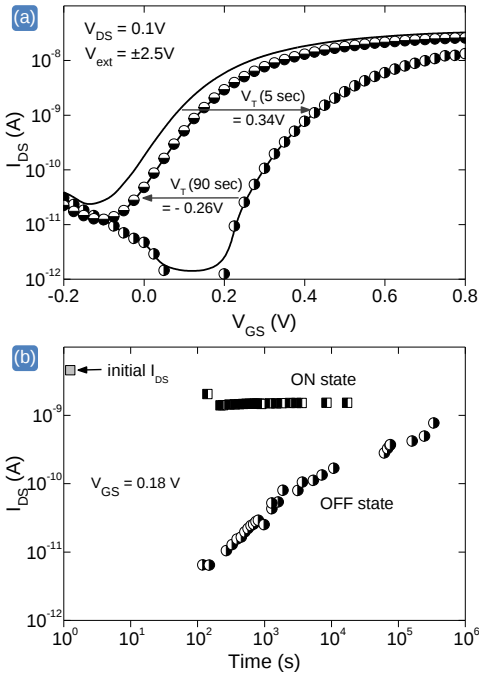

Figure 5.11: (a) Transfer curves for a low-voltage [60]PCBM OFET based on PHDA SAM dielectric before bias stressing (solid line), after bias stressing at $V_{ext} = 2.5\,V$ for 5 seconds (circles) and after bias stressing at $V_{ext} = -2.5V$ for 90 seconds (squares). (b) Retention time of the ON and OFF states measured from the same transistor.

magnitude. This low channel current defines the OFF state of the memory device while the channel current level before the writing cycle (i.e. the initial I_{DS} in Figure 5.11 (a)) defines the ON state. Accelerated recovery from the OFF state back to its initial ON state (i.e. "erasing" cycle) is achieved through the application of negative $V_{ext} = -2.5\,V$ at $V_{DS} = 0\,V$. From Figure 5.11 (a) it is evident that the transfer characteristic (squares) of the device does indeed return back to almost its initial value. Finally, it was found that the required erasing cycle is typically much longer $(10 - 100\,s)$ than the writing cycle $(0.1 - 5\,s)$. In order to assess the memory characteristics of these low-voltage SAM OFETs, the retention times of the OFF and ON states were measured. A typical set of retention characteristics obtained from a [60]PCBM-based SAM OFET are shown in Figure 5.11 (b). For the purpose of these measurements the channel current was measured at a low V_{GS} (0.18 V). From these measurements it can be seen that contrary to the rather stable ON state (remains unchanged for several days), the OFF state is found to fully recover (i.e. return to the initial ON state) within 30 hours (at room temperature). Similar retention times were measured in OFETs based on other SAMs, such as BOUDPA. Despite the relatively short data retention time of these devices, the present work demonstrates that the pronounced V_T shift in SAM OFETs could potentially be explored for low-power memory applications. Finally, one of the most intriguing aspects of the technology

that could potentially be explored in the future is the ability to tune the degree of the bias stress effect through molecular engineering of the SAM dielectric/semiconductor interface [183]. The latter characteristic qualifies this technology as a candidate for the development of scalable, low-power organic memories.

5.7 Low-voltage unipolar and complementary NOT gate

By combining low-voltage organic transistors based on SAM dielectrics, four different low-voltage complementary inverters were tested: a unipolar inverter based on vacuum-sublimed C_{60} transistors, a complementary inverter based on vacuum-sublimed p-channel pentacene and n-channel C_{60} transistors, a complementary inverter combining solution-processed p-channel P3HT and n-channel PCBM transistors and finally complementary-like inverter using two MS23-DPP ambipolar transistors. Their performance are presented and discussed in this study.

First two low-voltage C_{60} transistors based on ODPA SAM dielectric were combined in unipolar "$V_G = 0$" logic. The DC characteristic of this C_{60} inverter, shown on figure 5.12, exhibit excellent switching behavior with a gain of 30 (at $V_{DD} = 1.4$ V). This can be related to the sharp subthreshold slope of both devices (~ 100 mV/dec). Unfortunately the inverting voltage was found to be negative (-0.37 V). This can be attributed to the enhancement mode operation of C_{60} transistors (V_T ~ -0.4 V).

Using p-channel pentacene and n-channel C_{60} transistors, a low-voltage organic complementary inverter was tested. Both transistors were based on ODPA SAM dielectrics. Given the difference in carriers mobilities: 0.03 cm^2/Vs for p-channel device and 0.6 cm^2/Vs for n-channel transistor, the ratio $\frac{\beta_p}{\beta_n} = 0.35$ (where $\beta = \mu C_i W/L$) was compensated by choosing suitable channel dimensions. The channel width (W) and length (L) ratios were 2000/20 μm and 1000/70 μm for p-channel and n-channel FETs, respectively. Figure 5.12 (b) displays the transfer characteristic and gain of this inverter for supply voltage ranging from 0.6 V to 1.2 V. The maximum gain voltage was found to be 27 (at a supply voltage of 1.2 V). Similarly to the previous unipolar C_{60} inverter, this inverter has the drawback of operating partly in the second quadrant. An inverting voltage of -0.25 V is obtained for a supply voltage of 1.2 V. For practical applications in circuits, both the supplied voltage (V_{DD}) and the input node (V_{IN}) should be biased positively (operation in the first quadrant) or negatively (operation in the third quadrant). Klauk et al. reported a complementary inverter with a gain of 100, a switching voltage of 0.5 V and noise margin of 40% for a supply voltage V_{DD}= 2 V, comprising vacuum-sublimed p-channel pentacene and n-channel F_{16}CuPc TFTs based on ODPA SAM dielectrics. By chemical tayloring of the SAM dielectric surface with a mixture of alkyl- and perfluoroalkyl-phosphonic acids (ODPA:PDF-ODPA), they were able to tune the threshold voltage of the transistors so that the inverter characteristics could be optimized up to a gain of 230, a sharp

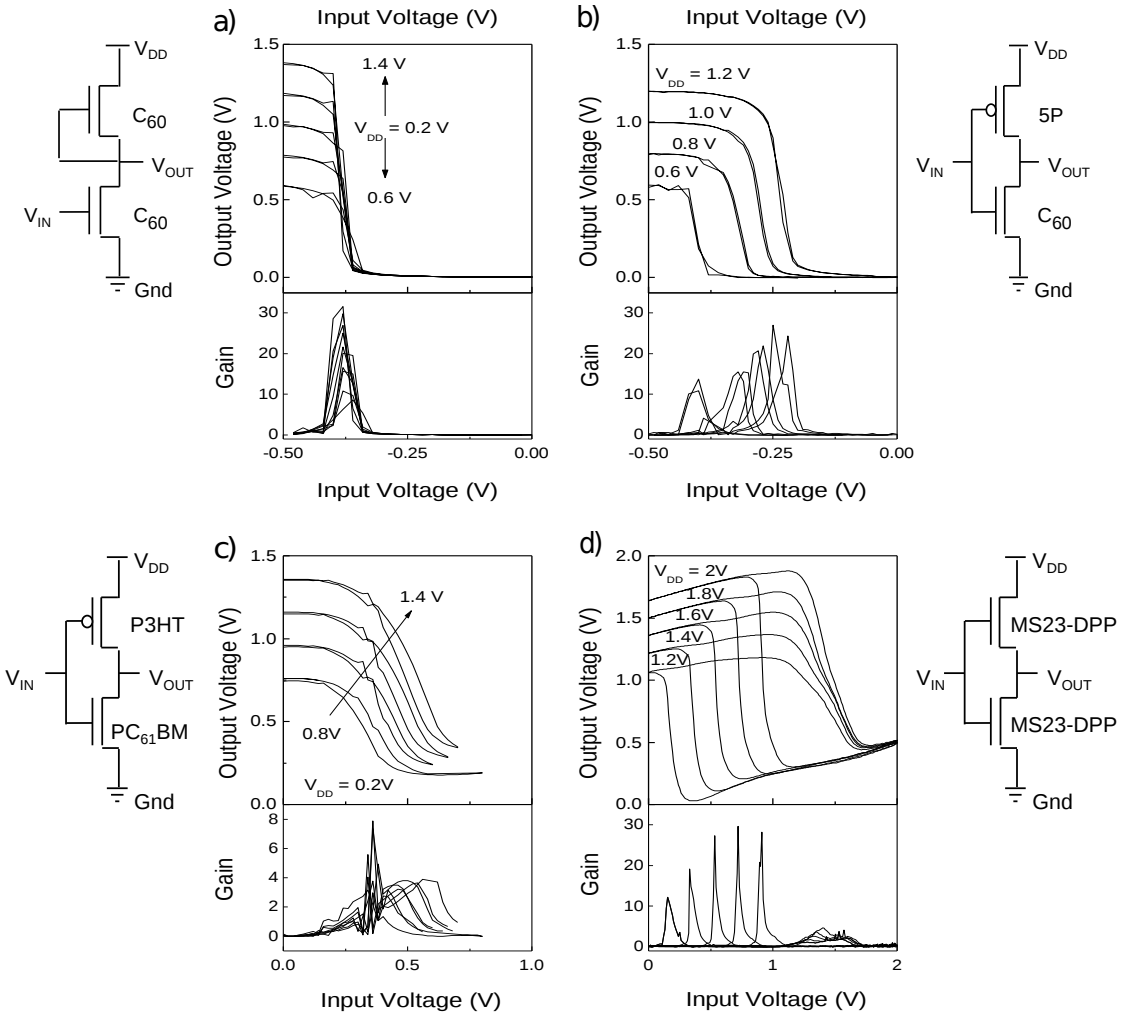

Figure 5.12: Transfer characteristics and gain for low-voltage inverters based on SAM dielectrics: unipolar inverter based on vacuum sublimed C_{60} transistors (a), complementary inverter employing p-channel pentacene and n-channel C_{60} transistors (b), complementary inverter using solution-processed p-channel P3HT and n-channel $PC_{61}BM$ TFTs (c), and complementary-like inverter based on ambipolar MS23-DPP transistors (d).

switching voltage of 1 V and large noise margins of 80%. This is a good example of the potential and advantage that SAM dielectrics offer for transistors an integrated circuits.

Electrical stability measurements were performed on C_{60} unipolar inverter and pentacene/C_{60} complementary inverter to study how bias stress affects the operation of the inverters. Bias stress measurements of inverters were performed by holding the supply voltage (V_{DD}) to 1 V and applying a continuous potential ($V_{ext} = \pm 1V$) to the input node. Figure 5.13 shows the shifts of the transfer curves for C_{60} unipolar inverter (a) and complementary pentacene-C_{60} inverter (c). The unipolar inverter transfer curve has shifted towards more positive voltages by 0.15 V after 3 hours, compared to

0.08 V for the complementary circuit. This result indicates that complementary logic suffers less from bias stress than unipolar logic circuits. The threshold voltage shift in an inverter is often described as [237] $\Delta V_{inv}(t) = \Delta V_T^1(t) + \Delta V_T^2(t) \cdot \sqrt{\frac{\beta_2}{\beta_1}}$, where $\Delta V_T^1(t)$ and $\Delta V_T^2(t)$ represent the threshold voltage shifts of the two transistors that compose the inverter, and $\beta = \mu C_i W/L$ is the design factor for each transistor. In the case of complementary logic, the threshold voltage shift of the p-channel and n-channel transistors are in the opposite direction and partially cancel each other whereas the shifts add one to the other in the case of unipolar logic. Figure 5.13 (b) shows the inverting voltage shift as a function of time. The data were fitted with a stretched exponential function. The shift at equilibrium ($\Delta V_{inv}(\infty)$) was found to be larger with unipolar logic (0.22 V) than with complementary logic (0.10 V). Minimizing the bias-induced shift of the inverting voltage is crucial to maintain descent noise margins. This example illustrates how complementary logic offers a better solution than unipolar logic towards reliable organic circuits.

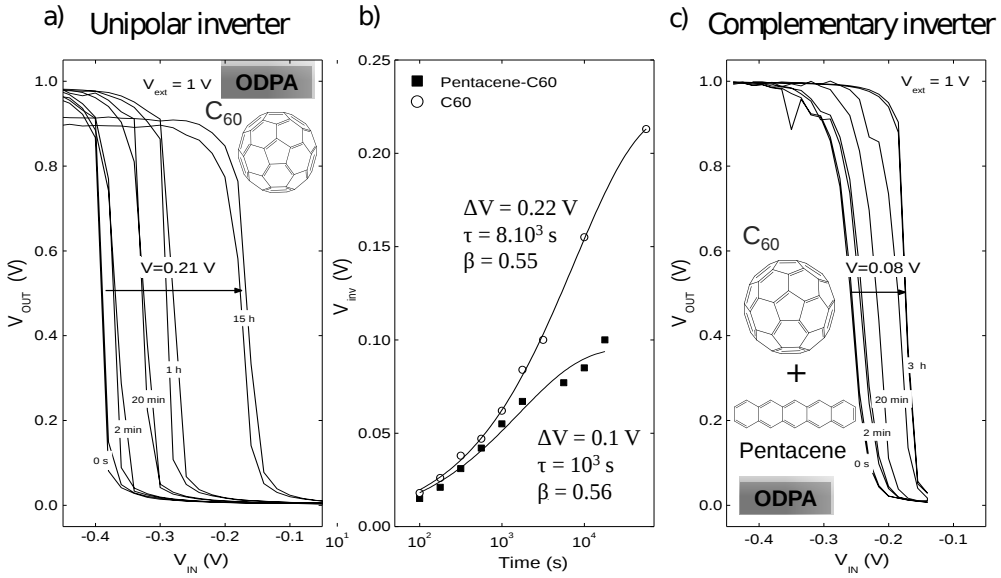

Figure 5.13: Shifts of the static transfer characterictic of (a) unipolar C_{60} inverter and (b) complementary pentacene/C_{60} inverter under electrical bias stress (V_{ext} = 1 V). Logic high (1 V) was applied at the common input while V_{DD}= 1 V. The shifts in the inverting voltage plotted as a function of time (b). Data (points) are fitted with a stretched exponential function (line).

The last two inverters employed semiconductors that were deposited by vacuum-sublimation. Here we report a low-voltage solution-processed complementary inverter built using p-channel P3HT and n-channel $PC_{61}BM$ FETs. Both P3HT polymer and $PC_{61}BM$ small molecules were deposited by spin-coating onto PHDA SAM surface. The static transfer curves of this inverter is presented in figure 5.12. The inverter exhibit small hysteresis, a trip voltage of 0.4 V and a gain of 5 (at V_{DD} = 1.4 V). The high and low noise margins were found to be 0.5 V and -0.1 V. The negative

low noise margin can be explained by the asymetric tranfer curve and the output can not be completely pulled down to the ground potential. Ball et al. reported good solution-processed complementary inverter based on small molecules diF-TESADT and $PC_{61}BM$ transistors [181]. A trip voltage of 0.3 V and a gain as high as 20 (at V_{DD} = 1.4 V) were extracted. In both cases, the p-type channel TFT presented lower conduction than the n-channel one. It was also found more challenging to form nice thin-films on SAM surfaces and obtain high-performance SAM-based transistors with p-type semiconductors. Developping p-type semiconductors that show high mobility and low threshold voltage in SAM-based transistors is important in order to build low-voltage organic inverters with high gain and large noise margins.

An alternative approach towards organic electronic circuits is the use of ambipolar transistors. Two ambipolar transistors with similar performances were connected using the complementary inverter circuitry. Their main advantage over complementary inverters based on unipolar transistors is that only one semiconductor needs to be deposited. By combining two low-voltage ambipolar transistors based on the solution processable MS23-DPP polymer (mentioned earlier in section 5.3), a complementary-like voltage inverter was fabricated. The channel dimensions for both transistors were identical (W/L=1500/50 μm). Figure 5.12 (d) shows the typical transfer characteristics of an ambipolar inverter. This inverter exhibit a good switching behaviour with a gain of 20 and an inverting voltage of 0.9 V, close to half the supply voltage (V_{DD} = 2 V). However the noise margins (NM_h = -0.1 V; NM_l = 0.3 V) are significantly reduced due to the large hysteresis observed (from 0.5 V to -0.1 V for the high margin). As often observed in ambipolar transistors [16, 235], the output voltage is not completely pulled-up to the supply voltage close to V_{in} = 0 V or pulled-down to the ground level close to V_{in}= V_{DD}.

Table 5.6: Summary of low-voltage inverters based on a SAM dielectric. The noise margin (NM) is given as a percentage of half the supply voltage (V_{DD}).

p-channel	n-channel	SAM	Gain (at V_{DD})	V_{inv} (V)	NM (%)	Ref.
(unipolar)	C_{60}	ODPA	30 (1.4V)	-0.37	...	
pentacene	C_{60}	ODPA	27 (1.2V)	-0.25	...	
P3HT	PCBM	PHDA	5 (1V)	0.4	(-15)	
P3HT	F_{17}-DOPF	PHDA	10 (1.4V)	0.44	15	
diFTESADT	PCBM	PHDA	20 (1.4 V)	0.3	...	[181]
(ambipolar)	MS23DPP	BOUDPA	20 (2V)	0.9	(-10)	
pentacene	F_{16}CuPc	ODPA	100 (2V)	0.56	40	[48, 184]
pentacene	F_{16}CuPc	PDF-ODPA	50 (2V)	(2.1)	(-30)	[184]
pentacene	F_{16}CuPc	PDF-OPDA:ODPA	430 (2V)	1.03	80	[184]

Conclusion

In summary, we have demonstrated that phosphonic acid self-assembled monolayer are highly suitable for use as ultrathin dielectrics in thin-film transistors. The molecular scale (2-3 nm) of these nanodielectrics enabled transistors operating at low voltages ($<|2|$ V). High-performance solution-processed organic transistors and circuits were demonstrated using these SAM dielectrics. Electrical stability measurements showed that all phosphonic SAM based organic transistors exhibit significant threshold voltage shift upon continuous bias stressing. The combination of different SAMs and organic semiconductors reveals that charge trapping within the semiconductor may not be the only mechanism responsible for the observed bias stress. The terminal functional group of the molecules that make up the SAM and possible electrochemical processes at the AlO_X/SAM/semiconductor interface may also play very important role. The present study is an important step towards understanding the bias instabilities in SAM-based OFETs and could prove important in future generations of low-power organic electronics.

Chapter 6

Graphene transistors based on self-assembled monolayer and fluoropolymer dielectrics

Graphene, an atomically thin layer of sp^2 carbon atoms forming a hexagonal lattice, continues to attract significant research attention because of its unique physical properties [259, 260]. A very important characteristic of graphene, when compared to traditional inorganic semiconductors, is the absence of dangling bonds in the basal plane, which implies chemical inertness and thus the possibility to process the material from solution [261, 29, 209, 262, 263] at low temperatures onto the surface of virtually any substrate material [264]. The latter characteristic is very important as it enables integration of graphene with various organic materials (e.g. dielectrics, semiconductors and conductors) to produce functional optoelectronic structures.

In this chapter we report the fabrication of graphene transistors at low-temperatures, using a solution-processable technique to transfer monolayer CVD graphene on organic dielectric interfaces. Graphene transistors based on these carefully engineered graphene/organic interfaces show improved performance and reliability when compared with traditional SiO_2 based devices. The dielectric materials investigated include Hyflon AD (Solvay), a low-k fluoropolymer, and various organic self-assembled monolayer (SAM) nanodielectrics. Both types of dielectric are solution processed and yield graphene transistors with similar operating characteristics, namely high charge carrier mobility, hysteresis free operation, negligible doping effect and improved operating stability as compared to bare SiO_2 based devices. Importantly, the use of SAM nanodielectrics enables the demonstration of low operating voltage ($<|1.5|$ V), solution-processable and flexible graphene transistors with tunable doping characteristics through molecular engineering of the SAM's molecular length and terminal group. The work is a significant step towards graphene microelectronics where large-volume and low-temperature processing are required.

6.1 Interface engineering of CVD graphene transistors with a fluoropolymer dielectric

It is well established that charge transport in graphene devices is greatly affected by intrinsic graphene acoustic phonons, Coulomb impurities, surface roughness and surface polar phonon scattering from the contiguous dielectric [52, 54]. In addition, polar substrates such as SiO_2, a commonly used dielectric in graphene devices, that retain water molecules, adversely affect the charge transport across the device channel. The primary origin of the hydrophilicity of the SiO_2 surface is the dangling bonds that are often functionalized with hydroxyl groups (-OH), which are very hydrophilic and attract water molecules. These molecules can modify the charge transfer at the SiO_2/graphene interface, which often results in extrinsic p-type doping of the graphene layer. Furthermore, carrier mobility degradation, Dirac voltage shift and operating hysteresis are commonly observed leading to electrical instabilities of the graphene transistors under test. In order to reduce these undesired effects and further improve the charge carrier transport within the channel, the graphene/dielectric interface has to be carefully engineered and optimized. Here we have investigated the effect of an amorphous fluoropolymer (Hyflon AD 3.6%) inserted between the graphene layer and the SiO_2 dielectric on the transistor characteristics.

6.1.1 Transistors based on the SiO_2/ Hyflon AD dielectric

Hyflon AD is a proprietary amorphous perfluoropolymer from Solvay comprising a copolymer of tetrafluoroethylene and a dioxole. Hyflon AD is transparent, highly hydrophobic (water contact angle $\sim 117°$) (figure 4.3) and is characterized by a very low permittivity ($\varepsilon \sim 2$). For the purpose of this study a thin layer of this perfluoro polymer was deposited onto 400 nm of SiO_2 by spin-coating a solution of Hyflon AD (3.6%) diluted in Galden (1:5). This is followed by the transfer of the graphene layer and the thermal evaporation of the gold source-drain electrodes. Due to its very high hydrophobicity, the graphene/Hyflon AD interface is expected to lead to better transistor performance than conventional SiO_2/graphene based devices. In an effort to elucidate the kinetics of water adsorption onto these very different graphene/dielectric interfaces, electrical measurements were performed under three different atmospheres: air, N_2 and vacuum. The transistors were then annealed at $200°C$ for 1 h in N_2 to remove any residual water molecules followed by electrical characterization. This measurement protocol enabled comparison of the effects of the ambient atmosphere and thermal annealing treatment on transistor operation.

Typical sets of transfer characteristics obtained from graphene transistors based on bare SiO_2 (control device) and SiO_2/Hyflon AD dielectric in N_2 and vacuum, before and after thermal annealing, are shown in figures 6.1 (a) and (b). It can be seen that as-prepared graphene transistors based on SiO_2 exhibit p-doping characteristics as evidenced by the high Dirac point (>60 V), defined in subsection 2.3.5. Because of this

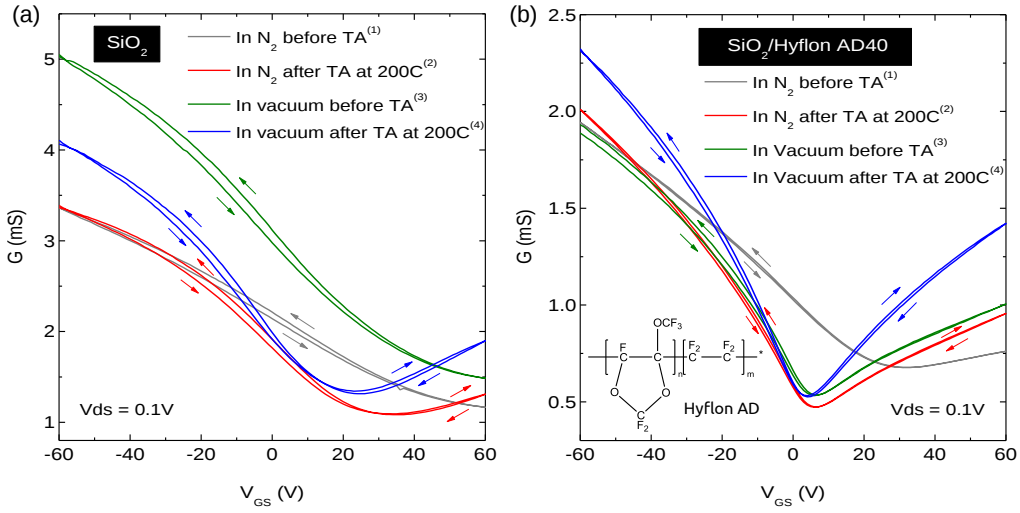

Figure 6.1: Transfer characteristics of transistors based on: (a) bare SiO_2(control device) and (b) SiO_2/Hyflon AD as the gate dielectric. Electrical characterization of the devices was performed in N_2 atmosphere (1-grey line), after annealing at T = 200°C for 1 h (2-red line) and in vacuum after a short exposure to ambient air before (3-green line) and after annealing at T = 200°C for 1 h (4-blue line). The maximum channel transconductance on/off ratio for the SiO_2 based transistor was 4.4 and was measured after vacuum annealing at 200°C. SiO_2/Hyflon based transistors show a maximum channel transconductance on/off ratio of 3.3 after annealing at 150°C in N_2. Inset: molecular structure of poly(2,2,4-trifluoromethoxy-1,3-dioxole-co-tetrafluoroethene) (Hyflon AD) fluoropolymer.

severe extrinsic p-doping behaviour only hole accumulation can be observed. After thermal annealing at 200°C for 1 h, the Dirac point is found to shift to ~34 V, with the graphene channel remaining significantly p-doped. When measured in vacuum after a short exposure to air (~5 min), the Dirac point shifts back to the values measured in as-prepared devices (>60 V). This set of measurements demonstrates the pivotal role that water molecules play on the doping characteristics of the SiO_2/graphene channel. When the same SiO_2/graphene based transistors are subjected to thermal annealing at 200°C in vacuum for 1 h, the Dirac point shifts to ~24 V and the corresponding charge density decreases to 1.29×10^{12} cm^{-2}. The latter value represents the lowest level of doping measured in our SiO_2/graphene transistors. As-prepared graphene transistors based on the SiO_2/ Hyflon AD dielectric, on the other hand, exhibit a lower Dirac point voltage (~ 31 V) when compared to SiO_2/graphene based devices (i.e. >60 V). This indicates an improved (i.e. more inert) graphene/dielectric interface. After thermal annealing at 200°C for 1 h (in N_2) the transistors exhibit an almost neutral behaviour with a Dirac point close to 6 V. When the transistor is exposed to air for 5 min, the Dirac point increases slightly to 8 V, while re-annealing the devices in vacuum at 200°C yields a Dirac point close to ~ 4 V. This value corresponds to a charge density of $1.32 \times 10^{11} cm^{-2}$, i.e. a value nearly one order of magnitude lower than that derived for SiO_2 based transistors. Therefore, it can be concluded that in the case of fluoropolymer/graphene interfaces, the extrinsic p-doping is significantly reduced

and the charge neutrality of the graphene can be maintained. The latter observation is most likely attributed to the highly hydrophobic nature of the Hyflon AD polymer, which prevents the absorption of water at the dielectric/graphene interface.

A further important characteristic is the negligible operating hysteresis observed in SiO_2/Hyflon AD based transistors when compared to bare SiO_2 based devices. Interestingly, the hysteresis is clockwise under electron accumulation and anticlockwise under hole accumulation. This is most likely attributed to charge carrier injection from the graphene to the graphene/dielectric interface [54] although further work would be required in order to verify the exact mechanism. By comparing the operating characteristics of the two types of device after annealing (200°C) in vacuum, further differences can be identified. For example, SiO_2/Hyflon AD transistors show much more pronounced ambipolar transfer characteristics when compared to bare SiO_2 based transistors although the channel conductance of SiO_2/Hyflon AD devices is lower than that measured for SiO_2 based transistors. This is attributed to the lower geometrical capacitance of the SiO_2/Hyflon AD dielectric layer (C_i ~ 5.3 nF/cm^2) when compared to bare 400 nm thick SiO_2 (~8.6 nF/cm^2). More importantly, graphene transistors based on SiO_2/Hyflon AD exhibit a maximum carrier mobility of ~1400 cm^2/Vs while for devices based on bare SiO_2 a maximum mobility value of 1000 cm^2/Vs has been obtained. This significant difference can be ascribed mainly to charged impurities present at the graphene/SiO_2 interface. In addition to higher carrier mobilities, graphene transistors based on SiO_2/Hyflon AD also exhibit higher channel transconductance on/off ratios with maximum values around 4.4 (measured in vacuum after thermal annealing at 200°C). Upon brief exposure to ambient air (2-3 min), transistors based on SiO_2/Hyflon AD exhibit negligible shift in the Dirac point, whereas in the case of bare SiO_2 based devices the Dirac point shifts significantly to positive gate voltages and the graphene channel exhibits strong p-doping characteristics. Table 6.1 summarizes the various operating parameters of our graphene transistors based on bare SiO_2 and SiO_2/Hyflon AD measured at different experimental conditions. Based on these results it can be concluded that in the case of CVD graphene transistors, passivation of the SiO_2 surface with a non-polar polymer such as Hyflon AD leads to a significant improvement in transistor operation and specifically higher charge carrier mobility and improved channel transconductance on/off ratio.

An interesting observation that is worth mentioning is that the operating characteristics of SiO_2 based graphene transistors closely resemble those obtained by Aguirre et al. for carbon nanotube (CNT) transistors based on SiO_2 [223]. In the latter study the workers observed a reduction in the electron conduction in the CNTs upon adsorption of a water layer containing solvated oxygen present on the SiO_2 surface. A similar effect is clearly observed in our SiO_2 based graphene transistors where the n-type conduction is found to reduce upon exposure to air (see table 6.1). This confirms that the electrochemically mediated charge transfer to the O_2/H_2O redox couple appears to be ubiquitous in many different carbon-based semiconductor materials.

Table 6.1: Summary of the operating parameters measured for CVD graphene transistors based on SiO_2 and SiO_2/Hyflon AD as the gate dielectric in nitrogen and vacuum. The transistor parameters were obtained before and after thermal annealing at 200°C for 1 h. The values in parentheses correspond to the Dirac point in the reverse sweep.

Dielectric	Atmosphere	Annealing conditions	μ_e (cm^2/Vs)	μ_h	V_{Dirac} (V)	G_{max}/G_{min}
SiO_2	N_2	As prepared	-	410	>60	2.6
	N_2	200°C	300	660	34 (34)	3.1
	Vacuum	As prepared	-	670	>60	3.4
	Vacuum	200°C	360	790	23 (25)	3.1
SiO_2/Hyflon	N_2	As prepared	126	632	31 (33)	2.9
	N_2	200°C	423	1210	6 (7)	4.3
	Vacuum	As prepared	406	1151	6 (7)	4.1
	Vacuum	200°C	703	1435	4 (4)	4.4

6.1.2 Electrical stability of graphene transistors based on SiO_2/Hyflon dielectric

In order to better understand how interface engineering of the SiO_2 dielectric interface with a polymer layer can improve the transistor operation, gate bias stress measurements were performed on SiO_2 and SiO_2/Hyflon based transistors. The gate electrode was continuously biased at 60 V over 15 hours, and then left to relax. The bias stress was briefly interrupted to measure periodically the transfer characteristics of the device.

Figure 6.2 (a) presents the evolution of the transfer characteristics over a prolonged period of time when the gate electrode is under continuous bias. In both cases, a shift towards more positive voltage and a current degradation, especially for the electron branch, are noticeable. However these undesired effects are much less pronounced for SiO_2/Hyflon based transistors. For example, the dirac point (V_{Dirac}) has shifted by only 3.5 V after a period of time of 13 hours when the SiO_2 surface is passivated with the fluoropolymer, this is considerably less than the 20 V shift observed without this passivation layer (see figure 6.2 (a,d)). The p-doping effect of graphene TFTs based on bare SiO_2 is intensified after bias stressing (from 20 V to 40 V). This shift is also accompanied by a degradation of the current and reduction of the mobility. As shown on figure 6.2 (b), the hole mobility decreases by more than 20 % in bare SiO_2 after 13 hours, compared to a reduction of 7 % for SiO_2/Hyflon gate dielectric. Whereas the electron has decreased by 23 % for SiO_2/Hyflon (after 13 hours) (figure 6.2 (c)). Noteworthy is the increase in electron mobility by 10 % for bare SiO_2 devices. While recovering from gate bias stress, the dirac point shifts back towards negative voltage with a smaller proportion, 1 V and 3 V after 3 hours for SiO_2/Hyflon and bare SiO_2, respectively (figure 6.2(d)). These shifts are most likely attributed to the presence of irreversible traps. The mobility values were observed to remain relatively constant after relaxation.

For both types of graphene TFTs, i.e. with and without the polymeric passivation

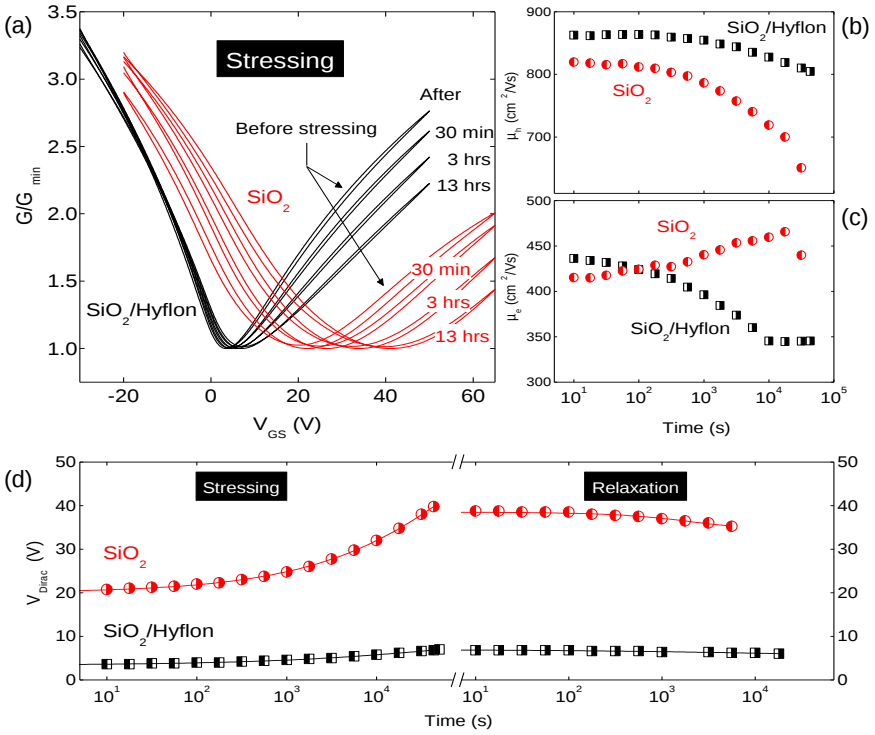

Figure 6.2: Transfer characteristics of transistors based on SiO_2/Hyflon and bare SiO_2 gate dielectrics under continuous bias stress (a). The transfer characteristics are displayed before stressing and after stressing at V_{ext} = 60 V for 30 min, 3 hours and 13 hours. Hole (b) and electron (c) mobility as a function of stressing time. Shift of the dirac point (V_{Dirac}) as a function of time under bias stressing (V_{ext} = 60 V) and under relaxation (V_{ext} = 0 V) (d). The measured data (symbols) were fitted with a stretched exponential (lines).

layer, the time-dependence of the Dirac point shift was found to be well described by the stretched exponential model (see section 2.4.3). The same model was also used to describe the reliability of devices in amorphous silicon and organic TFTs. The fitting parameters, summarized in table 6.2, clearly indicates different interface properties. Under the same stressing condition, the Dirac point shift at equilibrium is more pronounced in SiO_2based devices ($\Delta V(\infty) = 42\ V$), suggesting a larger number of trapping sites in these devices than in devices with the Hyflon passivation layer ($\Delta V(\infty) = 5.5\ V$). A time constant ($\tau$) of $5 \cdot 10^4\ s$ and a stretched parameter (β) of 0.38 were obtained for SiO_2/Hyflon based devices, compared to $\tau = 10^5\ s$ and $\beta = 0.41$ for SiO_2 dielectric without passivation layer. These results shows that passivation of SiO_2 with a thin fluoropolymer layer lead to an improved graphene interface with less trapping sites. These results are in good agreement to those obtained with interface engineering of the SiO_2 surface with phenylsilane-SAM in graphene transistors [54]. Compared to devices without interface engineering, CVD graphene transistors based on SiO_2 passivated by a thin fluoropolymer layer exhibit a superior interface quality and as a result a better electrical stability under bias stress.

Table 6.2: Summary of bias stress parameters obtained for CVD graphene transistors based on SiO_2/Hyflon and bare SiO_2(control device) gate dielectrics. Bias stress parameters include the Dirac point shift $\Delta V(\infty)$ between the equilibrium state and the initial state, τ the time constant and β the stretching parameter. The quality of each fit was assessed by its coefficient of determination (R^2), where a value closer to 1 represents a better fit. The threshold voltage shift at t = 10 000 s is also quoted as a marker.

Interface	$\Delta V(10^4 s)$ (V)	$\Delta V(\infty)$ (V)	β	τ (s)	R^2
SiO_2/Hyflon	2.4	5.5±0.6	0.38±0.02	$5 \cdot 10^4$	0.998
bare SiO_2	12	42±4	0.44±0.01	10^5	0.9997

6.1.3 Dielectric-graphene surface topography

In order to understand the origin of the difference in performance observed between SiO_2 and SiO_2/Hyflon based transistors one must also consider the dielectric-graphene surface topography. The AFM surface topography images of SiO_2 and SiO_2/Hyflon substrates are first presented in figure 6.3(a)-(b). As expected, SiO_2 exhibits very smooth surface, with a low root-mean-square (RMS) roughness value of 0.3 nm. The surface properties of SiO_2/Hyflon show regular patterns that are attributed to dewetting of Hyflon during spin casting. The latter is attributed to the very low surface energy of the Hyflon solution and its incompatibility, in terms of surface energetics, with SiO_2. Figure 6.3 displays tapping mode AFM images of the surface topography for SiO_2/Hyflon/graphene (d)-(f) and, for comparison, SiO_2/graphene (c)-(e). In all the samples, the transfered graphene layer covers the entire substrate. Importantly, the large range scans shown in figure 6.3(c) and (d) reveal substantially different graphene surface topographies. This is most likely due to graphene delamination which progressively decreases with increasing dielectric surface energy, i.e. from highly hydrophobic Hyflon AD (figure 6.3 (d)) to highly hydrophilic SiO_2 (figure 6.3 (c)), as well as with increasing dielectric roughness. In particular, wide bulged areas are visible on the SiO_2/Hyflon/graphene (figure 6.3 (f)), while narrow elongated wrinkles are present in the case of the SiO_2/graphene (figure 6.3 (e)), with the exception of some isolated bulges. This conformal nature of the graphene layer on SiO_2 is in agreement with prior observations [265] and is most likely attributable to the smoothness [266] and high surface energy of SiO_2. The extensive delamination observed in solution-transferred graphene on hydrophobic surfaces such as Hyflon AD further supports the idea that interfacial adhesion interactions, as well as surface roughness, play a pivotal role. Based on these observations it can also be argued that extended delamination detaches the graphene from the dielectric surface therefore limiting the extrinsic scattering of charge carriers and increasing their mobility. This is in agreement with the experimental data summarized in 6.1 where Hyflon AD based devices show consistently higher charge carrier mobilities as compared to bare SiO_2 based transistors.

The AFM phase images of graphene on both dielectrics are shown in figure 6.3

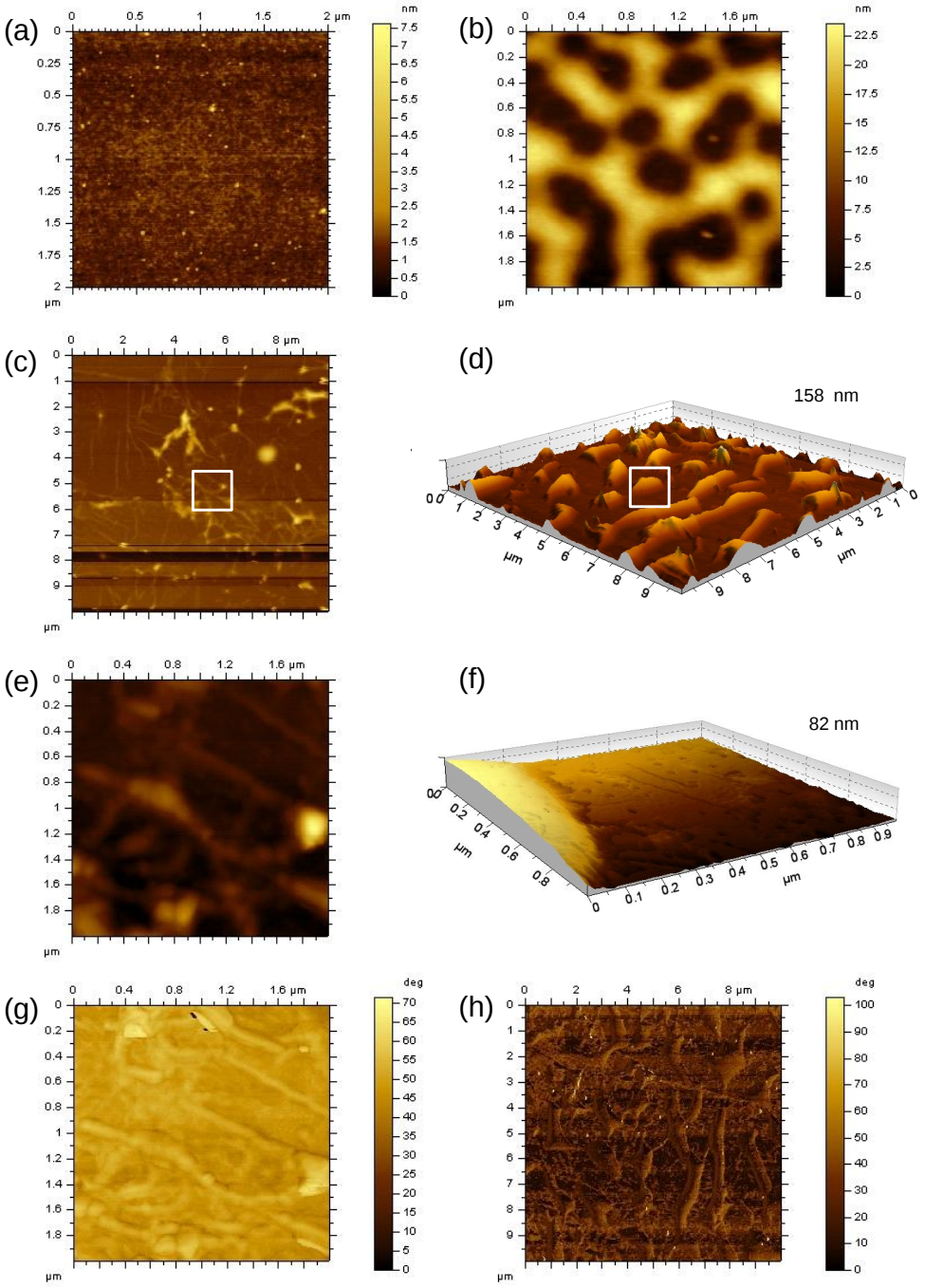

Figure 6.3: Tapping mode AFM images of the topography of SiO_2(a) and SiO_2/Hyflon (b) dielectric surfaces. Large area scan of SiO_2/graphene topography (c). Small area scan (e) of SiO_2/graphene identified by the white rectangle in (c). Large area scan of SiO_2/Hyflon/graphene topography (d). Small area scan (f) of SiO_2/Hyflon/graphene identified by the white rectangle in (d). Phase images of SiO_2/graphene (g) and SiO_2/Hyflon/graphene (h).

(g)-(h). In these measurements we have used the phase signal of the AFM cantilever to probe the presence of any residual of PMMA on the graphene surface. It can be seen in figure 6.3 that unlike SiO_2/graphene (g), in the case of SiO_2/Hyflon/graphene (h), a slight phase change is visible for the biggest bulges along the scanning direction (right to left). The latter it could be explained to be due to the variable tension induced by the bulge. In contrast, a significant change of the phase oscillation of the cantilever occurs in presence of impurities such as residual PMMA. This suggests that PMMA residuals were present on graphene layer.

6.1.4 Air stability of CVD graphene transistors

In order to better understand the impact of atmospheric oxidants on the long term stability, both bare SiO_2 and SiO_2/Hyflon AD based transistors were exposed to air for prolonged periods of time. Electrical measurements were then obtained at regular intervals over a period of six weeks during which the relative humidity (24-60%) and ambient temperature (18-22°C) were recorded.

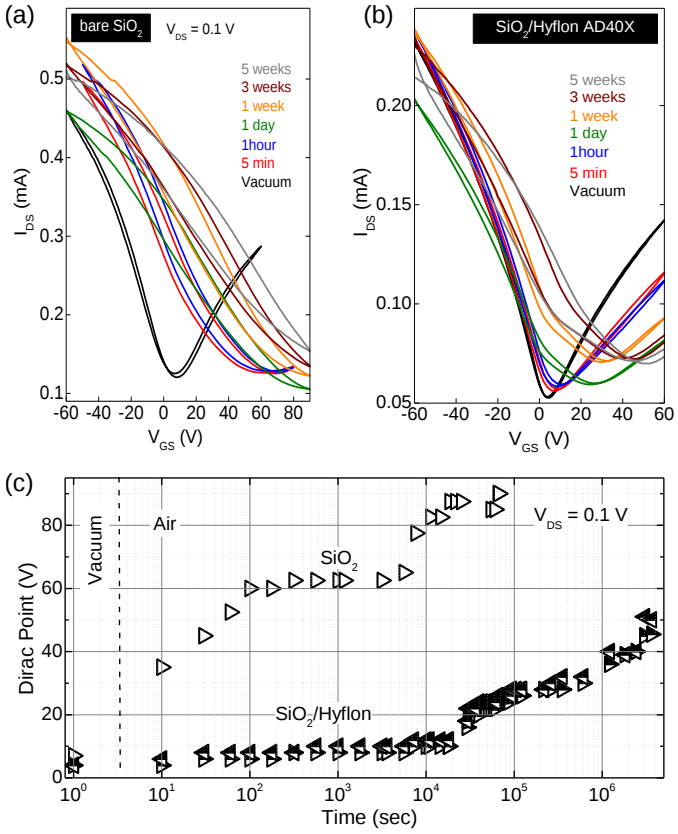

Figure 6.4: Transfer characteristics obtained from transistors based on bare SiO_2 (control device) (a), and from transistors based on SiO_2/Hyflon AD (b). Measurements were performed for different exposure times to ambient air. (c) The evolution of the Dirac point potential (V_{Dirac}) as a function of exposure time to ambient air.

Figure 6.4 displays the transfer characteristics for the two types of devices (i.e. graphene transistors based on SiO_2, figure 6.4(a), and on SiO_2/Hyflon, figure 6.4(b)) obtained in vacuum and after exposure to ambient air for 5 min, 1 h, 1 day, 1 week, 3 weeks and 5 weeks. For the bare SiO_2 based graphene transistors, the Dirac point is found to shift by more than 60 V within the first 5 min of exposure (figure 6.4(a)). On the other hand, the Dirac point in graphene transistors based on SiO_2/Hyflon AD has increased by only 20 V after being exposed to air for 1 day; 30 V after exposure for 2 weeks; and 40 V after exposure for 6 weeks (figure 6.4(b)). The evolution of the Dirac point as a function of exposure time is shown in figure 6.4(c). The latter plot demonstrates the important advantage of SiO_2 surface passivation with Hyflon AD as it significantly improves the air stability of the transistors. It can also be concluded that water absorption is much slower in graphene transistors based on Hyflon AD than for devices based on bare SiO_2. We emphasize that the same device trends have been observed for a large number of transistors with relatively small deviations. Although the passivation of SiO_2 with Hyflon AD provides a viable route towards high performance graphene transistors, it can clearly be seen from figures 2 and 3 that the resulting devices operate at relatively high voltages, an issue that will be addressed in the following subsections.

6.2 Low-voltage CVD graphene transistors based on solution processable SAM dielectrics

In an effort to reduce the operating voltage of our graphene transistors we have explored the use of ultra-thin (2-3 nm) self-assembled monolayer (SAM) nanodielectrics functionalized directly onto suitable gate electrodes. It has been shown that the use of such organic SAMs [168, 267] enables the fabrication of low voltage ($<|2|$ V) transistors based on a range of organic semiconductors as well as fullerene derivatives [168, 48]. However, despite the simplicity and potential of this approach, SAM dielectrics have never been used for realizing low voltage graphene transistors. The potential of various organic SAMs as nanodielectrics were investigated in our solution processed graphene transistors processed at temperatures below $140°C$. These transistors are shown to operate at ultra-low voltages ($<|1.5|$ V) and exhibit highly controllable doping characteristics.

6.2.1 SAM functionalization

The SAM molecules used consist of a phosphonic acid as the anchoring group, a linear aliphatic chain with tunable molecular lengths as spacers, and a end group (different between each molecule). The molecular structure of the different SAMs employed in this work were presented in figure 5.1 (chapter 5). In this study octadecylphosphonic acid (ODPA) and phosphonohexadecanoic acid (PHDA) will be of particular interest as nanodielectrics in CVD graphene transistors. The ODPA and PHDA molecules

are characterized by the highly hydrophobic methyl (-CH_3) and highly hydrophilic carboxyl (-COOH) end groups, respectively. The SAMs were deposited by submerging the gate electrodes containing substrates in a 5 mM solution of the corresponding SAM in isopropanol. Subsequently, the substrates were annealed for 12 h at 140°C in nitrogen atmosphere.

To verify the formation of a SAM, the surface energy of the functionalized gate electrode was measured using the Owens-Wendt-Kaelble method [248]. The $\theta = 0°$ wetting envelopes for the surfaces of the gate electrodes functionalized with the ODPA and PHDA SAMs together with the representative contact angle images [181, 268] were presented in figure 5.2 (a)-(c) (chapter 5). As expected, the ODPA functionalized electrode is found to be highly hydrophobic ($\theta \sim 109°$) with low surface energy mainly dominated by dispersive (non-polar) interactions. The surface of the PHDA functionalized electrode on the other hand is found to be hydrophilic ($\theta \sim 60°$) and exhibits relatively large surface energy characteristics [180, 268]. These results suggest that the SAMs are uniformly deposited forming a dense monolayer. It is worth noting that once the phosphonic SAMs are functionalized onto the native AlO_x, they appear to be thermally stable for temperatures up to 300°C (verified by contact measurements and current–voltage measurements).

The high coverage of the Al-AlOx gate electrode with the SAM was further verified by current (J) - voltage (V) measurements where the leakage current between two metal electrodes in a metal/SAM/metal structure was found to reduce from 10^{-3} A/cm^2 (i.e. no SAM: Al-AlOx/metal) to less than 10^{-8} A/cm^2 (at 1 V) upon SAM functionalization (i.e. Al-AlO_x/SAM/metal) [181]. Using similar metal/SAM/metal structures, the geometrical capacitances (C_i) of devices based on ODPA and PHDA have also been measured yielding values in the ranges of 450 nF/cm^2 and 550 nF/cm^2, respectively.

6.2.2 Quality of the graphene layer

The quality of our CVD graphene was confirmed by Raman spectroscopy and a representative spectrum is given in figure 6.5. This spectrum unambiguously shows the distinctive features of monolayer graphene (red spectrum) [38], namely the symmetric 2D band centered at ~2692 cm^{-1} with a full width at half maximum (FWHM) of ~31 cm^{-1} and 2D/G intensity ratio ~2.3. Two examples of Raman spectra of graphene few layers are also reported in figure 6.5 and it is worth noting that the D peak is barely perceptible in the single layer as well in the few-layered regions (these cover less than 5% of the surface), revealing the high crystal quality of the film.

6.2.3 Surface topography of graphene layer on SAM

As the dielectric plays a major role in device performance, AFM measurements were performed on the nanodielectric and Al/AlO_x/SAM/graphene surface. Figure 6.6 (a) displays the AFM topography image of Al-AlOx/ODPA SAM surface. This image

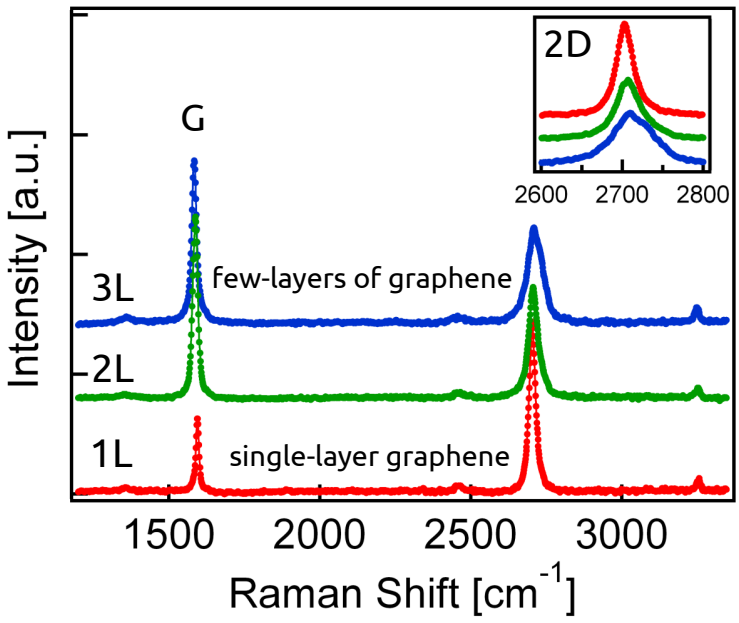

Figure 6.5: Raman spectra of single layer graphene (red spectrum) and two examples of graphene few layers (blue spectrum and green spectrum). In the inset the details of the 2D peaks are displayed. The 2D peak of the graphene few layers is asymmetric and broaden (FWHM 70 cm^{-1} for the blue spectrum and 40 cm^{-1} for the green spectrum) in comparison with the graphene single layer 2D peak (FWHM 31 cm^{-1}). The excitation wavelength of the laser used is 514 nm.

shows the high surface roughness of our Al-AlOx/SAM layer, with a root-mean-square value of ~3.3 nm. The latter is attributed to the high roughness of the Al-AlO_x layer which closely resembles the surface characteristics of Al-AlO_x/ODPA. Compared to the surface roughness of SiO_2(0.1-0.3 nm), the performance of CVD graphene transistors are likely to be lowered due to the rough surface of the nanodielectric, and hence likely to enhance short-range extrinsic scattering.

Figure 6.6 (b)-(d) displays the tapping mode AFM images of the surface topography for Al-AlO_x/ODPA/graphene. The topography of this surface presents few bulges, that are probably due to the roughness of the underlying layer. Figure 6.6 (c) shows a large scan AFM phase image of graphene on AlO_x/ODPA dielectric. On this scan (5 μm $\times$ 5 μm), no remarkable change in phase is observable, suggesting that no impurities are present on the surface. Like in the case of SiO_2/Hyflon/graphene surface (see section 6.1.3), the presence of any residual PMMA would result in a change of phase oscillation in the AFM image. However at a higher resolution (2 μm $\times$ 2 μm), these changes in phase were observable. Figure 6.6 (e)-(f) present the high resolution AFM topography and phase images for the AlO_x/ODPA/graphene. In figure 6.6 (f), the phase image on the graphene surface shows lighter spots/regions that are most likely due to the presence of PMMA residuals. The patterns of these

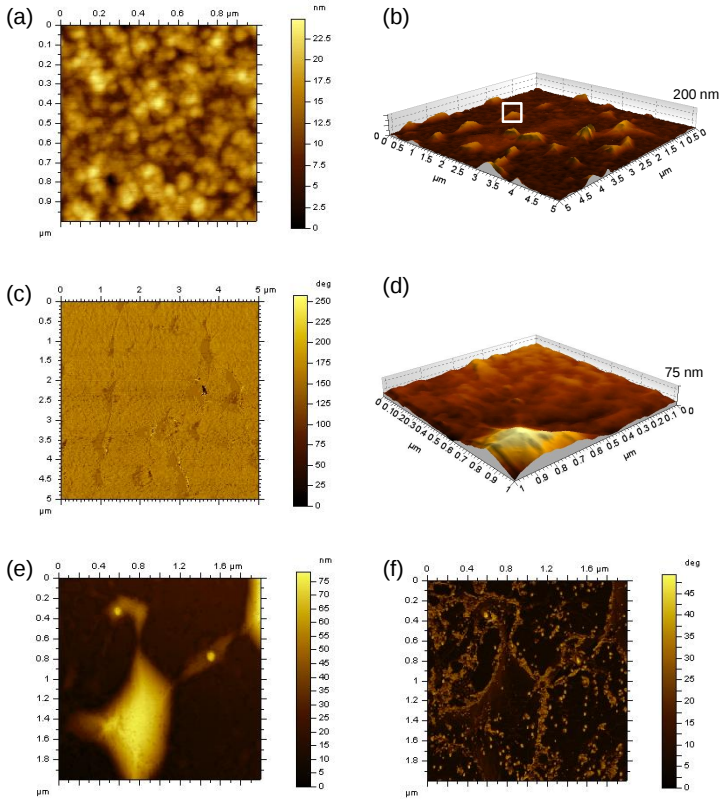

Figure 6.6: AFM tapping mode scans of the surface topography of Al-AlO_x/ODPA (a). AFM topography image (b), and phase image (c) of AlO_x/ODPA/graphene surface. The phase differences are most likely attributed to the presence of residual PMMA on the graphene surface.

regions corresponds to the increase of roughness on the topography image (figure 6.6 (e)). This suggest that cleaning of the PMMA residuals is a crucial step in device fabrication to obtain smooth high quality graphene interface.

6.2.4 Graphene transistors based on SAM nanodielectrics

The chemical vapour deposition of graphene on copper provides high quality material that can be transferred onto a variety of substrates. Here we have combined the high quality solution-transferred CVD graphene with solution-processed SAM nanodielectrics to produce low-voltage high-performance graphene transistors. Figures 6.7 (b) and (c) display the channel transconductance (G) as a function of gate voltage (V_G) for graphene transistors based on ODPA and PHDA nanodielectrics, respectively. Hysteresis free operation along with a high transconductance on/off ratio (G_{max}/G_{min}) of 5-6 and a lower level of p-doping than SiO_2/Hyflon AD transistors is observed for both SAM based devices. Although transistors based on both SAMs exhibit ambipolar transport, holes are moderately more mobile than electrons espe-

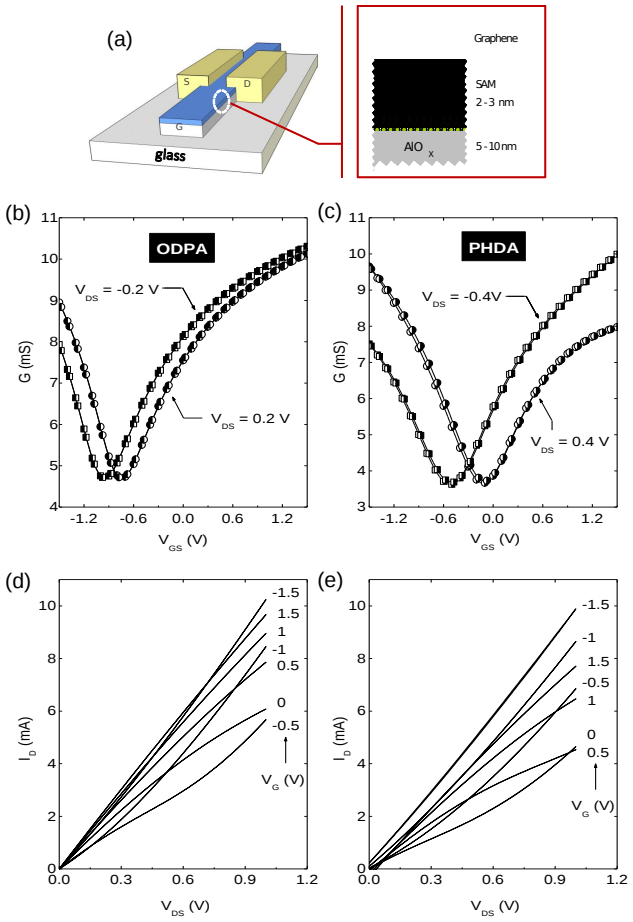

Figure 6.7: Schematic of bottom-gate graphene transistors based on SAM nanodielectrics (a). Transfer characteristics measured for CVD graphene transistors based on ODPA (b) and PHDA (c) SAM nanodielectrics. Output characteristics obtained from ODPA based devices (d) and those from PHDA based devices (e). The channel length (L) and width (W) are W/L = 1000/30 μm and W/L = 1500/40 μm for the ODPA and PHDA based transistors, respectively. ODPA based transistors exhibit a maximum channel transconductance on/off ratio of 3.4 while PHDA based transistors exhibit 2.8.

cially in the PHDA/graphene interface. In particular, ODPA based transistors exhibit higher maximum hole ($\mu_h \sim 637$ cm^2/Vs) and electron ($\mu_e \sim 372$ cm^2/Vs) mobilities than PHDA based graphene transistors ($\mu_h \sim 351$ cm^2/Vs and $\mu_e \sim 251$ cm^2/Vs). The superior characteristics of the ODPA/graphene devices as compared to PHDA can be understood in the light of the prediction that low polarity substrates [269] are beneficial for optimizing the carrier mobility in graphene. In the present case, the mobilities are adversely affected by the high surface roughness of the substrate and by the different graphene topographic features.

It is also worth mentioning that the dipole moment of the SAM's terminal group (i.e. methyl, carboxyl termination) affects the electrical characteristics of the graphene transistors through a noticeable shift in the neutrality point [182, 223]. Specifically, a

downshift of the threshold voltage (V_T) of -0.5 V is observed for positive V_D, and -1 V for negative V_D bias (figure 6.7(b)). The shift is highly reproducible and observed in all ODPA based graphene transistors. This can be attributed to the additional local field generated by the SAM surface [182, 223]. That is, the ordering of SAM molecules where molecular dipoles produce a built-in electric field superimposed over the externally applied gate field. This built-in field could shift the threshold voltage due to the modification in the carrier density within the transistor channel. This result suggests that CH_3-SAM molecules generate a local electric field that enhances electron accumulation. Similar observations have been reported by Yan et al. [223].

For CVD graphene transistors based on SiO_2-SAM, the charge carrier mobility varies between 200 cm^2/Vs and 12, 000 cm^2/Vs [270]. This large variation suggests sensitivity towards both the processing of the SiO_2 and its surface treatment with the SAM. Our results are in line with previously published data as regards of the importance of the dielectric surface. However, in the present study the SAMs do not only alter the electrostatic landscape of the dielectric-graphene interface but in addition define the overall dielectric thickness. This is a key feature of our approach as it allows fabrication of graphene transistors capable of operating at very low voltages ($<|1.5|$ V). To our knowledge this is the first demonstration of low operating voltage graphene transistors based on these solution-processable SAM nanodielectrics.

In the case of PHDA based graphene transistors, a negative shift in the V_{Dirac} between -0.5 V and -0.3 V (6.7(b)) for negative and positive V_D, respectively, was observed. Taking into account the built-in electric field model interaction, a positive shift of the neutrality point may be expected, as the hydroxyl groups are known to act as electron traps [52, 141]. However, charge transfer from the PHDA to the graphene could be a competitive mechanism, leading to a negative shift of the threshold voltage as observed in similar systems formed by carbon nanotubes (as well as fullerene derivatives) in close proximity with carboxylic groups [181]. It can thus be concluded that suitably engineered SAMs can be used to dope the graphene channel via electric dipoles and charge transfer mechanisms without compromising the charge carrier mobility through the introduction of charge scattering centres. Despite the early stage of this research it can be argued that the presence of long aliphatic chains at the graphene interface appears to be more beneficial to the electrical characteristics of graphene transistors than the presence of a polyfluorinated polymer as the passivation layer.

In order to demonstrate the compatibility of the low voltage CVD graphene devices with flexible plastic substrates, ODPA and PHDA based transistors on polyethylene terephthalate (PET) substrates have been recently fabricated in our labs. These devices exhibited good transistor operation at low voltages. However the hole and electron mobilities extracted from the flexible devices (100 cm^2/Vs for ODPA and 30 cm^2/Vs for PHDA) are lower than those measured from graphene transistors fabricated on rigid glass substrates. This lower values are attributed to the incompatibility of the PET substrates with some of the processing steps employed during the graphene

transfer. This demonstrates the potential of the use solution-processed SAM as nanodielectrics in low-voltage flexible graphene electronics.

6.2.5 Tuning of the dirac point in graphene transistors

By chemical modification of the molecular end-group of the SAMs, it is possible to accurately tune the surface energy characteristics of the monolayer nanodielectrics and hence alter the electronic properties of the transistors. The influence of the SAM molecular structure on the transport in graphene was investigated comparing eight different SAMs. In addition to ODPA and PHDA, two phenyl- and four perfluorophenylphosphonic acid SAM molecules were employed: benzyloxyundecylphosphonic acid (BOUDPA), benzyloxyoctyloxydecylphosphonic acid (BOOODPA), perfluorobenzyloxyundecylphosphonic acid (pFBOUDPA), perfluorobenzyloxyoctyloxydecylphosphonic acid (PFBOOODPA) perfluorophenoxyundecylphosphonic acid (PFPhOUDPA) and perfluorophenoxyoctyloxydecyl-phosphonic acid (PFPhOOODPA). Their molecular structure were depicted in figure 5.1 (see chapter 4).

The transfer characteristics of CVD graphene transistors based on these different SAM dielectrics are presented in figure 6.8 (a). The device performances are summarized in table 6.3. For all SAM-based devices, the transfer curves show a nice "V" shape characteristics and the output characteristics (not shown here) present good linear regime for both hole and electron transport. The primary difference observed between graphene devices incorporating different SAM nanodielectrics is a shift in the Dirac point, which can be attributed to the differences in the dipole moments of the SAM's terminal groups. ODPA SAM based devices were found to exhibit strong n-doping effect with a Dirac point of -0.5 V. The dirac point, at which the conductance reaches minimum, was found to be negative for PFBOUDPA (~ -0.2 V) and BOOODPA (~ -0.1 V) SAM based devices and positive for BOUDPA, PFBOOODPA and PFPhOOODPA (~ 0.1 V). The significant Dirac point shift towards more positive voltages can be attributed to the different built-in electrical field produced by the dipole moment of these SAM's end group. In comparison with the methyl end group of ODPA, the phenyl- and perfluorophenyl-SAM generate an electric field that enhance hole accumulation. This shift of 0.5 V, a third of the operating voltage, can be ascribed to the strong withdrawing character of the perfluorophenyl SAMs and/or on the quality of the graphene interface with the phenyl ring. Similarly, fluoroalkyl-SAMs were reported to induce significant threshold voltage shifts in C_{60} n-channel transistors [182] and pentacene p-channel transistors [183]. The Dirac point can be tuned from -0.5 V with ODPA SAM, passing by -0.2 V with PFBOUDPA or 0 V with PFPhOUDPA or to 0.2 V with PHDA SAM. These self-assembled monolayers offer a powerful technique to control the Dirac point in low-voltage graphene transistors.

The choice of the SAM molecule can also affect the mobility of the graphene transistors. Figure 6.8 (b) displays the mobility as a function of neutrality point for all the SAM based transistors that were tested. When comparing the mobility values

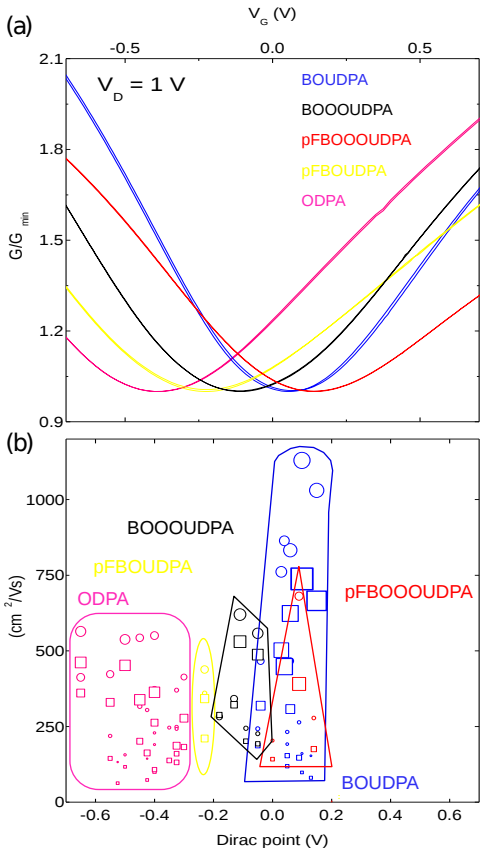

Figure 6.8: Transfer characteristics of CVD graphene FETs with the different SAM dielectrics: ODPA, BOUDPA, BOOOUDPA, PFBOUDPA, and PFBOOODPA (a). Distribution of device performances, hole (circle symbol) and electron (square symbol) mobility as a function of Dirac point (b). The size of the symbol is proportional to the corresponding opposite carrier.

of pFBOUDPA to the ones obtained for BOUDPA, both the hole and electron mobility of the perfluorinated SAM are reduced to almost half. Similarly the hole and electron mobility of pFBOOODPA SAM based devices are lowered by 55 % and 67 %, respectively, compared to BOOODPA SAM. TFTs based on pFPhOUDPA and pFPhOOODPA exhibited also mobility values lower than ODPA or BOUDPA SAM based devices (see table 6.3). The reasons that can explain these lower values can be the strong electron withdrawing of fluorine atoms, the presence of oxygen atoms that can act as trapping sites or the low surface adhesion energy of the fluorinated SAMs. Similar observations were reported with fluoroalkylsilane SAMs when combined with C_{60} as the semiconductor. Kobayashi et al. reported C_{60} TFTs with an electron mobility of 0.07 cm^2/Vs and 0.005 cm^2/Vs when the SiO_2 gate dielectrics was functionalized with octyltrichlorosilane and perfluorodecyltrichlorosilane [182]. We had also noticed a decrease of the mobility in C_{60} TFTs when using the perfluorinated phosphonic used in this study instead of ODPA or BOUDPA SAMs (see chapter 5.2).

Statistical analysis of characterization parameters showed relatively large device-

to-device variation in terms of mobility. The mean saturation mobility for holes and electrons over 7 devices was found to be 491±66 cm^2/Vs and 368±62 cm^2/Vs for ODPA-based devices, 237±62 cm^2/Vs and 177±34 cm^2/Vs for PHDA SAM, 820±202 cm^2/Vs and 533±135 cm^2/Vs for BOUDPA SAM. As these variations were observed to be more pronounced for short channel length compared to long channels, this suggests that for these graphene transistors side-currents at the edges of the device or contact resistance are not negligible. Non-uniformity of the graphene layer over the channel could also be another reason to explain these variations.

Table 6.3: Summary of the performance obtained for CVD graphene transistors based on different SAM dielectrics.

SAM	γ^D	γ^P	μ_h	μ_e	V_{Dirac}	G_{max}/G_{min}
	(mN/m)		(cm^2/Vs)		(V)	
ODPA	27.3	0.9	550	363	-0.4	2.5
PHDA	25.2	17.2	250	210	0.2	2.5
BOUDPA	26.1	3.7	832	623	0.1	2.6
BOOOUDPA	...	...	620	530	-0.1	2.1
PFBOUDPA	25.8	0.8	438	342	-0.2	1.8
PFBOOODPA	28.9	1.3	278	175	0.1	2.0
PFPhOUDPA	18	2.9	407	215	0	2.1
PFPhOOODPA	25.6	0.7	331	278	0.1	2.0

6.2.6 Electrical stability of SAM based graphene transistors

In addition to their exceptional electrical characteristics, the devices show exceptional bias stability (6.9) for stressing times of 50,000 s at V_G = 1 V. To demonstrate this, the transfer curve was measured at different times (10 s - 50,000 s) and then left to relax (i.e. no bias) for 10,000 s (figure 6.9 a).

As can be seen on figure 6.9, the neutrality point shifts by only 50 mV towards more positive voltages without a significant reduction in hole/electron mobilities. Only after 50,000 s of bias stress the drain current (I_{DS}) decreases by less than 1% (figure 6.9 b). The evolution of the Dirac point as a function of the bias stressing and recovery time is plotted in figure 6.9 (c). Its exceptional stability over such a long period of time is impressive in the light of other reports where the Dirac point has been found to shift up to ~10% over a much shorter period of time (1,000 s) [54]. In addition we notice that the Dirac point as well as the drain current (I_D) are constant during the initial ~32,000 s of bias stressing, and that the small changes occurs just during the last ~18,000 s. These measurements clearly demonstrate the superior electronic quality of the SAM/graphene interfaces developed in this work.

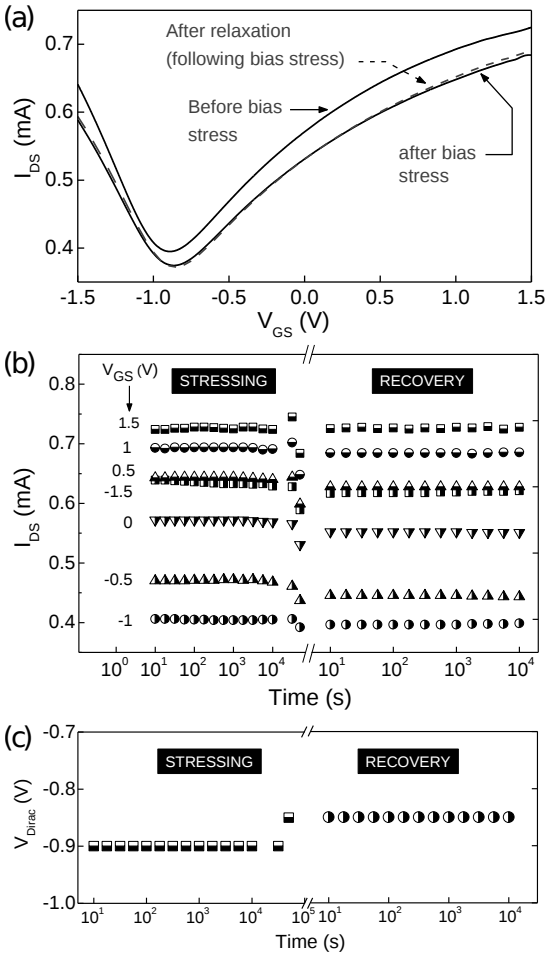

Figure 6.9: Transfer curves of a CVD graphene FET based on ODPA dielectrics bias stressed continuously for 50 000 s at $V_G = 1$ V (a). The initial transfer curve is given as a reference. After the release of the bias for 10 000 s the transfer curve was measured again. The current at different gate bias as a function of the time (b); position of the Dirac point at the stressing and recovery time respectively (c).

6.2.7 Molecular doping of graphene

In this section, we investigate the possibility of molecular doping of graphene through the adsorption of suitable chemical molecules on the graphene layer. The objective is to tune the charge transport properties via charge transfer between the dopant molecules and the graphene layer. This technique combines the outstanding transport properties of graphene with the diverse electronic properties of organic molecules. Ultimate aim of this work was to taylor and to optimize the electronic performance of graphene devices.

We have studied the doping effect of a molybdenum complex in CVD graphene transistors based on SAM nanodielectrics. The graphene layer is covered with the molybdenum tris-[1,2-bis(trifluoromethyl)ethane-1,2-dithiolene] ($Mo(tfd)_3$) complex,

which molecular structure is shown in figure 4.9. $Mo(tfd)_3$ is known to act as a p-type dopant in organic transistors [255, 256]. We demonstrate that the doping molecules lead to a tuning of the graphene FET properties due to charge transfer between the complex and the graphene layer.

In this experiment, the $Mo(tfd)_3$ dopant was deposited on the graphene layer by drop-casting of a 10 μL of the doping solution on the as-prepared substrate (heated at 70°C). $Mo(tfd)_3$ solution is prepared by diluting the complex in chlorobenzene at a concentration of 0.2 %. The experiment was carried out with CVD graphene transistors based on ODPA and BOUDPA SAM gate dielectrics. The devices were tested before and after drop casting the dopant solution. In the case of BOUDPA SAM based transistors, the substrates were annealed at 150°C for 1h following preliminary characterization and tested again.

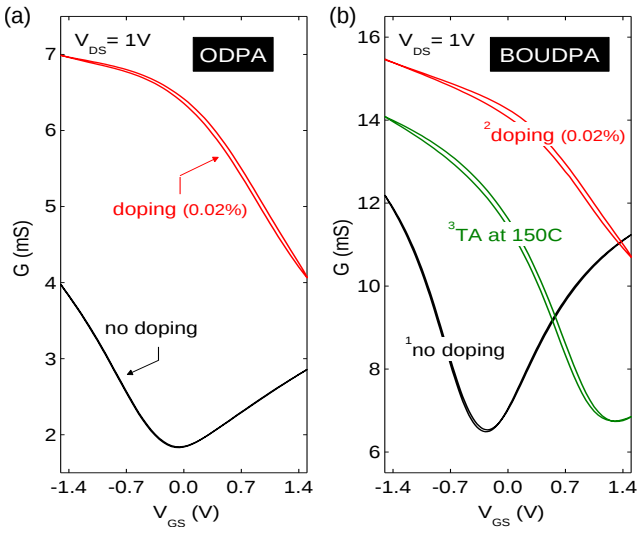

Figure 6.10: Transfer characteristics of CVD graphene transistors based on ODPA (a) and BOUDPA (b) SAM dielectrics before (black curve) and after (red curve) doping with $Mo(tfd)_3$ molecular complexes. In the case of BOUDPA based transistors, the sample was annealed at 150°C for 1 hour (green curve).

The transfer curves of graphene transistors based on ODPA and BOUDPA SAM dielectrics before and after doping treatment are presented in figure 6.10 (a)-(b). By introducing $Mo(tfd)_3$ dopant, the graphene layer is strongly p-doped, leading to a significant neutrality point shift towards more positive gate voltages. The shift is so important that the neutrality point is out of the sweeping window and only the hole branch can be observed (for higher gate voltages, there is a risk of dielectric breakdown). In the case of BOUDPA based devices (b), the doping effect is observed to be attenuated after annealing treatment at 150°C, the transfer curve shifts back toward more negative voltage. This suggests that the molecular complex is not thermally stable and that it may have partially been removed from the surface. After the annealing treatment, the neutrality point has shifted by 1.5 V compared to its

initial position (-0.2 V before doping). The doping effect can thus be reversed and controlled by thermal treatment.

Upon assembly of the dopant molecule on graphene, a decrease of the carrier mobility is observed. The hole mobility decreased from 115 cm^2/Vs down to 85 cm^2/Vs for ODPA SAM based devices and from 150 cm^2/Vs to 80 cm^2/Vs for BOUDPA SAM. After the thermal annealing, the hole mobility was found to recover to ~140 cm^2/Vs while the electron mobility retrieved to a fall of 75 % from its initial value (114 cm^2/Vs). This rather simple doping method of the graphene layer might introduce carrier scattering centers that limit the performance of the graphene device.

This work shows that the change of charge transport in graphene transistor from ambipolar to strong p-type transport is possible due to the charge transfer occurring between the dopant molecule and the graphene layer. In this way the neutrality point in graphene field-effect transistors can be tuned, either by varying the concentration of dopant and/or thermal treatment. Due to its ease of processing, this doping method is of major interest for graphene electronic applications since integration of both p and n type conduction are necessary in logic circuits. The next step would be to build a complementary-like inverter by combining doped and undoped devices to demonstrate the feasibility of this approach for practical applications.

Conclusion

In summary, we have demonstrated that graphene transistors based on carefully engineered graphene/organic dielectric interfaces exhibit improved electrical characteristics as compared to bare SiO_2 based devices. Passivation of SiO_2 dielectric with a thin fluoropolymer film yields graphene transistors with lower extrinsic p-doping, improved charge carrier mobility, higher channel transconductance on/off ratio, reduced operating hysteresis and better reliability under gate bias stress. These improvements have been attributed to the highly hydrophobic properties of Hyflon AD which prevents absorption of water molecules at the graphene/dielectric interface as well as in its peculiar surface morphology. Furthermore, we have shown that similar results can be obtained by replacing the SiO_2/Hyflon AD layer with molecular engineered SAM nanodielectrics. The ultra-thin nature of SAM dielectrics (2-3 nm) enabled the demonstration of the first low-voltage solution-processed CVD graphene transistors. The unique combination of high mobility and low operating voltage coupled with the solution processability of SAMs at low-temperatures, makes our approach attractive for the development of low-power graphene electronics over large areas using low-cost substrate materials and processing technologies.

Chapter 7

Conclusions and future perspectives

We have reported the development of unconventional gate dielectrics, such as a novel fluoropolymer and various self-assembled monolayers, and their implementation in high-performance organic and graphene-based transistors. These dielectrics can be solution-processed at low temperatures on flexible substrates, hence demonstrating their potential for large-area low-cost electronic applications. In this chapter, we summarize the key findings of this work and indicate the possible directions of research in this field. Organic electronics offer tremendous potential for a wide range of novel large-area applications by circumventing the limitations of inorganic materials while achieving comparable device performance at a considerably lower cost.

In chapter 4, the amorphous fluoropolymer Hyflon AD40 was successfully employed as a gate dielectrics in organic transistors. By spin-coating this polymer from solution, smooth uniform and pin-hole free films can be deposited. Hyflon films provide good insulating properties with low leakage current (10^{-8}A/cm^2 at 60 V) and high dielectric breakdown (>4 MV/cm). Because of these attractive properties, Hyflon AD 40 shows great promise as an insulator in organic electronics. Furthermore, due to its highly water repellent properties this fluoropolymer prevents charge trapping from impurities or presence of hydroxyl group at the interface. High performance solution-processed transistors with mobilities greater than 2 cm^2/Vs were obtained employing acene:polymer blends in combination with Hyflon as the gate dielectric using a top-gate transistor architecture. These devices exhibit excellent stability under electrical bias. The excellent transport properties were obtained by controlling the phase separation and charge trapping at the semiconductor-dielectric interface. However low linear mobility and non-linearity in the output characteristics at low drain voltages suggest the presence of contact resistance between the gold electrodes and semiconductor blends. This indicates that blend transistors are not yet fully optimized, leaving the door open for even higher hole mobility. The charge carrier injection was

enhanced by doping these blends with an organo-metallic complex (p-dopant). To further improve the device performances, other copolymers could in principle be designed as replacements of PTAA. Such polymers will offer higher intrinsic mobility and/or suitable electronic levels. Understanding of the microstructure of these blends is also important to chemically tailor these materials to specific requirements such as high charge carrier mobility, improved charge injection, air stability and/or solution processability. Hence development of new techniques that are compatible with solution processing while maintaining high performance are necessary. For example, extending the droplet pinned crystallization technique, employed for C_{60}[15], to other crystalline organic semiconductor such as acenes could be envisioned as it provides with an efficient method to prepare well-aligned single crystals over large areas.

In chapter 5, self-assembled monolayer based on phosphonic acid as the anchoring group were found to be a promising solution for use as ultrathin dielectrics in low-voltage thin-film transistors. The technology is compatible with portable and battery-powered applications requiring low-power consumption. The SAM nanodielectrics yield high geometric capacitance (~ 500 nF/cm^2) and drastic leakage current reduction (J ~ 10^{-9}-10^{-7} A/cm^2). High-performance solution-processed OFETs were demonstrated using the SAM nanodielectrics. Importantly, the use of SAMs enables the reduction of the operating voltage to below few volts (< 2 V). High mobility values were reported for not only vacuum-sublimed pentacene (p-type, 0.03 cm^2/Vs) and C_{60} (n-type, 1.2 cm^2/Vs) semiconductors, but also for solution-processed diFTESADT (p-type, 0.005 cm^2/Vs) and PCBM (n-type, 0.06 cm^2/Vs) small molecules. Solution-processing of various organic semiconductors onto the SAMs was possible by chemical tailoring of the SAM end-group because it modifies the surface energy of the monolayer. Excellent ambipolar transport with high mobility (0.2 cm^2/Vs for holes and 0.1 cm^2/Vs for electrons) were also observed employing copolymers based on the diketopyrrolopyrrole (DPP) unit.

Using SAM-based OFETs, low-voltage complementary inverter circuits were demonstrated with operating voltage below 2 V and a signal gain of 20-30. The electrical stability of low-voltage organic transistors based on phosphonic acid SAM gate dielectrics was investigated using four different organic semiconductors. It was established that all phosphonic SAM based organic transistors exhibit significant threshold voltage shifts upon continuous bias stressing. The combination of different SAMs and organic semiconductors reveals that charge trapping within the semiconductor may not be the only mechanism responsible for the observed bias stress. The terminal end-group of the SAM and possible electrochemical processes at the AlO_X/SAM/semiconductor interface may also play a very important role. The present study is an important step towards understanding the bias instabilities in SAM-based OFETs and could prove important in future generations of low-power organic electronics.

In chapter 6, we showed that engineering of the graphene/dielectric interface is a promising path towards high performance and highly stable graphene transistors. We first proposed the passivation of the SiO_2 dielectric by a thin fluoropolymer film,

Hyflon AD, and have demonstrated that these SiO_2/Hyflon-passivated graphene transistors exhibit better electrical characteristics than bare SiO_2 based devices. The improvements include lower extrinsic p-doping, air stability over weeks, improved charge carrier mobility, higher channel transconductance on/off ratio, reduced operating hysteresis and better reliability under bias stress. These improvements have been attributed to the highly hydrophobic properties of Hyflon AD which prevent absorption of water molecules at the graphene/dielectric interface as well as in its peculiar surface morphology. Graphene transistors based on SiO_2/Hyflon gate dielectric exhibit high performance, with mobility up to 1400 cm^2/Vs and current on/off ratio of 4. As the gate dielectric plays a major role for the performance of graphene transistors, further studies would be necessary to determine the role of the interfacial adhesion energy of graphene on different substrates [271] and its dependence on the surface roughness.

Furthermore, we have shown that similar results can be obtained by replacing the SiO_2/Hyflon AD layer with carefully engineered ultra-thin SAM nanodielectrics. Because of the molecular scale of the dielectric thickness (<3 nm), graphene transistors based on these SAMs operate at low voltages and typically <|1.5| V. The transistors exhibited hysteresis free ambipolar characteristics with high transconductance on/off ratio. Hole and electron mobility as high as 800 cm^2/Vs and 600 cm^2/Vs, respectively were reported for CVD graphene transistors based on SAMs. By combining the SAM nanodielectrics with plastic substrates we have also been able to demonstrate flexible low voltage graphene transistors with promising operating characteristics. CVD graphene transistors exhibited exceptional electrical stability. The drain current was found to reduce by less than 1% over prolonged bias stress (50,000 s). Furthermore the surface properties of the monolayer nanodielectric were modified by chemical tailoring of the molecular end-group of the SAMs. In this way the Dirac point of graphene transistors were finely tuned over a range of 0.8 V. These shifts result from the built-in electric field generated by the dipole moment of the SAM's end group, hence providing with a powerful method to control the Dirac point in low-voltage graphene transistors.

Finally molecular doping of graphene layer was shown to be a possible solution to tune the charge transport character of graphene transistors. Chemical absorption of a molybdenum complex on graphene leads to a change in charge transport from ambipolar to strongly p-doped behaviour. This results from charge transfer occuring between the metal transition complex and the graphene layer. The neutrality point in graphene transistors could be tuned by simply varying the concentration of dopant. However thermal stability of the complex is still an issue that would need to be addressed. The unique combination of high mobility and low operating voltage coupled with the solution processability of SAMs at low temperatures makes our approach attractive for the development of low-power graphene electronics over large areas using low-cost substrate materials and processing methodologies.

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