Solution Processed Metal Oxide Microelectronics: From Materials To Devices

by

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This thesis describes the work carried out between October 2009 and March 2013 in the Experimental Solid State Physics group of Imperial College London, under the supervision of Professor Thomas D. Anthopoulos. The material in this thesis has not been previously submitted for a degree at any University and except where explicitly stated is the product of my own work.

Stuart Richard Thomas
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Abstract

Owing to their many interesting characteristics, the application of metal oxide based electronics has been growing at a considerable rate for the past ten years. High performance, optical transparency, chemical stability and suitability toward low cost deposition methods make them well suited to a number of new and interesting application areas which conventional materials such as silicon, or more recently organic materials, are unable to satisfy.

The work presented in this thesis is focussed on the optimisation of high performance metal oxide based electronics combined with use of spray pyrolysis, as a low cost deposition method. The findings presented here are split into three main areas, starting with an initial discussion on the physical and electronic properties of films deposited by spray pyrolysis. The results demonstrate a number of deposition criteria that aid in the optimisation and fabrication of high performance zinc oxide (ZnO) based thin-film transistors (TFTs) with charge carrier mobilities as high a 20 cm^2/Vs. *Solution processed gallium oxide TFTs with charge carrier mobilities of* ~0.5 cm^2/Vs *are also demonstrated, highlighting the flexibility of the deposition method.*

The second part of the work explores the use of facile chemical doping methods suitable for spray pyrolysed ZnO based TFTs. By blending different precursor materials in solution prior to deposition, it has been possible to adjust certain material characteristics, and in turn device performance. Through the addition of lithium it has been possible alter the films grain structure, leading to significantly improved charge carrier mobilities as high as ~54 cm^2/Vs. *Additionally the inclusion of beryllium during film deposition has been demonstrated to control TFT threshold voltages, leading to improved integrated circuit performance.*

The final segment of work demonstrates the flexibility of spray pyrolysis through the deposition of a number of high-k dielectric materials. These high performance dielectrics are integrated into the fabrication of TFTs already benefiting from the findings of the previously discussed work, leading to highly optimised low-voltage TFTs. The performance of these devices represent some of best currently available from solution processed ZnO TFTs with charge carrier mobilities as high as 85 cm^2/Vs *operating at* 3.5 V.

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List of symbols and acronyms

TFT	Thin-film transistor
IC	Integrated circuit
FPD	Flat panel display
LCD	Liquid crystal display
a-Si	Amorphous silicon
a-Si:H	Hydrogenated amorphous silicon
p-Si	polycrystalline silicon
c-Si	crystalline silicon
FET	Field effect transistor
OLED	Organic light emitting diode
AMOLED	Active matrix organic light emitting diode (display)
RFID	Radio frequency identification tags
CBM	Conduction band minimum
VBM	Valence band maximum
In_2O_3	Indium oxide
SnO_2	Tin oxide
ZnO	Zinc oxide
M	Metal
O	Oxygen
Al_2O_3	Aluminium oxide
MgO	Magnesium oxide
Zn_i	Zinc interstitial
V_O	Oxygen vacancy
H_i	Hydrogen interstitial
V_{Zn}	Zinc vacancy
PLD	Pulsed laser deposition
VRH	Variable range hopping
E_T	Transport energy level (eV or J)
V_G	Gate voltage (V)
V_T	Threshold voltage (V)
V_S	Source voltage (V)

V_D	Drain voltage (V)
I_G	Gate current (A)
I_S	Source current (A)
I_D	Drain current (A)
MTR	Multiple trapping and release
μ	Charge carrier mobility (cm^2/Vs)
SiO_2	Silicon dioxide
k	Dielectric constant
C_G	Geometric capacitance (nF/cm^2)
D_T	Density of traps states per unit energy
N_T	Areal interface trap state density
PECVD	Plasma enhanced chemical vapour deposition
MOSFET	Metal-oxide semiconductor field-effect transistor
GCA	Gradual channel approximation
Q	Charge on an electron (C)
S	Subthreshold slope (V/Dec)
$I_{D(on)}$	Drain current on state (A)
$I_{D(off)}$	Drain current off state (A)
$I_{D(sat)}$	Drain current saturation state (A)
φ_M	Work function of metal (eV or J)
φ_B	Schottky barrier (eV or J)
R_C	Contact resistance (Ohms)
R_T	Total resistance (Ohms)
V_{IN}	Input voltage (V)
V_{OUT}	Output voltage (V)
V_{DD}	Supply voltage (V)
XRD	X-ray diffraction
AFM	Atomic force microscopy
UV-Vis	Ultraviolet to visible transmission spectroscopy
PL	Photoluminescence spectroscopy
FTIR	Fourier-transform infrared spectroscopy
TGA	Thermogravimetric analysis
DSC	Differential scanning calorimetry

Chapter 1

Introduction

1.1 Background

Since the earliest patents by J.E. Lilienfeld, and also O. Heil suggesting a number of ways in which the solid state could be used for electronic amplification devices, the semiconductor industry has continued to prosper and break new ground [1-4]. By 1947 the first working example of the transistor had been demonstrated at the Bell Telephone Laboratories [5, 6], whilst the first working example of the thin-film transistor (TFT) (Fig 1.1) followed some time later in 1962 [7]. These key components can be attributed to the beginning of the consumer electronic revolution started in the 1970s, where the development of large scale integrated circuits introduced electronics to the masses, putting microprocessors in the households of many [8]. Here and now at the beginning of the 21st century, microprocessors are prevalent almost everywhere. From simple household goods such as kettles and toasters, to much more complex items such as personal computers and smartphones, our reliance on the semiconductor industry becomes greater as each day passes.

The semiconductor and electronics industry is an incredibly diverse field. The microprocessor industry relies on extreme levels of integration where several billion transistors can be combined on a single

chip. The primary development hurdle in this area has always been the continued miniaturisation of circuit components. Large area electronics technologies, as are used for the fabrication of flat panel displays (FPDs), represent an entirely different sub-field of the electronics industry with its own unique set of challenges. Miniaturisation isn't the key issue here, rather the ability to deposit semiconductors over large areas at a low cost whilst maintaining high performance, is of higher concern. Likewise the ability to develop fabrication methods that can facilitate new and interesting applications, such as flexible displays, is also a fundamental driving force behind research in this area.

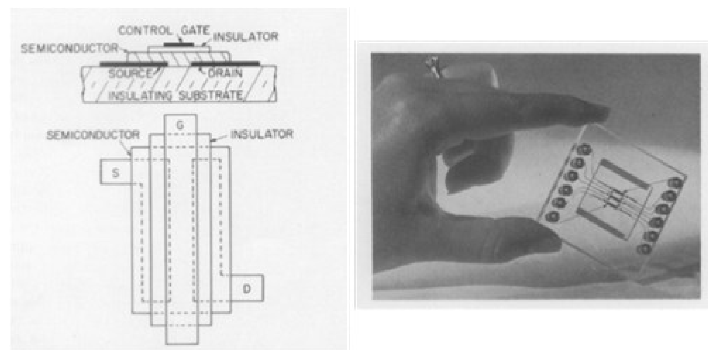

Figure 1.1: Cross-sectional and plan view of evaporated first thin-film transistor and photograph TFT having been deposited on 1-in square glass substrate. Image from [7].

In terms of the history of the FPD industry we know today, its beginnings could be said to originate from 1968, when RCA research laboratories held a press conference announcing the development of the first liquid crystal display (LCD) display [9]. Their initial work sparked further research leading to the development of the first digital watches and pocket calculators using simple matrix addressing schemes [10]. Whilst giving a talk at Sharp Laboratories in Japan in 1979, W.B Spear suggested the possible use of hydrogenated amorphous silicon (a-Si:H) as a suitable TFT material for LCD screens utilising an active matrix addressing system [11]. Spear had been working on a-Si:H for solar cells, but he had also been able to fabricate field effect transistors (FETs) using the material. This caught the attention of LCD engineers who were busy

searching for a suitable semiconductor for their TFTs, and by 1982 Cannon had developed the first dot matrix display based on a-Si TFT technology, this was followed in 1986 by Matsushita's demonstration of the first full colour TFT-LCD display [12, 13]. From this point forward the development of the FPD industry gained significant momentum, with the TFT ensuring its position as one of the most important fundamental electronic devices.

1.2 Motivation and applications

The more recent development of organic light emitting diodes (OLEDs) has led to something of a paradigm shift in the FPD market where the next generation of displays are expected to utilise the benefits of OLED technology. The use of OLEDs in FPDs is considered a superior option when compared to the current backlit LCD-TFT technologies, as they offer a thinner structured format with lower power consumption, improved colour gamut and potentially lower manufacturing costs [14].

Using OLEDs in displays means moving away from voltage driven capacitive pixel elements as used in LCDs, and toward the current driven OLED pixel elements. This brings with it new challenges for the TFTs used to drive each pixel. The a-Si:H currently in use in LCDs is only marginally satisfactory for the drive of OLEDs due to its relatively low charge carrier mobilities of ~0.5 to 1 cm^2/Vs. It is generally considered that mobility values of at least 5 times that of a-Si:H is needed before we are able to satisfactorily drive OLEDs for smaller display applications, and higher values again will be needed as display complexity, size and resolution increases. Polycrystalline silicon (p-Si) is currently in use in high-cost active matrix OLED (AMOLED) display applications such as smartphones, where the high cost of manufacturing can be passed on to the consumer. However, the prohibitive costs and stability issues associated with p-Si are currently holding back its use in large (television) sized AMOLED displays [14].

Metal oxide semiconductors and dielectrics are currently some of the most intensely researched materials for application in this area. This is primarily due of their inherent chemical stability, high performance in terms of charge carrier mobility, and their versatility in terms of deposition methods. In a similar fashion to conventional silicon semiconductors, we are able to adjust their electronic properties by doping the metal oxides. This in turn allows us some degree of control of the material and device parameters and properties, which helps diversify the range of application to which these materials are suited [10, 15].

Figure 1.2: (a) LG demonstrates their new high definition oxide TFT based display [16] and (b) is this the future of transparent oxide electronics? designer Fabio Merzari shows the world his smartphone concept [17].

The FPD display industry is one of the biggest application areas for metal oxide based semiconductors and dielectrics, however there are numerous other present and future application areas that would certainly benefit from their use. One of the other prime areas of application targeted by the work presented here is in low cost disposable electronics. Typical examples include devices such as radio frequency identification tags (RFID), smart sensors and detectors [18].

Another interesting property of metal oxide semiconductors is the fact they are largely transparent due to their large band gaps (>3.1 eV). This property is certainly beneficial to the FPD industry as reduced

aperture ratios and insensitivity to visible light can help reduce some of the headaches that display designers have to face. However, transparent electronic materials have driven a great deal of speculation as to what we may see in the future in terms of consumer electronics [18, 19]. Much of what has been postulated is currently restricted to the realms of science fiction, although transparent displays have now been demonstrated, suggesting we are certainly making progress [20].

At present there is still much work to do before we will see metal oxide based electronics as a standard component in the fabrication consumer electronics. Device stability, performance and processing methods are all areas that can still benefit from further work, and will need to be addressed before we see metal oxides as the prime material choice for large area electronics.

1.3 Thesis outline

This thesis describes work performed in the area of metal oxide semiconductors/dielectrics and devices. The focus of the work is twofold, but primarily the exploration and optimisation of metal oxide based thin-film transistors is the major concern. The use of spray pyrolysis as the key deposition method was the second focus of the work presented here. The combined use of metal oxides and spray pyrolysis opens several avenues for research, but importantly it presents a viable route toward low cost high performance electronics.

Some of the issues addressed by this work include the need for higher performing thin-film transistors that are suited for the next generation of FPD technologies, and also the need for devices that can help enable the fabrication of low power electronics. The solution to these issues presented here include the use of novel doping methods, offering a route to significantly improved device performance, and also the introduction of spray pyrolysed high-*k* dielectric materials that allow the fabrication of ultra-low voltage devices. Concurrently, all of these improvements are realised using spray pyrolysis as the deposition

method, offering a low cost, straightforward solution to the complex issue of semiconductor deposition.

The findings presented here are divided into three main chapters. The first chapter discusses work on simple binary oxides of zinc oxide and gallium oxide. These materials are investigated using a number of characterisation techniques and through the fabrication of thin-film transistors. Optimised devices are presented based on zinc oxide, and exhibit high electron mobility values (~20 cm^2/Vs) while gallium oxide based transistors yield electron mobilities on the order of ~0.5 cm^2/Vs.

The second chapter builds on the previous chapters work through the introduction of a facile chemical doping methodology. Results illustrate how the addition a number of different dopants can alter the crystalline structure of zinc oxide films grown by spray pyrolysis, in turn leading to significantly improved charge transport (mobilities of ~54 cm^2/Vs) and device characteristics (threshold voltage control).

In the final chapter, spray pyrolysis is used to deposit high-*k* dielectric materials including yttrium oxide, aluminium oxide and zirconium oxide. By combining the previously discussed spray pyrolysed semiconductors with these high dielectric constants oxides, the fabrication of low operating voltage, high electron mobility (~85 cm^2/Vs) transistors is demonstrated. These devices represent some of the best performing metal oxide based transistors reported to date and demonstrate the enormous potential of spray pyrolysis for the fabrication of future electronics.

Finally a short conclusion is presented, where a summary of the work and the future outlook for oxide based TFTs is discussed.

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Chapter 2

Theory

Abstract

There is now a significant interest in the use of oxide based semiconductors for their electronic and optoelectronic properties. The beneficial properties of these materials are becoming ever more clear and there is now a strong interest from industrial researchers in developing oxide semiconductors toward commercial applications [1-3]. This chapter will review the current theoretical understanding of oxide semiconductors, looking primarily at their electrical properties, band structure and charge transport mechanisms. There will also be a discussion on the properties of dielectric materials and their relevance to thin-film transistor applications. Finally a review of thin-film transistors, their operation and how we quantify their performance is presented, including an evaluation of what fundamental issues exist when considering the application of oxide based semiconducting materials for high performance electronics.

2.1 Electronic properties of oxide based semiconductors

To some degree there is a strong resemblance between oxide based semiconductors and their more conventional silicon and other inorganic binary compound semiconductors. Charge transport is considered as band like when discussing conventional covalently bonded semiconductors, and to a large degree there is some similarity between these materials and oxide based semiconductors [4]. However, due to the ionic nature of the bonding within oxide semiconductors there are differences which play a significant role in the way oxide semiconductors perform [5].

In conventional crystalline semiconductors, formed through highly covalent bonds, there is typically a very low concentration of defects within the lattice structure. This leads to a highly delocalised band structure, within which electrons and holes are able to move with minimal restraint. Typical scattering mechanisms present in these materials include phonon scattering, lattice defects and impurity scattering. A prime example of the effect of these scattering centres can be seen when comparing highly crystalline silicone to that of its amorphous state, whereby the high defect density present in amorphous silicon leads to a large drop in charge carrier mobility from over 1400 to 1 cm^2/Vs [6].

The oxide based semiconductors under discussion here are generally much more disordered materials due to how the materials are formed and also on their chemical makeup. Normally it is this disorder, and the nature of their chemical bonding that leads to localised states, and in turn poorer device performance when compared to that of highly crystalline semiconductors such as silicon. Typically oxide semiconductors exist in either amorphous or poly-crystalline phases, and in the case of polycrystalline materials there is the added issue of grain boundaries creating additional barriers to charge transport [7, 8]. For both cases we are able to utilise a number models used previously in the analysis of charge transport in silicon to help us better understand the nature of charge transport phenomenon within oxide based semiconductors.

2.1.1 Electronic structure and charge carrier generation

Much like conventional covalent semiconductors, the electronic properties of metal oxides are most accurately described by their band structures. However, the interaction between the metal and oxygen orbitals leads to more complicated electronic structures and in turn a significant disparity between electron and hole conduction in a given species.

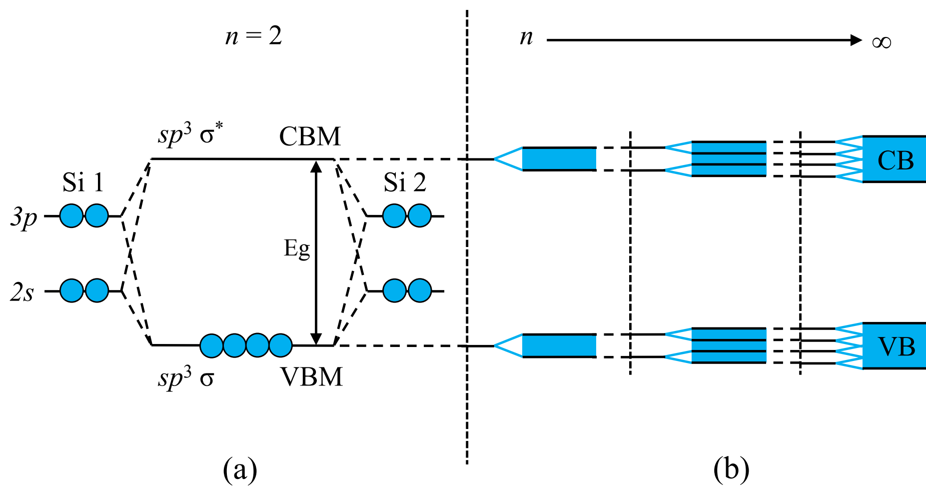

Figure 2.1: (a) Formation of band gap (Eg) through hybridised bonding of silicon atoms, and (b) formation for continuous energy bands through splitting of molecular orbitals contributed by increasing numbers of Si atoms, *n*.

When atoms are brought together in semiconductors such as silicon, a covalent bond is made resulting in hybridised anti-bonding (sp^3 σ*) and bonding (sp^3 σ) states. As many more atoms are brought together, their atomic orbitals continue to split into separate anti-bonding and bonding states, each with different energy levels leading to the formations of what can be considered continuous energy bands (Fig 2.1).

The most important of these bands are the conduction band and valence band, between which there is a forbidden band gap which no electron should be able to occupy. In silicon the conduction band minimum (CBM) and valence band maximum (VBM) are attributed to the anti-bonding (sp^3 σ*) and bonding (sp^3 σ) states of Si hybridised orbitals. Therefore the band gap is attributed to the energy difference of the σ*-σ levels [9].

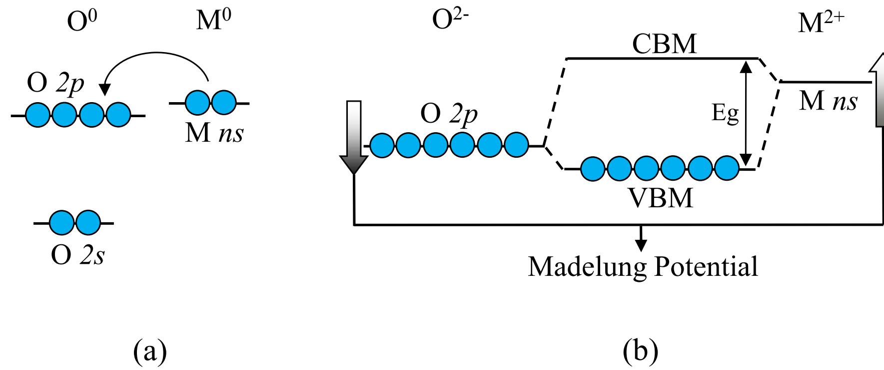

Figure 2.2: Energy gap diagram showing (a) Charge transfer between metal and oxygen atom. (b) Formation of energy gap in ionic semiconductor. Image adapted from [10].

The most commonly discussed semiconducting metal oxides, namely In_2O_3, SnO_2, and ZnO are valence compounds with a high degree of ionicity within their chemical bonding. This ionicity creates an electronic structure that differs from covalent semiconductors. The different electronegativity and ionisation energies of the two atomic species create a charge transfer from the metal to the oxygen atom and therefore an electrostatic potential, creating a stabilised ionic bond (Fig 2.2(a)). In metal oxide systems these different M n*s* and O 2*p* ionic species contribute in different ways to the conduction and valence bands, whereby the VBM is formed from the occupied O 2*p* orbital states and the CBM mainly from the unoccupied M n*s* orbital states, this in turn leads to a band gap attributed to the energy difference between the two states (Fig 2.2(b)) [8, 11].

Good electrical performance and specifically electron transport is attributed to the large spherical distribution of the M n*s* orbital states. This high level of distribution leads to well dispersed parabolic conduction band and in turn low electron effective mass (Fig 2.3). This is in contrast to the poor dispersion of the valence band caused by localised O 2*p* orbital states, leading to poor hole transporting properties [7, 8]. Good electron transporting properties are particularly prominent when considering the heavier post-transition metal oxides (In_2O_3, ZnO, SnO_2) whose conduction bands are much better dispersed than those of the lighter metal oxides (Al_2O_3, MgO), that typically form insulators [8].

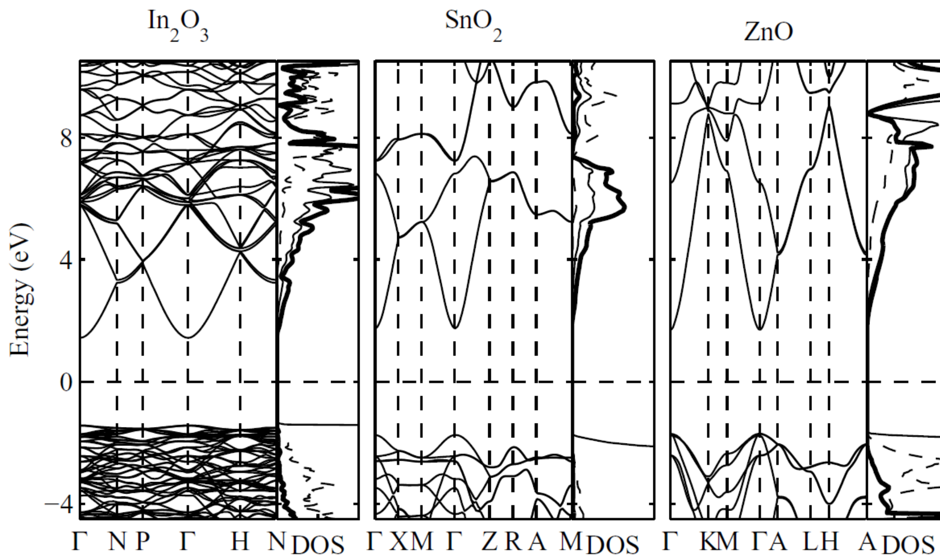

Figure 2.3: Band structures and partial density of states (PDOS) of In_2O_3, SnO_2, and ZnO calculated by screened-exchange local-density approximation (sX-LDA) method. For PDOS plots, the thick, dashed and thin lines represent metal s, metal p, and oxygen p states. Image taken from [8]

Another beneficial consequence of these well distributed M n*s* orbital states is the highly isotropic nature of conduction within these materials. When considering metal oxides in their amorphous state, there is a distinct lack of sensitivity toward disorder within the material structure. This is evident in the high electron mobilites achievable in devices in both the amorphous and crystalline phases [11-14]. This is in contrast to silicon whose charge carrier mobility suffers significantly when a high degree of structural disorder is introduced moving from the crystalline to amorphous phase (Fig 2.4). Some common properties known for the most common metal oxide semiconductors are shown in table 2.1.

When we consider ZnO, the Fermi level in the case of ideally stoichiometric materials, is associated with the filled O 2*p* states and the unoccupied M n*s* orbital states [4, 10, 15]. However, intrinsic defects and extrinsic dopants are both believed to lead to strong n-type conductivity and a shift in the Fermi level toward the conduction band. Almost always, the nature of these defects is found to favour that of n-type

characteristics, but a complete understanding of how this occurs is still under discussion. To some degree it is believed that Zn interstitials, Zn_i, and O vacancies, V_O, are the predominant intrinsic defects, leading to n-type characteristics, there are however a number of studies which contradict this thinking [16-19].

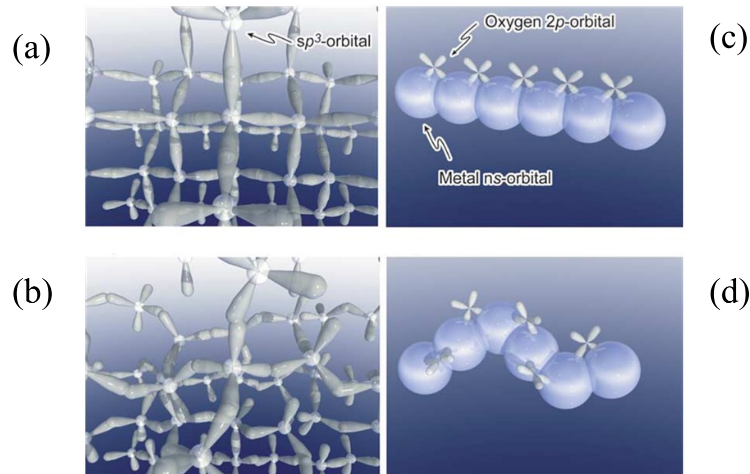

Figure 2.4: Illustration of conduction paths in (a) crystalline silicon (b) amorphous silicon (c) crystalline metal oxide and (d) amorphous metal oxide. Image taken from [11].

When considering extrinsic dopants, hydrogen is most commonly discussed as a contributor to the n-type characteristics of ZnO, specifically a number of studies suggest hydrogen interstitials, H_i, act as a shallow donors [16-20]. It is now generally agreed that useful levels of p-type conductivity in ZnO related to intrinsic defects is unlikely as most of the relevant defects require excessively high formation energies. When considering extrinsic dopants, there appears to be a lack of shallow acceptors, Li, Na, and K are considered to behave as either deep acceptors or interstitial donors that compensate the p-type conductivity [21-24].

There are numerous experimental studies into the effects of oxygen during ZnO film growth [25-28]. The predominant consequence of oxygen deficient growth conditions is an increase in free-carrier density within ZnO films. Indeed, it can be seen that by careful control of

growth conditions, the free-carrier density level can be adjusted across a range of ~10^{17} – 10^{21} cm^{-3} [7, 29, 30]. Even without the application of external processing factors, the low formation energy for V_O centres ensure they are the most predominant defect within ZnO and are known to lead to high free-carrier densities. However, in contradiction to these findings, V_O centres are also considered to function as deep level defects acting as colour centres, and are believed to be one possible cause of the of common green emission within ZnO. Therefore, according to this understanding, V_O centres should not contribute to charge carrier generation as a donor unless under the optical excitation conditions where $V_O^0 \rightarrow V_O^+ + e$, and $V_O^+ \rightarrow V_O^{2+}$ [31].

Oxide	Structure	Optical direct bandgap (eV)	Electron effective mass, m_e		
			$m^{[100]}$	$m^{[010]}$	$m^{[001]}$
ZnO	Wurtzite	3.41	0.35	0.35	0.35
In_2O_3	Byxbyite	3.38	0.28	0.28	0.28
SnO_2	Rutile	3.50	0.33	0.33	0.28

Table 2.1: Typical properties of most commonly discussed transparent oxide semiconductors [8].

Zinc interstitials, Zn_i, will in principle act as shallow donors, but their high formation energy renders them unlikely contributors to charge carrier generation in n-type ZnO [32]. Interestingly as the Fermi level shifts toward the VBM there is a significant reduction in the formation energy of Zn^{+2}, suggesting Zn_i as one of the sources of compensation in p-type ZnO [15]. There are however reports that under certain conditions Zn_i can be introduced as a shallow donor, for example when ZnO is heated in a Zn vapour followed by a rapid quenching, leading to a much higher defect rate than would normally be expected under normal processing conditions [25]. Generally this is all regarded as somewhat inconsequential as these mechanisms are not easily compatible with current processing methodologies.

The nature of zinc vacancies, V_{Zn}, has been studied with regard to their possible acceptor like behaviour within ZnO films. V_{Zn} is calculated to act as a deep acceptor and unlikely to contribute to hole generation [32]. Also the formation energy of V_{Zn} is calculated to decrease as the Fermi level shifts toward the CBM, therefore the likelihood of V_{Zn} being sufficiently abundant to act as acceptor in p-type ZnO is low [15]. More likely it is believed to act as a compensation centre in n-type ZnO, and has been shown to do so in a number of experimental studies [33, 34]. Importantly V_{Zn} has been suggested as one of the possible sources of green emission from ZnO, specifically when in the -2 charge state, equating to a deep acceptor level at 0.9 eV above the VBM. Therefore the 2.5 eV green emission is attributed to the CBM to V_{Zn} level transition [35, 36]. The remaining intrinsic defects, i.e. antisites, Zn_O, O_{Zn}, and oxygen interstitials, O_i, in principle could to some degree have an effect on charge generation in both p-type and n-type ZnO. However, they are generally believed to not be able to do so due to their high calculated formation energies [4, 15].

A number of extrinsic donor and acceptor dopants have been used in attempts to generate both n-type and p-type ZnO with varying degrees of success. However, the vast majority of work with extrinsic dopants has been targeted toward electron transporting ZnO. Aluminium, gallium and indium, when substituted on a Zn site are considered shallow donors with low ionization and formation energies [37-40]. Conventionally, the bonding structure associated with fluorine placed on an O site should behave as a deep localised state, however in practice it is observed to act as a shallow donor in ZnO, again with a low ionization energy and formation energy [40]. These materials have long been used in transparent conducting oxides as well as semiconductors and are considered worthy of use if alteration of the n-type behaviour of ZnO is required. There are also reports that commercially produced ZnO has been found to contain significant quantities of these materials [41].

Hydrogen is currently considered the most significant donor in ZnO. It is understood to behave as a shallow donor in the thermodynamically stable H_i^+ state [16, 17, 19, 42]. Hydrogen is

considered to act as an interstitial donor as well as a substitutional donor, H_O, replacing oxygen, whilst in both cases only requiring low formation energies [4, 16]. Experimentally, ZnO films exposed to hydrogen plasma have shown a three times enhancement in free electron concentration [43]. Likewise films grown by PLD in a hydrogen environment have shown up to three orders of magnitude improvement in carrier concentration when compared to films grown in an oxygen environment [44]. Interestingly, post growth annealing of ZnO films in a hydrogen environment is not seen to introduce shallow donors, as seen in films exposed to hydrogen during the growth process [45].

As stated previously p-type ZnO has remained a challenge and is yet to be realised. There are no significant reports of p-type ZnO used in devices with performance levels suitable for complimentary ZnO devices. There are a number of reports of p-type ZnO by hall measurement, but again performance is low and there are often stability issues associated with the films [21, 22, 46]. Meanwhile p-type investigations have moved more toward other metal oxide systems with more dispersive VBM, such as Cu_2O, delafossites $CuMO_2$ (M = Al, Ga, or In), and oxychalcogenides LaCuOCh (Ch = S, Se, or Te) [47-50]. The common feature in these Cu(I) compounds is the contribution of Cu 3*d* states near the VBM that leads to better hole transporting properties.

2.1.2 Charge transport in oxide semiconductors

Oxide semiconductors such as ZnO, although inorganic, are considered to exhibit both band like, and hopping like charge transport characteristics. Figure 2.5 shows a schematic illustration for the different charge transport regimes commonly associated with oxide semiconductors.

At lower temperatures impurity conduction dominates as the prevalent transport mechanism, where hopping between localised states caused by defects and impurities occurs. As we approach room temperature then charge transport becomes band like [51, 52]. In addition

to these mechanisms, in polycrystalline films we need to consider the effect of grain boundaries, where localised band bending/potential barriers can also hinder charge transport. The next few sections will discuss some of these characteristics.

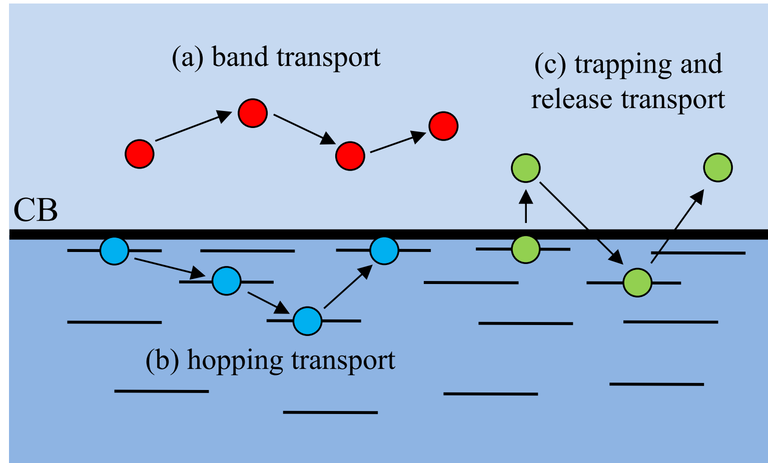

Figure 2.5: Schematic representation of (a) band like transport (b) hopping transport and (c) multiple trapping and release transport.

2.1.2.1 Band like transport

The energy levels that form the band structure, such as in silicon, (Fig 2.1) are effectively the overlapping molecular orbitals within the crystal, and these energy levels are delocalised and appear as continuous bands [6]. The weaker the overlap of the orbitals, then the less delocalised the charge carriers and therefore the higher their effective mass. The effective mass represents the inverse of the band curvature. The lower the band curvature the higher the effective mass, as seen as in the difference between the calculated conduction and valence bands of a number of oxide systems (Fig 2.3). At finite temperatures will be a number of electrons present in the conduction band (or conversely holes in the valence band), which under the application of an electric field are able to contribute to charge transport. The mobility of these carriers will be determined by scattering mechanisms such as impurity and phonon scattering. At higher lattice temperatures there is an increase in the

phonon scattering component. Conversely at lower lattice temperatures phonon scattering becomes less prevalent and impurities become the dominating scattering component.

At these low temperatures, carriers move more slowly making them more susceptible to the influence of impurities. As the lattice temperature increases, so does mobility until phonon scattering once again becomes the dominating scattering component. Therefore mobility that appears to be directly proportional low temperature dependence, and inversely proportional to higher temperatures is indicative of band like charge carrier transport [6, 53, 54].

2.1.2.2 Hopping transport

Hopping transport can be pictured as charge carriers hopping between neighbouring localised states within kT of the Fermi level, where the typical potential barrier between these states is referred to as the activation energy [53, 55]. As stated, charge transport in oxide semiconductors is a mixture of band like and hopping transport, the latter due to localized states caused by defects, ionic interactions and disorder within the material. This hopping transport has long been studied within organic and amorphous silicon semiconductors. Therefore there are a number of models that we are able to adapt to our use when studying oxide semiconductors.

Typically, hopping transport is studied using models where an energetic and spatial separation is considered between the two states across which the transport is trying to occur, in turn determining the rate at which charge can transfer. Miller and Abrahams created a model in an attempt to explain the temperature dependence of mobility by assessing the hopping rate due to tunnelling between sites [56].

To account for hopping between non-nearest sites there needs to be some modification to this model. Motts variable range hopping (VRH) model does this by accounting for short distance transfer with high

energy barriers, and also long range transfer with low energy barriers, where the latter may be preferable [57].

2.1.2.3 Multiple trapping and release

Disorder within oxide semiconductors, such as impurities, defects and grain boundaries lead trap states within the energy gap able to contain charge carriers for a period of time that is dependent on the trap energetic level and also the temperature. The transport energy level E_T, is the band edge or mobility edge of the semiconductor, and is the energy level that a carrier must attain in order to contribute to transport. This leads to a thermally activated trapping and release phenomenon within the semiconductor, in turn leading to a thermally dependant mobility characteristics, which is also dependent on the applied gate voltage, $V_{G.}$ The multiple trapping and release model (MTR), originally developed for charge transport in amorphous silicon [58], assumes transport of carriers only occurs above E_T and is limitless, but the overall rate is governed by the trapping and release of carriers below E_T. Also the model assumes all carriers that encounter a trap state are trapped and can subsequently only be released by thermal activation.

2.1.2.4 Grain boundary limited charge transport

Grain boundaries within polycrystalline oxide semiconductors play an important role in charge transport. It is normally assumed that charge transport within grains is delocalised and that the limiting factor is largely due to the trap states located at the grain boundaries. To this end there are a number of models that are used to explain the different electronic states at the grain boundaries (Fig 2.6). If the boundary width is large compared to the grain sizes, the basic MTR model is valid due to the spatially uniform distribution of trap states. Energetically distributed traps can occur where trapping of the charge carriers occurs at the boundaries due to the disorder at the boundary. The trapped charges are

screened by opposite charges creating a potential barrier to charge transport across the grain boundary (Fig 2.6(a)). Alternatively the potential well model for grain boundary trapping illustrates where an acceptor like trap state can create a localised band bending when occupied (Fig 2.6(b)) [59, 60]. We can split the measured mobility into grain boundary and bulk terms:

$$\mu^{-1} = \mu_{bulk}^{-1} + \mu_{boundary}^{-1} \qquad [2.1]$$

Grain boundaries with large energetic barriers will be the determining factor in overall mobility and we can say that generally, the barrier height will be influenced by the carrier concentration and the applied gate voltage, the latter having a direct effect on the carrier concentration. Transport across barriers can be made by thermionic emission at higher temperatures, but are more likely to be made by tunnelling at lower temperatures.

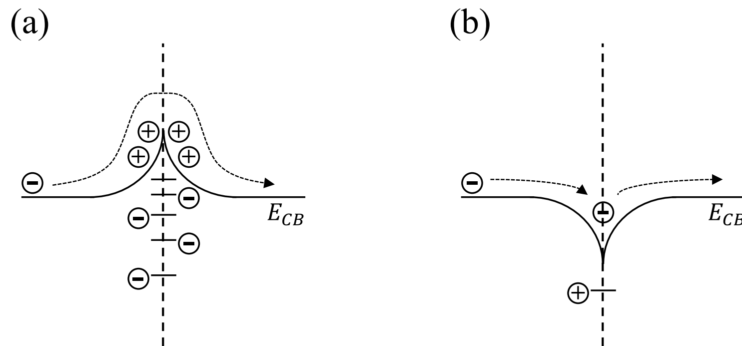

Figure 2.6: Grain boundary trapping showing (a) potential barrier trapping model and (b) potential well model for traps.

2.2 Properties of oxide dielectrics

Dielectric materials play as important a role in TFTs as semiconductors and are one of the building block materials employed in electronic device

fabrication. Within the silicon based integrated circuit (IC) industry there is an ever increasing drive toward smaller dimension transistors, driven primarily by the search for increased circuit miniaturisation and performance [61]. This has typically been achieved through advancements in process tooling and methods. Here, thinner dielectric materials are preferable as they offer circuit miniaturisation and higher levels of capacitance per unit area, but already the IC industry is approaching the fundamental limits of materials such as SiO_2. The use of new materials with high dielectric constants is now one of the strategies employed within this industry [62]. The usefulness of these materials is not only limited to the IC industry as there are a number of TFT based applications which can benefit from such materials, particularly their use in conjunction with oxide based semiconductors [63, 64]. A number of alternative oxide dielectrics with higher dielectric constants, or high-k, have already been used with oxide semiconductors. Specifically they are used due to their ability to lower the voltages at which oxide TFTs operate, and in turn lead to lower power consumption.

2.2.1 Theory of dielectrics

Dielectric materials or insulators are materials that do not transport charge, but under the application of an electrical field there is a shift in the distribution of charges within the material, or put another way they can be polarised. It is this polarisation that leads to dielectric behaviour and therefore capacitance, C [6]. If we take two electrodes distance, d, from one another and apply a voltage across them we induce an electric field given as $E = V/d$. The charge per unit area at the electrodes is proportional to the electric field and is given as:

$$Q = \varepsilon_0 E = \varepsilon_0 V/d \qquad [2.2]$$

Where ε_0 is the permittivity of free space. The capacitance, C is the proportionality constant between the charge and the applied voltage and is given as:

$$C = Q/V = \varepsilon_0/d \qquad [2.3]$$

Once we insert a dielectric material between the two electrodes then the capacitance is increased by a factor of, k, the relative permittivity of that material. Where relative permittivity is a measure of how polarisable the material is:

$$C = \varepsilon_0(k/d) \qquad [2.4]$$

2.2.2 Breakdown

At very high field strengths dielectrics suffer from breakdown where the material becomes highly conductive and often suffers from some form of damage beyond which the dielectric is no longer of any use. This is typically attributed charge carriers gaining significant levels of energy form the high field strength, enough so they are accelerated to a high enough velocity to ionise other atoms and free further charge carriers creating a chain reaction of events leading to very high free carrier concentration [6, 65]. The conduction band is essentially being filled with free carriers leading to an increase in material conductance. Typically the dielectric strength is measured in megavolts per meter *MV/m*.

2.2.3 The dielectric/semiconductor interface

The interface between the dielectric and semiconductor within TFT devices is one of the most important factors determining device performance. Application of a gate voltage creates a charge accumulation layer at the interface, extending only a small depth into the channel, of

the order of a few nanometres thickness at maximum [66, 67]. Clearly the nature of the interface in terms of structural order, trap density etc., will have some effect on the electronic properties of such a narrow accumulation layer [67]. Roughness at the interface limits charge transport and trap states lead to shifts in threshold voltages as they require filling before charge transport can take place in the accumulation layer [68] (Fig 2.7).

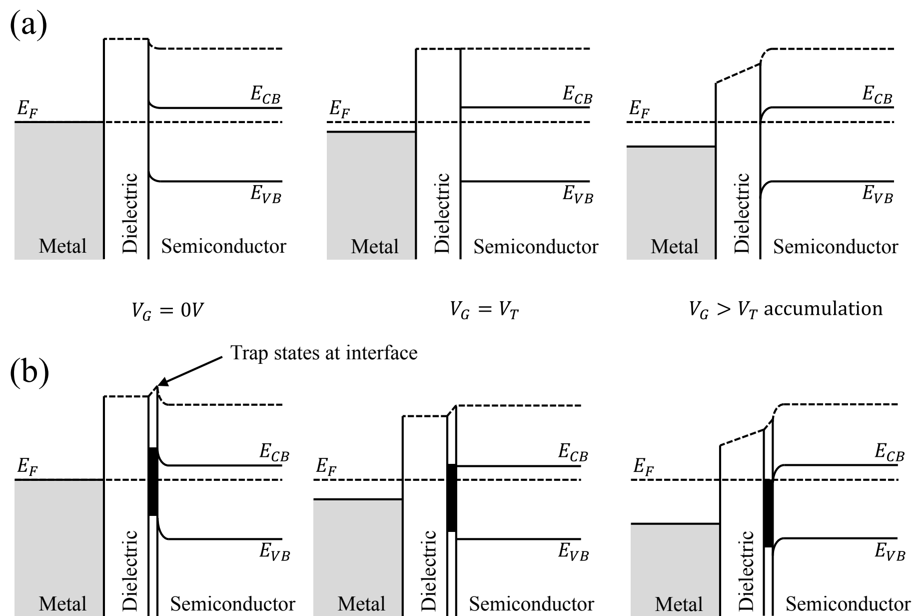

Figure 2.7: Band diagram representation of metal-dielectric-semiconductor interface (a) in the case of no interfacial traps and (b) in the presence of trap states. From left to right, $V_G = 0V$, flat-band condition and accumulation. The influence of the interfacial trap states leads to the pronounced shift required in V_G to acquire the flat-band condition.

An ideal dielectric material should have a high dielectric constant, high electric field breakdown strength, a smooth and defect free surface and should be free from contaminants. Processing considerations are of course important and will depend on device application and structure. Of course we are concerned about the quality of the interface rather than just the dielectric surface alone, so we must consider the both the dielectric

and semiconductor a complete system rather than two individual components.

2.2.4 Trap density estimation

As discussed, traps are formed at the interface due to a distribution of states that fall below the band edge. Therefore not all carriers are available for transport and so estimation of trap densities can be useful when studying the performance of different dielectrics and comparing processing methods. Trap states can be considered as additional series capacitance and will therefore affect the TFT subthreshold slope (discussed in section 2.3) and thus we use this to ascertain the density of trap states at the interface [69]. The slope can be expressed as:

$$S = \frac{kT\ln(10)}{e}\left(1 + \frac{C_{GT}}{C_G}\right) \quad [2.5]$$

Where S is the subthreshold slope, C_{GT} is the additional series geometric capacitance added due to the trap states. So at room temperature with no trap states the subthreshold slope should be approximately 60mV/dec. The relation of capacitance due to trap states, to density of traps states, expressed in units of $[\text{energy}]^{-1}[\text{length}]^{-1}$, is given as $C_{GT} = e^2 D_T$. So we can obtain D_T:

$$D_T = \frac{C_G}{e^2}\left(\frac{eS}{kT\ln(10)} - 1\right) \quad [2.6]$$

This method is not ideal as it doesn't account for the possibility of bulk states/traps which can also affect the overall conductivity of the film and of course the subthreshold slope [70]. Alternatively we can look at the threshold voltage as it gives an indication of the number of traps that require filling before the device turns on. This is generally considered the

point of equilibrium between all trap states being filled and carriers being fully mobile. So we can estimate an areal charge trap density by the following [6]:

$$N_T = \frac{C_G |V_T - V_{ON}|}{e^2} \quad [2.7]$$

It should be noted that as the temperature rises then the Fermi level approaches that of the band edge, therefore the number of trap states that are in need of filling for a given gate voltage will reduce. To this end it is often the case that the threshold voltage is to some degree influenced by temperature [71]. The density of trap states that are within a few kT of the band edge can be calculated as:

$$D_T = \frac{\partial N_T}{\partial E} = \frac{C_G}{ek} \frac{\partial V_T}{\partial T} \quad [2.8]$$

This suggests that threshold voltage is proportional to temperature, and close to the band edge the density of trap states is to some degree independent of energy. It should be noted that these methods for calculating trap densities can lead to different values as the energy systems probed in each case differ.

2.3 Field effect transistors

Thin-film transistors (TFT) are three terminal field effect devices similar in operation to devices such as the metal–oxide–semiconductor field-effect transistors (MOSFET) used in integrated circuits. However, MOSFETs and other similar devices are fabricated in such a way that the active device material i.e. silicon, or at least part of it, acts as the device substrate. For example, in the case of integrated circuits a silicon wafer is

cut from a high purity ingot providing the substrate, functionality is then added by a variety of methods including the diffusion of doping elements into selected areas of the substrates, lithography and etching steps. The major advantage of such fabrication methods are in the fact that charge transport in single crystal devices is much improved when compared to that of poly-crystalline or amorphous materials. This is all at the cost of complexity and often high temperature/vacuum processing methods [72].

TFTs on the other hand, are fabricated by the deposition of thin films of active and non-active materials onto substrates which are typically insulating and often made of glass or plastic. This is only possible using comparatively low temperature deposition techniques such as PECVD or sputtering. Although lower in cost, the nature of these deposition methods leads to TFT active layers that are amorphous or poly-crystalline with significantly lower performance characteristics. Poorer performance however, has not hindered the development of materials and fabrication methods for TFTs due to the ever increasing growth of the flat panel display (FPD) market, and the emergence of new market areas such as low cost disposable electronics [73].

2.3.1 Device architectures

Thin-film transistors in their most common and basic form are constructed using three main components, namely the dielectric layer, the semiconductor layer and three contacts consisting of the gate, source and drain contacts. The source and drain contacts are directly in contact with the semiconductor, whilst the gate contact is separated from the semiconductor layer by the dielectric. They can be fabricated using a number of different structural layouts (Fig 2.8). The transistor channel length is defined as the distance between the source and drain contact, whereas the channel width is defined as the distance over which the source and drain contact run parallel to one another.

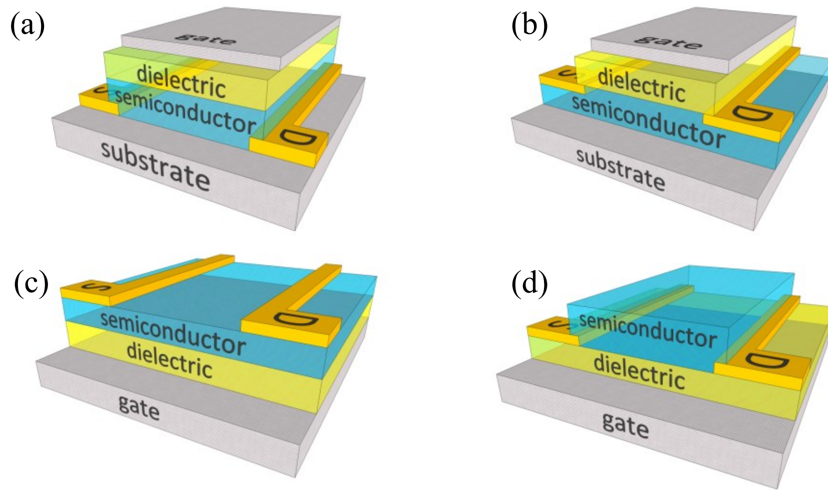

Figure 2.8: Typical TFT device architectures (a) Staggered, top-gate. (b) Coplanar, top-gate. (c) Staggered, bottom-gate. (d) Coplanar, bottom-gate.

2.3.2 Principles of operation

TFTs are classified as field driven current control devices. By application of a field at the gate contact, we are able to modulate the current that flows between the source and drain contacts. TFT operation can be classified as enhancement mode or depletion mode. In the case of an enhancement mode n-type TFT, it would be considered as normally off, i.e. no drain current under no gate bias, needing to be turned on by the application of a positive gate bias. A depletion mode device would be considered as normally on, and would require the application of a negative gate bias in order to turn the device off (Fig 2.9). Devices operating under both regimes have their uses, although enhancement mode devices are most commonly used for FPDs and IC as they allow for low power operation.

Similarly to MOSFETS charge transport in TFTs occurs in an induced accumulation layer at the semiconductor/dielectric interface. If we consider the structure shown in fig 2.10 (shown under saturation), assuming an n-type enhancement mode TFT (electron transporting), by grounding the source and drain (V_S, V_D = 0), and applying a positive voltage to the gate V_G, whose value is higher than the threshold voltage V_T, we create an accumulation of charge carriers at the

semiconductor/dielectric interface whose density decreases exponentially with increasing distance from the interface.

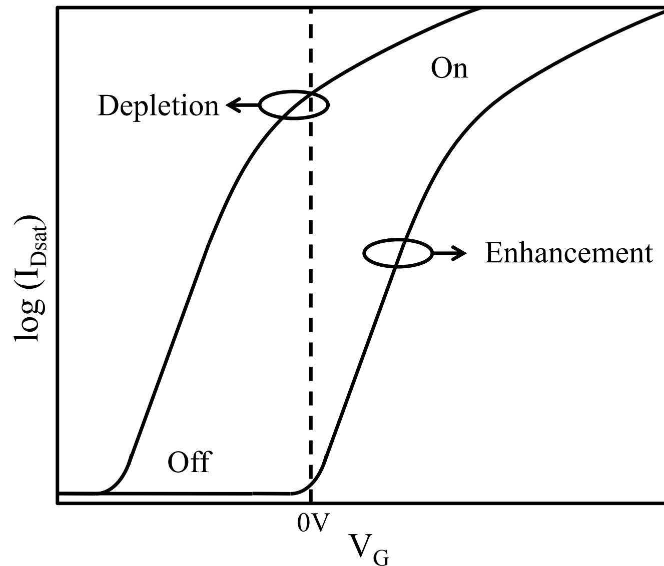

Figure 2.9: Ideal TFT transfer curves showing depletion and enhancement mode operation.

For small values of V_D we will see charge injection at the source creating a flow of current I_D, through the device, and finally charge extraction at the drain. Under these conditions the device behaves as a normal resistive element and we see the expected linear I-V relationship. As we increase V_D, so I_D will continue to increase linearly until we reach what is commonly referred to as the 'pinch off point', where the device current saturates. The difference between $V_{(x)}$, the local potential along the channel and V_G has now become less than V_T and a depletion region begins to form at the drain end of the device. With increasing V_D, so the depletion region extends into the channel (as shown in figure 2.10) creating a shorter channel, albeit a small change in comparison to the actual channel length. I_D remains saturated and only a small number of charge carriers can now be swept across the depletion region. The only way to now increase I_D is to increase V_G in order to increase the number of charge carriers at the semiconductor/dielectric interface.

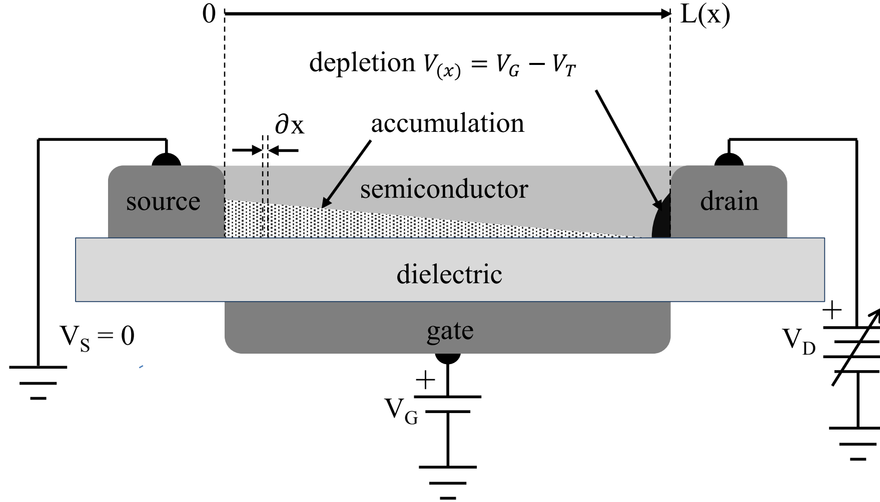

Figure 2.10: N-type TFT device under saturation, showing dielectric layer, source, drain and gate contacts, and semiconductor layer.

From this basic discussion it can be seen that TFTs present a 2-dimentsional field/transport problem comprised of two electric field components parallel F_x, and perpendicular F_y, to the semiconductor/dielectric interface. The gradual channel approximation (GCA) allows us to quantitatively solve this problem and help us extract device parameters for analysis [67]. The GCA deconstructs the problem into two, coupled one-dimension equations. One for the perpendicular charge distribution and a second charge transport equation for the parallel channel current. The approximation assumes the rate of variation of the parallel field is much smaller than that of the perpendicular one i.e.:

$$\frac{\partial F_x}{\partial x} \ll \frac{\partial F_y}{\partial y} \qquad [2.9]$$

Therefore the approximation should only be considered valid for long channel devices. Specifically, F_x should vary a minimal amount over lengths of the order of the dielectric thickness. In the case of TFTs this is generally true and the approximation remains valid. We can now begin to derive the current-voltage relationship of TFTs.

Firstly we should consider the density of accumulated charges at the semiconductor/dielectric interface using the relationship $Q = C \times V$. We can say that the charge density at point x across the channel will be proportional to the geometric capacitance C_G, of our dielectric, and the voltage at that point, given by:

$$Q_{(x)} = C_G\left[V_G - V_T - V_{(x)}\right] \qquad [2.10]$$

Where $Q_{(x)}$ is the charge density at point x across the channel, V_G the applied gate voltage, $V_{(x)}$ is the voltage at point x across the channel, and V_T is the threshold voltage. It is often the case that there is an offset in the accumulation of charges that contribute to charge transport. Typically this can be caused by donor or acceptor states leading to charge trapping in the semiconductor, or trap states at the dielectric/semiconductor interface. Likewise, an offset can be created by bulk charges present within the semiconductor when no field is applied. Therefore, as a catch all term to account for these situations, we include the threshold voltage V_T.

The drain current I_D is proportional to the charge density Q, channel width W, charge carrier mobility μ and electric field strength F. Therefore I_D at point x across the channel can be given as:

$$I_{D(x)} = W\mu Q_{(x)}F_{(x)} \qquad [2.11]$$

Where the field strength at point x given by, $F_{(x)} = \frac{\partial V_{(x)}}{\partial x}$.
Substitution gives:

$$I_{D(x)} = W\mu C_G\left[V_G - V_T - V_{(x)}\right]\frac{\partial V_{(x)}}{\partial x} \qquad [2.12]$$

To arrive at I_D we can solve for all of $I_{D(x)}$ by integrating along the channel length L, using the boundary conditions $V_{(0)} = 0$, $V_{(L)} = V_D$:

$$\int_0^L I_D \,\partial x = W\mu \int_0^{V_D} C_G \left[V_G - V_T - V_{(x)}\right] \partial V_{(x)} \qquad [2.13]$$

Giving:

$$I_D = \frac{W\mu C_G}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \qquad [2.14]$$

This general expression can be simplified for the different TFT operating regimes. Specifically, when $V_D \ll V_G - V_T$ the device is said to be operating in the linear regime, I_D is approximately proportional to V_D and charge accumulation across the channel is considered to be evenly distributed, we can therefore simplify equation 2.31 to:

$$I_{Dlin} = \frac{W\mu C_G}{L}(V_G - V_T)V_D \qquad [2.15]$$

When $V_D \gg V_G - V_T$ the device is said to be operating in the saturation regime, where the channel is depleted of carriers or *pinched off* at the drain end of the device due to the high V_D. The channel current is said to be independent of V_D and is obtained from 2.31 as:

$$I_{Dsat} = \frac{W\mu C_G}{2L}(V_G - V_T)^2 \qquad [2.16]$$

Equation 2.32 and 2.33 now provide the basis for parameter extraction when analysing experimentally obtained data.

2.3.3 Extraction of device parameters

We can extract and quantify a number performance metrics commonly used for the assessment and comparison of TFTs from experimentally acquired transfer (Fig 2.11(a)) and output curves (figure 2.11(b)). Using a combination of data and equation 2.31 we are able to extract parameters including the threshold voltage and switch on voltage V_T and V_{ON} respectively, the subthreshold slope S, the $I_{D(on)}/I_{D(off)}$ ratio and the charge carrier mobility μ in both the linear and saturation regime.

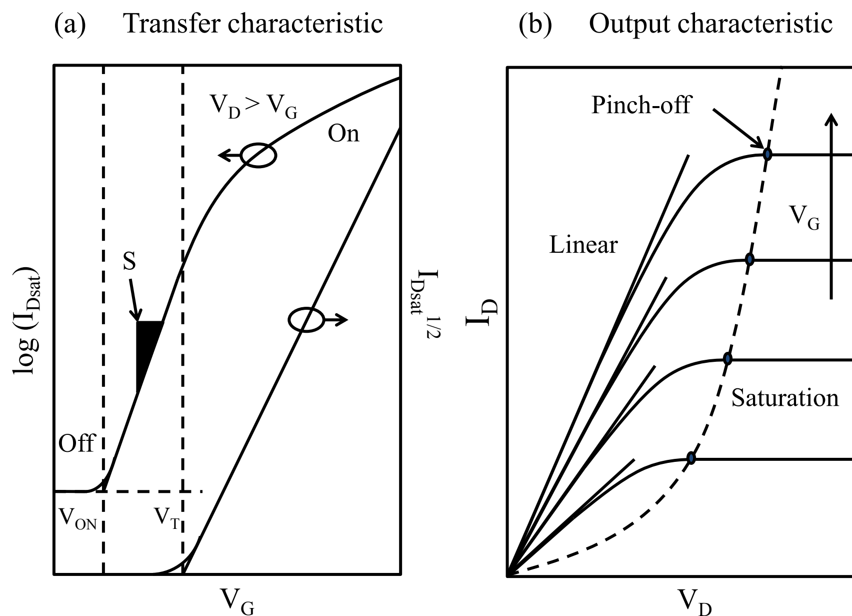

Figure 2.11: Ideal TFT measurement data showing (a) transfer characteristic for device in saturation. Here we can extract V_{ON} from the $\log(I_D)$ and V_T from the $\sqrt{I_D}$. From the output characteristics (b) we can determine under what values for V_D and V_G the device is working in the linear and saturation regimes. The intercept of the dashed line represents the channel current reaching pinch off.

The threshold voltage is not well defined when we considering TFT oxide semiconductors as the idea of V_T was anticipated for use in silicon FETs where there is first a depletion then inversion layer at the interface, as opposed to a straight accumulation within TFTs. Therefore there is some degree of ambiguity in values extracted from device

measurements [74]. Ideally in a TFT the threshold voltage will be proportional to the offset between the gate material work function and the semiconductor Fermi level under flat band conditions, which should be close to zero. As stated in section 2.2.7 this may not be the case due to various electronic states at the dielectric/semiconductor interface. When quoted, V_T is typically found by plotting $\sqrt{I_{Dsat}}$ and extrapolating a straight line fit to find it's intersect with V_G. The on voltage V_{ON}, is less ambiguous and is simply given as the value at which I_D begins to rise exponentially.

The $I_{D(on)}/I_{D(off)}$ ratio is given as the ratio between the maximum drain current and gate leakage/noise floor and is determined from the transfer curve measurements. Generally the higher the value the better and several orders of magnitude difference are preferable, somewhere on the order of 10^7 being typical for oxide based TFTs. The outright value for $I_{D(on)}$ will be determined by the charge carrier mobility and device dimensions, whereas $I_{D(off)}$ is determined by the dielectric leakage characteristics and source to drain leakage. Ideally the very low values for $I_{D(off)}$ are preferable particularly for low power consumption circuitry. The noise floor limit of measurement equipment used can sometimes have some influence on values obtained for $I_{D(off)}$, thus $I_{D(on)}/I_{D(off)}$ ratio alone is useful but should be carefully considered when viewing device performance as a whole. The subthreshold slope is a measure of how efficiently a channel forms within the device. It is expressed in *V/dec* and can be calculated as:

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)} \qquad [2.17]$$

It can be extracted from transfer characteristics and is the operating region of I_D prior to V_T where the device is starting to switch on and I_D begins to increase exponentially. As discussed in section 2.2.7,

this region of operation is where most of the injected charges are consumed in the filling of trap states in the dielectric/semiconductor interface and very few contribute to conduction.

Charge carrier mobility is arguable the most significant metric by which TFTs are assessed due to its influence on device current and speed capabilities [74]. We can extract values for the liner mobility, μ_{lin}, and saturation mobility, μ_{sat}, by differentiating equations 2.32 and 2.33 respectively. By doing so we arrive at:

$$\mu_{lin} = \frac{L}{C_G W V_D}\left(\frac{\partial I_{Dlin}}{\partial V_G}\right) \qquad [2.18]$$

And:

$$\mu_{sat} = \frac{L}{C_G W}\left(\frac{\partial^2 I_{Dsat}}{\partial V_G^2}\right) = \frac{2L}{C_G W}\left(\frac{\sqrt{I_{Dsat}}}{\partial V_G}\right)^2 \qquad [2.19]$$

Using the above equations we can extract the device mobility providing that the criterion $V_D \ll V_G - V_T$ is respected for μ_{lin}, and $V_D \gg V_G - V_T$ is respected for μ_{sat}. From equation 2.17 it can be seen that plotting $\sqrt{I_{Dsat}}$ against V_G will yield a straight line whose slope is proportional to charge carrier mobility. Extrapolation to interception of the x-axis yields the previously discussed threshold voltage V_T. Other useful methods have been proposed, specifically the concept of average mobility, μ_{AVE}, where an average mobility can be calculated that accounts for all charge carriers within the channel regardless of whether we are above or below V_T. Extracted from transfer curves when measured in the linear regime and utilising the channel conductance. μ_{AVE} is calculated as:

$$\mu_{AVE} = \frac{L}{C_G W V_D}\left(\frac{I_{Dlin}}{V_G - V_{ON}}\right) \qquad [2.20]$$

2.3.4 Metal-semiconductor interfaces

Efficient charge carrier injection and extraction between electrodes to semiconductors can sometimes provide a significant challenge when designing TFT devices.

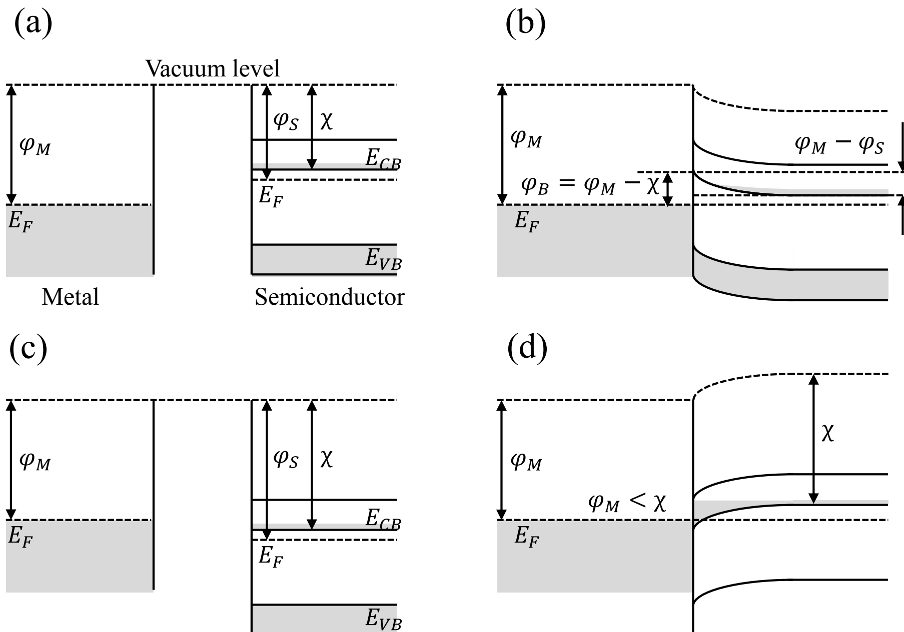

Figure 2.12: Band structure diagrams (a) and (b) for a metal-semiconductor interface, where the metal having a large work function relative to the Fermi level of the semiconductor, leads to a potential barrier at the interface φ_B, and in turn a rectifying contact. Figures (c) and (d) represent an ohmic contact due to the lower work function of the metal.

A number of factors can contribute to an improvement or worsening in the carrier injection and extraction, which in turn leads to a change in overall device characteristics. The work function of the electrode material plays the most significant role in this, where a difference between the work function of the metal electrode and the

electron affinity of the semiconductor can create potential barrier to charge carriers known as the Schottky barrier.

If we take a metal/semiconductor interface (Fig 2.12) we can see how choosing different electrode materials can lead to either an ohmic contact with no potential barrier to charge injection, or a rectifying contact with a potential barrier at the interface. Therefore, in the case of a rectifying contact, we have the formation of an energy barrier φ_B, which is a function of the metal work function φ_M, the electron affinity of the semiconductor X, and the term Δ included to account for possible metal-semiconductor interactions or surface states etc. Given by:

$$\varphi_B = \varphi_M - X + \Delta \qquad [2.21]$$

In the case of an n-type semiconductor where $\varphi_M > \varphi_S$, where φ_S is the work function of the semiconductor, we have a rectifying contact [6]. If $\Delta \rightarrow 0$ we approach the Mott-Schottky limit for charge carrier injection, and by choosing electrode materials with suitable work functions we can design devices with the more preferable ohmic electrode characteristics [75, 76]. In the case where $\varphi_M < \varphi_S$ an ohmic contact is formed, and we see a linear I/V relationship across the junction.

The effect of these material parameters can be seen in the device characteristics and we can extract a number of useful parameters in order to determine the quality of the interface, with an aim toward device optimisation. Contact resistance or parasitic series resistance R_C, can be determined using the transmission line method. This can be done by measuring the total channel resistance of a series of identical channel width transistors, but with differing channel lengths. For each device we can write the total resistance as:

$$R_T = \frac{\partial V_{DLin}}{\partial I_{DLin}} = R_{CH} + R_{CD} + R_{CS} \qquad [2.22]$$

Here $R_{CD} + R_{CS}$ are the drain and source contact resistances respectively and R_{CH} is the channel resistance per unit length. By plotting the values for R_T against channel length L, for different values of V_G we can determine the total contact resistance $R_{CD} + R_{CS}$, by extrapolation of a straight line fit, where the value is taken at the intercept at the y-axis.

2.3.5 Inverters

Beyond FPDs the next technological steps for oxide based semiconducting materials are in their application to ICs. ICs are the backbone of current electronic devices and are used in practically every electronic device available. The fundamental building blocks of integrated circuits are transistors, allowing the construction of inverters and other simple logic circuits. Inverters or NOT gates can be constructed using only two TFTs and take a single voltage level input and give an inverted voltage level on their output [7, 77]. They can be implemented using a variety of designs (Fig 2.13) utilising either a single unipolar semiconductor or by combining n-type and p-type semiconductors to create complimentary circuits. Unipolar inverters are more straightforward to fabricate but suffer from poorer noise margins and lower gains. Complimentary inverters are vastly superior performance wise, but at the cost of more complex fabrication methods.

Operation of unipolar inverts is straightforward. The TFTs are chosen so the load TFT, whose gate is tied to the positive supply rail, is permanently turned on (Fig 2.13(a)). With V_{IN}at 0V the drive TFT is effectively open circuit, therefore V_{OUT} is tied to V_{DD}. When V_{IN} is driven to V_{DD}, V_{OUT} is pulled to 0V as the drive TFT turns on. It is a requirement when designing such a circuit that the drive TFT has a significantly lower on resistance than that of the load TFT, essentially a wider channel

device, as the system overall is simply a potential divider. Complimentary inverters (Fig 2.13(b)) perform in a similar fashion, however, as V_{IN} is driven from rail to rail the two differing n or p-type TFTs are driven either hard on of hard off. This creates a much sharper inversion at the output, leading to much higher gain.

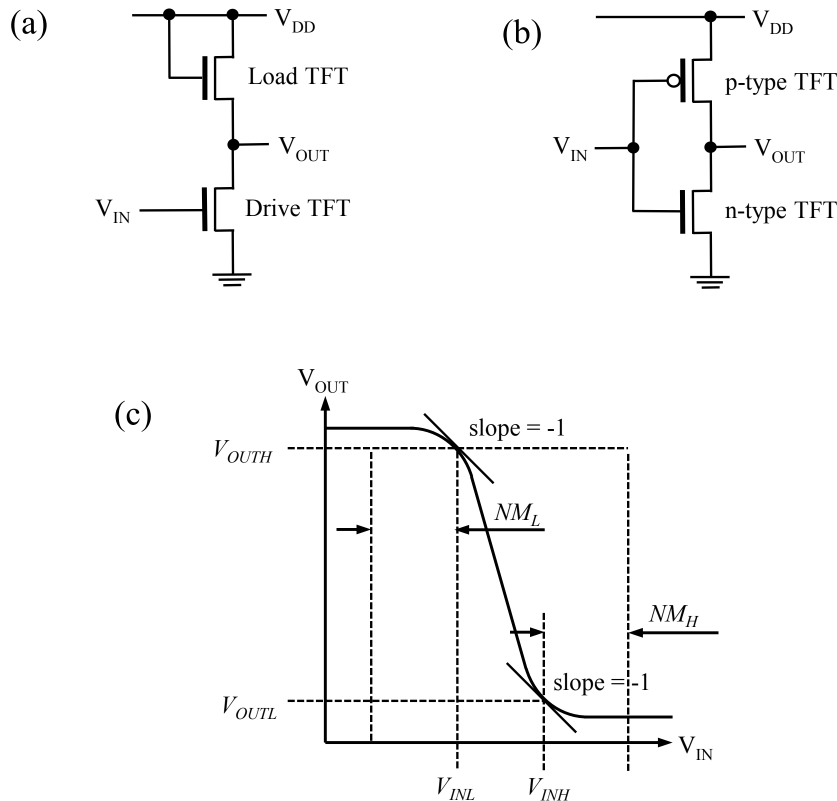

Figure 2.13: Inverter circuit schematic diagrams based on (a) unipolar TFTs and (b) complimentary n and p-type TFTs. (c) illustrating a voltage transfer curve for an inverter circuit and the relevant points used for calculation of noise margins.

In order to assess the performance of inverters we measure the voltage transfer curve plotting V_{IN} against V_{OUT}. By taking the slope of the transition range we arrive can find the inverter gain. Ideally the transition should appear as a step function, however in reality this is not the case and inverter noise margin is another metric by which performance is measured [78]. Noise margin for both the low and high input states are given as:

$$NM_L = V_{INL} - V_{OUTL} \text{ and } NM_H = V_{OUTH} - V_{INH} \qquad [2.23]$$

These margins are illustrated in Figure 2.12(c) and are calculated using the points beyond which gain becomes greater than unity. This is considered the threshold point at which we can have logic ‘1’. Therefore the larger the noise margins the better, as this translates to better signal propagation in more complex circuitry such as ring oscillators.

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Chapter 3

Metal-oxide based electronics in review

Abstract

This chapter discusses the recent progress in the field of metal oxide based electronics. Following a brief introduction, the earliest work on metal oxide TFTs is discussed, highlighting some of the most influential and recognised work. The work presented in this thesis is focussed toward the use of spray pyrolysis, a low cost solution processing deposition method, therefore a discussion on solution processed electron (n-type) and hole (p-type) transporting metal oxide based TFTs is presented, followed by a short review of the current status of complementary metal oxide electronics. Finally the chapter is rounded up with a short conclusion.

3.1 Introduction

Over the past ten years there has been a significant amount of progress in the field of metal-oxide based electronics. This class of materials, which has numerous uses as both active and passive components in the fabrication of electronic devices, is anticipated to be a key component in the realisation of a whole host of next generation consumer products. There are a several key characteristics that make materials such as zinc oxide (ZnO), tin oxide (SnO_2) and indium oxide (In_2O_3) well suited for use in a number of consumer electronic applications, such as flat panel displays (FPD), organic light emitting diodes (OLED), optical sensors/detectors and low cost microelectronics (Fig 3.1).

(a) (b)

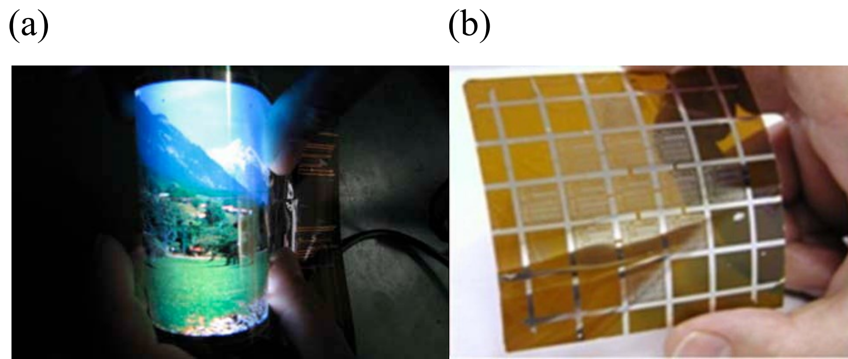

Figure 3.1: Practical demonstrations of (a) flexible oxide based flat panel display from Samsung Display [1] and (b) flexible high resolution microelectronics fabricated by Penn State University [2].

In most materials, optical transparency and electrical conductivity are properties considered to be mutually exclusive, yet in the case of some metal-oxides the two are combined. For a material to be transparent it must not absorb a photon with energy corresponding to the visible portion of the electromagnetic spectrum (380-750 nm). These materials, often referred to as transparent oxide semiconductors (TOSs) and transparent conducting oxides (TCOs), have a band gap greater than ~3.1 eV, corresponding to the transition from the visible to non-visible, ultra-violet (UV) portion of the electromagnetic spectrum at ~380 nm wavelength. Therefore they tend not to absorb photons of energies lower

than ~3.1 eV rendering them transparent and suitable for creating what have been termed as “invisible circuits”.

A second highly beneficial characteristic of oxide based semiconductors is their inherent high charge carrier mobilities, although this is only really the case with n-type metal oxide semiconductors. None the less the performance is typically orders of magnitude higher than that of amorphous silicon (a-Si), with values reported as high as 160 cm^2/Vs [3]. As discussed in chapter 2, the root cause of the high electron mobility of these materials lay in their electronic structure and is generally attributed to the nature of the metal (M) n*s* and oxygen (O) 2*p* orbitals that contribute to the conduction band minimum (CBM) and valence band maximum (VBM) respectively, giving rise to a highly dispersive CBM and a localising of the VBM.

An important aspect when considering the use of these materials is the ease with which they can be processed. Granted, their performance will never match that of crystalline silicon (c-Si) grown by the Czochralski process, but already the performance of metal oxide based transistors is similar to that of polycrystalline silicon (p-Si), with greater stability in terms of device performance, and can be deposited using very simple solution processing methods [4]. A small point to consider that is often overlooked, is the fact that many metal-oxide semiconductors can still be deposited using the more costly methods currently in use in the FPD production environment, therefore in principle the performance benefits of metal oxide materials can be realised quickly, whilst the lower cost manufacturing methods can be gradually integrated into current production lines.

3.2 Early development of metal oxide based electronics

Interest in the optical and electronic properties of metal oxide materials dates back quite some time, Badekar reported findings of a TCO in 1907 based on a thin film of cadmium oxide (CdO) [5]. The report showed that when cadmium is left to oxidise, the resulting thin film remains

conductive and is optically transparent. Typically TCOs offer good optical transparency (>80%) along with low resistivity ($<10^{-3}$ Ω cm) making them well suited to simple passive applications such as thin-film electrodes, and anti-static/conductive and optical coatings. For example tin doped indium oxide (ITO) has been recognised for some time as a high quality transparent electrode in flat panel displays and photovoltaic cells. However, its growing cost has led to increased research into alternatives based on impurity doped oxides of ZnO, In_2O_3 and SnO_2 as well as other new materials [6-9].

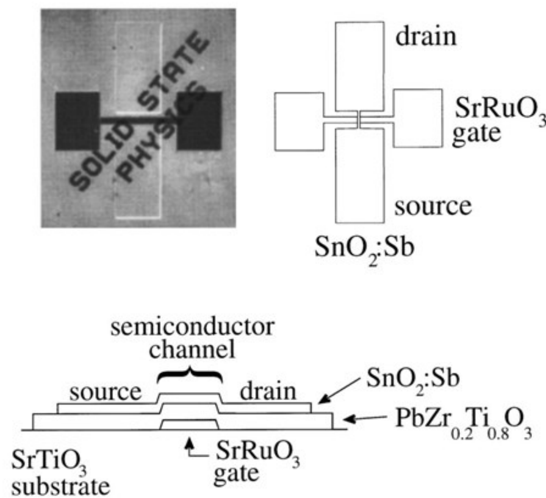

Figure 3.2: Photograph and structural layout of early all oxide SnO_2 TFT. Image taken from [10].

In terms of the practical application of metal-oxide materials in thin-film transistor (TFT) devices, it can be argued that the work of Prins *et al* in 1996 kick-started the recent upsurge in metal oxide TFT research (Fig 3.2). Their work, initially wishing to focus on the ferroelectric nature of SnO_2, demonstrated the operation of an entirely oxide based transparent TFT suggesting potentially good prospects in terms of device performance, alongside the possibility of a new generation of transparent electronics [10].

In 2001, Ohya *et al* published their findings demonstrating a ZnO based TFT fabricated using a novel solution processing deposition method [11]. Unfortunately the device performance was poor, and to

some extent they failed to convey the significance of their work. However, this was the first example of a solution processed ZnO TFT, and helped to illustrate the versatility and potential of ZnO based TFTs.

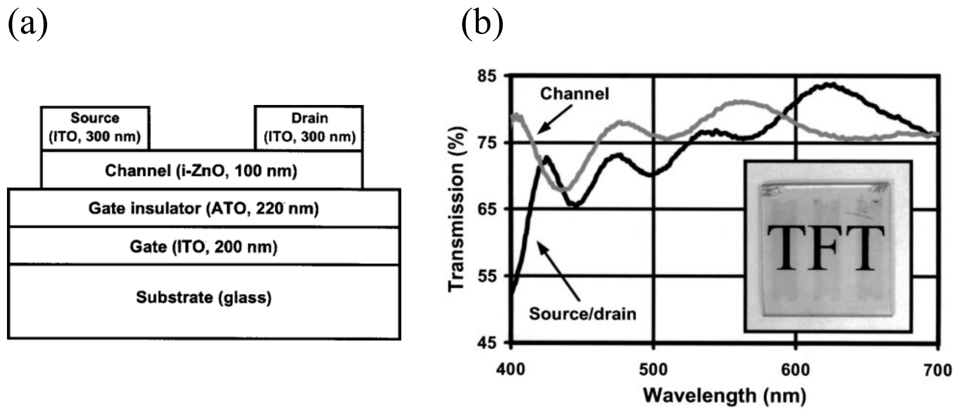

Figure 3.3: (a) Structural layout and (b) transmission data for entire film stack of an all oxide ZnO transparent TFT fabricated by Hoffman *et al* in 2003. Image taken from [12].

All of this work rekindled an interest in oxide based electronics, which by 2003 saw the beginning of a steady stream publications demonstrating ZnO based TFTs with performance levels that suggest metal-oxide semiconductors could easily replace a-Si, and possibly more. Hoffman *et al* were the first to publish their work on a transparent TFT fabricated on glass (Fig 3.3) [12]. Using ITO as the gate, source and drain electrodes, aluminium titanium oxide (ATO) as the dielectric layer, and a ZnO channel layer, these devices exhibited field effect mobilities between 0.3 to 2.5 cm^2/Vs, with $I_{D(on)}/I_{D(off)}$ ratios of ~10^7 and threshold voltages between 10-20 V. Optical transmission measurements showed approximately ~75% transmittance across the visible spectrum, including the glass substrate.

Publications by Masuda *et al* and Carcia *et al* followed almost immediately, both demonstrating their independent findings showing similar results [13, 14]. In each case device performance is similar with charge carrier mobilities between 0.1 and 2 cm^2/Vs. As with the work demonstrated by Hoffman, film deposition is generally performed using vacuum based techniques, such as sputtering, atomic layer deposition (ALD) or pulsed laser deposition (PLD). Similar device structures are

also used, utilising glass or silicon dioxide on silicon (SiO_2/Si) as substrates, with the transparent oxides forming the remaining TFT components.

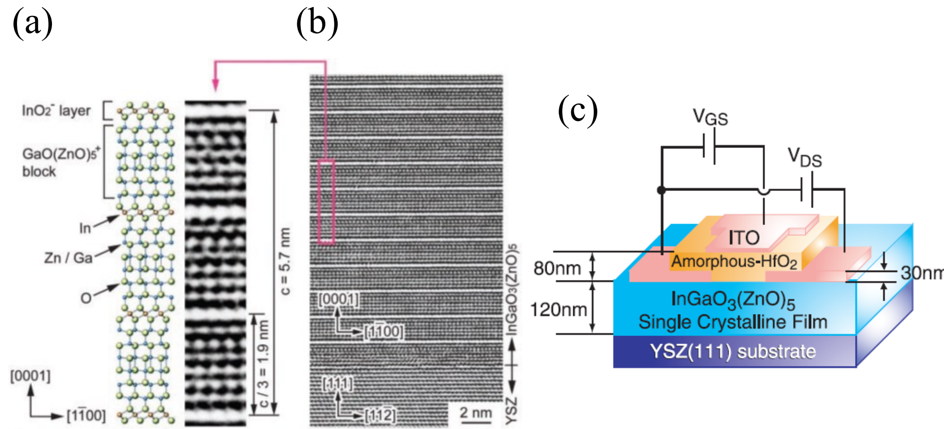

Figure 3.4: (a) Schematic of $InGaO_3(ZnO)_5$ crystal structure in reference to (b) cross-sectional HRTEM images of the InGaO3(ZnO)5 thin film grown on YSZ substrates. (c) Illustration of device structure. Images taken from [15].

These initial findings suggested great potential for metal oxide based devices, and in 2004 the work of Nomura *et al* really began to put metal-oxide based TFTs in the spotlight [15]. Their work on a single crystal $InGaO_3(ZnO)_5$ TFT demonstrated very high performance with a charge carrier mobility of ~80 cm^2/Vs, an $I_{D(on)}/I_{D(off)}$ of ~10^6 and a threshold voltages of 3 V. The device was fabricated using a somewhat complex super lattice semiconductor layer (Fig 3.4(a)) grown by PLD, and deposited onto an yttria-stabilized zirconia substrate. This was followed by the deposition of a hafnium oxide (HfO_2) gate dielectric and ITO gate, source and drain contacts (Fig 3.4(b)). Despite the excellent performance, the devices were difficult to fabricate and required high temperature annealing steps which aren't ideal when considering high throughput manufacturing. None the less, the work was still a significant breakthrough and certainly gained the attention of many people working in the field at the time.

J. F. Wager residing at Oregon State University took such an interest, publishing a short review article in Science in 2004 [16]. Having already been part of the team publishing the experimental results of

Hoffman *et al* in 2003, in the Science article he ponders the significance of firstly the future use of ZnO and secondly the findings of Nomura *et al*. Notably, he is one of the first to suggest some of the possible future applications of transparent electronics. In the review he discusses the possibility of a transparent display which, remarkably, has now been demonstrated in the form of a transparent display equipped notebook manufactured by Samsung Displays and utilising their latest AMOLED technology (Fig 3.5) [1]. A book by the same author later published in 2007 delves further into the realms of science fiction suggesting a further plethora of applications that may one day be realised [17].

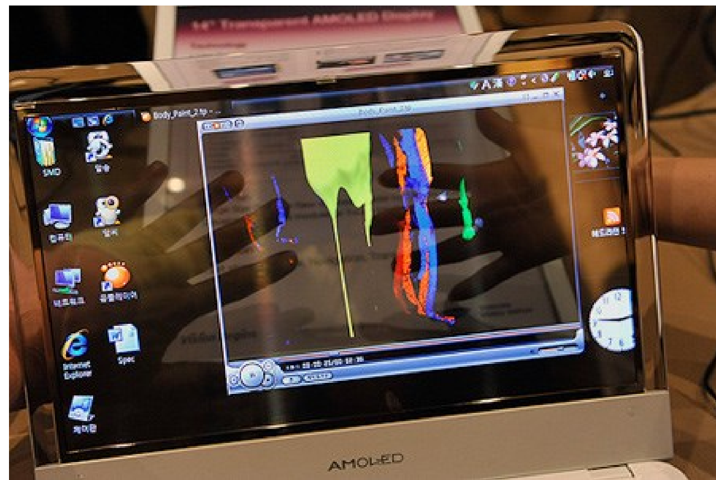

Figure 3.5: Samsung display showcase their transparent AMOLED display at the CES consumer electronics show. Image taken from [1].

Following on from this initial work, year by year there were an ever increasing number of reports illustrating the favourable characteristics and potential of ZnO based TFTs [18-21]. Research in the field began to diversify, with work becoming more focussed on specific areas that would need to be addressed before the metal-oxide materials would be suitable for commercial application. TFT stability was one area that gained a lot of attention [22-24]. High TFT switching rates in FPDs mean devices must be stable over prolonged periods of time and under significant bias stress conditions. Numerous studies suggest that ZnO based TFTs are likely to be stable for this application, and somewhat better than their competitor a-Si, whereas their threshold voltage stability

is also better than that of the higher performing p-Si or low temperature p-Si [4, 23-26]. As discussed in chapter 2 there have been several studies into the theoretical understanding of the electronic structure of ZnO as a semiconductor, and the related influence this has in terms of device performance [27, 28]. The influence of film stoichiometry and various intrinsic and extrinsic dopants have been discussed, yet there still seems to be some lack of agreement across the academic field on how to truly best describe the electronic makeup of ZnO, and particularly how we can relate this to device performance [29-34].

More recently there has been a shift toward research into low cost methods for the fabrication of metal-oxide based TFT devices, particularly methods that are well suited to large area deposition. As a-Si is now a mature and well established industry, if metal-oxide materials systems are to displace a-Si they will need to be cheap as well as offering high performance. To this extent much of the work in this thesis has been focussed on the use of solution processing methods that mostly avoid the high costs associated with vacuum based deposition techniques.

3.3 Solution processed n-type metal oxides

The bulk of the work presented in this thesis is centred on the use of spray pyrolysis (SP) as a deposition method. This straightforward low cost deposition method provides excellent results, and is currently the best deposition method available when requiring high performance ZnO based TFTs by solution deposition [35].

Presently, state-of-the-art metal-oxide based TFTs, processed by conventional deposition methods, offer electron mobilities of up to somewhere in the region of 160 cm^2/Vs. It's therefore wholly feasible that metal-oxide TFT technology is approaching performance levels good enough for many current as well as emerging applications [3]. Naturally the next step is to develop low cost processing methodologies, for both discrete TFTs and integrated circuits, which can be implemented without

compromising the high level of performance currently seen with metal-oxide devices [4, 36].

Semiconductors	Deposition methods	Ref.
ZnO	SC, IJ, SP	[11, 37, 38]
ZTO	SC, IJ	[39, 40]
IZO	SC	[41]
IZTO	SC, IJ	[42, 43]
IGZO	SC, DC, IJ	[44-46]
ZnO-np	SC	[47]
ZnO-nw	SC	[48]
Dielectrics	**Deposition methods**	**Ref.**
HfO_2	SC, SG	[49, 50]
ZrO_2	SC, SP	[35, 49]
Y_2O_3	SG, SP	[51, 52]
Al_2O_3	SG, SP	[52, 53]
Conductors	**Deposition methods**	**Ref.**
ITO	SC, SP	[54, 55]
ZnO:In	SP	[56]
FTO	SP	[55]

Key to material abbreviations: ZTO = zinc tin oxide, IZO = indium zinc oxide, IZTO = indium zinc tin oxide, IGZO = indium gallium zinc oxide, ITO = indium tin oxide, FTO = fluorine-doped tin oxide.

Key to deposition method abbreviations: SC = Spin coating, IJ = Ink jet printing, SP = Spray Pyrolysis, SG = Sol-gel deposition.

Table 3.1: Solution deposition methods for commonly used metal oxides, including semiconductors, dielectrics and conductors

A number of well-established processing methods are now available for solution based deposition of metal-oxide thin-films, all of which have various benefits as well as drawbacks. Table 3.1 illustrates some of the commonly deposited materials with some commonly associated solution processing deposition methods. It's worth noting the solution processing is not only restricted to the deposition of semiconductors, it is quite possible to fabricate each of the required device components utilising some form of solution processing.

Solution deposition typically involves taking a precursor material and creating an oxide thin-film via some kind of chemical conversion process, and it's this step that is identified as one of the biggest challenges for solution processed metal-oxide materials. It's often the case that deposition combined with chemical conversion requires some

amount of energy, and typically this involves high-temperature processing techniques, such as in the case of SP. We are therefore often limited to using substrate materials that are able to handle such temperatures. Conversely, there are now a number of methods available whereby the conversion from precursor to oxide can be made via low temperature methods, however, there is typically a trade-off here, where device performance is generally poorer due to the lower quality of the resulting films [54, 57]. In an ideal world we would like to be able to deposit high quality semiconducting films at low temperatures whilst using simple scalable processing techniques and low cost materials.

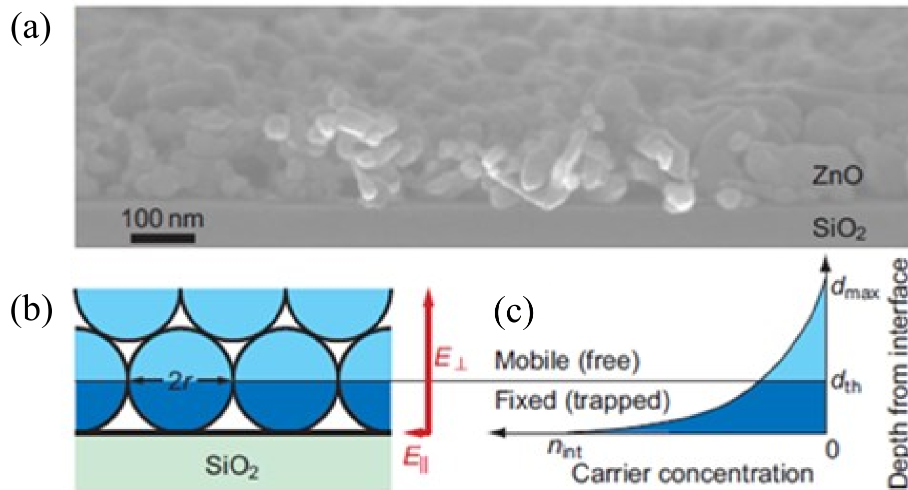

Figure 3.6: (a) Cross-sectional scanning electron microscope image of a nanoparticulate ZnO film formed by spin-coating. (b) Geometrical model of interface and (c) carrier concentration as a function of depth from interface used for numerical analysis. Image from [58].

Spin coating is arguably the most commonly used method for solution deposition of metal-oxide semiconductors [11, 59-61]. Its simplicity allows researchers to quickly deposit films, but is somewhat limited in scalability particularly toward large arrays of TFTs such as required by FPDs. For the sake of simplicity, we can divide spin-coating deposition into two fundamental categories, nanoparticle-based and precursor-based. The latter has generally been shown to provide the best results, due mainly to the *in situ* nature of the conversion process creating

much better quality films. Addressing the nanoparticle approach first, using metal-oxide nanoparticles does offer an interesting approach as no conversion of precursor material(s) is required, leaving the quality of the nanoparticles and the deposition method as the main determining factors affecting the overall device performance [58]. Nanoparticle based devices often struggle to perform as well as their non-nanoparticle counterparts. Poor device performance is often attributed to voids within the nano-particulate film and high semiconductor/interface roughness determined mainly by the particle size and how well they are dispersed prior to deposition (Fig. 3.6).

The voids and increased roughness create charge carrier traps, leading to poor current flow through the device. Okamura *et al* have done some simple numerical modelling in an attempt to understand this, and suggested even very small changes in the interface roughness of only a few nanometres, can affect device mobility by up to an order of magnitude [58]. The same group also went some way in corroborating their findings by experimenting with the concentration levels of the capping ligand used. They find that increasing the ligand concentration leads to smaller-sized nanoparticle agglomerates and in turn smoother films. These films therefore see improved mobilities, validating their hypothesis. As stated, nanoparticle-based oxide TFTs show poor performance characteristics, particularly when deposited at lower plastic substrate compatible temperatures, with the charge carrier mobility rarely seen to be greater than 1 cm^2/Vs [58, 62].

Moving on to more conventional spin coating methods, work by Hwang *et al* demonstrates a typical example of how this straightforward precursor based method can produce good results through the deposition of a-IGZO films [63]. The process involves the preparation of metal salt precursor sol-gel solutions with the required metal ion composition. The solutions are deposited using a spin coater and dried at 150 °C before being annealed at temperatures between 300 and 600 °C. In this particular work, device $I_{D(on)}/I_{D(off)}$ ratios of the order of 10^7 are achieved with a maximum electron mobility of ~6 cm^2/Vs. This work

focuses on the dependence of annealing temperature on device performance. However, these values are quite typical for devices fabricated in this fashion using conventional gate dielectrics. Numerous variations of this fabrication approach exist with slightly differing processing parameters [64, 65]. However, the common factor is the need for high temperature annealing, which is typically higher than 300 °C.

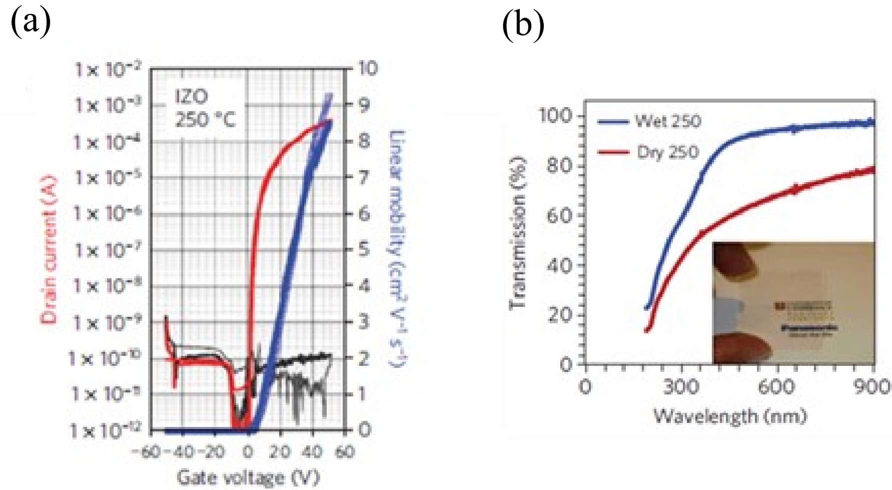

Figure 3.7: (a) Transfer curve of hydrolysed IZO TFT. (b) Optical transmission spectra of hydrolysed and dry-annealed IZO films annealed at 250 °C on spectrosil glass. Inset shows a photograph of a transparent, hydrolysed IZO film. Image from [41]

In 2010 Banger *et al* demonstrated an interesting low-temperature processing method [41]. Referred to as 'sol-gel on chip' hydrolysis, the process makes use of organic-inorganic alkoxide-based precursors that upon exposure to water, undergo reactions consisting of hydrolysis and condensation by nucleophilic substitution/addition mechanisms. This in turn leads to well-formed metal-oxide thin-films of ~20 nm thickness. Deposited onto SiO_2/Si substrates for TFT fabrication (Fig. 3.7), the precursor solutions are deposited by spin coating in an inert environment, followed by an aqueous hydrolysis annealing step performed in an ambient environment. Without hydrolysis (i.e., by dry annealing) the decomposition temperature of the precursors are high at 350 °C and beyond, depending on the precursor used. Once the hydrolysis step is introduced, there is a significant downward shift in the annealing

temperature required to form high quality metal oxide films. Devices fabricated at temperatures as low as 230 °C using this method exhibit electron mobilities of ~7 cm^2/Vs along with very good bias stability and high $I_{D(on)}/I_{D(off)}$ ratio of the order of 10^7.

More recently, Kim *et al* published their findings in which they have been able to demonstrate the growth of a number of different metal-oxide thin-films at temperatures as low as 200 °C and on plastic substrates [54]. Using a self-energy generating combustion chemistry technique, the films are formed by an *in situ* conversion process, with a processing cycle similar to the previously discussed 'sol-gel on chip' method. The process utilises acetylacetonate or urea as the fuel source and metal-nitrates as oxidisers which are all prepared in solution and deposited by spin coating. This is followed by annealing steps at a minimum of 200 °C in order to achieve working active devices. This redox-based combustion process is initiated at lower temperatures leading to an exothermic reaction generating local temperatures high enough to convert the precursors into the required oxides, and sufficiently eliminating any residual organic impurities. A number of different metal oxide thin-films were demonstrated including In_2O_3, a-ZTO, a-IZO and ITO. Utilising plastic substrates and applying a maximum anneal temperature of 200 °C, they were able to fabricate devices with electron mobility of ~6 cm^2/Vs. The $I_{D(on)}/I_{D(off)}$ ratio is relatively low on the order of 10^3. However, using more conventional Si substrates combined with aluminium oxide dielectrics, the authors are able to demonstrate improved device performance with charge carrier mobilities of ~39.5 cm^2/Vs and $I_{D(on)}/I_{D(off)}$ ratios on the order of 10^5, with only a minimal increase in processing temperature (250 °C).

Spray pyrolysis, the method discussed in this thesis, is another simple and inexpensive deposition method that utilises soluble metal-oxide precursors such as acetates and acetylacetonates [38]. The work discussed in the following chapters hopefully demonstrates the potential and versatility of this method to good effect, where the deposition of high quality semiconducting films as well as high-k dielectric thin-films is

demonstrated [35, 66-68]. With SP, a thin-film is deposited by spraying an aerosol of a precursor solution onto a heated substrate. Working devices are obtainable at substrate temperatures as low as 200°C although high-quality films need higher processing temperatures (350-400°C) [38, 69] (Fig 3.8). An advantage of this deposition technique is that only small quantities of precursor solutions are required to grow films over relatively large areas. Likewise, spray pyrolysis offers the ability to blend different precursor solutions prior to deposition, allowing effective doping and/or creation of multi component oxide films [66].

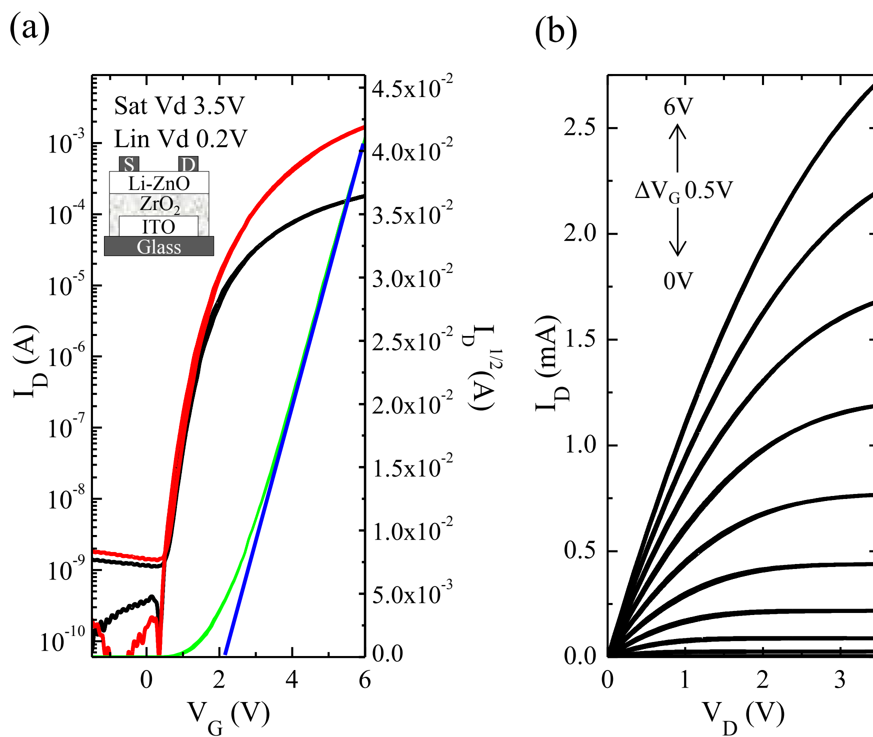

Figure 3.8: (a) Transfer and (b) output characteristics of a staggered bottom gate transistor (see inset) utilising a ZrO_2 dielectric and Li-ZnO semiconductor layer both deposited by spray pyrolysis.

Utilising SP it has been possible to demonstrate impressive ZnO based TFT device performance with low voltage operation and charge carrier mobility as high as ~85 cm^2/Vs with $I_{D(on)}/I_{D(off)}$ ratios on the order of 10^7 [35].

In a similar effort to develop inexpensive and scalable deposition techniques, Kim *et al* have developed an interesting photo-annealing

method capable of forming high quality films of IGZO, IZO and In_2O_3 at room temperature, although some unintentional heating (~150 °C) of the substrate is seen due to the photo radiation [57]. Initially starting with a sol-gel precursor solution preparation from typical acetate/nitrate based precursors, they proceed to deposit the solutions by spin coating (Fig 3.9).

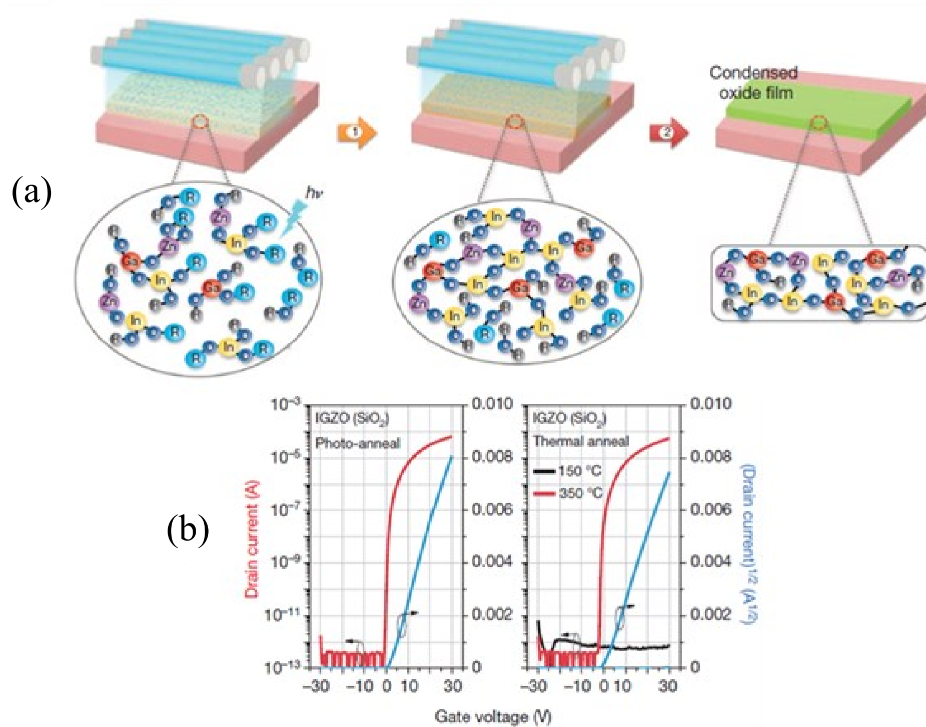

Figure 3.9: (a) Condensation mechanism of metal oxide precursors by DUV irradiation. Light-blue shading denotes illumination from the low-pressure mercury lamp and (b) Transfer curves of photo-annealed and thermally annealed (150 and 350°C) IGZO TFTs fabricated on SiO_2 (200nm)/Si wafers. Images taken from [57].

The deposited films are then subjected to deep ultraviolet radiation (DUV) using a mercury lamp with peak emission wavelengths of ~184.9 nm (10%) and ~253.7 nm (90%) under a nitrogen environment. The authors claim that under DUV radiation, photochemical cleavage of the alkoxy groups is promoted, which in turn triggers the metal and oxygen atoms to form M–O–M networks. Film densification is compared to that of high temperature annealed IGZO by comparison of areal density utilising Rutherford backscattering spectrometry, high-resolution transmission electron microscopy and spectroscopic ellipsometry, and is

found to show very similar characteristics. Using this method the group have been able to demonstrate oxide TFTs with electron mobility as high as 7 cm^2/Vs for devices fabricated on alumina dielectric and polymer substrates. They were also able to demonstrate seven-stage ring oscillators operating at 340 kHz with a 210 ns stage delay.

All of the work discussed here represents the current state-of-the-art in terms of solution processed electron transporting oxides with a particular emphasis on low temperature deposition methods. With the current level of research intensity into this area, we may soon see some of the more peculiar applications suggested by Wager *et al* become a reality.

3.4 Solution processed p-type metal oxides

Development of p-type metal oxide based TFTs using traditionally n-type oxides such as ZnO, In_2O_3, and SnO_2, has proven to be extremely difficult and it now appears that the best general strategy is to simply try and identify different material systems that are better suited to hole transport [28]. A great deal of work is currently still focusing on improving the performance of known p-type oxide semiconductors in the hope of achieving similar characteristics to that of their n-type counterparts. As such, more traditional vacuum based deposition methods are still used, and a move toward low cost solution-based processing methods is still proving to be slow, although some progress has been made recently [70].

At present, Cu_2O and SnO are the two materials that show most promise for p-type TFTs. Cuprous oxide (Cu_2O) was one of the first materials to be studied for its semiconducting properties [71-73]. In 1997 Kawazoe *et al* reported their method for modification of the energy band structure at the VBM [73]. By introducing metal cations with a closed valence shell and energy levels close to the O *2p* VBM, a hybridised orbital occurs at the VBM, in turn decreasing the localisation of holes. Their work demonstrates the use of $CuAlO_2$ as a p-type semiconductor

with Hall hole mobility's of 10.4 cm^2/Vs, and more recently it has been shown that under carefully controlled growth conditions, highly crystalline Cu_2O can show Hall hole mobility of up to 256 cm^2/Vs. [74]

In terms of Cu_2O TFTs, there are really only a handful of demonstrations to date, beginning with the work reported by Matsuzaki *et al* in 2008 [75]. Generally, almost all Cu_2O TFTs have been fabricated by either sputtering or PLD, and show poor charge carrier mobility, typically lower than 1 cm^2/Vs [75-77]. Work performed by Zou *et al* is one exception to this rule, where they were able to produce high quality epitaxial Cu_2O films on high-k HfO_2 dielectrics by PLD at substrate temperatures of 500-700 °C, in turn allowing them to obtain better device performance, with mobilities of up to 4.3 cm^2/Vs and $I_{D(on)}/I_{D(off)}$ ratios on the order of 10^6 (Fig. 3.10) [78, 79].

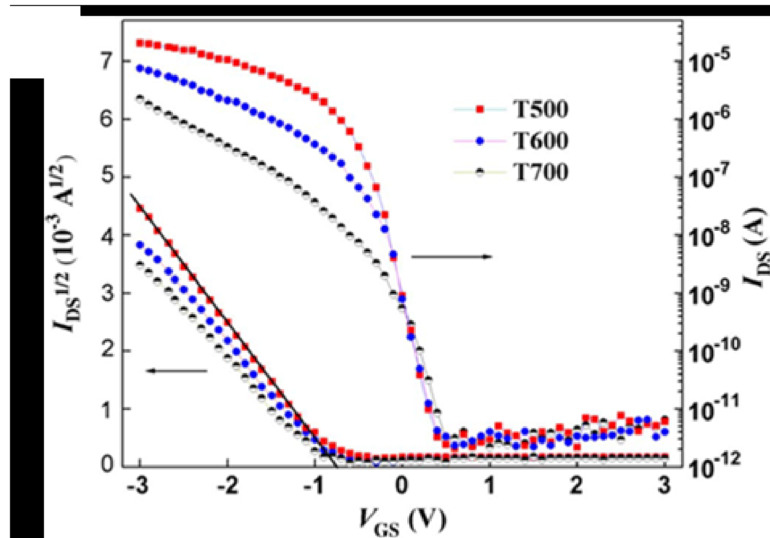

Figure 3.10: Transfer characteristics of best Cu_2O TFT to date. Device shows clear field-effect. Labels correspond to the deposition temperature. Taken from [79].

The work of Sohn *et al* is one example of Cu_2O TFTs produced from RF-sputtering at room temperature. They demonstrate an improvement in device performance by promoting crystal growth and suppressing carrier concentration, through annealing under vacuum at high temperatures of ~500 °C [80]. Unfortunately, the performance is

still poor with charge carrier mobility still only of the order of 0.07 cm^2/Vs.

In terms of solution processed Cu_2O TFTs, Pattanasattayavong *et al* have recently succeeded in demonstrating working Cu_2O devices deposited using the SP process [81]. The deposition is based on the conversion of Cu(II) acetate into Cu(I) oxide with glucose acting as a reducing agent [82]. The performance suffers from high trap density, similar to that seen in many other Cu_2O based TFTs, showing charge carrier mobilities between 0.001 and 0.01 cm^2/Vs and $I_{D(on)}/I_{D(off)}$ ratios of only 10^3. Nevertheless, these numbers are not far behind those of Cu_2O TFTs fabricated from physical deposition processes, suggesting there is still potential for solution deposition techniques.

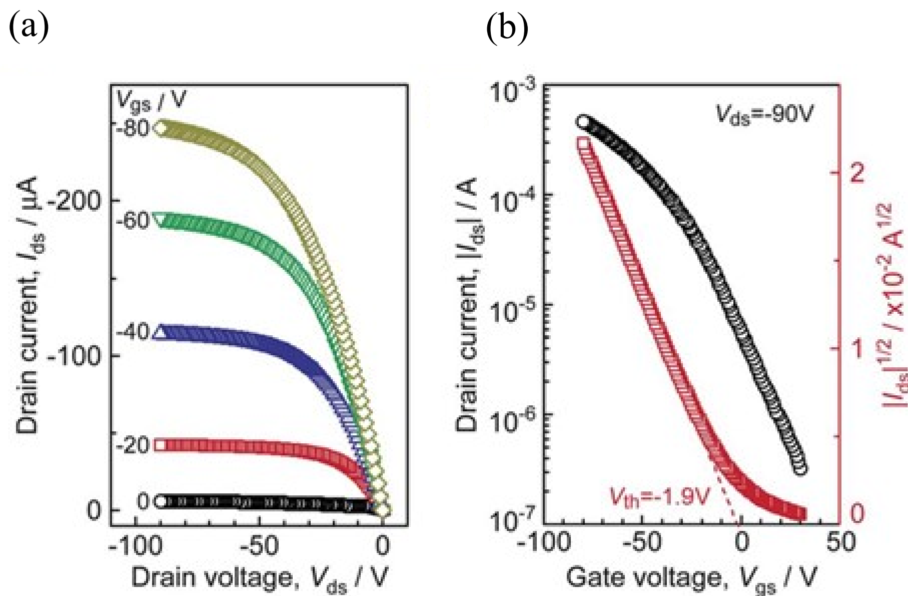

Figure 3.11: (a) Output and (b) transfer characteristics of solution-processed SnO TFT. Image from [70].

As previously stated, a number of tin (Sn) oxides have also recently gained interest as possible p-type materials. The multivalent nature of the Sn ion means both types of naturally occurring tin oxides, namely stannous oxide (SnO) and stannic oxide (SnO_2), remain stable under ambient conditions [83]. Reports of p-type TFTs typically identify the channel material as SnO [84-87], although there have been a number

of studies that claim their TFT channel material is actually p-type SnO_2 [88, 89].

Several studies on general SnO_x TFTs fabricated using various non-solution based deposition processes have been reported, with the majority showing charge carrier mobilities close to or above 1 cm^2/Vs, suggesting SnO might be a more promising candidate than Cu_2O. To date the highest TFT mobility of 4.6 cm^2/Vs comes from work reported by Fortunato *et al* [90]. Solution-processing of SnO has been shown to be possible in the recent work by Okamura *et al* [70]. Their work discusses the fabrication of p-type SnO TFTs from a solution of $SnCl_2 \cdot 2H_2O$ in methanol, spin-coated on Si/SiO_2 substrates in an inert nitrogen atmosphere. This was followed by NH_4OH exposure and annealing at 450-500°C. The best performing device yields a charge carrier mobility of 0.13 cm^2/Vs and with an $I_{D(on)}/I_{D(off)}$ channel current ratio of 10^5 (Fig 3.11).

3.5 Complementary metal oxide circuits

If we are to look beyond FPDs and basic unipolar circuitry, the next technological challenge for metal oxide based semiconducting materials are in their application within integrated circuits (IC). As already stated, cheap disposable electronics would be one of the major target applications for metal oxide based semiconductors, but if high performance complimentary technologies can be developed then there’s no reason why these materials cannot be used in more demanding application areas.

Inverters (NOT gates) are the most straightforward example of device integration, as they can be constructed using only two TFTs. Their function is to take a single voltage level input and give an inverted voltage level on their output. Unipolar inverters and circuits have been demonstrated by numerous people and are straightforward to fabricate but suffer from poorer noise margins and lower small signal gains. Complementary technology will be required to if we want to build the

high speed, low noise circuits needed for applications such as RFID tags and smart sensors etc. Clearly, before we can achieve this we will need to develop better p-type metal-oxide materials with performance characteristics closer to that of their n-type counterparts. Yet with only the few p-type oxides currently available, it has still been possible to demonstrate complementary circuits based on metal oxide materials.

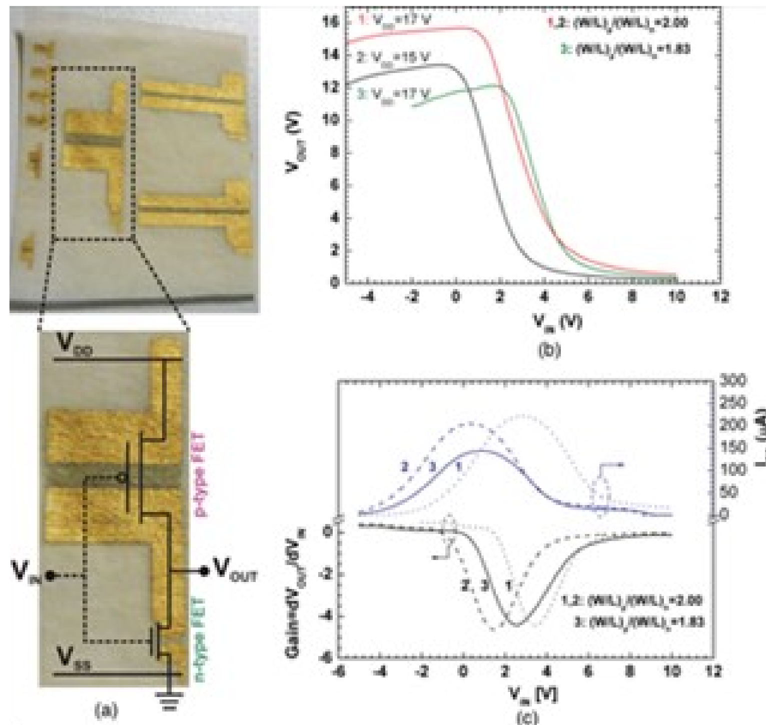

Figure 3.12: (left) Images of complementary oxide logic gate on a paper substrate with SnO_x as a p-FET and Ga-In-Zn-O as an n-FET and (right) Voltage transfer and gain characteristics for same device. Image from [91].

Following their first report on p-type TFTs based on SnO_2, Ou *et al* were able to combine their p-type TFTs with n-type In_2O_3 to obtain the first all-oxide complementary logic gates [88, 89]. Another interesting and noteworthy demonstration of metal oxide based complimentary electronics is the work of Martins *et al*, who were able to demonstrate a number of remarkable metal-oxide based voltage inverters. The remarkable aspect being they were able to fabricate the inverters on paper (Fig 3.12) using SnO_x and indium gallium zinc oxide (IGZO) as the p-type and n-type materials, respectively [91]. In an attempt to

simplify inverter fabrication, Nomura *et al* demonstrated the first ever use of air-stable ambipolar SnO TFTs to fabricate complementary-like inverters with promising operating characteristics (Fig 3.13) [92]. The devices were fabricated by PLD with relatively low substrate temperatures of 250 °C.

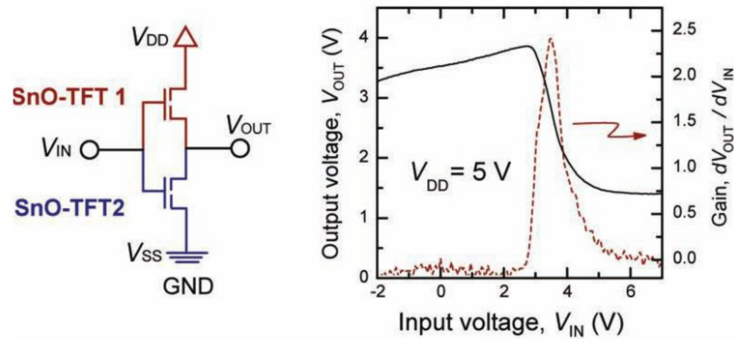

Figure 3.13: (a) Diagram of inverter circuit composed of two SnO ambipolar TFTs and (b) inverter characteristics showing output response (left axis) and gain (right axis) Image from [92].

In terms of performance these complementary circuits are some way behind their silicon counterparts, however, these recent studies do go some way in demonstrating the potential of metal-oxide based TFT technology for use in numerous applications in the field of large area microelectronics.

3.6 Conclusions

The work discussed here doesn't quite encompass all the work currently being carried out in the field of metal-oxide based electronics, but it hopefully covers most of the major developments of the last 10 years, and with something of a focus toward the challenges for low cost solution processing methods. The great progress of the last 10 years suggests there is much more to come for metal-oxide based TFTs, particularly when we consider the potential next generation of novel applications such as transparent displays.

Generally speaking, the display market seems to be the most likely application area for metal-oxide based TFTs, and with LG and Samsung having already demonstrated prototype full colour AMOLED displays using IGZO based TFTs [93]. It's also worth remembering that low cost disposable electronics such as RFID tags, smart labels and tags are currently another key application area for oxide based electronics, particularly having seen the recent demonstration of inverters deposited on paper.

Presently, there are still a number of issues that metal oxide-based electronics will have to overcome; particularly the high number of structural defects associated the low temperature processing methods used in most solution processing methods. Nonetheless, they are now beginning to offer performance compatible with a number of consumer technology requirements, and with their unique properties such as optical transparency, it seems quite reasonable to expect that metal-oxide electronics are likely to become a significant contributor to future technology developments.

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Chapter 4

Experimental methods

Abstract

This chapter will outline the experimental methods and techniques used during the work presented in this thesis. The primary focus of the work is in the enhancement of ZnO based thin-film transistor performance, whilst optimising the flexibility of spray pyrolysis as the deposition technique. This chapter discusses the methods and techniques that are used to fabricate devices, and also how material properties are examined in conjunction with electrical characterisation to enable a better understanding of how we can further optimise the fabrication of high performance metal-oxide TFTs.

4.1 Device fabrication techniques

This section introduces the various materials, methods, and techniques that were used during the fabrication of thin-film transistor (TFT) and metal-insulator-metal (MIM) capacitors. The focus of the work in this thesis is on the fabrication of devices utilising solution processing methods i.e. spray pyrolysis (SP), alongside more commonplace fabrication techniques such as thermal evaporation and acid etching and patterning. A number of differing device architectures are utilised, and are explained in detail.

4.1.1 Oxide thin film deposition by spray pyrolysis

Throughout this work oxide thin films have been deposited using a spray SP, a simple and cheap deposition method utilising solution based precursors. By spraying an aerosol of a precursor solution onto a heated substrate, an oxide thin film is formed on the substrate surface as the precursor decomposes under the influence of the high surface temperature. There are numerous benefits to this deposition method, for example only very small quantities of precursor solutions are needed to form films suitable for the fabrication of TFTs (typically less than 5 µl of precursor solution per cm^2 is required to deposit a ZnO TFT active layer).

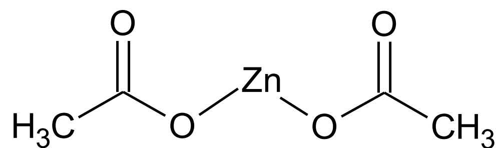

Figure 4.1: Zinc acetate structure, the precursor material used as the basis for most ZnO work, used with methanol (linear formula: CH_3OH) as a solvent.

Another important benefit of SP is the ability to blend different precursor solutions prior to deposition, allowing effective doping and/or creation of multi component oxide film. Probably the biggest benefit of

this deposition method is the potential for considerably lower manufacturing overheads when compared to that of much more complex vacuum based deposition methods.

Typically, the precursor solutions are prepared by dissolving precursor acetates in alcohol based solvents. Solvent choice varies depending on the precursor material used, but for a typical deposition of ZnO, a 0.1M solution of zinc acetate (linear formula: $(CH_3OO)_2Zn$) (Fig 4.1) in methanol (linear formula: CH_3OH) would be used. Some other precursor materials used for the deposition of dielectric materials appeared to be slightly more soluble in ethanol, otherwise the majority of the work was done using methanol as the main solvent.

Many of the potential nitrate based precursors are highly soluble in 2-methoxyethanol, which is also miscible with methanol and would be well suited for use when blending of the precursor solutions is needed. However, the quality of the deposited films was always significantly worse than those deposited using acetates combined with methanol as the precursor material. Specifically the device performance is always poor and the films exhibit a high degree of optical scattering, therefore the combination of acetates and methanol became the preferred choice of precursor materials.

Solutions are prepared in vials, having been thoroughly cleaned using acetone and isopropyl alcohol, and dried using compressed nitrogen. The solutions are sonicated and stirred for 30 minutes to ensure the precursor materials are fully dissolved. If blending of multiple precursor solutions is the objective, the solutions are prepared separately then mixed at a later stage according to the required ratios. The ratio of the different precursor solutions will be specific to the experimental design, but will typically be based on low-level molar ratios of the metal ions (discussed in detail in Chapter 6).

For the deposition of thin films an ultrasonic spray pyrolysis (SP) system employed (Fig 4.2). The system is fully automated utilising an ultrasonic spray nozzle attached to a programmable servo system giving variable x, y and z positioning control, combined with a custom built substrate hotplate, with temperature capabilities up to 500 °C. The

precursor solution is fed to the spray head from a syringe based, screw feed system at a constant rate, where it is then atomised by the ultrasonic spray head. The subsequent aerosol is then shaped and directed toward the substrate by a shaping nozzle fed by compressed nitrogen.

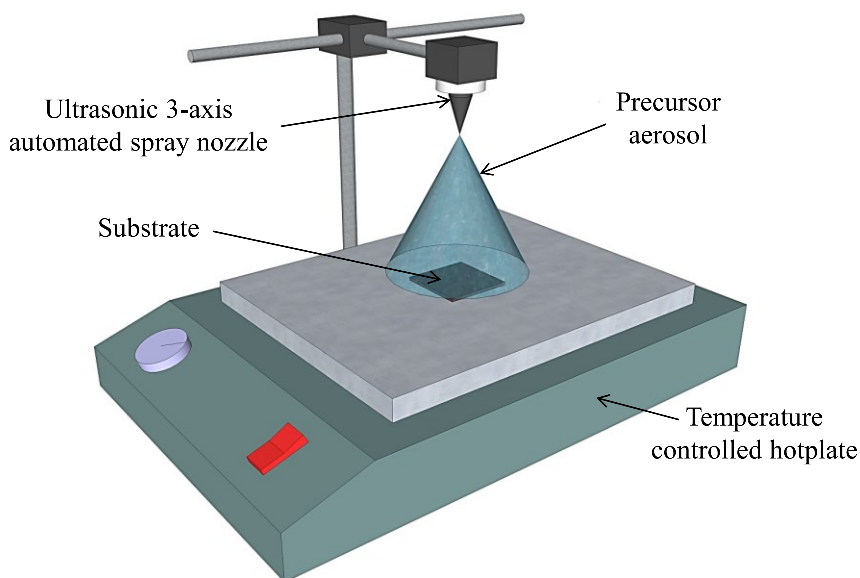

Figure 4.2: Schematic diagram illustrating spray pyrolysis system for deposition of thin oxide films. The system is controlled by a desktop computer and the deposition occurs in an isolated spraying chamber.

The size of the atomised droplet is dependent on the operating frequency of the nozzle and the viscosity of the precursor solution. For the deposition of ZnO alone, the hotplate is normally heated to temperatures upward of 250°C with higher temperatures resulting in better quality films. Typically a substrate is placed onto the hotplate and left to reach thermal equilibrium before being sprayed with the precursor aerosol. The spraying process consists of the nozzle following a raster pattern across a large portion of the hotplate area, encompassing any substrates by at least 30 mm. The spot size at the substrate is ~14 mm in diameter with each raster overlapping ~2 mm. Each deposition is followed by 120 second interruption to allow the precursor aerosol to decompose and form an oxide layer on the surface of the substrate. The

cycle is repeated until films of the required thickness are achieved. After the final deposition the substrates are left for a further 120 seconds before being removed and left to cool in ambient. A typical feed rate for the solution would be on the order of 1.5 um/min.

Spray pyrolysis can also be performed using non automated methods, and without the use of an ultrasonic nozzle. Most often a simple artist airbrush is used. Droplet size is controlled by the size of the regulating valve opening and is normally fixed on any individual device. Non-ultrasonic spraying devices typically require a minimum of 1.3 bar of pressure to atomise the precursor solution properly, which can sometimes be disadvantageous, particularly the cooling effect of high gas pressures on the substrates are of concern. Sonicating nozzles require very little gas pressure to shape and direct the aerosol spray, so offer a much wider degree of flexibility.

4.1.2 Substrate preparation

In order to fabricate TFTs a number of different substrate and dielectric material combinations are employed. The most commonly used substrates are based on heavily doped Si^{++} wafers utilising a thermally grown 400 nm layer SiO_2 for the gate dielectric (Fig 4.3(a)). The active material, such as ZnO, is deposited on top of the SiO_2 by SP followed by thermal evaporation of metal source and drain contacts. This yields what is commonly referred to as a staggered bottom-gate structure.

When investigating TFTs utilising spray pyrolysed dielectrics, indium tin oxide (ITO) coated glass substrates can be used. Usually an alkaline-earth boro-aluminosilicate float glass, on top of which would normally be a ~140 nm thin-film ITO with a sheet resistance of ~14 Ω/sq. The ITO is used to provide a gate contact on top of which a dielectric layer can be deposited by SP (Fig 4.3(b)). Typically the ITO is patterned to minimise unnecessary overlap with the parallel semiconductor plane and contacts in an attempt to decrease current leakage through the gate dielectric, as well as minimise any stray

capacitance. Again this method of fabrication yields a staggered bottom-gate device structure.

Bottom-gate coplanar architecture devices are fabricated utilising pre-patterned substrates using photolithographically defined gold contacts on top of a thermally grown 200 nm SiO_2 dielectric (Fig 4.3(c)). Using gold as a contact material is not optimal for performance when considering ZnO based devices, this is discussed in more detail in chapter 5. However, having pre-patterned substrates does allow for quick assessment of material properties and device characteristics, which is the primary reason for their use. Similarly pre-patterned substrates are used for the fabrication of circuits such as inverters, albeit comprised of a slightly more complicated structure and using poly-silicon rather than gold as the contact material.

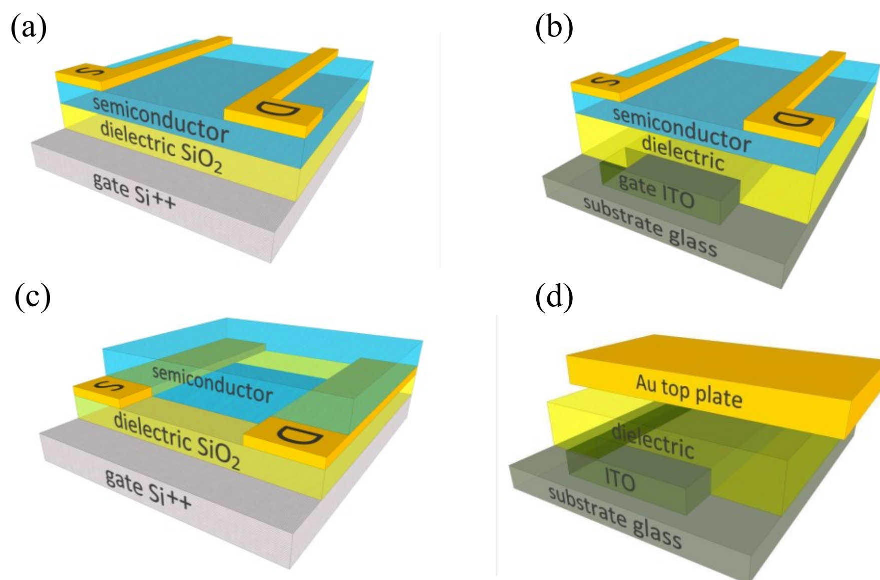

Figure 4.3: (a) schematic of bottom gate-top contact device architecture (b) bottom gate-top contact architecture based on patterned ITO gate and sprayed dielectric (c) bottom gate-bottom contact device architecture and (d) metal-insulator-metal structure used for the measurement of capacitance properties of dielectrics.

To facilitate the testing of the dielectric properties of the spray pyrolysed gate dielectrics, metal-insulator-metal (MIM) diodes were

fabricated (Fig 4.3(d)). A simple structure, where a substrate consisting of pre-patterned ITO on glass has a dielectric layer deposited across its entire area. This is followed by the thermal evaporation of the top contact using a specially designed mask that matches the bottom pattern of the ITO, giving contacts, or plates, that have specific areas of overlap. This allows the correct calculation of the geometric capacitance, which is needed for the extraction of accurate charge carrier mobilities.

Pre-deposition preparation involves thorough cleaning of the substrates by submerging them into a bath of acetone, which is then placed into a sonicator for fifteen minutes. The substrates were dried with compressed nitrogen, and the procedure is repeated using isopropyl alcohol to ensure thorough cleaning. A final UV-ozone plasma treatment step is also used if needed.

4.1.3 Deposition of contacts

Device electrodes are deposited quickly with a high degree of accuracy using a thermal evaporation system (Fig 4.4). Typically aluminium is used as a contact material due to its favourable work function, best suited to electron injection into the conduction band of ZnO, however, other metals and organic materials can also be deposited using the system if required. Thermal evaporation is used only for the fabrication of staggered bottom-gate TFTs and MIM structures (Fig 4.3 (a), (b) and (d) respectively), as the coplanar and IC substrates arrive pre-patterned from the supplier.

The deposition begins by placing a substrate in a holder on top of a mask. The holder is then inserted into the top of the chamber. The source boat is filled with the required raw material and the chamber is then pumped down to a vacuum of $\sim 10^{-6}$ mbar. Once the chamber is pumped down to vacuum, the source crucible is steadily heated to a temperature where the contact material is known to evaporate at a steady rate. The source shutter opens and the evaporation is then monitored for a few minutes in order to check the deposition rate and to allow any

impurities to evaporate. The substrate shutter then opens allowing the deposition to occur for a set time depending on the required contact thickness, typically between 30 nm and 60 nm. Once the required thickness level is achieved the substrate shutter is shut and the crucible is kept on until the remaining material is evaporated. After a cooling period the chamber is vented and the substrates are removed.

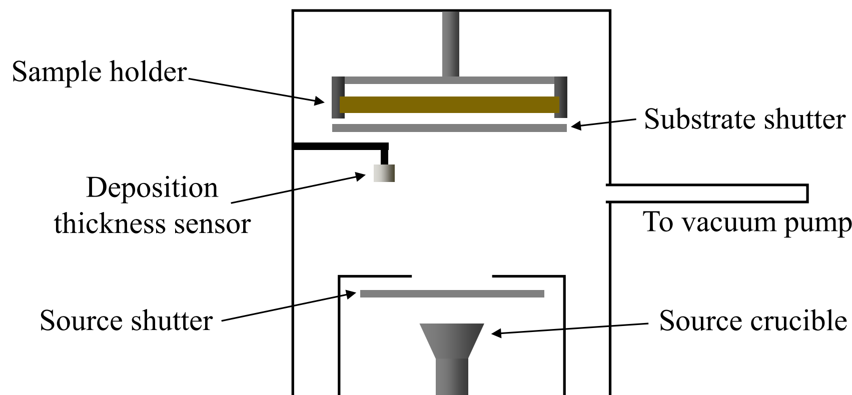

Figure 4.4: Schematic representation of evaporation system used to deposit metallic contacts/thin films.

4.2 Electrical and material characterisation

This section discusses the various characterisation techniques utilised in the analysis of the oxide materials and devices used within this thesis. The methods used can be split into two primary areas consisting of electrical characterisation methods such as currant-voltage measurements and capacitance spectroscopy, and materials characterisation techniques including atomic force microscopy (AFM), X-ray diffraction (XRD) experiments and optical measurements.

4.2.1 Current-voltage measurements

Typically TFT device performance is evaluated by analysis of experimentally acquired current-voltage measurements (Fig 4.5). Using

this data we can extract the parameters discussed in chapter 2.3.3. To take the required measurements a Keithley 4200-SCS semiconductor parameter analyser (SPA) is used in combination with a probe station. The probe station may be under vacuum, in an inert environment or an ambient environment depending on the requirements of the materials/device being tested. The device under test is placed on a chuck in the probe station and contact is made by use of fine needles as to allow for an accurate and good quality contact. The system is modular with a number of built in source-measurement units (SMU), which allow simultaneous and precise, control and measurement of current and voltage. Current-voltage measurements at each of the terminals are recorded and saved into a spread sheet file, whilst software on the SPA also allows for in-situ parameter extraction if the user requires.

For the measurement of ICs, the same system can be used, but utilising added SMUs depending on the circuit type. The entire system is modular and additional oscilloscopes and lock-in amplifiers can easily be added if required.

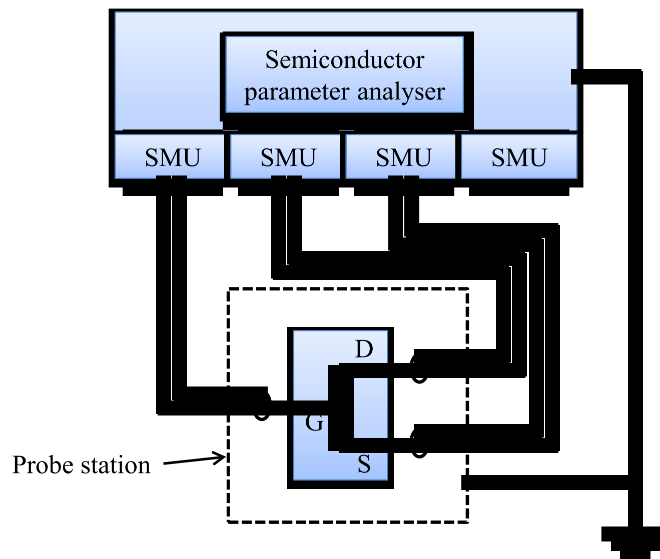

Figure 4.5: Schematic representation of electrical measurement apparatus. The numerous SMUs can be configured individually to measure current, voltage, capacitance and other parameters where required.

4.2.2 Capacitance spectroscopy

For accurate extraction of parameters such as charge carrier mobility, the gate capacitance per unit area, C_G, must be known of the device under test. If the dielectric thickness and permittivity is known then the geometric capacitance can be calculated. However, if devices are fabricated utilising a non-standard dielectric materials it is beneficial to first fabricate MIM capacitors in order to determine the geometric capacitance experimentally rather than by calculation. Once again this can be measured using the Keithley 4200-SCS SPA, using the internal capacitance analyser, and using only two of the SMUs (Fig 4.5). The system can measure capacitance values in the range of femtofarads (fF) to nanofarads (nF) across a frequency range of 1 kHz to 10 MHz. To make a measurement the probes are connected to the overlapping contacts of known size, on either side of the dielectric under investigation. A small ac voltage applied across the contacts and the voltage and current values are measured. From the phase and amplitude change of the current with respect to the applied voltage we are able to determine the real and imaginary part of the capacitor impedance ($Z = R + jX$). We are able to extract the capacitance values based on the following relationship:

$$C = \frac{1}{2\pi f X} \qquad [4.1]$$

The geometrical capacitance is calculated by dividing the total measured capacitance by the contact area overlap. It is often useful to apply a dc offset during the measurement, particularly if measuring a bilayer material. For example in a metal-insulator-semiconductor (MIS) device, by applying a bias, we can fill the semiconducting layer with carriers so it can be considered as a conductive contact, rather than a semiconducting layer that could affect measurement result.

4.2.3 UV-Visible spectroscopy

As transparency is one of the key concerns in oxide based TFTs, it is important to be able measure and quantify their optical properties. The optical absorption of these films can be found using an Ultraviolet-Visible (UV-Vis) spectrometer. A monochromatic beam of light is passed through the sample and a reference at the same time and the intensity of the transmitted light is measured and plotted as a percentage. Essentially the system is a transmission spectrometer.

UV-Vis spectroscopy is useful for not only examining the transparency of thin films, but also allows determination of the materials optical band gap. All measurements presented in this thesis were carried out using a Shimadzu 2550 spectrometer in dual beam mode.

4.2.4 X-ray diffraction

Thin-films deposited by SP are typically polycrystalline in nature. Therefore, analysis of their crystalline structure can give an insight and help explain the origin of certain observations seen during the electrical characterisation of TFTs. XRD methods allow the analysis of the crystalline structure of the materials under investigation by analysing the pattern of the diffracted incident beam on the sample.

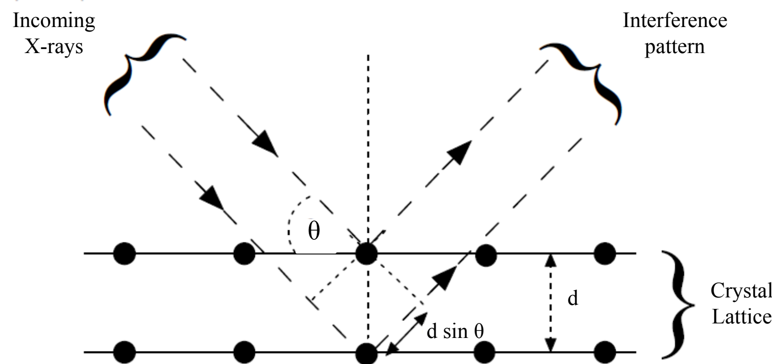

Figure 4.6: Bragg diffraction leading to constructive interference caused by diffraction that satisfies the conditions of Bragg's law i.e. the incident X-ray wavelength must equal *n* times the $2d\sin\theta$.

Using this method it is possible to extract a number of parameters about the material structure, including the average spacing between rows of atoms, d, the orientation of the crystal structure, and also the average size of the crystalline grains. An X-ray source typically Cu, emits high energy K-α radiation whose wavelength is on the order of the atomic spacing of crystalline materials. The sample is placed in the beam across a range of angles on the material under investigation. The resultant diffraction patterns can be analysed, where the constructive interference leads to intensity peaks corresponding to angles of diffraction whereby Bragg's law is met (Fig 4.6):

$$n \cdot \lambda = 2d \cdot \sin\theta \qquad [4.2]$$

Here, d, is the plane distance determined from the angular distribution of the minima and maxima of the incoming and outgoing radiation. As no crystal is perfect there will be some broadening of the diffraction peak caused by crystal domain orientation and size, and lattice spacing irregularity. When analysing X-ray diffraction patterns, the Scherrer formula relates the peak width at half maximum, B_W, to the average size of the crystallite domains, τ:

$$\tau = \frac{K\lambda}{B_W \cos\theta} \qquad [4.3]$$

Where, K, is a dimensionless shape factor and, λ, is the x-ray wavelength. It should be noted that this method of calculation is limited to the nanoscale crystallite scale, and there are a number of factors, instrumental and material specific that can contribute to peak broadening. For the work under discussion here, XRD measurements were carried out using a Phillips 1050/25 diffractometer.

4.2.5 Atomic force microscopy

Atomic force microscopy (AFM) is a surface analysis technique used to determine surface roughness and to understand the surface morphology at the nanoscale level. It is a technique that allows us to build a three dimensional image of the surface under investigation allowing further detailed analysis. AFM is typically used to acquire topography images using an atomically sharp tip at the end of a cantilever arm, the tips are used to probe the surface of the material under investigation to allow the extraction of data such as surface roughness. The cantilever is controlled by a piezoelectric actuator in combination with a laser/photo-detector feedback loop, the laser being reflected off the back of the tip (Fig 4.7).

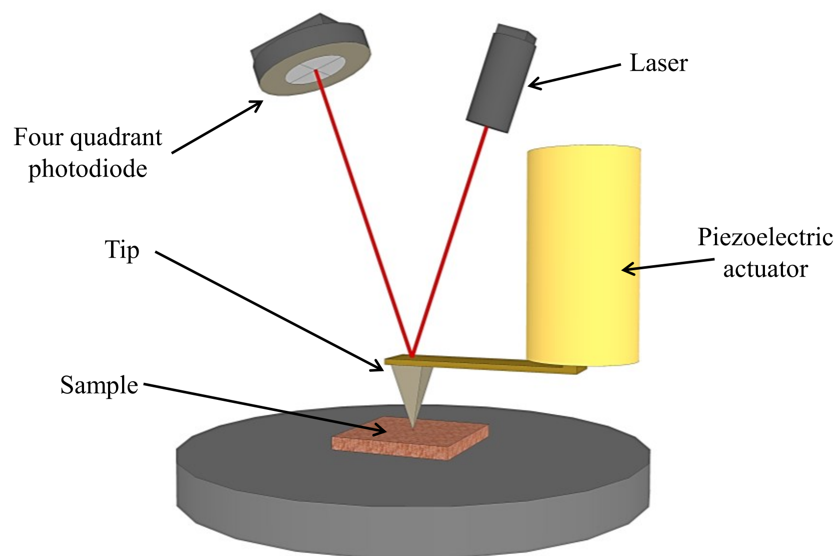

Figure 4.7: Schematic of AFM system. The four quadrant photodiode measures the tip deflection providing feedback for the control system. The piezoelectric actuator then keeps the tip at a predetermined set point, whilst the images are derived from the drive signals applied to the actuator.

For imaging the two most commonly used measurement techniques are contact mode and tapping mode. In contact mode the tip is in permanent contact with the surface to be measured. The tip is brought down into contact with the surface until a set level of deflection is reached. The tip is then scanned across the surface and the topography

image is then constructed from the applied drive signal required to maintain a constant deflection. In tapping mode the tip is oscillated near to its resonant frequency. The tip is scanned across the surface whilst the feedback system tries to maintain the tip at constant amplitude. The topography image is constructed from applied the drive voltage, required to maintain a stable amplitude of oscillation. Measurements were made using either a Veeco Dimension 3100 SPM or an Agilent 5420 AFM system, both capable of scanning areas in the region of 90 μm^2.

4.2.6 Thermal analysis techniques

A number of thermal methods are available for the analysis of the precursor materials that we use during the deposition process.

Thermo gravimetric analysis (TGA) of the precursor materials gives some insight into the temperatures required to successfully decompose the precursor materials during the deposition process. By monitoring the mass change of the material under investigation as a function of increasing temperature, we are able to see how the material decomposes, for example a small mass loss at ~100°C indicates the onset of dehydration. This technique is useful also to investigate the materials decomposition behaviour under different environments as well as determining the thermal stability of materials. For results shown in this work TGA measurements were carried out using a TA instruments Q500e at a scan rate of 10°C/min.

Differential scanning calorimetry (DSC) is a technique used to measure the amount of heat that is absorbed or released by a sample as a function of temperature, for example during phase transitions. DSC works by measuring the difference between the heat required to increase the temperature of a sample and reference material. Typically the reference will be some inert material such as alumina. The resulting plot shows heat flow as a function of temperature and is recorded under a nitrogen atmosphere at rate change of 10°C/min. For results shown in this work the measurements were carried out using a Mettler Toledo

DSC822 system, using precursor quantities of 15mg contained in aluminium crucibles.

Chapter 5

High performance oxide thin-film films by spray pyrolysis

Abstract

Metal-oxide semiconductors have now become some of the most intensely researched materials when considering high performance, low cost, solution deposited electronics. This chapter introduces spray pyrolysis (SP) as a simple and cost effective method for depositing high performance metal-oxide semiconductors. Thin films are deposited and investigated using a number material and electronic characterisation techniques. Through a combination of atomic force microscopy (AFM), X-ray diffraction (XRD) techniques, UV-Vis spectroscopy, and through the fabrication of differing architecture thin-film transistors (TFTs), an understanding of the specific qualities of zinc oxide films grown by SP is acquired. From this data it has been possible to optimise ZnO based device performance, as well as deposit for the first time, solution processed gallium oxide (Ga_2O_3) TFTs. To this end, high performance thin-film transistors based on ZnO are demonstrated, with charge carrier mobilites in excess of 20 cm^2/Vs, whilst Ga_2O_3 devices with charge carrier mobilities of the order of 0.5 cm^2/Vs are also demonstrated.

5.1 Introduction

The current thirst for electronic goods at increasingly lower cost is clearly driving research into metal-oxide based electronics, as well as a number of other areas within the consumer electronics sector. At the same time, speculation as to how we can take advantage emerging novel materials to create interesting and new products also maintains elevated interest from the general public and any others concerned. The prospect of consumer electronics with interesting properties such as transparency and flexibility is slowly becoming a reality, where only fifteen years ago these ideas would have been confined to the realms of science fiction [1].

For some time now there has been a substantial level of focus on organic materials and semiconductors for their electronic properties and their suitability toward low cost manufacturing methods as well as their other interesting properties such as flexibility. They have been used in a range of applications including solar cells, transistors, organic light emitting diodes (OLED) and even integrated circuits (IC) [2]. Yet, despite all these achievements, (OLEDs aside), they are yet to break though into mainstream production due to a number of obstacles. Poor environmental stability is one factor which has slowed progress for organic electronics. However, one of the biggest issues at present is still the inherent lack of high performance when devices such as transistors are considered. Transistors are in essence the building blocks of electronics, and if performance is poor then this has to be overcome before we can go any further.

Metal-oxides are a class of materials that have gained much interest over the last ten or so years, due mainly to their inherent stability and high performance. The requirements of some upcoming technologies necessitate the use high performance materials with properties not currently available from organic and silicon based technologies. The primary benefit of metal-oxide semiconductors over organic and amorphous silicon technologies is their significantly higher charge carrier mobilities, suitable for the needs of the next generation of current driven OLED backplane technologies. Currently the flat panel display (FPD)

industry relies largely on amorphous silicon as the active material used in liquid crystal display (LCD) TFT backplanes [3]. The implementation of OLED based FPDs are only achievable if low mobility amorphous silicon can be replaced with a material with relatively high charge carrier mobility, satisfying the higher current drive requirements of OLEDs. To this end, ZnO based semiconductors offer some of the best possible solutions.

OLED screen technology is probably the most immediately clear application area for ZnO TFTs, however there are numerous other applications that although not currently on the brink of delivery, are fundamentally well suited to metal oxides, indeed many of these applications/ideas have grown out of some of the unique properties that metal-oxides possess. The most often discussed is the use of metal-oxides in transparent electronics [4-6]. These large band gap semiconductors have been suggested as suitable for applications such as transparent displays, smart windows, etc. Transparent materials such as conductors (ITO, FTO), are already well established in the electronics industry [7], therefore high performance transparent semiconductors remains one of the final areas for development.

The deposition methods currently in use in the electronics industry and also in the research environment are based mostly around costly vacuum deposition techniques. The work presented in this chapter aims to illustrate how a simple and straightforward deposition method such as SP can offer a viable alternative to more complex methods currently in place. Typically thin films are deposited using a number of methods that can be divided into two categories, namely chemical and physical deposition methods. Examples of chemical deposition methods include plasma enhanced chemical vapour deposition (PECVD) and atomic layer deposition (ALD) [8-11], whereas physical deposition methods include sputtering and pulsed laser deposition techniques (PLD) [12-17] etc. All of these methods are costly and complex, in contrast to SP which is a very low cost and simple deposition method [18-20].

5.2 Zinc oxide thin-film transistors by spray pyrolysis

Primarily it has been the aim of this work to optimise the use of spray pyrolysed ZnO thin-film semiconductors for TFT applications. As such, and due to the nature and ease with which SP can be used to fabricate devices, it was typically the case that following an initial experimental design, fabrication and testing of devices was the first procedure conducted in order to test any hypothesis. If the results were found to be favourable, then further experiments and analysis were carried out from both a materials and electronic perspective.

In terms of preparation, films were sprayed onto a number of different substrates simultaneously. Films were prepared by spraying four coats with the spray nozzle at a rate of 1.5 ml/min, with a two minute gap between each pass. After the final coat was deposited the films were left on the hot plate for a further two minutes allowing the final deposition to fully convert. Finally the films were lifted off the hotplate and left to cool in ambient. For transistor fabrication, films were deposited on SiO_2 (400 nm dielectric) on Si, followed by thermal evaporation of source and drain contacts (staggered), and also on a thinner SiO_2 (200 nm) dielectric with pre-patterned source and drain contacts (co-planar). β-phase quartz and glass substrates were used for the deposition of films used for UV-Vis spectroscopy and XRD respectively. AFM was performed on the films used for transistor measurements, and measurements were taken at points from within the transistor channels as well as outside of the channels. During the deposition process, spraying masks are used to isolate the deposition to as small an area as possible. This was done to minimise the gate current leakage that can occur when the semiconductor deposition encroaches around the substrate edge.

5.2.1 Precursor materials

Zinc acetate is the principal chemical compound used for the preparation of precursor solvents used for the deposition of ZnO (Fig 5.1). Zinc nitrates along with several other compounds were examined; however the

resultant films were of poor quality, usually optically and electronically. Thermal analysis of zinc acetate was carried out using thermo gravimetric analysis (TGA), alongside differential scanning calorimetry (DSC) (Fig 5.2). Examining the TGA data a small mass loss can be observed at ~100°C, this first stage of degradation is attributed to the loss of any adsorbed or inter-crystalline water molecules. The second stage of degradation beginning at a low rate at ~150°C is attributed to the loss of any volatile impurities followed by the breakdown of the interlayer structure of the zinc acetate, in turn releasing numerous products including acetic acid, acetone, and carbon dioxide. At ~200 °C a clear sharpening of the loss rate can be seen, leading to a peak loss rate around 300 °C, suggesting the final stage of decomposition where the acetate groups are lost and decomposition of the precursor is complete leading to polycrystalline ZnO. This is confirmed by differential scanning calorimetry, suggesting the complete decomposition of the precursor by 350 °C [21-23].

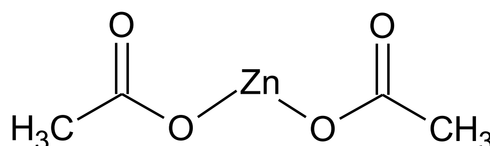

Figure 5.1: Chemical structure of zinc acetate used for the preparation of precursor solution. Liner formula: $(CH_3CO_2)_2Zn$.

Solvents trialled for the deposition of ZnO included water, anhydrous methanol, ethanol, and isopropyl alcohol. Isopropyl alcohol suffered from solubility issues, whereas methanol, ethanol and water worked successfully as solvents. Films deposited using water as the solvent performed less favourably, showing non-uniformity of film thickness with a tendency for the film thickness to increase toward the spraying mask edge. Together with this was an increase in observable optical scattering and poor device performance. When using methanol and ethanol as solvents there was no appreciable difference between the

optical and electronic performance of either films, however methanol (linear formula: CH_3OH) was deemed as the favourable solvent due to its lower cost per unit volume of equivalent assay.

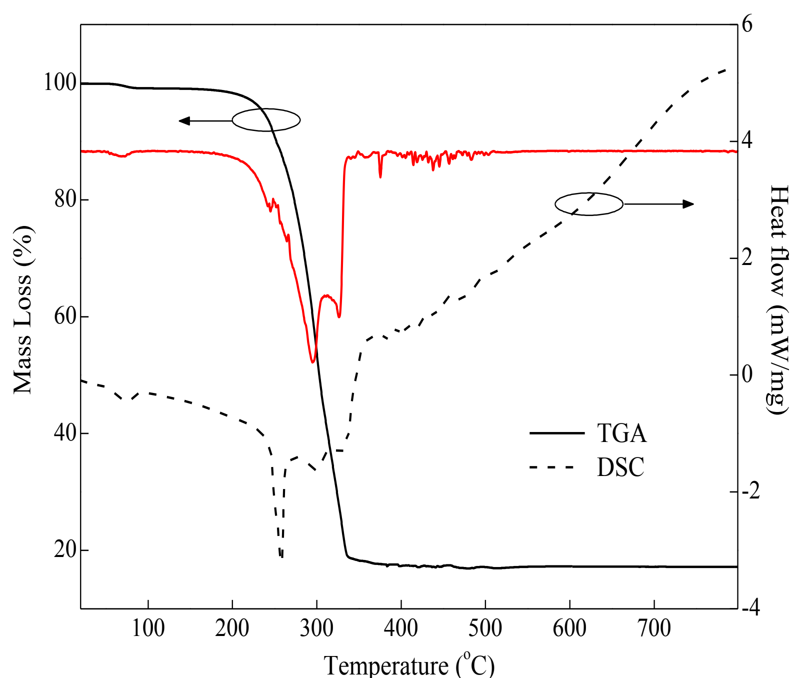

Figure 5.2: Thermogravimetric analysis of zinc acetate de-hydrate (left axis) including rate loss (red line), and differential scanning calorimetry (right axis). Measurement was carried out using 15 mg of material and at a scan rate of 10 °C/min. TGA and DSC measurements were carried out in an air and nitrogen environments respectively.

5.2.2 Optical properties of ZnO thin-films

The optical properties of ZnO films were investigated using UV-Vis spectroscopy (Fig 5.3). The properties of films deposited at increasing temperatures were investigated, as well as the properties of films deposited to differing thicknesses through adjustment of the deposition rate. In order to find the optimum deposition temperature for zinc acetate, films were deposited across a range of temperatures from room temperature to a maximum of 500 °C. Film thickness (where films had formed) was estimated to be approximately 20 nm by spectroscopic reflectometry (SR). At room temperature the precursor material appears to agglomerate unevenly on the substrate surface as slow evaporation of the solvent takes place, in turn no features are seen across the

transmission spectra that would indicate the presence of zinc oxide. Following an increase in deposition temperature to 100 °C a clear absorption onset can be seen to develop around 350 nm. In this instance the solvent appears to have evaporated quicker or possibly before contact with the substrate, helping the precursor disperse across the substrate more evenly, considering the TGA analysis it is unlikely that the precursor has decomposed and formed ZnO, therefore the absorption is likely due to the zinc acetate precursor only. Once a substrate temperature of 200 °C is reached, a strong absorption onset is observed at ~400 nm, becoming more prevalent with increasing substrate temperature. The increased sharpening of the exitonic feature at 370 nm is indicative of increasingly better quality films with higher deposition temperatures.

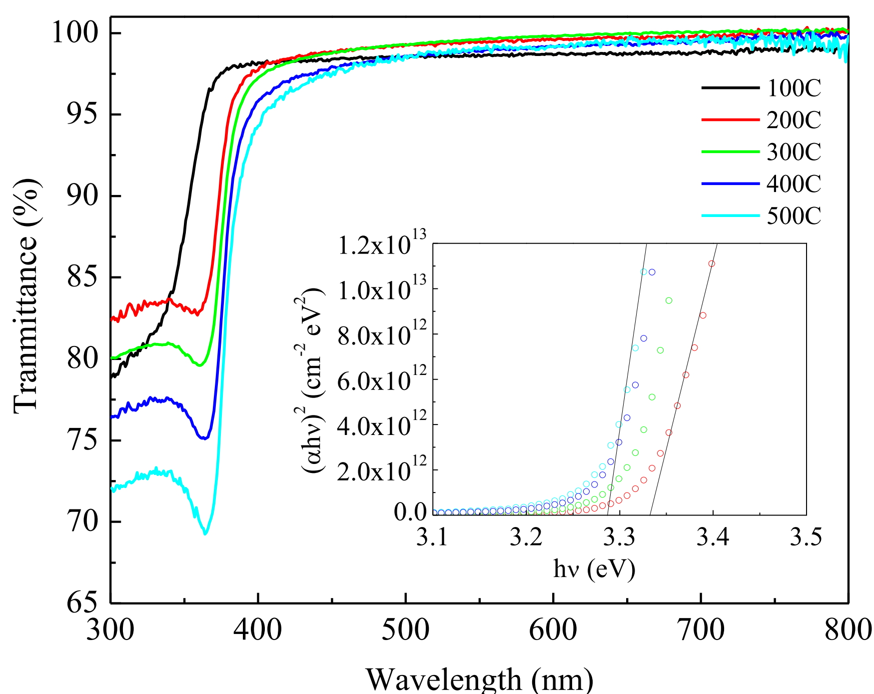

Figure 5.3: Optical transmittance of ZnO films (~25 nm) deposited by spray pyrolysis across a range of temperatures on β-phase quartz substrates and (inset) optical bandgap extracted using Tauc plots showing modification with increasing temperature.

A decrease can be seen in the extracted optical bandgap, corresponding with increasing temperature, with the highest value

estimated as 3.5 eV at 100 °C (not shown). This evolution, seen with other deposition methods also, is often attributed to a mixed phase composition of films deposited at lower temperatures where amorphous and nano-crystalline regions lead to quantum confinement. As deposition temperatures increase so do the crystalline/grain sizes seeing a shift in bandgap toward a final value of 3.28 eV [24-26].

Films were also investigated by UV-Vis concerning the effect of film thickness (Fig 5.4). One method used to achieve this was to change the feed rate of the precursor solution to the spray nozzle. Feed rates of 1000, 1500, 2000 and 2500 μl/min were used. Film thicknesses were measured using SR, and deposition was performed at 500 °C.

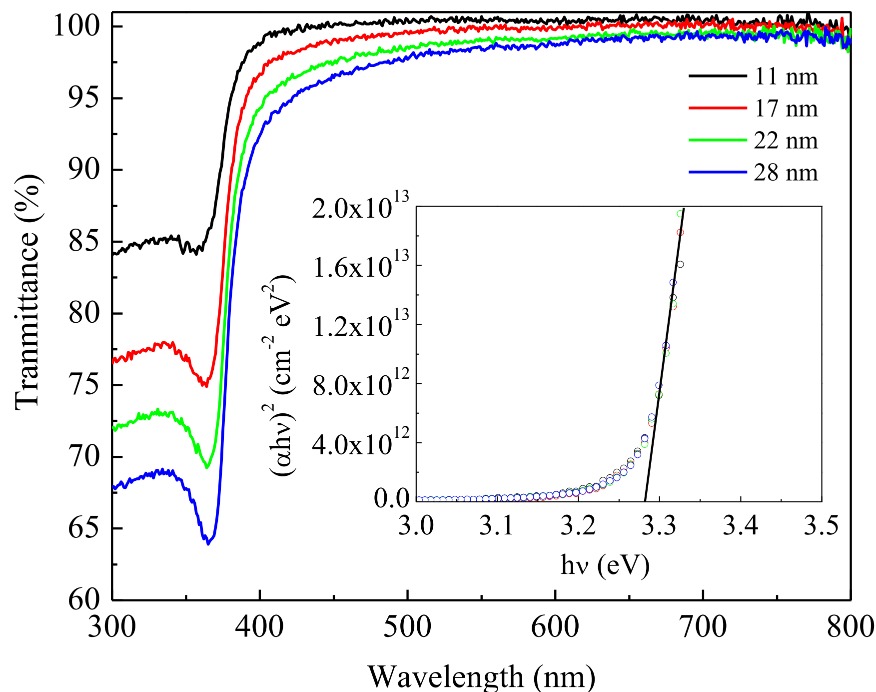

Figure 5.4: Optical transmittance of different thickness ZnO films (11-28 nm) deposited by spray pyrolysis on β-phase quartz substrates and (inset) corresponding Tauc plots showing no significant shift in bandgap as film thickness changes.

As would be expected, the transparency of the films clearly decreases as the film thickness increases, although even at the thickest values the transparency remains good at over 90% transmittance for all

films across the visible spectrum. The extracted bandgap of the films (Fig 5.5 inset) appear to maintain a value close to the 3.28 eV of the previously extracted values for films deposited by spray pyrolysis at ~500 °C and also those quoted in the literature [15, 27, 28].

5.2.3 Surface analysis on ZnO thin-films

Films were deposited for the preparation of devices at the same time as those discussed above, and were examined using atomic force microscopy over both large (90 μm^2) and small areas (1 μm^2) from within the channel region of fabricated devices.

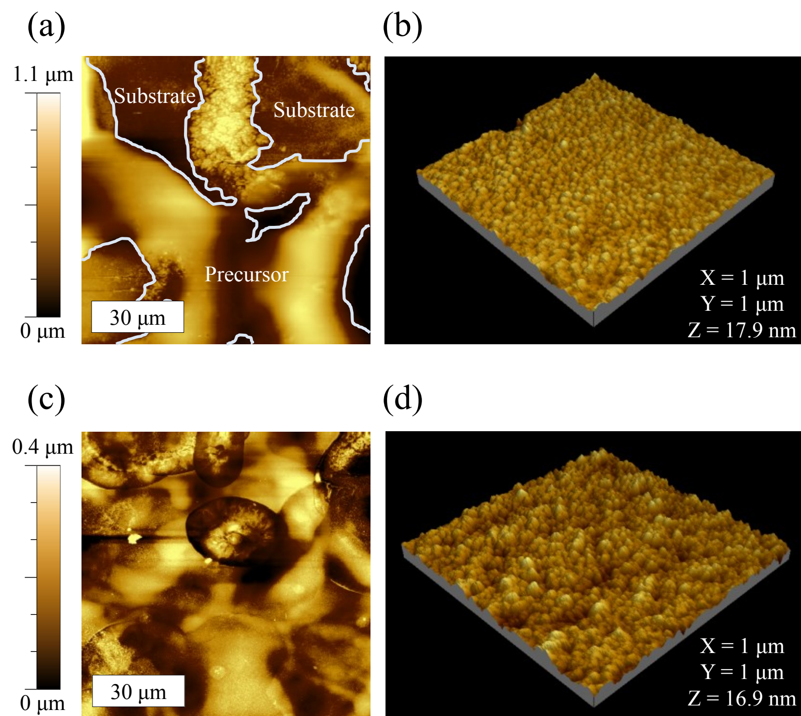

Figure 5.5: Atomic force microscopy images of zinc acetate precursor solution deposited at low temperatures. 90 μm (a) and 1 μm (b) topography image of films deposited at 100 °C, 1 μm image taken from substrate area. 90 μm (c) and 1 μm (d) topography image of films deposited at 200 °C, 1 μm image taken from substrate area.

At low substrate temperatures (room temperature to 200 °C), the sprayed precursor seems to agglomerate leading to areas alternating

between bare substrate and regions of acetate up to a thickness of ~1 μm (Fig 5.5(a)). On closer inspection of what appear to bare substrate areas, there does appear to be a thin-film of precursor material on the surface (Fig 5.5(b)), however the surface is quite smooth with none of the clear grain regions that are seen at higher temperatures. The same is seen as temperatures approach 200 °C (Fig 5.5(c) and (d)), although the agglomeration tends to become more confined to the droplet area, likely due to much faster evaporation of the solvent at higher temperatures.

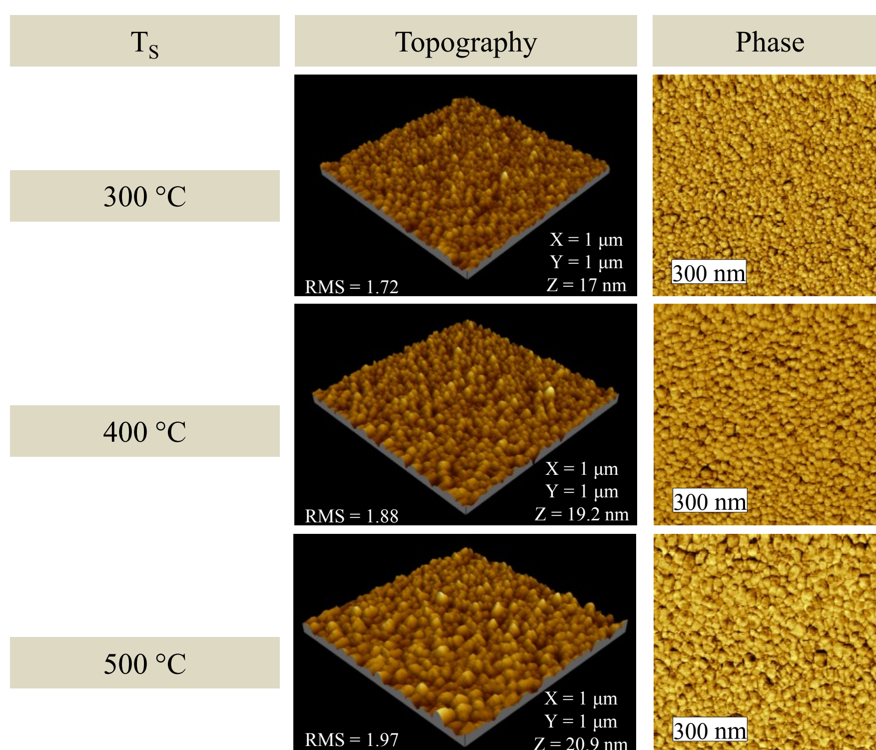

Figure 5.6: Atomic force microscopy images showing evolution of ZnO films deposited at higher temperatures 100 °C to 500 °C. 1 μm scan sized topography and phase images were taken, showing increasing grain size and surface roughness with increasing temperature.

Examining the films deposited at higher substrate temperatures (≥300 °C) there is a noticeable evolution of the surface characteristics (Fig 5.6). With increasing temperature the precursor no longer appears to agglomerate and is evenly distributed across the substrate. Grain size also increases, as does RMS surface roughness with increasing temperature.

Studies of pulsed laser deposited (PLD) films suggest films deposited at low temperatures tend toward the amorphous phase due to low surface diffusion mobility of adsorbed adatoms or molecules [16]. To some extent this is likely the case with spray pyrolysed films, however for spray pyrolysed films, precursor decomposition must also be considered. In this work it is likely that at low temperatures (<300 °C) films consists of a mixture of crystalline and amorphous ZnO, along with some remnants of the non-decomposed precursor materials, whilst at high temperatures there is only a polycrystalline presence of ZnO.

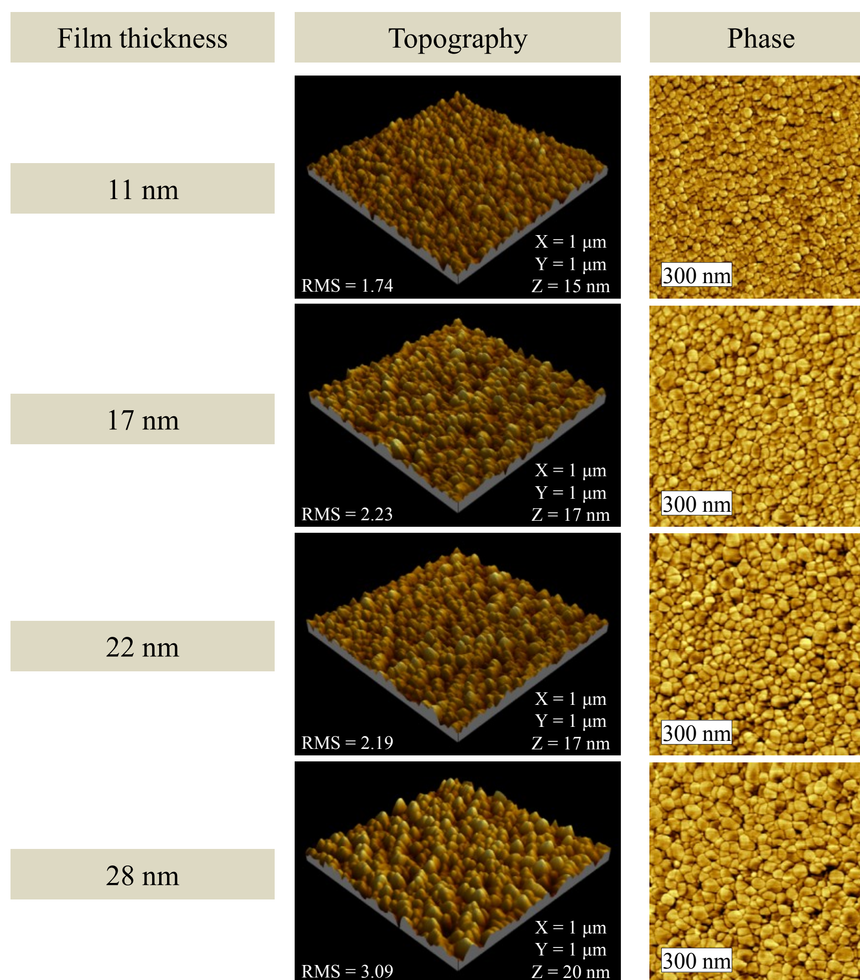

Figure 5.7: Atomic force microscopy images showing evolution of ZnO films deposited to different thickness levels. 1 µm scan sized topography and phase images were taken, showing increasing grain size and surface roughness as film thickness increases.

Films deposited to differing thicknesses were also investigated by AFM (Fig 5.7). The film thickness was adjusted by changing the precursor solution feed rate to the ultrasonic spray nozzle. From both the topography and phase images it can be seen that grain size and surface roughness tend to increase with increasing film thickness. This is generally seen to be the case with ZnO thin-films deposited by other methods, and there is typically a correlation between larger grain size and improved crystallinity [16, 29, 30].

5.2.4 Structural analysis of ZnO thin-films

XRD experiments were conducted in order to examine the crystalline quality of the zinc oxide films deposited at different temperatures (Fig 5.8). For XRD measurements the films were deposited on glass substrates, and a commercially available zinc oxide powder was used as a reference. The tail end of the broad band ending at ~39° corresponds to the glass substrate.

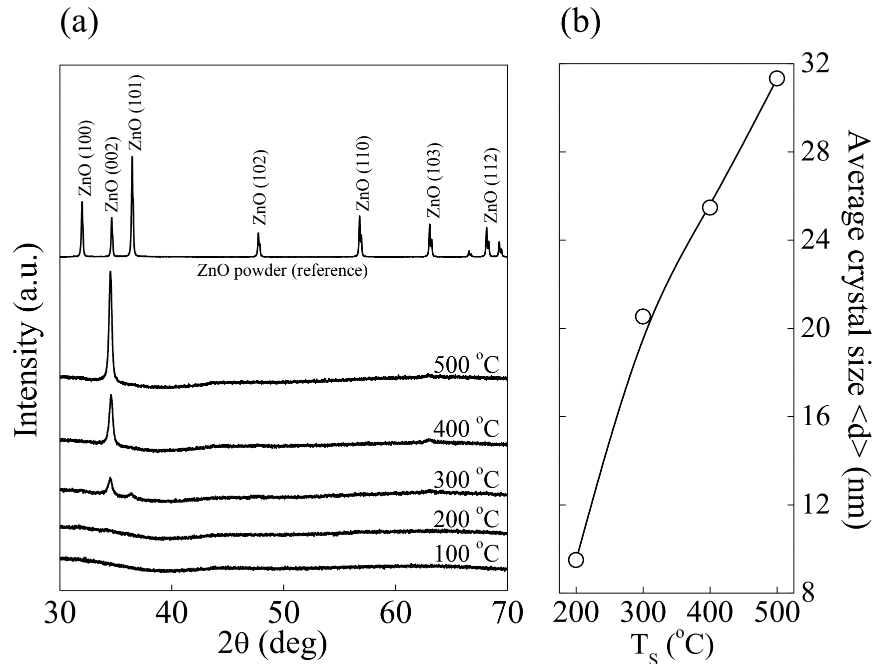

Figure 5.8: (a) X-ray diffraction data of ZnO films deposited at different temperature. The reference pattern is obtained using zinc oxide powder. (b) Average crystal sizes for measured films calculated from the (002) diffraction peak using the Scherrer formula, assuming a shape factor of 0.95.

At room temperature and 100 °C there are no peaks corresponding to the reference sample, suggesting no presence zinc oxide. Films deposited at temperatures of 200 °C and above show diffraction peaks at 34.6° and also a small peak at 63.05° that can be referenced to the (002) and (103) planes of reflection of a ZnO powder reference (Fig 5.8(a)).The crystallite domain sizes, calculated using the Scherrer formula [31] and utilising the (002) peaks of the XRD data shows the average crystallite size increasing with increasing substrate temperature (Fig 5.8(b)). Between 200 °C and 500 °C the crystallite size increases from 9.5 nm to 31.3 nm. With the increasing substrate temperature there is also a clear increase in the relative intensity of the reflection peak at 34.6° suggesting a primarily polycrystalline phase with preferred orientation in the (002) direction, as is common to ZnO films grown by a number of methods [15, 27, 32-35].

5.2.5 C-V characteristics of ZnO TFTs

To investigate the electronic quality of spray pyrolysed ZnO films, thin-film transistors were fabricated using a number of different architectures. Coplanar bottom-gate devices were fabricated using substrates comprising of a silicon substrate, on top of which is a thermally grown 200 nm dielectric, with photolithographically pre-patterned gold source and drain contacts. ZnO was deposited by SP as the last processing step. Staggered bottom-gate devices were fabricated using substrates comprising of a silicon substrate, on top of which is a thermally grown 400 nm dielectric. Source and drain contacts are deposited by thermal evaporation after the deposition of zinc oxide. In both cases the contact thickness is ~30 nm, and device channel dimensions range from 1.5 μm to 100 μm in length and 500 μm to 10000 μm in width. In the case of both architectures, the silicon substrate is heavily p-type doped and acts as the gate contact. All devices were characterised under vacuum at room temperature, and under dark conditions.

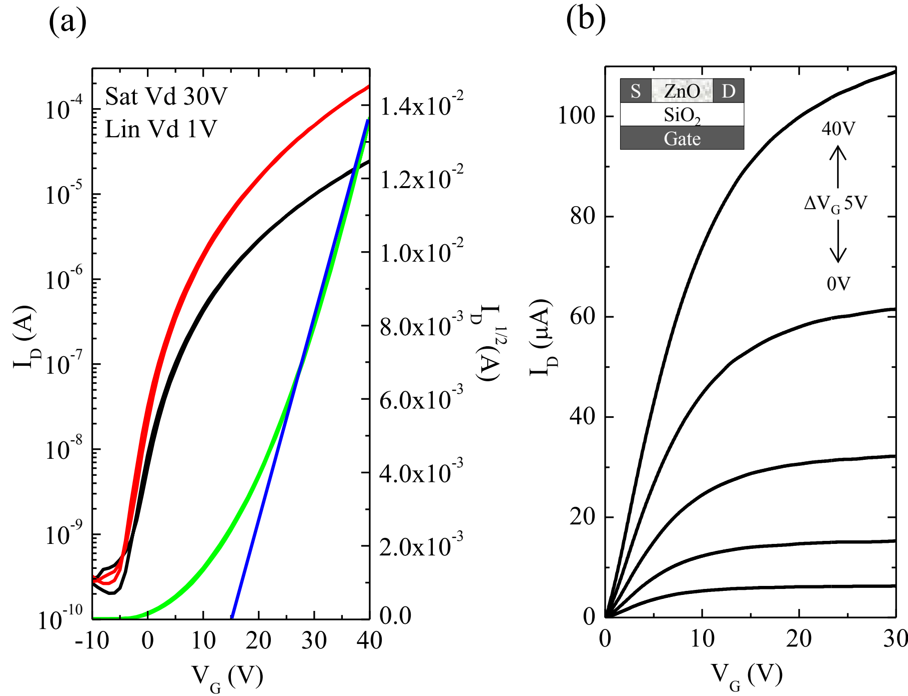

Figure 5.9: (a) Transfer and (b) output characteristics of coplanar bottom gate (see inset) transistor with channel dimensions of 10 μm length, and 10000 μm width, deposited at 400 °C.

Some typical device characteristics for films deposited at 400 °C and at a deposition rate of 2000 μl/min and utilising both gold and aluminium contacts are shown (Fig 5.10 and 5.11). The film thicknesses are estimated to be ~20 nm by SR. Common characteristics among ZnO based TFTs include n-type operation, relatively high charge carrier mobility when compared to amorphous silicon, high $I_{D(on)}/I_{D(off)}$ ratios, and hard saturation is typically observed in output characteristics.

Transfer (Fig 5.10(a)) and output (Fig 5.10(b)) curves for a coplanar bottom gate device with gold source and drain contacts shows good performance. The device channel width is 10000 μm and channel length is 10 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~1.2 cm^2/Vs, the $I_{D(on)}/I_{D(off)}$ ratio is ~10^6 and the threshold voltage, V_T, is estimated to be 15 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 1.8 *V/dec*. The low charge carrier mobility value is typical of ZnO

devices utilising gold contacts due to charge injection issues, this is discussed in further detail in section 5.2.6., and essentially effect is noticeable under close examination of output curves where a superlinear operation can be seen at very low drain voltages.

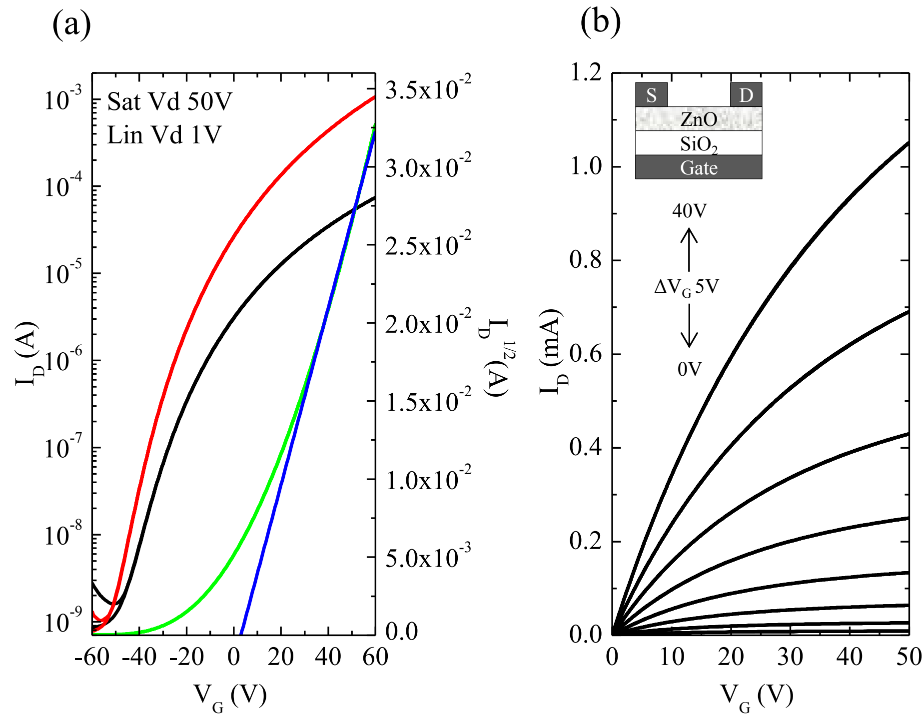

Figure 5.10: (a) Transfer and (b) output characteristics of staggered bottom gate (see inset) transistor with channel dimensions of 30 μm length, and 1000 μm width, deposited at 400 °C.

Transfer (Fig 5.11(a)) and output (Fig 5.11(b)) curves for a staggered bottom gate device with aluminium contacts also show excellent performance. For this device channel width is 1000 μm and channel length is 30 μm. In this device, μ_{sat}, is significantly higher and calculated to be ~16.9 cm^2/Vs, the $I_{D(on)}/I_{D(off)}$ ratio is ~10^6 and V_T is estimated to be 2.2 V and S is estimated to be 3.1 *V/dec*. The significantly improved mobility is attributed to the use of aluminium as source and drain contacts. No superlinear behaviour is seen in the output characteristics of any of the devices fabricated using aluminium for source drain contacts.

In general it can be observed of all devices fabricated at ≥300 °C that there is little to no hysteresis in the measured transfer curves. Transistor operation is achieved in devices fabricated at temperatures as low as 200 °C. However the device performance tends to be poorer in terms of charge carrier mobility and $I_{D(on)}/I_{D(off)}$ ratio, whilst there is noticeable hysteresis in the transfer curves.

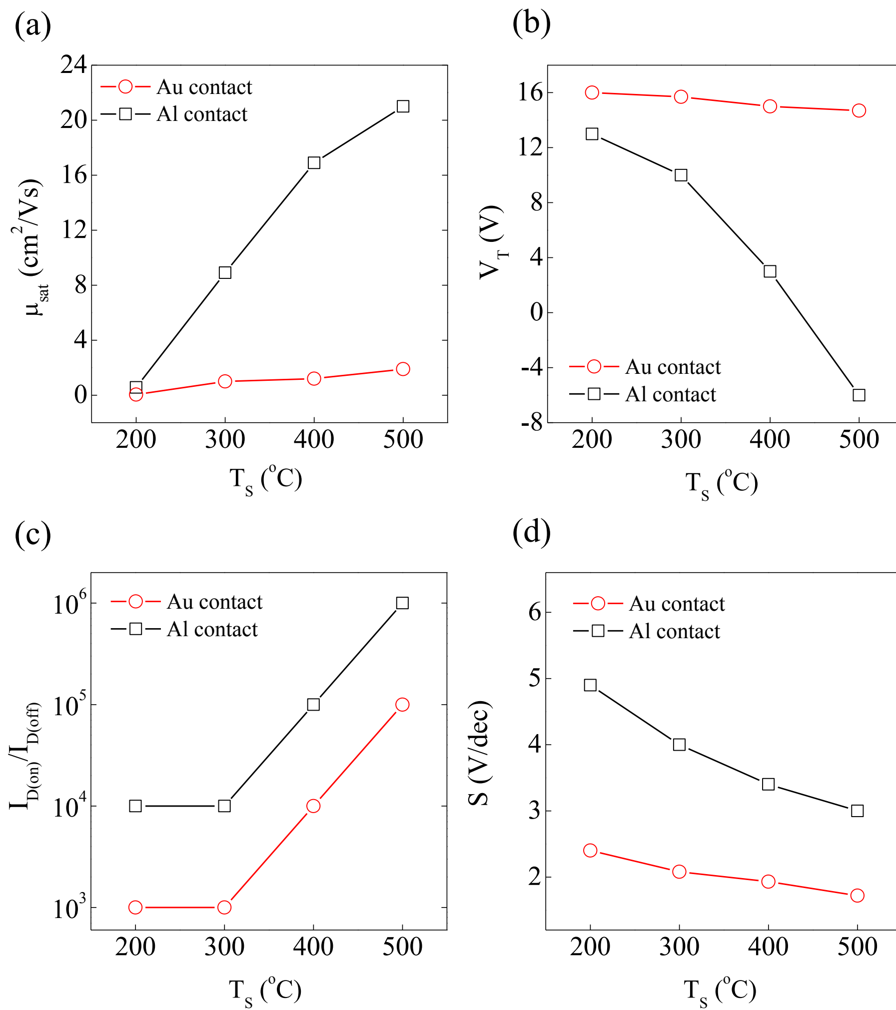

Figure 5.11: Parameter extraction as a function of deposition temperature ZnO devices (a) charge carrier mobility (b) threshold voltage evolution (c) $I_{D(on)}/I_{D(off)}$ evolution and (d) subthreshold voltage swing.

There are several significant changes in performance metrics when studying devices as a function deposition temperature (Fig 5.12).

With increasing temperature we generally see increasing charge carrier mobility, increasing $I_{D(on)}/I_{D(off)}$ ratio, a negative shift in V_T and an increase in the subthreshold slope S. These improvements are attributed to a number of factors.

Firstly, the improved crystalline quality of the deposited films, as evident from the XRD analysis in section 5.2.4., is one source of the improvement in the both the charge carrier mobility (Fig 5.12(a)) and $I_{D(on)}/I_{D(off)}$ ratio (Fig 5.12(c)), most likely due to an improvement of the semiconductor/dielectric interface. From both the XRD and AFM data in section 5.3.2., we can also see that with increasing temperature there is a clear reduction in the number of grain boundaries across the device channel length, this is considered the most significant factor in aiding mobility by reducing the number of grain boundary barriers opposing charge transport, as discussed in section 2.1.2.4.

In a similar fashion there is also a trend toward improved charge carrier mobility with decreasing channel length (not shown), but this is only seen with devices fabricated with aluminium contacts. This suggests that charge injection limitation due to the gold contact material has an overbearing effect on device mobility, and this is discussed in more detail later.

The main cause of the negative shift in V_T (Fig 5.12(b)) with deposition temperature is not entirely clear, but is likely due to a change in the film stoichiometry [36, 37], leading to a higher bulk charge carrier concentration, and in turn requiring increasingly negative gate voltages to deplete the dielectric/semiconductor interface of charges. This is most prevalent in the aluminium contact devices, where there is little charge injection limitation, however the high work function of the gold contacts appear to have an overbearing effect on V_T, leading to the requirement of much higher gate voltages before charge injection can occur.

The subthreshold slopes for both device structures are significantly affected by increasing temperatures (Fig 5.12(d)). Utilising the subthreshold slope, and also the threshold voltage and on voltage (not shown), we can assess the nature of the charge trapping within the

devices. Using the methods discussed in section 2.2.8 it is possible to estimate the trap concentration per unit energy, D_T (Fig 5.13(a)), using the subthreshold slope [38]:

$$D_T = \frac{C_G}{q^2}\left(\frac{qS}{kT\ln(10)} - 1\right) \qquad [5.1]$$

Secondly it is possible to extract the interface electron surface trap density, N_T (Fig 5.13(b)), using the threshold and on voltages [39]:

$$N_T = \frac{C_G|V_T - V_{ON}|}{q^2} \qquad [5.2]$$

From the data it is clear that in both cases, the increase in the deposition temperature leads to a reduction of the charge trapping. However, to some degree the analysis of the devices using gold contacts is somewhat flawed as the high work function of the gold leads to a rectifying semiconductor/contact interface, or Schottky contact.

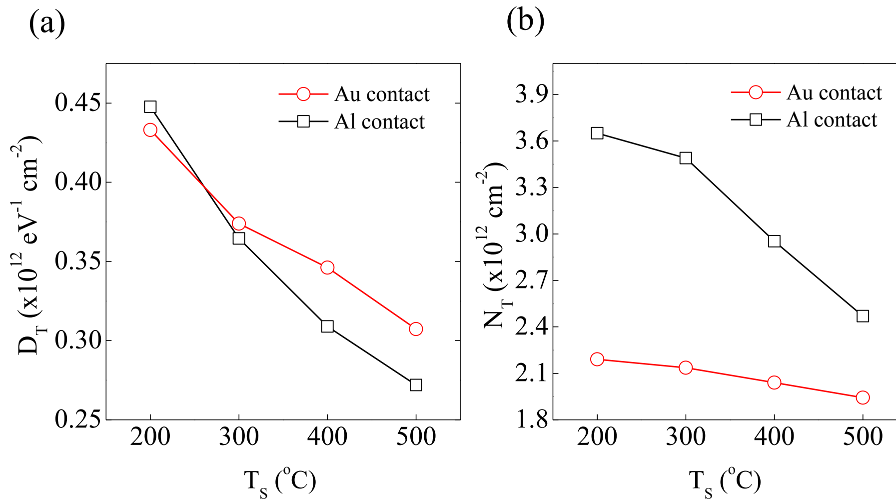

Figure 5.12: Impact of deposition temperature on (a) trap concentration per unit energy, D_T, and (b) interface electron surface trap density, N_T.

This in turn leads to a charge injection barrier that is modulated by the gate voltage giving spurious results that suggest a steeper subthreshold slope than would normally be expected with an ohmic contact. To that extent, the values for the aluminium contact devices offer a more realistic estimation of the nature of the trapping mechanisms within ZnO devices. In each case there is a clear trend suggesting higher deposition temperatures lead in general, to a lower number of trap states. At lower deposition temperatures where a combination of both poor conversion of the precursor materials, as well as an increase in grain boundary density is seen, there is an increase in both the trap concentration per unit energy, D_T, and also the interface electron surface trap density, N_T. Assuming a grain boundary trapping model, it would be expected that as the deposition temperature increases, and grain boundary density is reduced, a decrease in the trap concentration per unit energy would also occur. This is illustrated by a significant decrease in D_T when approaching the highest deposition temperature of 500 °C, where the trap density is estimated to drop to almost a half of the low temperature value for the aluminum contact devices.

The areal interface trap density, N_T, also reduces significantly with increasing deposition temperature. This suggests the quality of the semiconductor/dielectric interface morphology benefits significantly from higher deposition temperatures, most likely due to more favourable thermodynamic conditions at the substrate surface, leading to improved diffusion mobility of the deposited adsorbed adatoms or molecules. Regarding the gold contact devices, for reasons already discussed it is difficult to assign any validity to the estimations, but a similar change is noted corresponding to the trend witnessed in the aluminum contact devices.

Increasing film thickness through adjustment of the deposition rate sees a corresponding change in charge carrier mobility and threshold voltage. Films deposited at 400 °C and utilising only Al contacts were investigated, and in general the device characteristics were typical to those illustrated in figure 5.11. However, as the film thickness increases

so does the charge carrier (Fig 5.14(a)) mobility, and there is a corresponding negative shift in V_T (Fig 5.14(b)). Both of these metrics are also seen to change with decreasing channel length, except in the thinnest of films (11 nm). Improved mobility is attributed to the increase in grain size seen in the thicker films, as shown in the AFM data in section 5.2.3. The negative shift in V_T with increasing film thickness is attributed to an increase in the number of bulk charge carriers, requiring an ever more negative gate bias to deplete the channel of carriers. Film thickness has been used by others as a method for controlling V_T in amorphous metal oxide thin-film transistors [40].

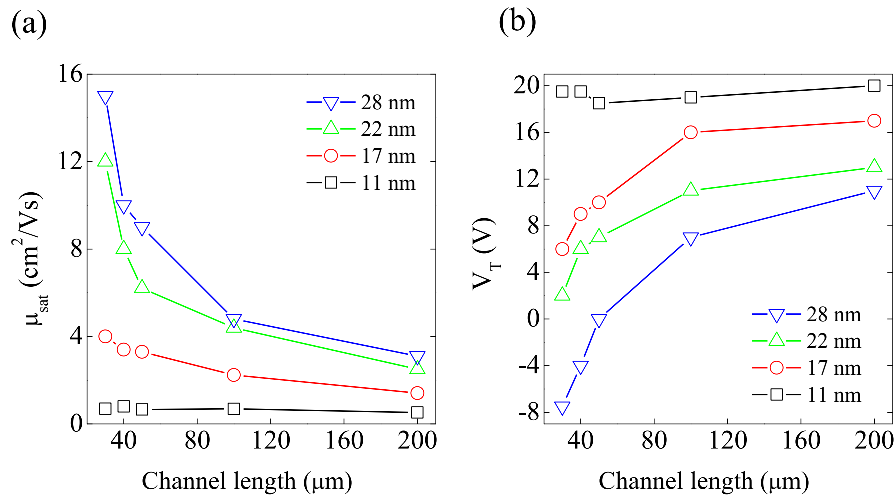

Figure 5.13: (a) charge carrier mobility (a) and threshold voltage (b) dependence on film thickness and device channel length for staggered bottom contact devices with aluminium source and drain contacts.

5.2.6 Contact resistance analysis

As referred to previously, the choice of contact material plays a significant role in device performance. In terms of analysis we can look at the contribution of material choice to device performance through analysing its effective contact resistance R_C. The total device series resistance R_T is a combination of the channel resistance and contact resistance for both the drain and source contacts. The total contact

resistance can be determined using the transmission line method as described in section 2.3.4.

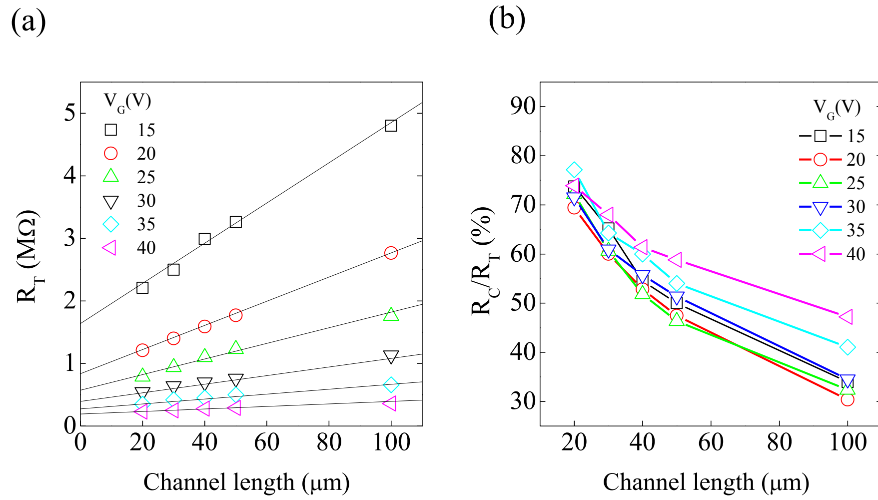

Figure 5.14: Calculated values for gold contact devices for (a) total device resistance at differing gate voltages and as a function of channel length and (b) R_c/R_T ratio for increasing gate voltages as a function of channel length.

A series of devices were fabricated utilising top contacts of both gold and aluminium. The devices used for the study were all of 1000 μm width and were deposited at 400 °C. The values for R_T were calculated for gold contact devices under the linear operating regime and plotted as a function of the device channel length at different values for V_G (Fig 5.14(a)). Extrapolation of the straight line fits toward the ordinate yields the effective total contact resistance R_C. For these gold contact devices, values between 200 kΩ and 86 MΩ are calculated for R_C. As expected, due to the high work function of the gold contact R_T decreases significantly as V_G increases. This is due to a decrease in the charge injection barrier at the contact as the increasing gate voltage pushes the Fermi level toward the conduction band. However R_C does not converge at zero channel length and remains strongly dependent on V_G. As the channel length reduces, so R_C becomes the dominating component of R_T (Fig 5.14(b). Therefore an increasing portion of the externally applied voltage is dropped across the contacts and so the effective device charge carrier mobility is reduced.

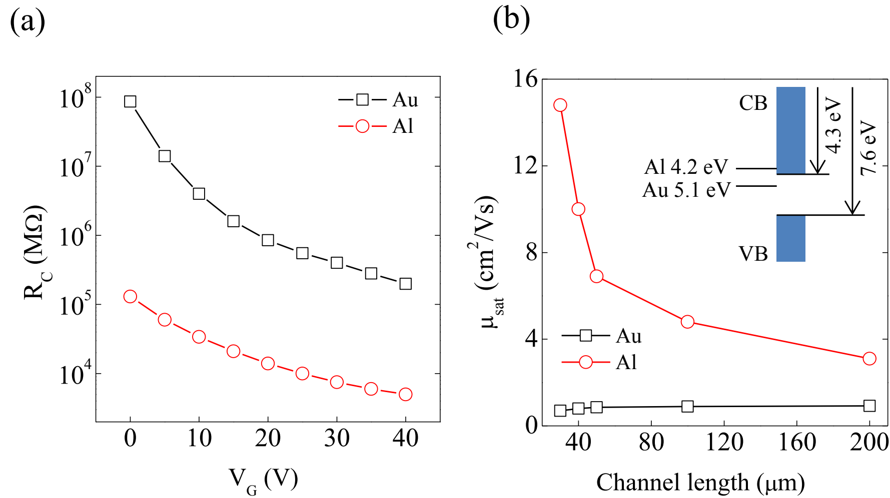

Figure 5.15: (a) Contact resistance for aluminium and gold as a function of gate voltage and (b) effect on device charge carrier mobility as a function of channel length. Inset, simplified ZnO energy diagram illustrating relative work functions of gold and aluminium contacts.

The same analysis was carried out on devices fabricated with the same geometries, but utilising aluminium contacts. Comparison of the two contact material choices (Fig 5.15(a)) shows that aluminium creates a device with a significantly lowered contact resistance, and in turn an improved effective device charge carrier mobility (Fig 5.15(b)). At ~ 4.2 eV, the lower work function of the aluminium creates a lower barrier to charge injection when compared to that of the gold, at ~5.1 eV (Fig 5.15 inset), leading to aluminium being the preferred choice of contact material.

5.2.7 Statistical observations in ZnO TFTs

Deposition by SP should in principle, offer a route to highly consistent device performance. The deposition of all the oxide films under discussion in this work was accomplished in ambient atmosphere outside of a cleanroom, in what could be considered a typical chemical laboratory. The entire SP system is enclosed, and is permanently connected to an extraction system such as connected to a regular chemical laboratory fume hood. The fact that the work presented here

isn't performed in a cleanroom environment is reflected in the variability of some of the performance metrics extracted from the measured devices.

In order to assess the impact of this deposition environment and also as a general guide to how much confidence can be asserted to the extracted performance metrics, a large batch of bottom-gate, top contact (staggered) devices were fabricated utilising Al as the S/D material. In total, 100 devices were fabricated and characterised together. The devices were all 1000 μm in channel width, with 5 different channel lengths varying between 30 μm and 200 μm.

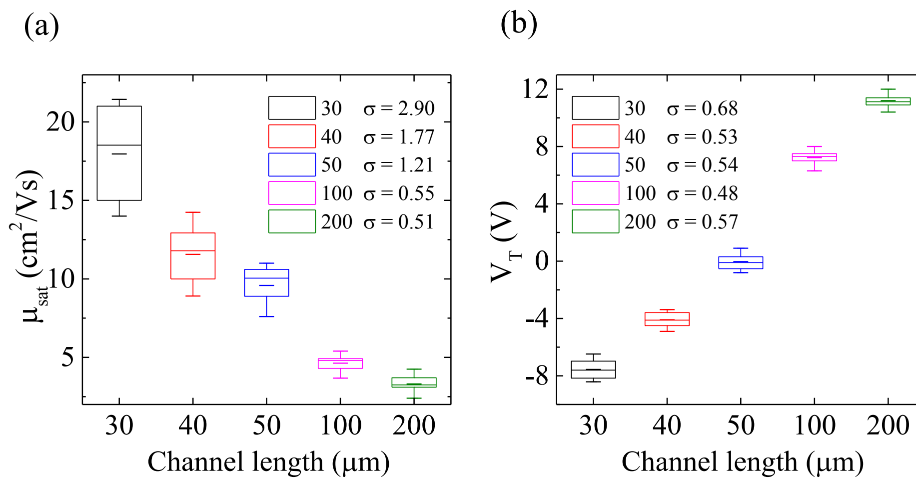

Figure 5.16: (a) Box chart showing variation in mobility extracted from a total of 100 devices, and shown as a function of channel length and (b) box chart for extrapolated threshold voltages for same devices. In each chart the whiskers represent max/min values, the box range covers the 25th and 75th percentile, the solid line through the box shows the median whilst the short line within the box represents the mean. One standard deviation, σ, for each set is shown inset.

The largest variation appears in the extracted mobility values (Fig 5.17(a)). As an example, for the 30 μm channel length devices, mobility values were found to vary between a minimum of 14 and 21 cm^2/Vs with a σ of 2.9 cm^2/Vs. If a grain boundary limited transport is assumed, a larger variation in the shorter channel devices is possibly due to the nature of the grain boundary trapping/barrier, which in turn, has a strong bearing on the device mobility. As we approach longer channel lengths the influence of the grain boundary trapping/barrier averages out

as we see a large increase of the total number boundaries across the channel. There is a significantly lower variation seen in the threshold voltages between device geometries, with the largest variation in extracted values only covering a range of ~2.2 V (Fig 5.17(b)), although there is a slight increase seen in the standard deviation as we approach shorter channel lengths. No figure is shown for the $I_{D(on)}/I_{D(off)}$ ratios as there is little variation seen for any given channel length, particularly as values are typically quoted as orders of magnitude difference. Typically at longer channel lengths the $I_{D(on)}/I_{D(off)}$ ratios are ~10^5, with values reaching ~10^7 for the shortest channel length devices. Finally the sub threshold slopes were also analysed, with little variation seen between identical dimension devices. Longer channel devices exhibit values of ~4.8 *V/dec*, with values approaching less than 3.05 *V/dec* for devices with 30 μm channel lengths. In all cases the standard deviation remains reasonably constant between 0.13 and 0.19 *V/dec* for all devices.

5.3 Gallium oxide thin-film transistors by spray pyrolysis

Much of the work within this thesis is focused toward the optimisation spray pyrolysed ZnO based devices. However, other materials where investigated if it was believed there may be the possibility of some interesting findings. The following data shows the successful deposition of Ga_2O_3 and fabrication of TFTs with charge carrier mobilities approaching 0.5 cm^2/Vs.

Ga_2O_3 is known to exist in a number of crystalline forms, however β-Ga_2O_3 is generally considered to be the most stable. As a transparent semiconductor with a wide bandgap it attracts interest for use in a number of areas including optical devices such as deep ultraviolet photo detectors and diodes an also gas sensing applications [41, 42]. High bandgap materials are attractive for device purposes due to their high breakdown strengths, leading to high power handling capacity. In terms of Ga_2O_3 based transistors there are demonstrations of tin and aluminium doped devices, grown using methods such as molecular-beam epitaxy (MBE) and pulsed laser deposition (PLD) [43, 44]. However, to

the author's knowledge this is the first demonstration of un-doped Ga_2O_3 TFTs by solution deposition.

In terms of film preparation, films were sprayed onto a number of different substrates simultaneously. These consisted of SiO_2 (400 nm) on Si, for the preparation of transistors, whilst β-phase quartz substrates were used for the deposition of films prepared for UV-Vis spectroscopy. The films were deposited at a substrate temperature of 450 °C.

5.3.1 Precursor materials

For the deposition of Ga_2O_3 films gallium acetylacetonate was used as the precursor acetate (Fig 5.17). Numerous other precursors were initially tried including gallium acetate and gallium nitrate, but the quality of the deposited films were poor from both an electronic and optical standpoint.

In terms of the solvents used with gallium acetylacetonate, solubility proved to be best using water, however issues similar to those encountered previously with zinc acetate were seen, including poor quality films with high levels of optical scattering and non-uniformity of film thickness. Ethanol (linear formula: C_2H_6O) was chosen due to the improved quality of the deposited films, both optically and electronically, however solubility proved to be quite poor, this in turn led a longer deposition time that had to be performed by spraying at a higher volume, comprised of 16 spray operations, and at a feed rate of 2500 μl/min.

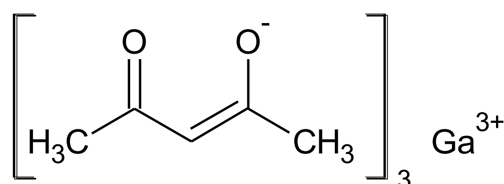

Figure 5.17: Chemical structure of gallium acetylacetonate used for the preparation of precursor solution. Liner formula: $[CH_3COCH{=}C(O\text{-})CH_3]_3Ga$.

5.3.2 Optical properties of Ga_2O_3 thin-films

The optical properties of the Ga_2O_3 films were investigated using UV-Vis spectroscopy. Optical transmittance spectra were measured across the spectral range from 200 to 800 nm (Fig 5.18).

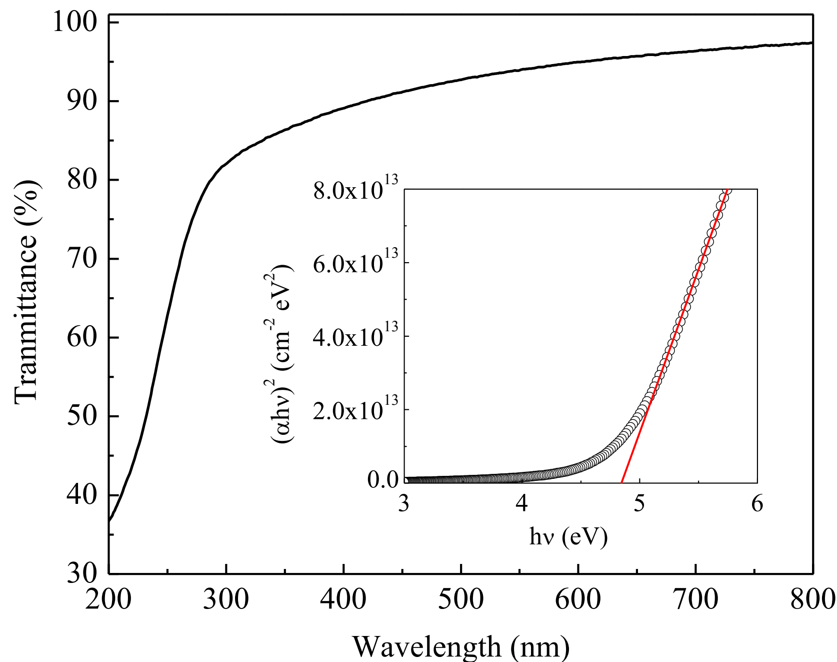

Figure 5.18: Optical transmittance spectra of Ga_2O_3 thin-films (~10 nm) deposited by spray pyrolysis on β-phase quartz substrates and (inset) optical bandgap extracted using Tauc plot based on direct band gap transition

Film thickness was estimated to be approximately 10 nm by SR. The films remain highly transparent at over 85% transmittance across the visible spectrum with a strong absorption onset feature in the UV region. From the Tauc plot (Fig 5.18 inset) the direct bandgap of the film is estimated to be 4.8 eV, this is in good agreement with reports from within the literature. There are numerous reports on the optical properties of Ga_2O_3 suggesting a wide range in values for optically extracted band gaps, ranging between 4.3 eV and 4.9 eV. Factors including deposition methods and growth conditions appear to have some bearing on the extracted values; however the values reported here are in line with those

found by others depositing Ga_2O_3 thin films, and utilising similar or the same deposition methods [45-49].

5.3.3 Surface analysis of Ga_2O_3 thin-films

The surface morphologies of the deposited films were examined using atomic force microscopy over areas of 1 μm^2 and 5 μm^2 (Fig 5.19). Measurements were taken from within the channel region of thin-film transistor devices.

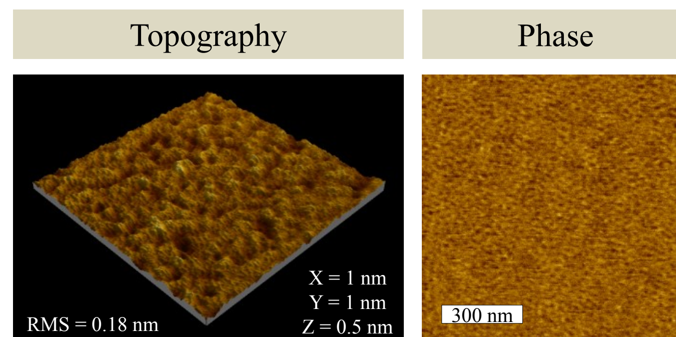

Figure 5.19: Atomic force microscopy images showing Ga_2O_3 thin-films. 1 μm scan sized topography and phase images were taken, showing no evidence of grain structure and very low surface roughness.

The acquired topography images show exceptionally smooth film surfaces with no evidence of grain boundaries. From the topography image the RMS roughness value is calculated to be 0.18 nm, identical in value to the underlying SiO_2 dielectric layer. This lack of grain structure and smooth surface suggests an amorphous nature to the deposited Ga_2O_3. This has been illustrated elsewhere, whereby spray pyrolysed Ga_2O_3 thin-films require high temperature annealing before that are able to attain the more commonly recognised β-phase Ga_2O_3 [48]. The phase images maintain essentially no phase change across all measurements, with none of the features associated with grain boundaries, as demonstrated in the ZnO films in section 5.2.3. Measurements were also

taken on the films deposited on the β-phase quartz substrates used for UV-Vis spectroscopy, and confirm the lack of grain structure and smooth nature of the deposited films.

5.3.4 C-V characteristics of Ga_2O_3 TFTs

Ga_2O transistors and their doped variants are electron transporting. In general device performance appears to vary depending on the nature of the deposition methods, doping etc., but is estimated to be as high as 300 cm^2/Vs for tin doped, single crystal β-Ga_2O_3 [43]. Some typical device characteristics for films deposited at 450 °C and at a deposition rate of 2500 μl/min are shown (Fig 5.20). Transfer (Fig 5.20(a)) and output (Fig 5.20(b)) curves for a staggered bottom-gate device with aluminium source and drain contacts show good performance. Channel width for this device was 1500 μm and channel length is 30 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~0.5 cm^2/Vs, the $I_{D(on)}/I_{D(off)}$ ratio is ~10^3 and the threshold voltage, V_T, is estimated to be 64.4 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 4 *V/dec*. The devices clearly work as enhancement mode devices and suffer from an excessively high V_T, this may be due to the undoped nature of the materials leading to lack of available charge carriers. This may also be exacerbated by the very thin nature of the films, where a similar shift in threshold voltage is seen as a function of film thickness in ZnO based transistors [40].

At 0.5 cm^2/Vs, charge carrier mobility not as high as zinc oxide, but is comparable to that of amorphous silicon. The inherently disordered nature of amorphous Ga_2O goes some way in explaining this. The output characteristics show hard saturation, with no indication of charge carrier injection issues, suggesting the limited mobility is likely due to the intrinsic properties of the deposited films.

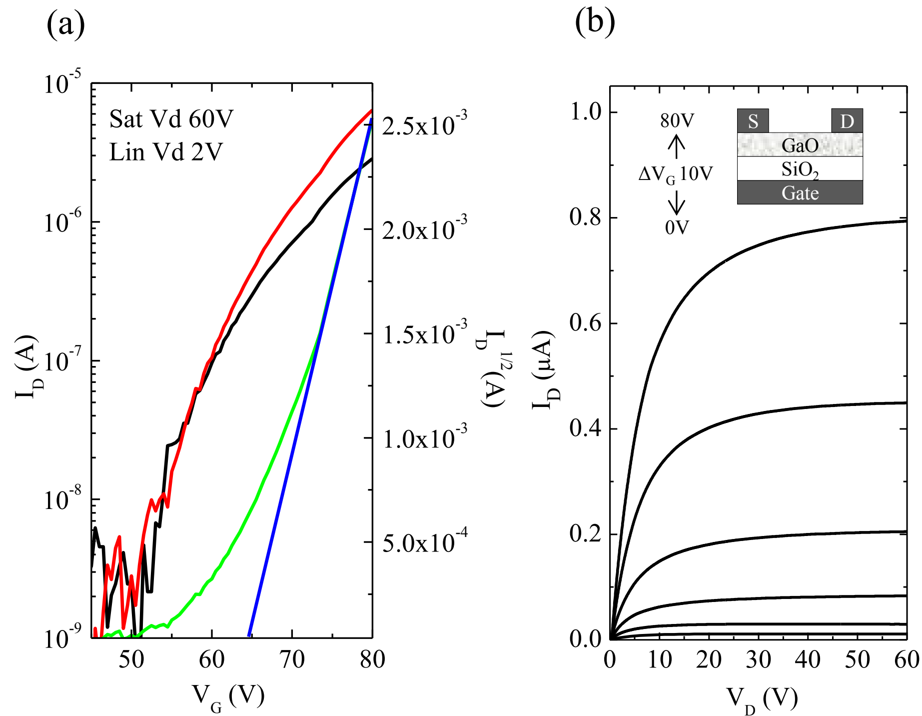

Figure 5.20: (a) Transfer and (b) output characteristics of staggered bottom gate (see inset) transistor with channel dimensions of 30 μm length, and 1500 μm width, deposited at 450 °C.

Using chemical doping methods discussed in the next chapter it is reasonable to expect that device performance can be improved beyond that of amorphous silicon, and possibly close to that of ZnO. In addition to this, high temperature post annealing of the deposited films, on the order of 900 °C, may also yield further improvements by possibly facilitating the conversion from amorphous to β-phase Ga_2O_3.

5.4 Conclusions

The use of SP, a simple yet effective and highly scalable solution processing method, has been applied in the deposition of high performance metal oxide based semiconducting materials suitable for thin-film transistors and low-cost, large volume electronics.

The role of growth conditions including deposition temperature and film thickness was investigated in order to understand and optimise the performance of spray pyrolysed zinc oxide transistors. Through the combined use of materials and electronic characterisation techniques a number of trends can be concluded.

Firstly, by increasing the deposition temperature there is a clear improvement in the crystalline quality of the deposited films, likewise there is an increase in the grain size. All of these features lead to an improvement in device performance, particularly charge carrier mobility, but also other import device metrics such as $I_{D(on)}/I_{D(off)}$ are seen to improve with higher deposition temperatures. Secondly, the adjustment of the deposited film thickness also plays as significant role in the device performance. Thicker films see higher charge carrier mobilities, which although beneficial, come at some cost when considering what device characteristics are most favourable. A benefit of thicker films is the formation larger grain sizes, again reducing the cross channel grain boundary density, as seen with higher deposition temperatures. However, as ZnO is inherently n-type, excessively thick films become overly conductive due large bulk charge carrier quantities. More problematic are the overly negative threshold voltages, leading to device behaviour that is more depletion mode rather than enhancement mode like. Through control and optimisation of the deposition process, film thicknesses are controlled and these issues can be somewhat mitigated.

The effects of contact material has been investigated and it has been concluded that due to its higher work function, gold as a contact material leads to high levels of contact resistance, resulting in lower device charge carrier mobilities. The work function of aluminium however, is somewhat lower, leading to a lower barrier to charge

injection, therefore lower contact resistance and improved device charge carrier mobility.

Finally, to the best of the author's knowledge, solution processed Ga_2O_3 thin-film transistors are demonstrated for the first time. Charge carrier mobilities on the order of those seen in amorphous silicon devices are demonstrated with other favourable device characteristics. Potentially, through the use of chemical doping techniques it should be possible to further enhance device performance, opening up new areas of research for high power devices deposited by low-cost, scalable solution processing.

In general it has been the aim of this chapter to introduce SP as viable and promising method for the deposition of high performance metal oxide semiconducting films, suitable for the next generation of large-area, low cost electronics. The following chapters will expand on the breadth of possibilities that are achievable through the use of SP for the deposition of functional thin-films.

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Chapter 6

Optimised thin-film transistors by solution processed doping

Abstract

Following on from the previous chapter the concept of facile chemical doping is introduced for the optimisation thin-film transistor (TFT) devices fabricated by spray pyrolysis (SP). Through the introduction of additional chemical dopants during the deposition process it is possible to further enhance the already high performance of zinc oxide (ZnO) based transistors. In this chapter lithium and beryllium dopants are used to achieve improved charge carrier mobilities and control of device threshold voltages. As with the previous chapter, material and electronic characterisation method are utilised in order to elucidate how these enhancements are brought about. Extremely high performance ZnO thin-film transistors are obtained, with charge carrier mobilites in excess of 50 cm^2/Vs, whilst the ability to significantly adjust the threshold voltage of devices, across the order of 40 V, is also demonstrated.

6.1 Introduction

The current demand for ever increasing performance electronic devices that are easily and cheaply deposited over large areas has significantly boosted interest into new and alternative semiconductor materials, such as organics and oxides. As discussed in the previous chapter the unique properties of oxide based semiconductors render them very well suited for application in the next generation of flat panel display technologies and other low-cost large area applications. Chemical stability, stress tolerance and high performance are particular attributes that are simultaneously combined in metal-oxide based semiconductors, but not necessarily available in many of the current alternative technologies. Presently, a clear demonstration of high performance, combined with controllability is what is required to convince manufacturers to take the next step toward full time implementation of metal-oxides for future technology applications.

There are numerous examples of doping of ZnO, with most emphasis typically being targeted toward improving electron charge carrier mobility [1-4]. There has been a steady increase in the mobility values reported from various groups, with improvements in processing and doping methods being the main contributing factors [5-11]. Attempts at adjustment or control of the predominant intrinsic defects such as Zn interstitials, Zn_i, and O vacancies, V_O are common. Control of the oxygen levels during depositions using vacuum based techniques is one method used to alter the stoichiometric parameters of ZnO, leading to a change in device characteristics. Oxygen vacancies are purported to have the lowest formation energy of the all intrinsic defects, but it is widely debated as to whether these oxygen vacancies are the root cause of the electron transporting characteristics of ZnO, however there is no disputing the experimental effects are noticeable and significant [12-17].

The use of extrinsic dopants, such as hydrogen, indium, gallium and tin are also commonly investigated for their capacity to alter device performance. Typically, these materials are used as they alter the electronic properties or band structure of ZnO, for example through the

introduction of shallow donor levels providing n-type doping. Hydrogen is still, in theory as well as practice, considered to be a likely cause of the electron transporting characteristic of ZnO [4, 18-20].

From an experimental point of view, there is also a significant body of work dedicated to the stability of devices, investigating bias stressing, the influence of the structure and properties of device back channels, and also the implementation and effects of various passivation techniques [21-25]. However, there is little in the way of investigation into the control of the device threshold voltages. The influence of the dielectric material has been studied and has been shown to have a significant effect on the threshold voltage of ZnO transistors [26, 27]. In terms of studies directly related to the properties of the deposited films, films thickness has been investigated, where a reduction of quantity of bulk charge carriers in thinner films is shown to have a positive shift effect on the threshold voltage [28]. In a similar fashion, control of film stoichiometry through oxygen doping during the deposition process has also been demonstrated to have an effect on transistor threshold voltage, again through the reduction of excessive bulk charge carriers [25]. As an extrinsic dopant, lanthanum has also been shown to act as a carrier suppressant in transistors utilising indium doped zinc oxide thin films [29].

With the above in mind, SP is uniquely advantageous as a deposition method due to the ease in which it is possible to add a chemical dopant during the deposition process. This facile deposition technique where additional precursor solutions are prepared and then blended according to differing molar ratios of the metal or dopant ions, allows for very quick assessments of new materials providing suitable solvents and molecules can be found, but most significantly it offers a simple and low cost method for the deposition of new high quality electronic materials.

6.2 Lithium doped zinc oxide thin-film transistors

This first section deals with the use of lithium doping which is demonstrated to have a substantial impact on the charge carrier mobility of the deposited films [30]. Overall device performance is improved significantly as more lithium is introduced during the deposition phase until a critical point is reached, where device performance begins to degrade. Through controlling the relative ratio of lithium to zinc metal ions within the precursor solution it is possible to adjust some of the properties of the deposited films during crystalline growth process. These changes seen in the structural properties of the deposited films lead to much better device performance through improved charge transport.

To prepare films for characterisation and device fabrication, precursor aerosols across a range of $[Li^{+1}]/[Zn^{+2}]$ ratios were sprayed onto a number of substrates. The films were deposited by spraying 4 coats/passes with the spray nozzle at a rate of 1.5 ml/min, with a two minute gap between each pass, and at a substrate temperature of 400 °C. After the final coat was deposited the films were left on the hot plate for a further two minutes giving the final deposition time to fully convert. Finally the films were lifted off the hotplate and left to cool in ambient. For transistor fabrication, films were deposited on SiO_2 (400 nm) on Si, followed by thermal evaporation of source and drain contacts (staggered structure). For Fourier transform infrared spectroscopy (FTIR) measurements films were deposited on caesium iodine. β-phase quartz and crystalline silicon substrates were used for the deposition of films for UV-Vis spectroscopy and photoluminescence spectroscopy (PL) respectively. X-ray diffraction (XRD) experiments were performed on films deposited on glass, whilst atomic force microscopy (AFM) was performed on the films used for transistor measurements from within the transistor channels as well as outside of the channels. During the deposition process, spraying masks were used to isolate the deposition to as small an area as possible. This was done to minimise the gate current leakage that can occur when the semiconductor deposition encroaches around the substrate edge.

6.2.1 Precursor materials and doping method

In order to deposit Li-doped zinc oxide films a number of precursor materials were initially screened. The use of nitrates and various solvents would typically lead to cloudy solutions when attempting to blend them, often with some form of precipitate appearing. Lithium acetate di-hydrate and zinc acetate (Fig 6.1) were found to be the most suitable materials for precursor solution preparation, offering easier preparation as both materials dissolved readily in methanol (linear formula: CH_3OH), providing two miscible solutions for the preceding blending. Also in terms of optical and electronic properties, the films deposited using lithium and zinc acetates where of the highest quality when compared to those deposited using other precursor materials.

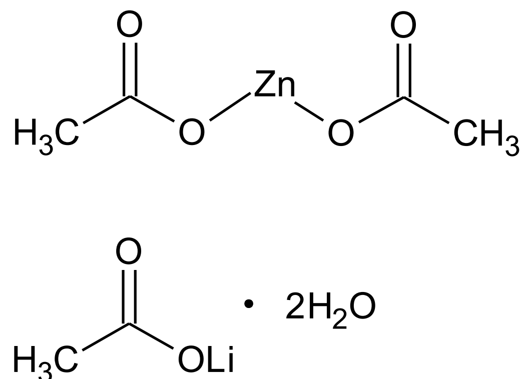

Figure 6.1: Chemical structure of zinc acetate and lithium acetate di-hydrate, used for the preparation of precursor solutions. Liner formula: $(CH_3CO_2)_2Zn$ and $(CH_3COO)Li$ respectively.

Doping was achieved by blending specific ratios of precursor acetate solutions so the required ratios between the metal ion masses are achieved within the final solution. To prepare solutions for the deposition of Li-doped ZnO, the procedure involves making separate 0.1M solutions for each of the precursor materials, these are left to fully dissolve for 30 minutes, followed by the blending step, which again is left for at least 30

minutes to ensure a completely homogeneous mixture. For the preparation of precursor solutions for Li-doped ZnO films, a range of $[Li^{+1}]/[Zn^{+2}]$ ratios were used including 0, 0.1, 0.2, 0.5, 1, 2 and 4%.

6.2.2 Optical properties of Li-doped ZnO thin-films

The optical properties of the Li-doped ZnO films deposited using the previously discussed range of doping ratios were investigated using FTIR, PL and also UV-Vis spectroscopy. Films were deposited at a temperature of 400 °C, and film thickness was estimated to be approximately 30 nm by spectroscopic reflectometry (SR).

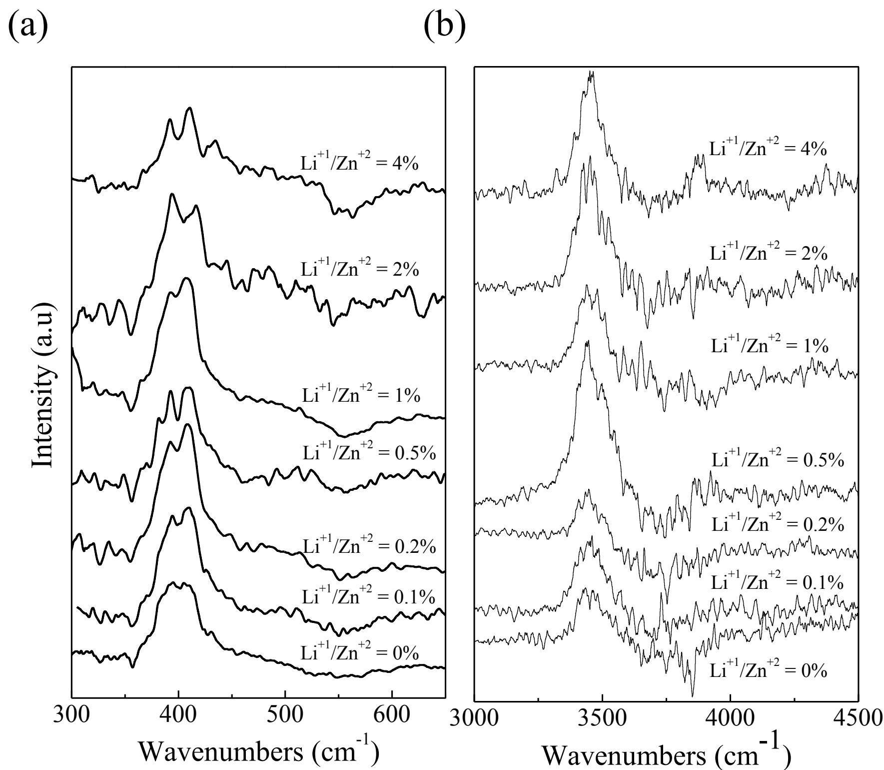

Figure 6.2: (a) Low and (b) high frequency FTIR absorption spectra of LI-doped ZnO on CsI substrates for thin films of varying Li doping ratio. Films were obtained at room temperature.

The molecular composition of the Li-doped ZnO films was investigated by FTIR (Fig 6.2). Measurements were conducted across the total ranges of 6000-370 cm^{-1} (KBr beam splitter), and 700-200 cm^{-1}

(polystyrene beam splitter) at a spectral resolution of 1 cm^{-1}. FTIR spectra measured between 700 cm^{-1} and 3000 cm^{-1} (not shown) revealed no features, typical of previous reports for spray pyrolysed ZnO deposited at 400 °C [31]. This is consistent with the fact that no zinc acetate and lithium acetate dihydrate moieties are present in the films indicating a complete precursor pyrolysis. The low frequency FTIR spectra (Fig 6.2(a)) show the stretching modes of the Zn–O bonding at ~400 cm^{-1}. The spectra are also characterised by the absence of any features at ~320 cm^{-1} that would be assigned to lithium oxide vibrational modes [32]. The high frequency FTIR region (Fig 6.2(b)) reveals a broad band that is assigned to the stretch mode of O–H complexes in ZnO.

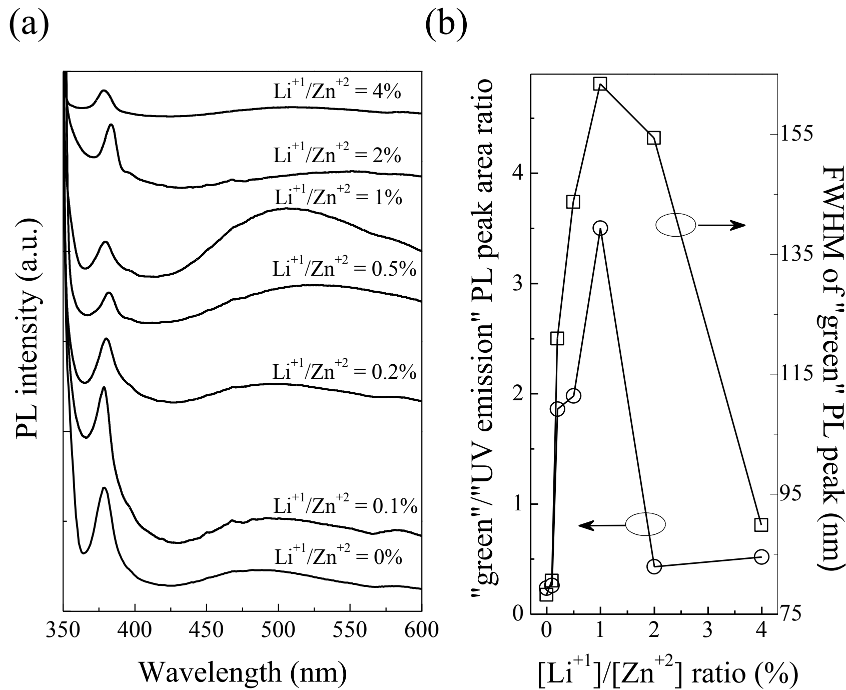

Figure 6.3: (a) Photoluminescence spectra of Li-doped ZnO films of varying of $[Li^{+1}]/[Zn^{+2}]$ ratio excited by 340 nm line of a xenon arc lamp and (b) "Green" to "UV" emission peaks area ratio (left y-axis) and FWHM of the "green emission" peak that illustrates its broadening for varying the Li doping level.

The asymmetry in peak shape suggests that this broad band consists of two O-H assigned features that appear at ~3326 cm^{-1} and

~3611 cm^{-1} and are associated to different defects that give rise to the free-carrier concentration [33, 34]. The lack of any significant change of the line shape of this band for different lithium doping levels denotes that lithium incorporation does not affect the hydrogen induced vacancies.

All of the films assessed using PL spectroscopy (Fig 6.3) show a strong UV emission peak centred on ~370 nm due to the exitonic transition, and also a broad band 'green' emission between 425 and 600 nm. The 1% $[Li^{+1}]/[Zn^{+2}]$ ratio doped films have a pronounced broadening and intensity of the 'green' emission band, as calculated from the FWHM of the peak value when compared to other films. This is attributed to an increase in the concentration of defects that act as radiative paths for visible luminescence. With increasing lithium content both the 'UV' and 'green' emission decrease, which suggests that increased lithium content leads to the formation complex defects, and in turn suppression of the visible 'green' emission [35].

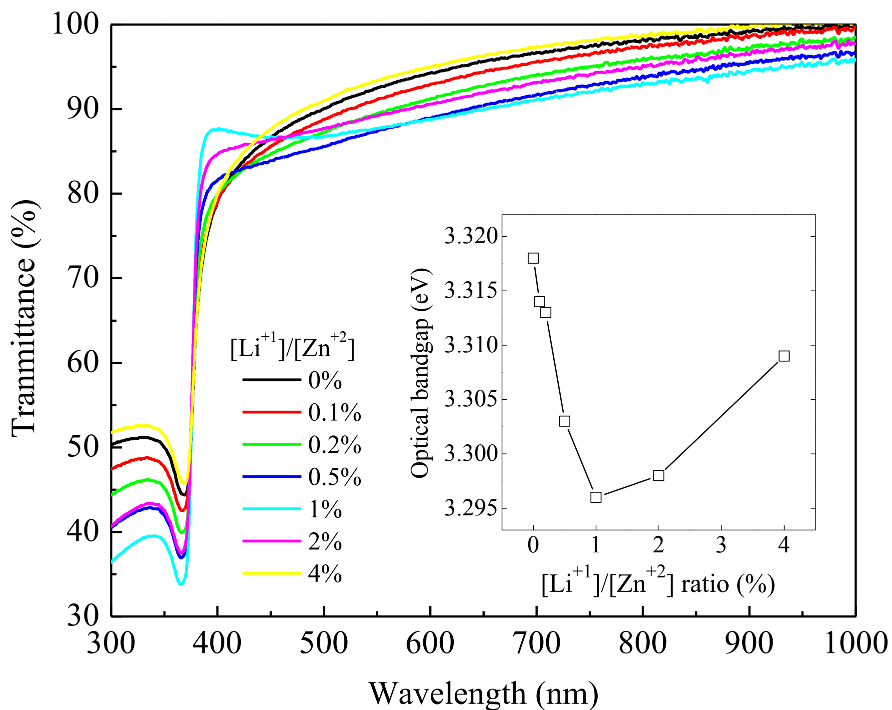

Figure 6.4: Optical transmittance of Li-doped ZnO films of varying of $[Li^{+1}]/[Zn^{+2}]$ ratio deposited on β-phase quartz substrates and (inset) optical bandgap extracted using Tauc plots showing modification as a function of lithium content, with a minimum bandgap corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio.

Transmission data collected by UV-Vis (Fig 6.4), for all films show high transparency across the visible spectrum, with absorption onsets beginning at ~400 nm. At ~470 nm there are clear absorption peaks visible in all films. The peaks appear to increase in intensity as we approach the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio, after which they begin to fall away with increasing lithium content.

A noticeable absorption feature is seen for the 1% doped film centred around 470nm which is not seen in the other films, likewise on closer analysis of the primary absorption peaks, we see a slight broadening as we approach the 1% doping ratio and again a drop as we continue to increase the lithium content. This broadening, along with the feature centred at 470 nm is attributed to the previously discussed formation of defect sites, leading to a degradation of the optical quality of the films. This enhanced 'green' emission seen in the PL measurement, and also the broadening of the absorption peak seen in the UV-Vis data is similar to that witnessed during the growth of films utilising other growth methods and is often attributed to defects such as zinc excesses or oxygen deficiencies. The root cause of the green emission seen in such films is still remains a topic of discussion [36]. A corresponding trend is seen in the extracted optical bandgap where a minimum value is noted for the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio film, again a typical feature of zinc rich or oxygen deficient films.

6.2.3 Surface analysis of Li-doped ZnO thin-films

The surface morphologies of both the undoped and Li-doped ZnO films were examined using atomic force microscopy over a 1 μm^2 area (Fig 6.5). Measurements were taken from both within and outside of the channel region of the fabricated transistors, illustrated here are measurements from within the channels. Phase and topography images shown for films utilising 0, 1 and 4% $[Li^{+1}]/[Zn^{+2}]$ ratio show a clear trend, where the grain size increases with increasing lithium concentration, approaching values close to double the actual film

thickness (~30 nm). This suggests the grains can be thought of as singular platelets, rather than spherical grains.

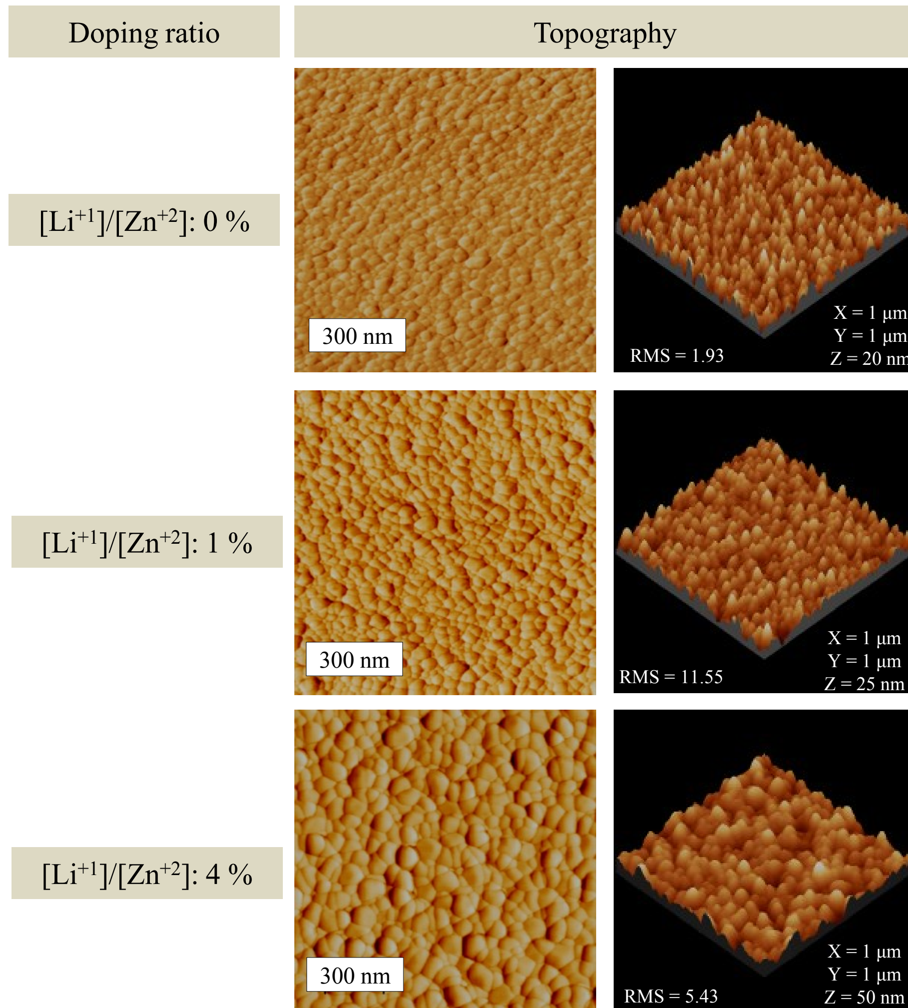

Figure 6.5: Atomic force microscopy images showing evolution of Li-doped ZnO films deposited as a function of $[Li^{+1}]/[Zn^{+2}]$ ratio. A noticeable increase in the grain size is clearly visible with increasing lithium content.

Statistical analysis of the measured topography images yields a trend indicating increasing grain size with increasing lithium content, average grain size is seen to increase from 22 nm to 60 nm corresponding to an increase in the $[Li^{+1}]/[Zn^{+2}]$ ratio (in solution) from 0 to 4%. The surface root mean square (RMS) and average roughness initially increase with increasing lithium content (Fig 6.6), reaching a maximum value of 11.55 nm and 9.83 nm respectively, at the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio. However as the lithium content is further increased, so the roughness,

both RMS and average, appears to reduce. Height distribution graphs (not shown) for all films show a Gaussian shape distribution. The significant increase in grain size corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio is of particular interest here, as this reduces the grain boundary density across the device channel, this appears likely to be the main contributing factor in the improved charge carrier mobility seen in device performance.

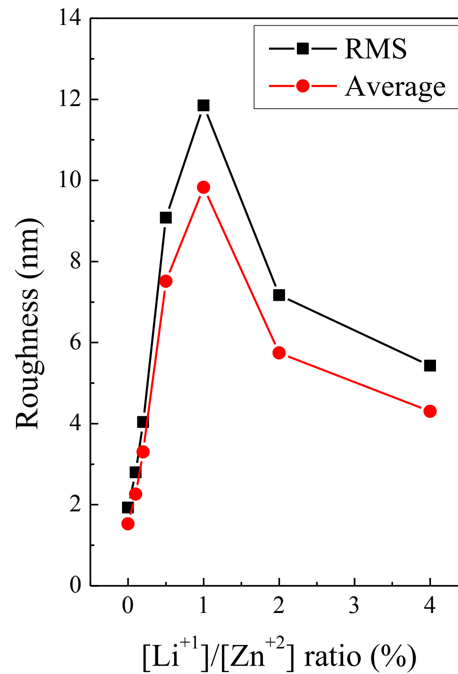

Figure 6.6: Root mean square (RMS) and average roughness of Li-doped ZnO films deposited on SiO_2 as a function of $[Li^{+1}]/[Zn^{+2}]$ ratio, with peak value corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio in both cases.

6.2.4 Structural analysis of Li-doped ZnO thin-films

XRD experiments were conducted on films deposited on glass substrates at a deposition temperature of 400 °C, and across the $[Li^{+1}]/[Zn^{+2}]$ doping ratios discussed previously (Fig 6.7). The tail end of the broad band ending at ~38° corresponds to the glass substrate. All films show a strong diffraction peak at 34.6°, and also a smaller peak at 63.05° that can be referenced to the (002) and (103) planes of reflection of a ZnO powder

reference (available commercially) indicating the polycrystalline nature of the films [37].

The strong (002) reflection suggests highly textured films with orientation aligned to the c-axis and perpendicular to the substrate surface. These diffraction patterns and orientation are typical of ZnO thin-films grown by spray pyrolysis and as well as other methods [21, 22, 38]. Likewise similar preferred orientation is often seen in the growth of numerous other nano-structures of ZnO, although not always along the same axis [39-41].

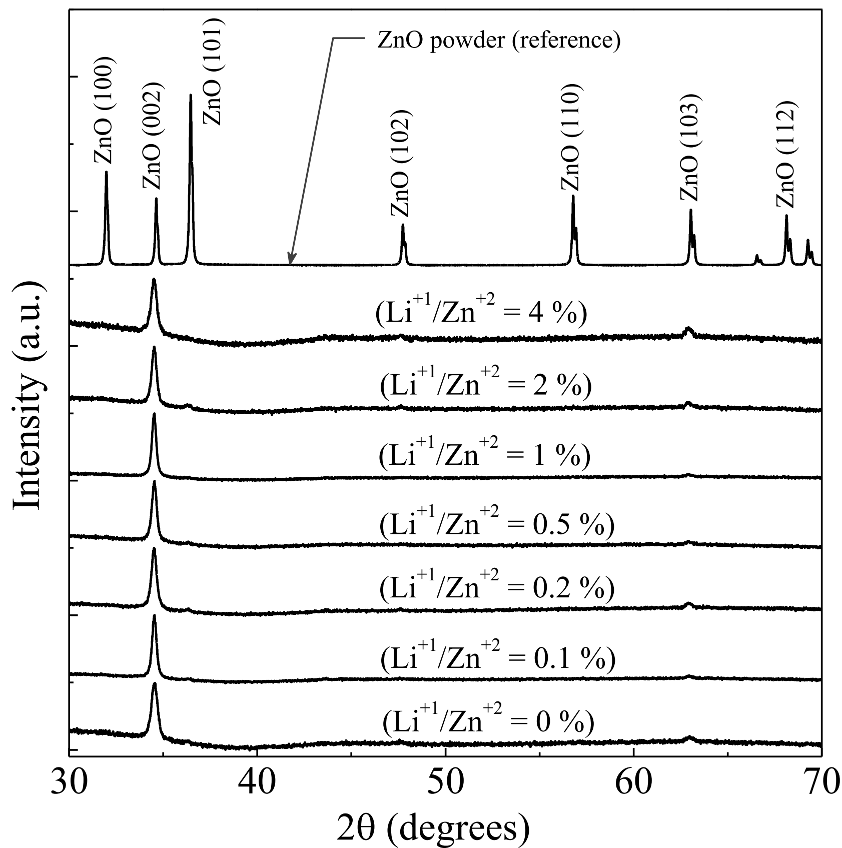

Figure 6.7: X-ray diffraction of Li-doped ZnO films of varying $[Li^{+1}]/[Zn^{+2}]$ ratios deposited on corning glass. A reference pattern of commercially available ZnO powder is also included.

The average crystallite domain sizes, were calculated using the Scherrer formula [42] utilising the (002) and (103) peaks from the XRD

measurement data shows the average crystallite size reaches a maximum value of ~39 nm at the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio level with a drop in crystallite size as we decrease or increase the lithium content during the deposition process (Fig 6.8(a)). The interplanar spacing d_{HKL} was also calculated for both the (002) and (103) planes of reflection for all films (Fig 6.8(b)). The same trend is seen in the evolution of these parameters, where maximum values are seen for the 1% $[Li^{+1}]/[Zn^{+2}]$ ratio, calculated to be 2.596 Å and 1.476 Å respectively.

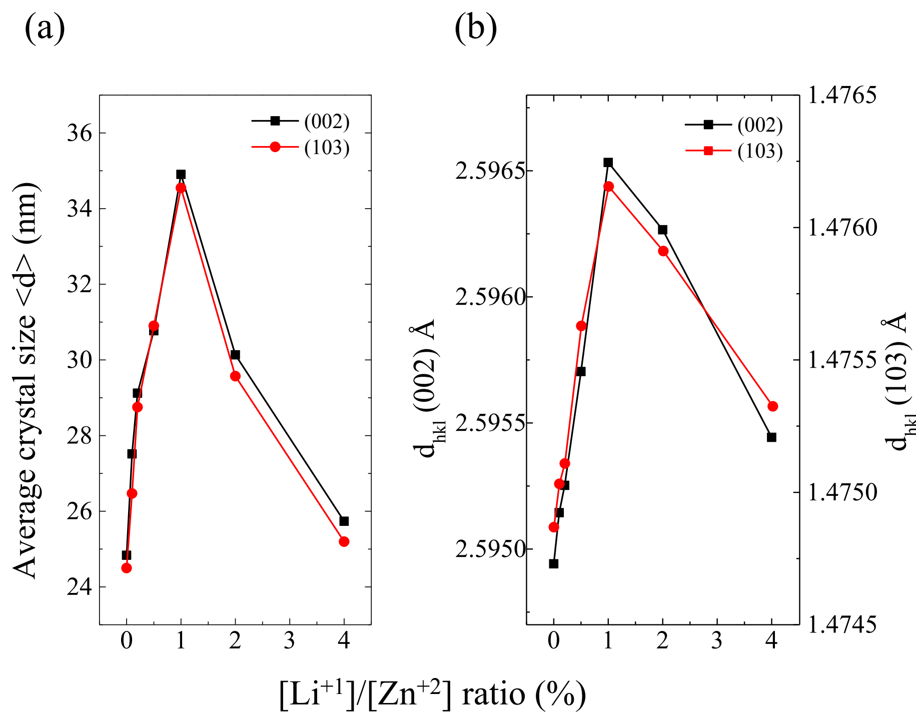

Figure 6.8: (a) Average crystallite size, calculated from (002) and (103) planes of reflection, showing peak size corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio and (b) interplanar spacing d_{HKL} calculated for both (002) and (103) planes, also showing maximum spacing corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio.

The lattice parameters *a, c* and *u* were calculated for all lithium concentrations with values reaching a maximum of 3.263 Å, 5.193 Å and 0.318 c units respectively for the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio (Fig 6.9) . Clearly from all of the data discussed the overriding trend denotes an increase in the zinc oxide crystal size corresponding to a maximum for

the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio. This trend fits well with that seen in the in the AFM data, where clearly the influence of the lithium is having a significant effect on the crystal morphology and quality.

For all films incorporating lithium during the deposition process, there appears to be no diffraction peaks that could be correlated to the presence of any lithium related compound, it is therefore possible that the films consist entirely of a ZnO phase.

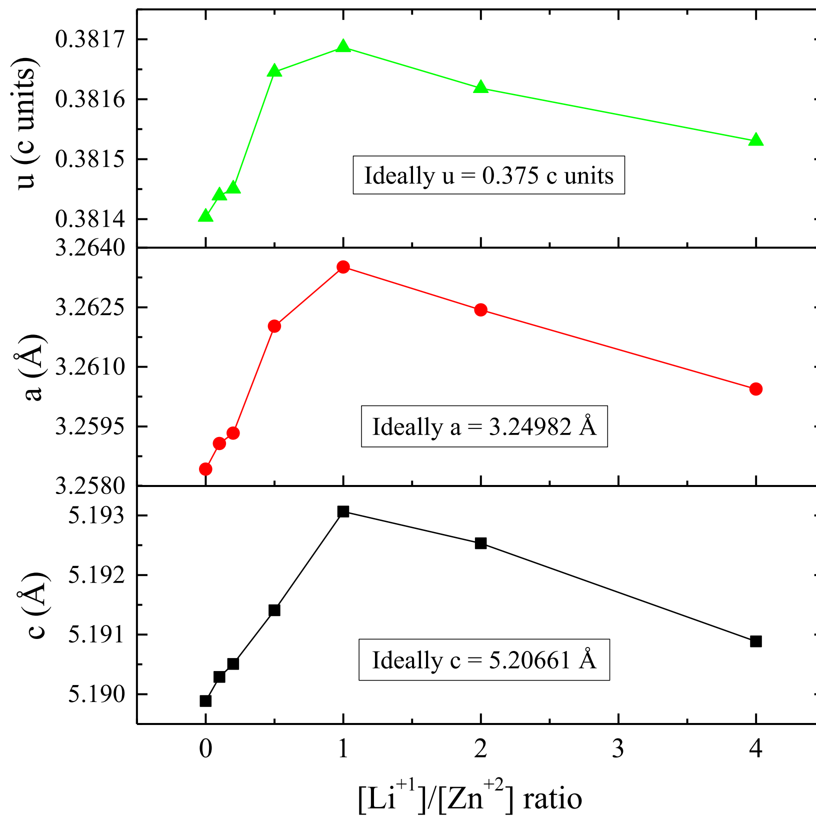

Figure 6.9: Lattice parameters *a, c* and *u* for Li-doped ZnO thin films, showing peak sizes for all parameters corresponding to the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio.

6.2.5 C-V characteristics of Li-doped ZnO TFTs

To investigate the electronic quality of spray pyrolysed lithium doped zinc oxide films, thin-film transistors were fabricated using a number of different architectures. Coplanar bottom-gate devices were fabricated utilising gold contacts, but unfortunately the performance was limited due to the high work function of the gold, as discussed in section 5.2.6.

although the performance of the these gold contact devices was still considerably better than that seen in amorphous silicon, aluminium contact devices performed better yet, therefore the following discussion will be limited to the aluminium contact devices.

The staggered bottom-gate devices were fabricated using substrates comprising of a silicon substrate, on top of which is a thermally grown 400 nm dielectric. Source and drain contacts are deposited by thermal evaporation after the deposition of zinc oxide, to a thickness is ~30 nm. Device channel dimensions range from 20 μm to 200 μm in length and 500 μm to 1500 μm in width. The silicon substrate is heavily p-type doped and acts as the gate contact. All devices were characterised under vacuum at room temperature, and under dark conditions.

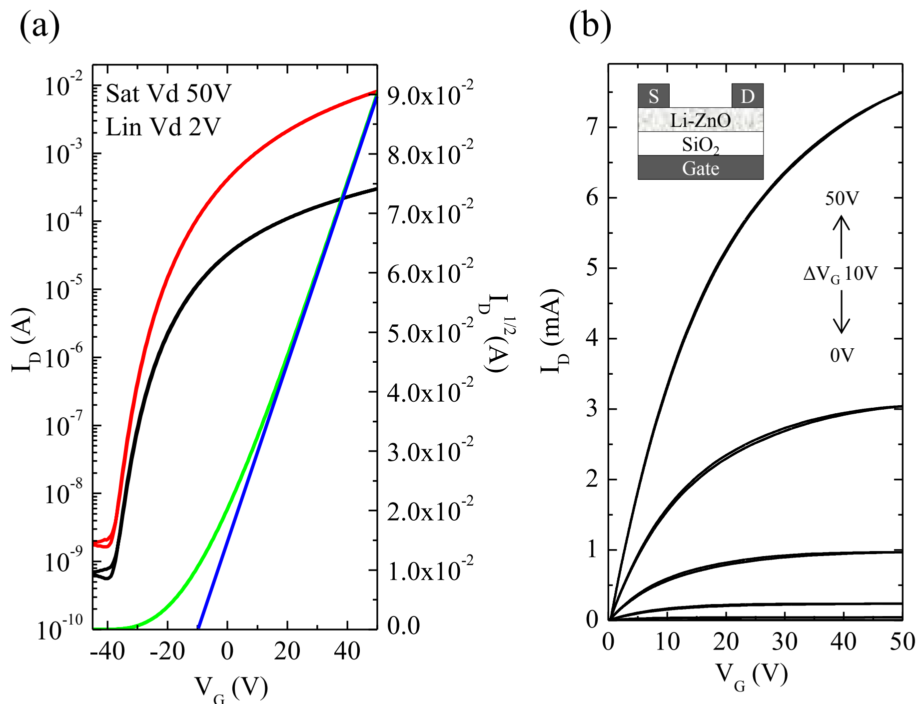

Figure 6.10: (a) Transfer and (b) output characteristics of a staggered bottom gate transistor (see inset) with channel dimensions of 30 μm length, and 1000 μm width. Deposited at 400 °C and using an optimised 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio.

The devices show behaviour that is typical of ZnO based transistors, as illustrated in the transfer (Fig 6.10(a)) and output (Fig

6.10(b)) curves of a typical device. This particular device has a channel width of 1000 µm and channel length is 30 µm, and utilises the optimum $[Li^{+1}]/[Zn^{+2}]$ doping ratio of 1%. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~44 cm^2/Vs, the $I_{D(on)}/I_{D(off)}$ ratio is ~10^7 and the threshold voltage, V_T, is estimated to be -10.7 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 1.77 *V/dec*. In terms of charge carrier mobility, the highest performing devices during this work have reached as high as ~54 cm^2/Vs, at the shortest 20 µm channel lengths.

When viewing device performance as a function of $[Li^{+1}]/[Zn^{+2}]$ doping ratio and also as a function of channel length, there is an observable trend in the performance in terms of charge carrier mobility (Fig 6.11). It is clear that as the ratio approaches the 1% doping level there is an increase in the charge carrier mobility. However, beyond this 1% ratio there is a drop-off in the performance of the devices. In terms of device channel length, it can be seen that as the channel length becomes smaller, so the charge carrier mobility also begins to increase.

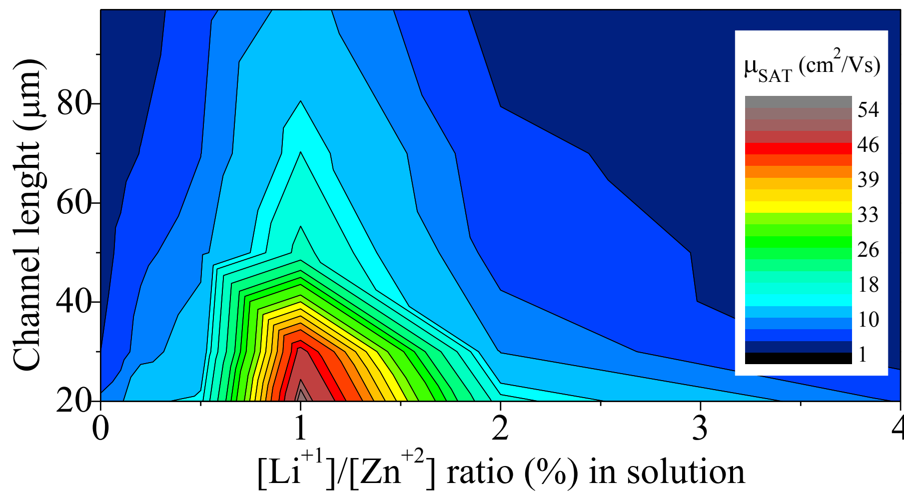

Figure 6.11: Contour plot illustrating the charge carrier mobility (in saturation) as a function of channel length and also $[Li^{+1}]/[Zn^{+2}]$ doping ratio.

When compared to undoped ZnO devices this accounts for a significant performance increase, typically doubling the charge carrier

mobility for longer channel lengths, whilst an almost three fold improvement is seen for shorter channel devices. Other device parameters are also improved, or to some extend affected by the inclusion of lithium during the deposition process (Fig 6.12). Typically there is an increase approaching one order of magnitude in the $I_{D(on)}/I_{D(off)}$ ratio of the devices utilising the optimum 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio, with non-doped devices having values of ~10^6-10^7, and lithium doped devices having values of ~10^7-10^8. This improvement is seen across all device geometries and does not appear to have any dependence on channel length.

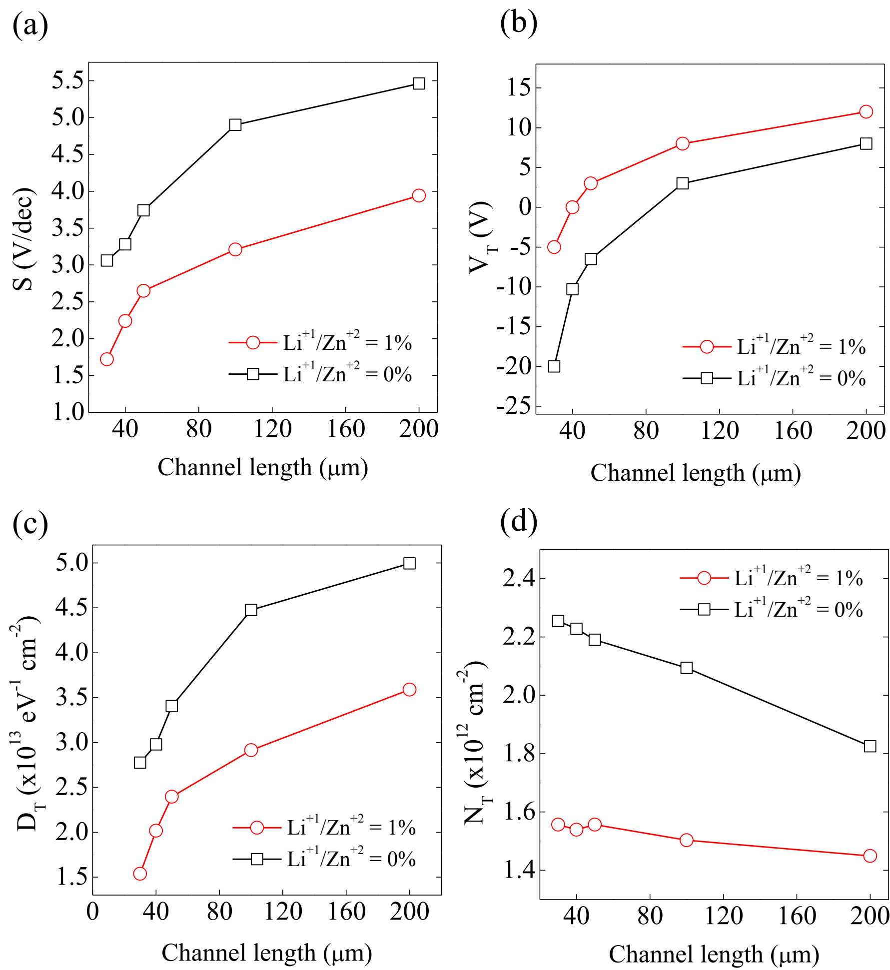

Figure 6.12: Comparison between undoped and 1% Li-doped ZnO TFT parameters. (a) Subthreshold slope (b) threshold voltage from extrapolation of $\sqrt{I_{Dsat}}$ (c) trap concentration per unit energy, D_T, and (d) interface electron surface trap density, N_T.

Both the subthreshold slope (Fig 6.12(a)) and threshold voltage (Fig 6.12(b)) are significantly affected by the inclusion of the lithium. The subthreshold slope becomes significantly steeper for devices fabricated using the 1% [Li^{+1}]/[Zn^{+2}] doping ratio, whilst the threshold voltage is shifted in a positive direction for the same devices. In both cases there appears to a dependence on the channel length.

From both the subthreshold slope, and also the threshold voltage and on voltage (not shown), we can infer some details of the nature of the trapping mechanisms from within the different films. Using the methods discussed in section 2.2.8 it is possible to extract firstly an estimation of the trap concentration per unit energy, D_T (Fig 6.12(c)) using the subthreshold slope [43]:

$$D_T = \frac{C_G}{e^2}\left(\frac{eS}{kT\ln(10)} - 1\right) \qquad [6.1]$$

Secondly it is possible to extract the interface electron surface trap density, N_T (Fig 6.12(d)) using the threshold and on voltages [44]:

$$N_T = \frac{C_G|V_T - V_{ON}|}{e} \qquad [6.2]$$

From the data it is clear the inclusion lithium is reducing the number of trap states in both cases.

In the case of D_T, it is likely that the inclusion of lithium is reducing the number of trap states situated at the grain boundaries, leading to the reduced calculated trap concentration per unit energy. This would be expected to some degree as the inclusion of lithium during the deposition process also sees a dramatic increase in both the grain and average crystallite sizes, reducing the grain boundary density across the device channel length. This also explains the dependence on channel length in both the doped and undoped devices, with D_T decreasing with decreasing channel length due, once again, to the reduced grain boundary

density across the channel. Examining N_T there is similar reduction seen with the 1% $[Li^{+1}]/[Zn^{+2}]$ doped devices, indicating the inclusion of lithium during the deposition process is having some positive effect on the zinc oxide to silicon dioxide interface morphology.

In general the improvement in the lithium doped devices is attributed to the reduction in grain boundary density across the device channel, minimising the effect of grain boundary limited transport. From the AFM and XRD data it clear that as we approach the 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio, so the grain and crystallite size reaches their maximum, leading to the reduction of grain boundaries across the device channel. The same reduction can be achieved by simply reducing the channel length. Interestingly, this would suggest that further reducing the channel length could possibly lead to further enhancement of the device performance. Unfortunately, this was not possible with the masks currently used for the deposition of the aluminum source and drain contacts. Devices fabricated using the photolithographically defined gold source and drain contacts did have channel lengths as low as 1.5 μm, with these devices there was a similar trend associated with decreasing channel length, but overall the performance of these gold contact devices was still poor when compared to their aluminum contact counterparts. Again the influence of the high work function of the gold contact appears to have an overbearing effect on the device performance in this instance.

There is no clear evidence of the presence of any lithium or lithium related compound in the deposited films. Possibly the use of secondary ion mass spectrometry (SIMS) may help at least identify if there is any lithium present within the films, but has not been performed to date. Lithium is used extensively in metallurgy, having a number functions. Of particular interest is its use in metal alloys, specifically aluminum alloys for precipitation hardening [45, 46]. Here lithium is used to help impede the movement of dislocations, or defects in a crystal's lattice during the crystalline growth process. It may be possible that lithium has some similar effect on the growth process of spray pyrolysed zinc oxide, and may be adjusting the nature of the nucleation sites at the semiconductor/dielectric interface.

6.3 Beryllium doped zinc oxide thin-film transistors

This section discusses the use of beryllium as a dopant. The introduction of beryllium, utilising the same methodology as used previously for lithium, allows to some extent the control of the threshold voltage, V_T[47]. By controlling the relative ratio of beryllium to zinc metal ions within the precursor solution during the deposition process it is possible to adjust some properties of the crystalline structure, leading to a change in device performance, specifically threshold voltage. It can be seen from much of the work already demonstrated within this thesis that transistors based on zinc oxide often tent to exhibit a somewhat negative shift in their threshold voltages, particularly this is evident in shorter channel length devices. Quite often this is attributed to an excess number of free charge carriers present within the bulk of the films, the cause of which is often said to be due to non-stoichiometry of the films, which can be made worse by excessive film thickness. Therefore, any method that helps control this behaviour could be of much benefit, as it should enable the design and fabrication of better performing integrated circuits. Some previous efforts have been made toward controlling the threshold voltage of ZnO based TFTs, including oxygen doping and adjustment of film thickness in an attempt to reduce the effects of the bulk charge carriers, whilst the use and effects of alternative dielectrics has also been investigated [25, 27-29]. To the best of the author's knowledge there are no other examples whereby an extrinsic dopant has been used to specifically control the threshold voltage of ZnO TFTs.

Numerous films were prepared for material characterisation and device fabrication and testing. For transistor fabrication, the spray pyrolysed ZnO based films were deposited on SiO_2 (400 nm) on Si, followed by a thermal evaporation of aluminium source and drain contacts to create a staggered device structure. Glass substrates were used for the deposition of films used for XRD measurements, whilst AFM measurements were performed from within the channels of the films used for transistor measurements. As with all previous work, during the deposition process, spraying masks are used to isolate the deposition to

as small an area as possible, in order to minimise the gate current leakage that can occur when the semiconductor deposition encroaches around the substrate edge.

6.3.1 Precursor materials and doping method

As with previous work, numerous precursor materials were trialled as a suitable source of beryllium for the preparation of the precursor solutions. As methanol combined with zinc acetate has already proven to provide the best results, the prime consideration was the suitability of the chosen precursors with these materials. For this work it was found that the use of beryllium acetylacetonate (Fig 6.13), combined with methanol as the solvent, provided the best means toward a stable soluble solution which is miscible with the zinc acetate and methanol parent combination.

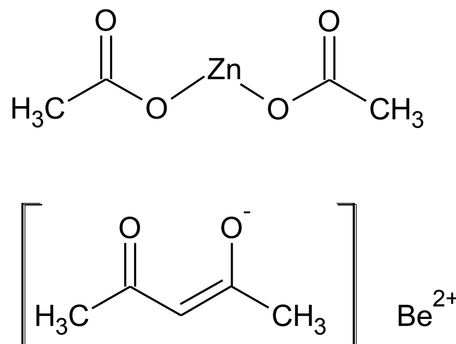

Figure 6.13: Chemical structure of zinc acetate and beryllium acetylacetonate, used for the preparation of precursor solutions. Liner formula: $(CH_3CO_2)_2Zn$ and $[CH_3COCH{=}C(O\text{-})CH_3]_2Be$ respectively.

The doping is once again achieved using the same method as used with lithium doped ZnO films. Solutions of 0.1M were prepared separately for each precursor material and were left to fully dissolve for 30 minutes. Following this the two solutions were blended according to the required $[Be^{+2}]/[Zn^{+2}]$ ratios, and left to stir for at least a further 30 minutes, ensuring a homogeneous mixture. For the work reported in this experiment, $[Be^{+2}]/[Zn^{+2}]$ ratios of 0, 0.1, 0.2, 0.5, 1% were used.

Previous experiments were carried out using coarser ratios, however it was found during these experiments that beyond a 2% $[Be^{+2}]/[Zn^{+2}]$ ratio device performance suffered dramatically.

6.3.2 Surface analysis of Be-doped ZnO thin-films

The surface morphology of the films was investigated by AFM (Fig 6.14). Images were taken from within the channels of fabricated devices. The phase and topography shows a dramatic reduction in the grain size of the films following the introduction of beryllium during the deposition process.

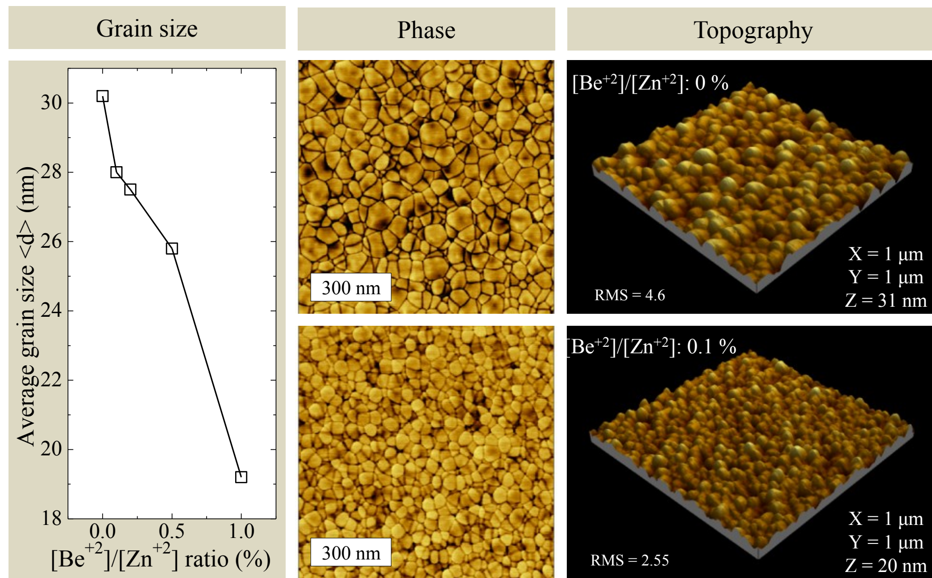

Figure 6.14: AFM images of undoped ZnO and 0.1% $[Be^{+2}]/[Zn^{+2}]$ Be-doped ZnO films deposited by spray pyrolysis at 400 C. Topography (right) and phase (centre) images taken from within the device channels. Grain size analysis (left) as a function of $[Be^{+2}]/[Zn^{+2}]$ doping ratio.

A corresponding change in the surface RMS roughness is also seen, where the roughness reduces from 4.48 nm for the undoped film, down to a value of 2.61 for the 1% $[Be^{+2}]/[Zn^{+2}]$ ratio doped film. Statistical analysis was performed on the topography images In an attempt to extract some quantitative measure of the grain size evolution

as a function of beryllium content (Fig 6.14 (left)), and it can be seen that with increasing beryllium content the grain size reduces for an initial value of 30.2 nm for the undoped film, to a value of 19.2 nm for the 1% $[Be^{+2}]/[Zn^{+2}]$ ratio doped film. For all films the height distribution graphs (not shown) follow a Gaussian line shape.

6.3.3 Structural analysis of Be-doped ZnO thin-films

To help establish a better understanding of how beryllium contributes to the structural characteristics of the deposited films, XRD experiments were conducted on films deposited on glass substrates (Fig 6.15). Measurements were taken of undoped and doped films with a $[Be^{+2}]/[Zn^{+2}]$ ratio range of 0 to 1%.

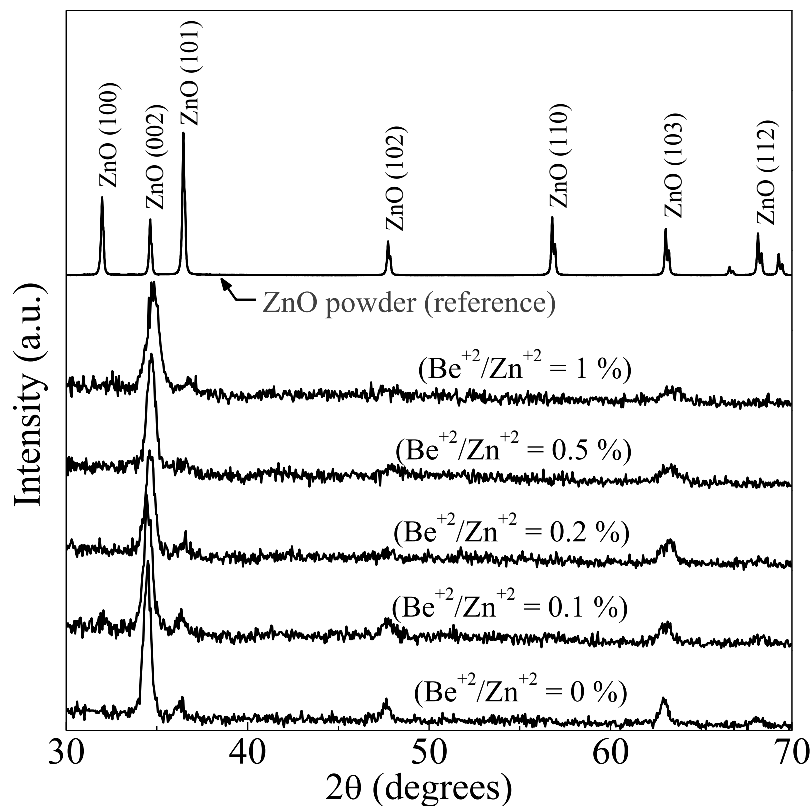

Figure 6.15: X-ray diffraction of Be-doped ZnO films of varying $[Be^{+2}]/[Zn^{+2}]$ ratios deposited on corning glass. A reference pattern of commercially available ZnO powder is also included.

The diffraction patterns can be referenced to the (002), (102) and (103) planes of reflection of the XRD patterns of a ZnO hexagonal-wurtzite powder reference (available commercially), indicating the polycrystalline nature of the films [37]. As is the case with the previous ZnO based films deposited by spray pyrolysis, these films also appear to be textured, or preferentially orientated. Where beryllium has been used during the deposition process there appears to be no beryllium related peaks visible in the diffraction patterns.

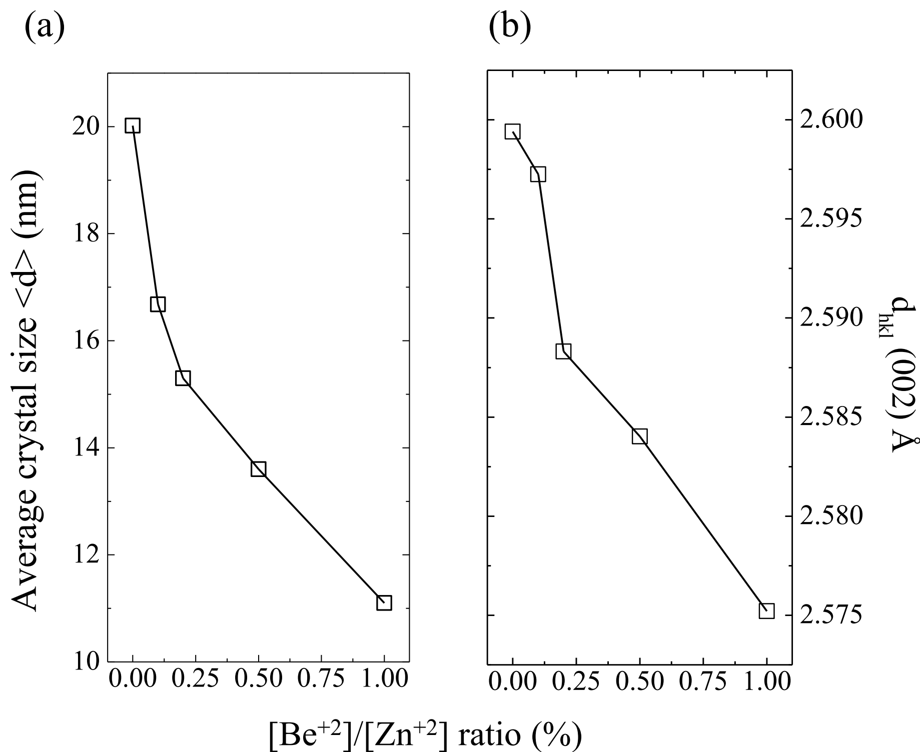

Figure 6.16: (a) Average crystallite size, calculated from (002) plane of reflection, showing reduction in crystallite size corresponding to increasing $[Be^{+2}]/[Zn^{+2}]$ doping ratio and (b) interplanar spacing d_{HKL} calculated for both (002) plane, also showing decreasing spacing corresponding to increasing $[Be^{+2}]/[Zn^{+2}]$ doping ratio.

The crystallite domain sizes, extracted using the Scherrer formula [42], and using the (002) peak, shows the crystallite size to reduce dramatically with increasing beryllium content (Fig 6.16(a)), from an initial value 20 nm for the undoped film to a final value of 11.1 nm for the 1% $[Be^{+2}]/[Zn^{+2}]$ ratio. The interplanar spacing d_{HKL} also reduces

with increasing beryllium content (Fig 5.16(b)), reducing from an initial value of 2.5994 at for the undoped film, to 2.5752 at the 1% $[Be^{+2}]/[Zn^{+2}]$ ratio. Although there are no peaks that could correspond to BeO seen in the XRD data, the presence of such a phase could possibly exist within the films. Beryllium oxide itself has the same hexagonal wurtzite structure as ZnO, with smaller lattice constants of a = 2.697 Å and c = 4.377 Å when compared to that of zinc oxide, typically quoted to be a = 3.25 Å and c = 5.2 Å [48]. It is reasonable to suggest that the presence of beryllium oxide may well have some influence on both the size of the grain and crystallite size seen in the AFM and XRD analysis.

6.3.4 C-V characteristics of Be-doped zinc oxide TFTs

To investigate the electronic quality of spray pyrolysed Be-doped ZnO films, coplanar bottom-gate thin-film transistors were fabricated, comprising of a silicon substrate, on top of which is a thermally grown 400 nm dielectric. The ZnO based films were then deposited by SP, followed by the deposition of aluminium source and drain contacts by thermal evaporation. Contact thickness is ~30 nm, and device channel dimensions range from 20 μm to 200 μm in length and 500 μm to 1500 μm in width. The silicon substrate is heavily p-type doped and acts as the gate contact. All devices were characterised under vacuum at room temperature under dark conditions.

In general the performance of the devices is typical for ZnO based thin-film transistors. Transfer curve measurements of the devices (Fig 6.17(a)) exhibit excellent transport characteristics with high carrier mobility under saturation, μ_{sat}, and good $I_{D(on)}/I_{D(off)}$ ratios at ~10^7. Output curves show hard saturation with no superlinear behaviour (Fig 6.17(b)), indicating no charge injection issues. The charge carrier mobility, calculated in saturation, does increase with decreasing channel length, as is typical in spray pyrolysed polycrystalline ZnO transistors, yet the inclusion of beryllium only has a small effect on the charge carrier mobility until a critical point is reached, after which device

performance drops (Fig 6.18(a)). At the higher $[Be^{+2}]/[Zn^{+2}]$ ratio there was some degradation in device performance, particularly at the 1% doping ratio, and predominantly in the longer channel devices. It appears that a $[Be^{+2}]/[Zn^{+2}]$ ratio of ~0.5% is the tipping point where device performance is most compromised.

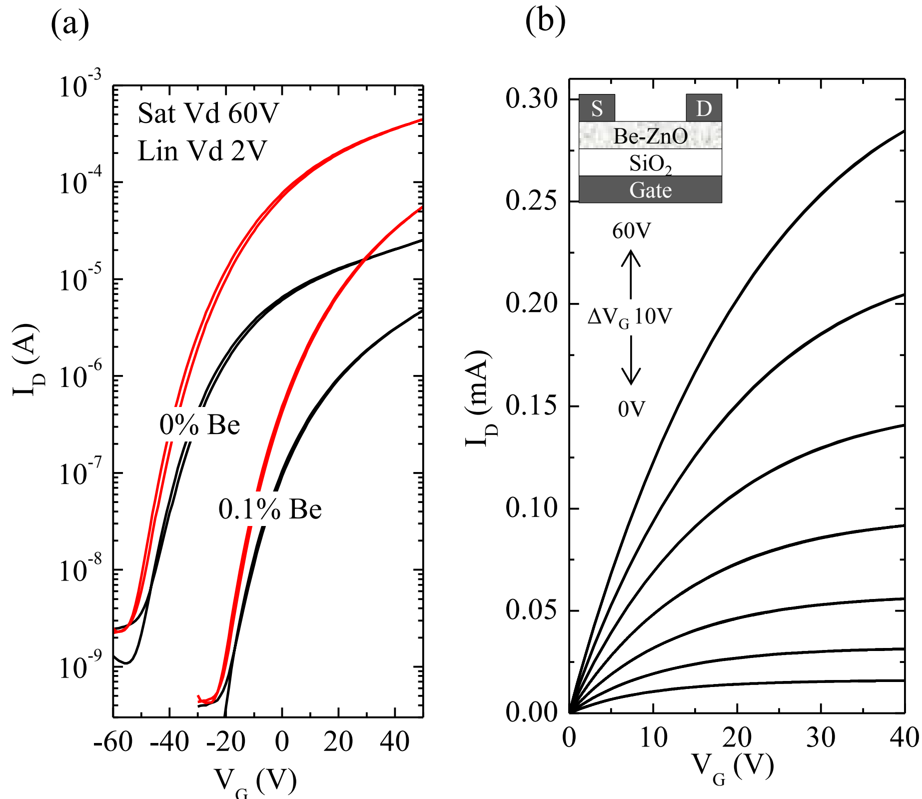

Figure 6.17: (a) Transfer characteristics of staggered bottom gate (see inset) transistor utilising both 0% and 0.1% $[Be^{+2}]/[Zn^{+2}]$ doping ratio with channel dimensions of 30 μm length, and 1000 μm width, deposited at 400 °C and (b) output curves for 0.1% $[Be^{+2}]/[Zn^{+2}]$ doped device.

The most significant finding from the data is the shift in the threshold (Fig 6.18(a)) and turn on voltages (not shown) of the devices, coinciding increasing beryllium content. Specifically there appears to be a significant step with the initial inclusion of beryllium at the 0.1% a $[Be^{+2}]/[Zn^{+2}]$ doping ratio, after which the addition of more beryllium doesn't appear to significantly affect the threshold voltages further, and

serves mainly to reduce device performance overall. As the channel lengths shorten, so the threshold voltages become more negative, this is often the case with ZnO devices fabricated by spray pyrolysis, and is attributed to reduced interfacial trapping due to smaller channel dimensions.

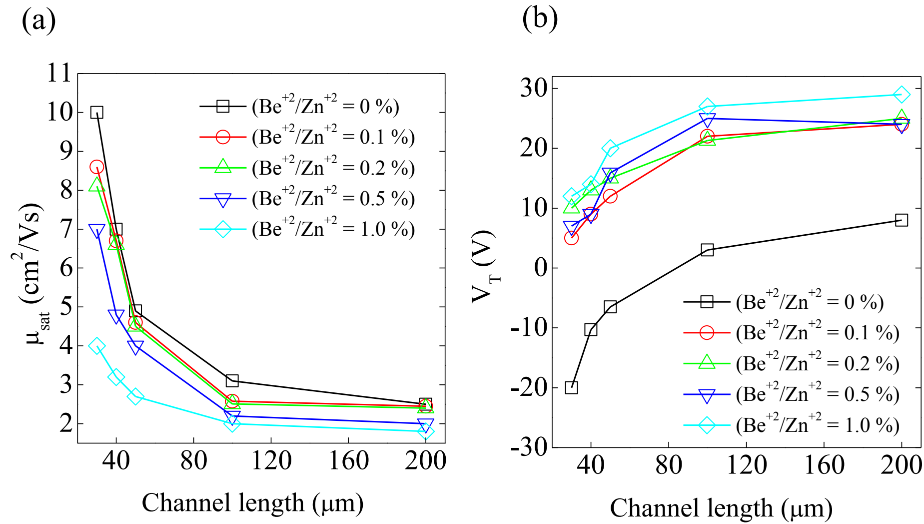

Figure 6.18: (a) Charge carrier mobility (in saturation) and (b) threshold voltage as a function of channel length and also [Be^{+2}]/[Zn^{+2}] doping ratio.

As with previous devices, the subthreshold slope and also the threshold voltage and on voltage were used to help understand the nature of the trapping mechanisms from within the different films. Trap concentration per unit energy, D_T (Fig 6.18(a)) was calculated using the subthreshold slope, and the interface electron surface trap density, N_T, (Fig 6.18(b)) using the threshold and on voltages. The trap states were studied as a function of the [Be^{+2}]/[Zn^{+2}] doping level, and are also shown as a function of channel length for the shorter channel lengths. At higher doping levels and longer channel lengths the device characteristics became too poor to enable an accurate analysis for all devices, so have been excluded.

In the case D_T, it appears that the inclusion of beryllium initially creates a significant reduction the number of trap states per unit energy,

after which there follows a gradual increase with increasing beryllium content. At present there is no definitive known cause as to how this mechanism is working, but it is suggested that initially for the 0.1% $[Be^{+2}]/[Zn^{+2}]$ doping level, the presence of beryllium is somehow screening or minimising the effect of trap states at the crystal grain boundaries. With increasing beryllium content the grain size reduces leading to increased grain boundary density within the device channel. It is suggested that as the grain boundary density increases, it begins to have an overwhelming effect on D_T, and any benefits seen from the inclusion of beryllium are lost. This then leads to an increase in the number of traps at the grain boundary interface, in turn contributing to a decrease in device performance. As a function of channel length, at each doping level there does appear to be a small increase in D_T, which is expected, however the overwhelming factor still remain to be the beryllium doping content.

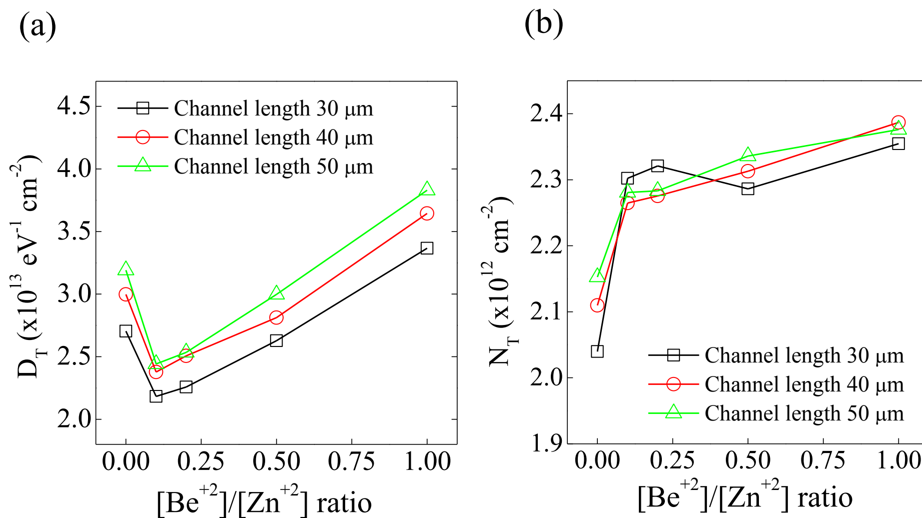

Figure 6.19: (a) trap concentration per unit energy, D_T, and (d) interface electron surface trap density, N_T as a function of channel length and also $[Be^{+2}]/[Zn^{+2}]$ doping ratio.

Examining N_T there is a different trend where there is an initial large increase in the areal trap state density for films deposited with the 0.1% $[Be^{+2}]/[Zn^{+2}]$ doping level, followed by a slower increase with increasing beryllium content. This is in agreement with the shift in

threshold voltages, suggesting the inclusion of beryllium is having some effect on the nature of the interface morphology, and that the root cause of the threshold shift may be due to the increased interface trap state density. There is no obvious dependence on channel length seen in this instance.

6.3.5 Unipolar circuits based on Be-doped ZnO TFTs

Minimal complexity is an essential criterion for fabrication of low-power microelectronic circuits with a high manufacturing yield [49-51]. Without the ability to accurately control important transistor parameters, such as threshold voltage, the need arises for more complex circuitry in order to compensate for such shortcomings. The close control we are able impose on the transistor threshold voltage characteristics through simple beryllium doping methods, offers one such method toward the fabrication of circuitry with minimal complexity.

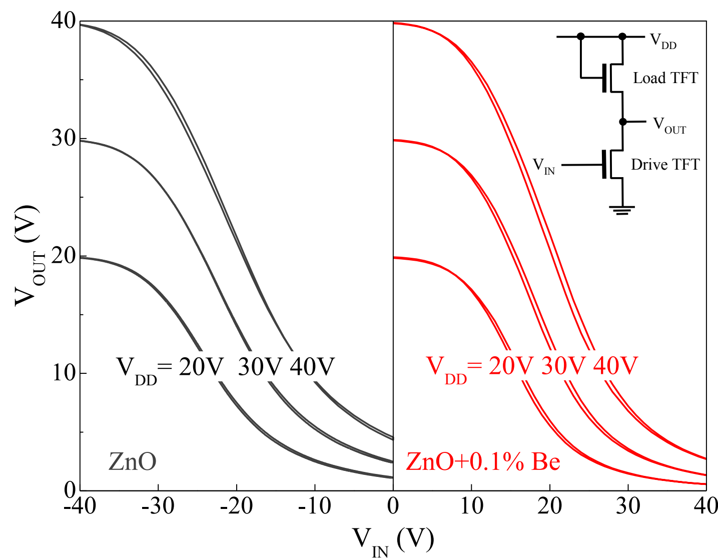

Figure 6.20: Transfer characteristics of unipolar inverters fabricated using transistors employing channel widths of 1500 µm and 1000 µm and channel lengths of 100 µm. Using 0.1% Be-doped ZnO devices (first quadrant) and undoped ZnO devices (second quadrant). Inset: inverter circuit structure employed.

Unipolar inverters were fabricated utilising the methods discussed in section 2.3.5 employing both un-doped and 0.1% $[Be^{+2}]/[Zn^{+2}]$ ratio doped ZnO TFTs (Fig 6.20(inset)). The inverter structure used in each case consists of two TFTs, utilising devices with identical channel lengths of 100 μm, and different channel widths of 1000 and 1500 μm for the load and drive device respectively. The transfer characteristics of inverters were measured at different supply voltages of 20, 30, and 40 V (Fig 6.20). Both the Be-doped and un-doped inverters exhibit voltage gains of ~2 at supply voltages of 40 V. When comparing the two sets of transfer curves the primary issue for concern is the negative input voltage required for effective switching of the un-doped inverter structure. The root cause of which is the negative threshold voltage of the component TFTs, specifically the drive transistor. By using fabricating inverters using devices whose threshold voltages are more positive, the inverter trip voltage, or switching point, is now in the first quadrant of the *Vout vs Vin* plot. This behavior is achieved with no significant effect on the inverter gain and with only an improvement in the transfer characteristics.

6.4 Conclusions

The combined use of facile chemical doping methods and spray pyrolysis have been used to deposit ZnO based thin films suitable for use in high performance TFTs and circuits.

The role of lithium has been investigated as a dopant for ZnO based TFTs. Through the use of a facile chemical blending process, Li-doped ZnO TFTs with charge carrier mobilities as high as 54 cm^2/Vs and excellent overall performance characteristics have been achieved. The physical properties of the deposited films have been investigated using number material and electronic characterisation techniques allowing a number of conclusions to be drawn. Improvements are seen in the crystalline quality the deposited films for specific $[Li^{+1}]/[Zn^{+2}]$ ratios leading to increased crystallite size coupled with increased grain size. The peak increase in grain and crystallite size corresponds with an increase in device performance, specifically charge carrier mobility as well as other device metrics. This suggests the reduction of grain boundaries across the device channel plays a significant role in device performance. Analysis of the trapping mechanisms within the doped and undoped films suggests that by reducing the number of the grain boundaries across the channel, there is a corresponding reduction in the trap concentration per unit energy, and that the interfacial trap density is also significantly reduces due to an improvement in the semiconductor/dielectric interface morphology.

The use of beryllium has also been demonstrated as a suitable dopant for ZnO, offering a simple method that enables the control of transistor threshold voltages. Spray pyrolysed ZnO transistors can often show slightly negative threshold voltages, therefore, being able to control the threshold voltage of a device without any degradation in performance is particularly useful when developing devices for use in integrated circuit applications.

The addition of beryllium during the deposition process sees a reduction in the crystallite size and also the grain size. Electrically, there is a significant positive shift in the transistor threshold voltages as the

beryllium is initially introduced, as the beryllium content is further increased there appears to be a stabilisation in the threshold voltage values. In terms of charge carrier mobility, with the initial introduction of beryllium there doesn't appear to be any significant drop in device performance, however as the $[Be^{+2}]/[Zn^{+2}]$ ratio increases beyond the 0.5% value, a drop in device performance is seen, in mobility as well as other parameters. Examining the trapping mechanisms within the doped and undoped films suggests the inclusion of beryllium is leading to a change in the semiconductor/dielectric interface morphology, in turn leading to an increase in the areal trap state density. It is this increase in the interface trap density that is suggested as the main cause for the shift in the transistor threshold voltages. Finally, inverter circuits were demonstrated, making use of the benefits offered through control of the transistor threshold voltages. These inverters show good performance characteristics, and through the use of Be-doped ZnO it has been possible to show how some of the shortcomings of undoped zinc oxide, specifically negative threshold voltages, can be overcome.

It has been the aim of this chapter to illustrate how spray pyrolysis can be used in conjunction with a facile chemical doping method to improve device performance, and also how it is possible to beneficially alter device characteristics, offering a low cost alternative to current thin-film transistor fabrication methods. The following chapter will discuss how spray pyrolysis can be utilised for the deposition of other oxide materials suitable for use as dielectric materials, and how these can be combined with what has already been discussed, offering a method toward the fabrication of low power thin-film transistors with extremely high performance.

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Chapter 7

High performance high-k dielectrics by spray pyrolysis

Abstract

Much of the work on solution processed oxide based transistors has focussed primarily on semiconductors, with significantly less attention paid to the dielectric materials being used. With the ever increasing requirement for low power technologies, the ability to utilise high-*k* dielectric materials alongside low cost deposition techniques will be crucial in the future. This chapter discusses the use of spray pyrolysis for the deposition of high-*k* dielectrics, specifically the use of zirconium, yttrium and aluminium oxide. Utilising these materials it has been possible to fabricate thin-film transistors with very low operational voltages, and through their combined use with lithium doped zinc oxide, discussed in the previous chapter, it has been possible to demonstrate spray pyrolysed transistors with charge carrier mobilities as high as 85 cm^2/Vs at operational voltages as low as 4V.

7.1 Introduction

In almost all fields of the electronics industry there is an ever increasing drive towards the production of goods with low energy requirements in both the manufacturing and end user phases. As an example, it estimated that 80-90% of the life cycle energy requirement of a typical laptop computer is expended during the manufacturing and end user phases, being split roughly evenly between the two [1]. Furthermore it is not difficult to see that a large proportion of the power consumption an item such as a laptop computer is consumed by the display [2]. Clearly, reducing operational power consumption is of very high importance, but also any method that can help reduce manufacturing energy costs is also very welcome. Without a doubt there are numerous sectors that will most likely benefit in the same manner, and with this in mind the use of low power oxide based electronics, combined with low cost and uncomplicated spray pyrolysis (SP) deposition methods, holds some promise in helping implement some of these energy savings.

The vast majority of work related to oxide based thin-film transistors, particularly those that are solution processed, has been performed using conventional dielectrics, specifically silicon dioxide (SiO_2). Of course there is good reason for this, namely the abundance of silicon in use across the electronics industry and the ease with which silicon dioxide dielectric layers can be thermally grown. However, there is only a small body of work dedicated solution processed dielectrics [3-5], with a further smaller body of work dedicated to oxide based thin-film transistors using solution processed dielectrics [6-9]. The net result of this is that the vast majority of work concerning zinc oxide (ZnO) thin-film transistors (TFTs) is based on devices operating at high voltages, which is less than ideal for the development of low power technologies. Therefore, in an attempt to circumvent this issue the work presented in this chapter is very much focussed toward the use of alternative high-*k* dielectric materials [8] with ultrathin layers [10, 11], which are suitable for low voltage transistor operation, whilst at the same time being compatible for use with the SP deposition method. The majority of those

oxide based TFTs that do use solution processed high-k dielectrics show relatively good performance with $I_{D(on)}/I_{D(off)}$ ratios between 10^3 and 10^6, charge carrier mobilities are generally between 1 to 15 cm^2/Vs, with some reaching as high as 28 cm^2/Vs [7, 8], typically these devices are working at voltages below 5 V and as low as 2 V [6-9].

In general, the most widely studied high-k dielectric materials have relative permittivity values between ~8 for aluminium oxide (Al_2O_3), and as high as ~40 for titanium dioxide (TiO_2) when compared to 3.9 for SiO_2, although there is some variation depending on deposition methods used [12]. Those most commonly studied include tantalum (Ta_2O_5) and TiO_2 [13-16], hafnium oxide (HfO_2) [17, 18], zirconium oxide (ZrO_2) [19, 20], Al_2O_3 [21, 22] and yttrium oxide (Y_2O_3) [23, 24] and silicates [14, 25], many of which find their use in commercial applications such as transistors and capacitors. HfO_2 in particular is one dielectric material that has been closely studied as a potential replacement for SiO_2 in the semiconductor industry [26]. Likewise Al_2O_3 and ZrO_2 have also been closely studied due to their good thermal stability and large band gaps [14, 27].

In almost all of the studies to date, device fabrication employs costly vacuum based techniques. SP as a deposition method offers a straightforward low cost alternative, capable of delivering high quality dielectric materials suitable for large area deposition with minimal cost and complexity. This chapter demonstrates how spray pyrolysed dielectric materials can be incorporated with the ZnO based semiconductors discussed in the previous chapters, to offer high performance low voltage TFTs suitable for a wide array of electronic applications. This work is split into two main areas. Firstly, ZnO based transistors utilising Al_2O_3 and Y_2O_3 are demonstrated, this is followed by work demonstrating optimised Li-doped ZnO TFTs utilising spray pyrolysed ZrO_2, and offering extremely high performance.

7.2 TFTs utilising spray pyrolysed Y_2O_3 and Al_2O_3 dielectrics

This first section discusses the use of SP as an alternative and promising method for the deposition of high quality dielectrics that are suitable for use with ZnO thin films. Specifically Y_2O_3 and Al_2O_3 have been deposited followed by a sequential deposition of ZnO, presenting a simple and quick method for the fabrication of high performance TFTs. Device performance, in terms of charge carrier mobility, is improved compared to the devices discussed in previous chapters where undoped ZnO was deposited on SiO_2. Other device parameters are similar, if not better than those seen in previous work. Operating voltages as low as 4 V are demonstrated due to the high relative permittivity values (~9.2 and ~16.2 for Y_2O_3 and Al_2O_3 respectively) when compared to SiO_2, with mobility values reaching as high as 34 cm^2/Vs.

To prepare the films for characterisation precursor aerosols were sprayed at a temperature of 400 °C onto a number of different substrates. In order to fabricate transistors, commercially available indium tin oxide (ITO) coated (~140 nm thickness) glass was patterned, followed by the deposition of the dielectric material then the semiconducting layer of ZnO, all by SP. The final step was the deposition of the aluminium source and drain contacts of ~30 nm thickness, yielding bottom contact coplanar devices. The process is discussed in a little more detail later in this chapter. To assess the dielectric properties of the Y_2O_3 and Al_2O_3, metal-insulator-metal (MIM) capacitors were fabricated, by once again using commercially available ITO coated glass, which in this instance had already been patterned by the manufacturer. The dielectric materials were deposited by SP across the entire substrate, followed by the deposition of gold contacts utilising a masks design specifically matching that of the bottom. Atomic force microscopy measurements (AFM) were performed on the films used for transistor measurements from within the transistor channels as well as outside of the channels regions of the devices. For the measurement of each deposited layer, additional substrates were added during the deposition process and removed

following whichever deposition was to be investigated. For extraction of the optical bandgap of the dielectric films, UV-Vis spectroscopy measurements were made on films deposited on β-phase quartz substrates. To examine the transparency of the complete films stack, measurements were taken on samples that were prepared alongside the device samples, but without the various masking and lithographic steps.

7.2.1 Precursor materials

In order to deposit Y_2O_3 and Al_2O_3 films a number of precursor materials were initially evaluated. The use of nitrates and various solvents would often lead to poor quality solutions, suffering from unwanted precipitates or simply poor device characteristics. It was found that the acetylacetonate complexes (Fig 7.1) proved to be the most suitable materials for precursor solution preparation, offering easy preparation as both materials dissolved in methanol (linear formula: CH_3OH). These films proved to be the highest quality when compared to those deposited using other precursor materials. As with previous work, solutions were prepared and left to stir for at least 30 minutes before deposition commenced, ensuring complete dissolution of the acetylacetonates.

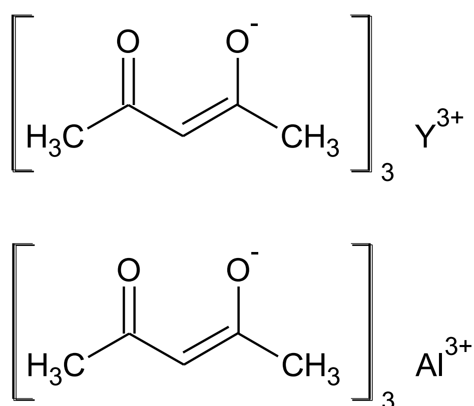

Figure 7.1: Chemical structure of yttrium acetylacetonate and aluminium acetylacetonate, used for the preparation of precursor solutions. Liner formula: $Y(C_5H_7O_2)_3$ and $Al(C_5H_7O_2)_3$ respectively.

One minor issue in each case was the molarity of the precursor solutions. Although the acetylacetonates do dissolve well in methanol, solutions could not be prepared at the same levels of molarity as they were when using zinc acetate, thus solutions of 0.015M had to be prepared leading to longer spraying times, and requiring the use of more precursor solution. Simply, this meant using the same process where a two minute period was left between each coat, although 25 coats were applied for the deposition of Y_2O_3, whilst 35 coats were applied for the deposition of Al_2O_3. The feed rate of the solution was also increased to 2.5 ml/min. Generally speaking, this is still a minor issue when considering the entire deposition process is automated, and has very low material cost. Exactly the same methods as used in the previous chapters were used for the preparation of the ZnO precursors.

7.2.2 Optical properties of Y_2O_3 and Al_2O_3 thin-films

The optical properties of both dielectric materials were investigated using UV-Vis spectroscopy, measured between 200 and 800 nm, as were the properties of the entire film stack (Fig 7.2). Films were deposited at a temperature of 400 °C, and film thickness was calculated to be approximately 107 nm and 163 nm for Y_2O_3 and Al_2O_3 respectively, which is in good agreements with values extracted experimentally by spectroscopic reflectometry (SR). As with previous work the zinc oxide layer was deposited to a thickness of ~30 nm, whilst the indium tin oxide gate layer was ~140 nm in thickness.

The optical transmittance through the indium tin oxide, high-*k*, and zinc oxide stack shows a very high level of transparency across the visible spectrum and there is no absorption onset until ~430 nm, with the average transmission in this region being ~82%. This holds much promise for future work on entirely transparent spray pyrolysed thin-film transistors. From the dielectric films deposited individually on β-phase quartz substrates it has been possible to extract the optical bandgap for each film. The extracted optical bandgaps (inset) are calculated to be

~5.62 eV and ~5.78 eV for Al_2O_3 and Y_2O_3 respectively, which are in good agreement with those reported in the literature [28, 29].

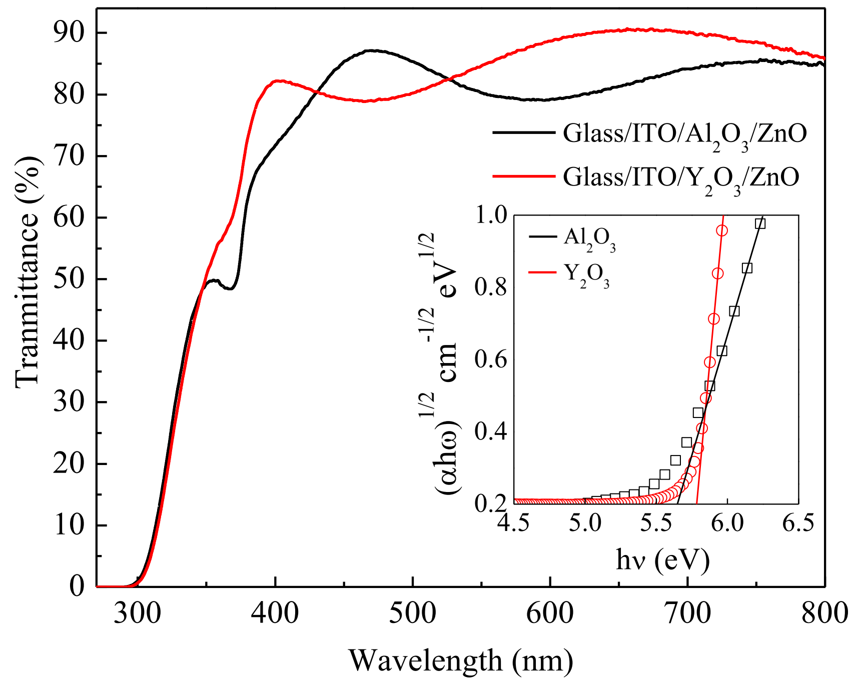

Figure 7.2: Optical transmittance of stacked ITO, dielectric, ZnO films deposited on glass and (inset) optical bandgap extracted using Tauc plots for films deposited on β-phase quartz substrates.

7.2.3 Surface analysis of Y_2O_3 and Al_2O_3 thin-films

The surface morphologies of the sequentially deposited films were analysed by AFM. The films were deposited alongside those used for device fabrication and consist of the same substrates, utilising ITO on glass. As each layer was deposited a substrate was removed for measurement purposes. For the sake of confirmation, the measurements were also performed in the channel region of the devices after they had been electrically characterises and were shown to have identical surface morphologies.

Measurement of the dielectrics alone on ITO, show grain like structure in both cases, with the average grain size calculated to be ~30 nm and ~50 nm for the Al_2O_3 and Y_2O_3 respectively. The root mean

square (RMS) surface roughness for Al_2O_3 and Y_2O_3 was found to be 2.33 nm and 2.96 nm respectively. The height distribution profile for the Al_2O_3 film shows a Gaussian distribution which differs from that of the ITO, which shows an asymmetric distribution toward the higher values.

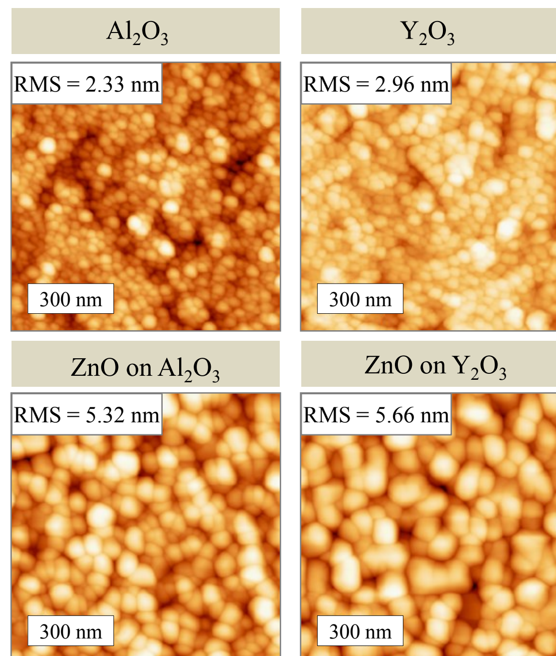

Figure 7.3: Atomic force microscopy images showing topography of Al_2O_3 and Y_2O_3 on ITO, followed by images of the final deposition of ZnO on each dielectric, all by SP.

A similar situation is seen with the Y_2O_3 films, although in this instance the films show an asymmetric line distribution toward the smaller values. In each case this suggests that there is no significant influence on the dielectric surface morphology from the underlying ITO layers, and rather the deposition process itself plays a more significant role in the final surface morphology. The higher surface roughness of the Y_2O_3 films are attributed to their polycrystalline nature, this is in contrast to the Al_2O_3 films which are amorphous. The latter has been confirmed by X-ray diffraction experiments showing the amorphous phase of the Al_2O_3 and the cubic phase for Y_2O_3 films, where an average crystallite size of ~5 nm was observed for Y_2O_3.

7.2.4 Capacitance spectroscopy of Y_2O_3 and Al_2O_3 films

The metal-insulator-metal (MIM) capacitors were measured by capacitance spectroscopy across a frequency range of 100 Hz to 10 MHz, whilst applying a 50 mV ac voltage to polarise the dielectric (Fig 7.2). The primary reason for this measurement is to extract an accurate measurement of the geometric capacitance, which in turn allows for the accurate extraction of mobility values for the fabricated TFTs. The measurements also help illustrate the maximum operating frequencies that may be expected from the working devices. Calculation of the dissipation factor gives some indication of the expected electrical loss rate though the dielectric at any given ac oscillation frequency. The lower the dissipation factor the better, as higher currents combined with too high a dissipation factor can lead to excessive heating and in turn shortened lifetime of the device.

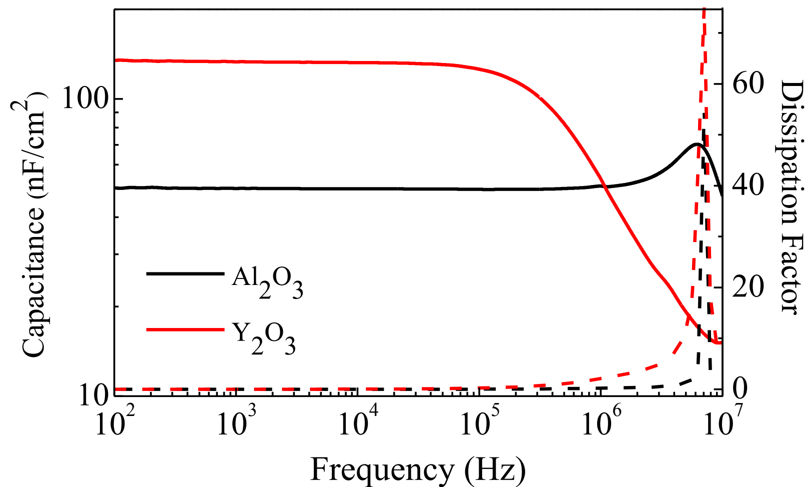

Figure 7.4: Capacitance (left ordinate solid line) and dissipation factor (right ordinate dashed line) as a function of frequency, measured between 100 Hz and 10MHz.

Example Bode plots show typical measurement data for both the Al_2O_3 and Y_2O_3 devices, showing stable capacitance values up toward the MHz range of operation (Fig 7.4 left ordinate). Geometric capacitance values extracted from these plots at 120 MHz are 50 nF/cm^2 and 133 nF/cm^2 for Al_2O_3 and Y_2O_3 respectively, and match well with

those calculated using the dielectric constants measured by spectroscopic ellipsometry. The resonance observed in the capacitance measurement of the Al_2O_3 dielectric between 6 MHz and 7 MHz is not known but is usually attributed to residual inductance within the device or ionic relaxation due to impurities etc. The dissipation factors (Fig 7.4 right ordinate) are low for both dielectrics with 0.09 and 0.01 for Al_2O_3 and Y_2O_3 respectively, with a peak at ~7 MHz in each case.

The current voltage characteristics of the MIM structures were also investigated. Both dielectric materials showed very low leakage current levels, with values typically lower than 100 nA/cm^2, when biased with voltages up to a maximum value of 6 V. Likewise the breakdown characteristics for both materials were excellent, with no breakdown observed until field strengths of 1.8 MV/cm were reached.

7.2.5 C-V characteristics of TFTs

To assess the quality and impact of the use of spray pyrolysed dielectrics when applied in ZnO TFTs, devices where fabricated utilising a less conventional method than used in previous chapters. Being able to use spray pyrolysis to deposit just the semiconducting layer is clearly a significant step toward low cost deposition methods for TFTs, however the benefits of this deposition method will be truly realised when all of the component parts of a TFT can be deposited in this way. Deposition of the gate dielectric, or insulator, is the next step.

In order to fabricate the transistors, commercially available indium tin oxide (ITO) coated (~140nm) glass was first patterned by using polyimide tape as a resist and a zinc oxide powder and hydrochloric acid as an etchant. This was done to form gate contacts with only the minimal surface area required in order to minimise the chance of any gate leakage current. Previously, devices had been fabricated without patterning, which although having no significant bearing on any of the other device characteristics, gate leakage was similar to that seen when using SiO_2 as a gate dielectric in combination with spray pyrolysis.

Patterning reduces the leakage current by several orders of magnitude, and whilst not essential it is at the very least a nice feature. Following the patterning step, the dielectric materials were deposited across the entire area by spray pyrolysis. The same spraying conditions and temperature used as with the deposition ZnO, with only adjustment to the number of passes made by the spying nozzle to compensate for the lower molarity of the precursor solutions. The next step was the deposition of the semiconducting layer of ZnO, following the methods discussed in previous chapters, and once again utilising specially fabricated spraying masks to help minimise the gate current leakage around the substrate edges. The final process required in the preparation of devices was to deposit the aluminium source and drain contacts by thermal evaporation to a thickness of ~30 nm, finally yielding bottom contact coplanar devices that are entirely transparent apart from the top contacts.

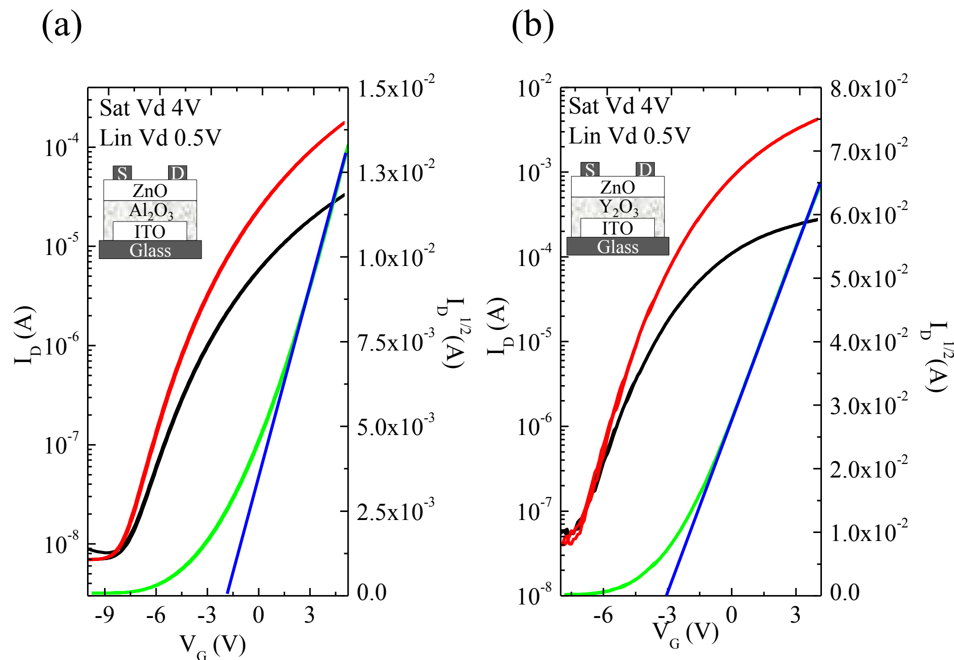

Figure 7.5: Transfer curves illustrating typical device characteristics for devices fabricated utilising (a) Al_2O_3 and (b) Y_2O_3 spray pyrolysed gate dielectrics. A Staggered bottom gate transistor (see inset) structure is utilised, with channel dimensions of 20 µm length, and 1000 µm width in each case.

The measured devices exhibit excellent operating characteristics that are typical of those shown in the previously discussed ZnO devices

deposited by spry pyrolysis, but most significantly operating at very low voltages of ~4 V. These operating voltages are typically one tenth of those seen when utilising conventional SiO_2 dielectrics.

The illustrative transfer curves shown for TFTs based on the Al_2O_3 dielectric (Fig 7.5(a)) offer the best outright performance in terms of mobility. Channel width is 1000 μm whilst channel length is 20 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~34 cm^2/Vs which is very high for undoped ZnO. The $I_{D(on)}/I_{D(off)}$ ratio is ~10^5 and the threshold voltage, V_T, is estimated to be -2.2 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 1.43 *V/dec*.

The example transfer curves shown the TFTs based on the Y_2O_3 dielectric (Fig 7.5(b)) also shows very good performance, but not quite as impressive as that seen with the Al_2O_3 dielectric. Channel width once again is 1000 μm whilst channel length is 20 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~7 cm^2/Vs. The $I_{D(on)}/I_{D(off)}$ ratio is also ~10^5 and the threshold voltage, V_T, is estimated to be -2.98 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 1.52 *V/dec*. In both cases the output curves show no superlinear behaviour, suggesting there are no charge injection issues, whilst the device clearly saturate well.

The discrepancy between the two charge carrier mobility values is attributed to the polycrystalline nature of the Y_2O_3 dielectric, specifically the interface morphology and lattice mismatch between the dielectric and the semiconductor. These kinds of interfaces have been studied before by experimental and theoretical means for ZnO and ytrria-stabilised zirconia interfaces, and demonstrate large band offsets and a small lattice mismatch, leading to similar conclusions [30].

In general the use of these spray pyrolysed dielectric materials has allowed the fabrication of very high performance ZnO thin-film transistors with extremely low operational voltages. The combination of this low cost facile processing method and low power performance metrics are ideal for disposable and low cost energy efficient electronics.

7.3 High performance TFTs utilising spray pyrolysed ZrO_2 dielectrics

This final section now discusses work that combines the best of the previously seen methods and results to produce thin film transistors with exceptionally high performance and low operational voltages. In terms of outright performance, specifically charge carrier mobility, spray pyrolysed zirconium oxide (ZrO_2) has proven to be the optimum material of those trialled as high-*k* dielectrics for use with spray pyrolysed ZnO. Therefore it was decided that an investigation into the possibility of utilising the previous gains realised through lithium doping, in combination with a ZrO_2 dielectrics would be worthwhile. Utilising the lithium doping at the optimum 1% $[Li^{+1}]/[Zn^{+2}]$ ratio combined with a high quality ZrO_2 dielectric it has been possible to fabricate devices with charge carrier mobilities as high as ~85 cm^2/Vs at operational voltages as low as 3.5 V. This is in comparison to the undoped devices, still utilising a ZrO_2 dielectric, whose charge carrier mobility values only reach ~33 ~cm^2/Vs. All other device parameters are excellent and typical of what has been seen in previous examples of spray pyrolysed ZnO transistors.

As with the previous work, films were prepared for characterisation by spraying precursor aerosols at a temperature of 400 °C onto a number of different substrates. To fabricate transistors, the same commercially available ITO coated glass was patterned, followed by the deposition of the dielectric material then the semiconducting layer of ZnO or Li-doped ZnO using the methods discussed previously. Deposition of the aluminium source and drain contacts of ~30 nm thickness was the final step, yielding bottom contact coplanar devices. To assess the dielectric properties of the ZrO_2, MIM capacitors were fabricated, once again using commercially available ITO coated glass that had already been patterned by the manufacturer. ZrO_2 was deposited by SP across the entire substrate, followed by the deposition of gold contacts utilising specifically designed mask.

X-ray diffraction (XRD) measurements were carried out on the as-purchased ITO on glass and ZrO_2 on glass. Also XRD measurements

were performed on the film stack following each deposition, these films were deposited on the ITO on glass substrate. AFM measurements were performed on the films used for transistor measurements from both within and outside of the transistor channels. For the measurement of each individual layer, additional substrates were added during the deposition process and removed following each individual deposition step. For extraction of the optical bandgap of the dielectric films, UV-Vis spectroscopy measurements were made on films deposited on β-phase quartz substrates. Measurements of the individual ZrO_2 and ZnO were performed and also measurements of the combined ZrO_2/ZnO film stack were performed.

7.3.1 Precursor materials

As with previous work in order to deposit ZrO_2 films a number of precursor materials were initially evaluated. Zirconium acetylacetonate (Fig 7.6) proved to be the most suitable material for precursor solution preparation, offering easy preparation as both materials dissolved in methanol (linear formula: CH_3OH), these films proved to be the highest quality when compared to those deposited using other precursor materials.

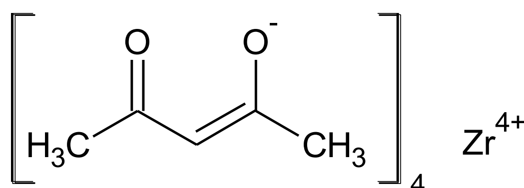

Figure 7.6: Chemical structure of zirconium acetylacetonate, used for the preparation of precursor solutions. Liner formula: $Zr(C_5H_7O_2)_4$.

Solutions were prepared and left to stir for at least 30 minutes before deposition commenced, ensuring complete dissolution of the acetylacetonates. Sonication of the solution for ~10 minutes was also

employed in order to help disperse any agglomerates and speed up dissolution of the precursor. As was the case with the deposition of the Y_2O_3 and Al_2O_3 dielectrics, a lower solubility of the zirconium acetylacetonate precursor led to a slightly protracted deposition process. In this case 25 coats were needed to attain a film thickness of ~100 nm. Again the feed rate of the precursor solution was kept at 2.5 ml/min. For the preparation of the zinc and lithium precursor solutions, the same materials and methods were used as those discussed in chapter 6, where 4 spray coats were applied at a feed rate of 1.5 ml/min. For this work however, only the optimum 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio was utilised.

7.3.2 Optical properties of ZrO_2 thin-films

The optical properties of the individual ZrO_2 dielectric layer, the ZnO layer and the combined ZrO_2/ZnO film stack were investigated using UV-Vis spectroscopy, measured between 200 and 800 nm.

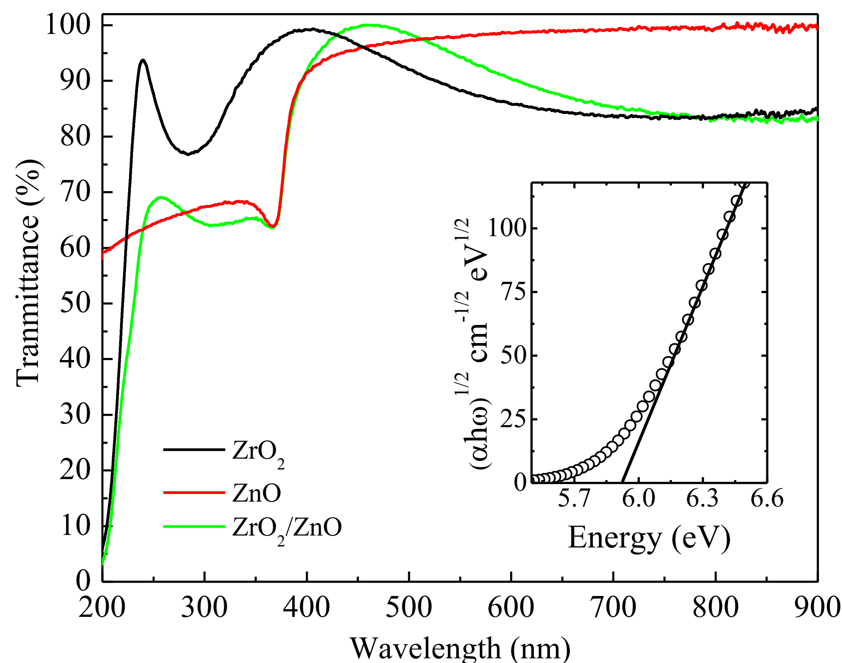

Figure 7.7: Optical transmittance of ZrO_2, Li-ZnO and stacked ZrO_2/Li-ZnO films deposited on β-phase quartz and (inset) optical bandgap extracted using Tauc plots for ZrO_2.

All films were deposited at a temperature of 400 °C onto β-phase quartz substrates. Film thickness for the ZrO_2 was calculated to be approximately 98 nm, which is in good agreements with values extracted experimentally by spectroscopic reflectometry. The ZnO layer was deposited to a thickness of ~30 nm. The optical transmittance through the individual films and combined stack show a very high level of transparency across the visible spectrum, with the average transmission for all films being greater than 80%. There is no absorption onset until ~410 nm for the combined stack and lower still at ~390 nm for the ZrO_2 film alone. From the ZrO_2 film deposited individually on β-phase quartz substrates it has been possible to extract the optical bandgap giving a value of 5.93 eV from extrapolation of the linear region of the Tauc plot. This is in good agreement with values extracted by SE, although slightly higher than values reported previously for spray pyrolysed ZrO_2 [12].

7.3.3 Surface analysis of ZrO_2 thin-films

The surface morphologies of the sequentially deposited films were analysed by atomic force microscopy, starting with the ITO on glass alone and followed by analysis of each successive deposition. Measurements were performed over a 1 μm area, whilst measurements were also performed over a larger area (5 μm) for confirmation of continuous films with the same morphological properties. All films were deposited alongside those used for device fabrication and consist of the same type substrates. Following the deposition of each layer a substrate was removed for measurement purposes. For the sake of confirmation, the measurements were also performed in the channel region of the devices after they had been electrically characterised and were shown to have identical surface morphologies properties.

Measurements of the ITO surface show a granular structure with a root mean square (RMS) surface roughness of ~2.9 nm. The average grain size of the ITO, calculated using statistical methods, is given as ~35 nm. The ZrO_2 surface maintains a relatively low RMS roughness value of

~3 nm, with grain size estimated to be ~30 nm. The final ZnO layer also maintains a low RMS surface roughness of ~3.3 nm. Grain size of the ZnO is estimated to be ~45 nm, which is comparable to that seen with ZnO films deposited on conventional SiO_2 dielectrics [31, 32]. The low surface roughness for each film is promising in terms of application for thin film transistors, suggesting the possibility of a high quality ZrO_2/ZnO interface is high. Height distribution for the ITO layer shows an asymmetric shape, with a preference toward higher values, whilst the ZrO_2 and ZnO layers show a Gaussian distribution, suggesting the ITO does not play any significant role in the morphology of the upper layers, and rather the deposition method has the most influence on their final morphology.

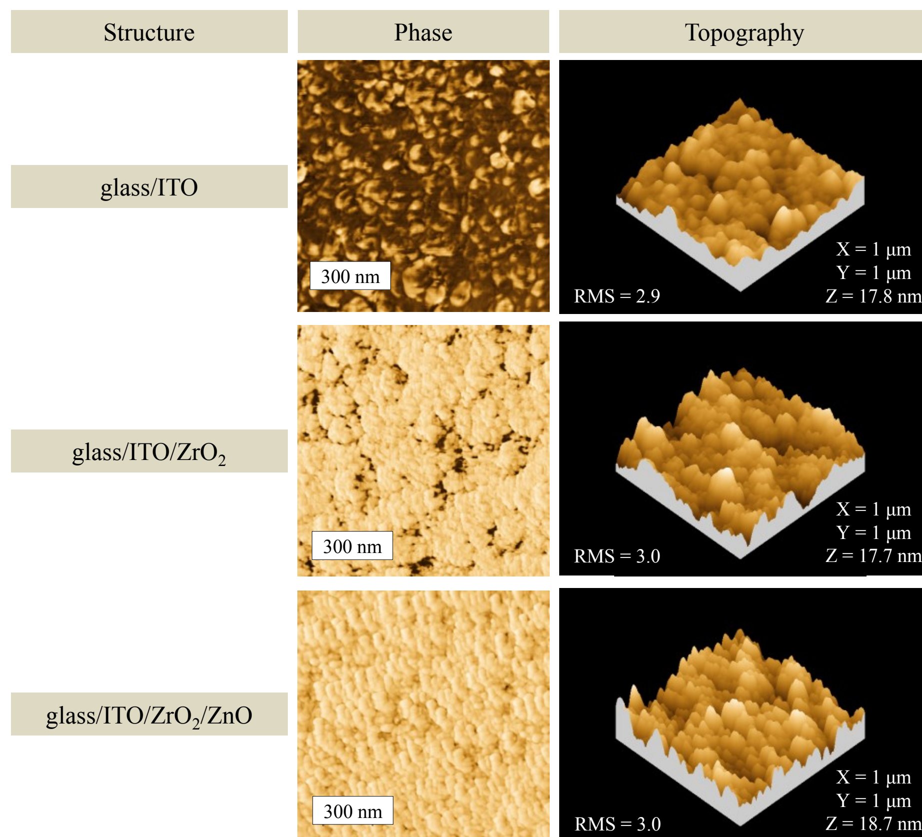

Figure 7.8: Atomic force microscopy images showing topography and phase for deposited thin films beginning with ITO, followed sequential deposition of ZrO_2 and ZnO.

7.3.4 X-ray diffraction of ZrO_2 thin-films

X-ray diffraction experiments were conducted on the as-purchased ITO on glass films, ZrO_2 deposited on glass substrates, ZrO_2 deposited on top of the ITO on glass, and finally measurements were made of the entire film stack (Fig 7.9). Deposition for all materials deposited by spray pyrolysis was performed at a temperature of 400 °C.

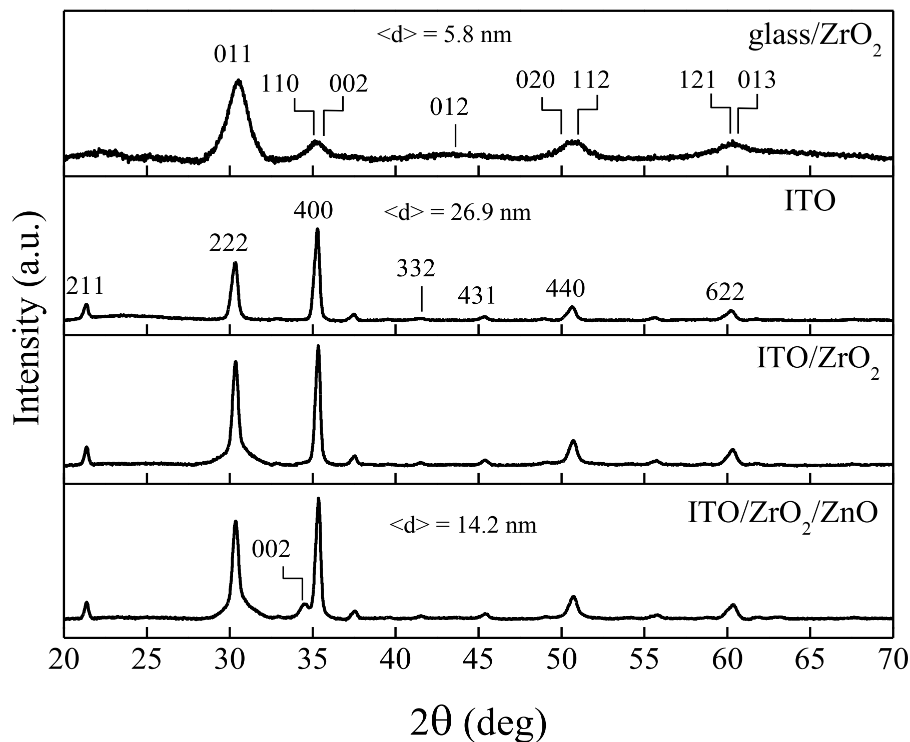

Figure 7.9: X-ray diffraction measurements of ZrO_2 on glass, ITO on glass, ZrO_2 on ITO on glass, and finally the entire film stack deposited on glass.

The ZrO_2 diffraction pattern show quite broad peaks, suggesting a small crystallite size. Using the Debye–Scherrer formula [33], analysis of the (011) peak at 30.5° yields an average crystallite size of 5.8 nm. The determination for the precise phase of the deposited films is difficult as the monoclinic and tetragonal structures are very similar and yield similar diffraction patterns [34]. Furthermore, the broad diffraction pattern and small crystallite size also make phase identification more difficult. Additional measurements carried out using Raman spectroscopy

have revealed the coexistence of both the tetragonal and monoclinic phases of ZrO_2 within the films. Unfortunately due to the small crystallite size the percentages of the different phases within the films could not be calculated. The impact of the different phases on device performance is not known, however the devices perform well and remain stable when stored in an inert environment. Ideally the development of single phase ZrO_2 would help give some understanding of the impact of the different phases, although this has not proved possible so far.

The remaining XRD patterns for the ITO alone and various stacked structures on top of the ITO show the ITO film to have the most dominant features. The average crystallite size of the ITO was calculated from the (400) peak, and is estimated to be ~27 nm, whilst the same analysis on the (002) peak of the ZnO suggests an average crystallite size of ~14 nm.

7.3.5 Capacitance spectroscopy of ZrO_2 films

To test the dielectric properties of the ZrO_2 films and to help extract accurate values for transistor charge carrier mobility values, metal-insulator-metal (MIM) capacitors were measured by capacitance spectroscopy, across a frequency range of 100 Hz to 10 MHz whilst applying a 50 mV ac voltage (Fig 7.10). The same structures were used as with the previous measurements of Al_2O_3 and Y_2O_3 dielectrics, where patterned ITO on glass and matching evaporation masks where used to fabricate a variety of different size (area of parallel plates) MIM structures. Measurements show a typical example for the ZrO_2 devices, displaying stable capacitance values at measurement frequencies into the MHz range of operation. Geometric capacitance values extracted from these plots at 120 MHz are 124 nF/cm^2 with a resonance appearing at ~4 MHz. These values are in good agreement with those calculated using the dielectric constants measured by SE (k ~14). Dissipation factor values on average were ~0.03.

The current-voltage characteristics of the MIM structures were also investigated and showed very low leakage current levels, with values typically lower than 0.5 μA/cm^2, when biased with voltages up to a maximum value of 6 V. Likewise the breakdown characteristics were excellent, with no breakdown observed until field strengths of 1.6 MV/cm were reached. These values are more than high enough for low voltage transistor operation, and could be further improved if a smoother ITO gate layer could be formed.

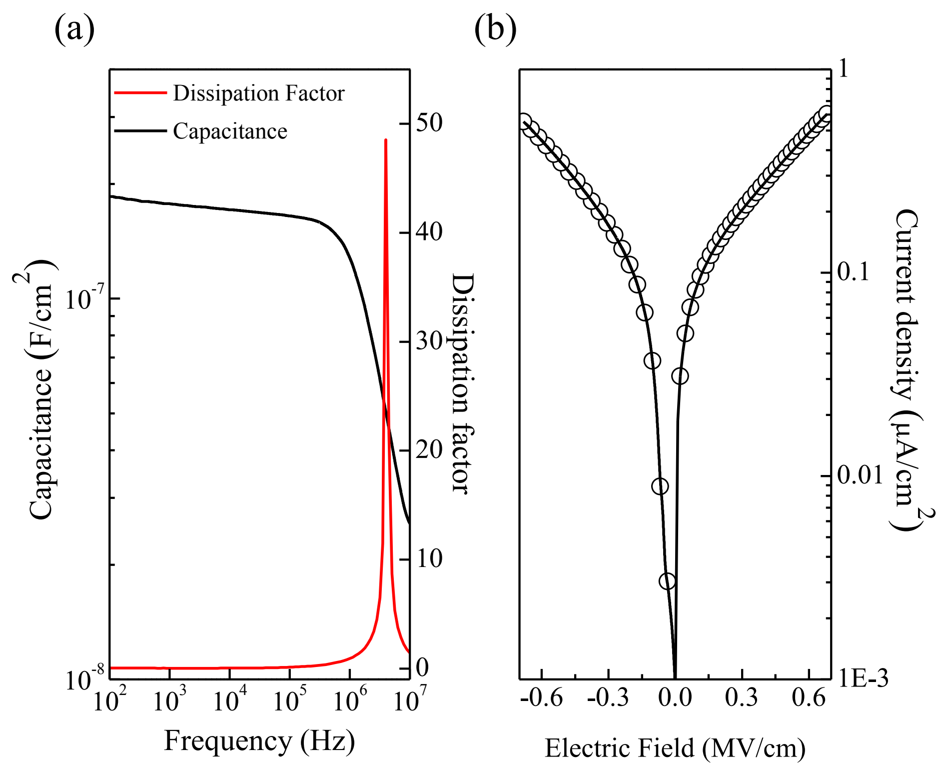

Figure 7.10: (a) Capacitance (left ordinate) and dissipation factor (right ordinate) as a function of frequency, measured between 100 Hz and 10MHz and (b) current-voltage characteristics of ZrO_2 based MIM structure.

7.3.6 C-V characteristics of TFTs

The final step in this work was to assess the quality of the ZrO_2 spray pyrolysed dielectric when applied in ZnO TFTs, particularly when used in conjunction with Li-doped ZnO. Devices where fabricated using the

same methods and structures as used for the previously discussed Y_2O_3 and Al_2O_3 dielectrics based devices, with the preparation of the Li-doped precursor solution being the only additional requirement. The 1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio was used, as identified as the optimum ration in the previous chapter.

Transfer and output curves representative of both the undoped and Li-doped devices (Fig 7.11 and 7.12 respectively) show excellent device characteristics, very typical of those found in the previous chapter. In both cases the output curves show no superlinear behaviour, suggesting there are no charge injection issues, whilst the devices clearly saturate well. For all the devices discussed here, operating voltages are very low at only 3.5 V, therefore ideal for low power applications.

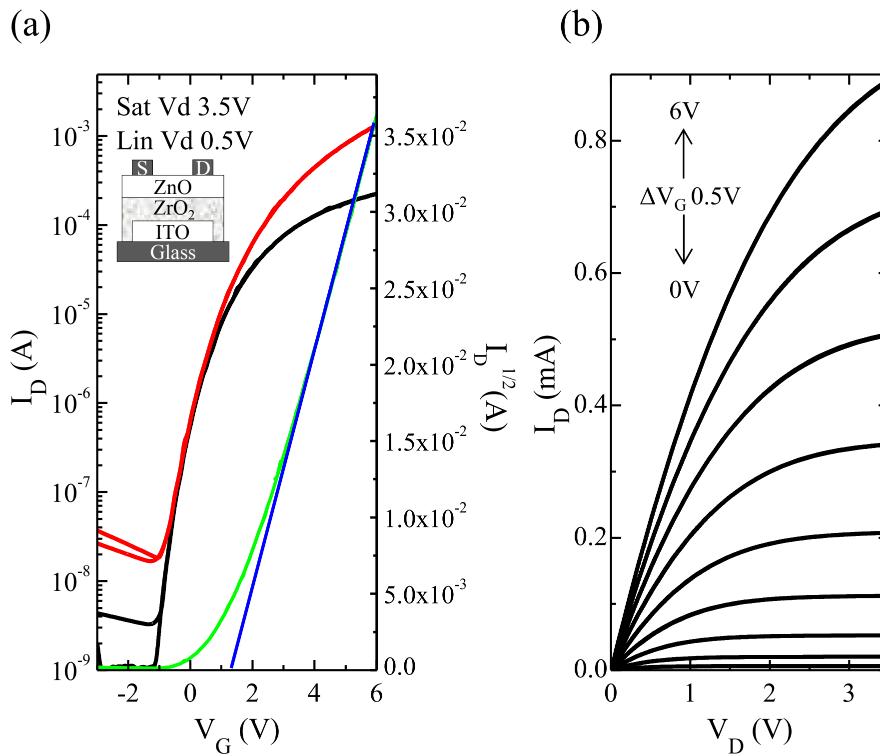

Figure 7.11: (a) Transfer and (b) output characteristics of a staggered bottom gate transistor (see inset) utilising a ZrO_2 dielectric with channel dimensions of 20 μm length and 500 μm width. Using ZnO as the semiconductor and deposited at 400 °C

The TFTs utilising the undoped ZnO combined with the ZrO_2 dielectric offer very good performance in terms of mobility as well as

other excellent device characteristics (Fig 7.11(a) and (b)). Channel dimensions for the device characteristics shown are 500 μm for the width, whilst channel length is 20 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be ~32 cm^2/Vs which is very high compared to undoped spray pyrolysed ZnO, typically not much higher than ~20 cm^2/Vs. The $I_{D(on)}/I_{D(off)}$ ratio is ~10^6 and the threshold voltage, V_T, is estimated to be 1.26 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 0.48 *V/dec*. This improved mobility could be attributed to a relatively small lattice mismatch and good epitaxy between the ZnO and ZrO_2 at the interface, when compared to that of a typical ZnO/SiO_2 interface [30]. Similar mobility enhancements have been reported using ZITO thin-film transistors using specially designed hybrid nano dielectrics [11].

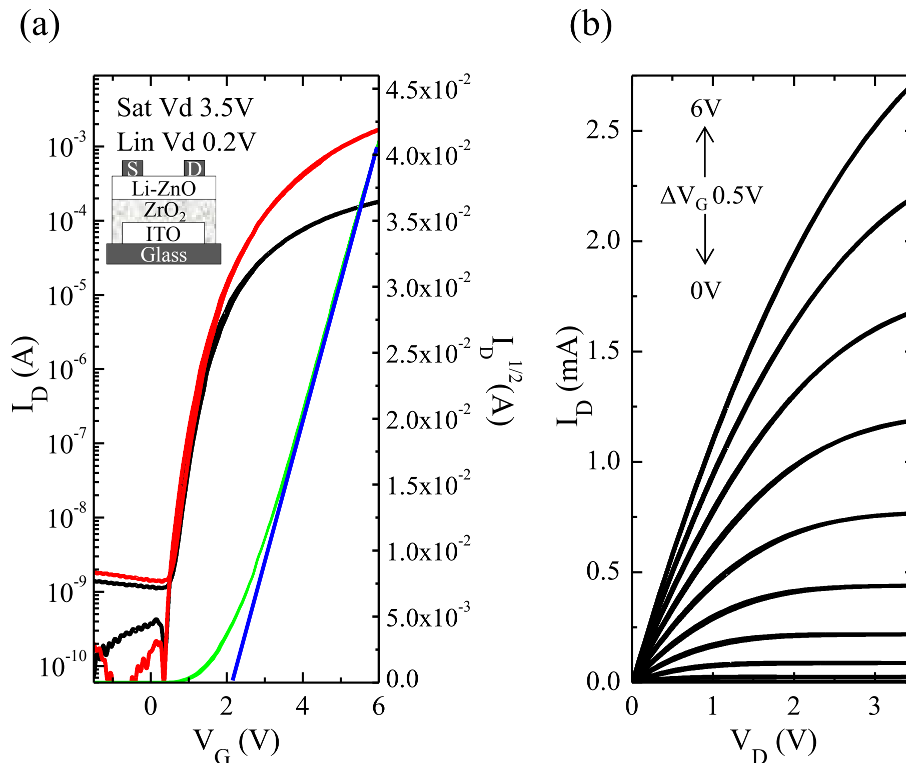

Figure 7.12: (a) Transfer and (b) output characteristics of a staggered bottom gate transistor (see inset) utilising a ZrO_2 dielectric with channel dimensions of 20 μm length and 500 μm width. Using Li-ZnO (1% $[Li^{+1}]/[Zn^{+2}]$ doping ratio) as the semiconductor and deposited at 400 °C.

The TFTs based on the Li-doped ZnO and ZrO_2 dielectric also show excellent operating characteristics and exceptionally high performance, particularly the charge carrier mobility. Channel dimensions for the device characteristics shown are once again 500 μm for the channel width, whilst channel length is 20 μm. Charge carrier mobility under saturation, μ_{sat}, is calculated to be extremely high at ~85 cm^2/Vs. The $I_{D(on)}/I_{D(off)}$ ratio is also $\sim 10^6$ and the threshold voltage, V_T, is estimated to be 2.12 V from extrapolation of a straight line fit of $\sqrt{I_{Dsat}}$. The subthreshold slope, S, is estimated to be 0.22 *V/dec*. This significantly improved mobility is attributed to a combined reduction in grain boundary density due to the Li-doped ZnO semiconductor, and a significant enhancement in the semiconductor/dielectric interface, resulting from the use of ZrO_2 dielectric. These devices, in terms of performance, are significantly better than many other examples of ZnO based thin-film transistors. At present it is possible to fabricate higher performance ZnO devices, but none of these examples use as simple solution based deposition method such as spray pyrolysis.

7.4 Conclusions

The primary aim of the work demonstrated in this chapter was to illustrate the suitability and use of high quality high-*k* dielectric materials in combination with ZnO and Li-doped ZnO. The physical properties of Al_2O_3, Y_2O_3 and ZrO_2 have been investigated, leading to the fabrication of transistors with low operating voltages and charge carrier mobilities of extremely values when compared other solution processed ZnO devices.

Al_2O_3 as a spray pyrolysed dielectric appears to integrate well with ZnO offering very high charge carrier mobilities when compared to ZnO devices fabricated using SiO_2 dielectrics, with the added benefit of low operational voltages. Y_2O_3 also integrates well with ZnO, however, device performance is comparable to that seen when using SiO_2 dielectrics and no better, although low voltage operation is still a clear

benefit. The discrepancy in device performance between these two dielectrics is attributed mainly to the polycrystalline nature of the Y_2O_3 dielectric leading to a less favourable semiconductor/dielectric interface. Finally, ZrO_2 has been demonstrated to give favourable results when combined with ZnO based semiconductors. Charge carrier values for devices are very high when using undoped ZnO as the semiconducting layer, but when used in combination with Li-doped ZnO significant gains are seen. This is attributed to the high quality of the dielectric/semiconductor interface, combined with the gains realised through the utilisation of Li doping, which reduces the grain boundary density across the device channel.

The secondary aim of the work presented here was in demonstrating the flexibility of spray pyrolysis, and to show its suitability to for the deposition of more than just zinc oxide thin films. Through the selection of suitable precursor materials it has been shown that high quality dielectric thin films can be deposited by spray pyrolysis, indicating that it may be possible to eventually fabricate transparent oxide based thin-film transistors entirely by spray pyrolysis. When this is realised, and the simplicity and low cost of spray pyrolysis deposition is taken into account, there is a strong argument to be made for the application of spray pyrolysis as a highly suitable deposition method for the future of low cost electronics.

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Chapter 8

Summary and outlook

Summary

The work presented in this thesis discusses some of the progress made in the field of solution processed metal oxide thin-film transistors (TFTs). In particular, the applicability of spray pyrolysis (SP) as a suitable method for the deposition of high-performance semiconducting and dielectric thin-films is explored. This unconventional low-cost alternative deposition process offers what could be the next step toward scalable low-cost large area electronics, and may well change our outlook toward future semiconductor deposition processes. The bulk of the work here discusses the use and optimisation of SP and its application in the fabrication of very high performance zinc oxide (ZnO) based TFTs. This final chapter will summarise what has been discussed in the previous three experimental results chapters, outlining the conclusions that are found, and also offers some indications on the future outlook.

The first experimental results chapter, chapter 5, introduces the concept of SP as a suitable deposition method for metal oxide based semiconductors, and demonstrates how the combination can be utilised to fabricate high performance TFTs with several novel features. The method was used to demonstrate primarily the deposition of ZnO, followed by some more recent work on the deposition of gallium oxide

(Ga_2O_3). The effects of varying the growth conditions such as deposition thickness and substrate temperature were investigated in order to correlate their influence on device performance. This was achieved using a number of materials and electrical characterisation techniques.

After an initial discussion explaining the reasoning behind precursor material choice and following some analysis of the thermal decomposition of the chosen materials, the first investigation was made into the influence deposition temperature has on the deposited films. It was clear that as the deposition temperature is increased there is a significant improvement in the crystalline quality of the films. This is indicated by numerous characterisation methods including UV-Vis spectroscopy, X-ray diffraction (XRD) and atomic force microscopy (AFM). Most evident is an increase in the crystallite and grain size, which is believed to be a key factor in the improvement in device performance. Choosing to use higher deposition temperatures (>400 °C) leads to significantly improved charge carrier mobilities, with values in excess of 20 cm^2/Vs.

Film thickness was also investigated by adjusting the quantity of the deposited material. The influence of film thickness in ZnO TFTs is interesting as increased film thickness sees an improvement in the charge carrier mobility. Looking at AFM data suggests the improvement is again due to increased grain size that is seen as film thickness in increased.

In both the cases the improved performance is attributed to the reduced density of grain boundaries across the device channels. Charge transport in polycrystalline films such as those demonstrated here is considered to be grain boundary limited, and this is also why there is typically a trend where charge carrier mobility improves as TFT device channels are reduced in length. The charge trapping characteristics of the films are is also investigated and it suggests that the increased temperatures lead to both a reduction in the trap per unit energy due to improved crystalline quality, and also a reduction in the areal trap density at the semiconductor/dielectric interface, due to an improvement in the interface morphology.

The choice of contact material has also been investigated, suggesting aluminium provides the best choice when considering the most commonly used and available choices. The high work function of gold appears to significantly limit charge injection into the ZnO conduction band, having an overwhelming effect on device performance. Utilising aluminium with its lower work function offers significantly improved charge injection characteristics, allowing not only improved device performance, but also a better experimental control test bed for further investigation into the characteristics of ZnO based TFTs.

Finally, toward the end of the chapter and to the best of the author's knowledge, solution processed Ga_2O_3 TFTs are demonstrated for the first time. This work is still in a preliminary stage, but already the performance of the devices is approaching those of amorphous silicon (a-Si). The deposition of these films differs from other examples of Ga_2O_3 TFTs not only because they are deposited by SP, but also as they are undoped which is not often the case in other examples of Ga_2O_3 reported in the literature. It is likely and entirely reasonable to expect that with further optimisation and the use of doping methods, a significant improvement in performance can be realised.

Chapter 6, the second experimental results chapter, introduces the concept of solution processed doping through the use precursor blending techniques. The use of two dopants is investigated, in each case having different effects on ZnO based device metrics. The use of lithium is shown to have a significant improvement in charge carrier mobility, pushing ZnO TFT performance closer to that of costly polycrystalline silicon (p-Si). Beryllium was found to offer a route toward controlling the threshold voltages of TFTs, and the benefit of its use is demonstrated in the fabrication of integrated circuits.

Following a discussion explaining the methods used to perform solution based doping, the influence of lithium on the characteristics of both the deposited films and fabricated TFTs was investigated. Through optimisation of the lithium to zinc metal ion ratio, it was possible to demonstrate Li-doped ZnO TFTs with charge carrier mobilities as high as 54 cm^2/Vs with excellent overall performance characteristics. In a

similar fashion to what's seen when the deposition temperature is increased for non-doped ZnO deposition, the crystalline quality of the deposited films for specific $[Li^{+1}]/[Zn^{+2}]$ ratios (centered around the 1% ratio) is significantly improved showing an increased crystallite size coupled with increased grain size. Again the improved performance is attributed to a reduction in the grain boundary density across the channel. Analysis of the trapping mechanisms within the devices suggests that reducing the number of the grain boundaries across the device channel leads to a corresponding reduction in both the trap concentration per unit energy, and also and improved semiconductor/dielectric interface giving a lower interfacial trap density.

In the second part of the chapter beryllium was identified as a suitable dopant for ZnO which enables the control of transistor threshold voltages. Being able to control the threshold voltage of a device without a loss in performance is particularly useful when designing integrated circuits, as ZnO alone often exhibits somewhat negative threshold voltages. With the addition of beryllium there is a significant positive shift in the transistor threshold voltages. Device performance in terms of mobility, doesn't appear suffer until the $[Be^{+2}]/[Zn^{+2}]$ ratio increases beyond the 0.5% value, although at this value a significant shift in the device threshold voltage has already occurred. Examining the trapping mechanisms within the TFTs suggests the inclusion of beryllium is leading to a change in the semiconductor/dielectric interface morphology, thus increasing the interface trap density and creating the shift in the transistor threshold voltages. Finally, inverter circuits were demonstrated taking advantage of the ability control of the transistor threshold voltages. These inverters show good performance characteristics, showing how the negative threshold voltages of ZnO TFTs, can be overcome.

The final experimental results chapter, chapter 7, demonstrates the versatility of the SP deposition method by combining the beneficial findings of previous two chapters with the use of SP to deposit high quality dielectric materials, enabling the fabrication of high performance low voltage TFTs, suitable for low power electronics. The physical

properties of aluminium oxide (Al_2O_3), yttrium oxide (Y_2O_3) and zirconium oxide (ZrO_2) films, all deposited by SP have been investigated using many of the same techniques discussed in the previous chapters, and have been implemented in the fabrication of ZnO based TFTs.

The use of Al_2O_3 and Y_2O_3 is demonstrated in the fabrication of low voltage TFTs where in each case device performance is very good reaching a maximum value of ~34 cm^2/Vs, with performance somewhat favourable when using Al_2O_3. The discrepancy in device performance between these two dielectrics is attributed mainly to the polycrystalline nature of the Y_2O_3 dielectric leading to a less favourable semiconductor/dielectric interface.

The second half of the chapter is dedicated to the improved performance ZrO_2 offers as a dielectric when used in combination with ZnO. ZrO_2 was found to integrate better with ZnO when compared with the previously discussed dielectrics, leading to significantly improved device performance. It was therefore decided to attempt to combine the dielectric with the optimised Li-doped ZnO films. This proved to offer good results where device performance was found to be extremely high with charge carrier mobilites reaching values as high as ~85 cm^2/Vs, whilst still operating at very low voltages of ~ 4 V. Again this is attributed to a high quality dielectric/semiconductor interface, used in combination with the benefits seen through Li-doped ZnO. This work currently represents the best in terms of performance when considering solution processed ZnO based TFTs.

In general it has been the aim of the work presented here to illustrate both the flexibility and potential of both metal oxide semiconducting and dielectric materials, and also the suitability of SP as a promising deposition method for future low cost electronic applications.

Outlook

In reality, the work presented here is merely an introduction to what may be possible when utilising SP as a deposition method for metal oxide electronic materials. There will need to be significant amounts of further investigation into the growth and control dynamics of metal oxides by SP before we see its commercialisation and application in the electronics industry, however there are no doubts of the potential it holds. Some key areas for further work are discussed below.

The films discussed in this work were grown in an ambient environment with no special precautions, a far cry from how things are done in the semiconductor industry. Yet the performance of the devices is quite remarkable when you consider they often perform significantly better than examples grown utilising complex vacuum based techniques. With that in mind there may be some degree of improvement to be seen from optimising the growth environment and generally making the deposition process more sophisticated.

A better understanding of growth dynamics of films deposited by SP would also be of significant benefit. The entire SP method, although incredibly simple, is far from understood when we consider the conversion and growth process of the deposited films. The development of some form of *in-situ* XRD system would be one interesting project, likewise an analysis of the droplet size and velocity may help build a better picture of how our films are grown. There are also so many variables that can be adjusted during the deposition process, that analysis like this could be very rewarding for not only the deposition of metal oxide TFTs, but for the entire thin-film deposition industry.

There are still many avenues left to investigate when discussing doping using the precursor solution blending method used here. Only a few materials have been touched upon here, but undoubtedly there are many more dopants that may be of some benefit to ZnO based TFTs. There are already numerous examples of ternary and quaternary doping of ZnO TFTs by other deposition methods, so there is no reason to think that SP deposited film may not realise the same benefits.

Finally, the possibility of low temperature deposition of high quality ZnO TFTs can be considered as one of the toughest yet most rewarding challenges for SP as a deposition method. The ability to deposit high performance electronic materials on plastic substrates is a challenge that many are trying to overcome. SP is certainly a suitable delivery method, but at present the high conversion temperatures required of the precursors is a limiting factor. Solving this issue going to be difficult and is likely to need the combined efforts and expertise chemists, physicists and engineers. However, progress is slowly being made, so maybe SP may play a role in this future application area.

Appendix

List of publications

Journal articles

Stuart R. Thomas, Pichaya Pattanasattayavong, Thomas D. Anthopoulos. Solution-processable metal oxide semiconductors for thin-film transistor applications. *Chemical Society Reviews*, 10.1039/C3CS35402D, June 14, 2013.

Pichaya Pattanasattayavong, Stuart R. Thomas, George Adamopoulos, Martyn A. McLachlan, Thomas D. Anthopoulos. p-channel thin-film transistors based on spray-coated Cu_2O films. *Applied Physics Letters*, 10.1063/1.4803085, April 26, 2013.

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Conference proceedings

Stuart Thomas, Thomas D. Anthopoulos. Oxide based semiconductors and high-k dielectrics for thin-film transistor applications (oral), at *The 4th International Symposium on Transparent Conductive Materials (TCM2012), Greece,* 2012,

Stuart Thomas, George Adamopoulos, Aneeqa Bashir, Donal D.C. Bradley, Thomas D. Anthopoulos. Crystallographic engineering of oxide based semiconductors for thin-film transistors and microelectronics (oral), at *Materials Research Society (MRS) Fall Meeting, Boston, USA,* 2011.

Stuart Thomas, George Adamopoulos, Aneeqa Bashir, Donal D.C. Bradley, Thomas D. Anthopoulos. Li-Doped Zinc oxide Transistors and circuits fabricated by spray deposition in ambient atmosphere (poster), at *The 7th International thin-film transistor Conference, Cambridge, UK,* 2011.