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Load Adaptive Zero-Phase-Shift Direct Repetitive Control for Stand-Alone Four-Leg VSI

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***Abstract* –This paper deals with a dedicated load adaptive phase compensation algorithm to be used in Repetitive Control based stand-alone 4-leg VSI. The plant model is achieved, its inherent modifications according to the operating point are highlighted and used to properly adapt the Repetitive Control structure. Modification of the repetitive control parameters is described to obtain the desired phase compensation capabilities achieving a Zero-Phase-Shift condition at each harmonic. This allows to increase the gain of the Repetitive Controller at high order harmonics thus yielding a better VSI output voltages with strongly reduced THD and faster dynamic response. As a consequence, the VSI output voltages are almost independent from the loads to be fed and the 4-leg VSI with the proposed Zero-Phase-Shift Direct Repetitive Control is an ideal candidate to supply sensitive loads in microgrid, in particular for stand-alone applications.**

I. Introduction

Different power electronics applications, such as Distributed Generation Systems, Uninterruptible Power Supplies or active filtering, have to comply with severe standards related to the harmonic content of the converter output currents and voltages.

Standards for grid requirements are the European Standards EN-50160 and EMC EN-61000, which specify the quality limits that the utilities must satisfy. Even if the European Union has its own regulation, each country can apply some restrictive mandatory requirements. Considering the voltage Total Harmonic Distortion (THDV), the EN-50160 is referred up to the 25th harmonic with respect to the fundamental component. On the other hand, when stand-alone power generation is considered, Uninterruptable Power Supply (UPS) systems reference standard is the IEC 62040-3, which denotes that the output voltages harmonic content should be within IEC 61000-2-4 Class 1 limits under specific linear and non-linear load conditions.

Reference application for the proposed control strategy is related to an AC stand-alone three-phase plus neutral power supply unit formed by a 4-leg VSI and its dedicated output power filter. It has to be able to hold up a 3ph+n isolated grid feeding linear and non-linear loads, with leading and lagging power factor, as shown in Fig. 1.

One of the Repetitive Control (RC) main competitors is the Multi Resonant Control (MRC) structure, which is able to locate a harmonic compensator at each desired harmonic with almost independent gain and phase [1, 2]. However, MRC main drawback is the difficult implementation and the requirement in terms of control platform memory and computational performance. On the other hand, RC is able to provide theoretically infinite resonant controllers, as well it is very simple to be implemented requiring only a couple of delay lines and few simple arithmetical calculations. These features allow the whole control algorithm to run faster with respect to the MRC considering the same control platform. Nevertheless, RC needs a gain limiting system to reduce high frequency gains ensuring the proper working of the whole control loop [3]. Accordingly, compensation of relative high order harmonics is limited by the stability issues related to the phase lagging effects introduced by sampling, measure filtering and mainly by the VSI output filter-load interaction, as it is shown in the following.

Consequently, the phase compensation algorithm is suggested to improve the overall harmonics regulation performance of the RC. However, system behaviors are not constant, but they strongly depend on the operating point, suggesting for a load-adaptive phase compensation strategy as it is proposed in the paper. Previously published papers started analyzing the issue related to phase lagging and some solutions have been proposed. High performance RC algorithms have been proposed as in [4] where a 4^{th} order FIR filter is used to cut high frequency gains. However, even though the wide pass band flatness and the sharp high frequency attenuation rate of the FIR filter, harmonics are only compensated up to the 19^{th}. In [5] a single-phase VSI with a simple output LC filter is considered for the non-adaptive RC phase compensation. It is achieved by directly changing the length of the output delay line under the implicit assumption of constant load (i.e. pure resistive and diode rectifier). In [6], with reference to the same system and operating conditions as in [5], a simple plant representation is used to obtain the zero-phase-shift RC. Main drawback is the non-causal

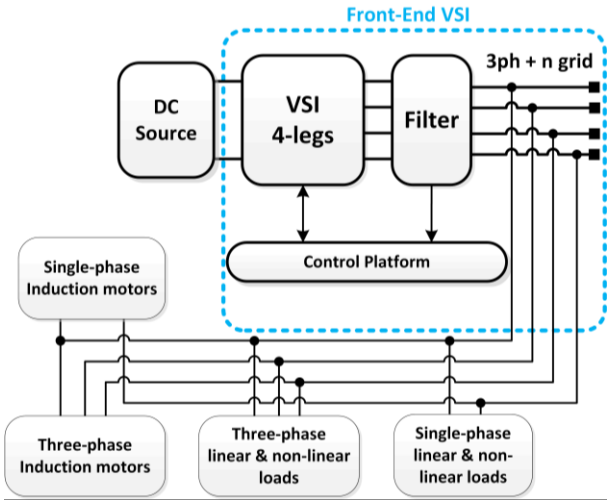


Fig. 1. Three-phase four-leg front-end inverter generating system.

transfer function to be managed at constant VSI operating point. Useful low-pass filter to be able to reduce high frequency RC gain are proposed in [3], allowing simpler compensation due to the introduced frequency independent delay. Direct form of Repetitive Control has been implemented in [7] where a notch filter is proposed to perform the required zero-phase-shift effect.

II. Power Generating Unit Modeling and Filter-Load Interaction

In this section, the modeling procedure of the proposed system is demonstrated, and the interaction between the filter and the load is briefly reviewed and discussed.

A. Converter Modeling

Power inverter is modeled by its first order approximation, which is very simple to manage. The inverter is seen from the control algorithm mainly as a gain with a delay due to the discretization caused by the PWM unit as shown in (1), where K_m is the gain depending to the modulation strategy, V_{dc} and F_{sw} are respectively the input DC-link voltage and the inverter switching frequency. Output phase voltages are filtered by means of a second order low-pass Butterworth filter having the transfer function as in (2), where ω_f is the filter cut-off frequency.

$$G_{4-leg}(s) = \frac{K_m V_{dc}}{1 + \frac{s}{2\pi F_{sw}}} \tag{1}$$

$$G_{lpf}(s) = \left(\frac{{\omega^2}_f}{s^2 + \sqrt{2}\omega_f s + {\omega^2}_f} \right) \tag{2}$$

Inverter output filters are necessary to remove the switching components from the output voltage and current waveforms. In the present study, it is considered the single-phase equivalent filter structure as shown in Fig. 2, where the conventional LC second order filter is connected with two tuned RLC branches: the trap-filter and the selective damper [8]. The selective damper is centered at the frequency of about 1.2 times the LC resonance frequency in order to damp the LC resonance peak, making the Rd resistor visible to the rest of the circuit only in a restricted range of frequencies. The trap-filter is instead tuned to resonate at the switching frequency (R_t is the sum of L_t and C_t ESRs), in order to short-circuit the switching fundamental component. Filter transfer function can be simply achieved considering the impedance of each part of the filter in the s domain as in (3) without a load connected at the filter output. The proposed system modeling procedure for the 4-leg voltage source inverter is intended for both 3-ph and 1-ph linear and non-linear loads.

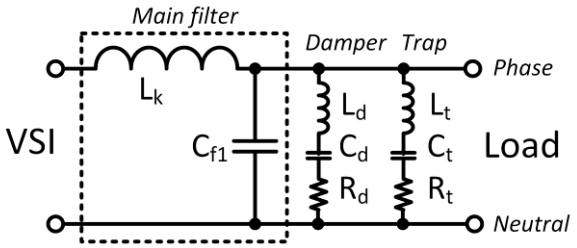


Fig. 2. Scheme of the considered output power filter.

Finally, the complete plant can be expressed by $G_P(s)$, where $G_L(s)$ is the load equivalent transfer function.

$$Z_{trap}(s) = sL_t + \frac{1}{sC_t} + R_t$$

$$Z_{dump}(s) = sL_d + \frac{1}{sC_d} + R_d$$

$$G_{pwf}(s) = \frac{Z_{dump}(s)//Z_{trap}(s)//\frac{1}{sC_{f1}}}{sL_k + \left(Z_{dump}(s)//Z_{trap}(s)//\frac{1}{sC_{f1}} \right)} \tag{3}$$

$$G_P(s) = G_{4-leg}(s) \cdot G_{pwf}(s) \cdot G_L(s)$$

B. Filter-Load Interaction

In reference to stand-alone applications, filter magnitude and phase behaviors are strongly affected by the actual inverter output power as previously depicted in [1] for loads having unitary, leading and lagging displacement power factor (DPF). Some results, are reported in the following. Loads having a power factor equal to one can be modeled as an equivalent resistive load: as the supplied power increases, the filter is more damped and its amplitude and phase responses are modified. Fig. 3 shows the Bode plots for the filter at four different output power values.

Inductive-resistive loads do not strongly affect system stability with respect to no-load condition, as pure resistive loads do. In fact, inductive loads lightly affect the complete filter phase. It can be noticed from Fig. 4 that the resonance is almost undamped and the characteristic frequency tends to move to higher frequency as highlighted. Fig. 4 shows the filter behavior when the inductive load having DPF=0.1 is connected. Hence, at light load there is not critical effect even if the current is lagging the regulated output voltage.

When capacitive loads are considered, the equivalent effect is to increase both the filter damping and the filtering action as it is depicted in Fig. 5 for a load having a leading power factor

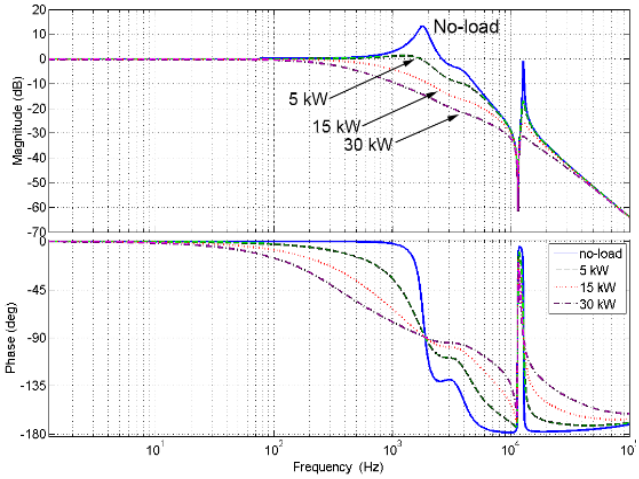


Fig. 3. Filter Bode-plot at different unitary power factor loads.

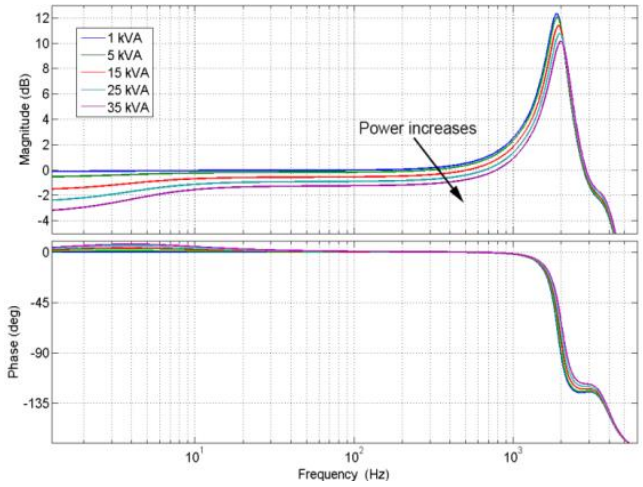


Fig. 4. Bode plots for resistive-inductive load with DPF=0.1.

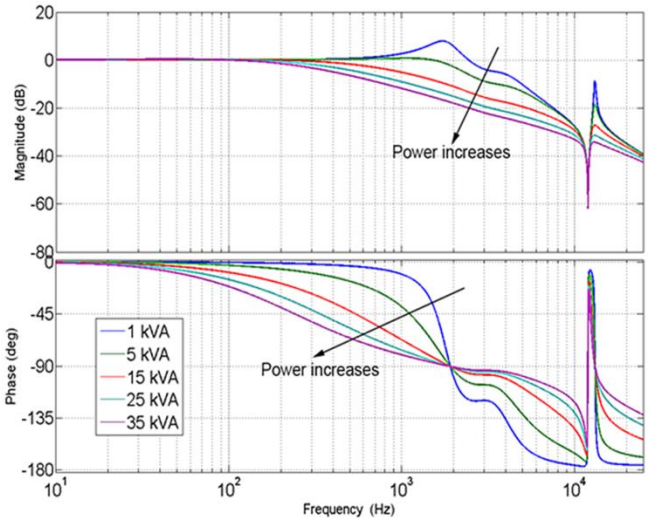


Fig. 5. Bode plots for resistive-capacitive load with DPF=0.8.

equal to 0.8. In fact, the reactive resistive-capacitive load acts as an additional filter due to the additional capacitance and as a damper due to the load active power (resistor). This behavior can usually introduce oscillations in the inverter output waveforms for either voltage or current controlled VSI; because of the strong interaction between filter and control algorithm, which leads to an increase of the phase delay. However, the proposed adaptive tuning control algorithm is theoretically able to boost the phase at the required value and then to compensate for the transfer function phase lag due to the capacitive loads.

III. Control Strategy and Load-Adaptive Algorithm

Inverter fourth leg, which is devoted to provide the neutral connection, is modulated without direct voltage regulation as suggested in [9]. Hence, the converter system can be considered as three fully independent single-phase inverters, and can be regulated by individual voltage controller. This feature can effectively decouple the load interaction of the three phases, which is particularly suitable for unbalanced load conditions.

In this work, individual Direct Repetitive Control (DRC) is proposed for the phase-to-neutral voltage regulation of the 4-leg inverter. From the control design point of view, each block of the

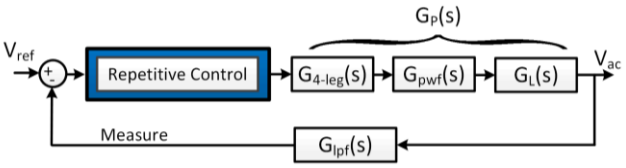


Fig. 6. Complete system block scheme with highlighted Direct Repetitive Control for each phase.

system can be represented through its characteristic transfer function as shown in Fig. 6. The investigated control strategy directly operates in the *abc* stationary reference frame. Being related to an off-grid application, the control loops are closed with respect to the output voltages. However, the illustrated Zero-Phase-Shift DRC can be absolutely extended to grid-tied inverters. In this former case, main differences are related to system modeling, being the control loops closed on the inverter output currents. The theory and the design of the DRC controller and the load adaptive algorithm are discussed in the following sub-section.

A. Direct Repetitive Control

The concept of repetitive control was initially presented in [10] for dealing with periodic signals in control systems. Based on the internal model principle (IMP), a repetitive controller processes the error signal of the previous period by particular algorithms, and applies the resultant signal to improve the control performance of the current cycle. Theoretically, with a suitably designed repetitive controller, the output of a stable feedback system can track the periodic reference signal or/and reject the exogenous periodic disturbance with zero steady state error [11]. Since the RC is not intended to stabilize the plant, it is often applied in conjunction with conventional controllers to form a combo control system, such as the parallel RC [12] and plug-in RC [13].

Previous work [13] has demonstrated the effective use of the plug-in type RC on the 4-leg VSI. With the aim of further enhancing the control performance and improving the overall harmonics regulation performance, the DRC control strategy is considered by taking the following factors into account. Firstly, the 4-leg VSI inverter system is internally stable, which enables the use of the direct RC. Secondly, the gain cut-off effect of the conventional controller on the high frequency band can be relieved, which makes the high order harmonic compensation possible. Thirdly, the absence of the conventional controller simplifies the control plant seen by the direct RC, which makes the design of the zero phase shift compensator and the load adaptive algorithm straightforward.

Fig. 7 shows the detailed structure of the direct RC controller, where k_{RC} is the repetitive learning gain, z^{-N} is the delay line, Q(z) is the robustness filter, and $G_f(z)$ is the stability filter. N is the ratio between the period time of the reference and

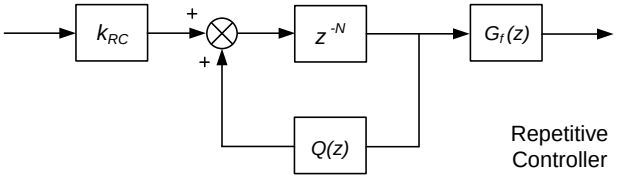


Fig. 7. Detailed structure of the direct RC controller.

the digital sampling time.

The use of the robustness filter Q(z) is to modify the internal model, which effectively increases the system stability margin. A close-to-unity constant of 0.99 has been chosen in this work, due to its simple implementation. The design of k_{RC} is associated with the selection of $G_f(z)$, and it is discussed in the following section.

B. Zero Phase Shift (ZPS) Compensator

The stability filter $G_f(z)$ is used to ensure that the overall system is stable after the introduction of RC. It is often chosen as a time advance unit for the straightforward implementation on digital control platforms [16]. However, there are two main drawbacks for this approach: 1) The value of the repetitive gain k_{RC} is coupled with the size of the time advance unit, and needs to be evaluated numerically. This implies that, when the time advance unit is adjusted to cope with different load conditions, the value of k_{RC} has to be modified accordingly. 2) The use of the time advance unit weakens the reference tracking and/or disturbance rejecting capabilities in the high frequency region, though this brings a relatively larger stability margin for the target system when model uncertainties present [17]. In order to yield a better VSI output voltage with strongly reduced THD for a wide load range, the zero phase shift (ZPS) compensator [11] is considered, and its detailed design procedure is discussed as follows.

For the direct RC control strategy, the plant seen by the RC is the system open loop transfer function, which can be represented in the gain-zero-pole manner as in (4). Since the system is internally stable, all the poles, p_1 to p_m, are located inside the unity circle. Without loss of generality, by assuming it contains *u* un-cancellable zeros and *n-u* cancellable ones, $G_{OL}(z)$ can be further expressed, where $D_{en}(z)$ represents the denominator; $N_{um}^{+}(z)$ and $N_{um}^{-}(z)$ are the cancellable and un-cancellable parts of the numerator, respectively.

$$G_{OL}(z) = G_P(z)G_{lpf}(z) = \frac{k(z - z_1)...(z - z_n)}{(z - p_1)...(z - p_m)} = \frac{kN_{um}^{+}(z)N_{um}^{-}(z)}{D_{en}(z)} \tag{4}$$

Based on it, the ZPS compensator can be designed as in (5), where $N_{um}^{-}(z^{-1})$ is obtained from $N_{um}^{-}(z)$ with z replaced by 1/z, and $[N_{um}^{-}(1)]^2$ is calculated by substituting z in $N_{um}^{-}(z)$ with 1.

$$G_f(z) = \frac{D_{en}(z)N_{um}^{-}(z^{-1})}{kN_{um}^{+}(z)[N_{um}^{-}(1)]^2} \tag{5}$$

C. Stablity Analysis

According to the small gain theorem [15], two sufficient stability conditions for the direct RC system can be summarized as follows: (a) system plant is internally stable; (b) equation (6) is guaranteed for all the frequencies below the Nyquist frequency ω_{nyq}.

$$\left|Q(e^{j\omega T_S}) - k_{RC}\, G_f(e^{j\omega T_S})G_{OL}(e^{j\omega T_S})\right| < 1 \tag{6}$$

The first condition can be guaranteed, as the 4-leg VSI system is internal stable. The second one can be proved by examining the Nyquist locus curve of equation (6). As analyzed in [11, 14], with the ZPS compensator employed as stability filter, the direct RC system is always stable for $0<k_{RC}<2$, given the robustness filter is chosen as 1. Also, it is worth to note that, when the system is a minimum-phase one, the numerator of $G_f(z)$ contains only cancellable zeros. In this case, both $N_{um}^{-}(z^{-1})$ and $[N_{um}^{-}(1)]^2$ are equal to 1, so that the corresponding $G_f(z)$ is just the inverse form of $G_{OL}(z)$ [17]. As it is in cascade with an N periods delay block (i.e. z^{-N}), there is no causality for its implementation.

For this work, since the Q(z) is chosen as 0.99 to enhance system robustness, equation (6) is always guaranteed for $0<k_{RC}<1.99$. The final value of k_{RC} has been chosen as 1.0, as a trade-off between convergence speed and transient performance.

Considering 2kW linear load condition as the nominal load level per phase, the corresponding ZPS compensator $G_{f\_2kW}(z)$ can be designed. Fig. 8 shows the Nyquist locus curve of equation (6) with $G_{f\_2kW}(z)$ implemented under 2kW linear load condition. Clearly, the magnitude stays within in the unitary circle, which proves that the overall control system is adequately stable.

D. Closed Loop Bode Plot

For different load conditions, the use of the direct RC controller with the corresponding ZPS compensator can guarantee not only a perfect regulation at the fundamental and the harmonic points up to Nyquist frequency, but also a high attenuation at other frequencies. This can be illustrated by the system closed loop bode plot shown in Fig. 9.

For 2kW load condition, the control system, with $G_{f\_2kW}(z)$ and k_{RC} of 1.0, can obtain unitary gain and zero phase shift at the fundamental frequency as well at all the harmonic points up to Nyquist frequency, while periodic inputs at other frequencies are largely attenuated. This implies perfect reference tracking and noise rejecting capability [14].

However, due to the interaction between the inverter output filter and the loads, the system behavior varies accordingly when the converter changes its operating condition. As it can be seen from Fig. 9, when the load moves away from the 2kW design level (i.e. either to a lighter load or heavier load), the amplitude response of the control system starts to present a large amplification (up to 1.63 dB) on the harmonic sidebands. Although the unitary gain and zero phase shift can still be maintained at the fundamental and harmonic frequency points, the system will be very sensitive (or even unstable) to noise or disturbance at high frequency, due to the high amplitude amplification caused by the improper ZPS compensator, which was designed for 2kW load condition. This will be experimentally demonstrated in Section IV.

With the aim of achieving high performance for the whole operation range and ensuring a high noise immunity capability, a load adaptive algorithm is considered to update the ZPS compensator automatically for this particular application.

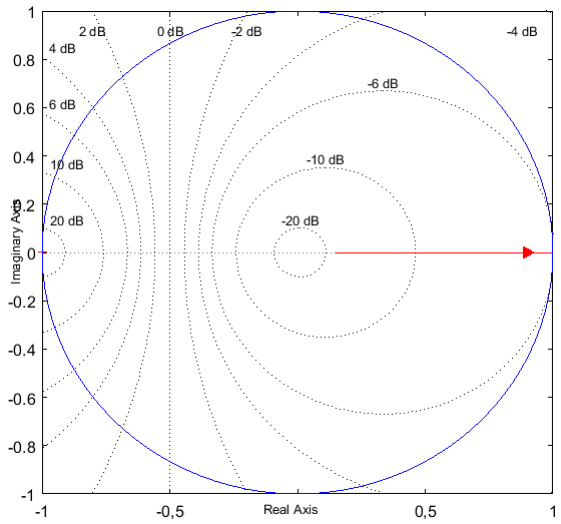
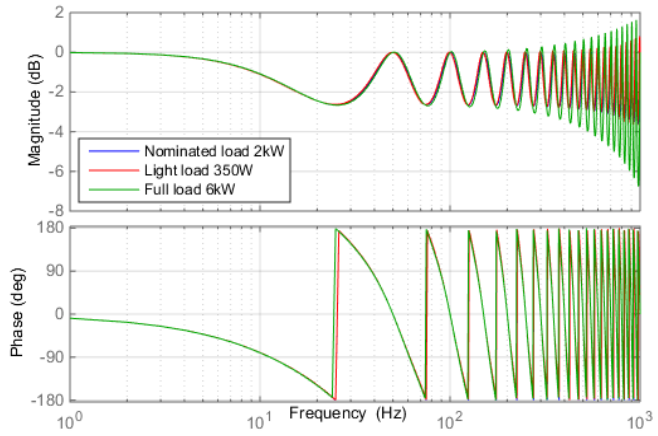
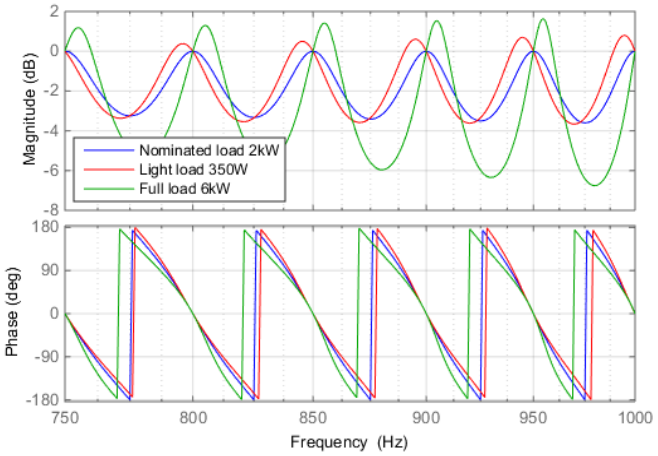


Fig. 8. Nyquist locus curve of equation (6) with $G_{f\_2kW}(z)$ and k_{RC} of 1.0 under 2kW linear load condition for RC stability verification.



(a) Complete view



(b) Zoomed in detail

Fig. 9. Completed closed-loop Bode plot of the direct RC system with $G_{f\_2kW}(z)$ and k_{RC} of 1.0 under 2kW (blue), 350W (red) and 6kW (green) load conditions.

E. Load Adaptive Algorithm

As analyzed in the previous section, a dedicated ZPS compensator shall be used for different load conditions, in order to obtain optimal reference tracking and noise rejecting capabilities. Based on the whole operating range of interest, the ZPS compensators are pre-evaluated according to the design procedure discussed above, and the associated coefficient of ZPS compensators are pre-stored in the micro-processor. To avoid unnecessary memory cost, a 1 kW tolerance band is introduced.

To apply the correct ZPS compensator, the operating condition of the power converter needs to be evaluated on a real-time basis. In order to relieve the system computation burden, the ADE7953 IC from Analog Devices is selected to perform power related calculations. It is able to acquire and elaborate up to the 24th harmonic of the output phase voltages and currents.

Fig. 10 illustrates the flow chart of the proposed load adaptive RC algorithm. The load adaptive algorithm is executed at a frequency of 2Hz. As soon as the algorithm starts, the load condition of each phase (i.e. the mean power level) is calculated, based on the data sent from the ADE7953 IC. If the load stays inside the 1 kW tolerance band, it is considered constant and the RC parameter is kept unchanged. When a large load change (i.e. load crossing different power levels) is detected, a sub-loop is triggered to adaptively update the RC parameter according to the new load condition.

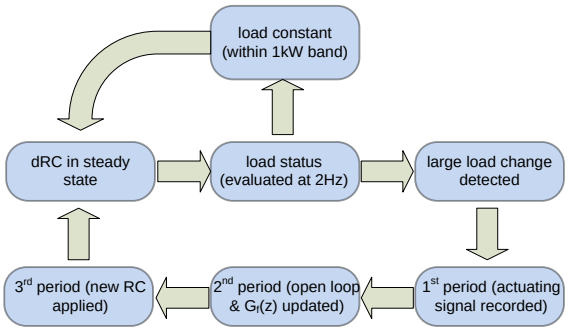


Fig. 10. Flow chart of the proposed load adaptive RC algorithm.

For the first following fundamental period, the current actuating signal is recorded by the micro-processor. Then, this recorded signal is applied as the actuating signal for the second fundamental cycle, which transfers the system into an open loop control. The use of this stage is essential, as it not only separates the current RC controller (mainly the ZPS compensator) from the system, but also ensures a smooth transition between the closed-loop and the open loop. During this open loop period, the internal variables of the RC is reset to zero, and the ZPS compensator parameter is updated from the pre-stored coefficients based on the new load condition. When this open loop cycle finishes, the new RC with the updated ZPS parameter is put back in to the control loop at the third fundamental cycle and the whole system recovers the closed-loop mode. This ends the load adaptive RC algorithm until the next load step action is detected.

IV. RESULTS

Prototypal realization of the 4-leg VSI as shown in Fig. 11 is used to experimentally investigate the load adaptive direct RC control system, while Fig. 12 shows the realized output power filter. Table I summarize the circuit parameter of the VSI and the filter.

Simulation results are achieved to investigate the behavior of the proposed control. Fig. 13 shows the voltage and current output the 4-leg VSI converter with non-linear load of 10kW, even in case of highly deformed line currents the phase voltage waveforms are sinusoidal shaped and show a very low THD. In order to evaluate the stability of the system, Fig. 14 depicts the Phase A voltage error signal of the control system when a step load change is applied. It can be noted that the system is stable and capable of reducing the error signal quickly and effectively.

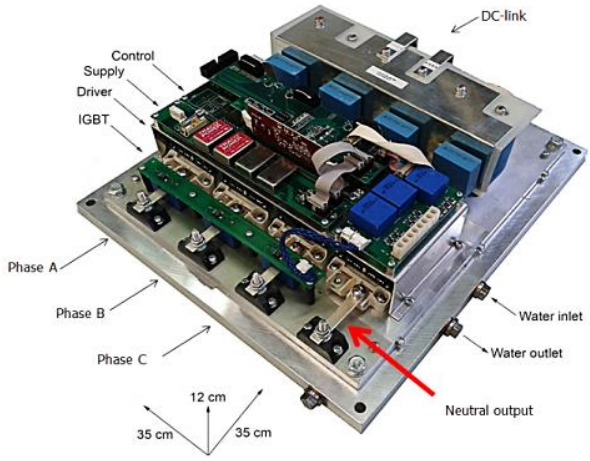


Fig. 11. Four-leg VSI prototype converter.

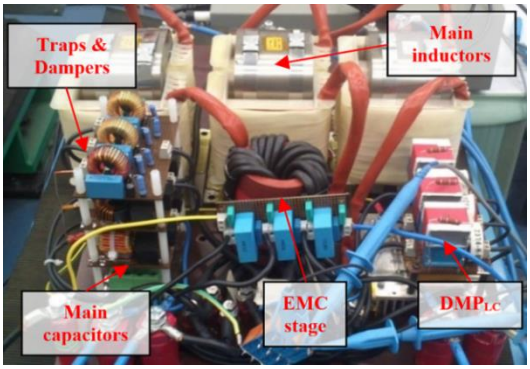


Fig. 12. Inverter output power filter.

The implemented algorithm is composed by different parts sequentially executed on the control platform. A detailed block scheme is reported in Fig. 15 where each task is highlighted. As soon as the main loop is called by the PWM interrupt service, system measures are acquired and the protection routine is executed. Second task is the evaluation of the inverter output power by communicating with the previously shown dedicated IC. If the resulting operating condition is outside the defined power band, then the load adaption part is executed and the new controller parameters are evaluated. After that, the main control structure, the direct Repetitive Controller, is finally executed and the new output modulating signal are sent to the PWM modulator.

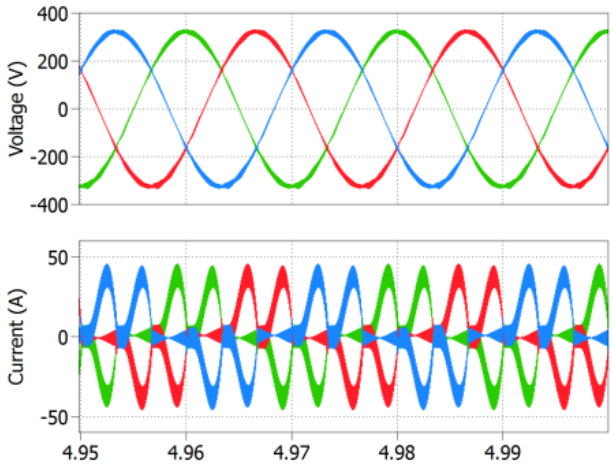


Fig. 13. Simulation results: voltage and current waveforms.

TABLE I – VSI AND OUTPUT FILTER PARAMETERS

L_k	800 µH	V_{dc}	700 V
C_{fl}	5 µF	I_{ph}	70 A
L_d	1 mH	$F_{sw}=F_{sample}$	12 kHz
C_d	2.2 µF + 0.47 µF	$F_{load-adaptiveZPS}$	500 Hz
R_d	15 Ω	R_t	50 mΩ
L_t	172 µH	C_t	2 x 0.56 µF

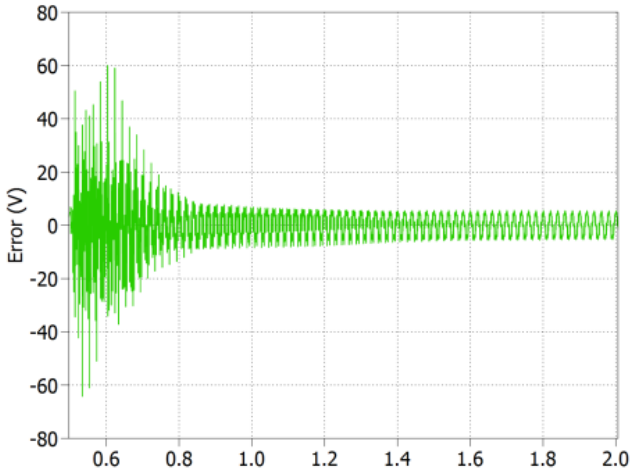


Fig. 14. Simulation results: phase A voltage error signal under step-load. change.

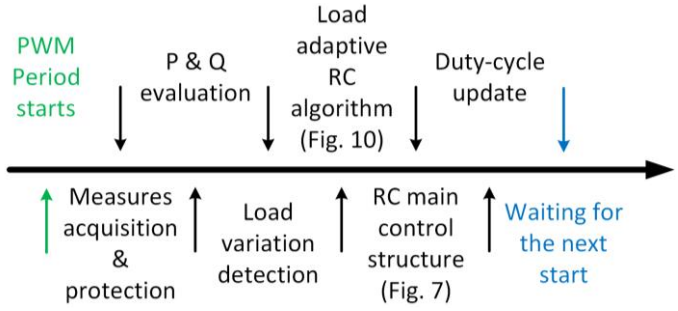


Fig. 15. Timeline of the implemented direct RC with load adaptive ZPH.

First experimental test to highlight the ZPS Direct Repetitive Control tracking capabilities has been accomplished by loading the 3-ph 4-leg VSI with a 6 kW balanced linear load. As it can be noticed from Fig. 16, the provided output voltages exhibit an ultra-low THD, resulting in negligible dead-time and harmonic distortion.

When non-linear balanced load is fed, such as a three phase diode rectifier having the parameters shown in Fig. 17, the proposed ZPS DRC is still able to fully compensate the output voltage harmonics. Current and voltage waveforms are shown in Fig. 18. Also in this case, voltage THD is still quasi-zero, and no difference in the voltage waveforms is evidenced with non-linear loads with respect to linear loads. Fig. 19 depicts the Fourier spectrum of the phase voltage in case of non-linear loads, both simulation spectrum and experimental spectrum are shown with reference to the limits of the international standard IEC 61000-2-4, which is related to the compatibility quality between the distribution network and devices. The IEC 61000-2-4 Class 1 sets the limits on the amplitude of single harmonics up to the 50th and the voltage THD lesser than or equal to 5%. From Fig. 19 it is evident as the proposed ZPS DRC assures a very low harmonic content in the full frequency range. The numerical values of the odd harmonics' amplitudes, up to the 19th order, are listed in Table II for both the simulations and the experimental results. The resulting experimental voltage THD is lower than 0.55%; which means a significant reduction with respect to results shown in [13], where the Zero-Phase-Shift capabilities were not considered.

Further experimental tests are achieved for unbalanced non-linear loads. The performance verification is accomplished by using a single phase diode rectifier as it is shown in Fig. 20. Even for such a critical load, ZPS DRC strategy is able to provide a quasi-zero THD of the output voltage as it is depicted in waveforms of Fig. 21.

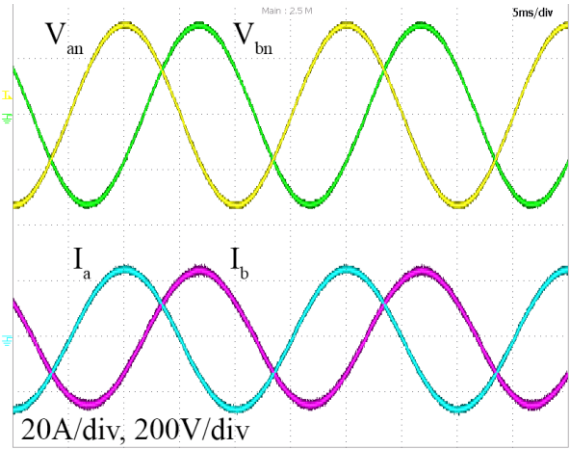


Fig. 16. Experimental results for three phase balanced linear load.

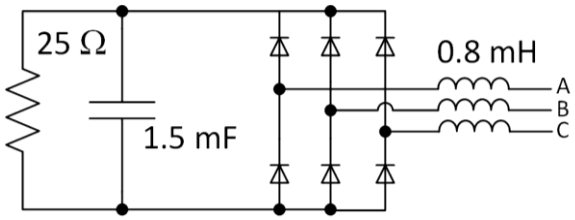


Fig. 17. Scheme of the balanced non-linear load.

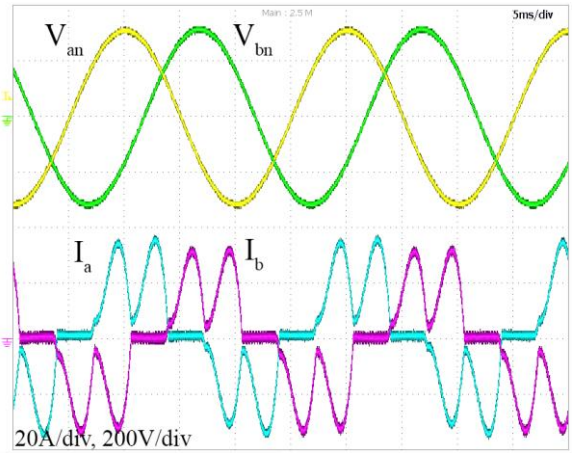


Fig. 18. Experimental results for the balanced non-linear load.

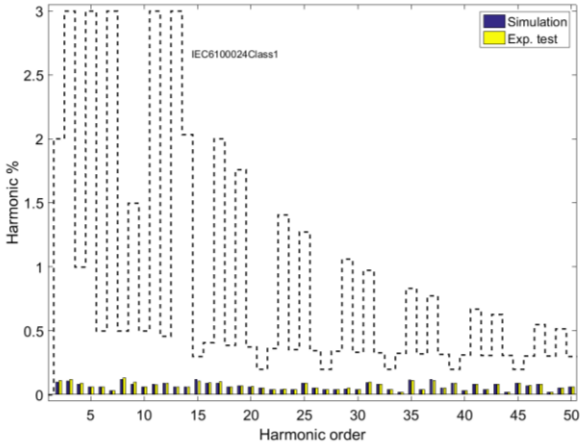


Fig. 19. Voltage Fourier spectrum for non-linear loads.

TABLE II – HARMONIC CONTENT OF THE PHASE-TO-NEUTRAL VOLTAGES WITH ZERO PHASE SHIFT DIRECT REPETITIVE CONTROL

Harmonic %	Simulation	Exp. test
3	0.105	0.11
5	0.061	0.064
7	0.032	0.033
9	0.08	0.099
11	0.08	0.0755
13	0.06	0.058
15	0.1	0.11
17	0.09	0.1
19	0.071	0.072

Proposed ZPS DRC algorithm have been tested also during load variations. In those cases, the controller has to detect at first the load changes by continuously monitoring the output power. It is accomplished evaluation the power on each phase separately. In fact, output load can be unbalanced and it has to be recognized to perform the DRC parameters adaption even during non-steady state conditions. Accordingly, Fig. 22 depicts the output voltage waveforms when the phase A load is changed from no-load condition to 4 kW resistive load. It can be notice the absence of oscillations on the phase-to-neutral voltages and the fast transient response of the proposed ZPS DRC.

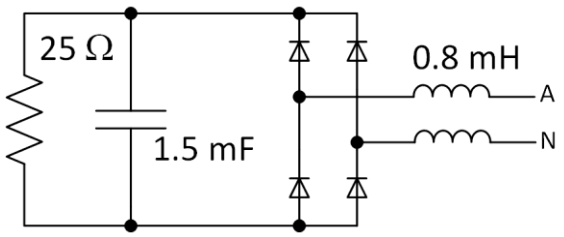


Fig. 20. Single phase non-linear load.

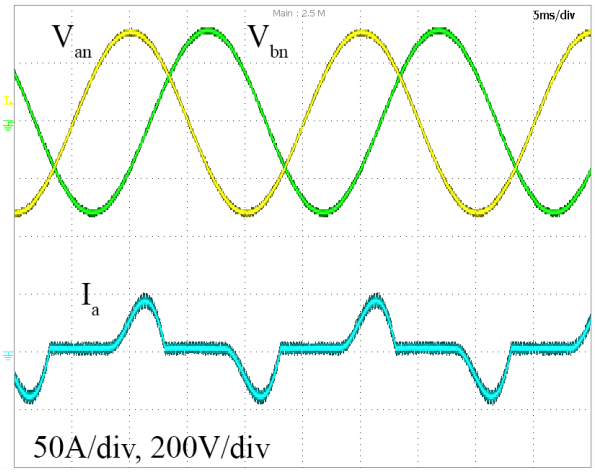


Fig. 21. Experimental results for the single phase non-linear load applied to phase A.

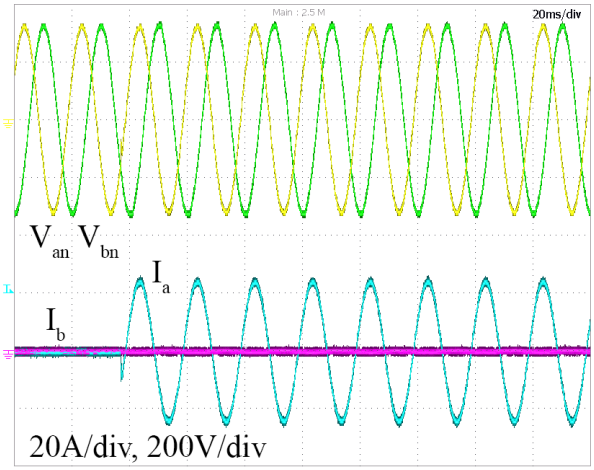


Fig. 22. Load step test from no-load to 4 kW pure resistive load.

Transient test is performed also for single-phase nonlinear loads. Fig. 23 illustrates the system behavior when the phase A load is changed from no-load to a 4 kW single-phase diode rectifier. Output voltage waveforms result in a very low distortion even during transient demonstrating the effectiveness of the Repetitive Controller in both transients and harmonic compensation conditions.

The effectiveness of the illustrated load adaptive zero phase shift algorithm has been tested under unbalanced load conditions. In Fig. 24 the VSI output is loaded as follows: phase A at no-load whereas phase B and C at 2 kW linear load each one. The comparison is performed disabling and enabling the proposed control structure. In Fig. 24a the load adaptive ZPS algorithm is not enabled, it can be noticed that phase B is completely stable whereas phase A starts oscillating due to the system resonance which interacts with the RC gains. Phase B and C are stable thanks to the linear load that acts as damper as previously illustrated in the paper. When the compensation algorithm is executed, results are shown in Fig. 24b where the stability of the system can be observed.

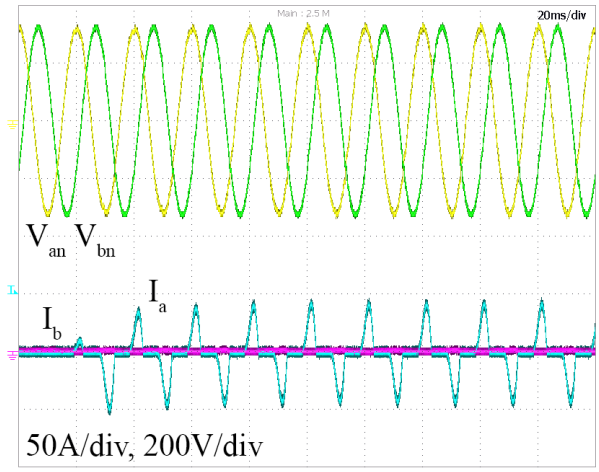
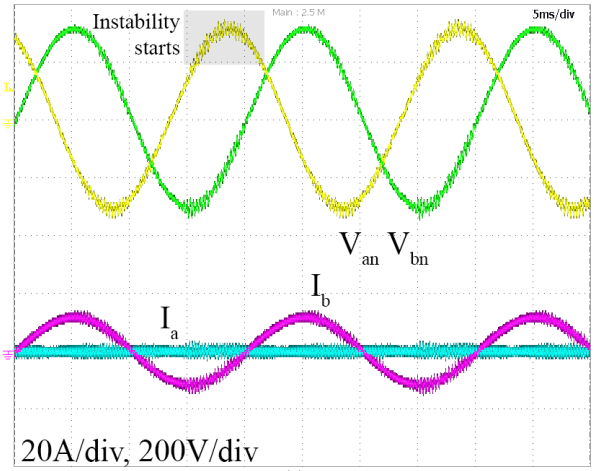
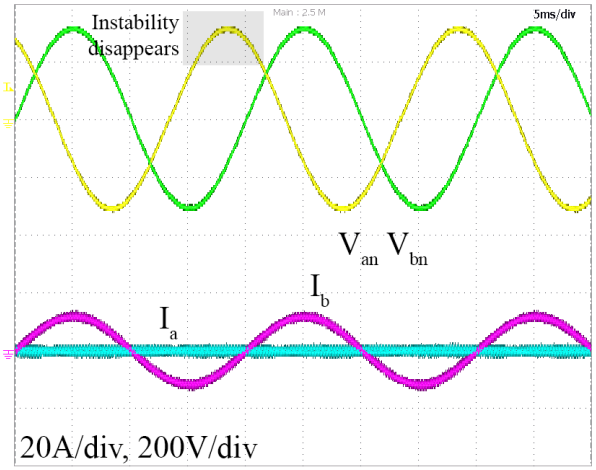


Fig. 23. Load step test from no-load to 4 kW single-phase diode rectifier load.



(a)



(b)

Fig. 24. Output voltages behavior under unbalanced linear load: phase A at no-load, phase B and C at 2.5 kW. (a) proposed load adaptive ZPS algorithm disabled. (b) load adaptive structure fully enabled.

Moreover, a similar comparison test has been performed where phase B and C are in the previous load condition of Fig. 25, whereas phase A is connected to a 6.5 kW pure resistive load. In this case, phase A controller has to deal with an increased phase shift introduced by the output power filter and load interactions. At shown, it causes a reduction of the stability margins for the RC higher frequencies. In fact, Fig. 25a depicts the output voltages and currents in such a load condition. It can be noticed how the phase A voltage starts oscillating being the phase compensation disabled. This is caused by the large amplitude amplification on the harmonic sidebands, due to the use of the improper ZPS compensator, as illustrated in Fig. 9. On the contrary, in Fig. 25b the system operates correctly, where the stability is increased due to the ZPH regulation.

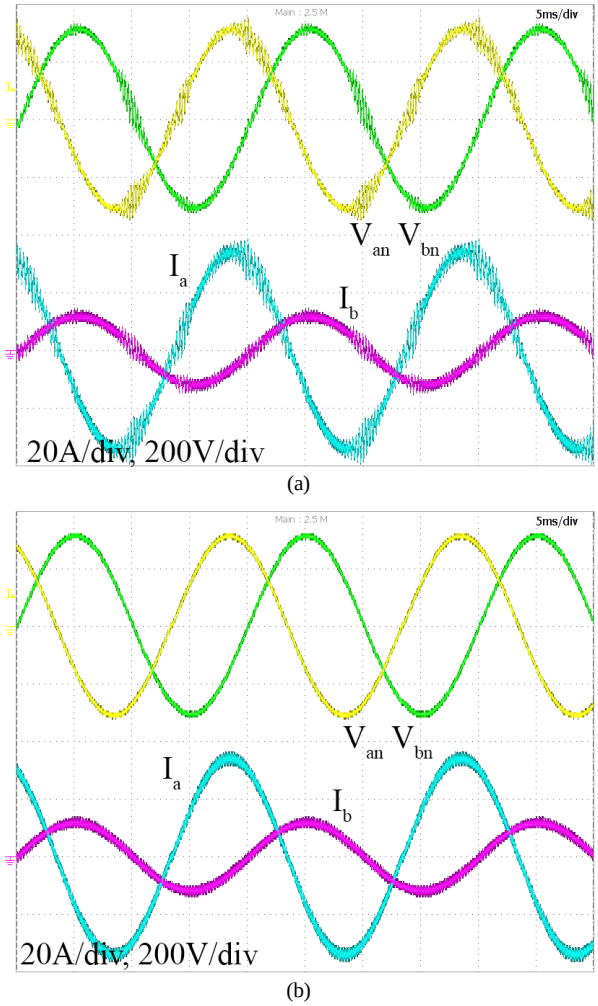


Fig. 25. System behavior under unbalanced linear load: phase A at 6.5 kW, phase B and C at 2.5 kW. (a) proposed load adaptive ZPS algorithm disabled. (b) load adaptive structure fully enabled.

V. Conclusions

Direct Repetitive Control for stand-alone VSI output voltage regulation has been improved by the adaptive Zero-Phase-Shift algorithm, which allows a lower reduction of the high frequency gains related to the RC. Zero-Phase-Shift algorithm is continuously evaluated by the VSI dedicated digital controller according to the whole system operating conditions. Depicted results confirm the benefits of the proposed improved control strategy. The inverter output voltages exhibit a negligible THD in all the presented operating conditions, even when non-linear balanced and unbalanced loads must be fed. Accordingly, thanks to the Zero-Phase-Shift algorithm, which provides better compensation of high order harmonics, the VSI output voltages are almost independent from the loads to be fed. Concluding, it makes the 3-ph 4-leg inverter with the proposed ZPS DRC an ideal candidate to supply sensitive loads in microgrid, in particular for stand-alone applications.

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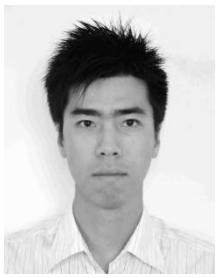

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