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Electrical performance of conducting polymer (SPAN) grown on GaAs with different substrate orientations

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This article reports the effect of n-type GaAs substrate orientation, namely (100), (311)A and (311)B, on the electrical properties of sulfonated polyaniline (SPAN)/GaAs heterojunction devices. In addition, the inhomogeneity of the interface between various GaAs substrates and SPAN is investigated in terms of barrier height and ideality factor by performing I-V measurements at different temperatures (20-420K). The I-V results indicate that the value of the rectification ratio (I_F/I_R) at 0.5V is higher for SPAN/(311)B GaAs samples than for SPAN/(100) GaAs and SPAN/(311)A GaAs samples. Moreover, the barrier height decreases and the ideality factor increases with decreasing temperature for all three heterostructure devices. The high value of mean barrier $\overline{\Phi}_b$ of SPAN/(311)B (calculated from the plots of Φ_{b0} as a function of $1/2kT$) confirms that the GaAs substrate orientation results in an increase of barrier homogeneities. Furthermore, the C-V characteristics were obtained at room temperature. The C-V measurements showed that the carrier distributions at the interface and away from the interface in high index (311) GaAs orientations are more uniform and have better barrier homogeneity than those grown on the conventional (100) GaAs substrates.

Keywords: (100) GaAs, (311)A GaAs, (311)B GaAs, I-V and C-V

1.   Introduction

Essentially conducting polymers, such as polyaniline (PANI), sulfonated polyaniline (SPAN), poly(p-phenylene-vinylene), polypyrrole, polyacetylene, polythiophene, etc., are promising semiconductors materials with confirmed technological potential due to their unique optical and electrical properties [1]. Among the family of organic semiconductors, the semiconducting polymers have attracted the most attention for applications in electronic and optoelectronic devices, particularly due to their exceptional electrical properties and easy synthesis [2–4]. As a result, this category of polymers has been used in several applications such as organic light emitting diodes (OLEDs) [5,6], solar cells [7,8], battery electrodes [9,10], photodiodes [11], energy storage [12], transistors [13], gas sensors [14], biosensors [15], radiation sensors [16], anti-corrosive coatings [17,18] and electromagnetic interference shielding [19].

Sulfonated polyaniline (SPAN), which is particularly a p-type semiconductor, represent a class of self-doped conducting polymers and a derivative of PANI, has received a great interest in recent years, because of its unique electroactive physical properties, enhanced process ability and potential industrial applications [20–22]. This material is environmentally stable over a wide range of temperatures. It can be grown as thin films over large areas at low cost [3]. In addition, SPAN has a big advantage in electronic circuitry design [8] because it forms Ohmic contacts with metals used in microelectronic applications such as Al, Ag and Cu. A typical band gap of SPAN is in the range 2.755–2.883eV [23].

On the other hand, in recent years III–V compound semiconductors, and in particular gallium arsenide (GaAs), have been used most frequently in the fabrication of electronic and optoelectronic devices. Recently, high index GaAs substrates, such as (311)B GaAs [24,25] and (311)A [24], have attracted much attention [25,26]. This is

because the optical properties of heterostructures grown on (311)A GaAs and (311)B GaAs are considerably better than those grown on (100) surfaces [24, 27].

As it is well known, the crystallographic orientation of the substrate has a significant effect on incorporation of impurities and defects and consequently on optical and electronic properties of III–V materials [28]. The ideality factor n and barrier height (BH) as well as the electrical characteristics are fundamental parameters of a Schottky barrier diode (SBD) and these give an indication about the quality of the Schottky interface. The SBD parameters must be determined over a broad range of temperatures because the analysis of the current-voltage (*I-V*) characteristics of the SBD measured only at room temperature does not provide accurate information about the conduction mechanism and the barrier nature created at metal semiconductor interface in order to understand these phenomena and determine precisely the parameters of the Schottky diodes. Chand et al.[29] and Hardikar et al.[30] analysed the experimental current-voltage data which revealed that there is an increase in the ideality factor and a decrease in the zero-bias barrier height with decreasing temperature. Consequently, the ideality factor and the barrier height established from forward *I-V* characteristics are found to be temperature dependent. This confirms that the Schottky barrier height is inhomogeneous in nature at the interface. This behaviour has been successfully described on the basis of the thermionic emission mechanism with Gaussian distribution of the barrier height [31].

To fabricate a hybrid organic/inorganic semiconductor heterojunction device with the aim to obtain specific optical and electrical properties on the bases of their doping levels, a thin organic film is deposited onto the surface of a conventional inorganic semiconductor substrate. This can be done by simple and inexpensive methods such as

spin coating used for thin film deposition at room temperature. Recently, a new technique of SPAN films preparation has been developed by Yang et al. [32].

==In this paper, we report on the fabrication and electrical characterization of Au/SPAN/GaAs heterojunctions grown on three different substrate orientations, namely n-type GaAs (100), (311)A and (311)B. We have investigated the effect of the substrate orientation on the heterojunction parameters such as barrier height and ideality factor as a function of the temperature. Additionally, in order to understand the behaviour of the devices barrier homogeneity Capacitance-Voltage (C-V) measurements were performed at room temperature.==

2.   Materials and Methods

2. 1. *Devices fabrication*

The n-type silicon-GaAs substrates with a concentration of $2 \times 10^{18} \, cm^{-3}$ were used to growth SPAN. The SPAN thin films have been grown on (100), (311)A and (311)B GaAs substrates by self-assembly. For this, after the cleaning process of substrates, a backside electrical contact of nickel (Ni)-gold (Au) was deposited by thermal evaporation using a BOC Edwards 306 system. For more details see procedure described elsewhere [13,33]. Subsequent to the backside electrical deposition, a 200 nm thick SPAN thin film was deposited onto the (100), (311)A and (311)B GaAs epitaxial layer at a rate of 1.8 nm/h by adopting a procedure based on the process initially developed by Yang et al. [32] and described in Ref.[13], except that the aniline and metanilic acid amounts (455 µl and 1.715 g, respectively) and the growth temperature (10 °C) are different. Finally, a circular electrical contact was obtained by thermal evaporation of 99.99% Au on the SPAN films with area of 0.0020 cm^2 for SPAN/(100)

GaAs, SPAN/(311)A GaAs and for SPAN/(311)B GaAs hybrids devices, as shown schematically in Fig. 1.

2. 2. *Device characterization*

The temperature dependence of the I-V characteristics in the temperature range of 20–420 K with intervals of 20K was measured by using a current source measurement unit (Keithley 236) and a closed-loop helium cryostat (Janis CCS-450). Capacitance-Frequency measurements were performed using LCR meter (Agilent E4980). The thicknesses of the thin films were measured on a profilometer (Dektak 6M).

3. **Results and Discussion**

3.1. *Current–Voltage Characteristics*

The electrical I-V measurements were performed in the temperature range of 20-420 K with a temperature step of 20 K on SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs samples to study the diode parameters such as the series resistance (Rs), the ideality factor (n) and the barrier height (ϕ_{Bo}). Typical forward and reverse bias I-V characteristics of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs n-type heterostructures in a semi-logarithmic scale are shown in Fig. 2(a–b), respectively. Fig. 2(d) shows a semi-logarithmic I-V plots at room temperature of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs. Clearly as illustrated in Fig. 2(d), the SPAN/(311)B GaAs heterostructures exhibit better I–V characteristics than those of SPAN/(100) GaAs and SPAN/(311)A GaAs devices. It was observed that

at room temperature and applied voltage of 0.5 V the value of the rectification ratio (which is the ratio of forward current (I_F) to the reverse current (I_R)) is approximately 2×10^2, 3.7×10^3 and 1.7×10^4 for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs samples, respectively. It is worth noting that the rectification value is highest in samples grown on (311)B GaAs substrates. This is one of the indications that the interface charges between SPAN and GaAs (311)B substrates are the lowest.

In order to explore further the electrical behaviour of the organic/inorganic semiconductor devices parameters such as series resistance, barrier height and ideality factor are extracted by modelling the devices as Schottky diodes. As can be seen from Fig. 2(a, b and c), the forward bias *I-V* plots were not perfectly linear and displayed a downward concave curvature at high voltage. This downward curvature originates from the presence of a small series resistance *(Rs)* as determined from the analysis of the experimental forward I-V characteristics. The obtained values of *Rs* ranged from 6.5–8.25 Ω, 12–20.7 Ω and 8.7–11 Ω for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B, respectively. The experimental current–voltage (I–V) data were modelled by the well-known thermionic emission (TE) equation at forward bias (V ≥ $3k$T/q) [34].

$$I = I_0 \exp\left(\frac{qV}{nkT}\right)\left[1 - exp\left(-\frac{qV}{kT}\right)\right] \qquad (1)$$

where I_0 is the saturation current determined by extrapolating the linear portion in the *ln(I)* versus *V* plot (Fig. 3) to the intercept point on the current axis at V = 0 [35] and defined by

$$I_0 = S\,A^*\exp\left(\frac{-q\Phi_{b0}}{kT}\right) \qquad (2)$$

When I_0 is determined, the barrier height Φ_{b0} can be calculated using equation (3)

$$\Phi_{b0} = \frac{kT}{q} \ln\left(\frac{S\,A^*T^2}{I_0}\right) \qquad (3)$$

In the above equations, q is the electronic charge, V is the forward-bias voltage, k is the Boltzmann constant, T is the absolute temperature, Φ_{b0} is the zero-bias barrier height, S is the effective diode area, and A^* is the effective Richardson constant of 8.16 $Acm^{-2}k^{-2}$ for n-type GaAs [35]. From equation (1), the ideality factor 'n', which is a dimensionless quantity, represents a measure of the conformity of the diode behaviour to pure thermionic emission. n can be expressed as

$$n = \frac{q}{kT}\left(\frac{dV}{d\,lnI}\right) \qquad (4)$$

According to the TE theory, the zero-bias BH Φ_{b0} and the ideality factor $n,$ for all three samples, are determined from intercepts and slopes of the forward-bias $ln(I)$ versus V plot at each temperature (Fig. 3), respectively. For SPAN/(100) GaAs heterojunctions, the values of Φ_{b0} and n changed from 0.039 eV and 25.24 (at 20K) to 0.76 eV and 1.48 (at 420 K), respectively. Whereas, for SPAN/(311)A GaAs device, these values change from 0.044 eV and 22.44 to 0.80 eV and 1.44, respectively, for the same temperature range. While for SPAN/(311)B GaAs devices the obtained values of Φ_{b0} and n varied from 0.053 eV and 19.4 to 0.86 eV and 1.4, respectively. The high quality of the SPAN/n-GaAs devices is confirmed by the high values of Φ_{b0} and the low values of n (an ideal diode has an n of 1) at room temperature. It can be seen from Fig. 4(a) and (b) that the zero-bias barrier height and ideality factor reveal strong temperature dependence, that is the value of Φ_{b0} decreases and n increases with the decrease of temperature for all three devices. This behaviour was also observed in polyaniline/porous silicon heterojunctions by El-zohary et al. [1]. The current transport

across the organic/inorganic interface is a temperature activated process, where electrons at low temperatures are able to overcome only the lower barriers and as a result, the current transport will be dominated by the current flowing through the regions of lower Φ_{b0} and larger n [1]. This means that more and more electrons have sufficient energy to surmount a higher barrier when the temperature increases. Subsequently, in addition to the regions of the heterojunction with low barrier heights, the dominant barrier heights in other regions will increase with temperature and voltage bias [35, 36]. Furthermore, an apparent decrease in BH and increase in ideality factor at low temperatures are due to the barrier inhomogeneity and other effects such as defects, thickness inhomogeneity and non-uniformity of the interfacial charges [30].

The zero-bias barrier height at room temperature, as seen in Fig. 4(a) is calculated to be 0.62 eV, 0.67 eV and 0.72 eV for the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterostructures, respectively. Φ_{b0} of SPAN grown on (311)B GaAs substrate is greater than that of SPAN grown on (100) and (311)A GaAs substrates. This value is also greater than the value reported by Felix et al. [37] for SPAN/4H-SiC hybrid devices. In addition, the ideality factor at room temperature is determined to be 1.77 for the SPAN/(100) GaAs, 1.63 for SPAN/(311)A GaAs and 1.61 for SPAN/(311)B GaAs devices, as shown in Fig. 4(b). Taking into account the fact that $n = 1$ for an ideal diode, it is observed that n values differ from unity for all the three devices, however the SPAN/(311)B GaAs device is nearest to the ideal case. When the experimental values of n are higher than unity, this deviation from unity is attributed to the bias dependence of the barrier height and barrier inhomogeneity. The high values of the ideality factor are also probably due to a potential drop in the interfacial layer and the presence of excess current as well as the recombination current through the interfacial states between the n-GaAs substrate and the SPAN organic layer [38]. It is

worth pointing out that the higher barrier height and lower ideality factor values for SPAN/(311)B GaAs devices is an evidence of their excellent electrical properties and good homogeneities when compared with SPAN grown on (100) and (311)A GaAs heterojunctions. It is important to note that the electrical properties and barrier homogeneities of SPAN grown on (311)A plane are better than those of sample grown on (100) orientation. Therefore, the substrate orientation has a strong impact on the electrical properties and barrier inhomogeneities of the devices.

Fig. 5(a – c), show the variation of Φ_{b0} as a function of n for the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions, respectively. According to these figures, the barrier height is correlated linearly with the ideality factor with an extrapolated Φ_{b0} at $n = 1$ that would correspond to the laterally homogeneous barrier height and for which pure TE applies as the unique mechanism through which conduction takes place. Note that the Φ_{b0} versus n characteristics for the three devices show two linear regions, namely first region (Fr) and second region (Sr), over two temperature ranges (420-200K) and (180-40K), respectively, with two extrapolated barrier heights at $n = 1$. For SPAN/(100) GaAs hybrid devices (Fig. 5(a)), the value of Φ_{b0} at $n = 1$ of Fr and Sr regions is 0.86 eV and 0.49 eV, respectively. While for SPAN/(311)A GaAs devices, the value of Φ_{b0} at $n = 1$ of the Fr region is 0.94 eV and of the Sr region is 0.55 eV, as shown in Fig. 5(b). However, for SPAN/(311)B GaAs devices, these values are 0.99 eV and 0.61 eV for the same regions, as shown in Fig. 5(c).

The value of barrier height Φ_{b0} at $n = 1$ of Fr and Sr regions for the three devices are presented in Table 1, where one can observe that the Φ_{b0} value of Fr region and Sr region increase as the substrate orientation n-GaAs is changed from (100) to (311)A and (311)B GaAs. This investigation confirms that the orientation of the substrate plays a

significant role in improving the electrical properties and barrier homogeneity of the devices. Sellai et al. [39] pointed out that the barrier height found by extrapolation to *n = 1* may be considered as a reasonable good estimate for the homogeneous barrier height. Thus, the barrier of SPAN/(311)B GaAs samples is more homogeneous, because Φ_{b0} value at *n = 1* for both regions are higher than those of (100) GaAs and (311)A GaAs samples.

The barrier height can also be determined by rewriting equation (3) (see equation 5) and using the Richardson plot of the saturation current

$$\ln\left(\frac{I_0}{T^2}\right) = \ln(S\,A^*) - \frac{q\Phi_{b0}}{kT} \qquad (5)$$

The plots of $\ln(I_o/T^2)$ versus 1000/T for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions are depicted in Fig. 6. The experimental data are seen to fit well with a straight line over a wide range of temperatures. According to equation (5), the plot of $\ln(I_o/T^2)$ versus 1000/T yields the zero-bias barrier height Φ_{b0} from the slope and the Richardson constant from the intercept of the straight line. The zero-bias barrier height Φ_{b0} values as obtained from the slope of the straight lines portion of the curves for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs devices are 0.18 eV, 0.29 eV and 0.38 eV, respectively. The higher barrier energy value for SPAN/(311)B GaAs devices could be indicative of less traps and defects, and therefore better electrical properties and homogeneity, when compared with SPAN grown on (100) and (311)A GaAs substrates. On the other hand, the value of Richardson constants obtained from the intercept of the straight lines portion of the curves and are 3.53×10^{-7} Acm^{-2}K^{-2}, 3.75×10^{-6} Acm^{-2}K^{-2} and 1.2×10^{-5} Acm^{-2}K^{-2} for SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs hybrid devices,

respectively. These values are much lower than the well-established value of 8.16 Acm^{-2}K^{-2} for n-type GaAs. These deviations from the known Richardson constant may be due to the spatial inhomogeneous barrier and potential fluctuations at the interface that consist of low and high barrier areas. Moreover, nonlinear behaviour of $\ln(I_o/T^2)$ as a function of 1000/T plot at low temperatures is as a consequence of the extra current contribution arising from the reduction in the barrier height [29, 40]. Although the Richardson constant values for the three devices differ from the expected Richardson value, SPAN/(311)B GaAs devices have the closest values. Consequently, it is worth pointing out that the samples grown on (311)B GaAs substrates are more homogeneous than samples grown on (100) and (311)A substrates.

The decrease in the ideality factor and the increase in barrier height with the increase of temperature can also be explained on the basis of a thermionic mechanism with Gaussian distribution of barrier heights due to the barrier height inhomogeneities prevailing at organic/inorganic semiconductor interface [41]. In other words the increase of the value of n with decrease of temperature is direct result of the bias dependence of the mean barrier $\overline{\Phi}_{b0}$ and the standard deviation σ of the Gaussian distribution of barrier heights in Schottky diodes. The Gaussian distribution of the barrier heights and variation of the ideality factor with temperature are expressed by the following equations[41,42].

$$\Phi_{b0} = \overline{\Phi}_{b0} - \frac{q\sigma^2}{2kT} \qquad (6)$$

and

$$\left(\frac{1}{n} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \qquad (7)$$

It is assumed that both the mean barrier at a given voltage ($\overline{\Phi}_b$) as well as σ^2 are linearly bias dependent on Gaussian parameters such as $\overline{\Phi}_b(V) = \overline{\Phi}_{b0} + \rho_2 V$

11

and $\sigma^2(V) = \sigma_0^2 + \rho_3 V$ [43], where $\overline{\Phi}_{b0}$, σ and n are mean barrier height, standard deviation of the barrier height distribution and the ideality factor, respectively. Usually the temperature dependence of σ is small and can be neglected. The coefficients ρ_2 and ρ_3 are the voltage deformation of the barrier height distribution. The plots of Φ_{b0} as a function of $1/2kT$ and $(n^{-1}-1)$ as a function of $1/2kT$ are shown in Fig. 7(a–c) for the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions, respectively. The plot of Φ_{b0} versus $1/2kT$ (Fig. 7(a), for SPAN/(100) GaAs) should be a straight line that gives $\overline{\Phi}_{b0} = 0.974$ eV from the intercept and $\sigma = 0.132$ V from the slope. In contrast, for SPAN/(311)A GaAs (see Fig. 7(b)) and SPAN/(311)B GaAs (see Fig. 7(c)), the values of $\overline{\Phi}_{b0}$ increased to 1.014 eV and 1.08 eV, respectively. However, σ is reduced to 0.130 V for SPAN/(311)A GaAs and 0.128 V for SPAN/(311)B GaAs. It is important to point out that the value of σ is not small compared to $\overline{\Phi}_{b0}$ value for all the three samples, confirming the presence of the interface inhomogeneties [42]. These values are displayed in Table 2. S. Chand and J. Kumar [42] argued that the decrease of the standard deviation leads to an increase in the barrier height and a decrease in the ideality factor. The standard deviation σ is a measure of the barrier homogeneity. The lower value of σ corresponds to a more homogeneous barrier height. Accordingly, the SPAN/(311)B GaAs devices have better homogeneity and excellent electrical properties when compared with SPAN grown on (100) and (311)A GaAs. The plot of $(n^{-1}-1)$ versus $1/2kT$ as illustrated in Fig. 7(a–c) is a straight line that gives the voltage coefficients ρ_2 and ρ_3 from the intercept and slope of the plot as $\rho_2 = -0.117$ and $\rho_3 = -0.0160$ for the SPAN/(100) GaAs hybrid devices (Fig. 7(a)), while these coefficients are changed to -0.104 and -0.0150, respectively, for the SPAN/(311)A GaAs hybrid devices (Fig. 7(b)). Whereas, for SPAN/(311)B GaAs hybrid devices (Fig. 7(c)), the values of ρ_2 and ρ_3 are -0.08 and -0.0145, respectively. These values for the three samples are

illustrated in Table 2. From this table it can be seen that the value of σ^2, ($-\rho_2$) and ($-\rho_3$) is decreased by changing the substrate orientation n- GaAs from (100) to (311)A and (311)B GaAs. Boyarbay et al.[41] investigated the electrical properties of the Au/PANI/p-Si/Al and Au/PANI TiO2 TTAB/p-Si/Al heterojunctions. They reported that the value of mean barrier $\overline{\Phi}_{b0}$ decreases due to $\rho_2 < 0$ and the value of σ^2 decreases with decreasing ($-\rho_3$). The same behaviour has been observed in this study, thus, the value of $\overline{\Phi}_{b0}$ increases as the substrate orientation is changed from (100) to (311)A and (311)B GaAs. It means that $\overline{\Phi}_{b0}$ of sample grown on (311)B substrate is greater than that of (100) and (311)A. However, σ^2 value of the SPAN/(311)B GaAs sample decreased with decreasing ($-\rho_3$) leading to an increase in barrier height. This confirms that the SPAN/(311)B samples have better barrier homogeneity and electrical properties than the other two samples.

3.2. *Capacitance–Voltage Characteristics*

In order to investigate further the barrier height homogeneity of the three samples, the capacitance (C) as a function of voltage measurements were performed at room temperature (300K). The C-V characteristics for the three devices demonstrate that the capacitance increases as the reverse voltage tends to zero, as presented in Fig. 8. On the other hand, as seen in Fig. 9(a), the $1/C^2$ versus V characteristics of the SPAN/(100) GaAs is not linear indicating that the doping (concentration of carriers as a function of depletion width) in the bias range -1.5V to 0V is neither uniform nor linearly graded [43]. These results infer non-uniformity in the carrier distribution at the interface and away from the interface. These effects could cause a non-homogeneous or a spatially distributed barrier potential at the interface. However, the experimental C-V data

represented as $1/C^2$ versus V plots for the SPAN/(311)A GaAs and SPAN/(311)B GaAs diodes (Fig. 9(b) and (c)) reveal approximately a linear behaviour which indicates that the doping is uniform in the same bias range (depletion region). As a result, the carrier distribution at the interface and away from interface is uniform and consequently the barrier height could be more homogeneous for SPAN grown on (311) GaAs orientations.

4.   Conclusion

Organic semiconducting polymer SPAN grown on (100), (311)A and (311)B GaAs substrates have been investigated. The current-voltage characteristics of the three samples show that the value of the rectification ratio (I_F/I_R) at 0.5V is higher for SPAN/(311)B GaAs samples than for SPAN/(100) GaAs and SPAN/(311)A samples. Furthermore, a lower Φ_{b0} and higher n values in the sample grown on (100) and (311)A GaAs could be attributed to more barrier inhomogeneity and other effects such as defects and non-uniformity of the interfacial charges than in the samples grown on the (311)B GaAs. The high values of Richardson constant and mean barrier $\overline{\Phi}_b$ also confirm that the GaAs substrate orientation results in an increase of barrier homogeneities. This is also supported by the higher value of ρ_2 and smaller value of ρ_3 observed in the SPAN/(311)B GaAs samples. The value of $\overline{\Phi}_b$ increases due to $(-\rho_2)$ and σ_0 decrease with decreasing $(-\rho_3)$. Moreover, the C-V measurements provide evidence that the carrier distributions at the interface and away from the interface in high index (311) GaAs orientation are more uniform and have better barrier homogeneity than those of samples grown on the conventional (100) GaAs substrates. Other studies on structures based on non-organic semiconductors grown on similar

substrate orientations of GaAs have also shown that the high index planes play a role in improving the electrical properties of the samples. However, it is clear from this work that the barrier homogeneity and electrical properties of the sample grown on the (100) GaAs are not as good as those of the SPAN samples grown on the high index (311) GaAs and particularly SPAN/(311)B GaAs.

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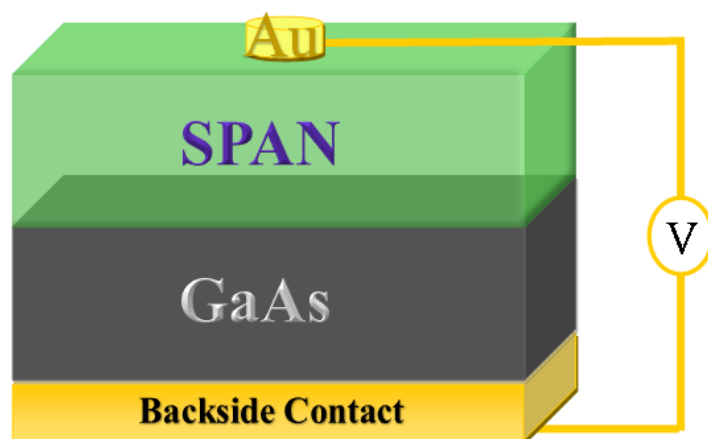
Figure Captions

Fig. 1: Layer structure of sulfonated polyaniline (SPAN) grown on (100), (311)A and (311)B GaAs substrates by self-assembly technique.
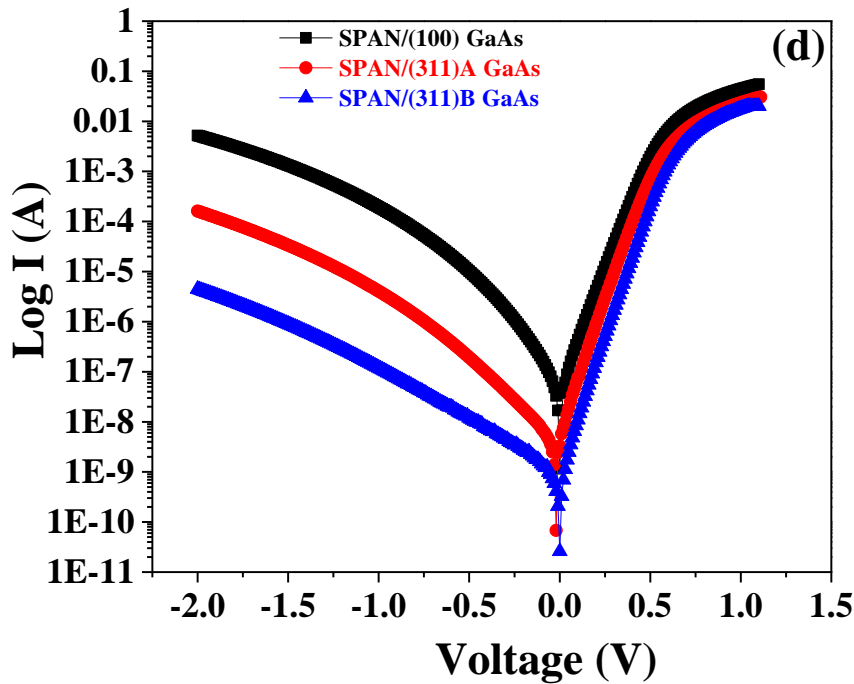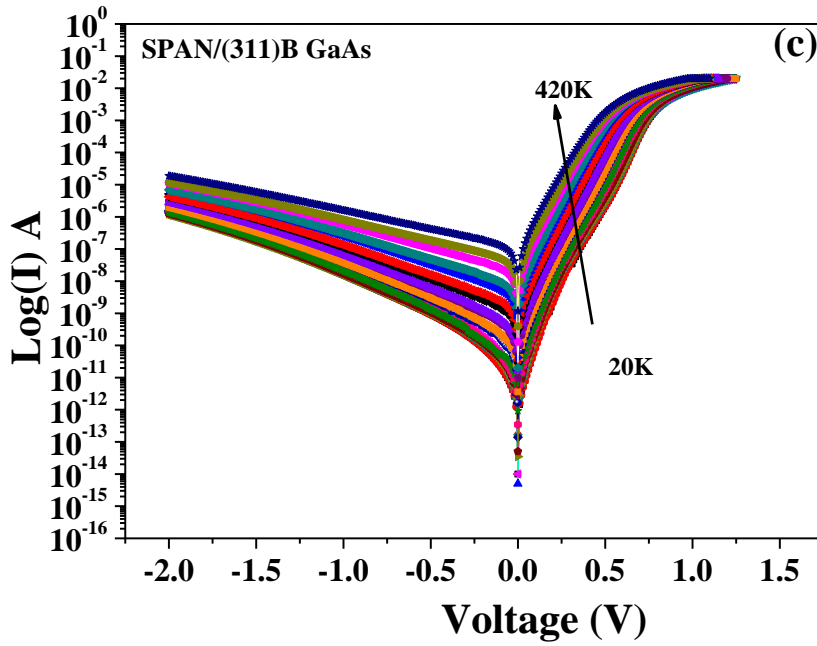
Fig. 2: Semi-logarithmic plots of dark I–V characteristics of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs, (c) SPAN/(311)B GaAs hybrid devices in the temperature range of 20–420 K at 20 K intervals and (d) Semi-logarithmic plots of dark I–V characteristics of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs hybrid devices at room temperature (300 K).
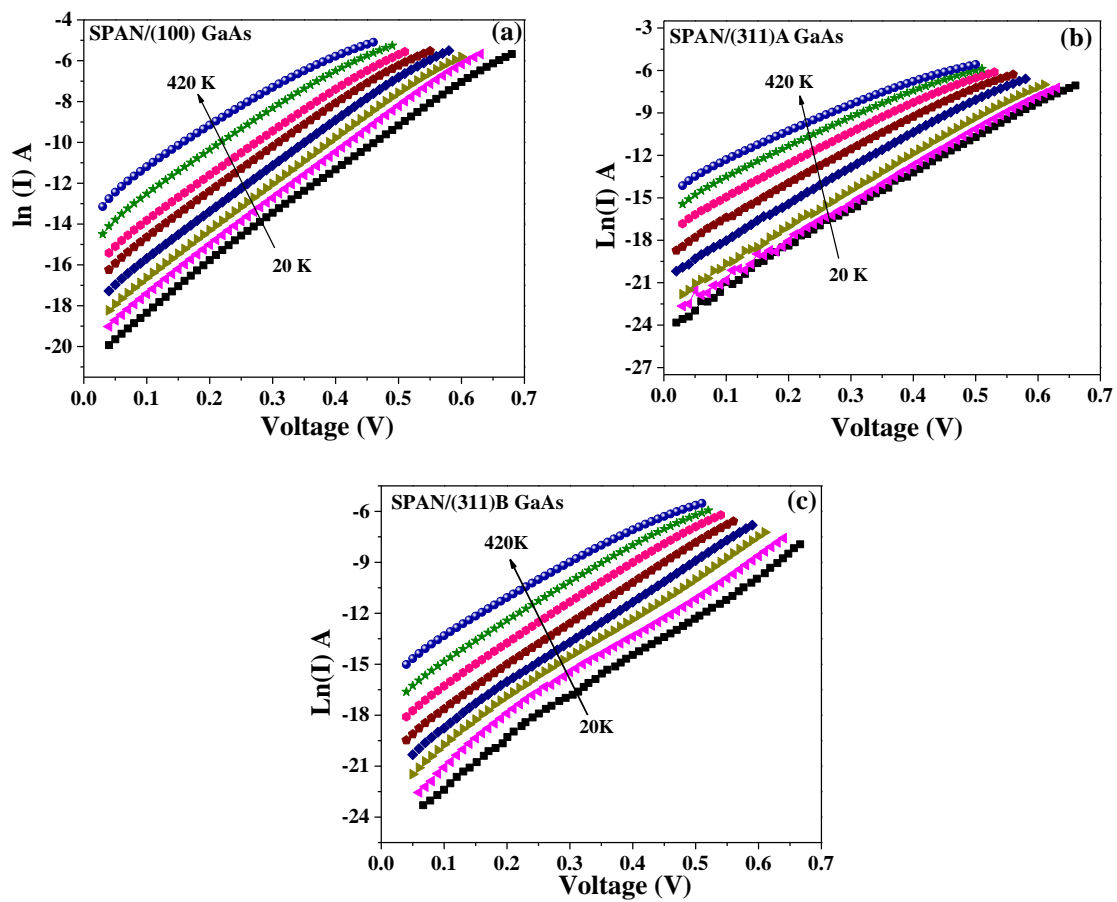
Fig. 3: Dark ln(I) versus bias voltage (V) characteristics for (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311)B GaAs heterojunctions at selected temperatures for clarity.

Fig. 4: Temperature dependence of (a) the barrier height and (b) ideality factor of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions determined from *I–V* characteristics in the temperature range of 20-420K at 20K intervals.

Fig. 5: Barrier height versus ideality factor of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311)B GaAs devices at various temperatures.

Fig. 6: Richardson plots for the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions.

Fig. 7: Zero-bias barrier height and ideality factor vs. 1/2kT curves of (a) the Au/SPAN/n-(100) GaAs, (b) the Au/SPAN/n-(311)A GaAs and (c) the Au/SPAN/n-(311)B GaAs diodes according to Gaussian distribution of the barrier heights.

Fig. 8: C-V characteristics of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311)B GaAs diodes at room temperature (300K).

Fig. 9: Measured $1/C^2$ vs. V characteristics of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311) B GaAs diodes at room temperature (300 K).

Table 1

Table 1: Summery of barrier height of both regions (Fr and Sr) at $n = 1$ for SPAN/(100), (311)A and (311)B GaAs samples.

Sample Name	Barrier height Φ_{b0} of Fr region (eV)	Barrier height Φ_{b0} of Sr region (eV)
SPAN/(100) GaAs	0.86	0.49
SPAN/(311)A GaAs	0.94	0.55
SPAN/(311)B GaAs	0.99	0.61

Table 2

Table 2: Mean barrier height $\overline{\Phi}_{b0}$, standard deviation σ and voltage deformation coefficients (ρ_2 and ρ_3) of the barrier height for SPAN/(100), (311)A and (311)B GaAs samples.

Sample name	$\overline{\Phi}_{b0}$ (eV)	σ^2 (V^2)	σ (V)	ρ_2	ρ_3
SPAN/(100) GaAs	0.974	0.0174	0.132	-0.117	-0.0160
SPAN/(311)A GaAs	1.014	0.0169	0.130	-0.104	-0.0150
SPAN/(311)B GaAs	1.08	0.0164	0.128	-0.08	-0.0145

Fig. 1: Layer structure of sulfonated polyaniline (SPAN) grown on (100), (311)A and (311)B GaAs substrates by self-assembly technique.

Figure 2
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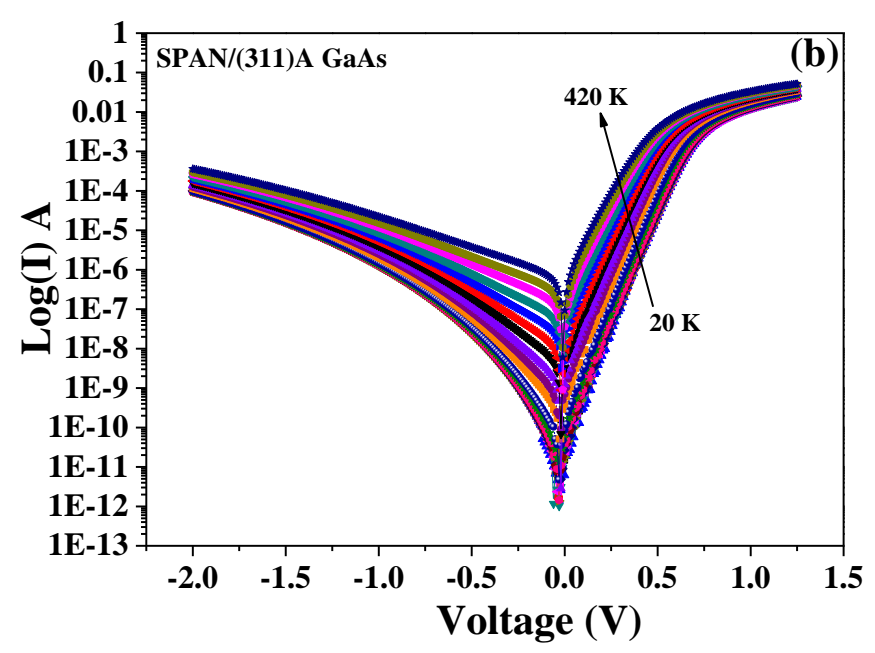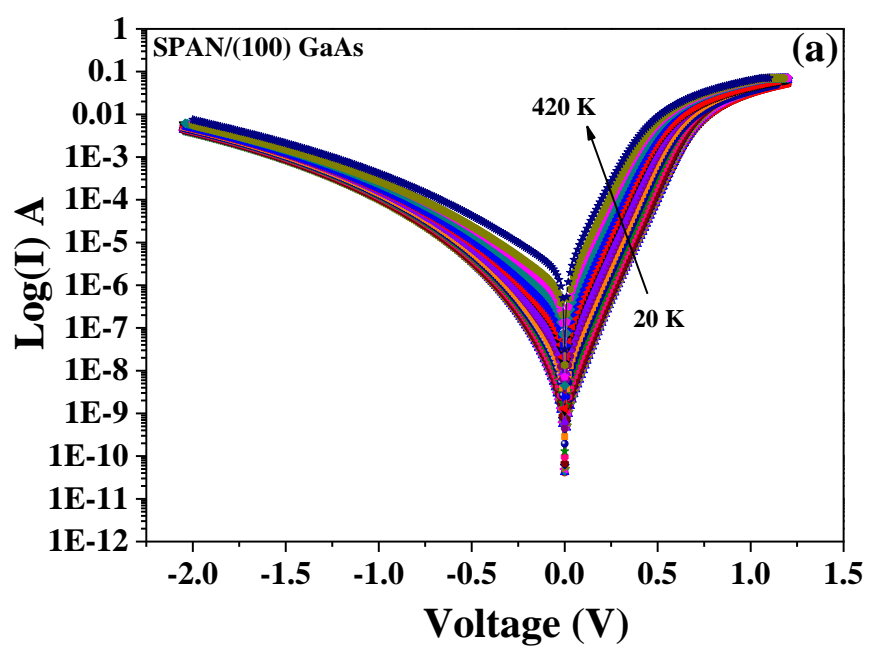
Fig. 2: Semi-logarithmic plots of dark I–V characteristics of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs, (c) SPAN/(311)B GaAs hybrid devices in the temperature range of 20–420 K at 20 K intervals and (d) Semi-logarithmic plots of dark I–V characteristics of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs hybrid devices at room temperature (300 K).

Figure 3
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Fig. 3: Dark ln(I) versus bias voltage (V) characteristics for (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311)B GaAs heterojunctions at selected temperatures for clarity.

Figure 4
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Fig. 4: Temperature dependence of (a) the barrier height and (b) ideality factor of SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions determined from *I–V* characteristics in the temperature range of 20-420K at 20K intervals.

(a) SPAN/(100) GaAs

$\Phi_{bo} = 1.16 - 0.3\,n$ — Fr

$\Phi_{bo} = 0.56 - 0.07\,n$ — Sr

Barrier Height (eV)

Ideality factor

(b) SPAN/(311)A GaAs

$\Phi_{bo} = 1.27 - 0.33\,n$ — Fr

$\Phi_{bo} = 0.63 - 0.08\,n$ — Sr

Barrier Height (eV)

Ideality factor

Fig. 5: Barrier height versus ideality factor of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311)B GaAs devices at various temperatures.
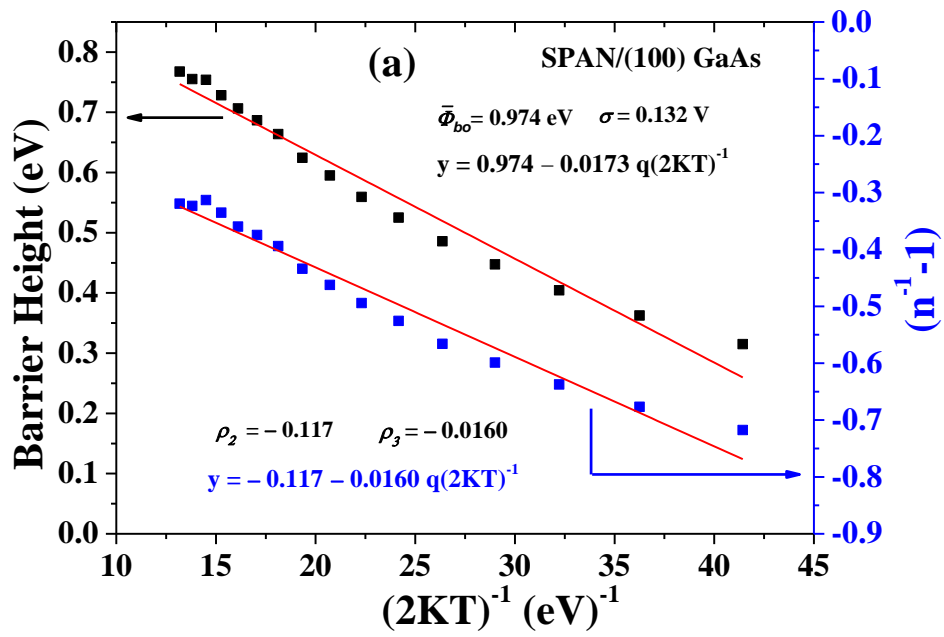
Figure 6
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Fig. 6: Richardson plots for the SPAN/(100) GaAs, SPAN/(311)A GaAs and SPAN/(311)B GaAs heterojunctions.

Figure 7
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Fig. 7: Zero-bias barrier height and ideality factor vs. 1/2kT curves of (a) the Au/SPAN/n-(100) GaAs, (b) the Au/SPAN/n-(311)A GaAs and (c) the Au/SPAN/n-(311)B GaAs diodes according to Gaussian distribution of the barrier heights.
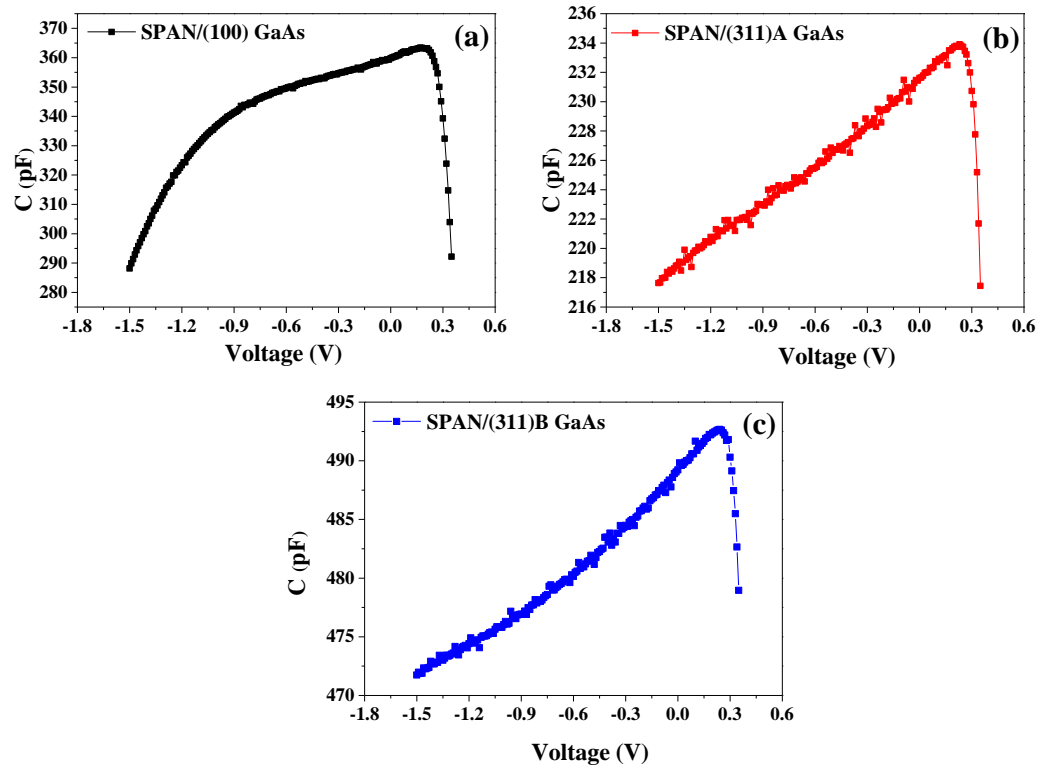
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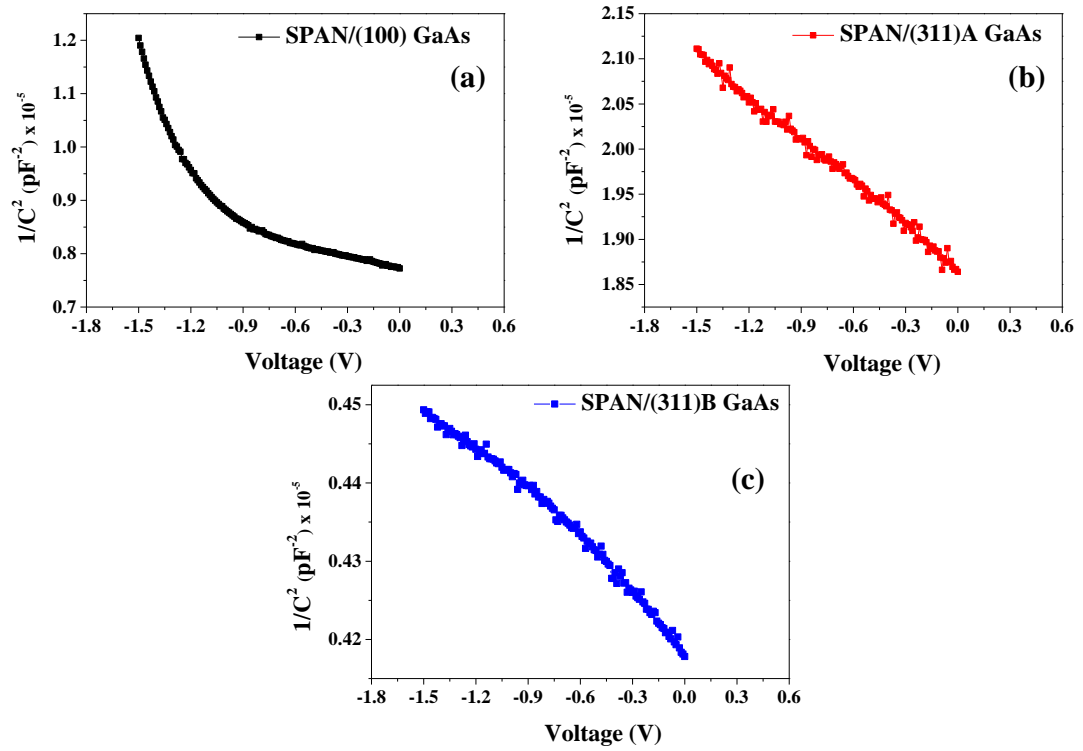
Fig. 9: Measured $1/C^2$ vs. V characteristics of (a) SPAN/(100) GaAs, (b) SPAN/(311)A GaAs and (c) SPAN/(311) B GaAs diodes at room temperature (300 K).