Experimental Validation of a Hybrid Converter with Enhanced Switching Ripple Cancellation

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Abstract: This study presents the experimental evaluation of a proposed new three phase hybrid converter topology for medium voltage applications. The topology is based on the interconnection of a low switching frequency voltage source inverter (VSI), rated at medium voltage, with a high switching frequency low-power rated current source inverter (CSI). The main function of the shunt connected CSI is to cancel the large switching current ripple produced by the VSI while operating at a reduced fundamental voltage enabled by the use of series connected capacitors. The simulations and design procedure outline the possibility of achieving high output grid current quality whilst the added installed power by the CSI remains at <4% compared with the VSI. The experimental results show good correlation between analytical simulated targets of 20% maximum CSI voltage stress albeit with added installed power of 6.7% due to a larger amount of current ripple processed.

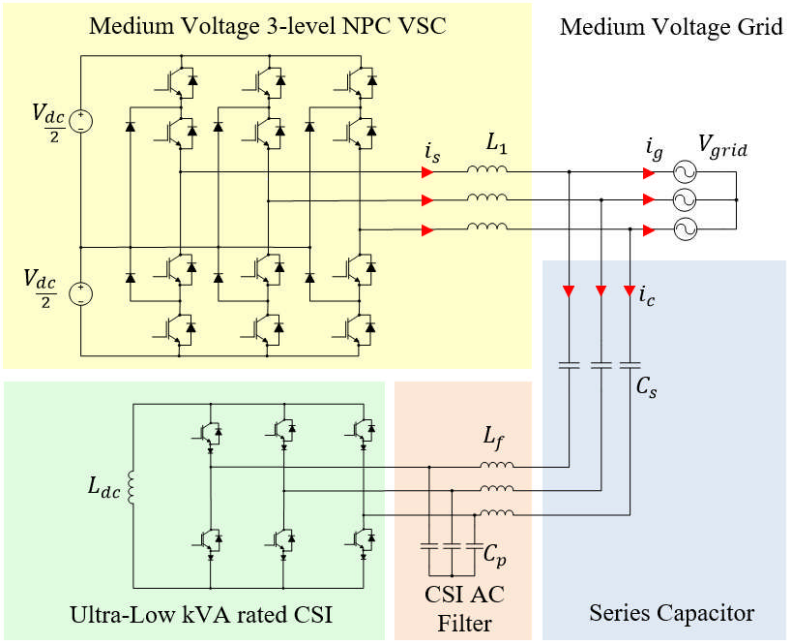


Fig. 1: Hybrid system topology highlighting the main features[1]

1. Introduction

Processing power efficiently via power electronic technology delivered to/from at medium and high voltage grids is predicted to increase in usage in the future, driven by the need to interface large off-shore wind farms to mainland grids or to interconnect distribution systems to HVDC transmission systems of the future. The first generation of commercial forced commutated HVDC systems favoured standard two-level inverters, built using series connected devices. The reasons were the simplicity and that it was straightforward to obtain redundancy by the addition of additional spare devices in the string; the downside was that sharing the voltage stress between the switches was difficult. Nowadays, commercial forced commutated IGBT devices with ratings of 3.3/4.5/6.5kV are widely available. This means it is much easier to build converters rated at medium voltage levels with less series connected devices. However, as the switching performance (J of loss/kVA switched) degrades more significantly with the increase of voltage rating (>3kV), it means that in order to preserve high efficiency, switching losses have to be kept to a minimum which means the switching frequency will remain a limiting factor

in the design of medium/high voltage power converters with reduced number of voltage levels and that the associated power quality will remain a problem. The reason is that the level of switching harmonics is high, characteristic for a 2-level PWM and that the switching frequency has to be kept low to preserve efficiency but the attenuation of an L/LCL filters is limited by the relative ratio of switching to cut-off frequency which is related to the fundamental frequency or one of the significant harmonic (5^{th}/7^{th})[2, 3].

To address these limitations, multilevel voltage inverter topologies [4-7] were proposed more than a decade ago. However due to the increase in complexity/cost their application was practically limited to a relatively low number of levels (three as is the case of the NPC inverter). The use of Selective Harmonic Elimination (SHE) in combination with the three level NPC enables for a better switching harmonic profile which results in a better LCL filter design for Medium voltage applications[8]. The Modular Multilevel Converter (MMC) proposed more recently [9] became very popular due to its suitability for mass production due to the use of identical building blocks, that could enable easy and cost effective implementation of custom systems. Achieving redundancy is also straightforward by inserting spare modules in the converter strings.

Another direction of research is represented by hybrid converter arrangements that aimed at enhancing the attenuation/behaviour of passive filters[10, 11] or to improve the waveform quality of slow/2-level converters by adding a faster auxiliary converters to provide active switching ripple cancelation (low current ratings) [8]-[9] whilst sharing the same DC-link (voltage stress). In [12], the idea of implementing an active filter that works at medium voltage by using a low voltage VSI connected in series with capacitors to block the 50Hz fundamental component was proposed. The use of series capacitors minimised the inverter voltage stress and the overall installed power/cost. The use of a series capacitor with a CSI has been investigated in [13-16] but for low voltage active power filter applications and in [17] for matching the voltage characteristic of photovoltaics with the AC grid voltage level and to maximize efficiency.

This paper is proposing and evaluating experimentally the performance of a hybrid converter solution, shown in Fig. 1 that consists of a slow switching medium to high voltage inverter whose switching harmonics are actively filtered by an auxiliary inverter having ultra-low installed power as a result of significantly lower voltage and current ratings compared to the main inverter. This can be a solution suitable also for retrofitting older implementations that cannot comply with newer power quality standards/limits. The auxiliary inverter is a Current Source Inverter (CSI) which is known to be capable of directly synthesising the AC current reference without the need of a current control loop, therefore requiring the lowest switching frequency and causing less switching losses. This aspect is very important as the reference current is the switching current ripple of the main inverter (hundreds Hz-few kHz). The use of a series capacitor to cancel most of the fundamental (50Hz) voltage enables the use of standard/fast switches with ratings up to 1.2kV in a medium voltage rated converter.

The novelty of this paper in relation to [13-16] is that it addresses applications where the main inverter is of a different voltage class and also that the installed power of the auxiliary inverter is further reduced by the series connected capacitors that block most of the fundamental (50Hz) AC voltage, similar to [18]. By using a CSI for the role of the auxiliary inverter as in [16], the circuit does not need the fast current controllers and the very fast switching that a VSI would need in an active filter application. The alternative to using a CSI would be to use an auxiliary VSI controlled by hysteresis current control. This is not straightforward as the reduced DC-link voltage of the auxiliary VSI in conjunction with a residually high level of grid impedance may limit the current ripple tracking capability (di/dt) and using capacitors to decouple this inductance may lead to resonances that can potentially be excited by the wide and uncontrolled harmonic profile of the hysteresis control.

Circuit Operation/Overview

The bulk power in the hybrid circuit topology is processed by a slow switching medium voltage three-level Neutral Point Clamped (NPC) VSC. The line side inductance L_1 is designed to limit the maximum switching current ripple as a percentage of the peak fundamental current. The Series Capacitor connected Active Power Filter consists of a three-phase two-level CSI with capacitor (C_s) designed to block the bulk of fundamental grid voltage. The second order low pass AC side filter necessary to smooth the output PWM CSI currents is formed by the combination of Capacitor C_p along with L_f and R_f (not shown). The primary role of the CSI is to provide active filtering on the switching current ripple produced by the VSC. In order to meet the minimal voltage stress requirement, a fundamental current is also injected through the series capacitors to enable control of the fundamental voltage sharing between the CSI and series capacitors while also ensuring DC-link current balancing.

The following section will provide a brief outline of the design considerations around the choice of series capacitor and choice of output filter and the dependence on the VSI design of a system connected to a 3.3kV MV grid as presented in [1]. Section 3 outlines the simulated performance before presenting the experimental results for a system scaled to a low voltage 415V grid validating system operation.

2. Design Procedure

The main VSC design is defined around the choice of output power which will define the maximum fundamental current amplitude for a grid voltage level. The current ripple produced by a three phase converter can vary depending on the topology and corresponding modulation strategy. The instantaneous amplitude will vary depending on the instantaneous modulation depth but with the resulting pattern over a fundamental cycle remaining identical. Similarly, as the maximum switching ripple amplitude is calculated based on the maximum duty cycle and DC link voltage level for a corresponding modulation strategy [2, 19, 20], the interface inductor L_1 is chosen to limit the maximum ripple to a percentage of the peak to peak fundamental current, in this case 20%. The amplitude of the maximum current ripple which needs to be cancelled by the CSI will subsequently define the maximum current CSI rating. The design specifications for a 1.9MVA system connected to a medium voltage grid (3.3kVrms line-to line) can be found in table one and the remaining design procedure focusing on the design of the CSI.

Table I: Specifications for simulated Hybrid Converter Medium Voltage Design

$V_{g\,L-L}$	I_g	$V_{g\,ph}$	S	ΔI_{max}	f_{sw}^{VSI}	f_{sw}^{CSI}
3.3 kVrms	330 Arms	2.7 kVpk	1.89 MVA	94A	1kHz	40kHz

2.1. Series Capacitor Design

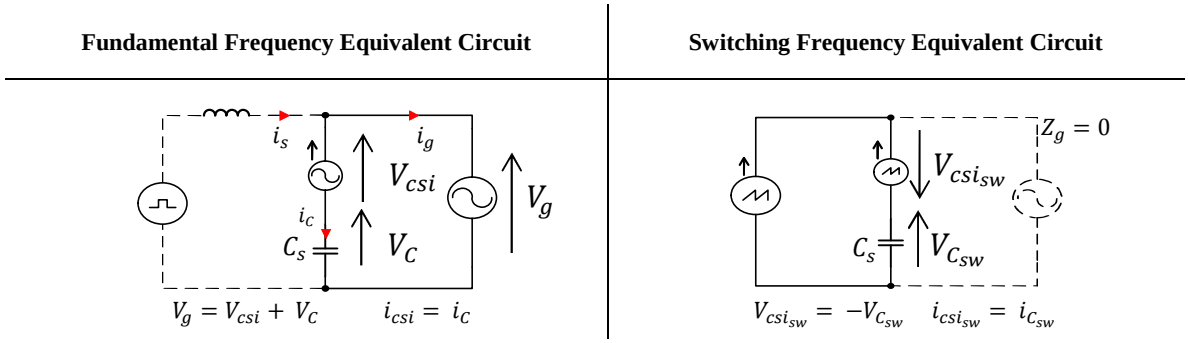


Fig 2: Hybrid Circuit Single Phase Equivalent at Fundamental and VSI Switching Frequency

The choice of series capacitance is perhaps the most critical aspect of the design procedure as it will define both the voltage and current rating of the CSI. The analytical design is done at the fundamental and VSI switching frequency with the single phase equivalent circuits shown in Fig 2 as the maximum

CSI voltage stress is created by the line-line fundamental and switching harmonics. At the fundamental frequency the grid voltage is shared between the CSI and series capacitor based on the injection of current I_c. The control approach is explained through the phasor diagrams shown in Fig 3. The objective is to minimise the CSI fundamental voltage drop to a fraction "K" of the grid voltage. This will result in a circular locus for the CSI voltage vector with radius K*Vg having as origin the tip of the grid voltage. This leads to a corresponding circular locus for the CSI current I_c phasor as shown in Fig 3a. (e.g. K=0.1 corresponds to a fundamental voltage reduction to 10%). Operation in region 2 would require a larger current amplitude for the same CSI voltage therefore operation should be limited to the quadrant shown as region 1. The synchronous reference frame dq components are outlined in fig 3b with the maximum and minimum current limits for I_c shown in Fig 3c and 3d.

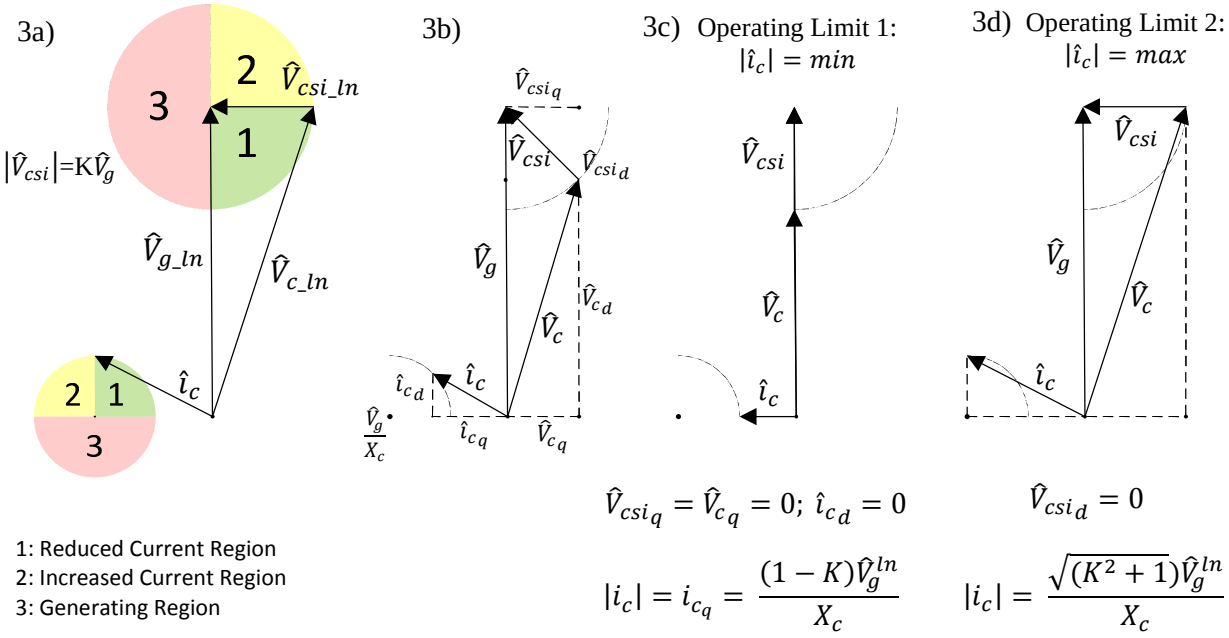
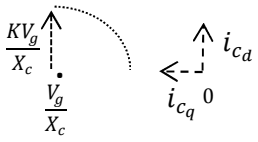


Fig. 3a-d: Fundamental frequency phasor diagrams and corresponding limits : a) operating quadrants for CSI fundamental voltage reduction ; b) *dq* decomposition of phasor quantities within the chosen operating quadrant; c) phasors and operating limits for lossless operation; c) phasors and operating limits at maximum current operation.



$$|i_{c_d}| \le \frac{KV_g}{X_c} \quad (1) \qquad i_{c_q} = \frac{V_g - \sqrt{(KV_g)^2 - (i_{c_d}X_c)^2}}{X_c} \quad (2)$$

Fig. 4: Current circle phasor and active current limit

The current circle limits are shown in Fig 4 reveal that for a given voltage reduction coefficient K, both the diameter and centre of the circle are scaled by the capacitance C_s. As a result, at the fundamental frequency the choice of a smaller capacitance is favoured due to the smaller current amplitude for a given voltage drop. The active current component Ic_d, used for the CSI DC link control, is limited to (1) while the reactive component(2) is used to control the CSI voltage drop within the operating quadrant.

Under the assumption of negligible grid impedance the switching harmonics are equally shared between the CSI and Series Capacitance with the amplitude inversely proportional to the capacitance (3) therefore favouring a larger capacitance for harmonic voltage reduction. The choice of series capacitor is therefore a compromise between ensuring a limited harmonic voltage drop and maintaining a low fundamental current demand. By limiting the maximum switching voltage ripple to be produced by a given current ripple in I_c the minimum capacitance can be chosen (4) while the maximum capacitance is given by limiting the reactive power absorbed by the capacitor(5) which is correlated to the reactive current amplitude.

$$V_{csi_{sw}}^{ln} = |i_{sw}|X_c = \frac{|i_{sw}|}{\omega_{sw}C_s} = -V_{c_{sw}}^{ln} \quad (3) \qquad C_{s_{min}} = \frac{|i_{sw}|}{\omega_{sw}|V_{c_{sw}}|} \quad (4) \qquad C_{s_{max}} = \left(\frac{Q}{S}\right)\frac{\sqrt{3}i_s^{RMS}}{V_g^{RMS}\omega} \quad (5)$$

For the design shown in table 1 and the reactive power limited to 20% the maximum capacitance is calculated at 110µF. The maximum voltage stress has been chosen as 20% of the line grid voltage with an equal share of fundamental and maximum switching voltage stress. The minimum capacitance has been calculated at 55µF.

$$\frac{i_{c_s\,fund}}{i_{c_p\,fund}} = \frac{|V_{c_{max}}|C_s}{|V_{csi_{max}}|C_p} \quad (6) \qquad G = 1 + \frac{C_p}{C_s} \quad (7)$$

2.2. CSI AC Filter Design

The CSI output filter design is restricted by the need to have a parallel decoupling capacitor C_p which has to be as small as possible to limit the bleeding of the main harmonic cancelation current based on the ratio to capacitor Cs (6) but needs to be large enough to provide sufficient smoothing of the PWM ripple generated by the CSI. The filter inductance L_f is subsequently chosen based on imposing a suitable cut-off frequency, ideally less than half of the CSI switching frequency, to give sufficient attenuation of the PWM ripple. The damping resistance R_f connected in parallel to Lf is selected to provide sufficient damping at the filter resonant frequency. This was chosen to achieve lower losses as well as negligible phase shift within the bandwidth of interest (up to 5 kHz). The calculated design parameters are summarised in table II.

Table II: Component Parameters and Settings for the Desired Operating Point used in Simulations

C_s min	C_s max	L_f	R_f	L_{dc}
55µF	110µF	23µH	10Ω	20mH
C_p	K	I_c max @55/110 µF	I_d lim @55/110 µF	I_{dc} @55/110 µF
11µF	0.1	47A/94A	4.66A/9.32A	140/184

3. Medium Voltage Hybrid System Performance Evaluation

The simulated performance of the circuit has been evaluated for the maximum series capacitance limit of 110µF.

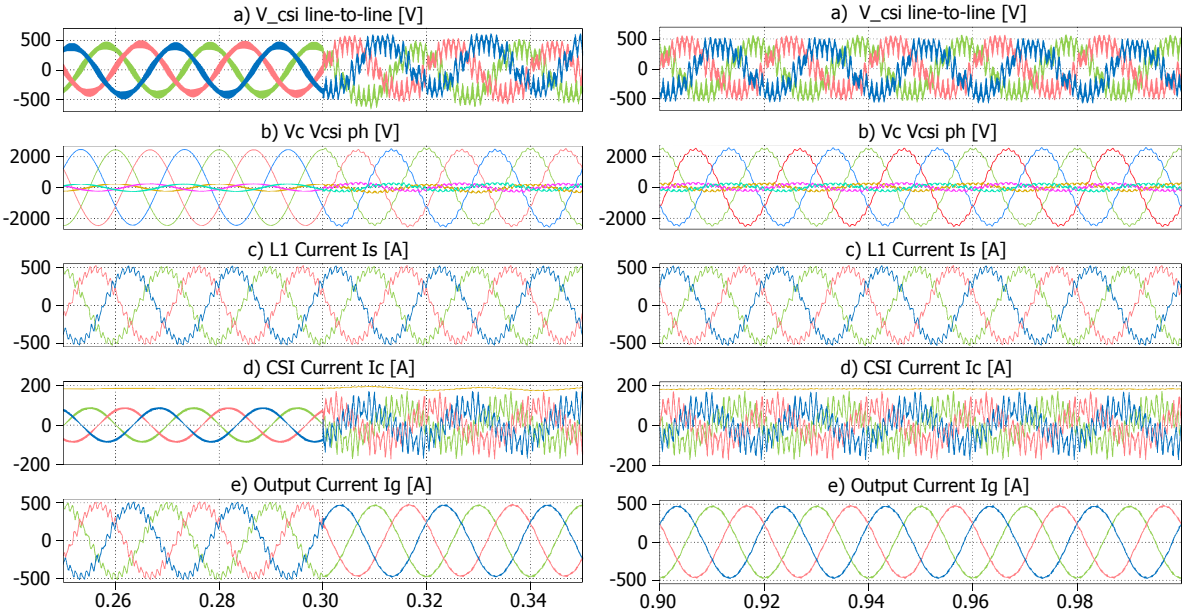


Fig. 5: Simulated waveforms showing transition to ripple cancellation (left) and steady state operation (right) for a) CSI Voltages(line to line); b) Series capacitor and CSI Voltages(phase); c) Input (Main Converter) Current (Is) d) CSI Current (Ic) and DC link current; e) Output Grid Current (Ig)

As shown in Table 2 the larger series capacitance choice benefits from lower switching harmonic voltage drop however requires a higher DC current amplitude of 184A compared to 140A due to the larger fundamental current that needs to be synthesised by the CSI to keep constant the fundamental voltage drop across the series capacitor. The set of waveforms on the left column of figure 5 demonstrates the hybrid system operation when the auxiliary inverter operates with a fundamental voltage drop coefficient K=0.1. The corresponding reduced CSI voltage stress is visible (480Vpk line-line) before switching ripple cancellation is activated (t=0.3s) and the phase CSI and series capacitor voltages are plotted together to clearly show the proportion of reduction. The transition to ripple cancellation is reflected by the absence of ripple in the output Ig currents but it results in a very small disturbance in CSI voltages and CSI DC-link current. Whilst performing switching ripple cancellation, the CSI voltage stress increases to 580Vpk (line-to-line) by the addition of the voltage drop across the series capacitors caused by the CSI current (current anti-ripple) passing, well below the 20% limit of 940V.

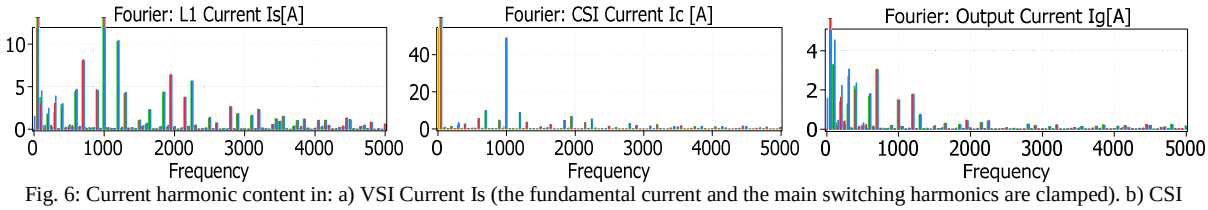


Fig. 6: Current harmonic content in: a) VSI Current Is (the fundamental current and the main switching harmonics are clamped). b) CSI Current Ic and C) Output grid current Ig (fundamental component clamped);

The harmonic content of the main VSI current, the CSI and grid current for harmonics up to 5 kHz is shown in Fig. 6. A comparison of the VSI and grid current harmonic contents shows a slight reduction of low order harmonics (3rd, 5th) while all switching current harmonics are reduced to less than 4.7A (1% of the fundamental current) with negligible harmonic amplitudes beyond 5 kHz. The main switching harmonic at 1 kHz is reduced to 3% (48A to 1.5A). The current THD up to the 100th harmonic has been reduced from 11% (VSI only) to 1.8% reflecting the output current quality increase. The hybrid system semiconductor loss has been estimated in simulation using the Infineon FF400R33KF2C 3.3kV/400A (up to 660A) IGBTs for the VSI and Semikron SEMiX202GB12E4s 1.2 kV/200 for the CSI. The total semiconductor losses have been estimated at 1.1% of the output power with 5.6kW accounting for the CSI losses and 14.5kW accounting for the VSI. The added installed power of the CSI based on the maximum voltage and current stress has been calculated at 3.7%.

3.1. Experimental Validation

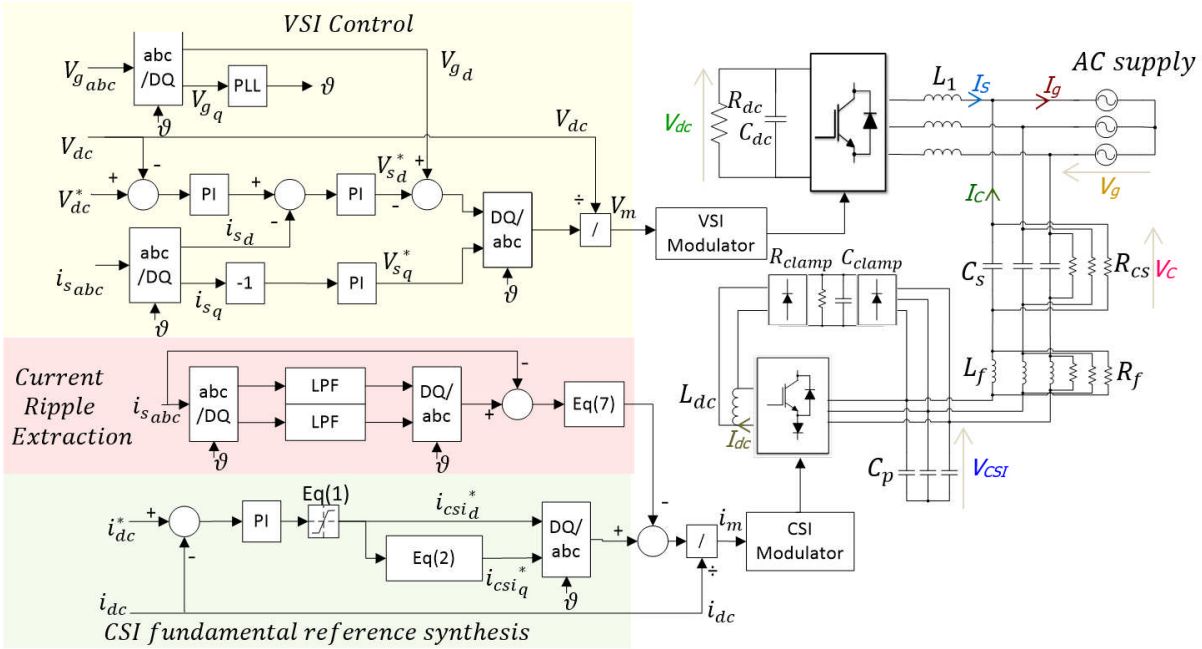


Fig 7: Circuit topology and control system of experimental setup. Oscilloscope measurements are shown in corresponding colours

The experimental validation of the hybrid system has been conducted on a three phase 415Vrms (line-to-line) grid. In order to evaluate the full extent of the ripple cancellation potential of the hybrid solution, a three phase electronic AC power supply (12kVA Chroma 61705) has been used, that emulates the best a stiff grid with negligible impedance, albeit with the limitation of unidirectional power flow.
All experimental results are therefore acquired having the VSI operating in rectifier mode with a resistor connected as a DC-link load as shown in Fig 7. The VSI active current component is determined by the DC voltage controller reference while the reactive reference is set to zero. The cross coupling terms that are typically used to cancel the voltage drops caused by a given axis current in the orthogonal axis voltage have been omitted in this implementation due to the undesirable effect of injecting large noise when operating with large current ripple. It is expected that the steady state d/q current errors will be compensated anyway by the PI current controllers. The option of the VSI compensating for the reactive current component associated with the series capacitor to achieve unity power factor could be easily implemented by feeding the corresponding series capacitor current as a negative q reference component to the VSI controller, a solution proposed also in [1]. This solution is also common for compensating the reactive currents produced by the capacitance required in an LCL filter with low cut-off frequency. This was not considered here as the motivation for this evaluation was to consider that the VSI operates independently.

In order to extract the VSI switching ripple with negligible phase shift, the filtered fundamental component is subtracted from the three phase VSI currents. This is done by transforming Is(a,b,c) into the dq synchronous reference frame where a second order low pass filter (LPF), attenuates any switching harmonics, with the remaining dc components reconstructed as the abc filtered fundamental VSI current components. The extracted ripple is multiplied by the gain given in Eq 7 to compensate for the effect of the current escaping from the circuit via Cp (6). A clamp circuit is connected on both the DC and AC sides of the CSI to provide overvoltage protection and enable monitoring of the CSI voltage stress as it will be shown later. The component values and operating conditions are summarised in Table 3.

Table III: Operating settings and component parameters for the experimental topology

R_{dc}	C_{dc}	L_1	L_f	L_{dc}	K	R_f	R_{clamp}	R_{cs}	C_{clamp}
140Ω	550μF	11mH	300μH	30mH	10%	50Ω	100kΩ	100kΩ	20μH
P	V_{dc}	V_{grid}	Is	Idc	C_s	C_p	f_o	f_{sw}^{VSI}	f_{sw}^{CSI}
4.2kW	750V	415V_{rms}	8Apk	5A	12μF	1μF	50 Hz	1 kHz	40 kHz

Results are captured in key transient moments to provide a thorough inspection of system operation.
Fig 8 shows the VSI and CSI voltages and currents during system start-up and CSI voltage drop coefficient K=0.1 before ripple cancellation. Before PWM activation the VSI is operating as a diode rectifier non-linear load, therefore accounting for the grid and VSI current shape, drawing a measured 2kW of power to the DC load resistor with the VSI DC-link voltage at 536V. Due to a very low current absorbed by the CSI filter capacitors (CSI disabled), the grid voltage can be seen mostly on the CSI inputs with only around 8% seen across the series capacitor reflecting the inverse proportion of the capacitance values (1/12).

Upon activation of the hybrid converter, the VSI DC-link voltage ramps up to the 750V reference value with the DC load power dissipation increasing to approximately 4.2kW. The CSI DC-link current overshoots to 7A before settling at the reference value of 5A with the fundamental AC current production remaining unaffected by the controller overshoot.

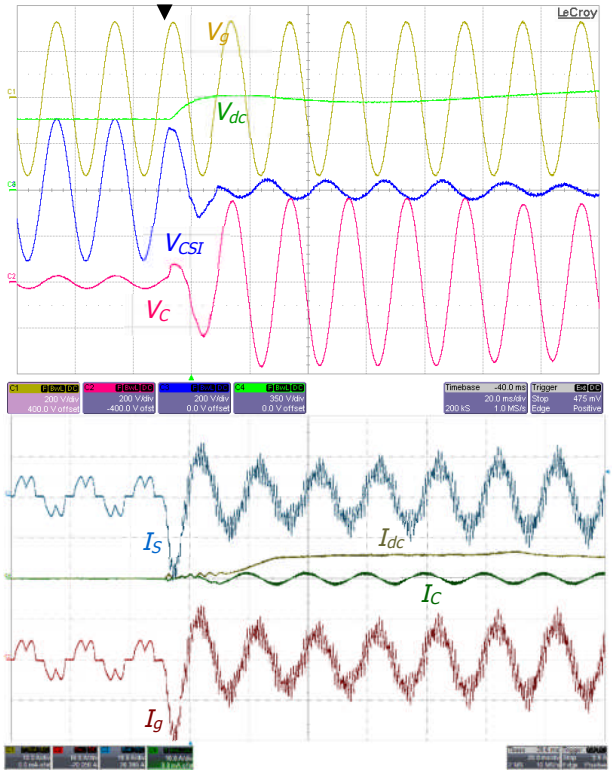


Fig 8: Transient showing the simultaneous activation of the VSI and CSI where only CSI voltage drop control is active (K=0.1).

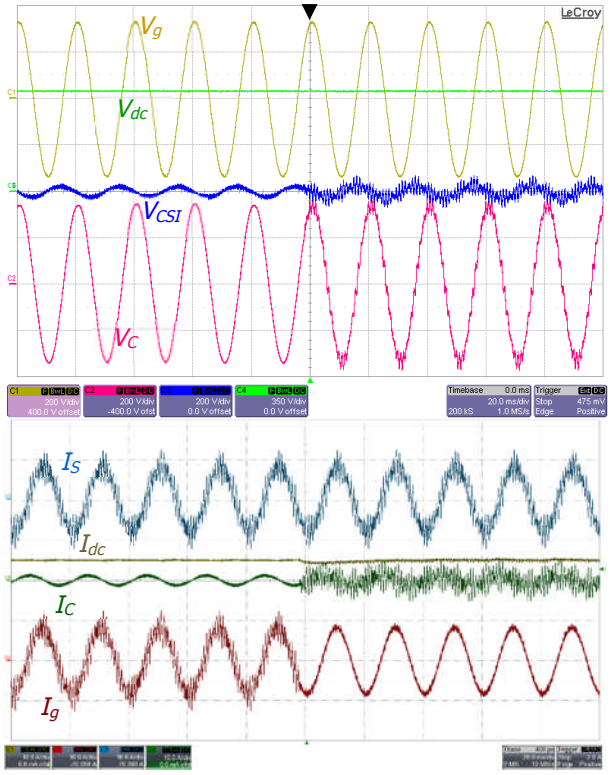


Fig 9: Transient showing the activation of the VSI ripple cancellation (the CSI operates with a fundamental voltage drop of K=0.1)

The activation of the CSI causes an immediate reduction of the CSI voltage which eventually settles at 34Vpeak matching the expected theoretical value of 10% of grid voltage (340V peak phase).The activation of ripple cancellation, shown in Fig 9, results in a significant improvement of the output current quality and with a very small transient visible on the CSI DC-link current while the VSI DC-link voltage remains unaffected. The voltage drop caused by the switching current ripple as it passes through the series capacitors is mirrored on the CSI inputs, as the main AC bus voltage has zero impedance for the switching ripple.

The relevant voltage waveforms of the hybrid system operating in steady state with switching ripple cancellation enabled is shown in Fig 10 where the peak CSI voltage is recorded at 68V, accounting for both the 50Hz and switching ripple) compared to 34V before cancellation (only 50Hz component), amounting to a peak CSI voltage stress of 20%, which is identical to the analytical design requirements. The RMS CSI voltage is at 11% (26.5V) of the grid voltage (235.7V) showing an even more significant reduction, but this doesn't have a direct impact in the auxiliary inverter design.

Fig 10 shows the FFT of the CSI voltage for harmonics up to 5 kHz, taken over a 1second time period. The fundamental component voltage component is the largest with a measured peak of 27V while the voltages at the main switching harmonics are 17V at 900 Hz and 14.5V at 1.1 kHz, whilst the remaining harmonics at negligible levels.

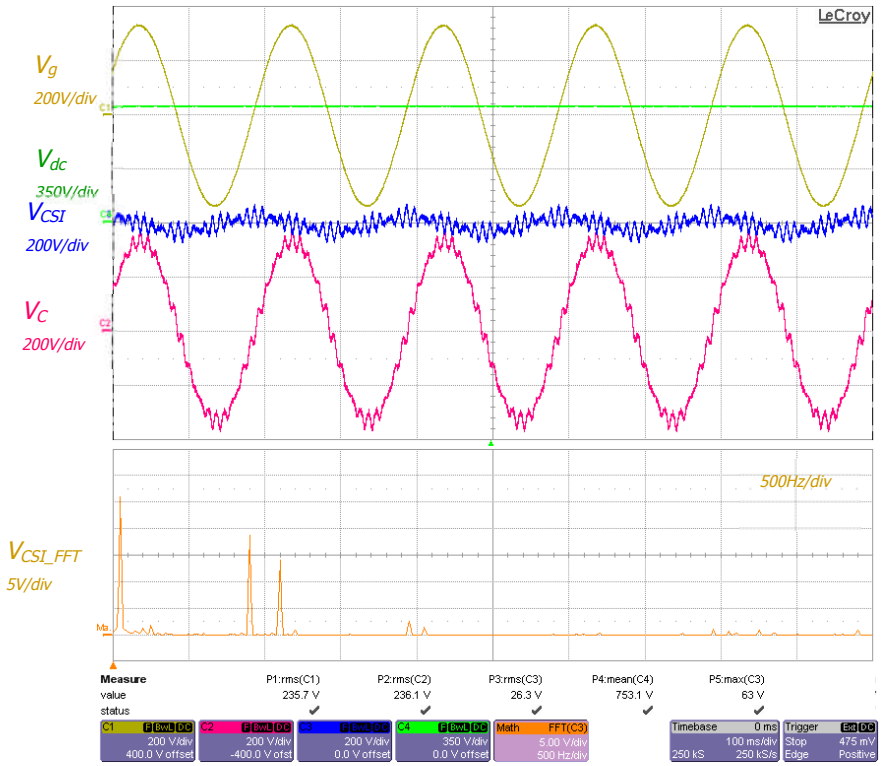


Fig 10: Steady state performance of hybrid converter showing phase A: AC grid voltage Vg, VSI DC link voltage Vdc, CSI voltage Vcsi and series capacitor voltage Vc as well as FFT of CSI voltage.

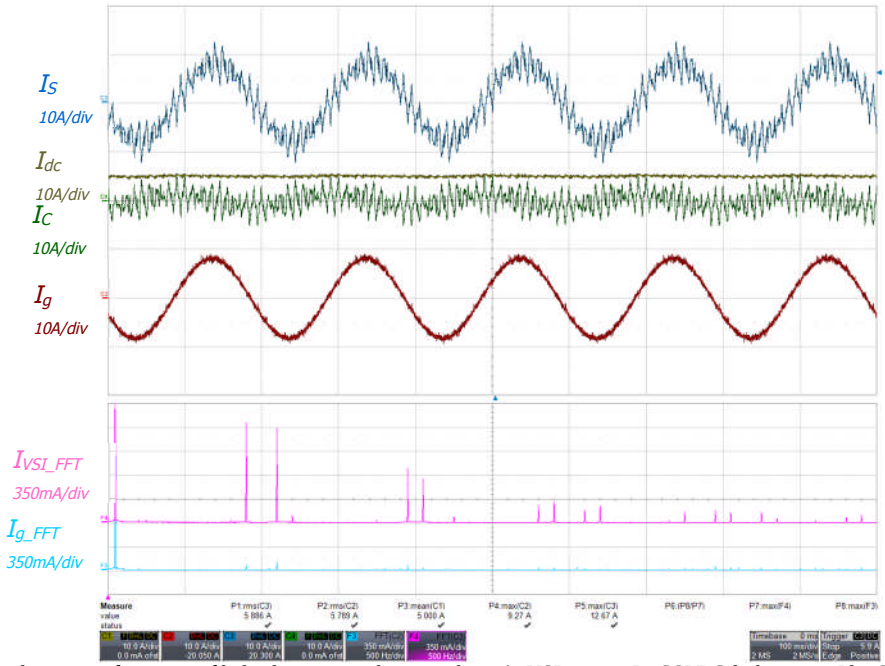


Fig 11: Steady state performance of hybrid converter showing phase A: VSI current Is, CSI DC-link current Idc, CSI AC current Ic and cumulated grid current Ig as well as FFT for VSI and grid current harmonic content

The current waveforms of the hybrid system operating in steady state are shown in Fig 11. The peak of the VSI fundamental current component is around 8A. The highest peak current is recorded at 12.25A which means the maximum current ripple is 4.2Apk. Compared to the peak of the fundamental component, the ripple is at 50% of the peak output current which is significantly higher than the specified 20% in the initial design. The use of a significantly higher switching ripple allows for a better demonstration of the harmonic cancellation capability and is representative for the operation of the system at reduced load, as switching ripple tends to remain independent on loading for same DC-link voltage. During cancellation the DC-link current is kept at a level as close as possible compared to the

peak ripple with the mean value matching the 5A reference value. The resulting grid current shape is very close to a pure sinusoidal waveform with the CSI switching ripple at 40 kHz being the main visible disturbance. Due to waveform clean-up, the grid current peak is reduced to 9A compared to 12.25A.

The effectiveness of the ripple cancellation can be assessed in more detail in the frequency domain where the FFT of the VSI and grid current are shown for frequencies up to 5 kHz. The highest harmonic at 900Hz is reduced from 1.46A to 93mA (6.5% of original harmonic level), the 1.1kHz harmonic is reduced to 7.6% of the original harmonic (105mA compared to 1.375A), 1950Hz harmonic to 8.4% (0.8A to 67mA) and the 2050 Hz harmonic is reduced to 5%(0.63A to 34mA). The fundamental component is measured at 7.67A on the VSI current compared to 7.89A on the grid current with the difference accounting for the power going towards the CSI(mostly reactive).

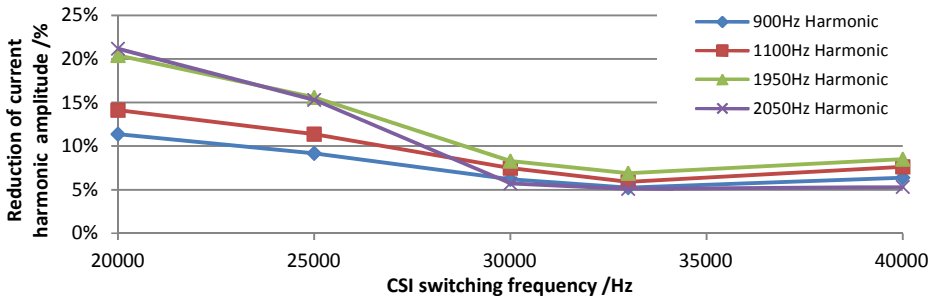


Figure 12: Percentage reduction of main current harmonics over a range of CSI switching frequencies

The effectiveness of the current harmonic cancellation over a range of CSI switching frequencies (20/ 25/ 30/ 33/40kHz) is presented in Fig 12 as a percentage reduction for each of the four main harmonics. As expected, The VSI switching ripple reduction is worse at 20 kHz with the most significant sidebands (900Hz and 1.1 kHz) reduced to 11% and 14% whilst the second set of sidebands (1950Hz and 2050Hz) is reduced to 21% revealing a limited effectiveness of the ripple cancellation bandwidth at frequencies less than 10 times the switching. This is verified by the steady improvement in harmonic reduction for the second set of sidebands as the CSI switching frequency is increased; with an additional 5% reduction observed at 25 kHz. For switching frequencies of 30 kHz or higher all harmonics are reduced to less than 10% with values ranging from 5% to 8%.

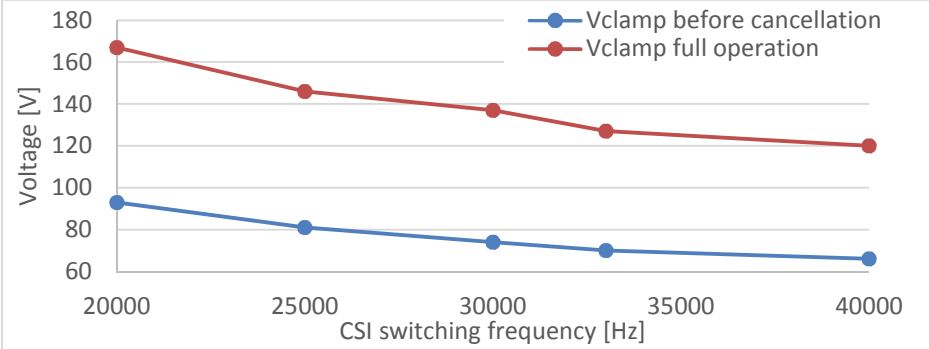


Fig. 13: Voltage clamp DC reading reflecting the maximum CSI voltage stress over a range of CSI switching frequencies before current ripple cancellation and during full system operation

Fig 13 shows the DC clamp voltage, which directly reflects the maximum CSI voltage stress over the range of CSI switching frequencies with the levels recorded before and after the switching ripple cancellation has been activated. The clamp voltage curve before ripple cancellation shows that the voltage stress of the CSI increases as the CSI switching frequency decreases which can be explained by the stronger interactions/resonances with the CSI LC filter at lower switching frequencies which was actually designed for the CSI switching at 40 kHz. At higher switching frequencies, the CSI clamp voltage seems to converge towards a level consistent with the 10% of the peak of the supply line-to-line voltage.

During full harmonic cancelation operation, the CSI voltage stress reflected in the clamp voltage increases due to the added voltage drop caused by the harmonic currents passing through the series capacitors and reflected at the CSI input. The minimum voltage stress during full system operation at 40kHz is recorded at 120V which is consistent with the design target of 20% of the peak of the supply line to line voltage while the highest voltage stress recorded at 20kHz is at 166V.

The peak VSI voltage stress, given by the peak DC voltage has been recorded at 760V, while the peak current ripple has been recorded at 12.5A. For operation at 40 kHz the maximum CSI current stress, given by the peak DC-link current ripple has been recorded at 5.3A with the maximum voltage stress given by the peak line-line voltage (or DC clamp voltage) at 120V. As a result the added installed power at 40 kHz is calculated at 6.7% which increases to 9.5% for 20 kHz switching frequency.

The experimental procedure as shown in figures 8 and 9 has been repeated for different CSI switching frequencies with measurements logged at one second intervals using a power analyser (N4L PPA 5530). The power analyser enables the measurement of the efficiency by recording the power in (two wattmeter method) as well as the calculated grid current total harmonic distortion (THD) up to the 100th harmonic. Non-lineal load behaviour can be observed in the following waveforms up to approximately t=30s where PWM is enabled, and full system operation is enabled at t=90s.

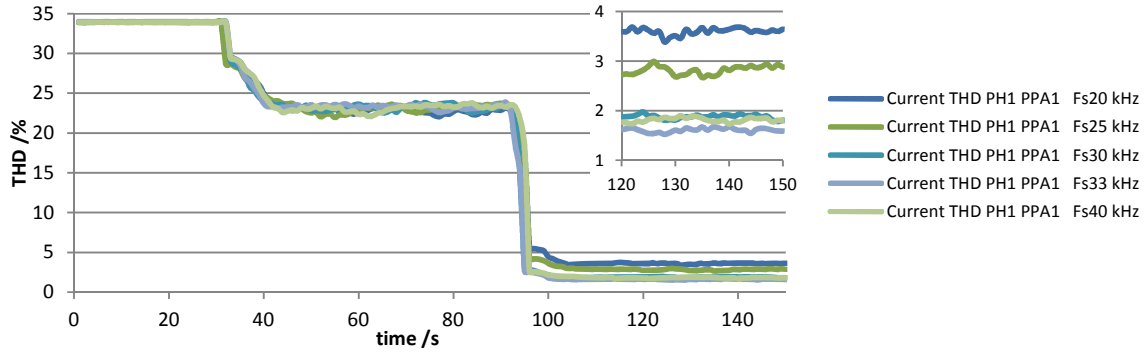


Fig 14: Power analyser grid current THD data for hybrid system operation before PWM (0 to 30s), PWM prior to ripple cancellation (30 to 90s) and during ripple cancellation with zoom in on low THD values during ripple cancellation period for different CSI switching frequencies.

The grid current THD is reduced from 33% during non-linear load operation to around 23% when PWM is enabled; with some reasonable fluctuation observed between waveforms. The effect of ripple cancellation is apparent by the immediate further reduction of the THD during full hybrid system operation for all CSI switching frequencies. At 20 kHz the value is around 3.5% with a slight improvement to less than 3% for 25 kHz and below 2% THD for all other frequencies. It can be noticed that the average THD per switching frequency reflects the reduction as measured in Fig 12.

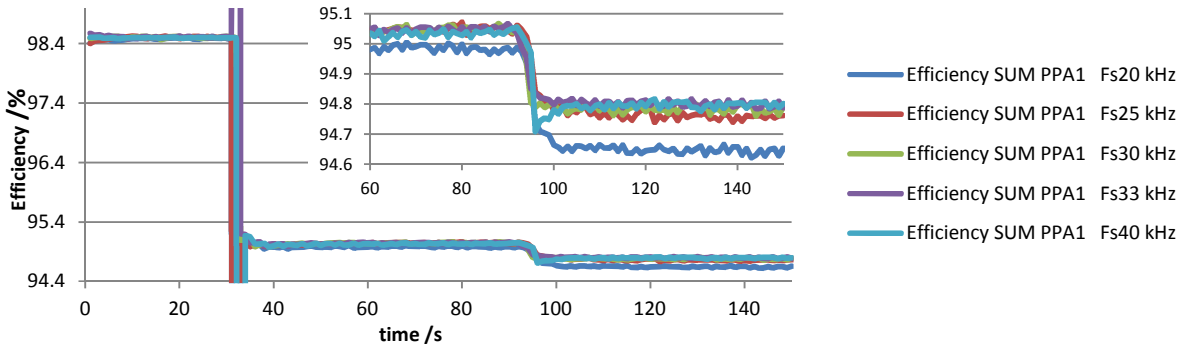


Figure 15: Power analyser efficiency data for hybrid system operation before PWM (0 to 30s), PWM prior to ripple cancellation (30 to 90s) and during cancellation for different CSI switching frequencies. Zoom in (top right) showing effect of enabling ripple cancellation.

The recorded efficiency reveals negligible effects of the CSI switching frequency under all modes of operation shown in Fig 15. A small deviation at 20 kHz could be caused by the additional voltage CSI stress due to the reduced AC side filter attenuation but is considered negligible (less than 5W). During full hybrid system operation the efficiency, including the passive losses of the system, remains around 94.8% compared to 96% for VSI standalone operation (not shown above) where the CSI and associated passives have been physically disconnected from the point of common coupling.

In comparison, the displacement power factor has been reduced from 1.0 for standalone VSI operation to 0.989 showing an insignificant impact of the series capacitor on the overall reactive power. Considering that the current evaluation is operating with a much larger ripple processed by the CSI with respect to the VSI fundamental current, it is expected that the impact on displacement power factor will be smaller with a lower relative VSI current ripple. The hybrid system setup is depicted in Fig 16 showing the VSI and the auxiliary CSI with all associated components including Series Capacitor, output AC filter and DC-link inductor.

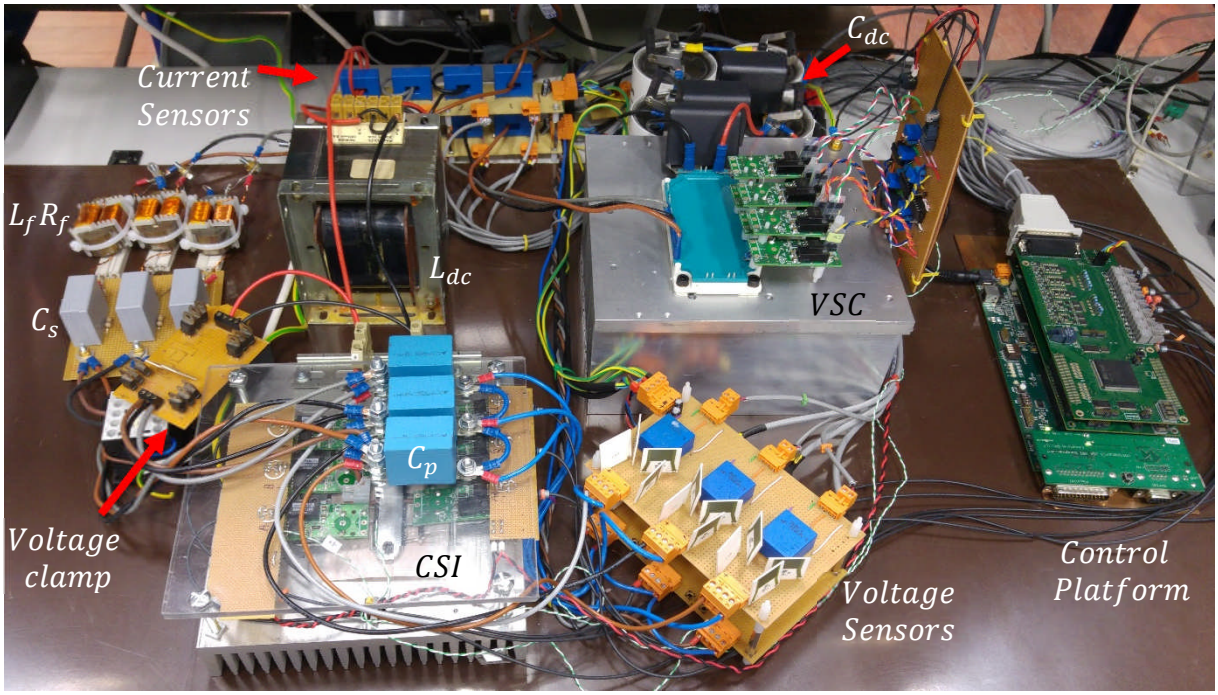


Fig 16: Picture showing experimental setup of hybrid system and associated components

It can be concluded that the overall experimental system performance is very similar to the simulated performance when connected to a stiff grid. It is also proven that the analytical design procedure to define the choice of series capacitor and the scaling of CSI and output filter has indeed yielded the expected performance targets. Under steady state operation the peak CSI voltage stress is at 20% of the grid voltage peak with the overall system benefitting from very low grid current distortion verified by the harmonic performance evaluation over a range of CSI switching frequencies. The CSI is shown to have a small effect on the overall losses and output power factor. The added installed power of the CSI compared to the main VSI which considers the peak voltage and current stresses and the number of switches is calculated at 6.7% with the increase from the 4% theoretical value accounting for the additional CSI loading.

Conclusion

This paper proposed and experimentally evaluated a hybrid power conversion solution consisting of a slow switching main inverter interconnected with an ultralow kVA rated CSI acting as an Active Power Filter to remove its switching current harmonics, which in this approach can be significantly larger (50% ripple was considered) than typically specified in the design of the filtering inductor. Series connected capacitors ensure that the fundamental voltage component seen by the CSI and the associated voltage stress are significantly reduced. A design procedure based on the interdependency between the main inverter switching current ripple, the desired fundamental voltage/current CSI stresses and the size of the series capacitance is proposed and validated by simulation and experimental results. The capability to provide high level of switching ripple attenuation (reduction to 5-8% of the original ripple level) with low installed power in the auxiliary CSI is proved by both simulation and experimental validation of a prototype scaled at typical grid voltage and power ratings. The only drawbacks noticed are the increase of converter losses and a slight decrease in the displacement power factor, both of which would also happen in case a higher order passive filter (LCL) would be used to provide more reasonable levels of current ripple. It can be concluded that the proposed hybrid solution provides an interesting extra performance vs extra cost trade-off.

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