Study of built-in amplifier performance on HV-CMOS sensor for the ATLAS Phase-II Strip Tracker Upgrade

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Abstract

This paper focuses on the performance of analog readout electronics (built-in amplifier) integrated on the high-voltage (HV) CMOS silicon sensor chip, as

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well as its radiation hardness. Since the total collected charge from minimum ionizing particle (MIP) for the CMOS sensor is ten times lower than for a conventional planar sensor, it is crucial to integrate a low noise built-in amplifier on the sensor chip to improve the signal to noise ratio of the system. As part of the investigation for the ATLAS strip detector upgrade, a test chip that comprises several pixel arrays with different geometry, as well as standalone built-in amplifiers and built-in amplifiers in pixel arrays has been fabricated in a 0.35 μm high-voltage CMOS process. Measurements of the gain and the noise of both the standalone amplifiers and built-in amplifiers in pixel arrays were performed before and after gamma radiation of up to 60 Mrad. Of special interest is the variation of the noise as a function of the sensor capacitance. We optimized the configuration of the amplifier for a fast rise time to adapt to the LHC bunch crossing period of 25 ns, and measured the timing characteristics including jitter. Our results indicate an adequate amplifier performance for monolithic structures used in HV-CMOS technology. The results have been incorporated in the next submission of a large-structure chip.

Keywords: HVCMOS, Silicon Strips, ATLAS phase-II upgrade

1. Introduction to ATLAS phase-II upgrade

The next major upgrade phase of the Large Hadron Collider (LHC) is currently foreseen to be completed in 2024 [1]. It is called the High Luminosity-LHC (HL-LHC), and it aims to increase the integrated luminosity to about ten times the original LHC design luminosity, resulting in an additional integrated luminosity of around 2500 fb^{-1}over ten years. These data will improve the precision of the measurement of the Higgs properties and enhance the sensitivity to search for new physics.

Silicon micro-strip sensors in the upgraded ATLAS experiment at the HL-LHC will be exposed to particle fluences of up to 2×10^{15} $n_{\mathrm{eq}}/\mathrm{cm}^2$ [2]. Another challenge in HL-LHC operation is that the number of pile-up interactions per crossing will increase to 140, which is about ten times larger than for the current LHC. The existing ATLAS inner detector (ID) cannot maintain the tracking performance due to this huge increase in the channel occupancy. Therefore, a completely new ATLAS inner tracker is needed for the HL-LHC data taking. The sensors need to be designed with finer granularity than the existing tracker to meet the challenges of very high pile-up

and to be able to reconstruct tracks in the core of multi-TeV jets.

2. Introduction to CMOS based silicon sensor

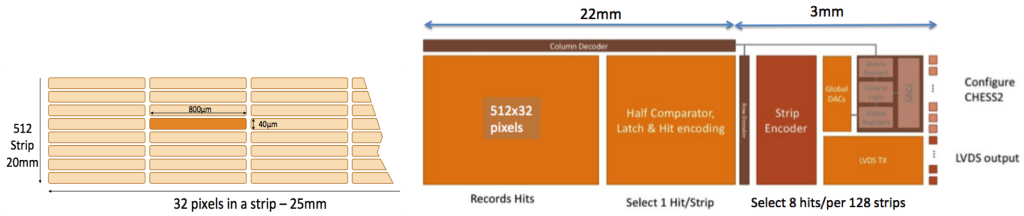
CMOS sensors can combine both silicon sensors and readout processing circuitry on one single CMOS-chip, which will significantly simplify the process of detector module building. CMOS sensors can provide high granularity, and the pitch of the strip sensor can be reduced to below 50 μm. Due to small feature size, this technology has the potential to be radiation hard. The cost of CMOS sensor fabrication has the potential to be significantly less compared to conventional planar sensors. Furthermore, CMOS-based sensors collect charge from a thin depleted region so the sensor can be thinned down to 50 μm to reduce material. The major drawback of the CMOS-based sensor is that it has a ten times lower total collected charge from a MIP than the conventional planar sensor. It is crucial to integrate a low noise built-in amplifier on the sensor chip to improve the signal to noise ratio of the system.

3. Designing strip sensor with CMOS active pixel array

In ATLAS Run1, the strip detector consists of double sided modules, where a pair of conventional planar sensors are back-to-back with 40 mrad stereo angle for the second coordinate measurement.

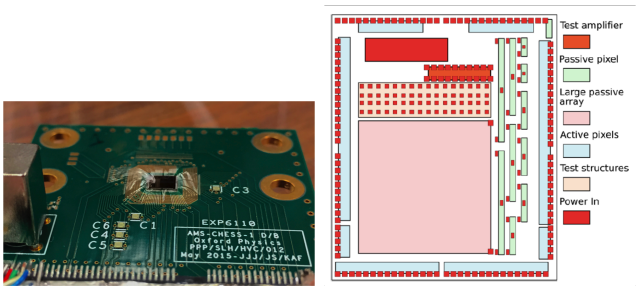
In order to use CMOS technology to build a strip sensor for the ATLAS upgrade, the basic design will be very different compared to the Run 1 detector. A full-size CMOS sensor is being designed for the ATLAS strip upgrade as shown in Fig. 1 (a). It is a single-sided sensor, which consists of 512 strips. Each strip has 32 segments that can provide the second coordinate measurement. Each segment is an active pixel with analog frontend (including built-in amplifier) and comparators.

The digital encoding is performed at the periphery of the CMOS chip. There is a hit encoding structure manages hits on each strip. Its purpose is to perform a sequential scan across the 32 segments of a strip and record the segment that was hit. Strip encoding can select up to 8 hits per 128 strips at 320 MHz per 25 ns bunch crossing. Preliminary physics simulation study shows that this readout architecture can meet the occupancy specifications for a strip detector for ATLAS Phase II physics.



(a) (b)

Figure 1: (a) The preliminary design of pixel array for full-size strip sensor (b) The preliminary design of CMOS strip sensor chip with pixel arrays and periphery.



(a) (b)

Figure 2: (a) A photo of HV-CHESS1 test chip (b) The layout of HV-CHESS1 test chip.

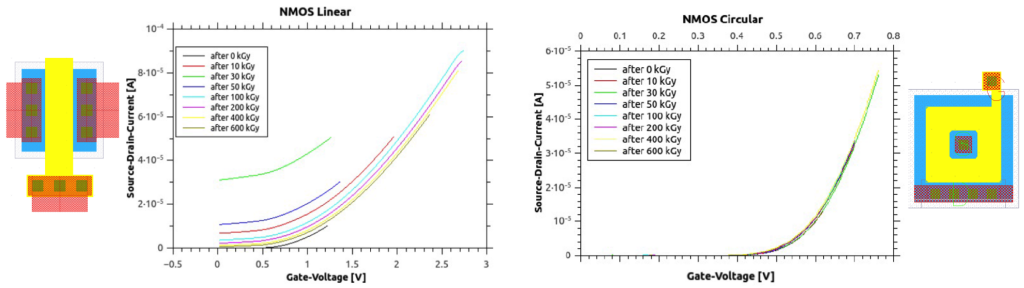
4. CMOS test chips

Two test chips have been fabricated in a AMS 0.35 μm high-voltage CMOS (HV-CMOS) process. The test chip HVStrip1 contains NMOS and PMOS transistors, a passive diode, and a 22x2 array of diode pixel sensors with active components implemented on the sensors. It can be used for a variety of active pixel characterizations.

Another test chip HV-CHESS1 contains several pixel matrices with different geometry, as well as built-in amplifier and stand-alone amplifier arrays. It permits pixel geometry optimization and characterization of a standalone built-in amplifier. A photo of HV-CHESS1 is shown in Fig. 2 (a), and the layout of HV-CHESS1 is shown in Fig. 2 (b).

5. Transistor performance in HV-CMOS chips

During the HL-LHC lifetime, the ATLAS strip detectors are expected to receive a dose of no more than 600 kGy of ionizing radiation. To understand



(a) (b)

Figure 3: (a)The source-drain current in NMOS transistors of HVStrip1 chip as a function of gate voltage after gamma irradiation for (a) a linear layout transistor, (b) a circular layout transistor. The layout of a linear layout transistor and a circular layout transistor are also shown, and the gate in the yellow layer of the layout figure.

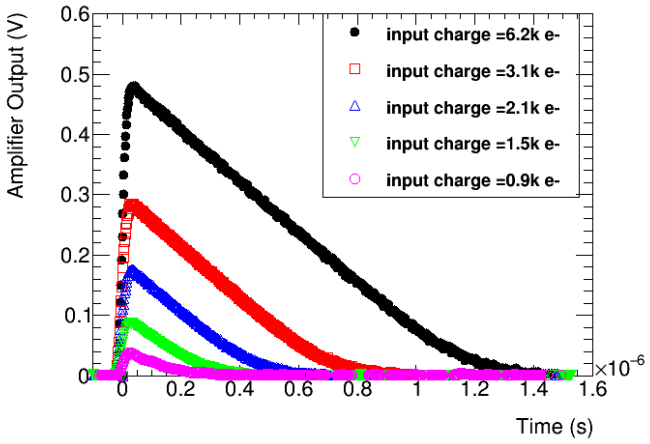
the radiation hardness of the electronics on CMOS chips, two type of NMOS transistor on HVStrip1 chip, as shown in Fig. 3, have been designed . The first one is a conventional linear transistor, while the other is designed in a circular (or enclosed) configuration which is expected to be radiation hard.

To test the radidation hardness, HVstrip1 chips were exposed to X-rays with a most probable energy of 35 keV [3]. Fig. 3 shows that source-drain current in NMOS transistors of HVStrip1 chip as a function of gate voltage after different doses of X-rays gamma irradiation. The source-drain current of NMOS transistor with linear layout increased significantly after gamma irradiation. This behavior is consistent with competing effects of oxide charge generation and the activation of interface traps [4]. At the same time, the circular layout NMOS transistors are not sensitive to gamma irradiation up to 600 kGy, which meets the radiation hardness requirements of the ATLAS phase II strip detector. Measurements of other devices on the HVStrip1 chip have been reported in Ref. [6, 7].

6. Built-in amplifier performance in HV-CMOS chips

A low noise built-in amplifier is used in the active pixel arrays in the HV-CHESS1 chip. The original design of amplifier is from Ivan Peric [5]. There are many configurable biases, including the bias in source followers (InSF) and feedback current (iFB).

In order to characterize the performance of this built-in amplifier, we use an external pulser to inject a fast signal on the amplifier input through a



(a)

Figure 4: The amplifier output pulse shape with fast pulses from external pulser as input.

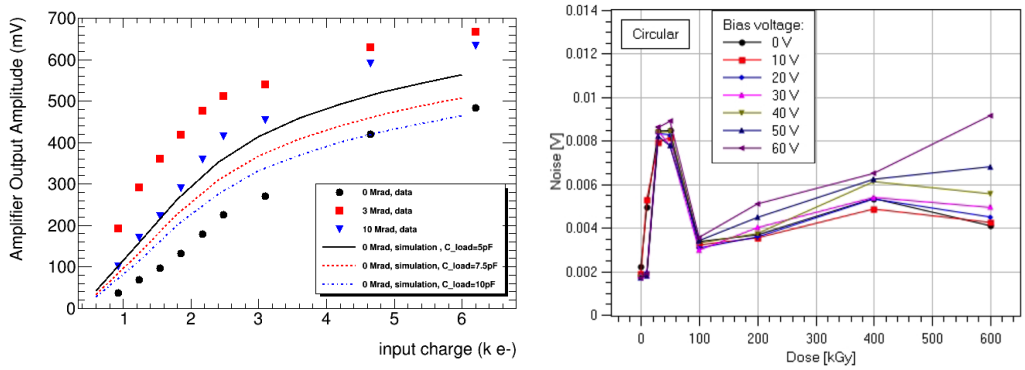
built-in calibration capacitor (50 fF). The amplifier output pulse shape for different input signals is shown in Fig. 4.

Based on the amplifier output pulse shape, the response curve of this standalone built-in amplifier is characterized and shown in Fig. 5 (a). Total collected charge from a MIP in a HV-CMOS sensor is more than 1500 e^-. According to the response curve, the gain of this built-in amplifier is about 1000 mV/fC at 1500 e^- input charge before irradiation. The measured gain agrees reasonablely well with the results from simulations. The gain increased to 1900 mV/fC at 1500 e^- input charge after 3 Mrad gamma irradiation.

The radiation hardness study in HVStrip1 chip shows that the noise also increased with gamma irradiation dose as shown in Fig. 5 (b).

Combining two results in Fig. 5, the signal-to-noise ratio for a MIP signal in HV-CMOS sensor would have been above 50 if one could neglect the influence of the in pixel n-well capacitance.

The configuration of the amplifier is optimized for a fast rise time to adapt to the LHC bunch crossing period of 25 ns. The timing performance of the standalone built-in amplifier on HV-CHESS1 chip is also characterized using an external pulser. The measured signal rise time is shown in Fig. 6 (d). According to Fig. 6, the timing jitter using different thresholds on amplifier output as a function of input charge is evaluated and shown in Fig. 6 (a). The time walk effect is evaluated by comparing the time stamp of the signal



(a) (b)

Figure 5: (a) Response curve of a standalone built-in amplifier on HV-CHESS1 chip. Due to uncertainty on capacitance load (C_{load}), three response curve predicted by simulations with different C_{load} are also provided. (b) The noise level of a standalone built-in amplifier on HVStrip1 chip as a function of gamma irradiation dose.

crossing threshold for different amounts of input charge. The uncertainty due to time walk effect is stable within ±5ns as shown in Fig. 6 (b). The uncertainty due to time walk and jitter is significantly less than the LHC bunch crossing time (25 ns). In order to evaluate the dead time of each pixel, pulse width using different threshold on amplifier output as a function of input charge is also evaluated and shown in Fig 6 (c). A typical dead time for 1500 e^- input charge is less than 400 ns. Since there are 32 pixels in one strip in a full-size CMOS sensor, the effective dead time for a strip is 12.5 ns.

7. Active pixel response to Sr^{90} electrons

The active pixel performance in HV-CHESS1 chip is evaluated by exposure to beta radiation from Sr^{90}. The energy spectrum from the beta decay of Sr^{90} is a continuum up to its end point energy of 2.2 MeV. A scintillator was placed below the chip to select high energy minimum ionizing electrons. A typical pulse shape of active pixel response to Sr^{90} electrons is shown in Fig 7. The noise in an active pixel output is slightly higher than an isolated built-in amplifier due to the influence of the in pixel n-well capacitance. The signal-to-noise ratio for MIP signal in active pixel is still sufficient. The performance of passive pixels after irradiation is described in Ref. [8, 9];

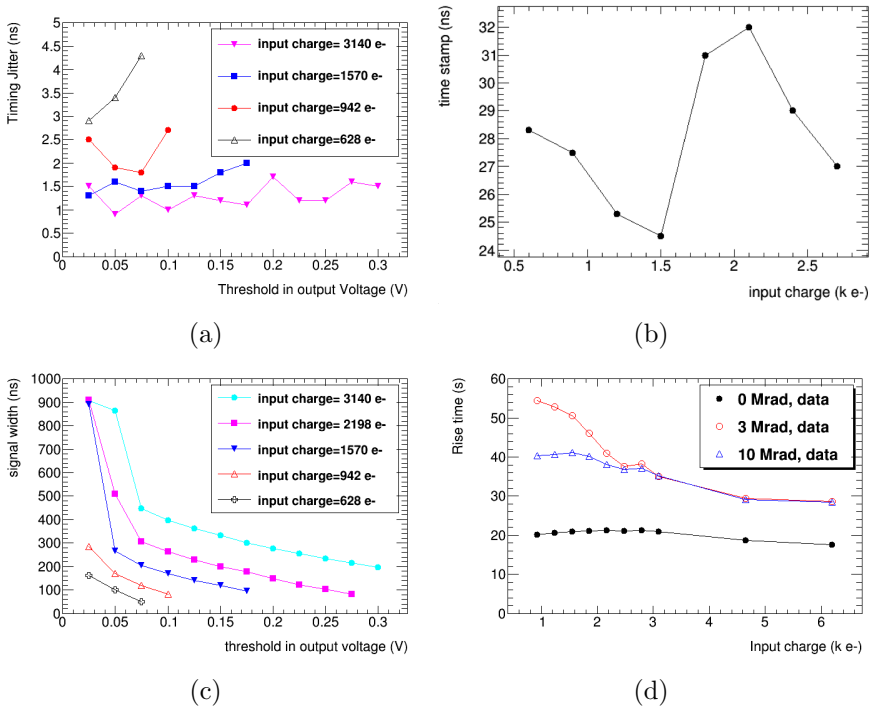


Figure 6: (a)The timing jitter using different threshold on amplifier output as a function of input charge (b) The time walk at various amount of input charge (c) Pulse width using different threshold on amplifier output as a function of input charge. (d) Signal rise time

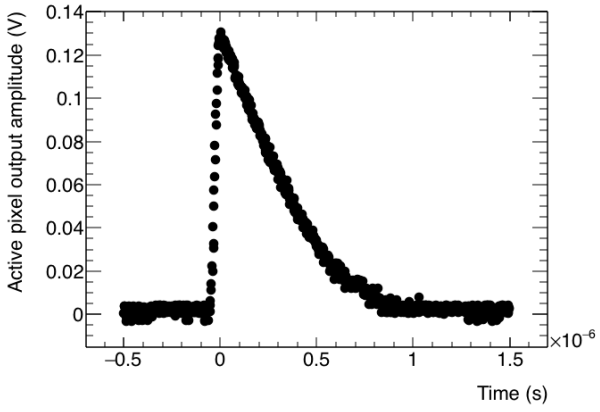


Figure 7: (a) A typical pulse shape of active pixel response to Sr^{90} electrons. The pixel size is 45 μm × 800 μm.

8. Summary

The HV-CMOS sensor technology is being developed as an alternative solution for ATLAS Phase II strip detector upgrade. To withstand the much harsher radiation in HL-LHC, two prototypes of radiation hard CMOS test chips (HVStrip1 and HVCHESS1) have been fabricated using the AMS H35 process .

The circular layout transistors are tested, and the results verify their radiation hardness, fulfilling the requirements of HL-LHC operations.

The standalone built-in amplifier in the CMOS test chips has been characterized. The uncertainty due to timing jitter and time walk effect is about 5 ns level, which is within a single LHC bunch crossing resolution (25 ns). The gain of the built-in amplifier is verified to be sufficient to readout small signal (1500 e^-), which is the lower limit of MIP signal from active pixel.

A prototype of a full-size strip sensor with fully digital readout is being developed. It will be fabricated in the next few months, and the readout architecture will be tested next year.

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[1] R. D. Heuer, EPS-ECFA meeting, Stockholm, July 2013.

[2] ATLAS Collaboration, CERN-2012-022, LHCC-1-023 (2013).

[3] See the public web page *http* : *//www.ekp.kit.edu/english/*265.*php*

[4] I. Peric, Ph.D. Thesis, Bonn University Physics Institute, (2004) *https* : *//cds.cern.ch/record/*1334577

[5] I. Peric, Nucl. Inst. and Meth A 582 (2007) 876-885

[6] I. Peric, et al. 2015 JINST 10 C05021.

[7] F. Ehrler, R. Blanco, R. Leys, and I. Peric, Nucl. Inst. and Meth A 650 (2011) 158

[8] V. Fadeyev et al, "Investigation of HV/HR-CMOS Technology for the ATLAS Phase-II Strip Tracker Upgrade", Hiroshima 2015 proceedings

[9] B.T. Huffman et al, "Radiation hardness of two CMOS MAPS prototypes for the ALTAS HL-LHC upgrade project", TWEPP 2015 proceedings