# CAMAC

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ISSUE No. 13 September 1975



#### PREPARATION OF CONTRIBUTIONS

Authors are requested to follow these instructions when submitting contributions for the Bulletin. Failure to do so may result in contributions being returned to the author for re-submission in a modified form, and may delay publication.

- English is the preferred language. Contributions in other languages are equally welcome but only the summary will be translated.
- Authors should state their name, business affiliation and postal address on a separate sheet if not included in the contribution.
- 3. The style, layout, use of bibliographic references and so on should follow as closely as possible the appropriate contents of this Bulletin.
- 4. For contributions to the New Products Section, each product description should be on a separate sheet and any one description must not exceed 250 words or 1/3 Bulletin-page, including illustrations.
- For contributed articles, 1 200-1 600 words are preferred. They must not exceed 2 000 words or 3 Bulletin-pages, including illustrations. They

- should be accompanied by a summary (abstract) suitable for translation into other languages and preferably not exceeding 50 words.
- 6. Manuscripts should be typed on alternate lines on only one side of the page.
- 7. Drawings and photographs should be included if they are relevant to the text. Original ink (not pencil) drawings and semi-mat prints of photographs, at least twice the final size, should be submitted. The author's name and the figure number should be written, lightly, in pencil on the back of each illustration. A list of all figure numbers and captions should be included on a separate sheet, even if these are given in the text or on the illustrations themselves.
- 8. Articles which are shortened, or adapted from, original papers should identify the original in the references.
- Authors must submit contributions before the closing dates announced elsewhere in this Bulletin.
- 10. Reprints can be ordered at any time, but authors who are likely to require reprints in bulk should request these when submitting a contribution.

#### PRINCIPAL CONTENTS OF THE PREVIOUS CAMAC BULLETIN ISSUE

ISSUE No. 12 INTRODUCTION TO CAMAC

April 1975

1. The CAMAC Serial Highway — a Functional View. D.L. Abbott.

#### APPLICATION NOTES

- A CAMAC Application in the Quality Control of High Temperature Reactor Fuel. W. Attwenger, F. F. Buschbeck.
- 2. A CAMAC-Based Laboratory Computer System. G.P. Westphal.
- 3. Ground Replay Equipment for the Alpha Jet Crash-Recorder. B. Müller, K. Rosenblatt.

#### DEVELOPMENT ACTIVITIES

- 1. CAMAC Modules for Angular Shaft-Position Measurement. F.A. Joerger, D.W. Zobrist.
- 2. A CAMAC Branch Driver for the PDP-8/E Computer. M. Nadachowski, J. Bundgaard.
- 3. A CAMAC Serial Driver-Receiver. G. Messing. J. Stolte, E. Kwakkel.
- 4. CAMAC Modules for Industrial Analog Measurement Equipment. J. Biri, L. Somlai, Gy. Somogyi.
- 5. A Fast Multi-Event Time Digitiser. J.P. Argyle, P.E. Dolley, G. Huxtable.
- 6. X-Interrupt CAMAC Module for Use with Borer 1533 Crate Controller. I. Török.

#### SOFTWARE

- 1. CAMAC Extension for BASIC 2/3 on the ALPHA-LSI Computer. J.L. Visschers, A. ten Hertog.
- 2. CAMAC Software-Driver for Real-Time System RSX-11D on the PDP-11/40 or 11/45. H. Heer, H. Pohl.

#### CONTRIBUTIONS TO FUTURE ISSUES

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News and New Products of Manufacturers:

Product Guide (Hardware, Software):

News:

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On the cover: Air view of the Centre of Warsaw. The Annual General Assembly of the ESONE Committee and a CAMAC Exhibition took place in the Hotel Forum in Warsaw, in September 1974.

### CAMAC

#### bulletin

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#### **CONTENTS OF ISSUE No. 13**

APPLICATION NOTES	
<ol> <li>An Optimized Architecture for a Multichannel Pulse Height Analyser</li> </ol>	
R. M. Keyser, R. H. Baldry	3
J. Lecoq, H. Tedjini, P. L. Wendel, G. Metzger	6
H. Mayer	9
DEVELOPMENT ACTIVITIES	
1. An Interface between CAMAC and the Digico Micro-16V Com-	
puter H. D. Blake, D. J. Folwell  2. An Alpha-Numeric and Graphical Display Driver in CAMAC	11
N.V. Toy	13
3. CAMAC Interface for a Buffered Card Reader K. van Dellen, F. Sporrel, L. M. Taff	14
4. CAMAC Interface Module for the Biomation Transient Recorder Type 8100  I. Török	16
SOFTWARE	
<ol> <li>MACRO-IML Implementations for the PDP-11 Computer M. Kubitz, R. Kind</li> </ol>	17
<ol> <li>CAMAC with FORTRAN on a CDC 3100 — An Approach Based on IML</li> </ol>	
W. Kneis, W. Karbstein	18
IDEAS AND TECHNIQUES	
1. Faster Address-Scan by Reading Only Non-Zero Data	21
<ul><li>E. V. Chernykh, J.I. Chmielewski, V. A. Smirnov</li><li>2. A. Rarely-Used Application of the X-Line</li></ul>	21
L. Stanchi, I. Török	22
ESONE-NIM SECTION	
ACTIVITIES OF THE CAMAC WORKING GROUPS	23
NEWS	23
HOW TO CONTACT CAMAC WORKING GROUPS MEMBERSHIP OF THE ESONE COMMITTEE	24 25
ESONE ORGANIZATION AND CAMAC ACTIVITIES	26
NEWS	
Conferences and Seminars 2, 5, 8, 10, 12, X	LIV
CAMAC Applications	
Announcements by CAMAC Manufacturers	LIV
NEW PRODUCTS	27
Index to CAMAC Manufacturer's News and New Products	36
PRODUCT GUIDE	
Hardware Products	II
Index to CAMAC Manufacturers (Hardware)	
PAPER ABSTRACTS TRANSLATIONS	37
PREPARATION OF CONTRIBUTIONS Cov	er 2

CAMAC BIBLIOGRAPHY . . . . . . . . . . . . . . . . . Cover 3 FEES FOR SUBSCRIPTIONS AND REPRINTS . . . . . . . Cover 4

### **NEWS**

### EUROPEAN CAMAC ASSOCIATION CAMAC SURVEY 1974

This survey of the use of CAMAC in 1974 has continued to steadily acquire data and, at June 1st, 104 respondents had supplied details about 295 systems applications on returned CAMAC SURVEY 1974 proforma. An interim analysis of this data will be supplied to these respondents only, and to encourage other CAMAC Users/Suppliers to respond, the following is one aspect of the analysis.

The total value of CAMAC equipment in the 295 systems was \$7.4M equivalent and was distributed in the following fields of application in order of rank:

Physics, Medicine, Space/Astronomy, Instrument Engineering, Fission, Engineering, Fusion, Environment, Chemistry, Energy, Product processing, Education, Public Utilities.

Of the total systems, 33% were unlikely to be expanded in the next 2 years, however for the 48% that were definitely scheduled for expansion their expansion in CAMAC equipment would be by 36%, on average, the highest expansion being in Engineering applications (automatic testing, avionics, automotive, mining).

Anyone requiring a Survey Form should contact Mr. H. Bisby, AERE Harwell, OX11 ORA, England (Telex: 83135) who is acquiring the database under conditions of strict confidentiality.

#### CAMAC IN STRESA

The 2nd Ispra Nuclear Electronics Symposium took place on May 20–23, 1975 in Stresa. Some 250 participants were present. Among the many interesting sessions a whole one was devoted to CAMAC and including 17 papers on quite different topics.

The first paper, an invited one, 'Applications and Development of CAMAC in North America' by D.A. Mack and L.J. Wagner, LBL, Berkeley, U.S.A., gave a broad review of recent CAMAC applications in this area. It demonstrated a great

interest in CAMAC serial systems. The mentioning of a serial system including optical transmission by means of laser light attracted special attention.

Several papers treated the use of microcomputers in connection with CAMAC. Speakers from both CEN, Saclay, and JRC, Ispra, presented papers on autonomous crate controllers using the INTEL 8080 microprocessor.

At the accompanying exhibition several CAMAC manufacturers showed their products.

#### 1975 NUCLEAR SCIENCE SYMPOSIUM

The 1975 NUCLEAR SCIENCE SYMPOSIUM, to be held in San Francisco, November 19–21, 1975, at the Sheraton Palace Hotel, has recently issued a Call for Papers. The symposium will feature papers on recent developments in nuclear detectors, circuits, instrumentation systems, novel applications in experimental and space physics including CAMAC and computer systems, energy conversion, nuclear medicine, environmental measurements, and reactor instrumentation. Program Chairman is Dick A. Mack, Lawrence Berkeley Laboratory, University of California at Berkeley. The conference,

which will run concurrently with the 1975 Nuclear Power Systems Symposium, will feature invited Plenary Sessions on important current issues in nuclear science, invited technical papers, panel discussions, as well as concurrent poster sessions. Detailed program information can be obtained by calling or writing:

R. Hamman — Publicity Chairman NSS Stanford Linear Accelerator Center P.O. Box 4349 Stanford, California 94305, USA.

#### CAMAC COURSES AT HARWELL

The next, and 16th two-day course on CAMAC at the Harwell Education and Training Centre will be held on 21–22 October 1975. It is intended for users of CAMAC, rather than for equipment designers, and deals with the CAMAC specifications covering all the aspects of the Dataway, Parallel Branch and Serial Highways and IML. The lecturing panel contains, among others, Messers H. Bisby, R.C.M. Barnes, I.N. Hooton and A. Lewis and the possi-

bilities are being explored of this course being run in conjunction with the activities of the UK CAMAC Association.

The course fee is £40, (exclusive of VAT and accomodation), and application forms are obtainable through the Education and Training Centre, AERE Harwell, Oxfordshire OX11 OQJ Telex 83135. Early application is advisable because attendance at the course is restricted to 30 places.

### **APPLICATION NOTES**



### AN OPTIMIZED ARCHITECTURE FOR A MULTICHANNEL PULSE HEIGHT ANALYSER

by

R. M. Keyser and R. H. Baldry

ORTEC Incorporated, Oak Ridge, Tennessee, USA Received in revised form, 13th January 1975

SUMMARY The architecture of multichannel analysers (MCA) has progressed from hardwired analysers to computer-based analysers. An architecture for the next generation MCA is based on a computer with CAMAC and a high-level interactive language.

The multichannel pulse-height analyzer (MCA) has been recognized as a valuable tool in many scientific disciplines during its relatively brief existence. Beginning as a group of single channel analyzers and counters that responded to adjacent and sequential amplitude ranges, it has been developed into a hardwired MCA with simplified controls such as the system shown in Fig. 1. The

Display CRT

Display Control

Hardcopy
Controller

Front Panel

ADC Control

Typewriter

Plotter
Punch

SCA

ADC

Fig. 1 Block Diagram of Modern MCA

input amplitude is measured by an ADC to select a memory channel for each pulse, and storage is conditioned by Single Channel Analyzer (SCA)

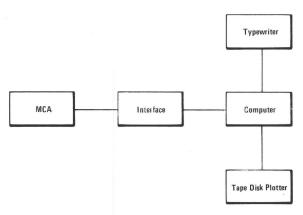


Fig. 2 Block Diagram of a Computerized MCA

recognition. Modifications of the original concept expanded the memory size and provided multidetector storage and multiparameter operation for newer techniques.

Recording and storage capabilities limited advancement until minicomputers were interfaced with MCAs, and they also provided some on-line analysis using the system of Fig. 2. This trend has now led to the next generation which is the computer-based MCA shown in Fig. 3. Advantages of the new

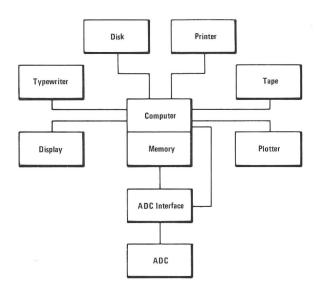


Fig. 3 Block Diagram of Computer-based MCA

system include ease of reconfiguration, output flexibility, more adequate displays, and easy expansion. The disadvantage is that the central processing unit and memory must be shared in time for storage, display, and data manipulation.

#### AN OPTIMUM ARCHITECTURE

With the advantages and disadvantages of these systems in mind, we have developed an architecture for a computer-based MCA system that attempts to retain the advantages of both the computer-based MCA and the hardwired MCA. Achievement of this goal required the following:

- high-performance (low dead time) data acquisition in several modes from more than one data source;
- flexible data manipulation between data storage areas, displays, and other peripherals;
- convenient operating conditions from a useroriented control panel;
- powerful computation facilities for on-line/off-line data reduction;

- flexibility of hardware configuration to match the experimenter's needs and his pocket; allowance for expansion;
- powerful but convenient program generation capability to match the overall system performance and flexibility.

The first step in this development was to divide the tasks associated with an MCA into those done best or fastest by hardware and those done best by software.

The hardware tasks consisted of:

- storing ADC data in a memory dedicated to that task:
- monitoring overflows, error conditions, and regions of interest in the data;
- transforming computer code into characters, vectors, and logarithms for display;
- encoding the control panel functions to minimize software decoding time;
- storing or refreshing the current display image.

The software tasks involve:

- generating display data, titles, and scale factors;
- manipulating data, transfer to other modes, etc;
- controlling the MCA by responding to encoded control-panel functions and executing the requested function;
- supplying on-line reduction of data;
- controlling data and program storage peripherals.

A block diagram of this system appears in Fig. 4. Parallel to the development of the architecture an operating system was developed to communicate with the user through the typewriter keyboard and control panel. Because this operating system has other applications it must have the following characteristics:

- support a high-level FORTRAN-like language;
- support any mixture of computer hardware including CAMAC;
- be able to respond to CAMAC interrupts by executing high-level language routines.

The architecture shown in Fig. 4 has been implemented with CAMAC modules, a PDP-11/05® computer, a removable-media disk, a storage-display

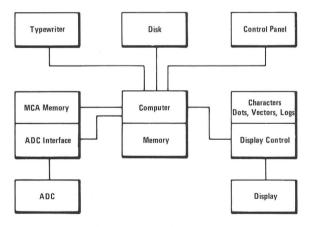


Fig. 4 Block Diagram of Hybrid Architecture

® Trademark registered by Digital Equipment Corporation.

unit, and the language/operating system ORACL®; see Fig. 5.

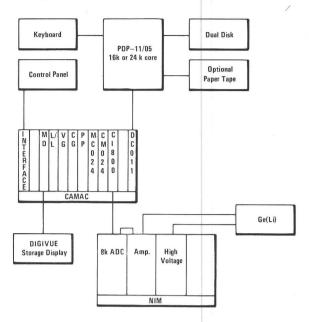


Fig. 5 Module Diagram of Fig. 4

#### THE SYSTEM AND ITS IMPLEMENTATION

The advantages of the system developed at ORTEC are many:

- The high data rate of a hardwired analyzer is achieved. The CAMAC-based ADC interface contains a live-time correction circuit so that proper dead times are accounted for.
- The addition of extra detectors does not affect system dead time. Other detectors can be added by simply adding the ADC, ADC controller, and CAMAC memory.
- The display functions are fast and the display itself can be quite complex with text, axes, and data shown, without flicker or distortion.
- Disks, magnetic tapes, paper tapes, plotters, etc., are readily available and easy to add in both software and hardware.
- The control of experimental parameters such as counting time, position of stepping motors, detector voltage, and others is easily achieved with standard CAMAC modules and high-level control subroutines.
- Other parameters, not usually recorded, can easily be entered via CAMAC modules.
- System checkout, maintenance, and downtime are significantly reduced by the combination of modular hardware and the high-level control language.

#### System Features

The avantages cited above are achieved by using the following system features:

- ORACL, which was developed by ORTEC for the purpose of creating interactive data collection systems, allows the user to communicate with CAMAC modules in a high-level FORTRAN-like language. The system also responds to CAMAC
  - ® Trademark registered by ORTEC, Incorporated.

LAMs (flags) and allows the user to create (in high-level language) the program to be executed when the LAM occurs.

- The memory used for data acquisition is separate from the program and computation memory of the PDP-11/05; in addition the ADC-to-memory data path is not time-shared with the CAMAC or computer buses. Once initialized and enabled, the ADC and the memory will acquire data independently of the system until a preset condition is met or a command to stop is received. The system generally accesses this memory only for display or data transfer (for computation or input/output); these functions are all performed infrequently. The modularity of this section readily permits expansion of one data channel or expansion to multiple data channels.
- The use of a storage type of display means that rapid refreshing of the screen image does not have to be used to maintain a high quality flicker-free display of large amounts of data and/or text. Nor are a display-refresh memory (or D/A channel) and associated hardware necessary for constraining the display image. A storage display reduces time loading of the CPU and memory bus, as the image is usually updated no more than three times per second during data acquisition and at intervals of seconds during analysis. Activity of these units is limited to the few milliseconds required to update the data display.

The aesthetic and technical limitations of a conventional bistable-storage cathode-ray tube are overcome by using a DIGIVUE® gasplasma storage display. This new device allows:

- permanent image retention without degradation;
- long life time;
- fast total-erase (0.5 millisecond);
- selective write or erase of any of 512 by 512 points on the screen;
- no image drift or distortion.

The system control panel contains a variable-sized matrix of pushbuttons interfaced to a CAMAC module. When pressed, each button generates a unique binary code and a LAM. The system responds to the LAM and executes the ORACL program associated with that button. This allows the user to specify exactly what each button should do.

® Trademark registered by Owens-Illinois.

A typewriter-like keyboard incorporated in the control panel is combined with the powerful text feature of the display to provide a high-performance silent computer terminal, in addition to its normal data display capability.

A removable-media dual disk drive is used as an economic program, data, and overlay storage

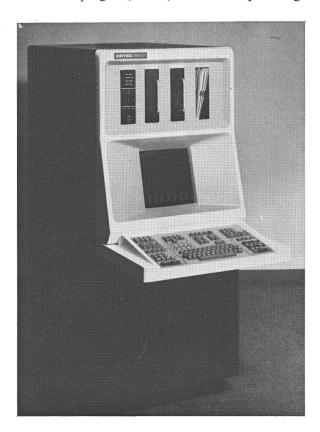


Fig. 6 Implemented System

device for the system. Fig. 6 shows the system as implemented.

In summary, the system architecture and high-level software language described above provide the user with a powerful tool-kit for easily and quickly configuring and programming a multichannel analyzer to match his needs. In addition, the use of a standard interfacing structure, CAMAC, readily allows the user to implement control and instrumentation features outside the range of an MCA or computer.

### **NEWS**

#### COMPEC EUROPE, BRUSSELS MAY 18, 19, 20, 1976

The organizers of the well known COMPEC exhibition and conference in England are announcing a COMPEC EUROPE at the Manhattan Centre in Brussels on May 18, 19, 20, 1976. COMPEC EUROPE will follow the pattern from COMPEC UK; it concentrates on small computers, computer peripherals, and systems.

The European CAMAC Association has been

invited by the organizers, Trident Conferences and Exhibitions Limited, to participate in both the exhibition and the conference in the same way as the UK CAMAC Association did in the COMPEC UK, where they took a 'CAMAC area' in the exhibition and took part in the organizing of a CAMAC session at the conference.



### MICROCOMPUTER CONTROLLED RANDOM DATA ACQUISITION SYSTEM

by

J. Lecoq, H. Tedjini, P. L. Wendel, and G. Metzger

Laboratoire d'Electronique et d'Instrumentation Nucléaire, CUHR Mulhouse : Laboratoire des Applications Electroniques, ULP, Strasbourg, France.

Received 30th January 1975

SUMMARY This CAMAC system for data acquisition and manipulation is controlled in an interactive way by an operator through a microcomputer. The system, built around an Intel 8008 chip, includes a magnetic tape unit, a CRT display, an XY recorder, a fast analogue-to-digital converter, and a CAMAC I/O register.

#### INTRODUCTION

The system described here is intended for data acquisition and manipulation (Fig. 1). The main features include:

- Interactive control with the operator through a Teletype
- Versatility (programmed system)
- Use of the Camac standard for most I/0 devices (easy expansion)<sup>5</sup>.
- Inclusion of a Magnetic Tape Unit.

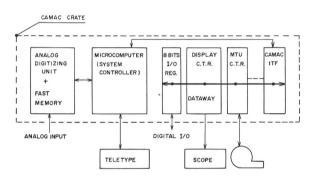


Fig. 1 System Structure

These features distinguish this system from many others of similar purpose<sup>1,2,3</sup>. It is typically used in processing pictures such as aerial photographs, or photographs of blood cells. The first step is to digitize the video signal from T.V. camera and store this data on a magnetic tape which is then processed by a UNIVAC 1108 computer. The second step is to read the processed picture-data from magnetic tape and present it on a CRT display, for example.

The reaction time of the system is not critical, because it is controlled by a man, and its computing power and memory requirements are not large. Therefore we chose a microcomputer rather than a minicomputer, since it fulfils our requirements without great expense.

#### **HARDWARE**

#### Microprocessor

This complete microcomputer is built around the INTEL 8008 chip (Ref. 4) and is composed of:

- Memory: 2.2k×8-bits PROM and 2k×8-bits RAM
- Control-Timing hardware (clocks, state decoders, registers)
- I/O hardware (multiplexers for input, registers for output).
  - The memory is divided into two main areas:
- 2.2k PROM are used by the operating system to ensure that the user cannot destroy it
- 2k RAM are used as scratch-pad and channel (DMA) areas.

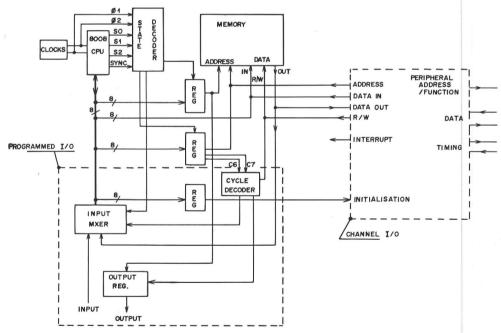


Fig. 2 Channel I/O Structure

The I/O system is subdivided into Programmed I/O and Automatic Block Transfer I/O channel (DMA), because of the slow speed of programmed

transfer (8 bits in 80 µsec), (Fig. 2).

The DMA channel works in the classical way: the first step is to establish the peripheral device address and function code, and to initiate the channel, the second is to transfer data autonomously between the peripheral device and RAM channel area  $(786 \times 8\text{-bit})$  words max.). The CPU is stopped during a transfer, and the channel restarts it with an interrupt at the end of the transfer. This is peculiar to our system and means that the channel does not free the CPU from tedious I/O operations but makes 'high' speed transfers possible (8 bits in 4 µsec).

#### I/O Interfaces

They are divided into general-purpose and special interfaces. The general purpose interfaces are naturally built in the CAMAC standard, so that we can use any of the numerous commercial CAMAC modules. The special interfaces are the TTY interface and the digitizing unit interface. The teletype is directly linked to input/output ports and has a 'programmed interface' (the hardware includes only three transistors, and it does not need an elaborate interface. The TTY is the only I/O device communicating with the operator in this conversational system.

#### **General Purpose Interfaces**

Digitizing Unit: This module contains an ADC converter (10 MHz, 8 bits) and a fast RAM memory ( $512 \times 8$  bits, 50 ns access time). It converts analog data and stores it. Then the digitized data can be read by the microcomputer and transferred into the main memory.

Display CTR: This is a somewhat modified S.A.I.P. display-driver CAMAC module for con-

trolling an XY recorder or a CRT.

We use it to display signals as functions of time X(t) or of another signal Y(X), and also to display pictures. For this latter mode Z modulation is obtained by addition of an amplitude-to-time converter. For example a true picture can be recorded in about one minute  $(512 \times 512 \times 8 \text{ bits})$  through a Tektronix 604 scope, onto a Polaroid film.

Magnetic tape controller: This module (6) is a laboratory-constructed CAMAC module to control a PEC 9-track 800 bpi 25 ips tape driver and formatter in both read and write mode. It includes some complex commands such as 'Write Forward a block of indefinite length and write an End of Block if no more data is available', to simplify programming of the microcomputer.

Digital I/O controller: This is also a laboratory-constructed module to match another equipment<sup>7</sup>) and to allow its connection to the microcomputer system.

#### **SOFTWARE**

#### General organisation

Our software system is built around two main principles:

- It must be possible for different and non-specialized physicists to use it.
- System operation must be fully interactive with the operator on a conversional mode through the TTY.

Thus it was necessary to provide a true small operating system, based on a TTY monitor, including service routines and library. All the programs can be written in Assembler: a Univac 1108 Cross Assembler, specially written, provides the binary object code on magnetic tape ready to be loaded into our microcomputer<sup>8</sup>).

#### Operating system

Operator communication package: This includes a TTY Driver, character identification program, error print, message writer and the main loop. The microcomputer is in the halt state at rest, and is started only by the TTY interrupt. After completion, it returns to the halt state.

The operator interacts at four levels:

- System call by control code 'ACQ' or 'TRF'
- Input or output call
- Typing an I/O Device call
- Typing an I/O presentation call.

#### Table 1 Command Mnemonics.

- STR STORE COMMAND
- LSB BINARY LISTING COMMAND
- LSD DECIMAL LISTING COMMAND
- JMP JUMP TO ADDRESS COMMAND
- TRF TRANSFER COMMAND
- AVF FORWARD N FILES COMMAND
- AVB FORWARD N BLOCKS COMMAND
- PSF FILE NUMBER QUESTION
- RWD REWIND COMMAND
- FMK FILE MARK COMMAND
- IPL LINK TO PROGRAM AT ADDRESS...
  COMMAND
  - COMMAND
- ECT WRITE COMMAND
- LEC READ COMMAND
- MGN MAGNETIC TAPE ACTIVATION
- SCP SCOPE ACTIVATION
- TRC RECORDER ACTIVATION
- REG I/O REGISTER ACTIVATION
- X/Y X/Y MODE OF PRESENTATION COMMAND
- Y/T Y/T MODE OF PRESENTATION COMMAND
- PR 1 PROVISIONAL USER PROGRAM
  - COMMANDS

PR 7

Program/Machine Housekeeping subsystem: The loaders are all binary; either manual from TTY keyboard or automatic from paper tape (Intel code) and from magnetic tape. The Editors are provided in binary or decimal code on the TTY printer or on the paper tape. Relocation and linking programs relocate and execute parts of programs loaded from the magnetic tape in an overlap mode. Some of these routine make use of a 122-word RAM area to store parameters. There is also a small library.

I/O Package: These subroutines are written to give a general form to all peripheral drivers using CAMAC and the channel. Special drivers for the others peripherals are provided. The first 128 words of the channel memory area are used to store labels which are written at the beginning of each block on the magnetic tape. The number of parameters and the block length are automatically updated. All device drivers are of classical form, except the MTU Driver which is expanded to allow easy tape manipulation by the users (see table 1).

#### CONCLUSION

A microcomputer-controlled system has been constructed for data acquisition, storage and display. Its primary goal has been far exceeded; this has been possible because of the hardware and software structure, which includes a microcomputer with CAMAC interface and a small operating system. This allows easy use of the system by non-specialists for different purposes, such as picture processing.

Easy system expansion is guaranteed through the use of the CAMAC standard for most I/O connections.

#### **ACKNOWLEDGEMENTS**

We are very grateful to Dr. J. Meyer Maître-Assistant, who gave the principal guidelines to the software structure, especially concerning the Operating System. The many discussions we had saved us much time and effort.

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- 7. 'Column video digitizer and display unit for digital image processing' by P. L. Wendel et al. submitted to Rev. Sci. Instr. December 1973.
- 8. '8008-UNIVAC 1108 Cross Assembler' by B. Colin and P. Keith. Internal Report, Laboratoire d'Applications Electroniques Strasbourg, September 1973.

### **NEWS**

### FIRST GENERAL ASSEMBLY OF THE EUROPEAN CAMAC ASSOCIATION

The General Assembly of the ECA will be held on Friday, 17th October, at the Sheraton Hotel, Brussels following on from the 2nd International Symposium on CAMAC in Computer Applications. Everyone, interested in any way with the use of the CAMAC Standards, is invited to attend this FIRST, and inaugural, Assembly of the Association since its foundation in May 1974.

The agenda includes acceptance of the Statutes and Standing Orders, drafted by the Interim Council of the Association, for regulating the affairs of the Association. Reports of the year's activities of the Management Board, the Interim Council and the two Working Groups (Industrial and Medical applications) will lead on to a discussion of proposals for a further programme to pursue the Objects of the Association, which are: 'To undertake and investigate methods that will lead to the expansion

and use of the CAMAC Standards in new areas of application, ensure the widest possible dissemination of knowledge of these Standards and encourage the use of CAMAC on a multi-national basis with a view to advancing and supporting the technology of automation'.

Application forms for membership of the ECA will be available from a sent to all those who announced their interest in ECA already. Further application forms are available from the ECA Secretariat (provisional address, c/o Commission of the European Communities, C.R.C.-CBMN, Steenweg naar Retie, B-2440, GEEL, Belgium), and at the Registration Desk of the 2nd International Symposium on CAMAC in Computer Applications (October, 14–16, 1975, Hotel, Manhattan Center, Brussels).

#### **CERN 'CAMAC NEWS'**

Issue No. 5 (April '75) of the CERN 'CAMAC NEWS' contains a report by Fred Iselin dealing with, among other things, interfacing CAMAC to NORD-10 computers and a CAMAC Pulse Amplitude Analysis System based on a Hewlett Packard HP 2100 computer. The NEWS also presents a survey of companies who manufacture or supply

CAMAC equipment or components. Several new facilities in the range of CAMAC modules are described.

Distribution of the 'CAMAC NEWS' is handled by J. Halon, NP Division, CERN, 1211 Geneva 23, Switzerland.



### CAMAC EQUIPMENT FOR MONITORING A TELECONTROL SYSTEM

by H. Mayer

Österreichische Draukraftwerke Aktiengesellschaft, Klagenfurt, Austria
Received 13th February 1975

SUMMARY CAMAC equipment and a minicomputer are used to monitor a large telecontrol system for a group of hydro-electric stations. This monitoring equipment attempts to solve the problem of trouble-shooting sporadic faults in the telecontrol system.

#### INTRODUCTION

A chain of three hydro-electric power plants is supervised from a central control room with the aid of a computer. One power plant, with its two kaplan turbines of 40 Megawatts each and the associated gates, is supervised directly from the central control room, which is situated near this plant. The other two (later-on three) plants are supervised by additional telecontrol systems. The telecontrol systems generate various signals when an internal fault occurs. These signals have to be collected in order to monitor the telecontrol equipment. Approximately 100 different signals may be generated by each telecontrolled power plant.

The telecontrol equipments themselves have a good reliability. In addition, a suitable configuration was chosen so that internal faults do not affect the ability to supervise the power plant. The telecontrol equipments work on the basis of pulse-time modulation, in which the message (information) is transmitted by a sequence of pulses and intervals. In this case the information is conveyed by the duration of the pulses and intervals. An additional transmission of paritymarks enables the receiver to recognize errors on the transmission line.

The task of the monitoring equipment, described here, is to gather the internal signals and print a short text of approximately 15 characters, together with the time. Such an output from the central processor is of no use to the shiftman in the central control room, but it is of value to the electronic service-man who is responsible for maintenance of the telecontrol equipment. If necessary, he can use the monitoring equipment to test the faulty telecontrol system. The tests may last for several days or weeks in the case of an intermittent fault.

#### SOLUTION

The requirement for generating a printed text when an internal signal occurs is easy to fulfill by a minicomputer and a teletype.

But how to monitor a telecontrol system in the best manner? The message (the block of pulses and intervals) has to be checked. The information block might be checked at the transmitting line, after the voice frequency equipment, and after the message has been assembled within the receiver. Naturally this kind of check is valid mainly for the receiver. By making observations at various points it is

possible to locate the faulty part of the equipment. For example if it is confirmed that an incorrect message was received, it is easy to decide whether the sender or the transmitting channel is defective.

For monitoring a sender, which is also possible, a similar checking routine is necessary. If the defect sender is situated in a controlled plant, the monitoring system, which is very compact, is transferred to the relevant location. The parallel output of the receiver is also brought to the monitoring system. The monitoring system itself transforms the message-block into parallel information and compares both. In this way the whole receiver unit is checked. As the result of its monitoring function the system described here can be used as a general stand-by receiver. In addition, periodical monitoring to obtain statistical information is possible at any time.

#### HARDWARE CONFIGURATION

The line signals, as well as the parallel output from the receiver are collected by digital inputs.

The checking of the duration of pulses and intervals is carried out by counting a clock frequency of 100 or 10 kHz, generated by the monitoring equipment. The input to this counter is controlled by the signal to be checked. The signal transition which stops the counting also gives an interrupt to the system, which then stores the content of the relevant counter.



Digital outputs for the parallel information are provided for use when the equipment is working as a receiver.

For the text output a silent teletype with a speed

of 30 ch/s has been chosen. It is combined with two built-in magnetic cassettes, and is very useful for editing and debugging programs because of its fast data transfer speed. The cassette equipment is not primarily intended for this purpose, but by using a little ingenuity it can be used.

A fast paper tape reader enables all the manufacturer's programs to be used. Finally, there is a minicomputer with 16-bit word-length, and as a result of the selected configuration there is only 8k

of core memory.

#### SUMMARY OF HARDWARE

1 Minicomputer 8k, 16 bit

1 clock

24 interrupts

346 digital inputs

64 digital outputs

48 digital pulse outputs

10 counters

1 Teletype with 2 cassettes

1 paper tape reader 150 ch/s

### **NEWS**

#### CONFERENCE ON TRENDS IN ON-LINE COMPUTER CONTROL SYSTEMS

This conference, at Sheffield on 21-24 April 1975, was organised by the UK Institution of Electrical Engineers and attracted over 200 delegates, of whom nearly a quarter were from overseas. The developments in the CAMAC standard since the previous Sheffield conference in 1972 were summarised in a paper by Barnes, et al.<sup>1</sup>. Other papers described major control systems using CAMAC. The control system for the ISR at CERN, with a capability of eight parallel and eight Serial Highways, was described by Verelst<sup>2</sup>. The computer networks at the Daresbury Laboratory, for controlling the NINA electron accelerator and the proposed Synchrotron Radiation source, were described by Atkins et al.<sup>3</sup>. The control system for the CERN 400 GeV accelerator, described by Crowley-Milling<sup>4</sup> has 25 minicomputers, many of them interfaced to the accelerator through CAMAC.

The conference indicated a marked trend towards multi-processor systems. The low costs of minicomputers and micro-computers now favours taking the processing power to the controlled plant, rather than transmitting the process variables to a central computer. The CAMAC Serial Highway is

obviously relevant to this situation.

There were interesting comparisons between CAMAC and other standards. A paper by Benson et al.5 of ICI Petrochemicals Division, described experience with some of the 30 systems based on the MEDIA interface system and the RTL-2 realtime language, both developed as proprietary standards by ICI. Several delegates took up the comment by Verelst that the name CAMAC does not guarantee the quality of the products. In this respect it was relevant to compare the case of CAMAC, as an international standard without

direct financial support, and the UK national and military computer language, CORAL 66 which receives government support for product-testing and promotional activities (described in a paper by Neve of the Royal Radar Establishment). Many existing users of CAMAC would surely challenge the claim made in a review of computer-based laboratory automation, by Sawyer et al.6 of the University of Bath, that undesirable factors of CAMAC result in system costs some two to three times those of other, proprietary, systems.

#### References

CAMAC — A Review and Status Report, Barnes R.C.M., Bisby H., Hooton I.N., Lewis A., UKAEA, Harwell, U.K.

Experience with CAMAC Standard for Control of a large Nuclear Facility, Verelst H., CERN,

Switzerland.

Computer Control Systems for Electron Accelerators at the Daresbury Laboratory of the Science Research Council, Atkins V.R., Hopkins J.C., Hughes E.A., Poole D.E., B.E., Daresbury Laboratory, S.R.C., U.K.

The Multi-Computer Control System for the CERN 400 GeV Accelerator, Crowley-Milling M.C., Hyman J.T., Shering G.C., CERN,

Switzerland.

Experience with a MEDIA/RTL-2 Process Control System, Benson R.S., Gladders M.J., ICI Ltd. U.K. Niblett J.D. GEC-Elliot Process Instruments Ltd., U.K.

Some Trends in Computer-Based Laboratory Automation, Sawyer P.E., Lockett A.D., Thompson J.W., University of Bath, U.K.

#### ANNOUNCEMENTS BY CAMAC MANUFACTURERS

KINETIC SYSTEMS CORPORATION, USA has established a representation in Europe:

Kinetic Systems International S.A. 2/6 Chemin de Tavernay

CH-1218 Grand-Saconnex, Geneva

that will be exclusively concerned with CAMAC. Serial CAMAC systems and over 50 different units are available from stock or on 4/6 weeks delivery.

Kinetic Systems International also offer:

Design assistance for systems at short notice and for any application.

Installation assistance for purchased equipment.

Maintenance by a 24 hours per day module replacement service and modern test facilities.

Ref. No. 13.0001

### **DEVELOPMENT ACTIVITIES**



### AN INTERFACE BETWEEN CAMAC AND THE DIGICO MICRO-16V COMPUTER

by

H. D. Blake and D. J. Folwell

Cranfield Institute of Technology, Bedford, England
Received 27th January 1975

SUMMARY A CAMAC interface unit has been developed to allow a Digico Micro-16V computer to be used with a GEC-Elliott Executive System.

#### M16V COMPUTER

The DIGICO M16V is a 16-bit digital computer with a 950 nsec core cycle. The core memory is expandable in 4k modules up to 64k.

It has a Medium Speed Interface (MSI) for peripheral data transfers and also a Direct Memory Access (DMA) facility.

A Multi Level Interrupt (MLI) option is also included, providing 16 levels of priority interrupts from the peripheral channels. Three of these levels are used for this interface.

#### **GENERAL DESCRIPTION**

It was decided that transfers between the M16V and CAMAC should be of two types: Program Transfers and Block Transfers, each using a separate DMA channel but both controlled from one MSI peripheral channel.

To make the interface compatible with the 24-bit word size of CAMAC, it was arranged that word transfers could be 24-bit or 16-bit as required. Twenty-four bit words are handled in two bytes, one of 8 bits and one of 16 bits.

For data transfers to take place, Control and Status information is required. This is held in two registers in the Interface Unit: Control and Status Register High (CSR H, 10 bits) and Control and Status Register Low (CSR L, 16 bits). The bit allocation is as follows:

Crate Code

CSK I		
BITS	0-2	CR
BITS	3-5	BR

CCD II

DIIDO	CIC	Crate Code
<b>BITS 3-5</b>	BR	Branch Code
BIT 6	CaR	Crate Address Register
BIT 7	Sr	Stock Register
BIT 8	P	Q Status bits
BIT 9	R	(Block Transfers)
CSR L		,
<b>BITS 0-4</b>	N	Station Code
<b>BITS 5-8</b>	A	Sub Address
BITS 9-13	F	Function
BIT 14	L or Q	L Trigger or Q Response
BIT 15	WS	Word Size $1 = 24$ -bit transfer
		0 = 16-bit transfer.

This information is decoded and gated onto the CAMAC Dataway to enable the correct operation to be performed.

Similarly Data words are held in two registers in the interface; Data Buffer High (DBH, 8 bits) and Data Buffer Low (DBL, 16 bits). Figs. 1 and 2 show the order in which data are held in core.

The interface also contains an Address Register, which at the start of a transfer will contain the intial core address, and a Word Count register which is used to control the number of word transfers in a Block.

The Q Response to a particular transfer is tested and, depending upon the Q status bits in the CSR registers and the type of transfer (Program or Block), appropriate action is taken within the interface.

Extra hardware is included within the interface to handle any Look-at-Me that might occur. A Grant Graded-L operation (REF 1, 2) is automatically performed.

#### **PROGRAM TRANSFERS**

A Program Transfer (Fig. 1) is a single CAMAC operation initiated by a specific computer instruction. The instruction is decoded, and initial core address transferred, by way of the computer's Medium Speed Interface.

Initially, two consecutive DMA cycles transfer control and status information to the interface.

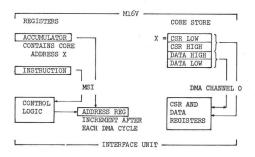


Fig. 1 Program Transfers

To transfer data, a further one or two DMA cycles follow, depending upon the word size selected (CSR L, bit 15).

For a 'data-less' operation, only control and status information transfer is necessary.

A Program Transfer, therefore, requires a maximum of four store locations. Figure 1 shows how the status information and data are arranged in core.

As a result of a CAMAC operation, the addressed module may generate a Q response signal. The response is compared, in the interface, with the Q status bit in the CSR L register. If the value is the same no action results, but if the values differ a computer interrupt is generated on a particular priority level to enable appropriate software action to be taken.

#### **BLOCK TRANSFERS**

Block Transfers (Fig. 2) as implied, enable consecutive data words to be transferred.

In addition to the Control and Status information, a Block Count and Data Start Address are required in the interface. This information is held in 4 consecutive store locations as a Control Block.

On initiation of a Block Transfer, four D.M.A. cycles transfer control information to the interface.

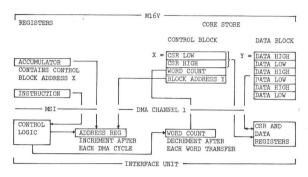


Fig. 2 Block Transfers

Data transfers will now commence, but can either be in Normal or L-Triggered mode, according to the significance of the L bit contained in CSR L.

In Normal mode, data transfers continue until 'end of block' is reached.

The 'end of block' depends upon the Q response and the significance of the Q status bits, P and R, in the CSR H register. These status bits are arranged to enable the following four types of Block Transfer to be performed

 $\begin{array}{ll} P=0,\ R=0 & Q\ suppressed \\ P=0,\ R=1 & Repeat \\ P=1,\ R=0 & Stop \\ P=1,\ R=1 & Address\ Scan. \end{array}$ 

Two levels of interrupts are used to inform the computer of 'end of block' or of a malfunction that may occur.

In L-Trigger mode, data transfers are delayed until a chosen module generates a Look-at-Me (LAM). Any LAM may be assigned for L-Trigger purposes by hardware patching but, to ensure immediate response, it should have the highest possible priority.

Block length is controlled by the Q response as for Normal mode.

### AUTOMATIC GRANT GRADED L (Auto GGL)

The AUTO GGL part of the interface can be enabled and disabled by specific computer instructions.

When enabled a Grant Graded-L operation is performed in response to a Demand signal presented by the Executive Controller (Ref. 1). The Demand is the result of any LAM in the system.

The pattern of LAMs is read, and placed on the Dataway R lines by the Executive Controller. They are priority sorted within the interface and the highest, together with the corresponding Branch Code, is formed into an 8-bit priority vector.

This vector, which can be read by the M16V, is also used in conjunction with a Re-Entrancy Trap Store within the interface, to prevent re-entering of service routines until they have been completed.

A third level of interrupts is used specifically for this facility.

#### CONCLUSION

A four-station prototype unit has been used successfully for developing test programs and operational software.

Commercially available modules are used for test purposes and for access to a Digital Differential Analyser.

#### **REFERENCES**

- 1. G.E.C. Executive Suite Handbook.
- 2. The CAMAC System of Data Handling (Smith, Drury and Troy, G.E.C. Ltd.).

### **NEWS**

#### UNITED KINGDOM CAMAC ASSOCIATION (UKCA)

Since its formation, the UKCA has published two News Letters, participated in COMPEC '74 and held two seminars at which the attendance was restricted in order to enable a meaningful forum for discussion.

The 2nd News Letter is double the size of the 1st and is packed tightly with interesting items concerned with reviews of ECA, UKCA, ESONE and NIM activities together with details of forthcoming events. The UKCA is planning to participate again in COMPEC '75 because of the successful reaction to that of last year.

The Association was encouraged to mount a second Seminar in March by the favourable reaction

from the 1st Seminar in February. An attendance of about 35 people heard and exposure of the various ways in which BASIC has been extended to incorporate CAMAC operations, presented by Francis Golding on behalf of Ian Pyle who was not able to be present. The same speaker discussed CATY and the reasons for this specific implementation of a BASIC-based CAMAC language. A lively forum started up as participants revealed and discussed their attitudes toward, and problems with, CAMAC software. In the afternoon, Peter Clout (Daresbury Lab) talked on LAM-handling and there followed an informative tour of the extensive use of CAMAC in the host Laboratory at Daresbury.



### AN ALPHA-NUMERIC AND GRAPHICAL DISPLAY DRIVER IN CAMAC

by N. V. Toy

GEC-Elliott Process Automation Ltd. Leicester, England
Received 7th February 1975

SUMMARY This micro-programmed CAMAC module provides comprehensive facilities for displaying alphanumerics and graphics on an oscilloscope. The display can be refreshed from a local memory. Operational modes such as character size, generation of single vectors and sequences of vectors, and the choice of intensity, style of lines, and blink mode are selected by ASCII codes.

#### INTRODUCTION

The alpha-numeric and graphical display—both informative and interactive—is now accepted as a growth market and much equipment is becoming available to the user in the form of V24 remote terminals, or various formate using in-house standards.

The display presentations are usually based on closed-circuit television techniques, refreshed displays, or storage tubes. However TV-style displays are poor where graphics are concerned and storage displays are generally used in this market area. Refresh techniques usually place a burden on store access.

New integrated-circuit technology now allows the addition of a local memory to refresh a fast display generator. This can then draw complex pictures of mixed alpha-numeric and graphic formats, with better contrast and definition than is possible with storage tubes. Local memory improves the refresh rate and reduces the data traffic on the peripheral highway; however, it is obviously important to employ an internal command set that allows the memory to be used efficiently.

The design of the CAMAC Display Driver DD1603 currently under development by GEC-Elliott Process Automation illustrates some of the above points. It is intended to be most effective when used in conjunction with the Hewlett Packard HP1300 Series Display Oscilloscopes and a local storage memory module.

#### **DISPLAY DRIVER DD1603**

A particular feature of the Display Driver DD1603 is the provision of a small internal memory  $(32 \times 16\text{-bit words})$  which is used for communication between the Display and the host computer. It is also used to store a pre-programmed cursor symbol —usually as a string of short vectors. This internal memory is separate from the private local memory. In fact the DD1603 may be used without the local memory in systems where computer—updating is not a penalty.

Apart from the definition of 128 alpha-numeric characters (including lower case, mathematical and Greek symbols) a sub-set of ASCII codes is used to control the Display Driver, switching it between operational modes or changing operating param-

eters, some of which are listed:

Short vector mode
Long vector mode
Histogram mode
Point-plot mode
Group operation
(one word per vector)
(automatic X increment)
(two words per point)
(see later)

Store Pointer word
Vector line type
Character size
Blink ON/OFF
(see later)
(dash-dotted-solid)
(×1, ×2, ×3 or ×4)
(causes display to flash)

Intensity (3 levels)Spot check (see later)

A mode or parameter remains as set until cancelled or changed.

All vectors are expressed as signed deviations from the current spot position; circles may be drawn by a small modification to the vector algorithm. Short vectors are  $2 \times 7$ -bit words and long vectors  $2 \times 11$ -bit words. Arcs require  $3 \times 12$ -bit words.

Group operation is analogous to a Jump-to-Subroutine call whereby a common complex symbol or figure may be formed from a string of suitable short vectors and called from any number of places in the main command sequence. A corresponding 'Return' command is placed at the end of

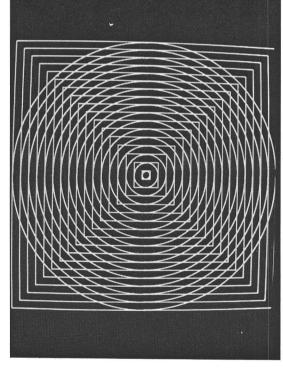


Fig. 1 Test Pattern for Vector and Arc Modes on the Display Driver DD1603

the group string. Thus, for example, such symbols as logic gates and circuit devices in computer-aided design work way be defined once with precision and used many times in a command sequence.

Light pens are used, in the main, for either selection of a matrix position defined by the X-Y co-ordinates or for 'menu-picking' where one of a number of alternative routines is selected by placing the pen over the symbol or word corresponding to the required routine. In this latter case the X-Y co-ordinates of the selected symbol are of no immediate value since they cover a range of values depending on which portion of the symbol activated the pen. These co-ordinates must then be related to the required routine probably by means of a jump table In the DD1603 'menu picking' is facilitated by the use of Pointer words.

During the display sequence a Pointer word may be transferred into a temporary location of the internal memory before each menu symbol is described. If the light pen is activated by the symbol, the Pointer word is automatically transferred from the temporary location into a specific communications location to be read by the computer.

The Pointer word may be any 16-bit word suitable to the program, e.g. a direct pointer to the selected routine. The Light Pen action will, of course, also cause the X and Y co-ordinates of the screen spot to be transferred to a specific pair of locations in the

internal communications memory, so that both the absolute position and the Pointer word are available to the software, to be used as convenient.

Separate on and off blink control commands may be used to cause any combination of lines and text defined between them to flash at a nominal rate.

As a spot check facility the X-Y co-ordinates may be stored at any time in a pair of specific locations in the internal memory and compared by program with the computed spot position.

The accompanying illustration (Fig. 1) shows one of the test patterns employed to check the vector and arc modes of operation.

#### CONCLUSION

No doubt some of the facilities described above appear to some users to be over-complex and unnecessary for their own requirements—but CAMAC equipment is finding use in a wide range of applications and what to one user is a redundant feature is essential to another. Since the design technique of the module is based on micro-programming techniques, once the basic data paths and memory storage have been established the extra facilities are not much more than extra ROM sequences. It is therefore more economic to design one module to cover a wide market need.

# )

#### CAMAC INTERFACE FOR A BUFFERED CARD READER

by

K. van Dellen\*, F. Sporrel, and L. M. Taff

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\* Now at CEVAN, Groningen, The Netherlands

Received 17th February 1975

SUMMARY This CAMAC module is an interface for a buffered card reader. Special hardware features include character decoding, packing characters into the computer's internal format, and detection of end-of-file cards.

A CAMAC module has been built to interface a Mohawk Data Sciences card reader (Model 6042, 400 card/min) to a Digital Equipment PDP-15 computer. CAMAC interfacing was chosen for the reader so that it could be switched easily between a pair of identical PDP-15's comprising the K.V.I. nuclear data acquisition system (DAS); each machine has a CAMAC branch driver (DEC model CA-15).

The CAMAC module has several special features, including hardware for (i) Hollerith character decoding, (ii) packing of characters into PDP-15 internal code, (iii) detection of end-of-file cards, and (iv) skipping to next card.

Since the computers are used in a real-time data-acquisition system, interrupt servicing could not be guaranteed within the column-to-column motion interval (about lms) as a card is processed. Therefore card-image buffering was required; such a buffer was purchased from the manufacturer of the reader and installed in the reader itself.

With the hardware architecture of Fig. 1, three data modes were implemented: binary (12 bits, 1 card column, per CAMAC transfer), 'image' ASCII (one 7-bit hardware-decoded right-justified character per CAMAC transfer), and the more efficient PDP-15 standard '5/7' ASCII (five 7-bit ASCII characters packed into two consecutive 18-bit memory locations, with 1 bit unused).

When the reader is turned on it automatically reads a card into its internal buffer, and then signals the CAMAC module that it is ready. The module sequentially reads the reader buffer, generating a

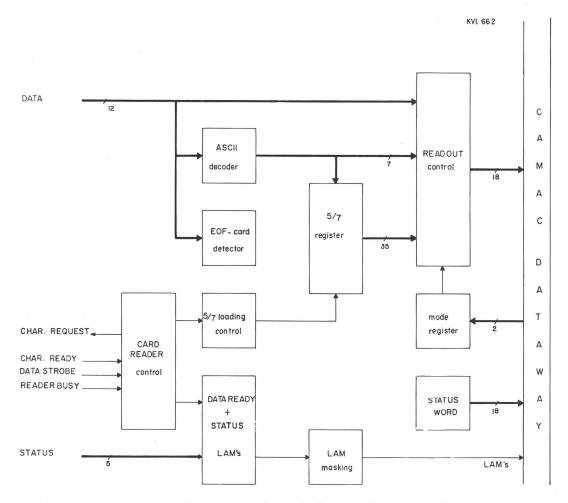


Fig. 1 Block Diagram of CAMAC Card Reader Interface

LAM for each card column in binary and image modes, and for each five columns in '5/7' mode. The reader automatically reads the next card when (and only when) its buffer is empty, setting a 'busy' line until it is ready again. If the CAMAC module detects a 12-11-0-1 or 7-9-8 punch in card column one, an end-of-file condition is generated; a 'skip card' function can then empty the reader buffer (by simply reading and ignoring the data) to proceed to the next card. To use the present module with an unbuffered reader, a provision must be added for initiating a read operation explicitly.

The module is built using wire-wrap techniques with 88 integrated circuits, and occupies two CAMAC stations. One of the two available LAMs is used for announcing error and status conditions; the other is a 'data-ready' signal wired to GL24 for PDP-15 CAMAC data-channel transfers. An 18-bit

status word containing detailed information about both the reader and CAMAC module is available through a 'read status' function. The hardware character decoding was done with field-programable read-only memories.

A software handler for the reader is operated under the standard PDP-15 single-user operating system. The hardware decoding and packing allows considerable reduction in handler size, though the card buffering requires somewhat complicated error and status processing.

The module was constructed by K. Nauta. Part of this work was performed within the research program of the 'Stichting voor Fundamenteel Onderzoek der Materie' (F.O.M.) with financial support from the 'Nederlandse Organisatie voor Zuiver Wetenschappelijk Onderzoek' (Z.W.O.).



### CAMAC INTERFACE MODULE FOR THE BIOMATION TRANSIENT RECORDER TYPE 8100

by

I. Török

Joint Research Center, Ispra, Italy
(on leave from the Institute of Nuclear Research of the Hungarian Academy of Sciences, Debrecen, Hungary)

Received 3rd October 1974

SUMMARY A single-width CAMAC module has been developed for control and read-out of a single Biomation Type 8100 transient recorder. The module performs programmed data transfers.

A single-width CAMAC module has been developed for control and read out of a single Biomation Type 8100 transient recorder. The transient recorder can be 'programmed' through the module by sending appropriate control words to its digital inputs. Almost all the front panel settings can be controlled through this interface.

The memory content of the transient recorder can be read out using two different methods. One of them is a Stop mode programmed block transfer, which uses the Q response for detecting the end of the block, and can be interrupted using a special LAM when the transient recorder is not ready for the next transfer. (This is the case when a refresh-cycle has been started in its MOS memory). Another

LAM warns when the 8100 is ready again.

The other method, a little slower, is to test the flag of the 8100 before every read out CAMAC command, and to test afterwards that the command was acknowledged by the 8100. The relatively high data-word rate of the 8100 makes it possible to transfer two 8-bit words from the transient recorder to the memory of the controlling computer in one Dataway cycle.

A LAM signal is generated from the trailing edge of the record signal of the 8100, which is at logic '1' during the recording time. This LAM starts the read out subprogram.

The module uses 19 CAMAC commands.

The X response signal is used to detect if the 8100 is not powered, simply AND-ing the X and the +5V of the 8100. If the 8100 is not powered, all CAMAC instructions sent to the module will give an X=0 response.

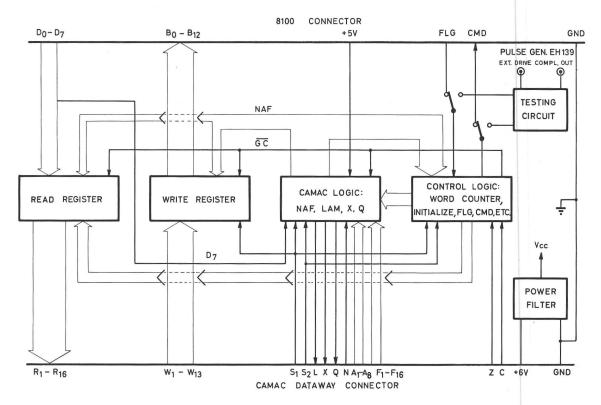


Fig. 1 Simplified Block Diagram of Interface Module for Biomation Transient Recorder Type 8100

Some built-in circuits are provided for testing the module without the 8100, using a pulse generator (e.g. EH139) to imitate the varying width flag pulse of the 8100.

A simplified block diagram of the module is

shown in Fig. 1.

The module will be used in a LIDAR system, for measuring air pollutants. The system uses a PDP-11 computer to control CAMAC equipment through a BORER 1533 A dedicated crate controller.

### **SOFTWARE**



#### MACRO-IML IMPLEMENTATIONS FOR THE PDP-11 COMPUTER

(A language for use in CAMAC systems)

by

M. Kubitz and R. Kind

Hahn-Meitner Institut für Kernforschung Berlin GmbH, Germany
Received 15th January 1975

SUMMARY IML has been implemented for the DEC PDP-11 computer with the DEC CA-11A CAMAC branch controller and the Borer 1533A single-crate controller, and with the DEC operating systems DOS, VO8/VO9 and RSX-11D (and in future with RSX-11M). The implementations follow the macro-syntax given as an appendix to the definition of IML.

#### INTRODUCTION

These IML implementations follow the macrosyntax as given in appendix A of the document "CAMAC—the definition of IML" (A language for use in CAMAC-systems)¹. This document has been adopted as a description by ESONE and US NIM in August/September 74. They implement IML for the DEC PDP-11 computer² with the CAMAC branch controller DEC CA-11A³ and the single crate controller BORER type 1533a⁴. For both DEC operating systems DOS VØ8/VØ9 and RSX-11D a full set of macros has been implemented, except block transfer on special LAM, X-error control statements and the subscript mode. Transfer modes not implemented by the hardware of the CA-11A are simulated by software.

### DESCRIPTION OF THE IMPLEMENTATIONS

The following fundamental conditions have been satisfied in the IML-implementations:

IML is made available for all DEC PDP-11 computers.

This has been obtained by writing the macro expansions in Macro Assembler of DEC PDP-11<sup>5</sup> and by using only those instructions which are implemented by hardware in all computers of the PDP-11 family.

• The macros can be executed under the DEC operating systems DOS VØ8/VØ9 and RSX-11D respectively, and in the future RSX-11M. All input/output (I/O) transfers are handled directly by MOV-INSTRUCTIONS in the appropriate IML statement. By embedding the I/O into the macros the need to write a CAMAC I/O handler for the particular DEC operating system has been avoided. A program running under RSX-11D has to be a privileged task to have access to the device register addresses. This method also allows the rapid implementation of IML for other operating systems, e.g. RSX-11M. Only the LAM handling part of the implementation requires redesigning if other operating systems are to be used.

• Short execution time of CAMAC I/O in action statements at runtime.

Because of address calculations at assembly time and the use of conditional assembly directives the macro expansions require little core memory at runtime and give an optimum execution time. On average, a single action statement (READ or WRITE) consists of five to six assembler instructions, depending on the controller. At assembly time, the core memory requirement is determined by the operating system and the macro assembler with its symbol table, and amounts to 24 K words (16 K for the IML subset) under DOS and 52 K words (44 K for IML subset) under RSX-11D. The high core memory requirement at assembly time is a consequence of the conditional assembly directives. It is expected that the core memory requirements for PSX-11M are similar to the DOS-system.

• Reservation of core in declaration statements as in high level languages. In the declaration statements of IML all decisions about the type of declaration and the type of parameters are made by direct assignments. Therefore declaration statements only require core memory at runtime in case of hardware or software variables because of the reservation of core memory. This kind of implementation offers the advantage of not requiring core memory reservation for variables in the host language.

• Detailed error checking at assembly time in order to protect a non-experienced user from non-recoverable errors at runtime. A very detailed error check is made to detect syntactical and semantic errors—as far as possible within assembly time. The assembler error directive with error messages has been applied within conditional assemblies.

 Modular programming for easy portability of IML to other CAMAC controllers.

The modular programming provides an easy portability of IML to other CAMAC controllers. Only some of the modules related to the hardware of the appropriate controller have to be changed, e.g. the address calculation.

#### LAM-HANDLING

The same LAM handling has been chosen for the two controllers:

Under the DOS operating system a LAM is decoded to a corresponding station number (N), and a branch to the appropriate interrupt service routine is performed. The assignment of a LAM to a station number is done by hardware in the BORER type 1533A controller and by software if the DEC CA-11A controller is used.

Under the operating system RSX-11D the LAM handling is performed as a separate task. In the event of a LAM the CPU traps into this separate task, which in case of the CA-11A controller assigns the LAM to a corresponding station number. A significant event is indicated by coded system eventflags. The user program must contain for each LAM a program sequence (e.g. a task) which is in a waiting condition for a significant event.

#### **CONCLUDING REMARKS**

The use of IML statements is not only restricted to assembler programs. For problems which can be solved by FORTRAN, the linkage from FORTRAN to assembler programs can be performed via the FORTRAN subroutine call. The implemented IML macros form a macro library which has to be declared in the command input string of the PDP-11 macro assembler<sup>5</sup>; this means that the whole IML program using assembler as host language is translated into object code in one step by the PDP-11 macro assembler.

A subset of IML can be easily achieved by eliminating from the macro library those macros which are not required by a specific application. The first implementation for the DEC CA-11A controller was completed by two men within four months. Due to the above mentioned features of the implementation the same two persons were able to implement Macro-IML for the BORER type 1533A controller within two weeks.

A manual describing the implementations more in detail is in preparation<sup>6</sup>.

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- 2. PDP-11 Processor Handbook 11/20, 11/40/11/45.
- 3. DEC CA-11A Controller Manual, Reading, England.
- PDP-11/CAMAC Crate Controller Type 1533A, BORER Electronics AG, Solothurn 2, Switzerland
- DEC PDP-11 MACRO Assembler Manual. DOS: DEC-11-OMACA-BrC. RSX: DEC-11-OXDMA-A-D.
- 6. Macro-IML Manual for DEC PDP-11 Computer with Controllers, DEC CA 11-A/BORER Type 1533A, M. Kubitz, R. Kind, HMI-B168, March 1975 Hahn Meitner Institut für Kernforschung Berlin GmbH.



### CAMAC WITH FORTRAN ON A CDC 3100 an approach based on IML

by

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Received 27th February 1975

SUMMARY This paper describes a straight-forward approach for using CAMAC with FORTRAN on a CDC 3100 computer. The solution is based on IML and consists of only four assembler subroutines and a LAM handler. It can be regarded as a high level expansion of an earlier implementation of IML in an assembler language environment.

#### INTRODUCTION

Since a language like FORTRAN is mainly intended for arithmetical operations, some problems arise when FORTRAN is used in a real-time environment like CAMAC. However, FORTRAN is widely known and used; therefore it is desirable to have tools in FORTRAN for handling CAMAC at this language level.

How to solve the various problems depends strongly on the facilities of the FORTRAN in use. An implementation of CAMAC in FORTRAN can be solved very conveniently by subroutines or function calls<sup>4,5</sup>.

#### THE MAIN PROBLEM

One of the main characteristics of FORTRAN is that its level is very far from that of the machine language. The reason for this is to reduce error possibilities. In assembly-language the programmer controls the flow of the program directly by

'labeling' the statements, and has tools to transfer labels from one subroutine to another. Moreover it is possible to return directly from subroutines to these labels.

Two typical examples of this problem in CAMAC are the Q-response and LAM-handling. These can be described in terms of IML<sup>1</sup>:

#### O-response:

SJQ READ MODUL DATA YLABEL SJNQ READ MODUL DATA NLABEL

LAM-handling:

#### ENL ALAM IRSERV UBL READ MODUL BUFFER CHANNEL BLAM

The meaning in the first case is that, depending on the state of Q, control goes either to the statement labeled by the jump address (to YLABEL if Q=1 for SJQ and to NLABEL if Q=0 for SJNQ), or to the statement following the SJQ or SJNQ. In the second case, the ENL statement establishes a connection between a GL-number defined by a LAM declaration and an interrupt service routine (IRSERV).

A LAM is declared by using names. A LAMname has an associated GL-number. CAMAC operations can be triggered by a LAM, and the CAMAC operations are performed, for example, by an interrupt service routine. Therefore for proper execution the GL-number must be connected to an interrupt service routine. This can be done at programming time by linking a LAM to an interrupt service routine. In the UBL instruction it is recommended that this connection is done implicitly. This means that the UBL instruction involves a special interrupt service routine, e.g. one single

CAMAC operation.

These tools are normally not available in FORTRAN because it merely contains the various GOTO's, the CALL SUBROUTINE and the RETURN for controlling the program flow. In various FORTRAN implementations it is not possible to transfer 'statement numbers' (the 'labels' and their runtime representation, an address) or at least to load the runtime representation of statement numbers into a FORTRAN variable and to transfer them into the subroutine. This is also true for the FORTRAN available on the CDC 3100<sup>3</sup>.

### SUBROUTINES AND FUNCTIONS FOR CAMAC

On the basis of IML, a straightforward solution for using CAMAC in FORTRAN has been implemented for the IAK II Cyclotron, using a CDC 3100 computer. We have implemented the Q-response as an integer variable holding the state of Q, and the interrupt service routine as an external subroutine address variable. The mnemonics of these routines are similar to the IML keywords used in the assembler implementation<sup>2</sup>, since our users are quite familiar with these names.

The four basic subroutines are:

- Declare a CAMAC address
   FUNCTION LOCD(C,N,A)
   e.g.: MODUL=LOCD(1,15,0)
- Perform a single CAMAC Operation
   SUBROUTINE SA(F,MODUL, [IDATA], [IQ])
   e.g.: CALL SA(0,MODUL,ID,IQ)
   IF(IQ.EQ.1)GOTO 100
- Declare a LAM

  FUNCTION LOCLA(C,N,A,[GL])

  FUNCTION LOCLI(C,N,BIT,[GL])

  e.g.: ALAM = LOCLA(1,15,0,1)

  ALAM = LOCLI(1,15,8,1)
- Link LAM to subroutine

  SUBROUTINE LINK(LAM, SUBROUTINE)

  e.g.: EXTERNAL IRSERV

  CALL LINK(ALAM, IRSERV)

#### **Parameters**

C,N,A – integer constants or variables containing the C,N,A-values.

MODUL - name of the station declared by LOCD. IDATA - internal computer reference address for data.

IQ – integer variable for Q-response.
GL – integer variable for GL-number.

BIT – integer constant or variable for the bitposition<sup>1</sup>.

ALAM – real variable for the LAM-declarations. IRSERV – subroutine where the control has to go when a ALAM arises.

denotes optional parameters.

#### LAM HANDLING

There are three steps involved in LAM handling: declaring a LAM, enabling/disabling a LAM, and linking a LAM to an interrupt service routine.

#### Declaration

A LAM is declared by one of the LAM declaration functions which defines its hardware reference. In the case of LAM-A the subaddress A is given, in the LAM-I case the bit-position of the LAM mask is given. The reference of the GL number depends strongly on the LAM grader in use. In our case the GL number causing interrupts is identical with the crate number. Therefore these GL numbers need not be specified. The remaining GLs must be indicated in the calls because they are hardwired for handling autonomous transfers.

#### Enable/Disable

This is a single CAMAC operation which can be done by a call to SA. In Fig. 1 an example is given for declaring and enabling a LAM of LAM-I type

INTEGER ILAM(2)
FEAL LAM
EXTERNAL IRSERV
EQUIVALENCE (ILAM(1), LAM)

CALL LINK(LAM, IRSERV)
CALL SA( 19, ILAM( 1), ILAM( 2), IQ)

RETURN END

SUBFCUTINE IRSERV

LAM= LCCLI(1,15,8)

CALL SA( · · · )

RETURN END

Fig. 1 Example of LAM-Handling in FORTRAN with LOCLI and LINK

with C=1, N=15, A=13 and BIT=8 (the mask bit for bit 8 of the LAM status register). ILAM(1) represents the LAM address and ILAM(2) its LAM mask.

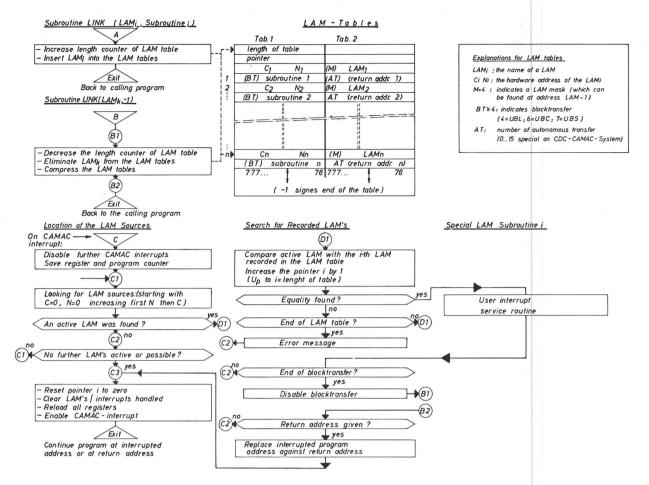


Fig. 2 Block Diagram of the LAM Handler for a Control Data 3100 Computer

#### Linking a LAM

The subroutine LINK enters all the relevant items into the LAM table of the LAM handler (Fig. 2). In the normal case these are the LAM address and the address of the subroutine to be linked to: whereas, for example for the LAM-I type additional information for the LAM mask is made available to the LAM handler via the LOCLI function. Since the length of the table of active LAMs is fixed, provisions have been made to dislink a LAM by a special call (CALL LINK(ALAM, -1)). The dislink call results in removing the LAM name and compressing the LAM table.

#### LAM handler

The LAM handler (Fig. 2) was designed for IML-assembler level<sup>2</sup> and therefore contains some additional facilities which are not used in this implementation. The LAM handler consists of three parts connected by the LAM table. These are the 'link- and dislink subroutine', the 'location subroutine' and the 'search subroutine', The location part traces the CAMAC interrupt back to the LAM source. The detection of each LAM source leads then to the search part where the linked LAM subroutine should be found and entered. The exit from this user—subroutine must always return the same way that the subroutine was entered. The LAM service is done in LIFO manner (last in first out).

#### CONCLUSIONS

The main features of this approach are ease of learning and ease of implementation. Moreover, no change in the former assembler implementation was necessary. Also it can be understood as an alternative to a complex cross-referenced subroutine system<sup>5</sup>. The time to implement these subroutines was only a few days, inclusive of testing and documentation.

The authors are indebted to the ESONE SWG Group for the 'Definition of IML' which is an excellent implementation guide describing all features of the CAMAC System from the software point of view.

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- 1. CAMAC. The Definition of IML. A Language for Use in CAMAC Systems. ESONE Committee, ESONE/IML/01 (1974).
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### IDEAS AND TECHNIQUES



### FASTER ADDRESS-SCAN BY READING ONLY NON-ZERO DATA

by

E. V. Chernykh, J. I. Chmielewski, V. A. Smirnov

Joint Institute for Nuclear Research, Dubna, USSR Received 4th April 1975

SUMMARY A 'floating sub-address' technique is suggested. This speeds up the address scan mode by reading only the non-zero data registers in CAMAC modules. Implementations are described for modules with less than 16, and 16 or more, data registers.

In address scan mode the CAMAC address of each register is calculated on a cycle-by-cycle basis, depending on the Q-response of the previous cycle. The registers accessed sequentially within the module must have consecutive sub-addresses starting with A(0), and the module must generate the appropriate Q responses.

In some applications a significant time-saving is possible by reading only those registers that have been filled with data, and ignoring those that contain zero data. The following solution is proposed to achieve this. Every data register in the module has a corresponding LAM-trigger (Fig. 1), where LAM<sub>i</sub>=1 indicates that register i contains non-zero data. All these LAM requests are ORed to the Lline. During the address scan the module responds first to the command N.A(0).F(Read) by setting Q=1 if L=1, and by transferring via the R-lines a demand-status word indicating the pattern of LAM requests in the module. Then, in response to subsequent commands N[A(1)+A(2)+...A(K)]. F(Read), where  $K \leq 15$ , the module sets Q=1 if L=1 and transfers data from a non-zero register i to the Rlines. During this cycle the LAM<sub>i</sub> trigger is reset. The controller increments the sub-address, but the next cycle reads the next non-zero register j, irrespective of its actual sub-address. Finally, when all the LAM triggers have been cleared and L=0, the

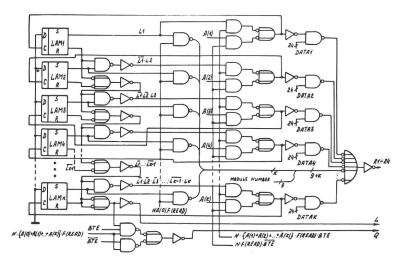


Fig. 1 The floating Sub-Address Logic in the Module with the Number of Sub-Addresses  $\leq$  15

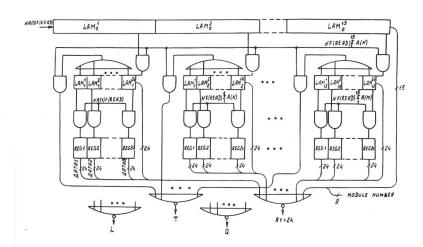


Fig. 2 The floating Sub-Address Logic in the Module with the Number of Sub-Addresses  $\geq 16$ 

module responds to the next command with Q=0 and the address scan within the module terminates

in the usual way.

Although the controller generates the usual sequence of consecutive sub-addresses, the registers in the module are not accessed at fixed sub-addresses. This is why the method is described as using 'floating sub-addresses'. The demand-status word provides the link between the data words and the true sub-addresses of the registers, and also includes a previously-assigned module number. The solution in this form does not allow a module to have more than 15 registers.

One can see from Fig. 1 that normal programmed access to a register is possible by changing the state

of the trigger BTE.

By using a special signal (let us call it T) transmitted via one of the Free-Use Dataway bus-lines to the controller it is possible to extend the solution to a module containing 360 registers, arranged as 15 groups of 24 registers. The block diagram of such a module is shown in Fig. 2.

Each group of 24 registers has a 24-bit demand-

status register LAM<sub>i</sub>, indicating the state of the registers in the group. There is also a 15-bit overall demand-status register LAM<sub>0</sub> indicating the state of the 15 groups.

When reading the data registers within a group the T-signal inhibits the incrementing of the sub-

address if A < 15 and Q = 1.

During the first cycle, with A(0), the LAM<sub>0</sub> register is read. The module generates T=0, and a sub-address increment is allowed. During the second cycle, with A(1) the LAM<sub>i</sub> register in the first non-zero group is read. The module generates T=1 in this and subsequent operations on this group of registers to inhibit the sub-address increment. During the following operations, still with A(1), the contents of the non-zero registers in group i are read, and the corresponding bits of LAM<sub>i</sub> are reset. When all the bits of LAM, have been reset the T-signal becomes zero, and the sub-address is incremented. After that, the process is repeated with A(2) in order to read the demand status LAM<sub>i</sub> of the next non-zero group, and the contents of the non-zero registers in the group.



#### A RARELY-USED APPLICATION OF THE X-LINE

by

L. Stanchi and I. Török\*

\*On leave from Institute of Nuclear Research of the Hungarian Academy of Sciences, Debrecen, Hungary Received 16th January 1975

SUMMARY The attention of CAMAC interface module designers is drawn to a simple method of indicating that a peripheral is unpowered or disconnected, by using the Command Accepted (X) line.

cation method is not given explicitly in EUR 4100e (1972). The cited literature<sup>2,3</sup> sets examples for the use of this possibility.

Some designers of CAMAC modules use only the simple OR-ed NAF signals for generating the X signal, even if the module interfaces a peripheral to the Dataway (e.g. Ref. 1). This arrangement does not indicate if the peripheral is disconnected or unpowered. In most cases, it is easy to generate in the module, from one of the power supply voltages of the peripheral, a signal which is logic '1' when the peripheral is connected to the module and is powered. An AND connection of this signal with the overall X, or with that part of X signal generated from the NAF signals that handle the peripheral, is enough to produce an X=0 in the case of a disconnected or unpowered peripheral. This useful indi-

#### REFERENCES

1. Vanuxem, J.P., APD/R7912 Controller, Interface between Textronix Waveform Digitizers and CAMAC Dataway, Type 161. CERN CAMAC Note 51-00, Feb. 1974.

 Instruction Manual for the Waveform Digitizer Interface Type DIF 1, for Biomation Type 8100. CCR Euratom, Ispra, Elettronica. To be

published.

3. Nanni, F., Verweij, H., REM.CTR, Interface between Remote Controlled Units and CA-MAC Dataway, Type 077. CERN CAMAC Note 54-00, Oct. 1974.

# ESONE-NIM COMMITTEES ACTIVITIES OF THE CAMAC WORKING GROUPS

The ESONE Committee in Europe and the U.S.AEC NIM Committee in America have both authorised different working groups to investigate specific aspects of CAMAC. The European and American working parties are performing their activities in close collaboration.

**ESONE-CAMAC WORKING GROUPS** 

During a joint session of the Dataway and Software Working Groups, at the time of their last meeting (KFA Jülich, June 1–5, 1975), it was agreed to organize two new, systems oriented working parties. One group will be concerned with remote intelligence of systems for which modern concepts are initiated by the availability of new semiconductor devices like microprocessors and RAM's.

The other Group will consider the possibilities of common agreements for systems with serial drivers

#### **Dataway Working Group**

It is expected that under favourable conditions a final chaft of the Serial Highway Specifications will be available at the time of the next Annual General Assembly of the ESONE Committee (November 5–7, 1975).

#### **Software Working Group**

A real-time extension of BASIC, RT BASIC FOR CAMAC, has been elaborated by members of the Group and was accepted by the Group. It is planned to present a description inclusive semantic and

syntactic definitions together with an implementation for the PDP-11 at the CAMAC Symposium in Brussels, October 14–16, 1975.

#### Information Working Group

In addition to the current work of preparation of the contents for the next issue of the CAMAC Bulletin, the Working Group has considered, at its last meeting in April 1975, three main topics:

- 1. Topic-oriented issues of the Bulletin.
- 2. How to make available, in different languages, the more important contributed articles.
- 3. The various possible methods for continuing the work of the Bulletin should the Commission of the European Communities decrease its support of the present Bulletin beyond 1975.

#### NIM-CAMAC WORKING GROUPS

The U.S. NIM Committee Dataway and Software Working Groups met March 24–28 at Florida State University in Tallahassee to consider the text of a document describing recommended block-transfer modes. An acceptable presentation of this information is being developed. The NSWG discussed some proposed clarifications to the IML report, considered a proposed implementation of IML in BASIC, and discussed further the organization and content of the proposed CAMAC Software Handbook.

The next NIM Working Group meetings are scheduled to be held at the National Bureau of Standards in Boulder, Colorado the week of July 21, 1975.

### **ESONE ANNOUNCEMENTS**

#### **ESONE COMMITTEE ANNUAL GENERAL ASSEMBLY, 1975**

The assembly will be held from November 5th to 7th, 1975 at Research Establishment Risö, Denmark. The agenda will include:

- Future activities in agreement with the needs of the member laboratories;
- Activity reports from the working groups;
- ESONÉ organization;
- Further developments of CAMAC;
- Activities of member laboratories;
- Relations between ESONE and ECA, IEC, and Purdue Europe.

The organization of the assembly is being carried out by the Risö Establishment and the address for correspondence will be:

Research Establishment Risö

Electronics Dept.

DK-4000 Roskilde

Denmark

Telephone 03-355101, ext. 347

Telex 43116

Contact: P. Skaarup

#### **ESONE-NIM COMMITTEES**

#### **HOW TO CONTACT CAMAC WORKING GROUPS**

Everybody who is interested in further information on the activities of the CAMAC Working Groups or who would like to obtain advice for the application of CAMAC specifications is invited

to contact the appropriate chairman or secretary of the existing working groups. The corresponding addresses are given below.

#### **ESONE-CAMAC WORKING GROUPS**

#### **Dataway Working Group (EDWG)**

*Chairman:* R. Patzelt, Technische Hochschule Wien, 1040 - Wien, Gusshausstr. 21, Austria.

Secretaries: R. C. M. Barnes and I. N. Hooton, both of Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Oxfordshire OX11ORA, England.

#### Software Working Group (ESWG)

Chairman: I. N. Hooton, see above.

Secretary: A. Lewis, Electronics and Applied Physics Div., AERE Harwell, Didcot, Oxfordshire OX110RA England.

#### **Analogue Signals Working Group (EAWG)**

Chairman: Th. Friese, Hahn-Meitner-Institut für Kernforschung Berlin GmbH, 1 Berlin 39, Glienickerstr. 100, Germany.

#### Mechanics Working Group (EMWG)

Chairman: F.H. Hale, Electronics and Applied Physics Div., Building 347.2, AERE Harwell, Didcot, Oxfordshire OX11ORA, England.

#### Information Working Group (EIWG)

Chairman: H. Meyer, CBNM EURATOM, Steenweg naar Retie, 2440 Geel, Belgium.

#### **NIM-CAMAC WORKING GROUPS**

#### **Dataway Working Group (NDWG)**

Chairman: F.A. Kirsten, Lawrence Berkeley Laboratory, University of California, Berkeley, Cal. 94720, U.S.A.

Secretary: R.J. Martin, FNAL, P.O. Box 500, Batavia, Illinois 60510, U.S.A.

#### Serial Systems Sub-group

Chairman: D.R. Machen, Los Alamos Scientific Laboratory, University of California, LAMPF/MP-1, Los Alamos, New Mexico 87544, U.S.A.

### Block Transfers Sub-group (joint with NSWG)

Chairman: E.J. Barsotti, FNAL, P.O. Box 500, Batavia, Illinois 60510, U.S.A.

#### Systems Compatibility Sub-group

Chairman: D. Horelick, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

#### Software Working Group (NSWG)

Chairman: R.F. Thomas, Jr., Los Alamos Scientific Laboratory, Los Alamos, New Mexico 87544, U.S.A.

Secretary: W.K. Dawson, University of Alberta, Dept. of Physics, Edmonton, Alberta, Canada.

### Mechanical and Power Supplies Working Group (NMWG)

Chairman: L.J. Wagner, Lawrence Berkeley Laboratory, University of California, Berkeley, California 94720, U.S.A.

### Analogue Signals Working Group (NAWG)

Chairman: D.I. Porat, Stanford Linear Accelerator Center, Stanford University, P.O. Box 4349, Stanford, California 94305, U.S.A.

### MEMBERSHIP OF THE ESONE COMMITTEE

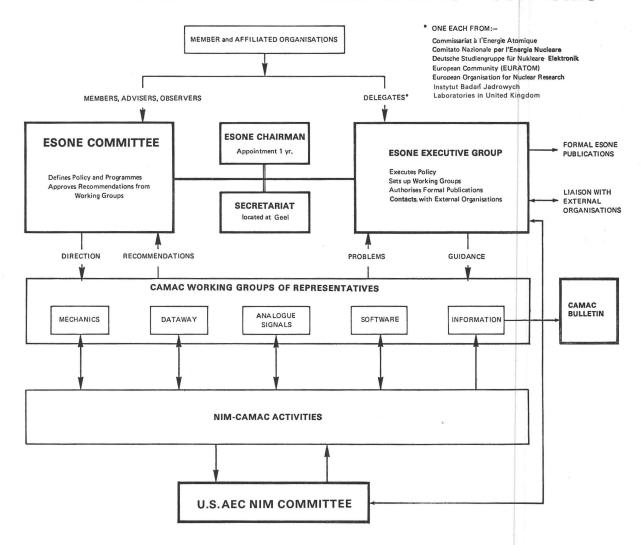
This list shows the member organisations and their nominated representatives on the ESONE Committee. Members of the Executive Group are indicated thus\*.

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International	European Organization for Nuclear Research (CERN)	F. Iselin*	Genève, Suisse		
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	Centro Informazioni Studi Esperienze	G. Perna	Milano		
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Netherlands	Reactor Centrum Nederland	A.T. Overtoom	Petten		
	Instituut voor Kernphysisch Onderzoek	E. Kwakkel	Amsterdam		
Poland	Instytut Badan Jadrowych	R. Trechciński*	Swierk K/Otwocka		
Romania	Institutul de Fizica Atomica	M. Patrutescu	Bucaresti		
Sweden	Aktiebolaget Atomenergi Studsvik	Per Gunnar Sjölin	Nyköping		
Switzerland	Schweizerische Koordinationstelle für die Zu-	H.R. Hidber	Basel		
	sammenarbeit auf dem Gebiet der Elektronik				
Yugoslavia	Boris Kidric Institute of Nuclear Sciences	M. Vojinovic	Vinča Belgrade		
Affiliated Labor					
Canada	TRIUMF Project, University of British Columbia	W V D	T.1		
	Simon Fraser University, University of Victoria,	W.K. Dawson	Edmonton		
University of Alberta  German Dem. Rep.					
German Deni. I	Akademie der Wissenschaften	I Lingartat	Berlin		
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### **ESONE ORGANIZATION AND CAMAC ACTIVITIES**



### **NEW PRODUCTS**

# DATA MODULES (I/O Transfers and Processing)

#### **Digital Serial Input Modules**

Ref. No. 13.0101 200-MHz 24-Bit Quad Scaler



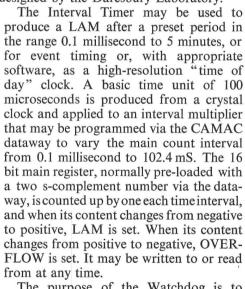
The Ortec S424F is a high-performance 24-bit quad scaler with a typical operating speed of 220 MHz and guaranteed continuous operation at 200 MHz. It is software-interchangeable with the Ortec S424B 150-MHz quad scaler and the Ortec S424S 50-MHz positive/negative input quad scaler. The S424F has a high-impedance bridging inhibit input circuit that will not increment the scaler. Its data inputs are protected against  $\pm$ 50V fast transients ( $\leq 1\,\mu$ sec/sec). Many options for overflow detection are provided utilizing the module's fully CAMAC-compatible LAM structure.

Ref. Ortec Inc.

#### **Digital Output Modules**

#### Ref. No. 13.0102 Interval Timer/Watchdog

The functions of Interval Timer and System Watchdog are combined in this single-width module Type EC384, designed by the Daresbury Laboratory.



The purpose of the Watchdog is to permit remote monitoring of the continuing operation of a CAMAC system; the output can drive a "system OK" LED

indicator, or other equipment via twisted pair cable. When enabled, the Watchdog monitors the use of the Interval Timer. If no reference is made to the Timer or the Watchdog in the selected period, or if power to the crate fails, an alarm signal is generated and is available at the front panel. A switch in the module (accessible only when the side cover is removed) enables the period to be set to 1, 2, 5, 10, 20, 50 or 100 seconds. Timing of the period is restarted each time a valid command is received by the module.

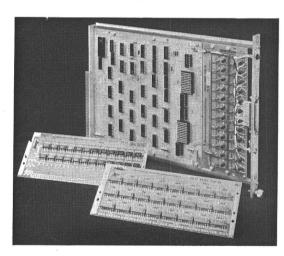
If a particular application does not require both facilities the Timer only or the Watchdog only may be used.

Ref. Sension Ltd.

### Ref. No. 13.0103 Output Register/Driver Modules

This 9600 family of CAMAC Output Register/Driver modules is derived from the basic module 9600. The basic unit has a maximum capacity of 24 Bits which can be Loaded, Read or Incremented as one word or as three 8-bit bytes. Integrated circuit sockets are provided on the output lines so that any pin compatible device can be used as a buffer. Driver outputs to the front panel socket are by means of links or optional sub assembly printed circuit cards.

Certain versions of the add on printed circuit card are listed as standard but many other configurations are possible and can be supplied to order of fitted subsequently by the user. This concept permits a system designer to drive peripheral devices by a tailor made approach and the standard versions offer the module user a useful range of software compatible driver concepts.



The add on standard option cards are coded by the two least significant digits and a letter of the module type number as follows.

9600A Output from totem pole 16 mA 5 V
 9600B Output from free collector 40 mA 30 V
 9600C Inverted output from free collector 40 mA 30 V
 9601 Output from free collector 1 AMP 60 V

9602A Relay contact closure multiplexer concept

9602B Relay contact closure free contact pairs 9603 Optical coupled outputs 7 mA.

#### **Applications**

1. Peripheral Driver.

2. Temporary Storage Register.

3. Preset Counting Register 24 Bits 50 MHZ.

4. Serial Parallel Converter.

Ref. Nuclear Enterprises Ltd.

#### Ref. No. 13.0104

#### **Eight-Bit Latched Triac Output Register**



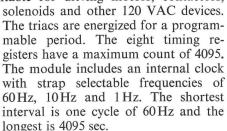
The model LT contains eight Triac switches in a single width CAMAC module. Each channel is identical and capable of switching inductive as well as resistive loads. The Triac switches can be opened or closed simultaneously or independently under program control. The outputs are triggered at zero voltage to minimize noise transients. To simplify wiring, each output has only two wires. Line voltage is sensed across the open triac to determine zero voltage. Each channel is floating and optically isolated. The outputs are normally opened but are available normally closed as an option. All outputs may be disabled from the Dataway. When logic power is first applied to the module, all the outputs are reset causing the output to open thus avoiding accidental trigger of any output devices attached.

#### Ref. Joerger Enterprises, Inc.

#### Ref. No. 13.0105

#### 8 Channel, Timed Triac Output

Kinetic Systems' Model 3040 is a double width CAMAC module that provides eight individually isolated triac output circuits. The triacs are particularly suitable for driving motors, contactors,



Each of the eight triac output circuits is a floating two-wire 'switch' which is connected to the AC source and load in the same manner as a relay contact. Each output can switch 120 VAC to loads of 2A each (5A inrush) and is capable of withstanding 200V of common mode voltage. The output circuits are optically isolated from the control logic and feature zero crossing detectors to prevent turn-on except near zero voltage. This reduces RFI and minimizes crosstalk into logic circuits. The output circuits are individually fused

and isolated from each other, increasing their versatility. The output circuits are of the 'Normally Open' type (i.e. open when there is a zero in the register). The output circuit includes transient and over voltage protection.

#### Ref. Kinetic Systems Corporation

### Digital I/O, Peripheral and Instrumentation Interfacing Modules

#### Ref. No. 13.0106

#### **CAMAC Disc System**

The system, Type (9)370, consists of two units.

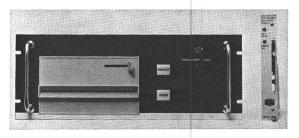
- (1) A 7" rack mounting chassis incorporating the CDS 110 Disc Drive and all the electronics for track and sector selection and serialisation from the parallel 8 Bit input, plus all the necessary power supplies.
- (2) A CAMAC module containing the Mode and Address register, Status register and connecting cable to the main unit.

The 'Floppy Disc' system provides a very rapid buffer storage for 1.4 million bits of information or program, and can provide a very attractive replacement for paper tape readers and punches, or even card systems where they are used for input/output to small computers with a CAMAC highway.

The system is designed to look like a paper tape punch and reader in that parallel 8 bit Words are the means of data transfer. These, of course, may be ASC11 or Binary data, and no great program changes are required to take system.

#### Disc Cartridge

The recording medium is a flexible, mylar, 7.5 ins diameter, oxide coated disc which is jacketed in a  $8.0 \text{ ins} \times 8.0 \text{ ins}$  envelope. A 1,25 ins recording



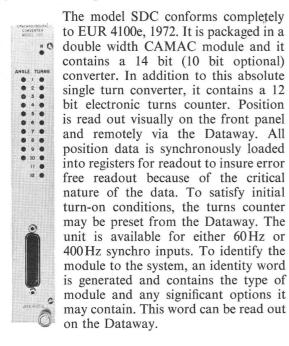
band containing up to 64 tracks is located in the most stable area of the disc and is accessible through an aperture in the envelope. The index and eight sector holes located on the periphery of the mylar disc are photo-electrically detected through another aperture in the envelope. A third aperture in the envelope is used for write protection.

#### Data Transfer

The data is recorded on and read from one side of the disc serially at 33.8 K bits per second via write data and read data lines interfaced to the CAMAC dataway.

#### Ref. Nuclear Enterprises Ltd.

#### Synchro-To-Digital Converter



Ref. Joerger Enterprises, Inc.

Ref. No. 13.0108

#### **Stepping Motor Controller and Driver**

The model SMC is a self-contained stepping motor controller and driver all housed in a single width

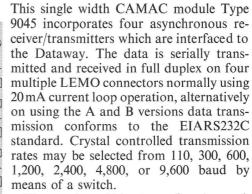
CAMAC module. It features an adjustable, linear acceleration and deceleration to provide an efficient method of driving high torque loads at their maximum speed. This maximum speed is adjustable from 50 pps to 2000 pps. The four drivers are capable of switching up to 2A per phase at a maximum of 28V. All components required to drive this load are internal with the exception of the current limiting resistors which are determined in each application by the motor voltage and current. Three external, high level logic inputs are used to test the status of the system, a clockwise limit, counter-clockwise limit and a signal that indicates power is being applied to the motor. Logic is provided that will inhibit the driver if a limit signal is received and the motor is requested to step in that direction. The number of steps is determined by a 16-bit command word that is in two's compliment. Bit 16 determines direction

and the remaining 15 bits contain the number of steps to be performed.

Ref. Joerger Enterprises, Inc.

#### Ref. No. 13.0109

#### **Quad Terminal Interface**



The number of bits, type of purity used, and number of stop bits may be selected by internal links. The standard module is provided with no links set, to give a mode op operation defined as no parity, 2 stop bits, 8 bits per character.

A comprehensive multiple LAM structure is incorporated and is designed to be compatible with other modules under development in this range.

The front panel is provided with four single pole LEMO sockets on which error signals are generated.

This module will find application in interfacing remote keyboard/display terminals to computer systems.

Power requirements +6, -6, +24, -24 volt.

Ref. Nuclear Enterprises Ltd.

#### Ref. No. 13.0110

#### Serial Input/Output register

This single width CAMAC module is capable of independent input and output 16 Bit serial transfers via front panel connectors. Data transmission

including handshake is made on a single twisted pair cable with transformer isolation at each end. This type of transmission permits high common mode rejection of 80dB plus.

After initialization by CAMAC command the output section of the module sets up a continuous handshake dialogue, each  $20 \mu S$ , with the external equipment to ensure that it is ready to receive data. Data written by F(16) to the shift register is coded and clocked onto the output line at a 1 MHz rate. A device 'NOT READY' handshake is then sent every  $20 \mu S$  until the device becomes ready again. This change of handshake state can be used to raise a LAM demand for new data. The external device could be another 9063 located in a remote crate, using this configuration data transmission of up to 17K by 16 bit words per second over 300 metres distance on a single twisted pair cable can be achieved.

The input and output sections of the module may be operated independently of each other. Status registers are provided to monitor the exact status of the CAMAC module and remote device.

Front panel LED indicators flash each time a transfer occurs. The fault condition is available at a rear panel connector.

Power requirements, +6, -6 V.

Ref. Nuclear Enterprises Ltd.

### Digital Handling and Processing Modules

#### Ref. No. 13.0111

5 + + + E \*O

#### 256-Word FIFO Buffer

Kinetic Systems' Model 3841 is a single-width module that contains a First-In First-Out memory stack organized as 256, 24-bit words. The memory has two parts for both input and output. It may be loaded and dumped from the Dataway or under control of external signals. External connections

for loading and dumping data are made by way of two 31-way front-panel connectors. All external signals are single-ended TTL.

Reading and writing operations are independent: The module finds use in application where input or output data operations require a clock rate that is different from the data transfer rate in the CAMAC system. For example, to load the memory externally and read it from the Dataway or to load the memory from the Dataway and dump it externally. An input which sets a LAM source and a signal indicating the state of the LAM are provided on the external connectors to allow communication of 'ready' and 'done' status information.

Two 3841's may be interconnected to transfer data between two CAMAC systems. A control register is provided to establish direction of data flow in such applications.

'Memory-full' and 'Memory-empty' signals are provided externally and also function to set respective bits in the LAM

register. A LAM source is also provided which indicates when the memory is three-quarters full. A 5-bit Status register provides information on the current stack size in the memory.

In addition to the 4-bit LAM source register a LAM mask register is provided which can be selectively set and selectively cleared as well as written and cleared. The LAM register can be cleared and selectively cleared, and bit 16 can be selectively set.

Ref. Kinetic Systems Corporation

#### **Analogue Modules**

#### Ref. No. 13. 0112

#### Digital Voltmeter

This double width CAMAC Type CS0080 module will perform as a full digital-voltmeter, combining the majority of the features associated with the more conventional rack mounted instruments.

Results of analogue to digital conversions are presented to the front panel as a  $4\frac{1}{2}$  digit BCD number and this may be read out via the Dataway as a binary number or as a string of ASC11 characters with sign.

High common mode rejection is obtained using a differential amplifier with up to 2,000 Volt isolation. Series mode rejection is achieved using dual ramp techniques together with a phase locked loop synchronised to the mains frequency.

The user may select one of two ramp intervals; either 20 ms for high resolution or 2 ms for fast conversion with lower resolution. Five programmed ranges may be selected from  $\pm 19999 \, \text{mV}$  to  $\pm 1,999.9 \, \text{volt full scale}$ .

Zero and full scale calibration measurements may be controlled from the Dataway thus eliminating the need to wait until the warm up drift interval has finished and permits the user to compensate for temperature variations within the crate.

The DVM may be operated in two conversion modes; the first, free running, and the second conversion on command. In each case data will not be transferred into the read out buffer unless the 'LAM' flag has first been cleared. A LAM is generated when the conversion is complete. If the conversion overranges this may be checked using a test status command.

Power requirements 117 v AC,  $\pm 24$ V, +6V. Input connector 3 pole LEMO RAO303.

Ref. Nuclear Enterprises Ltd.

#### Ref. No. 13.0113

#### Fast-Conversion, Event-Buffered ADC

The LRS Model 2250 consists of 12 complete, 9-bit, analogue-to-digital converters in a single width CAMAC module. A common front panel gate signal defines the signal integration time and initiates a fast conversion requiring only 9 µsec. A 9-bit digital word from each of the 12-channels is transferred into a 32-event deep first-in-first-out (FIFO) memory which is especially useful at accelerators with many events per beam spill. The event rate capability is further enhanced by the ability to fast clear unwanted information in  $1 \mu sec.$ For application requiring a faster conversion, the 2250 can be modified for use as an 8-bit unit with 3.2  $\mu$ sec conversion time at the expense of reduced sensitivity (1 pC/count in linear mode, .25 pC/count minimum in inverse quadratic mode).

To satisfy ever-increasing needs for a large dynamic range in calorimetry, lead glass shower counters, proportional or drift chamber application or similar total energy absorption counters, the model 2250 offers an inverse quadratic response, which gives a dynamic range of 10<sup>4</sup> with a sensitivity of .125 pC per count for small signals and 1.75 pC per count for full scale signals. A normal linear response (0.5 pC/count) is also switch-selectably available. The inverse quadratic response gives a large dynamic range without the attendant large errors associated with logarithmic response at large pulse amplitudes.

CAMAC commands and responses: Z, C, I, Q, X, L.

CAMAC functions: F(0), F(2), F(9), F(25). Available: May 1975.

Ref. LeCroy Research Systems Corp.

#### Ref. No. 13.0114

#### 12-Channel Peak Sensing ADC

The Model 2259 is based largely on the design of the popular LRS Model 2249A Integrating ADC. It accepts 12 negative-going analogue inputs upon application of an externally-supplied gate signal and converts the highest voltage point in each pulse to a 10-bit digital number. Input full scale is set at -2V, giving a per count resolution of -2mV. The common gate signal must enclose the peak to be measured, and the analogue inputs themselves must be either DC or of a risetime  $>25\,\mathrm{nsec}$ .

The 10-bit conversion time of the 2259 is  $51.2\,\mu\text{sec}$  or, as a factory option,  $12.8\,\mu\text{sec}$  for an 8-bit conversion. To eliminate the necessity of delaying the analogue inputs while waiting for a slow event trigger, conversion may be started within  $1.5\,\mu\text{sec}$ 

by a front panel fast clear.

The Model 2259 is suitable for use with a variety of particle detectors in high energy physics research, including liquid Argon ionization chambers, NaI total absorption counters, and liquid or gas proportional chambers. DC voltage measurements for general system maintenance may also be appropriately entered into the system computer by use of the 2259. Such measurements include CAMAC or NIM supply voltages, magnet currents, temperatures, high voltage supplies and clearing field supplies.

Power consumption of the 2259 is low enough to permit the use of 23 modules in a single, 25-amp,

CAMAC crate.

CAMAC Commands and Responses: Z, C, I, Q, X, L.

CAMAC Function Codes: F(0), F(2), F(8), F(9), F(10), F(24), F(25), F(26). Available: May, 1975.

#### Ref. LeCroy Research Systems Corp.

Ref. No. 13. 0115 Octal ADC



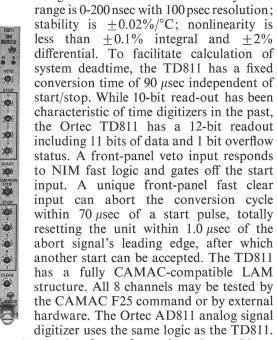
The Ortec AD811 comprises eight peakdetecting amplitude-to-digital converters connected to a common strobe and packaged in a single-width CAMAC module. It measures positive unipolar or bipolar signals ranging from 0 to  $>2.0\,V$  with a resolution of 1.0 mV and a full scale range of 2047 channels plus overflow. A unique front panel fast clear input can terminate the conversion of undesired events and reset the module within  $1.0 \mu sec$ ; to ensure acceptance of the clear input, CAMAC logic requires it to occur within the same conversion cycle (80 µsec after busy timer start). The AD811 has a fully CAMACcompatible LAM structure. All eight channels may be tested by CAMAC command F25. The Ortec AD811 ADC and TD811 TDC use identical logic and are therefore software interchangeable.

Ref. Ortec Inc.

Ref. No. 13.0116

#### 11-Bit Time Digitizer

The Ortec TD811 comprises 8 time to-digital converters coupled to a common start input and packaged in a single-width CAMAC module. Dynamic



Bot units are therefore software interchangeable.

Ref. Ortec Inc.

Ref. No. 13.0117

#### 96-Channel Drift Chamber Digitizer

The LRS Model 2770 is a double width CAMAC module designed to process signals from 96 Drift Chamber wires. Line-driven, ECL-compatible wire pulses are received differentially by the 2770 via inexpensive, field-proven, 34-conductor flat ribbon cables. The time between each wire pulse and the common event-defining trigger (delayed stop) is digitized to 8-bits in each of the 96 channels, giving a time resolution of 4nsec in its 1 µsec full scale range and 2nsec in its optional 500nsec range.

For each channel (of the 96) that contains

For each channel (of the 96) that contains digitized time data, an address encoding is done. This resultant address is stored along with the time information in a 16-bit, 40 deep first-in-first-out (FIFO) memory. Subsequent events are separated by 8 flag words (event separators) that are read out along with the actual wire data. Standard CAMAC readout from the memory can proceed asynchronous to data accumulation into the memory, and direct memory access (DMA) transfers can be accomplished also.

A significant feature of the 2770 is its ability to update itself with negligible deadtime (<20ns) each time a wire pulse is received. Time digitizing and encoding will only be performed on the last pulse on the wire to occur during the established full scale time interval. Double hits on a single wire can be monitored by dedicating two chambers to each plane, (which is typically done to remove left-right ambiguity), and provision is available via an accessory module for identifying and encoding multiplicities greater than 2.

CAMAC Commands and Responses: Z, C, Q,

X, L.

CAMAC Functions: F(0), F(2), F(9). Available: June, 1975.

Ref. LeCroy Research Systems Corp.

Ref. No. 13.0118

### 128-Channel Multiwire Proportional Chamber Encoder

The LRS Model 2720 is a double width CAMAC module designed to preprocess signals from 128 wires of a multiwire proportional chamber (MWPC).

The input to the Encoder module consists of eight 34-conductor flat ribbon cables connected to sockets on the printed circuit board. Each flat cable transmits 16 differential ECL levels to the 100 Ohm inputs.

Event selection is accomplished by strobing the pulses on the chamber wires with a fast (NIM level) coincidence gate signal. Wire 'hits' stored in primary registers are transferred to the secondary (or encoder) register in 100 nsec, permitting the acceptance of another event. 'Set' bits are then encoded as a series of 7-bit wire addresses which are stored in a 16-bit first-in-first-out (FIFO) memory capable of handling 80 8-bit half words. A special flag word signifies the end of each event.

The output memory may be read out asynchronous to the event rate as long as the FIFO memory is not full. Standard CAMAC commands including direct memory access (DMA) provisions may be used for readout.

The Model 2720 can be gated through CAMAC patch lines to inhibit the encoding and transfer after latching. In low rate situations, this procedure can eliminate the need for monostables or cable delays before latching. Alternately, the 2720 provides two optional front ends, one including a monostable delay where some lesser amount of deadtime can be tolerated, and one without any delay at a substantial cost savings, such that the user can provide cable delays for high rate situations.

Functions Used: F(0), F(2), F(9). Commands and responses: Z, C, Q, X, L. Available: June, 1975.

Ref. LeCroy Research Systems Corp.

#### Ref. No. 13.0119

#### Dual, Digital-to-Analog Converter



This double-width CAMAC module conforms fully to the EUR4100e, 1972 specifications. It contains two digitalto-analogue converters available with either 10-or 12-bit, resolution. The channel's register is loaded from the dataway with information from the write lines. An 'update' output is generated for each channel to indicate when it's converter has been updated. A visual update indication is also provided. The output range is switch selected internally. To verify the state of the module, the registers may be read out on the Dataway. The output range and the resolution of the converters is also included in this data word to provide a complete description of the analogue output signal being generated by that channel.

Ref. Joerger Enterprises, Inc.

Ref. No. 13.0120

#### Octal 8-bit DAC



This single-width CAMAC module (8 D/A) provides eight digital to analogue converters, each with 8-bit resolution. The output is a current from 0 to 2mA maximum. The maximum level is internally adjustable for each channel. Each channel contains an output buffer. The current output has been designed to be independent of line impedance. Each channel is loaded from the Dataway on command with data from the write lines. A lamp is provided for each channel to visually indicate when that channel is overwritten. An output signal is also provided for each channel when it has been overwritten. A test point is available to monitor each channel's output which is a voltage of 0 to  $+10\,\mathrm{V}$ . The module contains an identity word that may be read out to indicate the module's type.

Ref. Joerger Enterprises, Inc.

Ref. No. 13.0121

#### 12-Input Multiplexer

This unit, Type MX 2070, is identical to the MX 2025 (see, CAMAC Bulletin No 6), except that the reed relay switches of the 2025 have been replaced by FET's

CAMAC functions are the same as the MX 2025.

Specifications:

- FET unit switching.

Typical insulation between wires
 Switching time
 80 dB with three wires switching
 200 ns.

Signal range

- Input overloaded protection  $\overline{\text{diodes on } \pm 7\text{V}}$ .

+7V.

12 channels with almost unlimited cascading possibilities.

#### Ref. SEN Electronique

#### Ref. No. 13.0122

#### Wide-Band Router WBR 2073

Using wide-band relays to handle switching functions, this WBR 2073 single-width module is designed for analogue signal multiplexing in output mode (1 input, 12 outputs) and multiple analogue signal switching in input mode (12 inputs, 1 output).

Channel selection can be obtained in two ways: a Write instruction from the dataway loads the 12-bit selection register and any combination of the 12 channels can be selected in this way. Alternatively an increment instruction will give a channel by channel scan, and can be programmed to recycle.

All connections are made on the front panel via Lemo sockets and channel selection is timed by an internal clock and displayed by the associated LEDs.

Power Requirements:

+6V 700 mA +24V 80 mA

Ref. SEN Electronique

#### Ref. No. 13.0123

#### **Programmable Precision Attenuator**

This PPA 2071 is a 12-bit binary attenuator using an R/2R Ladder Network and reed relay switching. The attenuation value is selected by a dataway instruction which loads the 12-bit switch position register and the value is displayed by front panel LEDs. As the switching function is provided by reed relays an internal clock is used to define the positioning time.

The PPA 2071 is a single-width fully-shielded module with Lemo connectors on the front panel.

CMMR (2 wire system) <95dB.

Insulation:  $\pm 300 \text{ V DC-AC } 50 \text{ Hz}$ 

Max input signal

amplitude: 20 V.

Power Requirements

+6V  $700 \,\mathrm{mA}$ 

 $\pm 15 \text{V}$  50 mA (external power supply for common mode rejection).

#### Ref. SEN Electronique

### Other Digital and/or Analogue Modules

#### Ref. No. 13.0124

#### **CAMAC PROM Programmer**

The Sension PROM programmer is a double-width CAMAC module used to program (i.e. write data into) programmable read-only memories. The initial version is designed for programming the Intel 1602A, 1702A, 4702A, and 8702A PROM chips and other pin-compatible and electrically compatible PROMs. Versions will be available for other types of PROM.

The PROM to be programmed is mounted in a socket on the front panel. The Programmer is driven via the dataway and works under the control of suitable software in the crate control processor. Software is available for the S-800 and S-804 programmable crate controllers and can be supplied for other processors if required.

The module can be used to write and/or check the contents of PROM chips using data supplied from another device e.g. tape reader or teletype. Alternatively data can be read from a ROM or PROM chips and then copied to other PROM chips.

Ref. Sension Ltd.

#### SYSTEM CONTROL

## (Computer Couplers Controllers and Related Equipment)

### Interfaces/Drivers and Controllers (Parallel Mode)

#### Ref. No. 13.0201

#### Crate System Controller for PDP-8/E

For many small CAMAC systems (one crate) to be operated by mini-computers the typical configuration with Crate Controller Type A-1 and System Controller is more complex and expensive than would be required. Therefore a CAMAC Single Crate Controller has been developed as a crate controller that directly interfaces the Dataway to the Omnibus of a PDP-8/E computer. The module provides single word programmed transfers and block transfers, one channel is provided for single-cycle direct memory access transfers with the submodes 'Data to/from memory', 'Add data to memory' and 'Add one to memory'. Interleaved programmed and DMA transfers are permitted. In programmed operations the Controller has a full 24-bit data transfer capability. The word length for

autonomous transfers is 12-bit. The mode 'Addone-to-memory' allows the accumulation of spectra of 2K channels with a capacity of 24-bit per channel.

24 signals are connected through an OR-gate to the Interrupt Request line. These comprise the 22 LAM signals from the modules of which anyone may also be used as trigger signal for an autonomous transfer, a signal indicating 'End of block' for block transfers, and the overflow of a word counter in the Controller during autonomous transfers of data. The demand handling subsystem has a built-in priority order and gives fast access to the appropriate interrupt servicing routine on application of one special command.

This Controller Type, LEM 52/32.1 is a triple-width CAMAC unit. It is designed to be operated in the right-hand stations of the crate. The connection to PDP8/E buslines must not exceed 2 meters.

Ref. Eisenmann

Ref. No. 13.0202

### Crate System Controller for Microcomputer Micral

The JCMIC-10 Crate Controller, designed by CEN, Saclay, can be connected to each of the three MOCRAL versions, N, G or S. MICRAL is a  $3U \times 19''$  microcomputer based on Intel microprocessors (8008 for the N and G versions, 8080 for the S version) associated with RAM and REPROM memory and peripherals (TTY, Punch tape, Reades, floppy disk, display, etc.). Available software includes REPROM monitor, local assembler, basic interpreter, floating point subroutines, etc.)

JCMIC-10 is a double width module connected via 2 câbles to two 32 logical Input X 32 logical Output MICRAL cards. All CAMAC functions are performed, and LAMS are transmitted on two interrupt levels. An hexadecimal selector on the front panel associated with a LAM pushbutton allows the choice of one of 16 user's programms. 24 bit Read or Write CAMAC operations are (performed in 500, 250 or 50 ms respectively with MICRAL N, G or S. Distance between a CAMAC crate and MICRAL should not exceed 25 m.

The CAMAC timing being a programmed one, the JCMIC-10 controller may be connected to every type of computer having logical stored output with TTL-40 mA capability and logical TTL input.

Ref. R2E

Ref. No. 13.0203

#### **Programmable CAMAC Crate Controllers**

The S-800 and S-804 CAMAC Crate Controllers provide a computing capability directly within a

CAMAC crate. They act as fully autonomous programmed controllers, and, in many applications, can remove the need for an external computer. In other applications the controller can reduce the load on an external computer by carrying out data reduction and buffering. The basis of the controller is a complete micro-computer built around the Intel 8080 microprocessor chip.

With the S-800, communication with other processors and non-CAMAC devices is through normal CAMAC interface modules. The S-804 includes a universal asynchronous serial I/O port, by means of which it can communicate with a teletype, any other asynchronous terminal device, a conventional computer, or another S-804. An interesting possibility is to link a number of S-804s together through these ports, and have a serial highway system using the proposed CAMAC serial highway protocol but with normal asynchronous communication links.

The controller occupies the control station and one adjacent normal station, and is fully in accordance with EUR 4100e. The values sent to the N, A, F, W, Z, I and C lines are completely under program controls. The hardware latches the incoming values on the R, Q and X lines into registers at the appropriate time. The registers can be read as required by the processor. The L lines may be examined at any time by the processor. Also the presence of one or more L signals can optionally be allowed to cause an interrupt in the processor.

Ref. Sension Ltd.

#### Interfaces/Controllers/ Drivers for Serial Highway

Ref. No. 13.0204

### CAMAC Serial Highway Driver with Buffer Memory

Kinetic Systems' Model 3994 is a fivefold wide CAMAC module which transmits and receives messages on the CAMAC Serial Highway. The 3994 is designed for use with one or more FIFO buffer modules (Model 3841) to provide elastic buffering between the Dataway and the Serial Highway. Both bit-serial and byte-serial ports for serial messages are provided.

The 3994 can operate in programmed-transfer mode or in one of several block-transfer modes. Operation under programmed-transfer mode is identical to operation of Kinetic-Systems' Model 3992 Serial Driver module.

When operated in a block-transfer mode, serial messages (including data) or data are stacked in the FIFO from the Dataway, the serial messages are transmitted on the Serial Highway autonomously at a rate determined by the serial clock, and reply messages (including data) or data are stacked in the FIFO as serial messages are received. Reply messages and data stacked in the FIFO can be accessed by the Dataway for subsequent readout.



all transfers. whether programmed or block, SC, SN, SA and SF are provided to the serial transmitter in a 24-bit word. Serial write data is provided in another 24-bit word. The serial message is formatted by the 3994. Formatting includes generating a parity bit for each byte in the serial message, generating a SUM-byte, generating the correct number of SPACE-bytes, and automatically inserting WAIT-bytes between messages. As reply messages are received, reply status information and data, if present, are

stored in buffers for Dataway readout. A LAM-source indicates when a reply has been received.

The output clock can be controlled by crystal or by a variable frequency oscillator or from an external source. Means for selecting frequencies from 1 KHz to 5 MHz are provided for both the crystal-controlled and variable-frequency oscillators. The external source can range from arbitrarily slow to 5 MHz.

has four modes of The operation: MODE-A, MODE-B, MODE-C and MODE-D. Programmed transfers under direct control of the Dataway occur in MODE-A, and buffer registers provide communication between the Dataway and the Serial Highway. MODE-B, MODE-C MODE-D are block-transfers modes, and the FIFO buffer is used to provide an elastic link between the Dataway and Serial Highway. In MODE-B, two parameter registers provide the serial command information (SC, SN, SA and SF). Write data is taken from the FIFO (previously loaded from the Dataway), and read data is stored in the FIFO. In MODE-C messages, including data, are stacked in the FIFO for transmission in a predefined order; reply messages, including data, are stacked in the FIFO as they are received. A delimiter word separates commands from replies in the FIFO and halts the block transfer when it reaches the bottom of the stack. Reply messages are then next in line in the FIFO for Dataway readout. MODE-D is similar to MODE-C except that only the data from reply messages is stacked in the FIFO.

# Ref. Kinetic Systems Corporation

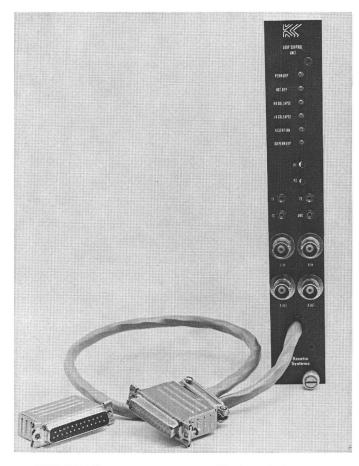
# Ref. No. 13.0205

# Serial Highway Loop Control Unit

Kinetic Systems' Model 3931 Loop Control Unit provides auxiliary loop control when used with a Type L-1 Serial Crate Controller such as the Model 3952 operated in bit serial mode. It fully complies with the specifications for U-port adapters in TID-26488. This module is a double-width unit.

The Model 3931 is intended to be used with coaxial cable such as RG-58U. A main highway (A loop) and a backup highway (B loop) are used. This provides redundancy in case the main highway is broken as well as allowing for special loop collapse features.

The serial highway input and output connections are isolated by transformers for high common mode rejection. This is necessary when the transient ground potential difference between adjacent crates on the serial highway exceeds approximately 10 V or very high electrostatic or magnetic fields couple into the serial highway. D-port (defined port from L-1 SCC clock and data are multiplexed in the 3931 using biphase modulation; this signal is coupled by a pulse transformer to the U-port (undefined port



per TID-26488) output connector. Clock and data are transmitted over a single circuit. The multiplexed signal from the previous crate is received via the U-port input connector and demultiplexed to form a separate clock and data signal for the D-port receivers in the L-1 SCC. The biphase signal is without dc component and can readily be coupled through transformers.

# Ref. Kinetic Systems Corporation

# Ref. No. 13.0206

# Type L-1 Serial Crate Controller

Kinetic Systems Model 3952 Type L-1 Serial Crate Controller meets or exceeds the requirements of *CAMAC Serial System Organization* (ESONE/SH/01-03, TID-26488) as amended. This controller is a double-width version of Kinetic Systems Model

3950. It is functionally equivalent to the 3950, that is currently in use at many facilities throughout the world. The 3952 uses the same proven printed circuit techniques used in all Kinetic Systems products. It is compatible with Kinetic Systems' full line of serial components, which includes serial system drivers, loop control units, LAM Graders, and autonomous controllers.

# Ref. Kinetic Systems Corporation

# Ref. No. 13.0207

# **Bit Serial Adapter**

Kinetic Systems Model 3932 Bit Serial Adapter is used with an L-1 Serial Crate Controller to provide transformer isolation of the data paths and loop bypass and loop collapse. It is also used with a serial driver containing the standard D Ports. The Bit Serial Adapter combines the clock and data from the U Port of the L-1 Crate Controller using biphase modulation. This combined signal is then transformer coupled onto a single data path to the next element on the serial highway. One Bit Serial Adapter can be used with a cluster of L-1 Crate Controllers that are interconnected by standard D Port cables. The Bit Serial Adapter provides the relays for bypass and loop collapse. These relays are controlled by the L-1 Crate Controller. The U Port serial highway can be twisted pair or coaxial cable. Several highway connector options are available. The Bit Serial Adapter is packaged in a single width CAMAC module.

# Ref. Kinetic Systems Corporation

# Ref. No. 13.0208

#### Serial Crate Controller:

The Serial Crate Controller, L-1, Model CR.6001 is an interfacing module between the CAMAC dataway (based on EUR 4100e specifications) and the Serial Highway Description in accordance with the ESONE documents SH/01 and SH/03 and latest revised papers issued by CERN.

The Controller provides a user selectable bit serial or byte serial mode of operation at a clock frequency of maximum 5 MHz. The Controller is a double-width unit.

Switches and led's on the front panel display the actual address and status of the Serial Crate Controller.

# Ref. Christian Rovsing A/S.

# **TEST EQUIPMENT**

# **Dataway Related Testers and Displays**

#### Ref. No. 13.0301

# **Dataway display**

This single-width CAMAC module, Type 9554, permits the signal lines of the Dataway to be displayed and memorised. It has three modes of operation; Follow, ON LINE, and Trigger.

In the *Follow Mode* the state of the Dataway lines is monitored continuously. This mode can be used to diagnose basic Dataway faults, to incidate errors presented on the Dataway by faulty modules and to immediately display the state of the Dataway when a control program halts.

The ON LINE MODE permits the signal lines of the Dataway to be monitored at time S1.

Trigger Mode. This mode is an extension of the ON LINE MODE. Register update occurs only in accordance with an external trigger input. In this mode the state of the Dataway lines is tracked while an external trigger is active (low) and memorised on the low/high transition. Thus the state of all lines is memorised at the instant defined by the user, possibly by patching the module under investigation to this trigger input.

A front panel reset switch clears all the registers. Power Requirements, +6V.

# Ref. Nuclear Enterprises Ltd.

# Index to Manufacturer's News and New Products

Borer Electronics AG News xi	LIV
Christian Rovsing A/S New Products	36
Eisenmann	33
Joerger Enterprises Incorporation New Products 28, 29,	32
Kinetic Systems Corporation New Products 28, 30, 34, 35, 3	36
News	10
LeCroy Research Systems Corporation New Products	32
Nuclear Enterprises Ltd New Products 27, 28, 29, 30,	36
Ortec Inc	31
R2E	34
SEN Electronique New Products	33
Sension Ltd New Products	34

# PAPER ABSTRACTS TRANSLATIONS

An optimized architecture for a multichannel pulse height analyser R. M. Keyser and R. H. Baldry

#### Summary

The architecture of multichannel analysers (MCA) has progressed from hardwired analysers to computer-based analysers. An architecture for the next generation MCA is based on a computer with CAMAC and a high-level interactive language.

#### Zusammenfassung

Die Struktur von Multikanal-Analysatoren (MCA) wurde von festverdrahteten zu rechnergestützten Analysatoren weiterentwickelt. Eine Struktur für die nächste MCA-Generation basiert auf einem Rechner mit CAMAC und einer hochentwickelten interaktiven Sprache.

#### Résumé

L'architecture des analyseurs multicanaux a évolué, passant des analyseurs en logique câblée à des analyseurs réalisés à partir d'ordinateurs. Une des architectures prévues pour la prochaine génération est basée sur un ordinateur associé à CAMAC et à un langage conversationnel évolué.

#### Riassunto

La struttura degli analizzatori multicanali (MCA) è evoluta dagli analizzatori a connessioni fisse agli analizzatori abbinati a un calcolatore. L'architettura delle prossima generazione di analizzatori multicanali è basata su un calcolatore associato al CAMAC e su un linguaggio interattivo ad alto livello.

#### Samenvatting

Meerkanaalsanalysators (MCA) hebben zich in korte tijd ontwikkeld van volledig in hardware uitgevoerde analysators tot computer gestuurde analyse systemen. De volgende generatie maakt gebruik van een computer met CAMAC-modulen en een geavanceerd interactief programma.

#### Резюме

Архитектура многоканальных анализаторов развивалась от типов с жесткой программой до вычислительных анализаторов. Архитектура следующего поколения анализаторов базирует на ЭВМ вместе с САМАС-ом и конверсационным языком высокого уровня.

Microcomputer controlled random data acquisition system J. Lecoq, H. Tedjini, P. L.Wendel and G.Metzger

This CAMAC system for data acquisition and manipulation is controlled in an interactive way by an operator through a microcomputer. The system, built around an Intel 8008 chip, includes a magnetic tape unit, a CRT display, an XY recorder, a fast analogue-to-digital converter, and a CAMAC I/O register.

# Zusammenfassung

Dieses CAMAC-System zur Datenerfassung und behand-lung wird durch einen Operator über einen Mikrocomputer (interaktiv) gesteuert. Das als Peripherie mit einem Intel 8008 Chip zusammenarbeitende System umfaßt eine Magnetbandeinheit, ein Sichtanzeigegerät, einen XY-Schreiber, einen schnellen Analog-Digital-Konvertor und ein CAMAC I/O-Register.

# Résumé

Ce système CAMAC destiné à la collecte et la manipulation des données est commandé en conversationnel par l'opérateur à l'aide d'un mini-ordinateur. Construit autour d'un circuit microprocesseur Intel 8008, le système comprend une unité de bandes magnétiques, une console de visualisation, un enregistreur XY, un convertisseur analogique/numérique rapide et un registre d'E/S CAMAC.

#### Riassunto

Questo sistema CAMAC per l'acquisizione e la manipola-zione di dati è controllato in modo interattivo da un operatore mediante un microcalcolatore. Il sistema, costruito partendo da un «microprocessor» Intel 8008, comprende una unità a nastro magnetico, un visualizzatore oscillografico, un registratore XY, un convertitore analogicodigitale rapido ed un registro CAMAC di ingresso-uscita.

#### Samenvatting

Samenvatting

Dit CAMAC-systeem dat voor de opname en verwerking van gegevens is bestemd, kan op interactieve wijze door een operator bestuurd worden. Het systeem, dat rond een Intel 8008 is opgebouwd, bestaat uit een magneetbandorgaan, een beeldbuis station, en XY-recorder, een snelle analoog-digitaalomzetter en een CAMAC I/Oregister.

# Резюме

Оператор управляет конверсационными способом систему САМАС для приёма и манипулации при помощи микро-компутера. Система построена на базе микросхемы Интель 8008 состоит из магнитофона, электроннолучевого дисплея, плоттера x-y, быстрого ЦАП-а и входно-выходного регистра САМАС.

CAMAC equipment for monitoring a telecontrol system H. Mayer

#### Summary

CAMAC equipment and a minicomputer are used to monitor a large telecontrol system for a group of hydro-electric stations. This monitoring equipment attempts to solve the problem of trouble-shooting sporadic faults in the telecontrol system.

#### Zusammenfassung

Ein CAMAC-Modul und ein Minicomputer sind in das Fernwirksystem zur Überwachung mehrerer Wasser-kraftwerke eingebaut. Diese Anlage soll das Problem sporadisch auftretender Fehler im Fernwirksystem lösen.

# Résumé

Un équipement CAMAC et un mini-ordinateur effectuent la surveillance d'un important système de télécommande, d'un groupe de stations hydro-électriques. Cet équipement de surveillance a pour but de résoudre le problème posé par les parasites entrainant des erreurs sporadiques du système de télécommande.

# Riassunto

L'apparecchiatura CAMAC ed un minicalcolatore sono impiegati per il monitoraggio di un vasto sistema di telecomando per un gruppo di centrali idroelettriche. Tale apparecchiatura di monitoraggio serve a individuare sporadici guasti nel sistema di telecomando.

# Samenvatting

Een installatie bestaande uit CAMAC-apparatuur en een minicomputer zorgt voor de besturing van een uitgebreid telebewakingssysteem bij een groep waterkrachtcentrales. Met deze installatie tracht men de moeilijkheden te voorkomen die gepaard gaan met het opsporen van sporadische gebreken in het telebewakingssysteem.

# Резюме

Аппаратура САМАС вместе с мини-ЭВМ применена для мониторования большой системы дистационного управления группы электрогидростанции. Надеются что эта установка решит проблему отброса случайных помех в системе телеуправления.

# An interface between CAMAC and the digico Micro-16V computer H. D. Blake and D. J. Folwell

A CAMAC interface unit has been developed to allow a Digico Micro-16V computer to be used with a GEC-Elliott Executive System.

#### Zusammenfassung

Um einen Digico-Micro-16 V-Rechner mit einem GEC-Elliott Executive System verwenden zu können, wurde eine CAMAC-Nahtstelleneinheit entwickelt.

#### Résumé

Une interface CAMAC a été mise au point en vue de permettre l'utilisation d'un ordinateur DIGICO Micro-16V avec un contrôleur de système GEC-Elliott.

E' stata preparata un'unità di interfaccia CAMAC per poter usare un calcolatore « Digico Micro-16V » con un sistema « GEC Elliott Executive ».

#### Samenvatting

Een CAMAC-interface werd ontwikkeld ten einde het gebruik van een GEC-Elliott Executive System bij een Digico Micro-16V computer mogelijk te maken.

#### Резюме

Разработан интерфейс CAMAC для ЭВМ Місяо-16 V фирмы Digico предназначен для работы в исполнительной системе фирмы GEC-Elliott.

# An Alpha-Numeric and graphical display driver in CAMAC N.V. Toy

#### Summary

This micro-programmed CAMAC module provides comprehensive facilities for displaying alphanumerics and graphics on an oscilloscope. The display can be refreshed from a local memory. Operational modes such as character size, generation of single vectors and sequences of vectors, and the choice of intensity, style of lines, and blink mode are selected by ASCII codes.

# Zusammenfassung

Dieses mikroprogrammierte CAMAC-Modul bietet um-fassende Möglichkeiten für die alphanumerische und graphische Bildschirmanzeige. Die Anzeige kann aus einem Lokalspeicher abgerufen werden. Betriebsvariable, wie die Zeichengröße, die Generierung einfacher Vektoren und Vektorensequenzen und die Wahl der Intensität des Zeilenstils und der Blinkart werden mit ASC II-Codes vorgewählt.

# Résumé

Ce module CAMAC micro-programmé permet la visualisation directe d'informations alphanumériques et graphiques sur un oscilloscope.

Le rafraichissement de l'image peut être effectué à partir d'une mémoire locale. Des modes opératoires tels que dinition des dimensions des caractères, génération d'un vecteur unique ou de séquences de vecteurs, choix de l'intensité, du type de lignes et du clignotement sont sélectionnés à l'aide de codes ASCII.

# Riassunto

Questo modulo CAMAC microprogrammato offre vasta possibilità di visualizzazione di dati alfanumerici e grafici su un oscilloscopio. L'indicazione può venire aggiornata da una memoria locale. I modi operativi, quali la dimensione del carattere, la generazione di singoli vettori e di sequenze di vettori, la scelta del-l'intensità, il tipo di linee. nonché il lampeggiamento vengono selezionati mediante codici ASCII.

# Samenvatting

Door toepassing van dit microprogrammeerbare CAMAC module, wordt het afbeelden van alfanumerieke en grafische tekens op een oscilloscoop aanzienlijk vereen-

voudigd. Uit een extern geheugen kan een nieuw beeld worden ingevoerd. Met behulp van ASCII-codes worden de verschillende mogelijkheden ingesteld, zoals: de lettergrootte, het genereren van een enkele vector of van reeksen vectoren, de helderheid, het lijntype en "blink mode".

#### Резюме

Этот микропрограмированный блок САМАС обеспечивает различные удобства при изображении альфанумерических и графических данных на оссуиллоскопе. Изображение восстановливается из местной памяти. При помощи кодов ASCII определяется режимы работы, такие как: размер знаков, генерирование отдельных векторов или серии векторов, выборка яркости и стиля линии, пульсирование.

# CAMAC interface module for the Biomation transient recorder Type 8100 I. Török

#### Summary

A single-width CAMAC module has been developed for control and readout of a single Biomation Type 8100 transfent recorder. The module performs programmed data transfers.

#### Zusammenfassung

Für die Steuerung und zum Auslesen des Typs Biomation 8100 ist eine CAMAC Einheit, für Programm-gesteuerte Datenübertragungen entwickelt worden.

Un module CAMAC 1/25° a été mis au point pour le contrôle et la lecture d'un seul enregistreur de transitoire Biomation de type 8100. Le module effectue des transferts de données programmés.

#### Riassunto

E' stato sviluppato un modulo CAMAC di largherra unitaria per il comando e la lettura di un singolo registratore di transitori Biomation Tipo 8100. Il modulo effettua trasferi-menti di dati programmati.

# Samenvatting

Beschreven wordt een enkelvoudig CAMAC module voor het besturen en uitlezen van een BIOMATION Type 8100 transient recorder.

# Резюме

Разработан одномодульный блок для считывания и управления одным рекордерем переходных процессов Биоматон 8100. Блок выполняет программный обмен

# CAMAC interface for a buffered card reader K. van Dellen, F. Sporrel and L. M. Taff

# Summary

This CAMAC module is an interface for a buffered card reader. Special hardware features include character decoding, packing characters into the computer's internal format, and detection of end-of-file cards.

# Zusammenfassung

Bei diesem CAMAC-Modul handelt es sich um eine Interface für einen gepufferten Kartenleser. Zu den Hardware-Merkmalen gehören die Zeichendecodierung, die Packung von Zeichen auf das Eigenformat des Rechners und die Ermittlung der Datei-Endkarten.

# Résumé

Ce tiroir CAMAC est une interface pour lecteur de cartes comprenant une mémoire. Des circuits spéciaux permettent le décodage des caractères, leur groupement au format interne du calculateur ainsi que la détection des cartes fin de l'abbien.

#### Riassunto

Questo modulo CAMAC è un'interfaccia per lettore di schede bufferizzato. Fra le Speciali caratteristiche di « hardware » comprendono la decodificazione dei caratteri, la compattazione dei caratteri nel formato interno del calcolatore e l'individuazione delle schede di fine « file ».

#### Samenvatting

Dit CAMAC-module dient als interface voor een ponskaartlezer met buffergeheugen. Bijzondere mogelijkheden van de hardware zijn ondermeer: decoderen van de tekens, rangschikken van de tekens in een vorm die overeenkomt met het interne formaat van de computer en het herkennen van afsluitkaarten (EOF).

#### Резюме

Этот блок CAMAC является интерфейсом устройства считывания карт с буфером. Как особенные свойства блока включены: декодирования знаков, упаковка знаков согласно внутренным стандартом ЭВМ и нахождение карты конца файля.

Macro-IML implementations for the PDP-11 computer M. Kubitz and R. Kind

#### Summary

IML has been implemented for the DEC PDP-11 computer with the DEC CA-11A CAMAC branch controller and the Borer 1533A single-crate controller, and with the DEC operating systems DOS, VO8/VO9 and RSX-11D (and in future with RSX-11M). The implementations follow the macro-syntax given as an appendix to the definition of IML.

#### Zusammenfassung

IML wurde für den DEC PDP-11-RECHNER mit dem DEC-CA-11A CAMAC vertikalen Datenweg und der Borer 1533A Einrahmensteuerung mit den DEC-Betriebssystemen DOS, VO8/VO9 und RSX-11D (und in Zukunft mit RSX 11M) eingesetzt. Die Anwendungen benützen die zur Definition der IML gehörenden Makro-Syntax.

#### Résumé

«IML» (Intermediate Language) a été mis au point sur ordinateur DEC PDP 11, équipé du contrôleur de branche CAMAC CA-11A et du contrôleur de châssis Borer 1533 A, sous contrôle des systèmes d'exploitation DOS, VO8/VO9 et RSX-11D (et dans l'avenir avec RSX-11M). Les instructions correspondent à la macro-syntaxe décrite dans l'annexe du document «Définition du IML».

# Riassunto

L'IML è stato applicato al calcoatore DEC PDP-11, con l'elemento di controllo del ramo principale DEC CA-11A CAMAC e il modulo di controllo per singolo conteintore «Borer 1533A», e con i sistemi operativi DEC «DOS, VO8/VO9 e «RSX-11D» (nonchè, in futuro con l'«RSX-11M»). In tali la applicazioni si segue la macrosintassi indicata in appendice alla definizione dell'IML.

# Samenvatting

In ditartikel wordt beschreven hoe IML kan worden gebruikt bij de DEC computer PDP-11 in combinatie met de CAMAC-branch driver DEC CA-11A, de Borer single-crate controller 1533A en bij de DEC besturingssystemen DOS, VO8/VO9 alsmede RSX-11D (en in de toekomst ook RSX-11M). Daarbij wordt de macro-syntaxis gevolgd die als bijlage in het document ESONE/IML/OI is opgenomen.

# Резюме

Сделана имплементация языка IML для ЭВМ ПДП-11 работающего вместе с контроллером ветви САМАС типа ДЕС СА-11А или однокрейтным контроллерем Вогег 1533А при использовании оперативных систем ДЕС: ДОЅ, VO8/VO9, RSX-11Д (в будущем RSX-11М). Имплементация в согласии с макро-синтаксисом представленом в виде приложения к определеню IML.

#### CAMAC with FORTRAN on a CDC 3100 An approach based on IML W. Kneis and W. Karbstein

#### Summary

This paper describes a straightforward approach for using CAMAC with FORTRAN on a CDC 3100 computer. The solution is based on IML and consists of only four assembler subroutines and a LAM handler. It can be regarded as a high level expansion of an earlier implementation of IML in an assembler language environment.

#### Zusammenfassung

Dieser Beitrag beschreibt eine direkte Möglichkeit zur Verwendung des CAMAC-Systems mit einer Fortran-Sprache auf einem CDC 3100-Rechner. Die Lösung basiert auf der IML und besteht aus nur vier Assembler-Unterprogrammen und einem LAM-handler. Sie kann als eine Weiterentwicklung einer früheren IML-Ausführung in einer Assembler-Sprache angesehen werden.

#### Résumé

Cet article décrit une approche directe de l'utilisation du CAMAC à l'aide de FORTRAN, sur un ordinateur CDC 3100. Basée sur l'emploi de l'IML, la solution est uniquement constituée de quatre sous-programmes assembleur et d'un programme de traitement des LAM. Elle peut être considérée comme une version évoluée d'une précédente version d'IML écrite dans le cadre d'un langage assembleur.

#### Riassunto

Questo documento descrive un approccio diretto dell'uso del CAMAC con il FORTRAN su un calcolatore CDC 3100. La soluzione è basata sull'IML e consiste di solo quattro sottoprogrammi assembler e di un programma di trattamento dei LAM. Essa puo' essere considerata un perfezionamento ad alto livello di una precedente applicazione dell'IML in un sistema a linguaggio assembler.

#### Samenvatting

In dit artikel wordt beschreven hoe CAMAC in combinatie met FORTRAN op eenvoudige maar doeltreffende wijze kan worden gebruikt in een CDC 3100 computer. De voorgestelde methode is gebaseerd op het gebruik van IML en vereist slechts vier sub-programma's in assemblertaal en een programma voor het verwerken van de LAM's. Deze oplossing kan worden beschouwd als een verdere en meer geavanceerde ontwikkeling van een reeds bestaand systeem waarbij IML op assembler-niveau wordt toegepast.

#### Резюме

Вестати описан простой подход к использовании САМАСа вместе с Фортраном на ЭВМ СДС 3100. Он основан на ILM и пользуется только четыремья подпрограммами ассемблеря и программой манипуляции запросами LAM. Можно его рассмотривать как высокого уровня расширение первоначальной имплементации IML в окружении языка ассемблера.

# A rarely-used application of the X-line L. Stanchi and I. Török

# Summary

The attention of CAMAC interface module designers is drawn to a simple method of indicating that a peripheral is inpowered or disconnected, by using the Command Accepted (X) line.

# Zusammenfassung

Die Konstrukteure von CAMAC Interfacemoduln werden auf eine einfache Methode aufmerksam gemacht, um mit Hilfe der X-Leitung anzuzeigen, ob ein Peripheriegerät stromlos oder abgeschaltet ist.

# Résumé

L'attention des concepteurs de tiroirs interface CAMAC est attirée sur une méthode simple utilisée pour indiquer qu'un périphérique n'est pas alimenté ou est déconnecté, cette méthode utilise la ligne « Commande acceptée » (X).

#### Riassunto

Si richiama l'attenzione dei projettisti di moduli interfaccia CAMAC su un metodo semplice per indicare che un'unità periferica non è alimentata da corrente o è disinserita usando la linea (X) di Comando Accettato).

#### Samenvatting

Ontwerpers van CAMAC interfacemodulen worden er attent op gemaakt dat er een heel eenvoudige methode bestaat om aan te duiden dat een randapparaat niet ingeschakeld of niet aangesloten is, namelijk door gebruik te maken van de Command Accepted (X) lijn.

#### Резюме

Обращается внимание разработчиков блоков — интерфейсов CAMAC на простой способ обнаружения что внешные устройство не получает питания или не включено, при помощи линии принятия комманды X.

# Faster address-scan by reading only non-zero data E. V. Chernykh, J. I. Chmielewski, V. A. Smirnov

#### Summary

A 'floating sub-address' technique is suggested. This speeds up the address scan mode by reading only the non-zero data registers in CAMAC modules. Implementations are described for modules with less than 16, and 16 or more, data registers.

#### Zusammenfassung

Vorgeschlagen wird eine symbolische Unteradressentechnik", die das Adressenabtastverfahren dadurch be-

schleunigt, daß nur die Ungleich-Null-Datenregister in CAMAC-Moduln ausgelesen werden. Anwendungen für Moduln mit weniger als 16 und mit 16 oder mehr Datenregistern werden beschrieben.

#### Résumé

Une technique de « sous-adresse relative » accélère le mode de scrutation d'adresse en limitant la lecture à celle des registres « non vides » des tiroirs CAMAC, ou en décrit la réalisation pour des tiroirs contenant moins de 16, 16 ou plus de 16 registres de données.

### Riassunto

Si propone una tecnica a sottoindirizzo mobile che consente di accelerare i trasferimenti di blochi di dati a scansione di indirizzi leggendo soltanto i registri con dati diversi da zero nei moduli CAMAC. Si descrwono le applicazioni per moduli con meno di 16 registri, e per moduli con 16 o più registri di dati.

# Samenvatting

In dit artikel wordt een methode beschreven "vlottende sub-adressen", waarbij alleen de registers met gegevens die niet gelijk zijn aan nul worden gelezen. Hierdoor wordt de adresaftastsnelheid aanzienlijk verhoogd. Er volgt een beschrijving van toepassingsmogelijkheden voor modulen met minder dan 16 en met 16 of meer registers.

#### Резюме

Предложен метод плавающего адреса. Он ускоряет работу в режиме сканирования адресов так как считывается только ненулевые содержания регистров данных в блоках САМАС. Описана имплементация для блоков с числом регистров меньше 16 или не меньше 16.

# SAMAC PRODUCT GUIDE

# CAMAC PRODUCT GUIDE

CLASSIFICATION GROUPS

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# CAMAC PRODUCT GUIDE

# **HARDWARE**

This guide consists of a list of CAMAC equipment which is believed to be offered for sale by manufacturers in Europe and the USA. The information has been compiled by CERN-NP-Electronics and is mainly based on information communicated by manufacturers and available up to the 10th May 1975.

Every effort has been made to ensure the completeness and accuracy of the list, and it is hoped that most products and manufacturers have been included. Inclusion in this list does not necessarily indicate that products are fully compatible with the CAMAC specifications nor that they are recommended or approved by the ESONE Committee. Similarly, omission from this list does not indicate disapproval by the ESONE Committee.

# Reader service

Readers are advised to use the Reader service enquiry card, inserted in this Bulletin, if you wish to obtain more information on CAMAC Products, and to be on the manufacturers mailing list.

Remarks on some columns in the Index of Products

#### Column

NC - N is new, C is corrected entry.

CODE - Classification code, a 2- or 3-digit decimal number (see below).

WIDTH – 1 to 25, indicates module width or—for crates—the number of stations available.

- 0 indicates unknown width or format.
- Blank, the width has no meaning.
- NA indicates other format, normally a 19 inch rack mounted chassis.

NPR - Number in brackets is issue number of the Bulletin in which the item was or is described in the New Products section.

DELIV - Date on which item became or will become available.

REF No - Reader service reference number.

# **CLASSIFICATION GROUPS**

code	9	page	code	page
1	DATA MODULES (I/O Transfers and Processing)		Crate Bus, Single-Crate Systems, Autonomous Systems)	XIX
11	Digital Serial Input Modules (Scalers, Time Interval and Bi-directional Counters, Serial Coded etc.)	111	Highway	XXII
12	Digital Parallel Input Modules (Storing and Non-Storing Registers, Coinc. Latch, LAM, Status etc.)	v	(Crate Controllers, Terminations, LAM Graders, Branch/Bus extenders)	XXII
13	Digital Output Modules (Serial: Clocks,		3 TEST EQUIPMENT	
14	Timers, Pulse Generators, Parallel: TTL Output, Drivers)	VIII	31 System Related Test Gear	XXIV
14	tation Interfacing Modules (Serial and Parallel I/O Regs, Printer-, Tape-, DVM-,		Displays	XXIV
15	Plotter- and Analyser Interfaces, Step-Motor Drivers, Supply CTR, Displays) Digital Handling and Processing Modules	XI	나는 맛있다면 하는 것은 사람들이 가장에 되었었다면 하는데	XXIV
	(and/or/not Gates, Fan-Outs, Digital Level and Code Converters, Buffers, Delays, Arithm. Processors etc.)	XIV	4 CRATES, SUPPLIES, COMPONENTS, ACCESSORIES	
16	Analogue Modules (ADC, DAC, Multiplexers, Amplifiers, Linear Gates, Discrimi-	VV	41 Crates and Related Components/Accessories (Crates with/without Dataway and	VVIII
17	Other Digital and/or Analogue Modules (Mixed Analogue and Digital, Not Dataway	XV	Supply, Blank Crates, Crate Ventilation Gear) 42 Supplies and Related Components/Accessories (Single- and Multi-Crate Supplies,	XXVI
	Connected etc.)	XIX	Blank Supply Chassis, Control Panels, Supply Ventilation)	XVIII
2	SYSTEM CONTROL (Computer Couplers, Controllers and Related Equipment)		43 Recommended or Standard Components/ Accessories (Branch Cables, Connectors etc.,	AVIII
21	Interfaces/Drivers and Controllers (Parallel Mode for 4600 Branch and Other Multi-		Dataway Connectors, Boards etc., Blank Modules, Other Stnd Components)	XXIX

#### 1 DATA MODULES — I/O TRANSFERS AND PROCESSING

Digital Serial Input Modules — Scalers, Time Interval and Bi-directional Counters, Serial Coded etc. 11

#### Simple Serial Binary Registers 111

1x24 BIT BINARY BLIND SCALER (20MHZ NIM OR 10MHZ TTL 1/P, EXT INHIBIT IN, OVF O/P)	J EB 10	SCHLUMBERGER	1	/71		13,1001
MINISCALER (2×16BIT, 30MHZ, SEPARATE GATES AND EXTERNAL RESET, NIM LEVELS)	1002	RORER	1	/69		13,1002
MINISCALER (2x16BIT, 30MHZ, SEPARATE GATES AND EXTERNAL RESET, NIM LEVELS)	002	NUCL. ENTERPRISES	i			13,1003
MINISCALER (2X16BIT, 30MHZ, SEPARATE GATES AND EXT RESET, NIM LEVELS)	C 104	ROT	1	/71		13,1004
DUAL SCALER (2X168IT, 50MHZ)	DS 050	STND ENGINEERING	1	/73		13,1005
DUAL 150 MHZ 16 BIT SCALER (QNE 50 OHMS, ONE UNTERMINATED NIM INPUT PER SCALER)	28 2024/16	SEN	1	/70		13,1006
DUAL SCALER (2X16BIT, 100MHZ)	DS 100	STND ENGINEERING	1	/73		13,1007
DUAL SCALER (2X16BIT, 150MHZ)	DS 150	STND ENGINEERING	1	174		13.1008
DUAL SCALER (2X16BIT, 200MHZ)	DS 200	STND ENGINEERING	1	174		13,1009
DUAL 24 BIT BINARY SCALER (15MHZ, NIM OR TTL INPUTS)	FHC 1313 -	FRIESEKE	- 1	/72		13,1010
DOUBLE SCALER (24/16BIT, 50MHZ, 2 I/P 8 3 GATE MODES, INHIBIT, P1=OVERFLOW)	C=DS=24	WENZEL ELEKTRONIK	1	/72		13.1011
DUAL 150 MHZ 24 BIT SCALER (ONE 50 OHMS, ONE UNTERMINATED NIM INPUT PER SCALER)	28 2024/24	SEN	1	/70		13,1012
QUAD CAMAC SCALER (4X16817 OR 2X32817, 100MHZ)	10044	RORER	1	01/75		13,1013
TIME DIGITIZER (4X16BIT,50MHZ CLOCK,WITH CENTRE FINDER, USABLE WITH PRE-AMP 511)	1005	RORER	1	/72		13,1014
SERIAL REGISTER (4X16BIT,2X32BIT SELECTABLE,25MH7,COMMON GATE,NIM LEVELS)	SR 1605	GEC-ELLINTT	1	/71		13.1015
MICROSCALER (4X16 BIT, 25MHZ, OPTIMIZED INPUT, 3 NSEC, GIVES TYP 80MHZ COUNTING)	003-4	NUCL' ENTERPRISES	1	/71	( 5)	13,1016
MICROSCALER (4x16BIT, 2x32BIT SELECTABLE, 25MHZ, COMMON GATE, NIM LEVELS)	c 102	RDT AND VARIABLE COMES	1 /	/71		13,1017
4X16 BIT BINARY BLIND SCALER (50 MHZ, 2X32BIT SELECTARLE, COMMON GATE, NIM/TTL)	J EB 20	SCHLUMRERGER	1	/71		13,1018
FOUR-FOLD SCALER (4X16BIT,2X32BIT SELECTABLE,50MH7,COMMON GATE,NIM LEVELS)	4 8 2003/50	SEN	1	/69		13,1019
FOUR-FOLD CAMAC SCALER (4X16BIT, 40MHZ, ONE 50 OHMS, ONE HI=Z NIM I/P PER SCALER)	4 8 2004	SEN SEN	8 1 V E	/70		13,1020
TIME DIGITIZER (4X16BIT, CLOCK RATE 70/85MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1	/72		13,1021
TIME DIGITIZER (4X16BIT, CLOCK RATE 70/85MHZ, NIM LEVELS)	TD 2041	SEN SEN	1	/72	(4)	13,1022
QUAD SCALER (4X16BIT, 50MHZ)	QS 050	STND ENGINEERING	1	/73		13,1023
SERIAL REGISTER (4x16BIT,2x32BIT SELECT- ABLE,100MHZ,COMMON GATE,NIM LEVELS)	SR 1608	GEC=ELLINTT	130°	/71		13,1024
FOUR-FOLD SCALER(4X16BIT,2X32BIT SELECT- ABLE,100MHZ,COMMON GATE,NIM LEVELS)	4 \$ 2003/100	SEN SEN	0 1	/70		13,1025
QUAD SCALER (4X16BIT, 150MHZ)	QS 150	STND ENGINEERING	1	174		13,1026
QUAD SCALER (4X16BIT, 200MHZ)	03 200	STND ENGINEERING	1	/74		13.1027
QUAD SCALER (4%24BIT, 50MHZ, DATAWAY AND/OR EXT FAST INHIBIT, NIM LEVELS)	84248	FG&G/ORTEC SO SANGE	1		(7)	13,1028
QUAD COUNTING REGISTER (4X24BIT, NIM INP T TIL INHIBIT IN, TIL CARRY AND DVF DUT)	709=2	NUCL. ENTERPRISES	1	/71	110-161	13,1029
SCALER (4X24BIT, 50MHZ)	9051	NUCL. ENTERPRISES	1	/73		13,1030
QUAD SCALER (4X24BIT,150/125MHZ,DATAWAY AND/OR EXT FAST INHIBIT,NIM LEVELS)	3424B	FGRG/ORTFC	1	/71		13,1031

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	QUAD SCALER (4X24RIT, 200MHZ, DATAWAY AND/OR EXT FAST INHIBIT, NIM LEVELS)	\$424F	FG8G/ORTEC		E HORE	(13)	13,1032
	QUAD SCALER (4X24RIT, 125MHZ,INTERRUPT STRUCTURE, INDIVIDUAL INHIBIT INPUTS)	sí	JOFRGER	i	172	( 5)	13,1033
	QUAD SCALER (4X24BIT, 200MHZ,INTERRUPT STRUCTURE, INDIVIDUAL INHIBIT INPUTS)	51=1	JOFRGER	1	/73		13,1034
	QUAD 100MHZ SCALER (4X24BTT,DISCR LEVEL =0.5V,TIME=INTERVAL APPL,NIM INHIB I/P)	854	JORWAY	18 178	/71	( 2)	13,1035
	QUAD 100 MH7 SCALER(4X16/24BIT,=0.5V I/P THRESHOLD,COMMON EXT FAST INHIBIT,NIM)	2550B	LRS-LECROY	i	170		13,1036
	QUAD SCALER (4X24BIT, 300MHZ, 7=SEGMENT DISPLAY/SCALER, OVF GIVES LAM)		SCHLUMBERGER	3		(12)	13,1037
	QUAD SCALER (4X24BIT OR 2X48BIT, 100MHZ, OVF GIVES LAM, COMMON INHIBIT GATE)	OS 100	STND ENGINEERING	1	/73	(12)	13,1038
	TIME DIGITIZER (6 CHANNELS, 16 BITS, 100 MHZ CLUCK RATE)	ŤD	JOERGER	1	174	(11)	13,1039
	12=CHANNEL 100MHZ SCALER (16BIT,=0.5V I/P THR, FAST CLEAR, CASCADABLE, LAM)	2252	LRS-LECROY	1	05/75		13.1040
	12-CHANNEL 16 BTT SCALER (CERN SPS2135)	9054	NUCL. FNTERPRISES	1		(10)	13,1041
	HEX TTL/NIM 50 MHZ SCALER	3610	KINETIC SYSTEMS	1	173		13.1042
	HEX COUNTING REGISTER (6x24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY DVF, BIN)	320	HYTEC	1	174		13,1043
	HEX NIM 100 MHZ SCALER	3615	KINETIC SYSTEMS	i	/73	(8)	13.1044
	12-CHANNEL 100 MHZ SCALER(12X24FIT,-0.5V I/P THR, COMMON FAST CLEAR & INHIR, NIM)	2551	LRS-LECROY	1	174	(12)	13.1045
	112 Simple Serial Decade F	Registers					
	1X6 BCD DECADE SCALER	J EA 20	SCHLUMBERGER	1	/73		13,1046
	(30 MHZ, BUILT-IN DISPLAY)  DUAL 24 BIT BCD SCALER	FHC 1311	FRIESEKE	1	/72		13,1047
	(15MHZ, NIM OR TTL INPUTS)  2X6 BCD DECADE SCALER - 100 MHZ	J EA 10	SCHLUMBERGER	1.	/71		13,1048
	WITH REMOTE DISPLAY  QUAD BCD SCALER (4x6 DECADES, 30MHZ)	9021	NUCL' ENTERPRISES	1	/71		13,1049
	HEX COUNTING REGISTER (6X24BIT, 100MHZ NIM & TTL LEVELS, TTL CARRY OVF, BCD)	321	HYTEC	1	174		13.1050
		gietore	TEACHAGA				
	113 Preset Serial Binary Re				- Paras		15.H100
	PRESET COUNTING REGISTER (1681T,10MHZ, NIM/TTL I/P,TTL INHIB + O/P,DATAWAY SET)	7039-1	NUCL' ENTERPRISES	nan Ase	/70		13,1051
	PRESET COUNTING REGISTER (24BIT, 10MHZ, DATAWAY SET, NIM, TTL INPUT, TTL O/P+INHIB)	703-1,	NUCL'. ENTERPRISES	1	/71		13,1052
	SCALER 50 MHZ (72/16/18/24BIT, PRESET WITH OVF LINE, CONSTANT DEADTIME)	C 72451=A3=A1	SIFMENS		172		13,1053
	PRESET SCALER(24/16BIT,50MHZ,DATAW. SET, BUFFER,2 I/P & 3 GATE MODES,INHIB,OVFLO)	C=PS=24	WENZEL ELEKTRONIK	1	/72		13.1054
	BIN.PRESET SCALER/BCD=DISPLAY(24BIT/8DEC 50MHZ, DATAWAY SET, 21/P&GATE MODES, INHIB)	C=SD=24	WENZEL ELEKTRONIK	1	/75		13,1055
	DUAL PRESET COUNTING REGISTER (1681T BIN)	2204	BI RA SYSTEMS	108	173		13,1056
	DUAL PRESET COUNTER/TIMER (2X16/24RIT, 40MHZ MIN, SELF RELOADABLE)	1006	RORER	1	174		13,1057
	2X24 BIT PRESET SCALER (100MHZ COUNTING)	J EP 30	SCHLUMBERGER	1	/73		13,1058
	PRESET QUAD BINARY COUNTER (4X24BIT, 75 MHZ, NIM & TTL LEVELS, TTL CARRY OVF)	310	HYTEC	1	/73		13,1059
2	(SAME BUT 50 MHZ)	350		1	174		
	114 Preset Serial Decade R	egisters					
	REAL TIME CLOCK (3.8 USEC TO 18.2 HRS, PRESET-TIME AND PRESET-COUNT MODES)	RTC 2014	SEN	1/1 = 1 - 1 1 - 1			13,1060
	24BIT BCD PRESET-SCALER (12MHZ, NIM OR TIL INPUTS, MANUAL OR DATAWAY PRESET)	FHC 1301	FRIESEKE	2 ,	/71	(1)	13,1061
	248IT BCD PRESET-SCALER (12MHZ, NIM OR TIL INPUTS, DATAWAY PRESET)	FHC 1302	FRIESEKE	1	/71		13.1062
	6 BCD DECADE SCALER (MANUAL AND DATAWAY PRESET, 1 MHZ, START/STOP DUTPUT)	J EP 20	SCHLUMBERGER	2	/71		13,1063
					AND DESCRIPTION OF THE PERSON NAMED IN		

VC	DESIGNATI	ON & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No
		, ADECADE BCD, 7 SEGM TS AND PRESET NO)	P\$R 0801	GEC-FLLINTT	1	/72	( 7)	13.106
		8 DECADE BCD, DISPLAY EXP, MAN PRESET, NIM)	C 103	PDT	3	/71		13,106
DUAL PRESE	T COUNTING	REGISTER (4 DECADES)	2204	RI RA SYSTEMS	1	/73		13,1066
		DUNTER (4X6 DECADES,	311	HYTEC	1	/73		13,106
	M & TTL LE	VELS, TTL CARRY OVF)	351		1	/74		
	117	Other Digital Serial In	put Modules (Bi-D	irectional Sequential, S	hift Type:	s)		
	RESETTABLE PULSE BURST	COUNTER (24BIT, 10MHZ,	82	JOFRGER	1	/72	( 5)	13.106
UP/DOWN PR	RESETTABLE	COUNTER(6 BCD DIGITS TAWAY PRESET)	82-1	JOERGER	1	/73		13,1069
		DOWN COUNTER	3640	KINETIC SYSTEMS	1	/73		13,107
				THE PARTY OF THE P				
		BY UP=DOWN COUNTER)	2IPE 2019	SEN		/71		13.107
	12	Digital Parallel Inp and Non-storing R		oring .atch, Lam, Status et	tc.			
	121	Non-Storing Registers	s (Gates)			relative		
PARALLEL I	NPUT GATE	(CERN SPS2133,16BIT)	9049A	NUCL' ENTERPRISES	1		(10)	13,107
ISOLATED I	NPUT GATE	16BIT, VERSION AG302D 302A FOR 115VAC)	AG 302*	STND ENGINEERING	1	/74	Alle qa	13.107
		DNTACT CLOSURE)	AG 302C	STND ENGINEERING	1	174		13,107
INPUT GATE			PG 301	STND ENGINEERING	1	/73		13,107
INPUT GATE	(24B]T, S	OURCE SELECTION BY GEN STROBE DUT)	J 007	JORWAY	1	174	(8)	13.107
INPUT GATE			3420	KINETIC SYSTEMS	1	/71	(4)	13,107
PARALLEL I	INPUT GATE	(24BIT STATIC DATA,	7059=1	NUCL. ENTERPRISES	1	/70		13.107
		(228IT STATIC DATA,	7060-1	NUCL. ENTERPRISES	1	/70		13,107
PARALLEL I	NPUT GATE	(24 BIT)	9049R	NUCL. ENTERPRISES	1		(10)	13,108
INPUT GATE	(24BIT)		PG 304	STND ENGINEERING	1	/73		13,108
24-BIT ISO	LATED INPU	T GATE	3471	KINETIC SYSTEMS	1	/73		13,108
STATIC DIG	SITAL INPUT	(2x16BIT, TTL)	C 76451-A8-A4	SIEMENS	1	/73	(6)	13,108
DUAL INPUT	GATE (168	IT)	PG 601	STND ENGINEERING	1	/73	RIA ILTRO	13,108
DUAL PARAL	LEL STROBE	D INPUT GATE (2X24BIT FER TO DATAWAY, TTL)	61	JORWAY	1	/70		13.108
DUAL PARAL	LEL INPUT	GATE (2×24BIT,NON=	61-1	JORWAY	1	/70		13,108
	DUAL 24 B		3472	KINETIC SYSTEMS	1			13,108
		STATIC DATA, INTEGR	321	POLON		174		13,108
FOR 1USEC,	TTL LEVELS	, 2X37-WAY I/P CONN) STATIC DATA, INTEGR	321A		1	/74		10.108
FOR 10USEC		S,2X37-WAY I/P CONN)	3218		1	174		
DUAL 24 BI		INPUT GATE	PG=604	STND ENGINEERING	1	172	( 6)	13,1089
	NPUT GATE	(3x16BIT INPUT FROM	1061	BORER	1	/72	(4)	13.109
3X16=BIT I	NPUT GATE	OPTO-COUPLERS)	1063	BORER	1	/73	(8)	13,1091
		ER WITH OPTO COUPLER	DO 200-2003	DORNTER	1	172		13,1092
(4x8BIT	PARALLEL :	INPUT GATES, WITH L)	DO 200-2203	Statement of the second second	1	/72		13,1092
	PUT REGISTI		DD 200=2001	DURNIER	1	/71		13,1093
INPUT GATE	S. STH BYTE	SETS LITTLIEH) L CONNECTOR)	00 200-2201		1	/72		13,109
(MODU)	JLF WITH ON	LY LOGIC BOARD)	00 200-2000		i	173		
	PUT REGIST	ER (5X8BIT PARALL SETS L,HLL,1=H)	DO 200-2002	DORNIER	1	/72		13,109
	COUNTY OTIC	CONNECTOR)						

PARALLEL IMPUT CATECIASSASCIE AS A 1092T   C. 241	NC DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF, No.
### 122 Storing Registers  OPTICAL IDULATED INPUT REGISTER (1981) (CDITING-ONS OR STRONG NORS (RESIDED NORS (COMPOLED by MEC)  PARALLE, INPUT REGISTER (1981) (CDITING-ONS OR STRONG NORS (RESIDED NORS (COMPOLED by MEC)  DYM. RIG. [UNIV.] (1981) (1981) (1981)  INPUT REGISTER (1981) (CDITING-ONS OR STRONG NORS (RESIDED NORS OR STRONG NORS (COMPOLED by MEC)  PARALLEL INPUT REGISTER (ASTING STRONG NORS OR AS 2020  STRONG THOUGH ROUTE (ASTING 1987)  INPUT REGISTER (ASTING LEVEL) (1982)  PARALLEL-INPUT REGISTER (ASTING STRONG NORS OR AS 2020  TREAT REGISTER (ASTING STRONG NORS OR ASTING PROTECTION STRONG NORS OF ASTING NORS OF ASTING PROTECTION STRONG NORS OF ASTING NORS OF ASTING NORS OF ASTING PROTECTION STRONG NORS OF ASTING NOR	PARALLEL INPUT GATE(16x168IT,TTL, 1=LOW)	IG 25601	GEC-FLLIDTT	2	/72		13,1095
OPTICAL ISOLATED IMPUT REGISTER 2001 RI PA SYSTEMS 1 7/4 13,1007  PARALLEL IMPUT REGISTER (CREST, CONTINUE) OND OF STRONGE MORES CONTROLLED BY ARE TO THE TOTAL DESCRIPTION OF THE TOTAL DESCRIPTION		C 341	INFORMATEK	1	/73		13.1096
PARALLEL INDUT RETITER (INSTITUTION   7014-1   NULL, ENTERPRISES   778   13,1008	122 Storing Registers						
DAY, OLD, TUNIT, CREATER, TIT., C 76451-A17-A4 SIFFAS 1 773 ( 8) 13,100  DAY, CLAN IT INDIT OF IOR 1-0 (DR GITH)  TANDET REGISTER (16817) PP 301 STAN ENGINEERING 1 773 ( 8) 13,1101  TROLATED INDIT REGISTER (16817) PP 301 STAN ENGINEERING 1 773 ( 8) 13,1102  12,220 ON ABOUR, AR302-FOR 1159/CD)  TANDET REGISTER (16817, CONTACT CLOSUME) AR 3020 STAN ENGINEERING 1 774 13,1102  TANDET REGISTER (16817, CONTACT CLOSUME) AR 3020 STAN ENGINEERING 1 774 ( 13,1103  PARALLELI, IMPLITEDERING (1010EL 16/40AIT OFF, FREEDRY 1 774 ( 13,1103  C INDIT REGISTER (16817, APEC CONTA ATT)  LED VIA LEGISTER (16817, APEC CONTA ATT)  LED VIA LEGISTER (16817, APEC CONTA ATT)  LED VIA LEGISTER (16817 APEC CONTA ATT)  LED VIA LEGISTER (16817 APEC CONTA ATT)  THOUR REGISTER (24817) PR 304 STAN ENGINEERING 1 773 13,1105  THOUR REGISTER (24817) PR 304 STAN ENGINEERING 1 773 13,1105  THOUR REGISTER (24817) PR 304 STAN ENGINEERING 1 773 13,1106  OFFICALLY ISOLATED.  BALANCED INPUT REGISTER MITH ADDRESSING 3430 KINCTIC SYSTEMS 1 775 ( 8) 13,1106  PARALLEL INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  TOUL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1110  THE STAN COMMAND AND THE SYSTEM CONTACT TO THE SYSTEMS 1 773 13,1110  DUAL LEG SIT INPUT REGISTER (XISBIT, TIL) 2312 PI RA SYSTEMS 1 773 13,1111  DUAL 24 SIT INPUT REGISTER (XISBIT TO THE SYSTEMS 1 773 13,1110  DUAL 24 SIT INPUT REGISTER (XISBIT TO THE SYSTEMS 1 773 13,1110  DUAL 24 SIT INPUT REGISTER (XISBIT TO THE SYSTEMS 1 773 13,1110  DUAL 24 SIT INPUT REGISTER (XISBIT TO THE SYSTEMS 1 773 13,1110  DUAL 25 STAN CHARLEL INPUT SEGISTER (XISBIT TO THE SYSTEMS 1 1 773 13,1110  DUAL AND	OPTICAL ISOLATED INPUT REGISTER	2601	BI RA SYSTEMS	1	174		13,1097
INDUT REGISTER (1881T)		7014-1	NUCL. ENTERPRISES	1	170		13,1098
OVMANIC DIGITAL IMPUT 1681T FLOATING I/P C 76451=17=43 SIEMENS 1 773 (6) 13,1101  ### ### ### ### ### ### ### ### ### #		C 76451-417-44	SIEMENS	1	/73	( 6)	13.1099
ISOLATED THRUIT REGISTER (1981TLAN3020 FUR AR 3024   STND ENGINEERING   1	INPUT REGISTER (1681T)	PR 301	STND ENGINEERING	1	173		13.1100
12,24 OR 460VE, AB3022 FOR 115VAC)   INPUT REGISTER (16017, CONTACT CLOSURE)	DYNAMIC DIGITAL INPUT 16BIT FLOATING I/P	C 76451-A17-A3	SIEMENS	1	/73	(6)	13.1101
PARALLEL-INPUT-REGISTER (SINGLE 16/24SIT MS PT 2 12SO/1 AEG-TELEPUNKEN 1 /70 ( 1) 13,1104 CMP*, REDNY TEGISTER (SIGHI, SPEC COMM.) # SITT FHC 1308 FRIESEKE 1 /71 ( 1) 13,1105 CMP*, REGISTER (SIGHI, SPEC COMM.) # SITT FHC 1308 FRIESEKE 1 /71 ( 4) 13,1106 INPUT REGISTER (SIGHI, SPEC COMM.) # SITT SIGHIA SITT SITT SITT SITT SITT SITT SITT SI		AR 302*	STND ENGINEERING	1.	/74		13,1102
OPT.READY SIGNALS.I/O TIL.CONTROL BUSY	INPUT REGISTER (16BIT, CONTACT CLUSURE)	AR 302C	STNO ENGINEERING	1	174		13,1103
ALSO VIA LEMOLIAM ON NON-FERO OR STRORE)  IMPUT REGISTER 24-BIT 3470 KINETIC SYSTEMS 1 /71 (4) 13,1106  IMPUT REGISTER 24-BIT PARABLET 3470 KINETIC SYSTEMS 1 /73 13,1107  IMPUT REGISTER (24 INPUTS, + STRORE, IR-2 JOERGER 1 /74 (11) 13,1108  OPTICALLY ISOLATED)  BALANCED IMPUT REGISTER WITH ADDRESSING 3430 KINETIC SYSTEMS 1 /72 (8) 13,1109  PARALLEL IMPUT REGISTER (2XIGBIT, TIL) 2312 RI RA SYSTEMS 1 /73 13,1110  IMPUT REGISTER (2XIGBIT, LAM & STRORE INFO & STRO		MS PI 2 1230/1	AEG-TELEFUNKEN	1	/70	( 1)	13,1104
INPUT REGISTER (248IT) PR 304 STMD ENGINEERING 1 /73 13,1107  OPTICALLY ISOLATED 24 INPUTS, * STMDBE, OPTICALLY ISOLATED 24 INPUT REGISTER WITH ADDRESSING 3430 KINETIC SYSTEMS 1 /72 (8) 13,1108  PARALLEL INPUT REGISTER WITH ADDRESSING 3430 KINETIC SYSTEMS 1 /72 (8) 13,1110  DIAL INPUT REGISTER (2X16BIT, TTL) 2312 RI RA SYSTEMS 1 /73 13,1111  DIAL INPUT REGISTER (2X16BIT, TTL) 2312 RI RA SYSTEMS 1 /73 13,1111  DIAL INPUT REGISTER (2X16BIT, LAM & STRDBE IFP & DATA-MEAD-STROBE OF WES CHANKEL) CONTROL OF THE CHANKEL) CONTROL OF THE CHANKEL OF T	C INPUT REGISTER (24BIT, SPEC CONN, 8 BIT ALSO VIA LEMO, LAM ON NON-ZERO OR STROBE)	FHC 1308	FRIESEKE	1	/71		13,1105
INPUT REGISTER (24 IMPUTS, + STROBE, OPTICALLY ISOLATED)  BALANCED INDUT REGISTER HITH ADDRESSING 3430 KINETIC SYSTEMS 1 772 (8) 13,1109  PARALLEL INPUT REGISTER (2X168IT, TTL) 2312 RI RA SYSTEMS 1 773 13,1110  OUAL INPUT REGISTORE (2X168IT, TTL) 2312 RI RA SYSTEMS 1 773 13,1110  OUAL INPUT REGISTORE (2X168IT, TTL) 2312 RI RA SYSTEMS 1 773 13,1111  OUAL INPUT REGISTORE (CANCERT CHANNEL) CAMAC UNTER, I/P'S VIA SCHMITT TEIGORS PR 1611 1 773 13,1111  OUAL 16 SIT INPUT REGISTER (CANCERT CHANNEL) CAMAC UNTER, I/P'S VIA SCHMITT TEIGORS PR 1611 1 772 13,1112  OUAL 16 SIT INPUT REGISTER (EXT STROBE OR DEATH OF THE CONTROL	INPUT REGISTER 24-BIT	3470	KINETIC SYSTEMS	1	171	(4)	13,1106
### DATICALLY ISOLATED  **BALANCED INPUT REGISTER WITH ADDRESSING 3430 KINETIC SYSTEMS 1 /72 (8) 13,1100  **PARALLEL INPUT REGISTER (2X168IT, ITL) 2312 RI RA SYSTEMS 1 /73 13,1110  **DUAL INPUT REGISTER (2X168IT, LAM & STROBE 17 & DATA-MELD-STROBE OF PER CHANNEL) COMPANIES 105E TO 10M3  **DUAL INPUT REGISTER SYSTEMS 1 1 /73 13,1111  **DUAL 10 SIT INPUT REGISTER PER COMPANIE 10 SEM 1 1 /73 13,1111  **DUAL 10 SIT INPUT REGISTER PER COMPANIE 10 SEM 1 1 /72 13,1112  **DUAL 10 SIT INPUT REGISTER STROBE OR 21 2010 SEM 1 1 /73 13,1114  **DUAL 10 SIT INPUT REGISTER STROBE OR 21 2010 SEM 1 1 /73 13,1114  **DIGITAL INPUT REGISTER (SAST) TO 10M3 SEM 1 1 /73 (6) 13,1115  **DUAL 24 SIT PARALLEL INPUT REGISTER FOR 10 STWD ENGINEERING 1 /73 (6) 13,1115  **DUAL 24 SIT PARALLEL INPUT REGISTER FOR 10 SIT INPUT STROBE OR 21 2322 SI RA SYSTEMS 1 /73 (6) 13,1116  **DUAL 24 SIT INPUT REGISTER STROBE OR 21 2222 SI RA SYSTEMS 1 /73 (6) 13,1116  **DUAL 24 SIT INPUT REGISTER PER CHANNELS CAMPAGE OF A STROBE OR 24 SIT INPUT STROBE OR PER CHANNELS CAMPAGE OF A SYSTEMS 1 /73 (7) 13,1116  **DUAL 12 SIT INPUT REGISTER PER CHANNELS CAMPAGE OF A SYSTEMS 1 /73 (7) 13,1116  **DUAL 12 SIT INPUT REGISTER STROBE OR 2400 SERIES GEC-ELLIOTT 1 /73 13,1116  **DUAL 11 SYSTEM SYSTEM SYSTEM SYSTEMS 1 /73 13,1116  **DUAL 12 SIT INPUT STROBE OR PER CHANNELS CAMPAGE OF A SYSTEMS 1 /73 13,1116  **DUAL 11 SYSTEM SYSTEM SYSTEM SYSTEMS 1 /73 13,1116  **DUAL 12 SIT INPUT STROBES OR PER CHANNELS CAMPAGE OF A SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEM SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEM SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGISTER SYSTEM SYSTEMS 1 /73 13,1120  **DUAL 12 SIT PARALLEL INPUT REGIS	INPUT REGISTER (24BIT)	PR 304	STND ENGINEERING	1	173		13,1107
PARALLEL INPUT REGISTER (2X16BIT, TTL) 2312 RI RA SYSTEMS 1 /73 13,1110  DUAL INPUT REGISTER (EXX16BIT, LAM & STROBE LYP & 1010 SEPIES GEC-ELLIDIT 1 /73 13,1111  LAMAC UNTERN. 1,P'S VIA SCHMITT TRIGGERS PR 1611 1		IR=2	JOERGER	1	174	(11)	13,1108
DUAL INPUT REGISTER (2X16BIT, LAM & STROBE 17% & DATA OF THE RESPONSE 10% OF THE CHANNEL)  CAMAGO UNTERM, 17% VIA SCHUTT TRIGGERS  DUAL 16 BIT INPUT REGISTER (2X16BIT) PR 1611  DUAL 16 BIT INPUT REGISTER (2X16BIT) PR 601  DUAL 16 BIT INPUT REGISTER (2X16BIT) PR 601  DUAL 16 BIT INPUT REGISTER (16BIT) PR 601  DUAL 17% OF THE PROPERTY OF THE PROPERT	BALANCED INPUT REGISTER WITH ADDRESSING	3430	KINETIC SYSTEMS	1	/72	(8)	13.1109
1	PARALLEL INPUT REGISTER (2X16BIT, TTL)	2312	BI RA SYSTEMS	1	/73		13.1110
DUAL 18 BIT INPUT REGISTER   21R 2002   SEN   1   /72   13,1112	I/P & DATA=READ-STROBE O/P PER CHANNEL) CAMAC UNTERM. I/P'S VIA SCHMITT TRIGGERS		GEC-ELLIDTT		/73		13,1111
DATAMAY COMMAND STORES DATA, TTL LEVELS)  DUAL INPUT REGISTER (168IT) PR 601 STND ENGINEERING 1 /73 13,1114  DIGITAL INPUT REGISTER (168IT) PR 601 STND ENGINEERING 1 /73 13,1114  DIGITAL INPUT REGISTER (168IT) C 76451=A8=A3 SIEMENS 1 /73 (6) 13,1115  DUAL 24 BIT PARALLEL INPUT REGISTER (TTL) 2322 BI RA SYSTEMS 1 /73 13,1116  DUAL 24 BIT INPUT REGISTER REGISTER RI=224 EGRG/ORTEC 1 /72 13,1117  (TTL, MANDSMAKE)  DUAL INPUT REGISTER(2X2BIT, LAM & STROBE I/P 2400 SEPIES GEC=ELLIOTT 1 /73 13,1118  I/P & DATA—EAD-STROBE 0/P PER CHANNEL) CAMAC UNTERN, I/P13 VIA SCHMITT TRIGGERS I/P 2401 1 /73  (SAME BUT MITH THISTED PAIR INPUTS) PR 2402 1 /73  (SAME BUT MITH MPTISTED PAIR INPUTS) PR 2403  DUAL INPUT REGISTER (2X24BIT, 1/P INTEGR 220 HYTEC 1 /73 13,1119  TTL, FULL LAM, DUTPUT STROBES)  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13,1120  ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LOAD REQUEST, 4 DREW HONDES), TTL LEVELS)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LOAD REQUEST, 4 DREW HONDES), TTL LEVELS)  DUAL 24 BIT DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LOAD REQUEST, 4 DREW HONDES), TTL LEVELS)  DUAL 24 BIT PARALLEL INPUT REGISTER (2X24 BITS) J RE 10 SCHLUMBERGER 1 /73 (7) 13,1122  CAHBIT DUAL PARALLEL INPUT REGISTER PR=604 STND ENGINEERING 1 /73 (7) 13,1123  DUAL 24 BIT PARALLEL INPUT REGISTER PR=604 STND ENGINEERING 1 /75 13,1125  DUAL 1 INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1125  DUAL 1 INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1125  DUAL 1 INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1125  DUAL 1 INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1125  DUAL 1 INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1126  DIAL INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1126  DIAL INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1126  DIAL INPUT REG. (2X24 BITS) J RE 10 SCHLUMBERGER 1 /75 13,1126	DUAL 16 BIT INPUT REGISTER	218 2002	SEN	1	/72		13.1112
DIGITAL INPUT (2X16BIT FLOATING INPUT) C 76451=A8=A3 SIEMENS 1 /73 (6) 13,1115  DUAL 24 BIT PARALLEL INPUT REGISTER (TTL) 2322 BI RA SYSTEMS 1 /73 13,1116  DUAL 24 BIT INPUT REGISTER RI=224 EGRG/ORTEC 1 /72 13,1117  (TTL, HANDSHAKE)  DUAL INPUT REGISTER (2X24BIT, LAM & STROBE I/P & DATA=PRAD=3TROBE O/P PER CHANNEL) CAMAC UNTERM, I/P'S VIA SCHMITT TRIGGERS PR 2400 SERIES GEC-ELLIOTT 1 /73 13,1118  I/F & DATA=PRAD=3TROBE O/P PER CHANNEL) CAMAC UNTERM, I/P'S VIA SCHMITT TRIGGERS PR 2401 1 /73  INFUT REGISTER (2X24BIT, I/P INPUT, PR 2403 1 /73  (GAME BUT HITH OFFICE PAR INPUTS, PR 2403 1 /73  (GAME BUT HITH OFFICE PAR INPUTS, PR 2403 1 /73  (DUAL INPUT REGISTER (2X24BIT, I/P INTEGR 220 HYTEC 1 /73 13,1119  TTL, FULL LAM, OUTPUT STROBES)  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOPRGER 1 /72 (7) 13,1120  ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LOAD REQUEST, 4 OPER MODES TTL LEVELS)  DUAL PARALLEL INPUT REGISTER (2X24BIT)  PARALLEL INPUT REGISTER (2X24 BITS) JR 10 SCHLUMREPGER 1 /73 (7) 13,1122  (A HAS LO-Z, R HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS) JR 10 SCHLUMREPGER 1 /73 (7) 13,1123  OUAL 24 BIT PARALLEL INPUT REGISTER PR=604 SIND ENGINEERING 1 /72 13,1124  DUAL 17 BEG, 2X24BIT, SPP, TIMING, LOGIC BITMS POS/NEG, ATIMING SDATA IN MODES)  OONNIER MODULES ALSO MARKETED BY SIEMENS SIFMENS 13,1126  OUGNIER MODULES ALSO MARKETED BY SIEMENS SIFMENS 13,1127		2IR 2010	SEN	1	/70		13,1113
DUAL 24 BIT PARALLEL INPUT REGISTER (TTL) 2322 BI RA SYSTEMS 1 /73 13,1116  DUAL 24 BIT INPUT REGISTER RI=224 EGRG/ORTEC 1 /72 13,1117  (TTL, HANDSHAKE)  DUAL INPUT REGISTER(2X24BIT,LAM & STROBE IVERS IN CAMAC UNTERH, IP/13 VIA SCHMITT TRIGGERS PR 2400 SERIES GEC-ELLIOTT 1 /73 13,1118  CAMAC UNTERH, IP/13 VIA SCHMITT TRIGGERS PR 2401 1 /73  (SAME BUT HITH THISTED PAIR INPUTS) PR 2402 1 /73  (SAME BUT HITH OFFICAL ISOLATION INPUT, PR 2403 1 /73  LOGIC 1 = 9V OR 12MA)  DUAL INPUT REGISTER (2X24BIT,I/P INTEGR 220 HYTEC 1 /73 13,1119  TIL-FULL LAM. OUTPUT STROBES )  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13,1120  ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER(2X24BIT,EXT LODA REQUEST, OPER MODES.TIL LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT,EXT LODA REQUEST, OPER MODES.TIL LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT)  CA HAS LO-2, R HAS UNTERHINATED INPUT)  PARALLEL INPUT REGISTER (2X24BITS) J RE 10 SCHLUMREPGER 1 /73 (7) 13,1122  CA HAS LO-2, R HAS UNTERHINATED INPUT)  DUAL INPUT REG. (2X24BIT, SEP, TIHING, LOGIC (C-IC-4B) WENZEL ELEKTRONIK 1 /75 13,1125  DURING MODULES ALSO MARKETED BY SIEMENS SIFMENS 13,1126  DIGITAL INPUT REGISTER, EXTERNAL STRUBE (AXBBIT INPUT LATCHERS, 1XBBIT SET LAM)	DUAL INPUT REGISTER (16817)	PR 601	STND ENGINEERING	1	/73		13,1114
DUAL 24 BIT INPUT REGISTER (TTL, HANDSHAKE)  DUAL INPUT REGISTER(2X24BIT, LAM & STROBE IF PR 2400 SERIES GEC-ELLIOTT 1 /73 13,1118  I/P & DATA-MEADA-STROBE O/P PER CHANNEL) CAMAC UNTERN, I/P'S VIA SCHMITT TRIGGERS 1 /73 13,1118  I/P FILTER RESPONSE IUSEC TO 10MS (SAME BUT MITH THISTED PAIR INPUTS) PR 2401 1 /73 (SAME BUT MITH THISTED PAIR INPUTS) PR 2402 1 /73 (SAME BUT MITH THISTED PAIR INPUTS) PR 2403 1 /73  LOGIC 1 = 5V OR 12MA)  DUAL INPUT REGISTER (2X24BIT, I/P INTEGR 220 HYTEC 1 /73 13,1119  TTL, FULL LAM, DUTPUT STROBES)  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13,1120  ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER(2X24BIT,EXT 60A JOFRAY 1 /70 13,1121  LOAD REQUEST, 4 DEER MODES, TIL LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT,EXT 60A JOFRAY 1 /70 13,1122  (A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24BITS) J RE 10 SCHLUMBERGER 1 /73 (7) 13,1123  OUAL 24 BIT PARALLEL INPUT REGISTER PR-604 SIND ENGINEERING 1 /72 13,1123  DUAL 24 BIT PARALLEL INPUT REGISTER PR-604 SIND ENGINEERING 1 /75 13,1124  CHITCH THE DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP. TIHING, LOGIC BITHISE POS/NEG. *TIMINGS JOATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS  DORNIER MODULES ALSO MARKETED BY SIEMENS  DORNIER MODULES ALSO MARKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRUBE (AXBBIT INPUT LATCHES), 1XABIT SET LAM)	DIGITAL INPUT (2X16BIT FLOATING INPUT)	C 76451-A8-A3	SIEMENS	1	/73	( 6)	13,1115
OUAL INPUT REGISTER (2X24BIT, IAM & STROBE PR 2400 SERIES GEC-ELLIOTT 1 /73 13,1118  I/P & DATA-READ-STROBE O/P PER CHANNEL) CAMAC UNTERM, I/PIS VIA SCHMITT TRIGGERS PR 2401 1 /73  I/P FILTER RESPONSE USEC TO 10MS (SAME BUT WITH TWISTED PAIR INPUTS) PR 2402 1 /73  (SAME BUT WITH TWISTED PAIR INPUTS) PR 2403 1 /73  COMMINITED TO PAIR INPUT PROJECT PR 2403 1 /73  DUAL INPUT REGISTER (2X24BIT, I/P INTEGR 220 MYTEC 1 /73 13,1119  TIL, FULL LAM, OUTPUT STROBES)  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13,1120  ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LOAD REQUEST, 4 OPER MODES, TIL LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BITS) 9041A/9041R NUCL. ENTERPRISES 1 /72 (7) 13,1122  (A HAS LO-Z, R HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS) J RE 10 SCHLUMRERGER 1 /73 (7) 13,1123  DUAL 24 BIT PARALLEL INPUT REGISTER PR-604 STND ENGINEERING 1 /72 13,1124  (WITH LED DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP, TIMING, LOGIC C-IC-48 MENZEL ELEKTRONIK 1 /75 13,1125  DURNIER MODULES ALSO MAKETED BY SIEMENS SIEMENS  DORNIER MODULES ALSO MAKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRURE DO 200-2004 DORNIER 1 /73 13,1127	DUAL 24 BIT PARALLEL INPUT REGISTER (TTL)	2322	BI RA SYSTEMS	1	/73		13,1116
1/P & DATA-READ-STROBE O/P PER CHANNEL    CAMAC UNITERM; 1/PIS VIA SCHMITT TRIGGERS   PR 2401   1		RI=224	EG&G/ORTEC	i	/72		13,1117
CAMAC UNTERM, 1/PIS VIA SCHMITT TRIGGERS INPFILTER RESPONSE 1USEC TO 10MS (SAME BUT WITH THISTED PAIR INPUTS) (SAME BUT WITH THISTED PAIR INPUTS) (SAME BUT WITH OFFICAL ISOLATION INPUT, PR 2402  DUAL INPUT REGISTER (2X24BIT, I/P INTEGR 220  HYTEC  I /73  DUAL INPUT REGISTER (2X24BIT, I/P INTEGR 220  HYTEC  I /73  INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13,1120 ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LEVELS)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT) (A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS)  DUAL 24 BIT PARALLEL INPUT REGISTER PR-604  STND ENGINEERING  DUAL 24 BIT PARALLEL INPUT REGISTER (WITH LED DISPLAY OPTION)  DUAL 1NPUT REG. (2X24BIT, SEP, TIHING, LOGIC WITH LED DISPLAY OPTION)  DUAL 1NPUT REG. (2X24BIT, SEP, TIHING, LOGIC BITHISE POS/NEG, 4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS		PR 2400 SERIES	GEC-ELLINTT	1	/73		13,1118
(SAME BUT WITH THISTED PATR INPUTS) (SAME BUT WITH OPTICAL ISOLATION INPUT, (SAME BUT WITH THISTED PATR INPUT, (I AMA, INPUT REGISTER (2X24BIT, IPPUT)  DUAL INPUT REGISTER (2X24BIT, IPPUT REGISTER (PROMA)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EVELS)  DUAL 24 BIT PARALLEL INPUT REGISTER (WITH LED DISPLAY OPTION)  DUAL 1NPUT REGISTER (2X24BIT, SEP. TIMING, LOGIC WITH LED DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP. TIMING, LOGIC BITWISE POS/NEG, 4TIMING SOLATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRUEE (AXBBIT INPUT LATCHES, 1XBBIT SET LAM)  PR 2403  1	CAMAC UNTERM' I/P'S VIA SCHMITT TRIGGERS	PR 2401		1	/73		
INPUT REGISTER (2X24BIT, 3 MODES OF DATA IR JOFRGER 1 /72 (7) 13.1120 ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT, EXT LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER 9041A/9041B NUCL. ENTERPRISES 1 /72 (7) 13.1122 (A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS) J RE 10 SCHLUMRERGER 1 /73 (7) 13.1123 DUAL 24 BIT PARALLEL INPUT REGISTER PR-604 STND ENGINEERING 1 /72 13.1124 (HITH LED DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP.TIMING, LOGIC C-IC-48 WENZEL ELEKTRONIK 1 /75 13.1125 BITWISE POS/NEG. 4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS SIEMENS 13.1126 DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200-2004 DORNIER 1 /73 13.1127 (4X8BIT INPUT LATCHES, 1X8BIT SET LAM)	(SAME BUT WITH TWISTED PAIR INPUTS) (SAME BUT WITH OPTICAL ISOLATION INPUT,						
ENTRY, LED DISPLAY)  DUAL PARALLEL INPUT REGISTER (2X24BIT,EXT LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER (2X24BIT) (A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS)  DUAL 24 BIT PARALLEL INPUT REGISTER PR-604  WENZEL ELEKTRONIK  DUAL 1NPUT REG. (2X24BIT, SEP.TIMING, LOGIC BITWISE POS/NEG. 4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200-2004  DORNIER MODULES ALSO MARKETED BY SIEMENS  DORNIER MODULES ALSO MARKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200-2004  DORNIER 1 /73 13.1127		220	HYTEC	1	/73		13,1119
LOAD REQUEST, 4 OPER MODES, TTL LEVELS)  24-BIT DUAL PARALLEL INPUT REGISTER 9041A/9041B NUCL. ENTERPRISES 1 /72 (7) 13.1122 (A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS) J RE 10 SCHLUMRERGER 1 /73 (7) 13.1123 DUAL 24 BIT PARALLEL INPUT REGISTER PR-604 STND ENGINEERING 1 /72 13.1124 (WITH LED DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP.TIMING, LOGIC BITWISE POS/NEG. 4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS SIEMENS 13.1126 DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200-2004 DORNIER 1 /73 13.1127 (4X8BIT INPUT LATCHES, 1X8BIT SET LAM)		IR	JOFRGER	1	/72	(7)	13,1120
(A HAS LO-Z, B HAS UNTERMINATED INPUT)  PARALLEL INPUT REGISTER (2X24 BITS) J RE 10 SCHLUMRERGER 1 /73 (7) 13.1123  DUAL 24 BIT PARALLEL INPUT REGISTER PR=604 STND ENGINEERING 1 /72 13.1124  (WITH LED DISPLAY OPTION)  DUAL INPUT REG. (2X24BIT, SEP.TIMING, LOGIC BITMISE POS/NEG. 4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS SIEMENS 13.1126  DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200=2004 DORNIER 1 /73 13.1127  (4X8BIT_INPUT LATCHES, 1X8BIT SET LAM)		60A	JORWAY	1	/70		13,1121
DUAL 24 BIT PARALLEL INPUT REGISTER PR=604 STND ENGINEERING 1 /72 13.1124 (WITH LED DISPLAY OPTION)  DUAL INPUT REG.(2X24BIT,SEP.TIMING,LOGIC BITWISE POS/NEG.4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS SIEMENS 13.1126  DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200=2004 DORNIER 1 /73 13.1127 (4X8BIT_INPUT LATCHES, 1X8BIT_SET_LAM)		9041A/9041B	NUCL. ENTERPRISES	1	/72	(7)	13,1122
(WITH LED DISPLAY OPTION)  DUAL INPUT REG.(2X24BIT,SEP.TIMING,LOGIC C=IC=48 WENZEL ELEKTRONIK 1 /75 13.1125 BITWISE POS/NEG.4TIMING& 3DATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS SIEMENS 13.1126  DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200=2004 DORNIER 1 /73 13.1127  (4X8BIT_INPUT LATCHES, 1X8BIT_SET_LAM)	PARALLEL INPUT REGISTER (2X24 BITS)	J RE 10	SCHLUMBERGER	1	/73	(7)	13,1123
BITHISE POS/NEG.4TIMING BOATA IN MODES)  DORNIER MODULES ALSO MARKETED BY SIEMENS  DIGITAL INPUT REGISTER, EXTERNAL STRUBE  DO 200=2004  DORNIER  1 /73 13.1127  (4XBBIT INPUT LATCHES, 1XBBIT SET LAM)		PR=604	STND ENGINEERING	1	/72		13,1124
DIGITAL INPUT REGISTER, EXTERNAL STRUBE DO 200=2004 DORNIER 1 /73 13.1127 (4XBBIT INPUT LATCHES, 1XBBIT SET LAM)		C=IC=48	WENZEL ELEKTRONIK	1	/75		13,1125
(4XBBIT INPUT LATCHES, 1XBBIT SET LAM)	DORNIER MODULES ALSO MARKETED BY STEMENS		SIFMENS				13,1126
		DD 200=2004	DORNIER	1	/73		13,1127
		DO 200-2204		1 .	/73		

NC

#### Terminated Signal Input Registers (Coinc. Latch, Pattern etc.) 123

있는 그 이번에 그렇게 이 있는 다양을 여성하셨다면 하는 이 내용을 의원하였다. 이 번째 그리고 있는 것이 한 사람들이 없다.		경기 가장 없는 사람들은 사람들이 가지 않는 것이 없는데 없다.					
12 BIT PARALLEL INPUT REGISTER (NIM)	2351	RI RA SYSTEMS	1	/73		13.1128	
STROBED INPUT REGISTER (12BIT COINC AND LATCH, NIM LEVELS, PATTERN AND LERED APPL)	SIR 2026	SEN	1	/70		13,1129	
1681T DISCRIMINATOR-COINCIDENCE REGISTER	2352	RI RA SYSTEMS	2	01/75		13,1130	
FAST COINCIDENCE LATCH (1681T, DISCR 1/P, MIN 2 NSEC STROBE-SIGNAL OVERLAP)	64	JORWAY	1	/71	(1)	13,1131	
16 FOLD DCR (16 DISCR, COMMON STROBE, -70MY THRESHOLD, FAST SUMMING OUTPUTS)	23408	LRS-LECROY	2	/71	(6)	13.1132	
16-CH COINCIDENCE REGISTER (STROBE I/P, 2NS OVERLAP, FAST SUM O/P AND CLEAR, NIM)	23418	LRS-LECROY	1	/71	(4)	13,1133	
PATTERN UNIT (16 INDIV NIM INPUTS, COMMON NIM GATE)	021	NUCL. ENTERPRISES	2	/71	( 5)	13,1134	
FAST INPUT REGISTER (ASSEMBLES 16BIT WORDS FROM IL2 INPUTS)	9053	NUCL. ENTERPRISES	1	/74		13,1135	
PATTERN UNIT (16RIT, I/P STROBED WITH COMMON GATE, 10 NSEC OVERLAP, NIM LEVELS)	C 101	RDT	2	/71		13,1136	
16 BIT PATTERN UNIT (NIM T/P AND GATE)	J PU 10	SCHLUMBERGER	1	/72		13,1137	
PATTERN UNIT 16 BIT (16 INDIVIDUAL NIM INPUTS, COMMON NIM GATE, CERN SPECS 021)	16P 2007	SEN	2	/70		13,1138	
16 BIT PATTERN UNIT (CERN 071, 16 INDIV NIM INPUTS, COMMON NIM GATE, LED DISPLAY)	16P 2047	SEN AND THE SECOND	1	/72	(11)	13,1139	
COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 116	STND ENGINEERING	1	174		13.1140	
COINCIDENCE REGISTER/LATCH (16 CHANNEL)	CR 216	STND ENGINEERING	1	/74		13,1141	
COINCIDENCE REGISTER (16 CH, COMMON GATE, MIN OVERLAP 2NS, DOUBLE PULSE RESOL 10NS)	CR=6001	STND ENGINEERING	1	/74	(12)	13,1142	
COINCIDENCE LATCH (24 NIM INPUTS WITH COMMON STROBE, EXT RESET, 2NSEC OVERLAP)	C124	EG&G/ORTEC	2			13,1143	
COINCIDENCE REGISTER/LATCH (24 CHANNEL)	CR 224	STND ENGINEERING	1	/74		13,1144	
COINCIDENCE BUFFER (2X12BIT, ONE STROBE PER 12BITS, MIN 2NS OVERLAP, NIM INPUTS)	C212	EG&G/ORTEC	2	/71		13,1145	

#### Manual Input Modules (Word Generators, Parameter Units) 124

	TER UNIT 12 BIT (PROVIDES 12 BIT ICATION, PUSH BUTTON L=REQUEST)	P 2005	SEN	1	/70		13,1146
	INPUT REGISTER (INPUTS A HAND-SET WORD, MANUAL AND ELECTR LAM I/P)	1041	BORER	1	/73	(8)	13.1147
24 BIT	PARAMETER UNIT	2501	RI RA SYSTEMS	1	/73		13.1148
	ENERATOR (24BIT WORD Ly set by Switches)	WG 2401	GEC-ELLIOTT	1	/71		13.1149
	WITCHES BITS, READABLE + CONTENT ADDR)	C 322	INFORMATEK	1	/72		13,1150
	INPUT/OUTPUT REGISTER (24 BITS, I/P + LAM, 24 LED O/P REGISTER)	201	JORWAY	1	174	(11)	13,1151
24-BIT	MANUAL INPUT	3460	KINETIC SYSTEMS	1	/73		13,1152
	ENERATOR (24 BITS OF BINARY DATA, SELECTED)	9020	NUCL. ENTERPRISES	1	/71	(2)	13,1153
24 BIT	WORD GENERATOR , WITH LAM	WGR=241	STND ENGINEERING	1	173		13,1154
MANUAL	REGISTER (FOUR 16 BIT WORDS)	231	POLON	3	174		13,1155
	TER UNIT (QUAD 4-DECADE BCD TERS MANUALLY SET)	022	NUCL. ENTERPRISES	) <b>4</b>	/71	(2)	13.1156
	TER UNIT (QUAD 4 DECADE BCD TERS MANUALLY SET)	C 105	RDT	4	/71		13,1157

# Other Parallel Input Modules (Incl. Lam and Status Registers, see 232 for Lam Grader)

가장 경영하다 보고 있다면 경영화 화장 사람들이 되었다. 그렇게 되었다면 하다 되었다.					
24-BIT INTERRUPT REGISTER (STATUS COMPARED, CHANGE GIVES LAM)	1051	BORER	1	/72 (3)	13,1158
PRIORITY INPUT REGISTER (1281TS ORE LAM, FAST COINC LATCH APPL, MASK REG		JORWAY	2	/70	13,1159
INPUT REGISTER (12 BIT, ORED TO LA		JORWAY	1	/74	13,1160

N	C DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	INTERRUPT REQUEST REGISTER	EC 218	NUCL. ENTERPRISES	1			13,1161
	LAM REQUEST REGISTER (16 BIT)	300	POLON	1	174		13,1162
	INTERRUPT ALARM REGISTER (16 BITS, INDIVIDUALLY MASKABLE)	J IR 10	SCHLUMBERGER	1	/74	(11)	13,1163
	64 LINE SURVEYOR (SINGLE OR CONTINUOUS SURVEY CYCLES, 3 SURVEY MODES)	64LS 2052	SEN	1		( 9)	13,1164
	ISOLATED INTERRUPT GATE (16BIT, **D FOR 12,24 OR 48V, **A FOR 115VAC VERSION)	AIG 302*	STND FNGINEERING	1	174		13,1165
	INTERRUPT GATE (16BIT, CONTACT CLOSURE)	AIG 302C	STND ENGINEERING	1	174		13,1166
	ISOLATED INTERRUPT REGISTER(16BIT, **D FOR 12,24 OR 48VDC, *** FOR 115VAC )	AIR 302*	STND ENGINEERING	1	174		13,1167
	INTERRUPT REGISTER (16817, COTACT CLOSURE)	AIR 302C	STND ENGINEERING	1	174		13,1168
	INTERRUPT GATE (24BIT)	IG 304	STND ENGINEERING	1	174		13.1169
	DUAL INTERRUPT GATE (2481T)	IG 604	STND FNGINEERING	1	174		13,1170
	INTERRUPT REGISTER (1281T) INTERRUPT REGISTER (1681T) INTERRUPT REGISTER (2481T)	IR 012 IR 016 IR 024	STND ENGINEERING	1 1 1	/74 /74 /74		13,1171
	INTERRUPT REGISTER (24BIT)	IR 304	STND ENGINEERING		174		13,1172
	STATUS INTERRUPT (24BIT, I/PBLATCHELAME MASK, GROUPESEL=LAM=TEST, VAR . LOGICELEVEL)	C=SI=24	WENZEL ELEKTRONIK	1	/74	(12)	13,1173
	13 Digital Output Mo Pulse Generators, I 131 Serial Output Module	Parallel: TTL Outp	out, Drivers				
	Supplied the second section of the second section of the second section of the second section of the second second section of the second secon						
	PRESET SCALER (LEVEL OR PULSE TRAIN O/P, DURATION SET BY COMMAND, SINGLE & REPEAT)	PSR 0801	GEC-ELLIOTT	1	/73		13,1174
	CRYSTAL CLOCK GENERATOR (7 TTL DUTPUTS FOR 1HZ TO 1MHZ FREQUENCY DECADES)	FHC 1303	FRIESEKE	1	/71	(1)	13,1175
	CRYSTAL CONTROLLED PULSE GENERATOR (7 DE- CADES-1HZ TO 1MHZ-500NS PULSES OUT, TTL)	PG 0001	GEC-ELLIOTT	1	/71		13,1176
	REAL TIME CLOCK (4SEC CLOCK/5MSEC STOP WATCH)	C 320	INFORMATEK	1	/72		13,1177
	CLOCK GENERATOR (INT 10MHZ, EXT 50MHZ, 8 DECADE STEPS, PLUS PROGRAMMABLE DUTPUT)	CG	JOERGER	1	/72	(7)	13,1178
	GATED CLOCK (10MHZ TO 1HZ, INT=EXT CLOCK, SYNCHRONOUS GATING)	217	JORWAY	1	174	(11)	13,1179
	CLOCK PULSE GENERATOR (7 OUTPUTS-1HZ TO 1MHZ-IN DECADE STEPS, 10MHZ EXT IN, TTL)	7019=1	NUCL. ENTERPRISES	1 1 1	- /70		13,1180
	CLOCK GENERATOR (INTERN 1MMZ, EXT 10MMZ, 7 DECADES 1HZ-1MHZ TTL 0/P, 5USEC WIDTH)	730A	POLON	1	174		13,1181
	CLOCK PULSE GENERATOR (7 DECADES=1HZ TO 1MHZ=500 NSEC PULSES OUT, TTL AND NIM)	C 109	RDT	1	/71		13,1182
	1 HZ = 1 MHZ QUARTZ CLOCK (7 O/P = 1HZ TO 1MHZ=200 TO 800 NSEC WIDTH,TTL LEVEL)	J HQ 10	SCHLUMBERGER	1	/71		13,1183
c	QUARZ-CLOCK WITH 2 TIMER FUNCTIONS	C 76451=A14=A2	SIEMENS		/72		13,1184
	CAMAC-CLOCK-GENERATOR(7 DECADES=10MHZ TO 1HZ,50/500 NSEC D/P PULSES,2.8V/50 DHMS)	C=CG=10	WENZEL ELEKTRONIK	1	/71		13,1185
	CLOCK/TIMER (0.0018 TO 10 HRS TIME INTERVAL, TIME-OF-DAY OUTPUT)	1411	BORER	1	172	(3)	13,1186
	REAL TIME CLOCK, LIVE TIME INTEGRATOR, PRESET TIMER	RC014	EGRG/ORTEC	i	/73		13,1187
	REAL TIME CLOCK (COUNTS .1 SEC TO 999 DAYS, DISPLAYS HRS/MIN/SEC, 50/60HZ GEN)	RTC	JOERGER	2	/73	(7)	13,1188
	REAL TIME CLOCK	9064	NUCL. ENTERPRISES	1		(10)	13,1189
	REAL TIME CLOCK (3.8 USEC TO 18.2 HRS, PRESET=TIME AND PRESET=COUNT MODES)	RTC 2014	SEN	1	/71	H (8034.5	13,1190
	INTERVAL TIMER/WATCHDOG (100USEC=300SEC INTERVAL, 1 SEC==100 SEC TIMEOUT)	EC 384	SENSION	1,6710	174	(13)	13,1191
	REAL TIME CLUCK (PRESET COUNTER, PRESET TIMER 3.8USEC TO 18.2 HRS, ELAPSE TIME)	RTC 018	STND ENGINEERING	1 13	174	(12)	13,1192
	DEAD TIME COUNTER	2203	RI RA SYSTEMS	1	174		13,1193
	TIMER MODULE	3655	KINETIC SYSTEMS	1	/73		13,1194
	TIME BASE (10 TO 100MHZ IN INCREMENTS OF	TB 2032	SEN	1	/71		13.1195

TIME BASE (10 TO 100MHZ IN INCREMENTS OF 10MHZ, USED WITH TO 2031/TD 2041)

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
TTMED	(MIN 1USEC, DVF FROM COUNTER-PP1)	C 76451-A12-A1	SIEMENS	2	/73	( 6)	13,1196
TEST P	ULSE GENERATOR (5 TO 50 NSEC NIM LSE DERIVED FROM \$1.F(25) OR EXT)	TPG 0202	GEC-ELLIDIT	. 1	/71		13,1197
	ULSE GENERATUR (NIM PULSE PAIR)	215	JORWAY	1	/75		13,1198
8 CHAN	NEL DELAY GENERATOR (DELAY O TO 99 CLOCK, DELAYS CASCADABLE)	220	JORWAY	1	/74	(11)	13,1199
	ROGRAMMED PULSE GENERATOR (50HZ/ MHZ PULSE TRAIN, LENGTH BY COMMAND)	2PPG 2016	SEN	1	/71		13,1200
	132 Parallel Output Regist	ers (TTL, HTL, NIM	etc.)				
DRTICA	L ISOLATED OUTPUT REGISTER	3601	RI RA SYSTEMS	1	174		13,1201
	PARALLEL DUTPUT REGISTER (NIM)	3251	RI RA SYSTEMS	1	/73		13,1202
16 BIT	PARALLEL OUTPUT REGISTER (RIT SABLE, NIM LEVELS OR PULSES)	C 343	INFORMATEK	1	/73		13,1203
12 BIT	OUTPUT REGISTER (DC OR PULSE O/P, NG STRUBE OUTPUT, NIM LEVELS)	41	JORWAY	1	/71	( 2)	13,1204
QUTPUT	REGISTER (12RIT, NTM PULSES OR OUT)	NR 2027	SEN	1	/70		13,1205
OUTPUT	REGISTER (12BIT)	PR 312	STND ENGINEERING	1 =	/73		13,1206
DIFFER	ENTIAL OUTPUT REGISTER	3030	KINETIC SYSTEMS	1	/72	(8)	13,1207
OUTPUT	REGISTER (12 CHANNEL)	DR 612	STND ENGINEERING	1.1	/73		13,1208
C OUTPUT	REGISTER (248IT TTL VIA SPEC CONN LSO VIA FRONT PANEL LEMO)	FHC 1309	FRIESEKE	1	/72		13,1209
N OUTPUT	REGISTER (24 BIT, 16 MA 5V DUT)	9600A	NUCL. ENTERPRISES	0		(13)	13.1210
-	REGISTER (24BIT, OPTO=COUPLER, 7MA)	9603	NUCL. ENTERPRISES	0		(13)	13,1211
OUTPUT (24BIT	REGISTER WORD, TTL O/P VIA 37-WAY CONN)	351	POLON	1	/73		13,1212
OUTPUT	REGISTER (24BIT)	PR 314	STND ENGINEERING	1	/73		13,1213
PARALL TTL, AC	EL OUTPUT REG. (24BIT, NEG/UPT POS J. DURATIONSLEVEL, 4 TIMING MODES)	C=0C=24	WENZEL ELEKTRONIK	1	/73	(10)	13,1214
DUAL 1	GBIT PARALLEL OUTPUT REGISTER(TTL)	3212	BI RA SYSTEMS	1	/73		13,1215
DUAL S	6 BIT OUTPUT REGISTER (SELECTABLE PAGES ON PLUGABLE PC, FP CONNECTOR)	20R 2051	SEN	1		(9)	
DUAL S	24 BIT PARALLEL OUTPUT REGISTER	3222	RI RA SYSTEMS	220422 <b>1</b> 123 22522	/73		13,1217
QUTPUT	REGISTER (2X24BIT DATA DUT, DATA + BUSY FORM HANDSHAKE, TTL)	PO=224	EGRG/ORTEC	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	/72		13,1218
	r REGISTER (2X24BIT OR 6X8BIT, ISPLAY)	OR	JOFRGER		/72	(7)	13,1219
24-BI	T DUAL OUTPUT REGISTER	9042	NUCL' FNTERPRISES	22 2 2 3 (1)	/72	(7)	13,1220
DUAL (	OUTPUT REGISTER (2X24BIT, DATAWAY AND WRITE, HANDSHAKE CONTROL, LO=Z)	9043A	NUCL. ENTERPRISES	1		(7)	13,1221
	(SAME RUT HI-Z)	90438		1		(7)	
PARALI	LEL OUTPUT REGISTER (2×24 BITS)	J RS 10	SCHLUMBERGER	1	173	(7)	13,1222
	24 BIT PARALLEL OUTPUT REGISTER LED DISPLAY OPTION)	PR=612	STND ENGINEERING	ung 66 <b>1</b> 50	/71	( 6)	
	AL OUTPUT REGISTER (4X8BIT PARALL T REGISTER, NO L,TTL,1=H)	00 200-2501	DORNIER	1	/71		13,1224
(	WITH FRONT PANEL CONNECTOR) (MODULE WITH ONLY LOGIC BOARD)	DO 200=2701 DO 200=2500		1			748773E
	AL OUTPUT REGISTER (4X8BIT PARALLEL UT REGISTER, HLL 12V)	DO 200-2505	DORNIER	1	/73		13,1225
(SAME	WITH FRONT PANEL CONNECTOR) , NO F.P. CONNECTOR, INVERTING) WITH FRONT PANEL CONNECTOR)	DO 200-2705 DO 200-2506 DO 200-2706		1 1	/73 /73 /73		
	AL OUTPUT REGISTER (4X8BIT PARALLEL	DO 200-2507	DORNIER	1	/73		13,1226
OUPTP (SAME (SAME	UT REGISTER, HLL 24V) WITH FRONT PANEL CONNECTOR) NO F'P' CONNECTOR, INVERTING)	DO 200=2707 DO 200=2508 DO 200=2708		1 1 1	/73 /73 /73		
	WITH FRONT PANEL CONNECTOR)	00 200=2708	SIEMENS	Ne and the second			13,1227
128 B	ER MODILES ALSO MARKETED BY SIEMENS IT OUTPUT REGISTER (ADDRESSABLE AS	c 342		1	/73		13,1228
	IT OR 128 1-BIT WORDS)						

#### Parallel Output Drivers (Open Coll., Relay, etc.) 133

TRIAC OUTPUT PEGISTER (8 BITS, 2 AMPS, ZERO VOLTAGE SWITCHING)	LT	JOFRGER	1	174	(13)	13,1229
8 CHANNEL TIMED TRIAC DUTPUT	3040	KINETIC SYSTEMS	2	174	(13)	13.1230
8 BIT TRIAC OUTPUT REGISTER	3080	KINETIC SYSTEMS	1	173		13,1231
12-BIT OUTPUT REGISTER (WITH OPTICAL ISOLATION, OPEN CULL D/P, MAX 30V/100MA)	3082	KINETIC SYSTEMS	1			13,1232
12-BIT OUTPUT REGISTER WITH ISOLATED RELAY	3087	KINETIC SYSTEMS	1	/71	(4)	13,1233
SHITCH (12BIT DATAWAY CONTROLLED RELAY REGISTER FOR SHITCHING AND MULTIPLEXING)	7066-1	NUCL. ENTERPRISES	1	/71		13,1234
DRIVER (16BIT, OPEN COLLECTOR OUTPUT VIA MULTIWAY CONNECTOR, MAX 150MA/LINE)	9002	NUCL. ENTERPRISES	1	/71		13,1235
OUTPUT REGISTER (16BIT, 48V/.05A MAX, 2X37=WAY O/P CONN)	360	POLON	1	/73		13,1236
OUTPUT REGISTER (16BIT,250V,1A MAX, 2X37=WAY O/P CONN)	360A		1	/73		
(SAME, 25V/1A MAX)	360B		1	/73		
RELAY DRIVER (16 WAY RELAY DUTPUT)	J RD 10	SCHLUMBERGER	1	/73	(8)	13,1237
PARALLEL OUTPUT REGISTER (1681T REED RE- LAY, MAX SWITCHED PWR 10W, 4 TIMING MODES)	C=OR=16	WENZEL ELEKTRONIK	1	/72	(10)	13,1238
DRIVER (24BIT DUTPUT REGISTER, SET AND READ BY COMMAND, 24BIT I/P DATA ACCEPTED)	9017	NUCL. ENTERPRISES	1	/71	( 1)	13.1239
N OUTPUT REGISTER (24 BIT, 40 HA 30V OUT) N (SAME INVERTED OUTPUTS)	9600B 9600C	NUCL. ENTERPRISES	0		(13)	13.1240
N OUTPUT REGISTER (24 BIT, 1 AMP 60V OUT) N (SAME WITH RELAY CONTACTS, MUX CONCEPT) N (SAME WITH RELAY CONTACTS, FREE CONTACTS)	9601 9602A 9602B	NUCL. ENTERPRISES	0 0		(13) (13) (13)	13,1241
OUTPUT REGISTER (2X16BIT, OPEN COLLECTOR)	1084	BORER	1	174		13,1242
OUTPUT DRIVER(2x16BIT, 40MA SINKING, 1=LO,	OD 1613	GEC-ELLIOTT	1	172		13,1243
DATAWAY READ & WRITE, LAM I/P, STRUBE O/P) (SAME, 1mHI)	OD 1614		1	/72		
OUTPUT DRIVER (2x16BIT, 125MA SINKING, 1=LO	OD 1617	GEC-ELLIOTT	1	/72		13,1244
DATAWAY READ & WRITE, LAM I/P, STRUBE O/P) (SAME, 1=HI)	OD 1618		1	/72		
OUTPUT DRIVER(2x16BIT,TOTEMPOLE,30 LOADS DATAWAY READ & WRITE,LAM I/P,STROBE O/P)	OD 1620	GEC-ELLINTT	1	/72		13,1245
2X16 OR 4X8 BIT OUTPUT REGISTER	J RS 30	SCHLUMBERGER	1	174	(11)	13,1246
DUAL 16 BIT OUTPUT REGISTER (TTL LEVELS, OPEN COLL OUTPUTS VIA CABLE)	20R 2008	SEN	1	/70		13,1247
DUAL DUTPUT DRIVER (200MA SINKING,24V)	20R 2051HC	SEN	1		(9)	13,1248
DUAL OUTPUT DRIVER (HI VOLTAGE DRIVER)	20R 2051HV	SEN	1		(9)	13,1249
DIGITAL OUTPUT (2X16BIT, MAX 30V)	C 76451-A9-A4	SIEMENS	1	173	( 6)	13,1250
OUTPUT REGISTER (2X16BIT VIA ISOLATING CONTACTS)	1082	BORER	1	/72	( 4)	13,1251
DIGITAL OUTPUT (2X16BIT RELAYS)	C 76451-A9-A3	SIEMENS	1	173	(6)	13,1252
PARALLEL-OUTPUT-REGISTER (DUAL 24BIT, OR GUAD 12BIT, OPEN COLLECTOR OUTPUT)	MS PO 1 1230/1	AEG-TELEFUNKEN	1	170	( 1)	13,1253
PARALLEL-OUTPUT REGISTER (24BIT, OPEN COLLECTOR DUTPUT, HANDSHAKE FACILITY)	MS PO 2 1230/1	AEG-TELEFUNKEN	1	/72	( 4)	13,1254
OUTPUT DRIVER(2X24BIT,40MA SINKING,1=LO, DATAWAY READ & WRITE,LAM I/P,STRORE O/P) (SAME, 1=HI)	OD 2403	GEC-ELLIOTT	1	/72		13,1255
OUTPUT DRIVER(2x24BIT,125MA SINKING,1=LO	DD 2407	GEC-ELLIOTT	1	172		17 1004
DATAWAY READ & WRITE, LAM T/P, STROBE D/P) (SAME, 1=HI)	DD 2408			/72		13,1256
OUTPUT DRIVER(2x24BIT,TOTEMPOLE,30 LOADS	DD 2410	GEC-ELLINTT	1	172		13,1257
DATAWAY READ & WRITE, LAM T/P, STROBE O/P)						
DUAL OUTPUT REGISTER (2X24BIT, OPEN COLL O/P, FULL LAM, OUTPUT STROBES)	200=2	HYTEC	1	/73		13,1258
OUTPUT REGISTER (2X24BIT OR 6XBBIT, 250MA SINKING, DIODE CLAMPED)	OR-1	JOERGER	1	/73		13,1259
DUAL 24 BIT OUTPUT REGISTER(DC OR PULSE O/P,UPDATING O/P STROBE,TTL OPEN COLL)	40	JORWAY	1	/71	( 5)	13,1260
DUAL 24 BIT OUTPUT REGISTER (DC OR PULSE O/P UPDATING, 300MA SINK, DIODE CLAMPED)	40-2	JORWAY	1	174		13,1261
				The second second		

DUAL 24-BIT OUTPUT REGISTER (OPEN COLL DRIVERS, MAX 24V OR 250MA, REAR CHIPPUTS)	3072	KINETIC SYSTEMS	1		13,1262
DIGITAL OUTPUT REGISTER (4X8BIT PARALLEL	DD 200-2502	DORNIER	1	/72	13,1263
OUTPUT REGISTER, NO L, OPEN COLL O/P, 1=HI) (SAME WITH FRONT PANEL CONNECTOR, 1=HI)	DU 200-2702		1	172	
(SAME, NO F.P. CONNECTOR, 1=LO)	DO 200-2503		1	172	
(SAME WITH F.P. CONNECTOR, 1=LO)	DO 200-2703		1	172	
DIGITAL OUTPUT REGISTER WITH REED RELAYS  (4xabit Output Reg,OPEN CONTACT=0)	DO 200-2504	DORNIER	1	/71	13,1264
(WITH FRONT PANEL CONVECTOR)	00 200-2704		1	/71	
DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMFNS			13,1265

Digital I/O, Peripheral and Instrumentation Interfacing modules — Serial and Parallel I/O Regs, Printer-, Tape-, DVM-, Plotter- and Analyser Interfaces, Step-Motor Drivers, Supply CTR, Displays 14

141	Serial Input	/Output	Modules	(General	Purpose)

	141 Serial input/Output iv	nodules (Gellelal F	urpose)				
	SERIAL INPUT/DUTPUT REGISTER 1681T CODED	9063	NUCL. ENTERPRISES	1	174	(13)	13,1266
	142 Parallel I/O Registers	(General Purpose)					
	UNIVERSAL INPUT/OUTPUT REGISTER (36BIT DATA+RANGE IN,12BIT REG D/P FOR CONTROL)	1031	BORER	1	/72	( 3)	13,1267
	UNIVERSAL INPUT/OUTPUT REGISTER	SPS 2090	NUCL. ENTERPRISES	1	01/75	(12)	13,1268
	16 BIT INPUT/OUTPUT REGISTER (O/P STAGES ON PLUGABLE PC, FP CONNECTOR)	IOR 2053	SEN	1	/74	(11)	13,1269
	INPUT/OUTPUT REGISTER (24 BITS IN, 12 BITS OUT, OPTICALLY COUPLED)	IOR-1	JOERGER	1	/74	(11)	13,1270
	INPUT/OUTPUT REGISTER (24BIT)	10 302	STND ENGINEERING	1	02/75		13,1271
N	INPUT/OUTPUT REGISTER (24817, INTEGRATED INPUT, OUTPUT STROBES, FULL LAM)	210	HYTEC	1	07/75		13,1272
N	INPUT/OUTPUT REGISTER (24 BIT, POS & NEG LOGIC O/P SINKING 450 MA)	9048	NUCL. ENTERPRISES	1			13,1273
	DUAL INPUT DUAL OUTPUT REGISTER (16BIT, TTL IN, OPEN COLL TTL OUT, MAX 40MA,30V)	C110	RDT	1	/72		13,1274
	INPUT/OUTPUT REGISTER(2X24BIT IN,2X12BIT OUT, 3 ENTRY MODES, LED DISPLAY)	IR=1	JOERGER	1	/72	(7)	13,1275
	BUFFER STORE/REGISTER (32×24BIT, WITH	104	HYTEC	1			13,1276
	EXTERNAL ADDRESSING FACILITY) (SAME, 32X24BIT, WITHOUT EXT ADDR) (SAME, 32X16BIT, WITHOUT EXT ADDR)	100		1	/72		
	BUFFER STORE/REGISTER (32X16BIT, WITH	105	HYTEC	1			13,1277
	EXTERNAL ADDRESSING FACILITY) (SAME, 16x24BIT, WITHOUT EXT ADDR) (SAME, 16x16BIT, WITHOUT EXT ADDR)	102 103		1 1	/72 /73		
	143 Peripheral Interfacing	Modules (For TTY)	, Tape etc.)				
	DESK CALCULATOR CTRL (DIEHL INTERFACE TO FHC 1301/02/11 AND FHC 1309)	FHC 1312	FRIESEKE	1	/72		13,1278
	INTERFACE FOR ASR33 TTY, SERIAL DATA LINK	6711	BI RA SYSTEMS	1	174		13.1279
	TELETYPE O/P CTRL (10 FHC 1301/02/11 AND FHC 1309 VIA SPEC CONN,TTY MOTOR ON/OFF)	FHC 1307	FRIESEKE	1	/71		13.1280
	TELETYPE INTERFACE	90	JORWAY	2	/71		13,1281
	TELETYPEWRITER INTERFACE(I/O DATA TRANSF AND CONTROL, LAM USED AS TWO-WAY FLAG)	7061=1	NUCL. ENTERPRISES	1	/7.0	(1)	13,1282
	TELETYPE INTERFACE (FOR ASR 33, SER I/O)	500	POLON	1	174		13,1283
	TERMINAL DRIVER	J TY 20	SCHLUMRERGER	1	/73	(11)	13,1284
	TELETYPE OR CRT INTERFACE	TCO 100	STND ENGINEERING	1	174		13,1285
	VERSATEC LINE PRINTER INTERFACE	3320	KINETIC SYSTEMS	1	172		13,1286
	INTERFACING OUTPUT UNIT(BRIT DATA, CONTR & STATUS REGS, FOR FACIT SP1 INTERFACE)	SP1/ACCEPTOR	ARSYCOM	1	/74	(12)	13,1287
(	PAPER TAPE PUNCH INTERFACE, COUPLES TO FACIT 4070, DATA DYNAMICS, RACAL DIGISTORE	TP 0801	GEC-ELLIOTT	1	01/75	(1)	13,1288
	INTERFACING INPUT UNIT (8817 DATA/STATUS & CONTR REGS, FOR FACIT SP1 INTERFACE)	SP1/SOURCE	ARSYCOM	1	174	(12)	13,1289
(	C PAPER TAPE READER INTERFACE (COUPLES TO LINHOOD, TREND, & RACAL DIGISTORE)	TR 0801	GEC-FLLINTT	1	01/75	(1)	13,1290

NC DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
MAGNETIC TAPE INTERFACE (TAPE DECKS OF CASSETTES)	CS 0042	NUCL. ENTERPRISES	1	/73	(8)	13.1291
CASSETTE INTERFACE (READS & WRITES BY B	J CK 10	SCHLUMRERGER	1	/75	(12)	13.1292
CASSETTE DRIVER FOR 1 CASSETTE CASSETTE DRIVER FOR 2 CASSETTES	C CK 10 C CK 11			/75 /75	(12)	
PORTABLE CASSETTE DRIVER(FOR 1 CASSETTE)	P CK 10	SCHLUMBERGER		/75		13,1293
N DISK DRIVE FOR CDS=110 N INTERFACE FOR DISK DRIVE	9370 9370	NUCL. ENTERPRISES	NA O		(13)	13,1294
UNIVERSAL ASYNCHRONOUS TRANSMITTER/RECEIVER (129 CHAR.BUFFER)	C 317	INFORMATEK	1	/73	(13)	13,1295
PERIPHERAL READFR(8BIT PARALLEL DATA IN, NEG OR POS TTL, MANDSHAKE CONTROLS)	7064-1	NUCL. ENTERPRISES	1	/71	(1)	13.1296
PERIPHERAL DRIVER (8BIT DATA DUT, NEG OR POS TTL, HANDSHAKE CONTROLS)	7065-1	NUCL. ENTERPRISES	1	/71	(1)	13,1297
144 Display Modules, Disp	olay and Plotter I	nterfacing				
24 BIT LED BCD DISPLAY (ONE FHC 1301/02/11 VIA SPEC CONNECTOR)	FHC 1305	FRIESEKE	1	/71	(1)	13,1298
24 BIT NIXIE BCD DISPLAY (SELECTS ONE OF	FHC 1306	FRIESEKE	2	/71	(1)	13,1299
10 FHC 1301/02/11 VIA SPEC CONNECTION)  24 BIT LED BINARY DISPLAY (ONE FHC 1313	FHC 1315	FRIESEKE	1	/72		13,1300
OR FHC 1309 VIA SPECIAL CONNECTION) DECIMAL DISPLAY UNIT (ADDRESS AND 5 DATA		To Maria de				
DECADES + MULTIPLIER DISPLAYED) DISPLAY CONTROLLER (FOR 9007, INCLUDES BIN TO DECIMAL CONVERTER)	9007	NUCL. ENTERPRISES	NA 2	/71		13,1301
COLOUR DISPLAY INTERFACE	9062	NUCL. ENTERPRISES	NA	04/75	(12)	13,1302
EXTERNAL DISPLAY FOR J EA 10 SCALER	C AE 10	SCHLUMBERGER	NA	/73		13,1303
SCALER DISPLAY THROUGH, COMPUTER (DISPLAY OF 24BIT WORD, 30MHZ)	J AF 15	SCHLUMBERGER	2	/71		13,1304
MANUAL BINARY DISPLAY (CONTENT OF A REGISTER DISPLAYED, EXT MULTIWAY CONN)	J AF 20	SCHLUMBERGER	1	/71		13,1305
GRAPHIC DISPLAY DRIVER FOR HP1311/TEK604	4301	BI RA SYSTEMS	1	174		13.1306
GRAPHIC DISPLAY DRIVER FOR STORAGE DISPLAY TEK 602	4301A	BI RA SYSTEMS	2	174		13,1307
N INTERACTIVE GRAPHICS DISPLAY PROCESSOR N 128 CHARACTERS, 9X7 DOT MATRIX, 4 SIZES, VECTORS.ARCS,CIRCLES IN THREE LINE TYPES	DP 1603 DP 1603A	GEC-ELLIOTT	4 2	09/75		13,1308
N LIGHT PEN & TRACKER BALL INPUTS. 32 CON- TROL INSTRUCTIONS. BUILT IN 4K STORE.	DP 1603B		2			
CRT DECIMAL DISPLAY SYSTEM (INCLUDING) DISPLAY DRIVER	72A 72A	JORWAY	NA 5	/71	( 5)	13.1309
DISPLAY SYSTEM COMPRISING DISPLAY SYNCHRONIZING	3200	KINETIC SYSTEMS	1	/71 /71	(4)	13,1310
(COMPATIBLE WITH 60HZ 525 LINE MONITORS) DISPLAY SYNCHRONIZING (COMPATIBLE WITH 50HZ 625 LINE MONITORS)	3200E		1	174	(12)	
DISPLAY TIMING DISPLAY CONTROL	3205		1	/71		
DISPLAY REFRESH (ALPHANUMERIC + GRAPHS) DUAL LIGHT PEN INTERFACE	3210 3212		1	771		
COLOR MONITOR	3225 RGB 5200 M		1	171		
STORAGE DISPLAY DRIVER	3260		1	172		
DISPLAY DRIVER (TWO 10BIT DAC, OUTPUT RANGE +5V TO =5V, TWO OPERATION MODES)	7011=2	NUCL. ENTERPRISES	2	170	(1)	13,1311
STORAGE OSCILLOSCOPE (DRIVER FOR TEKTRONIX 611 OR 601, USED WITH 7011)	9028	NUCL. ENTERPRISES	1	/71	( 2)	13,1312
SCOPE DISPLAY DRIVER MANUAL CONTROL OF J DD 10	J DD 10 MC 10	SCHLUMBERGER	NA NA	/73	(7)	13,1313
SCOPE DISPLAY DRIVER X=Y=Z (SYSTEM) STORAGE DISPLAY DRIVER FOR TEKTRONIX 611 OR 601	FDD 2012 SDD 2015	SEN	1 1	/71 /71	(1)	13,1314
CHARACTER GENERATOR VECTOR GENERATOR LIGHT PEN FOR FOD 2012 OR CG 2018	CG 2018 VG 2028 LP 2035		1 1	/71 /71	(1)	
PLOTTER DRIVER	J XY 10	SCHLUMBERGER	1	/71	(8)	13,1315
145 Instrumentation Interfa Pulse Analyser CTR)	cing Modules (D	OVM, Supply CTR, Steppi	ng Motor	Drivers,		

BI RA SYSTEMS

13,1316

DUAL 15 CHANNEL SERIAL OUTPUT MODULE (STEPPER MOTOR CONTROLLER, TTL)

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	DTOR PRIYER (MAX 32760 STEPS, PATE, DN AND START/STOP FILLY COMMANDED)	1161	BORER	10019	/72	(3)	13,1317
	IG MOTOR CONTROLLER & DRIVER TABLE ACCEL/DECEL, TIME & MAX FREQ)	SMC	JOERGER	1	174	(13)	13,1318
	G MOTOR CONTROLLER, DUAL	3360	KINFTIC SYSTEMS	1	/72	(4)	13,1319
STEPPIN	NG MOTOR CONTROLLER, ACCELERATING	3361	KINETIC SYSTEMS	1	/73		13.1320
STEPPIN	G MOTOR DRIVER (USED WITH 7045)	0709	NUCL. ENTERPRISES	1	/71		13,1321
	PULSE GENERATOR (4 TTL 0/P,0.042 Z RATE, LEVEL AND DIRECTION CONTR)	7045-1	NUCL . ENTERPRISES	1	/70		13.1322
	NG MOTOR DRIVER FOR J CP 20	J CP 20 C APP 10	SCHLUMBERGER	1	/74 /74	(9)	13,1323
	OUS STEPPER CONTROL (65536 STEPS, DN/DIRECT'/SPEED/ACCELER, CONTROL)	C=ST=4	MENZEL ELEKTRONIK	2	172		13,1324
	NTAL STEPPER CONTROL (65536 STEPS, DN/DIRECT'/SPEED/ACCELER, CONTROL)	C-ST-4-I	MENZEL ELEKTRONIK	2	/72		13,1325
VARIABL MODULE	E PULSE DURATION TRIAC OUTPUT	3701	BI RA SYSTEMS	2	174		13,1326
	DUTPUT REGISTER . 2 AMPS, ZERO VOLTAGE SWITCHING)	LT	JOERGER	1	/74	(13)	13,1327
POWER S	SUPPLY CONTROLLER 12-BIT	3158	KINETIC SYSTEMS	1	/73		13,1328
CAMAC-1	TO-SCIPP PHA INTERFACE	2323	BI RA SYSTEMS	2	/73		13.1329
	ACE CAMAC-TO-LABEN 8000SERIES	5380	LABEN	3		(12)	13.1330
	AC INTERFACE (FOR PULSE ADC 8215, 211,8212,8112 & T=0=F CONV 8270)	5910	LABEN	1		(12)	13,1331
	HANNEL ANALYZER - CAMAC INTERFACE ACKARD 9000 AND 900 SERIES MCA)	9701	PACKARD	3		( 4)	13,1332
	TO DIGITAL CONVERTER E AND MULTI-TURN CAPABILITIES)	SDC	JOERGER	2	/73	(13)	13,1333
DUAL SY	NCHRO-DIGITAL CONVERTER (14817)	CS 0047	NUCL. ENTERPRISES	2	/73		13,1334
	NCREMENTAL POSITION ENCODER (2X20 y DIGITIZATION BY UP-DOWN COUNTER)	21PE 2019	SEN	1	. /71		13,1335
	ACE FOR MEASURING DEVICES (DUAL INPUT FOR 2 INSTRUMENTS)	DO 200=1412	DORNIER	1	174	(10)	13,1336
	REGISTER (16 OR 24 BIT TTL DRIVER ST-ROUTING MULTIPLEXER SYSTEM)	CM 665	J AND P	1	/71		13,1337
PULSE I	DURATION DEMODULATOR	3720	KINETIC SYSTEMS	1	/73		13,1338
PLUMBIC	CON READ OUT TERMINAL .	J PG 10/PUDDING	SCHLUMBERGER	0 1	/71	(6)	13,1339
	CON READ OUT (5 SCALERS RECORD ZED DUTPUTS FROM PLUMBICON CAMERA)	J PM 10/PLUM	SCHLUMBERGER	1	/71	( 6)	13.1340
SPARK (	CHAMBER READ OUT	J SC 10		2	/72		
	MAC INTERFACE (FOR ANY ADC, 2X16BIT FFER, STATUS, LAM HANDL, CLOCK TIME)	C-A1-2	WENZEL ELEKTRONIK	1	/73	(10)	13,1341
	147 Other Digital I/O M	odules (Incl. Data Link	(s)				
	DATA LINK MODULE T PARALLEL, ASYNCHRONOUS DATA LINK)	6701	RI RA SYSTEMS	2	/73		13.1342
BIT-SY	NCHRONIZER - HARDWARE PROGRAMABLE OV INPUT, PCH-SIGNAL IN SERIES	00 200-2251	DORNIER	3	/73		13,1343
FORMAT	-SYNCHRONIZER (IDENT & S/P OF DATA SOFT- & HARDWARE PROGRAMMABLE)	DO 200=2260	DORNIER	4	/73		13,1344
COMMUN	ICATION INTERFACE (V24/V23/V21 INTERFACE WITH AUTO-DIAL OPTION)	DD 200-2911	DORNIER	1	/73	(10)	13,1345
START-	STOP CONTROLLER(START, STOP, RESET, OR DATAWAY CONTROL, 100HZ CLOCK)	FHC 1304	FRIESEKE	1.	/71	(1)	13,1346
SERIAL	INTERFACE (V24 SPEC, QUAD VERSION LE TRANSMISSION RATES)	9045	NUCL. ENTERPRISES	1	/73	(13)	13,1347
START-	STOP UNIT (START, STOP CLOCK AND	J AM 10	SCHLUMBERGER	1	/71		13,1348
FOUR FO	DLD BUSY DONE (START SIGNAL TED BY COMMAND, DEVICE RETURNS LAM)	4BD 2021	SEN	1	/71		13,1349

BINARY TO DECIMAL CODE CUNVERTER (24 BIT BINARY TO 8 DECADE)

BCD TO BINARY CONVERTER (29817 BCD TO 24817 BINARY, CONV TIME 325 NSEC)

BINARY TO BCD CONVERTER (CONV TIME 325 NSEC, 24BITS TO MAX 16777216=1 BCD CODED)

BINARY TO BCD-CONVERTER(24BIT TO 8 DECA-DE,DISPLAY,CONV 4USEC,TTL LEVEL OUT,1=H)

15 Digital Handling and Processing Modules — and/or/nor Gates, Fan-Outs, Digital Level and Code Converters, Buffers, Delays, Arithm. Processors etc.

Delays, Arithm. Pr	ocessors etc.				
151 Fan-Outs, and/or/no	t-Gates			and the second of	
FAN=DUT UNIT (2 DRED INPUTS PROVIDE 8 TRUE,2 COMPLEM DUTPUTS,NIM SIGNALS)	FO 0801	GEC-FLLINTT	1	/71	13.1350
NIM FANDUT (DUAL FOUR FOLD & COMPLEMENT, NIM DRIVER, =14MA INTO 500HMS)	FON	JOFPGER	1	/73	13,1351
TTL FANOUT (DUAL FOUR FOLD & COMPLEMENT, TTL DRIVER, 50MA CURRENT SINK)	FOT	JOERGER	1	/73	13,1352
NIM FANOUT (7=ORED INPUTS, 8 O/P+2 COMPL O/P GATED FROM DATAWAY)	216	JORWAY	1	/75	13,1353
FAN OUT MODILE (IL2 I/P, 16 IL2 O/P)	9050	NUCL. ENTERPRISES	1	/73	13,1354
SIX=FOLD CONTROLLED GATE (INDIV GATING, FAN=IN AND FAN=OUT CONTROLLED BY 3 REGS)	6CG 2017	SEN	1	/71 (4)	13,1355
C FAST LOGIC UNIT (4X4 NIM INPUTS)	FLU 2062	SEN	1	(12)	13,1356
152 Digital Level Convert	ers				
6 CHANNEL TTL/NIM CONVERTER	5601	RI RA SYSTEMS	1	/73	13,1357
6 CHANNEL NIM/TTL CONVERTER	5602	BI RA SYSTEMS	1	/73	13,1356
HEX CONVERTER (NIM TO TTL LEVELS PLUS THO COMPLEMENT OUTPUTS)	CNT	JOERGER	1	/73	13,1359
HEX CONVERTER (TTL TO NIM LEVELS PLUS TWO COMPLEMENT OUTPUTS)	CTN	JOERGER	1	/73	13.1360
MEX IL1 TO IL2 CONVERTER (6 TTL SIGNALS IN,6 NIM SIGNALS OUT)	7052-1	NUCL'. ENTERPRISES	1	/70	13,1361
153 Code Converters					
DECIMAL INPUT 6 NUMBERS	DD 200-2005	DORNIER	2	/74	13,1362
3 DIGITS CODE CONVERTER (SAME BUT 3 NUMBERS)	DO 200=2006		2	174	
CAMAC BCD=TO=BINARY CONVERTER	LEM-52/5.7	EISENMANN	1		13,1363
CAMAC BINARY=TO-BCD CONVERTER WITH DECIMAL DISPLAY	LEM=52/5.8	EISENMANN	1		13,1364
GRAY CODE TO BCD CONVERTER (DUAL CHANNEL INPUT WITH MEMORY)	EIR	JOERGER	1	174	13,1365
BINARY CODE CONVERTER (BIN-BCD OR BCD-BIN CONVERSION, DATA FROM DATAMAY OR FRONT)	9044	NUCL. ENTERPRISES	1	( 7)	13,1366

154 Buffer Memories, Stor	age Units					
PROGRAM STORE/RFGISTER (256×24817 RAM + 64×24817 ROM, Ext ADDR, USE WITH 7025-2) (SAME BUT WITHOUT EDIT ROM) (SAME BUT NO BUFFER AND NO EXT ADDR)	110A 110 112	НҮТЕС	1 1 1	/73		13,1371
N 1024 WORD 24 BIT STATIC STORE (NORMAL & BYTE MODES, CLEAR, INCR, DECR, READ, & OVERWRITE ON ADDRESS REG ARE PERFORMED) N (SAME WITH MEMORY ACCESS ALSO FROM FRONT	130	HYTEC	1 2	07/75		13,1372
PANEL. MASTER/SLAVE OPERATION) 3-DECADE ADC 8 16-WAY MUX (PRESET X1-X10	131 500=1	HYTEC	1	08/75 /73		13,1373
AMPL, 16x24 STORE, 100USEC/CH UPDATE)  N (SAME AS 500=1 BUT WITH 8=WAY MUX) (SAME BUT BINARY ADC)  N (SAME AS 501 BUT WITH 8=WAY MUX) (SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	502 501 503 510		1 1 1 2	/74 /74 /74 /74		
N 256 WORD FIFO BUFFER (24 BITS PER WORD)	3841	KINETIC SYSTEMS	1	05/75	(13)	13,1374
2048-WORD 16 BIT STORE	9061	NUCL. ENTERPRISES	2		(10)	13,1375
16 WORD STORE	CS 0003	NUCL. ENTERPRISES	1		(4)	13,1376

STND ENGINEERING

STND ENGINEERING

WENZEL ELEKTRONIK

/73

173

(12)

(12)

13,1368

13,1369

13.1370

CD 001

CD 002

C-88C-24

NC DESIGNATION	ON & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
256 WORDS OF 24 BIT S	STURE MODULE	CS 0015	NUCL. ENTERPRISES	1	/72	(7)	13,1377
PROGRAMMABLE READ ONL	Y MEMORY (32 WORDS,	221	POLON	1	03/75		13.1378
BUFFER MEMORY (256 168IT WURDS, US	E WITH J CAN 21/C/H)	J MT 20	SCHLUMBERGER	1	/72		13.1379
CAMAC CORE MEMORY MO		MM 216C MM 416C MM 816C MM 224C MM 424C	STND ENGINEERING	3 3 3 3	/74 /74 /74 /74 /74	(12) (12) (12) (12) (12) (12)	13.1380
155	Logic and Arithmetic	Processing Modules					
PLOATING POINT ARITH		C 327	INFORMATEK	1	/73		13,1381
N 96 CHAN. DRIFT CHAMB		2770	LRS-LECROY	2	05/75	(13)	13,1382
F.S., 8 BIT, 32 DEEP N 128 CHAN, MWPC ENCOD LATCH, ENCODER, 80 H	BUFFER, DIFF I/P) ER (RECEIVER, DELAY,	2720		2	05/75	(13)	
16	Analogue Modules Linear Gates, Disci		Aultiplexers, Amplif	iers,			
161	Analogue Input Modu	les (DC and Pulse A	ADC, TDC)				
32 CHANNEL ANALIG DA (EXPANDABLE WITH ADD	TA SYSTEM ITIONAL MUX MODULES)	5301	RI RA SYSTEMS	2	174		13,1383
	L SLOPE ADC, +/-16V N,0.2SEC CONVERSION)	DO 200-1021	DORNIER	1	/72		13,1384
IN CONVERTER CARDS A	INTEFACE (WITH PLUG- DC/8Q, ADC/100 AND D 12 BIT CONVERSION)	ADC 1201	GEC-ELLINTT	1	/71	(-1)	13,1385
N 16 CHANNEL, SCANNING		3510	KINETIC SYSTEMS	1	174		13,1386
INTEGRATING ADC (128 0 TO =5V, 40MSEC CON	IT, RANGES 0 TO +5V, VERSION TIME)	700	POLON	1	/73		13,1387
VOLTAGE - FREQUENCY		J CTF 10	SCHLUMBERGER	2	/73		13,1388
(USED WITH MULTI UP-DOWN SCALER/FREQU	PLEXERS J MX 10/20) PENCY METER	J EF 10		1	/73		
DUAL DIGITAL VOLTMET 10 BIT, DIFFERENTIAL		2DVM 2013	SEN	1	/71		13,1389
DIG. VOLTMETER (128) RANGES = AC/DC .02V	T + SIGN, POT-FREE 20V,DC 5-100MA)	C 76451=A13=A1	SIEMFNS	2	/73		13.1390
DIGITAL VOLTMETER (S TYPE C 76451-413-41	BAME AS WITH DISPLAY)	C 76451-A13-A2	SIEMENS	2	/73		13,1391
8 DIFF I/P,+/-10V RA	ULTIPLEXER-ADC, ANGE, 78178/10V+SIGN)	DO 200=1013	DORNIER	2	/72 /72		13.1392
(SAME FOR +/-5V RANGE (SAME FOR +10V RANGE		00 200=1016 00 200=1019		2	172		
DORNIER MODULES ALSO	MARKETED BY STEMENS		SIFMENS				13,1393
ANALOG INPUT (AU 7BITS/10V+SIGN)	C. +/=10V RANGE,	DO 200-1027	DORNIER	2	/72		13,1394
(SAME FOR +/-5V RANGE (SAME FOR +10V RANGE		DD 200=1028 DD 200=1029		5	172		
ANALOGUE TO DIGITAL RANGE 0 TO +5V OR 0	CONVERTER(8BIT, I/P TO =5V,25 USEC CONV)	7028-1	NUCL. ENTERPRISES	i	/70		13,1395
HIGH SPEED DIGITIZES RESOLUTION, WITH 25		SA/D 01	STND ENGINEERING	1	/74	(12)	13.1396
DUAL 10 BIT ANALOG	TU DIGITAL CONVERTER	3515	KINETIC SYSTEMS	1	/73		13,1397
SINGLE 10BIT ANALOG	TO DIGITAL CONVERTER	35158	KINETIC SYSTEMS	1	174		13,1398
DUAL ADC (10BTT, 10	USEC CONV TIME)	A/D 210	STND ENGINEERING	2	03/75		13,1399
DUAL SLOPE ADC (+AN 11BIT RESOLUTION, 20	D= 0.01/1/10V RANGES, MS CONV TIME)	1241	BORER	2	/72	(3)	13,1400
SUCCESS. APPROX', AD 0 TO +/=10V, 10=BIT	C (WITH S+H, +/=5V OR ,20/11 USEC ACCESS)	1243/1243A	RORER	2	/72	(9)	13.1401
	C (WITH S+H, +/=5V UR ,23/13 USEC ACCESS)	1244/12444	RORER	2	/73	(9)	13.1402
ANALOG INPUTS (	MULTIPLEXER-ADC, ANGE, 118173/10V+SIGN)	nu 200=1003	DORNIER	,5	/72		13,1403
(SAME FOR +/=5V RANG	GE, 11BITS/5V+SIGN)	00 200-1006 00 200-1009		2 2	/72 /72		

							REF. No.
	ANALOG INPUT (ADC, +/=10V RANGE, 11BITS/10V+SIGN)	DO 200-1024	DORNIER	2	172		13.1404
	(SAME FOR +/=5V RANGE, 11BTTS/ 5V+SIGN) (SAME FOR +10V RANGE, 12BTTS/10V)	DO 200-1025 DO 200-1026			/72 /72		second Le. 47
	OCTAL ADC (8X11RIT + OVF, POS INPUT, 1 MV RESOL, COMMON STRUBE, FAST CLEAR)	AD811	FG8G/NRTEC	1	03/75	(13)	13,1405
	3-DECADE ADC & 16-WAY MUX (PRESET X1-X10 AMPL, 16X24 STORE, 100USEC/CH UPDATE)	500=1	HYTEC	* i **	/73		13,1406
N	(SAME AS 500=1 BUT WITH B=WAY MUX) (SAME BUT BINARY ADC)	502 501		1 1	174		
N	(SAME AS 501 BUT WITH B=WAY MUX) (SAME, BUT AMPL GAIN CAN BE SET AND STORED INDIVIDUALLY/CHANNEL, BCD/BIN)	503 510		1 2	174		
	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM-1	JOERGER	2	174	(11)	13,1407
	A/D CONVERTER (128IT, MAX 20 USEC CONVERSION, +AND=5V, +AND=10V, +10V RANGES)	30	JORWAY	2	/71	(2)	13,1408
	16 CHANNEL A/D CUNVERTER (FET MUX DIFF INPUTS, 1281T AUTO CYCLING, DUAL SLOPE)	34	JORWAY	2	174		13,1409
	DUAL 12 BIT ANALUG TO DIGITAL CONVERTER	3520	KINETIC SYSTEMS	1	/73		13,1410
	SINGLE 1281T ANALOG TO DIGITAL CONVERTER	35208	KINETIC SYSTEMS	01.10	174		13,1411
N	INSULATED ADC (128ITS, 100 USEC, 10MV, FULL SCALE, 300V COMMON MODE)	TADC 2069	Cares Disc Nas 10	2			13.1412
	DUAL ADC (12817, 25USEC CONV TIME)	A/D 212	STND ENGINEERING	2	03/75		13,1413
N	DIGITAL VOLTMETER (19.999MV TO 1999.9V)	CS 0080	NUCL' ENTERPRISES	2		(13)	13.1414
	DUAL ADC (14BTT, 50USEC CONV TIME)	A/D 114	STND ENGINEERING	1	03/75		13,1415
	OCTAL CHARGE DIGITIZER (8×88IT CHARGE SENSITIVE ADC, READOUT IN 4×168IT WORDS)	QD808	EGRG/ORTEC	1		(7)	13.1416
	QUAD FAST GATED INTEGRATOR (CHARGE DIGITIZER, 4×10 BIT)	QD410	FG&G/ORTEC	50 (9 <b>1</b> - 1 - 23 (99)	174	(10)	13,1417
	OCTAL ADC (A FAST I/P,881T/CH, COMMON GATE, NIM LEVELS, BILINEAR MODE)	2248	LRS-LECROY	1	/71		13.1418
	12-CHANNEL ADC (12 FAST I/P, 10BIT/CH, ,25PC SENSITIVITY, FAST CLEAR)	22494	LRS-LECROY	2 - <b>1</b>	174	(9)	13,1419
N	12-CHAN. FAST CONV. ADC (3US/8BIT, 9US/9 BIT, 12 EVENTS x 32 DEEP RUFFER, 0-256PC)	2250	I RS-LECROY	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	04/75	(13)	13,1420
c	12-CHANNEL PEAK ADC (10BIT/CH, =2V FULL SCALE, FAST CLEAR, COMMON GATE)	2259	LRS-LECROY	1	02/75	(13)	13.1421
	OCTAL ADC (MIN 5 NSEC PULSES, POS OR NEG 8BIT/100 PC RESOLUTION, 250 USEC CONV)	9040	NUCL. ENTERPRISES	1	/72	( 4)	13,1422
	ANALOGUE TO DIGITAL CONVERTER (80MHZ, 12 BITS)	9060	NUCL. ENTERPRISES	1	/74	(10)	13.1423
	15,000 CHANNEL PULSE ADC (200MHZ CLOCK)	J CAN 21 C/H	SCHLUMBERGER	6	172	( 6)	13.1424
	1024 CHANNEL PULSE ADC (100MHZ CLOCK)	J CAN 40	SCHLUMBERGER		172	(6)	13.1425
	FAST ADC(10 & 12BIT VERSIONS, WITH SAMPLE AND HOLD, CONV TIME 2USEC/4.5USEC)	FADC 2067	SEN		DATE VEX	(12)	13,1426
	FAST DUAL ADC (DATA AS FOR 2067)	2 FADC 2068		2		(12)	
	EVENT TIMER(4-CHANNEL TIME DIGITIZER, 88	2205	RI RA SYSTEMS				13,1427
	QUAD CAMAC SCALER (4X16bIT OR 2X32BIT, 100MHZ)	1004A	RORER	1	01/75		13,1428
	TIME DIGITIZER (4X16BIT, 50MHZ CLOCK, WITH CENTRE FINDER, USABLE WITH PRE-AMP 511)	1005	RORER	1	/72		13,1429
	TIME DIGITIZER (4 NIM STOP CHANNELS, COMMON START, 200 PSECS RESOLUTION)	TD104		1		(7)	13.1430
	OCTAL TDC (AX11RIT+OVF, COMMON START, 100PSEC RESOLUTION, FAST CLEAR)	TD811	EG&G/ORTEC		03/75	(13)	13,1431
	TIME DIGITIZER (6 CHANNELS, 16 HITS, 100 MHZ CLOCK RATE)	TD		(100 <b>1</b> 0 tell		(11)	13,1432
	QUAD TIME=TO=DIGITAL CONVERTER(9BIT/CH, 102/510NSEC RANGES, 13USEC CONVERS, NIM)	2226A		1 1	170	(2)	13,1433
c	UCTAL TIME=TU=DIGITAL CONVERTER(10RIT/CH 102/204/510 NSEC RANGES, FAST CLEAR)	2228	LRS-LECROY	1	174		13,1434
	96 CHAN. DRIFT CHAMBER TDC (.5US/1US F.S., 8 BIT, 32 DEEP BUFFER, DIFF I/P)	2770	LPS-LECRNY		05/75	(13)	13,1435
N	128 CHAN, MWPC ENCODER (RECEIVER, DELAY, LATCH, ENCODER, 80 HIT BUFFER, DIFF I/P)	2720			05/75	(13)	
	SIXTEEN FOLD TIME-TO-DIGITAL-CONVERTER				174		13,1436

NC DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
TIME DIGITIZER (4X168IT, CLOCK RATE 70/85MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1 2	/72		13,1437
TIME DIGITIZER (4X16BIT, CLOCK RATE 70/85MHZ, NIM LEVELS)	TD 2041	SEN	i .	/72	( 4)	13.1438
SERIAL TIME DIGITIZER (8x8BIT 100MHZ, SER + SEQUENT COUNT MODE, SHIFT=REG GATE)	STD 2050	SEN	1	/72		13,1439
OCTAL TIME TO DIGITAL CONVERTER	TD 008	STND FNGINEERING	1	04/75		13,1440
162 Analogue Output Mo	odules (DAC)					
8 CHANNEL 8 BIT D/A CONVERTER (CURRENT OR VOLTAGE O/P, SLOW ANALOG METER DRIVER)	5405	BI RA SYSTEMS	1	/73		13,1441
ANALOG DUTPUT (DAC, +10V D/P RANGE, 5MA, BRIT RESOLUTION, SINGLE D/P)	PO 200-1511	DORNIER	1	/73		13,1442
(SAME WITH 12BIT RESOLUTION, SINGLE O/P) (SAME WITH BOTT RESOLUTION, DUAL O/P) (SAME WITH 12BIT PESOLUTION, DUAL O/P) (SAME WITH BOTT RESOLUTION, QUAD O/P) (SAME WITH 12BIT RESOLUTION, QUAD O/P)	DO 200=1521 DO 200=1512 DO 200=1522 DO 200=1517 DO 200=1527		1 1 1 1	/73 /73. /73 /73 /73		
ANALOG DUTPUT (DAC,+8=10V D/P RANGE,5MA, 8BIT RESOLUTION, SINGLE D/P)	00 200-1513	DORNIER	1	/73		13,1443
(SAME WITH 128IT RESOLUTION, SINGLE O/P) (SAME WITH 8BIT RESOLUTION, DUAL O/P) (SAME WITH 128IT RESOLUTION, DUAL O/P) (SAME WITH 8BIT RESOLUTION, GUAD O/P) (SAME WITH 128IT RESOLUTION, GUAD O/P)	DO 200=1523 DO 200=1514 DO 200=1524 DO 200=1518 DO 200=1528		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	/73 /73 /73 /73 /73		
ANALOG DUTPHT (DAC, +8+5V O/P RANGE,5MA, BBIT RESOLUTION, SINGLE O/P)	DO 200=1515	DORNIER	1	/73		13.1444
(SAME WITH 12BIT RESOLUTION, SINGLE U/P) (SAME WITH 8BIT RESOLUTION, DUAL 0/P) (SAME WITH 12BIT RESOLUTION, DUAL 0/P) (SAME WITH 8BIT RESOLUTION, GUAD 0/P) (SAME WITH 12BIT RESOLUTION, GUAD 0/P)	DO 200=1525 DO 200=1516 DO 200=1526 DO 200=1519 DO 200=1529		1 1 1 1 1	/73 /73 /73 /73 /73		
DORNIER MODULES ALSO MARKETED BY SIEMENS		SIFMENS				13,1445
OCTAL DAC (10BIT,0=5V,500HMS,10USECS) (SAME BUT WITH 2'S CUMPLEMENT 9BIT+SIGN, +AND= 5V, 500HMS)	DAC 1082 DAC 1082(B)	GEC-ELLIOTT	1	/73 /73		13.1446
GUAD DAC (4 CHANNEL VERSION OF DAC 1082) (SAME, 4 CHANNEL VERSION OF DAC 1082(B)	DAC 1042 DAC 1042(B)	GEC-ELLIOTT	1 1	174		13.1447
N DUAL 12 BIT DAC (+/= 10V OR +/= 5V O/P, FOR X=Y DISPLAY DRIVE)	550	HYTEC THE STATE	1	10/75		13,1448
DUAL D/A CONVERTER (10 BIT, 1008EC CONV TIME, +10V, +AND=10V, +AND=5V RANGES)	D/A=10	JOERGER	1	/73	(13)	13,1449
DUAL D/A CONVERTER (12 BIT, 30USEC CONV TIME, +10V, +AND=10V, +AND=5V RANGES)	D/A=12	JOERGER	1 1	/73	(13)	13,1450
OCTAL D/A CONVERTER (BBIT RESOLUTION, O TO 2MA OR O TO +10V DUT)	8 D/A	JOERGER	111	/73	(13)	13,1451
D/A CONVERTER (128IT,5 USEC CONVERSION, O/P RANGES +AND=2.5V/5V/10V AND +5V/10V)	31	JORWAY		/71	( 2)	13,1452
8 CHANNEL 10 BIT D-A CONVERTER	3110	KINETIC SYSTEMS	1	/72		13,1453
DUAL DIGITAL=TO=ANALOG CONVERTER (10BIT, OUTPUT 0 TO +10v OR =5 TO +5v)	2DAC 2011	SEN '- A BOTTO	905 <b>1</b> 5A	/71		13,1454
DUAL DAC (12BIT, +AND=10V DR +AND=20MA)	C 76451-A15-A4	SIFMENS	1	/73		13,1455
ISOLATED DUAL DAC (10817,30USEC,10V/5MA, OPTOCOUPLER,4 TIMING MUDES,RANGE-MODIF)	C-DA-210	MENZEL ELEKTRONIK	13041 32	/74		13,1456
QUAD DAC (8RIT,10USEC,5V/50MA,4TIMING-M, +,- grange modif, npt, ground-rej&,5USEC)	C=DA=408	WENZEL ELEKTRONIK	0.1001	174	(11)	13.1457
QUAD DAC(10RIT, 10USEC, 5V/50MA, 4TIMING+M, +, - &RANGE MODIF, OPT, GROUND-REJ&, 5USEC)	C=DA=410	WENZEL ELEKTRONIK			(11)	13,1458
164 Analogue Handling a	nd Processing Modu	ules I (MX)				
SEE ALSO DORNIER ADC TYPES						13.1459
12 INPUT ANALOGUE MULTIPLEXER (PANDOM OR SCAN ACCESS CONTROLLED BY SKIP REGISTER)	MX 2025	SEN SEN			( 6)	13,1460
N 12-CHANNEL ANALOGUE MULTIPLEXER (FET, 5 USEC SWITCHING TIME, +/-10v)	MX 2070	SEN				13,1461
N WIDE-BAND ROUTER (12-CHANNEL 50 OHMS ANALOGUE MULTIPLEXER)	WBR 2073	SEN	1 - 1			13,1462
15 CHANNEL MULTIPLEXER (ANALOGUE SIGNALS ROUTED TO ANC/DVM, DIRECT + SCAN MODES)	1701	RORER	8 1 1 1 1 C			13,1463
DORNIER MODULES ALSO MARKETED BY SIEMENS		SIEMENS				13,1464

ı	NC DESIGNATION & SHORT DATA	ТҮРЕ	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	RELAY MULTIPLEXER(16 CHANNELS, MAX 200V/	00 200-1036	DORNIER	1	/72		13.1465
	500MA (IR 10VA, DATAWAY SET+INCR ADDRESS) (WITH FRONT PANEL CONNECTOR)	DD 200=1236		1	/72		
	(SAME WITH LOW THERMO VOLTAGE CONTACTS) (WITH FRONT PANEL CONNECTOR)	DO 200-1035 DO 200-1235		2	771		
	ANALOG MULTIPLEXER (15 CHANNELS, REED RELAYS, MAN AND DATAWAY SEL, EXPANDABLE)	AM	JOERGER	2	/72	( 6)	13.1466
	16-CHANNEL A/D CONVERTER (DIFFERENTIAL INPUTS, 11 BITS + SIGN)	AM-1	JOFRGER	5	/74	(11)	13,1467
	15 CHANNEL RELAY MULTIPLEX	3530	KINETIC SYSTEMS	2	/73		13,1468
	MASTER MULTIPLEXER (16 CH, 4 POLE REED) SLAVE MULTIPLEXER (16 CH, 4 POLE REED)	601	NUCL. FNTERPRISES		/70 /70		13,1469
	16 CHANNEL RELAY MULTIPLEXER	J MX 10	SCHLUMBERGER	1	/73		13.1470
	STANDARD LEVEL) (SAME FOR LOW LEVEL) MULTIPLEXER MANUAL CONTROL	J MX 20 J AX 10		1	/73 /73		
	MULTIPLEXER 16X4 CONTACTS		SIEMENS	i	174		13,1471
	16-CHANNEL FAST MULTIPLEXER (FET	1704	BORER	1	172	(4)	13.1472
	SWITCHES FOR ADC 1243 AND 1244)  FET MULTIPLEXER (16 CHANNELS,	DD 200=1031	DORNIER	1	172		13,1473
	MAX +OR=10V, DATAWAY SET + INCR ADDRESS) (SAME WITH FRONT PANEL CONNECTOR)	DO 200-1231	DUNIEN	i	/72		13,14/3
	FET MULTIPLEXER (16 DIFF I/P,	DD 200-1034	DORNIER	1	/72		13,1474
	MAX +OR=10y, DATAWAY SET+INCR ADDRESS) (WITH FRONT PANEL CONNECTOR)	DO 200-1234		1	172		
	16 CHANNEL A/D CONVERTER (FET MUX DIFF INPUTS, 12BIT AUTO CYCLING, DUAL SLOPE)	34	JORWAY	2	/74		13,1475
	MULTIPLEXER-SOLID STATE (16 SINGLE-ENDED OR 8 DIFF CHAN, RANDOM OR SEQUENT ACCESS)	9026	NUCL' ENTERPRISES	1	/71		13,1476
	SOLID STATE MULTIPLEXER (16 CH, RANDOM, & SEGUENT ACCESS, MULTI-MUX SCAN MODE)	MX 016	STND FNGINEERING	1	174	(12)	13,1477
	32 CHANNEL ANALOG MULTIPLEXER (SERVE AS CHANNEL EXPANDER FOR 5301 DATA SYSTEM)	5101	RI RA SYSTEMS	1	. 174		13,1478
	RELAY MULTIPLEXFR (32 CHANNELS)	750	POLON	2	03/75		13,1479
	MULTIPLEXER (32 CHANNEL, 2 CONTACTS)	C 76451-A4-A1	SIFHENS	2.	/73		13,1480
	MULTIPLEXER (32 CHANNEL, 4 CONTACTS)	C 76451-A4-A2	SIEMENS	2	/73		13,1481
	MULTIPLEXER 32X2 CONTACTS	C 72468-A0628-A001	SIFMENS	1	174		13,1482
	FET MULTIPLEXER MAX +OR-10V, DATAWAY SET+INCH ADDRESS) (WITH FRONT PANEL CONNECTOR)	DO 200=1032	DORNIER	1	/72		13,1483
	FET MULTIPLEXER (32 DIFF I/P,	DO 200-1037	DORNIER	2	/72		13,1484
	MAX +OR=10V, DATAWAY SET+INCR ADDRESS) (SAME WITH FRONT PANEL CONNECTORS)	DU 200-1237		2	172		
	FET MULTIPLEXER (64 CHANNELS	DO 200-1061	DORNIER	2	/73		13,1485
	MAX +OR=10V, DATAWAY SET+INCR ADDRESS) (WITH FRONT PANEL CONNECTOR)	DO 200-1261		2	/73		
	165 Analogue Handling and	d Processing Module	s II (LIN. Gates, Amp	ol., Discri	minators	etc.)	
	ACTIVE FILTER AMPLIFIER(10 = 1000 GAIN, .25=4USEC GAUSS' PULSE SHAPING,0=10V OUT	1101	POLON	3	174		13.1486
	BASELINE RESTORER(.1% COUNT RATE STABIL UP TO SOKHZ,0-10 I/O SIGNALS,1V/V GAIN)	1102	POLON	2	174		13,1487
	DELAY AMPLIFIER(,25 - 4,75USEC DELAY, 0 TO 10V INJOUT STGNALS, 1V/V GAIN)	1103	POLON	2	03/75		13,1488
	SUM-INVERT AMPLTFIER(.2% NUN-LINEARITY, 1V/V GAIN, 0 TO 10V IN/DUT SIGNALS)	1104	POLON	1	174		13,1489
	LINEAR GATE (.2% NON-LINEARITY, +/- 1V/V GAIN, 0 TO 10V IN/OUT SIGNALS)	1105	POLON	1	/73		13.1490
	PULSE STRETCHER(.059USEC I/P WIDTH, 1USEC O/P WIDTH OF PULSES, .9 V/V GAIN)	1106	POLON	1	174		13.1491
	SINGLE CHANNEL ANALYSER ('2=10V LO/HI LEVEL, '2=2V WINDOW, '5=2.5USEC DELAY)	1201	POLON	3	/74		13.1492
	LINEAR RATEMETER (10 TO 100K CPS RANGE, 18 TO 308 TIME CONSTANTS)	1301	POLON	3	174		13,1493
	LOGIC SHAPER AND DELAY (.2 TO 110USEC DELAY, .2 TO 11USEC U/P PULSE WIDTH)	1401	POLON	2	174		13,1494
	UNIVERSAL COINCIDENCE (.1 TO 20SEC RESOLVING TIME)	1402	POLON	5	174		13,1495

FAN DIJT (1 NIM IN, 2 NIM & 1 COMPL TTL DUT)	1504	POL.ON	1	/73		13,1496
CAMAC CONTROLLED PULSE SHAPER (4 PM I/P, 4 NIM I/P & 6 NTM U/P)	CPS 2065	SEN	1		(12)	13.1497
DUAL PULSE DELAY UNIT	PD 002	STND ENGINEERING	5	173		13.1498
SAMPLE-AND-HOLD AMPLIFIER (DUAL DIFF	DO 200=1040	DORNIER	2	172		13,1499
AMPL,+/=10V RANGE,20MA DUT,5USEC SETTL) (SINGLE AMPL VERSIUN, ROTH TYPES HAVE HOLD AND TRACK MUDES)	DO 200=1041		2	/72		
PROGRAMABLE AMPLIFIER/ATTENUATOR (GAIN	DO 200-1052	DORNIER	2	/73		13,1500
ODB TO GODB IN 10 STEPS, ATTENUATION .5) (SAME BUT DUAL CHANNEL VERSION)	DO 200-1053		1	/73		
PROGRAMMABLE AMPLIFIER	DO 200-1054	DORNIER	1	05/75		13,1501
(SAME BUT DUAL CHANNEL VERSION)	DO 200=1055		1	05/75		
DIFFERENTIAL AMPLIFIER (GAIN CONTROLLED FROM DATAWAY)	CS 0014	NUCL' ENTERPRISES	2	/72		13.1502
N PROGRAMMABLE PRESISTON ATTENUATOR (1/1 TO 1/2048, 200 MAX I/P RANGE)	PPA 2071	SEN	1		(13)	13,1503
DIGITAL WINDOW DISCRIMINATOR (WITH 128X16BIT BUFFER, PARALLEL + SERIAL I/P)	DWD 2046	SEN	1	/72	(8)	13,1504

# 17 Other Digital and/or Analogue Modules — Mixed Analogue and Digital, Not Dataway Connected etc.

DETECTOR BIAS SUPPLY (0 TO +/=2000V, 1MOHM AND 10MOHM OUTPUT RESISTANCE)	1901	POLON	<b>4</b>	174	13,1505
NUMERICAL CONTROL SYSTEM, COMPRISING DATA MRITER AND DISPLAY SERIAL CONTROLLER DATA RECEIVER FOR MECHANICAL OPERATIONS	C 500 C 504 C 502 C 501	RDT	N A 0 0	( 7)	13,1506
(5 DECADE DATA, 3 DECADE INSTRUCTION REG)  CAMAC PROM PROGRAMMER		SENSION .	2	(13)	13,1507
CURRENT SOURCE	C 76451=A5=A1	SIFMENS	2	/73	13,1508

# 2 SYSTEM CONTROL EQUIPMENT — COMPUTER COUPLERS, CONTROLLERS AND RELATED EQUIPMENT

21 Interfaces/Drivers and Controllers — Parallel Mode for 4600 Branch and Other Multi-Crate Bus, Single-Crate Systems, Autonomous Systems

# 211 Interfaces/Drivers for Multicrate Systems I (4600 Branch Compatible)

	EXECUTIVE SUITE ASSEMBLY OF MODULAR CONTROLLERS IN CAMAC CRATE, COVERS SYSTEM COMPLEXITY FROM SINGLE SOURCE-SYNGLE CRATE TO MULTI		GEC=ELLIÖTT			13,2001
	SOURCE-MULTI CRATE SYSTEMS, COMPRISING EXECUTIVE CONTROLLER (TRANSFORMS STANDARD CRATE INTO SYSTEM CRATE)	MX=CTR=2		2	/72	
	BRANCH COUPLER (ONE PER BRANCH, MAX 7)	BR=CPR=2		2	/72	
	AND SYSTEM INTERFACE SOURCE UNITS, ALSO OPTIONALLY AUTONOMOUS CONTROLLER SOURCE UNITS (ALL INSERTED INTO SYSTEM CRATE)	nivers and	GEC-ELLIOTT			13,2002
	PDP=11 SYSTEM INTERFACE, COMPRISING		GEC-ELLIOTT			13,2003
	PROGRAM TRANSFER INTERFACE	PTI=11 C/D		3	172	
C	UNIBUS TERMINATION UNIT	TRM=11=1		1	174	
	INTER UNIT BUS (LINKS UNIBUS TO	TUB-X			174	
-	ALL SI SOURCE UNITS FORMING INTERFACE)	100-1				
	INTERRUPT VECTOR GENERATUR (ADDS AUTUNO-	IVG=11		1	172	
	MOUS ENTRY OF GL =DERIVED INTERRUPTS)					
N	AUTONOMOUS MEMORY ACCESS CONTROLLER (2 USEC/WORD TRANSFER TO PDP=11 STORE)	AMC=11		2	08/75	
	(E OCCUPANTO TRANSPORT TO TO THE STORE)				STATE OF THE STATE	
	NOVA/SUPERNOVA SYSTEM INTERFACE, COMPR		GEC-FLLIOTT			13,2004
	PROGRAM TRANSFER INTERFACE	PTI=N C/D		3	172	
	I/O BUS TERMINATION UNIT	TRM-N		1	172	
C	INTER UNIT BUS	TUB-X			174	
N	INTERRUPT VECTOR GENERATOR (256 BIT TRAP	IVG-2402		1	174	
	STORE, BRANCH OR GL PRIDRITY MODES)					
	INTERDATA 70-SERIES SYSTEM INTERFACE		GEC-FLLIOTT			13,2005
	COMPRISING					
	PROGRAM TRANSFER INTERFACE	PTI=70 C/D		3	/73	
	I/O BUS TERMINATION UNIT	TRM=70		1		
٢	INTER UNIT BUS	TUB=X			174	
	INTERRUPT VECTOR GENERATOR (256 BIT TRAP	IVG=2402		1	174	
	STORE . BRANCH OR GL PRIORITY MODES)	. 10-6-102				

N	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	HONEYWELL 316/516 SYSTEM INTERFACE, COMPR PROGRAM TRANSFER INTERFACE I/O BUS TERMINATION UNIT SYSTEM INTERFACE BUS	PTI=H16 C/D TRM=H16 SI=BUS=XH16	GEC-ELLINTT	3	/73 /73		13,2006
NCC	GEC 4080 SYSTEM INTERFACE, COMPRISING DIRECT TRANSFERS INTERFACE INTERRUPT VECTOR GENERATOR BLOCK TRANSFER CHANNEL CONTROLLER INTER UNIT BUS AUTONOMOUS MEMORY ACCESS CONTROLLER (2,5 US/WORD TRANSFER TO GEC=4080 STORE)	PTI=2050 C/D IVG=2402 PTI=2050 D IUB=X AMC=4080	GEC-ELLINTT	3 1 3	/73 /74 /73 /74 08/75		13.2007
c	GEC 2050 SYSTEM INTERFACE (SAME ITEMS AS FOR GEC 4080 INTERFACE)		GEC-FLLIOTT		174		13,2008
	SYSTEM CRATE TEST UNIT (TWO-COMMAND TEST UNIT FOR CHECKING SYSTEM CRATE SYSTEMS)	SC=TST=1	GEC-ELLIOTT	3	172		13,2009
	BRANCH HIGHWAY DRIVER	3991	KINETIC SYSTEMS	2	/75		13,2010
c	MICROPROGRAMMED BRANCH DRIVER FOR PDP=11	1201	BI RA SYSTEMS	NA	/72	(5)	13,2011
	(FROM 256 UP TO 4K WORDS MEMORY) UNIBUS CABLE ASSEMBLY	8101	,		/72	Part Alla	ATA DEL
	PDP=11 CAMAC CUNTRULLER(SEQUENTIAL READ/ WRITE,24 GRADED=L INTERRUPT DIRECTLY)	CA 11-A	DEC	NA	/71	( 2)	13,2012
	PDP=15 CAMAC INTERFACE(18/24BIT, PROGR, SEQUENT ADDR AND BLOCK TRANSFER MODES)	CA 15 A	DEC	NA	/71	(1)	13,2013
	PDP=11 INTERFACE/BRANCH DRIVER (24 VECTOR ADDRESSES, PRUGRAMMED AND MULTIPLE DMA=TRANSFER, ADDRESS SCAN AND -LIST MODE, REPEAT=, LAM- AND STOP MODE)	CA 11-C	DEC	NA	/72	(4)	13,2014
	PDP=11 BRANCH DRIVER (EUR 4600 COMPATI- BLE, PROGRAMMED AND SEQUENT ADDR MODES)	BD=011	EGRG/ORTEC	NA	/71		13,2015
	PDP=11 BRANCH DRIVER	KS 0011	KINETIC SYSTEMS	NA	/71	(4)	13,2016
	INTERFACE AND DRIVER FOR PDP 11 OR PDP 8		NUCL' ENTERPRISES				13.2017
	MULTI-CRATE SYSTEM, COMPRISING BRANCH INTERFACE 16-BIT CONTROLLER (WITH EITHER OF THE FOLLOWING INTERFACE (AROS )	9031 9030		2 3	/72	(7)	
	PDP 11 INTERFACE CARD INTERFACE CARD FOR DEC PDP 8 SERIES	9032			/72	(7)	
	INTERFACE CAMAC-PDP 11 (PROGRAMMED, BLOCK TRANSFER AND SEQUENTIAL ADDR MODES)	ICP 11/ICP 11 A	SCHLUMBERGER	NA	/71	( 4)	13.2018
	NOVA BRANCH DRIVER	1251-1	BI RA SYSTEMS	NA	/73	(5)	13.2019
	NOVA BRANCH DRIVER WITH DATA CHANNEL	1251=2	BI RA SYSTEMS	NA	174	( 5)	13,2020
	NOVA BRANCH DPIVER	NBD 100	STND ENGINEERING	2	174		13,2021
	INTERFACE/SYSTEM CONTROLLER TO HP2100, 2114, 2115, 2116	2201	RORER	NA	/71	(4)	13,2022
c	PRIME COMPUTER BRANCH DRIVER (WITH DTM. PRIME COMPUTER BRANCH CABLE TYPE 8103)	1260	BI RA SYSTEMS	NA	/74		13,2023
	INTERFACE FOR VARIAN 6201/L/F COMPUTER (PROGR, SEGUENT AND BLOCK TRANSFERS)	2204	RORER	NA	/72		13,2024
	SYSTEM CONTROLLER FOR SIEMENS 404/3 (TRANSFER OF 16 OR 24 BIT DATAHORDS	DO 200-2921	DORNIER	6	/73		13,2025
	PARALLEL BRANCH COMMAND CHAINING) (SAME BUT WITHOUT COMMAND CHAINING)	00 200=2922		6	/73		
	SYSTEM CONTROLLER FOR SIEMENS 404/3 (TRANSFER OF 16 OR 24 BIT DATAWORDS PARALLEL BRANCH BUT NO COMMAND CHAINING)	DU 200-2923	DORNIER	6	/73		13.2026
	MICRODATA 800/CTP 2000 BRANCH DRIVER	91	JORWAY	NA	/73	(7)	13,2027
	BRANCH DRIVER (248IT, PROGR, SEQUENT AND BLOCK TRANSFER MODES, MAX 7 (RATES)	5400	LABEN	4		(8)	13,2028
	INTERFACE DRIVER FUR VARIAN 73/6201/620L MULTI-CRATE SYSTEM, COMPRISING		NUCL' ENTERPRISES			(8)	13,2029
	BRANCH INTERFACE 16-BIT CONTROLLER . AND	9031 9030		2	/72 /72	(7)	
	INTERFACE CARD FOR VARIAN 73/6201/620L SERIES CUMPUTERS	CS 0044				(8)	
	SYSTEM CONTROLLER FOR SIEMENS 320/330 (AUTO-GL, 24 VECTOR ADDR, PROGRAMMED &	C 72451 A1602	SIEMFNS	8	174		13,2030

# 212 Interfaces/Drivers for Multicrate Systems II (for other Parallel Mode Control/Data Highway)

DEDICATED CRATE CONTROLLER FOR NOVA	NC023 NT022	FGRG/URTEC	2	/73 /73	13,2031
BIDIRECTIONAL DATA BREAK MODULE FOR PDP8	1000	HYTEC	2	174	13,2032
PROGRAMMED DATAWAY CUNTROLLER (PART OF	7025-2	NUCL. ENTERPRISES	2	/70	13,2033
7000-SER SYSTEM WITH EXT CONTR HIGHWAY) COMMAND GENERATOR TRANSFER REGISTER	7062-1 7063-1		2	/71 /70	
PROGRAM CONTROL UNIT	0362=2 7044=1		NA 1	/70 /70	
PLUGBOARD STORE	7077-1		3	/71	
CONTROLLER/INTERFACE FOR 11600 COMPUTER (MAX 8 CRATES, PROG/ADDR.SCAN/STOP MODE)	JCT 16-10	NUMELEC	2		13.2034
DMA MODULE	JDM 16.10		2		
CRATE CONTROLLER FOR NOVA COMPUTER CRATE CONTROLLER BUS TERMINATOR FOR	CC 2023A/B BT 2022	SEN	2	/70 /71	13,2035
CC 2023A /B /ONE DED SYSTEM)					

# aces/Drivers for Single-Crate Systems (4100 Dataway Compatible)

	213 Interfaces/Drivers for S	Single-Crate Syste	ms (4100 Dataway Com	patible)			
	SINGLE CRATE SYSTEM CONTROLLERS (SEE EXECUTIVE SUITE, CLASS .211)		GEC-FLLIOTT				13,2036
	PDP=11=SERIFS CRATE CONTROLLER	1304	BI RA SYSTEMS	2	/73		13.2037
	CRATE CONTROLLER/PDP11 UNIBUS INTERFACE	1533A	BORER	2	/72	(4)	13,2038
	NPR CONTROLLER FOR DMA TO PDP11 E.G. VIA 1533A CRATE CONTROLLER/INTERFACE	1542	BORER	NA	/73	(8)	13,2039
	SINGLE CRATE CONTROLLER/PDP=11 INTERFACE. (MULTIPLE BUS ADDRESS VERSION)	CA-11-E	D E C	2	174	( 9)	13.2040
	SINGLE CRATE CONTROLLER/PDP-11 INTERFACE (PROGRAMMED TRANSFERS, WITH NAF REG &	CA=11=FP	DEC	2	06/75		13.2041
	CONNECTOR TO DMA OPTION CA-11-FN) PDP-11 DMA INTERFACE FOR CA-11-FP (8 DMA CHANNELS, MI OR LIST MUDE, 16BIT MC, CA, OFFSET FOR FACH CHANNEL, LIMIT REGISTER)	CA=11=FN	gare	2	06/75		
1	DEDICATED CRATE CONTROLLER FOR PDP=11 (MULTIPLE TRANSFER OR AUTO ADDRESS SCAN)	DC011	FGRG/ORTEC	2		(7)	13.2042
	SINGLE CRATE CONTROLLER FOR PDP-8/E ADDR,-SCAN MODE, DMA I/O, MAX 22 LAMS)	LEM=52/32.1	EISENMANN	3		(13)	13.2043
	UNIBUS CRATE CONTROLLER POP=11	3911	KINETIC SYSTEMS	2	/72		13.2044
	INTERFACE AND DRIVER FOR PDP 11 DR PDP 8		NUCL' ENTERPRISES				13,2045
	SINGLE CRATE SYSTEM, COMPRISING 16-BIT CONTROLLER (WITH EITHER OF THE	9030		3	/72	(7)	
	FOLLOWING INTERFACE CARDS ) PDP 11 INTERFACE CARD INTERFACE CARD FOR DEC POP 8 SERIES	9032 9034			/72 /73	( 7)	
	AUTONOMOUS CONTROLLER FOR PDP 11	9033	NUCL. ENTERPRISES	2	/73	(8)	13.2046
	CAMAC CRATE=PDP 11 INTERFACE UNIBUS TERMINATOR UNIBUS EXTENDER	J CC 11 J UT 11 C BEX 11	SCHLUMBERGER	2	/74 /74	(7)	13,2047
	CRATE-SYSTEM CONTROLLER FOR PDP=11 (24 BIT READ & WRITE CAPABILITIES)	C=CSC=11	WENZFL ELEKTRONIK	2	/72		13,2048
	NOVA-SERIES CRATE CONTROLLER	1303	BI RA SYSTEMS	2	. /73		13.2049
	SINGLE CRATE CONTROLLER TO HP COMPUTERS WITH EXT SYNCHRONISATION FACILITIES	1531A	BORER	2	02/75		13,2050
	INTERFACE FOR HP 2114-2115 COMPUTERS,		NUCL. ENTERPRISES				13,2051
	COMPRISING 16-BIT CONTROLLER	9030		3	/72	(7)	
	INTERFACE CARD FOR HP 2114-2115	CS 0058			174		
	VARIAN-CAMAC INTERFACE CRATE CONTROLLER (16BIT SEQUENT+BLOCK TRANSF, 1 CC/CRATE)	c 300	INFORMATEK	2	/72		13,2052
	INTERFACE-DRIVER FOR VARIAN 73/6201/620L		NUCL. ENTERPRISES			(8)	13.2053
	SINGLE CRATE SYSTEM, COMPRISING 16-BIT CONTROLLER	9030		3	/72	(7)	
	AND INTERFACE CARD FOR VARIAN 73/6201/620L SERIES COMPUTERS	CS 0044				(8)	
	INTERFACE FOR HONEYWELL 316-516 COMPUTERS, COMPRISING		NUCL. ENTERPRISES				13.2054
	16-BIT CONTROLLER	9030		3	/72	(7)	
	INTERFACE CARD FOR HONEYWELL 316-516	CS 0057			174		

NC DESIGNATION & SHORT	DATA TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
INTERFACE FOR K202 COMPUTER (24BI NOMOUS BLOCK TRANSFERS TO/FROM ME L=NUMBER INTERRUPT FNCODER)		PNLNN	3	/73		13,2055
N SINGLE CRATE CONTROLLER FOR MICRA	L N/G/S JC MIC 10	R 2 F	2	02/75	(13)	13,2056
CRATE INTERFACE FOR MULTI 20 OR M	ULTI 8 J CM 8/20	SCHLUMBERGER	3	/74		13.2057
CRATE CONTROLLER 320	C 72451=A1446=	A6 SIEMENS	3	172		13,2058
CRATE CONTROLLER 404	C 76451=A1446=	A7 SIEMENS	2	/73		-13.2059
214 Controllers	for Autonomously Operate	d Systems (and Related I	Inite)			
	The second of th	a dystoms (and Helated C	into)			
DATA PROCESSOR (AUTONOMOUS PROGRA SINGLE DATAWAY CONTROLLER 16 REGI		DURNIER	3	/73		13,2060
DATA PROCESSOR (AUTONOMOUS PROGRA SINGLE DATAWAY CONTROLLER 16 REGI REGISTERS AND MEMORY EXPANDABLE)	MARLE DD 200-2951		3	/73		
CADET (SINGEL-CRATE CONTROLLER FO	R READ- CT 2058	SEN	4		(12)	13.2061
ONLY SYSTEM, INCL MODULE TEST & D PRINT BUFFER (ALLOWS A PARALLEL P TO BE USED WITH THE CT 2058)			0		(12)	
N PROGRAMMABLE CRATE CONTROLLER	\$ 800	SENSION	22		(13)	13.2062
N PROGRAMMABLE CRATE CONTROLLER	3 804	SENSION	55		(13)	13.2063
CAMAC MICROPROCESSOR CRATE CONTRO	LLER MIK XA	STND ENGINEERING	0	174		13.2064
217 Other Parall	el Mode Interfaces/Drivers	/Controllers				
SYSTEM CRATE CONTROLLER MODCOMP I, MODCOMP II & MODCOMP II	3960 3970	KINETIC SYSTEMS	2	/73 /73		13,2065
SYSTEM DRIVER(USE WITH 3960) PDP=11 SYSTEM DRIVER (USE WITH 39 CONTROL DATA 6000 SERIES SYSTEM D (USE WITH 3960)			2 3	/74 /75		
MANUAL SYSTEM DRIVER (USE WITH 396	0) 3980	KINETIC SYSTEMS	2	/73		13,2066
22 Interfaces	Controllers/Drivers for	Serial Highway				
N SERIAL CRATE CONTROLLER TYPE L=1 (CONFORMING TO ESONE/8H/01 AND ER	RATA)	GEC-ELLIOTT	2	06/75		13,2067
SERIAL EXTENSION UNIT. 8 BIT BYTE LINK, BRANCH COMPATIBLE, CONSISTI		JOFRGER		/73	( 8)	13.2068
SERIAL CRATE CONTROLLER *L=1* (CO) TO ESONE/SH/01 % TID=26488 + ERRA	NFORMS 74		2	/74	(11)	
MANUAL SERIAL DRIVER (BIT/BYTE MO MULTIPLE MESSAGES, ERROR GENERATION	ON)	JORWAY	4	174		13.2069
N SERIAL HIGHWAY LOOP CONTROL CIRCU	3931	KINETIC SYSTEMS	2		(13)	13.2070
TRANSF. ISOLATED SERIAL D-PORT AD	APTER 3932	KINETIC SYSTEMS	1	/75	(13)	13,2071
C TYPE L=1 CRATE CONTROLLER FOR THE "STANDARD" SERIAL HIGHWAY	3952	KINETIC SYSTEMS	2	174	(13)	13,2072
DRIVER FOR SERIAL HIGHWAY	3992	KINETIC SYSTEMS	3	174	(11)	13,2073
DRIVER FOR SERIAL HIGHWAY	3994	KINETIC SYSTEMS	4	/75	(13)	13,2074
(WITH 256, WORD FIFO BUFFER)  N SERIAL CRATE CONTROLLER SPECIFICA	TION L1 CR 6001	ROVSING	2			42.004
23 Units Rela Highway –	ted to 4600 Branch or ( – Crate Controllers, Ter	Other Parallel Mode C	ontrol/[	11/75 Data	(13)	13,2075
DISPLAY DRIVER (CONTROLS 72A DISPLAND CRATE CTR AND BRANCH DRIVER)	us Extenders	JORWAY	5	/71		13.2076
231 Crate Contro	llers (Type A-1, Other CC	Types)				
TYPE A=1 CRATE CONTROLLER	1301	AI RA SYSTEMS	2	/73		13.2077
CRATE CONTROLLER /ESONE TYPE A1/	1502	BORER	2	/72		13,2078
CRATE CONTROLLER TYPE CCA=1 ACCORD EUR4600 SPECS WITH CERN OPTIONS	DING TO DO 200=2905	DORNIER	2	171		13.2079
CAMAC CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECIFICATION	- CC101	EGRG/ORTEC	2	/72		13,2080
ESONE TYPE A.1 CRATE CONTROLLER(CO	INFORMS CC 2405	GEC-ELLIDIT	2	/73		13,2081
TO EUR4600 SPECS, INCL CERN HOLD I	OPTION)					.0,2081

CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECS)	CCA=1	JOERGER	2	177	(5)	13,20A2
BRANCH CRATE CONTROLLER/TYPE 4=1 (CONFORMS TO EUR 4600 SPECS, 1972)	70A	JORWAY	2 4	/73	(7)	13,2083
TYPE A=1 CRATE CONTROLLER	3900	KINETIC SYSTEMS	2	/73		13.2084
CRATE A=1 CONTROLLER	9016	NUCL. ENTERPRISES	2		(4)	13,2085
(CONFORMS TO FUR 4600 SPECS)			2	/71		13,2086
CRATE CONTROLLER TYPE A (CONFORMS TO EUR4600 SPECS)	C 106	RDT		2017-019		Actes 4
CRATE CONTROLLER TYPE A=1 (CONFORMS TO EUR4600 SPECS)	J CRC 51	SCHLUMBERGER	2	/72	(1)	13,2087
A=1 CRATE CONTROLLER (CONFORMS TO EUR4600 SPECS, INCL CERN SPEC HOLD LINE)	ACC 2034	SEN	2	/72		13,2088
CRATE CONTROLLER A1 (EUR 4600 SPECS AND CERN NOTE 38=00)	C 72451=A1446=A2	SIEMENS	2	/70	( 1)	13,2089
TYPE A-1 (ESONE) CRATE CONTROLLER	CC=A1	STND ENGINEERING	5	/72	(6)	13,2090
TYPE A1 CONTROLLER WITH TERMINATOR (MEETS 4600 SPECS OF JAN 1972)	CCT-A1	STND ENGINEERING	2	/73		13,2091
232 Lam Graders						
LAM GRADER (24 BIT MASK REGISTER, PLUG-IN PATCH BOARD, CERN 064)	LG 2401	GEC-ELLIOTT	1	/72		13,2092
LAM GRADER (INTERNALLY PATCHABLE, SWITCH SELECTABLE MULTI-CRATE BG-RESPONSE)	LG	JOERGER	1	/73	(8)	13.2093
LAM GRADER-SORTER	<b>7</b> 5	JORWAY	2	/73	(7)	13.2094
LAM GRADER (DESIGNED TO EUR 4600 SPECS)	064	NUCL. ENTERPRISES	1	/72	(4)	13,2095
PRIORITY GRADER	9037	NUCL' ENTERPRISES	1		(10)	13.2096
LAM GRADER (CERN SPECS 064)	C 107	RDT	1	/71		13.2097
LAM GRADER (CERN SPECS 064)	LG 2001	SEN	1	/72	(6)	13,2098
LAM GRADER (24BIT MASK REG, WITH CABLE, PATCHABLE C-ADDR-REG FOR MULTI-CRATE BG)	C 76451=A18=A1	SIEMENS	0	/74		13.2099
233 Terminations (Simple,	with Indicators)					
BRANCH HIGHWAY TERMINATOR	6601 (	BI RA SYSTEMS	1	/73		13,2100
BRANCH TERMINATION UNIT (WITH BUILT=IN CABLE)	1592	RORER	1	/73		13.2101
BRANCH TERMINATION UNIT (NON INDICATING)	BT 6503	GEC-FLLIOTT	2	/72		13.2102
BRANCH TERMINATION UNIT	BT 6601	GEC-ELLIOTT	2	/71		13,2103
BRANCH TERMINATOR	BT	JOERGER	2	/72		13,2104
BRANCH TERMINATION WITH INTEGRAL CABLE	500	JORWAY	2	/72		13.2105
BRANCH TERMINATOR IN A CONNECTOR	BT=01	KINETIC SYSTEMS	NA	/73		13,2106
BRANCH TERMINATOR	J BT 20	SCHLUMBERGER	2	/71		13.2107
BRANCH TERMINATOR (NON-INDICATING, 40 CM FLYING CABLE WITH BRANCH CONNECTOR)	RT 231	SEMRA-BENNEY	resure	174		13,2108
(DITTO, XXX# CARLE LENGTH IN CM)	BT 231XXX	SEN	1	//4		13,2109
CRATE CONTROLLER BUS TERMINATOR FOR A=1 , CRATE CONTROLLER	BT 2042	SEN	(200007F)	/74	(11)	13,2110
BRANCH HIGHWAY TERMINATOR	BHT 2055	SEN				Aura)
BRANCH HIGHWAY TERMINATOR	BHT=001	STND ENGINEERING	1	/73		13,2111
BRANCH HIGHWAY TERMINATOR, WITH DISPLAY	BHT=002/D	STND ENGINEERING	2	/73		13,2112
BRANCH TERMINATOR (FULL BRANCH MONITOR WITH INTERNAL STORAGE AND LED DISPLAY)	RT 6502	GEC-ELLINTT	2	/72		13,2113
VISUAL BRANCH TERMINATOR (STORES AND DISPLAYS ON LEDS BRANCH SIGNALS)	VBT	JOERGER	2	/72	(6)	13.2114
BRANCH TERMINATION WITH BRANCH DISPLAY	51	JORWAY	2	/72	١.	13,2115
BRANCH TERMINATION UNIT (WITH INDICATOR AND POWER SUPPLY)	C 72451-A10-A1	SIFMENS	NA	/73	( 3)	13,2116

# Branch Extenders, Bus Extenders

				세계 게임에 시간된 사람들이 없었다.	
EXTENDED BRANCH SERIAL DRIVER	3990	KINETIC SYSTEMS	5	174	13,2117
DIFFERENTIAL BRANCH EXTENDER (FOR EXTENDING BRANCHES UP TO 3 KM)	DBE 6501	GEC-ELLINTT	2	/71	13,2118
DIFFERENTIAL MUDE BRANCH HIGHWAY EXTENDER (BT-DIRECTIONAL)	55	JORWAY	NA -	/73 (7)	13,2119
BRANCH HIGHWAY TRANSCEIVER FOR LONG DISTANCE TRANSMISSION	J BHT 10	SCHLUMBERGER	2	( 4)	13,2120
SERIAL DRIVER (TERMINATES BRANCH HIGHWAY AND RETRANSMITS COMMAND SERIALLY)	SD	JOERGER	2		13,2121
SERIAL RECEIVER (RECEIVES SERIAL DATA, DRIVES TYPE A=1 SYSTEM, OPTICAL ISOL)	SR		2	1 3 2 m 1 4 3 2 2 3 1 1	
UNIBUS EXTENDER, TRANSMITTER  RECEIVER (FOR DISTANCES UP TO 200 METRE OR MORE)	1594 1595	RORER	5	/72 /72	13,2122

#### 3 TEST EQUIPMENT

#### 31 System Related test Gear

N SYSTEM CHECK OUT UNIT. STORES DATA & COMMAND IN READABLE REGS. PROGRAMMABLE L	DTM 4	GEC-ELLIOTT	1	174	13.3001
SYSTEM TEST UNIT (FOR EXECUTIVE SUIT SYSTEM CONFIGURATION, SEE MX=CTR=2)	SC-TST-1	GEC-FLLINTT	3	172	13,3002

#### 311 Computer Simulators

PDP-11 SIMULATUR	6101	BI RA SYSTEMS	NA	172	( 5)	13.3003
TEST MODULE (USED IN SYSTEM TEST OF READ/WRITE CAPARILITY)	TM024	FGRG/DRTEC	2	/71	ROAGE	13.3004
TEST CONTROLLER WITH PROGRAM PLUGROARD	SPS 2048	NUCL. ENTERPRISES	2	01/75	(12)	13,3005
CAMAC SYSTEM SIMIL ATOR/TESTER	C99/T	STND ENGINEERING		177		13 3004

#### 32 Branch Related Testers/Controllers and Displays

#### 321 Branch Testers/Controllers (Manual, Programmed)

MANUAL BRANCH TESTER (TYPE A SYSTEM TEST SET WITH MX-CTR-2 & BR-CPR-2)	SC-TST-1	GEC-ELLIOTT	7			13.3007
BRANCH HIGHWAY TEST POINT HODULE(24 DIR- ECT,22 INDIRECT ACCESS POINTS FOR TEST)	CD 18104	FMIHUS	NA	/71	( 3)	13,3008
BRANCH HIGHWAY REMOVE INHIBIT MODULE (REMOVES INHIBIT FROM BCR/BA/BF/BN/BTA)	CD 18105	EMIHUS	NA	/71	( 3)	13.3009
MANUAL BRANCH DRIVER (FOR TESTING TYPE A SYSTEMS)	MBD	JOERGER	14.8 5	177	( 6)	13.3010
MANUAL BRANCH CONTROL SET (COMPRISING TYPES C COB 10 AND T CMB 10)	C CMB 10	SCHLUMBERGER	NA	/71	( 1)	13,3011

#### **Dataway Related Testers and Displays** 33

#### 331 Dataway Controllers/Testers (Manual, Programmed)

MANUAL CRATE CONTPOLLER	GFK=LEM	FISENMANN	8	/71		13,3012
MANUAL CRATE CONTROLLER	MCC	JOERGER	5	/72		13,3013
MANUAL DATAWAY CONTROLLER	7024=1	NUCL. ENTERPRISES	8	/70		13,3014
MANUAL DATAWAY CONTROLLER/DISPLAY SYSTEM INTERFACE TO DATAWAY CONTROL AND DISPLAY CRATE	D AI 10 J DA 10 C AI 10	SCHLUMBERGER	1 NA	/71		13.3015
MANUAL CRATE CONTROLLER	J CMC 10	SCHLUMBERGER	8	/71	(1)	13,3016
TEST MODULE FOR CRATE CONTROLLER AND	DTM 2040	SEN.	f	/72		13,3017
MANUAL 24 BIT CRATE CONTROLLER	MCC=240	STND ENGINEERING	2	172	( 5)	13.3018
DYNAMIC TEST CONTROLLER (GENERATES ALL POSSIBLE CAMAC COMMANDS IN SINGLE CRATE)	TC 2403	GEC-ELLINTT	3	/71		13,3019
DYNAMIC TEST CONTROLLER (2 SIMULT TRANSF SINGLE, STEP-BY-STEP AND CONTINUOUS MODE)	C 108	PDT	8	/71	(4)	13.3020
DATAWAY SERVICE MODULE	J DS 10	SCHLIMBERGER	1	174	(12)	13,3021
CONTROLEUR SORTIE DATAWAY	41403	TRANSRACK	1	/70		13,3022

332 Dataway Displays						
CAMAC TEST MUDULE/DATAWAY DISPLAY	6102	BI RA SYSTEMS	2	/73		13,3023
CAMAC DATAWAY DISPLAY (DATAWAY SIGNAL PATTERN STORED/DISPLAYED, 2 TEST MODES)	1801	BORER	1 (1)	/71	( 1)	13,3024
CAMAC DATAWAY TEST AND DISPLAY MODULE	LEM-52/16.2	FISENMANN	1			13,3025
DATAWAY MEMORY (DISPLAY + READABLE REGISTER)	C 340	INFORMATEK	20 <b>1</b> 10	/72		13.3026
DATAWAY DISPLAY (STORES AND DISPLAYS DATAWAY SIGNALS, FARWQXCIZS152BP1P2)	00	JOERGER CONTROL OF	1	/72	( 6)	13.3027
DATAWAY DISPLAY (SEPARATE R & W DISPLAY, TRACKS OR STORES, MANUAL CLEAR)	202	JORWAY	1	/74	(11)	13.3028
DATAWAY DISPLAY	3290	KINETIC SYSTEMS	1	/72		13,3029
N DATAWAY DISPLAY (WITH MEMORY, FOLLOW, ON-LINE & TRIGGER MODES)	9554	NUCL. ENTERPRISES	1		(13)	13.3030
DATAWAY DISPLAY	C 76451=A16=A1	SIEMFNS	1	/73	(6)	13,3031
DATAWAY DISPLAY MODULE	DD=002	STND ENGINEERING	1	/72	( 5)	13,3032
DATAWAY DISPLAY (DISPLAYS AND STORES DATAWAY SIGNAL PATTERN)	C=D1=24	WENZEL ELEKTRONIK	1	/72		13,3033
34 Module Related T	est Gear (Module	Extenders)				
CAMAC MANUAL MODULE TESTER	6103	RI RA SYSTEMS	NA	174		13,3034
341 Modulę Extenders						
CAMAC EXTENDER MODULE	8201	BI RA SYSTEMS	1	/73		13,3035
EXTENSION FRAME (MODULE EXTENDER)	EF: 1=1	GEC-ELLINTT	1	/71		13,3036
MODULE EXTENDER (+AND=6V,+AND=24V FUSED, RETRACTABLE LOCKING DEVICE)	ME .	JOERGER	(*) <b>1</b>	/72		13,3037
EXTENDER MODULE	11 -	JORWAY	1	/71		13,3038
EXTENDER MODULE (FUSED +8=6V AND +8=24V, SUPPORT ARM)	114	JORWAY	1	174		13.3039
EXTENDER CARD	1100	KINETIC SYSTEMS	1	/71	( 4)	13,3040
EXTENSION UNIT	7007=1	NUCL' ENTERPRISES	1	170		13,3041
BUFFERED EXTENDER (25NSEC PROPAGATION DELAY, 60 CM FLEXIBLE CABLE)	060	POLON	1	03/75		13.3042
EXTENDER MODULE	061	POLON	1	/73		13,3043
EXTENDER	CEX	RDT	1	172		13,3044
MODULE EXTENDER	ME 2030	SEN	1	/70		13.3045
DATAWAY EXTENDER MODULE	EB 01	STND ENGINEERING	1	172		13,3046
EXTENDER (XXX=LFNGTH OF CABLE IN MM BEYOND RACK, SINGLE WIDTH) C (DITO, DOUBLE WIDTH, FIXED SIDES)	577/XXX 5813/XXX	TEKDATA		/72	(5)	13.3047
N (DITO, DOUBLE WIDTH, HINGED SIDES)	5824/XXX		5	/75		
PROLONGATEUR POUR TIROIRS CAMAC CABLE (WIRED EXTENDER)	41401	TRANSRACK	1	/70		13,3048
PROLONGATEUR POUR TIROIRS CAMAC NON CABLE (UNWIRED FXTENDER)	41402	TRANSRACK	1	/70		
37 Other Test Gear fo	or CAMAC Equipn	nent				

1 /73 13,3050 TRANSIENT GENERATOR (MODULE NOISE SUSCEPT TG

# CRATES, SUPPLIES, COMPONENTS, ACCESSORIES

Crates and Related Components/Accessories — Crates with/without Dataway and Supply, Blank Crates, Crate Ventilation Gear 41

#### 411 Crates with Dataway and Supply

	CRATE (270VA, CUNLED, MODULAR POWFRED BY MAX 8x1922 OR 1x1923/1925 + MAX 4x1922)	19024	BORER	25	/69		13,4001
	VOLTAGE REGULATOR (FOR +DR=24V/6A, +/=12V/7A,+/=6V/8A/16A/24A)	1922			/69		
	VOLTAGE REGULATOR (+8-6V 25A MAX, OR 40A MAX WITH EXTERNAL +6V SUPPLY)	1923			/74		
	VOLTAGE REGULATOR (+AND=6V, 25A MAX, 270W RATING, USABLE WITH 4X1922)	1925			/73		
	CAMAC MINICRATE (19 INCH RACK MOUNTING) (+6V/15A,-6V/5A, +24V/2A,-24V/2A,200H)	307,100CC	EDS SYSTEMTECHNIK	17	/73	(10)	13.4002
	POWERED CRATE	MC200	EG&G/ORTFC	25	174		13,4003
N	POWERED CRATE (INCL. CRATE AND POWER SUPPLY COOLING TO SUPPL CP 1 SPEC)	PS 004/PA1/VC 0040	GEC-ELLIOTT	25	05/75		13,4004
c	POWERED CRATE (+8=6V/40A, +8=24V/8A, 200V/,1A, 117V AC, MAX 300W)	CPC/14	GRENSON		/73		13.4005
	POWERED CRATE	1500	SEC 2012/01/02/04/04/05 12:00	NA	/73		
	POWER CRATE (9070 CRATE WITH 9022 POWER SUPPLY)	9071	NUCL. ENTERPRISES	24	/74	(12)	13,4006
	POWERED CRATE (+AND=6V/25A, +AND=24V/6A, (INCL POWER DESIGN TYPE AEC432 SUPPLY)	NSI-875CC100AEC432	NUCL. SPECIALTIES	25	/72		13.4007
	POWERED CRATE (6U, VENTILATED, NO FAN, 130W +6V/15A, =6V/4A, +AND=24V/2A, +200V/50MA)	015	POLON	25	/71		13.4008
	POWERED CRATE	CCHN-CSAN	RDT	25	/71		13,4009
	POWERED CRATE(SEE P7 ALJ 13)	C7 ALJ 13 DW	SAPHYMO-STEL	25		(1)	13.4010
	POWER SUPPLY (CAMAC CRATE)	CM5125/53/DW/BLOCS	SAPHYMO-STEL	25	172		13,4011
	POWERED VENTILATED CRATE (+6V/24A, -6V/16A, +AND=24V/3A, MAX 400W)	C JAL-41	SCHLUMBERGER	25	/73	(8)	13,4012
	POWER CRATE (200W MAX,+6V/25A,-6V/10A,	PC 2006/R	SEN	25	170		13,4013
	+AND=12V/3A,+AND=24V/3A,200V/0,05A) PDWER CRATE (200W MAX,+6V/25A,=6V/10A, +AND=24V/3A,200V/0,05A)	PC 2006/C		25	/71		
	COMPLETE POWER CRATE	CPC 2057	SEN	25	174	(11)	13,4014
	POWERED CRATE (70, VENT, +AND=69/26A, +AND=	C 76455=A2	SIEMENS	25	/71	( 3)	13,4015
	12V/6.5A,+AND=24V/6.5A,200V/0.1A,200W) POWERED CRATE (SAME BUT WITH 117V AC)	C 76455=A1		25	/71		
	POWERED CAMAC CRATE	PCS/12	STND ENGINEERING	25	172		13,4016
	POWERED CAMAC CRATE	PC3/42	STND ENGINEERING	25	172		13,4017
N	POWERED CRATE (SEE CRATE C-CF AND SUPPLY	C=CF + P=156	WENZEL ELEKTRONIK	25	05/75		13,4018
	P=156 FOR RATINGS)  POWERED CRATE (SEE C=CF & SUPPLY P=264)  POWERED CRATE (SEE C=CF & SUPPLY P=300F)	C=CF + P=264 C=CF + P=300F		25 25	03/75 04/75		
	412 Crates with Dataway, v	vithout Supply					
	VENTILATED CRATE (HEAVY DUTY 25 STATION FASTON CONNECTORS, 6U HIGH)	VC 0022	GEC-ELLIOTT	25	174		13,4019
N	(SAME BUT WITH ALL PATCH LINES BUSSED AS PER COGELAB REQUIREMENTS)	VC 0030		25	/74		
N	5U CRATE 25 STATION HEAVY DUTY, FITS TO PS 0004 USING ADAPTOR PA 1.	VC 0040	GEC-ELLINTT	25	05/75		13,4020
	CONVERTS FASTON CONNECTORS TO RECOMMEND- ED FIXED POWER CONNECTOR ON CHOSEN CRATE	/AMP	GEC-ELLIOTT		/73		13,4021
	CAMAC CRATE VERDRAHTET (EMPTY CRATE WITH WIRED DATAWAY)	2,084,000,6	KNUERR	25	/73	(2)	13,4022
	CRATE	9070	NUCL. ENTERPRISES	24	174		13,4023
	CAMAC COMPATIBLE CRATE (WIRED)	NSI-875 DB-WV	NUCL. SPECIALTIES	25	/71		13.4024
	CAMAC CRATE (WIRED)	NSI=875 CC 100	NUCL. SPECIALTIES	25	/72		13,4025
	UNPOWERED CRATE WITH DATAWAY (6U, EMPTU, VENTILATED, NO FAN)	012	POLON	25	/71		13,4026
	UNPOWERED CRATE WITH DATAWAY (360 MM) (525 MM)	CM 5125/33/DW CM 5125/53/DW	SAPHYMO-STEL	25 25			13.4027
	INPOWERED CRATE WITH DATAWAY AND CONNECTORS	UPC 2029	SEN	25	/70		13,4028

NC	DESIGNAT	ION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	CRATE (WIRED CRATE)		WCS	STND ENGINEERING	25	/72	(5)	13,4029
N	WIRED CRATE (HEAVY DUNIT, 60, USE WITH P		C+CF	WENZFL ELEKTRONIK	25	03/75		13,4030
	CRATE (WITH DATAWAY	AND VENTILATION)	C 76455=A3	SIFMENS	25	/72		13,4031
	413	Crates without Dataw	ay, with Supply					
	CAMAC CRATE		DO .200=3001	DORNIER	NA	174		13,4032
	(+6Y/25A,-6Y/12,5A,+ (SAME WITHOUT +8=12Y		DD 200-3002		NA	/74		
	417	Blank Crates and Othe	er Components and A	ccessories				
	CRATE (5U,EMPTY, 25 (SAME BUT WITH CRATE (6U,EMPTY,WITH	24 STATIONS)	MCF/5CAM/S/25 MCF/5CAM/S/24 MCF/6CAM/SV/25	TMHOF-BEDCO	25 24 25	/71 /72 /71		13,4033
	25 STATIONS, HARWELL (SAME BUT WITH CRATE (6U, EMPTY, WITH REMOVABLE PANEL, 25	24 STATIONS) VENTILATION RAFFLE, STNS, HARWELL 7000)	MCF/6CAM/8V/24 MCF/6CAM/8VR/25		24 25	/72 /71		
	(SAME BUT WITH	24 STATIONS)	MCF/6CAM/SVR/24		24	/72		
	CAMAC CRATE (EMPTY) CAMAC CRATE (EMPTY, I CHASSIS AND VENTILAT		2,080,000,6 2,086,000.6	KNUERR	25 25	/70	( 2)	13,4034
	CAMAC COMPATIBLE CRA	TE	NSI 875 DB/WV	NUCL. SPECIALTIES	25	/70		13,4035
	CAMAC CRATE (UNWIRED	)	NSI 875 CC 100	NUCL. SPECIALTIES	25	/72	( 5)	13,4036
	CHASSIS CAMAC (6 UNI	TES AVEC FENTE	9905=1=05	nsı	25	/71		13,4037
	DE VENTILATION, 525	MM PROFONDEUR)	9905=2=05		25	/71		
	CAMAC CRATE WITH VEN		9905HVD3/98/525	OSL	25			13,4038
		( 6U, 525MM DEPTH ) T WITH 460MM DEPTH ) T WITH 360MM DEPTH )	99055HV3AVD/98/460 99055HV3AVD/98/360		25 25			
	CRATE (60, EMPTY, VE	NTILATED, NO FAN)	010	POLON	25	/71		13,4039
	VENTILATED CRATE NO	POWER NO DATAWAY	CCHN	RDT	25	/71		13,4040
	(TWO FANS) (SAME WITH 3 F	ANS)	CCHNA		25	172		
	UNPOWERED CRATE		UC 2057	SEN	25	174	(11)	13,4041
	CAMAC CRATE (EMPTY C	RATE)	c	STND ENGINEERING	25	/72		13,4042
	CHASSIS CAMAC NORMAL		40206	TRANSRACK	25	174		13,4043
	(##7 FOR 460MM & ##8		4020*		25			
	CHASSIS CAMAC 50 UTI		40203	TRANSRACK	25	174		13.4044
	TOTAL, 360MM DEEP, VEN		4020*		25			
	CHASSIS CAMAC 50 UTI		40200	TRANSRACK	25	174		13.4045
	TOTAL, 360MM DEEP, WIT (*=1 FOR 460MM & *=2		4020*		25			
	CAMAC CRATE (EMPTY) 6U WITH VENTILATION 5U NON VENTILATED DEPTH OPTIONS 360MM,	BAFFLE	9905=5HV 9905=5H	UST/MITTSHEK#Onick	25 25	/73 /73 /73		13,4046
	CAMAC CRATE WITH VEN	TILATION BAFFLE	99055HV3AVD/98/525	OSL/WILLSHER&QUICK	25	/73		13,4047
	(6U, 525MM DEPT (SAME BUT WITH (SAME BUT WITH	460 MM DEPTH)	99055HV3AVD/98/460 99055HV3AVD/98/360		25 25	/73 /73		
	VENTILATION UNIT		CAM/FV	IMHOF=BEDCO		/73		13,4048
	LUFTEREINHEIT (VENTI		2.081.000.6	KNUERR		/70		13,4049
	WITH 3 FANS AND FIL		2.085.000.6					
	AIR SCOOP (STOPS CHI		NSI=12109=AS	NUCL. SPECIALTIES	NA	/71		13,4050
	VENTILATION MODULE		VM 2057	SEN		/74	(11)	13,4051
	10 VENTILATION GRILL		1 UG	OSL/WILLSHER&GUICK		/72		13,4052
	CARD EXTENDER (FOR S	UPPLY OF 2057)	CE 2061	SEN				13,4053

Supplies and Related Components/Accessories — Single-and Multi-Crate Supplies, Blank Supply Chassis, Control Panels, Supply Ventilation 42

#### 421 Multi-Crate Supplies

C	POWER SUPPLY FLEXIBLE SYSTEM (TO SPECS	CPU/10	GRENSON	/71	13.4054
	CERN-ISR-CO/72-43), COMPRISING				
	BASIC CRATE(FOR SUPPLY MODULES, INCLUDES	CFC			
	REFERENCE, CONTROL AND 200V/0.1A)				
	SUPPLY MODULE ( * IN TYPE = P FOR POS AND	CF*/6		A destruction of the second	
	N FOR NEG DITPUT VOLTAGE 6V/ 6A)	C1 -70			
	(12V/ 3A)	CF*/12			
	(24V/ 3A)	CF*/84			
		Dates For Build Build State			
	POWER SUPPLY SYSTEM (CRATE)	C4BMT204/C6BMT306	SAPHYMO-STEL	172	13.4055
	(MODULE OPTIONS AS FULLOWS)				
	POWER SUPPLY MODULE 6 V/10 A	BP 75 6.10			
	(6V/20A & 6V/40A OPTIONS ALSO AVAILABLE)	SECOND STREET, SECOND		12 1 10 10 10 10 10 10 10 10 10 10 10 10 1	
	12 V/ 2 A	BSN		THE RESERVE OF THE PERSON	
	(ALSO 12V/4A, 7A, 15A & 25A OPTIONS)				
	24 V/ 1.2A	BSN			
	(ALSO 24V/2 54, 3.54, 94 & 154 OPTIONS)	B3N			
	(ALSU 24V/2 has 5.5As VA & 15A UPTIONS)				

#### 422 Single-Crate Supplies

N	POWER SUPPLY AND COOLING UNIT (+6V/42A, -6V/25A, +8-24V/6A, 375W, 2U FAN UNIT)	PS 0004	GEC-FLLIOTT	05/75	13,4056
	CAMAC POWER UNIT (+6V/15A.=6V/3A,+24V/2A =24V/2A,200V/0,05A,117VAC)	CPU/4	GRENSON		13,4057
	CAMAC POWER SUPPLY - RACK MOUNTING (+6V/20A,-6V/5A,+AND=24V/5A,200V/0,05A)	CPU/2	GRENSON	/71	13,4058
	CAMAC POWER SUPPLY - RACK MOUNTING (+6V/20A,-6V/5A, +&=12V/2A, +&=24V/3A)	CPU/8	GRENSON	/71	13,4059
	POWER SUPPLY (RACK MOUNTING, +64/25A, -64/15A, +AND=244/5A, 2004/0, 1A)	CPU/6	GRENSON	/71	13,4060
	POWER SUPPLY (RACK MOUNTING, +6V/25A, -6V/15A, +AND=24V/5A, +AND=12V)	CPU/7	GRENSON	/71	13,4061
	POWER SUPPLY (+6V/20A,-6V/5A, +AND=24V/5A,200V/0.05A)	9001	NUCL. ENTERPRISES	/71	13,4062
	POWER UNIT (+6Y/15A,=6Y/3A, +AND=24Y/2A,200Y/0,05A)	9022	NUCL. ENTERPRISES	/71 (2)	13,4063
	POWER SUPPLY (BACK MOUNTING, +6V/15A, -6V/4A, +AND-24V/2A, +200V/50MA, 130W)	CZC=10	POLON	/73	13,4064
	POWER UNIT (+6V/20A, =6V/15A,+24V/2A, =24V/2A,200V/0.1A)	SP 426	POWER ELECTRONICS	/74	13,4065
N	POWER UNIT (+6V/25A, =6V/25A, +24V/5A, =24V/5A, 200V/100MA)	SP 558	POWER ELECTRONICS	/75	13,4066
	POWER SUPPLY (+6V/25A,=6V/5A, +AND=12V/2A,+AND=24V/3A,200V/0.1A)	c 303	RDT	/71	13,4067
	POWER SUPPLY UNIT -MAINTENANCE ONLY- (+64/10A,-64/2A,+AND-24/1.5A) (+64/5A,-64/1.5A,+AND-12/1.5A, +AND-24/1.5A) -MAINTENANCE ONLY-	P4 ALJ 13 P6 ALJ 13	SAPHYMO-STEL	/71	13,4068
1	(+6V/25A,=6V/10A,+AND=12V/3A, +AND=24V/3A,+200V/0,1A,MAX 200W)	P7 ALJ 13	SAPHYMO-STEL	ATTORNE SHIETH	13,4069
	POWER SUPPLY (+6V/32A, +6V/32A, +24V/6A, -24V/6A, +200V/.1A, 300W. POWER FAIL LAM)	PS 2057	SEN	/74 (11)	13.4070
	SUPPLY (+AND=6V/26A,+AND=12V/6,5A,+AND= 24V/6,5A,200V/0,1A,117V AC, 200W MAX) SUPPLY (SAME BUT WITHOUT 117V AC)	C 76455=A4	SIEMENS	/72	13.4071
	POWER SUPPLY (+AND=6Y/6A SHARED AND +AND=24Y/2A SHARED, METERING OF Y AND I)	825	STND ENGINEERING	/72	13.4072
	POWER SUPPLY AND BLOWER UNIT	1410	STND ENGINEERING	/72 (5)	13,4073
	CAMAC POWER SUPPLY	1510/12	STND ENGINEERING NA	/72	13.4074
	CAMAC POWER SUPPLY	1510/42	STND ENGINEERING NA	/72	13,4075
N	PLUG-IN POWER SUPPLY 156W (+-6V/5A,	P=156	WENZFL ELEKTRONIK	05/75	13.4076
N	+=12V/5A,+=24V/1A,117VAC) PLUG=IN POWFR SUPPLY 264W (+=6V/10A,	P=264		03/75	
N	+=12v/2A,+=24v/2A,OPT.+200v/40MA,117vAC) PLUG=IN POWER SUPPLY 300WRFAN(+=6v/32A, +=12v/3A,+=24v/6A,+200v/100MA,117vAC)	P=300F		04/75	

#### Blank Supply Chassis, Other Components/Accessories 427

POWER SUPPLY CRATE (STANDARD) POWER SUPPLY CRATE (WIRED)	MCF/4/PPC MCF/PPC/WV	IMHOF-BEDCO	NA NA	/71 /71	13,4077
NETZTEILCHASSIS (EMPTY SUPPLY CHASSIS)	2.082.000.6	KNUERR		170	13,4078
POWER SUPPLY CRATE (FOR SEPARATE SUPPLY)	CSAN	POT POT		/71	13,4079
MAINS SWITCH ASSEMBLY	MS 3	GEC-ELLIOTT	NA .	/71	13,4080
POWER INDICATOR	0704	NUCL' ENTERPRISES	NA	170	13,4081

Recommended or Standard Components/Accessories — 43 Branch Cables, Connectors etc., Dataway Connectors, Boards etc., Blank Modules, Other Stnd Components

#### 431 Branch Related (Cables, Connectors etc.)

	BRANCH HIGHWAY CABLE	8102	BI RA SYSTEMS	773	13,4082
	BRANCH HIGHWAY CABLE	BH001	EG8G/ORTEC	/71	13,4083
	BRANCH HIGHWAY CABLE ASSEMBLY	CC 66 POL PB=27	EMIHUS	/71	13.4084
	(WITH CONNECTORS, 27 CM LONG) (XX CM LONG, PVC JACKET)	CC 66 POL PB=XX			
	BRANCH HIGHWAY CABLE	CD 18067=27	EMIHUS	/70	13,4085
	(COMPLETE PTFE CABLE ASSEMBLY,27CM LONG) (**** 107, 207 - OR CUSTOMER SPECIFIED - FOR CORRESPONDING LENGTH IN CM)	CD 18067/***		9923414) /71 3344635 14 803414) 804624	
	BRANCH HIGHWAY CABLE (WITH CONNECTORS, 27 CM LONG)	BHC 027	GEC-ELLINTT	172 Jan 172	13,4086
	SAME, ***=067,107 & 207 FOR CORRESP LENGTH IN CM,OTHER LENGHTS TU SPEC ORDER	BHC *** 153 585 581		/72	
	BRANCH HIGHWAY CABLE		JOERGER		13,4087
	BRANCH CABLE WITH CONNECTOR (1.5 FT TO 75 FT LONG)		JORWAY	day and 771 mouse out	13,4088
	BRANCH HIGHWAY CARLE (66 TWISTED PAIRS)	CL 90	SCHLUMRERGER	/71	13.4089
	BRANCH HIGHWAY CABLE ASSEMBLY (COMPLETE	BHC 27	SEMRA-BENNEY	/72	13,4090
	(SAME, XXX=LFNGTH IN CM, 040,100 ETC)	BHC XXX		/72	
C	BRANCH HIGHWAY CABLES (COMPLETE WITH CONNECTOR, XXX = LENGTH IN METERS)	2000/132/XXX	TEKDATA PERSONALA	/71 ( 4)	13.4091
	BRANCH HIGHWAY CONNECTOR (FREE MEMBER, PIN MOULDING WITH METAL PIN PROTECTOR)	WSS0132P08BN527=M	FMTHUS	/73	13,4092
	BRANCH HIGHWAY CONNECTOR (FIXED MEMBER, SOCKET MOULDING)	WS\$0132500BN000	FMIHUS	/70	13.4093
	(FREE MEMBER, PIN MOULDING, PXX YYY SELECTS JACKSCREW)	WSS0132PXXBNYYY		SELECT STREET STREET, A	
	HOOD (FOR FREE MEMBER)	WAC 0132 H005	AND TRUE PROPERTY.	And the street, the i	
	BRANCH HIGHWAY CABLE ONLY (PLAIN PVC JACKFT)	66 POL PR	EMTHUS	10 mg 3 and 271	13.4094
	EXTENDED BRANCH CABLE (LOW COST TELE- PHONE CABLE FOR LONG BRANCH RUNS)	EBC XXXX	GEC-ELLIOTT	/72	13,4095
	BRANCH HIGHWAY CABLE (132-WAY)	LIY=Y72X2X0.088	LEGNISCHE	/72	13.4096
	BRANCH HIGHWAY CABLE (TRUE 132-WAY WITH METALISED POLYESTER SCREEN, PVC JACKET)	LI2Y(ST)Y66X2X0.18	LEONISCHE	Participant Find E. d. S. os.	13,4097
	CABLE FOR BRANCH HIGHWAY (PVC JACKET)  (BRAIDED RILSAN JACKET)	132 PE 189 132 PE 210 132 PE 291	PRECICABLE BOUR	/71 /72	13,4098
	(MEPLAT 20MMX10.8MM, GAINE PVC NOIR)	CD 18106	FMIHUS	/72	13.4099
	CABLE EXTENSION MODULE (JOINS TWO BRANCH HIGHWAY CABLES)	CO 10100	THE STATE OF THE S	STEEL TELATOR DESMI	34443
	BRANCH HIGHWAY TO PDP-11 (COMPLETE WITH CONNECTORS, XXX= LENGTH IN METERS)	5805/P/132/XXX	TEKDATA	/73 (8)	13.4100
	BRANCH HIGHWAY JUNCTION BOX	5849	TEKDATA	/75	13,4101

#### 432 Dataway Related (Connectors, Boards, Assemblies)

ADDRESS & FUNCTION DECODING PC	AFD 2066	SEN ATTEMENT		13.4102
DATAWAY MOTHERBOARD (MULTILAYER PNB)	DM=1	STND ENGINEERING	/72	13.4103
DATAWAY MOTHERBOARD (WITH CONNECTORS)	1186	WEHRMANN	/74 (10	13,4104
DATAWAY SOCKET (MOTHERBOARD COMPLETE WITH 25 CONNECTORS)	CIM	RDT	/7.0	13,4105
DATAWAY MINT WRAPPING	J/DW	SAPHYHO-STEL	/71	13,4106

NC	DESIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
	DATAWAY MOTHERBOARD ASSEMBLY	DM 2	STND ENGINEERING		/72		13,4107
	DATAWAY CONNECTOR, EDGE TYPE II	1=163633=0	AMP AG		/70		13,4108
	(MIRE MRAP) (TERMI=POINT/MIRE HRAP) (MOTHERBOARD SULDER) (WIRE SOLDER)	1=163634=0 1=163635=0 1=163636=0			/70 /70 /70		
	DATAWAY CONNECTOR WITH CARD GUIDES (MAND SOLDER, DIP SOLDER & MINI-WRAP)	PBC SERIFS	RURNDY	NA	174		13.4109
	DATAWAY CONNECTOR (MINIWRAP)	EAA 043 D301	FMIHUS		/71	( 2)	13,4110
	CONNECTEUR, FUTS DROITS (DATAMAY CONNECTOR, STRAIGHT PINS) FUTS WRAPPING (WIRE WRAP PINS) FUTS A SOUDER (SOLDER PINS)	KF86 254 BED T KF86 254 BEY T KF86 254 BES T	FRA CONNECTRON		/70		13,4111
	CAMAC DATAWAY CONNECTOR (* INSERT A FOR SOLDER TAG, B SOLDER PIN, C MINI WRAP)	G03D 086P 2B * BL	ITT CANNON		/73	( 6)	13,4112
	CAMAC-LEISTE (DATAWAY CONNECTOR, WIREWRAP)	4,000,060,0	KNUERR		/70		13,4113
	DATAWAY FEMALE CONNECTOR, MINI-WRAP +01 FOR WIRE SOLDER, 5 FOR BOARD SOLDER	2422 061 64334 2422 061 643*4	PHILIPS		/71	(5)	13,4114
	DATAWAY MALE CONNECTOR (MATING THE CRATE MOUNTED 86-WAY CONNECTOR SOCKET)	2422 060 14314	PHILIPS		/72	( 5)	13,4115
	CONNECTEUR 254 QUUBLE FACE (DATAWAY CONNECTOR, MIRE WRAP)	254 DF 43 BWV	SOCAPEX		/70		13,4116
	(MOTHERADARD SOLDER) (WIRE SOLDER)	254 DF 43 AYV 254 DF 43 AZV			/70 /70		
	DATAMAY CONNECTOR (MINI-WRAP) (WIRE-SOLDER) (FLOW SOLDER)	8606 86 21 15 000 8606 86 21 10 000 8606 86 21 14 000	SOURIAU		/71		13.4117
	DATAWAY CONNECTOR (*=2 FLOW SOLDER, *=3 SOLDER LUGS, *=4 MINIWRAP, AU PLATING)	C 288* CSP 221	UECL		/71		13.4118
	(FLOW SOLDER,NI + AU PLATING) (13 MINIWARP CUNTACTS,UTHER ARE FLOW SOLDER,NI + AU PLATING)	C 2885 CSP 221 C 2886 CSP 221					3414 TO
	(+m7 MINIWRAP, +m8 SOLDER LUGS, NI + AU PLATING)	C 288* CSP 221					
	HOUNTING BRACKETS FOR ABOVE	C 8523					
	DATAWAY CONNECTOR HOOD (43-WAY DOUBLE SIDED, 2.54 MM PITCH CONTACTS)	8 4051	TEKDATA	1	/75		13.4119
	433 Module Related (Blan	k Modules, Patchboa	rs etc.)				
	CAMAC CARRYING CASE (TAKES 8 MODULES)	C/NCC8-4	HENESA		/73		13,4120
	CAMAC CARRYING CASE (TAKES 12 MODULES	C/NCC12=6	HENESA		/73		13,4121
	BLANK MODULE KIT (SINGLE WIDTH) (SAME, *=2,3 & 4 FOR CORRESP WIDTH)	BM 1 BM #	GEC-ELLIOTT	1	/73		13.4122
	SINGLE CARD MOUNTING KIT (EMPTY MODULE, SMORT SCREEN PLATE)	CAM/M1/A	IMHOF-REDCO	1	/72		13.4123
	(SAME, *=2,3 & 4 FOR CORRESP WIDTH) SINGLE CARD MOUNTING KIT (EMPTY MODULE, (EMPTY MODULE, LONGT SCREEN PLATE)	CAM/M*/A CAM/M1/B		i	/73 /72		
	(SAME, +=2,3 & 4 FOR CORRESP WIDTH)	CAM/M*/B			/73		
	CAMAC HARDWARE	CH-001	KINETIC SYSTEMS	1	/71	(4)	13.4124
	CAMAC-KASSETTE (EMPTY HODILE, WIDTH 1/25) (*=2,3,4,5,6 FOR CORRESPONDING WIDTHS)	2.090.001.8 2.090.00*.8	KNUERR	1	/70 /70	( 2)	13,4125
	CAMAC COMPATIBLE MODULE (EMPTY, WIDTH=1, ALSO IN 2 & 3 UNIT WIDTHS)	NSI 875 DM	NUCL. SPECIALTIES	1	/70		13.4126
	CAMAC MODULE (EMPTY MODULE MARDWARE) (SAME, *= 2, 3, & 4 FOR CORRESP WIDTH)	NSI 875 CM=100=1 NSI 875 CM=100=*	NUCL. SPECIALTIES	1	/72 /72	(5)	13,4127
	CAMAC MODULE, SHIELDED (EMPTY, 1 WIDTH) (SAME, *=2, 3, AND 4 FOR CORRESP WIDTH)	NSI-875-DM/SPH-1 NSI-875-DM/SPH-*	NUCL. SPECIALTIES	1	/71 /71		13,4128
	CAMAC MODULE (EMPTY, M=1/25) (*=2,3,4,6 & 8 FOR CORRESP MIDTH) (*=0&2 FOR MIDTH 10 & 12 RESPECTIVELY)	021 02* 03*	POLON	1	/71 /71 /71		13,4129
	EMPTY MODULE 1 UNIT (SAME, +=2,3 & 4 FOR CORRESP WIDTH)	CCA 1	RDT	i	/70		13,4130
	EMPTY MODULE SCREENED (1 WIDE, ADD TYPE SUFFIX A FOR SHORT, B FOR LONG SCREENS) (DITO, *=2,3,4 or 6 FOR CORRESP WIDTH)	CM1	SEMRA-RENNEY	1	/73		13.4131
	MODULE MARDWARE (EMPTY MODULE, W#1/25, ALSO AVAILABLE W#2/25,3/25 % UP TO 8/25)	11	STND ENGINEERING	1	/72		13,4132
	TIROIRE MODULAIRE POUR CARTE BASCULANTE	41405	TRANSRACK	2	/72		13,4133
	(EMTY MODULE FOR MINGED CARD) TIROIRE MODULAIRE POUR 2 CARTES BASCUL. (EMTY MODULE FOR 2 MINGED CARDS)	41406		3	/72		

	DECIGNATION & SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR	REF. No.
NC	DESIGNATION & SHORT DATA		MANOTAGTOTIC				
	TIRDIR MODULAIRF (EMPTY MODULE, W=1/25) (**2,3,4 & 5 FOR CURRESPONDING WIDTH)) (**=06,08,10 AND 12 FOR CORRESP WIDTH)	TM 50125 TM 50*25 TM 5**25	TRANSRACK	1	/70		13,4134
	CAMAC MODULE (EMPTY, 1/25 CARD MODULE) (**2,3 & 4 FOR CORRESPONDING WIDTH)	CAMCAS 1 CAMCAS *	WILLSHER & QUICK	1	/71	( 2)	13,4135
	CAMAC MODULE (EMPTY, 1/25 CARD MODULE) (*=2,3 & 4 FOR CORRESPONDING WIDTH)	CAMCAS 1=G CAMCAS *=G	WILLSHER & QUICK	1	/72 /72		13.4136
	CAMAC MODULF (EMPTY, 1/25 SCREENED MODULE) (*=2,3 & 4 FOR CORRESPONDING WIOTH)	CAMMOD 1=G CAMMOD *=G	WILLSHER & QUICK	1	/72 /72		13,4137
	CAMAC MODULE (EMPTY, 2/25 SCREENED MODULE) (**3 & 4 FOR CORRESPONDING WIDTH)	CAMMOD 2 CAMMOD #	WILLSHER & GUICK	2	/71	(5)	13,4138
	EMTY MODULE WITH HINGED CARDS (2/25) (3/25)	9905=CR2 9905=CR3	OSL/WILLSHER&QUICK	2 3	/73 /73		13.4139
	EMPTY MODULE (1/25) (*** 12, 13, 14, 15, 16, 18, 110, AND 112 FOR CORRESPONDING WIDTH)	9905=5T1 9905=5**	OSL/WILLSHER&QUICK	1	/73 /73		13,4140
	TIRGIR MODULAIRE POUR COMMANDE	9905=TC=1	nsı	1	/71		13,4141
	TIRGIR MODULAIRE DE COMMANDE (SUPPLY CONTROL MODULE)	41703	TRANSRACK	1	/70		13,4142
	BLANK CAMAC MODILE PC BOARD (GOLD PLATED & ETCHED FINGERS BUTH SIDES)	NSI=04071=PC	NUCL. SPECIALTIES	•	/71		13.4143
	GENERAL-PURPUSE IC PATCH BOARD	18605	VERO ELECTRONICS		. 174		13,4144
	MK-1 KLUGE MODULE	8301	BI RA SYSTEMS	2	/73		13,4145
	(131 MIXED 14, 16, 24 PIN SOCKETS) MK-5 KLUGE MODULE (HAS 70 14 PIN, 13	8305		2	/73		
	AND 2 24 PIN WIRE HRAP SOCKETS) MK=6 KLUGE MODULE (HAS 34 14 PIN, 16 16 PIN & 3 24 PIN WIRE HRAP SOCKETS)	8306		1	/73		
	CAMAC-UNIVERSAL-BOARD (PRINTED CARD MODU- LE WITH 28 14-PIN + 28 16-PIN SOCKETS)	DO 200=2900	DORNIER	2	/71		13.4146
	CAMAC PROTOTYPE ASSEMBLY BOARDS (MX B1 HAS 68 SITES, MX B2 MAS 80 SITES) (MX B3 HAS 68 SITES, MX B4 HAS 80 SITES, MX B3/MX B4 INCLUDE 54 CIRCUIT)	MX B1/MX B2 MX B3/MX B4	GEC-ELLINTT	NA NA	/71		13.4147
	PRINTED CIRCUIT TEST BOARD	10	JORWAY	1	/71		13,4148
	KLUGE BOARD FOR WIRE WRAP	15	JORWAY	3	174		13,4149
	KLUGE CARD (FOR CREATING YOUR OWN CAMAC	2000=36	KINETIC SYSTEMS	1	/71	(4)	13.4150
	MODULES) KLUGE CARD	2000		1	/73		
	EXPERIMENTIERPLATTE	4,000,087.0	KNUERR	NA	/70		13,4151
	(PRINTED CIRCUIT BOARD) EXPERIMENTIERPLATTE (P.C.R.)	4.000.088.0		NA	/73		
	DECODED MATRIX ROARD (FOR PROTOTYPE WIRING OF 64 14-PIN SITES, A&F DECODED)	D 21 62	NUCL. ENTERPRISES	0	/74		13,4152
	MODULE PRINTED CIRCUIT BOARDS (TAKE 24,16	CBP 1	RDT	NA	/72		13,4153
	OR 14 PIN, ON THE WHOLE 1092 PINS) (SAME, WITH MINI=WRAP TO 0V AND +6V)	CBP 2		NA	/72		
	BLANK MODULE (COMPLETE WITH PRINTED BOARD FOR 69 INTEGRATED CIRCUITS: 1 U WIDTH)	BM 2020/1U	SEN	1	/70		13.4154
	(SAME, 2U WIDTH)	BM 2020/2U		2	/70		
	EXPERIMENT PLATE	C 72468=A453=A1	SIFMENS	1	/72		13,4155
	437 Other Recommended	or Standard Compo	nents/Access.				
	NIM/CAMAC ADAPTOR	NCA=1	GEC-FLLIOTT		/74		13,4156
	NIM ADAPTOR	9072	NUCL. ENTERPRISES		174		13,4157
	NIM-CAMAC ADAPTOR	CAN	RDT	NA	/71		13,4158
	NIM/CAMAC ADAPTOR	ANC 10	SCHLUMBERGER		/72		13,4159
	CAMAC NIM ADAPTOR	CNA 2033	SEN	2	/71		13,4160
	LAM GRADER CABLE (20CM, WITH CONNECTORS) (40CM, WITH CONNECTORS)	LGC 20 LGC 40	GEC-ELLIOTT		/72 /72		13.4161
	LAM GRADER CABLE		JOERGER				13,4162
	52 WAY CANNON 208528 HARNESSES LAM GRADER CARLE, XXX= LENGTH IN METERS)	5809/\$/52/XXX	TEKDATA		/73		13,4163
	LAM GRADER CONNECTUR (52=PIN FIXED MEMBER, TAKES PIN TYPE 031=9540=000)	2 DB 52 P	TTT CANNON		/70		13,4164
	COAXIAL CONNECTOR (PANEL MOUNTING, CARLE CONNECTOR HAS TYPE F 00.250 & FS 00.250) T= & L=ADAPTERS, FREE DOUBLE SUCKET, AND ARE ALSO AVAILABLE	PA 00.250	LEMO		/70	(4)	13,4165

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# INDEX OF MANUFACTURERS

AEG-Telefunken Elisabethenstrasse 3, Postfach 830 D-7900 Ulm, Germany AMP AG Haldenstrasse 11 CH-6000 Luzern, Switzerland Applied Computer Systems Ltd. 2 Charlton Street, Manchester M1 3JL, England Arsycom B.V. Kabelweg 43-47, Amsterdam 1016, Netherland BF Vertrieb GmbH (Sales of F & H Products in Germany) Bergwaldstrasse 30, Postfach 76 D-7500 Karlsruhe 41, Germany BI RA Systems, Inc. 3520 D Pan American Freeway, N.E. Albuquerque, New Mexico 87107,

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EDS Systemtechnik GmbH Trierer Strasse 281 D-5100 Aachen, Germany EG & G/ORTEC, Inc. High Energy Physics Department 500 Midland Road, Oak Ridge, Tennessee 37830, USA J. Eisenmann, Elektronik für Prozessautomatisierung

Vogesenstrasse 6 D-7513 Stutensee-Buechig, Germany Emihus — See Hughes **FRB** Connectron 3-5, Rue des Tilleuls, F-92600 Asnières, France Frieseke & Hoepfner GmbH Export Dept. & Production Tennenloher Strasse D-8520 Erlangen-Brück, Germany

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C Imhof-Bedco Standard Products Ltd Colne Way Trading Estate, By-Pass, Watford, Herts, England Informatek Z.A. de Courtabœuf, B.P. 81 F-91401 - Orsay, France

ITT Cannon — See Cannon J and P Engineering (Reading) Ltd. Portman House Cardiff Road, Reading Berkshire RG1-8JF, England

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Jorway Corporation 27 Bond Street, Westbury, New York 11590, USA

Kinetic Systems Corporation Maryknoll Drive, Lockport, III. 60441, USA

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respectively Willsher and Quick

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Vero Electronics Ltd. Industrial Estate, Chandler's Ford, Eastleigh, Hants SO5 3ZR, England

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Willsher and Quick Ltd.
Walrow, Highbridge
Somerset, England
Willsher and Quick GmbH
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D-4054 Nettetal 2, Germany
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00-086 Warsaw, Bielanska 1, Polar

### INTRODUCTION

The Software Products Section of the CAMAC Products Guide lists a number of software packages, programs and routines which have been developed by software firms, manufacturers of CAMAC equipment, and at research laboratories.

Work is going on to implement IML — the intermediate level CAMAC language. One contribution to IML implementation is listed below, but at least five other laboratories are at present engaged in implementing IML on several computers.

The products listed below are either in current use or will be so in the nearest few months. Some

of the software listed is commercially available, information about other is presumably available from respective authors. The correctness of each entry has been carefully checked against data provided.

Inclusion in the list does not necessarily indicate endorsement, recommendation or approval by the ESONE Committee, nor does omission indicate disapproval.

The classification used tentatively and reproduced below, is the same as was proposed in the March 1974 issue (No. 9) of this Bulletin.

# SOFTWARE CLASSIFICATION GROUPS

	Page			Page
.5	Software.	.54 .541	Support Software I (translators). Assemblers (with/without macros).	XL
.50	Fundamental Concepts, General Subjects. XXXVI General Descriptions, Documentation,	.542 .543	Cross-Assemblers, Cross-compilers. Compilers.	
.501	etc. Languages.	.544	Interpreters.	
.502	Algorithms.	.55 .551	Support Software II. Loaders.	XLII
.51	User-Oriented Programs I (full system support with user run-time and CAMAC system service programs). XXXVII		Linking Programs.	
.52	User-Oriented Programs II (specific run-time programs). XXXVIII	.57 .571	Other Service Programs. Editors.	XLIII
.53	User-Oriented Programs III (subprograms, routines, Hardware programs). xxxvIII	.572 .573	Debugging Routines. Test Routines.	

#### .50 Fundamental Concepts, General Subjects

READER SERVICE CLASS CODE -TITLE- - -AUTHOR(S)- -

PS'REF. 13, 5001
.50
IMPLEMENTING CAMAC BY COMPILERS
W. KNEIS, GFK, ZYKLOTRON-LB.,
KARLSRUME, GERMANY
PROC CAMAC SYMPOS, LIIXMBG, DEC 1973

PURL. REF. .

RS'.REF. 13. 5002

AUTHOR(S) - -

PROCEDURE CALLS - A PRAGMATIC
APPROACH
J. MICHELSON, H. HALLING,
KFA, JUELICH.
PROC CAMAC SYMPOS, LUXMBG, DEC 1973

PURL. REF. -

ESONE REGSTR DATE 31 MAY 1974

READER SERVICE CLASS CODE -TITLE- - -

NAME/ACRONYM =

OPERATIVE DATE=

COMPUTER =

INTERFACE(S) =

SOFTWARE TYPE =

RS'.REF. 13. 5003
.501(PL=11)
CAMAC FACILITIES IN THE PROGRAMMING
LANGUAGE OF PL=11
ROBERT D RUSSELL, CERN, GENEVA
PRIC CAMAC SYMPOS, LUXMBG, DEC 1973
YELLOW REPORT, CERN 74-24, DEC 1974
EXTENDED PL=11
1971/72
PDP=11, MORD LENGTH 16 BITS
CA=11 (EG&G/ORTEC)
LANGUAGE, PL=11(EXTENDED)
IN-LINE CODING OF CAMAC STATEMENTS
SYMBOLIC DEVICE NAME USED
DEMAND HANDLING IS INCLUDED

READER SERVICE
CLASS CODE =
AUTHOR(S) =
NAME/ACRONYM =
COMPUTER =
SOFTWARE TYPE =

RS.REF. 13. 5004
.501 (CATY)
F R GOLDING, DARESBURY LABORATORIES
CATY

LANGUAGE (BASED ON BASIC)

NEW ENTRY
RS.REF. 13. 5005
.501 (CATY)
SPECIFICATION OF THE LANGUAGE CATY C1030
R F CRANFIELD, GEC ELLIOTT
(SFE ALSO PREVIOUS ENTRY)

CATY
GEC ELLIOTT (SEE LIST OF MANUFACTURERS)
DESCRIPTION
LANGUAGE (BASED ON BASIC)

READER SERVICE CLASS CODE -TITLE- - -

RS'.REF. 13. 5006
.501 (IML)
THE DEFINITION OF IML
A LANGUAGE FOR USE IN CAMAC SYSTEMS
ESONE COMMITTEE, SOFTWARE W.G. AND
AEC NIM COMMITTEE, SOFTWARE W.G. AND
AEC NIM COMMITTEE, SOFTWARE W.G.
REPORT ESONE/IML/01, OCT 1974, AND
REPORT TIO-25615, JAN 1975
IML PREPARED BY . PUBL REF. -

NAME / ACRONYM - MAINTENANCE BY-

IML
ESONE COMMITTEE IN COLLABORATION
WITH NIM COMMITTEE
ESONE SECRETARIAT AND U.S. GOVERNMENT PRINTING OFFICE RESPECTIVELY
AUG/SEPT 1974
ANV OBTAINABLE FROM

ESONE REGSTR DATE
COMPUTER SOFTWARE TYPE -

LANGUAGE

NEW\*\*\*\*\*\*\*\*\*
PEADER SERVICE
CLASS CODE =
TITLE= - - AUTHMR(S) = NAME/ACRONYM =
OBTAINABLE FROMAVAILABLE ON/AS=
SOFTWARE TYPE=

NEW ENTRY
PS'.REF. 13. 5007
.501 (casic)
J m Servent (SCHLUMBERGER)
CASIC
SCHLUMBERGER (SEE LIST OF MANUFACTURERS) DESCRIPTION
LANGUAGE (EXTENDED BASIC)

DESCRIPTION - 
DESCRIPTION - 
DEMANDS ON REAL-TIME SYSTEMS SUCH AS MINIMUM EXECUTION TIME MINIMUM CORE REQUIREMENTS, FTC., RECOMMEND THE USE OF COMPILERS IN PROGRAMMING, THE POSSTBILITY TO IMPLEMENT A CAMAC LANGUAGE BY A COMPILER IS FIRST OF ALL A FUNCTION OF THE LEVEL AND CONCEPT OF THE LANGUAGE. META-LANGUAGES, THE SYNTAX OF A PROGRAMMING LANGUAGE, ARE USFO TO FORMULATE A COMPILER FOR A SPECIFIC LANGUAGE. THE METHOD DESCRIBED HAS BEEN USFO TO WRITE A COMPILER FOR IML, THE INTERMEDIATE LEVEL CAMAC LANGUAGE, IMPLEMENTED IN AN ASSEMBLER ENVIRONMENT.

DESCRIPTION -DISCUSSION OF PROCEDURE CALLS AS THE MASIS FOR CAMAC SOFTWARE
MITHIN MIGH-LEVEL LANGUAGES. COMPARISON MITH SYNTAX MODIFI=
CATIONS TO LANGUAGES, DISCUSSION OF IMPLEMENTATION
RESTRICTIONS DUE TO LANGUAGE REQUIRFMENTS FOR EXISTING HIGHLEVEL LANGUAGES, E.G. CLOSED SYSTEM-SUBROUTINES WHICH EXECUTE ONE DEFINED OPERATION (INVOLVING ONE OR MORE CAMAC
CYCLES AS A GROUP). COMPARISON OF US-NIM CAMAC FORTRAN
SUBROUTINES AND PROCEDURE-CALL SYNTAX OF ESONE SWG IML
LANGUAGE. APPLICATION OF PROCEDURE-CALLS TO APPLICATION=
ORIENTED SOFTWARE.

DESCRIPTION= =
PL=11 IS AN INTERMEDIATE=LEVEL, MACHINE=ORIENTED PROGRAMMING
LANGUAGE EXTENDED TO INCLUDE CAMAC FEATURES. SYNTACTIC FORM
OF CAMAC STATEMENTS ARE ANALOGOUS TO STANDARD PL=11 STATE=
MENTS. SYMBOLIC NAMES FOR VARIABLES AND FUNCTIONS ARE DE=
CLARED AT ONCE, AND OPERATIONS ARE EXECUTED BY STATEMENTS
REFERRING TO THESE NAMES. USE OF SYMBOLIC NAMES MAKES PROGRAMS READABLE, AND SIMPLIFIES MODIFICATIONS OF CAMAC CONFIGURATIONS.
EXAMPLE OF STANDARD STATEMENT=WHILE PRINTSTATUS = BUSY DO
EXAMPLE OF CAMAC STATEMENT=WHILE CRISTATUS = BUSY DO

DESCRIPTION - CATY IS A MACHINE INDEPENDENT HIGH-LEVEL LANGUAGE BASED UPON A SUBSET OF BASIC WITH EXTENSIONS FOR ADDRESSING CAMAC. PROGRAMS WRITTEN IN CATY ARE COMPILED AND NOT INTERPRETED. THUS, THE SPEED OF OPERATION WHEN CAMAC IS TESTED UNDER CATY IS COMPARABLE WITH THE SPEED OF OPERATION IN APPLICATIONS, CATY HAS BEEN IMPLEMENTED ON SEVERAL COMPUTERS (SEE .543).

DESCRIPTION - THE MAIN SPECIFICATION DESCRIBES THE FACILITIES AVAILABLE IN
THE MACHINE INDEPENDENT HIGH LEVEL LANGUAGE CATY, APPENDICE:
TO THE SPECIFICATION DESCRIBE THE ADDITIONAL FEATURES ASSOCIATED WITH IMPLEMENTATIONS, ALL USING GEC ELLIOTT SYSTEM CRATI
INTERFACES ON THE PDP-11, NOVA, GEC-4080, AND GEC-2050
COMPUTERS.

DESCRIPTION = 
IML IS A LANGUAGE USED TO EXPRESS THE OPERATIONS DESCRIBED IN THE CAMAC HARDWARE SPECIFICATIONS, AND THEIR INTERACTION HITH A COMPUTER SYSTEM. IML STATEMENTS LINK CAMAC STRUCTURES AND HODES OF OPERATION TO DATA STRUCTURES AND REAL =TIME FEATURES IN THE COMPUTER SYSTEM.
THIS DEFINITION IS A GUIDE FOR THOSE IMPLEMENTING LANGUAGES AND OPERATING SYSTEMS WHO WISH TO MAKE CAMAC INPUT/OUTPUT AVAILABLE TO USERS, FFATURES ARE INCLUDED WHICH SUPPORT THE CAMAC BRANCH HIGHWAY AND THE CAMAC SERIAL HIGHWAY.
THE LANGUAGE IS DEFINED SEMANTICALLY = THE SYNTAX USED TO EXPRESS IML DEPENDS ON THE FAVIRONMENT, THE MACRO SYNTAX IML=M1 IS DEFINED IN AN APPENDIX.

DESCRIPTION = CASIC IS BASIC AND PROVIDES ALL STANDARD STATEMENTS OF BASIC PLUS A SET OF CAMAC RELATED STATEMENTS.

CASIC = LIKE BASIC = IS CONVERSATIONAL. THE MOST RECENT VERSION CONFORMS TO THE IML LANGUAGE (SEE .501(IML)) DEFINED BY THE FSONE COMMITTEE.

CASIC IS IMPLEMENTED ON PDP=11 (SEE .544).

# .51 User-Oriented Programs I (full system support)

READER SERVICE CLASS CODE -

AUTHOR(S) = PUBL. REF. = NAME/ACRONYM = AVAILABLE UN/AS OPERATIVE DATE= COMPUTER INTERFACE(S) SOFTWARE TYPE LANGUAGE CAMAC FACILITIES RS'REF. 13. 5008
.51
CAMAC OPERATING SYSTEM OR
CONTROL APPLICATIONS
DR B. MERTENS, IKP, KFA, JUELICH
CAMAC BULLETIN NO 9, MARCH 1974 COS PAPER TAPE, ASCII CODE

RS'REF. 13. 5009

PAPER TAPE, ASCII CUDE
1972
PDP=15, CORE REQUIREMENTS= 16K
TYPE 2200 (BORER)
SYSTEM PROGRAM
FORTRAN & MACRO-ASSEMBLER
SYMBOLIC DEVICE NAMES USED, SINGLE &
MUITIPLE ACTION PER INSTRUCTION,
REAL/TIME DEMEND HANDLING INCORPORATED

DESCRIPTION - THE SYSTEM SOFTWARE PERMITS START AND STOP OF BLOCK TRANSFER FROM THE A/D CONVERTERS TO THE POP-15 MEMORY (LIST MODE OUTPUT ONTO MAGTAPE ON-LINE SORTING IF DESIRED).
THE BORRE INTERFACE MAS BEEN MODIFIED TO ALLOW BLOCK LENGTHS UP TO 4K 18 BIT WORDS.

READER SERVICE CLASS CODE = TITLE= = = =

AUTHOR(S) = -NAME/ACRONYM = AVAILABLE ON/AS OPERATIVE DATE= COMPUTER = INTERFACE(S) -MIN SYSTEM CONFIG

SOFTWARE TYPE -

151
BACKGROUND=FOREGROUND SYSTEM FOR
PULSE=HEIGHT ANALYSIS OF TWO=
DIMENSIONAL MULTIWIRE PROPORTIONAL
CHAMBER DATA
DR A HEUSLFR, IPK, KFA, JUELICH DR A HEUSLEK.

BFG
PAPER TAPE, ASCII CODE

PAPER TAPE, ASCII CODE PAPER TAPE, ASCII CODE
1974?
PDP=15, CORE REGUIREMENTS = 24K
TYPE 2200 (BORER)
HAGTAPE, DECTAPE, DISK, &
MEMORY SCANNING DISPLAY (IN-HOUSE)
SYSTEM PROGRAM
FORTRAN & MACRO-ASSEMBLER

READER SERVICE CLASS CODE -TITLE- - -AUTHOR(8)- -

PURL' REF. 
OPERATIVE DATE
COMPUTER 
INTERFACE(S) 
SOFTWARE TYPE -

RS'REF'. 13. 5010 .51
TRIUMF CONTROL SYSTEM SO THARE
D. P. GURD, W. K. DAWSON, TRIUMF,
UNIVERSITY OF ALBERTA, CANADA
CAMAC BULLETIN NO 5, NOVEMBER 1972

1973
4 SUPERNOVAS
IN-HOUSE TYPE
FULL SYSTEM SUPPORT FOR CONTROL OF
TRIUMF CYCLOTRON

DESCRIPTION = 
THE SYSTEM SOFTWARE PACKAGE MONITORS OVER 1000 ANALOGUE
PARAMETERS AND 1000 DIGITAL STATUS POINTS, SEARCHES OUT-OFLIMIT READINGS, DISPLAYS MEASUREMENTS ON REQUEST,
SETS OVER 300 ANALOGUE POINTS FROM A CENTRAL CONSOLE AND
PERFORMS A NUMBER OF OTHER ROUTINES.
A REAL-TIME EXECUTIVE PROGRAM - NATS (FOR NOVA ASYNCHRONOUS
TASKING SUPERVISOR) - SCHEDILES AND SUPERVISES CAMAC TASKS,
SUPPORTED BY A SUBPROGRAM LIBRARY, AS THEY ARE REGUESTED.
JOBS TO BE PERFORMED ARE STRUCTURED INTO SEGUENCES OF CAMAC
OPERATIONS SPECIFIC TO A PIFCE OF HARDWARE (= CAMAC MODULE).
THERE IS THUS A DIRECT MODULAR HARDWARE-SOFTWARE CORRESPONDENCE, CONTROL IS BASICALLY CLOCK-INITIATED SOFTWARE SCAN OF.
CYCLOTRON MONITORING, BUT INTERRUPTS ARE INCLUDED, MAINLY
INITIATED BY CONSOLE.

NEWA\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = = =
NAME/ACRONYM = OBTAINABLE FROM-SOFTWARE TYPE-COMPUTER - -INTERFACE(S) -

.51
R SIC SINGLE PARAMETER MCA SYSTEM (MISP)
MISP\_ NUCLEAR ENTERPRISES (SEE INDEX OF MFRS) SYSTEM SOFTWARE
PDP=11, 8K MEMORY & REAL TIME CLOCK
9030 (NUCL, ENTERPR)
(PROGRAMMED TRANSFERS & INTERRUPT ONLY)
ADC (LABEN OR 9060),9021 LIVE TIME RTC,
TTV/READER (7064),TEK603/604 OR LANSCOPE HARDWARE CONFIG

NEW ENTRY RS, REF. 13. 5011

DESCRIPTION = =
THE PROGRAM OCCUPIES 2K OF MEMORY AND USES A DATA AREA OF 4K
FOR UP TO 4096 CHANNELS ACQUISITION.
THE PACKAGE CONSISTS OF A DISPLAY DRIVER, A USER ORIENTED
TELETYPE HANDLER, ACQUISITION CONTROL, AND A DATA MANIPULA—
TION ROLITINE.
THE DISPLAY DRIVER IS RUN AS A BACKGROUND TASK WHICH IS
INTERRUPTED BY THE ADC, CLOCKS AND TELETYPE.
THIS PACKAGE CAN RE OBTAINED WITH MULTISCALER OPTION, THE
MARDWARF IS EXTENDED WITH A 9003 OR 003 SCALER, DATA AREA IS
DIVIDED INTO 4 AREAS, EACH ONE THOUSAND CHANNELS.

NEW\*\*\*\*\*\*\*\*
PEADER SERVICE
CLASS CODE =
TITLE= - NAME/ACRONYM =
OBTAINABLE FROMSOFTWARE TYPE=
COMPUTER = =
INTERFACE(S) =

HARDWARE CONFIG

NEW ENTRY RS\_REF. 13. 5012 DUAL MCA SYSTEM (DAMCAS) DUAL MCA SYSTEM (DAMCAS)
DAMCAS
NUCLEAR ENTERPRISES (SEE INDEX OF MFRS)
SYSTEM SOFTMARE
PDP=11, 16K MEMORY & REAL TIME CLOCK
9030 & 9033 (NUCL ENTERPR)
(PROGRAMMED & AUTONOMOUS TRANSFERS)
ADC (LABEN OR 9060),9021 LIVE TIME RTC,
TTV/READER (7064), PUNCH (7065), MAGTAPE
(CS 0042),TEK603/604 OR LANSCOPE DESCRIPTION - THE PROGRAM OCCUPIES 6K LEAVING 10K OF MEMORY FOR DATA ACQUISITION (4K OF 16 RITS & 4K OF 24 BITS).
THE SOFTMARE PACKAGE CONSISTS OF A DISPLAY DRIVER, A TELETYPE
HANDLER FOR OPERATOR CONTROL OF DATA ACQUISITION, DATA MANTPULATION ROUTINE, AND A ROUTINE FOR AUTONOMOUS CONTROL OF
DATA ACQUISITION AND MAG TAPE TRANSFERS.

HARDWARE CONFIG

NEW ENTRY RS.RFF. 13. 5013 .51 MULTI PARAMETER DATA ACQUISITION SYSTEM MULTI PARAMETER DATA ALGUSTION CONTROL WIDAS I NUCLEAR ENTERPRISES (SEE INDEX OF MFRS) SYSTEM SOFTMARE PDP=11, 8K MEMORY & REAL TIME CLOCK 9030 (NUCL. ENTERPR) (PBOGRAMMED TRANSFERS & INTERRUPT ONLY) ADC'S (LAREN OR 9060) & COTNC SELECTOR (CG 9049), 9021 LIVE TIMER RTC, TTY & MAG TAPE, TEK 603/604. DESCRIPTION - THE SYSTEM IS CAPABLE OF ACCEPTING FIVE PARAMETER EVENTS AND STORING THEM ON MAG TAPE, STMULTANEOUSLY PERFORMING MULTICHANNEL ANALYSIS ON ONE SELECTED PARAMETER.
WINDOWS MAY BE SET ON EACH PARAMETER FOR BOTH MODES, TOGETHER WITH A COUNT DIVISION FACTOR SET OVER THE REGION OF INTEREST, DATA DUMPED IN LIST MODE MAY BE READ BACK FOR ANALYSIS.

CLASS CODE =
AUTHOR(S) = NAME/ACRONYM =
OPERATIVE DATE=
SOFTWARE TYPE =

RS'REF. 13. 5014

NO.REF. 13. BU14
.51
D GURD, TRIUMF,UNIV. ALBERTA,CANADA
CAMAC
1973
SYSTEM SOFTWARE

DESCRIPTION = THE SYSTEM SOFTWARE - CAMAC - CONSISTS OF SEVERAL SURROUTINE CALLS, THESE ARE - PRIMITIVE SURROUTINES PERFORMING THE ACTUAL I/O OPERATIONS, MODULE SUBROUTINES, THE MUX/ADC SUBROUTINES, CAMAC LAMS OR INTERRUPTS, SERIAL TASKS, AND AN INTERPRETER (FOR DATA).

# . 52 User-Oriented Programs II (specific run-time programs)

READER SERVICE
CLASS CODE TITLE- - NAME/ACRONYM MAINTENANCE BYOBTAINABLE FROM
OPFRATIVE DATECOMPUTER INTERFACE(S) SOFTWARE TYPE -

RS'.REF. 13. 5015 

DESCRIPTION = THE SOFTWARE PACKAGES ARE COMPLETE OPERATING SYSTEMS.

CONTROLLERS AND OPERATING SYSTEMS ARE RELATED AS FOLLOWS == CA=11=C USES RSX=11=D OPERATING SYSTEM

CA=11=E USES RSX=11=M OR RT=11

CA=11=F USES RSX=11=M OR RT=11

NAME/ACRONYM =
OBTAINABLE FROM=
SOFTWARE TYPE=
COMPUTER = =
INTERFACE(S) =

NEW FNTRY RS.REF. 13. 5016 .52 CASPAC - A SOFTWARE PACKAGE FOR COMMUNI-CATION WITH CAMAC-PROCESS-PERIPHERALS

CASPAC

IDAS (SEE INDEX OF MANUFACTURERS)

SYSTEM OF RE-ENTRANT ASSEMBLER ROUTINES

PDP-11 (DEC), MIN 740 WORDS OF MEMORY

I CP-11 (SCHLUMBERGER)

DESCRIPTION = THE SYSTEM OF ASSEMBLER ROUTINES ALLOW COMMUNICATION WITH CAMAC-PROCESS-PERIPHERALS USING SINGLF-WORD TRANSFER MODE AS WELL AS BLOCK TRANSFER MODE ON FORTRAN AND ASSEMBLER LEVEL. INTERRUPT ACTIONS CAN BE OBTAINED IN THE FORM OF AN ARBITRARY SEQUENCE OF CAMAC TRANSFERS ON FORTRAN LEVEL. NO SOFTHARE OPERATING SYSTEM IS NEEDED, AND CASPAC CAN THEREFORE BE USED AUTONOMOUSLY AS WELL AS IN CONNECTION WITH A REAL TIME OR BATCH OPERATING SYSTEM.

# .53 User-Oriented Programs III (subprograms, etc.)

READER SERVICE
CLASS CODE =
TITLE = = =
AUTHOR(S) = =
PUBL' REF. =

NAME/ACRONYM = MAINTENANCE BY= OBTAINABLE FROM AVAILABLE ON/AS OPERATIVE DATE= COMPUTER = COMPUTER = INTERFACE(S) = MIN SYSTEM CONFIG SOFTWARE TYPE = LANGUAGE = CAMAC FACILITIES

RS'REF. 13. 5017
.53 (BASIC)
CAMAC AND INTERACTING PROGRAMMING
DR E M RIMMER, CERN, GENEVA
PROC CAMAC SYMPOS, LUXMBG, DEC 1973
E RASIC CALLABLE ROUTINES,
NP GROUP NOTE, NP-DHG, CERN
MPCMA, HPCMB, MPCMC
DR E M RIMMER
NP DIV, CERN, CH-1211 GENEVA
PAPER TAPE, ASCII CODE
1971/72
H=P 2100-SERIES, 8K 16 BIT WORDS
2201(BORER), 7218 & HPCC-066(CERN)
TTY OR TEK 4010 TERMINAL & CC-A1
SET OF SUBROUTINES
HP ASSEMBLY
BASIC (NP EXTENSION OF)
TN-LINE CODED CALLS IN BASIC,
SUBROUTINES IN ASSEMBLY, ABS ADDR
SINGLE & MULTIPLE ACTION PER
INSTRUCTION, NO DEMAND HANDLING

READER SERVICE CLASS CODE = TITLE= = = =

FACILITIES -

RS.REF. 13. 5018
.53(FORTRAN)
SPECIFICATIONS FOR STANDARD CAMAC
SUBROUTINES
RICHARD F THOMAS JR.
CAMAC BULLETIN NO 6, MARCH 1973
SEF DESCRIPTION
USAEC NIM COMMITTEE, CAMAC SHG
ALGORITHM
1973
INDEPENDENT, MEMORY SIZE NOT SPEC.
ANY

FORTRAN
FUNDAMENTAL CAMAC OPERATIONS, STANDARD
BLOCK TRANSFERS IN SINGLE & MULTIPLE
ACTION STATEMENTS

AUTHOR(S) = PUBL' REF. =
NAME/ACRONYM =
OBTAINABLE FROM
AVAILABLE ON/AS
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
SOFTWARE TYPE =
LANGUAGE =
CAMAC FACILITIES ANY SET OF SUBROUTINES FORTRAN

READER SERVICE
CLASS CODE =
TITLE= = =
AUTHOR(S) = =
NAME/ACRONYM = RS'REF. 13. 5019 '53(FORTRAN) FORTRAN SUBROUTINES H POHL FORTRAN CALLS FORTRAN CALLS
V002

## PONL, ZEL, KFA, JUELICH
DECTAPE
MARCH 1972
PDP=11, 16K 16 BIT HORDS MEMORY
TYPE 1533A (BORER)
PROCEDURE CALLS
FORTRAN ON PDP=11 (THREADED CODE)
IN-LINE SUBROUTINE CALLS
SINGLE ACTION STATEMENTS NAME / ACRONYM = VERSION = = ORTAINABLE FROM AVAILABLE ON / AS OPERATIVE DATE-COMPLITER = INTERFACE(S) = SOFTHARE TYPE = LANGLIAGE = VACCUMPAGE | VA

DESCRIPTION= =

THESE BASIC=CALLABLE CAMAC SUBROUTINES IN THREE VERSIONS FOR

THREE INTERFACES PROVIDE MOST COMMAND FACILITIES FOR CONTROL

AND DATA TRANSFER. DATA WORDS MAY BE 16 OR 24 BITS LONG

(ONLY 16 BITS FOR HPCC=066), RINARY, BCD OR LOGIC (0 OR 1).

ROUTINES COVER BLOCK TRANSFERS, PROGRAMMED AND SEQUENTIAL.

ADDRESSING R UTILITY ROUTINES, IN TOTAL 18 & 3 OPTIONALLY.

GENERAL FORM OF CALL STATEMENT==

- = CALL (SUBROUTINE NUMBER,C,N,A,F,D,Q)

= = CALL (SUBROUTINE NUMBER,C,N,A,F,D,Q),W)

WHERE W IS MORD COUNT, D IS DATA, C,N,A,F, & Q HAVE USUAL

MEANING

EX== CALL(10,1,2,0,16,D(I),Q,20)

TIME IS APPR 5 MSECS/STATEMENT, BLOCK TRANSFER CALL GENE=

RATED DIRFCTLY BY INTERFACE ARE MUCH FASTER.

DESCRIPTION= =

A SET OF 6 SUBROUTINES, OF WHICH ONE IS CALLED BY ALL THE OTHER PERMITS A GREAT VARIETY OF SINGLE AND MULTIPLE CAMAC OPERATIONS TO BE PERFORMED. DEMAND HANDLING, OTHER THAN BY TEST LAM, IS NOT COVERED.
THE SUBROUTINES EXECUTE CAMAC OPERATIONS AS FOLLOWS==
CMCRSC = SINGLE CAMAC FUNCTION AT SINGLE ADDRESS
ONE OR MORE TIMES
CMCSEG = SINGLE CAMAC FUNCTION AT SUCCESSION OF ADDRESSES
CMCASC = SPECTFIED CAMAC FUNCTION IN ADDRESS SCAN MODE
CMCRPT = SPECIFIED CAMAC FUNCTION IN STOP MODE
CMCSTP = SPECIFIED CAMAC FUNCTION IN STOP MODE
CMCCUP = SPECIFIED CAMAC FUNCTION AT A HIERARCHICAL SEQUENCE
OF ADDRESSES WITH OPTIONAL SKIP OF SEQUENCE BASED ON G.
GENERAL FORM OF STATEMENT==
CALL CMC... (PARAMETER LIST)
EXAMPLE== CALL CMCSTP (F,R,C,N,AD,LN,DATA,ERRORA,NEX)

DESCRIPTION= = FOR SINGLE ACTIONS. MUCH SIMPLER THAN THE NIM APPROACH (REF. R. F. THOMAS) FOR THE BORER 1533A CONTROLLER WRITTEN IN RE-ENTRANT CODE.

INCORP TECHNIQUE

RS'.REF. 13. 5020 '.53 CAMAC UNCTION FOR RT11 L RYARS, R KEYSER CAMAC, CAMINT READER SERVICE CLASS CODE = TITLE= - = = AUTHOR(S)= = AUTHOR (S) = NAME/ACRONYM = VERSION = = MAINTENANCE BY= OBTAINABLE FROM AVAILABLE ON/AS OPERATIVE DATE= RTII
ORTEC
ORTEC (SEE INDEX OF MANUFACTURERS)
PAPER TAPE
1974
1974
PDP=11
DC011 (ER&G/ORTEC)
SUBROUTINES
PDP=11 ASSEMBLY
RTII/FORTRAN
CALLS TO FORTRAN LIBRARY ROUTINES
SINGLE OF MULTIPLE INSTRUCTIONS,
DEMAND HANDLING COMPUTER INTERFACE(S) SOFTWARE TYPE LANGUAGE HOST LANGUAGE INCORP TECHNIQU
CAMAC FACILITIE

RS',REF, 13, 5021 REF 12,5015 '53(FORTRAN) J M STEPHENSON, L A KLAISNER READER SERVICE READER SERVICE CLASS CODE = AUTHOR(8)= = AUTHOR(3) = NAME/ACRONYM = ORTAINABLE FROM OPERATIVE DATE = COMPUTER = INTERFACE(S) = KSCLIB
KINETIC SYSTEMS (SEE INDEX OF MFRS) 1974 PDP=11, 16K CORE MEMORY REQUIRED TYPES 3911A, 3991 & 3992 (KINETIC)

TYPES 3911A, 3991 & 3992 (KINETIC FORTRAN LIBRARY OF FORTRAN FUNCTIONS AND SUBROUTINES LANGIJAGE = SOFTWARE TYPE =

CORRECTED, REVISION A
RS.REF. 13. 5022
'53
I/O MACROS FOR CAMAC
D STUCKENBROCK, G KLENERT,
SIFMENS AG, KARLSRUHE
MACAM
SIEMENS (SEE TUREY OF MERCA CORR\*\*\*\*\*\*\*\*\*
PEADER SERVICE
CLASS CODE =
TITLE= = =
AUTHOR(S) = = SIFMENS AG, KARLSRUHE
MACAM
SIFMENS (SEE INDEX OF MFRS)
PAPER TAPE, CARDS & SOURCE DECK
NOVEMBER 1974
PR 320/330
CC 320 & SC 330 (SIEMENS)
"5K = 1K OF 16 BITS (SUPERVISOR EXCL)
DEPENDING ON HARDWARE
TITY AND SUPERVISOR PROGRAM
I/O ROUTINES, LAM HANDLING
CAMAC SOFTMARE IS ASSEMBLER 300
MACROS = ASSEMBLER, CALLS = FORTRAN
CONCURRENT MULTI-USER OPERATION, SYSTEM
RUNS UNDER REAL-TIME SUPERVISOR NAME/ACRONYM =
OBTAINABLE FROM
AVAILABLE ON/AS
OPERATIVE DATE= COMPUTER = INTERFACE(S) = MIN MEMORY SPACE

MIN SYSTEM CONFIG SOFTWARE TYPE = ENVIRONMENT FOR = LANGUAGE = FACILITIES = 

NEW ENTRY
RS'REF'. 13. 5023
'.53 (BASIC)
BASIC = SUBROUTINES
D STUCKENBROCK, SIEMFNS AG, KARLSRUHE BASIC - CALLS SIEMENS (SEE INDEX OF MANUFACTURERS) PAPER TAPE, CARDS PAPER IAPL,
1973
PR 320
1K OF 16 BITS (BASIC COMPILER EXCLUDED)
CC 320
SUBROUTINES
TTY AND BASIC COMPILER
FMREDDED BASIC CALLS TO SUBROUTINES
LAM HANDLING

NEW ENTRY RS.REF. 13. 5024 RFADER SERVICE CLASS CODE = TITLE = = = AUTHOR(S) = = PUBL / REF. =

NEW ENTRY
RS.REF. 13. 5024
:53
TMM-LEVEL CAMAC PERIPHERAL HANDLER
L M TAFF, UNIV OF GRONINGEN, NETHERLANDS
COMPUTER PHYSICS COMMUNICATIONS
(TO BE PUBLISHED)
AUTHOR
AUTHOR
DECTAPE (ASCII CODE)
1974
DEC PDP=11, MIN 8K OF MEMORY
CA=15 (DEC)
(3NFTWARE) = DEC MONITOR SYSTEM (ADSS)
CAMAC DRIVER/LAM HANDLER SUBROUTINE,
I/O DEVICE HANDLERS, CMCBSC SUBROUTINE
ASSEMBLER
ANY SUPPORTED BY SYSTEM
LINKED AT LOAD TIME
SINGLE CAMAC OPERATIONS, DATA CHANNEL
TRANSFERS, DEMAND HANDLING, RE-ENTRANT MAINTENANCE BY
OBTAINABLE FROM=
AVAILABLE ON/AS=
OPERATIVE DATE =
COMPUTER = =
INTERFACE(S) =
OPERATING SYSTEM
SOFTWARE TYPE=

LANGUAGE = = HOST LANGUAGE= INCORP TECHNIQUE CAMAC FACILITIES

NEW ENTRY
RS.REF. 13. 5025
.53
CAMAC/FORTRAN V INTERFACE SUFTWARE
A GSPONNER, SEN ELECTRONIQUE
SEN
DISK (RDOS). FULL RDOS COMPATIBILITY
MAY 1975 NEW\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = =
AUTHOR(S)= = MAINTENANCE BY
AVAILABLE ON/AS=
OPERATIVE DATE =
COMPLITER = = MAY 1975
ANY NOVA (MITHWITHOUT FLOATING POINT)
CC 2023 (SFN)
POST PROCESSOR COMPUTER - INTERFACE(S) SOFTWARE TYPE-

DESCRIPTION = THIS SOFTWARE PACKAGE CONSISTS OF A NUMBER OF SUBROUTINES FOR FORTRAN/RT11 CALLING CAMAC FUNCTIONS.
THE CAMAC CALL STATEMENT HAS THE FOLLOWING FORM == CALL CAMAC (IF, IN, IA, IG, IDATA)
THEY ARE USED TO TRANSFER DATA TO/FROM CAMAC AND FOR TEST THEY ARE USED TO TRANSPER DATA TOFFICE CAPAC TO THE PURPOSES.

IF, IN, IA ARE RESPECTIVELY FUNCTION, STATION ADDRESS AND SUBADDRESS, IG IS BOTH QBIT AND XBIT.

CAMINT IS USED TO HANDLE INTERRUPTS FROM CAMAC CRAFF, AND HAS THE GENERAL FORM——

CAMINT(IN, NAME1)

WHERE IN IS THE STATION NUMBER AND NAME1 JS THE NAME OF THE SUBROUTINE TO BE EXECUTED WHEN THE INTERRUPT OCCURS.

DESCRIPTION = THIS SOFTWARE PACKAGE IMPLEMENTS THE CMCBSC SERIES OF STANDARD FORTRAN CALLS DESCRIBED IN CAMAC BULLETIN NO 6, 1973.
IT ALSO INCLUDES THE BIT MANIPULATION FUNCTIONS EXCLUSIVE
OR, INCLUSIVE OR, AND, NOT, 8 SHIFT. THE PACKAGE SUPPORTS
UP TO 8 CRATES INTERFACED THROUGH MODEL 3911A UNIBUS \*)
CRATE CONTROLLERS, UP TO 7 CRATES PER 3991 BRANCH DRIVER AND
UP TO 61 CRATES PER 3992 SERIAL BRANCH DRIVER. THE NUMBER
OF PARALLEL AND SERIAL BRANCHES SHOULD RE LESS THAN 8.

\*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP.

DESCRIPTION = A SET OF I/O MACRO SUBROUTINES CAN BE CALLED BY ANY USER PROGRAM CONCURRENTLY RUNNING ON THE COMPUTER, PROVIDED THEY OPERATE UNDER A REAL-TIME SUPERVISOR PROGRAM, THE ROUTINES COMPRISE THE FUNCTIONS READ, WRITE, AND EXECUTION OF CONTROL COMMANDS. BLOCK TRANSFERS ARE PERFORMED ON CONSTANT OR VARIABLE CAMAC ADDRESS, AND IN INCREMENT MODE OR RANDOM-LIST MODE. THE CORDINATION OF USER PROGRAMS AND CAMAC PROVIDED BY THE SUPERVISOR, FACILITATES GREATLY THE LAM HANDLING. THE SYSTEM ALLOWS UP TO 8 BRANCHES, EACH WITH 7 CRATES. SYSTEM SOFTWARE ENVIRONMENTS FACILITATE INCORPORATION OF THE SUBROUTINE CALLS AS STATEMENTS EMBEDDED IN FORTRAN PROGRAMS.

DESCRIPTION= =
THE SUBBOUTINES IN ASSEMBLER ARE MANDLED BY THE BASIC=ON=320
COMPILER (INTERPRETER?).
THE STATEMENT = COMPILER (INTERPRETER?).
THE STATEMENT = CALL (CM, PARAMETER LIST)
CAUSES PROGRAM TO JUMP TO SUBROUTINE CALLED.
THE FOLLOWING CAMAC OPERATIONS CAN RE EXECUTED = = SINGLE OPERATION (READ, WRITE, CONTROL)
= INTERRUPT REGISTRATION AND JUMP TO LAM HANDLING ROUTINE
= NAITING FOR LAM
'PARAMETER LIST' IS A STRING OF CHARACTERS SPECIFYING THE
OPERATION TO BE EXECUTED.
EXAMPLE = CALL(CM,NAF,11,0,0,X1)
= WHERE 11,0,0, = STATION,SUBADDRESS,FUNCTION, X1 = VARIABLE

DESCRIPTION = 
THE CAMAC DRIVER/LAM HANDLER IS A GLORALLY LINKED SUBPOUTINE FOR EXECUTING SINGLE CAMAC OPERATIONS, CONTROLLING ACCESS TO 2 HARDWARE DATA CHANNELS VIA QUEUFS, AND GIVING CONTROL TO THE PROPER HISFR ROUTINE WHEN A LAM OCCURS. IT MAY BE CALLED BY ASSEMBLER CODED USER PROGRAMS, THOMAS! STANDARD SUBPOUTINE CMCBSC (HENCE ALL OTHER OF HIS ROUTINES WHICH CALL CMCBSC) = SEE .53 ABOVE = AND I/O HANDLERS FOR CAMAC INTERFACED PERIPHERALS, FITHER FROM MAYNSTREAM OR LAM HARDWARE PRIORITY. CAMAC INTERFACED DEVICES FOR WHICH HANDLERS CURRENTLY EXIST INCLUDE A LINE PRINTER, CARD READER, TNCREMENTAL PLOTTER, AND A TEXTRONIX 4010 TERMINAL. FOR DEVICE HANDLERS, CAMAC IS TRANSPARENT.
IT IS RELATIVELY FASY TO ADAPT A HANDLER FOR AN I/O BUS DEVICE TO CAMAC SIMPLY BY SUBSTITUTING SUBROUTINE CALLS TO THE DRIVER FOR I/O OPERATIONS AND OBSERVING A FEW NON-RESTRICTIVE CONVENETIONS. THIS TWO-LEVEL APPROVACH CAN ACCOMPOSE CAMAC LANGUAGES IF ACTION STATEMENTS ARE COMPILED INTO SUBROUTINE CALLS.

DESCRIPTION - -

## .54 Support Software I (translators)

READER SERVICE
CLASS CODE =
TITLE = - AUTHOR(S) =
MAINTENANCE BYOBTAINABLE FROM
OPERATIVE DATESOFTMARE TYPE =
LANGUAGE =
COMPUTER =

RS'REF. 13. 5026
'.54
S/UNIP AN UNIVERSAL MACRO PROCESSOR
SOFTWARE-PARTHERS
SOFTWARE-PARTHERS
SAME, (SEE INDEX OF MANUFACTURERS)
APRIL 1974
MACRO PROCESSOR
WRITTEN IN HIGH LEVEL LANGUAGE
CAN RUN ON 19M, UNIVAC, CDC, ICL,
SIEMENS, ETC.
INCORPORATED IN-LINE FOR FULL-SET
IMI WITH MACRO PROCESSOR DIRECTIVES

CAMAC FACILITIES

CORR \*\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = = =

CORRECTED, REVISION A
RS.REF. 13. 5027
.541
A MACRO ASSEMBLER FOR TYPE MBD=11
MICROPROGRAMMED BRANCH DRIVER
PDP=11
BI RA SYSTEMS (SEE INDEX OF MFRS)
MACRO ASSEMBLER (TRANSLATOR)
MBD=11 (BI RA SYSTEMS)

COMPUTER = OBTAINABLE FROM SOFTWARE TYPE = INTERFACE(S) =

READER SERVICE
CLASS CODE =
TITLE = = =
AUTHOR(S) = =
NAME/ACRONYM =
MAINTENANCE BY=
OBTAINABLE FROM
AVAILABLE ON/AS
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
MIN SYSTEM CONFIG
SOFTWARE TYPE =
LANGUAGE =
CAMAC FEATURES =
ENVIRONMENT FOR =
CAMAC FACILITIES RS'.REF. 13. 5028
.541(MACRO11)
MACROS FOR 1533A
MR, HEER
MACRO 1533A
MR, HEER
MR, HEER, ZEL, KFA, JUELICH
DECTAPE
FEBRUARY 1973
PDP=11, MIN 8K 16 BIT WORDS
TYPE 1533A (BORER)
DOS V004, 008, 009
MACRO-8ET
ACRO 11

MACRO 11
ARE INCORPORATED IN-LINE
CAMAC SOFTWARE IS ASSEMBLER
SINGLE ACTION STATEMENTS,
SYMBOLIC DEVICE NAMES

CORR\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE TITLE- - -

CORRECTED, REVISION A
RS.REF. 13. 5-29
.541(IML)
MACRO-IML IMPLEMENTATIONS FOR DEC
PDP=11 COMPUTERS
M KUBITZ, R KIND, HM1-BERLIN
CAMAC BULLETIN NO 12, APRIL 1975
M KUBITZ, REREICH D/E, HMI-BERLIN
GERMANY
ALL MEDIA

AUTHOR(S) = -PUBL. REF. = OBTAINABLE FROM

ALL MEDIA

AVAILABLE ON/AS
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
MIN SYSTEM CONFIG
SOFTWARE TYPE =
LANGUAGE =
CAMAC FEATURES=
CAMAC FACILITIES

1974
PDP=11, 16K, 24K, 44K, OR 52K
CA=11A (DEC), 1533A (BORER)
DOS VO8/09, RSX=11D, RSX=11M
MACRO SET OF IML (IMPLEMENTED)
PDP=11 ASSEMBLY
INCORPORATED BY MACROS
FULL SET OF IML=MACROS
INCLUDING DEMAND HANDLING

CORR\*\*\*\*\*\*\*\*

READER SERVICE

CLASS CODE =

TITLE= = = =

AUTHOR(\$) = =

NAME/ACRONYM =

OBTAINABLE FROM

CORRECTED, REVISION A
RS'.RFF. 13. 5030
'.543(CATY)
A CAMAC TESTING AID FOR USE ON PDP=11
F R GOLDING, APPLIED COMPUTER SYST.
CAT11
APPLIED COMPUTER SYSTEMS LTD,
WENZEL ELEKTRONIK, NUCL ENTERPRISES,
(SFE INDEX OF MANUFACTURERS)
1973
PDP=11, 4K OR 8K MEMORY REQUIRED
DEPENDING ON VERSION

OPERATIVE DATE-

PDP=11, 4K OH 6K MEMNEY MEGUIRED DEPENDING ON VERSION C=csC=11 (MENZEL), 9030 (N.E.) CONTROL VISTA, READER, PUNCH SYRTFM (EXECUTIVE, COMPILER ETC) CATY (BASED ON BASIC) INTERFACE(S) =
MIN SYSTEM CONFIG
SOFTWARE TYPE =
LANGIJAGE =

NEW ENTRY
RS'REF. 13. 5031
'543(CATY)
A CAMAC TESTING AID = CATY = FOR PDP=11
F R GOLDING, R F CRANFIELD
GEC ELLIOTT (SEE INDEX OF MANUFACTURERS)
1974
PDP=11, MIN 4K REQUIRED TITLE - - AUTHOR(S) - OBTAINABLE FROMOPERATIVE DATE COMPUTER - MIN MEMORY SPACE
INTERFACE(S) MIN SYSTEM CONFIG
LANGUAGE - -

PTI-11C/D, IVG-11 (GEC ELLIOTT) CONTROL TTY OR VISTA, READER, PUNCH CATY (BASED ON BASIC)

DESCRIPTION= =

3/UNIP TS A LANGUAGE INDEPENDENT MACRO PROCESSOR AND
THEREFORE A TOOL FOR MACRO EXPANSION OF EVERY EXISTING OR
OR FUTURE PROGRAMMING LANGUAGE. THUS S/UNIP MAINTAINS AND
PROCESSES MACROS IN HIGH LEVEL LANGUAGES (FORTRAN, BASIC,
ALGOL, PEARL, ETC.) AS WELL AS ASSEMBLY LANGUAGES. 3/UNIP
OPERATES AS A PRE-PROCESSOR GENERATING SOURCE CODE
STATEMENTS FOR SUBSEQUENT COMPILATION, POSSIBLY ON ANOTHER
COMPUTER.

DESCRIPTION = THE MACRO ASSEMBLER HAS BEEN DEVELOPED TO FACILITATE THE WRITING OF PROGRAMS FOR THE MRD-11 MICROPROCESSOR-INTERFACE. THE ASSEMBLER TRANSLATES PROGRAMS WRITTEN IN MACRO CODE INTO INSTRUCTIONS ACCEPTABLE BY THE MBD-11. UP TO 4K INSTRUCTIONS CAN BE STORED IN THE MRD-11, A FUNCTION OF MEMORY SIZE WHICH GO FROM 256 TO 4K WORDS IN INCREMENTS OF 256 AND 1K. INSTRUCTIONS ARE MICRO-STRUCTURED FORMING A POWERFUL SET,

DESCRIPTION = = THIS IS A SIMPLE MACRO SET (NO DECLARATIONS) FOR SINGLE ACTION STATEMENTS. EXECUTION SPEED IS HIGHER (APPROX 30 MICROSERS PER INSTRUCTION, DEPENDING ON TYPE OF INSTRUCTION ON TYPE OF PDP=11). NOT INTERRUPTABLE MACROS (PRIORITY=7)

DESCRIPTIONS =

IML IS THE LEWISTED ON PDP=11 IN ACCORDANCE WITH THE MACRO
SYNTAX AS DEFINED IN THE DOCUMENT ESONE/IML/01 (SEE CLASS
"501 ABOVE). VERSIONS ARE AVAILABLE FOR INTERFACE»
CONTROLLERS AND DEC OPERATING SYSTEMS AS MENTIONED IN THE
LEFT COLUMN.
IMPLEMENTATION COVERS THE FILL SET OF IML MACROS AND DEMAND
HANDLING EXCEPT BLOCK TRANSFER ON SPECIAL LAM, X=ERROR
CONTROL STATEMENTS, AND SUBSCRIPT MODE. TRANSFER HODES NOT
IMPLEMENTED BY HARDWARE ARE SIMILATED BY SOFTWARE.
I/O TRANSFER INSTRUCTIONS ARE EMBEDDED IN THE MACROS AND ARE
PERFORMED DIRECTLY IN ACTION BY THE MACROS.
ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMIZED
ADDRESS CALCULATION AT ASSEMBLY TIME GIVES OPTIMIM RUN TIME
CODE. HOST LANGUAGES CAN BE PDP=11 MACRO ASSEMBLE OR
FORTRAN (VIA SUBROUTINE CALL).
MEMORY REQUIREMENTS VARY WITH OPERATING SYSTEM AND IF FULL
SET IS NEFDED, OR A SUB-SET IS ACCEPTABLE. 16K IS REGUIRED
FOR A SUB-SET WITH DOSVOS/09 OR RSX=11M AND 52K FOR FULL SET
AND RSX=11D.

DESCRIPTION - USERS TEST PROGRAMS ARE TYPED IN AND THERFAFTER COMPILED AND
RUN. IT IS POSSIBLE TO EDIT THE PROGRAM AND RERUN IT WITHOUT HAVING TO RETYPE THE ORIGINAL PROGRAM. CAMAC COMMANDS
ARE EMBEDDED IN PROGRAM AS STATEMENT LINES.
CAT11 HAS INTERRUPT AS SYSTEM FEATURE, THE USER MAY TYPE HTS
OWN INTERRUPT ROUTINE.
THE CAT11 EXECUTIVE PROGRAM CHANGES SLIGHTLY WITH INTERFACE
USED, BUT ALL ROUTINES ARE IDENTICAL.
VERSIONS OF THIS SYSTEM IS ALSO AVAILABLE FROM GEC ELLIOTT
(SEE FOLLOWING ENTRIES)

DESCRIPTION - -SFE PRECEDING ENTRY

NEW\*\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = = =
AUTHOR(\$) = =
OBTAINABLE FROM=
OPERATIVE DATE =
COMPUTER = =
INTERFACE(\$) =
MIN SYSTEM CONFIG
LANGUAGE = =

NEW ENTRY

PS'REF, 13, 5032

.543(CATY)

A CAMAC TESTING AID = CATY = FOR NOVA

F R GOLDING, R F CRANFIELD

GEC ELLIOTT

MARCH 1975,

NOVA SERIES (DATA GENERAL), MIN 4K

NOVA EXECUTIVE SUITE (GEC ELLIOTT)

CONTROL TTY OR VDU, READER, PUNCH

CATY (BASED ON BASIC)

NEW\*\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = = =
OBTAINABLE FROM=
COMPUTER = =
INTERFACE(S) =
LANGUAGE = =

NEW ENTRY
RS'.REF. 13. 5033
.543/CATY)
A CAMAC TESTING AID = CATY = FOR THE
GEC ELLIOTT
2050 AND 4080 (GEC)
EXFCUTIVE SUITE FOR 2050/4080 (GEC)
CATY (BASED ON BASIC)

RS'REF. 13. 5034
.543
A BASIC MACRO=11 COMPILER
B RECKS
CAMAC BULLETIN NO 10, JULY 1974
MABA
B RECKS, ZEL, KFA, JUELICH
DECTAPE
JANUARY 1974
PDP=11, 16K 16 BIT WORDS OF MEMORY
TYPE 1533A (BORER)
DOS YOS OR YOS, 16K
COMPILER
BASIC
IN-LINE
CAMAC SOFTWARE IS MACRO ASSEMBLER READER SERVICE
CLASS CODE =
TITLE= = =
AUTHOR (8) =
PUBL. REF. =
NAME/ACKONYM =
MAINTENANCE 8Y=
OBŢAINABLE FROM
AVAILABLE ONVAS
DPERATIVE DATE=
COMPUTER =
INTERFACE(S) =

COMPUTER =
INTERFACE(S) =
MIN SYSTEM CONFIG
SOFTWARE TYPE =
LANGUAGE =
INCORP TECHNIQUE
ENVIRONMENT FOR =
CAMAC FACILITIES

CAMAC SOFTWARE IS MACRO ASSEMBLER SINGLE ACTION STATEMENTS

READER SERVICE CLASS CODE = TITLE = = = AUTHOR(S) = = PUBL, REF. =

AVAILABLE ON/AS
OPERATIVE DATECOMPUTERS:
INTERFACE(S) MIN MEMORY SPACE
SOFTWARE TYPE LANGUAGES-

INCORP TECHNIQUE HOST LANGUAGE = FACILITIES =

RS'REF. 13. 5035
.543
PRECOMPILER FOR IML SUBSET
W. KNEIS
CAMAC BULLETIN NO 10, JUNE 1974, AND GFK
REPORT KFK2121, GFK, 1975 (IN PRESS)
META=II/X
W. KNEIS, IAK II/CYCLOTRON,GFK,
D 7500 KARLSRHE, POSTFACH 3640
TAPE, CARDS
JULY 1974
IBM/370 (TRANSL.), CDC 3100 (EXECUTION)
IN-HOUSE TYPE
36K BYTES (MAX 86K BYTES)
PRECOMPILER (METACOMPILER SYSTEM)
IML (USER), FORTRAN IV (SYSTEM),
META=II (FOR COMPILER/MRITING)
TN-LINE
COMPASS ASSEMBLER (CDC 3100)
SINGLE ACTIONS, MULTIPLE ACTION(MA)
BLOCKTRANSFERUBL), AND LAM-,
CRATE-, AND SYSTEM-STATEMENTS

READER SERVICE CLASS CODE -TITLE - - -

RS'REF. 13. 5036 .544(BASIC) A PDP-11 BASIC EXTENSION FOR CAMAC PROGRAMMING AUTHOR(S) = PUBL REF. = OPERATIVE DATE = COMPLITER = INTERFACE(S) = SOFTWARE TYPE = INCORP TECHNIQUE ENVIRONMENT FOR ANGUSE = ANGUSE = OPERATION = OPE T RALS, E DE AGOSTINO, CNEN, ROME CAMAC BULLETIN NO 7, JULY 1973 CAMAC BULLETIN NU /, JULY 1973 1973 PDP=11 EXECUTIVE SUITE (GEC ELLIOTT) INTERPRETER SURROUTINES IN ASSEMBLY CODE CAMAC SOFTWARE IS BASIC BASIC (EXTENDED)

LANGUAGE

CORR\*\*\*\*\*\*\*

READER SERVICE

CLASS CODE =

TITLE= = = =

AUTHOR(S) = =

PUBL. REF. =

NAME/ACRONYM =

OBTAINABLE FROM

OPERATIVE DATE=

COMPUTER =

INTERFACE(S) =

MIN SYSTEM CONFIG

SOFTWARE TYPE = CORRECTED, REVISION B
RS.REF. 13. 5037
.544(BASIC)
A CAMAC EXTENDED BASIC LANGUAGE
J M SERVENT (SCHLUMBERGER)
PROC CAMAC SYMPOS, LUXMBG, DEC 1973
CASIC
SCHLUMBERGER (SEE INDEX OF MFRS)

SCHLUMBERGER (SEE INDEX OF MFRS)
1973
PDP=11, 16K WORDS MEMORY
ICP11 OR JCC11 (SCHLUMBERGER)
TTY
INTERPRETIVE LANGUAGE, EXTENDED
WITH MACRO-INSTRUCTION GENERATOR
BASIC (EXTENDED)
IN-LINE CAMAC STATEMENTS
SYMBOLIC DEVICE NAMES, INTERPUPT
HANDLING, RE-ENTRANT. LANGUAGE = INCORP TECHNIQUE CAMAC FACILITIES

DESCRIPTION = (SEE CLASS .501(CATY) AND PRECEEDING FNTRIES CLASS .543)

DESCRIPTION = (SEE CLASS .501(CATY) AND PRECEEDING FNTRIES CLASS .543)

DESCRIPTION = THIS COMPILER TRANSLATES TESTED (INTERPRETIVE) BASIC PROGRAMS INTO MACRO=11 SOURCE CODE, RUN TIME IS IMPROVED BY A FACTOR OF 15 TO 20. EASILY ADAPTABLE TO OTHER CONTROLLERS (MACROS).

OUTPUT CODE LINKED WITH FLOATING POINT PACKAGE CAN RUN ON STAND-ALONE MINI=COMPUTERS.

DESCRIPTION = 
META=II/X IS A SYSTEM FOR WRITING COMPILERS. THE IMPLEMENTED VERSION OF THE IML PRECOMPILER IS A CROSS=COMPILER VERSION, I.E. TRANSLATION IS DONE ON AN IBM/370, EXECUTION ON A COC 3100 COMPUTER. THE OBJECT CODE FOR PRECOMPILING IS THE MNEMONIC COMPASS ASSEMBLER (CDC), THEREFORE AN ADDITIONAL ASSEMBLER STEP IS INVOLVED, MITH META=II/X A PRECOMPILER CAN BE WRITTEN AND TESTED IN A FEW DAYS. THE IML SUBSET CONTAINS THE DECLARATION— (LOCL, LOCD) AND ACTION—STATEMENTS (SA, SJO, SJNG, MA, UBL, ALL LAM HANDLING—, SYSTEM—AND CRATE—CONTROLLER—STATEMENTS).

SET CONTAINS THE DECLARATION STATEMENTS LOCA AND LOCD. THE SUBSET ALSO CONTAIN ACTION STATEMENTS SUCH AS SA, SJO, SJNG, MA, UBL, ALL LAM—HANDLING STATEMENTS, SYSTEM STATEMENTS, AND CRATE CONTROLLER STATEMENTS.

DESCRIPTION= =

THE SUBROUTINES WHICH EXTEND THE BASIC INTERPRETER TO CAMAC ARE CALLED BY AN EXTERNAL FUNCTION STATEMENT, WHERE ADDRESS, FUNCTION, ETC, ARE TRANSMITTED AS ARGUMENTS. THE STATEMENT HAS THE FOLLOWING GENERAL FORM= 
LET U = EXF (A1:A2, ..., A10)

THE FIRST ARGUMENT SELECTS THE APPROPRIATE SUBROUTINE.

DATALESS, READ, AND WRITE OPERATIONS WITH DIRECT/INDIRECT ADDRESSING ARE POSSIBLE. ALSO SINGLE OR BLOCK TRANSFERS IN ADDRESS SCAN, REPEAT OR STOP MODES CAN BE PERFORMED.

THE EXTENSION FEATURES LAM HANDLING.

DESCRIPTION= =

STANDARD BASIC IS EXTENDED WITH A SET OF CAMAC RELATED

STATEMENTS, EXECUTION TIME FOR A 100 LINE PROGRAM IS ABOUT

10 SECONDS, DECLARATIVE STATEMENTS ALLOW SYMBOLIC REFERENCE

OF A MODULE, ADDRESS PARAMFTERS CAN BE CONSTANTS

OR VARIABLES, EVEN EXPRESSIONS, THUS PROVIDING GREAT

FLEXIBILITY. SEVERAL CONTROL FUNCTIONS ARE IN MACRO-STATE
MENT FORM, SUCH AS = 1ST LAM MODULE (SAME AS MODULE(8)).

SOME SYNTAX CHANGES FACILITATES IMPLEMENTATION OF THE SEMAN
TICS OF IML (SEE .501(IML)). TYPICAL STATEMENTS ARE = 

ASSIGN ADDRESS = STATION (MODULE) = (B,C,N,A)

EXECUTING STATEMENT = 

SINGLE TRANSFER = SA(F,MODULE,A)

MULTIPLE TRANSFER = MA(F,MODULE,A)

CONTROL FUNCTION = EXEC MODULE(F)

LAM MEG OPERATION= CLR LAM MODULE (HODULE(10))

LAM/INTERRUPT = ON LAM(MODULE) DO 100

READER SERVICE CLASS CODE -TITLE - - -

AUTHOR(S) = VERSION = MAINTENANCE BY=
ORTAINABLE FROM
AVAILABLE UN/AS
OPERATIVE DATECOMPUTER = COMPUTER INTERFACE(S) MIN SYSTEM CONFIG
SOFTWARE TYPE LANGUAGE INCORP TECHNIQUE

RS.REF, 13, 5039
"544(BASIC)
8=USER BASIC UNDER DOS WITH
INTERPRETER EXTENDED FOR CAMAC
PFEIFFER, SPICKMAN, CARLEBACH
001
D P PFEIFFER, ZAM, KFA, JUELICH
DECTAPE
JANUARY 1974
PDP=11, 16K OF 16 BIT WORD MEMORY
TYPE 1533A (BORER)
DOS VO8 OR VO9, 16K
DOS SYSTEM INTERFACE TO CAMAC
BASIC
EXTENSION OF INTERPRETER

READER SERVICE CLASS CODE = TITLE = = =

AUTHOR(S) = = NAMEJACRONYM = MAINTENANCE BY= OBTAINABLE FROM AVAILABLE ON/AS OPERATIVE DATE= COMPLITER = INTERFACE(S) = MIN SYSTEM CONFIG SOFTWARE TYPE = LANGUAGE = INCORP TECHNIQUE CAMAC FACILITIES

RS'REF. 13. 5040
'544

DRACL (TM), AN INTERPRETIVE REALTIME MONITOR WITH CAMAC SUPPORT
L HYARS, R KEYSER (ORTEC INC)
ORTEC
ORTEC (SEE INDEX OF MANUFACTURERS)
PAPER TAPE AND DISK
APRIL 1974
PDP=11, MIN SK 1L BIT MEMORY
TYPE DC011 (EGGG)
TIY & DC011
INTERPRETER, SYSTEM MONITOR
PDP=11 ASSEMBLER
EMBEDDED CAMAC FEATURES
SINGLE OR MULTIPLE INSTRUCTIONS,
DEMAND HANDLING IS INCLUDED. RS'.REF. 13. 5040

NEW\*\*\*\*\*\*\*\*\*\*\*
READER SERVICE
CLASS CODE =
TITLE= = =
AUTHOR(S) = =
MAINTENANCE BY
ORTAINABLE FROMOPERATIVE DATE =
AVAILABLE ON/AS=
COMPUTER = INTERFACE(S) =
SOFTWARE TYPE= NEW ENTRY
RS.REF. 13. 5041
.544
GENERAL PURPOSE I/O INTERFACE SOFTWARE
F WORM, SEN ELECTRONIQUE
SEN
SEN (SEE INDFX OF MANUFACTURERS)
MAY 1975
DISK
NOVA SERIES (DATA GENERAL)
ANY (IRRESPECTIVE OF MAKE)
INTERPRETER
FULLY RODS/SOS COMPATIBLE SOFTWARE TYPE-

DESCRIPTION = 
THE INTERPRETER IS PRIMARILY INTENDED FOR EASILY PROGRAMMED ON-LINE CAMAC SYSTEMS IN NON-TIME-CRITICAL CONTROL AND DATA HANDLING APPLICATIONS AND FOR TEST ROUTINES.
THERE ARE 9 CAMAC STATEMENT TYPES COVERING GENERAL CONTROLS (Z, C, I) AND CAMAC COMMANDS MITH/MITHOUT DATA TRANSFER.
THE GENERAL FORM OF A CAMAC STATEMENT IS ==

+A CF,C,N,A,F,FB,HW [,W,O]
WHERE SPVERAL PARAMETERS MAY BE DMITTED.

DESCRIPTION - THE 8-USER BASIC CAN BE RUN UNDER DOS, A HELP FILE CONTAINS
ALL MODIFICATIONS OF THE 1 TO 8 USER RASIC, NO INTERRUPT
ANDLING, COMMUNICATION BETWEEN THE A USERS IS POSSIBLE BY
ONE COMMUNICATION WORD PER USER, EXPANDED ERROR MESSAGE
HANDLING, FILE HANDLING EXTENDED, TIME COMMAND ADDED.

DESCRIPTION - ORACL INTERPRETS ARITHMETIC STATEMENTS, PROGRAM CONTROL STATEMENTS, COMMENTS, I/O STATEMENTS, AND HARDWARE CONTROL STATEMENTS AND EXECUTES THE DESIRED FUNCTION.

ORACL (TM) IS A TRADE MARK REGISTERED BY ORTEC, INC.

DESCRIPTION -

# . 55 Support Software II

READER SERVICE
CLASS CODE =
TITLE = = =
AUTHOR(S) = PUBL. REF. =
NAME/ACRONYM =
OPERATIVE DATE=
COMPUTER =
SOFTWARE TYPE =

RS'.REF. 13. 5042 .553(FOCAL/PAL) A FOCAL INTERRUPT HANDLE FOR CAMAC F MAY, W MARSCHIK, H HALLING CAMAC BULLETIN ND 6, MARCH 1973 FOCALINT 1971 PDP=8 INTERRUPT HANDLEP (SYSTEM PROGRAM)

DESCRIPTION = =
FOCALINT IS A GENERAL PURPOSE SYSTEM PROGRAM, ADAPTABLE FOR
SPECIAL USE. UP TO 3 CRATES WITH 24 INTERRUPTS EACH CAN BE
SERVICED. ONE PROGRAM LINE IN FOCAL IS RESERVED FOR EACH
INTERRUPT. SHORT ROUTINES CAN BE TYPED INTO THESE LINES
SERVICING THE ASSOCIATED INTERRUPTS, ALTERNATIVELY A FOCAL
SUBROUTINE CAN BE USED. CURRENT LINE IN THE BACKGROUND
PROGRAM WILL BE FINISHED REFORE JUMPING TO INTERRUPT ROUTINE
AND RETURNS TO NEXT LINE IN THE BACKGROUND PROGRAM AFTER
SERVICING.

### .57 Test Routines

READER SERVICE CLASS CODE -TITLE - - -

OBTAINABLE FROM OTHER REMARKS RS'REF. 13. 5043
'57
TEST PROGRAMS FOR SYSTEMS, BRANCH
DRIVER & MODULES
BI RA SYSTEMS (SEE INDEX OF MFRS)
FOR BRANCH DRIVER MBD=11, SYSTEM TEST
MODULE 6102, AND DATA MODULES

READER SERVICE
CLASS CODE =
TITLE = - AUTHOR(S) = AVAILABLE ON/AS
OPERATIVE DATE =
COMPUTER =
INTERFACE(S) =
SOFTWARE TYPE =

RS'REF. 13. 5044
.573
CAMAC TEST PROGRAM
DR' B MERTENS, IKP, KFA, JUELICH
PAPER TAPE, ASCII CODE
1971
PDP=11, 16K OF 16 BIT WORDS MEMORY
TYPE 2200 (BORER)
TEST ROUTINES, STAND-ALONE PROGRAMS

READER SERVICE
CLASS CODE =
TITLE= = AUTHOR(S) = OBTAINABLE FROM
OPERATIVE DATE=
COMPUTER =
INTERFACE(S) =
SOFTWARE TYPE =

RS'REF. 13. 5045
'.373
3911A TEST CAMAC
L A KLAISNER
KINETIC SYSTEMS (SEE INDEX OF MFRS)
1973
PDP-11, 4K OF CORE MEMORY REQUIRED
TYPE 3911A (KINETIC)
TEST ROUTINE

READER SERVICE
CLASS CODE =
TITLE= = = =
OBTAINABLE FROM
OPERATIVE DATE=
INTERFACE(S) =
COMPUTER =
SOFTWARE TYPE =

R8'REF. 13. 5046 .573 TEST CAMAC KINETIC SYSTEMS (SEE INDEX OF MFRS) 1972 TYPE KS0011 (KINETIC) PDP=11, 4K OF CORE REGUIRED TEST ROUTINE

READER SERVICE
CLASS CODE =
TITLE= = - OBTAINABLE FROM
OPERATIVE DATE=
COMPLITER INTERFACE(S) =
SOFTWARE TYPE =
LANGUAGE =

RS'REF. 13. 5047
.573
PDP=11 INTERFACE TEST PROGRAM
GEC=ELLIOTT (SEE INDEX OF MFRS)
1974
PDP=11
PDP=11 EXECUTIVE SUITE/GEC=ELLIOTT
TEST ROUTINE
PAI =11 ASSEMBLER

OBTAINABLE FROMCOMPUTER - INTERFACE(S) SOFTWARE TYPEMIN SYSTEM CONFIG

NEW ENTRY
RS,REF. 13. 5048
'573
TEST PROGRAMS FOR BRANCH DRIVER AND
SYSTEM WITH MODULE 6102 AND TYPE A
BI RA SYSTEMS (SEE INDEX OF MFRS)
PRIME COMPUTER
1260 (BI RA SYSTEMS)
DIAGNOSTIC PROGRAMS
BRANCH DRIVER 1260, 6102 CAMAC TEST
MODULE/DATAHAY DISPLAY

DESCRIPTION - A SET OF THREE DIAGNOSTIC PROGRAMS ARE SUPPLIED WITH THE
MBD=11 MICROPROGRAMMED BRANCH DRIVER, TESTS OF MEMORY, FILE
REGISTERS, INSTRUCTION SET, DMA TRANSFERS, INTERRUPTS ETC.
A COMPLETF SYSTEM TEST IS SUPPLIED WITH 6102.
A CAMAC TEST ROUTINE IS SUPPLIED FOR CAMAC MODULE TESTING
FROM THE TELETYPE. NO ASSEMBLY LANGUAGE KNOWLEDGE REQUIRED.

DESCRIPTION - STAND ALONE PROGRAMS TEST SOME FUNCTIONS OF THE BORER TYPE 2200 INTERFACE, THE CRATE CONTROLLER AND THO IN-HOUSE MODULES (CO1 & CO2).

ERROR MESSAGES ARE OUTPUT IF THERE ARE HARDWARE FAILURES.

DESCRIPTION= A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A
TELETYPE. TO SUPPORTS UP TO 8 CRATES HITH MODEL 3911A
UNIBUS \*) CRATE CONTROLLERS. A FUNCTION MAY BE EXECUTED
ONCE OR REPFTITIVELY.

\*) UNIBUS IS A TRADE MARK OF DIGITAL EQUIPMENT CORP.

DESCRIPTION = A STAND ALONE PROGRAM FOR EXERCISING A CAMAC SYSTEM FROM A
TELETYPE. IT SUPPORTS ONE RRANCH DRIVER WITH UP TO 7
CRATES. A FUNCTION MAY BE FXECUTED ONCE OR REPETITIVELY.

DESCRIPTION = THIS IS A STAND-ALONE PROGRAM USED IN CHECKING THE EXECUTIVE SUITE, A MODULAR PDP-11 = CAMAC INTERFACE. DIAGNOSTIC MESSAGES ARE ISSUED.

DESCRIPTION- - A SET OF DIAGNOSTIC PROGRAMS ARE SUPPLIED WITH THE MODEL 1260 PRIME COMPUTER BRANCH DRIVER. A COMPLETE SYSTEM TEST IS SUPPLIED, BUT REQUIRES MODEL 6102 TEST MODULE.

# **NEWS**

# ANNOUNCEMENTS BY CAMAC MANUFACTURERS

BORER ELECTRONICS AG is introducing an autonomous crate-controller fitted with a built-in microprocessor (Intel 8080), teletype port (V 24), real-time clock, automatic power fail restart, and RAM with the possibility of up to 64K bytes. Interfaces to various peripherals such as floppy disks, modems etc, are in preparation and provision is made for use of the controller in conjunction with the standard serial highway.

A large amount of software support will be imme-

diately available thanks to collaboration with the KFA, Jülich, F.R. Germany. Amongst the many packages available are a cross-assembler and a simulator which can be run on a PDP-11.

Production is scheduled to start autumn 1975 and a live demonstration of a system will be given at the CAMAC Symposium in Brussels from October 14–16th, 1975.

Ref. No. 13.0002

# CAMAC AT THE 1st CONFERENCE OF IRAQI ATOMIC ENERGY COMMISSION

The 1st Conference of Iraqi AEC took place in Baghdad on April 7-11, 1975. In addition to the general topics of the Conference (radioisotopes, radiology, food preservation, radiochemistry, biology, medicine, theoretical physics and energy from reactors) CAMAC was presented by the chairman of the ESONE Committee, F. Iselin, CERN, in a

paper entitled, CAMAC Interfacing at CERN and future trends. At the moment CAMAC is used in Iraq at the Nuclear Research Institute near Baghdad which is working with a 2MW research reactor. An exhibition took place at the time of the Symposium informing also about existing facilities in CAMAC.

## READER SERVICE ENQUIRY CARD

In issue 12, a Reader Service Enquiry Card was introduced, and this is intended to be a standard feature of the CAMAC Bulletin. You will find that reference numbers are attached to the products mentioned in both the 'New Products' section, in the 'Product Guide' and for News of manufacturers. Six digits of which the first two are referring to the

issue number are used in the reference number. This number reflects the techniques used in the editorial work.

The Reader Service Enquiry Cards are received by the ESONE Secretariat which passes them to the relevant manufacturers.

# SECOND INTERNATIONAL SYMPOSIUM ON CAMAC IN COMPUTER APPLICATIONS

The second CAMAC symposium will take place in Brussels on October 14th to 16th, 1975. The symposium is jointly organized by the ESONE Committee and the European CAMAC Association, and sponsored by the Commission of the European Communities.

The main topics of the symposium will be the application of CAMAC in Industrial Process Control, Laboratory Automation, Medicine and Health Services, Data and Computer Communications, Public Utilities, and Environmental Control. There will be survey talks in plenary sessions, and users of CAMAC will give applications papers in parallel sessions. In all, 59 papers will be presented orally and 21 additional papers will be mentioned shortly.

An exhibition of CAMAC equipment, including complete systems, and related products from more than 30 companies and institutes is being arranged

to take place simultaneously with the symposium.

An invitation for the symposium and a preliminary programme were distributed already in May,

1975.

The latest data of registration is September 1st, while organized hotel reservation must take place before August 15th.

Further information and copies of invitation and programme are available on request from the secretary of the symposium:

H. Meyer Commission of the European Communities CRC, CBNM Steenweg naar Retie B-2440 GEEL Belgium.

# CAMAC BIBLIOGRAPHY

# Specifications and Supplementary Information\*

CAMAC: A Modular Instrumentation System for Data Handling. Description and Specification. EUR 4100c, CEC, Luxembourg 1972, 64 p., and AEC Report TID-25875, U.S.AEC, Washington DC, U.S.A., supercedes EUR 4100e (1969).

CAMAC: Organisation of Multi-Crate Systems. Specification of the Branch Highway and CAMAC Crate Controller Type A. EUR 4600e, CEC, Luxembourg 1972, 46 p. and AEC Report TID-25876, U.S.AEC, Washington DC, U.S.A. CAMAC: Specification of Amplitude Analogue Signals within a  $50\Omega$  System, EUR 5100e, CEC, Luxembourg 1974, 13 p.

CAMAC: Supplementary Information on CAMAC Instrumentation System. AEC Report TID-25877, U.S.AEC, Washington DC, U.S.A., and Supplement to *CAMAC Bulletin* No. 6, CEC, Luxembourg, March 1973, 16 p.

CAMAC: Serial System Organization, a Description. ESONE/SH/01, ESONE Secretariat and TID-26488, U.S.AEC, Washington DC, U.S.A., December 1973, 83 p. Addenda and Errata to: CAMAC Serial System Organization, a Description (ESONE/SH/01 and TID-26488). ESONE/SH/03, ESONE Secretariat, Nov. 1974, 11 p.

CAMAC: Proposal for a CAMAC Language. ESONE Committee Software Working Group. Supplement to *CAMAC Bulletin* No. 5, CEC, Luxembourg, Nov. 1972, 42 p.

BARNES, R.C.M. A CAMAC Glossary. Supplement to *CAMAC Bulletin* No. 7, CEC, Luxembourg, July 1973, 18 p. CAMAC, Bibliography. Supplement to *CAMAC Bulletin* No. 8, CEC, Luxembourg, Nov. 1973, 16 p.

CAMAC: The Definition of IML, a Language for Use in CAMAC Systems, ESONE/IML/01, ESONE Secretariat, Oct. 1974, 36 p.

### **Recommended Introductory Reading**

Proceedings of the 1st International Symposium on CAMAC in Real-Time Computer Applications, Luxembourg, Dec. 1973. (\*)

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# WAS IST CAMAC?

CAMAC ist ein international verbreitetes Instrumentierungssystem zum Anschluss von Prozessperipheriegeräten an digitale Prozessoren und Rechner für automatische Mess- und Steuereinrichtungen.

Die System-Spezifikationen umfassen:

ein digitales Interface, in dem Daten über einen standardisierten Datenweg übertragen werden;

ein modulares Gerätekonzept zur Anpassung von Peripheriegeräten und Rechnern an den Datenweg.

Mit den modularen, in Überrahmen zusammengefassten Einheiten können viele Peripheriegeräte im Multiplexverfahren über den Datenweg betrieben werden. Weitere Spezifikationen bestehen für parallele und serielle Datenübertragungswege zur Realisierung grösserer Systeme mit mehreren Überrahmen.

CAMAC gewährleistet, dass Geräte verschiedener Hersteller austauschbar oder kompatibel sind und gemeinsam in unterschiedlichen Systemen verwendet werden können. So sind auch Änderungen der Systemkonfiguration aufgrund neuer Anforderungen leicht möglich. Für unterschiedliche Anwendungen stehen kompatible Geräte von Firmen aus vielen Ländern zur Verfügung.

Verfügung.
CAMAC ist das Ergebnis einer multinationalen Zusammenarbeit von System-Ingenieuren, aus dem Gebiet der Prozess-datenverarbeitung und ist ein firmenunabhängiger internationaler Standard, der von jedermann lizenzfrei benutzt werden kann.

### WHAT IS CAMAC?

CAMAC is an internationally used scheme for connecting digital processors and computers to on-line peripherals in systems for Computer Automated Measurement And Control.

There are rules for:

a digital interface for transferring data on a common highway;

a modular equipment format for adaptors to match peripherals and computers to the highway.

A compact assembly of these modular units can be used to multiplex many peripherals. Additional parallel and serial highways are defined for larger systems consisting of several of these assemblies.

CAMAC ensures that items of hardware from various suppliers are compatible and can be used together in any system, and also their subsequent reconfiguration to meet changing needs. Compatible products are available from firms in many countries and for uses in different application areas.

CAMAC is the result of multinational cooperation between data-processing system engineers. It is a non-proprietary international standard that can be freely used by any organisation.

# QU'EST-CE QUE CAMAC?

CAMAC est un concept utilisé sur une base internationale pour relier des processeurs digitaux et des ordinateurs à des périphériques en ligne, dans des systèmes de « Contrôle – Commande Ainsi que Mesure Automatisés par Calculateur ».

Des règles définissent:

Des regies dennissent:

— une interface numérique transférant des données sur une interconnexion générale;

— un format d'équipement modulaire pour l'adaptation des périphériques et des ordinateurs à cette interconnexion.

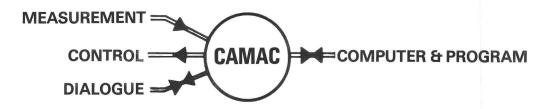
Un ensemble compact de ces unités modulaires peut être utilisé pour multiplexer de nombreux périphériques. Des interconnexions complémentaires, parallèle aussi bien que série, sont également définies pour des systèmes plus importants composés de plusieurs de ces ensembles.

CAMAC assure la compactibilité de l'écompactibilité de l'

CAMAC assure la compatibilité des éléments matériels fournis par différents producteurs ainsi que leur utilisation conjointe dans tout système; il facilite la constitution et la programmation des systèmes de même que leur reconfiguration consécutive à des changements d'utilisation. Dans de nombreux pays, différentes firmes proposent des produits CAMAC.

CAMAC résulte d'une coopération multinationale entre ingénieurs spécialistes des systèmes de traitement de données.

C'est une norme internationale non brevetée pouvant être utilisée librement par tout organisme.



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