CAMAC

bulletin

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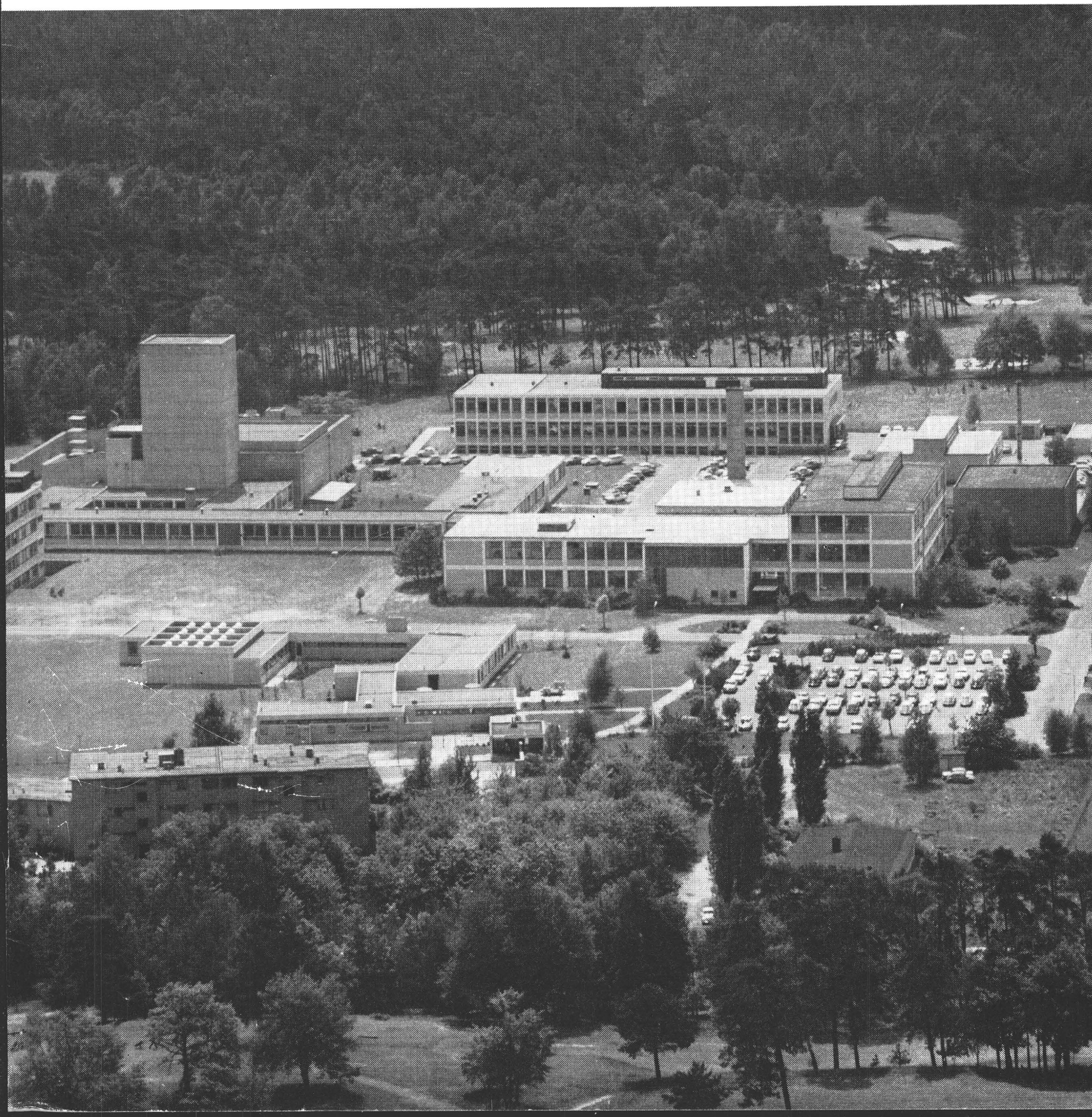

PRINCIPAL CONTENTS OF PREVIOUS CAMAC BULLETIN ISSUES

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New Products and Manufacturer News:	Dr. H. Meyer, CBNM Euratom, Steenweg naar Retie, Geel, Belgium.
Product Guide:	Mr. O.Ph. Nicolaysen, N.P. Division, CERN, 1211, Geneva, 23, Switzerland.
Bibliography and any ESONE News Items, etc.:	Dr. W. Becker, JRC Euratom, 21020 Ispra (Varese), Italy.

On the cover:

View of the Hahn-Meitner-Institut für Kernforschung, the German nuclear research centre in West Berlin. The fourth ESONE General Assembly was held here in 1964.

CAMAC

bulletin

Editorial Working Group:

H. Meyer, Chairman
W. Attwenger
R.C.M. Barnes
W. Becker
H. Bisby
P. Gallice
O.Ph. Nicolaysen

Production Editor:

C E C — DG XIII

Correspondence to:

the Secretary of the
ESONE Committee
W. Becker, JRC Euratom
I-21020 Ispra (Va) Italy

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Luxembourg

CONTENTS OF THIS ISSUE

HAHN-MEITNER-INSTITUT für Kernforschung Berlin GmbH
SEKTOR ELEKTRONIK

Progress in the development of the CAMAC system is remarkable. Since the publication of the documents EUR 4100 and 4600, the range of CAMAC modules and controllers offered by industry and others has considerably increased in number and quality due to the European-North American co-operation.

New non-nuclear fields of scientific areas, for example in medicine, environmental research, astronomy and industrial applications for process- and laboratory-automation are becoming extensively interested in the CAMAC System.

Developments arising in East European countries, as demonstrated on the occasion of the 6th International Symposium for Nuclear Electronics in Warsaw (Sept. 1971), and now also in Australia, contribute to the dissemination of CAMAC and to the completion of its introduction on a world-wide basis. At the present time, the hardware is very well advanced in design, development and production.

But what about software? In most cases programs are still written in assembler languages, which are computer-orientated, inconvenient and not obvious for the unexperienced user. Instead superior, easy-to-use, problem-orientated real-time languages will achieve the breakthrough necessary for successful applications of the CAMAC system in all the different fields.
The joint efforts of the Software Working Group, concerning the definition of a CAMAC real-time language, are about to be tested on fundamental pilot implementations. For this a strong and intimate co-operation is required of all the qualified institutions involved.

Shouldn't we recognise just in time that we have to concentrate all our attention and the strength of our abilities in solving these most important software problems?

Karl Zander

Karl Zander, Head
Electronic Division

① INTRODUCTION TO CAMAC

METHODS OF DEMAND-HANDLING

by

Hans-Jurgen Trebst

University of Erlangen, Germany

SUMMARY This paper describes some methods and uses of demand-handling in CAMAC Dataway and Branch Highway Systems and gives an example of a LAM-sorting unit.

INTRODUCTION

It is important to understand the function of demand-handling and its possibilities in a computer-controlled CAMAC system. Demand-handling has three different purposes and often there is a tendency to concentrate on one only, at the expense of the others. Of course, they are inter-related but, to avoid confusion, they may be considered separately and the purposes categorised as follows:

Category 1. Priorities
Category 2. Actions
Category 3. Sources

Category 1 — Priorities

Demand-handling defines the order in which different demand sources are served by executing the appropriate programs (tasks):

(*a*) If several demand sources occur simultaneously, or are taken into account at the same time, the one with the highest priority has to be served first.

(*b*) If the system controller design allows a routine, serving some CAMAC modules, to be interrupted by another demand, then the decision whether the routine in progress should be interrupted or not will be based on the relative priority of the new demand.

Category 2 — Actions

Demand-handling selects the task that has to be started in response to a demand.

Category 3 — Sources

Demand-handling identifies the address of the module, or the part of a module, that contributed to a demand.

FACILITIES FOR DEMAND-HANDLING IN EUR 4100

Every station in a CAMAC-crate has a Look-at-Me (LAM) line, over which a module in that station can send an L-signal (L_i) to the crate-controller if the module demands service. When the crate-controller is coupled directly to the computer the controller can use these signals as allowed by the interrupt structure of the computer. The CAMAC Specification (here only EUR 4100) imposes no further restrictions. The computer for example may accept all L-signals on separate interrupt lines with specified priority. Special hardware may derive an address from the LAM-pattern (e.g., base address + + k·No. of highest LAM) containing a pointer or program vector with the starting address of the routine that performs the required action. The crate-controller may also combine the L-signals into several groups or present the logical OR of all of them as a single interrupt. Then the interrupt handling routine will search for the LAM by the 'Test LAM' function [F(8)] or by reading and analysing a LAM pattern. For a small number of L-signals in one group the 'TESTLAM' function is preferred since it is easy to program and requires no additional hardware.

A module may be able to generate several LAM requests. To find which part of the module is requesting service, the same scheme as before may be applied to the next level of the search tree; if there are many LAM requests one reads them as a register by F(1)·A(14). For a few LAM requests it may again be easier to search for them by 'Test LAM', [F(8)A(i)]. The sub-address A(i)—also used for Clear LAM, [F(10)]—must be chosen suitably. This may not be easy since although A(0) would be a good choice for addressing the overall L-signal of the module, other considerations may suggest it is better that the features of the module selected by the sub-address code should be numbered from A(0).

It is clear that the requirements of the three categories 1, 2 and 3 (Priorities, Actions and Sources) can be met. Whether 1(b) will be also performed (nesting of interrupts with different priorities) or only 1(a), is not influenced by the CAMAC Specification.

FACILITIES FOR DEMAND-HANDLING IN EUR 4600

In a system which also uses the Branch Highway, the Branch Highway Specification (EUR 4600) restricts the freedom of demand-handling, for economic reasons. The following sections show how, nevertheless, all requirements can be met.

Assume that crate-controllers Type A are used. They have an external connector through which the L-signals generated in that crate are brought out, the LAM-Grader connector. This allows the L-signals to be re-arranged in order, wire-ORed together or channelled through a separate LAM-sorting unit. The resulting signals (GL_i) are referred to as Graded-L signals (where $i = 1, \ldots, 24$). Their OR-combination becomes the Demand from this crate and is applied to the BD-line of the Branch

Highway, where it is ORed together with the Demands from other crates. The normal response of the branch driver to a branch demand is a Graded-L operation. It is performed either by the hardware of the branch driver or by the computer with the BD-signal connected as interrupt. By the Graded-L operation, the branch driver reads the GL_i from all crates, bit-wise ORed together. Proper use of the GL-pattern is the key to satisfactory performance of demand-handling.

(1) One-Step Search

Consider a system with not more than 24-demand sources. Each GL-line may be assigned to a specific L-signal or demand source* by the back-wiring of LAM-Grader plug inserted into the LAM-Grader connector, or in a LAM-sorting unit. By reading the GL-pattern, the branch driver and computer obtain complete information on the demand sources as described earlier. This means that the requirements of categories 2 and 3 can be met. By suitably rearranging the L-signals in the GL-pattern, 1(a) is easily obtained. But 1(b) can only be achieved by frequent insertion of GL-operations into the execution of the current CAMAC-program, unless the special LAM-sorting unit described below is used. Another drawback is that the assignment of L-signals to GL_i signals has to be done by wiring and is therefore not under program control. At this state of the art, a software controlled assignment device would be expensive.

(2) Two-Step Search

A CAMAC branch may contain up to 161 modules (7 crates, 23 modules/crate). Although in a practical system not every module will produce an L-signal, a large number of L-signals is a possibility. They can however, be grouped into 24 priority classes, and this division should be sufficiently fine. By comparison most computers have fewer priority levels. Some priority classes will have a unique connection to the action required to serve them, especially the ones with higher priority. For these all considerations of the previous sections are valid. But even if 24

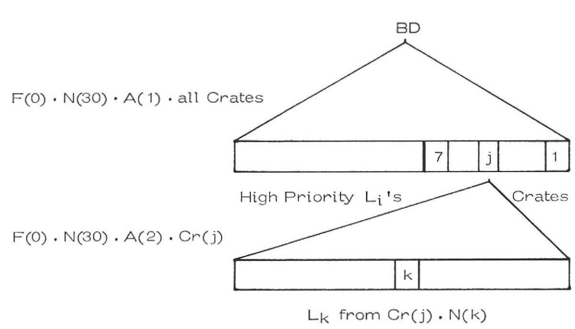


Fig. 1 LAM-Search Tree

* A demand source means here any Boolean function of any number of LAM's of one crate which can be cleared by a number of Clear LAM-operations [F(10)]. This excludes for example, $\overline{L_i}$ or 1. A legal example would be $L_p \cdot L_q\ L_q \cdot \ldots L_r$ or $L_p + L_q$. In the simplest case, a demand source is just an L-signal.

different (primary) actions would be sufficient it may be necessary to obtain more detailed information on the LAM sources.

If only a few L-signals are in one priority class they may be scanned by F(8). But for more than say 3 to 6 L-signals this becomes a time-consuming process and a better strategy is needed. The obvious choice is to use a search tree which first identifies the crate address(es) where demands originate, then the station number(s) in this crate (see Fig. 1). This can only be done by a special LAM-sorting unit that in addition to responding to the BG signal (Branch Give Demand Pattern), also responds to a Read Command $F(0) \cdot N(30) \cdot A(i)$, $i = 0, 1, 2$. These latter operations are practically identical to Graded-L operations.

Going through the search tree, in the first step the 'OR' of all demand sources in a crate is routed in the LAM-sorting unit to GL_j, where j is the number of this crate, i.e., $j = 1, 2, \ldots, 7$. This is performed by $F(0) \cdot N(30) \cdot A(1)$, addressed to all (on-line) crates (see Fig. 2). In the second step, the system controller addresses only that crate (j) where it found a demand source in the first step. By means of $F(0) \cdot N(30) \cdot A(2)$ all LAM's from that crate are switched to the GL-lines, giving the system controller a geographical representation of the origin of the LAM's. In the third step the LAM requests from different parts of a module can be found as described for demand handling in EUR 4100.

There are still 17 bits available in the pattern of the first step of the search tree (see Fig. 2). Therefore supplementary to this procedure, up to 17 demand sources can be given privileged treatment by assigning them to the GL-lines 8-24. If one of these carries a '1' the search is finished in the first step. The system controller responds to this demand source, thereby clearing the LAM(s). So its double occurrence (once in the privileged group GL_{8-24} and also in the normal group served by the two-step process) does not matter. If more than one demand source is found, the system controller first processes the one of highest priority. Thereafter the whole process is repeated until all are served.

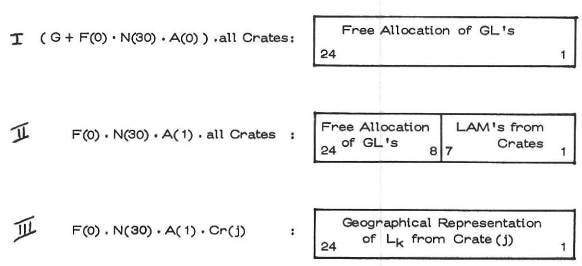


Fig. 2 GL-Patterns

So again requirement Category 1(a) is easily fulfilled by genuine CAMAC-operations, and may be also that of Category 2. For efficiency in Category 3 and possibly 2, a LAM-sorting unit with features described in Fig. 3 is needed. Category 1(b) cannot be handled adequately by this means, for the reasons given earlier. The two-step LAM search of Fig. 1 has the advantage that it provides a means for locating LAM's without the need for special individual wiring.

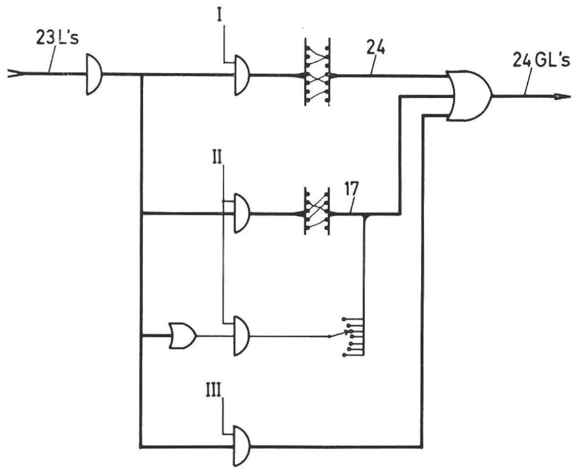


Fig. 3 Block Diagram of LAM-sorting unit. I, II and III are the commands of Fig. 2.

PRIORITY CONTROLLED DEMAND

The normal use of BD has the drawback that the system controller cannot know, before it has made a BG-operation, whether a new signal on the BD-line comes from a demand source of higher or lower priority than the demand source it is presently dealing with. However, the BG-operation may cost a lot of register saving and restoring and GL-pattern checking, perhaps only to find that it was unnecessary because the new demand did not have higher priority. Therefore there is a tendency, at present, not to allow interruption of a CAMAC-routine in progress, i.e., to exclude 1(b). But even 1(b) can be solved efficiently by a suitable strategy implemented in the LAM-sorting unit.

Assume that the demand sources are assigned to the GL-lines in order of their priority. In a BG-operation, the GL-lines are connected to the BRW-lines and in this way the complete information on the demand sources is conveyed to the system-controller. This information can be fed back to the LAM-Grader units, e.g., by a multi-crate 'Write' operation after the BG operation. Even during the BG operation the LAM-Grader may get this information from the BRW-lines via the W-lines, thus saving the additional operation. This path is not guaranteed by the CAMAC Specifications and depends on the design of the crate-controller. But crate-controllers do exist which provide this path during BG, e.g., the Siemens CCA. The LAM-Grader can use this knowledge of the complete demand situation to connect only demand sources of higher priority to the BD-line. One may think of this as a 'sliding mask'. During the BG-operation, or the multi-crate 'Write' operation, it raises the mask just high enough to exclude all demand sources of equal or lower priority than the demand currently being serviced. The difference in the priority of different demand sources should be of more than marginal value to the performance of the system, so that it is not degraded too much by the overhead due to changing programs. If it is inconvenient to group several LAM's together because they should be connected to various actions, there is the further possibility of raising the priority of a CAMAC-routine in progress by writing a suitable bit pattern into the sliding-mask registers, e.g., the GL-pattern shifted some position to the left.

After a demand source has been served the sliding mask must be reset. If it was set by BG then another BG operation resets it to the rest state if there is no further demand, or to the appropriate state if another demand has been waiting. Otherwise the sliding mask has to be cleared by a multi-crate 'Clear' operation.

ESONE ANNOUNCEMENTS

Availability of EUR 4100 (1972), EUR 4600 and EUR 5100

The final document EUR 4600e (corresponding to AEC TID 25876), 'CAMAC, Organisation of Multi-Crate Systems, Specification of the Branch Highway and CAMAC Crate Controller Type A-1' is now available Probably the document EUR 5100e 'CAMAC, Specification of Amplitude Analogue Signals' and the document EUR 4100e (1972) (Corresponding to AEC TID 25875), 'CAMAC, A Modular Instrumentation System for Data Handling', a revised version of the EUR 4100e (March 1969), will by available in July 1972.
Orders can be submitted already now to the following address:

Office for Official Publications
of the European Communities.
LUXEMBOURG, P.O. Box 1003

Endorsement of EUR 4100e (1972)

The Executive Group of the ESONE Committee endorsed during their 13th meeting (May 3-4, 1972) the revised version of EUR 4100e 'CAMAC a Modular Instrumentation System for Data handling' with the designation EUR 4100e (1972).

The ESONE Committee recognizes the importance of making revisions to the CAMAC specifications only when this is essential, and of maintaining compatibility between CAMAC equipment.

None-the-less corrections, extensions and interpretations of these specifications made in collaboration with the USAEC NIM Committee can be expected occasionally and will be announced in the CAMAC Bulletin.

(2)

THE REVISED CAMAC SPECIFICATION EUR 4100e (1972)

by

R. C. M. Barnes

Electronics and Applied Physics Division
A.E.R.E., Harwell, U.K.

SUMMARY A revised version of the basic CAMAC Specification, defining the Dataway and mechanical standards, is being published as EUR 4100e (1972) and TID-25875. This paper describes the main changes that have been introduced.

INTRODUCTION

The basic CAMAC Specification EUR 4100e was first published three years ago. Since then the branch highway and Crate Controller Type A have come into use, much work has been done on a CAMAC programming language, and designs have been influenced by a vastly improved range of integrated circuit components. As a consequence it has become necessary to consider changes to the Specification in order to add new features, to strengthen some existing features, and to define others more clearly. The ESONE Committee has therefore authorised the publication of a revised specification EUR 4100e (1972) to replace the previous version.

Equipment conforming to the original specification will continue to be 'CAMAC Compatible', but it is intended that all new designs not already committed to conforming to EUR 4100e (1969) will conform to the revised specification. Although only systems conforming entirely to the revised specification will obtain the full benefits of the improved features, the revision has been guided by the principle that new equipment should be able to work in conjunction with equipment and systems conforming to the original specification. The effect of this revision on the Branch Highway specification (EUR 4600e) is discussed later in this paper.

MECHANICAL STANDARDS

Revised dimensions, already announced in CAMAC Bulletin No. 1 on page 26, are included in the new specification. They extend the tolerances of the width of individual guides and the separation between the top and bottom guides in order to overcome manufacturing difficulties.

Important changes have been made to the dimensions of the Dataway connector socket and plug (in the crate and on plug-in units, respectively). The dimensions of the contacts on the plug and socket have been re-defined with wide tolerances. The chamfers on the plug are now reduced, and the insertion-depth at which the plug first makes contact with the socket is defined, thus ensuring that there is no electrical contact until the plug and socket are correctly aligned. A maximum insertion and withdrawal force is recommended for the socket, in order to avoid difficulty and risk of damage, particularly when inserting and withdrawing units with more than one connector plug. The object has been to define the essential characteristics of the Dataway socket in a more meaningful way. Most sockets now used in CAMAC crates should satisfy the new specification.

A new non-mandatory diagram, Figure 8, gives the principal dimensions of a printed wiring card suitable for most existing designs of module chassis.

DATAWAY STANDARDS

Command accepted

There was previously no means by which the controller could detect such serious malfunctions as commands addressed to vacant stations or to modules unable to perform the required function. This weakness has been corrected by assigning the Dataway X bus-line for a Command Accepted Signal. When a module is addressed with a command that it is equipped to perform it generates $X = 1$. At the controller the signal $X = 0$ indicates a malfunction. This feature is not applicable to multi-addressed operations, since $X = 1$ from one module will mask $X = 0$ from any other module. If necessary, existing modules could be modified to give a partial implementation of Command Accepted by generating $X = N_i$.

Effective use of the Command Accepted line is encouraged by a new mandatory requirement that all ***function*** and ***sub-address codes*** used in a module must be ***fully decoded.*** Full decoding has already been widely adopted in recent designs of CAMAC equipment, although it was not mandatory.

Response (Q)

The new specification defines three ways by which the Response signal (Q) can be used to control the transfer of blocks of data. The ***Address Scan mode,*** as previously defined, is used to operate on an array of registers that do not necessarily occupy consecutive CAMAC addresses. The ***Repeat mode*** is used if a register is sometimes not ready to transfer data. The ***Stop mode*** is used if the module itself determines the end of the data block. The use of Q during read and write operations is not restricted to these three modes of block transfer. Previously the Address Scan mode appeared to be mandatory for all data registers, in all read and write operations.

Demand Handling

The new specification introduces a consistent terminology for the means by which Look-At-Me

(LAM) conditions in a module are enabled, tested, cleared, and combined to form the Dataway L-signal. The general structure, and the commands available to operate on it, are summarised in a new non-mandatory diagram (Figure 11). The provision of means for testing the L signal and individual LAM requests is now made mandatory.

In modules with few LAM requests it is recommended that access to the features associated with LAM_i should be via sub-address A(i). In more complex modules it is recommended that the LAM status bistables should be accessed as a Group 2 register at A(12), the control of enabling and disabling LAM requests should be by a mask register in Group 2 at A(13), and the LAM requests should be examined by reading a Group 2 register at A(14). Access to the features associated with LAM_i is then via bit (i) of the data words read from or written to these registers. (A further Group 2 register at A(15) has been recommended for the 'module characteristic', if required, without specifying the bit-allocation of this register).

In large systems there can be appreciable delays between the generation or removal of the *L* signal at a module and the corresponding change in the demand signals at the system controller. To counteract these delays the mandatory gating of *L* signal outputs has been changed. The *L* signals are gated by Busy (B) and so could only be generated between Dataway operations. Now each *L* signal can be maintained continuously except during an operation that will cancel it. The precise implementation of this principle, to obtain the maximum advantage, may sometimes be difficult. The specification therefore also describes simple implementations, including gating L_i by N_i. The permitted signal loading on the *N* line at each station has been doubled so that existing modules can be modified easily, if required.

Selective Write Functions

The function codes F(18), F(19), F(21) and F(23) have been re-defined in order to provide more powerful means of operating on individual bits of Group 1 and Group 2 registers. Function codes F(18) and F(19), previously Selective Overwrite, are now Selective Set Group 1 Register and Selective Set Group 2 Register. These set bit X_i of the register to the '1' state if the corresponding data bit on Write line W_i is in the '1' state. Two reserved function codes F(21) and F(23) are now Selective Clear Group 1 Register and Selective Clear Group 2 Register. These clear bit X_i of the register to the '0' state if the corresponding data bit on Write line W_i is in the '1' state. Otherwise X_i is unchanged. The Selective Set operations form the OR combination $W_i + X_i$, and the Selective Clear operations form $\overline{W}_i . X_i$.

In the new LAM structure diagram (Figure 11) Selective Set and Clear are shown as means of operating on selected bits of the Group 2 LAM status register and LAM mask-register.

Group 2 Registers

There are still no mandatory distinctions between the uses of Group 1 and Group 2 registers, but there are recommendations that any registers requiring privileged access, or associated with status and system organisation, should be in Group 2. The specific recommendations for the use of sub-addresses A(12) to A(15) in Group 2 do not exclude the use of these sub-addresses for other purposes.

Execute Function

The natural use of the Disable and Enable functions, F(24) and F(26), is for establishing and maintaining the appropriate condition. There was no obviously suitable function code for 'single-shot' actions such as generating a pulse. Therefore F(25) has been renamed 'Execute' and defined for this purpose, which conveniently includes its previous use for Increment.

Common Control Signals

Timing sequences for the generation of Initialise (Z) and Clear (C), accompanied by Strobe S2 and Busy (B), are now defined in a new Figure 10. These sequences are called Unaddressed Dataway Operations. It is made clear that Initialise is intended for use at start-up, to set the system into a defined inactive state in which the generation of Inhibit (I) is also appropriate. Units that can generate a maintained I signal are now required to do so in response to Z, and units that generate Z are also required to generate an I signal overlapping the signal from other I-generators. It is now mandatory for all units that use Z and C to gate them with S2 (previously this was only recommended).

Free Bus-Lines

Signal standards were defined for the patch contacts P1-P5 at each normal station but this left complete freedom for the significance of the signals and the pattern of interconnections. It is now mandatory that two of these contacts, P1 and P2, must be linked by two new Free Bus-Lines. Signals on these lines must conform to the standards of either the data lines or the remaining patch contacts (the latter allowing more variation in the number of signal sources and receivers). Modules may use these lines in conflicting ways, and must therefore have a means of disconnection from the Free Bus-Lines. For an example of one use of a Free Bus-Line see the paper by Iselin, Löfstedt and Ponting in CAMAC Bulletin No. 3, pages 7-8, describing a Hold signal using the P2 line.

SIGNAL STANDARDS

The lower limit of the mandatory voltage range for 'O' state outputs of Dataway signals has been raised from +3.0 V (for which there were no corresponding current standards) to +3.5 V (previously a recommended value).

Apart from doubling the permitted current loading on the N line the current standards are not significantly changed, although they are now defined in terms of the currents flowing through the Dataway connector.

POWER LINE STANDARDS

To avoid misunderstanding it is now stressed that the permitted ranges of the power supply voltages are defined at the Dataway connector. Therefore Section 8 and Table X do not directly define a CAMAC power supply unit.

INTERACTION WITH EUR 4600e

The formal specification of the Branch Highway and Crate Controller Type A which was published in April 1972 as EUR 4600e*, has been brought into alignment with the main changes in EUR 4100. Thus the Branch Highway now includes a Command Accepted line BX. Crate Controller Type A(CCA) also generates BX signals when it is addressed. The new requirements for the generation of Inhibit with Initialise are included in the specification of CCA in the on-line state. To avoid software incompatibilities with existing crate controllers the use of Enable F(26) for generating Initialise and Clear is continued, although Execute F(25) would have been more appropriate. The defined features of CCA do not involve the use of the Free bus-lines. It may be assumed that most, if not all, uses of the Free bus-lines by CCA are excluded by the mandatory requirement that "it must have no other features that would affect its interchangeability with any other Crate Controller Type A". This does not apply to crate controllers other than CCA.

* See below for a 'summary of the main differences between the final text of EUR 4600e and the preliminary issue'.

NEWS

SUMMARY OF THE MAIN DIFFERENCES BETWEEN EUR 4600e AND THE PRELIMINARY ISSUE (NOVEMBER, 1971)

1. The Reserved lines BX9 and BX9(R) are now allocated to the cable screen, with mandatory grounding in units that terminate the signal lines, and optional grounding in other units. (Section 6.1).
2. The Reserved line BX8 is now allocated to the Command Accepted signal BX, derived from the Dataway X line and from Crate Controller Type A. (Sections 4.2.3 and A1.8).
3. The designations of the remaining seven Reserved lines are now BV1 to BV7. (Tables I, VI and VII).
4. The transition time of the BD signal is reduced from 400±200 ns to 100±50 ns (Section 4.4.1).
5. The maximum delay between an L signal transition and the corresponding BD signal transition is now defined as 400 ns, of which not more than 250 ns is due to Crate Controller Type A. (Sections 4.4.1 and A1.9.2).
6. The Dataway Inhibit signal (I) is now established before t_3 when Crate Controller Type A generates Z, in order to meet the requirement of EUR 4100e (1972). (Section A1.5.3).
7. It is now emphasised that other methods of interconnection of crates are permitted, including methods using crate controllers dedicated to specific computers. (Abstract).
8. Crate controllers conforming to this final specification and EUR 4100e (1972) may use the designation Crate Controller Type A-1 (CCA-1). (Footnote to Section 1).

U.S. AEC NIM COMMITTEE CONFERENCE AND U.S. AEC NIM CAMAC WORKING GROUP MEETINGS

The NIM Committee is scheduled to meet in Miami Beach, Florida, during the week of December 4 in conjunction with the 1972 IEEE Nuclear Science Symposium. NIM-CAMAC Working Group meetings are also scheduled for Miami Beach beginning about November 30.

The Nuclear Science Symposium will include a session devoted to CAMAC papers. Commercial exhibits at the Symposium, December 6-8, will include CAMAC equipment. The Exhibits manager is Trade Associates, Inc., 5454 Wisconsin Avenue, N.W. Washington, D.C. 20015, U.S.A.

NIM-CAMAC Working Group meetings are also scheduled for the week of July 10 at the U.S. National Bureau of Standards in Boulder, Colorado.

1

APPLICATION NOTES

A VERSATILE INTERCONNECTION OF FOUR SPECTROMETERS TO A PDP-11 COMPUTER

by

Y. Lefebvre and A. Axmann

Institut Max von Laue — Paul Langevin, Grenoble, France

SUMMARY Data Acquisition and Processing over long distances generate great problems which can be solved by using an extension of the PDP-11 UNIBUS. The new BUS, consisting of 100 balanced lines, may have any length. A unit called a SYSTEM CONTROLLER takes the place of both the usual SYSTEM CONTROLLER and CRATE CONTROLLER. The primary interfacing of four spectrometers is done using CAMAC modules and crates.

INTRODUCTION

Three curved-crystal, gamma-ray spectrometers[1] and a magnetic-conversion-electron spectrometer, used at the Grenoble High Flux Reactor for investigation of slow-neutron capture reactions, are connected to a common PDP-11 computer. The computer controls the operation of the spectrometers, e.g., crystal positioning and magnetic field settings, and collects data. It will also, eventually, evaluate the spectra thus obtained.

REQUIREMENTS OF THE SYSTEM

The 5.8 m γ-spectrometer (GAMS 1) is adjacent to the PDP-11, however, the 24 m double-γ-spectrometer (GAMS 2 and 3) is situated at a distance (85 m) away from the PDP-11 and so too is the β-spectrometer (BILL) which is located on the upper floor of the reactor and requires 140 m of cable to connect it to the computer. The first requirement then is to interface these major electronic devices and connect them to the computer using parallel-data transmission lines because of the high data rates involved.

The experimenter requires a current spectrum display at each γ-spectrometer during a measurement run, consequently GAMS 1, 2 and 3 must have independent direct memory access in order to perform multi-scaling in 12,000 channels.

CAMAC has been chosen as a standard at the Institute for interfacing experiments to computers for the following reasons:

- Many similar compatible modules can be used on a large variety of experiments.
- These experiments can profit from the development efforts in other laboratories and from the instrument industry.
- The local effort required in the laboratory can be minimised due to the standardisation of functions by CAMAC.

Thus the major devices in the system are interfaced for control and data acquisition via CAMAC modules and crates, however the CAMAC Branch Highway has limitations on length which fall short of the distances involved in the system requirements.

The four spectrometers must be treated as four separate and completely independent experiments by the software which must therefore fulfil the requirement of a multi-user system.

For such a multi-processing system, a high degree of transparency is required and at the same time must allow elaborate on-line and off-line testing to be done.

FEATURES OF THE SYSTEM BEING DEVELOPED

Adressing

An internal register of a CAMAC module connected on the Dataway is treated by the computer as a word in memory or as if it were any other peripheral.

Interrupt System

One interrupt vector is available from any CAMAC module in a crate.

Display

Any module register can be displayed 'on-line' from the system controller by setting up a NAF code on the controller's front-panel. This display technique utilises the rest-time of the Dataway.

Other Features

These include the possibility of incrementing memory directly from the CAMAC modules and the essential feature of long distances between CAMAC crates and the computer.

DESCRIPTION OF THE SYSTEM

System Organisation

A block schematic of the system is shown in Fig. 1.

A PDP-11 Unibus cannot be used beyond 10 m so that a UNIBUS Relay Unit has been developed which allows the use of telephone line twisted-pairs to extend the UNIBUS lines over the required distances. Every module connected to the extended UNIBUS is treated as a processor peripheral, thus several PDP-11 peripherals can be located in a crate and for example:

- The System Controller.
- The memory increment module.
- The Teletype interface module.
- The UNIBUS Display.

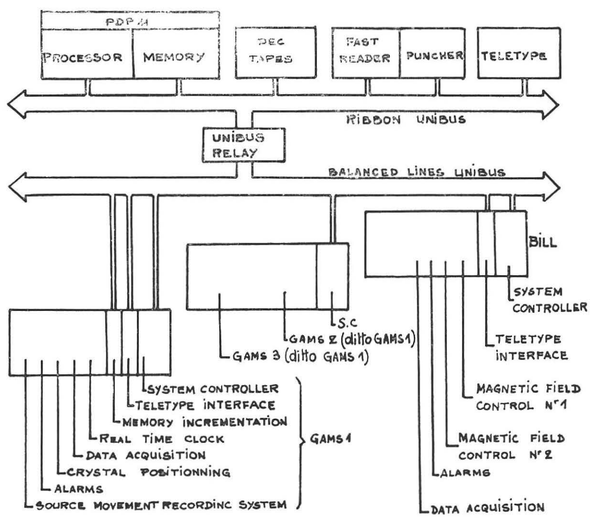


Fig. 1 Schematic of the total System

These are connected into the UNIBUS via double-density Cannon connectors situated on rear-panels and can be on either side of the UNIBUS Relay Unit. This feature enables these devices to be used within the basic PDP-11 configuration. The system controller can be replaced by a simulator for static or dynamic tests.

UNIBUS Relay

The extended UNIBUS has 50 twisted pairs. It extends the duration of a computer instruction to about 250 nanoseconds when the source or destination of transfer is located in a CAMAC crate. Internal computer instructions and data transfers to and from DECtapes and Teletypewriters are not affected.

System Controller

The extended UNIBUS replaces the CAMAC Branch Highway, so that the functions of system-control and crate-control are also combined in this system controller.

The system controller can generate 24 interrupt vectors for the computer and is also able to change the word length. A 24-bit data output requires 2 instructions and a 24-bit data input needs 3 instructions. Whenever a data output of function code only, or function code + 8 data-bits, is to be performed, the transfer can be reduced from 2 to 1 instruction. In the same way a data input of 16-bits needs only 2 instead of 3 computer instructions.

Standard Module Interface

This module may be used to connect many different electronic devices to the Dataway; it is so powerful and flexible that only the one type of module may be required in a crate for most general purposes.

The module will enable eleven 24-bit registers to be loaded via the Dataway. It will also allow four 24-bit data sources, of which one is memory-buffered, to be read. Twelve events may be connected to the L-line so that every change of event

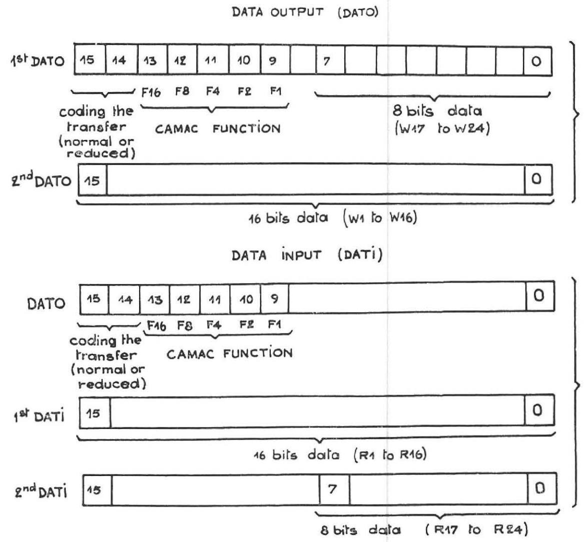


Fig. 2 Input/Output Instruction

can generate an interrupt. Thus 24 sources of interrupt are available for one interrupt vector.

A 24-bit control register permits staticised commands to be sent to several electronic devices by means of internal strapping.

The connection to external electronic devices is made via two 100-way Cannon connectors on the front-panel.

The functions used by the module are:

READ DATA	F(1)·A(0, 1, 2, 3)
READ CONTROL REGISTER*	F(1)·A(11)
READ BUFFER*	F(1)·A(12)
READ MASK REGISTER*	F(1)·A(13)
READ LAM PATTERN**	F(1)·A(14)
READ STATUS REGISTER**	F(1)·A(15)
WRITE BUFFER*	F(16)·A(0 to 10)
WRITE CONTROL REGISTER*	F(16)·A(11)
WRITE MARK REGISTER*	F(17)·A(13)
TEST L (not used)	F(8)·A(0)
CLEAR ALL REGISTERS	Z
CLEAR L_i	[F(10)·A(i) exclusive or F(10)·A(14)·(i)]+Z
LAM INHIBIT (made valid by a strap)	F(10)+F(16)+F(17)

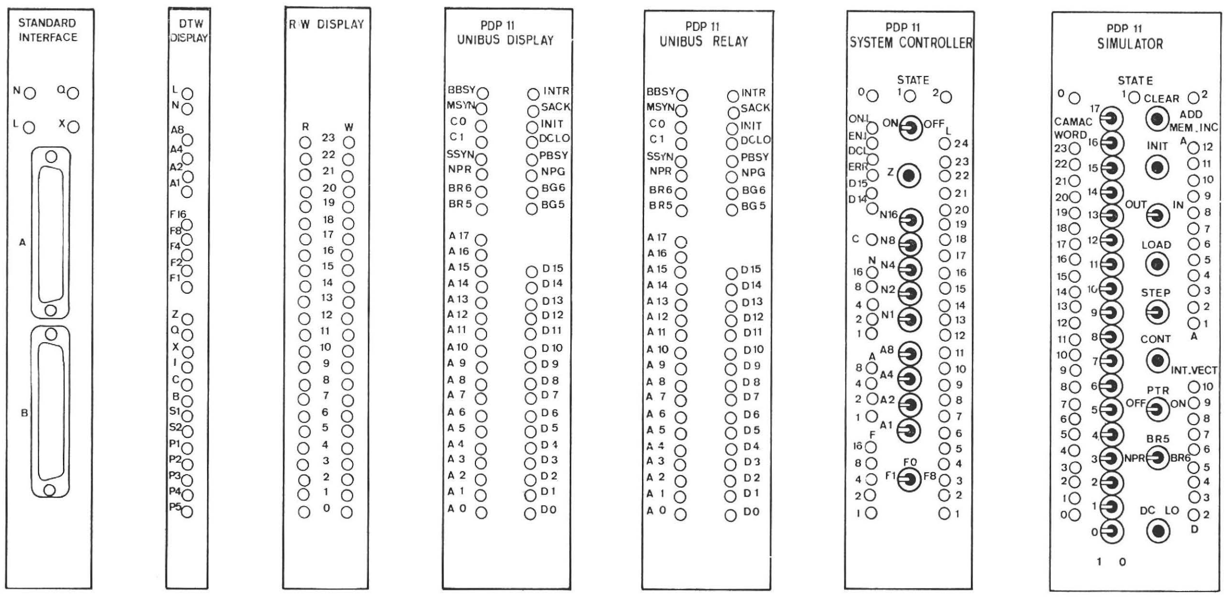
* (24 bits)
** (12 bits)

Display Modules

Because of the wide geographical location of the total system, several displays using luminous diodes have been developed to make software and hardware and hardware checking and maintenance relatively easy. Some examples are given in Fig. 3.

Simulation

A Simulator has been developed to test the system controller and the memory increment interface. This has been found useful in saving computer time. Data transfers using one, two or three computer instructions may be performed while granting interrupt demands.



BSSY . . . . .BUS BUSY
MSYN . . . . .MASTER SYNCHRONISATION
SSYN . . . . .SLAVE SYNCHRONISATION
NPR . . . . .NON PROCESSOR REQUEST
BR . . . . .BUS REQUEST
NPG . . . . .NON PROGRESSOR GRANT
BG . . . . .BUS GRANT
INTR . . . . .INTERRUPT
SACK . . . . .SLAVE ACKNOWLEDGE
C0, C1 . . . . .CONTROL BITS

PBSY . . . . .PERIPHERAL BUSY
INIT . . . . .INITIALIZE
DCLO or DCL . . . . .DC LOW
ON L . . . . .ON LINE
EN I . . . . .ENABLE INTERRUPT
ERR . . . . .ERROR (SOFTWARE)
PTR . . . . .PRIORITY TRANSFER
CONT . . . . .CONTINUE
INT VECT . . . . .INTERRUPT VECTOR
MEM INC ADD . . . . .MEMORY INCREMENTATION ADDRESS

Fig. 3 Front-panel Layouts of Units which have been developed

CONCLUSION

The development of the interconnection between CAMAC and the PDP-11 is the result of an attempt to get the best performance from the PDP-11/CAMAC facility. For example, a register can be addressed directly, each CAMAC module can initiate a sub-routine; only one computer instruction need be used for a CAMAC function; simplified data transfers are possible whenever a change of word-length is not required and the distances between the PDP-11 and CAMAC crates, and the distances between crates themselves can be any length.

ACKNOWLEDGEMENTS

The authors wish to thank Messrs. H. Halling, K. Zwoll and K. Müller of K.F.A. Jülich for most helpful discussions concerning the PDP-11 Crate System Controller developed by them.

REFERENCE

1. Conference on Nuclear Structure Studies with Neutrons. Budapest, July 1972. Neutron Capture γ-Ray Spectrometry at the Grenoble High Flux Reactor.

NEWS

CAMAC SEMINARS

The TENTH of the popular two-day seminars on CAMAC has brought the number of attendances to close on 300. The next seminar will be held on 25th-26th October, 1972 and the fee is £30, excluding accommodation. Application forms are available from the Post Graduate Education Centre, A.E.R.E., Harwell, Berkshire, England and early application is recommended owing to the restricted number of vacancies available. The lecturers are normally, Messrs. R.C.M. Barnes, A. Lewis and H. Bisby.

ESONE/CAMAC LIBRARY

An ESONE-CAMAC Library is being set up at Ispra by the ESONE Committee Secretariat. It will comprise a collection of all papers and other documents relevant to the many aspects of CAMAC and a library loan-service which can supply a copy of any required article.

In order to commission the library in the first place and to keep it up-dated, the Secretariat appeals to all authors to supply one copy of any relevant document which is available now and is not listed in the Karlsruhe Bibliography (KFK 1471 Sept. 1971) and any documents which become available in the future.

The secretariat address is:

EURATOM, CCR

21020 ISPRA (VARESE), ITALY

2

APPLICATION OF A MULTICRATE CAMAC SYSTEM TO A PION ELECTROPRODUCTION EXPERIMENT (PEP)

by

D. Clarke, M.W. Collins and A.G. Wardle

Science Research Council
Daresbury Nuclear Physics Laboratory, U. K.

SUMMARY Signals from a bank of photomultipliers are buffered in a NIM fast-logic system and event data-buffers and other functions interfaced via CAMAC to a Honeywell DDP-516 computer. The DDP-516 is connected via a CAMAC data-link interface and an IBM 1800 multiplexor to a large time-shared IBM 360/65 computer. Feedback of status information and the display of the results of current data analysis allow efficient control of the experiment to be exercised.

INTRODUCTION

This note describes the application of CAMAC to the PEP experiment recently completed on the NINA electron synchrotron at the Daresbury Nuclear Physics Laboratory. The experiment measured cross-sections of the process: ep $\rightarrow$ enπ^+.

Signals from 330 photomultipliers in the detection system are buffered in a NIM fast-logic system. Event data-buffers and other functions interfaced to CAMAC are organised by a HONEYWELL DDP-516 (8K) computer. The DDP-516 is linked via a CAMAC data-link interface and IBM 1800 multiplexer to a large time-shared IBM 360/65 computer. Such a system permits (a) storage of event data and DDP-516 programs on IBM 360 disc, (b) on-line analysis of event data and (c) monitoring of various experimental parameters. Feedback of experimental status information, as well as the results of current data analysis for visual or hard-copy presentation enable the physicist to exercise more efficient control of his experiment.

DDP-516 SYSTEM SOFTWARE

The main programming effort has been directed towards providing an efficient executive and diagnostic software package PEPER, which may be used to run the experiment by personnel unskilled in computer programming. PEPER, written in the DDP-516 assembler language DAP16, supervises the following areas of interaction as shown in Fig. 1:

(a) Setting up and controlling the experiment using a CAMAC interfaced 'run control' panel.
(b) Nested servicing of eight real-time interrupts including acquisition and double buffering of 50 × 16-bit word event data buffers.
(c) On-line sampling and display of raw event data.
(d) Bi-directional communication between DDP-516 and IBM 360 computers with local control of the IBM 360 on-line program by means of a CAMAC interfaced keyboard.
(e) Local automatic magnetic tape back-up for event data storage in case of link failure.
(f) Organisation of background housekeeping, diagnostic and experimental monitoring tasks using a cyclic executive routine, JOBQ in which an overlay facility is used for infrequent tasks.

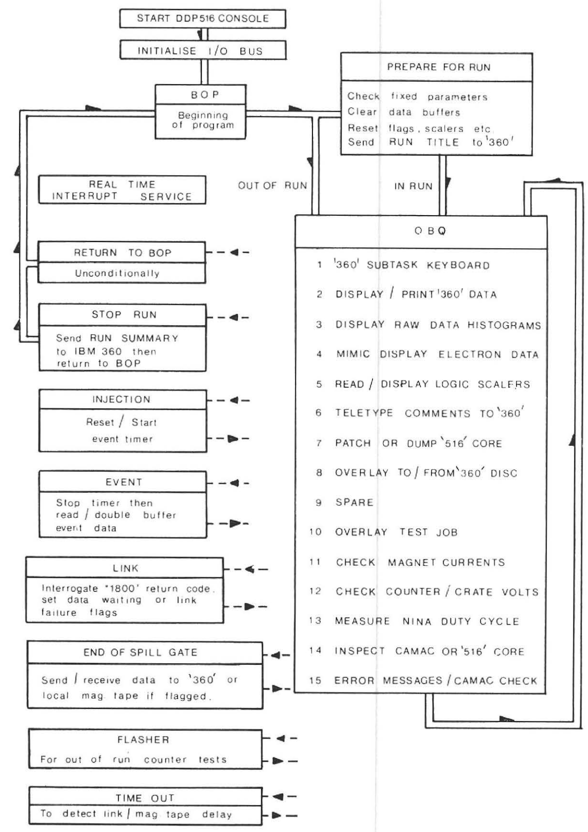


Fig. 1 PEPER Organisation

The PEPER software has been continually updated for the purpose of commissioning CAMAC interfaced hardware as well as to optimise specific areas of supervision where operating experience has shown this to be necessary.

CAMAC ORGANISATION

CAMAC is interfaced to the DDP-516 I/0 bus by means of an in-house controller (EC325) whilst Harwell 7000 series intercrate interface and slave dataway controllers provide CAMAC intercrate control as shown in Fig. 2. The mastercrate houses modules which are most frequently called by the PEPER software. The three slave-crates are used for arrays of modules predominantly assigned to specific experimental functions.

EXPERIMENTAL APPLICATIONS

The various experimental applications of CAMAC are outlined in Fig. 3. For historical reasons, much of the interfacing is NIM orientated with data fed in parallel to high input-density

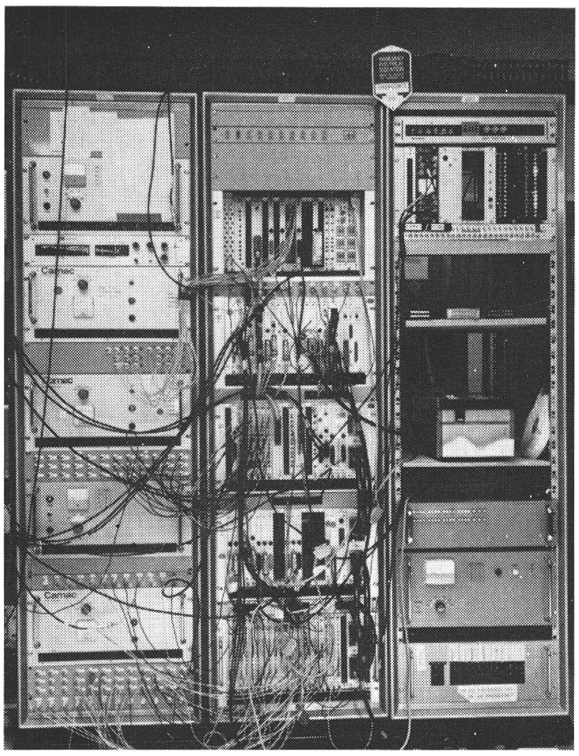


Fig. 2 CAMAC System used on the PEP Experiment

CAMAC modules. For example a 256-bit input gate (EC221) enable a variety of experimental functions to be interfaced to the DDP-516:

(a) A 16-bit keybord providing operator interaction with the IBM360 on-line program.
(b) Binary-coded-decimal (BCD) thumb-wheel selector switches containing semi-fixed experimental parameters.
(c) BCD digital clock data.
(d) BCD thumb-wheel swtiches providing operator interaction with the PEPER program.

This latter interaction may be illustrated by considering the rate at which specific tasks are executed on the PEPER JOBQ. Tasks are preassigned to one of four thumb-wheel decades each of which may be altered to control the relative task execution frequency. For example, magnet currents and logic scalers may be read every 100 sec, data histograms updated every 3 sec, but requests to display IBM360 data or print error messages are honoured every 10 mS. Thus important background tasks get the priority they deserve yet, for test purposes, the operator may increase the frequency of low priority tasks by simple thumb-wheel control.

Real-time interrupts are organised by a CAMAC interrupt register (EC218) which generates a computer interrupt from one of eight external sources patched according to priority as shown in Fig. 1. Interrupt lines may be separately masked and requests memorised whilst more important interrupts are being serviced.

A CAMAC data-link interface (EC318) is used for high speed transfer of data blocks between the DDP-516 and the IBM360 via the IBM1800 which concurrently multiplexes data from many other data links. Interrupts raised by the DDP-516 request input or output service at the IBM1800. When the request is granted the transfer commences asynchronously at a rate of 50×10^3 16-bit words per sec, although rates of 260×10^3 words per sec are possible using a DMA channel. Input interrupts inform the DDP-516 of current data transfer status, or IBM360 status or that data for the DDP-516 is awaiting collection at the IBM1800. A priority structure set up within the DDP-516 allows up to sixteen separate jobs to use the facilities of the IBM360.

As an example of the use of the data-link, the application can be described of an analogue voltage multiplexer which is used to scan up to 750 DC lines throughout the experimental system. A digital voltmeter (DVM) measures voltages presented to

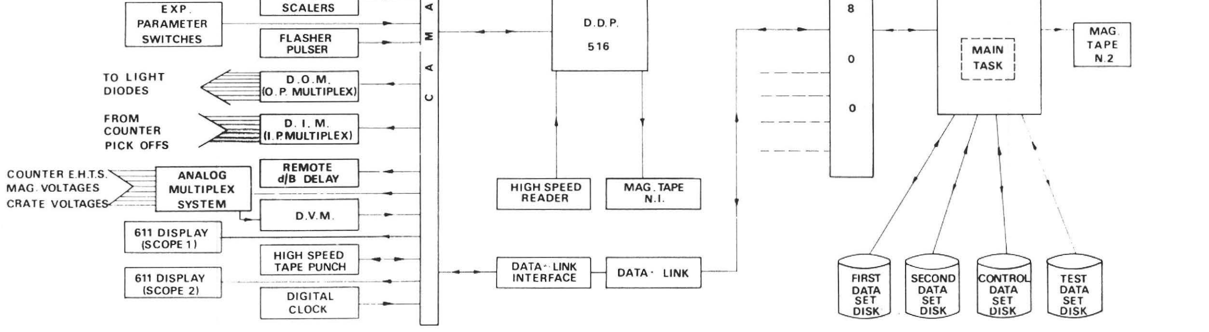


Fig. 3 PEP Data-Handling System

it by the CAMAC controlled analogue scanner (EC250). The DVM presents BCD data to a DVM interface (EC311) and the voltages are read and buffered under JOBQ control. Data sent to the IBM 360 is compared against a list of correct voltage settings held on disc. Out-of-limit voltages together with the correct setting are returned and listed at the DDP-516. It is possible to make a complete scan of the system in under two minutes. Manual interruption of the analogue scanner driver permits corrections to be made off-line to errant channels.

CAMAC is used extensively for the purposes of checking scintillation counters. Each counter is fitted with a light diode and output signal pick-off point. The light diodes are driven by multiplexing, under CAMAC control, the output of a common avalanche pulser. Similarly, a selected signal pick-off may be routed by means of an input strip line multiplexer to a common monitoring system interfaced to CAMAC.

CAMAC SOFTWARE

Contrary to more recent CAMAC practice, the controller used did not provide for interrupting during two part CAMAC operations, viz. (1) set up NAF code (2) read/write data. Consequently CAMAC operations had to be software inhibited which resulted in inefficient core usage. It was decided, therefore, to compromise by using simple CAMAC utility routines, shown in Table I, which although they doubled execution time, led to comparative ease of programming and saved valuable core space. Similarly, the absence of controller crate registers led us to use utility routines for changing and then memorising the current operational crate.

Table I CAMAC Utility Routines

Name	Function
ICAM	CAMAC READ OPERATION
OCAM	CAMAC WRITE OPERATION
CONCAM	CAMAC CONTROL FUNCTION
QCAM	TEST CAMAC Q RESPONSE
SECX	SET CRATE X (X = 0, 1, 2 or 3)

The first four of these routines are entered with the OCTAL NAF code in the location following the 'CALL'.

```
viz. CALL  SEC1   Set CRATE 1
     CALL  ICAM   Read & Clear register
     OCT   3142   N = 3; A = 3; F = 2
     STA   BUFR   Store data
```

The CAMAC utilities described are never interruptable and may therefore be used in the background as well as at all levels of interrupt programming. An important advantage is that they are real-time orientated and might be used to improve the efficiency of CAMAC interpretative languages in future real-time systems. Their use in the present system has led to some degradation of its real-time capabilities but this was acceptable experimentally.

Wherever increased CAMAC execution times have been tolerable we have used the CAMAC utilities but on two occasions this has not been feasible:

(1) Reading of 50 word CAMAC event data block.
(2) Transfer of 250 word data blocks to and from the IBM 360.

Both of these operations will shortly be executed under DMA control. At the same time a Branch Highway using type 4600 controllers and a new DDP-516 controller will be installed to replace the current non-standard system. With a little alteration the utility software will be adapted to conform to current CAMAC practice. Moreover because of the general use of CAMAC utilities it will be possible to accommodate these hardware modifications with a minimum of alterations to the PEPER software.

SYSTEM CONTROL USING CAMAC

The concept of CAMAC has relieved us of much of the burden of producing specialised control hardware. Switches, push-buttons, indicator lamps and input-output gating functions are interfaced directly to the computer via CAMAC. Special control hardware has in fact been replaced quite satisfactorily by software modules.

In the event of catastrophic CAMAC failure the experimenter is prevented from taking data until the fault is rectified. If CAMAC is reliable then its use for control functions serves to build up confidence in the overall system. If CAMAC is not reliable enough to support control logic then effort must be expended to correct the matter, either by improving operating conditions or by writing suitable on-line diagnostics.

CAMAC control software uses far less core space than a compatible teleprinter language. For instance one 16-bit word may be used to flag up to 16 standard output messages on a labelled control panel. In addition there is the benefit of improved response time. In the PEPER system, the teleprinter is reserved for important error messages as well as providing hard copy of experimental parameters and conditions for the log book.

SOME ASPECTS OF CAMAC RELIABILITY

The CAMAC system described has proved extremely reliable over a two-year operational period, although several possible areas of failure have demanded constant attention.

In order to keep CAMAC modules working at low ambient temperatures the system was run in a well ventilated environment. Power supplies were situated separately in a similar environment. Besides reducing the ambient temperature of CAMAC, this arrangement enabled faulty power supplies to be changed easily without disturbing CAMAC modules.

This policy of non-disturbance together with continuously powering the system for long periods even when not in operational use, we feel sure has contributed greatly to the excellent operational reliability.

Testing of modules in situ may be effected using simple CAMAC on-line diagnostic routines executed under JOBQ control. More exhaustive tests can be made by removing a suspect module to a TEST crate fitted with a dynamic test controller. This controller has not yet been used to replace the computer for system testing. Simple input switch/output lamp equipment has proved invaluable for testing CAMAC input-output module functions in situ.

Occasionally, faulty modules or intercrate cabling have led to CAMAC data lines becoming permanently set, reset or wire-ORed with adjacent lines. To prevent this type of fault from corrupting data it was necessary to run an on-line diagnostic every 10 mS which checked inter-crate read-write consistency, bit by bit. This diagnostic took 100 µs to execute under JOBQ control and, upon detection of an error data acquisition was inhibited immediately. The procedure for locating the fault has been somewhat unsatisfactory. After locating the faulty crate by working outwards from the master-crate, it was then necessary to remove each module in turn in that crate until the fault was found. However a diagnostic for use under these circumstances has been written. This diagnostic is designed to trap errors which occur due to faulty scaler registers. A fault of this type usually disappears when the register is reset upon initialisation. The routine clears and then increments registers under computer control (F25). The fault is located as soon as non-zero data is read from an empty CAMAC station. The teleprinter is used to print the station and sub-address of the offending register.

CONCLUSION

Extensive use of the CAMAC system together with a simple, yet flexible, approach to system software has led to a system whose power has exceeded initial expectations.

ACKNOWLEDGEMENTS

The authors are grateful to members of the Computer and Electronics Group at Daresbury for the many services provided for the PEP experiment, to members of our own group for discussion of our application, to Dr. D. Braben for his encouragement and to Dr. D. Botterill for his work on the IBM 360 on-line programs. In addition the authors wish to thank P. Salvadori (University of Pisa) and A. E. Groome for their help in commissioning the system.

3

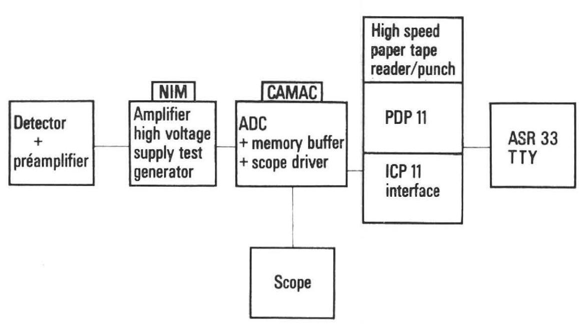
NUCLEAR SPECTROMETRY

by

J.M. Servent

SAIP-CRC Schlumberger, Malakoff, France

SUMMARY To illustrate some interesting features of using CAMAC with an on-line computer, SAIP-SCHLUMBERGER has developed an experimental system for nuclear spectrometry. This system and its software are not the most sophisticated, many other improvements can be provided but they fill the main function encountered in the nuclear spectrometry field.



DESCRIPTION OF THE SYSTEM

Analogue Treatment

This part of the system is classical; it comprises a linear amplifier, a high voltage supply and a test generator (in NIM standard) associated with a charge-sensitive pre-amplifier. The detector is a true coaxial Ge Li and the FWMH is 2.5 KeV with 8% efficiency and a Peak/Compton ratio of 25.

CAMAC Modules

The CAMAC modules are:

- A high performance analogue-to-digital converter, model JCAN 20+JCAN 20H (4/25+2/25), 8192 channels and 100 MHz clock frequency. The conversion time is $(15+N\times0.01)$ µsec, where N = channel number.
- A memory buffer with 256 × 16-bit words capacity, model JMT20 (1/25).

— Three service modules (1/25 each) to drive a memory display.
— A crate controller type A, model JCRC 50 (2/25).

Computer and Interface

The computer is a PDP-11/20 with 8 K × 16-bit memory and arithmetic extension. The CAMAC PDP-11 interface (ICP 11) is constructed in a PDP-11 standard 'System unit' and is located in the computer itself. This interface can work in programmed mode, in normal direct memory access mode (NDMA) for block transfers and in automatic direct memory access mode (ADMA) for data transfers by scanning. The PDP-11 is also equipped with an ASR 33 Teletype and a high-speed, paper-tape reader and punch.

Data Acquisition and Processing

In the computer, 4 K memory are reserved for spectrum storage. Data acquisition is made as follows:

The ADC fills the 256 words of memory buffer. When filled, the buffer sends a LAM to the computer. This high priority interrupt starts a NDMA operation to transfer the 256 words block into a reserved location of the computer memory. The transfer is executed in 500 µsec. The buffer and ADC are then acknowledged and the computer effects the +1 operation in the addresses contained in the 256 data block. After that, the spectrum is displayed until a new LAM appears. When the experiment is started, the computer asks for information via a teletype:

— Location of the CAMAC modules.
— Preset count.
— 8 K or 4 K storage (in the 8 K storage case, two adjacent channels are stored in the same memory address).
— Starting channel of the 4 K to be stored among the 8 K channels coded by the ADC.
— Zone to be displayed.

After calibration with a radio-active source of known energy, an unknown spectrum can be analysed.

When the preset count is reached, data acquisition is stopped and the computer outputs onto the teletype the channel number, the energy and the FWMH of peaks selected by two bright points on the scope. It is also possible to get a listing of channel numbers, between the two bright points on the scope, with their contents and energy.

For the spectrum display on the memory scope, the user can continuously select the memory zone he wishes to display and the horizontal and vertical scales.

Other programs for background subtraction, peak areas and automatic peak search will be available shortly.

ADVANTAGES OF USING CAMAC

The realisation of a nuclear spectrometer in CAMAC offers many advantages. In comparison with a classical PHA, direct access to a computer confers much more power and versatility. The user can always modify and extend his equipment and the corresponding software. At his disposal is a great choice of standard modules with the inherent advantages of standard equipments i.e., reliability, short delivery and low prices.

NEWS

CAMAC ACTIVITIES OF THE 'DEUTSCHE STUDIENGRUPPE FÜR NUKLEARE ELEKTRONIK'

The Deutsche Studiengruppe für Nukleare Elektronik (German Study Group on Nuclear Electronics) is an association of representatives from German research institutes and universities, which are responsible for instrumentation problems in nuclear physics and other experimental establishments. Twice each year the Group meets for two days to exchange experiences and information. Manufacturers of equipment and components are also invited to the meetings. Papers are presented but care is taken to allow enough time for discussions and for personal contacts to be made.

For several years now the Group has discussed the application and development problems with CAMAC.

During the last meeting (15th–17th March, 1972), several papers concerning CAMAC were presented To some extent, short versions of these papers might appear in the next issue of this bulletin. The presented papers are:

'CAMAC-Statusbericht' by H. Klessmann, HMI, Berlin.

'Zum Stand der CAMAC-Spezifikationen Analoger Signale' by O. Fromhein, GfK, Karlsruhe.

'CAMAC-Crate-Controller 320, Anpassung des CAMAC-Dataway-Crate an den Siemens Prozebrechner 320' by H. Stiehl, Siemens.

'Funktionstest des Induktions-spulenexperimentes der HELIOS-Sonnensonde unter Verwendung des CAMAC-Systems' by G. Schirenbeck, Institut f. Nachrichtentechnik der TU Braunschweig.

'CAMAC bei Digital Equipment' by P. Reisser, Digital Equipment GmbH.

'CAMAC-Module neue Entwicklungen' by W. Heep, T.G. Ottes, GfK, Karlsruhe.

'Vorstellung eines n-aus-4-Koinzidenz-Moduls in CAMAC-Ausführung' by H. Krug, Fakultät für Physik, Freiburg.

'Software-Aspekte zur 'schnellen' Datenerfassung mit einem CAMAC-System (DEC-CAMAC-I/O-Processor CA-15)' by D.J. Franz, Fakultät für Physik, Freiburg.

'Die Entwicklung eines CAMAC-Betriebs-systems' by T. Schlurick Physikalisches Institut, Erlangen.

ESONE ANNOUNCEMENTS

ESONE Annual General Assembly and CAMAC Exhibition 1972

The 1972 ESONE General Assembly will be held at the Kernforschungsanlage Jülich, West Germany. The programme will start on Tuesday morning, 3rd October, and continue until Thursday, 5th October.

An exhibition of CAMAC systems, equipment and components will be organised during the assembly on October 3 and 4 from 9 a.m. to 7 p.m. at the same place.

Everybody interested in CAMAC is invited to attend the meeting and to visit the exhibition.

Agenda of the Assembly

*Tuesday**, October 3

Morning (9 a.m. – 1 p.m.)

— Opening of the meeting.
— Review of ESONE activities, 1971/72.
— General Information and discussion.
— Presentation of new ESONE members.

Afternoon (2.30 p.m. – 7 p.m.)

— Status reports, Mechanics and Dataway Working Groups with discussion.
— Session of ESONE Committee members

*Wednesday**, October 4

Morning (9 a.m. – 1 p.m.)

— Status report, Software Working Group with discussion.
— Session of ESONE Committee members.

Afternoon (2.30 p.m. – 7 p.m.)

— Status report, Analogue Signals Working Group with discussion.
— Status report, Information Working Group with discussion.
— Session of ESONE Committee members.

Thursday, October 5

*Short presentations on CAMAC activities***

— Developments and applications by laboratories and manufacturers.
— Industrial applications of CAMAC and associated problems.

Concluding session with discussion

Booth reservations for the exhibition should be made by CAMAC manufacturers before September 1. 25 companies have already reserved their booth. There will be no charge for exhibitors who may also invite interested people on their own for the exhibition.

Participants requesting hotel reservation should write to the address below before September 15.

* The time schedule during the meeting will reserve sufficient time to visit the exhibition.

** Original papers are invited for oral presentation (10 min); short summaries should be sent before September 15

Address for paper submission and reservations:

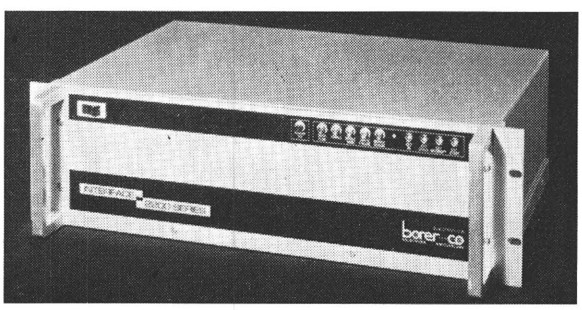
K.D. Müller
K.F.A. Jülich, ZELNE
517 Jülich, Germany
P.O. Box 365; Tel. No. 02461 – 616522

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

BORER & CO has developed Branch interfaces for coupling CAMAC systems to Hewlett Packard and Digital Equipment computers respectively.

The interface units are built into standard Borer 2200 Series cases.



1. HP COMPUTER-CAMAC INTERFACE

Interface Type 2201 provides a very efficient and flexible means of coupling any CAMAC system configuration, containing up to seven crates, to a Hewlett Packard 2100, 2114, 2115 or 2116 computer.

The Interface, housed in one standard Borer 2200 Series case, is fully modular throughout, permitting each instrument to be tailored to the application. Each section of the Interface is constructed on a separate plug-in circuit card and all interconnections made through a base-board/dataway.

Connection between the Interface and the computer is made through a buffer card in each of two 10 slots in the computer.

Every operation in which the Interface is used is carefully supervised to ensure that no non-valid commands, false arrangements or system failures can occur unnoticed.

Programmed Data Transfers

Every Interface contains a 24-bit input/output buffer memory, address register (for C, N and A), a function register and sufficient administrative circuits to ensure correct timing and to detect errors.

Additionally, module-to-module data transfers can be executed without using any memory capacity in the computer.

Automatic Transfers (optional)

Transfers in either a Block Transfer or an Auto-CNA mode can be executed with optional additions to the Interface.

2. DEC COMPUTER-CAMAC INTERFACE

Interfaces Types 2202 and 2203 provide a very efficient and flexible means of coupling any CAMAC system configuration, containing up to seven crates, to a PDP9 or PDP15 computer respectively.

The Interface, housed in two standard Borer 2200 Series cases, is fully modular throughout thereby permitting each instrument to be tailored to the application but with the possibility of extension and/or modification at a later date. Each section of the Interface is constructed on a separate plug-in circuit card and all interconnections are made through a base-board-dataway.

Connection between the Interface and the computer is made through a single 10 Bus Cable as for a normal peripheral.

Programmed Data Transfers

Each Interface contains a 24-bit input/output buffer memory, address registers (for C, N and A), a function register and sufficient administrative circuitry to ensure correct timing and to detect errors. Additionally, module to-module data transfers can be executed without using any memory capacity in the computer.

Automatic Transfers (optional)

Transfers in ‚block Transfer' or ‚Auto-CNA' modes can be execute dwith optional additions to the Interface.

4

THE COMPUTER SYSTEM OF THE HARWELL SYNCHROCYCLOTRON GROUP

by

Dr. C. Whitehead, Dr. O.N. Jarvis and Dr. A. Langsford

A.E.R.E., Harwell, U. K.

SUMMARY A direct-access multi-user system (DAMUSC) allows data collection from several independent nuclear physics experiments, using a single central computer and multiprogramming techniques. The experiments are interfaced through CAMAC in each of the remote counting rooms. These CAMAC crates are connected to a CAMAC system-crate in the computer room by parallel highways. User programs are supported by OLERT—an on-line real-time executive—with user coded modifications to take account of CAMAC hardware and the extensive use of magnetic tapes.

INTRODUCTION

A Direct-Access Multi-user system (DAMUSC) has been provided to ease data collection problems for nuclear physics experiments performed on the Harwell 110ins. Synchrocyclotron. The important features of the experimental environment, in which this system is required to operate, are as follows:

(i) Experimental requirements change frequently. Experiments take accelerator time on a roughly week-by-week basis though a few experiments are of shorter duration. Longer duration experiments are broken up into a series of weekly runs. In some cases two experiments can be proceeding simultaneously.

(ii) Not only is the computer system required for data taking during an experimental run, but also when setting up an experiment, since the computer and its interfaces form an integral part of that experiment. Similarly the system is required for re-analysis of data taken during experiments.

(iii) Very few resident members of the Synchrocyclotron Group or members of visiting teams are expected to have a detailed knowledge of this system. However, most have programming experience of 'number crunching' problems, mainly coded in FORTRAN. They are not expected to code assembly language programs for a system with which they are unfamiliar.

(iv) Because there is a frequent change of experiments there is a steady program-preparation load which involves the compilation and testing of new software.

From these considerations it was decided to provide a moderately powerful system with a single central processing unit, which would service a number of independent demands using multi-programming techniques.

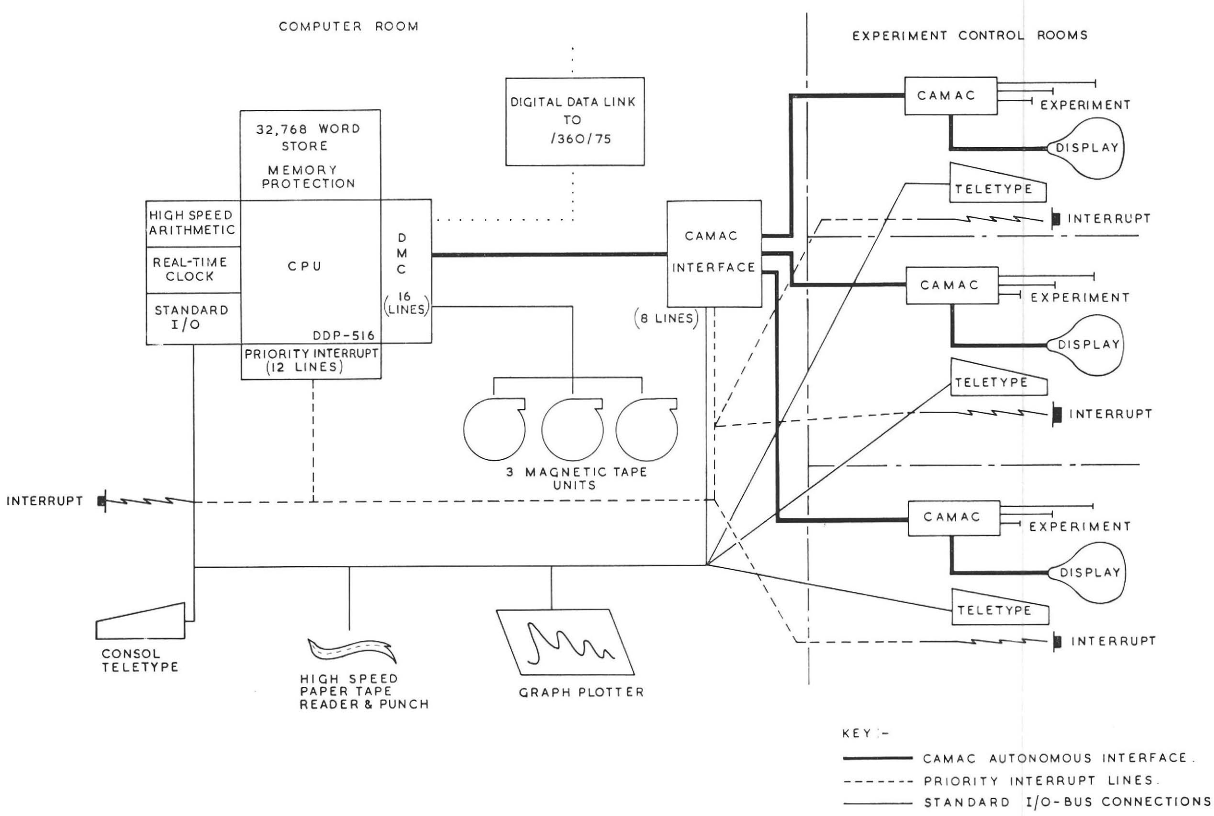


Fig. 1 Schematic of Total System

A Honeywell DDP-516 computer system was chosen, the hardware interface to experiments being built up from standard Harwell 7000 Series units in a multicrate CAMAC system. The user programs are supported by the Honeywell 'On-Line Executive for Real-Time' (OLERT) with user coded modifications to take account of CAMAC hardware and the extensive use made of magnetic tapes. A schematic diagram of the system hardware is shown in Fig. 1.

The organisation of the CAMAC crates in the present system is shown in Fig. 2. It consists of a single master-crate adjacent to the computer and five remote crates, driven over distances up to 50 m. These slave-crates are driven in parallel from the master-crate but each slave-crate can drive further slave-crates in a tree arrangement provided that the total number of crates within the system does not exceed eight.

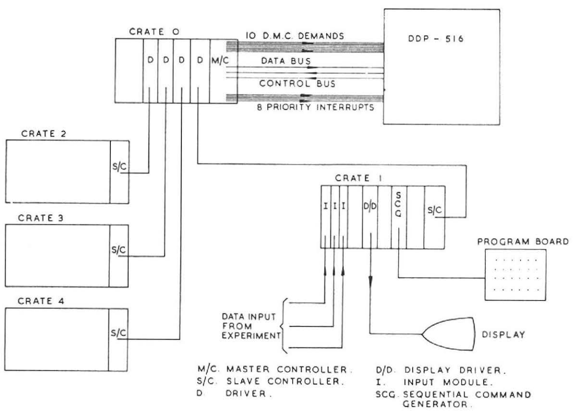


Fig. 2 Typical CAMAC Interface in Experimental Room

CAMAC modules communicate with the computer either by program-controlled input/output through the accumulator of the CPU, or by generating an interrupt which is received by one of eight priority interrupt lines (one allocated to each crate), or by a direct store (autonomous) transfer via a DMC channel (the system supports 10 such channels). The CAMAC commands that control a direct (DMC) transfer are set up within CAMAC using a local instruction store (a diode-pin plugboard in the present system). The unit which controls these direct transfers (Harwell Series 7037 Sequential Command Generator) plays an important role in the present system. Its hardware organisation is such as to recognise that the CPU is signalling the end of a series of transfers to or from core thus allowing transfers to be terminated by hardware means. The sequential command generator can also be used to execute CAMAC commands in response to an interrupt from a module and to store the source of the interrupt for CPU interrogation. In this manner, elaborate hardwired parallel processing can be achieved within CAMAC concurrently with CPU operation. Thus the user can generate application dependent hardware to match his software, without the need to modify the OLERT routines with special software peculiar to each experiment.

SYSTEM SOFTWARE

To carry out experiment-oriented tasks, specified by the physicist, calls for a series of real-time applications programs, each tailored to its specific task and supported by the facilities of the real-time executive. These provide program scheduling, interrupt handling, a system timer and clock and input/output facilities for various system peripherals and CAMAC modules.

To correspond with the three methods by which CAMAC hardware interacts with the DDP-516, there are three software facilities.

(a) Priority Interrupts are associated with user code, one interrupt per crate, so that users may activate core on the receipt of a crate interrupt and, having identified the interrupting module, carry out any desired operations.

(b) Standard CAMAC input and output commands can be carried out. Each crate is defined as a unique system peripheral which a programmer can ATTACH to his program to provide a degree of software protection. Transfers to and from the crates are made through INPUT and OUTPUT statements which are provided as extensions of FORTRAN READ and WRITE statements.

(c) Each autonomous channel is defined as a unique system peripheral. Transfers are initiated by executing an INPUT or OUTPUT statement dependent upon the direction of transfer.

THE SYSTEM IN USE

Twelve experiments have made extensive use of the system to date. The most straightforward experimental application is to multi-channel analysis, including options for data storage and retrieval through magnetic tape, graphic output and the mathematical manipulation of data. Other experiments have generated highly correlated data where each event is described by a number of data words from as many as fifteen different sources.

All these experiments have been run under the real-time operating system using a hierarchical structuring of program priorities to ensure that subsidiary data manipulating operations do not hinder the prime task of data collection. In general, it is not possible to make a full analysis of the data in real-time and the real-time analysis is restricted to validating the incoming data, followed by simple collation, display and archival storage. Real-time operator control is executed by teletype dialogue or through a special-purpose, push-button, panel that is read on demand through CAMAC.

For a more detailed description of the system, the reader is referred to the Harwell Report, No. AERE-R6832.

LABORATORY REVIEWS

CAMAC SYSTEMS AT THE ATOMIC ENERGY ESTABLISHMENT WINFRITH, DORSET (U.K.)

by

A.B. Keats and G.B. Collins

UKAEA
Control and Instrumentation Division
AEE Winfrith, Dorchester, Dorset, U. K.

SUMMARY The capability of two on-line computer systems using CAMAC interfaces at the AEEW is described. One is concerned with plant dynamic measurements, and requires occasional interface reconfiguration. The second is for the automation of a radiaoctive sample analysis laboratory controlled by a Honeywell H316 computer.

A third system is under development, in which a CAMAC interface is being implemented in parallel with an existing interface on a Ferranti Argus 500 computer. The architecture of the Ferranti-CAMAC dataway controller is outlined and its application described.

Two on-line computer systems employing CAMAC interfaces have been commissioned at AEE Winfrith, and three others are being assembled. The first, using a Honeywell H316 computer, is designed for on- and off-line plant dynamic measurements catering for special reactor pulse experiments as well as the more usual step, sine and binary cross-correlation test methods. Using a crate controller and, with one exception, standard Harwell '7000 series' plug-in modules, the interface shown in Fig. 1 has been assembled. This provides the following facilities:

(i) A 1 mS crystal controller timer, capable of accurately timing any computer set delay.
(ii) A source of actuator commands and multiplexer addresses for an external high speed ADC and multiplexer system.
(iii) An input data buffer for the ADC.
(iv) An output DAC for the sine-wave test mode.
(v) Analogue output signals for CRT display.
(vi) External interrupt handling.
(vii) Data buffering, drive and status encoding for a paper-tape punch.

The last item illustrates the freedom of peripheral device choice which arises when the user controls his own interface structure. The same paper-tape punch (which has a suitably low cost/speed rating) was not made available by the computer manufacturer through his own interface system for more than a year after the CAMAC system was operational. The whole system also demonstrates the ease with which it can be expanded as experiment requirements develop; it started with only 5 modules and now has a complement of 9. Each module can operate in the busy, test or interrupt mode as appropriate by simply changing a pinboard selector connected to the crate controller, which carries only those 'look at me' lines through to the computer interrupt line which are appropriate to the chosen mode of operation. The users' preferences for one or other mode of operation are not inhibited.

The second CAMAC system is used for the automation of a radioactive sample analysis laboratory which houses 10 automatic sample changers and their associated nucleonic instrumentation. Sequence control of, and data collection from, the

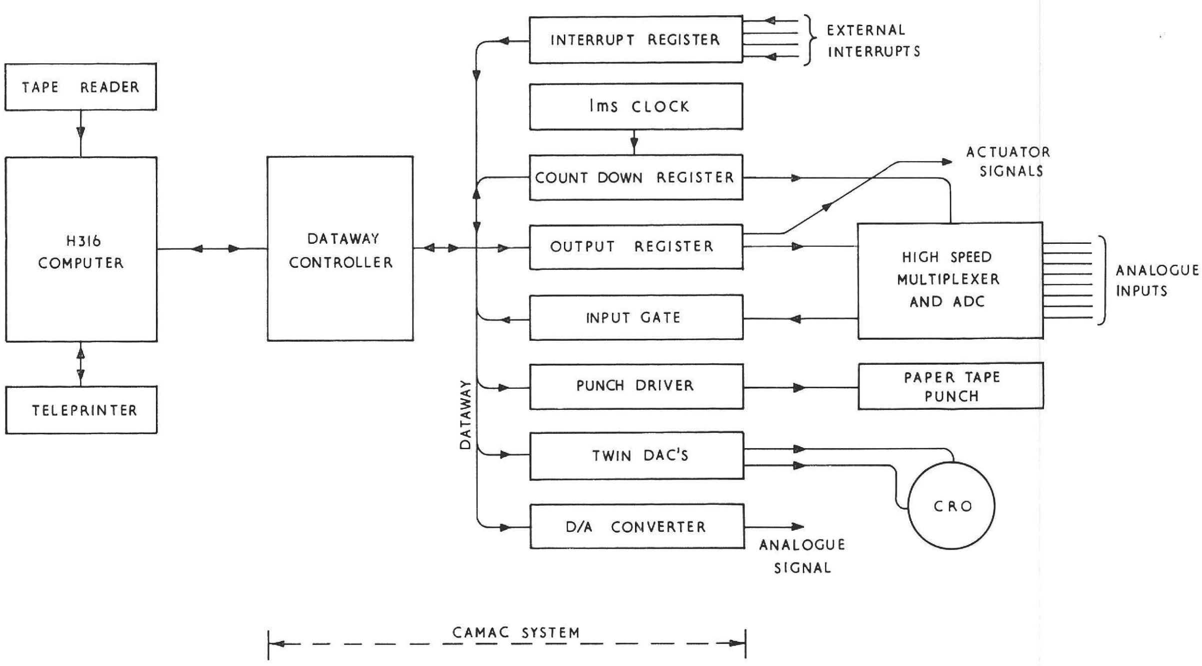


Fig. 1 Computer Interface for On-line Analyser

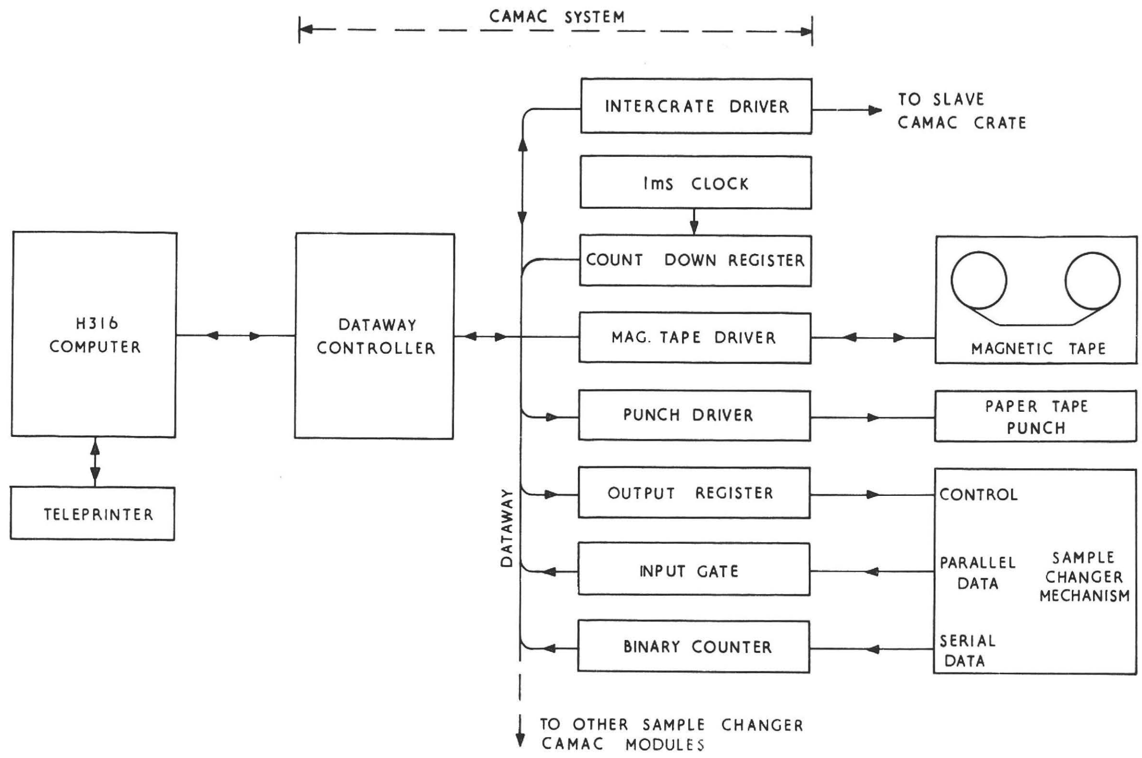


Fig. 2 Automation of Radioactive Sample Analysis Laboratory

10 sample changers is performed by a single Honeywell H316 computer interfaced as shown in Fig. 2. Standard CAMAC input and output modules occupying 2 crates provide the means of communication between the computer and the sample changers. Time sharing of the computer between the various functions is controlled by timed interrupt from a CAMAC crystal-controlled clock and countdown register. The processed output of the computer is recorded on computer compatible magnetic tape via a locally designed CAMAC module. A standby paper-tape punch is also interfaced using another locally designed CAMAC module, first designed for the dynamic measurement system. The facilities provided through the CAMAC system are as follows:

(i) A source of 20mS timing pulses which interrupt the computer.
(ii) A source of control commands to the sample changing mechanisms.
(iii) Parallel input of identity and status information.
(iv) Serial input counting and staticising of nucleonic pulses from photomultipliers, fission counters, etc.
(v) Input-output to computer compatible magnetic-tape handler.
(vi) Output to paper-tape punch.
(vii) Output to control 'watchdog' timer.

The principal advantage of the use of CAMAC in this application is not so much its flexibility as the availability of standard Harwell 7000 series modules which perform most of the functions required. This reduced the design and production of special hardware to the one new CAMAC module required to interface the magnetic-tape handler, and a series of very simple units which rationalise the inputs and outputs of the several different types of sample changer used in the laboratory.

The third application forms an extension to an older, locally-designed, reactor intrumentation interface on a Ferranti Argus 500 computer. The original interface system, designed in 1966, is now fully utilised and rather than perpetuate the original non-standard system by further expansion, it was decided to introduce a CAMAC interface to work in parallel with the existing system. As no crate controller existed for the Ferranti Argus computers, a design was evolved at AEE Winfrith. The architecture of the controller was influenced by the desire for software compatibility with the original interface and by the powerful addressing capability of the Ferranti Argus Interface 'A'. For this reason a specific Argus dataway controller is used rather than the ESONE Branch system with a standard crate controller. The full CAMAC specification is provided for with indirect addressing of up to 8 crates. The controller is 'transparent' to data in either direction, i.e., the 24 bit CAMAC Read and Write highways are linked directly to the Argus DIN and DO highways respectively under control of the appropriate commands.

The Argus computer interface 'A' uses a 12-bit address highway with octal addresses ranging from 0000 to 7777. The normal CAMAC addressing system requires 14 bits for the station address, subaddresses and function code, so a strategy has been evolved to reduce the number of directly decoded function code bits from 5 to 3, and to separately select the crate in use. The latter is achieved by adopting the convention that if the computer addresses are in a given range, then the address highway is not decoded to provide CAMAC station address or function information, but is used either to select the required crate or to preset F4 to 1 for the duration of the next instruction. Since F4 = 0 for all except non-standard and reserved function codes the penalty involved in using this special instruction will seldom be realised. Once a crate is selected it is held until an alternative crate is addressed. Finally the state of F16 is derived from the status of the I/O strobe signals from the Argus computer.

The resulting system is therefore one in which addresses 0 to 777 are allocated both to Ferranti and the original non-standard interface peripherals, 1000 to 3777 and 5000 to 7777 are true CAMAC addresses and functions, and 4000 to 4007 are crate addresses with 4100 used to preset the state of F4 to 1 when required.

The first application of this CAMAC system will be for reactor power spectrum measurement using parallel-plate fission chambers. This is a combined multiscaler and pulse-height-analysis measurement which can be implemented entirely with standard CAMAC modules, as shown in Fig. 3.

Two further CAMAC systems will come into use at AEE Winfrith in the near future. The first of these is an optical anisotropy measuring system based on a Nova 1200 computer. The second is a pulse-height-analysis system based on a PDP11 computer which forms part of a post-irradiation examination facility for power reactor fuel elements.

The CAMAC system for the on-line analyser has operated for 2 years with only one failure, due to poor connection between the crate controller and CAMAC dataway. It is noted that more recently produced crates conform to tighter mechanical tolerances which should completely eliminate this class of fault. Experience with CAMAC software suggests the creation of control pseudo-operations to perform common sequences such as: set up a command; output it to the dataway controller command register; input or output the data word being transferred from or to a particular crate address. Since these types of system operate in fixed word length form, with strict control of scaling and double length working only where necessary, it is convenient and economical to program them in a low level symbolic language, such as DAP-16 for the Honeywell computers. The assembly bottleneck which is liable to arise on mini-computers with low speed peripherals is avoided by assembling off-line on a larger computer system, and thus such modifications to the assembler could readily be made. The recommendations of the CAMAC software working group are therefore awaited with interest.

The automated laboratory application has been in use for about 6 months with no CAMAC failures so far. A noteworthy feature of this system is the ease with which it was commissioned. The availability of test modules, such as the Manual Dataway Controller, expedited this task and demonstrates a further advantage of using a standard interface system.

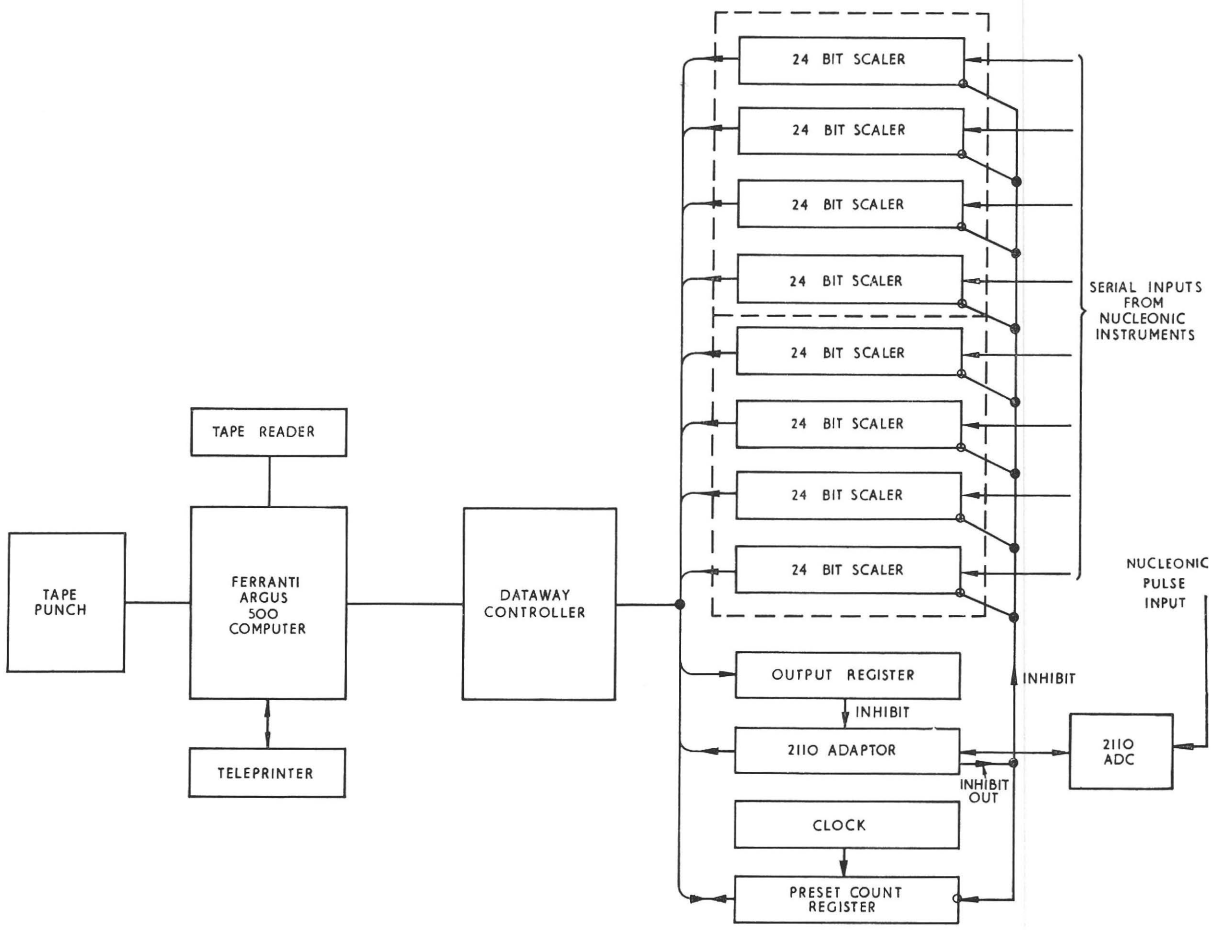


Fig. 3 Nuclear Reactor Experimental Instrumentation System

DEVELOPMENT ACTIVITIES

A SLAVE-CONTROLLER FOR CAMAC SUB-SYSTEMS

by
F. May* and J. Schwarzer**
Elektronik-Institut der Österreichischen Studiengesellschaft für Atomenergie,
Forschungszentrum-Seibersdorf, Austria

SUMMARY A programmable controller for an independent CAMAC sub-system is described together with an application which does not employ a computer. This controller can be installed in any station of the CAMAC crate and can use the Dataway during the time when the crate-controller does not. These CAMAC sub-systems may be used advantageously for control and/or data-handling systems which do not warrant the use of a computer, although connection to a computer is not precluded.

INTRODUCTION

To give an impression how a CAMAC sub-system can work, first of all a short description is given of the problem, which has been solved by designing a CAMAC sub-system (see Fig. 1).

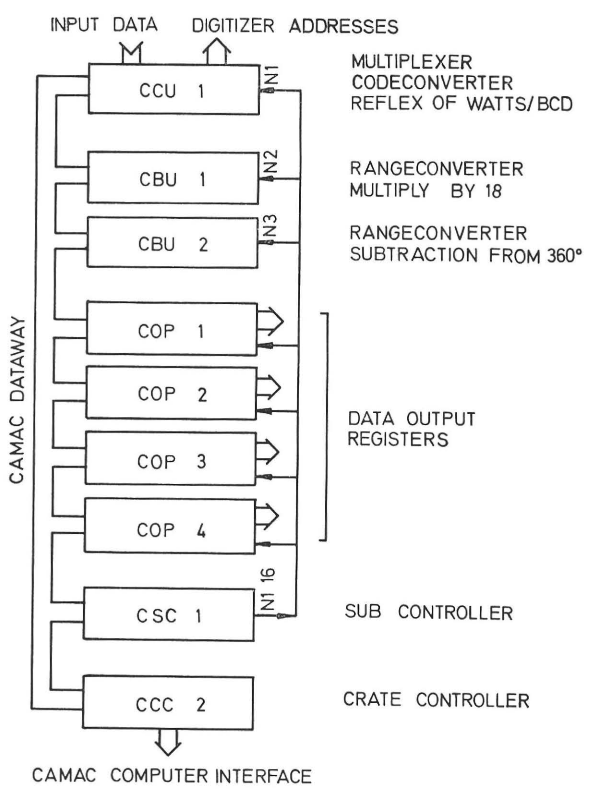


Fig. 1 CAMAC Sub-System for Triple-Axis Spectrometer

Four digitizers provide the actual position of four axes of a triple-axis spectrometer. The information is coded in the reflex-code of Watt. The least significant of the least significant decade represents the value of 0.018°. The outputs of the digitizers are connected to a common external databus and can be gated to this bus by calling the proper address-line of the digitizers. The data of the digitizers should be treated as follows:

(1) The information of each digitizer should be converted to a BCD-code (8, 4, 1, 2) (CCUl).
(2) The information should be converted to angular degrees (CBUl).
(3) Further treatment of the data is wanted, i.e., subtraction from a fixed number 360 (CBU2).
(4) The converted output of each digitizer should be stored in output-registers, one for each digitizer (COP1-COP4).
(5) The tasks 1 to 4, should be executed without computer.
(6) If a computer can be connected, it should be possible to use the same modules.
(7) The system should work independently if available stations in the crate are occupied by other CAMAC modules, which are controlled by a computer via a crate-controller or by another sub-controller.

It is obvious that the solution of the problem is rather simple, if the different modules can be controlled by standard CAMAC commands. The only problem is how to tell the sub-controller when the Dataway will be occupied by the crate-controller.

DESCRIPTION OF THE SYSTEM

It is assumed that the sub-controller is able to generate standard CAMAC commands accompanied by standard Dataway timing signals. In this case the program of the sub-controller can be described as below:

(1) WRITE sub-address A(0) into the multiplexer and code converter module CCU1. A(0) is stored in this module and the gate of the first digitizer will be opened. The information of the digitizer will be converted to BCD-code but is not stored within the code converter module.
(2) Read information from code converter module and store it in the sub-controller.
(3) WRITE this information into the next module (CBU1), which is the range converter (multiply by 18). The multiplication is done within 1 μsec or less.
(4) Read converted information (angular degrees) and store it in the sub-controller.

Further treatment of data (i.e., CBU2) can be continued until the proper result appears at the output of the last module, from where it can be taken and stored into the data output register belonging to the first digitizer (COP1).

The next step would be to address the next digitizer by sub-address A(1), etc. For this 'run' the

* Now with: Österreichische Elektrizitätswirtschafts AG.
** Now with: ITT Standard AG.

treated data will be stored in a second data output register (COP2), etc.

A complete cycle which stores the actual position of all four digitizers as angular degrees into four different output registers (COP1-COP4) lasts about 600 µsec, i.e., every 600 µsec new data of a digitizer will be available.

Since the maximum speed of any from the four axis is 10°/min, any indicated position of the digitizer is sampled nearly 200 times before changing to the next value.

THE SUB-CONTROLLER

A block diagram is given in Fig. 2. An astable multivibrator is used as clock-pulse generator. A J-K flip-flop is used to synchronize start-stop commands (F26, F24 or manual) with the clock-pulse generator. Using a second flip-flop, the clock-pulses are split into CP1 and CP2. CP2 is used to start the CAMAC

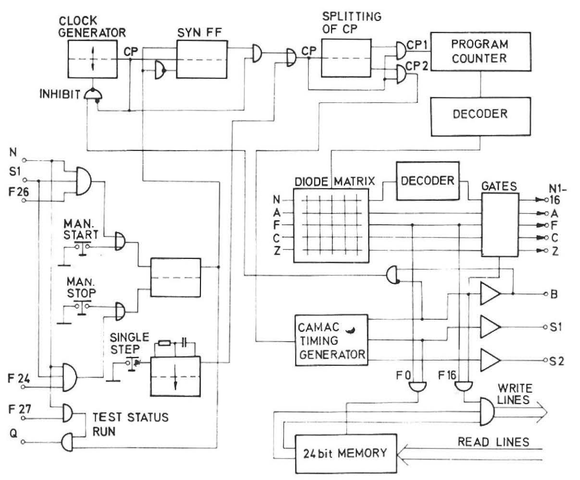


Fig. 2 Schematic for Total System

timing generator, which occurs between every step of a program counter which is driven by CP1. The program counter is able to count up to 32. The output of the program-counter is fully decoded from two 4-bits to 1 out of 16 decoders. By a diode matrix each output can be connected to generate N, A, F or CLEAR and INITIALISE which may be desired for a definite step of the program-counter. N appears like A and F as a binary number and has to be decoded again. One line of the diode matrix can be used to set the program-counter to zero and this gives the possibility of adjusting the number of steps done by the program-counter.

The sub-controller can be also controlled manually step-by-step. This feature is highly suited for test purposes, or sequential control systems. In addition the sub-controller can accept commands Disable and Enable (F26, F24) generated by a standard crate-controller and are interpreted as stop and start by the sub-controller. In this case the sub-controller cannot be placed at the control station and the N lines for the modules must be wired via an additional connector at the rear of the sub-controller. For each module which is controlled by the sub-controller, one patch-point at the module station is used for N. (Wired OR with normal CAMAC N line.)

TIMING OF DATAWAY SIGNALS

The sub-controller generates the standard CAMAC timing signals, where Busy is accompanied by S1 and S2. If the crate-controller generates Busy, the clock-pulse generator of the sub-controller is stopped for the duration of this signal (see Fig. 2) but the current CAMAC Dataway timing pulses of the sub-controller are not influenced by it (Fig. 3).

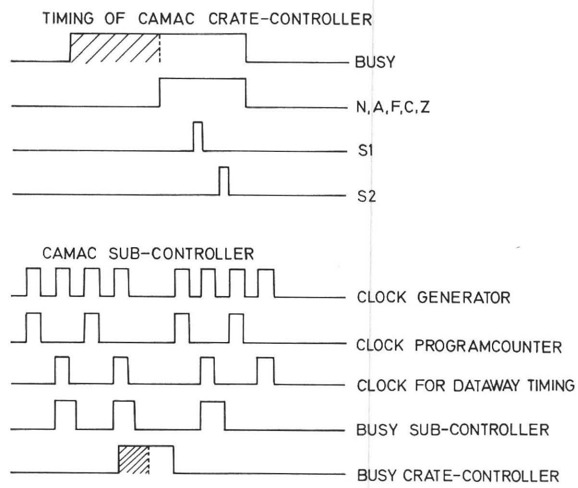


Fig. 3 Timing of Dataway Signals

A Busy signal which is generated by the sub-controller does not stop the clock-pulse generator, because the sub-controller 'knows' that Busy has been generated by itself (Fig. 2).

To avoid a simultaneous Dataway operation of the sub-controller and the crate-controller, the crate-controller must generate Busy at least 1 µsec before opening the gates for other signals on the Dataway including S1 and S2 (Fig. 3).

Since the duration of the Dataway signals generated by the sub-controller is not longer than 1 µsec, and the clock-pulse generator of the sub-controller is stopped by the Busy signal of the crate-controller at least one µsec before the Dataway is used by the crate-controller, a simultaneous Dataway operation by the crate-controller and the sub-controller can not occur.

As mentioned above, two or more sub-systems can work 'simultaneously' within one crate. In most cases the Dataway of a crate is occupied by one controller only for a small percentage of the time available. The timing and priority problem can be solved by ways similar to that described for a crate-controller sub-controller system.

2 DIRECT CONNECTION OF CAMAC CRATE CONTROLLERS TYPE 'A' TO THE PDP-11 UNIBUS

by

W. Stüber

Euratom CBNM, Geel, Belgium

SUMMARY Standard Crate Controllers Type 'A' can be easily interfaced to a PDP-11 computer using an interface between the UNIBUS and CAMAC branch for only those signals which are not compatible. The number of incompatible signals is kept low by using some of the UNIBUS address lines as CAMAC F-code lines. The method described is mainly of advantage for small CAMAC systems but can be extended to large systems.

INTRODUCTION

Looking at the CAMAC-branch specification[1] the reader will soon realise that this standardisation is quite adequate for large computer-based data acquisition systems, but might be expensive for small systems. Therefore another approach may be more economical, using special crate controllers rather than a typical CAMAC branch driver[2].

If the computer is a PDP-11 (Digital Equipment Corp.), an intermediate solution is possible. Obviously, many of the PDP-11 UNIBUS-signals[3] have equivalent counterparts on the CAMAC branch. So it is possible to connect the standard Crate Controller Type 'A' directly to the UNIBUS using a special interface between the CAMAC branch and UNIBUS for those signals only which are incompatible.

INTERFACING CONSIDERATIONS

Branch signals which have no counterparts on the UNIBUS are mainly the 8 highest data-bits, the function code bits, and the Q-response. It is common practice to store these bits in special registers, which can be read, or set, by extra program steps. Assuming that only small CAMAC systems are involved, some simplifications can be made. If only modules with not more than 16-bits are used, the register for bits 17-24 can be discarded. If the computer is not equipped with maximum memory then lots of addresses will be unused and these can be made available for CAMAC. So it is possible to treat the CAMAC F-codes as 'sub-sub-addresses', which can be addressed directly from the UNIBUS address lines. This not only means that the function register can be avoided but also that each CAMAC module can be addressed directly and treated as easily as any memory cell on the UNIBUS. Thus the instruction ADD A,B will work if A or B or both are CAMAC registers. As the UNIBUS signal C1 is equivalent to function code bit F16, only the remaining 4 F-code bits must be connected to the address lines. There is some freedom in arranging the connections to the 16 UNIBUS address lines, but the following arrangement seems the most favourable although it does not result in the shortest possible sub-address-search routine.

CR	F	N	A	F
4, 2, 1	4	16, 8, 4, 2, 1	8, 4, 2, 1	2, 1, 8
2^{15}	2^{12}	2^{9}	2^{6} 2^{3}	2^{0}

The read-write bit F16 is automatically set by the processor in normal read or write operations. However, in CAMAC command operations with F8 = '1', F16 must be set by appropriate choice of the PDP-11 instruction. For example:

TSTB 160205; clear Look-at-Me of module 1, sub-address 0.

CLRB 167525; enable BD output of crate controller A.

Concerning the BQ line, the interface may connect this line to the UNIBUS data line D15, when the processor executes a TSTB instruction at a CAMAC address. In this manner Look-at-Me can be tested, but not Status, because the latter has been coded somewhat illogically with F16 = '1'.

So far things look very simple, but some complication is caused by the fact that CAMAC timing and UNIBUS timing are different, i.e., BTB and SSYN are not equivalent. A simple way to overcome this problem will be shown elsewhere[4]. Anyhow, an interface for connection of one crate to the UNIBUS has been built with only 7 integrated circuits, and only slightly more are needed for more crates.

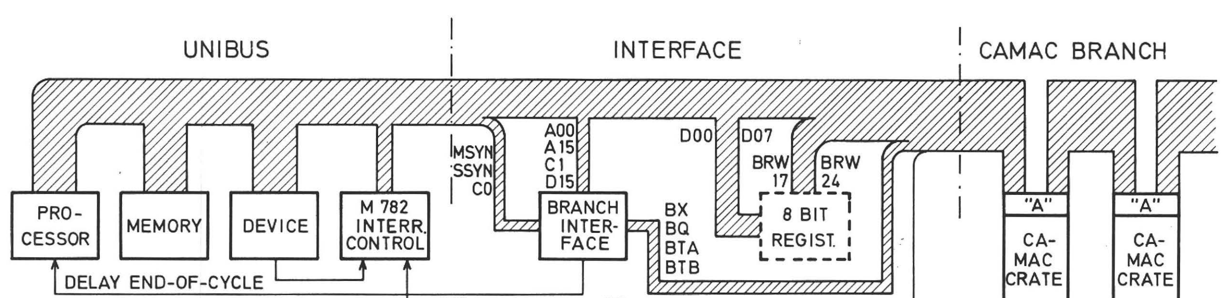


Fig. 1 Connection of Crate Controllers 'A' to the UNIBUS

Interrupts can be generated in the usual way via M 782 interrupt control cards. If the interrupt need not be fast, it is possible to trigger an interrupt search routine with branch demand BD, to read and evaluate the Graded-L signals[4]. This is shown in Fig. 1, which gives a block diagram of the interfacing discussed.

With the addressing scheme proposed, a crate needs 4k bus addresses; thus the system configuration can be varied between 28k memory + 1 crate and 4k memory + 7 crates. Driving the seldom-used F4 line by a program-loaded flip-flop would halve the number of bus addresses per crate. If this is not sufficient, an additional register can be used for F code or crate address. The latter would be preferable because, normally, the crate address is changed less often than the Function code. The crate address register can be pre-loaded with the decoded crate address(es) as well as with a branch address and, say, 4 Control and Status bits besides the F4 bit. This addressing scheme would allow 16 CAMAC branches, with 7 crates each, to be served via the 2k unassigned and user device addresses of the PDP-11. Thus the computer can be equipped fully with 28k memory and all possible DEC-devices.

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1. *Manuscripts should be typed on alternate lines, on one side of the sheet.*
2. *Papers should be about 1200-1600 words, with a maximum of 2000 words, or 3 pages including illustrations.*
3. *The preferred language is English; papers in other languages will be published without translation.*
4. *Follow as closely as possible the style used in this issue of the Bulletin fot the title of the paper, name of the author, his business affiliation, city and state, layout of headings, and the use of bibliographic references.*
5. *Each paper should be accompanied by a summary (abstract) for translation into other languages. The text should therefore be as short as is consistent with clarity.*
6. *Drawings: supply original ink (not pencil) drawings.*
7. *Photographs : supply semi-mat prints at least twice the final size.*
8. *Write the author's name and the figure number lightly in pencil on the back of each illustration.*
9. *List all captions with figure numbers on a separate sheet, even if they are given in the text or on the illustrations.*
10. *Papers which are a shortened or adapted version of an original paper, should identify the original in the references.*

NEWS

CERN CAMAC NOTES

CERN CAMAC Notes are intended as a flexible and informal link between designers, users, manufacturers.

Copies of these Notes can be obtained on request from:

Mr. J. Halon, N.P. Division, CERN
1211 GENEVE 23, Switzerland.

Some 'typical' Notes are:

Note No.		*Year*
1-00	CAMAC CERN NP-Options	1968
8-00	Pattern A	1969
9-00	Parameter A	1969
11-00	Miniscaler	1969
12-00	Bin. Display	1969
13-00	Bin. to Dec. CVTR	1969
15-00	Preset Scaler	1969
16-00	Microscaler	1970
19-00	SCRO (Spark Chamber Read-Out)	1970
23-01	CAMAC Product Reference (New Edition)	1972
25-00	Introduction to CAMAC	1971
26-00	LAM Grader	1971
27-00	HP-CC	1971
28-00	DAC	1971
29-00	DAC	1971
31-00	CERN NP-Type 057 Interfaces and their use	1971
32-00	Pattern B	1971
33-00	2 IN-Register	1971
34-00	Branch Test Box	1971
35-00	Branch Selector Unit	1971
37-00	Branch Mixer Unit	1971
38-00	CAMAC Timing with Spec. Ref. to CCTR.	1971
39-00	DOR Decoded Output Reg	1972
40-00	Autonomous Transfer Controller for PDP-11	1972

ACTIVITIES OF THE CAMAC WORKING GROUPS

The ESONE Committee in Europe and the USAEC NIM Committee in America have both authorised different working groups to investigate specific aspects of CAMAC. The European and American working parties are performing their activities in close collaboration.

ESONE-CAMAC WORKING GROUPS

Dataway Working Group

Chairman: H. Klessmann, HMI, Berlin

The ESONE Dataway Working Group reached agreement on the *final* text of the revised 'Dataway' document at a meeting held in April 1972. This was achieved by close co-operation with the ESONE Software Working Group and NIM-CAMAC Dataway Working Group.

After release by the ESONE Executive Group, the revised document will be published by the ESONE Committee as EUR 4100e (1972). In the United States, the AEC NIM Committee will publish an identical text, with references to the ESONE document, as TID-25875.

The future activity of the Working Group is now being directed into three major areas:

- Preparation of the supplementary notes to the CAMAC Specifications in response to a proposal from and with the co-operation of the NIM-CAMAC Dataway Working Group. This Supplement is intended to assist designers and users by interpreting definitions in the standard and giving specific examples of preferred practice for various problems.
- Consideration of a serial-branch transmission system which may be useful where long-distance transmission is involved, low data transmission rates can be tolerated and possibly where a simple Teletype port of a computer can be used to drive a CAMAC system.
- Evaluation of Multibranch- and Multisource-systems. Several proposals for operation of systems with more than one branch and/or more than one computer have been worked out by different member laboratories, Extensive discussion on this topic by the Working Group has not been possible because of the higher priority for completion of the revision of the EUR 4100 document.

Software Working Group

Chairman: Mr. I.N. Hooton, AERE, Harwell

The revisions of the CAMAC Language are now well advanced and it is expected that a Draft Proposal will shortly be presented to the Executive Group for authorisation to publish. This draft is intended to give all interested persons or organisations not represented on the ESONE and NIM-CAMAC Committees an opportunity to comment on the language.

A small study group has been set up to prepare the first working draft of the Intermediate Language (see Bulletin 3).

Collaboration with the NIM-CAMAC Software Working Group, on the basis of interchanging minutes and cross-representation, continues to prove extremely valuable.

Analogue Signals Working Group

Chairman: Dr. K. Tradowski: G.F.K. Karlsruhe

The NIM Analogue Signals W.G. has made a proposal for an extension of the Specification of Amplitude Analog Signals (to be published as EUR 5100) for Broadband Amplitude Analogue Signals. This proposal has been discussed at the ESONE Analog Signals W.G. meeting at Karlsruhe from February 21-22. Our recommendations have been given to the NIM Analogue Signals W.G. meeting, February 29, at Washington D.C. It is hoped that a definite proposal will be available for the ESONE General Assembly in October.

Information Working Group

Chairman: Dr. H. Meyer, CBNM, J.R.C. Euratom, Geel, Belgium

The Working Group decided during its last meeting to add to future issues of CAMAC Bulletin a multilingual presentation of abstracts from papers published in the corresponding issue. Translations into English, French, German, Italian, Dutch and eventually Russian should be available.

NIM-CAMAC WORKING GROUPS

Introduction

Louis Costrell, Chairman NIM Committee

The NIM-CAMAC working group structure is similar to that of ESONE. The corresponding working groups are therefore able to consider CAMAC matters simultaneously on both sides of the Atlantic. In addition, there continues to be considerable direct contact between the European and North American working groups, with ESONE members participating in working group meetings in the United States and NIM members participating in ESONE working group meeting in Europe. This close cooperation has been of immense value in the development of the CAMAC specifications and in the utilization of CAMAC in numerous and diverse applications in many parts of the world.

All four of the NIM-CAMAC working groups met in Washington, D.C. February 28 – March 2. ESONE representatives at the meetings were K.D. Müller of KFA – ZEL, Jülich, Chairman of the ESONE Committee, A.C. Peatfield of DNPL Daresbury, and R. Kurz of KFA – ZEL, Jülich.

The working groups plan to meet at the National Bureau of Standards in Boulder, Colorado during the week of July 10 and in connection with the IEEE Nuclear Science Symposium in Miami Beach, Florida in early December.

Dataway Working Group

Chairman: F.A. Kirsten, Lawrence Berkeley Laboratory

This Working Group has been working closely with the ESONE Dataway Working Group on the revision of the Dataway specification. Our mutual objective has been that NIM and ESONE maintain identical CAMAC specifications. At our meeting in Washington, D.C., February 28 and 29, we were therefore pleased to be able to endorse and accept the revised CAMAC specification that resulted from a series of ESONE and NIM Working Group meetings. At this meeting, we were pleased to have as guests, from ESONE K.O. Müller and A.C. Peatfield. The presence of NIM and ESONE delegates at the others' meetings has been most helpful, particularly in the work of revising the Dataway Specification.

Several CAMAC users in the United States and Canada have been working with systems in which the crates are distributed over extended distances. In recent meetings, the working group has been examining these systems in order to determine whether further standardization in this area would be beneficial. The systems which have been discussed include:

a) Fully parallel balanced-to-unbalanced converter modules;
b) Completely serial command and data transmission; and
c) Various systems intermediate to the above.

The Working Group is also considering several proposals for the CAMAC Supplement that the NIM committee plans to publish.

Mechanical and Power Supply Working Group

Chairman: D.A. Mack, Lawrence Berkeley Laboratory

We have appreciated the opportunity of cooperating with the ESONE Mechanical Working Group on the revision to EUR 4100. We believe that the 1972 revision answers a number of questions that have arisen over the years.

Although at least 1,000 crates have been purchased in the U.S. and Canada, a large number were delivered without wiring or associated power supplies. The wide-spread application of CAMAC has been hampered by the difficulty of obtaining wired powered crates. This difficulty appears to be disappearing with the availability of wired crates and power supplies from several manufacturers in early summer.

Two jigs, one to facilitate the mechanical assembly of modules and the other to check crate dimensions and dataway socket alignement, have been designed and will be described in the CAMAC Supplement, Report No. TID-25877. Detailed drawings are available from Berkeley.

The suggestion for employing a color designation adjacent to panel coaxial connectors indicating signals levels has met with wide approval. Recommendations for the proposed signal-level classes are now under discussion.

Software Working Group

Chairman: Satish Dhawan, Yale University

At its meeting in March, the Working Group agreed on a general approach in specifying a standard CAMAC subroutine for performing CAMAC functions. Detailed specifications for a set of five subroutines are in preparation. Each meeting continues to be occupied, to a considerable extent, with a critical review of the CAMAC language syntax and semantics. The NIM-ESONE collaboration in this area has been very close, and it appears that the final form of the language will contain significant ideas from both sides of the Atlantic. The NIM SWG is also studying the problem of multitask scheduling features which it is felt should be defined and incorporated into the language at an early date.

Analog Signals Working Group

Chairman: D.I. Porat, Stanford Linear Accelerator Center

Specifications for broadband analog signals were formulated at meetings in Washington, D.C. and San Francisco in 1971 and were further developed by the ESONE working group. These specifications were reviewed and revisions were proposed by representatives from both sides of the Atlantic in a session held in Washington, D.C. on February 29. These are now being circulated for comment.

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

NUCLEAR ENTERPRISES can now supply a CAMAC Crate Controller 'A' (N.E. type 9016). This new unit has been developed in parallel with a programme, now being completed, to develop a PDP 11 computer to CAMAC interface and 'Branch Driver' System.

The 9016 conforms with the latest version of EUR 4600e and incorporates the following:

(1) Command registers to eliminate jitter on the N, A, and F lines.
(2) Gating of N, A, and F lines only when controller is on-line and addressed.
(3) Gating of R and W lines onto and from BRW lines only when required.
(4) Precautions against current loading of the branch highway in the absence of controller power.
(5) Maximum logic '1' output voltage measured at the branch highway port of 0.3 volt at 133 mA sink current, remaining true when all lines are driven to logic '1'.

NEW PRODUCTS

SYSTEM UNITS, TEST EQUIPMENT

PDP-11—CAMAC Interface

A Branch System Controller for the DEC-PDP-11 computer has been developed in two versions (ICP11 and ICP11A) which conform to the CAMAC Specification EUR 4600. Data transfers can be performed in:

Programmed Mode
Direct Memory Access Mode (D.M.A.)

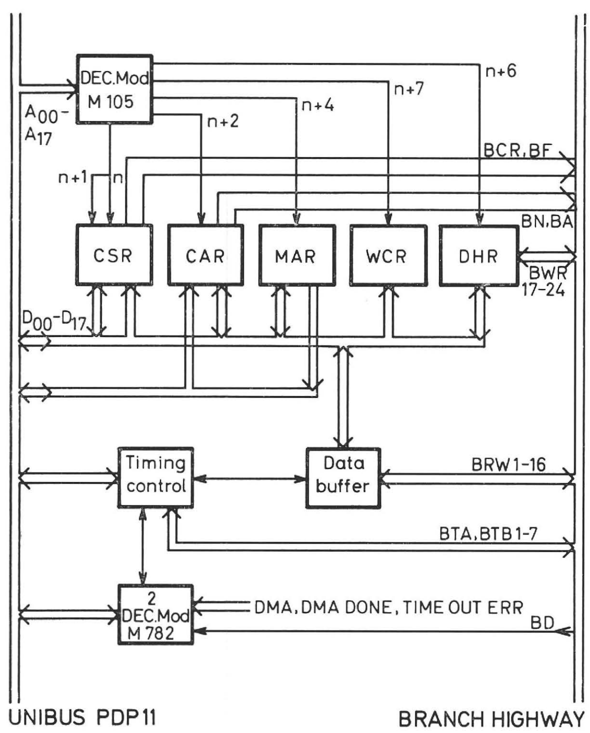
Programmed Mode

In the programmed mode, a CAMAC function is selected using one PDP-11 instruction and a 16-bit data transfer can be effected in one PDP-11 instruction. For a 24-bit data transfer, two PDP-11 instructions are necessary. A CAMAC device (defined by C, N and A) is addressed as directly as any standard peripheral.

D.M.A. Mode

In the D.M.A. mode, only 16-bit data transfers are accepted; two D.M.A. modes are available:

- Normal D.M.A.: In this mode, the CAMAC device address N and sub-address A are unchanged (block transfer mode).
- Automatic D.M.A.: In this mode, the CAMAC device address and sub-address are automatically incremented (scanning mode).



In D.M.A. mode, the CRATE address, the function code, the CAMAC device address and sub-address, the starting memory address and the word-count to be transferred has to be initialized.

The transfer starts automatically by setting to '1' the D.M.A. control bit, and stops when the word-count is reached.

Five service registers are used:

CSR: Control Status Register.
CAR: CAMAC Address Register.
MAR: Memory Address Register.
WCR: Word-Count Register.
DHR: Data High Register

and their addresses are taken in the 'user address' field available in the PDP-11.

The two versions of the CAMAC PDP-11 interface are:

- Model ICP11 for short distance transmission ($\leqslant$ 30 m) (unbalanced inputs and outputs);
- Model ICP11A for long distance transmission ($\leqslant$ 250 m) (balanced inputs and outputs);

and are constructed in the DEC 'System Unit' for PDP-11.

Ref. SAIP-CRC-Schlumberger

PDP-11—CAMAC Interface

The Crate Controller/Interface Type 1533 provides, in a double-width CAMAC unit, an economical means of connecting one or more CAMAC crates to a PDP11 Unibus. The organisation of the Interface is such that each crate appears as a conventional peripheral on the Unibus. Each module and sub-address is individually addressable from the computer for which a total of 512 addresses is required per crate. The address for each crate can, however, be freely chosen. Handshake timing is used between a module and the computer with the CAMAC timing and the Unibus timing interleaved for optimum speed. Of special interest is the incorporation of an interrupt vector generator for 16 vectors which can be placed anywhere in the core memory. Further ancilliary modules are under development for program independent DMA data transfers with non-processor-request and a Unibus extender to permit the siting of crates at distances of up to 200 m.

Ref. Borer & Co.

DEC PDP-11 Branch Driver

The model KS0011 Branch Driver is the interface between Digital Equipment Corporation's PDP-11 computer and the standard CAMAC Branch Highway (described in EUR 4600). It brings to the PDP-11 the modularity, flexibility, simplicity and economy of CAMAC equipment. Operations are performed under program control.

The Branch Driver resides in a single PDP-11 system unit. Connection is made to the unibus via the DEC unibus jumper, and 5-volt power is provided from the computer power supply. The Branch Highway exits the computer on four 34-conductor flat cables that connect to a standard branch highway female connector mounted on a 19″ × 1-$\frac{3}{4}$″ panel. The branch is terminated in the Branch Driver.

Ref. Kinetic Systems Corporation

Branch Highway Transceiver for Long Distance Transmission

This 2/25 width CAMAC module allows Branch Highway transmissions over distances up to about 250 meters in balanced mode. It can be used either as an 'emitter' or as a 'receiver', the mode being selected by a switch on the front-panel.

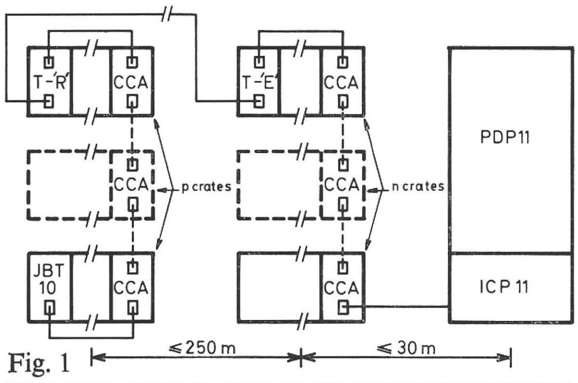


Fig. 1

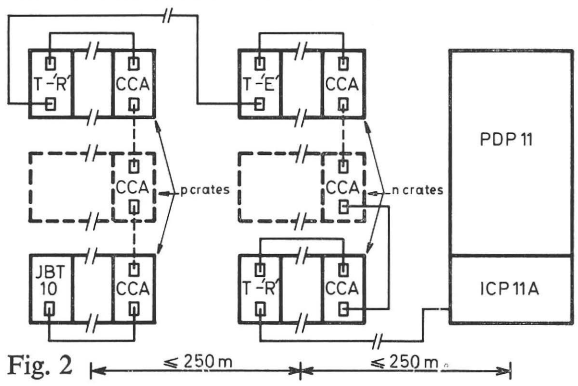


Fig. 2

CCA: Crate controller, type A (JCRC) 50.
T-'E' Trans-ceiver in emitter mode (JBHT 10'E').
T-'R' Trans-ceiver in receiver mode (JBHT 10'R').
JBT10 Branch Highway terminal.

Branch assemblies for long distance transmission.

Fig. 1 *Long distance between a group of p crates and the rest of a branch containing n crates ($n+p \leq 7$), short distance between branch and computer.*
Fig. 2 *As for Fig. 1; long distance between branch and computer.*

A transmission set includes:

- one JBHT 10 in 'emitter' mode.
- one JBHT 10 in 'receiver' mode.
- a Branch Highway cable.

It can be used between two crates of one branch and several times inside that branch up to a maximum of 7 crates.

As a receiver, the JBHT 10 can be directly connected to a Branch Highway cable to the PDT-11-CAMAC interface, model ICP11A (manufactured by SAIP-Schlumberger).

Ref. SAIP-CRC-Schlumberger

Dynamic Dataway Controller

A Dynamic Dataway Controller Type C108 is a 6/25 CAMAC unit designed to allow the testing of modules in a CAMAC crate at the maximum speed of Dataway operations. The unit performs two independent 1 μsec Dataway operations in succession. For this purpose it has two sets of switches on the front-panel to set the Station Number (N), Sub-Address (A) and Function (F) for each operation. Facilities also available on the instrument can apply commands, I, Z and C onto the Dataway in conformity with the latest modifications of the CAMAC Specification EUR 4100. A cycle push-button starts the operations and 'continuous cycling', 'step-by-step' or 'transfer-by-transfer' modes are available.

The ease by which transfers can be set up and the comprehensive way in which they can be executed ensures that modules and systems are tested under realistic Dataway conditions and that faults can be diagnosed rapidly.

During Read operations, the state of the Read lines is stored in a register in the controller and displayed on light-emitting diodes on the front-panel. During a Write operation, the state of 24 Write switches is strobed onto the Dataway to simulate any 24-bit word defined by the setting of the switches. The signal levels on the Q, L, X, S lines are also displayed.

Ref. R.D.T., Rosselli del Turco.

LAM Grader

The LAM Grader, type 064 (CERN Spec.), a single-width unit, is designed to the EUR 4600 e specification. It sorts, by patch wiring, the L priorities in conjunction with a Crate Controller A, to which it is connected by a cable at the rear of the crate.

Special features of the 064 are:

- 4 front-panel demands,
- a masking register on the SL response line.

Additional features include:

- buffering of Z lines to eliminate termination and loading problem in the patch-panel,
- full use of X line,
- use of only compulsory power supplies and solid state lamps.

Ref. Nuclear Enterprises Ltd.

I/O REGISTERS, DISPLAYS

Quad Six-Decade Counter

The Quad Counter Type 1007 is a single-width CAMAC module intended for industrial use in logging and documentation systems. Each channel contains a 24-bit (six-decade) scaler and input circuits designed to accept and count pulses arriving, even when the content of the scalers is being read out, so that no counts are lost. The input thresholds and the input filters are adjustable to suit the application. The input sensitivity can be set for pulses from 5 to 60 V amplitude. With the associated filters, the cut-off frequency is independently variable between 100 and 1000 Hz.

Ref. Borer & Co.

24-bit Input Gate

The input gate (model 3420) is a single-width module that has provision for gating 24 bits of external data onto the Dataway. The data may be selected either low-true or high-true by a front-panel switch. For applications where the input data is multiplexed from a number of sources, the module provides a 6-bit output for selecting one out of 64 channels. Three output strobes, each 2 microseconds in duration, are provided for use as commands to the external devices. One such strobe, produced by the READ command at S2, is useful as a digitize command to analog-to-digital converters (command F(0).A(X) where X may range from 0 to 15). Another command, F(1).A(X) gates external 'group two' data onto the Dataway and produces also an output strobe at S2. The command F(27)·A(0) produces a 'Test Status' output strobe at S1.

The unit is capable of performing interrupts for a dialogue with peripherals. For this purpose an input is provided which sets the LAM on a negative-going transition. This input can be used to signal that the data is ready in the external device. An output, that monitors LAM status, is provided so that devices that gather data asynchronously with the computer may be instructed to hold the data until read.

All external connections are made via a 36-pin edge connector located above the dataway connector on the rearside of the CAMAC crate. The true-false threshold is approximately 1.7 V for all inputs and the input voltages may range between plus and minus 30V.

Ref. Kinetic Systems Corporation

3×16-bit Input Gate

The Type 1061 Input Gate is a low-cost, single-width CAMAC module which enables up to 48 independent signals, indications, switch positions, etc. to be communicated to an industrial automation control system. The various input signals are passed to the module via relays, contactors etc., offering electrically isolated closing contacts. The incoming data is handled in three 16-bit words for compatibility with minicomputers.

Ref. Borer & Co.

24-bit Input Register

The input register (model 3470) is a single-width module that provides a 24-bit register for holding binary input data. The register consists of six 4-bit registers, each having an independent strobe to allow independent latching of data from various sources. The incoming data is latched 2 microseconds after the negative-going edge of the strobe, which allows the strobe to be generated simultaneously with the data in the external device. The read command causes the entire 24-bit register to be gated onto the Dataway (F(0)·A(1)).

The command, F(6)·A(0) gates a module indentifying number onto the Dataway.

A LAM flip flop is associated with each of the six external strobes and becomes set, when enabled, 2 microseconds after the negative-going edge of the strobe.

A command is provided which reads and clears the LAM's (F(0)·A(0)). The six LAM's are ORed to drive the L-line and an independent Interrupt Status output.

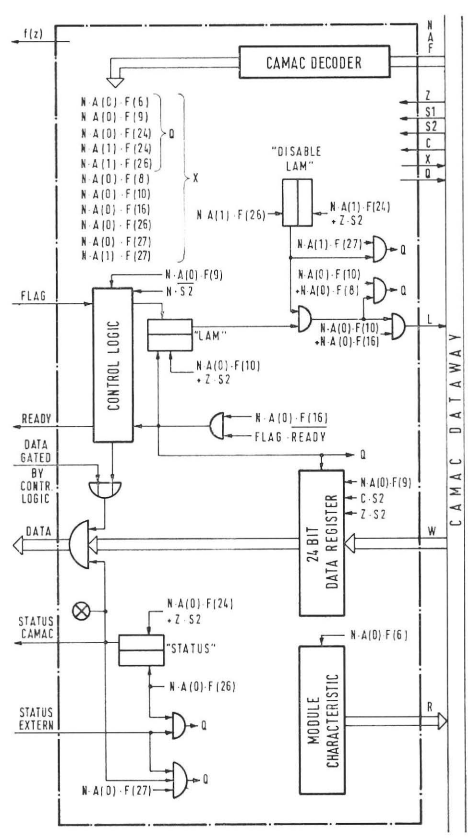
All external connections are made via a 36-pin edge connector located above the Dataway connector on the rear side of the CAMAC crate.

Ref. Kinetic Systems Corporation

Parallel Output Register With Handshake Facility

A new 24-bit parallel output register (model MS PO2 1230) is available from AEG-Telefunken. This new unit allows a peripheral to become either master or slave during an operation, dependent on the mode of operation.

Data transfer between the output register and a peripheral data receiver can be performed by the application of Request/Acknowledge signals. The output register generates a LAM to inform the computer when the data receiver is ready to accept a new data word.



Parallel Output Register MS PO 2 1230/1

The Request/Acknowledge facility can be switched off if the peripheral equipment is such that it is always to accept new data. In this operation mode the computer is allowed to transfer new data at any time.

Conforming with all other CAMAC units of AEG-Telefunken, this unit is equipped with a module characteristic. On/Off control of the CAMAC unit and the peripheral can be performed by a computer or by the peripheral. The computer is also able to test the On/Off state of the CAMAC unit and the peripheral.

Ref. AEG-Telefunken

12-bit Output Register With Isolated Relay Contacts

The output register (model 3086) is a single-width module that contains a 12-bit register for holding binary output data. Twelve relays, whose states are determined by the bits in the register, each supply an isolated contact to the I/O connector. The relays may be energized and de-energized singly or in combination by a versatile set of CAMAC commands, making the module particularly useful for control applications. The register can be written, cleared, set, selectively cleared, selectively set, and read. Individual bits may be set or cleared via command and sub-address. With the command, F(6)·A(0) a module identifying number is read.

The 3086 fully decodes all Functions and Sub-addresses and returns Q for valid commands.

A LAM flip flop is provided which, when enabled, may be set by a negative-going transition of an external input, by a command, or by a front panel switch. The LAM is cleared by direct command or by any command that affects the contents of the register. Sequences of programmed outputs can thus respond to internal or external control.

All external connections are made via a 36-pin edge connector located above the dataway connector. Each of the 12 outputs is a floating reed-relay contact rated at 50 V, 1/2A. Contact protection in the form of arc suppression and surge current limiting is provided. The maximum allowable resistive load is 10W for each contact.

Ref. Kinetic Systems Corporation

2×16-bit Output Register

This single-width Output Register Type 1082 provides a very simple means of controlling up to 32 independent functions, devices, indicators, etc. The electrically isolated outputs are relay contacts having a 10W, 100V, 500mA dc rating. The unit has built-in flexibility since the two groups of 16 relays are steered from independent registers which can be separately overwritten.

Modified forms are available with open-collector outputs (30V at 40mA max), in place of the relays, or output drivers with electrical isolation through optical couplers.

Ref. Borer & Co.

Multichannel Analyser Interface

A 3125 width CAMAC module has been developed which accepts address information (up to 14 bits) and then reads 24-bit data from, or writes 24-bit data into, the Packard 904 Series MCA at the address (channel) specified.

Using a second mode, the MCA can be put into accumulate, display or readout by transfer of a coded word into the module. This function can be cancelled by a front panel switch.

The module can respond to 'end of accumulate' or 'end of readout' to produce an interrupt. There is also an 'external interrupt' input-jack on the front-panel. All three interrupts are software enabled and in addition can be manually cancelled by a front-panel switch. The unit takes 1.25A from the +6V line.

Commands

F(0) · A(0): to read 24 bit word from MCA.
F(16)·A(0): to write 24 bit word into MCA.
F(16)·A(1): to establish MCA channel number (Address 14 bit).
F(16)·A(2): to command MCA mode of operation.
F(26)·A(0), F(26)·A(1), F(26)·A(2): to enable interrupts.
F(8) · A(0), F(8)·A(1), F(8)·A(2): to test interrupt requests.
F(10)·A(0), F(10)·A(1), F(10)·A(2): to reset interrupt requests.
F(27)·A(0), F(10)·A(3): to allow Q response for synchronization to the MCA memory cycle.

Ref. Packard Instrument Company

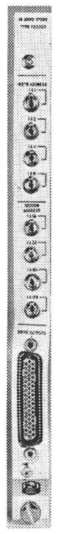
16-Channel Coincidence Register

The LRS Model 2341 Coincidence Register offers 16 complete channels in one CAMAC double-width module. The unit operates from standard NIM logic levels. The logic channels, which seek a coincidence between each input and a common fast-gate input, employ MECL III integrated circuits and provide coincidence resolving-times under 2 nanoseconds.

The time-coincidence between the common gate input and the 16 inputs are stored in a 16-bit fast buffer register for later readout under CAMAC commands. The facility for performing majority logic is provided by two front-panel summing outputs which are each driven by 8 logic channels. The output current of the summing circuit is proportional, in increments of 4mA per register bit, to the number of coincidences stored in the register. Bridged high impedance outputs permit cascading any number of summing outputs. Other operating features include a front-panel clear input which responds to negative logic levels and a built-in test mode.

Ref. Lecroy Research Systems Corporation

16 Word Store



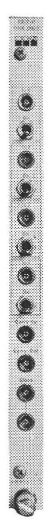
This single-width CAMAC unit (type CS 0003) provides sixteen 24-bit registers which may be accessed via the Dataway and addressed from front-panel plug-pins. The contents of the selected register are routed to the front-panel plug as a 24-bit word with 48 mA drive capability.

Apart from its use as a multiple buffer register (16 word scratch-pad memory) and a multiplexed driver, it has been proved invaluable as a Read/Write instruction memory for the 7025 Programmed Dataway Controller to increase the flexibility of such systems.

Ref. Nuclear Enterprises Ltd.

MULTIPLEXERS, CONVERTERS

Time Digitizer TD 2041



A Time Digitizer (model TD 2041) has been designed as a data acquisition module for spark chambers with magneto-strictive readout. It is also useful in connection with related equipment, such as proportional wire chambers (with shift register readout) and large scintillation counter arrays. More generally, its function is to record the time of occurence of a succession of events.

Outstanding features of the TD 2041 are:

- Four digitizing scalers in a single-width unit.
- Very simple command structure and low cost per event.
- Any 'scaler-per-plane' distribution without idle scalers. A fan-out of 1 is only required from the transducer discriminator.
- Built-in test logic.
- Implemented with high speed and normal TTL IC's to enhance performance.

Ref. SEN Electronique

8 Bi-linear ADC's

The LRS Model 2248 contains eight complete 8-bit ADC's in a single-width CAMAC unit. Input polarity is negative for photo-multiplier anode pulses; however, positive pulses or negative pulses with positive undershoot can also be handled linearly. A common, linear gate establishes the time-window during which the analogue inputs are active. This input is operated by standard NIM-level signals from 10 to 200 ns in duration.

The Model 2248 offers a number of convenient and flexible features. A unique conversion-mode control provides the choice of two linear modes with sensitivities of 0.25 pC/count or 1.0 pC/count, or three bi-linear modes. The bi-linear modes provide an effective increase in the dynamic range, as compared with simple linear conversion, by digitizing the lower quarter of the output range at 0.25 pC/count and switching at one of three selected points to 1.0 pC/count. A simple, CAMAC-controlled, internal test checks all ADC's simultaneously from input to output. Other flexible features include readout of two adjacent modules in the form of eight 16-bit words, and suppression of Q response for modules with less than a pre-selected number of counts in all of the eight channels.

Full Scale Ranges:	From 64 pC to 256 pC (3.2 to 12.8 V/ns, 50 ohms impedance), dependent upon bi-linear mode position.
ADC Resolution:	8 bits actual (0.4%); 10 bit equivalent (0.1%) in bi-linear mode.
CAMAC Function Codes:	F0; F2; F9; F25.

Ref. Lecroy Research Systems Corporation

Fast ADC

The fast ADC Type 1242 is a 'successive approximation' double-width CAMAC module. It is designed to be compatible with the Borer FET-Multiplexers Type 1703 and 1704 for rapid scanning and digitisation of a large number of analogue signals. The resolution is normally 12 bits (including sign) but can be supplied as an S- or a 10-bit converter. The differential input gives an impedance in excess of 100 M ohms and will accept signals of up to ± 10 V. Conversion time is 20 µs for 12-bit full scale. Particular attention has been given to linearity and temperature coefficient.

Ref. Borer & Co.

Fast Fet Multiplexers

The two fast Multiplexers, Types 1703 and 1704, have been designed to work in conjunction with the Borer fast ADC Type 1242. Both are identical single-width CAMAC modules except that one offers 32 'single-ended' inputs and the other 16 differential inputs. The inputs will handle signals of ± 10 V amplitude with a change-over time from channel to channel of only 2 µs. Many such Multiplexers can be operated in tandem thereby requiring only one ADC for several hundred measurement channels. The 'Scan-Through' mode of operation is fully automatic. It can start at any channel number in one module and end at any other number in another module without intermediate reference to the computer. The re-cycle operational mode is similar except that, on reaching the 32nd channel (1703) or 16th channel (1704), the scanning action returns to channel 1 of the same module instead of passing to the next. In both operational modes, the necessary Scan + 1 pulse (to cause the Multiplexers to step to the next channel) comes from an external source such as the ADC or the Borer Input/Output Register Type 1031 when a non-CAMAC DVM or ADC is in use. Interlocked operation of all the

Multiplexers and the ADC/Input Register in a system is ensured by a bussed Wait/Ready line linking all elements.

Ref. Borer & Co.

Octal ADC

This single-width CAMAC plug-in unit (type 9040) is an eight channel Analogue to Digital Converter for narrow analogue input pulses, typically from fast photomultiplier tubes. Each input channel contains a linear gate and integrator which stores the input charge occurring during the gate signal which is common to all channels. The stored charge is digitized to 8-bit accuracy by measurement of the time to discharge the storage capacitor under constant current conditions. Conversion of all channels is concurrent and the data is readout as four 16-bit words and an overflow condition is indicated by all '1's. A dataway 'L' signal is generated for any input above a digital level which is patchable for each channel.

In response to F(25) a test charge of 60pC is injected into all channels, to simulate gate and input signals. Full-scale sensitivity is 100 pico coulombs and conversion time for all 8 channels is less than 250µsec.

Ref. Nuclear Enterprises Ltd.

OTHER MODULES

Power Supply Controller

A CAMAC unit for the control of power supplies has been developed (model 3155). It is a single-width module containing a data register that can be written or read, a digital-to-analogue converter to provide an analogue output, four digital control signals and provision for reading four bits of status information. Data sent to the module must be in sign and magnitude form. The sign bit (W16) controls a polarity relay, while remaining data bits control the current (or voltage). All connections to the external power supply are made via a 36-pin edge connector located above the dataway connector on the rearside of the CAMAC crate.

The analogue output is a 0 to plus 10 V signal supplied from a precision operational amplifier. A drift in signal amplitude is less than the inaccuracy determined by the resolution of the applied DAC. The 3155 is available with either 10-bit or 12-bit resolution.

The four digital control signals are TURN ON, TURN OFF, RESET, and POLARITY. Each output is a floating relay contact rated at 50 V, 0.5 A.

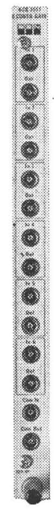
The control signals are triggered by CAMAC commands. The signals are present for 300 msec with the exception of POLARITY which is a d.c. signal.

A four-bit input gate is provided for the reading of low-true status information from the power supply.

One of the status bits may be preselected within the module to set the LAM flip-flop upon a positive-going transition. An external input for setting the LAM on a falling edge is also provided. A signal on this input can be used, for example, to direct the computer to check and log the power supply status. Reading the status bits also clears the LAM flip-flop.

Ref. Kinetic Systems Corporation

Six-fold Controlled Gate 6CG 2017



The 6CG2017 is a gate network intended to set the flow of fast electronic pulses under computer control. All inputs/outputs are designed for standard NIM pulses or signals. Pulse rates up to 50 MHz can be accepted. The gate network is made from MECL II integrated circuits. Output rise- and fall-times are typically under 5 ns.

Ref. SEN Electronique

Dual-Pulse and Stepping-Motor Controller

A single width module (mod. 3360) contains two separate channels for producing trains of serial ouput pulses. Writing a 16-bit sign and magnitude word into a count-down register initiates a process that counts the register down to zero while generating an output pulse at each count.

Two transformer-coupled outputs are provided for each pulse-train, and the pulse-train is steered to one or the other by the sign bit. The count-down is halted at a count of zero or upon ground closure of one of two external inputs. The sign bit determines which of the external inputs is able to inhibit the counting process, and an attempt to restart the counting, by writing a signed number while the related input is grounded, will tail. The number will not be written and NO-Q will be returned.

A separate clock is provided for each channel, and the pulse-rates are adjustable from 50Hz to 400Hz. Nominal pulse-width is 100 microseconds. Means are provided to allow external control of the pulse rates.

The count-down registers can be read on written into.

A LAM source bi-stable is provided for each channel. The bi-stable is cleared by a write command and is set by the count reaching zero or by the count stopping due to external inhibit. The LAM sources may be tested or the 8-bit status register, which contains LAM source information, may be read. The LAM sources may be separately enabled and disabled.

The 3360 is particularly useful as a dual-channel stepping motor controller.

Ref. Kinetic System Corporation

COMPONENTS

Branch Highway Cable Assembly

TEKDATA's Branch Highway harnesses comprise twisted-pair cables in ribbon form. By using ribbon cables the electrical characteristics (e.g., characteristic impedance) are held to better tolerances than when ordinary round harness cable is used, thus giving a superior interface medium.

Each assembly has 68 twisted pairs; 66 are terminated to the CAMAC approved connector and two are spare. The twisted pairs are screened with either copper or stainless steel mesh/braid and sheathed overall with PVC tubing. All harnesses are extremely flexible; the stainless steel screening being the most flexible.

Standard lengths are held in stock and any length can be supplied to customer specification without delay. When ordering, the following code should be used 2000/S/0132/xxx. (xxx = length in metres.)

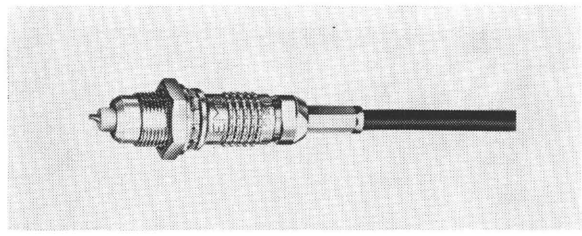
Ref. TEKDATA Ltd.

Standard Coaxial Connector

First to launch its self-locking connectors, LEMO presents a new design of its 00 coaxial plug, standardised for the CAMAC system.

Connection to the cable is simple and quick by crimping the screening and the central contact.

Small size and easy handling of the connector permit 5,000 connectors to be installed in an area of one square meter. They are strongly built and their mechanical and electrical properties are guaranteed even after 10,000 connections. They are particularly recommended for fast-logic circuits and all HF apparatus that requires little space.



Ref. Lemo SA

Metallic Pin Shield CD 15014

A metallic pin shield has been designed to overcome breakages and cracking to the diallyl phtalate (d.a.p.) shield on the WSS-0132-P08-BN-502 and 527 type connectors.

The new shield, manufactured in 'Mazak' 3 material, complies with the specification BS1004, is finished in black and is suitable for use with any thickness of front-panel on CAMAC plug-in units. The 'rabbit ears' on the shield permit normal panel-fixing screws to be used without interference from the connector hood-fixing screws.

The shield is fixed to the connector body by a CIBA adhesive, SW 409.

A full service is being offered for repair of damaged connectors, which are fitted to cable assemblies, and for modifying connectors held in stock at laboratories.

Availability: May 1972.

Ref. Emihus Microcomponents Ltd.

PREPARATION OF NEW PRODUCTS CONTRIBUTIONS

Please follow as closely as possible the style used in this issue of the Bulletin, and the relevant instructions given elsewhere for contributed papers, with the exceptions:

1. *Please type each product description on a separate page.*
2. *The description of a single product should not exceed 250 words, or one third-page including illustrations.*
3. *Photographs and drawings may be used, if they are essential to illustrate the product and are suitable for reduction to fit the available space.*
4. *Unless translations are specifically requested, the contributions will be printed as submitted, apart from minor corrections (e.g., spelling, punctuation and layout).*

Manufacturer's Index to News and New Products Information

MEMBERSHIP OF THE ESONE COMMITTEE

This list shows the member organisations and their nominated representative on the ESONE Committee. Members of the Executive Group are indicated thus*.

International	European Organization for Nuclear Research (CERN)	*F. Iselin**	Geneva, Switzerland
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	ESONE Secretariat	*W. Becker**	
	Bureau Central de Mesures Nucléaires (Euratom)	*H. Meyer**	Geel, Belgique
Austria	Studiengesellschaft für Atomenergie	*R. Patzelt*	Wien
Belgium	Centre d'Etude de l'Energie Nucléaire	*L. Binard*	Mol
Denmark	Forsögsanläg Risö	*Per Skaarup*	Roskilde
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	Culham Laboratory	*A.J. Vickers*	Abingdon
	Daresbury Nuclear Physics Laboratory	*B. Zacharov*	Warrington
	Rutherford High Energy Laboratory	*M.J. Cawthraw*	Chilton
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	Institut Max von Laue - Paul Langevin	*A. Axmann*	Grenoble
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	Gesellschaft für Kernforschung	*K. Tradowsky*	Karlsruhe
	Institut für Kernphysik der Universität	*W. Kessel*	Frankfurt/Main
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Hungary	Central Research Institute for Physics	*J. Biri*	Budapest
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	Istituto di Fisica dell'Università	*G. Giannelli*	Bari
Netherlands	Reactor Centrum Nederland	*P.C. van den Berg*	Petten
	Instituut voor Kernphysisch Onderzoek	*E. Kwakkel*	Amsterdam
Poland	Instytut Badan Jadrowych	*R. Treckinski*	Swierk K/Otwocka
Sweden	Aktiebolaget Atomenergi Studsvik	*Per Gunnar Sjölin*	Nyköping
Switzerland	Institut für Angewandte Physik der Universität	—	Basel
Yugoslavia	Boris Kidrič Institute of Nuclear Sciences	*M. Vojinovic*	Vinča Belgrade

LIAISON WITH THE USAEC NIM COMMITTEE IS MAINTAINED THROUGH:

L. Costrell (Chairman), National Bureau of Standards – Washington, DC.

F.A. Kirsten (NIM-CAMAC Dataway Working Group), Lawrence-Berkeley Laboratory – Berkeley, California.

S. Dhawan (NIM-CAMAC Software Working Group), Yale University – New Haven, Connecticut.

D.A. Mack (NIM-CAMAC Mechanics Working Group), Lawrence-Berkeley Laboratory – Berkeley, California.

D.I. Porat (NIM-CAMAC Analogue Signals Working Group), Stanford Linear Accelerator Center – Stanford, California.

CAMAC PRODUCT GUIDE

(products available up to April 12, 1972)

CAMAC PRODUCT GUIDE

This guide consists of a list of CAMAC equipment which is believed to be offered for sale by manufacturers in Europe and the USA. The information has been taken from a CAMAC Product Reference compiled by CERN-NP-EL II from manufacturers' catalogues, advertisements and written communications available to them on 12th April, 1972.

The number of items of commercially available CAMAC equipment is still increasing. The current list containing some 70 more items than in Issue No. 3 of the Bulletin. Every effort has been made to ensure the completeness and accuracy of the list, and it is hoped that most products and manufacturers have been included. Inclusion in this list does not necessarily indicate that products are fully compatible with the CAMAC specifications nor that they are recommended or approved by the ESONE Committee. Similarly, omission from this list does not indicate disapproval by the ESONE Committee. Users are advised to obtain detailed information from the manufacturers or their agents in order to check the compatibility and operational characteristics of equipment.

Some changes have been introduced in the listing for this Issue as a result of comments made on the lists contained in the previous Issues. The signs indicating special external interconnections and front-panel connections have been removed, the explanatory comment in brackets following the manufacturers designation contains instead this indication.

Names of some manufacturers appearing in earlier lists have changed, the appropriate reference is given in the Index of manufacturers at the end of this guide.

The general arrangement of the equipment list is based on a classification according to the main operational application of each item. This has the advantage that the main classes of unit (such as scalers, I/O registers and gates, crates, etc.) are grouped together. Some other units are difficult to classify using the available information, and readers are therefore advised to search under several categories.

Remarks on some columns in the Index of Products:

N/C – N is new, C is corrected entry;

WIDTH – NA indicates other format, normally 19 inch rack mounted chassis,
– 0 indicates unknown width,
– Blank, the width has no meaning,
– 24 or 25 indicates number of stations;

DELIV – Date on which item became or will become available.

NPR – Number in brackets is issue number of the Bulletin in which the item was or is described in the New Products section or as News respectively.

CLASSIFICATION GROUPS

INDEX OF PRODUCTS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	BRANCH HIGHWAY RELATED SYSTEM UNITS (Computer Couplers, Crate Controllers, Terminations)					
N	CRATE CONTROLLER/PDP11 UNIBUS INTERFACE	1533	BORER	2	05/72	(4)
C	INTERFACE/SYSTEM CONTROLLER TO HP21CC, 2114, 2115, 2116	2201	BORER	NA	/71	(4)
C	INTERFACE/SYSTEM CONTROLLER TO DEC PDP9 (PROGR,SEQUENT AND BLOCK TRANSFERS)	2202	BORER	NA	/71	(4)
C	INTERFACE/SYSTEM CONTROLLER TO DEC PDP15 (PROGR,SEQUENT AND BLOCK TRANSFERS)	2203	BORER	NA	/71	(4)
	INTERFACE FOR VARIAN 620I/L/F COMPUTER (PROGR,SEQUENT AND BLOCK TRANSFERS)	2204	BORER	NA	/71	
	PDP-11 CAMAC CONTROLLER(SEQUENTIAL READ/ WRITE,24 GRADED-L INTERRUPT DIRECTLY)	CA 11-A	D E C	NA	05/71	(2)
	PDP-15 CAMAC INTERFACE(18/24BIT,PROGR, SEQUENT ADDR AND BLOCK TRANSFER MODES)	CA 15 A	D E C	NA	05/71	(1)
	PDP-9 CAMAC INTERFACE (SOMEWHAT MODIFIED CA 15 A)	CA 15 A/PDP-9	D E C	NA	07/71	
	PDP-11 BRANCH DRIVER (EUR 4600 COMPATI- BLE,PROGRAMMED AND SEQUENT ADDR MODES)	BD-011	EG+G	NA	/71	
	PDP-11 INTERFACE SYSTEM COMPRISING	SI-11	GEC-ELLIOTT		/71	
	EXECUTIVE CONTROLLER	MX-CTR-1		2		
	BRANCH COUPLER	BR-CPR-1		2		
	PROGRAMMED TRANSFER INTERFACE (CAN DRIVE DATAWAY ALONE)	PTI-11 CD		2		
	UNIBUS TERMINATION UNIT	TRM-11		1		
	INTERRUPT VECTOR GENERATOR	IVG-11		1		
	DISPLAY DRIVER(CONTROLS 72A DISPLAY, ALSO CRATE CTR AND BRANCH DRIVER)	72A	JORWAY	3	07/71	
N	BRANCH DRIVER PDP-11	KS 0011	KINETIC SYSTEMS	NA	/71	(4)
	BRANCH DRIVER	7081	NUCL. ENTERPRISES	C	/71	
	PDP 11 INTERFACE AND BRANCH DRIVER SYSTEM		NUCL. ENTERPRISES	O		
C	INTERFACE CAMAC-PDP 11 (PROGRAMMED,BLOCK TRANSFER AND SEQUENTIAL ADDR MODES)	ICP 11/CP 11 A	SAIP-CRC	NA	/71	(4)
N	BRANCH HIGHWAY TRANSCEIVER FOR LONG DISTANCE TRANSMISSION	J BHT 10	SAIP-CRC	2		(4)
	NOVA COMPUTER TO CAMAC MASTER BRANCH HIGHWAY DRIVER (ONE TO THREE BRANCHES)	MC-2010	TECHCAL	O	11/71	
	SLAVE BRANCH HIGHWAY DRIVER	MC-2016		O	11/71	
	CRATE CONTROLLER /ESONE TYPE A/ (CONFORMS TO EUR4600 SPECS)	1501	BORER	2	01/71	
	ESONE TYPE A CRATE CONTROLLER (CONFORMS TO EUR 4600 SPECS)	CC 2404-1	GEC-ELLIOTT	2	01/71	
	CONTROLEUR DE CHASSIS MULTI 8-CAMAC (24BIT,PROGR,SIMULT I/O,INTERRUPT MODES)	JCM 8	INTERTECHNIQUE	3	09/71	
	BRANCH CRATE CONTROLLER/TYPE A (CONFORMS TO EUR 4600 SPECS)	70	JORWAY	2	01/71	
N	CRATE CONTROLLER	3901	KINETIC SYSTEMS	2	/72	
N	CRATE A CONTROLLER ((CONFORMS TO EUR 4600 SPECS)	9016	NUCL. ENTERPRISES	2		(4)
	CRATE CONTROLLER TYPE A (CONFORMS TO EUR4600 SPECS)	C 106	RDT	2	06/71	
	CONTROLEUR DE CHASSIS TYPE A (CONFORMS TO EUR4600 SPECS)	J CRC 50	SAIP-CRC	2	02/71	(1)
	A CRATE CONTROLLER (CONFORMS TO EUR4600 SPECS)	ACC 2034	SEN	2	06/71	
	CAMAC CRATE CONTROLLER TYPE A (CONFORMS TO EUR4600 SPECIFICATIONS)	CC100L	EG+G	2	/71	
C	BRANCH TERMINATION UNIT	C 72451-A 1454-A1	SIEMENS	NA		(3)
	CRATE CONTROLLER A (CONFORMS TO EUR 4600 SPECS)	C72451-A1446-B1	SIEMENS	2	10/70	(1)
	TERMINATION UNIT	1591	BORER	2	/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	TERMINATOR MODULE (BRANCH HIGHWAY TERMINATOR)	TC024	EG+G	2	/71	
	BRANCH HIGHWAY TERMINATION MODULE(MOUNTS DIRECTLY ON BRANCH HIGHWAY ASSEMBLY)	CD 18107	EMIHUS	NA	/72	
	BRANCH TERMINATION UNIT	BT 6601	GEC-ELLIOTT	2	01/71	
	BRANCH TERMINATION	50	JORWAY	2	01/71	
	TERMINAISON DE BRANCHE CAMAC	J BT 20	SAIP-CRC	2	11/71	
	CRATE CONTROLLER BUS TERMINATOR FOR *A* CRATE CONTROLLER ACC 2034	BT 2042	SEN	1	04/72	

DATAWAY RELATED SYSTEM UNITS
(Computer Couplers, Controllers)

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	CRATE CONTROLLER TYPE D (CONFORMS TO EUR 4100, USED WITH DO 280 COMPUTER SYSTEM)	DO-C280-2901	DORNIER	2	11/71	
	CRATE CONTROLLER FOR NOVA COMPUTER	CC 2023A/B	SEN	2	/70	
	CRATE CONTROLLER BUS TERMINATOR FOR CC 2023A/B (ONE PER SYSTEM)	BT 2022		0	11/71	
	DATAWAY CONTROLLER DDP-516(PART OF 7000-SER SYSTEM WITH EXT CONTROL HIGHWAY)	7022-1	NUCL. ENTERPRISES	4	/70	
	DATAWAY CONTROLLER PDP-8 (PART OF 7000-SER SYSTEM WITH EXT CONTROL HIGHWAY)	7048-2	NUCL. ENTERPRISES	2	/70	
	AUXILIARY CONTROLLER PDP8	7049-1		3	/71	
	AUXILIARY CONTROLLER	7047-1		1	/70	
	COMPUTER INTERFACE		INTERDATA	0	07/71	

OTHER SYSTEM UNITS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	START-STOP CONTROLLER(START,STOP AND RESET OUTPUTS,MANUAL OR DATAWAY CONTROL)	FHC 1304A	BF VERTRIEB	1	01/71	(1)
N	LAM GRADER (DESIGNED TO EUR 4600 SPECS)	064	NUCL. ENTERPRISES	1		(4)
	LAM GRADER (CERN SPECS 064)	C 107	RDT	1	06/71	
	COMMANDE *ARRET-MARCHE* (START-STOP UNIT ,START,STOP,CLOCK, AND GATE OUTPUTS)	J AM 10	SAIP-CRC	1	01/71	
	FOUR FOLD BUSY DONE (START SIGNAL INITIATED BY COMMAND,DEVICE RETURNS LAM)	4BD 2021	SEN	1	02/71	
	STORE	N600	TEXAS INSTR. LTD	0	07/71	
	PROGRAMMED DATAWAY CONTROLLER (PART OF 7000-SER SYSTEM WITH EXT CONTR HIGHWAY)	7025-2	NUCL. ENTERPRISES	2	/70	
	AUXILIARY CONTROLLER	7080-1		0	/71	(2)
	SEQUENTIAL COMMAND GENERATOR	7037-1		2	/70	
	COMMAND GENERATOR	7062-1		2	/71	
	TRANSFER REGISTER	7063-1		1	/70	
	PROGRAM CONTROL UNIT	0362-2		NA	/70	
	PLUGBOARD STORE	0361-2		NA	/70	
	WIRED STORE	7044-1		1	/70	
	STORE INTERFACE	7067-1		0	/71	(2)
	PLUGBOARD STORE	7077-1		3	/71	
	(MULTICRATE SYSTEM WITH EXTERNAL CONTROL HIGHWAY,COMPRISING)	7000-SERIES	NUCL. ENTERPRISES		/70	
	LOCAL INTERCRATE INTERFACE	7033-1		2		
	LOCAL SLAVE DATAWAY CONTROLLER	7034-1		2		
	REMOTE INTERCRATE INTERFACE	7035-1		2		
	REMOTE SUB-MASTER DATAWAY CONTROLLER	7036-1		2		
	DIGITAL CONTROL MODULE(BIDIRECTIONAL CON TROL VIA R/W-LINES OF FOUR 4BIT DEVICES)	TC-0440	TECHCAL	2	11/71	
	DIGITAL CONTROL MODULE(BIDIRECTIONAL CON TROL VIA R/W-LINES OF FOUR 8BIT DEVICES)	TC-0840	TECHCAL	2	11/71	

MANUAL CONTROLLERS AND TEST EQUIPMENT

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	MANUAL DATAWAY CONTROLLER	7024-1	NUCL. ENTERPRISES	8	/70	
C	DYNAMIC DATAWAY CONTROLLER	C 108	RDT	8	06/71	(4)
	CONTROLEUR MANUEL DE CHASSIS (MANUAL TEST MODULE)	J CMC 10	SAIP-CRC	8	06/71	(1)
	DISPOSITIF DE CONTROLE MANUEL DE DATAWAY (MANUAL CONTROLLER/DISPLAY SYSTEM)	D AI 10	SAIP-CRC	1	11/71	
	TIROIR DE PRISE D'INFORMATION (INTERFACE TO DATAWAY)	J DA 10		1	11/71	
	CHASSIS DE CONTROLE ET AFFICHAGE (CONTROL AND DISPLAY CHASSIS)	C AI 10		NA	11/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	CHASSIS DE CONTROL MANUEL DE BRANCHE (COMPR TYPES CCOB10/TCMB10/TIC10/TIC20)	C CMB 10	SAIP-CRC	NA	C9/71	(1)
	CAMAC DATAWAY DISPLAY (DATAWAY SIGNAL PATTERN STORED/DISPLAYED,2 TEST MODES)	1801	BORER	1	/71	(1)
	TEST MODULE (HARDWARE AND SOFTWARE TEST UNIT FOR BD-011)	TM024	EG+G	2	/71	
	MANUAL CRATE CONTROLLER	GFK-LEM	EISENMANN	8	11/71	
	BRANCH HIGHWAY TEST POINT MODULE(24 DIR-ECT,22 INDIRECT ACCESS POINTS FOR TEST)	CD 18104	EMIHUS	NA	10/71	(3)
	BRANCH HIGHWAY REMOVE INHIBIT MODULE (REMOVES INHIBIT FROM BCR/BA/BF/BN/BTA)	CD 18105	EMIHUS	NA	10/71	(3)
	DATAWAY TEST MODULE (NEON INDICATION OF STATE OF ALL DATAWAY LOGIC LINES)	DTM 1	GEC-ELLIOTT	2	C1/71	
	CRATE CONTROLLER TESTER	NU 969	GEC-ELLIOTT	C	10/71	
	DYNAMIC TEST CONTROLLER (GENERATES ALL POSSIBLE CAMAC COMMANDS IN SINGLE CRATE)	TC 2402	GEC-ELLIOTT	4	C1/71	
	DATAWAY DISPLAY (INDICATES LOGIC STATE OF DATAWAY LINES)	9019	NUCL. ENTERPRISES	NA	/71	(1)
	DATAWAY BUFFER (OUTPUTS TO 9019 DATAWAY SIGNALS ACCESSIBLE IN NORMAL STATION)	9018		1	/71	(1)
	TEST MODULE FOR CRATE CONTROLLER CC 2023A/B	TM 2040	SEN	1	04/72	
N	DATAWAY DISPLAY	3290	KINETIC SYSTEMS	1	/72	

SERIAL INPUT MODULES (Scalers)

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	COUNTING REGISTER (1X24BIT,15MHZ,TTL/NIM SIGNALS,EXT INHIBIT IN,CARRY OUT)	7070-1	NUCL. ENTERPRISES	1	/70	
	ECHELLE BINAIRE 24 BITS(SCALER,20MHZ NIM OR 10MHZ TTL I/P,EXT INHIBIT IN,OVF C/P)	J EB 10	SAIP-CRC	1	01/71	
N	MINISCALER (2X16BIT,30MHZ,SEPARATE GATES AND EXTERNAL RESET,NIM LEVELS)	002	NUCL, ENTERPRISES	1		
	MINISCALER (2X16BIT,30MHZ,SEPARATE GATES AND EXTERNAL RESET,NIM LEVELS)	1002	BORER	1	11/69	
	MINISCALER(2X16BIT,30MHZ,SEPARATE GATES AND EXT RESET,NIM LEVELS)	C 104	RDT	1	C6/71	
	DUAL 150 MHZ 16 BIT SCALER (ONE 50 OHMS, ONE UNTERMINATED NIM INPUT PER SCALER)	2S 2C24/16	SEN	1	/70	
	DUAL 100MHZ SCALER (2X24 BIN BITS OR 2X6 BCD DIGITS,DISCR LEVEL -0.5V)	80A	JORWAY	1	10/70	(1)
	DUAL 150 MHZ 24 BIT SCALER (ONE 50 OHMS, ONE UNTERMINATED NIM INPUT PER SCALER)	2S 2024/24	SEN	1	/7C	
	TIME DIGITIZER(5X16BIT,CLOCK RATE 40MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1	02/72	
	TIME DIGITIZER (4X16BIT,CLOCK RATE 70/85MHZ,NIM LEVELS)	TD 2041	SEN	1	02/72	(4)
	MICROSCALER (4X16BIT,2X32BIT SELECTABLE, 25MHZ,COMMON GATE,NIM LEVELS)	10C3	BORER	1	C5/69	
	QUAD CAMAC SCALER (4X16BIT OR 2X32BIT, 40MHZ)	1004	BORER	1		
	QUAD SCALER (4X16BIT,SELECTABLE 2X32BIT, 50MHZ,COMMON GATE,NIM LEVELS)	S416L	EG+G	1	/71	
	QUAD 16-BIT SPARK READ-OUT REGISTER (20MHZ RATE,TTL LEVELS)	SR 1604	GEC-ELLIOTT	1	01/71	
	SERIAL REGISTER (4X16BIT,2X32BIT SELECTABLE,25MHZ,COMMON GATE,NIM LEVELS)	SR 1605	GEC-ELLIOTT	1	C1/71	
	QUAD 40 MHZ SCALER (4X16BIT,2X32BIT SELECTABLE,COMMON GATE,NIM LEVELS)	SR 1606	GEC-ELLIOTT	1	C1/71	
	SERIAL REGISTER (4X16BIT,2X32BIT SELECT-ABLE,100MHZ,COMMON GATE,NIM LEVELS)	SR 1608	GEC-ELLIOTT	1	/71	
	MICROSCALER (4X16 BIT,25MHZ,OPTIMIZED INPUT,3 NSEC,GIVES TYP 80MHZ COUNTING)	003-4	NUCL. ENTERPRISES	1	/71	
	QUAD COUNTING REGISTER(4X16BIT,NIM INPUT TTL INHIBIT IN,TTL CARRY AND OVF OUT)	706-2	NUCL. ENTERPRISES	1	/71	
	QUAD SCALER	9015	NUCL. ENTERPRISES	C	/71	
	MICROSCALER(4X16BIT,2X32BIT SELECTABLE, 25MHZ,COMMON GATE,NIM LEVELS)	C 102	RDT	1	C6/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	ECHELLE BINAIRE 4 X 16 BITS(SCALER,30MHZ 2X32BIT SELECTABLE,COMMON GATE,NIM/TTL)	J EB 20	SAIP-CRC	1	01/71	
	FOUR-FOLD SCALER (4X16BIT,2X32BIT SELECTABLE,50MHZ,COMMON GATE,NIM LEVELS)	4 S 2003/50	SEN	1	/69	
	FOUR-FOLD SCALER(4X16BIT,2X32BIT SELECTABLE,100MHZ,COMMON GATE,NIM LEVELS)	4 S 2003/100	SEN	1	/70	
	FOUR-FOLD CAMAC SCALER (4X16BIT,40MHZ, INPUTS A AND B-NIM RESP TTL-ARE ANDED)	4 S 2004	SEN	1	/70	
	QUAD 25 MHZ SCALER (4X16BIT,2X32BIT SELECTABLE,COMMON GATE,NIM LEVELS)	QS-003/25	TECHCAL	1	11/71	
	QUAD 80 MHZ SCALER (4X16BIT,2X32BIT SELECTABLE,COMMON GATE,NIM LEVELS)	QS-003/80	TECHCAL	1	11/71	
	QUAD 100 MHZ SCALER (4X16BIT,2X32BIT SELECTABLE,COMMON GATE,NIM LEVELS)	QS-003/100	TECHCAL	1	11/71	
	CAMAC SCALER(4X16BIT,2X32BIT SELECTABLE, 30MHZ,COMMON GATE,LAM MASK,TTL AND NIM)	C-Z4-16	WENZEL ELEKTRONIK	1	11/71	
	QUAD SCALER (4X24BIT,150/125MHZ,DATAWAY AND/OR EXT FAST INHIBIT,NIM LEVELS)	S424	EG+G	1	/71	
	QUAD 100MHZ SCALER (4X24BIT,DISCR LEVEL -0.5V,TIME-INTERVAL APPL,NIM INHIB I/P)	84	JORWAY	1	03/71	(2)
	QUAD 100 MHZ SCALER(4X16/24BIT,-0.5V I/P THRESHOLD,COMMON EXT FAST INHIBIT,NIM)	2550B	LRS-LECROY	1	08/70	
	QUAD COUNTING REGISTER(4X24BIT,NIM INPUT TTL INHIBIT IN,TTL CARRY AND OVF OUT)	709-2	NUCL. ENTERPRISES	1	/71	
	DUAL COUNTING REGISTER (2X4 DECADES, SEPARATE EXT INHIBIT AND RESET,OVF OUT)	700-1	NUCL. ENTERPRISES	1	/71	
	DUAL COUNTING REGISTER (2X3 DECADES, SEPARATE EXT INHIBIT AND RESET,OVF OUT)	7040-1	NUCL. ENTERPRISES	1	/70	
	DOUBLE ECHELLE 6 DECADES-100 MHZ A AFFICHAGE REPORTE(SCALER WITH REG O/P)	J EA 10	SAIP-CRC	1	11/71	
N	QUAD SIX-DECADE COUNTER WITH VARIABLE THRESHOLD AND INPUT FILTER, SLOW)	1007	BORER	1	/72	(4)
	QUAD BCD SCALER (4X6 DECADES,30MHZ)	9021	NUCL. ENTERPRISES	0	/71	
	OCTAL SCALER (12BITS,8 INPUTS,50MHZ,EACH SCALER GIVES EXT INHIBIT,NIM LEVELS)	S812	EG+G	1	/71	
	BIDIRECTIONAL COUNTING REGISTER (20BIT,WITH SIGN AND OVERFLOW)	7071-1	NUCL. ENTERPRISES	C	/71	
	DUAL COORDINATE RECORDER	XYRCDR/042	SAIP-CRC	1	10/70	
	DUAL INCREMENTAL POSITION ENCODER (2X20 BIT X-Y DIGITIZATION BY UP-DOWN COUNTER)	2IPE 2019	SEN	1	04/71	

PRESET COUNTING MODULES (Scalers, Timers)

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	24BIT BCD PRESET-SCALER/TIMER (10MHZ,NIM OR TTL INPUTS,MANUAL OR DATAWAY PRESET)	FHC 1301A	BF VERTRIEB	2	01/71	(1)
	24BIT BCD PRESET-SCALER/TIMER (10MHZ,NIM OR TTL INPUTS,DATAWAY PRESET)	FHC 1302A	BF VERTRIEB	1	01/71	(1)
	PRESET COUNTING REGISTER (16BIT,10MHZ, NIM/TTL I/P,TTL INHIB + O/P,DATAWAY SET)	7039-1	NUCL. ENTERPRISES	1	/70	
N	SCALER 50 MHZ (12/16/18/24BIT,PRESET WITH OVF LINE,CONSTANT DEADTIME)	C 76451-A3	SIEMENS	1	01/72	
N	SCALER 300 MHZ (12/16/18/24BIT,PRESET WITH OVF LINE,CONSTANT DEADTIME)	C 76451-A11	SIEMENS	1	01/72	
	PRESET SCALER(24BIT,30MHZ,DATAWAY PRESET COUNT/TIME,INPUT GATED,NIM LEVELS)	1001	BORER	1	06/71	(1)
	PRESET COUNTING REGISTER (24BIT,10MHZ, DATAWAY SET,NIM/TTL INPUT,TTL O/P+INHIB)	703-1	NUCL. ENTERPRISES	1	/71	
	REAL TIME CLOCK (NEEDS EXT CLOCK,MAX 100 DAYS PERIOD WITH 1HZ PULSES IN,TTL I/O)	712	NUCL. ENTERPRISES	1	/71	
	CAMAC PRESET-SCALER(24BIT,30MHZ,NIM SIGNAL AND GATE,EXT INHIBIT,MAN RESET)	C-ZE-24 K	WENZEL ELEKTRONIK	1	11/71	
	PRESET SCALER(10MHZ,8 DECADE BCD,DISPLAY OF 2 SIGNIF NUMBERS+EXP,MAN PRESET,NIM)	C 103	RDT	3	06/71	
	ECHELLE 6 DECADES A PRESELECTION(SCALER, MAN/DATAWAY PRESET,1MHZ,START/STOP O/P)	J EP 20	SAIP-CRC	2	01/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	PARALLEL INPUT REGISTERS					
	PARALLEL-INPUT-REGISTER (SINGLE 16/24BIT OPTION,READY SIGNALS,I/O TTL,ADC APPL)	MS PI 1 1230/1	AEG-TELEFUNKEN	1	10/70	(1)
	PARALLEL-INPUT-REGISTER (SINGLE 16/24BIT OPT,READY SIGNALS,I/O TTL,CONTROL BUS)	MS PI 2 1230/1	AEG-TELEFUNKEN	1	10/70	(1)
	PARALLEL REGISTER (SINGLE 16BIT INDICAT, 50NS OVERLAP REQUIRED,TTL LEVELS)	PR 1601-1	GEC-ELLIOTT	1	06/71	
	PRIORITY INPUT REGISTER(12BITS ORED TO LAM,FAST COINC LATCH APPL,NIM LEVELS)	63	JORWAY	2	10/70	
N	INPUT REGISTER 24-BIT	3470	KINETIC SYSTEMS	1	/71	(4)
N	INTERRUPT REQUEST REGISTER	EC 218	NUCL. ENTERPRISES	0		
	INTERRUPT REQUEST REGISTER (8BIT, TTL INPUTS TO REGISTER,ANY INPUT GIVES LAM.	7013-1	NUCL. ENTERPRISES	1	/70	
	PARALLEL INPUT REGISTER (16BIT,CONTINUOUS OR STROBED MODES CONTROLLED BY REG)	7014-1	NUCL. ENTERPRISES	1	/70	
	STROBED INPUT REGISTER (12BIT COINC AND LATCH,NIM LEVELS,PATTERN AND L-REQ APPL)	SIR 2026	SEN	1	/70	
	INPUT REGISTER (24BIT,NON-ZERO CONTENT SETS LAM,REGISTER E/D FROM DATAWAY)	FHC 1308A	BF VERTRIEB	1	11/71	
	UNIVERSAL INPUT/OUTPUT REGISTER (36BIT DATA+RANGE IN,12BIT REG O/P FOR CONTROL)	1031	BORER	1	05/72	(3)
	24-BIT STATUS CHANGE/ALARM REGISTER (STATUS COMPARED,CHANGE GIVES LAM)	1051	BORER	1	05/72	(3)
	PARALLEL REGISTER (DUAL 16BIT INDICAT, 6NS OVERLAP REQUIRED,NIM LEVELS)	PR 1602	GEC-ELLIOTT	2	01/71	
	DUAL PARALLEL REGISTER (2X16BIT INDICAT, 6NS OVERLAP REQUIRED,NIM LEVELS)	PR 1604	GEC-ELLIOTT	3	01/71	
	DUAL 16 BIT INPUT REGISTER(EXT STROBE OR DATAWAY COMMAND STORES DATA,TTL LEVELS)	2IR 2010	SEN	1	/70	
	DUAL 16 BIT INPUT REGISTER(CONTINUOUS, STROBED AND ONE-STROBE DATA ENTRY,TTL)	PR-602	TECHCAL	1	11/71	
N	DUAL 16 BIT PARALLEL INPUT REGISTER (WITH LED DISPLAY OPTION)	PR-604	TECHCAL	0	/72	
N	DUAL 24 BIT INPUT REGISTER	RI-224	EG+G	1	/72	
	DUAL PARALLEL INPUT REGISTER(2X24BIT,EXT LOAD REQUEST,4 OPER MODES,TTL LEVELS)	60	JORWAY	1	10/70	
	COINCIDENCE BUFFER (2X12BIT,ONE STROBE PER 12BITS,MIN 2NS OVERLAP,NIM INPUTS)	C212	EG+G	2	/71	
	FAST COINCIDENCE LATCH(16BIT,DISCR I/P, MIN 2 NSEC STROBE-SIGNAL OVERLAP)	64	JORWAY	1	01/71	(1)
	16 FOLD DCR(I/P DISCR,STROBE-INPUT OVERLAP 2NSEC,CH1-8 AND CH9-16 SUM O/P,NIM)	2340A	LRS-LECROY	2	05/71	(2)
	16-CH COINCIDENCE REGISTER (16 CHANNELS, STROBE-INPUT OVERLAP 2NSEC,NIM LEVELS)	2341	LRS-LECROY	2	01/71	(4)
	PATTERN UNIT (16 INDIV NIM INPUTS,COMMON NIM GATE)	021	NUCL. ENTERPRISES	2	/71	
	PATTERN UNIT(16BIT,I/P STROBED WITH COMMON GATE,10 NSEC OVERLAP,NIM LEVELS)	C 101	RDT	2	06/71	
	PATTERN UNIT 16 BIT (16 INDIVIDUAL NIM INPUTS,COMMON NIM GATE)	16P 2007	SEN	2	/70	
	PARALLEL INPUT GATES (Dataway connecting)					
N	PARALLEL INPUT GATE (3X16BIT INPUT FROM ISOLATING CONTACTS)	1061	BORER	1	05/72	(4)
N	INPUT GATE 24-BIT	3420	KINETIC SYSTEMS	1	/71	(4)
	PARALLEL INPUT GATE (16 BIT,TTL INPUT, 1 USEC INTEGRATION OF INPUTS)	7017-1	NUCL. ENTERPRISES	1	/70	
	PARALLEL INPUT GATE (16BIT,TTL INPUT,EXT STROBE TO INPUT GATES)	7018-1	NUCL. ENTERPRISES	1	/70	
	INPUT DATA GATE (24BIT NEGATIVE LOGIC TTL INPUT,1=LOW)	713	NUCL. ENTERPRISES	1	/71	
	INPUT DATA GATE (24BIT POSITIVE LOGIC TTL INPUT,1=HIGH)	714	NUCL. ENTERPRISES	1	/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	PARALLEL INPUT GATE (24BIT STATIC DATA, INTEGRATED FOR 1 USEC,TTL LEVELS)	7059-1	NUCL. ENTERPRISES	1	/70	
	PARALLEL INPUT GATE (22BIT STATIC DATA, 500 NSEC INTEGRATION,STROBE SETS L,TTL)	7060-1	NUCL. ENTERPRISES	1	/70	
	DIGITALES EINGANGSREGISTER(5X8BIT PARALL INPUT GATES,5TH BYTE SETS L,TTL,1=H)	DO 0200-2001	DORNIER	1	11/71	
	DIGITALES EINGANGSREGISTER(5X8BIT PARALL INPUT GATES,5TH BYTE SETS L,HLL,1=H)	DO 0200-2002	DORNIER	1	11/71	
	DIGITALES EINGANGSREGISTER MIT OPTOKOPP-LER(4X8BIT PARALLEL INPUT GATES,WITH L)	DO 0200-2003	DORNIER	1	11/71	
	DUAL PARALLEL STROBED INPUT GATE(2X24BIT HANDSHAKE MODE TRANSFER TO DATAWAY,TTL)	61	JORWAY	1	10/70	
	DUAL PARALLEL INPUT GATE (2X24BIT,NON-INTERLOCK CONTROL TRANSF TO DATAWAY,TTL)	61-1	JORWAY	1	10/70	

MANUAL INPUT MODULES

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	PARAMETER UNIT 12 BIT (PROVIDES 12 BIT COMMUNICATION,PUSH BUTTON L-REQUEST)	P 2005	SEN	1	/70	
N	24 BIT WORD GENERATOR	WRG-24	TECHCAL	0	/72	
	WORD GENERATOR (24BIT WORD MANUALLY SET BY SWITCHES)	WG 2401	GEC-ELLIOTT	1	01/71	
	PARAMETER UNIT (QUAD 4-DECADE BCD PARAMETERS MANUALLY SET)	022	NUCL. ENTERPRISES	4	/71	(2)
	WORD GENERATOR (24 BITS OF BINARY DATA, SWITCH SELECTED)	9020	NUCL. ENTERPRISES	1	/71	(2)
	PARAMETER UNIT (QUAD 4 DECADE BCD PARAMETERS MANUALLY SET)	C 105	RDT	4	06/71	

DATA STORAGE MODULES

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
N	16 WORD STORE	CS 0003	NUCL. ENTERPRISES	1		(4)
	QUAD REGISTER (4X16BIT BCD OR BIN,LOAD, CLEAR AND INCREMENT VIA DATAWAY)	716-2	NUCL. ENTERPRISES	1	/71	
	QUAD REGISTER (4X24BIT BCD OR BIN,LOAD, CLEAR AND INCREMENT VIA DATAWAY)	717-2	NUCL. ENTERPRISES	1	/71	
	MEMOIRE TAMPON (BUFFER MEMORY,256 13BIT BYTES,USED WITH J CAN 20C/H)	J MT 10	SAIP-CRC	1	11/71	

PARALLEL OUTPUT MODULES

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	12 BIT OUTPUT REGISTER(DC OR PULSE O/P, UPDATING STROBE OUTPUT,NIM LEVELS)	41	JORWAY	1	03/71	(2)
N	OUTPUT REGISTER 12-BIT ISOLATED RELAY	3086	KINETIC SYSTEMS	1	/71	(4)
N	OUTPUT REGISTER 24-BIT	3071	KINETIC SYSTEMS	1	/71	
	OUTPUT REGISTER (12BIT, NIM PULSES OR LEVELS OUT)	OR 2027	SEN	1	/70	
	PARALLEL OUTPUT REGISTER (24BIT TTL OUTPUT VIA 25-WAY CONNECTOR)	7054-3	NUCL. ENTERPRISES	1	/70	
N	OUTPUT REGISTER (2X16BIT VIA ISOLATING CONTACTS)	1082	BORER	1	05/72	(4)
	DIGITALES AUSGANGSREGISTER(4X8BIT PARALL OUTPUT REGISTER,NO L,TTL,1=H)	DO 0200-2501	DORNIER	1	11/71	
	DIGITALES AUSGANGSREGISTER(4X8BIT PARALL OUTPUT REGISTER,NO L,OPEN COLL O/P,1=H)	DO 0200-2502	DORNIER	1	11/71	
	DIGITALES AUSGANGSREGISTER(4X8BIT PARALL OUTPUT REGISTER,NO L,OPEN COLL O/P,1=L)	DO 0200-2503	DORNIER	1	11/71	
	DUAL 16 BIT OUTPUT REGISTER (TTL LEVELS, OPEN COLL OUTPUTS VIA CABLE)	2OR 2008	SEN	1	/70	
	PARALLEL-OUTPUT-REGISTER (DUAL 24BIT, OR QUAD 12BIT,OPEN COLLECTOR OUTPUT)	MS PO 1 1230/1	AEG-TELEFUNKEN	1	10/70	(4)
N	OUTPUT REGISTER (2X24BIT DATA OUT,DATA-READY + BUSY FORM HANDSHAKE, TTL)	RO-224	EG+G	1	/72	
	DUAL 24 BIT OUTPUT REGISTER(DC OR PULSE O/P,UPDATING O/P STROBE,TTL OPEN COLL)	40	JORWAY	1	07/71	(2)
	DIGITALES AUSGANGSREGISTER MIT REED-RELAIS(4X8BIT OUTPUT REG,OPEN CONTACT=0)	DO 0200-2504	DORNIER	2	11/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
C	OUTPUT DRIVER (2X16BIT, 150 MA SINKING)	CD 1601	GEC-ELLIOTT	1	06/71	(1)
C	OUTPUT DRIVER (2X16BIT, 40 MA SINKING)	CD 1605	GEC-ELLIOTT	1	06/71	(1)
	DRIVER(8BIT OUTPUT VIA 15-WAY CONNECTOR, 150MA SINKING CAPABILITY,MAX 6V)	7016-1	NUCL. ENTERPRISES	1	/70	
	SWITCH (12BIT DATAWAY CONTROLLED RELAY REGISTER FOR SWITCHING AND MULTIPLEXING)	7066-1	NUCL. ENTERPRISES	1	/71	
	DRIVER (16BIT,OPEN COLLECTOR OUTPUT VIA MULTIWAY CONNECTOR,MAX 150MA/LINE)	9002	NUCL. ENTERPRISES	1	/71	
	DRIVER (24BIT OUTPUT REGISTER,SET AND READ BY COMMAND,24BIT I/P DATA ACCEPTED)	9013	NUCL. ENTERPRISES	1	/71	
	DRIVER (24BIT OUTPUT REGISTER,SET AND READ BY COMMAND,24BIT I/P DATA ACCEPTED)	9017	NUCL. ENTERPRISES	1	/71	(1)

DISPLAY MODULES AND UNITS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	DISPLAY (24BIT BCD DISPLAY OF ONE SCALER FHC1301/02,SPEC CONNECTION TO SCALER)	FHC 1305A	BF VERTRIEB	1	01/71	(1)
	DISPLAY (6 DECADE NIXIE FOR ONE OF 12 SCALERS FHC1301/02,SPEC BUS TO SCALERS)	FHC 1306A	BF VERTRIEB	2	01/71	(1)
	CRT DECIMAL DISPLAY SYSTEM (INCLUDING)	72A	JORWAY	NA	07/71	(2)
	DISPLAY DRIVER	72A		3		
N	DISPLAY SYSTEM COMPRISING		KINETIC SYSTEMS		/71	(4)
N	DISPLAY SYNCHRONIZING	3200		1	/71	
N	DISPLAY TIMING	3205		1	/71	
N	DISPLAY CONTROL	3210		1	/71	
N	DISPLAY REFRESH (ALPHANUMERIC + GRAPHS)	3212		1	/71	
	DIGITAL DISPLAY (PART OF 7000-SER MULTICRATE SYSTEM)	0705-1	NUCL. ENTERPRISES	NA	/71	(2)
	DISPLAY DRIVER (TWO 10BIT DAC,OUTPUT RANGE +5V TO -5V,TWO OPERATION MODES)	7011-2	NUCL. ENTERPRISES	2	/70	(1)
	DECIMAL DISPLAY UNIT (ADDRESS AND 5 DATA DECADES + MULTIPLIER DISPLAYED)	9007	NUCL. ENTERPRISES	NA	/71	
	DISPLAY CONTROLLER (FOR 9007,INCLUDES BIN TO DECIMAL CONVERTER)	9006		2	/71	
	INDICATOR (1X16BIT OR 2X8BIT,INDICATES STATE OF REGISTER LOADED FROM DATAWAY)	9014	NUCL. ENTERPRISES	1	/71	
	STORAGE OSCILLOSCOPE (DRIVER FOR TEKTRONIX 611 OR 601,USED WITH 7011)	9028	NUCL. ENTERPRISES	C	/71	(2)
	AFFICHAGE DECIMAL PAR L'INTERMEDIAIRE D' UN CALCULATEUR (DISPLAY OF 24BIT WORD)	J AF 15	SAIP-CRC	2	01/71	
	AFFICHAGE BINAIRE MANUEL (CONTENT OF A REGISTER DISPLAYED,EXT MULTIWAY CONN)	J AF 20	SAIP-CRC	1	01/71	
	SCOPE DISPLAY DRIVER X-Y-Z (SYSTEM)	FDD 2012	SEN	1	04/71	(1)
	STORAGE DISPLAY DRIVER FOR TEKTRONIX 611 OR 601	SDD2015		1	04/71	(1)
	CHARACTER GENERATOR	CG 2018		1	04/71	(1)
	VECTOR GENERATOR	VG 2028		1	05/71	(1)

PERIPHERAL INPUT/OUTPUT MODULES

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	TYPEWRITER DRIVE UNIT	TD 0801	GEC-ELLIOTT	0	08/71	(1)
	INPUT-OUTPUT-INTERFACE(TELETYPE-DATAWAY I/O TRANSF OR 12 SCALER O/P ON SPEC BUS)	FHC 1307A	BF VERTRIEB	2	01/71	(1)
	TELETYPE INTERFACE	90	JORWAY	C	10/71	
	TELETYPEWRITER DRIVER (FOR ASR 33)	7043-1	NUCL. ENTERPRISES	1	/70	
	TELETYPEWRITER INTERFACE(I/O DATA TRANSF AND CONTROL,LAM USED AS TWO-WAY FLAG)	7061-1	NUCL. ENTERPRISES	1	/70	(1)
	TELETYPEWRITER TERMINAL	TWTML/045	SAIP-CRC	1	10/70	
	PAPER TAPE PUNCH OUTPUT DRIVER (FOR FACIT 4070)	TP 0801	GEC-ELLIOTT	1	06/71	(1)
	TAPE READER INTERFACE UNIT (FOR ELECTROGRAPHIC READER)	TR 0801	GEC-ELLIOTT	1	01/71	(1)
N	STEPPING MOTOR CONTROLLER	3360	KINETIC SYSTEMS	1	/72	(4)
	STEPPING MOTOR DRIVERS (USED WITH 7045)	0707,8,9,10	NUCL. ENTERPRISES	1	/71	
	B.S.INTERFACE READER (8BIT DATA + PARITY BIT,BRITISH STANDARD)	7057-1	NUCL. ENTERPRISES	1	/71	
	B.S.INTERFACE DRIVER (8BIT DATA + PARITY BIT,BRITISH STANDARD)	7058-1	NUCL. ENTERPRISES	1	/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	PERIPHERAL READER(8BIT PARALLEL DATA IN, NEG OR POS TTL,HANDSHAKE CONTROLS)	7064-1	NUCL. ENTERPRISES	1	/71	
	PERIPHERAL DRIVER (8BIT DATA OUT,NEG OR POS TTL,HANDSHAKE CONTROLS)	7065-1	NUCL. ENTERPRISES	1	/71	
	UNIVERSAL INPUT/OUTPUT REGISTER (36BIT DATA+RANGE IN,12BIT REG O/P FOR CONTROL)	1031	BORER	1	05/72	(3)
	INTERFACE CAMAC POUR CODEUR CA25/CA13/ C97 (INTERFACING PULSE ADC TO CAMAC)	J CCA 10	SAIP-CRC	2	01/71	
	STEP MOTOR DRIVER (MAX 32768 STEPS,RATE, ROTATION AND START/STOP FULLY COMMANDED)	1161	BORER	1	06/72	(3)
	OUTPUT REGISTER (16 OR 24 BIT TTL DRIVER FOR FAST-ROUTING MULTIPLEXER SYSTEM)	CM 665	J AND P	1	07/71	
	DELAYED PULSE GENERATOR (4 TTL O/P,0.042 HZ-40KHZ RATE,LEVEL AND DIRECTION CONTR)	7045-1	NUCL. ENTERPRISES	1	/70	
	MCA INTERFACE (I/O MODULE FOR MULTI-CHANNEL ANALYSER)		PACKARD	3		(4)
	PROPORTIONAL CHAMBER READ-OUT (USED WITH SPEC CONTROLLER TYPE COFIL OR ALONE)	REFIL	SAIP-CRC	2	/71	
	SEQUENTIAL OUTPUT REGISTER (SERIAL-CODED NIM PULSES OUT,LOGIC 0=40NSEC,1=150NSEC)	SOR	SAIP-CRC	1	/71	
	SEQUENTIAL INPUT REGISTER(16 8BIT BYTES, STORES CODED NIM PULSES,0=40,1=150NSEC)	SIRE	SAIP-CRC	1	/71	
C	SPARK CHAMBER READ OUT (POSITION AND ADDRESS CODING OF MULTIPLE SPARK SITES)	SCRO-041	SAIP-CRC	2	10/70	
	SPARK CHAMBER READ OUT TERMINAL	SCRO TML-043		5	10/70	
C	PLUMBICON READ OUT (5 SCALERS RECORD DIGITIZED OUTPUTS FROM PLUMBICON CAMERA)	PLUM	SAIP-CRC	1	/71	
	PLUMBICON READ OUT TERMINAL	PUDDING		1	/71	
	DUAL INCREMENTAL POSITION ENCODER (2X20 BIT X-Y DIGITIZATION BY UP-DOWN COUNTER)	2IPE 2019	SEN	1	04/71	
	LIGHT PEN FOR FDD 2012 OR CD 2018	LP 2035	SEN	NA	06/71	
	CAMAC COMMUNICATIONS CONTROLLER INTERFACE UNIT	MC 4036	MICRO CONSULTANTS	1	08/71	(2)
	CAMAC VID-MOS INTERFACE UNIT	MC 4037	MICRO CONSULTANTS	1	08/71	(2)
	CAMAC MOD 15 INTERFACE UNIT	MC 4038	MICRO CONSULTANTS	1	08/71	(2)

MULTIPLEXERS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	15 CHANNEL MULTIPLEXER (ANALOGUE SIGNALS ROUTED TO ADC/DVM,DIRECT + SCAN MODES)	1701	BORER	1	05/72	(3)
N	32-CHANNEL FAST MULTIPLEXER (FET SWITCHES FOR ADC 1242)	1703	BORER	1	06/72	(4)
N	16-CHANNEL FAST MULTIPLEXER (FET SWITCHES FOR ADC 1242)	1704	BORER	1	06/72	(4)
	ELEKTRONISCHER MULTIPLEXER (16 CHANNELS, +OR-10V RANGE,DATAWAY SET + INCR ADDR)	DO 0200-1031	DORNIER	2	11/71	
	ELEKTRONISCHER MULTIPLEXER (32 CHANNELS, +OR-10V RANGE,DATAWAY SET + INCR ADDR)	DO 0200-1032	DORNIER	2	11/71	
	ELEKTRONISCHER MULTIPLEXER(16 DIFF I/P, +OR-10V RANGE,DATAWAY SET+INCR ADDRESS)	DO 0200-1033	DORNIER	3	11/71	
	ELEKTRONISCHER MULTIPLEXER(32 DIFF I/P, +OR-10V RANGE,DATAWAY SET+INCR ADDRESS)	DO 0200-1034	DORNIER	3	11/71	
	RELAISMULTIPLEXER (16 CHANNELS,MAX 200V/ 750MA OR 10VA, DATAWAY SET+INCR ADDRESS)	DO 0200-1035	DORNIER	2	11/71	
	MULTIPLEXER-SOLID STATE (16 SINGLE-ENDED OR 8 DIFF CHAN,RANDOM OR SEQUENT ACCESS)	9026	NUCL. ENTERPRISES	1	/71	
N	MULTIPLEXER (32 CHANNELS, I OR 4 WAYS)		SIEMENS	2		

CODE CONVERTERS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	BINARY TO-BCD-CONVERTER (24BIT BIN,8 DECIMAL DIGIT OUTPUT VIA TWO CONNECTORS)	7068-1	NUCL. ENTERPRISES	1	/70	(2)
	BINARY TO BCD-CONVERTER(24BIT TO 8 DECA-DE,DISPLAY,CONV 4USEC,TTL LEVEL OUT,1=H)	C-BBC-2	WENZEL ELEKTRONIK	2	11/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	ANALOGUE-TO-DIGITAL CONVERTERS (ADC, DVM)					
	ANALOGE EINGAENGE(MULTIPLEXER-ADC,8 I/P TO ONE ADC,+OR-10V RANGE,8BITS/20V)	DO 0200-1011	DORNIER	2	11/71	
	ANALOGE EINGAENGE(MULTIPLEXER-ADC,16 I/P TO ONE ADC,+OR-10V RANGE,12BITS/20V)	DO 0200-1012	DORNIER	2	11/71	
	8-BIT ADC (10 MICROSECS)	ADC 0801	GEC-ELLIOTT	0	06/71	(1)
	MULTI-MODE LINEAR ADC (8BIT,40MHZ CLOCK, AREA AND PEAK MODES,NIM LEVELS)	2243A	LRS-LECROY	1	08/70	(2)
	OCTAL ADC (8 FAST I/P,8BIT/CH, 150USEC CONVERSION,COMMON GATE,NIM LEVELS)	2248	LRS-LECROY	1	10/71	
N	OCTAL ADC (MIN 5 NSEC PULSES, POS OR NEG 8BIT/100 PC RESOLUTION, 250 USEC CONV)	9040	NUCL. ENTERPRISES	1		(4)
	ANALOGUE TO DIGITAL CONVERTER(8BIT, I/P RANGE 0 TO +5V OR 0 TO -5V,25 USEC CONV)	7028-1	NUCL. ENTERPRISES	1	/70	
	CONVERTISSEUR ANALOGIQUE NUMERIQUE A 512 CANAUX(PULSE ADC,10MHZ CLOCK,0.1/10V)	J CAN 31	SAIP-CRC	3	01/71	
N	DIGITALVOLTMETER (RANGES: DC0.02 TO 20V, 5 MA TO 100 MA,AC 0.01 TO 20 V BOTH POL)		SIEMENS	2		
	10-BIT ADC (13 MICROSECS)	ADC 1001	GEC-ELLIOTT	C	06/71	(1)
	DUAL SLOPE ADC (+AND- 0.01/1/10V RANGES, 11BIT RESOLUTION,20MS CONV TIME)	1241	BORER	2	05/72	(3)
N	FAST ADC (11BIT+SIGN, +AND- 10V DIFF IN, 20 USEC CONVERSION)	1242	BORER	2	06/72	(4)
	ANALOGE EINGAENGE (MULTIPLEXER-ADC,8 I/P TO ONE ADC, +OR-10V RANGE,12BITS/20V)	DO 0200-1001	DORNIER	2	11/71	
	ANALOGE EINGAENGE(MULTIPLEXER-ADC,16 I/P TO ONE ADC, +OR-10V RANGE,12BITS/20V)	DO 0200-1002	DORNIER	2	11/71	
	ANALOGE EINGAENGE(MULTIPLEXER-ADC,8 DIFF I/P TO ONE ADC,+OR-10V RANGE,12BITS/20V)	DO 0200-1003	DORNIER	2	11/71	
	ANALOGE EINGAENGE(MULTIPLEXER-ADC,8 DIFF I/P TO ONE ADC,+OR-10V RANGE,12BITS/20V)	DO 0200-1004	DORNIER	2	11/71	
C	ANALOGUE TO DIGITAL INTERFACE (12,10 OR 8 BIT, 20 USEC CONVERSION)	ADC 1201	GEC-ELLIOTT	1	06/71	(1)
	A/D CONVERTER (12BIT,MAX 20 USEC CONVERSION, +AND-5V, +AND-10V, +10V RANGES)	30	JORWAY	2	06/71	(2)
	ANALOGUE TO DIGITAL CONVERTER (12BIT, 20 MSEC CONVERSION,RANGE -5V TO +5V)	7055-1	NUCL. ENTERPRISES	1	/70	
	ANALOGER EINGANG(DUAL SLOPE 15BIT ADC, +OR-10V RANGE,0.1 SEC CONVERSION)	DO 0200-1021	DORNIER	1	11/71	
	CONVERTISSEUR ANALOGIQUE NUMERIQUE RAPIDE A 8000 CANAUX(PULSE ADC,100MHZ CLOCK)	JCAN20C/JCAN20H	SAIP-CRC	6	01/71	
	INTERFACE POUR CODEUR J CAN 20 ET BLOC MEMOIRE BM 96 (ADC-MEMORY INTERFACE)	J CAN 20 I	SAIP-CRC	2	01/71	
	DIGITAL-TO-ANALOGUE CONVERTERS (DAC)					
	ANALOGE AUSGAENGE (DAC,12BIT RESOLUTION, +OR-10V OUTPUT RANGE)	DO 0200-1501	DORNIER	2	11/71	
	ANALOGE AUSGAENGE (DAC,12BIT RESOLUTION, +OR-10V OUTPUT RANGE,2 OUTPUTS)	DO 0200-1502	DORNIER	2	11/71	
	D/A CONVERTER (12BIT,5 USEC CONVERSION, O/P RANGES +AND-2.5V/5V/10V AND +5V/10V)	31	JORWAY	1	06/71	(2)
	DIGITAL TO ANALOGUE CONVERTER (8BIT,OUTPUT RANGE 0 TO +5V OR 0 TO -5V)	7015-1	NUCL. ENTERPRISES	1	/70	
	DUAL DIGITAL-TO-ANALOG CONVERTER (10BIT, OUTPUT 0 TO +10V OR -5 TO +5V)	2DAC 2011	SEN	1	04/71	
	DUAL DIGITAL TO ANALOG CONVERTER (10BIT RESOLUTION,10MSEC CONV TIME,O/P 5V MAX)	DA-2000	TECHCAL	1	11/71	

	N/C DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	TIME-TO-DIGITAL CONVERTERS					
	QUAD CAMAC SCALER (4X16BIT OR 2X32BIT, 40MHZ)	1004	BORER	1	03/72	
	TIME-TO-DIGITAL CONVERTER(4X14BIT,CLOCK RATE 20MHZ,QUAD/DUAL/SINGLE CONFIG)	1005	BORER	1	/70	
	QUAD 16-BIT SPARK READ-OUT REGISTER (20MHZ RATE,TTL LEVELS)	SR 1604	GEC-ELLIOTT	1	01/71	
	QUAD TIME-TO-DIGITAL CONVERTER(9BIT/CH, 102/510NSEC RANGES,13USEC CONVERS,NIM)	2226A	LRS-LECROY	1	10/70	(2)
	TIME DIGITIZER(5X16BIT,CLOCK RATE 40MHZ, WITH CENTER FINDING LOGIC)	TD 2031	SEN	1	02/72	
	TIME DIGITIZER (4X16BIT,CLOCK RATE 70/85MHZ,NIM LEVELS)	TD 2041	SEN	1	02/72	(4)
	OTHER ANALOGUE AND/OR DIGITAL MODULES					
	FAN-OUT UNIT (2 ORED INPUTS PROVIDE 8 TRUE,2 COMPLEM OUTPUTS,NIM SIGNALS)	FO 0801	GEC-ELLIOTT	1	01/71	
N	POWER SUPPLY CONTROLLER 10-BIT	3155-10	KINETIC SYSTEMS	1	/71	(4)
	HEX IL2 TO IL1 CONVERTER (6 NIM SIGNALS IN,6 TTL SIGNALS OUT)	7051-1	NUCL. ENTERPRISES	1	/70	
	HEX IL1 TO IL2 CONVERTER (6 TTL SIGNALS IN,6 NIM SIGNALS OUT)	7052-1	NUCL. ENTERPRISES	1	/70	
	QUIN L1 TO IL1 CONVERTER(5 HARWELL STANDARD L1 SIGNALS IN 5 TTL SIGNALS OUT)	7053-1	NUCL. ENTERPRISES	1	/70	
	DIFFERENTIAL AMPLIFIER (RANGES +0.1V TO -0.1V AND 0.5/5/50/500C BOTH POLARITIES)	9027	NUCL. ENTERPRISES	2	/71	
	SIX-FOLD CONTROLLED GATE (INDIV GATING, FAN-IN AND FAN-OUT CONTROLLED BY 3 REGS)	6CG 2017	SEN	1	11/71	(4)
N	STROMGENERATOR (CURRENT SOURCE)		SIEMENS	2		
	PULSE GENERATORS AND CLOCKS					
	TIMER (1HZ TO 1MHZ PULSES-7 DECADES-OVER 7 TTL OUTPUTS,LAM BY 1,10 OR 100 HZ)	FHC 1303A	BF VERTRIEB	1	01/71	(1)
	CLOCK/TIMER (0.001S TO 10 HRS TIME INTERVAL,REAL-TIME OUTPUT)	1411	BORER	1	05/72	(3)
	CRYSTAL CONTROLLED PULSE GENERATOR(7 DECADES-1HZ TO 1MHZ-500NS PULSES OUT,TTL)	PG 0001	GEC-ELLIOTT	1	01/71	
	FAST TEST PULSE GENERATOR (5 TO 50NS NIM O/P PULSE DERIVED FROM S1.F(25) OR EXT)	TPG 0202	GEC-ELLIOTT	1	01/71	
	CLOCK PULSE GENERATOR (7 OUTPUTS-1HZ TO 1MHZ-IN DECADE STEPS,10MHZ EXT IN,TTL)	7019-1	NUCL. ENTERPRISES	1	/70	
	CLOCK PULSE GENERATOR(7 DECADES-1HZ TO 1MHZ-500 NSEC PULSES OUT,TTL)	C 109	RDT	1	11/71	
	HORLOGE A QUARTZ 1 MHZ(CLOCK,7 O/P-1HZ TO 1MHZ-200 TO 800 NSEC WIDTH,TTL LEVEL)	J HQ 10	SAIP-CRC	1	01/71	
	REAL TIME CLOCK (3.8 USEC TO 18.2 HRS, PRESET-TIME AND PRESET-COUNT MODES)	RTC 2014	SEN	1	04/71	
	DUAL PROGRAMMED PULSE GENERATOR(50HZ/ 2KHZ/5MHZ PULSE TRAIN,LENGTH BY COMMAND)	2PPG 2016	SEN	1	04/71	
	TIME BASE (70 MHZ, USED WITH TD 2031 AND TD 2041)	TB 2032	SEN	0	11/71	
N	MULTIPULSER (0.5-300 MHZ BURSTS,NIM SIGNAL,TTL TRIGGER,NIM OUT,600PSEC RISE)	C 72454-A1450-A1	SIEMENS	2	/72	
	CAMAC-CLOCK-GENERATOR(7 DECADES-10MHZ TO 1HZ,50/500 NSEC O/P PULSES,2.8V/50 OHMS)	C-CG-10	WENZEL ELEKTRONIK	1	11/71	
N	STEPPING MOTOR CONTROLLER	3360	KINETIC SYSTEMS	1	/72	(4)

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	LOGIC FUNCTION MODULES					
	DUAL GATE (4 INPUTS/GATE,LOGICAL AND/OR, NAND/NOR PERFORMED UNDER CONTROL)	7020-1	NUCL. ENTERPRISES	1	/70	
	FAN-OUT (3 INPUTS IN LOGICAL COMBINATION A.OR.B,A.OR.C,EACH WITH FAN-OUT OF 4)	7021-1	NUCL. ENTERPRISES	1	/70	
	SIX-FOLD CONTROLLED GATE (INDIV GATING, FAN-IN AND FAN-OUT CONTROLLED BY 3 REGS)	6CG 2017	SEN	1	11/71	(4)
	DELAY AND ATTENUATOR UNITS					
	DUAL ATTENUATOR(50 OHMS,DATAWAY CONTROL-LED,RANGE 0DB TO 31DB IN 1DB STEPS)	9004	NUCL. ENTERPRISES	1	/71	
	ATTENUATEUR PROGRAMMABLE(MAN AND DATAWAY CONTROL OF ATTENUATION,0 DB TO 60 DB)	J AT 10	SAIP-CRC	3	10/70	
	CRATES- NO POWER, NO DATAWAY					
	CAMAC CRATE (EMPTY)	2.080.000.6	KNUERR	25	10/70	(2)
	CAMAC CRATE (EMPTY,INCL HARDWARE SUPPLY CHASSIS AND VENTILATION PANEL)	2.086.000.6		25		(2)
N	CHASSIS CAMAC (6 UNITES AVEC FENTE DE VENTILATION, 525 MM PROFONDEUR)	9905-1-05	CSL	25	05/71	
N	(360 MM PROFONDEUR)	9905-2-05		25	05/71	
	CHASSIS CAMAC POUR TIROIRS MODULAIRES, VIDES (EMPTY CRATES)		POLON	25	08/71	
	CAMAC SYSTEM BIN (WITH MODULAR SUPPLY)		RO ASSOCIATES	25	03/70	
N	CRATE, EMPTY	C 76455-A3	SIEMENS	25	01/72	
	CHASSIS CAMAC NORMALISE 5U (EMPTY CRATE,360 MM DEEP)	CM 5025 30	TRANSRACK	25	10/70	
	(460 MM DEEP)	CM 5025 40		25		
	(525 MM DEEP)	CM 5025 50		25		
	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,VENTILATION HARDWARE)	CM 5125 30	TRANSRACK	25	10/70	
	(460 MM DEEP)	CM 5125 40		25		
	(525 MM DEEP)	CM 5125 50		25		
	CHASSIS CAMAC 5U UTILES (EMPTY CRATE, TOTAL 6U,360 MM DEEP,WITH ONE FAN)	CM 5125 31	TRANSRACK	25	10/70	
	(460 MM DEEP)	CM 5125 41		25		
	(525 MM DEEP)	CM 5125 51		25		
	CHASSIS CAMAC 5U UTILES (EMPTY CRATE,6U TOTAL,360MM DEEP,WITH TWO FANS)	CM 5125 32	TRANSRACK	25	10/70	
	(460 MM DEEP)	CM 5125 42		25		
	(525 MM DEEP)	CM 5125 52		25		
	CRATE (5U,EMPTY)	MCF/5CAM/S	IMHOF-BEDCO	25	06/71	
	CRATE (6U,EMPTY,WITH VENTILATION BAFFLE,HARWELL TYPE 7000)	MCF/6CAM/SV		25		
	CRATE (6U,EMPTY,WITH VENTILATION BAFFLE AND REMOVABLE PANEL,HARWELL 7000-SER)	MCF/6CAM/SVR		25		
	CAMAC COMPATIBLE CRATE	NSI 875 DB/WV	NUCL. SPECIALTIES	25	02/70	
	VENTILATED CRATE NO POWER NO DATAWAY	CCHN	RDT	25	06/71	
	CAMAC CRATE (5U NON-VENTILATED,380 MM DEEP)	5UCAM	WILLSHER + QUICK	25	10/71	(2)
	(6U VENTILATED,NO FAN,380 MM DEEP)	6UCAM		25		(2)
	(6U VENTILATED RECESSED,NO FAN,430 MM)	6URCAM		25		(2)
	CRATES- WITH DATAWAY, NO POWER					
N	CAMAC-RAHMEN MIT DATENWEG	1250-0001	DUCKERT	25	/72	
	VENTILATED CRATE	VC 001C	GEC-ELLIOTT	24		
	CAMAC CRATE VERDRAHTET (EMPTY CRATE WITH WIRED DATAWAY)	2.084.000.6	KNUERR	25	10/70	(2)
	UNPOWERED CRATE WITH F.P.C. DATAWAY	9	MB METALS	0	01/72	
	CRATE WITH F.P.C. DATAWAY AND POWER RAIL ASSEMBLY	TYPES 1,2,5,6	MB METALS	0	01/72	
	CRATE	7005-2	NUCL. ENTERPRISES	24	/70	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	UNPOWERED CRATE WITH DATAWAY ( )	CM 5125/33/A	SAPHYMC-SRAT	25	/71	
	(360 MM)	CM 5125/33/D		25		
	( )	CM 5125/53/A		25		
	(525 MM)	CM 5125/53/D		25		
	UNPOWERED CRATE WITH DATAWAY AND CONNECTORS	UPC 2029	SEN	25	/70	
	CRATES- WITH DATAWAY AND POWER					
	CRATE, POWERED (SEE 1902,1912,1922)	1902/12/22	BORER	25	/70	
	CRATE MAINFRAME (CRATE SYSTEM INCLUDING THE FOLLOWING)	1902	BORER	25	12/69	
	POWER PACK, 270 VA	1912			12/69	
	VOLTAGE REGULATION MODULE (+AND- OF 6V/9A,12V/8A,24V/7A)	1922			12/69	
	REGULATOR (+OR-6V)	1925			/71	
	REGULATOR (+AND-12V OR 24V)	1926			/71	
	ALARM UNIT	1930			12/69	
	ALARM UNIT (ALTERNATIVE TO 1930)	1931			12/69	
	CAMAC CRATE (+6V/25A,-6V/5A,+12V/2A, +24V/4A,-24V/3A,400W)	DC 0200-3001	DORNIER	25	11/71	
	CRATES WITH DATAWAY AND POWER	1250-0006	DUCKERT	25	06/71	
N	CAMAC-RAHMEN MIT DATENWEG UND DREHSTROMNETZGERAET	1250-0021	DUCKERT	25	/72	
N	CAMAC-RAHMEN MIT DATENWEG UND 220 V 50 HZ NETZGERAET	1250-0022	DUCKERT	25	/72	
	POWERED CRATE	MC100	EG+G	25	/71	
	POWERED CRATE (+AND-6V/25A,+AND-24V/6A)	CPU/8	GRENSON	24	09/71	(2)
	POWER CRATE (7005-2 CRATE WITH 9022 POWER SUPPLY)	9023	NUCL. ENTERPRISES	24	/71	(2)
	CHASSIS ET TIROIRS AVEC ALIMENTATION (POWERED CRATE)		POLON	25	08/71	
	POWERED CRATE	CCHN-CSAN	RDT	25	10/71	
	CAMAC CRATE (POWERED BY MODEL 1410, VENTILATED)	1410 NSI	RODCOR	25	09/71	
	CHASSIS ALIMENTATION (POWERED CRATE, VENTILATED,+6V/25A,-6V/15A,+AND-24V/3A)	C ALJ 40	SAIP-CRC	25	11/71	
	POWERED CRATE(SEE P4 ALJ 13)	C4 ALJ 13 D	SAPHYMC-SRAT	25	/71	(1)
	POWERED CRATE(SEE P6 ALJ 13)	C6 ALJ 13 D		25		(1)
	POWERED CRATE(SEE P7 ALJ 13)	C7 ALJ 13 D		25		(1)
	POWER SUPPLY (CRATE)	CM5125/53/D/BIP	SAPHYMC-SRAT	25	/71	
	POWER SUPPLY (CRATE)	CM5125/53/A/BIP		25		
	POWER CRATE (300W MAX,+6V/25A,-6V/10A, +AND-12V/3A,+AND-24V/3A,200V/0.05A)	PC 2006/A	SEN	25	05/70	
	POWER CRATE (200W MAX,+6V/25A,-6V/10A, +AND-12V/3A,+AND-24V/3A,200V/0.05A)	PC 2006/B		25	05/70	
	POWER CRATE (200W MAX,+6V/25A,-6V/10A, +AND-24V/3A,200V/0.05A)	PC 2006/C		25	11/71	
C	POWERED CRATE (7U,VENT,+AND-6V/26A,+AND-12V/6.5A,+AND-24V/6.5A,200V/0.1A,200W)	C 76455-A2	SIEMENS	25	10/71	(3)
N	POWERED CRATE (SAME BUT WITH 117V AC)	C 76455-A1		25	10/71	
	POWER SUPPLIES AND SUPPLY CONTROLS					
	POWER SUPPLY (+AND-6V/25A,+AND-24V/5A,200V)	PS 0002	GEC-ELLIOTT		01/71	
	COMPACT POWER SUPPLY UNIT 200/300W	PS 0003	GEC-ELLIOTT		10/71	
	CAMAC POWER SUPPLY (+6V/20A,-6V/5A,+AND-24V/5A,200V/0.05A)	CPU/2	GRENSON		04/71	
	SAME WITH SWITCHED METERING	CPU/2M			04/71	
	POWER SUPPLY (+6V/20A,-6V/5A, +AND-12V/2A,+AND-24V/3A)	CPU/5	GRENSON		04/71	
	POWER SUPPLY (RACK MOUNTING,+6V/25A, -6V/15A,+AND-24V/5A,200V/0.1A)	CPU/6	GRENSON		07/71	
	POWER SUPPLY (RACK MOUNTING,+6V/25A, -6V/15A,+AND-24V/5A,+AND-12V)	CPU/7	GRENSON		07/71	
	CRATE WITH F.P.C. POWER RAIL ASSEMBLY	TYPES 3,4,7,8	MB METALS		01/72	
	POWER SUPPLY (+6V/20A,-6V/5A, +AND-24V/5A,200V/0.05A)	9001	NUCL. ENTERPRISES		/71	
	POWER UNIT (+6V/15A,-6V/3A, +AND-24V/2A,200V/0.05A)	9022	NUCL. ENTERPRISES		/71	(2)

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	POWER SUPPLY (+AND-6V/25A SHARED,+AND-12V/2A,+AND-24V/6A SHARED,200V)	1C31	B.L.PACKER		C2/71	
	POWER SUPPLY (+6V/25A,-6V/5A, +AND-12V/2A,+AND-24V/3A,2C0V/0.1A)	C 303	RDT		06/71	
	CAMAC POWER SUPPLY(+AND-6V/25A MAX 150W, +AND-24V/6A MAX 150W,12V AND 200V OPT)	1410	RCDCOR		C9/71	(3)
	POWER SUPPLY UNIT (+6V/10A,-6V/2A,+AND-24V/1.5A)	P4 ALJ 13	SAPHYMC-SRAT		/71	
	(+6V/5A,-6V/1.5A,+AND-12V/1.5A, +AND-24V/1.5A)	P6 ALJ 13				
	(+6V/25A,-6V/10A,+AND-12V/3A, +AND-24V/3A,+200V/0.1A,MAX 200W)	P7 ALJ 13				
	POWER SUPPLY (MAX 300W,+6V/25A,-6V/10A, +AND-12V/3A,+AND-24V/3A,200V/0.05A)	PS 2036	SEN		C6/71	
N	SUPPLY (+AND-6V/26A,+AND-12V/6.5A,+AND-24V/6.5A,200V/0.1A,117V AC, 200W MAX)	C 76455-A4	SIEMENS		01/72	
N	SUPPLY (SAME BUT WITHOUT 117V AC)	C 76455-A5			01/72	
	POWER SUPPLY FLEXIBLE SYSTEM COMPRISING	CPU/1	GRENSON		07/71	
	BASIC CRATE(FOR SUPPLY MODULES,INCLUDES REFERENCE,CONTROL AND 200V/0.1A)	CFC				
	SUPPLY MODULE (+6V/6A)	CFP/6				
	(-6V/6A)	CFM/6				
	(+12V/3A)	CFP/12				
	(-12V/3A)	CFM/12				
	(+24V/3A)	CFP/24				
	(-24V/3A)	CFM/24)				
	POWER UNIT(FOR SUPPLY MODULES)		RO ASSOCIATES		C6/71	
	CAMAC SYSTEM POWER SUPPLY MODULE (+AND-12V/72W, OR +12V/6A OR +24V/3A)	C 301			03/70	
	(6V/10A)	C 210			C3/7C	
	(6V/5A AND 24V/1A)	C 211			C3/7C	
	(6V/5A, +12V/0.4A, -12V/0.4A)	C 213			03/70	
	(12V/4A)	C 250			06/71	
	(24V/2A)	C 251			C6/71	
	POWER SUPPLY SYSTEM (MODULE OPTIONS AS FOLLOWS)	C4 BIP 203	SAPHYMO-SRAT		/71	
	POWER SUPPLY MODULE 6 V 10 A	BIP B6 10				
	6 V 15 A	BIP C6 15				
	6 V 20 A	BIP D6 20				
	6 V 40 A	BIP E6 40				
	12 V 7 A	BIP B12 7				
	12 V 10 A	BIP C12 10				
	12 V 15 A	BIP D12 15				
	12 V 25 A	BIP E12 25				
	24 V 3.5A	BIP B24 35				
	24 V 6 A	BIP C24 6				
	24 V 9 A	BIP D24 9				
	24 V 15 A	BIP E24 15				
	SUPPLY CHASSIS 2KW (RAW SUPPLY FOR REGULATOR MODULES)	ALB/10	SAPHYMC-SRAT		/71	(2)
	FAN UNIT	VALB/10				
	WIRED RACK 42 U	BC 42				
	POWER SUPPLY MODULE 6 V 5 A(REGULATOR)	BPR 605				
	6 V 10 A	BPR 610				
	6 V 25 A	BPR 625				
	12 V 2 A	BPR 122				
	12 V 5 A	BPR 125				
	24 V 3 A	BPR 243				
	24 V 5 A	BPR 245				
C	VOLTAGE MONITOR PANEL	MP 1	GEC-ELLIOTT	1	C1/71	
C	MAINS SWITCH ASSEMBLY	MS 3	GEC-ELLIOTT	NA	01/71	
	POWER INDICATOR (INSERTS INTO SPECIAL STATION ONLY,USED WITH TYPE 7005 CRATE)	0704-1	NUCL. ENTERPRISES	1	/71	
	POWER INDICATOR (PLUGS INTO ANY NORMAL STATION)	7074-1	NUCL. ENTERPRISES	1	/71	
	SUPPLY CONTROL INDICATOR		B.L.PACKER	1	07/71	
	TIROIR MODULAIRE DE COMMANDE (SUPPLY CONTROL MODULE)	TCM 525	TRANSRACK	1	1C/7C	
	NETZTEILCHASSIS (EMPTY SUPPLY CHASSIS)	2.082.000.6	KNUERR		10/7C	
	POWER UNIT CRATE	0700	NUCL. ENTERPRISES		C1/71	
	POWER SUPPLY CRATE(FOR SEPARATE SUPPLY)	CSAN	RDT		06/71	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	VENTILATION EQUIPMENT					
	LUFTEREINHEIT (VENTILATION UNIT,COMPLETE WITH 3 FANS AND FILTER)	2.081.000.6	KNUERR		1C/70	
	(VENTILATION UNIT,NO FAN,NO FILTER)	2.085.CCC.6				
	FAN UNIT (FOR ALB/10 SUPPLY SYSTEM)	VALB/10	SAPHYMO-SRAT		/71	
	VENTILATION UNIT	1UVCAM	WILLSHER + QUICK		1C/71	(3)
	EXTENDERS AND ADAPTERS					
	EXTENSION FRAME	EF 2	GEC-ELLIOTT	1	1C/71	
	EXTENDER MODULE	11	JORWAY	1	01/71	
N	EXTENDER CARD	100C	KINETIC SYSTEMS	1	/71	(4)
	EXTENSION UNIT	7007-1	NUCL. ENTERPRISES	1	/70	
N	EXTENDER	CEX	RDT	1	/72	
	MODULE EXTENDER	ME 2030	SEN	1	03/7C	
	PROLONGATEUR POUR TIROIRS CAMAC (EXTENDER)		TRANSRACK	1	1C/70	
	NIM ADAPTOR	7009-2	NUCL. ENTERPRISES	NA	/7C	
	CAMAC NIM ADAPTOR	CNA 2033	SEN	NA	03/71	
	NIM-CAMAC ADAPTOR	CAN	RDT	NA	C6/71	
	MODULE PARTS					
	BLANK MODULE KIT (SINGLE WIDTH)	BM 1	GEC-ELLIOTT	1	C1/71	
	(DOUBLE WIDTH)	BM 2		2		
	(TRIPLE WIDTH)	BM 3		3		
	(CUADRUPLE WIDTH)	BM 4		4		
	SINGLE CARD MOUNTING KIT (EMPTY MODULE)	BCK/5CAM/CM1	IMHOF-BEDCO	1	06/71	
	DOUBLE CARD MOUNTING KIT	BCK/5CAM/CM2		2		
	TRIPLE CARD MOUNTING KIT	BCK/5CAM/CM3		3		
	QUADRUPLE CARD MOUNTING KIT	BCK/5CAM/CM4		4		
	DOUBLE ENCLOSED BIN KIT (EMPTY MODULE)	BCK/5CAM/BM2	IMHOF-BEDCC	2	06/71	
	TRIPLE ENCLOSED BIN KIT	BCK/5CAM/BM3		3	C6/71	
	QUADRUPLE ENCLOSED BIN KIT	BCK/5CAM/BM4		4	C6/71	
N	KLUGE CARD (FOR CREATING YOUR OWN CAMAC MODULES)	2000	KINETIC SYSTEMS	1	/71	(4)
	CAMAC-KASSETTE (EMPTY MODULE,WIDTH 1/25)	2.090.001.8	KNUERR	1	10/70	(2)
	(WIDTH 2/25)	2.090.002.8		2		
	(WIDTH 3/25)	2.090.CC3.8		3		
	(WIDTH 4/25)	2.090.CC4.8		4		
	(WIDTH 5/25)	2.090.C05.8		5		
	(WIDTH 6/25)	2.090.006.8		6		
	CHASSIS KIT (EMPTY MODULE,1 UNIT WIDTH)	7001	NUCL. ENTERPRISES	1	C1/71	
	(EMPTY MODULE,2 UNITS WIDTH)	7002		2	01/71	
	MODULE KIT (EMPTY MODULE,1 UNIT WIDTH)	9005-1	NUCL. ENTERPRISES	1	/71	
	(EMPTY MODULE,2 UNIT WIDTH)	9005-2		2	/71	
	CAMAC COMPATIBLE MODULE (EMPTY MODULE,1 UNIT WIDTH)	NSI 875 DM	NUCL. SPECIALTIES	1	02/70	
	(2 UNIT WIDTH)			2		
	(3 UNIT WIDTH)			3		
N	TIROIR MODULAIRE (W=1/25)	99C5-1-L	CSL	1	C5/71	
N	(W=2/25)	9905-2-L		2	C5/71	
N	(W=3/25)	9905-3-L		3	05/71	
N	(W=4/25)	9905-4-L		4	C5/71	
N	(W=5/25)	9905-5-L		5	C5/71	
N	(**=06,08,10 AND 12 FOR CORRESP WIDTH)	9905-**-L			C5/71	
	EMPTY MODULE 1 UNIT	CCA 1	RDT	1	10/70	
	2 UNITS	CCA 2		2		
	3 UNITS	CCA 3		3		
	4 UNITS	CCA 4		4		
N	BLANK MODULE WITH 60 WIRE-WRAP SOCKETS	WW-001	TECHCAL	C	/72	
N	BLANK MODULE WITH 56 WIRE-WRAP SOCKETS AND COMPLETE DECODING OF A AND F LINES	WW-002		0	/72	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	TIROIR MODULAIRE (EMPTY MODULE,W=1/25)	TM 50125	TRANSRACK	1	10/70	
	(W=2/25)	TM 50225		2		
	(W=3/25)	TM 50325		3		
	(W=4/25)	TM 50425		4		
	(W=5/25)	TM 50525		5		
	(**=06,08,10 AND 12 FOR CORRESP WIDTH)	TM 5**25				
	CAMAC MODULE (EMPTY,1/25 CARD MODULE)	CAMCAS 1	WILLSHER + QUICK	1	10/71	(2)
	(2/25)	CAMCAS 2		2		(2)
	(3/25)	CAMCAS 3		3		(2)
	(4/25)	CAMCAS 4		4		(2)
	CAMAC MODULE(EMPTY,2/25 SCREENED MODULE)	CAMMOD 2	WILLSHER + QUICK	2	10/71	(2)
	(3/25)	CAMMOD 3		3		(2)
	(4/25)	CAMMOD 4		4		(2)
	BLANK MODULE(COMPLETE WITH PRINTED BOARD FOR 69 INTEGRATED CIRCUITS,1 U WIDTH)	BM 2020/1U	SEN	1	/70	
	(SAME,2U WIDTH)	BM 2020/2U		2	/70	
	PRINTED CIRCUIT TEST BOARD	10	JORWAY	NA	01/71	
N	CAMAC HARDWARE	CH-001	KINETIC SYSTEMS	1	/71	(4)
N	TIROIR MODULAIRE POUR COMMANDE	9905-TC-1	CSL	1	05/71	
	CAMAC-UNIVERSALKARTE (PRINTED CARD MODULE WITH 28 14-PIN + 28 16-PIN SOCKETS)	DO 0200-2900	DORNIER	3	11/71	
	PC BOARD (MX B1 HAS 68 SITES, MX B2 HAS 80 SITES)	MX B1/MX B2	GEC-ELLIOTT	NA	10/71	
	(MX B3 HAS 68 SITES,MX B4 HAS 80 SITES, MX B3/MX B4 INCLUDE 5V CIRCUIT)	MX B3/MX B4		NA	10/71	
	GENERAL PURPOSE IC PATCHBOARD (MAX 33 14/16-PIN AND 5 24-PIN DIP,WIRE WRAP)	CAMAC CG 164	GSPK	NA	12/70	(2)
	EXPERIMENTIERPLATTE (PRINTED CIRCUIT BOARD)	4.000.002.0	KNUERR	NA	10/70	
	MODULE PRINTED CIRCUIT BOARDS(TAKE 24 16-PIN AND 36 14-PIN DIP,CBP3 HAS SOCKETS)	CBP1/CBP2/CBP3	RDT	NA	06/71	
	CONTROLEUR SORTIE DATAWAY (DATAWAY TEST MODULE)		TRANSRACK	1	10/70	
	CARTE CIRCUIT IMPRIME CAMAC (PRINTED CIRCUIT BOARD FOR CAMAC MODULE)		TRANSRACK	NA	10/70	

DATAWAY COMPONENTS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	DATAWAY CONNECTOR		AMP-HOLLAND		10/70	
	DATAWAY CONNECTOR,FLOWSOLDER TERMINATION (ADD MOUNTING BRACKETS R500014900000000)	R500014800000000	CARR FASTENER		10/70	
	MINI WRAP TERMINATION	R500016800000000			10/70	
	SOLDER SLOT TERMINATION				10/70	
	CONNECTEUR,FUTS DROITS (DATAWAY CONNECTOR,STRAIGHT PINS)	K/47995	FRB CONNECTRON		01/70	
	FUTS WRAPPING (WIRE WRAP PINS)	K/48326				
	FUTS A SOUDER (SOLDER PINS)	K/49016				
	CAMAC-LEISTE(DATAWAY CONNECTOR,MINIWRAP)	4.000.000.0	KNUERR		10/70	
	(SOLDER PINS)	4.000.001.0				
	DATAWAY CONNECTOR,MINI-WRAP	2422 061 64334	PHILIPS		09/71	
	BOARD SOLDER	2422 061 64354				
	WIRE-SOLDER	2422 061 64314				
	DATAWAY CONNECTOR (WIRE SOLDER)	EAA 043 D100	SABCA		06/71	
	(FLOW SOLDER TO BOARD)	EAA 043 D200			06/71	
	(MINIWRAP)	EAA 043 D301			06/71	(2)
	CONNECTEUR 254 DOUBLE FACE (DATAWAY CONNECTOR,WIRE WRAP)	254 DF 43 AWV	SOCAPEX		01/70	
	(MOTHERBOARD SOLDER)	254 DF 43 AYV			01/70	
	(WIRE SOLDER)	254 DF 43 AZV			01/70	
	DATAWAY CONNECTOR (**=15 FOR MINIWRAP, ALSO SOLDER LUG AND FLOW SOLDER TYPES)	86068621**000	SOURIAU		11/71	
	DATAWAY CONNECTOR (*=2 FLOW SOLDER,*=3 SOLDER LUGS,*=4 MINIWRAP,AU PLATING)	C 288* CSP 221	UECL		11/71	
	(FLOW SOLDER,NI + AU PLATING)	C 2885 CSP 221				
	(13 M2NIWRAP CONTACTS,OTHER ARE FLOW SOLDER,NI + AU PLATING)	C 2886 CSP 221				
	(*=7 MINIWRAP,*=8 SOLDER LUGS, NI + AU PLATING)	C 288* CSP 221				
N	MOUNTING BRACKETS FOR ABOVE	C 8523				
N	DATAWAY SOCKET (MOTHERBOARD COMPLETE WITH 25 CONNECTORS)	CIM	RDT		/72	
	DATAWAY ASSEMBLY (FILM WIRE PACKAGING)		MB METALS		07/71	(3)
	DATAWAY (MOTHERBOARD,COMPLETE WITH 25 CONNECTORS)	CDW	RDT		10/70	

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	DATAWAY (MOTHERBOARD WITH 25 DATAWAY CONNECTORS)	J/D	SAPHYMC-SRAT		11/71	
	CAMAC MULTILAYER (DATAWAY MOTHERBOARD)	CM-8-69	TECH AND TEL		08/71	

BRANCH HIGHWAY COMPONENTS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	BRANCH HIGHWAY CONNECTOR (FIXED MEMBER,SOCKET MOULDING)	WSS0132S008NCCC	EMIHUS-SABCA		10/70	
	(FREE MEMBER,PIN MOULDING, PXX YYY SELECTS JACKSCREW)	WSS0132PXXBNYYY				
	HOOD (FOR FREE MEMBER)	WAC 0132 H005				
N	BRANCH HIGHWAY CABLE (132-WAY)	LIY-Y72X2X0.088	LEONISCHE		04/72	
	BRANCH HIGHWAY CABLE (COMPLETE PTFE CABLE ASSEMBLY,27CM LONG)	CD 18067-27	EMIHUS		10/70	
	(1 METER LONG)	CD 18067/107			11/71	
	(2 METERS LONG)	CD 18067/207			11/71	
	BRANCH CABLE WITH CONNECTOR (1.5 FT LONG)		JORWAY		03/71	
	CABLE FOR BRANCH HIGHWAY (PVC JACKET)	132 PE 189	PRECICABLE BOUR		10/71	
	(BRAIDED RILSAN JACKET)	132 PE 210				
	BRANCH HIGHWAY CABLE ONLY (PLAIN PVC JACKET)	66 POL PB	SABCA		06/71	
	(WOVEN RILSAN JACKET)	66 RIL PB				
	BRANCH HIGHWAY CABLE ASSEMBLY (WITH CONNECTORS,27 CM LONG)	CC 66 RIL PB-27	SABCA		06/71	
	(XX CM LONG,RILSAN JACKET)	CC 66 RIL PB-XX				
	(XX CM LONG,PVC JACKET)	CC 66 POL PB-XX				
	CABLE POUR BRANCH HIGHWAY (66 PAIRES TORSADEES,66 TWISTED PAIRS)	CL 90	SAIP-CRC		11/71	
C	BRANCH HIGHWAY CABLES(COMPLETE WITH CONNECTOR,XXX = LENGTH IN METERS)	2000/S/0132/XXX	TEKDATA		08/71	(4)
	CABLE EXTENSION MODULE (JOINS TWO BRANCH HIGHWAY CABLES)	CD 18106	EMIHUS		/72	

OTHER STANDARD CAMAC COMPONENTS

N/C	DESIGNATION + SHORT DATA	TYPE	MANUFACTURER	WIDTH	DELIV.	NPR
	COAXIAL CONNECTOR	RA 00 C50	LEMC		01/70	(4)
	52-WAY DOUBLE DENSITY CONNECTOR (FIXED MEMBER WITH PINS.LAM GRADER CONNECTOR)	2 DB 52 P	CANNON		10/70	

Note

Manufacturers requiring their new products to appear in the PRODUCTS GUIDE Section or intending to complete or correct already presented information should submit data on each item separately and, preferably, in the format used in this issue.

INDEX OF MANUFACTURERS

AEG-Telefunken
Elisabethenstrasse 3, Postfach 830
D-7900 Ulm, Germany

AMP-Holland
Papierstraat 2-4, Postbus 288
'S-Hertogenbosch, Netherlands

Berthold/Frieseke – See BF Vertrieb

BF Vertrieb GmbH
Bergwaldstrasse 30, Postfach 76
D-7500 Karlsruhe 41, Germany

B. L. Packer Co. Inc.
5-05 Burns Avenue,
Hicksville, N.Y. 11801, USA

Borer & Co., Electronics AG
Postfach 4500
CH-4500 Solothurn 2, Switzerland

Cannon Electric, Ltd.
Lister road, Winchester road
Basingstoke, Hampshire, England

Carr Fastener Co. Ltd.
Station House, Darkes Lane
Potters Bar, Herts, England

Digital Equipment Corporation (DEC)
146 Main Street
Maynard, Mass. 01754, USA

Dornier AG
Vertrieb Elektronik, Abt. VC 20
Postfach 317
D-799 Friedrichshafen, Germany

Duckert – See Juergen Duckert

EG+G Inc.
Nuclear Instrumentation Division
500 Midland Road
Oak Ridge, Tenn. 37830, USA

Eisenmann Elektronische Geräte
Blumenstrasse 11
D-7500 Karlsruhe, Germany

EKCO – See Nuclear Enterprises

Elliott – See GEC-Elliott

Emihus Microcomponents Ltd.
Clive House
12-18 Queens Road
Waybridge, Surrey, England

Emihus-SABCA
See respectively Emihus and SABCA

FRB Connectron
30, Avenue Gabriel Péri
F-92 Gennevilliers, France

Frieseke – See BF Vertrieb

GEC-Elliott Process Instruments Ltd.
Century Works, Lewisham
London SE13 7LN, England

Grenson Electronics Ltd.
Long March Industrial Estate
High March Road
Daventry, Northants NN11 4HQ,
England

GSPK (Electronics) Ltd.
Hookstone Park
Harrogate, Yorks HG2 7BU, England

Hans Knuerr KG
Ampfingstrasse 27
D-8000 Muenchen 8, Germany

Hewlett-Packard (Schweiz) AG
7, Rue du Bois-du-Lan
CH-1217 Meyrin-Genève, Switzerl.

Imhof-Bedco Ltd.
Ashley Works
Cowley Mills Road
Uxbridge, Middlessex, England

Interdata Ltd.
Station House, Harrow Road
Wembley, Middlessex, England

Intertechnique
F-78 Plaisir, France

J and P Engineering (Reading) Ltd.
Portman House
Cardiff Road
Reading, Berkshire R61-8JF, England

Jorway Corporation
27 Bond Street
Westbury, N.Y. 11590, USA

Juergen Duckert Projekttechnik
Adam-Berg Strasse 5
D-8000 Muenchen 83, Germany

Kinetic Systems Corporation
PO Box 571
Downers Grove, Ill. 60515, USA

Knuerr – See Hans Knuerr

Le Croy Research Systems Corp.
126 North Route 303
West Nyack, N.Y. 10994, USA

Lemo SA
CH-110 Morges, Switzerland

N Leonische Drahtwerke AG
Abholfach
D-8500 Nurnberg 2, Germany

LSR-Le Croy – See Le Croy

MB Metals Ltd.
Victoria Road
Portslade, Sussex BN4 1YH, England

Micro Consultants Ltd.
Interface House
Croydon Road
Caterham, Surrey, England

Nuclear Enterprises Ltd.
Bath Road
Beenham, Reading RG7 5PR, England

Nuclear Specialties Inc.
(Precision Metal Fabricators)
540 Lewelling Blvd
San Leandro, Calif. 94579, USA

OSL—See Société Outillage

Packard Instrument Company, Inc.
Subsidiary of AMBAC Industries, Inc.
2200 Warrenville Rd.
Downers Grove, Ill. 60 515, USA

Packer – See B. L. Packer

Philips Ned. N.V.
Dept. Elonco, Building VB 11
Eindhoven, Netherlands

Polon – See Zjednoczone

Precicable Bour
151, Rue Michel-Carre
F-95 Argenteuil, France

RDT Ing. Rosselli Del Turco
Rossello S.L.R.
Via di Tor Cervara 261
Casella Postale 7207
Roma Nomentano,
I-00155 Rome, Italy

RO Associates Inc.
3705 Haven Avenue
Menlo Park, Calif. 94025, USA

Rodcor Industries Inc.
44 255 Fremont Bvld
Fremont, Calif. 94 538, USA

SABCA (S.A. Belge de Construction Aéronautique)
Chaussée de Haecht, 1470
B-1130 Bruxelles, Belgium

SAIP-CRC – See Schlumberger

SAPHYMO-SRAT
51, Rue de l'Amiral Mouchez
F-75 Paris 13e, France

Schlumberger Instruments
et Systèmes
Centre d'Instrumentation Nucléaire
38, Rue Gabriel Crié
F-92 Malakoff, France

SEN Electronique
31, Avenue Ernest Pictet
CH-1211 Genève 13, Switzerland

Siemens AG
Bereich Mess- und Prozesstechnik
Postfach 21 1080
D-7500 Karlsruhe 21, Germany

SOCAPEX (Thomson-CSF)
9, Rue Edouard Nieuport
F-92 Suresnes, France

N Société Outillage Scientifique et
de Laboratoire (OSL)
4, Avenue du Château
F-06 La Trinité, France

Souriau et Cie
13, Rue Gallieni, B. P. 119
F-92 Boulogne-Billancourt, France

Tech and Tel – See Technograph

Techcal Electronic Services
2346 Spruce Street
Vancouver 9, B.C., Canada

Technograph and Telegraph Ltd.
Fleet
Aldershot, Hampshire, England

Tekdata Ltd.
Pentagon House
Bucknall New Road, Hanley
Stoke on Trent ST1 2BA, England

Telefunken – See AEG-Telefunken

Texas Instruments Ltd.
Dallas Road
Bedford, England

Transrack
22, Avenue Raspail, B.P. 12
F-94 Saint-Maur, France

Ultra Electronics (Components) Ltd.
Fassetts Road
Loudwater, Bucks., England

Wenzel Elektronik
Lamontstrasse 32
D-8000 Muenchen 80, Germany

Willsher and Quick Ltd.
Walrow
Highbridge, Somerset, England

Zjednoczone Zaklady Urzadzen
Jadrowych Polon, Bjuro Zbytu
Warszawa, Poland

NEWS

ANNOUNCEMENTS BY CAMAC MANUFACTURERS

KINETIC SYSTEMS has announced a CAMAC display system. A series of four basic single-width units provide a CAMAC system with a flexible visual interface. Both alpha-numeric and graphical information can readily be displayed on inexpensive TV monitors. The monitors are operated without interface and results in a flicker-free display refreshed at 60 Hz. The character capacity is 44 across by 24 down, for a total screen capacity of 1056 characters. The writing speed is such that the entire screen may be up-dates in less than 0.1 sec.

The units comprising the display series are: Model 3200—Display Synch, Model 3205—Display Timing, Model 3210—Display Control, and Model 3212—Display Refresh. This partitioning of functions results in units which are all single-width and allows more displays to be added without duplicating the common synchronizing and timing functions.

A display system requires one 3200 per system, one 3210 and one 3212 per unique display, and one 3205 for each crate containing one or more 3210's and 3212's. All inputs, outputs, and interconnections are made via a 36-pin edge-connector located above the Dataway connector on the rear side of the CAMAC crate. A printed-circuit motherboard, complete with mating connectors, interconnects modules for as many as ten displays.

The *Display Synch* (3200) supplies basic clock signals to the 3205 timing units and provides synchronizing signals for the TV monitors.

The *Display Timing* (3205) contains a number of counting registers that receive signals from the 3200 and keep track of the position of the CRT scanning beam. Parallel data are transferred for that purpose to the 3210's and the 3212's.

The *Display Control* (3210) provides the control functions for one display. It contains all CAMAC Function and Sub-address decoding for a display, and thus the N line of this module is activated for all commands and data transfers associated with its particular display screen.

The *Display Refresh* (3212) provides 1056 12-bit words of addressable circulating memory. The memory is both writeable and readable. Two character generators are provided, one for alphanumeric and the other for graphical information.

DIGITAL EQUIPMENT is offering now several CAMAC Branch controller interfaces for their computers PDP 11 and PDP 15.

1. *PDP 11 CAMAC INTERFACE MODEL CA 11-A*

Data transfer is via the programmed I/O (Ref. CAMAC Bulletin No. 2, p. 25).

2. *PDP 11 CAMAC INTERFACE MODEL CA 11-NPR*

Data transfer is via the programmed I/O identical to the CA 11-A and DMA. DMA transfer is used for memory increment mode and list mode. In list mode, block transfer as well as linear and random scanning is possible. In a third mode, a transfer between CAMAC modules can be realised (LAM-Command or LAM-read-write combination). A more detailed description of the CA-11-NPR interface will be submitted for publication in the next issue of the CAMAC Bulletin: 'A universal CAMAC branch highway interface for the PDP 11' by P. Reisser, Digital München.

3. *PDP 15 CAMAC INTERFACE MODEL CA 15-A*

This interface generates command, read and write functions either singly, under program control, or in blocks, using the PDP 15 Data channel facility for data transfers. Program transfer is preceded by loading the command register with a 17-bit word which defines C, N, A, F. For block transfer, two data break channels can be used. Each has its own data-pointer address and word-count address in core and its own device-count and command register in the interface.

4. *PDP 15 CAMAC INTERFACE MODEL CA 15-B*

Data transfer of 18- or 24-bits may be accomplished between any of the CAMAC peripherals and the PDP 15 accumulator under program control. The Branch Demand is connected to the PDP 15 Bus Program Interrupt Request line.

CAMAC BIBLIOGRAPHY

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