GaN Schottky Diodes for Signal Generation and Control

Vom Fachbereich Elektrotechnik und Informationstechnik
der Technischen Universität Darmstadt
zur Erlangung des akademischen Grades eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

M. Sc.
Chong Jin
geboren am 29. November 1982
in Sichuan, V.R. China

Referent	:	Prof. Dr.-Ing. Dimitris Pavlidis
Korreferent	:	Prof. Dr. rer. nat. Sascha Preu
Tag der Einreichung	:	15.July.2014
Tag der mündlichen Prüfung	:	7.November.2014

D17
Darmstadt 2015

Erklärung laut §9 PromO

Ich versichere hiermit, dass ich die vorliegende Dissertation allein und nur unter Verwendung der angegebenen Literatur verfasst habe. Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient.

Datum und Unterschrift

Preface and Acknowledgement

This dissertation is a summary and a precious memory of my research conducted in the High Frequency Electronic Department of the Technische Universität Darmstadt and continued at the Institute of Electronics, Microelectronics and Nanotechnology (IEMN)/ University of Lille1.
I would like to express my sincere appreciation to my supervisor Prof. Dr.-Ing. Dimitris Pavlidis for his invaluable guidance, support and encouragement throughout the years of my study. Without them, this dissertation would never have been initiated, progressed and come to fruitful conclusions. My sincere appreciation goes also to my co-examiner Prof. Dr. rer. nat. Sascha Preu for his great interest in the subject of my research and serving in my committee.
My colleagues in our research group are warmly thanked for all kinds of assistance and help. I would like to thank in particular Dr. Oktay Yilmazoglu, Dr. Jens-Peter Biethan, Frau. Karin Boye, Dr. Sanghyun Seo, Dr. Eunjung Cho and Mr. Giorgi Aroshvili.
The help on high frequency measurement provided by Dr. Yuliang Zheng is warmly acknowledged. I would also like to thank Dr. Christian Gierl, Dr. Sandro Jatta for their help in PECVD deposition; Dr. Oleg Cojocari for his guidance in cleanroom.
I am grateful to IEMN for hosting me over the years and providing me with access to excelent fabrication and characterization facilities. Special thanks go to Dr. Mohammed Zaknoune, Dr.Damien Ducatteau, Mr. Etienne Okada and Ms. Vanessa Avramovic who have provided great help in technology developing and device characterization, as well as Dr. Henry Happy for his continuous support.
Finally I would like to thank my parents Qingbi Chen and Tinghao Jin, my wife Yong Long and our son Shen Jin for their continuous assistance and trust in me for carrying out my Ph.D work while thinking of my family.

Abstract

The aim of this work is to explore the potential of GaN Schottky diodes for high frequency signal generation and control, with emphasis on their power handling capability. GaN Schottky diodes are expected to provide superior power handling capability due to the wide band-gap of GaN. Theoretical analysis has been performed analytically and numerically. Devices have been fabricated and their performance has been evaluated experimentally. Demonstration of monolithic integrated circuits utilizing the realized devices was also made.

The diode figure of merits e.g. C_{j0}, R_s, V_{br}, have been considered with respect to power handling and harmonic generation to permit evaluation of the diode design requirements for satisfying specific circuit needs. Numerical simulation allowed the prediction of device performance for specific geometry and material properties. Simulation results have shown that GaN Schottky diodes have a power handling capability at least 2 times higher than their GaAs counterparts, while maintaining acceptable losses.

Several fabrication technology approaches have been studied and implemented for realizing GaN-based Schottky diodes. Their key steps include dry etching, metal contacts, as well as interconnects. The surface treatment before metal deposition necessary for good quality Schottky contacts has been thoroughly studied. Three means of interconnect methods were demonstrated for on-wafer tests. They allowed rapid evaluation of the electrical characteristics of the diodes and set up the basis for the development of monolithic integrated circuits.

High frequency small-signal measurements have been performed for the GaN Schottky diodes. The obtained S-parameters were used to extract equivalent circuit models. A parameter extraction procedure was established to de-embed the pad parasitics, and obtaining information about their intrinsic elements permitting in this way diode optimization.

The large-signal characteristics of the fabricated diodes were measured on-wafer using a large-signal network analyzer. This novel characterization method provided immediate information about diode features such as power handling, loss etc. The time-domain waveforms of the diodes were obtained under various operating conditions allowing a better insight into the diode operation.

Large-signal models of the diodes have been obtained by considering the extracted small-signal equivalent circuit characteristics and the large-signal measurement results. GaN-based circuits using diodes have been studied. They include a frequency doubler and an analog phase shifter. Consideration of their large-signal characteristics was possible

using the extracted diode large-signal models. Doublers made with this technology are expected to provide an output power of 10 dBm at 94 GHz. MMIC phase shifters were designed, fabricated and characterized. They showed a phase tuning ($\Delta\phi$) of 45° and 6-7 dB insertion loss in the 32-38 GHz range.

Kurzfassung

Das Ziel dieser Arbeit ist es, das Potenzial der GaN-Schottky-Dioden zur Hochfrequenz-Signalerzeugung und -Steuerung zu untersuchen, mit Schwerpunkt auf ihrem Leistungsvermögen. Für GaN-Schottky-Dioden werden überlegene Leistungsvermögen aufgrund der großen Bandlücke von GaN erwartet. Es wurden theoretische Untersuchungen analytisch und numerisch durchgeführt. Mehrere Bauelemente wurden hergestellt und ihre Leistung experimentell bewertet. Weiterhin wurden monolithisch integrierte Schaltungen mit diesen hergestellten Bauelementen demonstriert.

Die Diodengütefaktoren wie z. B. C_{j0}, R_s, V_{br}, wurden hinsichtlich Leistungsvermögen und Oberwellenerzeugung untersucht, um die Design-Anforderungen der Dioden für spezielle Schaltungen bewerten zu können. Die numerische Simulation erlaubte die Vorhersage der Bauelementleistung für spezifische Geometrien und Materialeigenschaften. Die Simulationsergebnisse haben gezeigt, dass GaN-Schottky-Dioden ein Leistungsvermögen von mindestens 2 mal höher als GaAs-basierte Dioden aufweisen, während sie die akzeptablen Verluste beibehalten.

Mehrere Fertigungstechnologieschritte wurden untersucht und zur Realisierung der GaN-basierten Schottky-Dioden eingesetzt. Die wichtigsten Schritte sind das Trockenätzen, die Herstellung von Metallkontakten sowie die Verbindungstechniken. Die Oberflächenbehandlung vor der Metallabscheidung, notwendig für qualitativ hochwertige Schottky-Kontakte, wurde detailliert untersucht. Weiterhin wurden drei Verbindungstechniken geeignet für On-Wafer-Tests entwickelt. Sie erlauben eine schnelle Auswertung der elektrischen Diodeneigenschaften und legen die Basis für die Entwicklung von monolithisch integrierten Schaltungen.

Mehrere Hochfrequenz-Kleinsignalmessungen wurden für die GaN-Schottky-Dioden durchgeführt. Die gemessenen S-Parameter wurden verwendet, um Ersatzschaltbilder zu extrahieren. Ein Parameter-Extraktionsverfahren wurde eingesetzt, um die parasitären Effekte der Kontaktpads zu entfernen und Informationen über ihre intrinsischen Komponenten zu erhalten. Auf diese Weise soll die Diodenoptimierung ermöglicht werden.

Die Großsignalcharakteristiken der hergestellten Dioden wurden mit einem Großsignal-Netzwerkanalysator On-Wafer gemessen. Diese neue Charakterisierungsmethode stellt direkt Informationen über die Diodenmerkmale wie Leistungsvermögen, Verlust usw. zur Verfügung. Die Zeitbereichsuntersuchungen der Dioden bei verschiedenen Betriebsbedingungen gaben ein besseres Verständnis zum Diodenbetrieb.

Die Großsignal-Modelle der Dioden erhielt man unter Berücksichtigung des extrahierten Kleinsignal-Ersatzschaltbildes und der Großsignal-Messungen. Anschließend wurden

GaN-basierte Schaltungen mit diesen Schottky-Dioden untersucht. Diese waren namentlich ein Frequenzverdoppler und ein analoger Phasenschieber. Die Bestimmung ihrer Großsignal-Eigenschaften war unter Verwendung der extrahierten Großsignalmodelle der Diode möglich. Für den mit dieser Technologie gebauten Verdoppler wird eine Ausgangsleistung von 10 dBm bei 94 GHz erwartet. Zum Schluss wurden MMIC-Phasenschieber entworfen, hergestellt und charakterisiert. Sie zeigten eine Phasenschie-bung ($\Delta\phi$) von 45° und 6-7 dB Einfügungsdämpfung zwischen 32 und 38 GHz.

Contents

1 Introduction

1.1 From Microwave to THz: Applications and Signal Sources

1.1.1 Microwave to THz Applications

The work presented in this thesis addresses semiconductor devices that find applications at frequencies ranging from microwaves to THz. The signal generation and control reported here using III-Nitride Schottky diodes is explored at frequencies varying from microwaves to millimeter waves but have the potential for THz applications. This section will discuss some of the key features of THz frequencies that are often reached by frequency multiplication based on diodes. Diodes based on GaN such as those explored in this thesis have the potential of delivering higher amount of power at very high frequencies than traditionally used components.

Terahertz (THz) designates frequencies that correspond to 10^{12} Hz. This term has also been used widely in referring to electro-magnetic waves in the frequency range from 0.1 THz to 10 THz, which corresponds to a wavelength from 3 mm to $30\,\mu\mathrm{m}$, an approximate photon energy from 0.41 to 41 meV and an equivalent black body temperature from 4.8 to 480 K. The THz specific wave features, as well as, their application areas have been revealed with the deepening of research in recent decades, and the lack of the signal sources at these frequencies.

The changing of the universe, including star formation, galaxy evolution and the formation of planetary systems, happens with energy radiation in THz spectrum. It's therefore no wonder why THz detectors are of such a great interest to astronomers. As ambient background on Earth is well above the universe radiation, space-borne observation is the best choice, like the recently launched Herschel by European Space Agency and VESPER by NASA[1]. For ground based astrophysics, the location of equipment has to be at high altitudes and dry atmosphere environment. A good example of them is the Atacama Large Millimeter Array (ALMA), which is expected to work up to 1.5 THz[2].

Planetary scientists also employ THz waves to monitor the abundances, distributions, and reaction rates of species involved in ozone destruction, global warming, total radiation balance, and pollution through the feature THz spectrums of water, oxygen, chlorine and nitrogen compounds, etc.

Due to the atmospheric opacity, the applications of THz wave in communications and radars are much limited. However, this is considered as an advantage for realizing secure communication in short distance.

The availability of high frequency signals allows high bandwidth for data transmission. It has been demonstrated that a data transfer rate of 10 Gbit/s can be achieved using signal sources at 0.2 THz [3].

THz waves have much lower energy than X-rays. This feature makes them suitable for medical imaging and DNA studying, since the bio-tissue will not be damaged by T-ray.

THz waves can easily penetrate cloths, plastic, leather, ceramic materials, etc. This feature can be utilized for homeland security or industry scatheless examination, like detecting concealed weapons or contraband from a safe standoff distance.

THz applications are not limited to the ones discussed above. All the applications except passive detection require local oscillators (LO), which remain the focus of study due to the difficulty in obtaining THz sources with adequate power, frequency agility and spectral purity. It is the purpose of this study to address the possibility of signal generation at high frequencies with adequate power levels.

1.1.2 THz Signal Sources

Motivated by the demands of THz sources, several technologies are being developed to generate THz signals. These technologies can be classified into 3 categories, Vacuum Electronic Devices (VEDs for short, including backward-wave oscillators, klystrons, grating-vacuum devices, traveling-wave tubes, and gyrotrons), solid state devices (including Gunn diodes, resonant tunneling diodes, harmonic frequency multipliers, transistors, and monolithic microwave integrated circuit), and photonic (including quantum cascade lasers, and a variety of optoelectronic RF generators). A comprehensive review of the state-of-the-art of all the available technologies can be found in [4, 5]. A comparison of the mainstream technologies is listed in Table.1.1. Fig.1.1 shows the output power and operation frequency range of the available technologies.

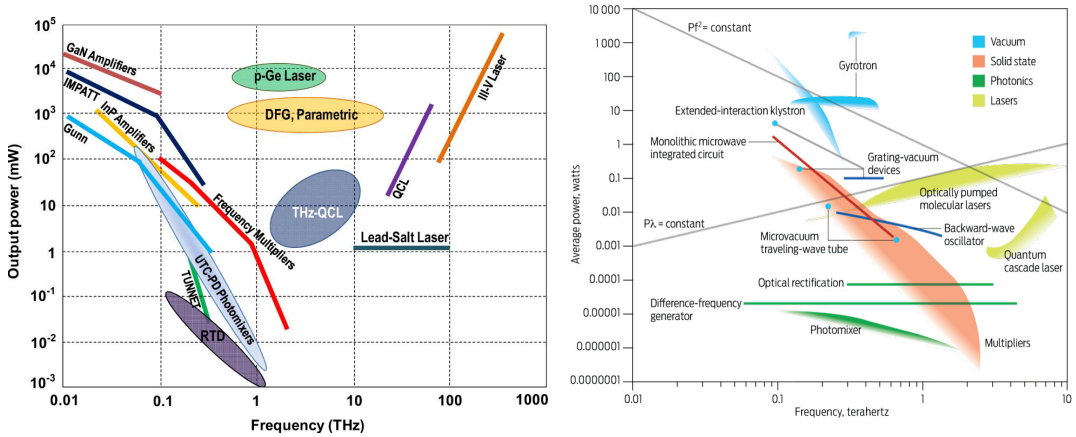


Figure 1.1: The state-of-the-art available power of THz source[4, 6].©2011 IEEE

Source Type	Advantages	Drawbacks	Recent Progress
Vacuum Electronic Devices	High output power;	bulky; high voltage operation; filament stability and lifetime	compact source with micromachining technologies; novel anode materials
Quantum cascade lasers	Choice for frequency above 2-3 THz	need cryogenic cooling; frequency stability; limited bandwidth; limited lifetime	Better frequency control; Tunable cavities; improved coupling efficiency
Photonic generation (LTG-GaAs, UTC-diodes, etc.)	Wide frequency bandwidth; high stability; Optical signal can be transmitted by optical fiber over long distance	Lower output power than multipliers	Structure optimization for higher output power
Frequency multiplier	Room temperature operation; Adequate output power; Adequate bandwidth; compact, lightweight	Limited maximum frequency	Frequency has been extended to 2.7 THz

Table 1.1: Comparison of THz sources

The vacuum electronic devices are in general bulky, though the studies on compact VED design are ongoing[7]. They are capable of providing high output power but the required input voltages are also high. The filament degradation makes the stability and lifetime questionable.

Quantum cascade lasers have been a promising choice for frequencies above 2 THz, but they have more recently been considered to be more appropriate above 3 THz after the demonstration of multiplier chains operating at 2.7 THz [8].

Photonic generation methods utilize photomixers like low-temperature-grown GaAs and Uni-Travelling-Carrier (UTC) photodiodes to downconvert optical signals to the THz range. Currently the available power of these sources is lower than generated by multipliers. An important application would be high-resolution and -precision molecular spectroscopy [9]. Signal transition by optical fibers makes such sources suitable for distributing signals to remote antennas [10].

The limiting factors for solid state devices are either frequency or output power, or both. Frequency multipliers are an exception. Their adequate output power at extended operation frequency and maturity of the technology used for them makes them being widely used. They are especially used in most space projects due to the lightweight properties. An excellent review on THz instruments used in space missions can be found in [1]. As one example, Herschel-HIFI launched in 2009 utilizes planar Schottky diodes based multiplier chain as local oscillator to drive hot electron bolometer (HEB) mixer in both 1.6-1.7 THz and 1.7-1.9 THz bands. The realized power are $100\,\mu W$ and $30\,\mu W$ respectively, well beyond the required $2\,\mu W$ [11].

1.1.3 Frequency Multipliers

The development of frequency multipliers can be backdated to 1950s. Millimeter-wave multipliers arose in the 1980s, where whisker contacted discrete diodes were the choice. In the 1990s, the planar Schottky diodes were developed to replace unreliable whisker contacted diodes. Efforts were made to replace hybrid mounting of diodes on quartz substrate by MMIC like chips in the past decade. GaAs has been the material of choice over several decades. In recent years, the development of frequency multipliers has been greatly enhanced by advanced design tools and fabrication technology. A review of frequency multipliers performance demonstrated in recent years can be found in [4]. A good review for the frequency multipliers developed before 2002 can be found in [12].

To the author's knowledge, the highest frequency of frequency multiplier achieved so far is 2.7 THz [8]. This is realized by a tripler from 840-900 GHz with input power around 1 mW, and a maximum output power of $18\,\mu W$ obtained at 2.58 THz. Based on the above presented reviews, the state of the art room temperature output power of Schottky multipliers can be considered being 1 mW at 1 THz, above 10 mW at 300-500 GHz and above 100 mW at 100 GHz. This is shown in Fig.1.1.

Both the frequency and output power increase demonstrated during the last decade are based on technological advances. Integration of diodes and matching circuits on the same substrate allows better controlling of the device parasitics and circuit optimizition[4, 13]; Computer numerical control milling machines are employed for waveguide block machining with micrometer precision [14]; Full 3-D electro-magnetic software and nonlinear circuits simulators are commercially available, which eases the co-simulation of the nonlinear diodes and linear matching circuits. Besides, one of the driving forces is to enhance the power handling capability of GaAs Schottky diodes and multipliers built with them, which are limited by their relatively low breakdown voltage.

Following the demonstration of single diode multipliers with maximum power, it is natural to seek solutions for higher power using several diodes connected in series. By connecting n identical diodes in series one obtains a breakdown voltage n times higher than for a single diode. The utilization of 2, 4 even 6 diodes in series has been demonstrated. However, the maximum number of diodes is limited by the waveguide dimensions [15]. Besides, the thermal dissipation problem becomes more serious as the diode number increases. Electro-thermal models have to be employed for design optimization[16]. Substrates with high thermal conductivity like diamond also provide a good solution [17]. The recently developed power combining multipliers is another option. The utilization of power combination techniques assures adequate input pump power level for the aforementioned 2.7 THz tripler. Furthermore, all the first stages of the multiplier chain rely on power combination techniques; an output of $\sim$500 mW at W-band was provided by combining four GaAs power amplifier chips , $\sim$40 mW by quad-chip power combined tripler at 300 GHz and $\sim$1 mW by double-chip power combined tripler at 900 GHz [18, 19].

The required rigorous design and assembling, characteristic of all the above solutions can not overcome the GaAs breakdown limitation due to its intrinsic material properties. A wide bandgap material like GaN with high breakdown voltage is thus a suitable candidate. Theoretical studies indicate that eight GaAs diodes are required for a 200 GHz doubler with input power of 150 mW, while one GaN diode with similar anode area is capable of handling this input power [20], i.e. the power handling capability of a GaN Schottky diode is almost one order higher than its GaAs counterpart. Diodes of this type have been the component on which this thesis has focused.

1.2 Properties of Nitride Materials

III-Nitrides have the crystal structures of wurtzite, zincblende and rocksalt. The thermodynamically stable structure is wurtzite, as illustrated in Fig.1.2. A Ga-face is shown here since it is the case for MOCVD grown GaN epitaxial films on c-plane sapphire, which are studied in this work exclusively. The wurtzite structure has a hexagonal unit cell and thus two lattice constants *c* and *a*, with values of 5.185 Å and 3.189 Å respectively. The properties of GaN are listed in Table.1.2 together with those of GaAs for comparison.

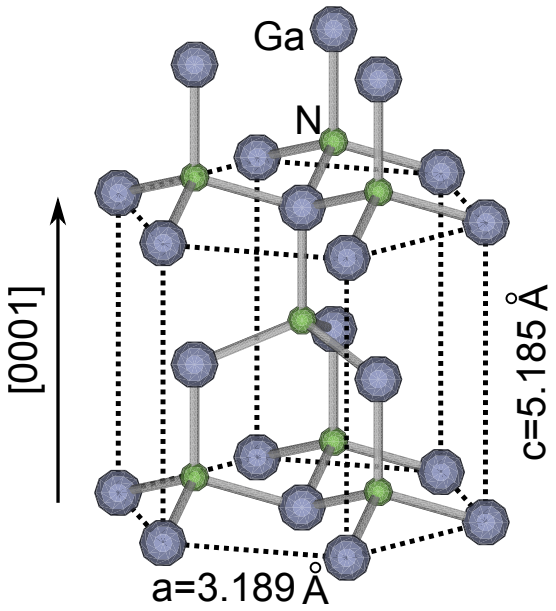


Figure 1.2: wurtzite GaN crystal structure with Ga-face [21]

	GaN	GaAs
Density $(\mathrm{g/cm^3})$	6.15	5.32
Dielectric constant	8.9	12.9
Bandgap (eV)	3.39	1.424
Effective mass	$0.2\,\mathrm{m_0}$	$0.063\,\mathrm{m_0}$
Electron mobility $(\mathrm{cm^2\,V^{-1}\,s^{-1}})$	1000	8000
saturation velocity $(\mathrm{cm/s})$	2.5×10^7	1×10^7
peak velocity $(\mathrm{cm/s})$	3.1×10^7	2×10^7
peak velocity field $(\mathrm{kV/cm})$	150	3.5
breakdown field $(\mathrm{MV/cm})$	>5	0.4
Thermal conductivity $(\mathrm{W\,cm^{-1}\,K^{-1}})$	>2.3	0.55

Table 1.2: GaN and GaAs material properties [22, 23]

GaN is considered to be a wide-bandgap material due to its large bandgap of 3.4 eV, which is greater than that of Si (1.12 eV) and GaAs (1.42 eV). Benefiting from the larger bandgap, the breakdown electric field of GaN is larger than 5 MV/cm. The intrinsic carrier concentration at room temperature is $2.8 \times 10^{-10}\,\mathrm{cm}^{-3}$ for GaN [23], compared to $1 \times 10^{10}\,\mathrm{cm}^{-3}$ for Si and $2.1 \times 10^{6}\,\mathrm{cm}^{-3}$ for GaAs and increases with temperature. The low intrinsic carrier concentration of GaN allows its use under very high ambient or junction temperature, without being affected by thermally generated carriers. Both the high breakdown field and low intrinsic carrier concentration are crucial attributes for the enhancement of power handling capability of GaN Schottky diodes.

A high electron drift velocity is favorable for frequency multiplier application. The electron velocity versus electric field is shown in Fig.1.3. Due to the multi-valley band structure of GaAs, its electron velocity is high at relatively low fields but reduces at values beyond the critical field. This has found to be the reason for lower multiplication efficiency, since current saturation lead in increased equivalent series resistance [24]. However, this is not an issue for GaN. The electron drift velocity is even higher than GaAs if the pump power is high enough to provide an electric field over 12 kV/cm.

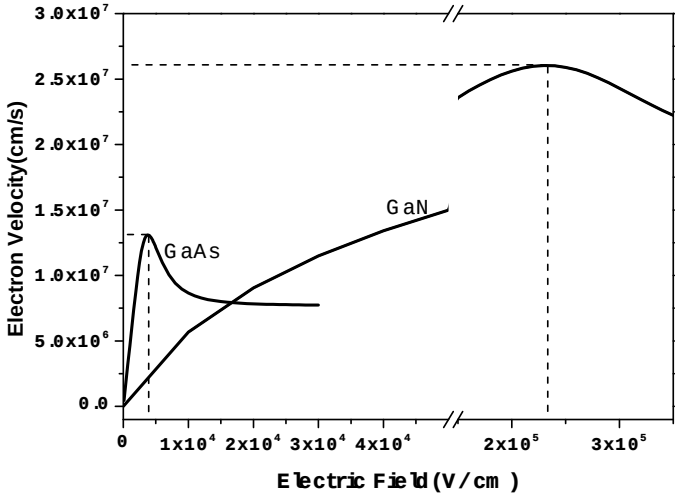


Figure 1.3: electron velocity versus electric field

Thermal conductivity is another parameter of importance. A thermal conductivity of $2.3\,\mathrm{W/cm \cdot K}$ [25] has been reported for GaN, while as this value is $0.55\,\mathrm{W/cm \cdot K}$ for GaAs. Thanks to the elevated thermal conductivity, the aforementioned electron-thermal model may not be needed for GaN multiplier diodes/chip design, thus the design procedure is simplified.

The superior properties of GaN have been utilized successfully to develop HEMTs for RF power amplifier applications. The current gain cutoff frequency of GaN-based HEMTs achieved so far is 370 GHz [26], and devices of this type have the potential of operating up to 500 GHz. The RF output power of W-band GaN-based HEMTs has been reported to be more than 1 W for a $600\,\mu\mathrm{m}$ gate width [27], resulting in a power density of 1.7

W/mm. As a comparison, the output power density for a GaAs-based p-HEMT with the same gate width is 0.28 W/mm [28]. By power combining, an output power of 3 W [29] and 5 W has been reported[30] for GaN-based HEMTs.

W-band amplifiers are of interest for the work reported in this thesis since they are used as first stage pump source for THz multiplier chains. GaAs or InP based Gunn diodes have traditionally been the choice for this purpose, but fail to provide very high output power. It has been estimated theoretically that an output power of $1400\,\mathrm{kW/cm^2}$ can be obtained from GaN Gunn diodes as compared to $4.9\,\mathrm{kW/cm^2}$ from GaAs diodes [31]. Despite the numerous papers on theoretical studies of GaN Gunn diodes, experimental studies are still in the beginning and only preliminary results are available [32] . One of the remaining big challenges is the high dislocation density of epitaxial GaN, which may limit the performance of GaN Schottky diodes.

1.3 Motivation, Challenges and Outline of the thesis

The superior material properties of Nitrides is a key motivation factor for exploring the properties of multipliers based on them. However, the mobility of Nitrides is lower than that of Arsenides and one may expect the operation frequency of Nitride-based devices to be limited. This work is mainly motivated by the expectation of higher output power by utilizing the previously discussed superior material properties.Obtaining such devices requires considerable research. In this work, the fabrication technology for multiplier diodes was first demonstrated with optical lithography. Dielectric bridges were used to demonstrate first devices. Micron-size diodes were characterized to understand their properties. The dielectric bridges were later replaced by air bridges, which allowed higher cut-off frequency by decreasing the parasitic capacitances. Modeling of such devices was performed and allowed the multiplier performance to be predicted. E-beam lithography was employed for further studies to ease the realization of smaller anode size. A technology based on E-beam lithography was also developed.

Due to the fact that multiplier diodes are working under large-signal excitation, their performance can not be known until diodes of this type are used in well designed waveguide circuits. Studies of this type involve considerable fabrication, mounting and packaging. On-wafer large-signal characterization was thus explored in this thesis in order to provide a quick feedback to the device studies.

The outline of this thesis is as follows. Chapter 2 reports the approaches used for analyzing Schottky diodes using traditional analytical expressions, as well as modern TCAD and EDA software. By implementing material parameters into the analysis , the properties of Schottky diodes based on GaN and GaAs material are compared. Chapter 3 presents the technologies developed in this work, using optical and E-beam lithography. Device characteristics resulted from the foregoing technologies are included in Chapter 4. The characteristics of diodes fabricated using these technologies are reported in Chapter 4. Chapter 5 provides information regarding on-wafer large-signal measurements.

The device modeling presented in Chapter 6 is obtained by tuning the model parameter to match the large-signal measurement characteristics and the multiplier performance is then predicted with the improved model. A multiplier and a phase shifter circuit utilizing the obtained diodes were designed and discussed in Chapter 6 together with the experimental data obtained for the phase shifter. Chapter 7 concludes the studies and discusses future work.

2 Theoretical Consideration of GaN Schottky Diode Design

The basic operation principles of Schottky diodes as well as the design aspects of GaN Schottky diodes are discussed in this chapter. Based on the basic current-voltage/charge-voltage relationship, the frequency multiplication performance of ideal Schottky diodes was evaluated analytically. Figures of merit like cut-off frequency (f_c), maximum input power (P_{in_max}) and conversion efficiency (η), were used. Taking the material properties of GaN into account, Schottky diodes were numerically analyzed by a commercial semiconductor device simulator. This allowed physical device modeling. The advantage of GaN over GaAs will be discussed and the design aspects of GaN based Schottky multiplier diodes will also be addressed.

2.1 Basic theory of Schottky Multiplier Diode

To obtain a full picture of Schottky multiplier diodes, characteristics of various basic aspects were considered. First, the Schottky contact theory will be briefly reviewed. Based on the obtained nonlinear C-V relationship , the nonlinearity arising from it will be analyzed to estimate the frequency doubler performance. The last section discusses the impact of diode series resistance, which is the key factor determining device losses.

2.1.1 Schottky Contact

Schottky contact theory is most important for understanding the operation of Schottky multiplier diodes. The performance of Schottky diodes relies on the quality of Schottky contacts. The theory of Schottky contacts is described briefly here and will be applied to the n-type semiconductors used in this study.

As shown in Fig.2.1, the initial state to consider is the one where the metal and semiconductor are separated. Vacuum energy E_0 is a common reference for both metal and semiconductor. The metal work-function W_m (E_0-E_{fm}) is the minimum energy required for electron emission from metal to vacuum. Electron affinity χ is the minimum energy required for a electron emission from semiconductor to vacuum, due to the fact that electrons in a semiconductor occupy the bottom of the conduction band, which is located higher than the Fermi-energy E_{fs}.

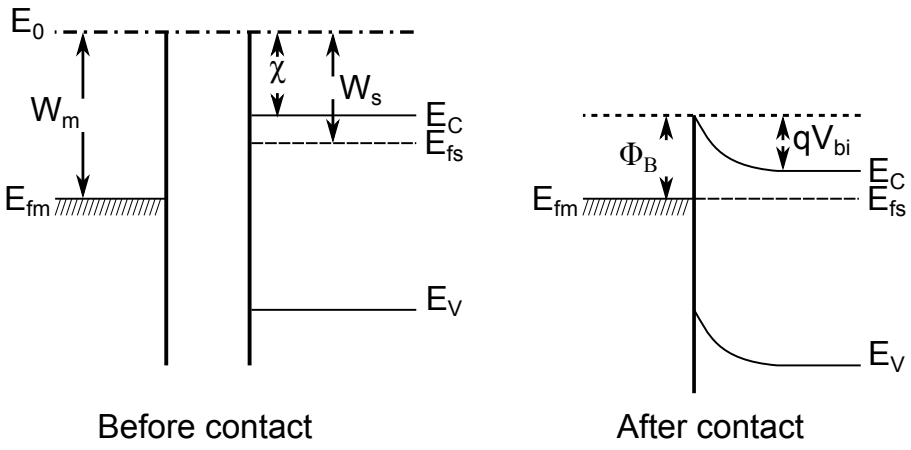


Figure 2.1: Band structure of Schottky contact formation

Ideally, Schottky contacts can be obtained at the metal-semiconductor interface when a metal contacts a semiconductor . Since E_{fs} is larger than E_{fm}, electrons in a semiconductor flow into the metal leaving fixed ionized dopants behind. The whole system, however, remains neutral. E_{fs} is lowered after contact establishment. The rise of E_{fm} can be ignored since the metal side has an enormous electron density and equilibrium is achieved when E_{fm}=E_{fs}. As a result, fixed ionized dopants remain in the near surface of a semiconductor and the same amount of electrons accumulates in metal. The bands are bent and an electric field (E-field) exists between the dopants and electrons, with a direction from semiconductor(dopants) towards metal(electrons). Since the electron concentration in semiconductor is much lower than in metal, the ionized dopants from certain depth near the surface respond providing E-field lines. This region is referred to as depletion region and its depth is the depletion depth. The potential difference between semiconductor surface and body(over the depletion region) is the built-in potential:

$$qV_{bi} = -(W_m - W_s) \tag{2.1}$$

which is also the barrier faced by the electrons moving from semiconductor to metal. Correspondingly, the barrier for the electrons moving from metal to semiconductor is given by:

$$\Phi_B = W_m - q\chi \tag{2.2}$$

Assuming that the dopants are fully ionized, implies that the electron concentration can be considered as N_D if the semiconductor is uniformly doped with a concentration of N_D. If the electrons in the depletion region are completely depleted(this is known as the depletion approximation), the depth of the depletion region is given by:

$$w_D = \sqrt{\frac{2\varepsilon_s}{qN_D}(V_{bi} - V - V_T)} \tag{2.3}$$

where ε_s is the dielectric constant of the semiconductor, V the applied voltage. $V_T = kT/q$ is a correction factor for built-in potential, caused by majority carrier distribution

tails. k is Boltzmann constant, and T the temperature.
The space charge Q_{SC} in the depletion region and capacitance C_D are given by

$$Q_{SC} = A_s q N_D w_D = A_s \sqrt{2\varepsilon_s q N_D (V_{bi} - V - V_T)} \tag{2.4}$$

$$C_D \equiv A_s \frac{\varepsilon_s}{w_D} = A_s \sqrt{\frac{\varepsilon_s q N_D}{2(V_{bi} - V - V_T)}} \tag{2.5}$$

The current flow through an ideal Schottky barrier is described by thermionic emission theory, and the equation for it is:

$$I = I_s[exp(\frac{V}{V_T}) - 1] \tag{2.6}$$

where I_s denotes saturation current under reverse bias

$$I_s = A_s A^* T^2 exp(-\frac{\Phi_B}{V_T}) \tag{2.7}$$

A^* is Richardson constant, which is related to the effective electron mass of specific semiconductor material.

I-V and C-V characteristics resulting from the equations above are shown in Fig.2.2(a) and Fig.2.2(b).

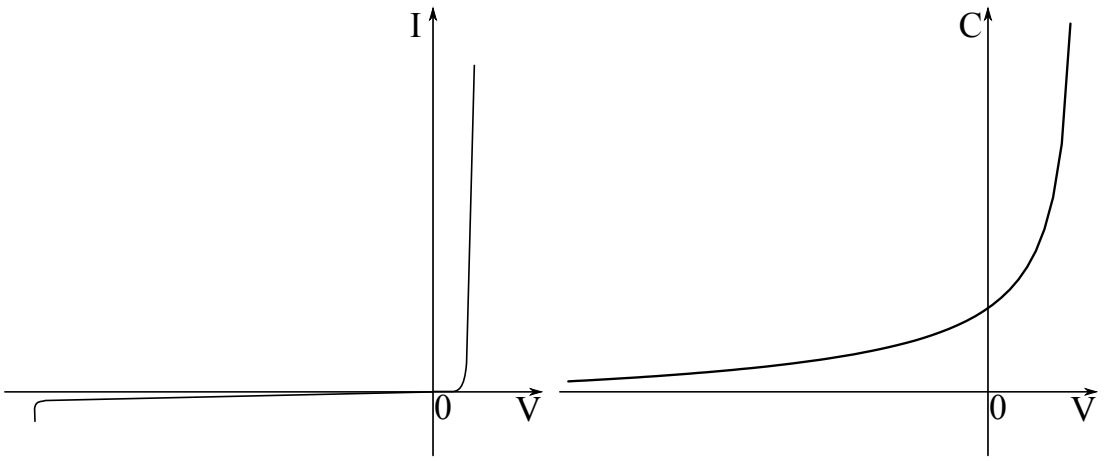


Figure 2.2: I-V and C-V characteristics of an ideal Schottky contact

2.1.2 Nonlinearity and Harmonic Generation

A nonlinear element converts a sinusoidal input signal to a periodic output signal containing high order harmonics. The I-V and C-V characteristics of Schottky diodes are

both nonlinear and can be considered as a nonlinear resistor and nonlinear capacitor respectively. Manley-Rowe equations [33] provide the fundamental limit of harmonic generation by nonlinear elements. Consideration of power conservation implies that the sum of power into and out of a nonlinear resistor is larger or equal to 0. The n^2 coefficient in the resulted Eq.2.8 [34] corresponds to severe loss at higher harmonic. It has been shown that n-order harmonics generated by a nonlinear resistor have at best a power of $1/n^2$ with respect to the pumping power , corresponding therefore to 1/4, 1/9 and 1/16 for 2^{nd} order, 3^{rd} order and 4^{th} order harmonic generation respectively.

$$\sum_{n=0}^{\infty} n^2 P_n \geqslant 0 \tag{2.8}$$

For a lossless nonlinear capacitor, the sum of all harmonic power is 0 simply because of power conservation and the lossless device, as indicated in Eq.2.9. The absence of n^2 coefficient suggests that the generated high order harmonic has in principle the same power as the pump signal. Based on the discussion above, one can conclude that the nonlinear C-V characteristics of Schottky diodes are preferred than I-V characteristics for harmonic generation.

$$\sum_{n=0}^{\infty} P_n = 0 \tag{2.9}$$

The operation principle of harmonic generation from nonlinear capacitance is described in Fig.2.3. Q-V curves are derived from Equation2.4, where the total amount charge Q is modulated by the applied voltage. It can be written in form of power series of voltages as follows:

$$Q(V(t)) = A_0 + A_1 V(t) + A_2 V(t)^2 + A_3 V(t)^3 + \cdots \tag{2.10}$$

Since the current is the time derivative of charge, one obtains

$$I(t) = \frac{dQ(t)}{dt} = [A_1 + 2A_2 V(t) + 3A_3 V(t)^2 + \cdots] \frac{dV(t)}{dt} \tag{2.11}$$

A n-order frequency multiplier is achieved by embedding the Schottky diode in a properly designed circuit, which should behave as filter or idler at the unwanted frequencies. Frequency multiplication efficiency (η) is defined by the resulting n-order output signal power over the input fundamental signal power. The presence of a resistance is inevitable in real Schottky diodes making the theoretical frequency multiplication efficiency of 100% unachievable. Early research has related the efficiency η to the cut-off frequency (f_c) of a Schottky diode, where f_c is given by

$$f_c = \frac{1}{2\pi R_s C_{j0}} \tag{2.12}$$

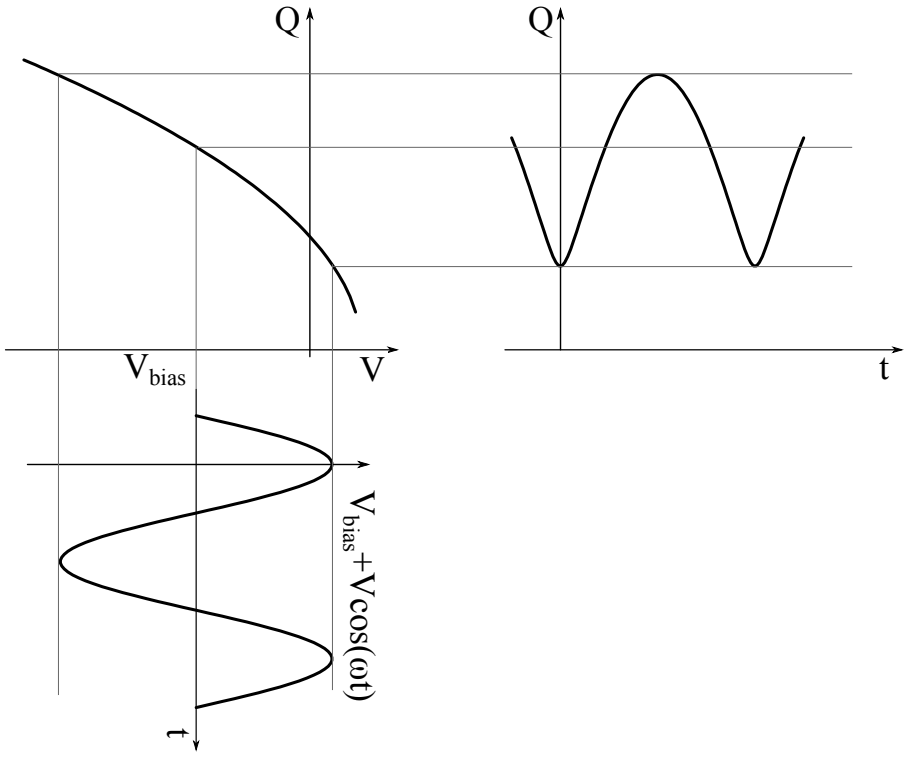


Figure 2.3: Harmonic generation from nonlinear Q-V

In terms of obtaining efficient frequency multiplication, f_c of the Schottky diode has to be much higher than the operation frequency. Fig.2.4 shows the dependence of theoretical efficiency of frequency doublers [35] on the operation frequency over the cut-off frequency. The efficiency is steadily decreasing as the operation frequency increases.

2.1.3 Nonlinearity of Ideal Schottky Diode

As already discussed, the harmonic generation relies mainly on the nonlinearity of the device. In the case of Schottky diodes, the nonlinear junction capacitance is the main source of the nonlinearity. Good understanding of the nonlinear behavior of junction capacitance is essential for its application in harmonic generation. Formulas in closeform have to be derived [36] showing the correlation between the doubler performance (maximum input power, efficiency) and the nonlinear capacitance of varactor physical parameters(elastance $S = 1/C$, barrier height eφ and junction capacitance at 0 V C_{j0}). These were obtained under certain conditions i.e. constant doping epitaxial layer, presence of only fundamental and second harmonics, diode being fully driven and losses arising only from a constant R_s.

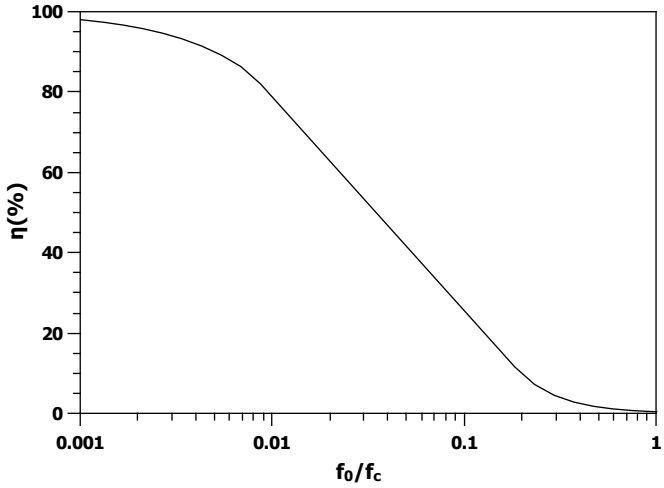


Figure 2.4: The dependence of multiplication efficiency on f_0/f_c

For a Schottky diode with constant doping profile, the capacitance-voltage characteristics can be adopted from equation.2.5 to

$$C = \frac{1}{S} = \frac{C_{j0}}{\sqrt{1 - \frac{v}{\varphi}}} \tag{2.13}$$

Where C_{j0} is the junction capacitance at zero voltage and φ is $V_{bi} - V_T$.

The elastance modulation factor was defined to be the coefficients when using the series of all harmonic components in Eq.2.14 to describe the nonlinearity of elastance.

$$s = S_0(1 + m_1 e^{j\omega t} + m_1{}^* e^{-j\omega t} + m_2 e^{j2\omega t} + m_2{}^* e^{-j2\omega t} + ...), \tag{2.14}$$

By limiting the harmonics up to second order (ideal frequency doubler), the elastance modulation factor for the fundamental and second harmonic can be derived with a self-consistent method to be $|m_1| = 0.502$ and $|m_2| = 0.166$ respectively. The fully driven assumption requires that the fundamental signal is sinusoidal with an amplitude of $\varphi - V_{bias}$. The relation between V_{bias} and S_{bias} is given by

$$V_{bias} = \varphi - \varphi(C_0 S_{bias})^2(1 + 2|m_1|^2 + 2|m_2|^2) \tag{2.15}$$

The power handled by such a nonlinear capacitance satisfying the above assumptions is expressed by

$$P_c = 4\varphi^2 C_{j0}(C_{j0} S_{bias})^3 \omega |m_1|^2 |m_2| \tag{2.16}$$

where the S_{bias} represents the elastance at the chosen operation point. The bias voltage and breakdown voltage play their role through S_{bias}. The resulted output power has exactly the same expression due to Manley-Rowe energy relations, when no lossy elements exist. For the case of constant R_s, the power loss of fundamental and second harmonic are

$$\begin{cases} P_{loss1} = 4\varphi^2 {C_{j0}}^2 (C_{j0} S_{bias})^2 \omega^2 |m_1|^2 R_s \\ P_{loss2} = 16\varphi^2 {C_{j0}}^2 (C_{j0} S_{bias})^2 \omega^2 |m_2|^2 R_s \end{cases} \tag{2.17}$$

Overall, the resulted input power, output power and conversion efficiency of a Schottky diode under the above assumptions are

$$\begin{cases} P_{in} = P_c + P_{loss1} + P_{loss2} \\ P_{out} = P_c \\ \eta = \dfrac{P_{out}}{P_{in}} \end{cases} \tag{2.18}$$

Having the above relationship unfolded, the performance of frequency doubling for a diode with specific capacitance-voltage characteristics can be easily obtained. A diode with barrier height (eφ) of 0.85 eV, junction capacitance at zero volte (C_{j0}) of 50 fF, series resistance (R_s) of 5 Ω was evaluated to represent the above relationship in an intuitive manner. The capacitance-voltage characteristics are given in Fig.2.5 assuming a breakdown voltage of 20 V. With this breakdown voltage of 20 V set, the maximum bias voltage allowed is about -10 V. Using this diode as frequency doubler, the resulting input and output power versus bias voltage are given in Fig.2.6.

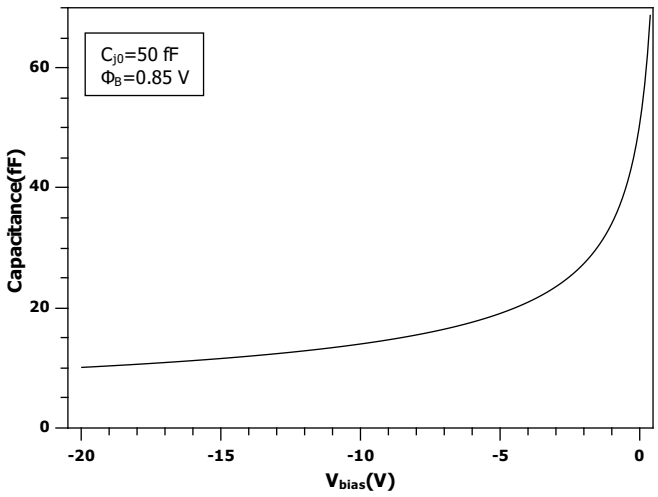


Figure 2.5: C-V characteristics of a diode with φ =0.85 V, C_{j0}=50 fF

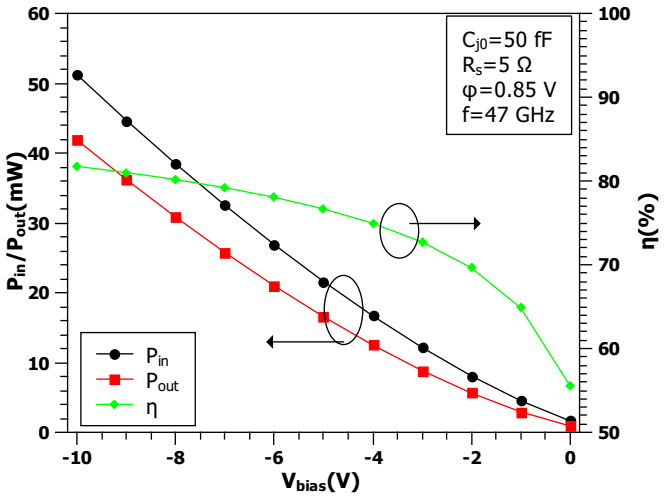


Figure 2.6: Doubler input and output power using the diode characteristics in Fig.2.5

As shown in the figure, the input power increased from 21 mW to 51 mW for a bias voltage of -5 V and -10 V respectively. This requires the breakdown voltage to be -10 V and - 20 V respectively. The resulted 2.5 times increase of power for a change of maximum bias voltage from -5 V to -10 V suggests a dependence $P_c \propto {V_{br}}^{1.3}$. As expected from Eq.2.15 and 2.16, the power that can be handled by such a diode is proportional to the breakdown voltage to the power of 1.5, when (φ) is relatively small compared to V_{bias}. Nevertheless, the power handling capability of a diode increases considerably with breakdown voltage.

The output power P_{out} in Fig.2.6 poses the same trend as P_{in}. This can be explained by the dissipation power $P_{loss} \propto V_{br}$ as shown in Equation.2.17. However, this is not true in practice since a larger R_s is the by-product of enhancing breakdown voltage, as will be discussed later.

In the same manner, the impact of φ and C_{j0} on the frequency doubler were also examined and are shown in Fig.2.7 and Fig.2.8. The increase of both φ and C_{j0} results in larger power absorbed by the diode. This is natural given the fact that a larger capacitance (also charge) resulted from increased φ or C_{j0}. Meanwhile, the current becomes higher and results in higher loss. This is consistent with the rule that higher conversion efficiency can be achieved for diodes with larger cut-off frequency.

The analytical approach discussed here represents very well the operation of harmonic generation from a nonlinear capacitance, which is correlated directly to the diode structure. The R_s, on which the conversion loss relies, was however set without considering its physical significance. It's thus necessary to study the evaluation of R_s for a given diode structure.

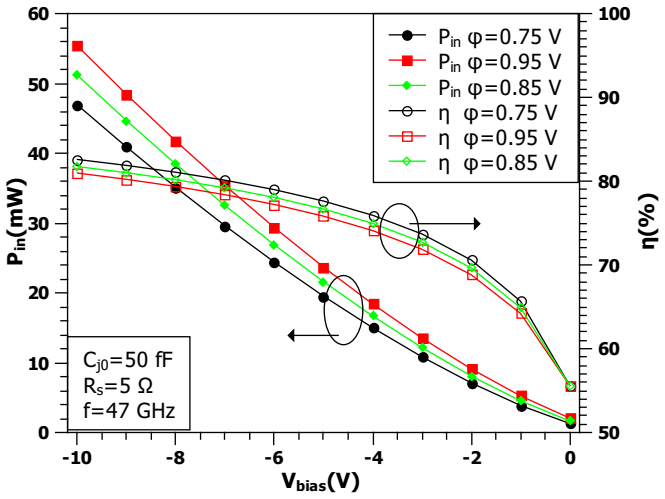


Figure 2.7: The dependence of input power and efficiency on φ

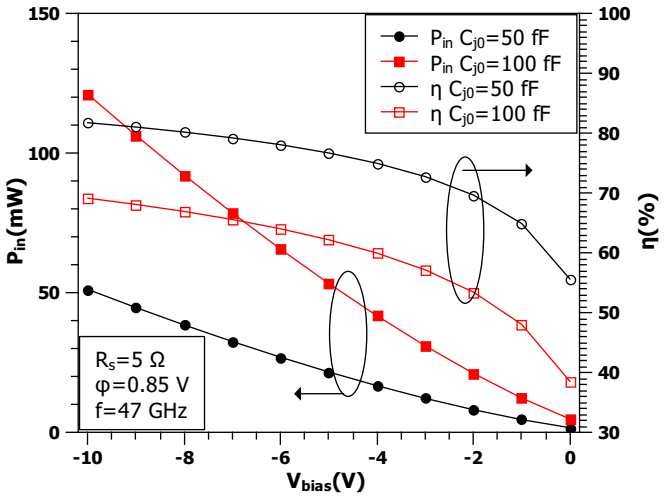


Figure 2.8: The dependence of input power and efficiency on C_{j0}

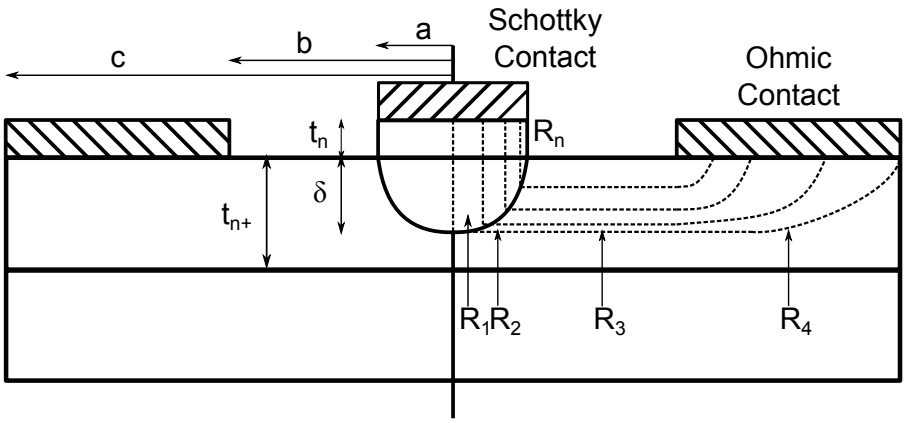


Figure 2.9: Schematic for determining series resistance, redrawn from [37]

2.1.4 Series Resistance

The role of series resistance R_s and its effects on doubler performance will be discussed in this section to allow for further understanding of its impact on diode performance and permit its minimization. A planar diode with the cross section shown in Fig.2.9 is discussed here. The path of current flow has been divided into several segments and the R_s of the diode is calculated by the sum of all the resistances corresponding to each segment. The analytical equations given below are based on previous reports [37, 38].

The resistance of the N^- layer is considered to correspond to a cylinder where the area perpendicular to current flow is the same as that of the mesa, and its thickness t_{n^-} equals the undepleted N^- layer.

$$R_n = \frac{(t_{n^-} - t_d)\rho_{n^-}}{\pi a^2} \tag{2.19}$$

where t_d is the depletion layer thickness, ρ_{n^-} is the resistivity of the N^- layer which depends on the doping concentration N_D and carrier mobility μ; t_d is given by Equation.2.3.

R_1 represents the spherical cap under the mesa, with base radius a and cap height δ_{n^+},

$$R_1 = \frac{\rho_{n^+}\delta_{n^+}}{2\pi(a^2 + {\delta_{n^+}}^2)} \tag{2.20}$$

R_2 is associated with a cylinder under the mesa but without the spherical cap of R_1.

$$R_2 = \frac{\rho_{n^+}}{4\pi\delta_{n^+}} \tag{2.21}$$

R_3 represents the access region between mesa and ohmic metallization.

$$R_3 = \frac{\rho_{n^+}}{2\pi\delta_{n^+}} \ln(\frac{b}{a}) \tag{2.22}$$

R_4 is the resistance of ohmic metallization, which is expressed by Bessel functions.

$$\begin{aligned} R_4 = \frac{\gamma}{\frac{\delta_m}{\rho_m} + \frac{\delta_{n^+}}{\rho_{n^+}}} \{ & \frac{\delta_{n^+}}{\rho_{n^+}} [AI_0(\beta c) + BK_0(\beta c)] + \\ & \frac{\delta_m}{\rho_m} [AI_0(\beta b) + BK_0(\beta b)] \} \end{aligned} \tag{2.23}$$

where

$$A = \frac{1}{2\pi\beta\Delta} [\frac{\rho_{n^+}}{b\delta_{n^+}} K_1(\beta c) + \frac{\rho_m}{c\delta_m} K_1(\beta b)] \tag{2.24}$$

$$B = \frac{1}{2\pi\beta\Delta} [\frac{\rho_{n^+}}{b\delta_{n^+}} I_1(\beta c) + \frac{\rho_m}{c\delta_m} I_1(\beta b)] \tag{2.25}$$

$$\Delta = I_1(\beta c)K_1(\beta b) - I_1(\beta b)K_1(\beta c) \tag{2.26}$$

$$\beta = \left[\frac{1}{\rho_c} (\frac{\rho_m}{\delta_m} + \frac{\delta_{n^+}}{\rho_{n^+}}) \right]^{1/2} \tag{2.27}$$

$$\gamma = \frac{b}{c-b} \ln \frac{c}{b} \tag{2.28}$$

I_i and K_i are modified Bessel functions of the first and second kind, where i denotes the order. ρ_c is ohmic contact resistance, ρ_n ρ_{n^+} and ρ_m are the resistivities of N^- layer, N^+ layer and metal respectively. δ_{n^+} and δ_m are the current distribution depths, which equal the skin depths when the semiconductor layer and metal layer are thick enough. The correction factor γ arises from the radial distribution of current density.

The series resistance was calculated for a GaAs diode structure based on the above equations and the results are shown in Table.2.1[37] . The resulting total resistance is 0.915 Ω,and was found to be slightly different from the measured value of 0.87 Ω in [37]. The observed discrepancy arises from the material parameters used for calculation. It should be noted that the mobility of GaAs, ohmic metal thickness and resistivity were not mentioned in the referenced article.

The resistance of a GaN diode with the same dimensions was evaluated by replacing the GaAs material parameters by those of GaN. This included the mobility, doping and dielectric constant. The resulting total resistance is about 10 times larger for GaN than GaAs. The individual segments of the resistance were also larger , except R_4, which is less dependent on semiconductor material resistivity.

The dependence of series resistance on Schottky contact dimensions is shown in Fig.2.10, where the anode radius was varied from 1 μm to 10 μm, while the cathode radius and

Table 2.1: Example of R_s estimation for GaN and GaAs

Diode Dimensions (µm)	a=8 b=10 c=20 t_n=0.65 t_{n^+}=2.5	
Metal thickness(µm)	t_m=1	
Resistivity($\Omega \cdot$ cm)	$\rho_m = 5 \times 10^{-5}$	
Specific Resistivity ($\Omega \cdot \mathrm{cm}^2$)	$\rho_c = 1 \times 10^{-6}$	
Material	GaAs	GaN
epsilon	13.1	8.9
N_n (cm^{-3})	7×10^{16}	1×10^{17}
μ_n ($\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$)	4780	400
N_{n^+} (cm^{-3})	8×10^{18}	3×10^{18}
μ_{n^+} ($\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$)	1280	200
Calculated R		
$R_n(\Omega)$	0.476	4.31
$R_1(\Omega)$	0.0343	0.589
$R_2(\Omega)$	0.193	3.31
$R_3(\Omega)$	0.0859	1.48
$R_4(\Omega)$	0.127	0.651
$R_{total}(\Omega)$	0.915	10.3

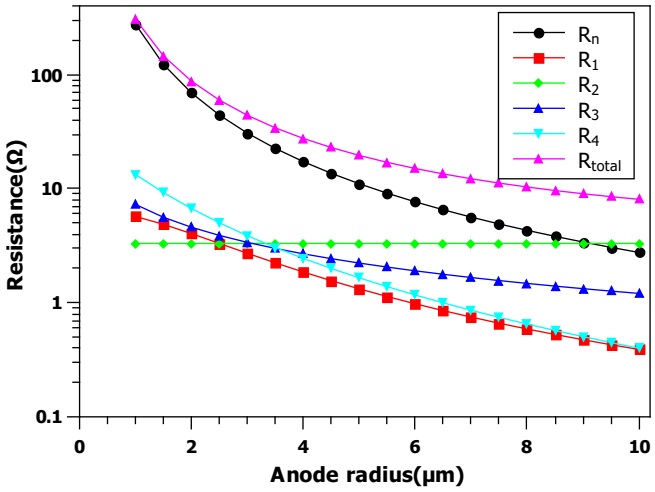


Figure 2.10: Evaluated resistance of GaN diode versus diode anode size

space between anode and cathode were maintained at 10 μm and 2 μm respectively. R_n was found to be the dominant part of the total series resistance when the diode is scaled down. R_2 is almost constant, contributing mainly in the total resistance of large diodes but less for smaller diodes. The other three diode segments increase steadily with decreasing diode radius. It can be concluded that smaller diodes require better attention of the N^- layer design.

The analysis of R_s shown above assumes the Schottky contact being enclosed entirely by ohmic metallization, while for most practical cases the ohmic metal is not a complete ring. Thus the series resistance value is in practice higher than estimated above.

2.2 Analysis by numeric simulation

Although useful conclusions can be drawn from the analytical considerations made above, these are limited to specific designs as in the case discussed here, i.e. constant doping profile for the device and only second harmonic generation considered for the multiplier circuit. However, in practice an arbitrary doping profile may be required and Schottky diodes can in such a case be used as a tripler (for 3^{rd} order harmonic generation). Numerical simulation offers a universal approach in such a situation. Moreover, numerical simulation provides insight into the internal physical mechanisms associated with device operation. Techniques of this type are discussed in this section and used to analyze different device structures.

2.2.1 Introduction of Semiconductor Device Numerical Simulation

A flowchart of the numerical simulation procedure used for the diodes and also applying in general to semiconductor devices is shown in Fig.2.11. In addition to defining the device geometry and employing an appropriate mesh, material parameters and good physical understanding are a key for successful simulation. Material parameters define the basic properties of a semiconductor material, such as bandgap, dielectric constant, etc. Physical models describe a specific physical mechanism associated with device operation. Examples of them are the mobility model and impact ionization model. Some physical models are valid for all semiconductor materials, by simple variation of the material parameter values.

Following the definition of device geometry, material parameters and physical models, the device can be analyzed by solving a series of partial differential equations. The basic equations for semiconductor devices are the Poisson, Current Continuity and Carrier Transport (also referred as Current Density) Equations. These coupled equations are solved numerically by either finite element or finite difference method.

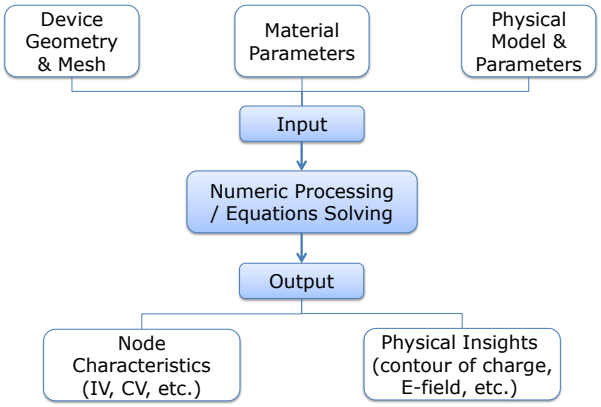


Figure 2.11: Flowchart of semiconductor device numerical simulation

The electrical characteristics at each node of the device can be obtained from the numerical simulation, including static current-voltage, capacitance-voltage, transient current-voltage characteristics and S-parameters under high frequency operation. Physical insights into device operation is given by numerical simulation results, such as charge distribution, E-field strength, etc. These complement the understanding of device operation obtained through experimentation.

2.2.2 Parameters for GaN Based Device Simulation

Unlike Silicon, the understanding of material parameters of Nitrides is far from mature. For example, the bandgap of InN has recently been recognized to be around 0.7 eV, far below the earlier predicted value of 2 eV [39]. No such major parameter discrepancy has been reported for GaN, detailed bandgap material parameters are listed below for reference. Parameters for GaAs are also given, as GaAs Schottky diodes will also be simulated numerically for comparison. Since no ternary compound was used in this study, only the physical model dependence on doping concentration and temperature are discussed.

Temperature dependence of Bandgap

The bandgap is a function of temperature for both GaN and GaAs, and can be expressed by Eq.2.29

$$E_g(GaN) = 3.507\,\mathrm{eV} - \frac{0.909 \times 10^{-3}\,\mathrm{eV/K} \cdot T^2}{T + 830\,\mathrm{0K}} \tag{2.29}$$

Table 2.2: Material parameters used in numerical simulation (at 300K)

Material	GaAs	GaN
Dielectric constant	13.2	8.9
Bandgap(eV)	1.42	3.43
Electron Affinity(eV)	4.07	4.31
Conduction band density of states(cm^{-3})	4.35×10^{17}	2.24×10^{18}
Valence band density of states(cm^{-3})	1.29×10^{19}	2.51×10^{19}
Intrinsic carrier density(cm^{-3})	2.67×10^{6}	1.06×10^{-10}
Electron thermal velocity($\mathrm{cm/s}$)	4.51×10^{7}	2.61×10^{7}
Hole thermal velocity($\mathrm{cm/s}$)	1.46×10^{7}	1.17×10^{7}

$$E_g(GaAs) = 1\,519\mathrm{eV} - \frac{5.405 \times 10^{-4}\,\mathrm{eV/K} \cdot T^2}{T + 204.0\,\mathrm{K}} \tag{2.30}$$

.

The above equations predict a decrease of GaN bandgap from 3.43 at 300 K to 3.39 at 400K and 3.34 at 500K. While for GaAs the bandgap changes from 1.42 at 300 K to 1.376 at 400 K and 1.327 at 500 K.

Mobility Model

The electron mobility model of GaN is based on Monte Carlo simulation as reported in [40, 41], where both low field and high field mobility were fitted with an empirical equation. The low field mobility is given below as a function of temperature and doping concentration

$$\mu_{LE}(T,N) = 295\,\frac{\mathrm{cm}^2}{\mathrm{V\,s}}\left(\frac{T}{300\,\mathrm{K}}\right)^{-1.02} + \frac{1165.7\,\frac{\mathrm{cm}^2}{\mathrm{V\,s}}\left(\frac{T}{300\,\mathrm{K}}\right)^{-3.84}}{1 + \left[\frac{N}{1\times10^{17}\,\mathrm{cm}^{-3}\left(\frac{T}{300\,\mathrm{K}}\right)^{3.02}}\right]^{0.66(T/300\,\mathrm{K})^{0.81}}} \tag{2.31}$$

In case of operation under high E-field, the electron velocity saturation has to be considered. The high field mobility as a function of low field mobility and E-field are given by

$$\mu_{HE} = \frac{\mu_{LE}(T,N) + 1.9064 \times 10^{7}\,\frac{\mathrm{cm}}{\mathrm{s}}\left(\frac{E^{7.2044-1}}{220\,893.6\,\frac{\mathrm{kV}}{\mathrm{cm}}^{7.2044}}\right)}{1 + 6.1973\left(\frac{E}{220\,893.6\,\frac{\mathrm{kV}}{\mathrm{cm}}}\right)^{0.7857} + \left(\frac{E}{220\,893.6\,\frac{\mathrm{kV}}{\mathrm{cm}}}\right)^{7.2044}} \tag{2.32}$$

Based on these two equations, the low field mobility and velocity are calculated at selected temperature, doping concentration and a wide range of E-field values. These values are shown in Fig.2.12 and Fig.2.13, that illustrate the mobility and velocity E-field dependence at various temperatures and doping concentration.

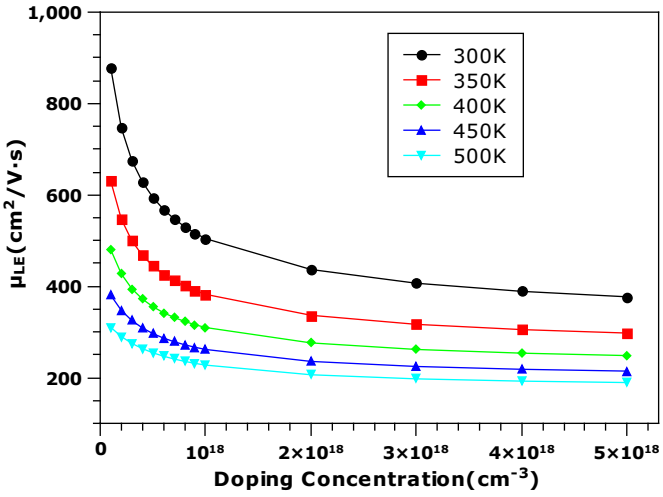


Figure 2.12: GaN low field mobility

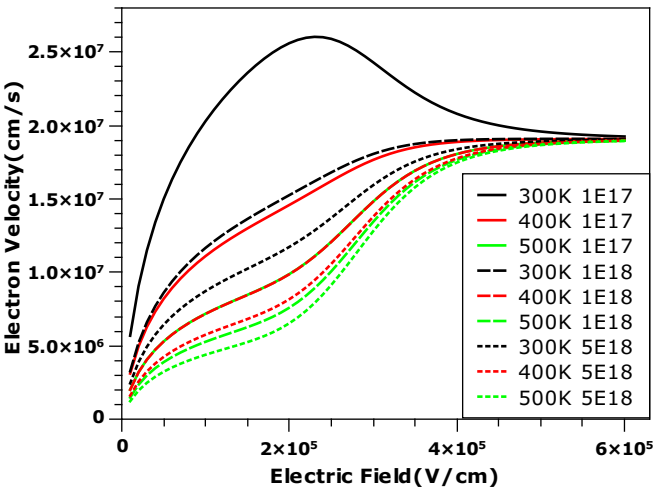


Figure 2.13: GaN electron velocity

In case of GaAs, the low field mobility used for a comparative study is provided as a function of doping concentration. For example, for a doping concentration of $1 \times 10^{17}\ \mathrm{cm}^{-3}$ and $1 \times 10^{18}\ \mathrm{cm}^{-3}$ the mobility is 4600 cm^{-3} $cm^2/V\dot{s}$ and 2600 $cm^2/V\dot{s}$ respectively.

The temperature dependence is given by the simple relation

$$\mu_{LE,GaAs}(T,N) = \mu_{GaAs}(N)\frac{300\,\mathrm{K}}{T} \tag{2.33}$$

The high field mobility is calculated as a function of saturation velocity. GaAs is known for its intervalley scattering which causes a Negative Differential Mobility (NDM). Its mobility can be expressed as

$$\mu_{HE,GaAs} = \frac{\mu_{LE,GaAs}(T,N) + (\frac{v_{sat,GaAs}}{E})(\frac{E}{4\,\frac{\mathrm{kV}}{\mathrm{cm}}})^4}{1 + (\frac{E}{4\,\frac{\mathrm{kV}}{\mathrm{cm}}})^4} \tag{2.34}$$

As explained in [41], the NDM model may introduce instability in the numerical process. For the GaAs Schottky diode simulated in this study, the saturation velocity is more important than the NDM. Thus the following modified mobility model is used as default expression.

$$\mu_{HE,GaAs} = \mu_{LE,GaAs}(T,N)[\frac{1}{1 + (\frac{\mu_{LE,GaAs}(T,N)\cdot E}{v_{sat,GaAs}})^2}]^{1/2} \tag{2.35}$$

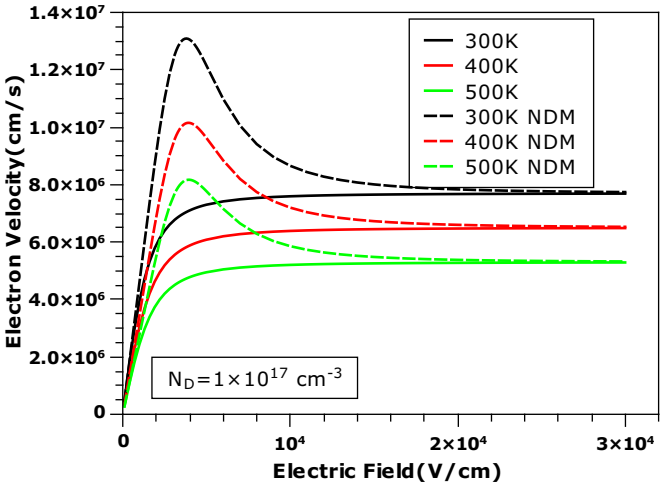
where the dependence of saturation velocity on temperature is described by a linear function

$$v_{sat,GaAs} = 1.13 \times 10^7\,\frac{\mathrm{cm}}{\mathrm{s}} - 1.2 \times 10^6\,\frac{\mathrm{cm}}{\mathrm{s\,K}} \cdot T \tag{2.36}$$

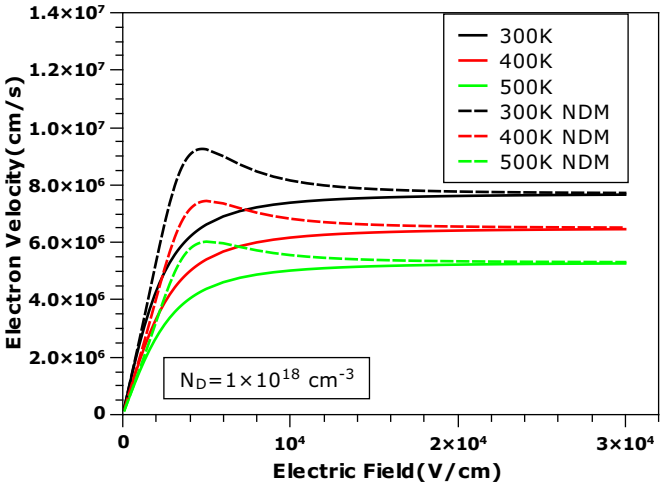
The resulting electron velocity is plotted versus electric filed in Fig.2.14 for the sake of comparison. The velocity based on both NDM model and a modified model are also given to highlight the difference. The modified high field mobility model assumes that the electron velocity increases steadily with E-field until reaching the saturated velocity.

Impact Ionization Model

The breakdown voltage is evaluated by calculating the impact ionization integral. The ionization integral is introduced as a criterion for determining when avalanche is triggered. The integration of generation rate along a distance corresponds to the multiplication efficiency of newly generated electron-hole pairs over this distance. Once the



(a) Doping $1 \times 10^{17} cm^{-3}$



(b) Doping 1×10^{18} cm^{-3}

Figure 2.14: GaAs electron velocity versus E-field

Table 2.3: Parameters of Selberherr's model used in simulation (at 300K)

Material	GaAs	GaN
$A_N(\mathrm{cm}^{-1})$	1.889×10^5	2.52×10^8
$B_N(\mathrm{V/cm})$	5.57×10^5	3.41×10^7
β_N	1.82	1
$A_P(\mathrm{cm}^{-1})$	2.215×10^5	5.37×10^6
$B_P(\mathrm{V/cm})$	6.57×10^5	1.96×10^7
β_P	1.75	1

integral value exceeds 1, the number of electron-hole pairs increases resulting in high current which then leads to breakdown.

In the simulation, the E-field over the entire device structure is calculated first, followed by the derivation of the E-field dependent impact ionization generation rate, based on which the integral is further evaluated along E-field lines. This method avoids current equation solving, which very often causes instability in the numerical process. The generation rate is described by Selberherr's model for both GaN and GaAs material, but with different coefficients.

$$\alpha_n = A_N exp[-(\frac{B_N}{E})^{\beta_N}] \tag{2.37}$$

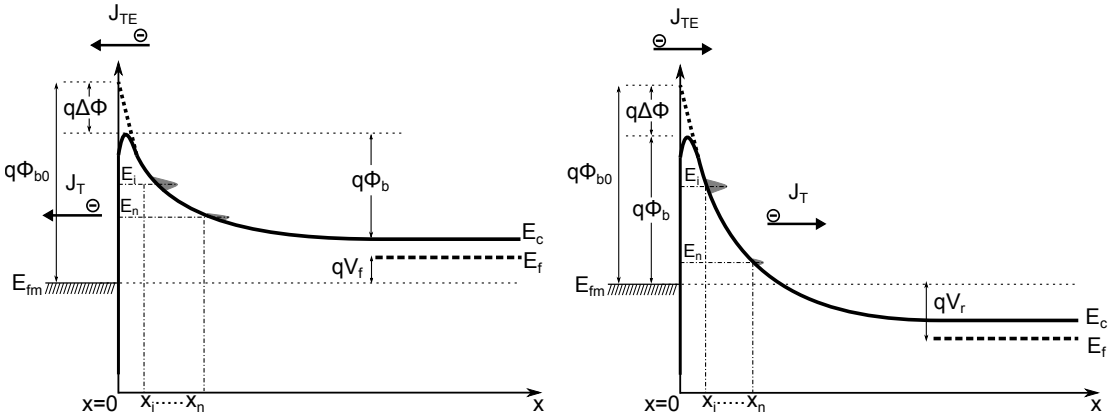
$$\alpha_p = A_P exp[-(\frac{B_P}{E})^{\beta_P}] \tag{2.38}$$

The temperature dependence of this model is given by temperature dependent coefficients; all the coefficients listed in Table.2.3 are temperature dependent. However, only the breakdown voltage at room temperature will be discussed, since the temperature dependence of these coefficients was not available in literature.

Carrier Transport Model for Schottky Contact

Both Thermionic emission theory and Thermionic Field emission (tunneling) were considered in the simulation. Thermionic emission theory describes the current flow through the Metal-Semiconductor (MS) contact due to electrons with energy above the barrier height $q\Phi_b$. The current depends therefore on barrier height exponentially, as given in Eq.2.6 and 2.7. The $q\Phi_b$ value faced by the electrons is different depending on the bias voltage polarity. For the case where electrons need to be emitted from metal to semiconductor, i.e. for a reverse biased MS contacts (Fig.2.15(b)), $q\Phi_b$ remains constant. The resulting current is thus also constant for any reverse bias voltage. In the forward biased condition (Fig.2.15(a)), $q\Phi_b$ decreases as the forward voltage increases. This gives naturally an exponentially increasing current versus forward voltage.

$$J_T = \frac{A^* T_L}{k} \int_E^\infty \Gamma(\xi) \ln[\frac{1 + f_s(\xi)}{1 + f_m(\xi)}] d\xi \tag{2.39}$$



(a) Forward (b) Reverse

Figure 2.15: Schematic of Schottky contact band structure

The tunneling current can be expressed by the general form given in Eq.2.39, where $\Gamma(\xi)$ is the tunneling probability, $f_s(\xi)$ and $f_m(\xi)$ are the Maxwell Boltzmann distribution functions in semiconductor and metal respectively. As can be seen, both the tunneling probability and electron distribution are given as a function of energy. In order to calculate J_T for a device structure represented by discrete grids, one needs to find the local generation rate by applying a gradient on J_T, which provides the generation rate for a specific grid. This generation rate will be further included into the current continuity equations [42].

$$\begin{aligned} G(x) &= \frac{1}{q}\nabla J_T \\ &= \frac{1}{q}\frac{dJ_T}{d\psi}\nabla\psi \\ &= \frac{dJ_T}{dE}\vec{E} \end{aligned} \tag{2.40}$$

where ψ,$E = -q\psi$,$\vec{E} = -\nabla\psi$ are the potential, energy level, and electric field respectively.

The tunneling probability as a function of grid location is given by the Wentzel-Kramers-Brillouin (WKB) approximation by assuming a triangular barrier shape.

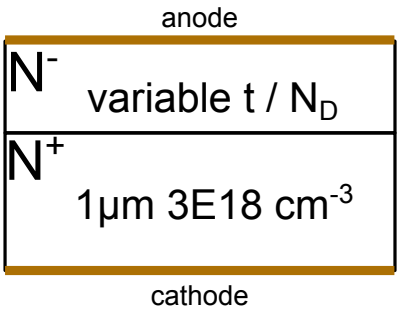
$$\Gamma(x) = exp[\frac{-4\sqrt{2m^*}x}{3\hbar}(E_{fm} + q\Phi_b - E_c(x))^{1/2}] \tag{2.41}$$

A key parameter of this model in Silvaco [41] is the distance from electrode, within which all the grid points will be calculated in a way shown above. The default value of this distance is 10 nm, which is found sufficient for our study.

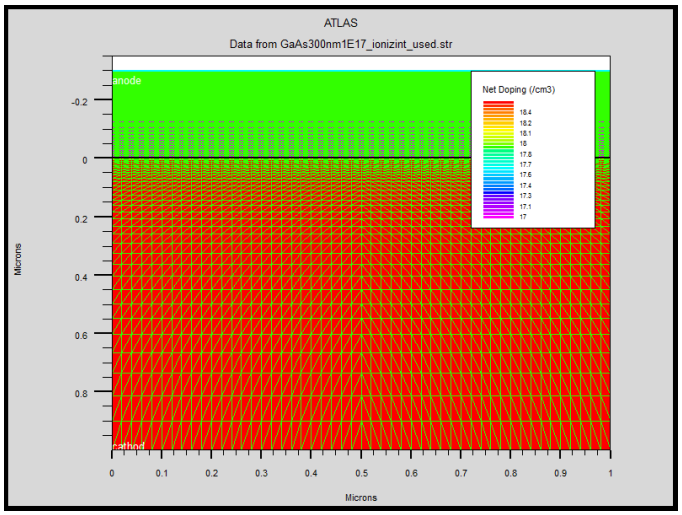
2.3 Simulation Results

Device Structure

The vertical structure shown in Fig.2.16(a) was used as common reference for comparing GaN over GaAs. This simplified structure contains a N^- layer for Schottky contact and a N^+ layer for Ohmic contact. Various thickness and doping concentration values were considered for the N^- layer, while the N^+ layer was maintained to be 1 μm thick with a doping concentration of 3×10^{18} cm^{-3} for both GaAs and GaN diodes. A typical structure cross-section generated by simulation is shown in Fig.2.16(b), where the dense mesh grid covering the entire N^- layer guaranteed the simulation accuracy.



(a)



(b)

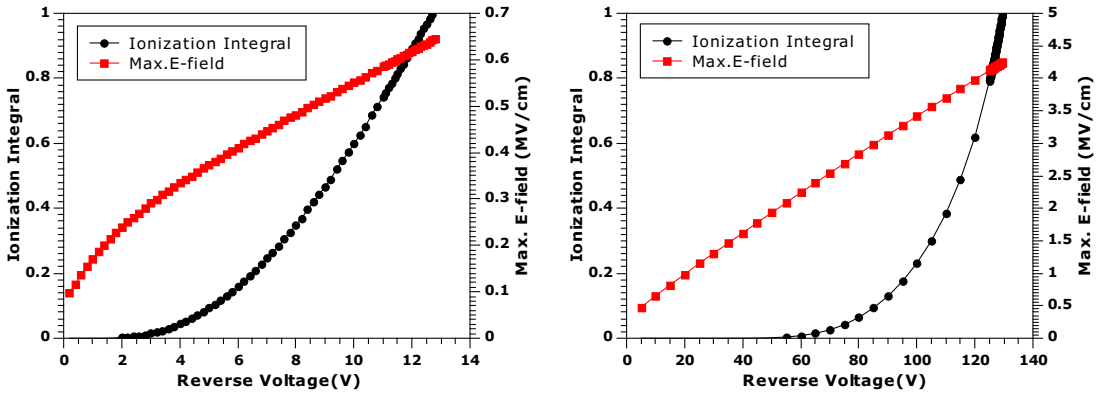
Figure 2.16: (a)schematic of epi-structure used in simulation (b) an example of formed structure and the mesh grids

Though planar diodes are the workhorses for most studies, a simple vertical diode structure will be discussed here as applied to the frequency conversion and signal control studies conducted in this thesis. This simple structure allows to focus on the material properties without being impacted by the more complex design of planar devices due for

example to horizontal distribution of electric fields, anisotropic mobility, etc. Numeric efficiency is also enhanced due to the simplified structure.

Breakdown voltage

The calculated ionization integral and corresponding maximum electric field are shown in Fig.2.17 for both GaAs and GaN diodes with a N^- layer of 300 nm thickness and 1×10^{17} cm^{-3} doping. The simulated breakdown voltages were 12.8 V and 129.6 V for GaAs and GaN respectively, corresponding to an electric field of 0.63 MV/cm and 4.25 MV/cm. The greater breakdown voltage for GaN diodes allows a higher RF input power to be applied to the diodes. N^- layers with different thickness and doping concentration



(a) GaAs (b) GaN

Figure 2.17: Simulated ionization integral and electric field vs. bias voltage

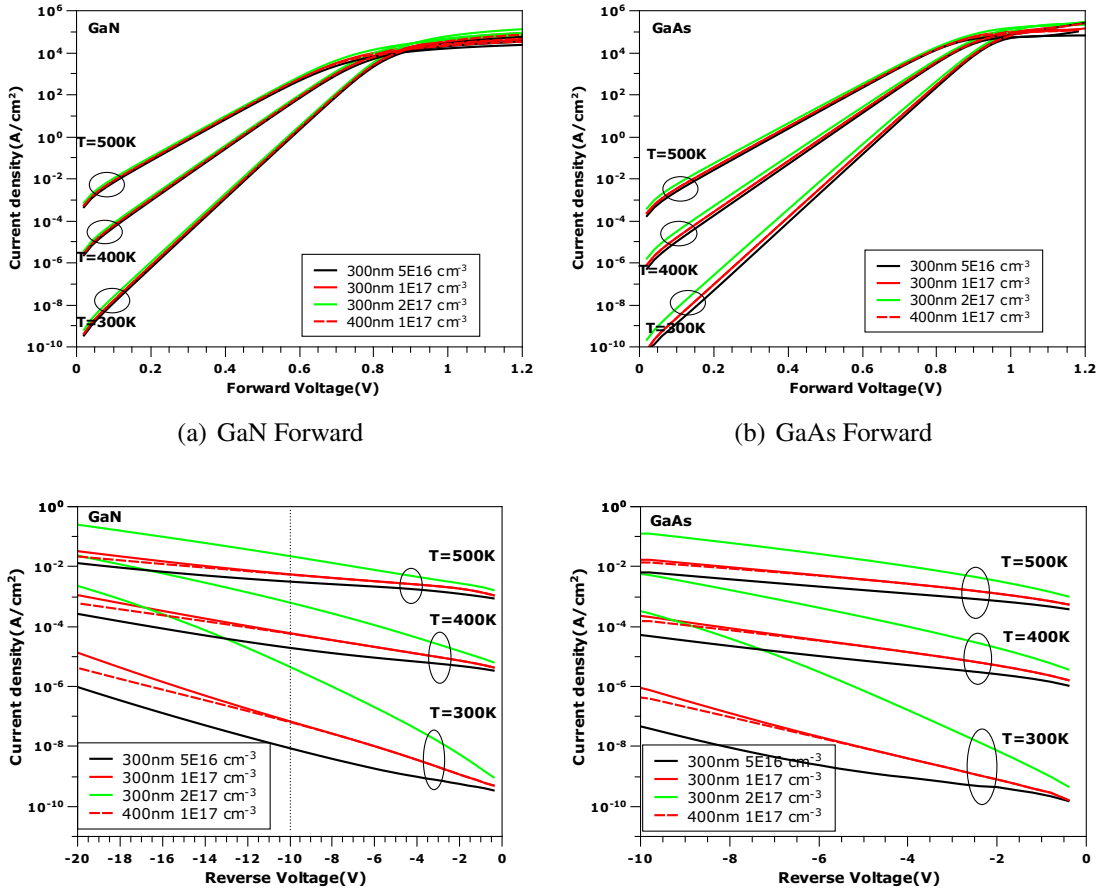
were simulated and the results are listed in Tab.2.4. In all cases, the breakdown voltage of GaN diodes is about 10 times larger than GaAs. The difference is even greater for thicker N^- layers.

Table 2.4: Breakdown voltage based on Ionization Integral (at 300K)

t & N_D	GaAs	GaN
300nm 5×10^{16} cm^{-3}	13.2V	132.8V
300nm 1×10^{17} cm^{-3}	12.8V	129.6V
300nm 2×10^{17} cm^{-3}	11.2V	122.8V
400nm 1×10^{17} cm^{-3}	15.1V	168.2V
500nm 1×10^{17} cm^{-3}	16.5V	204.5V

I-V characteristics

The simulated static I-V characteristics are shown in Fig.2.18, for variable N^- layer doping, thickness as well as temperature. In general, the current is greater in both the forward and reverse region when the doping or temperature are higher. The scale of the current axis is the same, for easier comparison. Under the same structure conditions, i.e. same barrier height, N^- layer doping, thickness, temperature, GaN diodes show slightly higher forward current than GaAs. This can be explained by the greater Richardson constant of GaN over GaAs. Another feature observed from the forward I-V characteristics R_s of GaN diodes, is their smaller saturation voltage in the forward region. This results naturally from the lower mobility of GaN. In the reverse region, the voltage applied to GaAs



(a) GaN Forward

(b) GaAs Forward

(c) GaN Reverse

(d) GaAs Reverse

Figure 2.18: Simulated I-V characteristics

is limited to -10 V while it's -20 V for GaN. Thanks to the wide bandgap, GaN leads in lower reverse leakage current than GaAs. The difference between the two technologies is one order of magnitude when comparing them at -10 V.

Series resistance

R_s is considered to be one of the key diode figures-of-merit and represents how lossy a diode is. The R_s of the above simulated diodes was extracted from the forward I-V characteristics and is shown in Fig.2.19. GaN diodes have undoubtedly a larger R_s than GaAs, due to the inferior mobility of GaN.

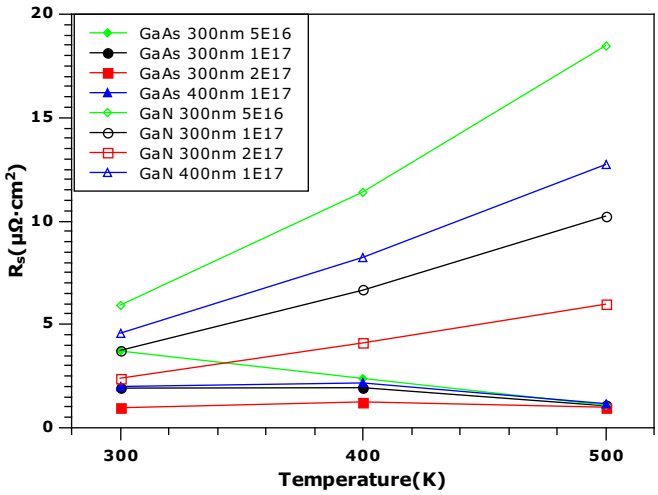


Figure 2.19: Series resistance extracted from forward IV curves in Fig.2.18(a) and Fig.2.18(b)

Considering the diode resistance at 300K, the values of GaN based diodes is 2-3 times higher than for GaAs with the same N^- layer doping. This difference increases to 6-18 times when the temperature is 500K. The R_s temperature dependence for GaAs is not monotone; the R_s increases when the temperature is elevated from 300K to 400K, while R_s decreases when the temperature increases further to 500K. This is due to the two temperature dependent mechanisms involved, namely mobility and thermally activated carriers, that have reverse temperature dependence and compensate each other at a medium temperature. The R_s increase of GaN at elevated temperature relies on mobility drop, since the contribution of thermally activated carriers can be neglected due to the properties of wide bandgap materials.

C-V characteristics

Quasi-static C-V characteristics were obtained by AC analysis and shown in Fig.2.20. For the same barrier height, N^- layer doping, thickness, and bias voltage, GaAs diodes show a larger capacitance than GaN. This is due to the different depletion region width arising from the dielectric constant difference (see Eq.2.5 and Eq.2.5).

C_0 (with bias voltage of 0 V) is larger for diodes with higher doping concentration. Despite the doping concentration, for given N^- layer thickness C_{min} remains practically constant independent of carrier concentration. This corresponds to the case of completely depleted N^- layer. For the same reason, the 400 nm thick N^- layer exhibits the same C_0 but smaller C_{min} than the 300 nm thick N^- layer with same doping concentration.

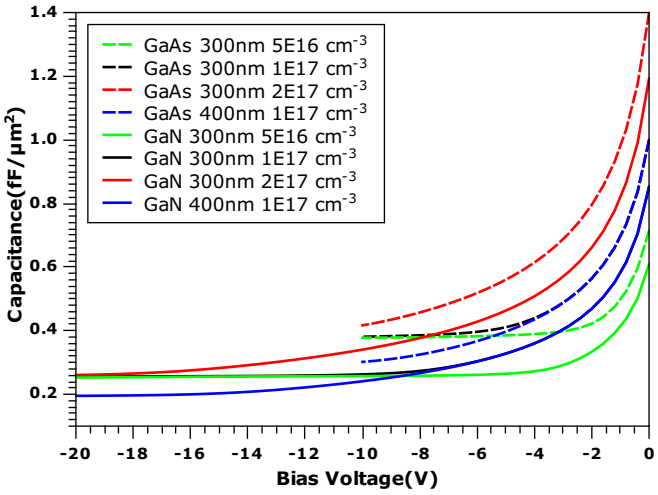


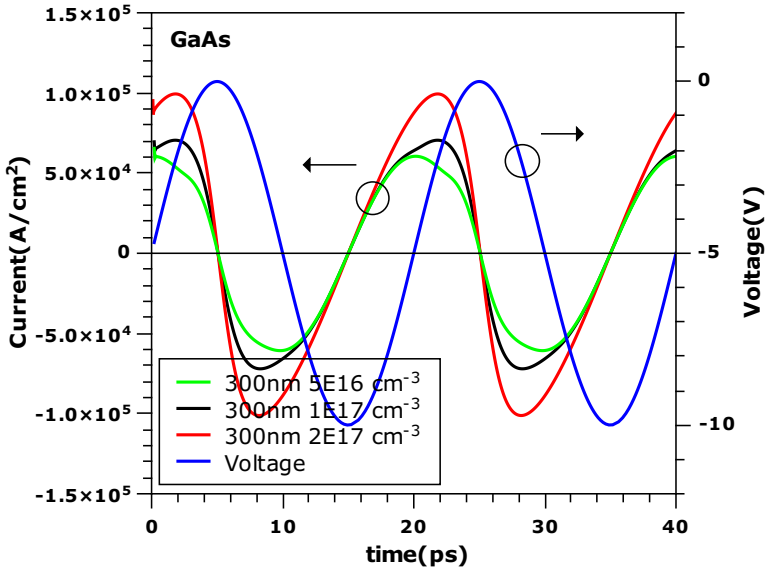
Figure 2.20: Simulated capacitance-voltage characteristics

Time Domain Transient Analysis

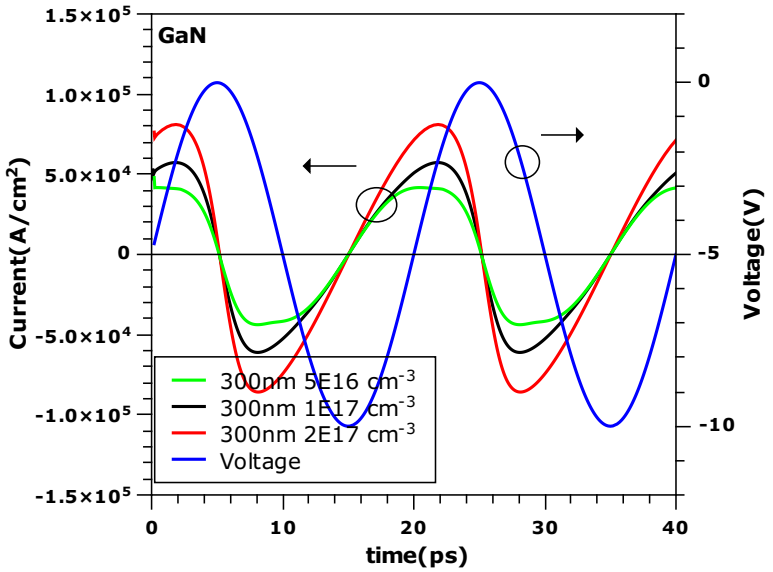
Transient analysis was performed by applying a sinusoidal voltage stimulus to the diodes. Consistent with previous simulations, the operation of GaAs diodes was limited to a peak-to-peak amplitude of 10 V and offset of -5V. GaN diodes were simulated with the same stimulus condition for comparison. A 20 V amplitude and offset of -10 V was applied to GaN diodes for revealing the advantage of power handling.

With a 50 GHz stimulus, the obtained current waveforms are shown in Fig.2.21 for 300 nm thick N^- layer and variable doping concentration. Lower doping corresponds to a lower current since less electrons participate in the process. For the same doping concentration, GaN diodes lead to a smaller transient current amplitude than GaAs diodes. This can be explained by the lower electron mobility of GaN material. As a result, diodes with lower current have smaller power exchange with the signal source in one signal cycle. The instant power is given in Fig.2.22.

The time domain waveforms contain useful information, such as power handling capability and nonlinearity, which requires further data processing. Applying Fourier Transform on the current waveform $I(t)$, the amplitude of current on each harmonic order (I_1,I_2,I_3...) can be obtained. The squared current amplitude corresponds to power, and the diode nonlinearity can be evaluated by $\frac{I_i^2}{\sum_1^n I_i^2}$.

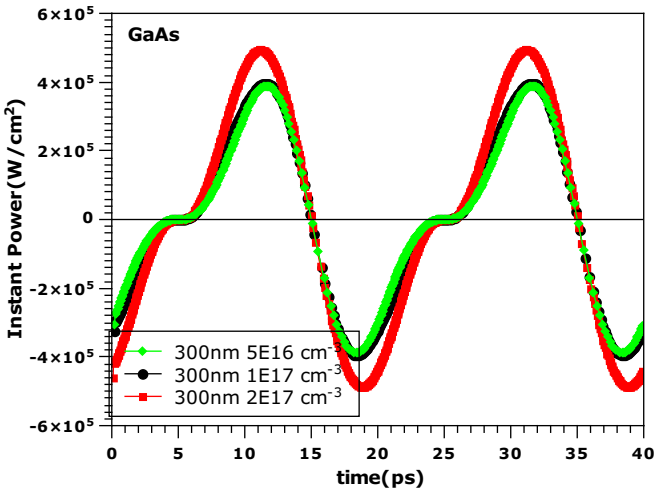


(a) GaAs V(t) and I(t)

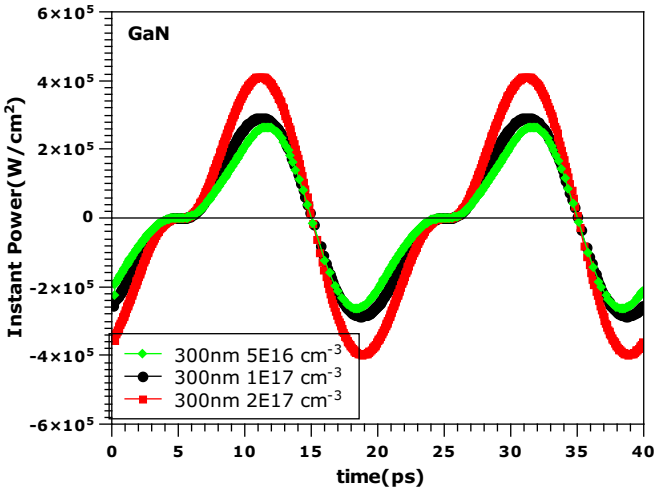


(b) GaN V(t) and I(t)

Figure 2.21: Transient V(t),I(t) characteristics



(a) GaAs P(t)



(b) GaN P(t)

Figure 2.22: Transient P(t) characteristics corresponds to Fig.2.21

The positive instant power corresponds to power absorption of the diode from the source, while the negative instant power corresponds to power provided by the diode. Thus the integration over one time period reveals the power handling capability of each diode, where the positive half-cycle represents the power handling capability and the negative half-cycle represents a reactive power stored in the diode over the positive half-cycle. The difference between the two corresponds to power loss. It has to be pointed out that the results were obtained from one operation cycle and the signal frequency has to be taken into account when comparing with experimental results.

Considering a 300 nm thick, $1 \times 10^{17}\ \mathrm{cm}^{-3}$ doped N^- layer as reference structure, and 10 V V_{pp} (-5 V offset) sinusoidal voltage as reference stimulus, one obtains the results discussed next. A 20 V V_{pp} (-10 V offset) stimulus was applied to GaN diodes in order to evaluate the power enhancement due to the increased breakdown voltage.

As shown in Fig.2.23(a), higher absorbed power , reactive power as well as loss can be observed for heavier doped diodes. The loss, denoted by P_{abs}-P_{rac}, was larger for GaN than GaAs devices. When doping was increased to $2 \times 10^{17}\ \mathrm{cm}^{-3}$, the loss remained small at increased absorbed power levels, which indicates that the doping can be further increased.

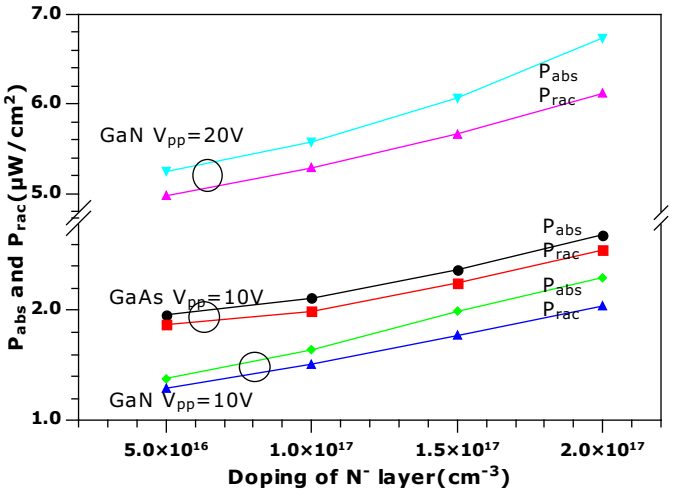
The nonlinearity comparison shown in Fig.2.23(b) suggests that GaN diodes produce greater harmonics than GaAs. This can be attributed to the larger C_0/C_{min} ratio of GaN diodes. The 2_{nd} harmonic ratio of GaN diodes driven by 10 V V_{pp} stimulus (green diamonds in the figure) showed a fast increase when the doping increased from 5×10^{16} cm^{-3} to $1 \times 10^{17}\ \mathrm{cm}^{-3}$, but remained nearly unchanged when the doping increased further. Similar "saturation" trends were observed for all 3^{rd} and 2_{nd} harmonics generated by GaAs diodes; the absolute amplitude of 2_{nd} harmonic generated was increased due to the increased absorbed power.

The dependence of power performance on N^- layer thickness is shown in Fig.2.24(a), where the doping was fixed as $1 \times 10^{17}\ \mathrm{cm}^{-3}$. It was found that P_{abs} and P_{rac} was smaller for thicker N^- layer, while the loss increased with N^- layer thickness.

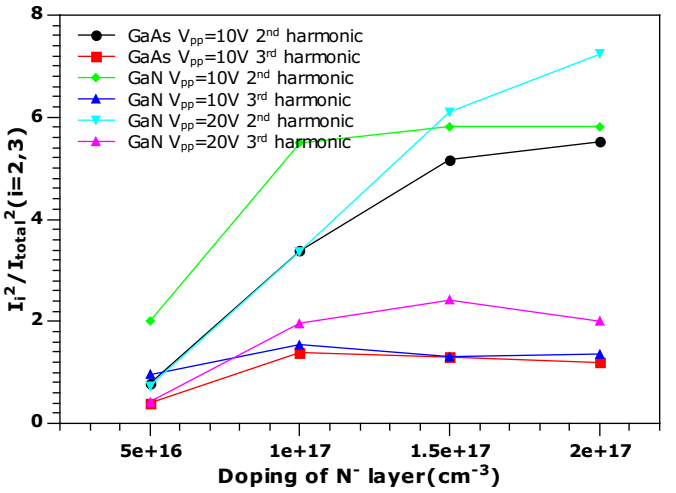
The dependence of nonlinearity on N^- layer thickness was found to be weak, except for the 2^{nd} harmonics generated by GaN diodes driven by a 20 V V_{pp} stimulus and GaAs diodes driven by a 10 V V_{pp} stimulus. This was explained by the smaller C_{min} arising from thicker N^- layer, which was present at the highest peak of negative voltage swing of each stimulus cycle.

The temperature dependence of power performance is shown in Fig.2.25(a). Due to mobility drop at higher temperature, the loss becomes higher. The P_{abs} was found to increase while the P_{rac} decreased. This implied that the increased part of the P_{abs} has been consumed by loss, instead of storage in P_{rac}.

It is worth noting that the simulation was performed under isothermal condition. The elevated temperature was set within a range of values permitting to estimate the general trends of device characteristics replicating self-heating but not determined by such an

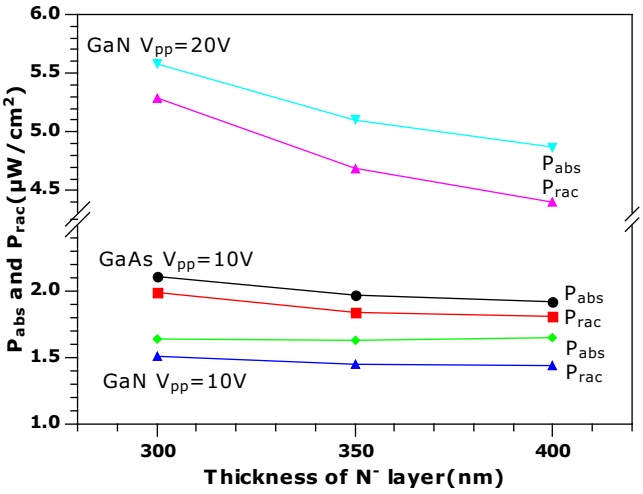


(a) absorbed power P_{abs} and reactive power P_{rac} in one sinusoid stimulus cycle

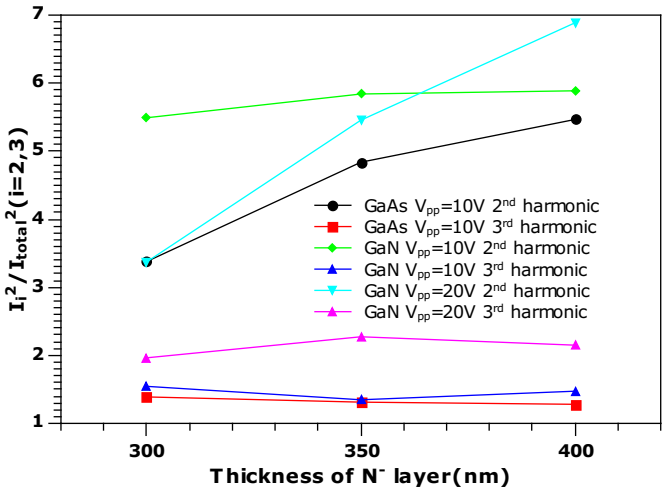


(b) power of 2^{nd} and 3^{rd} harmonics, relative to sum of all harmonics power

Figure 2.23: Power and nonlinear performance of 300 nm thick N^- layer with various doping concentration.

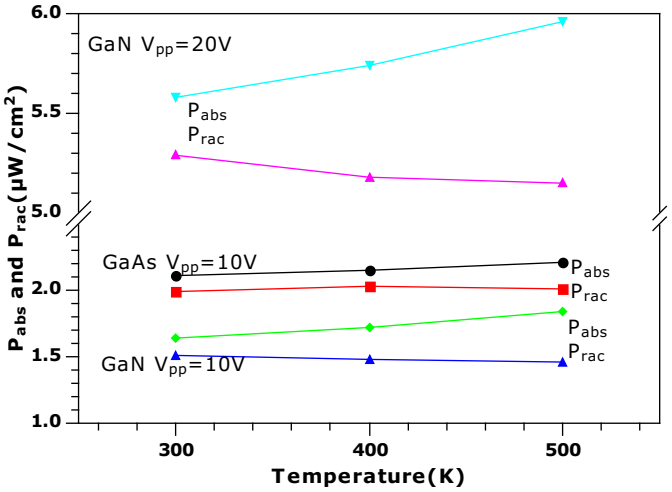


(a) absorbed power P_{abs} and reactive power P_{rac} in one sinusoid stimulus cycle

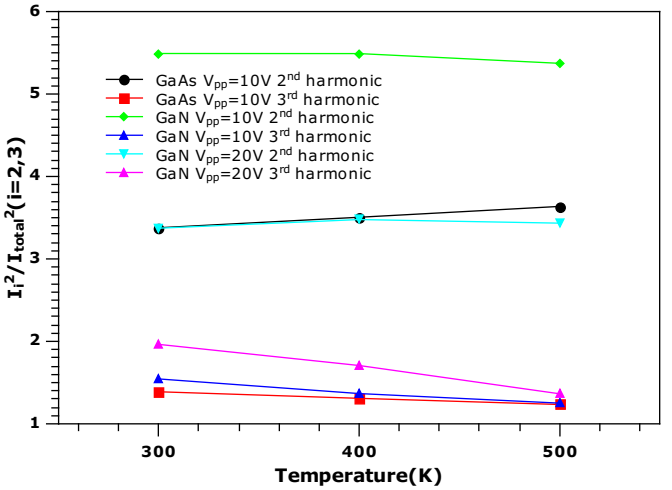


(b) power of 2^{nd} and 3^{rd} harmonics, relative to sum of all harmonics power

Figure 2.24: Power and nonlinear performance of 1×10^{17} cm^{-3} doped N^{-} layer with thickness varying from 300 nm to 400 nm

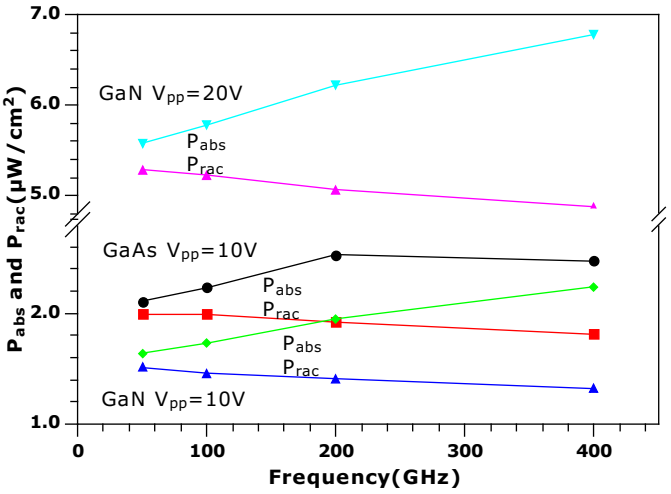


(a) absorbed power P_{abs} and reactive power P_{rac} in one sinusoid stimulus cycle

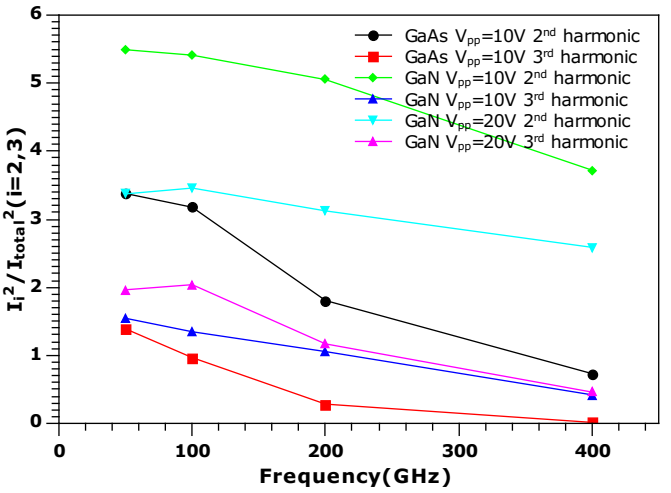


(b) power of 2^{nd} and 3^{rd} harmonics, relative to sum of all harmonics power

Figure 2.25: Power and nonlinear performance of 1×10^{17} cm^{-3} doped 300 nm thick N^{-} layer, with temperature from 300 K to 500 K



(a) Absorbed power P_{abs} and reactive power P_{rac} in one sinusoid stimulus cycle



(b) power of 2^{nd} and 3^{rd} harmonics, relative to sum of all harmonics power

Figure 2.26: Power and nonlinear performance of 1×10^{17} cm^{-3} doped 300 nm thick N^{-} layer, with operation frequency from 50 GHz to 400 GHz

effect. Considering the fact that the thermal conductivity of GaN is at least 4 times higher than GaAs, one expects that for the same dissipated power, GaN didoes will have a lower junction temperature than their GaAs equivalent. A full thermal-electrical simulation would be helpful for revealing the junction temperature of GaN diodes subjected to large-signal operation and thus high power dissipation conditions.

Overall, GaN materials have been demonstrated to be excellent candidates for high power high temperature applications. This study indicates that performance variation has to be taken into consideration in designing such a diode. The temperature had less impact on nonlinearity, as shown in Fig.2.25(b).

Current saturation has been reported to limit GaAs diodes performance under high power and high frequency operation[24]. As shown in Fig.2.26(a), P_{abs} was found to be increased with higher operation frequency for GaN diodes. But in GaAs case, the P_{abs} was slightly reduced from 200 GHz to 400 GHz. As a result of increased loss at higher frequency, P_{rac} became smaller. It's also worth noting that in Fig.2.26(b), the harmonic power ratio dropped much faster with increased operation frequency for GaAs than GaN. This indicates the potential of using GaN Schottky diodes for higher frequency, despite the lower mobility of this material.

Based on all the results shown above, it was concluded that,
1. The power handling capability of GaN Schottky diodes is 2-3 times higher than that of GaAs diodes, when the input stimulus voltage is doubled.
2. The increase of loss is compensated by increased absorbed power.
3. GaN diodes are more nonlinear than GaAs diodes, and this nonlinearity provides them an advantage for higher power stimulus.
4. The nonlinearity of GaN diodes drops less than in GaAs diodes under high frequency operation.
5. Thanks to the higher input power that can be applied , GaN Schottky diodes are expected to be robust and working at higher operation temperature. Designers need also to pay attention to the power variation with operation temperature.

2.4 Conclusion

In this chapter, the key analysis methodologies used for exploring the power handling capability, losses and nonlinearity have been described in detail. An analytical approach based on ideal Schottky diode C-V and I-V characteristics allowed performance correlation such as power handling capability, losses and nonlinearity to the diode parameters (C_0, V_{bias}, R_s etc.) in an efficient way. The numerical simulation based on TCAD tools, on the other hand, allowed accurate verification of the performance for a specific design, and also provides physical insights of the diode operation. These two approaches together compose an effective way for understanding the operation principles of Schottky diodes and further analysing their performance.

The results of the analysis demonstrate, the superior power handling capability of GaN Schottky diodes. The potential of GaN Schottky diodes in high frequency has also been shown. This chapter allows better understanding of the characteristics of fabricated devices that will be discussed in the following chapters.

3 Fabrication Process of GaN Schottky Diodes

This chapter discusses the various processing steps necessary for GaN-based diodes. Schottky varactor diodes are a key component for frequency multiplication, due to their nonlinear properties which are necessary for harmonic signal generation. Diode multipliers evolved from whisker contacted single diode designs to planar structures. Modern multipliers employ even MMIC-like chips, which operate not only using diodes alone but have also integrated passive components.

The material properties of GaN make the fabrication technology to be different from GaAs-based technology. For example, GaAs is easily etched by wet solutions, permitting flexibility in fabrication. Trench isolation can in this way be done after interconnection metallization, allowing beam-lead realization [43]. Devices can also be made using Titanium as Schottky contact offering the possibility of combining Schottky and pillar metallization in the same step.

The work described in this chapter discusses the various steps involved in GaN diode fabrication as needed for on-wafer characterization and eventual use in signal generation and control circuits. The developed technology allows device fabrication together with its access pads and air-bridge, facilitating diode measurement. Both optical and E-beam lithography technology were used in the study, and the details of the processes involved are also provided in this chapter.

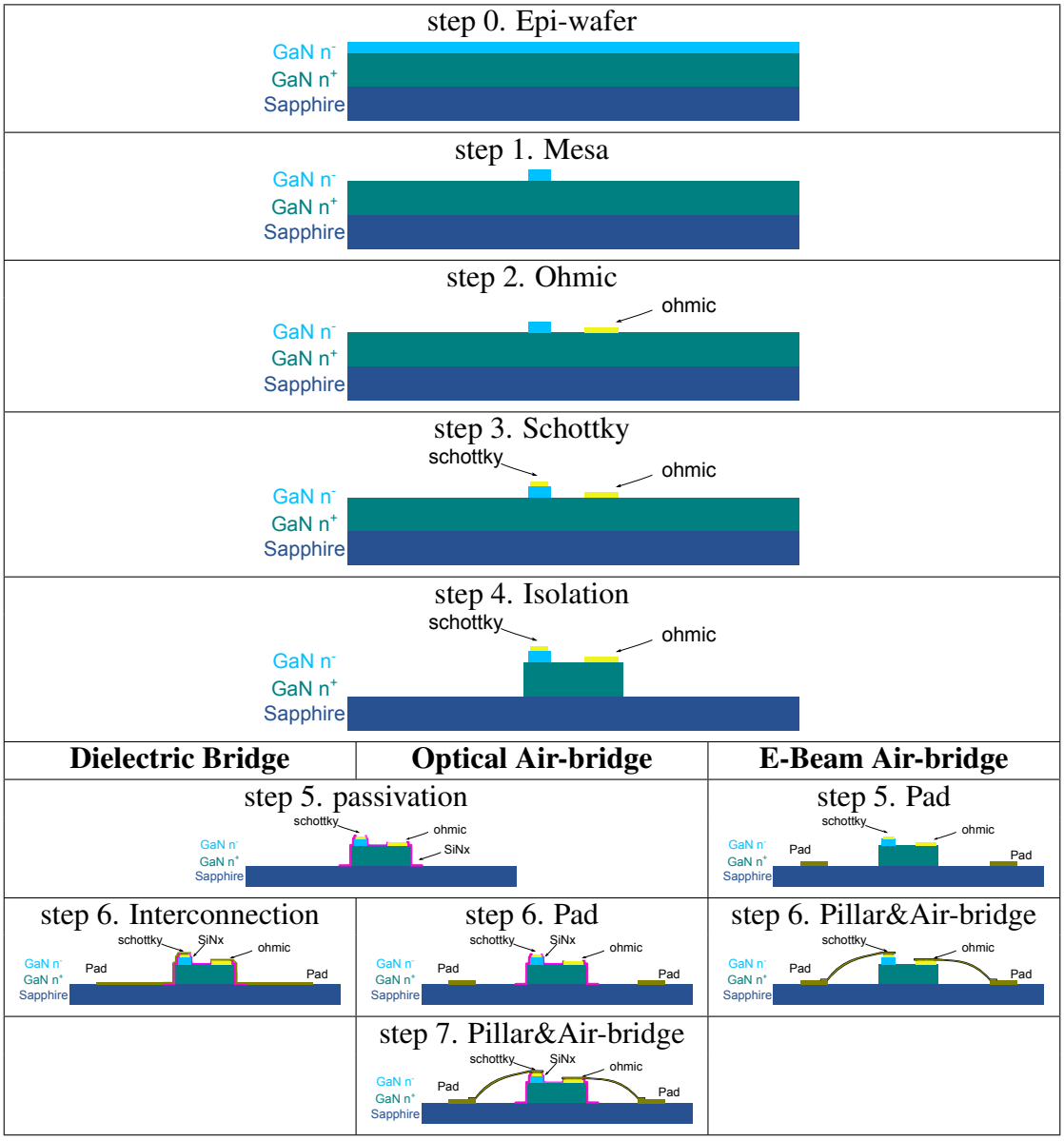
3.1 Prospect of Fabrication Process

The steps necessary for fabricating GaN Schottky diodes are listed in Table.3.1, which also includes a comparison of various fabrication technologies adopted for contacting the diode anodes. A general description of the technologies used is provided first, followed by a detailed discussion on each step.

The materials used for the study were grown by an in-house MOCVD facility. The GaN epitaxial structure used for Schottky diodes in this study employs GaN layers with two different doping concentrations. A N^+ layer was grown first on Sapphire substrate and served as cathode contact of the Schottky diodes. A doping concentration between 3×10^{18} and 5×10^{18} cm^{-3} was used in order to obtain ohmic contacts with minimum resistance. The thickness of the N^+ layer was 2 $\mu\mathrm{m}$. The N^- layer grown on top of the N^+ layer acts as the active layer. The Schottky metal is deposited on this layer at a later step to form a Schottky contact. The nonlinear properties of the device depend both on the N^- GaN layer and Metal-Semiconductor interface established on it. The overview

of GaAs based Schottky diodes in Chapter 1 showed that diodes used for frequency multiplication have often a doping concentration as low as $10^{16}\mathrm{cm}^{-3}$ in order to obtain higher barrier height and lower leakage current as necessary for higher power handling capability. A doping concentration of this value is in the limit of what can be achieved by MOCVD growth of GaN, and can not be easily controlled, leading often to resistive material. It was therefore decided to have the N^- layer grown for this study at a doping concentration of $1 \times 10^{17}\mathrm{cm}^{-3}$.

Table 3.1: Process flow of the three technologies used in this study



Considering the two-layer (N^+ and N^-) epitaxial structure, the cross section of the processed diode can be represented as shown in step 4 of Table.3.1. To obtain a device of this type, the following fabrication steps are necessary.

1.Mesa etching: to remove the N^- layer outside the active area of the diode, and allow the formation of Ohmic contacts on the N^+ layer.
2.Ohmic contact metallization to obtain Ohmic contacts on the N^+ layer.
3.Schottky contact metallization: for establishing Schottky contacts on the N^- layer.
4.Isolation: to completely remove the GaN layer down to Sapphire substrate and ensure isolation of a diode from those adjacent to it.

After Schottky contact formation, the characteristics of the diodes were measured in order to determine their performance. The small anode size of the fabricated devices posed a difficulty in performing such measurements. Additional process steps were therefore introduced to permit the connection of the small size anodes and cathodes to a larger size contact pad. Moreover, co-planar waveguide transmission lines allowed on-wafer high-frequency characterization.

The three process technology approaches explored in this study prevent the aforementioned difficulties by employing additional process steps as shown in Table.3.1. The first approach, is referred to as dielectric bridge technology, and was developed for rapid evaluation of the diode characteristics. The use of a dielectric layer, allowed simultaneous realization of the inter-connect metal and a larger size outer pad in a single evaporation step followed by lift-off. It involves the minimum number of steps compared with the other two technologies that were based on air-bridges, and therefore the overall fabrication time associated with it was minimized. This approach was useful for rapid testing of wafer or Schottky contact quality, where DC characterization is adequate for this purpose and no high-frequency characterization is required.

The second and third technology approaches aimed at the realization of air-bridges, which are important for high-frequency evaluation due to the presence of smaller parasitics from the metal lines which are in this case separated from other interconnections by air. These two approaches differ from each other by the lithography process, which is in one case based on optical and in the other on E-beam technology. The alignment accuracy of optical lithography makes it uncertain for aligning the pillars with respect to the anode; if the pillar is shifted the device may end up with a larger anode size or lower barrier height. Note that the metal of the bridge footprint is normally Titanium for adhesion purposes. Thus a passivation step is employed in optical air-bridge technology, to prevent that the bridge metal contacts the N^- semiconductor layer; here the opening of the passivation layer has a smaller diameter size than the Schottky metal contact. For E-beam air-bridge technology, the alignment accuracy is assured, thus no passivation step is needed. Another difference between the two developed air-bridge technologies is the method of bridge metal formation: Optical lithography-based approaches use often electroplating while evaporation and lift-off are usually employed for E-beam technology.

As described in this section, all the technologies considered employ three basic steps, namely etching, metallization and bridge formation. Etching is used for mesa and isolation. Metallization includes the Ohmic and Schottky contact. The steps necessary for bridge formation will also be discussed in this section. The pad step is considered as an

integral part of the bridge, since it depends critically on resist profile for lift-off rather than metal stack formation.

3.2 Etching

Most of the semiconductor materials can be etched by chemical solutions. This process step is normally referred to as wet etching since the semiconductor material is dissolved by chemicals in an aqueous environment. However, wet etchants for III-Nitride materials are limited. Under normal conditions, only molten salts like KOH or NaOH at elevated temperature are capable to etch GaN at reasonably high rates [44] . Moreover, etching of this type requires an appropriate etching mask, which in most cases is not photoresist. Thus the application of wet etching in III-Nitride device processing is limited and dry etching has been developed.

Dry etching of III-Nitrides normally employs a plasma generated in a vacuum chamber coupled to an RF signal. The removal of III-Nitrides is accomplished by either physical sputtering, chemical reaction or combination of both. Physical sputtering relies on momentum transfer from the accelerated ions formed in the plasma to the substrate surface, where the substrate material is removed. The energy of the ions has to be higher than a threshold value, below which the ions will be absorbed at the substrate surface leading therefore only to damage at a depth of a few atomic layers. Under such condition, this method will result in a rough surface morphology, surface damage and poor selectivity. The typical gas used for physical etching of GaN is Argon. The achieved etching rate depends on the plasma density and energy of accelerated Ar^+ ions.

In contrary to the above, the mechanism of chemical reaction etching relies on the chemical reaction of the surface material with reactive ions formed in the plasma. Products from the chemical reaction have to be volatile and an etched surface is produced following the formation of volatile products. Chemical reaction provides normally a good morphology due to the low energy of the reactive ions. However, low energy of ions implies that omnidirectional and lateral etching can not be avoided. Practical etching recipes for III-Nitrides, however, don't follow the ideal description above. A conventionally used gas is Chlorine-based, like Cl_2 or BCl_3. Ion bombardment has found to be the dominant mechanism due to the high bond energy of III-Nitrides. Thus the energy of ionized Cl^- has to be high enough to act properly.

The combination of both physical sputtering and chemical reaction is expected to lead in faster etching rate as well as anisotropic profile. A key part in this technology is the definition of an optimized condition where the physical and chemical process are balanced. This has been the dominant etching technique as will be discussed below.

The realization of all the approaches described above relies on the generation of a plasma. Considering the various approaches necessary for plasma generation, one can define

three types of instrumentation. These are Reactive Ion Etching (RIE), Inductively Coupled Plasma (ICP) and Electron Cyclotron Resonance (ECR). Fig.3-1 gives the schematic of both RIE and ICP, the working principle of which will be discussed below. ECR will not be discussed since it was not used in this work.

Fig.3.1(a) shows a parallel plate RIE system. The two plates are placed in the top and bottom of a vacuum chamber. Wafers are normally placed on the bottom plate while the top one is electrically shorted to ground. By applying a RF voltage between the two plates, an electromagnetic field is generated and thus the gas molecules are ionized into electrons and positive ions. A large region of the gas-filled space between the plates will come to equilibrium. This equilibrium region is called glow region, due to the fact that a glowing light is seen when energy release of the gas molecules takes place from the excited state to the normal state. A potential difference between the glow region and the wafer plate will accelerate ions near boarder of glow region toward the wafer plate. The ions colliding on the wafer surface lead in etching by either sputtering or reaction. Given the working principle described above, the energy and density of ions are both proportional to RF voltage. Higher ion density is desired for faster etching rate. However, the ion energy is correspondingly increased, introducing more defects on the surface and degrading the morphology.

Fig.3.1(b) presents a schematic of ICP system. By employing an individual source for plasma generation, ICP provides an ion density 2 to 4 orders [44] higher than RIE while maintaining low ion energy . Thus a faster etching rate can be obtained from ICP without increasing the surface roughness.

The instruments used in this study are an Oxford plasmalab 80 RIE and an Oxford plasmalab 100 ICP platform. The RIE was used for Ar physical sputtering only, with an etching rate of 20 nm/min. The choice of these conditions was to some extent made based on the system's specifications. Similar conditions were successfully applied to GaN HEMTs and AlN MISFETs[46]. However, unlike the HEMT structure where an active layer of 300-400 nm is normally used, the epitaxial structure of Schottky diodes has a much thicker N^+ layer for minimizing the series resistance. As a result, the etching time needs to be considerably prolonged . Although a nickel layer is normally used as a hard mask in literature, a photoresist based etching mask would be attractive due to faster processing. Thanks to the relaxed dimension requirement for mesa definition, a layer of AZ4562 has been considered in this study to resist in Ar plasma for more than one hour.

For ICP etching, a Cl_2/Ar gas mixture was used and resulted in an etching rate of 200 nm/min. This process has been successfully applied to the fabrication of GaN mechanical resonators[47]. Fig.3.2 presents SEM images of etched mesas by Ar sputtering in RIE and Cl_2/Ar mixture in ICP. Good etched profile and surface roughness has been achieved by both of them.

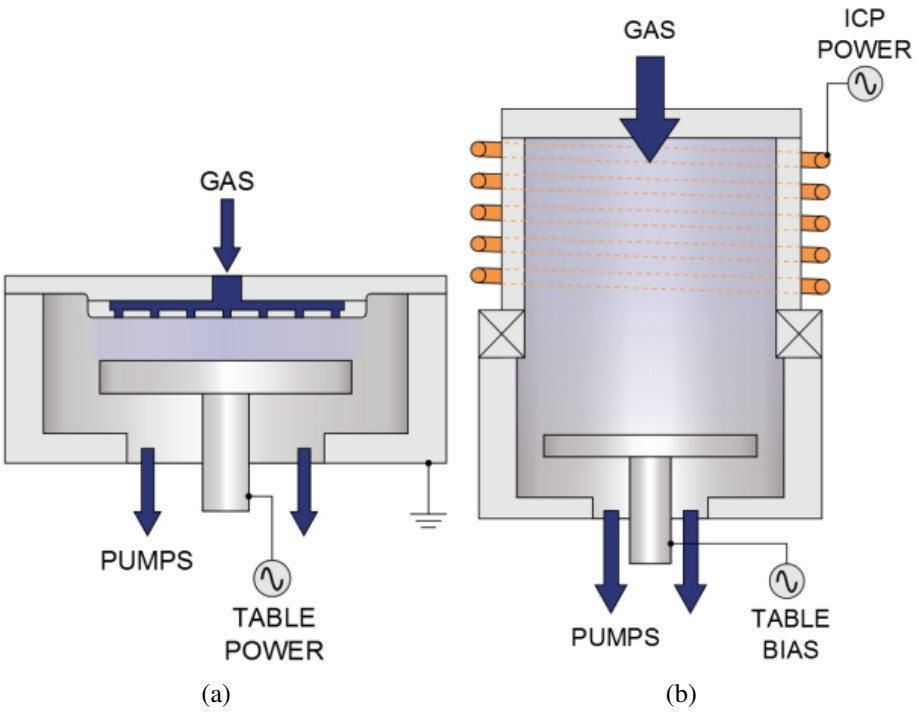


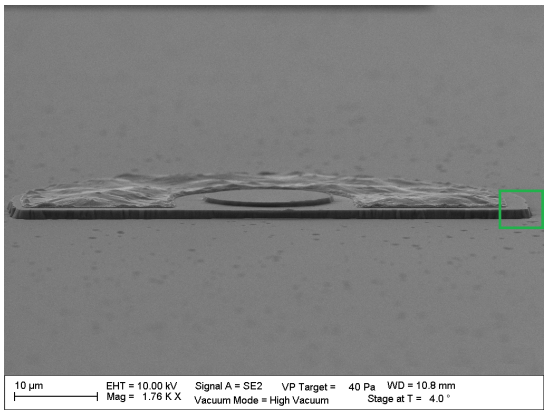
Figure 3.1: Schematic of (a) RIE and (b) ICP [45]

3.3 Metallization

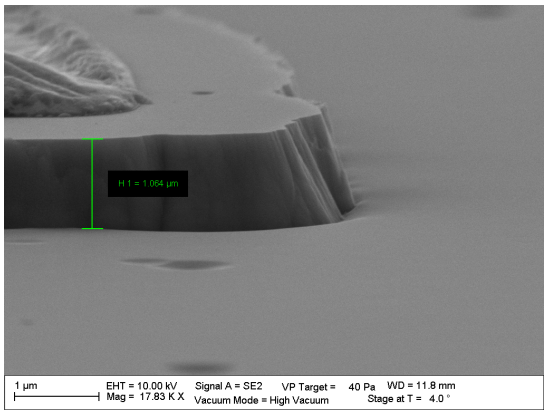
This section presents the process developed for formation of Schottky and Ohmic contacts, which are of major importance for proper device operation. A metal with high work function deposited on top of a N^- layer results in a Schottky contact. Ohmic contacts are required to be formed on N^+ layer. Conventional evaporation and lift-off techniques are used for both optical and E-beam technology. The metal schemes for Ohmic contact on GaN will be discussed here and the specific resistance obtained in this way will be reported.

3.3.1 Ohmic Contacts on GaN

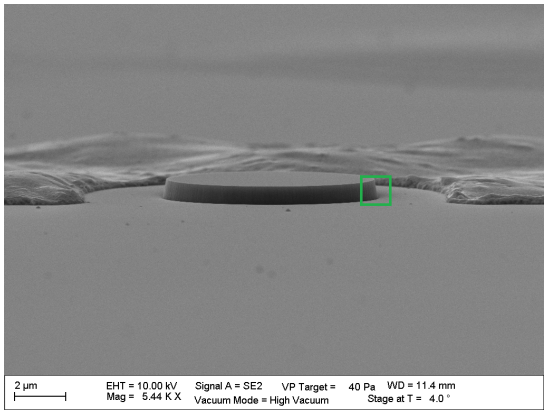
The requirement for good Ohmic contacts is lowest possible specific resistance and thus lower series resistance. For III-Nitrides, a metal scheme with a four layer Ti/Al/X/Au stacks has often been reported, where X can be Ti, Ni, Pd and Pt. The first Titanium layer is believed to react with nitrogen atoms on the GaN surface. The resulting semiconductor surface tends to be highly doped due to the N-vacancies. A thin barrier is thus formed due to the highly doped layer, which increases the probability for electrons to tunnel through. Contact formation benefits also from the Titanium layer due to its capability of dissolving the native oxide and improving adhesion. Better Ohmic contact quality can



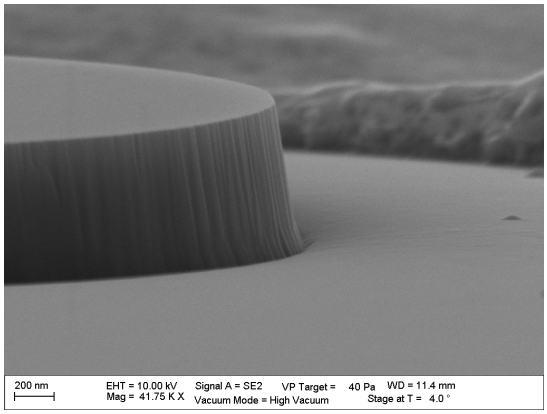
(a) mesa etched by RIE



(b) mesa etched by RIE(zoomed in)



(c) mesa etched by ICP



(d) mesa etched by ICP(zoomed in)

Figure 3.2: SEM images of etched mesa by (a,b) Ar sputtering only in RIE and (c,d) Cl_2/Ar mixture in ICP

be achieved without native oxide, and better mechanical stability is possible by adhesion improvement.

The importance of Aluminium layer has been evidenced by the dependence of its contact resistivity on the ratio of Al over Ti thickness. [48, 49] . The Al layer is believed to prevent the underlaying Ti layer from oxidizing by forming a Al_3Ti layer at elevated temperature. TEM studies of the annealed microstructures[50], showed that micro-voids tend to be formed at the interface when only the Ti layer is present on GaN. The use of a Ti/Al bilayer leads in Al_3Ti formation as predicted by the Ti-Al bulk phase diagram, thus making the Ti-GaN reaction less aggressive.

Both Ti and Al can be oxidized easily, preventing the successful formation of Ohmic contact. It has been shown that the oxygen content in the annealing ambient has a pronounced impact on the resulting contact resistance [49]. A Au layer has often been used to protect them from oxidization. The conductivity of the metal stacks can in this way be increased. However, a blocking metal layer is required in this case to prevent the diffusion of Au to the Al layer as well as, the out-diffusion of Al. This blocking layer is noted above by X, since several metals like Ti, Ni, Pd and Pt maybe used.

The Transfer Length Method (TLM) is normally used to evaluate the quality of Ohmic contact. It provides information on contact resistance (R_c, $\Omega \cdot mm$), specific contact resistance (ρ_c, $\Omega \cdot cm^2$) as well as sheet resistance (R_{sh}, Ω)of the semiconductor film. The resistance between two Ohmic contacts formed on a semiconductor layer with a space d_i can be written as

$$R_{m,i} = \frac{R_{sh} d_i}{W} + 2R_c \tag{3.1}$$

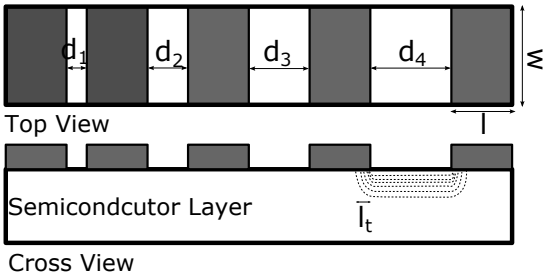
Where the R_c and R_{sh} are correlated through ρ_c

$$R_c = \frac{\sqrt{R_{sh}\rho_c}}{W} coth(\frac{l}{l_t}) \tag{3.2}$$

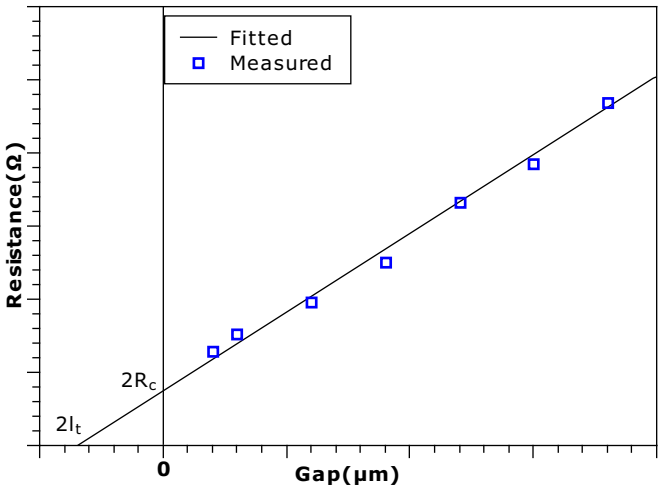
l_t is the transfer length which corresponds to a distance where most of the current transfers from semiconductor layer to metal or vice versa. Since $l \gg l_t$, one obtains $coth(l/l_t) = 1$, and thus l_t is given by

$$l_t = \sqrt{\frac{\rho_c}{R_{sh}}} \tag{3.3}$$

A series of Ohmic contacts with varying spacings, as shown in Fig.3.3(a) forms a set of resistances with different d_i. A large number of d_i dots is normally required for minimizing the measurement uncertainty. By fitting the obtained data points using the least square method, the resulted line represents the dependence of resistance between two Ohmic contacts on their spacing. The slope of this line is R_{sh}/W, the intercept on R-axis is $2R_c$ and the intercept on d-axis is $2l_t$.



(a)



(b)

Figure 3.3: Schematic of TLM pattern structure (a); Interpretation of TLM results (b)

A Ti (25 nm) / Al (150 nm)/ Ti (25 nm)/ Au (150 nm) stack for optical process and Ti (12 nm) / Al (200 nm) / Ni (40 nm) / Au (100 nm) for E-beam process were employed in this study. The same Rapid Thermal Annealing (RTA) condition was applied to both metal stacks. This was 850 °C annealing in N_2 ambient for 30 seconds. Typical Ohmic contact results achieved in this study are shown in Fig.3.4, and correspond to a R_c of $10^{-1}\ \Omega \cdot mm$, and ρ_c about $3 \times 10^{-6} \Omega \cdot cm^2$. These results are consistent with literature data. Lower resistance can be obtained by further optimization.

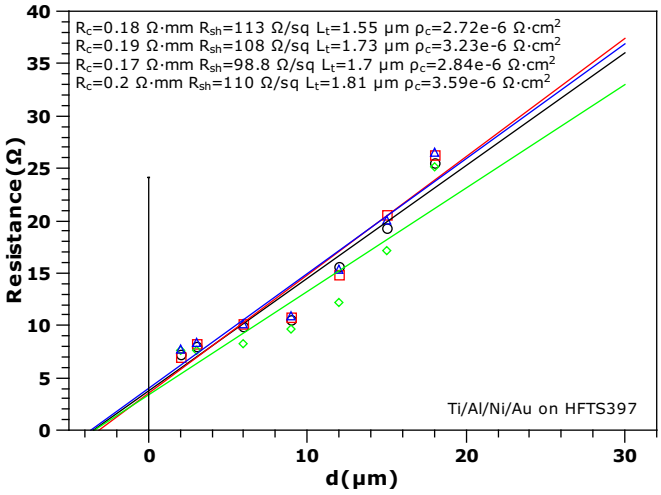


Figure 3.4: Typical Ohmic contact results

This line TLM pattern requires mesa etching to obtain a well defined current flow path. The circular TLM pattern shown in Fig.3.5 has the advantage of limiting the current in a ring between the inner and outer metal contacts, saving therefore the need for mesa etching. This technique is useful, especially for homoexpitaxial GaN substrates, since the N^+ layer is too thick for making a mesa. By analogy to the discussion presented

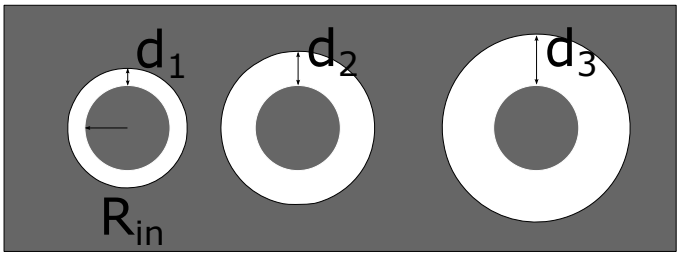


Figure 3.5: Schematic of circular TLM

above, the resistance between two Ohmic contacts of circular TLM patterns depends on space d_i as follows

$$R_{m,i} = \frac{R_{sh} 2\pi R_{in}}{(d_i + 2l_t)} C \tag{3.4}$$

where C is a correction factor of the circular geometry,and is given by

$$C = \frac{R_{in}}{d_i} ln(1 + \frac{d_i}{R_{in}}) \tag{3.5}$$

With this correction factor, a fitted line from measured $R_{m,i}(d_i)$ provides the same information as in Fig.3.3(b), i.e. the intercept on R-axis is 2R$_c$ and the intercept on d-axis is $2l_t$, except that the slope should in this case be R$_{sh}/2\pi R_{in}$.

Fig.3.6 shows results obtained from circular TLM patterns. The calculated ρ_c of one pattern is as low as $4.77 \times 10^{-7} \Omega \cdot cm^2$. The fitted lines from the other two patterns do not deviate considerably but result in ρ_c values five times higher. This discrepancy indicates that the circular TLM method is sensitive to needle contact resistance. R$_{in} \gg d_i$ has to be satisfied to assure the linear dependence of resistance on gap distance. This requires larger area of Ohmic contacts so that the resistance between two adjacent contacts can be much smaller. By way of an example the measured resistance shown in Fig.3.6 is a few Ohms. The needle contact resistance can thus impact the results markedly. One considers in practice the lowest value from several repeated measurements.

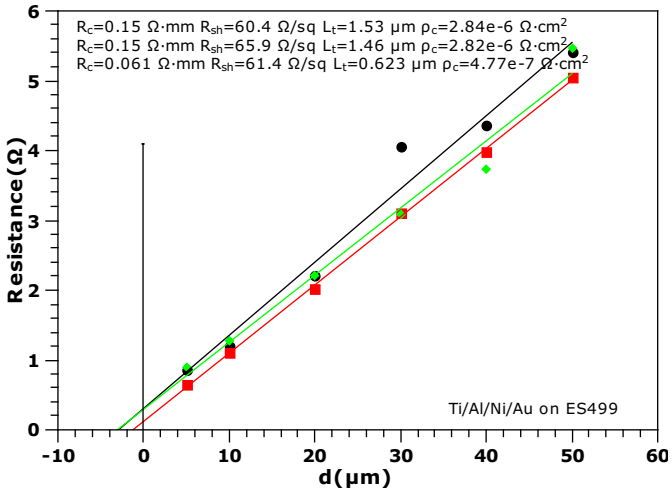


Figure 3.6: Results of circular TLM

3.3.2 Schottky Contacts on GaN

Schottky contacts are the most critical part for the diodes discussed here. From the Metal-Semiconductor contact theory introduced in the last chapter, we know that the metal has to have a high work function to form a Schottky contact on GaN. The conventionally used metals for GaN Schottky contacts include Ni (W_m=5.15 eV), Pt (W_m=5.65 eV), Pd(W_m=5.12 eV) and Au(W_m=5.1 eV). Pt was chosen in this study due to the possibility of forming a high barrier. a comparative study was also made with Ni Schottky contact.

The process flow of Schottky contact metallization is straightforward. One defines first the opening area by lithography, and then deposits the metallization. As clean GaN surface is the key to good Metal-Semiconductor contact every effort has to be made to guarantee it.

The development following resist exposure may not be sufficient to dissolve all the resist. A thin residual resist film remains very often on the semiconductor surface. This residual resist film behaves as insulator, forming a Metal-Insulator-Semiconductor contact instead of the desired Metal-Semiconductor contact. The resulting devices have in this case bad uniformity and are unstable. Oxygen plasma treatment can remove this residual resist film [51] and is often used for semiconductor and quartz mask cleaning. The plasma on the other hand may cause surface defects and its power needs therefore to be optimized to avoid surface defects.

Schottky contact quality relies strongly on surface treatment before metal deposition. Many publications about GaN Schottky contacts report various surface treatment approaches. HF and HCl are the commonly used solutions for removing the surface native oxide [52–54] . The alkaline counterpart for this purpose is NH_4OH [51, 55]. Aqua regia (HNO_3:HCl=1:3)[56] and $(NH_4)_2S_x$ [57] were also suggested in literature. Besides, Fluoride based plasma treatment has also been implemented [58]. The study performed in this thesis showed that HF and HCl lead in clean surface. Right after the treatment, samples were loaded into an E-beam evaporator for metal deposition.

Analysis of Schottky contact characteristics

The quality of Schottky contacts is normally described by the parameters n (ideality factor) and Φ_B (barrier height). Both parameters can be extracted from IV characteristics. Ideal MS contacts obey Thermionic Emission (TE) theory, while in practice the current transport across Schottky contacts involves also other mechanisms like Tunneling. The deviation from pure TE transport is evaluated by n and Eq.2.6 is in such a case modified to Eq.3.6.

$$I = I_s[exp(\frac{V}{nV_T}) - 1] \tag{3.6}$$

where I_s is saturation current under reverse bias and remains the same as Eq.2.7

$$I_s = A_s A^* T^2 exp(-\frac{\Phi_B}{V_T}) \tag{3.7}$$

The "Hypothesis testing" method is applied in practice to analyze the IV curves of Schottky diodes. Assuming TE is the dominant mechanism, a value of n is obtained by fitting the measured IV with this equation. Obviously, n=1 corresponds to pure TE transport, and therefore the obtained n is in practice often larger than 1.

Fitting is performed in log scale. The logarithm of Eq.3.6, for $V \gg V_T$

$$lnI = lnI_s + \frac{V}{nV_T} \tag{3.8}$$

In the lnI-V plot the slope of the fitted curve is therefore $1/nV_T$ and the intersection on lnI axis equals lnI_s, from which n and I_s can be derived. With I_s obtained, Φ_B can also be determined from Eq.3.7.

The fitting procedure above assumes that the applied external voltage drops on the junction only. When the current is large or R_s is large, the voltage drop on the R_s can not be ignored. Based on the fitted n and I_s, the voltage drop on the junction V_J can be derived for a given current. The voltage drop on R_s is calculated from the difference between the applied external voltage and V_J. R_s can also be derived:

$$R_s = \frac{V - nV_T(lnI - lnI_s)}{I} \tag{3.9}$$

Cheung's method is another way of deriving the above parameters. One applies in this method a current sweep in the forward conduction region and then measures the resulting voltage drop over the diode. The relation is given as Eq.3.10.

$$V = R_s A_s J + n\Phi_B + (nV_T) ln(J/A^* T^2) \tag{3.10}$$

where $J = I/A_s$ is the current density.

Differentiating Eq.3.10 with respect to J , we have

$$\frac{d(V)}{d(lnJ)} = R_s A_s J + nV_T \tag{3.11}$$

Thus a plot of $\frac{d(V)}{d(lnJ)}$ versus J will give $R_s A_s$ as the slope and nV_T as the y-axis intercept.

One can at this stage define another equation $H(J)$ from Eq.3.10,

$$V - (nV_T) ln(J/A^* T^2) \equiv H(J) = R_s A_s J + n\Phi_B \tag{3.12}$$

with n being determined, $H(J)$ is a function of only J. A plot of $H(J)$ versus J results in a straight line which has a y-axis intercept equaling $n\Phi_B$. The slope of $H(J)$ versus J provides another R_s value, which can be used to check the consistency with the first derived R_s.

Post annealing of Schottky contacts

It has been reported that Schottky contacts annealed at an appropriate temperature show a barrier height enhancement. A Ni/GaN Schottky contact was found to have a barrier height of 0.86 eV and ideality factor of 1.19 was obtained after 5 min annealing at 600°C in N_2 ambience, compared with the as-deposited 0.69 eV barrier height and ideality factor of 1.47 [59]. This has been attributed to the formation of Gallium Nickel (Ga_4Ni_3)[60]. Barrier height enhancement after annealing was also found on Pt/GaN contacts [61], where 30 min 500°C annealing in N_2 ambience was employed.

Both Ni and Pt Schottky contacts on GaN were tested in this work. The epi-layer was 300 nm thick with a surface doping concentration of $3 \times 10^{17}\mathrm{cm}^{-3}$. The sample was designed to have 16 identical chips; mesa and Ohmic contacts were common for all pattern. Then 8 of them were processed with Ni Schottky contacts while the other 8 with Pt Schottky contacts. Oxygen plasma together with BHF etching was applied to clean the GaN surface before metallization. After Schottky contact formation, the sample was diced into 16 separate chips . Each chip was annealed in N_2 ambience for 5 min but with temperature ranging from 350°C to 500°C. At least 5 diodes were measured on each chip to make sure that the obtained IV curves were representative of the technology under evaluation.

The results obtained are shown in Fig.3.7. The barrier height and ideality factor extracted based on the method introduced previously in this section are shown in Table.3.2 and Table.3.3 respectively. The Ni contacts have in general higher current than Pt contacts in both the forward and reverse region, due to their lower work-function. For both Ni and Pt contacts, an appropriate annealing temperature resulted in the largest measured barrier height and lowest ideality factor, as well as reverse saturation current, which was 450°C for Ni and 500°C for Pt in this study. It's also noted that before annealing at the desired temperature, the barrier height of annealed contacts was lower than that of the as-deposited contacts.

Different ideality factor, barrier height and series resistance were obtained when extracting in different regions such as in the lower bias range (0.1 V - 0.2 V) and the higher (0.5 V- 0.08V) bias range. The larger ideality factor resulting by Cheung's method indicated that the deviation from TE mechanism was severe under higher bias. This deviation resulted therefore in a lower effective barrier height.

As a result of increased barrier height after post-annealing, the reverse leakage current density was considerably decreased. However, the best barrier height obtained (0.625 eV for Ni and 0.68 for Pt) was still far from the values calculated from work-function difference.Consideration of the process employed indicated that surface cleaning before Schottky metallization could potentially cause surface damage.

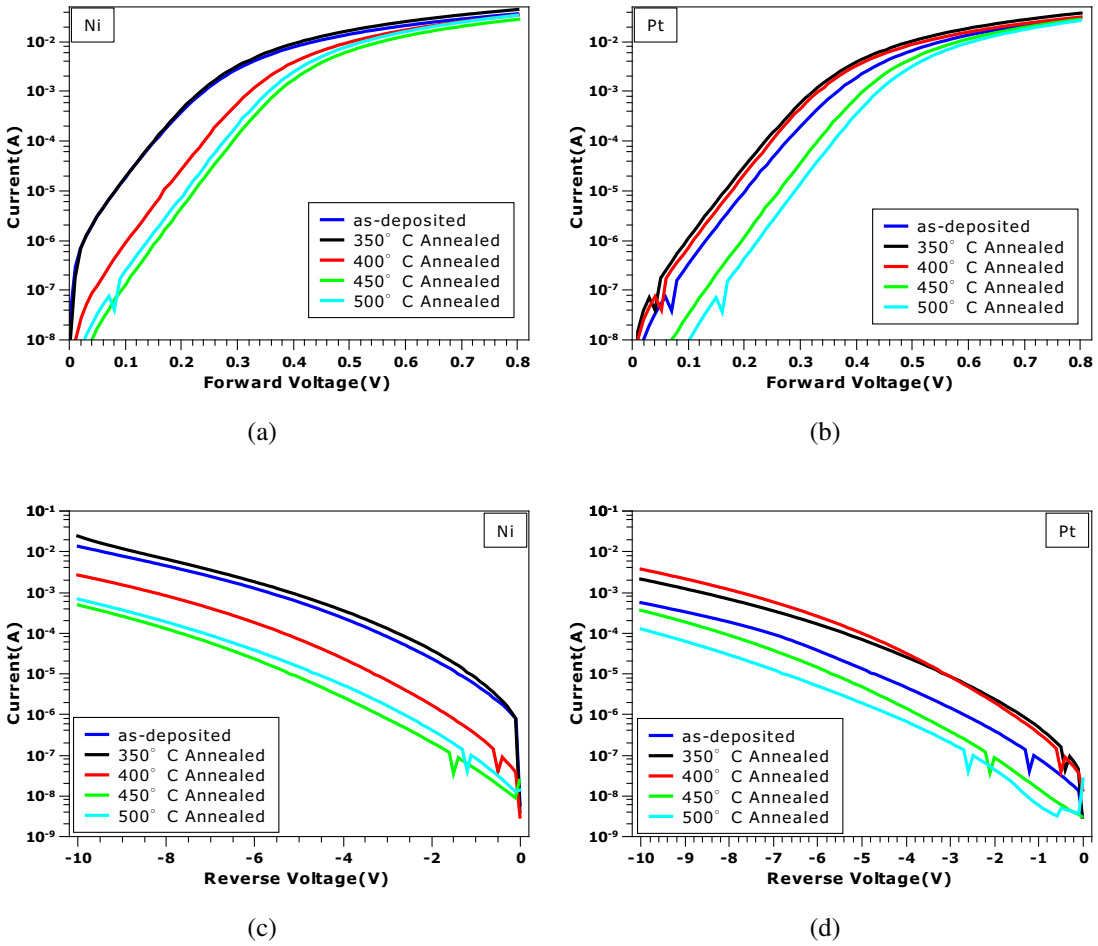


Figure 3.7: IV characteristics of Ni/GaN Schottky contact in forward region (a) and in reverse region (c); Pt/GaN Schottky contacts in forward region (b) and in reverse region (d)

Table 3.2: Results of Ni/GaN contacts after post-annealing at different temperature

	as-deposited	350°C	400°C	450°C	500°C
	Fitting in the range of 0.1 V - 0.2 V				
n	1.258	1.22	1.12	1.087	1.11
Φ_B(eV)	0.484	0.486	0.573	0.625	0.607
I_s(A)	8.8×10^{-7}	8.1×10^{-7}	2.8×10^{-8}	3.7×10^{-9}	7.5×10^{-9}
$R_s^0(\Omega)$	12.52	10.28	11.51	12.63	10.55
	Fitting in the range of 0.5 V - 0.8 V with Cheung's method				
n^1	2.04	2.4	1.82	1.41	1.74
$R_s^1(\Omega)$	11.25	8.69	9.89	11.4	9.14
$R_s^2(\Omega)$	11.28	8.71	9.88	11.38	9.18
Φ_B^1(eV)	0.4	0.376	0.464	0.56	0.492
J@(-10V)(A/cm^2)	200	200	40	10	15

Table 3.3: Results of Pt/GaN contacts after post-annealing at different temperature

	as-deposited	350°C	400°C	450°C	500°C
	Fitting in the range of 0.1 V - 0.2 V				
n	1.15	1.156	1.14	1.08	1.05
Φ_B(eV)	0.596	0.565	0.577	0.66	0.68
I_s(A)	1.2×10^{-8}	3.9×10^{-8}	2.4×10^{-8}	9.2×10^{-10}	4.7×10^{-10}
$R_s^0(\Omega)$	12.05	10.37	12.33	11.26	11.03
	Fitting in the range of 0.5 V - 0.8 V with Cheung's method				
n^1	1.94	1.84	1.95	1.61	1.54
$R_s^1(\Omega)$	9.67	8.79	10.52	9.41	9.2
$R_s^2(\Omega)$	9.75	8.79	10.5	9.48	9.21
Φ_B^1(eV)	0.477	0.465	0.455	0.545	0.566
J@(-10V)(A/cm^2)	20	40	60	8	1.5

Oxygen plasma before Schottky metallization

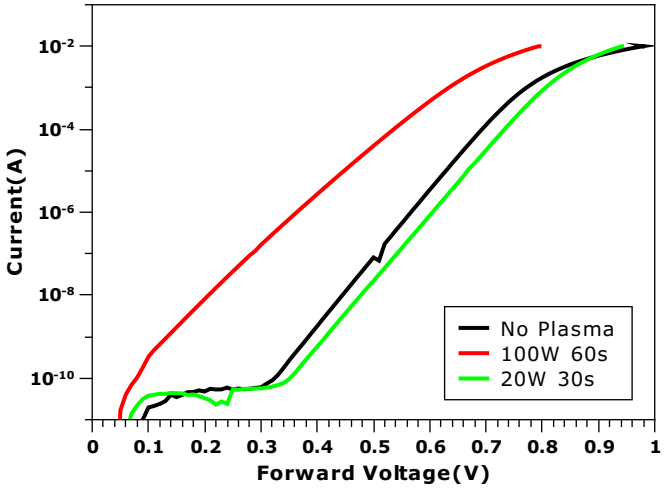
As described earlier, Oxygen plasma treatment is necessary to ensure fabrication of Pt Schottky contacts. Pt is known for its poor adhesion on semiconductors and the presence of a residual resist layer is expected to lead to even worse characteristics . Appropriate processing using oxygen plasma is necessary to be developed for removing the residual resist layer without considerable damage of the semiconductor surface. Simple comparative tests were performed in order to find the appropriate conditions.

The epi-layer used had a nominal doping concentration of $1 \times 10^{17}\mathrm{cm}^{-3}$. The samples were processed in a comparable way, i.e. only the oxygen plasma treatment condition was different for each sample. The equipment used for oxygen plasma treatment was Oxford Plasmalab 80. The pressure and O_2 flow rate were maintained to be 100 mT and 30 sccm respectively. Two different plasma power levels and treatment time conditions were tested. These were 100 W 60 seconds and 20 W 30 seconds. The reference sample had the Schottky metal been lifted off for half of the devices, since no plasma treatment was applied. This can be interpreted as corresponding to a surface that was free from Oxygen plasma damage.

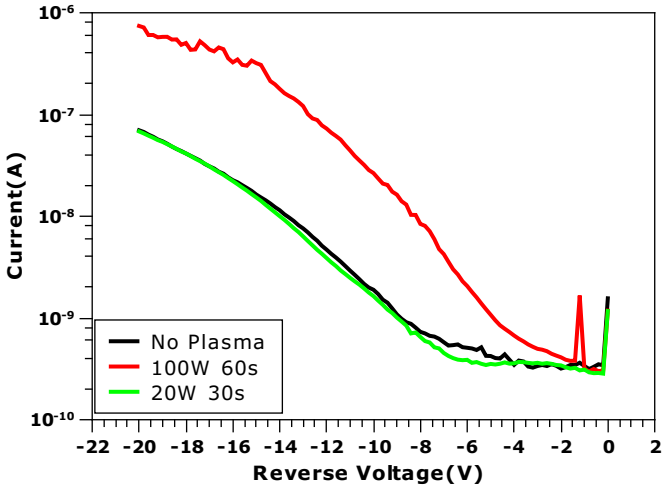
The measured IV characteristics are shown in Fig.3.8. The devices subjected to 100 W 60 seconds O_2 plasma treatment showed higher current in both forward and reverse region, while the 20 W 30 seconds O_2 plasma treated device showed a current similar as the reference sample. This finding suggested that O_2 plasma excited with a power of 100 W was too energetic and could introduce additional defects on the GaN surface before Schottky metallization. A power of 20 W was verified to be appropriate for our application. This is "strong" to remove the residual resist but also "soft" enough to keep GaN surface free from additional damage.

Using the same extraction methods described earlier, the ideality factor and barrier height were evaluated and are shown in Tab.3.4. The barrier height was lower and the ideality factor was larger for the device subjected to 100 W O_2 plasma treatment, reflecting therefore the presence of the non-ideal thermionic emission transport mechanism due to the surface defects. Despite the similar ideality factor and barrier height, the I_s and R_s for the non-plasma treated reference device were 2 time higher than that for 20 W plasma treated device. This may be explained as an effect of random distribution of residual resist on the GaN surface without plasma treatment.

Compared with other samples treated by 100 W O_2 plasma in previous tests, such as the post-annealing test samples, one sees an improved barrier height for the current sample. This is believed to be due to material quality. As shown in the last line of Tab.3.4, a reverse current density as low as $10^{-5}A/cm^2$ under -10 V bias could be achieved. The state of the art low leakage current density also reflected the material quality.



(a)



(b)

Figure 3.8: IV characteristics of Pt/GaN Schottky contact in forward region (a) and in reverse region (b) under different O_2 plasma conditions

Table 3.4: Summary of O_2 plasma tests on Pt/GaN contacts

	No Plasma	100 W 60 seconds	20 W 30 seconds
	Fitting in the lower range		
n	1.03	1.33	1.07
Φ_B(eV)	1.05	0.776	1.07
I_s(A)	5.8×10^{-16}	2.5×10^{-11}	3.3×10^{-16}
$R_s^0(\Omega)$	16.4	11.6	8.27
	Fitting in the higher range with Cheung's method		
n^1	1.09	1.56	1.09
$R_s^1(\Omega)$	15.7	7.55	7.95
$R_s^2(\Omega)$	15.75	7.59	8.04
Φ_B^1(eV)	1.01	0.73	1.05
J@(-10V)(A/cm^2)	1.68×10^{-5}	2.35×10^{-4}	1.45×10^{-5}

With the extracted barrier height, a reverse current was calculated using the equations in [62], which assume tunneling as the dominant transport mechanism. The equation is re-written below as follows:

$$I_r = \frac{A_s A^* T}{k} \int_{-(V_r - V_n)}^{q\Phi_{b0}} exp[-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}\frac{(q\Phi_{b0} - E)^{\frac{3}{2}}}{q\xi} - \frac{E}{kT}]dE \tag{3.13}$$

whereV_r is the reverse bias voltage, V_n the potential difference between Fermi level and conduction band and ξ is the electric field strength.

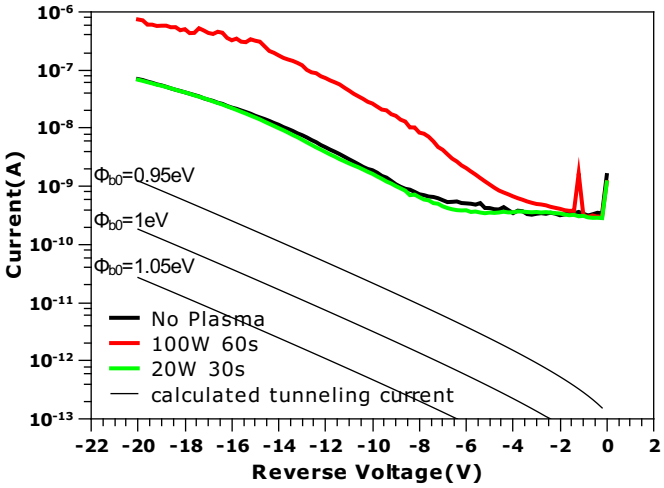


Figure 3.9: Comparison of the measured reverse current with theoretical calculation after tunneling mechanism

The calculated reverse current is shown in Fig.3.9. The dependence of reverse leakage current on the barrier height was examined by artificially altering the barrier height by $\pm$

0.05 eV around 1 eV. As can be seen, the measured leakage current was 2 orders higher than the theoretically obtained results, indicating that other mechanisms dominate the reverse leakage instead of tunneling. A possible explanation is the presence of dislocation related leaky paths [63], which would allow larger leaky current density due to their low barrier height.

3.4 Bridge

As discussed in the beginning of this chapter, bridges are important for characterizing the fabricated devices. The small dimension of the anodes of the explored diodes make their direct measurement not possible. The three different technologies employed at different phases of this research will be discussed in this section.

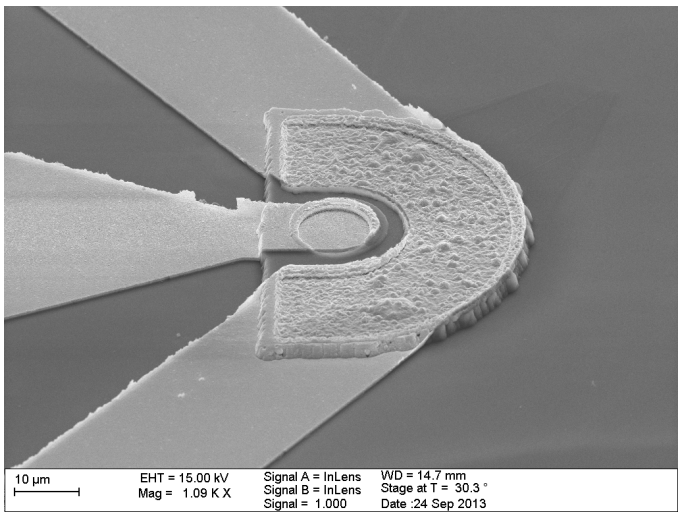
Dielectric Bridge

The successful fabrication of dielectric bridges relies on the rounding off of PECVD deposited dielectric layer to assure the continuity of bridge metal. SiN_x was used as the dielectric layer in this study. The process flow is straightforward: After isolation etching, a SiN_x layer is deposited all over the wafer. The resulting dielectric is rounded off compared with the shape of etched mesa step. One step lithography and SF_6 etching in RIE followed this step to open the Schottky and Ohmic contact metal for accessing it. The bridge metal was realized by conventional lift-off at the last step. The resulted device can be seen in Fig.3.10(a).

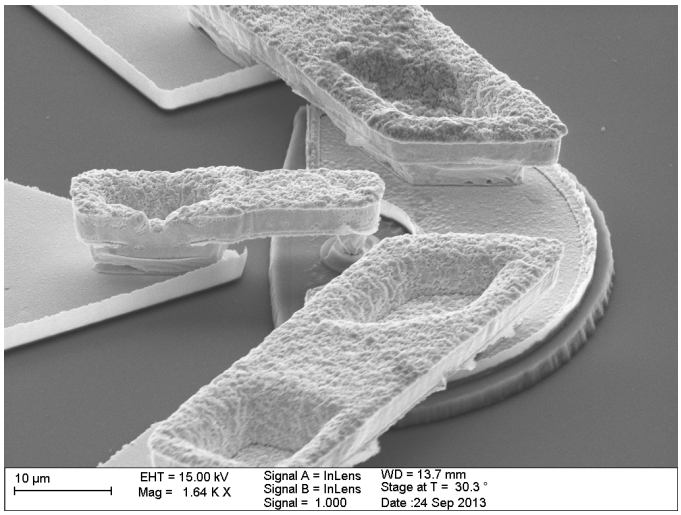
Optical Air-bridge

The optical lithography-based air-bridge process starts with a pad metallization, where a conventional lift-off technique is employed. The subsequent steps correspond to pillar definition and bridge realization. However, alignment accuracy in this process was limited and thus a passivation step was introduced to achieve a reproducible process. The same process as for dielectric bridges was applied but with an additional opening on contact pads.

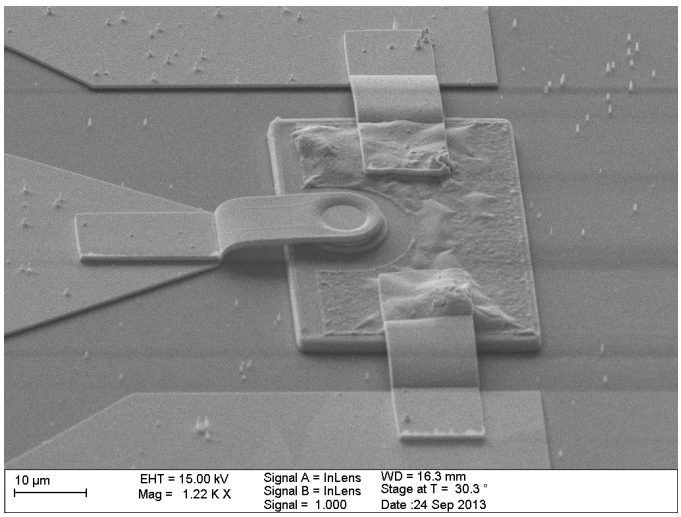
The pillar step followed next. The photoresist used in this step has to be thick enough to offer a planar surface over the nearly 2 μm thick mesa. The areas where the bridge pillar will rest were then defined by lithography. A reflow of this photoresist layer was performed after to achieve a smooth profile. This was important to assure the continuity of the seed layer for electro-plating of the gold bridge. A thin metal layer which acts as plating seed layer was then deposited by either evaporation or sputtering. This metal layer has the additional function of isolating the pillar photoresist from the one used for the bridges.



(a) dielectric bridge



(b) optical air-bridge



(c) E-beam air-bridge

Figure 3.10: Devices realized in this study

The photoresist for bridge definition was then deposited on top of the metal layer. The development of this step did not affect the pillar resist thanks to the metal layer. To perform gold plating, this metal layer has to be exposed at the sample edge to allow current flow. During plating, the current has to be controlled to avoid fast plating, which may short the device anode and cathode. Releasing of the bridges is also of major importance. The top layer photoresist has to be removed by flood exposure and development, rather than remover or solvent. The seed metal layer was removed by metal etchant, which in this study was a gold etchant. The time of etching has to be long enough to assure no metal left, which allows easier removing of pillar photo resist layer. But the etching time has also to be as short as possible to avoid the gold bridge being etched.

E-Beam Air-bridge

The process of E-beam air-bridge is less time consuming compared with optical air-bridge process for two reasons: first, the alignment of lithography is guaranteed and there is no need for passivation; second, the bridge is based on conventional lift-off, which eliminates the plating step as well as the complicated bridge releasing step.

3.5 Conclusion

The technology approaches used in the study were described in detail. Besides the key steps for diode realization, approaches for interconnection were also discussed, including dielectric bridge for rapid testing, air-bridge with optical and E-beam lithography. Optical lithography is low cost, while the E-beam lithography can be further adopted for sub-micron anode realization, meeting the requirements for certain mixer diode applications. Successful technology results good yielding, which ensures the realization of good quality diodes.

4 Small-signal High Frequency Characterization of GaN Schottky Diodes

Equivalent circuit (EC) model is an effective method for analyzing high frequency semiconductor devices, where the electrical behavior of the device is represented by a circuit composed of lumped elements. The parameter values of elements, as well as their dependence on bias and frequency, are linked to the device physically. They are also correlated to the material parameters, device structure, and fabrication processes. This chapter presents the DC and small-signal characteristics of GaN Schottky diodes fabricated in this work, based on extracted equivalent circuit models. The difficulties associated with small-signal equivalent circuit modeling are explained and followed by a detailed discussion of the method used for GaN Schottky diode evaluation. The intrinsic elements, i.e. junction capacitance and junction resistance are also presented for the EC models.

4.1 Current-Voltage Characteristics

The fabricated diodes had diameters between 2.5 to 20 μm, while the epi-structures had a N^- layer thickness of 300 nm and 600 nm. The analysis methods discussed in section 3.3.2 were applied for obtaining information regarding Schottky contacts from DC I-V characteristics. This section focuses on how the extracted data may be used for further modeling. Typical results are shown in Fig.4.1, where a large number of diodes with various diameters have been measured to check their uniformity.

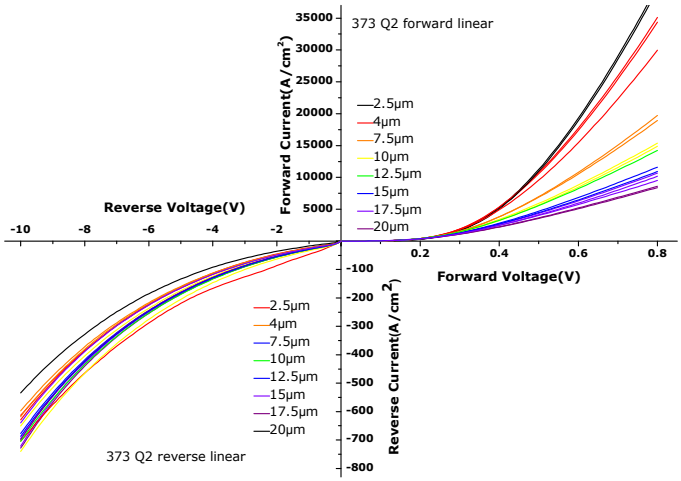


Figure 4.1: I-V characteristics of diodes with various diameter

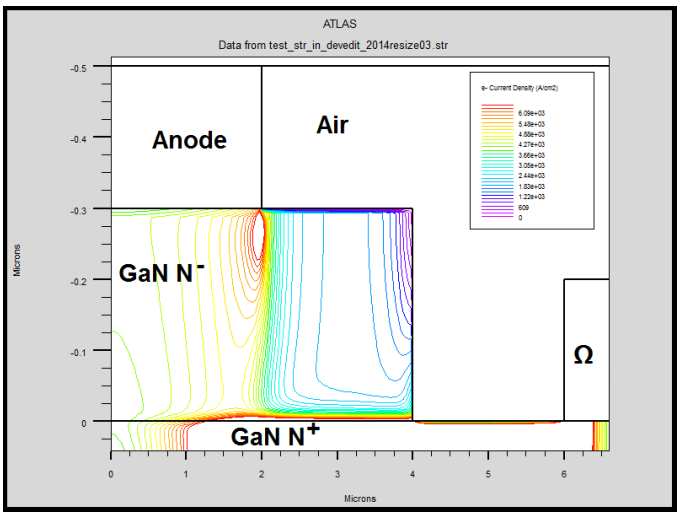


Figure 4.2: Simulated current density contour of a diode

All curves have been normalized to the nominal anode area , so that a comparison can be made based on current density. As can be seen the forward current density depends very much on anode diameter, and diodes with smaller diameter have higher current density. The current density of 2.5 µm devices is about 4.6 times higher than for 20 µm diodes. This indicates that periphery effects have to be taken into account.

In general, electric field lines show crowding at the edge of the Schottky metal which causes the current density at the metal periphery to be higher than in the rest of the contact area. This can be better explained by numerically simulated results as shown in Fig.4.2, where a current density about two times higher was found to exist at the metal edge.

The periphery effect is in principle valid regardless of the bias. The leakage current of a reverse biased diode depends much more on the edge current, given the high tunneling rate resulting from the electric field peak at the anode edge. However, the measured reverse I-V shown in Fig.**??** showed that the dependence on diode diameter was less significant. This indicates that the dominant current transport mechanism under reverse bias is dislocation related other than simply thermionic field emission.

Conventional SPICE diode models have an area factor which accounts for model scaling. The existence of a periphery effect and its bias dependence makes it difficult to obtain a scalable model. In other words, diodes with different diameters need to be modelled independently. The device selected for discussion in this chapter had only 2.5 to 10 µm diameter.

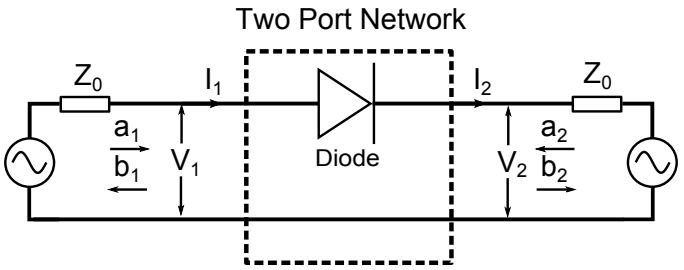


Figure 4.3: Definition of two port S-parameters

4.2 Small-signal High Frequency Characteristics

The high frequency characteristics of the fabricated diodes were obtained with a Vector Network Analyzer (VNA). VNAs are the most common and most important measurement equipment in the high frequency range. The operation principle is based on Scattering parameters (S-parameters). The definition of S-parameters has largely advanced the development of microwaves, as they are easier to measure and to work with than with any other voltage- or current-based parameters.

Fig.4.3 shows the general configuration of a two-port network, where the a/b quantities are defined by

$$\begin{aligned} a_i &= \frac{V_i^+}{\sqrt{Z_0}} = I_i^+ \sqrt{Z_0} \\ b_i &= \frac{V_i^-}{\sqrt{Z_0}} = I_i^- \sqrt{Z_0}, \end{aligned} \tag{4.1}$$

where V_i^+, V_i^- stands for the incident and reflected voltage, I_i^+, I_i^- stands for the incident and reflected current. It can be seen that the a/b quantities are power related. a_i, b_i correlate to the incident and reflected power of port i. S-parameters are defined in a way that allows the evaluation of the power ratio of incident, reflected and transmitted signals as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}. \tag{4.2}$$

The measurement setup used in this work was an Agilent E8361A PNA Network Analyzer, which has a measurement frequency range of 0.01 GHz $\sim$ 67 GHz. The devices could be externally biased by means of computer controlled external voltage sources and bias tees and the VNA could measure in this way the bias dependence of the S-parameters. A conventional Short, Open, Load, and Thru (SOLT) calibration procedure was applied before each measurement.

Given the fact that the diodes are placed in series between the signal ports of the VNA, as indicated in Fig.4.3, it is expected that S_{12}/S_{21} provides information about the diode itself, while S_{11} and S_{22} are affected by the parasitics at port 1 and port 2 respectively.

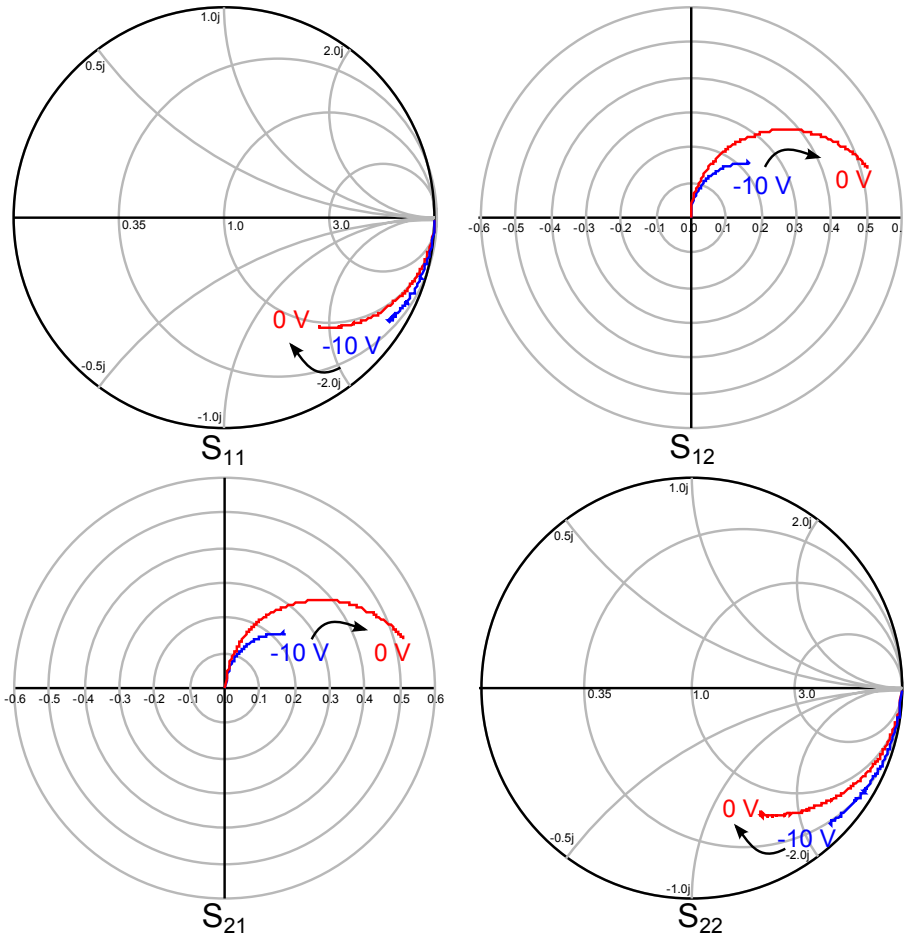


Figure 4.4: S-parameter data for 4 µm diode from 100 MHz to 50 GHz

Typical results are given in Fig.4.4, where a 4 µm diode were measured from 0.1 GHz to 50 GHz. The bias voltage was swept from -10 V to 0 V, but results for intermediate voltages are omitted for clarity.

The difference in curves upon biasing can be explained by the capacitance increase as the bias increases from -10 V to 0 V. Curves under 0 V correspond to better transmission, as well as greater phase delay, related to the diode capacitance at this bias. The measured S_{12} and S_{21} were the same due to the symmetric configuration of the diodes. S_{11} and S_{22} were almost the same due to the presented reactance which is similar for both ports. The slight difference between S_{11} and S_{22} arises by the presence of different parasitic pad capacitances.

Having discussed the measured S-parameters above, it can be seen that to obtain better understanding of the diode properties by as-measured S-parameters is an involved process. Further data treatment and analysis are required to understand the physical significance of the S-parameters. The equivalent circuit modeling, to be discussed in the next section, provides such information.

4.3 Small-signal equivalent circuit modeling

Based on the measured S-parameters, the methodology used for high frequency semiconductor device analysis, consists of deriving their equivalent circuit to represent their port characteristics. The elements of the equivalent circuit correspond to the device under test and should ideally have some physical significance. The GaN Schottky diodes fabricated as described in the last chapter have the cross-section shown in Fig.4.5, which also includes the equivalent circuit of the diode.

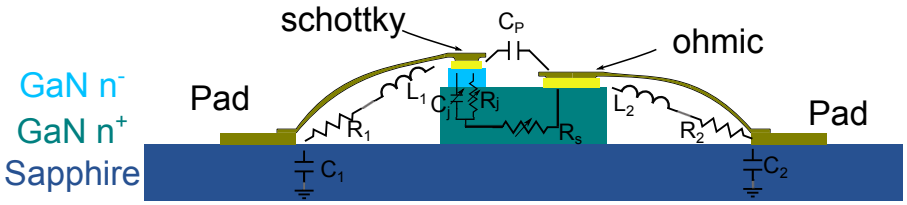


Figure 4.5: Cross-section of GaN Schottky diode and the corresponding equivalent circuit model

L_1/L_2, R_1/R_2, C_1/C_2 correspond to the parasitic inductance, resistance and capacitance respectively related to the anode and cathode pads and interconnects, while C_P is the parasitic capacitance between the anode and cathode. The intrinsic diode characteristics are represented by three bias dependent elements, namely the junction resistance (R_j), junction capacitance (C_j) and series resistance (R_s).

The parameter extraction procedure for FETs has been well established. All the elements can be expressed to be linear functions of port characteristics (S/Y/Z parameters) and can thus be derived by a set of operations of S/Y/Z parameter matrixes [64]. In contrast to FETs, such a straightforward extraction method is still lacking for diodes. This is due to their elements being entangled to each other and therefore not being possible to be expressed individually as a function of port characteristics. Optimization by tuning the elements towards the measured S-parameter values is the most commonly used method. In a recent paper [65], the authors claimed to provide a straightforward analytical method to extract parameters for high frequency diodes. However, fitting was used to derive the junction capacitance (C_j) and a linear regression method was used to derive finger inductance.

The modeling strategy in this study is based on a combination of extraction and fitting to derive the initial values for the elements, followed by optimization and fine tuning of the element values for minimum error. This procedure is described below in detail with example data from one of the characterised diodes.

Step 1. Parasitic elements

On-wafer high frequency measurements generally employ coplanar waveguides (CPW) to access the active region. The effects of the CPW have to be removed to obtain accurate device characteristics. The "removal" of the access CPW is implemented by de-embedding structures, as shown in Fig.4.6. Parasitic elements of the diode equivalent circuit correlate directly to the access section of the CPW, and can therefore be derived from de-embedding structures.

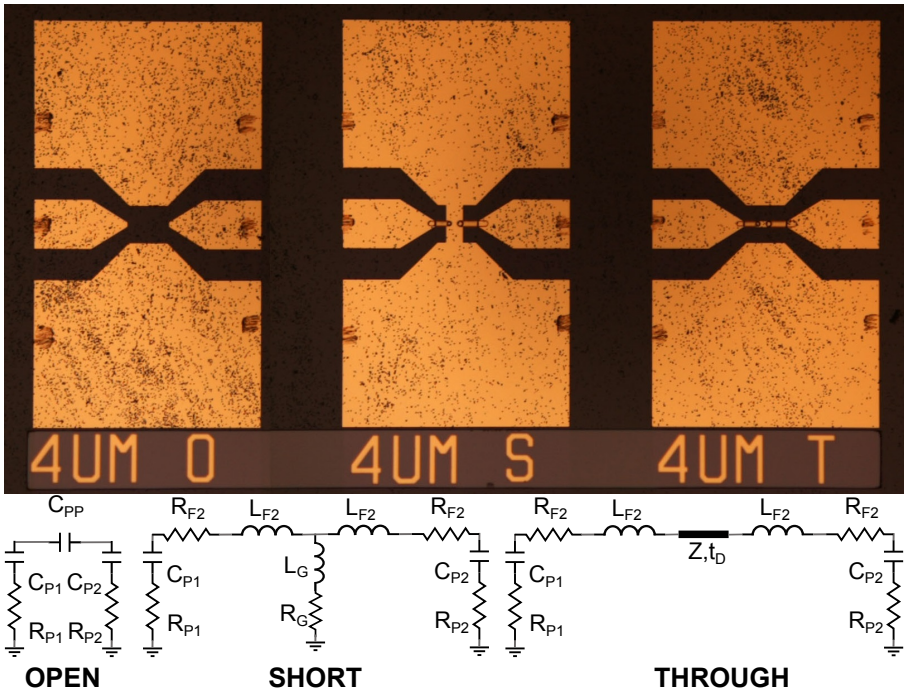


Figure 4.6: De-embedding structures and the corresponding equivalent circuits

The de-embedding structures are ideally designed with the same dimension as the device, in order to avoid any discrepancy. The open, short and through lines shown here were all adapted from the layout of 4 μm diameter diode. Open structures are realized by simply removing from the diode layout all other layers except the pad . Short structures shorted the signal pad to ground through bridge fingers. Through lines are simply lines which are used to verify the de-embedding structure quality.

The validity of the de-embedding process was tested by the through line, the characteristics of which should correspond to a delay line with an impedance Z and delay time t_D after de-embedding. From the Fig.4.7, a physically short transmission line can be seen after de-embedding the open and short. The resulting line was fitted to an impedance of 40 Ω and a delay time of 73 fs.

The equivalent circuit elements can be easily obtained by fitting to measured S-parameters. Values of 10.74 fF and 10.57 fF for C_{P1} and C_{P2} respectively were found to fit well the

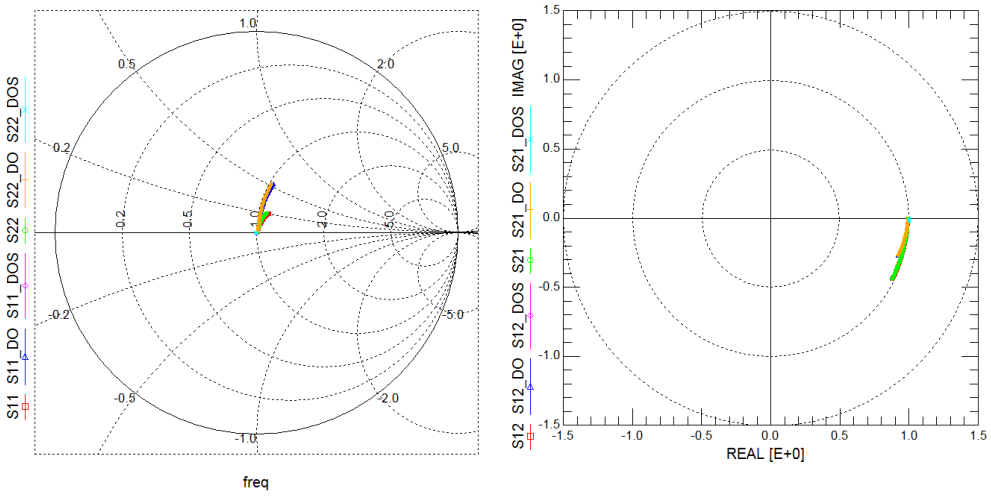


Figure 4.7: S-parameters of the through line without de-embedding, de-embedded with open structure (denoted as DO) and de-embedded with open short (denoted as DOS)

Phase(S_{ii}) of open structures, while 5 Ω for both R_{P1} and a R_{P2} were found to fit the Magnitude. A C_{PP} of 0.75 fF was found to satisfy the Phase(S_{ij}) indicating weak coupling between the two signal pads. Both measurement and fitted data are shown in the figure below.

As far as the pad capacitance is concerned, it's convenient to utilize an extraction rather than optimization method. With the assumption of no pad resistance existing (i.e. R_{P1} and R_{P2} being omitted), the pad capacitance can be simply expressed as

$$C_{Pi} = \frac{Im(Y_{ii} + Y_{ij})}{\omega} \tag{4.3}$$

where i and j denote pad 1 or 2, and ω is the angular frequency.

Using the equivalent circuit fitted here, the validity of the extraction method can be checked by artificially tuning R_{Pi}. The results are shown in Fig.4.9, where only C_{P1} is given for simplicity. While keeping C_{P1} constant at 10.74 fF, the S-parameters of the equivalent circuit were calculated for R_{P1} being artificially set to 5, 25, 50 Ω. The pad capacitance was extracted based on Eq.4.3 and compared with the real value of 10.74 fF. The deviation of the extracted from the real value becomes greater for larger R_{P1} and higher frequency. However, a maximum error of 0.3 fF resulted for R_{P1}=50Ω and a frequency of 50 GHz. This indicates that the directly extracted pad capacitance discussed here is accurate enough.

For short structures, the elements of concern are the finger inductance and resistance, which can be extracted from the Z-parameters after de-embedding from the "open" structure. The corresponding Z-parameters are denoted by the suffix "S-O" in the formulas below:

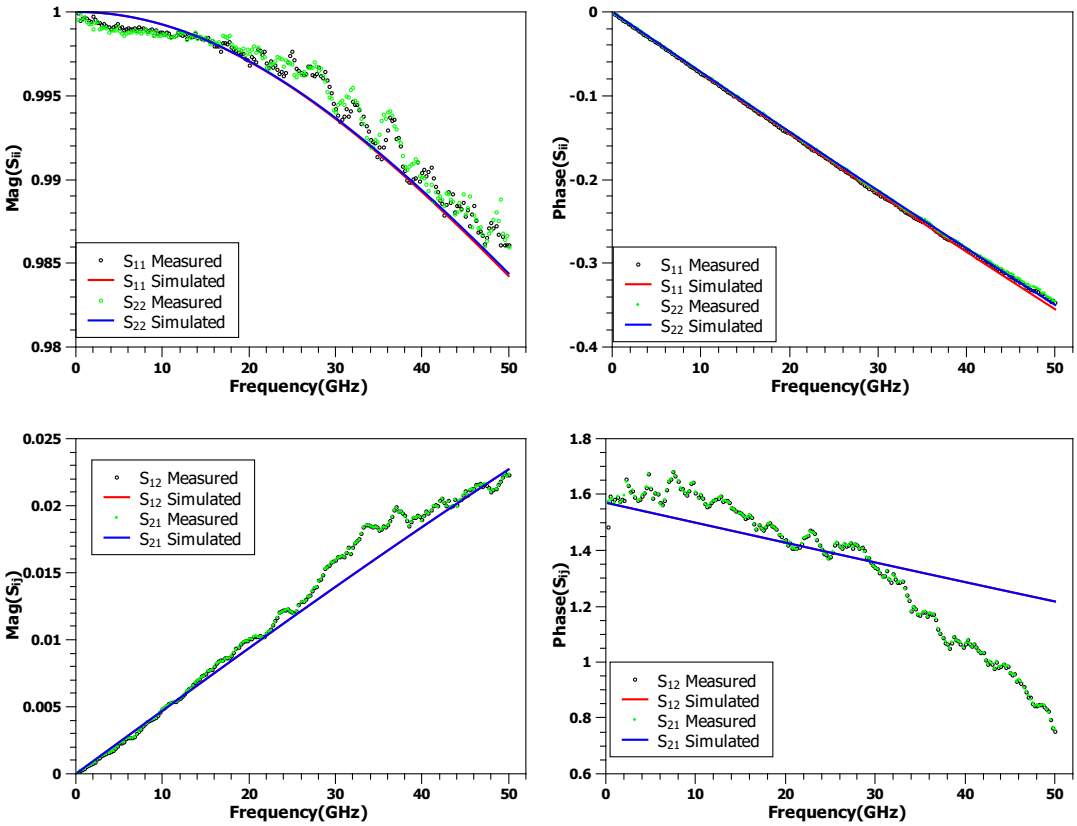


Figure 4.8: Measured (scatter plot) S-parameters of open structure and fitted (lines) by equivalent circuit extraction

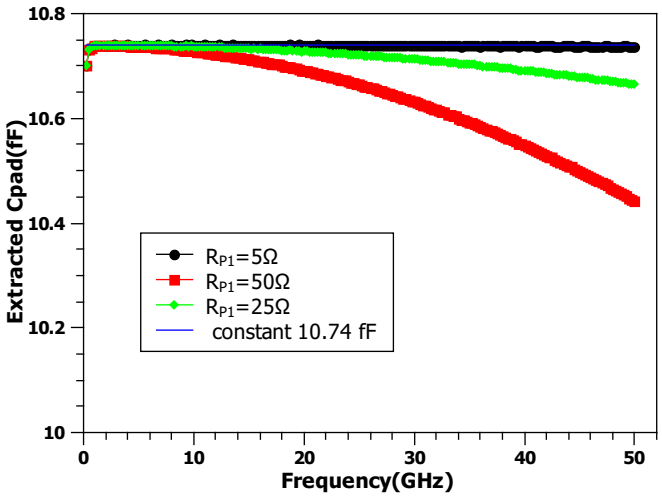


Figure 4.9: The dependence of extracted pad capacitance value on pad resistance

$$
\begin{aligned}
Y_{S-O} &= Y_{Short} - Y_{Open} \\
L_{F1} &= \frac{Im(Z_{S-O,11} - Z_{S-O,12})}{\omega} \\
R_{F1} &= Re(Z_{S-O,11} - Z_{S-O,12}) \\
L_{F2} &= \frac{Im(Z_{S-O,22} - Z_{S-O,21})}{\omega} \\
R_{F2} &= Re(Z_{S-O,22} - Z_{S-O,21}) \\
L_G &= \frac{Im(Z_{S-O,12})}{\omega} = \frac{Im(Z_{S-O,21})}{\omega} \\
R_G &= Re(Z_{S-O,11} - Z_{S-O,12})
\end{aligned}
\tag{4.4}
$$

The values extracted from the short structure are given in Fig.4.10, from which one finds that the equivalent inductance of the fingers is about 45 pH and the resistance about 0.5 Ω. The path from finger to ground was found to be equivalent to an inductance of 3 pH with a resistance below 0.1 Ω.

Step 2. Junction Capacitance

The junction capacitance can be extracted from the imaginary part of Y_{ij} in the low frequency range, as shown by Eq.4.5 [65], given the fact that junction capacitance dominates the impedance at this frequency range while series resistance and inductance are negligible. This is justified by simply calculating the impedance at lower frequency for a capacitor, resistor and inductor with values representative of a diode.

The capacitance extracted from Y_{12} (denoted as C_{Y12}) of the 4 μm diameter diode studied here is shown in Fig.4.11, where the results after de-embedding are also given. The extracted C_{Y12} is not exactly constant over the entire frequency range measured, due to the greater impact of inductance (as measured) versus frequency or series resistance (de-embedded). In any case, the resulting values of C_{Y12} at lower frequency remain without considerable change, which validates this method. The C_{Y12} at 250 MHz was used for further C-V fitting.

$$
C_{Yij} = \frac{-Im(Y_{ij})}{\omega} = C_{j0}(1 - \frac{V}{V_{bi}})^{-\frac{1}{2}} + C_{pp} \tag{4.5}
$$

The resulting C_{Y12} vs. V_{bias} is shown in Fig.4.12. It's worth noticing from the diode equivalent circuit that C_{Y12} is the combination of C_j and C_{PP}, and both have to be derived by fitting the curve using Eq.4.5 [65]. The fitted results were listed in the inset of the figure. The junction capacitance was obtained simply by subtracting the (C_{PP}) from C_{Y12}. The fitted junction capacitance at 0 V (C_{j0}) and built-in voltage (V_{bi}) , together with the grading factor of 0.5 for constant doping profile, describe the C-V characteristics of the diode under study in the SPICE model.

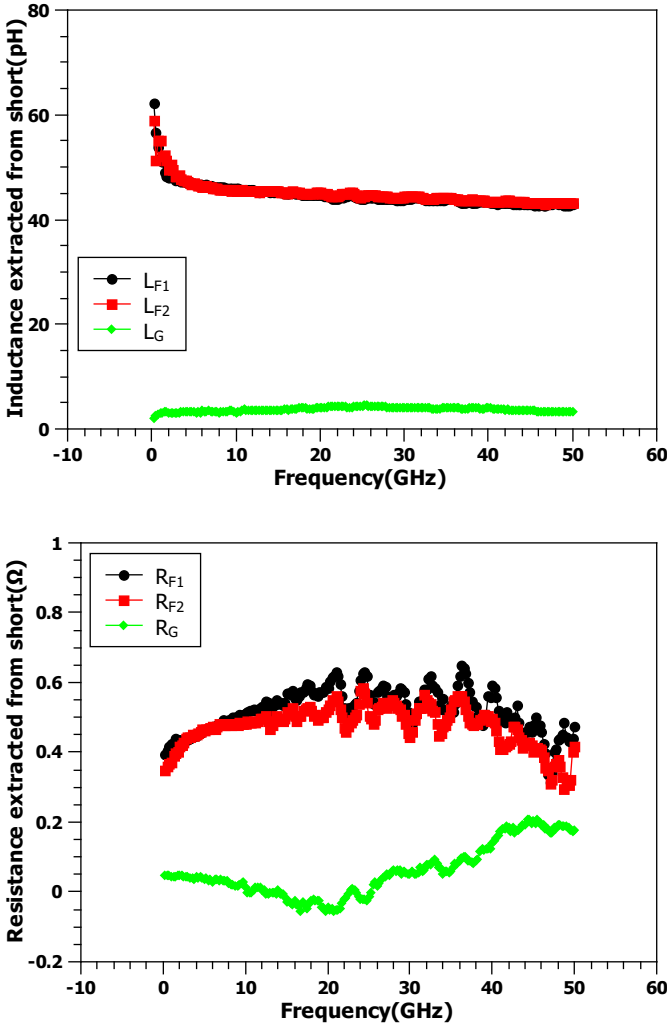


Figure 4.10: Extracted inductance and resistance from the short structure

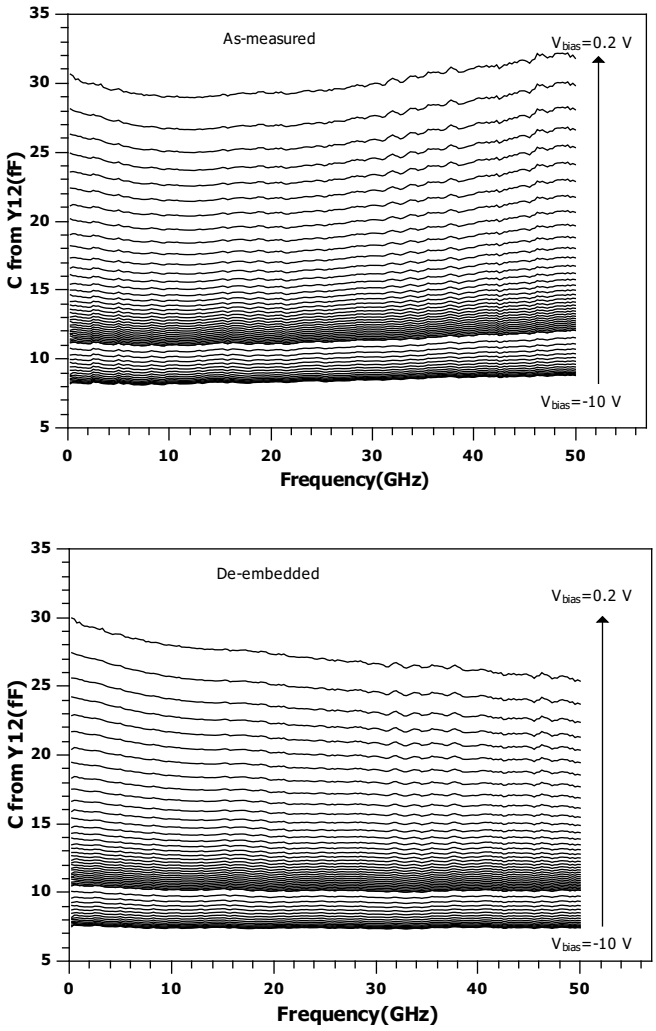


Figure 4.11: Extracted C_{Y12} from both as-measured and de-embedded Y-parameters

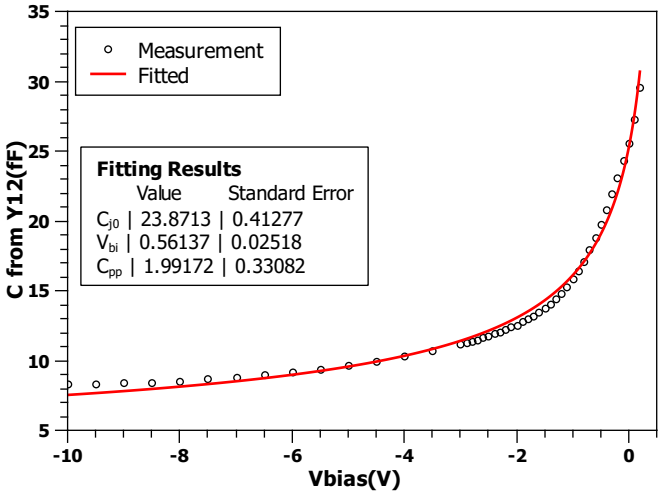


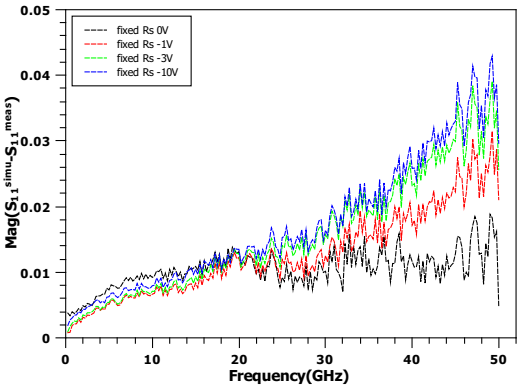
Figure 4.12: Extracted C_{Y12} versus bias voltage

Step 3. Optimization

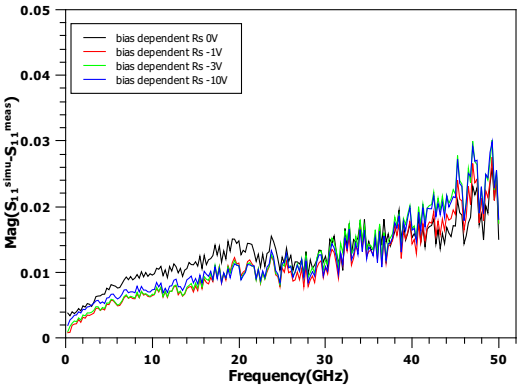
The analysis of DC IV characteristics and high frequency small signal S-parameters allows the complete derivation of the equivalent circuit elements. The deviation of the fitted S-parameters from the measured ones is described by the error function of Eq.4.6,

$$Error_{Sij} = Mag(S_{ij}^{simu} - S_{ij}^{meas}) \tag{4.6}$$

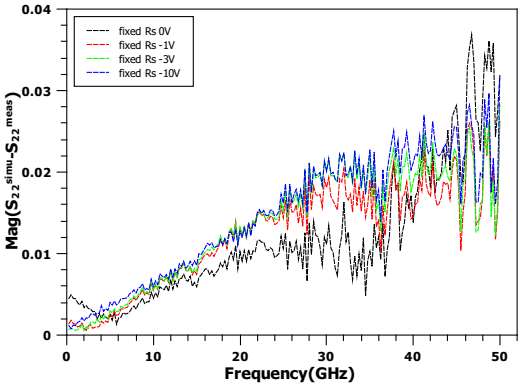
This error function represents physically the distance between two S-parameter points on the polar plane. By employing this error function, one can perform a fine tuning of the element values to further decrease the error. The errors resulting between fitted and measured S-parameters are shown in Fig.4.13 versus frequency for selected bias voltages. S_{12} is identical to S_{21}, and therefore the error of S_{21} was omitted. The figures in the left column of Fig.4.13 were obtained using parameters from the above analysis. It is worth mentioning that R_s was assumed to be a fixed value in the above analysis, which physically relates to the resistance of the N^+ layer and contact resistance. The resulted errors indicate that the above equivalent circuit fits the measurements very well. However, the undepleted N^- layer also plays a role in the derivations and results in a bias-dependent resistance [66]. Such a feature can be fitted by tuning R_s at each bias voltage towards smaller errors. The bias dependent R_s obtained in this way is shown in Fig. 4.14 and the reduced S-parameters error is shown in the right column of Fig.4.13 for comparison.



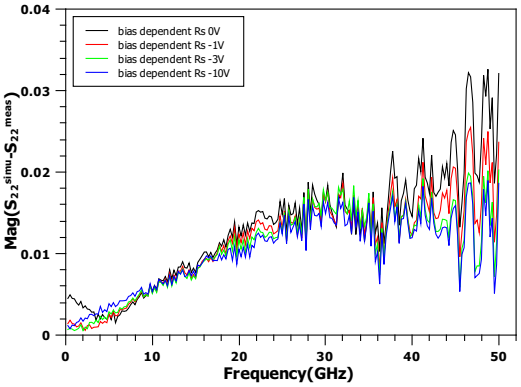
(a) S_{11} error with fixed R_s



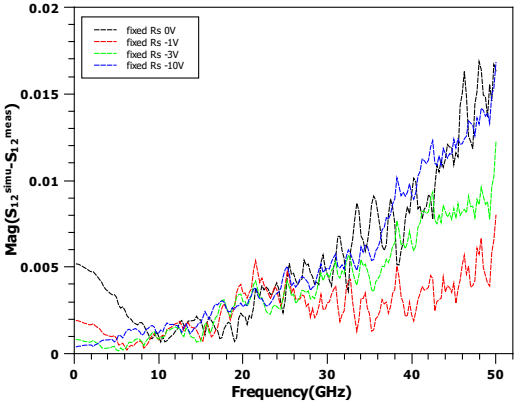
(b) S_{11} error with bias dependent R_s



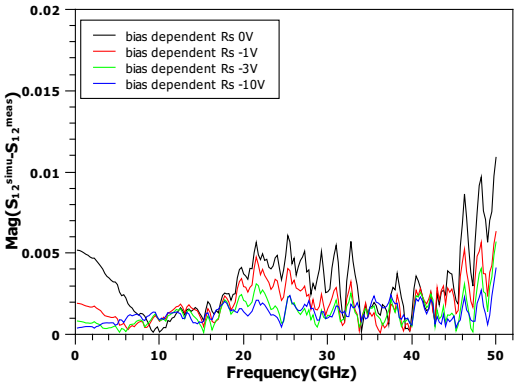
(c) S_{22} error with fixed R_s



(d) S_{22} error with bias dependent R_s



(e) S_{12} error with fixed R_s



(f) S_{12} error with bias dependent R_s

Figure 4.13: Errors of fitted S-parameters over measurements, with fixed R_s (left-column) and bias dependent R_s (right-column)

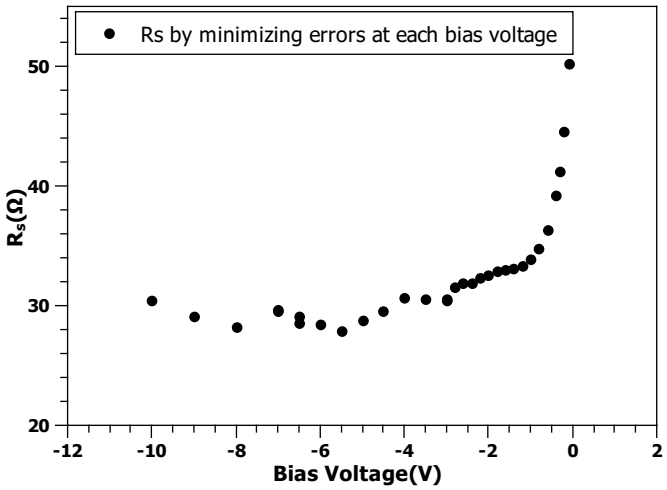


Figure 4.14: Optimized R_s at each bias voltage

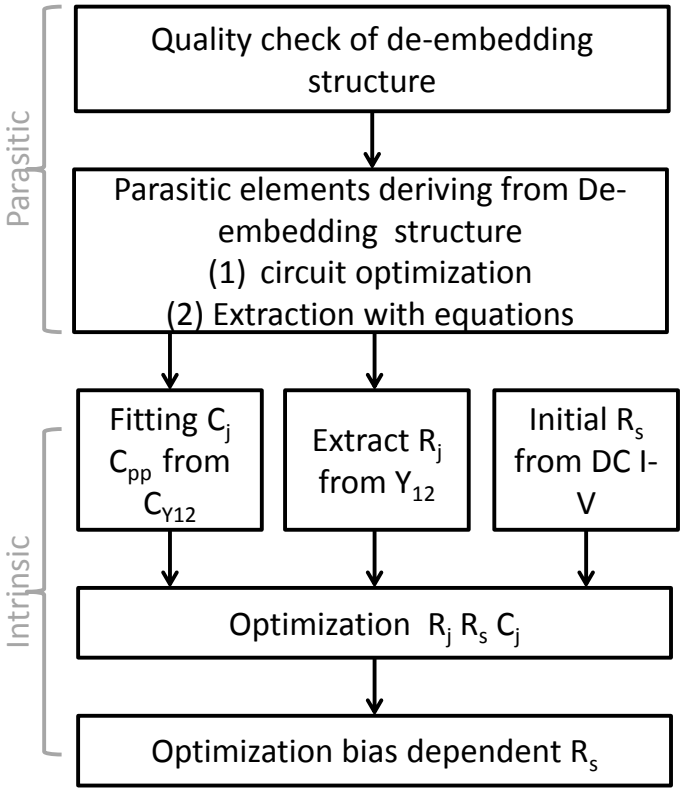


Figure 4.15: Flow chart of EC modeling based on small-signal S-parameters

Table 4.1: EC Parameters of 4 μm diode

parasitics			
R_{P1}	5Ω	R_{P2}	5Ω
C_{P1}	10.74 fF	C_{P2}	10.57 fF
C_{PP}	2 fF		
R_{F1}	0.5Ω	R_{F2}	0.5Ω
L_{F1}	45 pH	L_{F2}	45 pH
intrinsic			
R_j	10 kΩ	C_j	5.5∼27.9 fF
R_s	30∼50Ω		

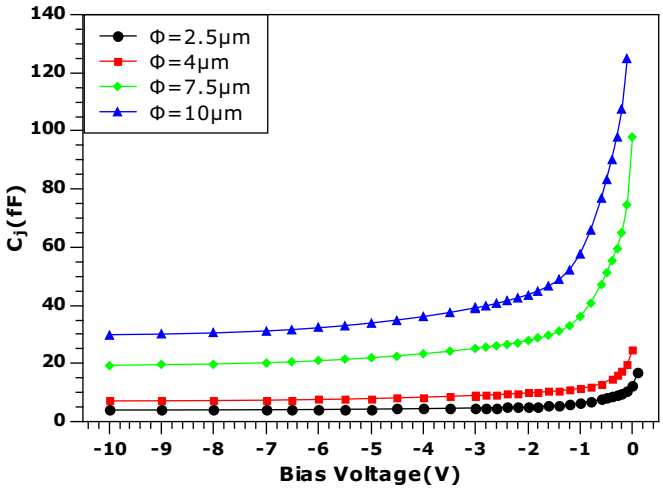
Summary

The modeling flow used in this work is summarized in Fig.4.15, and was implemented with the help of in Agilent ICCAP. Once again, it is worth pointing out that the nature of the intrinsic parameters requires an optimization-based modeling method using a circuit simulator, where all the intrinsic elements are varied together to obtain a minimum error from measured data. This impacts the modeling procedure in two ways.
1. Taking the bias dependence of C_j into consideration, a standard diode SPICE model would be beneficial for performing optimization in ICCAP. Without it, the use of a lump capacitor for representing C_j will require lengthy optimization, depending on the total number of bias points.
2. Due to the GaN material, R_s has greater impact on the port characteristics than using more traditional materials. R_s is set to a fixed value for the first optimization step, while further tuning of R_s at each bias point is necessary to permit good matching between simulated results and measured data.
The realized modeling procedure proved to be highly efficient and accurate.

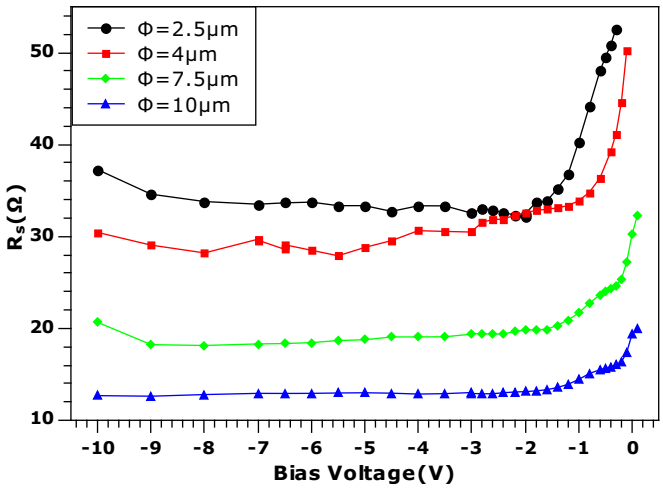
The derived EC elements of this 4 μm diode are summarized in Tab.4.1. Diodes with other anode diameters have the same pad dimensions, but differ in the dimensions of air-bridge width. Thus the pad parasitics remain the same as the diode analyzed here, while the finger parasitics change slightly.

4.4 Results

The main objective of modeling is to find the values of intrinsic elements, which represent the core part of the Schottky diode. This objective was reached by the modeling method described in this chapter, which allowed to evaluate the bias and diameter dependence of the C_j and R_s as shown in Fig.4.16. The evaluated C_j and R_s for different diameters provided a good reference for circuit design.



(a) Junction capacitance



(b) Series resistance

Figure 4.16: Extracted intrinsic parameters of diodes diameter from 2.5 to 10 μm

The diode cut-off frequency (f_c), defined in Eq.2.12 was calculated from C_j and R_s and is shown in Fig.4.17. Higher operation frequency is shown to be possible for smaller anode diameter diodes. For example, a cut-off frequency of 1.2 THz is expected from 2.5 µm size anodes, while 400 GHz are expected from 7.5 µm size anodes.

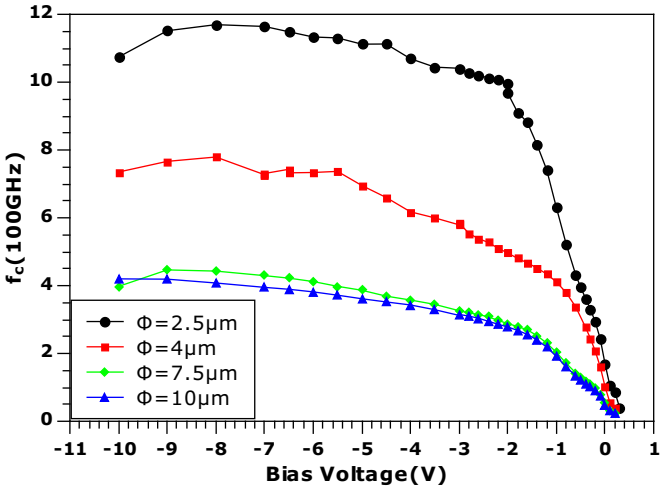


Figure 4.17: Calculated cut-off frequency from extracted C_j and R_s

The diode cut-off frequency is defined by the inverse of the RC time-constant, where R and C correspond to the diode's R_s and C_j. This implies an intrinsic physical limitation on diode operation frequency as determined by C_j and R_s. f_c is correlated to harmonic conversion efficiency as shown in Fig.2.4. f_c becomes higher for either a smaller C_j or R_s. R_s is in practice more important since a smaller C_j is corresponding to lower power handling capability. The obtained R_s in this work is high compared with that of GaAs-based diodes, leaving therefore room for improvement.

4.5 Conclusion

This chapter presented the characteristics of fabricated GaN Schottky diodes. High frequency small-signal measurements were performed for diodes with variable diameter and bias voltage values. The obtained S-parameters were analyzed by Equivalent Circuit modeling. This provided information on the Schottky junction and the way it is described by intrinsic elements of the EC model. The difficulties arising from periphery effects, dislocation assisted reverse current, as well as the way intrinsic elements interact with each other were explained. A modeling procedure was established and explained in detail using a 4 µm device as example. The obtained intrinsic elements were shown for different diode diameters and the diode cut-off frequency was derived.

5 Large-Signal On-wafer Characterization

On-wafer measurements are attractive for high frequency device/circuit characterization and modeling, due to the flexibility and convenience they offer. Looking at the past multiplier varactor research, one distinguishes two main areas of work, devices and circuits. Research on devices focuses on the epi-structure design and device geometry optimization, and key figures-of-merit like cut-off frequency (where series resistance and junction capacitance are included by definition) are used as performance indicator. These do not specify frequency multiplication related parameters such as conversion efficiency and maximum power, that are very useful for certain application. Multiplier circuit design requires considerable modeling effort for the varactor, matching/filtering at input/output and assembling the varactor into a waveguide, till the multiplication characteristic can be evaluated. The complexity of the design arises from the nonlinear nature of the device/circuit, which prevents one from an easy, direct evaluation of the multiplication performance. An attempt has been made in this work to explore the possibility of predicting the multiplication performance by on-wafer measurements, namely by a Large-Signal Network Analyzer (LSNA) as well as harmonic load-pull, instead of building a test waveguide circuit.

This chapter starts with a brief introduction on LSNA, where the setup schematic, operation principle as well as the way it can be applied to diode characterization are addressed. It is followed by the obtained results and their analysis applied to the fabricated GaN Schottky diodes. The measurement procedure and typical results are given first, followed by their interpretation. The measurements performed for GaN Schottky diodes include bias sweep, power sweep and harmonic loadpull. Different aspects of diode operation will be revealed with the help of LSNA.

5.1 Measurement Setup

Introduction on LSNA

The concept of S-parameters and the realization of commercial instruments for measuring them, have been successfully applied to the measurement, modeling and design of microwave devices and circuits. However, this is applicable under the assumption that the devices or systems behave in a linear way, i.e. when the nonlinear properties are not dominant and can thus be ignored. As technology is further developed, a large number of devices and circuits are required to operate in nonlinear region, as for example the case of high efficiency power amplifiers that require operation closer to compression

point[67]. Under such circumstances the device performance can not be easily described by S-parameters and nonlinear measurements are highly demanded to provide insight into the device operation.

There are mainly two methods demonstrated for nonlinear measurements [68]: these are based on a Large Signal Network Analyzer (LSNA) and Nonlinear Vector Network Analyzer (NVNA). These two methods are differentiated by the way of down-converting the signal to test, LSNA is sampler-based, while NVNA is mixer-based. In order to capture accurately time-domain waveforms, the calibration of signal power and phase is an absolute requirement.

The setup used in this research is a Maury MT4463A, whose block schematic is shown in Fig.5.1. The incident and scattered voltage waves are firstly sensed by couplers at both DUT ports. After attenuation, the sensed signals are sent to an RF-IF converter, which converts all the spectral components coherently to a lower frequency "copy". The resulting "copied" low frequency signals are further digitized by ADCs and collected by a control PC for data processing. The RF-IF converters decide the input bandwidth of the LSNA, which is 600 MHz to 50 GHz for MT4463A. The operation principle and calibration of the LSNA is beyond the scope of this thesis. A detailed introduction of it can be found in [69].

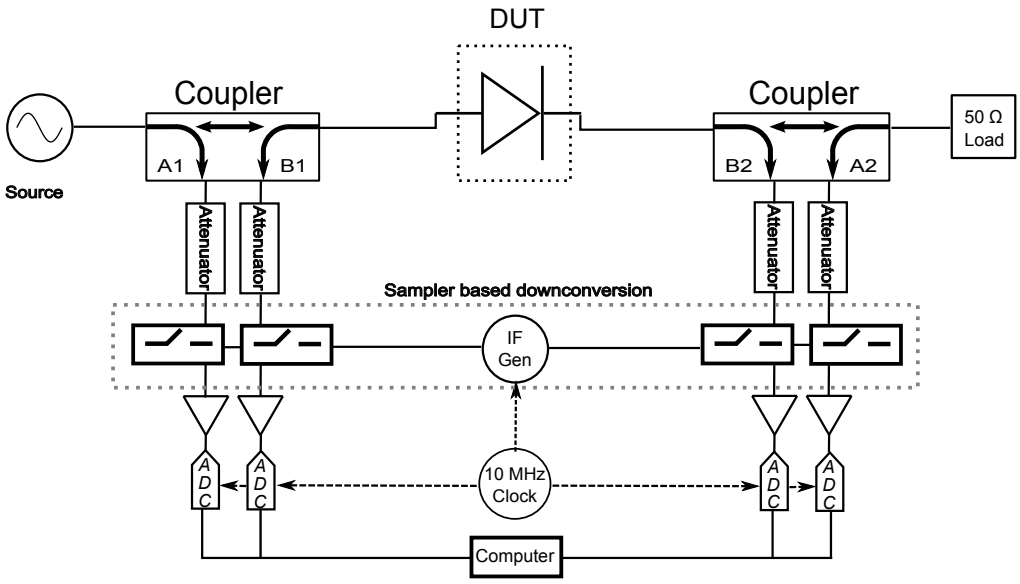


Figure 5.1: simplified block schematic of sampler-based LSNA

The results provided by LSNA can be in the format of voltage/current (V/I), incident/reflected voltage waves(A/B), time domain, frequency domain or envelop domain. Both A/B and V/I formats were used in our measurements and their significance is explained in Fig.5.2. They are equivalent in terms of information contained, and can be inter-converted using Eq.5.1.

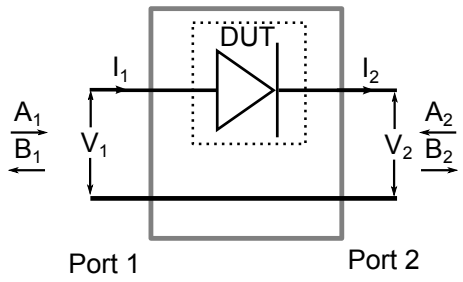


Figure 5.2: Port quantities definition in the measurement

$$\begin{cases} V_1 = A_1 + B_1, I_1 = \dfrac{A_1 - B_1}{Z_0} \\ V_2 = B_2 + A_2, I_2 = \dfrac{B_2 - A_2}{Z_0} \end{cases} \tag{5.1}$$

where, Z_0 is the characteristic impedance, normally equal 50 Ω.

Load pull is a common method used for transistor or circuit characterization. It provides information about the best load impedance for maximum output power or maximum efficiency by simply varying the load impedance systematically within a certain range. Load-pull is an exhaustive characterization technique, requiring measurement of numerous impedance points, from which the best load impedance is chosen. Load-pull systems can be classified into two types depending on the technique used for the impedance tuner, which maybe either passive or active. Conventional passive tuners, either electromechanically tuned or electrically tuned, provide a limited reflection factor (Γ), usually not exceeding 0.8 [70]. Active load-pull employs an additional signal generator which injects a signal into the DUT to analogue the reflected signal from load. According to the operation principle, the equivalent signal "reflected" by the "load" does not rely on the outgoing signal from DUT and thus a reflection factor as high as 1 can be obtained. A active load-pull system is used in this study as dictated by the fact that the S_{22} of the diodes has been measured to be larger than 0.9.

Applications of LSNA

LSNA has been applied to various types of devices and applications. In some cases, a device or circuit is characterized under exactly the same conditions (Bias voltage, incident power, input/output impedance etc.) as it will be used in a circuit or subsystem. Thus the measurement results represent the behavior of such device/circuit under real operation conditions. The results obtained are then used directly for circuit design/verification or diagnose.

As an example, efficiency enhancement of a power amplifier was demonstrated by time-domain waveform optimization [71]. By carefully tuning the load impedance at harmonics, the voltage and current waveforms may be monitored to obtain minimum overlap of

the voltage and current. A PAE as high as 84% at 1.8 GHz was achieved in this way. LSNA is also used as diagnostic tool for devices and circuits. The non-ideal characteristics of a mixer were identified by LSNA measurements with a special odd multisine IF signal [72].

In most cases, the devices or circuits under test need to be modelled for subsequent use in circuit simulation. Models are simply divided into two categories, equivalent circuit models formed by lumped elements and behavioral models. Models were developed to take into account the nonlinear effects, where LSNA techniques are very useful. Optimization can be applied to an equivalent circuit model by considering the waveforms provided by LSNA [73]. Behavioral models, however, consider the DUT as a black box and simply describe the relationship between the port quantities. The port quantities can be either in time domain, like V/I or frequency domain i.e. A/B. The so called Cardiff model applies in time domain, [74] and has been applied to LDMOS and HBT [75, 76] . A frequency domain behavior model was built for power amplifiers [77], where a table-based model described the transmitted and reflected waves as a function of the incident wave at both ports.

5.2 Large signal measurements of GaN Schottky diodes

5.2.1 LSNA with 50 Ω load

The default port impedance for LSNA is 50 Ω, as in most microwave measurement equipment. GaN Schottky diodes were characterized with the default load impedance first. The measurement configuration is shown in Fig.5.3. A power source with an intrinsic impedance of 50 Ω provides the incident power. Part of the power is absorbed by the diode and delivered to a 50 Ω load. The time-domain voltage and current waveforms at both anode and cathode are monitored by LSNA.

Two parameters can be swept in order to evaluate the nonlinear properties of the fabricated diodes, the power or bias voltage. By means of power sweeping, the bias voltage is fixed normally in the middle of the expected working range. Step by step increase of the power from small to large values allows the RF voltage swing to cover the entire working range. Bias voltage sweeping requires, however, the power to be relatively small. Then the minimum/maximum bias voltage has to be chosen to allow the RF voltage swing reach the lower/upper boarder of the full working range. Both methods can provide useful information for a diode under large signal operation. For the diode study here a high reactance impedance is present. As a result, a big part of the incident power is reflected. The expected RF voltage swing cannot be achieved even with the highest power available from the setup. Thus bias voltage sweeping is more practical for this purpose.

The results obtained by LSNA are in phasor form for either V/I or A/B, which contain naturally all harmonics from DC to the highest specification frequency of the setup. Given the maximum frequency of 50 GHz for LSNA, the fundamental frequency was

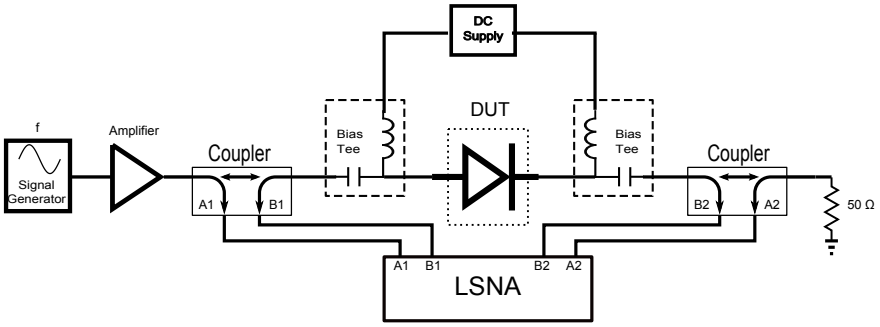
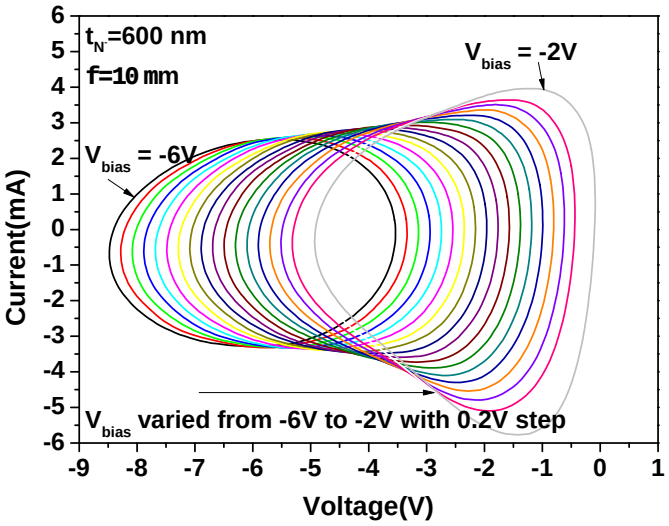


Figure 5.3: Configuration of measurement with 50 Ω

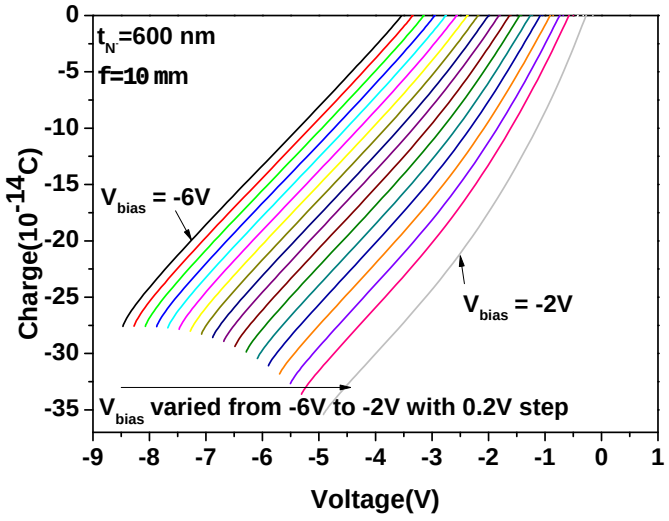
chosen to be 14 GHz. This choice was based on the availability of a power amplifier at this frequency as well as the harmonics that can be characterized. Thus the output typically contains four frequency components, DC, 14, 28 and 42 GHz, by which the time domain waveforms can be accurately represented. The power level beyond 4^{th} harmonic order was small, and could thus be neglected.

Time domain waveforms

Fig.5.4(a) shows typical time domain waveforms obtained from diode characterization. The I-V locus plot of time domain V/I waveforms was found to be easier to interpret than I/V-t plots by avoiding curve crowding. The current follows the RF voltage signal periodically thus forming the circle locus curves on the I-V plane. The space between each I-V circle represents the bias sweep step. Most of the spaces are uniform and equal to the value used here, i.e. 0.2 V, except when the RF voltage swing reaches 0 V, which indicates a pronounced nonlinearity. Comparing the I-V locus plots obtained by bias sweeping, the following could be concluded regarding the diode operation.
1. Significance of the locus curve. Each I-V locus curve is the instant current and voltage amplitude presented at the diode in one signal cycle. The product of current and voltage stands for the power of one signal cycle, thus the the area of a I-V locus curve stands for the power exchange between the diode and source. The shape of the locus curve corresponds to the nonlinearity characteristics of this operation region, while an irregular shape implies greater nonlinearity.
2. Bias dependence. As Schottky diodes show larger capacitance under a less negative bias voltage, the instant current is greater due to a larger displacement current required for charging/discharging the junction capacitance. Correspondingly, the power exchange is higher. This also explains the deformation of I-V locus curves, i.e. the nonlinearity is enhanced as the capacitance varies more.
3. Diameter and frequency dependence. The same principle applies when the diode diameter increases or the working frequency increases, i.e. the displacement current will be higher for the above cases and thus the power will also be higher.



(a)



(b)

Figure 5.4: (a) Typical time-domain waveform in I-V plot; (b) Q-V relation obtained by integration of current over time. The device is 10 μm on 600nm N^- GaN layer, measured at 15 dBm source power and bias sweeping

Time-domain waveforms contain essential information. However, a comparison between different devices and measurement conditions is not straightforward. Thus the time domain waveforms were further processed to compare the junction capacitance and the power performance.

Instant C-V under large-signal driven

The charge transfer driven by the RF voltage at the diode terminals leads in the generation of RF current. In light of this, it's worth comparing the total electron charge displaced in one RF signal cycle, forward or backward. This is calculated by integrating the current over time. Giving the periodic change of the input signal, the amount of moved charge starts from 0 in the beginning, and reaches a maximum value at half period, returns afterwards back to 0 by the end of the period and repeats the same cycle over the next period. Fig.5.4(b) shows how the total amount of charge increases over a half cycle, i.e. by a monotonous increase from the lowest voltage peak to highest voltage peak. As expected, the calculated total amount of charge increases when the bias voltage shifts towards 0 V.

An instant capacitance under large signal condition can be obtained by the differential of the charge over the RF voltage swing. Since the charge is instantaneously following the RF voltage swing, the capacitance calculated in this way corresponds better to the conditions encountered by the diode under real operation than under quasi-static and small-signal capacitance measurement conditions. Fig.5.5 shows the instant capacitance results versus instant voltage. The sharp capacitance decrease or increase is due to the RF voltage swing changing polarity, where the gradient of the voltage swing is infinitely small. By ignoring this abnormal part of the curves, several curves corresponding to different bias voltage, trace out the C-V relationship. The observed trend resembles the values extracted from small-signal measurements, but the minimum capacitance was larger than the small-signal one, while the maximum capacitance was smaller. In other words, the C_{max}/C_{min} ratio evaluated by LSNA was smaller. There is consequently a difference existing in the diode capacitance derivation from small-signal equivalent circuit modeling and large-signal evaluation.

With increased source power, the input RF voltage swing becomes larger. The instant C-V relations derived under such a condition and shown in Fig.5.6, can be used for better comparison. The source power applied to devices with 300 nm thick N^- layer was 18 dBm, while it was 23 dBm for its 600 nm counterpart. The instant capacitance calculated shows a lower minimum capacitance for a 600 nm than 300 nm thick N^- layer. However, due to the overall larger charge stored in the 600 nm thick N^- layer, the capacitance is larger when the voltage is not negative enough. Note that the 0 V condition was not achieved by RF voltage swing, and it was not therefore possible to compare the instant capacitance at 0 V directly. This larger maximum and smaller minimum capacitance are expected to offer higher power handling capability. These figures also show a deviation

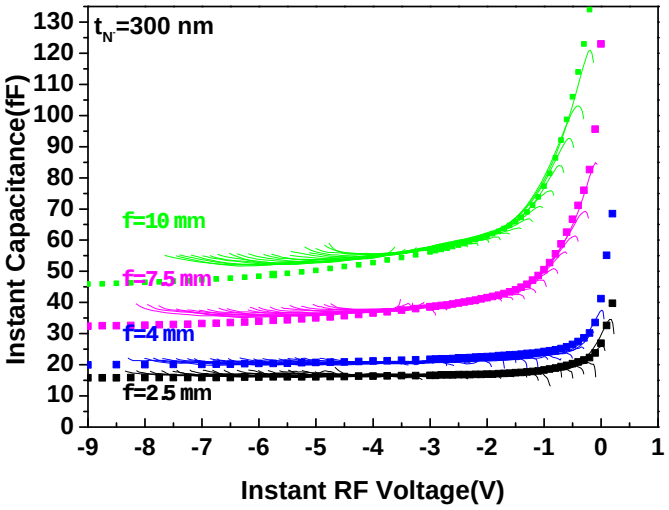


Figure 5.5: Derived instant Capacitance-Voltage relationship (solid lines), in comparison with extracted Capacitance from Small Signal condition (scatter dots)

of the instant C-V from the small-signal derived C-V characteristics, which manifests the necessity of performing large-signal measurements.

Power handling characteristics

The power handling capability of the fabricated devices was extracted from LSNA measurement results, using the same way of analyzing the time-domain waveforms as reported in Chapter 2. The measurements were performed with fixed bias voltage but the source power was swept. Then a source power level was chosen for each device under certain bias voltage to allow a voltage swing between 0 V and double the bias voltage. A comparison was made based on the same large-signal voltage waveform of each diode.

The two wafers discussed in the last section were compared in fig.5.7 for their power handling capability under the conditions explained above. Diodes with diameters ranging from 2.5 μm to 15 μm were characterized with a bias of -4 V and -6 V. These bias voltages were chosen to ensure the same voltage swing for all diodes.

Thanks to the greater capacitance of larger diameter diodes, the power handled is higher, and a value of about 100 mW was found for it in case of a 15 μm diode biased at -6 V. For the -4 V biased condition, this value is about 40 mW. Despite the thickness difference, the absorbed power is quite similar for diodes with same diameter and bias voltage. However, the reactive power for the diodes on 600 nm N^- layer wafer is lower than the ones on 300 nm N^- layer wafer. This is interpreted by a larger resistance arising from the thicker N^- layer, as already seen in the simulation results. Fig.5.8 shows the percentage of the ratio of power loss over the absorbed power. The loss depends strongly on the diode dimension. The ratio decreases as the diameter increases. When the diameter is larger than 10 μm, the ratio becomes less dependent on the diode diameter. For the cases

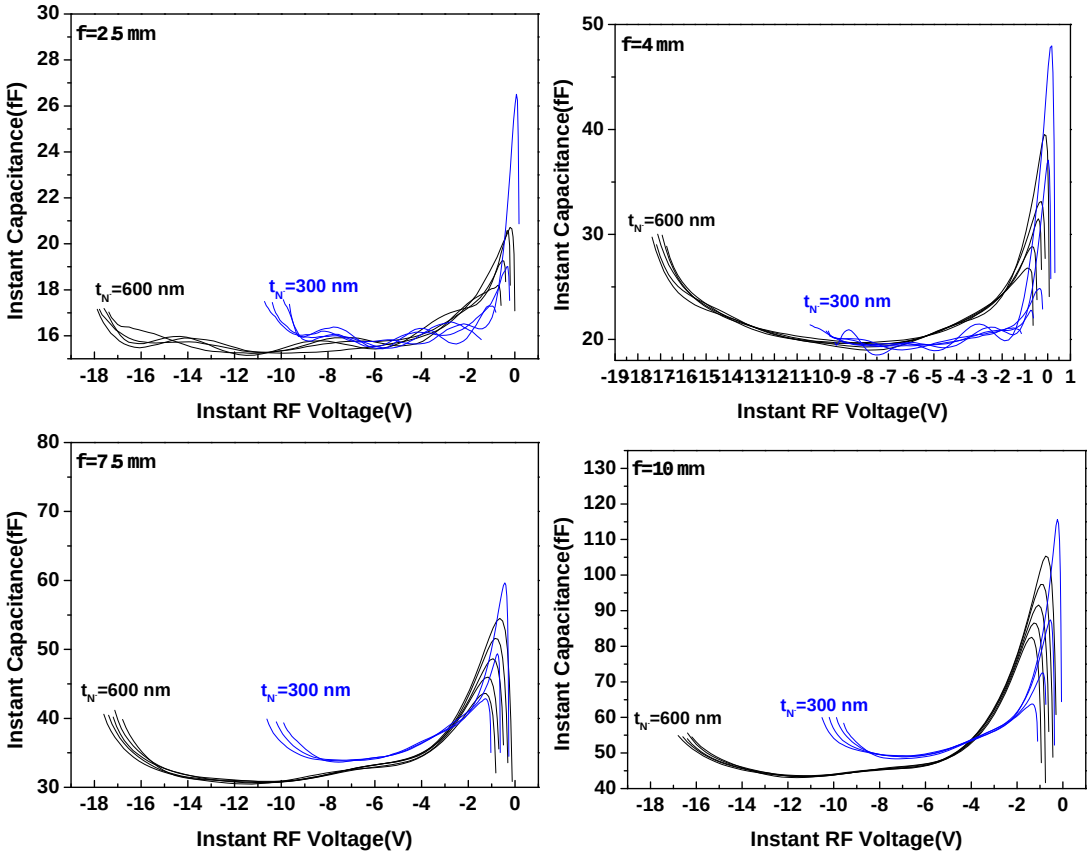
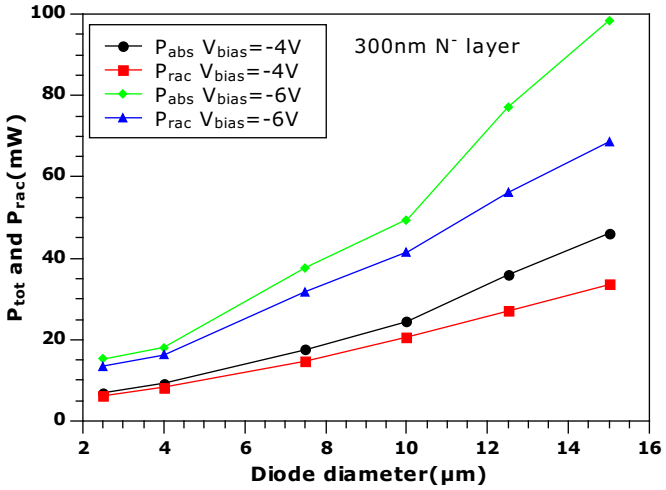
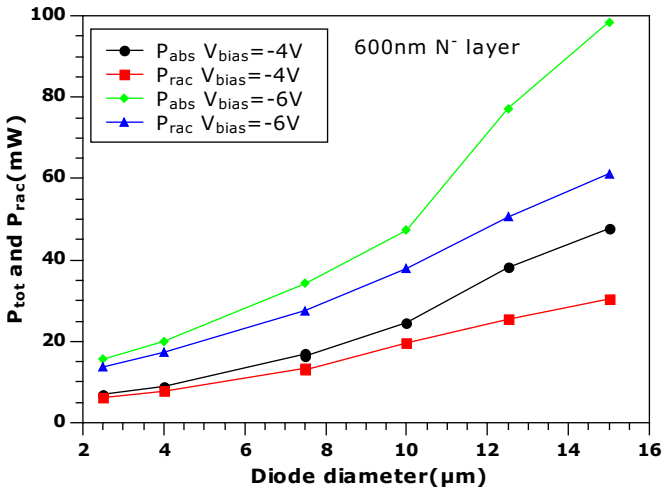


Figure 5.6: calculated instant Capacitance-Voltage relationship. Comparison of 300 nm N^- GaN layer with 600 nm N^- GaN layer, with device diameter from 2.5 μm, to 10 μm.



(a)



(b)

Figure 5.7: Power handling capability for (a) 300 nm thick N^- layer (b) 300 nm thick N^- layer

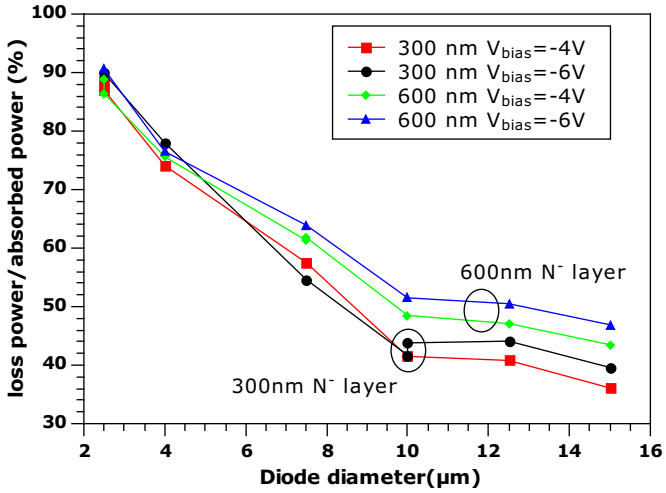


Figure 5.8: Percentage of loss power over the absorbed power

shown in the figure, the 600 nm N^- layer wafer has a higher loss ratio than the 300 nm N^- layer design.

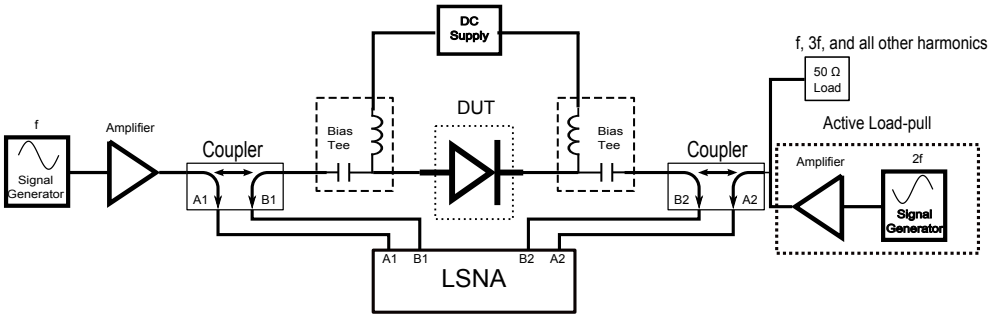


Figure 5.9: Configuration of measurement with load-pull at 2^{nd} harmonic

5.2.2 LSNA with harmonic loadpull

The discussion above addressed the characteristics of GaN Schottky diodes under large-signal conditions. However, due to the mismatch between the diode output and 50 Ω load, the harmonic power at the load is weak. In order to explore the nonlinearity of the diodes by considering the harmonic output of all orders, harmonic load-pull was employed to match the diode's output and allow maximum power of second harmonic transfer to load. The measurement setup is shown in Fig.5.9, where the only difference from the previous setup configuration is that the 50 Ω load has been replaced by an active load-pull, which is realized with an additional signal source operating at the second harmonic. The fundamental frequency was chosen to be 14 GHz. Thus the maximum frequency of 50 GHz for LSNA allows to obtain harmonics up to third order. It has to be noted that

the active load-pull allowed the presence of a variable load impedance at 28 GHz, while the load impedance for fundamental and third harmonic remained at 50 Ω.

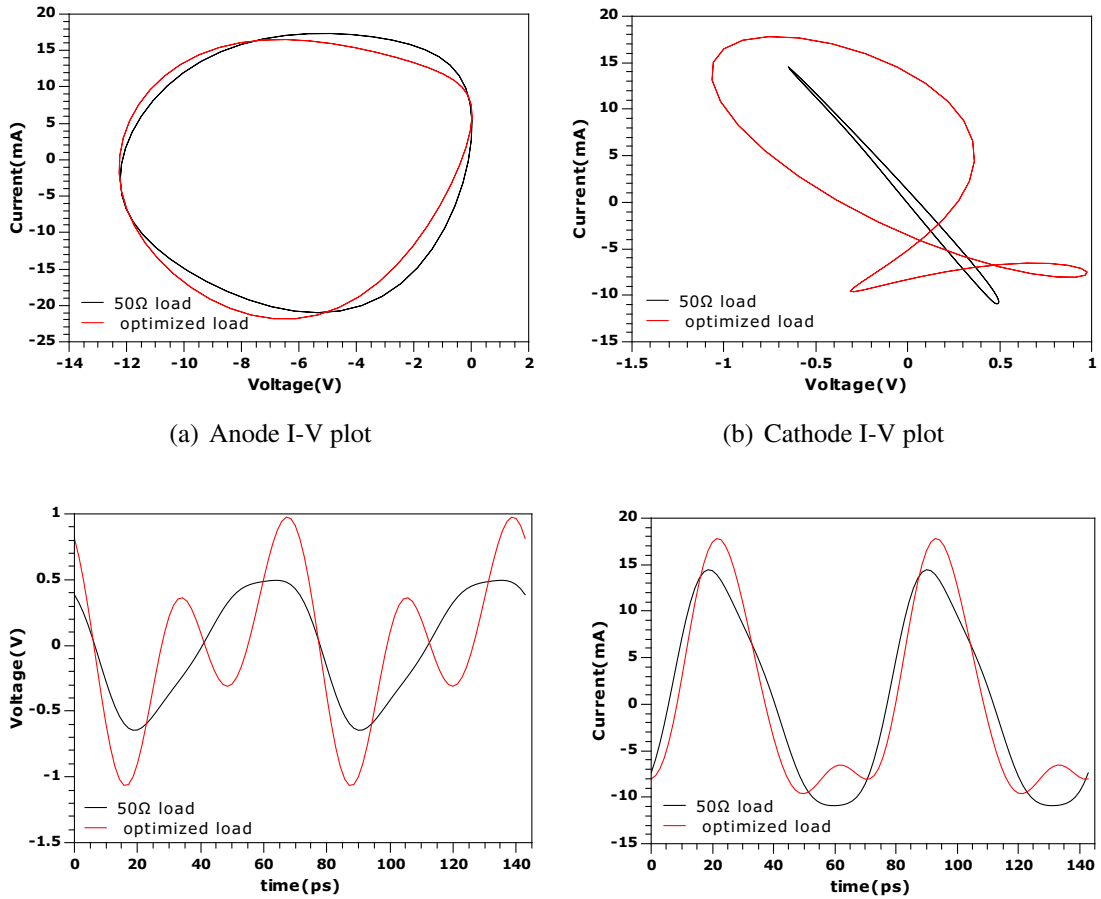
Searching of the optimum load impedance was performed first, by varying the amplitude and phase of the generated 2f signal. Once the optimum load impedance was found, the source power was swept to the maximum of the setup capability in order to explore the maximum diode potential. Typical time domain waveforms are shown in Fig.5.10, where a diode of 7.5 μm diameter on 300 nm thick N^- layer was measured with a bias of -6 V. The operation range was chosen to be similar for comparison purposes and corresponded to -12 V to 0 V as shown in Fig.5.10(a). Other than the circular shape I-V locus in the 50 Ω load case, the cathode I-V locus was crosslinked, which indicates enhanced harmonic amplitude. This is evidenced by the remarkably increased amplitude of the second harmonic as shown in the separate V-T and I-T waveforms of Fig.5.10(c) and Fig.5.10(d) respectively.

Comparison of output power was made based on the same operation range as for the 50 Ω load case. The total output power (sum of all harmonics) is shown in Fig.5.11(a) for different anode diameters, N^- thickness and bias. As a result of increasing the diameter, the total output power was found to be proportional to the anode area. A greater operation range indexed by bias voltage also caused higher output power. The dependence on N^- thickness was not significant.

The ratio of the 2^{nd} harmonic power over the total output power, shown in Fig.5.11(b), reflects the nonlinearity of the diodes. Enhancement of harmonic generation has been found to arise from better matching of the load impedance at the 2^{nd} harmonic.

It is worth mentioning that the voltage range chosen was only for comparison purposes, while the maximum capability of the diodes under study was not fully explored, since it required higher input power for achieving fully driven conditions that were not possible. Moreover, a high power driving condition could not be achieved due to the input mismatch between the diode and source. An attempt was made for diodes with 2.5 μm diameter, as shown in Fig.5.12. The measured device was driven by source power as high as 23 dBm, however, the corresponding power absorbed by the diode biased at -6 V was 9 dBm. The corresponding voltage range extended from -16 V to 1 V. The conversion loss was defined as the 2^{nd} harmonic power over the an absorbed power by the diode. It was found that it would achieve a saturated value of -10 dB for absorbed power above 5 dBm, which was about 10% in the linear scale. Considering the high loss and low reactance power offered by the 2.5 μm diodes, larger diodes are expected to provide higher power as well as 2^{nd} harmonic power.

One should keep in mind that the measurement performed here matched only the 2^{nd} harmonic at the output. Thus for frequency doubler circuits, where the input is matched and the harmonics are well isolated, the conversion of fundamental frequency to 2^{nd} harmonic would be inherently better. Overall, LSNA measurements provided basic information on the large-signal performance of the GaN Schottky diodes.



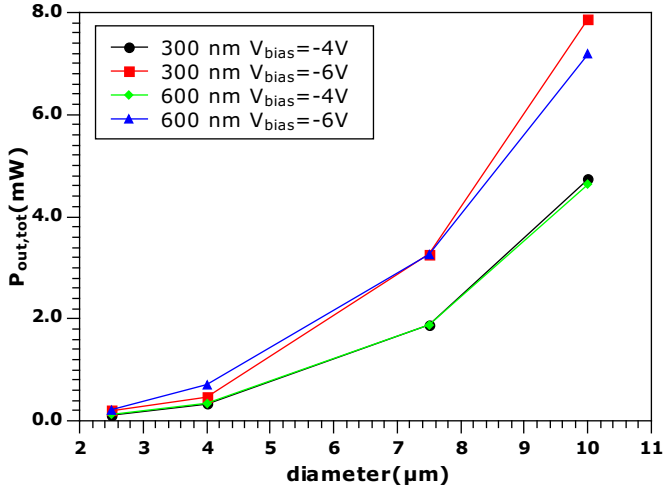
(a) Anode I-V plot

(b) Cathode I-V plot

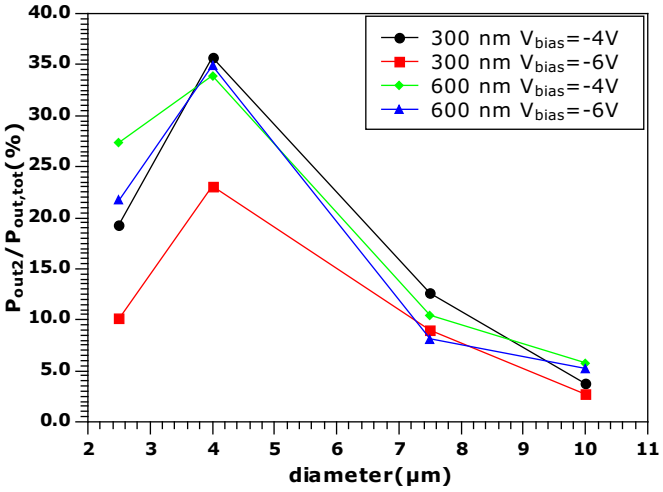
(c) Cathode V-t plot

(d) Cathode I-t plot

Figure 5.10: Time-domain waveforms of optimum load compared with 50 Ω load case. The results shown a diode of 7.5 μm diameter on 300 nm thick N^- layer, biased at -6 V.



(a) total output power



(b) percentage of the 2^{nd} harmonic power over the total output power

Figure 5.11: Comparison of output power based on the same operation range

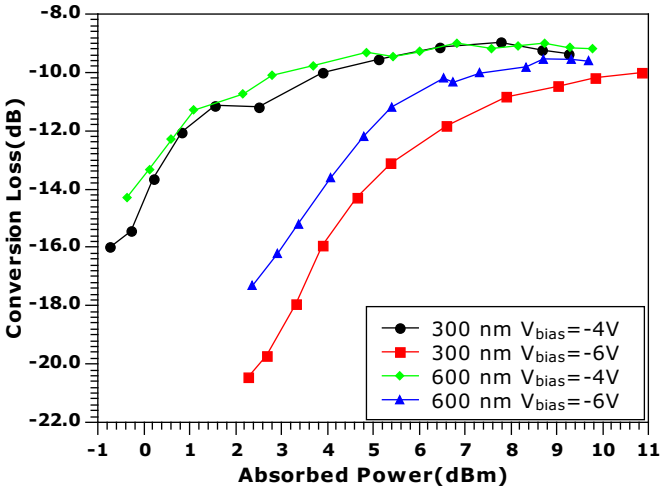


Figure 5.12: Conversion loss of 2.5 μm diodes

5.3 Conclusion

Diode characterization under large signal conditions was performed using LSNA and on-wafer tests. This novel characterization method allowed access of the time-domain large-signal waveforms of GaN Schottky diodes. The characterization demonstrated in this chapter allowed parameters such as instant capacitance, total power, reactance power to be derived under large-signal conditions and opened the way to the understanding of the large signal diode operation.

The described LSNA method can be standardized to provide rapid evaluation of diodes. This is important for device development as the case of Schottky diodes based multipliers, where the performance can not be easily predicted until a circuit is realized.

6 Circuit applications of GaN Schottky diodes for Signal generation and Control

This chapter presents two GaN Schottky diode applications, frequency multipliers for signal generation and phase shifters for signal control. To enable circuit simulation, a large-signal equivalent circuit model of the diodes was developed. The applicable modeling techniques will be first briefly reviewed. Frequency doubler circuits have been simulated using an equivalent circuit (EC) model, combined with a harmonic load-pull approach to achieve maximum output power. The use of GaN diodes in T-phase shifters was also explored. The diode capacitance required for such applications was obtained from theoretical analysis of T-phase-shifter circuits. Phase shifter MMICs were designed, fabricated and tested.

6.1 Large-signal modeling of GaN Schottky diodes

6.1.1 Review of large-signal modeling of semiconductor devices

The device modeling discussed in this chapter aims in finding a mathematical description of the device port parameters. The mathematical description has to represent satisfactorily the device characteristics, but be also incorporated into circuit simulators. A brief review of modeling techniques is reported first to facilitate the understanding of this task. As shown in Fig.6.1, modeling can be categorized with respect to three aspects [78]. First, the domain in which the measurements will be performed has to be selected with respect to the targeted application. This can be frequency-domain, time-domain or mixed-domain. The representation of the device under test can be in form of an equivalent circuit or a black-box. The latter one is also known as behavior model or measurement-based model. The "black-box" notation is associated with a model describing the relations of the port quantities, the so-called state-function, without knowing the information contained in the box. The equivalent circuit model, however, requires previous knowledge of the device operation principle. Moreover, the principle has to be well described by lumped circuit elements. The parameters linked in the models have to be determined by numerical techniques. If the measurement results can be expressed analytically by a series of equations with the desired parameters as independent variables, the parameters may be obtained easily by solving the equations. De-embedding of the parasitic elements from small-signal S-parameter results is one of the examples applicable to this case. Should this not be the case, a numerical method is applied to search

the value of the desired parameter within certain range and use the one fitting the results best.

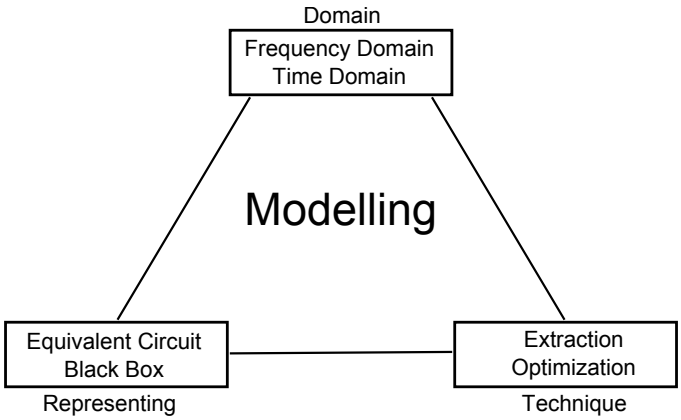


Figure 6.1: 3 aspects of modeling

With the development of large signal characterization instruments, models to which large signal measurement results can be applied have emerged. Examples of such models have been mentioned in chapter 5 [69, 74]. According to the discussion above, one expects behavioral models to be very attractive with respect to equivalent circuit models, due to the fact that it is much more convenient to derive state-functions than obtaining equivalent circuit elements. Behavioral models can be build based on the time domain waveforms, a good example of which is the Cardiff model [79]. Time domain waveforms of a two-port network can be expressed as

$$\begin{cases} I_1(\omega) = A_0 \cdot \delta(\omega) + \sum A_n \cdot V_{IN}^n(\omega) \cdot \delta(\omega - 2\pi \cdot n \cdot f_0) \\ I_2(\omega) = B_0 \cdot \delta(\omega) + \sum B_n \cdot V_{IN}^n(\omega) \cdot \delta(\omega - 2\pi \cdot n \cdot f_0) \end{cases} \tag{6.1}$$

where V_{IN} is input stimulus, n is the order of harmonics, f_0 is the fundamental frequency. The coefficients A_n and B_n correlate the input stimulus V_{IN} in a way that physical meaning can be provided to the Y parameters. A_0 and B_0 are in fact the DC components of the current waveforms. It's desirable that A_n and B_n depend on bias conditions, input voltage stimulus, as well as load impedance,

$$\begin{cases} A_n = \dfrac{I_1(nf_0)}{V_{IN}^n(f_0)} = F_1(|V_{IN}|, \Gamma_{Load}, V_{DC,IN}, V_{DC,OUT}) \\ B_n = \dfrac{I_2(nf_0)}{V_{IN}^n(f_0)} = F_2(|V_{IN}|, \Gamma_{Load}, V_{DC,IN}, V_{DC,OUT}) \end{cases} \tag{6.2}$$

By look-up tables for A_n and B_n, circuit simulators can quickly evaluate the port currents at given conditions. The implementation of this model has been demonstrated in ADS for LDMOS [75] and HBTs [76].

Frequency domain-based behavioral models employ traveling voltage waves as independent variables. The reflected waves B_{pm} are expressed as a spectrum mapping function[69],

$$B_{pm} = F_{pm}(A_{11}, A_{12}, \cdots, A_{21}, A_{22}, \cdots) \tag{6.3}$$

where A is the incident wave and B the reflected wave while subscript pm stands for the mth order harmonic at port p.

This spectrum mapping function has been used to define $\mathbb{S}$-parameter [80], which follow the same physical definition as small-signal S-parameters but also take harmonics into account. Thus the subscript of a $\mathbb{S}$-parameter element has four number, two of them stand for the port while the other two stand for the harmonic order. An element $\mathbb{S}_{ijkl}$ is associated to the ratio of the outgoing wave at port i with harmonic order k over the incoming wave at port j with harmonic order l. The letter $\mathbb{S}$ is used to allow differentiation from small signal S-parameters. Considering three harmonic orders for a two-port network, the $\mathbb{S}$-parameter matrix has 36 elements. This function is non-analytic, and can therefore only be derived in a table-based approach.

By taking the phase of A_{11} as reference, and linearizing around the large signal operation point, a model called Poly-Harmonic Distortion (PHD) [69] is formed. This can be expressed as:

$$\begin{aligned} B_{pm} =& K_{pm}(|A_{11}|)P^{+m} \\ &+ \sum_{q,n\neq 1} G_{pq,mn}(|A_{11}|)P^{+m}\Re A_{qn}P^{-n} \\ &+ \sum_{q,n\neq 1} H_{pq,mn}(|A_{11}|)P^{+m}\Im A_{qn}P^{-n}, \end{aligned} \tag{6.4}$$

whereby

$$\begin{aligned} P &= e^{j\phi(A_{11})} \\ K_{pm}(|A_{11}|) &= F_{pm}(|A_{11}|, 0, ...0) \\ G_{pq,mn}(|A_{11}|) &= \frac{\partial F_{pm}}{\partial \Re A_{qn}P^{-n}} \mid_{|A_{11}|,0,...0} \\ H_{pq,mn}(|A_{11}|) &= \frac{\partial F_{pm}}{\partial \Im A_{qn}P^{-n}} \mid_{|A_{11}|,0,...0}, \end{aligned} \tag{6.5}$$

This is in fact the mathematic foundation of Agilent X-parameters. Eq.6.4 suggests that to construct the model, it is necessary to perform a three-step measurement. First, a large signal has to be applied, from which the K_{pm} parameter will be determined. Then a small signal has to applied together with the existing large signal over all the ports and harmonics. In a third step, step two is repeated with a phase rotated small signal. Having results from all three steps, the equation can be solved to determine the K_{pm}, $G_{pq,mn}$ and $H_{pq,mn}$ parameters.

Thanks to the PHD model, it is possible to extract data about parameters that have not been measured by extrapolation. However, work reported by the Cardiff group indicates

that it's best to simulate accurately under conditions corresponding to those used for model extraction [81]. In case of time domain models used in nonlinear circuit simulation, such as harmonic balance or envelope analysis, the simulation algorithms have to transform back and forth between time and frequency domain. Frequency domain based behavioral models are therefore attractive for simulation [82]. Behavioral models in both domains face the same problem in data size when the measurement density and numerically independent parameter increases.

The validation of a model depends very much on the used characterization conditions. In typical PA design, it is required to specify the load impedance, input power and bias condition. These parameters can be easily varied in a measurement, thus the validation of the model for specific application is guaranteed. In case of the diode multipliers studied in this thesis, filters are required to isolate the input fundamental signal and output harmonic signal. As depicted in last chapter, the output power at f_0 is maintained at around 50% of the total output power. If a filter working at f_0 is placed at the output side of the diode, this power will be reflected back into the diode and enhance the output at $2f_0$. The lack of such filters during measurements make it harder to predict the performance of a diode as doubler based on the measured data.

6.1.2 GaN Schottky Diode Modeling

Considering the various modeling approaches applicable to diodes, it appears that the most practical and efficient approach is the one based on parameter extraction using small signal S-parameter measurements and optimization/verification combined with large signal measurements. The large-signal model will in this case replace the bias dependent components in the small-signal model with a mathematic description, which allows the circuit simulator to perform simulation under non-static operation conditions. In the case of diodes, the bias dependent components correspond to R_j, R_s and C_j, which are extracted using as EC modeling technique of small-signal S-parameters. The implementation of this approach is discussed further in this section. The developed large signal modeling and optimization procedure resembles a "LEGO" piecewise method as described in [83], where Symbolically Defined Devices (SDD) in ADS have been employed[84].

The realized model is composed of four building blocks as shown in Fig.6.2, where "DIODE1" was used to represent the forward current and breakdown voltage, "SDD1P1" stands for R_j for reverse DC current, "SDD1P2" for R_s and "SDD_cap" for the C_j. The four building blocks are discussed below in detail in terms of their roles and the way they can be derived.

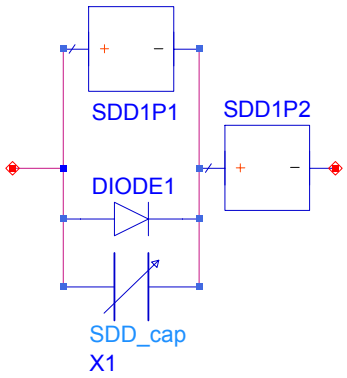


Figure 6.2: Large signal diode model schematic for GaN Schottky diodes

DC I-V Representation

The SPICE model of diodes considers a diode whose I-V characteristics can be described as a set of equations[85], where the current in the operation range (between reverse breakdown and heavily forward conduction) is given by Eq.6.6.

$$\begin{cases} I_d = I_s(e^{\frac{V_d}{n \cdot V_T}} - 1), & -10 \cdot n \cdot V_T \leq V_d \leq V_{max} \\ I_d = I_s(e^{-10} - 1) + \dfrac{I_s}{n \cdot V_T} e^{-10}(V_d + 10 \cdot n \cdot V_T), & V_{br} \leq V_d \leq -10 \cdot n \cdot V_T \end{cases} \tag{6.6}$$

where n is the ideality factor, I_s the reverse saturation current, V_T the thermal voltage, V_{max} the maximum forward voltage and V_{br} the breakdown voltage.

The forward conduction current of the GaN Schottky diodes studied here was modelled easily by the first equation, where the values of I_s and n were obtained by fitting of the forward I-V characteristics. However, the current in the reverse bias region given by these equations is nearly of the same order as I_s. This implies that for the GaN Schottky didoes studied here, the reverse leakage can not be modeled in a simple way. The alternative solution used was a SDD symbol whose resistance was fitted to represent a bias dependent R_j in the reverse bias region. This component was placed in parallel with the diode component based on the SPICE model, as shown in the resulting model schematic of Fig.6.2.

R_s Representation

As discussed is section 4.4, a bias dependent R_s was found to be more appropriate for GaN Schottky diodes than a constant R_s value. The validity of this statement will be further proved using the phase shifter circuit results of Section 6.3. For the diodes under study, their R_s was found to be exponentially changing with bias, thus an exponential function was applied. Fig.6.3 shows an example of how the R_s was fitted.

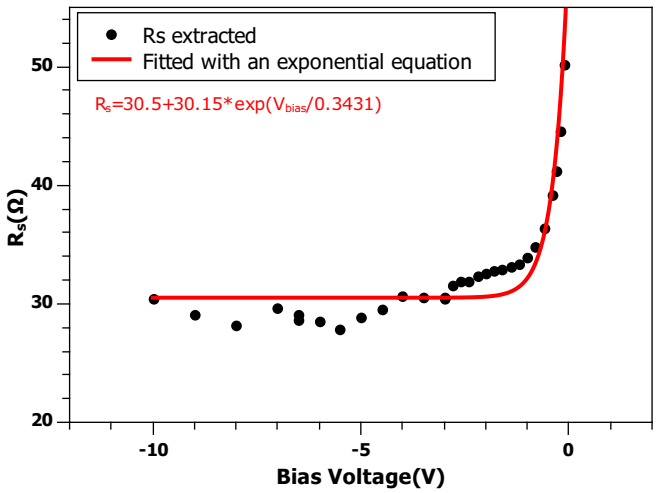


Figure 6.3: Fitting R_s with an exponential function

C_j Representation

C_j and its dependence on bias voltage were extracted from small-signal S-parameter as discussed in chapter 4. These data set up the basis for the evaluation of the large-signal model of C_j. The SPICE model of the diode describes C_j as follows

$$C_j = C_{j0}(1 - \frac{V_d}{V_j})^{-M} \tag{6.7}$$

where C_{j0} is the capacitance at 0 V, V_j the barrier height and M the grading factor, which is 0.5 for a constant doping epi-layer.

For the GaN Schottky diodes under study, the C-V curves are usually flat at bias voltages below the one corresponding to full depletion of the N^- epi-layer. The region of flat C-V characteristic has to be taken into account when the diodes are driven by a large voltage amplitude, which is normally the case of GaN diodes. As it turns out it is difficult to match such a C-V curve with Eq.6.7, where the flat C-V region is normally underestimated compared with the sharp increasing portion of the C-V characteristics. An example explaining the above discussion is shown in Fig.6.4. The proposed solution was to replace the SPICE equation with an exponential equation. If two exponential sections are included in the equation, it is even easier to obtain a better fitting accuracy.

A two-port SDD device has to be used for the implementation of such a capacitor [86]; it employs an intermediate variable to represent the derivative of voltage over time. Then the current of the capacitor is expressed by the product of capacitance and this intermediate variable.

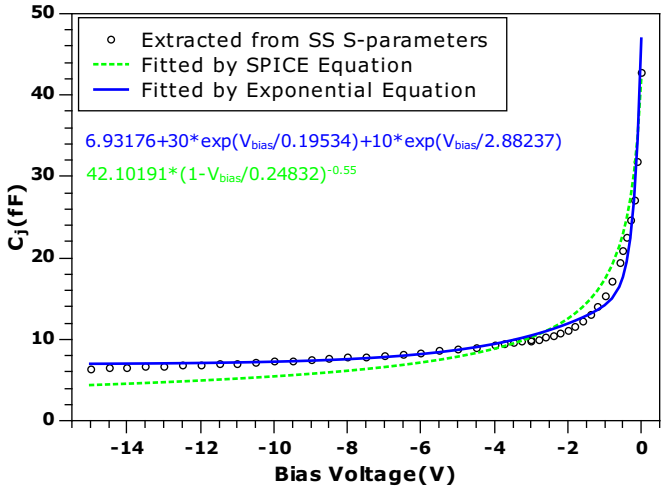


Figure 6.4: Comparison between exponential and SPICE functions for C_j modeling

C_j Tuning Based on Large-Signal Network Analyzer Characterization

For Schottky varactor diodes, C_j is the most critical component in the EC model. As has been seen in chapter 5, the C_j derived from LSNA results differs from the values derived from small signal S-parameters. The LSNA measurement, permitted to evaluate the deviation of C_j under large signal conditions, a task that is otherwise rather complicated. The obtained LSNA results also allow to tune C_j correspondingly in order to obtain a model that matches better the measured characteristics.

Fig.6.5 shows an example of such an attempt. The large signal EC model has been built based on the approach described above. The model was used under the same conditions as those applied to the diode in a harmonic load-pull test. As expected from the analysis, the large-signa performance predicted by S_VNA (simulation based on results by Small signal Vector Network Analyzer) differs considerably from the one expected based on measurement data. Since the power absorbed and stored by a capacitor is directly proportional to the capacitance value, the higher absorbed power suggested by this model indicates an over-estimated junction capacitance C_j.

By tuning the junction capacitance C_j, a new S_LSNA model was determined and found to better match the large-signal measurement results. As shown in Fig.6.5 by the symbols with dashed lines,, the results from this model match the measurement results for both the absorbed and output power under large absorbed power conditions. For low absorbed power levels, such as for example at -6 V bias, the simulation results from the S_LSNA model lead to under-estimated characteristics of output power. This was suspected to be caused by the exponential function used for describing the C_j-V curve, which leads to relatively weak bias dependent C-V trends in the bias range < -6 V compared with measurements. The above findings indicate that the S_LSNA model leads to a smaller deviation from the real device characterization when the device is subjected to very large

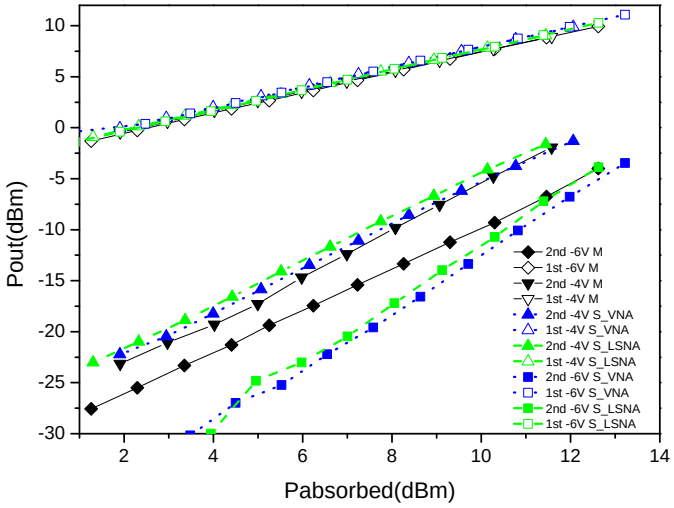


Figure 6.5: P_{out}(dBm) versus $P_{absorbed}$(dBm). Symbols with solid lines: measured results(abbr. as M); symbols with dotted lines : simulation results with model extracted from small-signal S-parameter(abbr. as S_VNA); symbols with dashed lines : simulation results with model tuned towards LSNA(abbr. as S_LSNA); Solid symbols: 2^{nd} harmonic; Hollow symbols: fundamental harmonic.

high-frequency power levels. The C_j-V characteristic adjusted for this purpose is shown in Fig.6.6 for comparison.

Summary of the modeling procedure

The modeling procedure using the large-signal EC model is reviewed in Fig.6.7. As can be seen a key step is to find the right equation describing the bias dependence of each component; this equation has then to be included into the circuit simulator. DC and Small-signal measurements provide all necessary information for the large-signal modeling. However, the model built in such a way relies very much on the bias range of small-signal measurements. In principle, the resulting large-signal model can not be used for predicting performance outside the measured bias range. For example, the exponentially fitted R_s was valid for negative bias values, but not in the forward region, where it predicts values much higher than in practice.

Overall, this procedure allowed to obtain a large-signal diode model for circuit design and simulation. The bias range where the model is valid depends on the measurements.

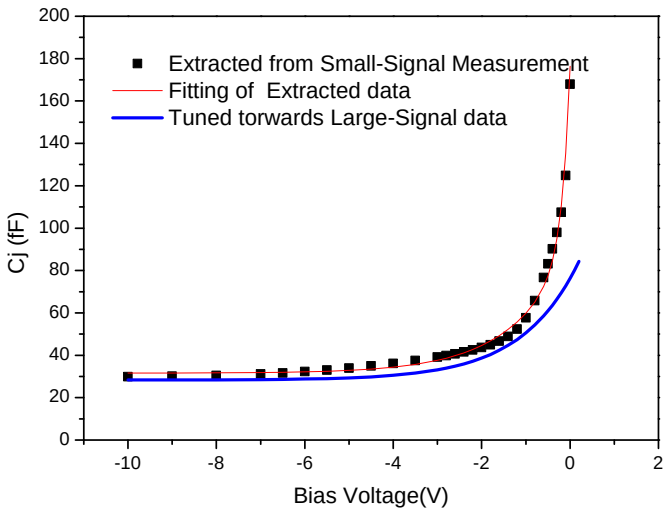


Figure 6.6: Junction capacitance C_j extracted from small-signal S-parameter of a 10 μm GaN diode

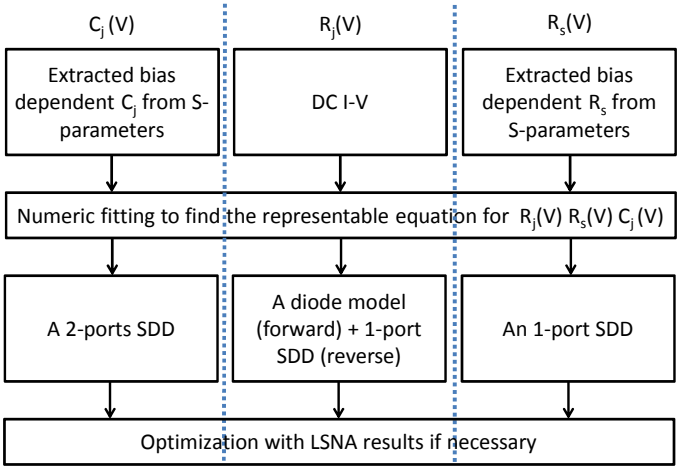


Figure 6.7: Flow chart of large-signal modeling for GaN Schottky diodes

6.2 Frequency Doubler

The obtained large-signal models allow to evaluate the characteristics of diode-based circuits. This section presents the characteristics of a 94 GHz frequency doubler based on a single 10 µm diode.

The diagram in Fig.6.8 shows the configuration used for frequency doublers. Frequency doublers need to separate input (fundamental) and output (second harmonic) signals by filters. Ideally, the filter is placed at the input side and is designed to be transparent to the fundamental signal but shorten out all other harmonics. The filter at the output side, on the other hand, should allow only the second harmonic signal to be delivered to the load. Matching networks at both input and output are also required for delivering maximum power to the load.

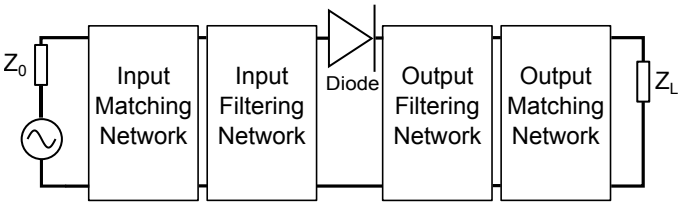


Figure 6.8: Block diagram of a single diode frequency doubler

This diode was modeled and represented as shown in Fig.6.9, where all the parasitic and intrinsic elements are included. The intrinsic elements were described in the way presented in last section, and all parameters were list in separate "VAR"(= variable) components.

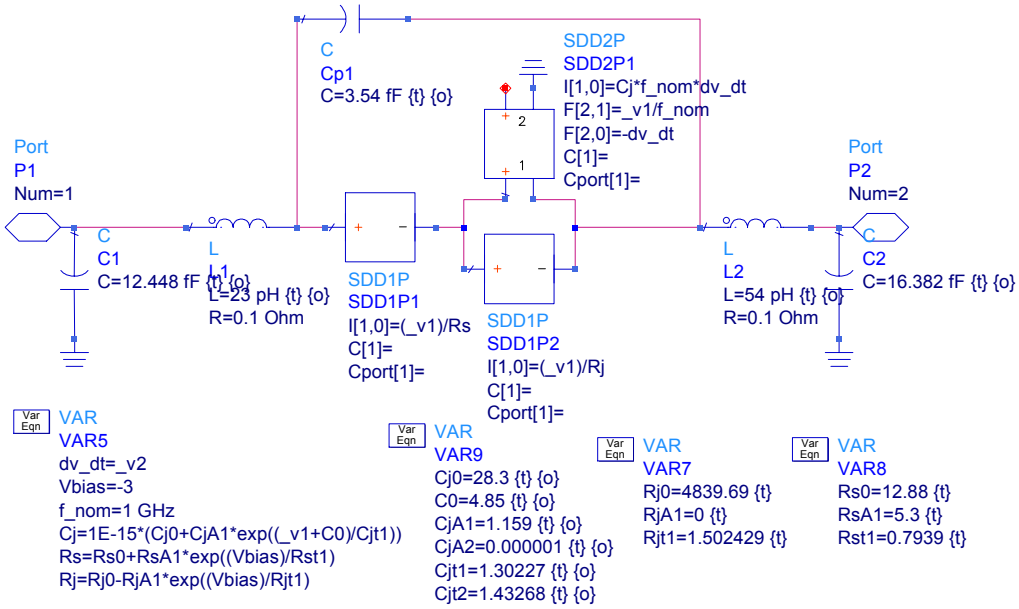


Figure 6.9: Schematic of large-signal model of the 10 µm diode

The filters had to be considered next. The filters can be realized by $\lambda/4$ stubs [37], as shown in Fig.6.11. The input short stub "TL2" had a length $\lambda/4$ at 47 GHz, which is equivalent to $\lambda/2$ at 94 GHz. It creates therefore a reflective short for currents at 94 GHz without affecting currents at 47 GHz. The open stub "TL1" had also a length $\lambda/4$ at 47 GHz, behaving as reflective short for currents at 47 GHz. The stub acts as a $\lambda/2$ open section at 94 GHz and does not consequently perturb the output signal.

The overall effects of these two stub filters can be understood as two "walls", where the "TL2" prevents the generated second harmonic from propagating towards the source while the "TL1" prevents the fundamental signal from propagating towards load. For a given substrate, the stub width and length are decided only by the frequency. Considering a 254 µm (10 mil) substrate with a dielectric constant of 9.6 and an ideal conducting metal, one finds for the stub dimensions using LineCalc in ADS a width of 274 µm and length of 594 µm for the stub "TL1", and a width of 352 µm and length of 557 µm for "TL2". The resulting S_{21} characteristics of the two stubs are shown in Fig.6.10. In the absence of stubs the transmission characteristics resemble those of a high-pass filter that allows both the fundamental and second harmonic to travel through all parts of the circuit. When "TL1" alone is used (dash line), the signal at the fundamental frequency of 47 GHz is prevented from going through (S_{21}=0 at 47 GHz). On the other hand if one has "TL2" alone (dot line), the second harmonic at 94 GHz is stopped from Propagating (S_{21}=0 at 94 GHz). The combination of the two stubs results in the solid curve that illustrates the possibility of isolating (S_{21}=0) the fundamental and harmonic frequency. A study of the impact of substrate on the stub characteristics showed that an increase in substrate thickness leads in sharper transition form stop to pass frequency.

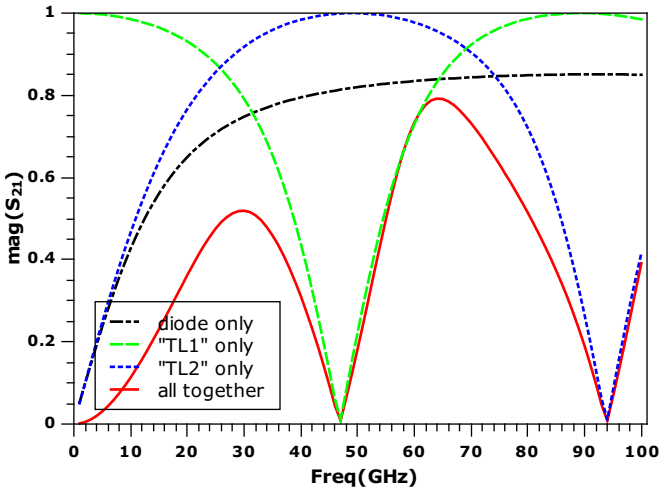


Figure 6.10: S_{21} of the diode and with the presence of stubs

The design of matching network was simplified due to the utilization of filters. The doubler circuit can be considered as consisting of two separate equivalent circuits. One included the diode and the output filter, and the other included the input filter and diode.

Input matching was established by considering the former network , while output matching was calculated based on the latter. Such a configuration allowed the load and source impedance not to interact with each other during the design of the matching network.

The simulation performed at this stage allowed to find the optimum source and load impedance providing maximum output power. Harmonic Balance (HB) and load-pull techniques were used for this purpose. Since maximum output power is sought at the second harmonic, load-pull was performed at this frequency. With both the input and output matched, the ratio of second harmonic output power over fundamental source power is defined to be the conversion efficiency. This was indexed by $\mathbb{S}_{2121}$ under the large-signal $\mathbb{S}$-parameter definition [80] as discussed in section 6.1. $\mathbb{S}_{2121}$ was shown to be useful for the optimization of frequency doublers.

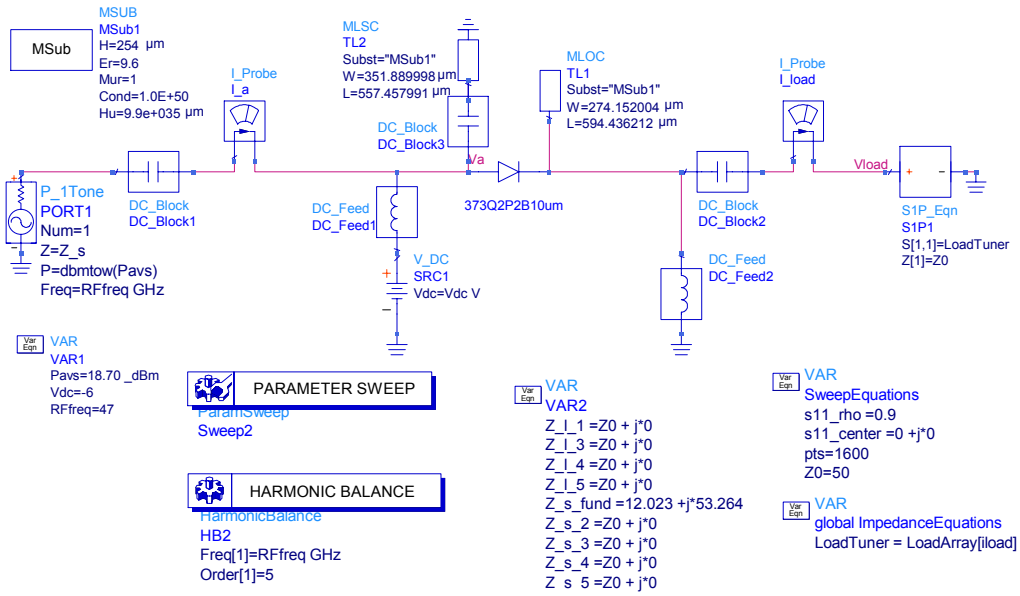
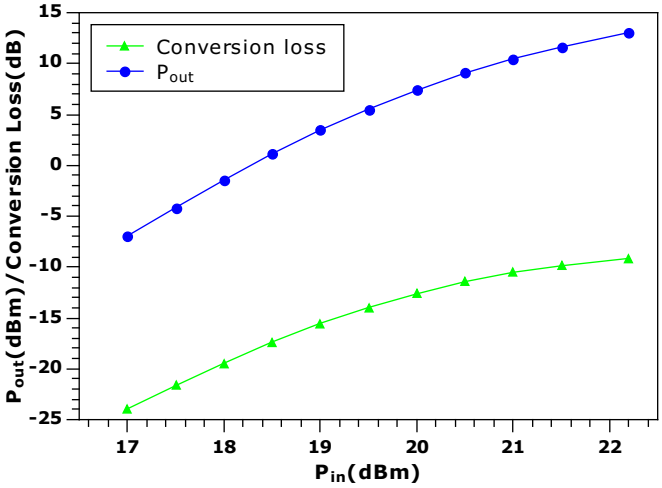


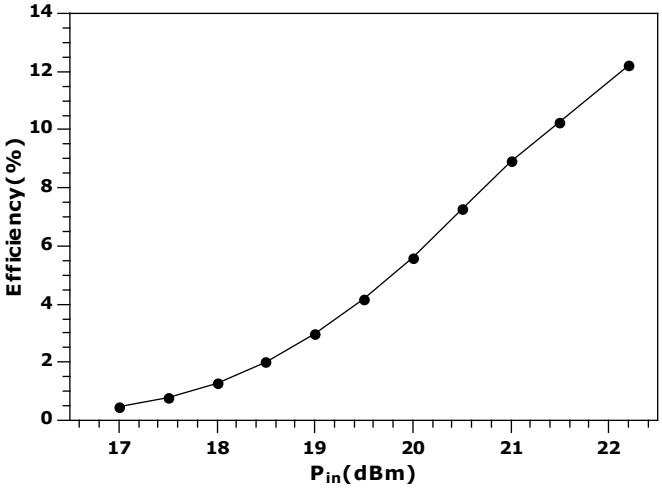
Figure 6.11: Schematic of circuit setup used for combining harmonic balance and harmonic load-pull for doubler design

A schematic of the doubler simulation approach used in this study is shown in Fig.6.11. The HB simulation was set to include up to 5^{th} order harmonic. The source and load impedance were also set to respond up to 5^{th} harmonic, while adjustment of their values was possible at each harmonic independently. Under certain bias voltage and source power level, the simulation was performed first with the source impedance defaulted to 50 Ω. This resulted in load-pull mapping in the impedance plane, and allowed to find the maximum output power and corresponding load impedance. Moreover, the input impedance (reflection coefficient) at the fundamental frequency could also be obtained for this specific load impedance. Maximum power delivery could be achieved at the input after setting the source impedance to equal the conjugate of the input impedance. The optimum source impedance, load impedance, as well as input and output power under optimum impedance conditions could be obtained after two to three iterations.

The results obtained in such a way are shown in Fig.6.12, where the diode was biased at -10 V and the input power was swept up to a value allowing a maximum operation range between -20 V and 0 V. The output power increased with input power monotonously but the conversion loss indicated for the diode was found to approach saturation.



(a) P_{out} and conversion loss



(b) Efficiency

Figure 6.12: Simulated results of the 10 µm diode biased at -10 V, input power swept

The resulting load-pull contour and time domain waveforms under the defined maximum input are shown in Fig.6.13 and 6.14. This 10 µm diode biased at -10 V could absorb an input power of 22.2 dBm (166 mW). An optimum load impedance of $14.46 - j8.57$ was found from the load-pull impedance mapping contour, to allow a maximum output power of 13.05 dBm (20.2 mW). The source impedance of $11.4 + j56.79$ assured delivery of 22.2 dBm source power to the diode. The corresponding conversion efficiency was

12.2%. The time domain waveforms were monitored to assure the diode operates well in the determined range. Both voltage and current waves at the cathode side showed frequency doubling compared with waves at the anode side.

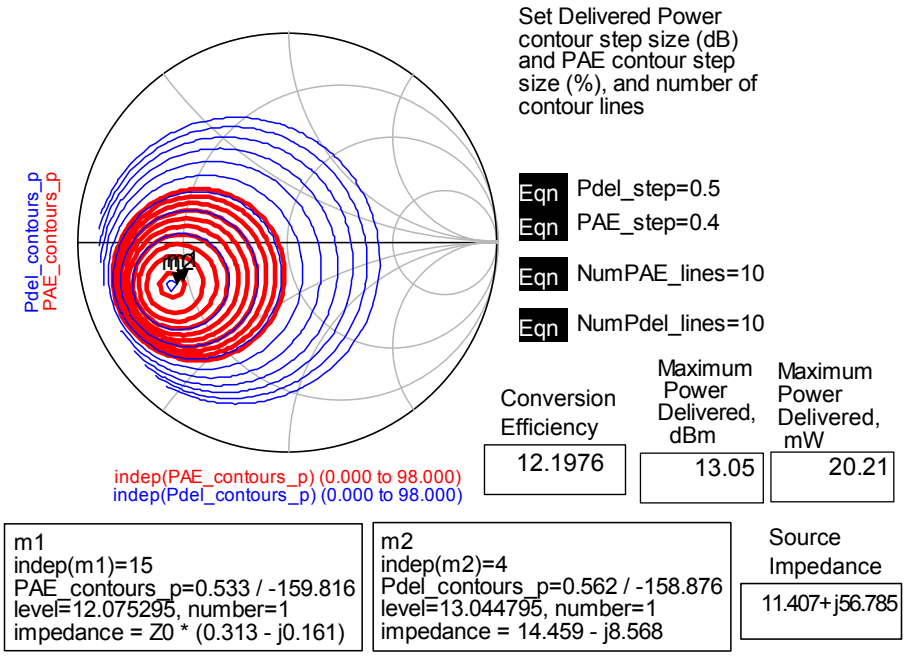


Figure 6.13: Simulation results of the single-diode doubler

A 16 µm GaAs diode with N^- layer thickness of 650 nm and $7 \times 10^{16} cm^{-3}$ doping has been found to convert an input power of 330 mW into 65 mW output with 19.7% efficiency [37]. Taking the diameter difference into account, the 10 µm GaN diode under study had shown better power handling capability permit anode area than the GaAs diode. It's worth noting that an extension of the operation range into the forward region would further enhance the doubler performance.

6.3 Phase shifter MMIC

This section presents a phase shifter circuit based on GaN Schottky diodes. To the author's knowledge, this is the first report on T-phase shifters using GaN-based Schottky diode design.

High power amplifiers have been demonstrated with good performance at microwave and millimeter-wave frequencies such as an output power of more than 1.7 W [27] and 3 W [29] at W-band. As the performance of power amplifiers continues to be improved, other components based on GaN have been the focus of intensive studies aiming in a fully integrated solution. In light of this, one-bit 45° phase shifters based on GaN technology have been investigated at X-band using HEMTs by permitting switching between two states [87].

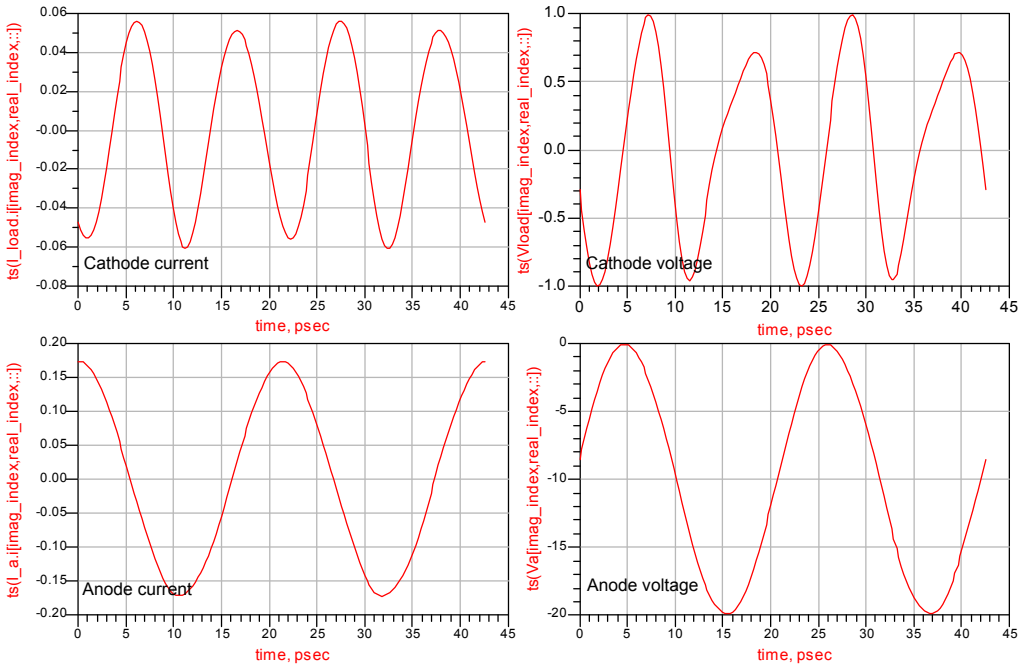


Figure 6.14: Time domain voltage/current waves of at anode and cathode

GaN-based approaches offer the possibility of realizing robust components as necessary for various applications. This study reported in this section presents the design, fabrication and experimental characteristics of a 35 GHz Microwave Monolithic Integrated Circuit (MMIC) analog phase shifter using GaN Schottky diodes to enable continuous phase shifting rather than digital/bit operation normally possible by HEMTs. The phase shifter design is based on the well known [88] "T" concept and includes integrated passive components for matching and biasing. The use of GaN technology permits the same concept to be explored for robust applications that extend the power capability beyond that offered by other technologies [89]. The experimentally obtained characteristics and models from the discrete diodes reported in this thesis, were used for simulating the phase shifter.

Diode Selection

The T-Phase Shifter topology used in this work is shown in Fig.6.15. Circuit operation with optimum matching and phase shifting characteristics requires a shunt diode capacitance with a value which is twice that of the series capacitance element. An inductor is also included in the shunt arm. The high-pass T-network considered here was analyzed with the help of the equations below and the ADS software. This allowed the evaluation of the resulting phase shift and impedance presented at each port.

The impedance of each branch is assumed to be Z_1, Z_2, Z_3, while the impedances presented at port-1 and port-2 are Z_{P1}, Z_{P2} respectively. The impedance of each branch of

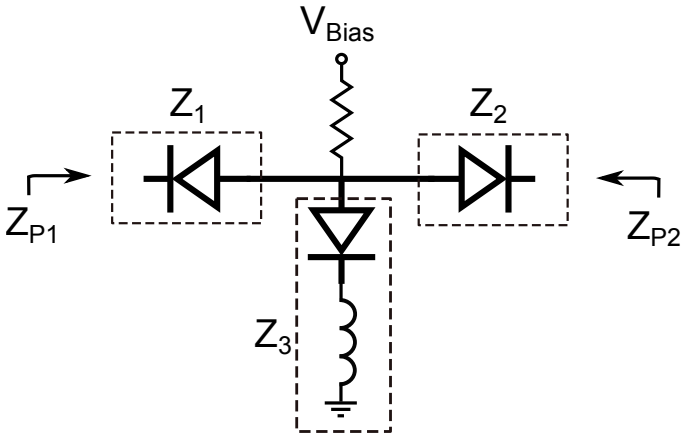


Figure 6.15: T-Phase shifter Circuit Configuration

the T-network can be expressed by the port impedance and the phase difference between two ports (β), as shown by the equations below.

$$Z_1 = -j * (Z_{P1} * \cos(\beta) - \sqrt{Z_{P1} * Z_{P2}}) / \sin(\beta) \tag{6.8}$$

$$Z_2 = -j * (Z_{P2} * \cos(\beta) - \sqrt{Z_{P1} * Z_{P2}}) / \sin(\beta) \tag{6.9}$$

$$Z_3 = -j * \sqrt{Z_{P1} * Z_{P2}} * \sin(\beta) \tag{6.10}$$

The diode specifications required for the T-phase shifter were defined by evaluating a simplified T-network with the help of the above equations. In Fig.6.16, the left Y-axis shows the phase shift versus capacitance. As the capacitance increases from 10 fF to 100 fF, the signal received at port-2 will have a leading phase from -165° to -70° with almost linear bias dependent characteristics. This suggests that a 45° phase shift requires a capacitance change of about 45 fF. Assuming a port impedance of 50 Ω , the required shunt inductor can also be calculated and is plotted in the right Y-axis of Fig.6.16. The corresponding variation of the inductance versus capacitance manifests that a capacitance between 10 fF to 30 fF will lead to mismatch. A constant inductance value when the capacitance is beyond 40 fF is thus of interest for designing a matched T-Phase shifter.

Considering the diode capacitance of various diode diameter sizes between 7.5 µm and 12.5 µm as redrawn in Fig.6.17 indicates that the diode diameter matching the requirement best is 12.5 µm, which corresponds to a capacitance variation from 45 fF to 100 fF.

The study allowed to determine a suitable geometry and capacitance providing the desired 45° phase shift at 35 GHz. The diodes were characterized on-wafer with a VNA up to 50 GHz and their equivalent circuit was extracted by numerical fitting after de-embedding. This allowed to obtain information on the intrinsic elements, such as junc-

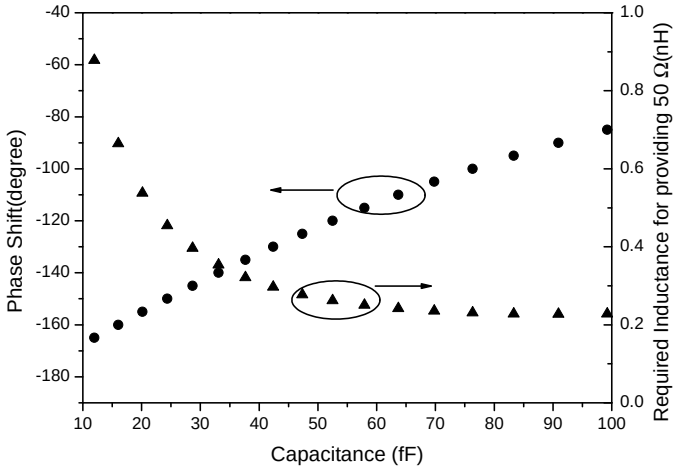


Figure 6.16: Phase shift of the high-pass T-network and the corresponding inductance for 50 Ω impedance matching

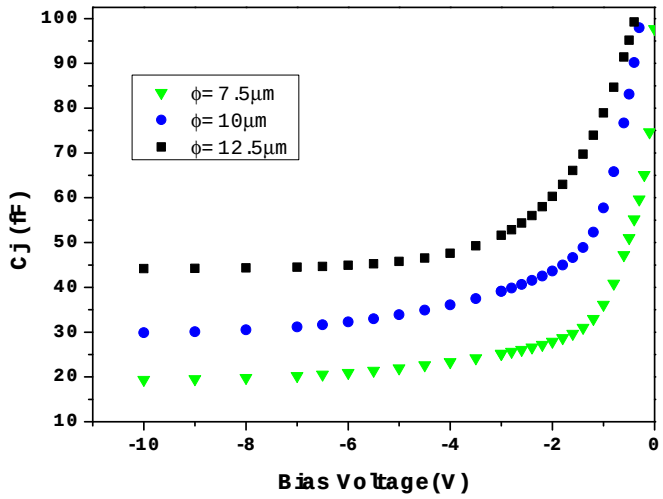


Figure 6.17: Extracted junction capacitance of the GaN Schottky diodes

tion capacitance C_j and series resistance R_s. The extracted capacitance of different diameter devices is shown in Fig.6.17.

Beyond a certain negative bias voltage, the capacitance changes only slightly with bias voltage. This determines the minimum value of junction capacitance which corresponds to maximum depletion of the N^- layer. Larger diameter diodes led in general to a larger difference between the minimum and maximum capacitance values. Capacitance ratios up to 3:1 were possible. The absolute value of capacitance variation is of prime importance for the resulting circuit characteristics as will be discussed below. The breakdown voltage of GaN-diodes of this type can exceed 40V permitting robust operation in the presence of high power RF signals.

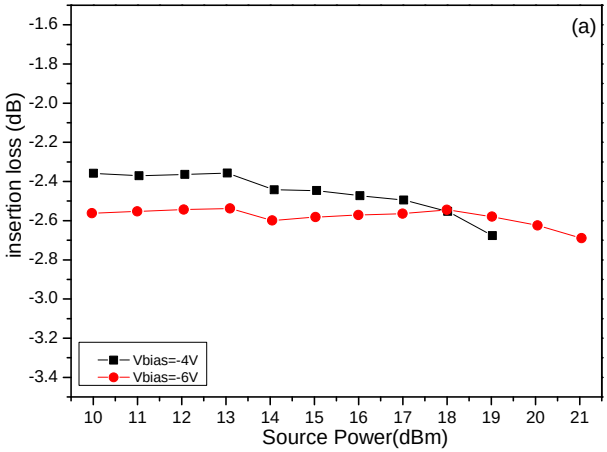
Diode Properties and Modeling

The Equivalent Circuit (EC) model of the 12.5 μm diode was extracted in the same way as described earlier in section 6.1. The junction capacitance was fitted to an exponential function of bias voltages in the form of $44.15 + 1.81\exp[(v + 4.85)/1.3]$, which was found to represent the diode characteristics better than the initially obtained results using a SPICE model. The series and junction resistance of the diode were 12.5 Ω and 10 kΩ respectively.

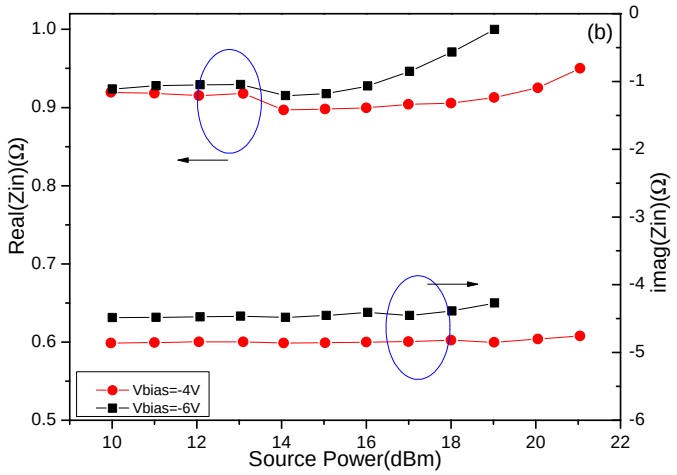
The high-frequency large signal characteristics of the diodes were measured to permit an estimate of the T-Phase Shifter power handling performance. The voltage and current on each node of the GaN diode were measured simultaneously with the help of the large signal network analyzer (LSNA), which permitted characterization at 14 GHz with the help of a power amplifier delivering up to 23 dBm at this frequency. The diode was placed in series between a 50 Ω source and load and the insertion loss was measured by sweeping the source power from 10 dBm to 21 dBm for various Schottky diode bias values. As shown in Fig.6.18(a), the insertion loss for such a diode is $\sim$ 2.5 dB, and remains very little influenced by the increased level of power incident to it. Fig.6.18(b) shows that the resistive and reactive part of the diode impedance are also not significantly affected when operated under large-signal conditions.

Phase Shifter Simulation

Having the diodes selected, the inductance needs to be adjusted in order to obtain low insertion loss and good matching. A first pass circuit simulation with a lumped inductor having ideal characteristics shows that an inductance of 0.4 nH would be appropriate. Then several inductor layouts were simulated using Momentum, the electromagnetic simulator of ADS. The resulted inductor design is shown in Fig.5. The target inductance was achieved with a 1.5 turn spiral inductor where the outer turn length, line width and

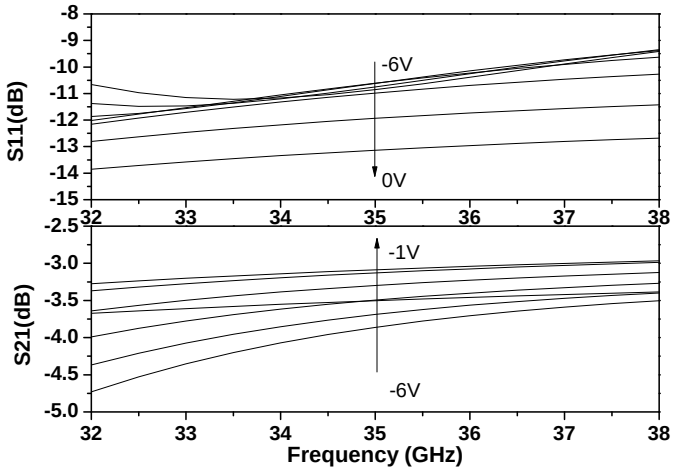


(a) insertion loss

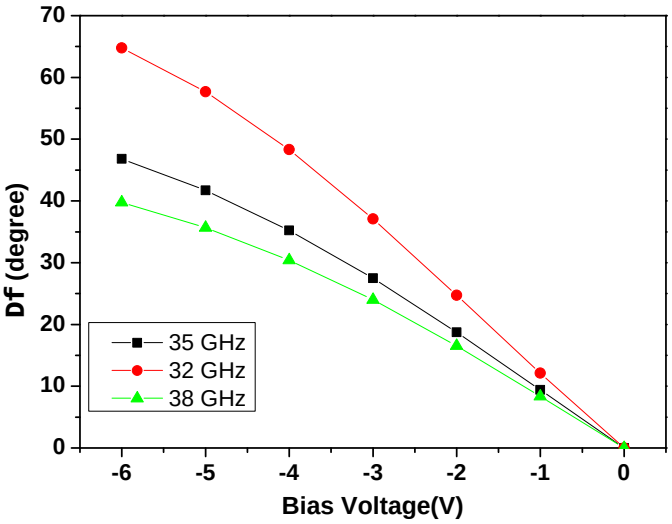


(b) impedance

Figure 6.18: Measured single diode insertion loss and its impedance under large-signal driven conditions



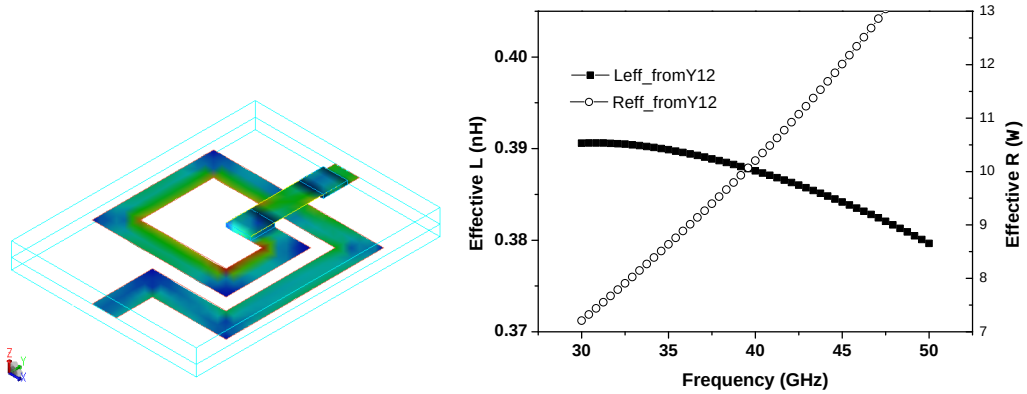
(a) return loss and insertion loss



(b) phase shift

Figure 6.19: Simulated results of GaN T-phase shifter performance based on experimentally obtained characteristics of the Schottky diodes in the frequency range of 32 GHz to 38 GHz

space are 130 µm, 15 µm and 10 µm. The inductance was found to be frequency dependent, and varies from 0.36 nH at 35 GHz to 0.45 nH at 45 GHz. The estimated resistance is about 10 Ω.



(a) schematic of inductor model (b) inductor properties

Figure 6.20: Inductor layout used for the T-Phase shifter and simulation of the frequency dependence of its effective equivalent circuit characteristics

The results obtained for the input reflection coefficient and transmission of the phase shifter circuit are shown in Fig.6.19 as a function of frequency. The insertion loss (IL) varies from 3 to 4.2 dB at 35 GHz over the entire T-Phase Shifter bias range of -6 V to 0 V. The insertion loss remains constant at higher frequencies but increases in the lower frequency range. This is due to the high-pass nature of the circuit topology. The input return loss varies from -9 to -15 dB. The phase difference for an input at 35 GHz can be tuned from 98° to 52° with a bias voltage from -6 V to 0 V, resulting in a phase tuning of 45°.

MMIC fabrication and measurements

Fig.6.21 shows the photograph of the realized phase shifter circuit, fabricated using the developed technology described in chapter 3. The passive components were realized in the same step as the interconnection lines, thus no additional fabrication step was required for that.

The fabricated phase shifters were characterized by a VNA up to 50 GHz. The applied bias voltage was varied from 0 V to -6 V with a 0.5 V step. As shown in Fig.6.22, the maximum VSWR is ∼2:1 in the frequency range of 32 GHz to 38 GHz.The insertion loss of the phase shifter varied between -6.5 dB and -8.5 dB depending on bias voltage. The increased insertion loss compared with the value expected based on discrete diode characteristics was attributed to increased ohmic contact resistance of the fabricated MMICs.

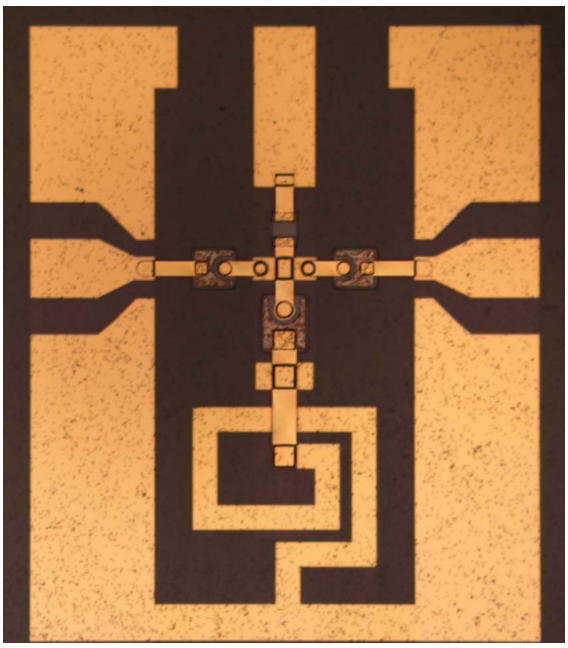


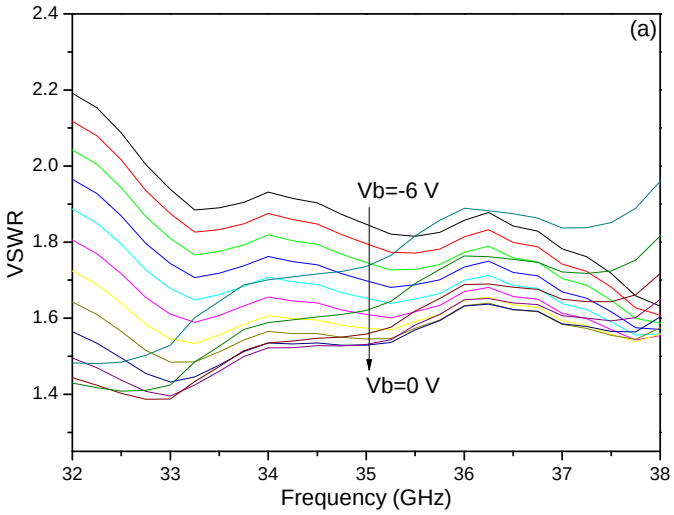
Figure 6.21: Microscope photograph of the fabricated T-Phase shifter MMIC

The phase tuning range versus bias voltage is shown in Fig.6.23, where a phase shift at 0 V was used as reference. The experimentally achieved phase tuning range decreased with frequency and was 45° at 32 GHz, 38° at 35 GHz and 33° at 38 GHz.

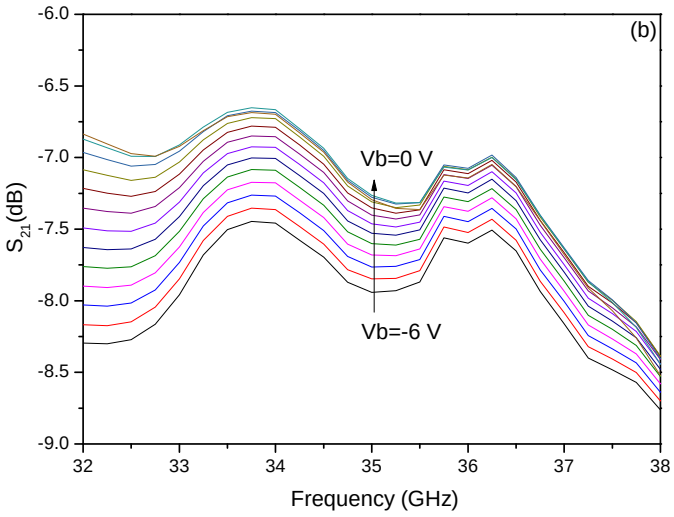
The insertion loss characteristics of the T-phase shifter were investigated next by considering the loss characteristics of the experimentally characterized discrete diodes. As discussed earlier their minimum loss at 14 GHz was 2.5 dB accounting therefore for almost the total loss of 7 dB at 35 GHz in the MMIC under study that had two diodes connected in series. The remaining loss was attributed to the shunt connected diode. Further improvement in insertion loss can be expected by epi-layer optimization and processing.

Considering the large breakdown of wide bandgap semiconductor materials such as GaN used here, one can develop more robust phase shifter modules than with materials such as GaAs. The device simulation results discussed in chapter 2 showed a breakdown voltage of more than 100 V versus less than 15 V for GaN and GaAs respectively using the same device structure (i.e. 300 nm $1 \times 10^{17} cm^{-3}$ doped N^- and 1 µm $3 \times 10^{18} cm^{-3}$ doped N^+). Even if the GaN breakdown voltages in practice only half the simulated value, the power handling of GaN Schottky T-Phase shifters can be up to 10 dB higher than in case of GaAs MMICs of the same topology.

With the equivalent circuit model of the designed phase shifter, large signal simulation was performed using harmonic balance at 35 GHz. As shown in Fig.6.24, the input return loss and insertion loss remain almost the same as in the small signal case for input power levels up to 26 dBm for the selected diode size. The phase tuning range is also



(a) VSWR



(b) Transmission

Figure 6.22: Measured phase shifter reflection and transmission characteristics

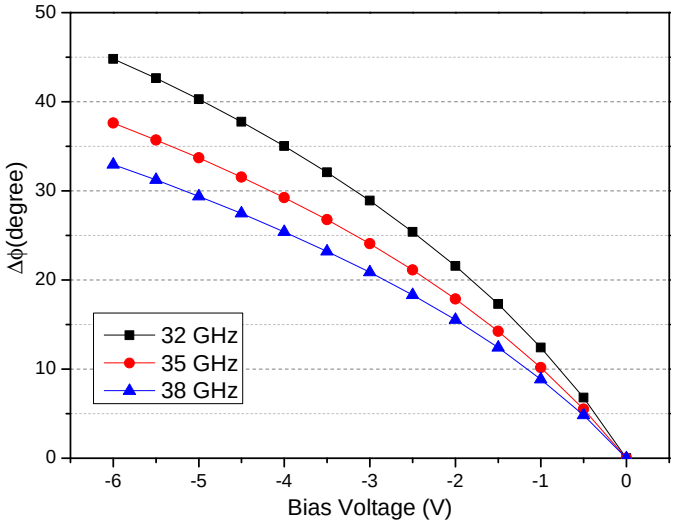


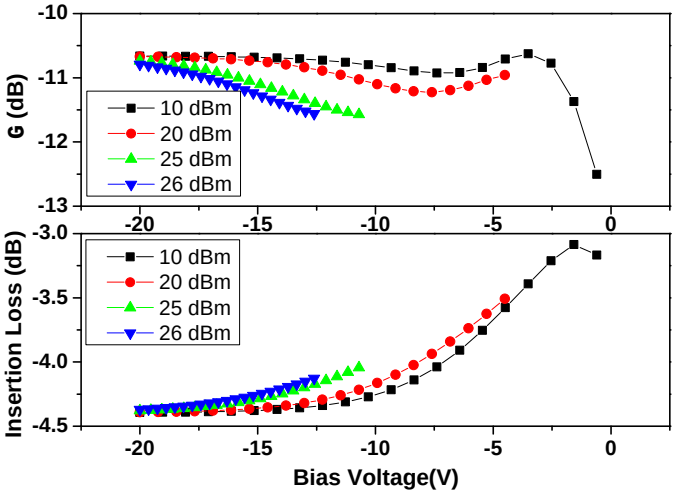
Figure 6.23: Measured phase tuning range $\Delta\phi$ vs. bias

not changing significantly but appears to be more affected than the return loss of the reflection coefficient. The results are plotted here as a function of bias voltage applied to the circuit for phase shifting and are presented up to bias voltages that lead in a combined DC-HF amplitude not exceeding a large DC window that may extend from 0.3 V up to -40 V. The obtained characteristics highlight the weak impact of input power on the T-Phase shifter performance. This is expected to be less limiting in practice due to the instantaneous in nature HF amplitude.

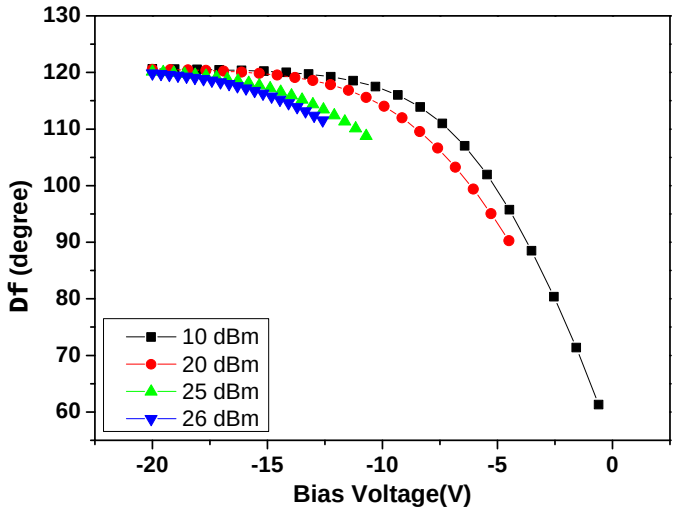
The small and large-signal characterized GaN Schottky diodes with a 12.5 μm diameter were used for designing and fabricating an analog Phase-Shifter MMIC in T-configuration. The circuit contained two series connected diodes and another diode in the shunt arm which is connected to a spiral inductor for an operation frequency of 35 GHz. A phase shift of 45° and insertion loss about 7 dB were obtained. The highly robust characteristics shown by the results benefit from the superior breakdown voltage of GaN-based technology and present an improvement of up to 10 dB in power handling compared with similar circuits fabricated using traditional III-V technology.

6.4 Conclusion

Two circuit applications of the GaN Schottky diodes were presented in this chapter, based on the developed diode large-signal model. After reviewing the methods of large-signal modeling an equivalent circuit approach was employed for circuit design. Key aspects of the diode large signal modeling were discussed in detail. A 10 μm diode has been evaluated as single-diode frequency doubler at 94 GHz and the results showed the potential of GaN Schottky diodes for signal generation by frequency multiplication. A phase shifter



(a) loss and Γ



(b) phase

Figure 6.24: Simulated large signal characteristics of the designed phase shifter

MMIC was designed, fabricated and tested. The design procedure was discussed to reveal how the phase shifter features are correlated with the diode capacitance and thus the way of selecting the appropriate diode geometry and characteristics. Simulation results based on large-signal modeling were presented and measurement results confirmed the validity of the design.

7 Conclusions and future work

This thesis focused on GaN-based Schottky varactor diodes for signal generation and control. Several aspects of this topic were covered, including theoretical design and simulation, fabrication technologies, characterization approaches and circuit applications. Conclusions were drawn for each aspect and suggestions for future work are also given.

7.1 Theoretical prediction

Conclusions

A comprehensive study was carried out both analytically and numerically to evaluate the high power handling potential of GaN Schottky diodes. The diode analysis was based on the assumption of a constant doping epi-layer, the C-V characteristics of which correspond to the inverse square power function of voltage. This assumption simplifies the study and allows to calculate the power handling capability, losses and nonlinearity with the help of rather simple equations. The obtained equations can also be used to define the diode specifications for given power handling requirement.

Simulations based on a commercially available semiconductor device software were performed to evaluate the perspectives of GaN Schottky diodes. These included static, small-signal AC and transient analysis. Important material parameters and physical models were described in detail and used for the prediction of diode performance. The temperature dependence of the parameters and models were utilized to evaluate the diode performance at elevated temperature by iso-thermal simulation. The breakdown voltage, I-V, C-V and power characteristics resulting from transient analysis were obtained. These results were presented in the same way that the GaAs-based diode features are described and allowed demonstration of the advantages of GaN-based diodes in terms of power handling.

Future work

The simulation studies suggest that certain advantages can be expected by employing diode structures other than those with constant doping described in the study. Future

designs could have exponentially doped carrier-distance from the surface profiles or employ heterojunctions. Both these types are expected to provide rich nonlinearity and signal conversion efficiency due to their strong C-V nonlinearity.

Thermal-electrical simulation is more attractive than iso-thermal simulation for estimating the diode performance under operation conditions. Given the fact that such a diode often operates under strong self-heating, thermal dissipation is an important factor to be considered in studies of this type.

The simulations performed above were based on theoretical material properties. By way of an example, the mobility used was obtained from Monte-Carlo simulation results. The experimentally realized GaN Schottky diodes behave far from the simulated ideal case. Proper physical models accounting for these non-ideal effects would be beneficial for matching the experimental results, hence providing results close to realistic device performance. As an example, phonon assistant tunneling was found to account for the leakage in practical Schottky diodes [90]. The modeled equations have been implemented in Silvaco and allowed to represent the leakage current close to the characteristics observed in practice.

Device co-simulation with a nonlinear circuit simulator is also of interest. The device simulation discussed earlier lacks the capability of predicting the diode performance in a circuit with embedded RF impedances. Using a nonlinear circuit simulator to evaluate the impact of embedded networks, which is normally done in the frequency domain, the voltage and current presented at the diode can be found. The diode can then be simulated in the time domain by the obtained stimulus. Such a co-simulation framework has been demonstrated by an in-house CAD software [91].

7.2 Fabrication technologies

Conclusions

Three different technology approaches were explored and demonstrated to be successful for GaN Schottky diodes and MMIC fabrication. The realized low resistivity Ohmic contacts, evaporation based Pt Schottky contacts, as well as access interconnects for high-frequency characterization allowed the realization of good quality GaN diodes for characterization and analysis.In particular, the obtained Ohmic contact resistivity was $3 \times 10^{-6}\,\Omega \cdot \mathrm{cm}^2$, which allows the diode to operate in high-frequency with low loss; the barrier height achieved by evaporated Pt contacts was ~ 1 eV, which would be beneficial for an extended capacitance modulation range; the realized access interconnect bridge allowed to contact the diodes in a satisfactory way despite the $2\ \mu\mathrm{m}$ height difference between the anode and the substrate. The above deployments can be easily employed for the realization of other GaN device types.

Future work

Future technology work should include further improvement of the Schottky contact quality and demonstration of novel epi-structures. Good Schottky quality in terms of high barrier height, low leakage currents are key features for successful use of Schottky diodes in circuits and thus it's worth attempting to obtain better characteristics. These may be based on the use of other high work function metals, electroplating of Schottky metal, atomic layer deposition (ALD) of Schottky metal and advanced surface treatment prior to metal deposition.

The experiments performed in this study were mainly based on epitaxially grown layers on Sapphire substrates. Better performance is expected from diodes fabricated on a homoepitaxial GaN wafer due to its good crystal quality. However, GaN substrates necessary for homoepitaxial purposes are normally highly conductive. Fabrication of access interconnection lines suitable for high-frequency measurement on such a conductive substrate is challenging. One possible approach would be to utilize a Coplanar Waveguide lines deposited on the SiO_2 dielectric layer[92]. A first attempt was made in this direction and reported by the author[93].

7.3 Characterization approaches

Conclusions

The characterization studies made in this thesis includes both small-signal and large-signal approaches. The measured small-signal S-parameters were used to extract information of the intrinsic diode characteristics. This was possible using a well defined procedure which involves de-embedding of the parasitics followed by obtaining the intrinsic elements C_j, R_s and R_j. R_s by optimization. R_s was found to be significantly bias dependent, which is a special feature of GaN diodes.

On-wafer large-signal measurements based on Large-Signal Network Analyzer (LSNA) were used for the first time to study the varactor diode characteristics. The obtained results allowed understanding of the large-signal operation of the diodes, which would otherwise not have been possible with other approaches.

Future work

A key step in C_j extraction from small-signal S-parameters is the assumption of an inverse square power function of voltage i.e. grading factor of 0.5 in Eq.4.5, for its representation. In order o extend the use of this procedure it is necessary to evaluate such a grading factor for other structures such as for example, Schottkys on AlGaN/GaN heterojunction and exponentially doped structures. This implies that the application of the

reported procedure is limited to constant doping structures while other constraints have to overcome and applied in case of heterostrucutres and exponential doping profiles.

For the direct application of LSNA in characterizing a single diode as frequency doubler, integrated filters would be beneficial for allowing input and output signal isolation. For wafers on Sapphire substrate, Coplanar Waveguide stubs are preferred for easy grounding. Such a configuration would ease the behavior modeling of the diode chip and lead to a faster evaluation of diode performance for frequency doubling.

7.4 Circuit applications

Conclusions

The potential of GaN Schottky diodes for frequency doublers has been demonstrated by circuit simulation, which was performed based on the developed large-signal model. A phase shifter MMIC was also simulated based also on the same large-signal model, and experimentally evaluated. The modeling and circuit design methodologies demonstrated in this study indicate the feasibility of achieving circuits operating at higher frequency and high power levels.

Future work

MMICs such as the ones discussed in this study require strip metal lines and other lumped or distributed passive components. The development of Electro-Magnetic (EM) simulation tools allows to predict the characteristics of such components with better accuracy. This can help improving the predictions of passive component prediction leading to performance that matches better the predicted characteristics. Integrated filters and matching circuits for the doubler studied in this thesis and spiral inductor used in the phase shifter can profit from such studies. 3D interconnects, metal-dielectric stacks for realizations on conductive substrates could be other aspects of future studies.

Bibliography

[1] Peter H Siegel. Thz instruments for space. *Antennas and Propagation, IEEE Transactions on*, 55(11):2957–2965, 2007.

[2] `http://www.almaobservatory.org/en/about-alma/how-does-alma-work/technology/front-end`.

[3] G. Ducournau, Y. Yoshimizu, S. Hisatake, F. Pavanello, E. Peytavit, M. Zaknoune, T. Nagatsuma, and J.-F. Lampin. Coherent thz communication at 200 ghz using a frequency comb, utc-pd and electronic detection. *Electronics Letters*, 50(5):386–388, Feb 2014.

[4] Goutam Chattopadhyay. Technology, capabilities, and performance of low power terahertz sources. *Terahertz Science and Technology, IEEE Transactions on*, 1(1):33–53, 2011.

[5] Masayoshi Tonouchi. Cutting-edge terahertz technology. *Nature photonics*, 1(2):97–105, 2007.

[6] C.M. Armstrong. The truth about terahertz. *Spectrum, IEEE*, 49(9):36–41, September 2012.

[7] Mikko Kotiranta. *Development of Terahertz Vacuum Electronics for Array Receivers*. PhD thesis, Johann WolfGaNg Goethe University, http://d-nb.info/1044609508, 2013.

[8] A. Maestrini, I. Mehdi, J.V. Siles, J.S. Ward, R. Lin, B. Thomas, Choonsup Lee, J. Gill, G. Chattopadhyay, E. Schlecht, J. Pearson, and P. Siegel. Design and characterization of a room temperature all-solid-state electronic source tunable from 2.48 to 2.75 thz. *Terahertz Science and Technology, IEEE Transactions on*, 2(2):177–185, March 2012.

[9] Jaime A Alvarez, F Patricio Mena, Josip Vukusic, Jan Stake, Ernest A Michael, et al. Vertically illuminated tw-utc photodiodes for terahertz generation. In *SPIE Astronomical Telescopes+ Instrumentation*, pages 84522I–84522I. International Society for Optics and Photonics, 2012.

[10] I Cámara Mayorga, Andreas Schmitz, Thomas Klein, Christian Leinz, and R Gusten. First in-field application of a full photonic local oscillator to terahertz astronomy. *Terahertz Science and Technology, IEEE Transactions on*, 2(4):393–399, 2012.

[11] John S Ward, Goutam Chattopadhyay, John Gill, Hamid Javadi, Choonsup Lee, Robert Lin, Alain Maestrini, Frank Maiwald, Imran Mehdi, Erich Schlecht, et al. Tunable broadband frequency-multiplied terahertz sources. In *Infrared, Millimeter and Terahertz Waves, 2008. IRMMW-THz 2008. 33rd International Conference on*, pages 1–3. IEEE, 2008.

[12] Kamaljeet S. Saini. Development of frequency multiplier technology for alma. `http://www.alma.nrao.edu/memos/html-memos/alma337/memo337.pdf`.

[13] Suzanne Martin, Barbara Nakamura, Andy Fung, Peter Smith, Jean Bruston, Alain Maestrini, Frank Maiwald, Peter Siegel, Erich Schlecht, and Imran Mehdi. Fabrication of 200 to 2700 ghz multiplier devices using gaas and metal membranes. In *Microwave Symposium Digest, 2001 IEEE MTT-S International*, volume 3, pages 1641–1644. IEEE, 2001.

[14] Alain Maestrini, John Ward, Goutam Chattopadhyay, Erich Schlecht, and Imran Mehdi. Terahertz sources based on frequency multiplication and their applications. *Frequenz*, 62(5-6):118–122, 2008.

[15] J.V. Siles, A. Maestrini, B. Alderman, S. Davies, Hui Wang, J. Treuttel, E. Leclerc, T. Narhi, and C. Goldstein. A single-waveguide in-phase power-combined frequency doubler at 190 ghz. *Microwave and Wireless Components Letters, IEEE*, 21(6):332–334, June 2011.

[16] Aik Yean Tang, Erich Schlecht, Robert Lin, Goutam Chattopadhyay, Choonsup Lee, John Gill, Imran Mehdi, and Jan Stake. Electro-thermal model for multi-anode schottky diode multipliers. *Terahertz Science and Technology, IEEE Transactions on*, 2(3):290–298, 2012.

[17] Choonsup Lee, John Ward, Robert Lin, Erich Schlecht, G Chattopadhyay, John Gill, Bertrand Thomas, A Maestrini, Imran Mehdi, and Peter Siegel. A wafer-level diamond bonding process to improve power handling capability of submillimeter-wave schottky diode frequency multipliers. In *Microwave Symposium Digest, 2009. MTT'09. IEEE MTT-S International*, pages 957–960. IEEE, 2009.

[18] Alain Maestrini, Imran Mehdi, Robert Lin, José Vicente Siles, Choonsup Lee, John Gill, Goutam Chattopadhyay, Erich Schlecht, Thomas Bertrand, and John Ward. A 2.5-2.7 thz room temperature electronic source. In *Proc. 22nd International Symposium on Space Terahertz Technology*.

[19] Alain Maestrini, John S Ward, John J Gill, Choonsup Lee, Bertrand Thomas, Robert H Lin, Goutam Chattopadhyay, and Imran Mehdi. A frequency-multiplied source with more than 1 mw of power across the 840–900-ghz band. *Microwave Theory and Techniques, IEEE Transactions on*, 58(7):1925–1932, 2010.

[20] José V Siles and Jesús Grajal. Capabilities of GaN schottky multipliers for lo power generation at millimeter-wave bands. In *Proc. 19th International Symposium on Space Terahertz Technology*, pages 504–507, 2008.

[21] Koichi Momma and Fujio Izumi. *VESTA3* for three-dimensional visualization of crystal, volumetric and morphology data. *Journal of Applied Crystallography*, 44(6):1272–1276, Dec 2011.

[22] M.S Shur, R Gaska, and A Bykhovski. Gan-based electronic devices. *Solid-State Electronics*, 43(8):1451 – 1458, 1999.

[23] IOFFE. Gallium nitride band structure and carrier concentration. `http://www.ioffe.ru/SVA/NSM/Semicond/GaN/bandstr.html`.

[24] EL Kolberg, TJ Tolmunen, Margaret A Frerking, and Jack R East. Current saturation in submillimeter-wave varactors. *Microwave Theory and Techniques, IEEE Transactions on*, 40(5):831–838, 1992.

[25] C Mion, JF Muth, EA Preble, and D Hanser. Accurate dependence of gallium nitride thermal conductivity on dislocation density. *Applied physics letters*, 89(9):092123–092123, 2006.

[26] Yuanzheng Yue, Zongyang Hu, Jia Guo, B. Sensale-Rodriguez, Guowang Li, Ronghua Wang, F. Faria, Tian Fang, Bo Song, Xiang Gao, Shiping Guo, T. Kosel, G. Snider, P. Fay, Debdeep Jena, and Huili Xing. Inaln/aln/GaN hemts with regrown ohmic contacts and f_T of 370 ghz. *Electron Device Letters, IEEE*, 33(7):988–990, July 2012.

[27] D.F. Brown, A. Williams, K. Shinohara, A. Kurdoghlian, I. Milosavljevic, P. Hashimoto, R. Grabar, S. Burnham, C. Butler, P. Willadsen, and M. Micovic. W-band power performance of AlGaN/GaN dhfets with regrown n+ GaN ohmic contacts by mbe. In *Electron Devices Meeting (IEDM), 2011 IEEE International*, pages 19.3.1–19.3.4, Dec 2011.

[28] M. Micovic, A. Kurdoghlian, H.P. Moyer, P. Hashimoto, M. Hu, M. Antcliffe, P.J. Willadsen, W.-S. Wong, R. Bowen, I. Milosavljevic, Y. Yoon, A. Schmitz, M. Wetzel, C. McGuire, B. Hughes, and D.H. Chow. GaN mmic pas for e-band (71 ghz - 95 ghz) radio. In *Compound Semiconductor Integrated Circuits Symposium, 2008. CSIC '08. IEEE*, pages 1–4, Oct 2008.

[29] A Fung, J Ward, G Chattopadhyay, R Lin, L Samoska, P Kangaslahti, I Mehdi, B Lambrigtsen, P Goldsmith, M Micovic, et al. Power combined gallium nitride amplifier with 3 watt output power at 87 ghz. In *proc. of the Intl. Symposium on Space THz Technology*, 2011.

[30] James Schellenberg, E. Watkins, M. Micovic, Bumjin Kim, and Kyu Han. W-band, 5w solid-state power amplifier/combiner. In *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, pages 240–243, May 2010.

[31] A.K. Panda, G. N. Dash, N. C. Agrawal, and R.K. Parida. Studies on the characteristics of GaN-based gunn diode for thz signal generation. In *Microwave Conference, 2009. APMC 2009. Asia Pacific*, pages 1565–1568, Dec 2009.

[32] O. Yilmazoglu, K. Mutamba, D. Pavlidis, and T. Karaduman. First observation of bias oscillations in GaN gunn diodes on GaN substrate. *Electron Devices, IEEE Transactions on*, 55(6):1563–1567, June 2008.

[33] JM Manley and HE Rowe. Some general properties of nonlinear elements-part i. general energy relations. *Proceedings of the IRE*, 44(7):904–913, 1956.

[34] R.H. Pantell. General power relationships for positive and negative nonlinear resistive elements. *Proceedings of the IRE*, 46(12):1910–1913, Dec 1958.

[35] Paul Penfield and Robert P Rafuse. *Varactor applications*. MIT Press, 1962.

[36] GE Dunaevskii and VI Perfil'ev. Analysis and synthesis of varactor frequency doublers. part 1. basic relationships. *Russian Physics Journal*, 52(10):1052–1059, 2009.

[37] Seng-Woon Chen, T.C. Ho, K. Pande, and P.D. Rice. Rigorous analysis and design of a high-performance 94 GHz MMIC doubler. *Microwave Theory and Techniques, IEEE Transactions on*, 41(12):2317–2322, Dec 1993.

[38] Joseph A. Calviello. Advanced devices and components for the millimeter and submillimeter systems. *Electron Devices, IEEE Transactions on*, 26(9):1273–1281, Sep 1979.

[39] J. Wu, W. Walukiewicz, K. M. Yu, J. W. Ager, E. E. Haller, Hai Lu, William J. Schaff, Yoshiki Saito, and Yasushi Nanishi. Unusual properties of the fundamental band gap of inn. *Applied Physics Letters*, 80(21):3967–3969, 2002.

[40] M. Farahmand, Carlo Garetto, E. Bellotti, Kevin F. Brennan, M. Goano, E. Ghillino, G. Ghione, J.D. Albrecht, and P. Paul Ruden. Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: binaries and ternaries. *Electron Devices, IEEE Transactions on*, 48(3):535–542, Mar 2001.

[41] *ATLAS User's Manual*. Silvaco Int. Santa Clara, CA, 2012.

[42] Meikei Ieong, P.M. Solomon, S.E. Laux, H.-S.P. Wong, and D. Chidambarrao. Comparison of raised and schottky source/drain mosfets using a novel tunneling contact model. In *Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International*, pages 733–736, Dec 1998.

[43] Kyushik Hong, P.F. Marsh, Geok-Ing Ng, D. Pavlidis, and Chang-Hee Hong. Optimization of MOVPE grown $in_xal_{1-x}as/in_{0.53}ga_{0.47}as$ planar heteroepitaxial schottky diodes for terahertz applications. *Electron Devices, IEEE Transactions on*, 41(9):1489–1497, Sep 1994.

[44] S.J. Pearton, J.C. Zolper, R.J. Shul, and F. Ren. GaN: Processing, defects, and devices. *Journal of Applied Physics*, 86(1):1–78, Jul 1999.

[45] `http://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition`.

[46] SEO Sanghyun, Kaustav Ghose, Guang Yuan Zhao, and Dimitris Pavlidis. Aln/GaN metal insulator semiconductor field effect transistor on sapphire substrate. *IEICE transactions on electronics*, 91(7):994–1000, 2008.

[47] M. Faucher, Bertrand Grimbert, Y. Cordier, Nicolas Baron, Arnaud Wilk, Hacene Lahreche, Philippe Bove, Marc Francois, Pascal Tilmant, T. Gehin, Christiane Legrand, M. Werquin, Lionel Buchaillot, C. Gaquiere, and Didier Theron. Amplified piezoelectric transduction of nanoscale motion in gallium nitride electromechanical resonators. *Applied Physics Letters*, 94(23):233506–233506–3, Jun 2009.

[48] Joon Seop Kwak, S E Mohney, Je-Yi Lin, and R S Kern. Low resistance al/ti/n-GaN ohmic contacts with improved surface morphology and thermal stability. *Semiconductor Science and Technology*, 15(7):756, 2000.

[49] Christopher M Pelto, Y Austin Chang, Yong Chen, and R Stanley Williams. Issues concerning the preparation of ohmic contacts to n-GaN. *Solid-State Electronics*, 45(9):1597–1605, 2001.

[50] B. Van Daele, G. Van Tendeloo, W. Ruythooren, J. Derluyn, M.R. Leys, and M. Germain. The role of al on ohmic contact formation on n-type GaN and AlGaN/GaN. *Applied Physics Letters*, 87(6):061905–061905–3, Aug 2005.

[51] N. Miura, T. Oishi, T. Nanjo, Muneyoshi Suita, Yuji Abe, T. Ozeki, Hiroyasu Ishikawa, and T. Egawa. Effects of interfacial thin metal layer for high-performance pt-au-based schottky contacts to AlGaN-GaN. *Electron Devices, IEEE Transactions on*, 51(3):297–303, March 2004.

[52] Jin-Ping Ao, D. Kikuta, N. Kubota, Y. Naoi, and Y. Ohno. Copper gate AlGaN/GaN hemt with low gate leakage current. *Electron Device Letters, IEEE*, 24(8):500–502, Aug 2003.

[53] Neung-Hee Lee, Minseong Lee, Woojin Choi, Donghwan Kim, Namcheol Jeon, Seonhong Choi, and Kwang-Seok Seo. Effects of various surface treatments on gate leakage, subthreshold slope, and current collapse in AlGaN/GaN high-electron-mobility transistors. *Japanese Journal of Applied Physics*, 53(4S):04EF10, 2014.

[54] P Kordoš, J Bernàt, D Gregušovà, M Marso, and H Lűth. Impact of surface treatment under the gate on the current collapse of unpassivated AlGaN/GaN heterostructure field-effect transistors. *Semiconductor Science and Technology*, 21(1):67, 2006.

[55] K Suzue, S Noor Mohammad, ZF Fan, W Kim, O Aktas, AE Botchkarev, and H Morkoç. Electrical conduction in platinum–gallium nitride schottky diodes. *Journal of applied physics*, 80(8):4467–4478, 1996.

[56] P Hacke, T Detchprohm, K Hiramatsu, and N Sawaki. Schottky barrier on n-type GaN grown by hydride vapor phase epitaxy. *Applied physics letters*, 63(19):2676–2678, 1993.

[57] Chul Huh, Sang-Woo Kim, Hyun-Soo Kim, In-Hwan Lee, and Seong-Ju Park. Effective sulfur passivation of an n-type GaN surface by an alcohol-based sulfide solution. *Journal of Applied Physics*, 87(9):4591–4593, May 2000.

[58] Rongming Chu, L. Shen, N. Fichtenbaum, D. Brown, Stacia Keller, and Umesh K. Mishra. Plasma treatment for leakage reduction in AlGaN/GaN and GaN schottky contacts. *Electron Device Letters, IEEE*, 29(4):297–299, April 2008.

[59] Yuanping Sun, X M Shen, J Wang, D G Zhao, G Feng, Y Fu, S M Zhang, Z H Zhang, Z H Feng, Y X Bai, and Hui Yang. Thermal annealing behaviour of ni/au on n-GaN schottky contacts. *Journal of Physics D: Applied Physics*, 35(20):2648, 2002.

[60] JD Guo, FM Pan, MS Feng, RJ Guo, PF Chou, and CY Chang. Schottky contact and the thermal stability of ni on n-type GaN. *Journal of applied physics*, 80(3):1623–1627, 1996.

[61] Jun Wang, D G Zhao, Y P Sun, L H Duan, Y T Wang, S M Zhang, Hui Yang, Shengqiang Zhou, and Mingfang Wu. Thermal annealing behaviour of pt on n-GaN schottky contacts. *Journal of Physics D: Applied Physics*, 36(8):1018, 2003.

[62] Wei Lu, Siyuan Gu, DPR Aplin, DM Estrada, PKL Yu, PM Asbeck, et al. Analysis of reverse leakage current and breakdown voltage in GaN and inGaN/GaN schottky barriers. *Electron Devices, IEEE Transactions on*, 58(7):1986–1994, 2011.

[63] Yong Lei, Hai Lu, Dongsheng Cao, Dunjun Chen, Rong Zhang, and Youdou Zheng. Reverse leakage mechanism of schottky barrier diode fabricated on homoepitaxial GaN. *Solid-State Electronics*, 82:63–66, 2013.

[64] Jianjun Gao. *RF and microwave modeling and measurement techniques for field effect transistors*. SciTec, 2010.

[65] Aik Yean Tang, V. Drakinskiy, K. Yhland, J. Stenarson, T. Bryllert, and J. Stake. Analytical extraction of a schottky diode model from broadband s-parameters. *Microwave Theory and Techniques, IEEE Transactions on*, 61(5):1870–1878, May 2013.

[66] Jyrki T. Louhi and A.V. Raisanen. On the modeling and optimization of schottky varactor frequency multipliers at submillimeter wavelengths. *Microwave Theory and Techniques, IEEE Transactions on*, 43(4):922–926, Apr 1995.

[67] Andrei Grebennikov. High-efficiency power amplifiers: Turning the pages of forgotten history. *High Frequency Electronics*, 7:18–26, 2008.

[68] W. Van Moer and L. Gomme. Nvna versus lsna: enemies or friends? *Microwave Magazine, IEEE*, 11(1):97–103, Feb 2010.

[69] J. Verspecht and D.E. Root. Polyharmonic distortion modeling. *Microwave Magazine, IEEE*, 7(3):44–57, June 2006.

[70] Fadhel M Ghannouchi and Mohammad S Hashmi. *Load-pull techniques with applications to power amplifier design*, volume 32. Springer, 2012.

[71] D. Barataud, F. Blache, A. Mallet, P.P. Bouysse, J.-M. Nebus, J.P. Villotte, J. Obregon, J. Verspecht, and P. Auxemery. Measurement and control of current/voltage waveforms of microwave transistors using a harmonic load-pull system for the optimum design of high efficiency power amplifiers. *Instrumentation and Measurement, IEEE Transactions on*, 48(4):835–842, Aug 1999.

[72] K. Vandermot, W. Van Moer, Johan Schoukens, and Y. Rolain. Understanding the nonlinearity of a mixer using multisine excitations. In *Instrumentation and Measurement Technology Conference, 2006. IMTC 2006. Proceedings of the IEEE*, pages 1205–1209, April 2006.

[73] Jan Verspecht, Frans Verbeyst, Marc Vanden Bossche, et al. Large-signal network analysis : Going beyond s-parameters. In *62nd ARFTG Conference digest*, 2003.

[74] P.J. Tasker and J. Benedikt. Waveform inspired models and the harmonic balance emulator. *Microwave Magazine, IEEE*, 12(2):38–54, April 2011.

[75] Hao Qi, J. Benedikt, and P.J. Tasker. Novel nonlinear model for rapid waveform-based extraction enabling accurate high power pa design. In *Microwave Symposium, 2007. IEEE/MTT-S International*, pages 2019–2022, June 2007.

[76] S. Woodington, T. Williams, H. Qi, D. Williams, L. Pattison, A. Patterson, J. Lees, J. Benedikt, and P.J. Tasker. A novel measurement based method enabling rapid extraction of a rf waveform look-up table based behavioral model. In *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pages 1453–1456, June 2008.

[77] Frans Verbeyst and M.V. Bossche. Measurement-based behavioral model under mismatched conditions: a new and easy approach for an accurate model. In *Microwave Conference, 2005 European*, volume 1, pages 4 pp.–, Oct 2005.

[78] D Schreurs. Overview of rf large-signal modelling techniques based on time-domain large-signal measurements. In *2002 URSI General Assembly Proceedings*. GA, 2002.

[79] Hao Qi, J. Benedikt, and P.J. Tasker. A novel approach for effective import of nonlinear device characteristics into cad for large signal power amplifier design. In *Microwave Symposium Digest, 2006. IEEE MTT-S International*, pages 477–480, June 2006.

[80] Jeffrey A Jargon, Donald C DeGroot, and KC Gupta. Frequency-domain models for nonlinear microwave devices based on large-signal measurements. *Journal of Research - National Institute of Standards and Technology*, 109(4):407, 2004.

[81] M. Heimlich. Get on the same nonlinear page. *Microwave Magazine, IEEE*, 12(2):32–37, April 2011.

[82] D.E. Root, J. Verspecht, D. Sharrit, J. Wood, and Alex Cognata. Broad-band poly-harmonic distortion (phd) behavioral models from fast automated simulations and large-signal vectorial network measurements. *Microwave Theory and Techniques, IEEE Transactions on*, 53(11):3656–3664, Nov 2005.

[83] V. Cojocaru and F. Sischka. Non-linear modelling of microwave pin diode switches for harmonic and intermodulation distortion simulation. In *Microwave Symposium Digest, 2003 IEEE MTT-S International*, volume 2, pages 655–658 vol.2, June 2003.

[84] Agilent Technologies. Symbolically defined devices (sdd) in ads. `http://edocs.soco.agilent.com/pages/viewpage.action?pageId=58331014`, 2009.

[85] `http://cp.literature.agilent.com/litweb/pdf/ads2008/ccnld/ads2008/Diode_Model_(PN-Junction_Diode_Model).html`.

[86] Alternative implementation of a capacitor. `http://edocs.soco.agilent.com/display/ads2008U1/Custom+Modeling+with+Symbolically-Defined+Devices`.

[87] K. Hettak, T. Ross, D. Gratton, and J. Wight. A new type of gan hemt based high power high-pass/low-pass phase shifter at x band. In *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, pages 1–3, June 2012.

[88] D. Pavlidis, Y. Archombault, D. Gratton, and J. Meyersheck. Adjustable impedance network and control circuit, 1985.

[89] J.-L. Cazaux, D. Pavlidis, Geok-Ing Ng, and Marcel Tutt. The use of double heterojunction diodes in monolithic phase shifters. In *Microwave Conference, 1988. 18th European*, pages 1005–1010, Sept 1988.

[90] P. Pipinys and V. Lapeika. Temperature dependence of reverse-bias leakage current in gan schottky diodes as a consequence of phonon-assisted tunneling. *Journal of Applied Physics*, 99(9):093709–093709–3, May 2006.

[91] J.V. Siles and J. Grajal. Physics-based design and optimization of schottky diode frequency multipliers for terahertz applications. *Microwave Theory and Techniques, IEEE Transactions on*, 58(7):1933–1942, July 2010.

[92] E. Peytavit, P. Latzel, F. Pavanello, G. Ducournau, and J.-F. Lampin. Cw source based on photomixing with output power reaching 1.8 mw at 250 ghz. *Electron Device Letters, IEEE*, 34(10):1277–1279, Oct 2013.

[93] Chong Jin, Mohammed Zaknoune, and Dimitris Pavlidis. Low-dislocation density bulk gan schottky diodes. In *Proceeding of 38th Workshop on Compound Semiconductor Devices and Integrated Circuits*, 2014.

Publications

[1] C. Jin; E. Okada; M. Faucher; D. Ducatteau; M. Zaknoune; D. Pavlidis: A GaN Schottky Diode-Based Analog Phase Shifter MMIC, *EuMIC 2014*, accepted

[2] C. Jin; M. Zaknoune; D. Pavlidis: Low-Dislocation Density Bulk GaN Schottky Diodes, *Proceedings of the 38th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)* Delphi, Greece, Jun.15-18 2014

[3] C. Jin; M. Zaknoune; D. Ducatteau; D. Pavlidis: Properties of GaN Frequency Multipliers Based on Large-Signal Network Analyzer and Harmonic Active Load-Pull, *Proceedings of the 10th Topical Workshop on Heterostructure Microelectronics (TWHM)*, Hakodate, Japan, Sep.2-5 2013

[4] C. Jin; M. Zaknoune; D. Ducatteau; D. Pavlidis: Properties of GaN Frequency Multipliers Based on Large-Signal Network Analyzer and Harmonic Active Load-Pull, *IEEE International Microwave Symposium (IMS)*, Seattle, U.S., June 2-7, 2013

[5] C. Jin; M. Zaknoune; D. Ducatteau; D. Pavlidis: All E-beam Technology of GaN Schottky Diodes and their Large-Signal Characteristics, *Proceedings of the 37th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)* Warnemünde, Germany, May 27-29, 2013

[6] C. Jin; D. Pavlidis; L. Considine: Frequency Multiplication Using Wide bandgap-based Diodes, *Workshop on Compound Semiconductor Materials and Devices (WOCSEMMAD)*, New Orleans, LA, February 17-20, 2013

[7] C. Jin; D. Pavlidis; L. Considine: DC and High-Frequency Characteristics of GaN Schottky Varactors for Frequency Multiplication, *IEICE Transactions on Electronics*, Vol.E95-C, No.8, pp. 1348šC1353 Aug. 2012

[8] C. Jin; D. Pavlidis; L. Considine: A Novel GaN-Based High Frequency Varactor Diode, *European Microwave Integrated Circuits Conference (EuMIC)*, pp. 118šC121, Paris, France, Sep. 27-28, 2010

[9] C. Jin; K. Boye; M. Abe; D. Pavlidis: GaAs-Based IR Detector for Array Applications, *Proceedings of the 34th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE)*, pp. 117-118, Seeheim/Darmstadt, Germany, May 17-19, 2010

[10] S. Seo; E. Cho; G. Aroshvili; C. Jin; D. Pavlidis; and L. Considine: Dispersion, High-Frequency and Power Characteristics AlN/GaN Metal Insulator Semiconductor

Field Effect Transistors with in-situ MOCVD deposited Si_3N_4, *IEICE Transactions on Electronics*, Vol.E93-C No.8 pp.1245-1250 Aug. 2010

[11] E. Cho; S. Seo; C. Jin; D. Pavlidis; G. Fu; J. Tuerck; and W. Jaegermann: Impact of in-situ SiN_x layer grown with metal organic vapor phase epitaxy on the electrical and optical properties of AlN/GaN metal insulator semiconductor field effect transistor structures, *J. Vac. Sci. Technol. B*, 27 (5), pp 2079-2083, Sept/Oct 2009

[12] S. Seo; E. Cho; C. Jin; D. Pavlidis; L. Considine: AlN/GaN Metal Insulator Semiconductor Field Effect Transistors with in-situ MOCVD deposited Si_3N_4, *35th International Symposium on Compound Semiconductors (ISCS)*, Rust, Germany, Sep. 2008

Curriculum vitae

Name Chong Jin

Birth 29.11.1982 born in Sichuan, P.R.China

Family status

Married Wife: Yong Long
Son: Shen Jin

School/Study

1988-1993 Liangshui Elementary School, Lezhi County, Sichuan, China

1993-1996 Dafo Middle School, Lezhi County, Sichuan, China

1996-1999 Lezhi High School, Lezhi County, Sichuan, China

1999-2003 University of Electronic Science and Technology, Chengdu, China
Bachelor of Science: majored in Microelectronics

2003-2006 University of Electronic Science and Technology, Chengdu, China
Master of Science: majored in Microelectronics

2008-2014 Dr.-Ing. Thesis, Department of High Frequency Electronics, Electrical Engineering and Information Technology, TU Darmstadt and Institute of Electronic, Microelectronic and Nanotechnology, University of Lille1

Work experience

2006-2007 University of Electronic Science and Technology
Research Assistant

2008-2011 Department of High Frequency Electronics, TU Darmstadt
Research Assistant

2011-2014 Institut of Electronics, Microelectronics and Nanotechnology
Research Assistant