Investigation of Variation in Organic Thin-film Transistors (OTFT) and Design of Variation-aware Organic Circuits

Untersuchung von Parameterschwankungen in organischen Dünnfilmtransitoren und der Entwurf von schwankungstoleranten Schaltungen

Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
genehmigte Dissertation von M.Sc. Ramkumar Ganesan aus Surulipatty, Indien
April 2016 — Darmstadt — D 17

TECHNISCHE UNIVERSITÄT DARMSTADT

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Eletrotechnik und Informationstechnik
Institut für Datentechnik
Forschungsgruppe Mikroelektronische Systeme

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Genehmigte Dissertation von M.Sc. Ramkumar Ganesan aus Surulipatty, Indien

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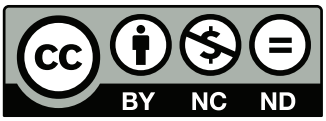
Tag der Einreichung: 28.10.2014
Tag der Prüfung: 29.04.2015

Darmstadt — D 17



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Darmstadt, den April 4, 2016

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(Ramkumar Ganesan)

I dedicate this to my caring wife and our baby girl Shanvitta. I also dedicate this work to my mom, dad and my brother.

"Live as if you were to die tomorrow.
Learn as if you were to live forever."

- Mahatma Gandhi

Acknowledgments

First of all, I would like to express my heartfelt thanks to Professor Manfred Glesner for being my PhD advisor. Since the day when I first met him, he has been always supportive and helped me to have a big picture in my research. The past 4 years were a crucial period in my life that shaped my personality. His advices have been and still guide me in my scientific and professional path. I would also like to thank my project mate Dr.Ing. Sebastian Pankalla for the fruitful discussions we have had that helped me better my understanding of the semiconductor physics and modelling of organic devices. I am also grateful to Professor Edgar Doersam from the Institute of Printing Science and Technology (IDD) at TU Darmstadt for coordinating the PolyTOS project. I also thank Dr.Ing. Dieter Spiehl, Dr.Ing. Hans Martin Sauer, Simone Ganz and other colleagues from IDD institute for helping me understand the various aspects involved in the printing process.

I would also like to express my sincere thanks to Dr.Ing. Juergen Krumm and Klaus Ludwig from PolyIC GmbH for their support with the fabrication of organic circuits. I also thank Dr.Ing. Oliver Hoerer and Erwin Schmidt from Pepperl+Fuchs GmbH, for providing the silicon based RFID test environment containing a front-end circuit and its reader. I would also like to thank all my friends and colleagues at TU Darmstadt. The list would be too long to fit here. But I want to thank Dr.Ing. Christopher Spies, Dr.Ing. Surapong, Dr.Ing. Ashok Jaiswal, Dr.Ing. Yuan Fang, Dr.Ing. Francois Philipp, Rakash Sivasiva Ganesan and Dr.Ing. Harish Balasubramaniam in particular. They generously provided me suggestions and gratitudes when I encountered challenges during the course of my research.

Finally, I would like to thank my wife, Swathi, for her patience and support throughout this work. She was always there to support me through all my ups and downs and often helped in taking away the stress involved in my research. I am also deeply grateful to my parents in India whose encouraging words kept me motivated. Their sacrifices have made me what I am today.

Abstract

This work investigates the key sources of variability in Organic Thin-film Transistor (OTFT) namely process variations and bias-stress induced variation, and presents circuit design techniques to build robust variation-aware digital and analog circuits using OTFTs. OTFTs suffer from a relatively large V_T variation due to the bias stress effects, and process mismatch variations. Though these effects are also prevalent in silicon based transistors, their magnitude is comparatively larger in the case of OTFTs. This renders the well-established silicon based circuits unsuitable for organic electronics. Therefore, direct adaptation of the silicon based circuits for realising organic circuits does not effectively handle the relatively large parameter and mismatch variations associated with OTFTs. In this work, we first investigate the bias-stress induced threshold voltage (V_T) variation and process variations to understand the impact of these variations on the performance of organic circuits. Then, two different strategies were employed to design robust organic circuits. The first method involves designing new load topologies that are more robust to the threshold voltage variations without compromising on gain. The other strategy was to realize the essential analog circuit functionalities like comparator, Analog to Digital Converter (ADC) using digital circuit blocks. In this direction, a digital comparator and digital A/D converter circuits were developed. Finally to demonstrate the system integration, a temperature sensing organic smart label system was designed.

Kurzfassung

Diese Dissertation untersucht die Hauptursachen von Parameterabweichungen in organischen Dünnschichttransistoren (engl.: Organic Thin-film Transistor, OTFT), wie Prozessvariationen und durch Vorspannungsbelastung verursachte Variationen. Weiterhin werden Entwurfstechniken für digitale und analoge Schaltungen mit OTFTs unter Berücksichtigung dieser Variabilitäten präsentiert. Aufgrund von Vorspannungsbelastungen und Prozessvariationen leiden OTFTs viel stärker unter Variationen der Schwellspannung VT als Siliziumtransistoren. Dies führt dazu, dass gängige Schaltungstechniken für Siliziumtransistoren nicht direkt auf organische Elektronik anwendbar sind, da diese für solch grosse Variationen nicht ausgelegt sind.

In dieser Arbeit werden die Einflüsse der oben genannten Variationen der Schwellspannung auf die Leistungsfähigkeit organischer Schaltungen untersucht. Anschliessend werden zwei Entwurfsmethoden für robuste organische Schaltungen vorgestellt. Die erste Methode berücksichtigt den Entwurf von optimalen Lasttopologien, durch welche die Auswirkung der Schwellspannungsvariation auf die Verstärkung der Schaltung minimiert wird. Der zweite Ansatz ist die Realisierung von essentiellen analogen Blöcken, wie Komparatoren oder Analog-zu-Digital Wandlern (engl.: Analog-to-Digital Converter, ADC), durch digitale Blöcke. Ein digitaler Komparator sowie ein digitaler ADC wurden entwickelt. Schliesslich wurde ein sogenanntes Smart Label mit Temperatursensor auf Basis organischer Elektronik entworfen, um die Systemintegration zu demonstrieren.

Contents

List of Symbols

α	scaling constant for the bias-stress model	[]
C_i	capacitance per unit area of the gate insulator	[F]
ΔV_T	bias-stress induced shift in the threshold voltage of an OTFT	[V]
E_F	Fermi energy level	[eV]
γ	mobility exponent factor	[]
$g_{m,lin}$	transconductance of the transistor in the linear regime	[$\mathrm{A\,V^{-1}}$]
$g_{m,sat}$	transconductance of the transistor in the saturation regime	[$\mathrm{A\,V^{-1}}$]
I_{DS}	drain to source current	[A]
$I_{DS,lin}$	drain to source current in the linear regime of transistor operation	[A]
$I_{DS,sat}$	drain to source current in the saturation regime of transistor operation	[A]
k_B	Boltzmann's constant	[$\mathrm{eV\,K^{-1}}$]
L	length of the transistor channel	[m]
λ	channel-length modulation constant	[]
μ_{FE}	effective field-effect mobility	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
μ_0	ideal charge-carrier mobility without gate-voltage dependency	[$\mathrm{cm^2\,V^{-1}\,s^{-1}}$]
N_{it}	surface density of interface traps	[$\mathrm{eV^{-1}\,cm^2}$]
I_{ON}/I_{OFF}	on/off current ratio of the transistor	[]
q	elementary electric charge	[C]
S_{sw}	subthreshold swing i.e. inverse subthreshold slope of the transistor	[dec/V]
T	absolute temperature	[°C]
T_0	width of the Density of State (DOS) distribution	[°C]
τ	time constant for the bias-stress model	[s]
T_{Stress}	Time duration of the applied stress voltages	[s]
V_{DS}	drain to source voltage	[V]
V_{FB}	flat-ban voltage of the transistor	[V]
V_{GS}	gate to source voltage	[V]
$V_{GS,eff}$	effective gate to source overdrive voltage	[V]
V_{OH}	output high of the logic gate	[V]
V_{OL}	output low of the logic gate	[V]
V_T	threshold voltage of the transistor	[V]
V_{T0}	threshold voltage of a pristine OTFT	[V]
$V_{T,final}$	saturated threshold voltage value of a stressed OTFT	[V]
$V_{T,initial}$	initial threshold voltage value of a stressed OTFT	[V]
W	width of the transistor channel	[m]

List of Acronyms

a-Si	Amorphous Silicon
ADC	Analog to Digital Converter
BTI	Bias Stress Instability
CMOS	Complementary Metal-Oxide-Semiconductor
DNL	Differential Non-Linearity
DOS	Density of State
EPC	Electronic Product Code
FDC	Frequency to Digital Converter
HCI	Hot-Carrier Injection
HOMO	Highest Occupied Molecular Orbital
INL	Integral Non-Linearity
LSB	Least Significant Bit
LSE	Least Square Error
LUMO	Lowest Unoccupied Molecular Orbital
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTR	Multiple Trapping and Release
OFET	Organic Field-Effect Transistor
OLED	Organic Light Emitting Diode
OPV	Organic Photovoltaic
OSC	Organic Semiconductor
OTFT	Organic Thin-film Transistor
P3HT	Poly(3-hexylthiophene)
p:Si	Polycrystalline Silicon
PMOS	P-Channel Metal-Oxide-Semiconductor
RF	Radio Frequency
RFID	Radio Frequency Identification
SC-OTFT	Single Crystal Organic Thin-film Transistor
Si	Silicon
TFT	Thin-film Transistor
THD	Total Harmonic Distortion
V-f	Voltage versus Frequency
VCO	Voltage Controlled Oscillator
VCRO	Voltage Controlled Ring Oscillator
VRH	Variable Range Hopping
WORM	Write-Once-Read-Many

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1 Introduction

Until the year 1977, all carbon based polymers (plastics) were strictly regarded as insulators with almost negligible conductivity. This property has made them to be widely used as an insulating material in the electronics industry. This perspective was challenged by the work of A. J. Heeger, A. G. MacDiarmid and H. Shirakawa in [Chi+77; Shi+77] where they had reported on the conducting property of polymers. This paved the way for a variety of new applications using conducting polymers and laid a foundation for the organic electronics research. Recognizing the importance of conducting polymers, in 2000, they were awarded a joint Nobel Prize in Chemistry for their discovery.

This chapter starts with a brief motivation to organic electronics. The key advantages and disadvantages, overview of organic semiconducting materials, fabrication methods, and their potential applications are described concisely. In Section 1.2, a review of progress in organic circuits is presented. Section 1.3 introduces the research objectives of this work. Finally, Section 1.4 offers a brief outline of this dissertation.

1.1 Motivation

The reporting of the first Organic Field-Effect Transistor (OFET) by Koezuka *et al.* in 1987 caught the imagination of the researchers worldwide. Since then, there has been a vast advance in organic materials, processing methods, fabrication techniques and devices. The term "organic electronics" designates electronics that uses carbon based small-molecules or polymers as functional materials for semiconductors, conductors and dielectrics. The key reasons for this choice are listed below:

- **Low Process Temperature**: Unlike a modern Si-based technology where processing temperature exceeds 1000 °C, Organic materials can be processed at low temperatures typically below 200 °C. This enables the use of inexpensive and flexible substrates, such as plastic foils, paving the way for flexible electronics, stretchable electronics etc.

- **Solution Processable**: The long-chain polymers are readily soluble in solvents and therefore, can be fabricated by various solution-processed printing techniques, such as spin coating, gravure printing, ink-jet printing, flexographic printing etc., with a significant reduction in the number of vacuum processing steps. This enables low-cost large-area electronics.

- **Large Material-Choice**: Organic chemistry comprises of a limitless variety of materials exhibiting diverse electrical and chemical properties. This has paved way for the realization of physically diverse devices like the Organic Light Emitting

Diode (OLED) [TV87], OTFT [KTA87], Organic Photovoltaic (OPV) [Sar+92], organic gas sensors [Tor+00], organic bio-sensors [WKW84], and organic memories [Ouy+04].

- **Low-Cost Manufacturing**: When using solution-processed organic devices, the absence of high temperature and clean-room facilities make this a potentially low-cost manufacturing technology.

- **Roll-to-Roll Manufacturing**: Given the fact that organic devices can be fabricated on flexible substrates, circuits can be manufactured on large substrates in a roll-to-roll style. This offers mass-manufacturing capability that drives down the cost significantly.

- **Large-Area Electronics**: Because it is low-cost, the surface area of a circuit is not a limiting factor. This paves way for large-area electronics, such as a sheet of pressure sensors.

Despite all these advantages, organic electronic technology presents serious drawbacks that does not allow them to compete with the Silicon (Si)-based electronics. The important drawbacks are the following:

- **Mono-type Circuits**: The first and foremost challenge is that the organic devices can be only mono-type i.e. n- or p- type. This implies that the modern and well established Complementary Metal-Oxide-Semiconductor (CMOS) design techniques cannot be directly applied to organic circuit designs. Though complementary OTFT circuits [Bod+10; BKF09; Oh+07] have already been reported, they usually need to incorporate inferior and less reliable n-type OTFTs [Zha+11] or involve complex process integration steps like in the case of hybrid Thin-film Transistors (TFTs) that uses both organic and inorganic materials [Oh+07]. This inevitably affects the circuit performance like speed, yield, and manufacturability [Hua+11].

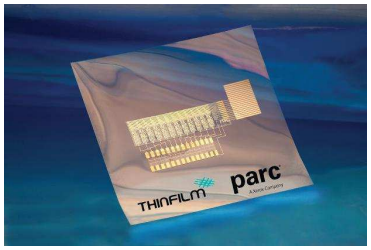
- **Low Carrier Mobility**: Non-availability of band-like charge transport mechanism, as seen in Si devices, leads to a relatively poor mobility. The reported mobility were in the range of $40\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [Yua+14] for small-molecular organic semiconductors and a typical value between 0.1 to $1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for long-chain organic semiconductor using the state-of-the-art solution-processed printing technique.

- **Large Variability**: The electrical characteristics of organic devices are affected by environmental factors at production time and also during run time. Organic semiconductors, especially n-type, are sensitive to environmental factors like oxygen, moisture etc. and lead to a poor shelf time. In addition, there is a profound degradation in the electrical characteristics due to the bias stress effects (i.e. the stress caused by the electric field from the applied bias voltages) which lead to a poor operational lifetime.

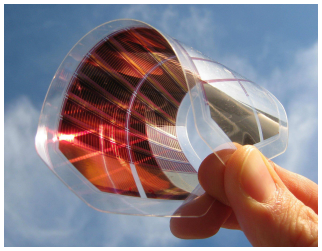
- **Limited Controllability**: Organic semiconductors are difficult to dope. As a consequence, key transistor parameters like V_T and contact resistances are uncontrollable.

1.1.1 Potential Applications of Organic Electronics

A number of potential applications using OTFT have been developed so far which covers a broad range of products and technologies including displays, memories, sensor arrays, lightings, Radio Frequency Identification (RFID) tags and OPVs. The applications can be broadly classified based on two driving factors: a) cost constrained and b) form constrained applications. Figure 1.1 illustrates a few commercial opportunities envisioned for organic electronics.

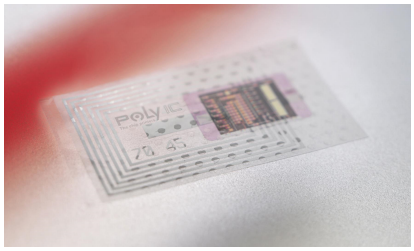


(a) Memories (PARC, Thin Film Electronics)



(b) Organic Photovoltaics (Fraunhofer ISE)

(c) OLED lightings (Osram Opto Semiconductors)



(d) RFID tags (PolyIC)

(e) Flexible batteries (Enfucell)

(f) Flexible plastic displays (LG Display)

Figure 1.1: Few applications using organic electronics.

The roadmap for future applications using organic and printed electronics is illustrated in Figure 1.2. It can be seen from this figure that the future holds a great potential for organic electronics by bringing products to the market in new forms and in disruptive ways. In the recent years, there has been a greater interest among the research community in developing circuits and systems that are required to realise integrated smart systems. These smart systems consist of one or more sensors along with the processing circuitry on an RFID tag. They can be used for brand protection, intelligent tracking and monitoring of goods. Among others, this is also one of the objectives of this dissertation and will be explained in detail in Chapter 6.

1.2 Review of Progress in Organic Circuits

The research in the field of organic electronics, in the early years, was largely focused on the device-level, mainly targeting for OTFTs with higher mobilities. The focus shifted from the largely material perspective to an electronics point of view with the reporting of the first organic integrated circuit by Brwon *et al.* [Bro+95] in 1995. They

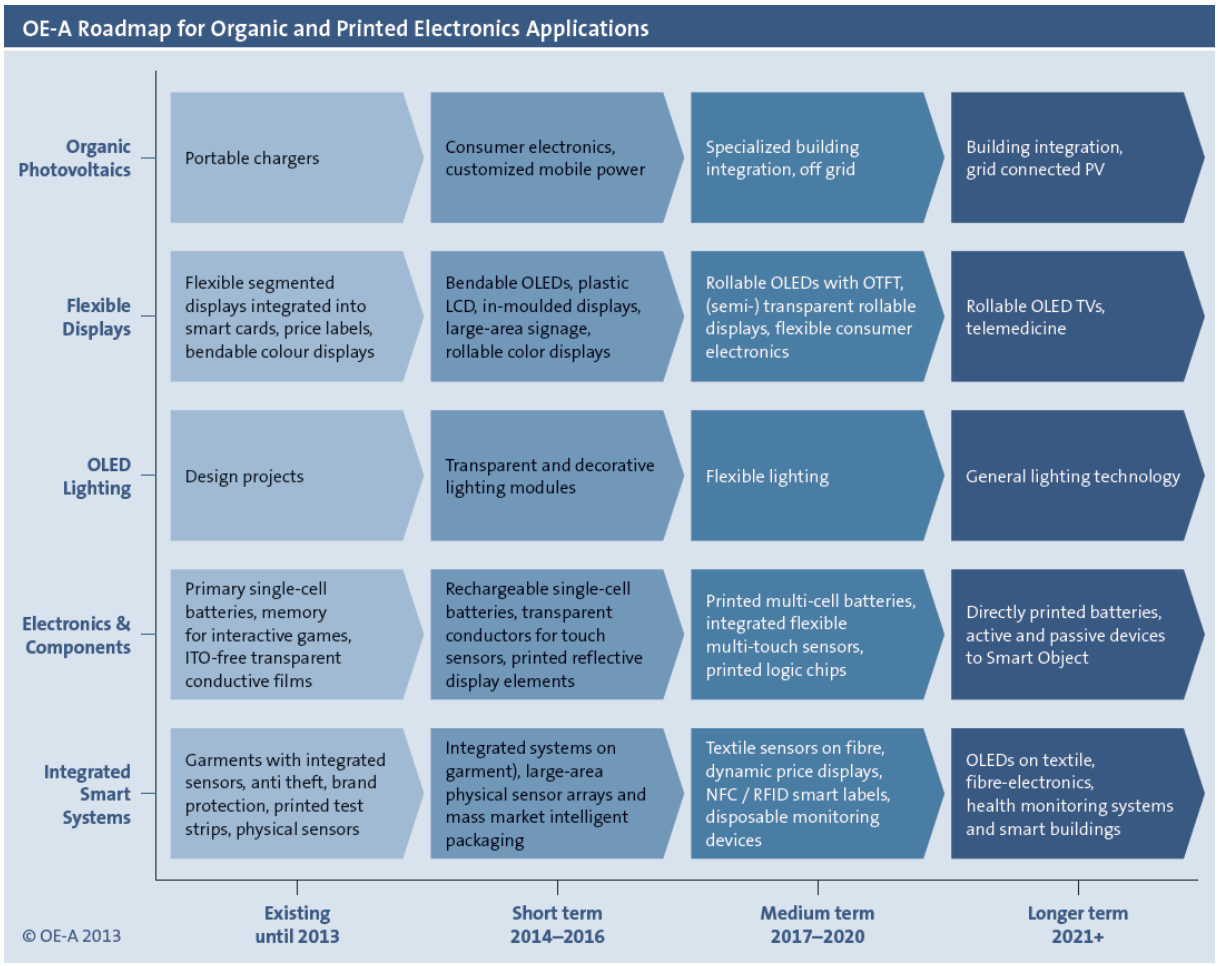


Figure 1.2: OE-A Roadmap for organic and printed electronics (Source: Organic Electronics Association OE-A).

demonstrated a 5-stage ring oscillator using pentacene-based OTFTs having mobilities in the range of $10^{-2}\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$. This provided the breakthrough required for the circuit-design community to shed their scepticism about the OTFT technology. From this point on, circuit development using organic technology rapidly gained interest and more and more groups started embracing organic circuit design. The first phase of organic circuits developed were mostly digital in composition. The great majority of these works comprising inverters, digital gates and ring oscillators were primarily driven by the motive to prove its feasibility and performance. [GGL00; Dod+96; Lin+99; Fix+02; KGJ99; Dru+98; De +06; Bre+03] show the inverters and ring oscillators using organic p-type transistors.

The first analog circuit using OTFTs was reported by [Kan+00] in which they described an organic differential amplifier. Following this, Baude *et al.* demonstrated an RFID circuitry using OTFTs [Bau+03]. This demonstration together with several reporting of different types of organic sensors [Cro+02; Cro+01; Tha+02; Dar+05; Zhu+02] were the first step towards the successful realisation of organic sensor tags. In the recent years, there has been a significant improvement in the performance of Electronic Product Code (EPC) compatible organic RFID transponder circuits [Myn+12; TS09; BKF09; Gue+12; Myn+08; Myn+09; Fio+14; Sub+05; Boh+06; Can+07]. To use these RFID

transponder circuits to form a sensor tag, analog circuits especially ADC are very much essential. In this direction, few organic analog circuits have also been reported by various groups in the literature. These are mainly limited to basic analog circuits like amplifiers [Nau+11; Rai+11; Mar+12; MX10; Gay+06; KB+14; GF07], comparators [Mar+09; Nau+11; Ish+12] and ADCs [Xio+10a; Mar+10; Rai+13; Mar+11; Abd+13; Mar+12; Gay07]. Though the reported analog circuits offer limited performance, they represent significant steps toward successful commercialisation of organic electronic products. In this work a sensor tag for temperature sensing applications is conceptualised and designed. This will be described in detail in Chapter 6.

The use of organic n-type semiconductors, along with the p-type semiconductors, led to the development of organic complementary circuits [Dod+96; Lin+99; Cro+00]. However, compared to their p-channel counterparts n-channel organic semiconductors typically have higher sensitivity to oxygen and moisture. Furthermore, the low work-function metals, required for electron injection in n-channel TFTs, are also reactive and oxidise instantly in air [DM02]. Therefore, until the electrical characteristics of the n-type OTFTs catches up with that of the p-type counterpart, organic circuits will be mostly mono-type using only P-Channel Metal-Oxide-Semiconductor (PMOS).

1.3 Research Objectives

The key objectives of this research are as follows:

- To study, understand and model the bias-stress effects and process variations occurring in OTFTs.
- To develop circuit techniques to realise organic circuits which operates reliably even in the presence of the bias-stress induced V_T variation and process variations.
- To design and integrate all the circuit blocks that are necessary to realise an organic smart label.

1.4 Organization of this Dissertation

This dissertation is organized as follows: Chapter 1 is an introduction. In Chapter 2, the basics of OTFT are discussed. This chapter starts with a review of Organic Semiconductor (OSC) materials. In addition, this chapter also deals with the charge transport models, architecture, operation and electrical characteristics of OTFT. In chapter 3, key sources of variability affecting the OTFT parameters are presented. In chapter 4, a standard cell library of organic digital circuits is presented. Chapter 5 presents the design of variation-tolerant organic circuits. This chapter provides a brief overview of the issues with existing active load circuits and proposes new enhanced load circuits for realising simple organic circuits. Digital based ADC architectures namely VCO-based ADC and all-digital flash ADC are also described in this chapter. In chapter 6, an organic smart label system using p-type organic thin film transistors (OTFT) for temperature sensing applications has been demonstrated. Chapter 7 concludes the work by presenting a summary of the work and makes suggestions for future work.

2 Organic Thin-film Transistors (OTFT)

Contents

This chapter will introduce the structure and characteristics of an OTFT. This chapter starts with a brief overview of organic semiconducting materials that is described in Section 2.1). Section 2.2 gives an overview of different charge transport models applicable for OSCs. In Section 2.3, the focus is on the architecture and fabrication of an OTFT. Following this, the operation and electrical characteristics of an OTFT are discussed in Section 2.4 and 2.5 respectively. Section 2.6 discusses the models used for simulating an OTFT. Finally, Section 2.7 provides a comparison between the electrical characteristics of OTFT and crystalline-Si MOSFET.

2.1 Organic Semiconducting Materials

2.1.1 Review of Organic Semiconducting Materials

Though the polymer initially used by Heeger, MacDiarmid and Shirakawa [Chi+77; Shi+77] lacked interesting electronic properties, the scientific community quickly came up with many advances. Towards the end of 1980s, a series of reporting on OLED [TV87] and OTFT [KTA87; BJF88] marked the real beginning of organic electronics. The first reported OTFT had a field-effect mobility in the range of $10^{-5}\,cm^2\,V^{-1}\,s^{-1}$. Around the same time, a new class of organic semiconducting material was introduced comprising of small-molecules [Cla+88; Hor+89] instead of the long polymeric chains. Unlike the small-molecule oligomers, the polymeric organic materials were easily soluble in solvents. Hence, OTFTs could be fabricated using vacuum sublimation methods that resulted in films of high orderliness. As a result, their mobilities (in the range of $10^{-3}\,cm^2\,V^{-1}\,s^{-1}$) were at least an order of magnitude larger than that from the solution-processed polymers. Horowitz *et al.*, in 1992, reported an OTFT using pentacene that is, now, one of the most widely used small-molecule materials. This was immediately followed by the discovery of C_{60} which exhibits n-type semiconducting property [Hos+93; Had+95]. The year 1996 marked a milestone in the progress of organic electronics. The advances in the OSC [Hor+96; BDL96] led to a significantly higher charge carrier mobilities and for the first time organic electronics was perceived to be a potential competitor

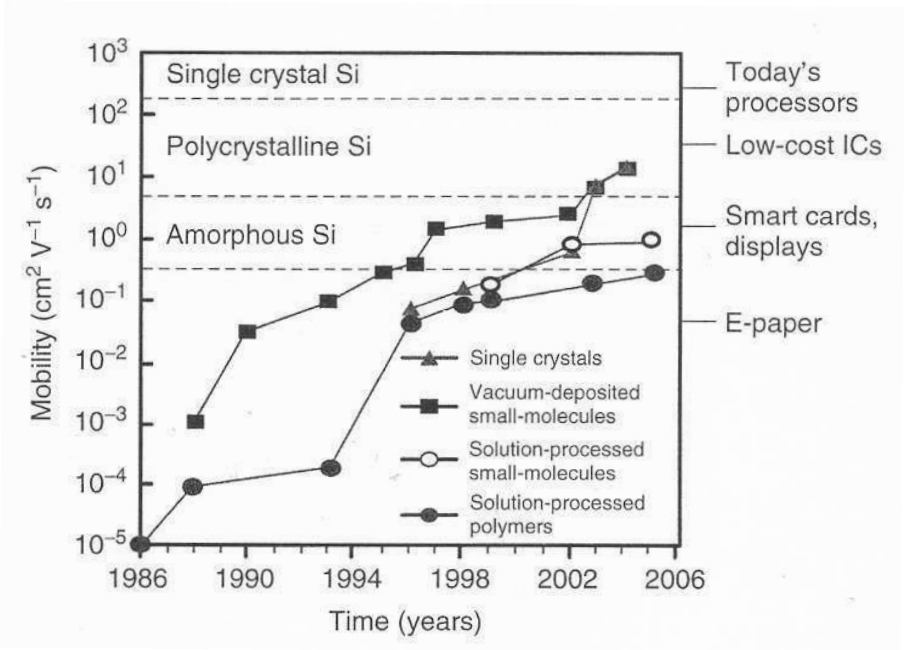


Figure 2.1: Progress in the mobility of organic semiconductors (Reprinted, with permission, from [Li+11])

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to amorphous Si. Horowitz *et al.* reported a Single Crystal Organic Thin-film Transistor (SC-OTFT). A new polymer known by its chemical name P3HT, which will be explained in Section 2.1.2, was introduced by Bao *et al.* that had a mobility of $10^{-2}\,cm^2\,V^{-1}\,s^{-1}$ with a relatively high on/off current ratio typically greater than 10^3. For the first time, OTFTs exhibited sufficient performance that deemed fit for the construction of logic gates using them. Towards the end of 2000, OTFT using solution-processed pentacene was reported. From then on, the mobility of organic semiconducting materials have improved many scales and even exceeded that of Amorphous Silicon (a-Si) and has even approached the mobility of Polycrystalline Silicon (p:Si) [Yua+14; Nak+11]. An overview of the progress in the mobility among various types of organic semiconducting materials is shown in Figure 2.1.

2.1.2 Poly(3-hexylthiophene) (P3HT)

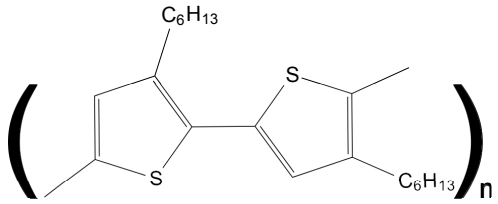


Figure 2.2: Chemical structure of P3HT where *n* denotes the polymer length.

One of the most popular solution-processable organic semiconductor is P3HT. It is a p-type semiconducting polymer with thiophene, a ring of four carbon atoms and one sulphur atom, as a basic building block. A hexyl (C_6H_{13}) side chain is added to the

thiophene ring in order to make P3HT soluble in organic solvents [Kru08]. The chemical structure of P3HT is shown in Figure 2.2.

2.2 Charge Transport Models

Unlike the transistors based on inorganic semiconducting materials, charge transport mechanism in OTFTs is not yet fully understood. The main challenges arise from the fact that the charge carriers are affected by both the physical and chemical changes that happens at the dielectric/semiconductor interface layer, and in the conducting channel. This includes interface defects, trap states, differences in grain size and molecular packing structures. Despite these challenges, several transport models have been proposed to explain the charge transport mechanism in OTFTs. The most important and relevant ones are discussed briefly in the following paragraph.

2.2.1 Band Transport Model

In crystalline semiconductors, charge transport occurs through a band-like transport mechanism along well-defined conduction or valance bands. This results in high mobilities in the range of few $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. Analogous to the conduction and valence bands in crytalline materials, Highest Occupied Molecular Orbital (HOMO) and Lowest Unoccupied Molecular Orbital (LUMO) are used in OSCs. OSCs can be characterized by strong intra-molecular covalent bonds and weak inter-molecular bonds through weak van der Waals forces. This results in discontinuities in the band structure with the band energy widths typically smaller than $k_B T$ [GL67]. The fact that the OSCs have much smaller mobilities ($< 100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) show that the traditional view of band-like transport in an OTFT is not very appropriate. It can be concluded that the charge carriers experience a band-like transport phenomenon only within the molecules. Therefore, the mobility of an OSC is largely limited by the inter-molecular transport mechanism.

2.2.2 Multiple Trapping and Release Model

Experiments have shown that the field-effect mobility of OTFTs depends on the temperature as well as on the gate bias voltage [HHD95]. This behaviour has been explained by Horowitz *et al.* using a Multiple Trapping and Release (MTR) model [HHD95]. In this model, charge carriers are assumed to travel by band-transport. However, an assumption is made that most of the charge carriers are trapped in localized states also known as traps. These traps are caused by the presence of impurity atoms, structural defects and grain boundaries. These trapped charge carriers are temporarily released to an extended-state transport level (valence and conduction bands) and the level of trapping depends on the energy level of the localized states, the temperature and the gate voltage. The charge carriers are trapped and released multiple times during their travel. Though an extended-state transport may occur in highly ordered vacuum-evaporated molecular films [HHD95], it can not occur in disordered organic semiconductor films [Bro+97]. Therefore, this model can not accurately explain the charge transport in disordered organic semiconductor materials.

2.2.3 Variable Range Hopping Model

In disordered organic semiconducting materials, the charge carriers are held in localized states known as hopping sites and they cannot move freely. The charge transport is governed by hopping of thermally activated charge carriers between localized states, rather than by activation of charge carriers to an extended-state transport level. Mobility of charge carriers in a constant Density of State (DOS) can be represented by the Mott equation [Mot68] which is shown in 2.1.

$$\mu_{FE} = \mu_0 \exp\left[-\left(\frac{T_0}{T}\right)^{\frac{1}{4}}\right] \tag{2.1}$$

where T is the absolute temperature, T_0 is a measure of the width of the exponential DOS distribution, μ_0 is the ideal charge-carrier mobility without gate-voltage dependency and μ_{FE} is the effective field-effect mobility taking into account the hopping. The exponential part indicates that the mobility increases with the increase in temperature. Therefore, hopping is a thermally activated phenomenon. Vissenberg and Matters, in [VM98], described a Variable Range Hopping (VRH) model using an exponential distribution of traps. The VRH theory is based on the idea that charge carriers are localized but every now and then a carrier may either hop over a small distance with a high activation energy or hop over a long distance with a low activation energy [VM98]. This model exhibits a thermally activated mobility and also predicts that the mobility depends on the gate voltage according to a power law, as given in equation 2.2.

$$\mu_{FE} = \mu_0 \exp\left[V_{GS} - V_T\right]^{\frac{2(T_0-T)}{T}} \tag{2.2}$$

where V_T is the threshold voltage, μ_0 is the ideal mobility, T is the absolute temperature and T_0 is a measure of the width of the exponential DOS distribution.

2.3 OTFT Architecture and Fabrication

2.3.1 Device Structure

Four possible TFT device structures can be defined depending on the position of the gate, source, and drain contacts relative to the organic semiconductor film, as shown in Figure 2.3. They can be broadly classified into coplanar and staggered structures. In a coplanar structure, also called as bottom-contact structure, the conducting channel, drain and source terminals are all located on the same side of the semiconductor layer, as shown in Figure 2.3(b) and 2.3(d). On the contrary, in a staggered structure, also called as top-contact structure, the conducting channel is on the opposite side of the semiconductor film that contains the source and drain contacts, as shown in Figure 2.3(a) and 2.3(c). The coplanar and staggered devices can each be further classified into bottom-gate and top-gate depending on the position of the gate contact with respect to the substrate. OTFTs using a coplanar structure have a narrow contact

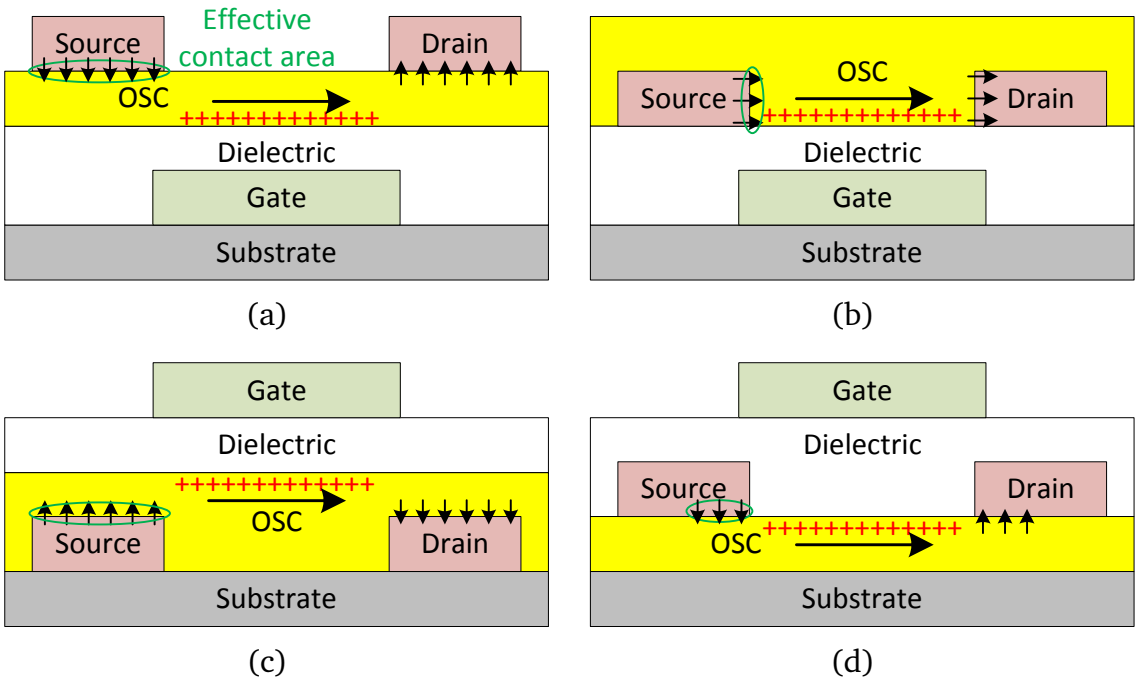


Figure 2.3: Schematic cross-section of OTFT device structures having (a) bottom-gate top-contact, (b) bottom-gate bottom-contact, (c) top-gate top-contact, and (d) top-gate bottom-contact configurations. The conducting channel is schematically shown in red.

region between the source/drain terminal and the conducting channel. Therefore, devices in such a configuration generally suffer from large contact resistance, which can limit their operation at high frequencies. On the other hand, in a staggered structure, the contact resistance is relatively less due to the large effective contact area between the source/drain terminal and the channel.

2.3.2 Technology Description

The low charge-carrier mobility of amorphous OSC materials results in OTFTs having a large channel width, often in the millimetre range so as to conduct a reasonable drain-source current. Therefore, OTFTs are often realized as interdigited structures. Figure 2.4 presents the structure of a typical OTFT with an interdigited source and drain contact structure from a top-view. In this work, we have used OTFTs in a top-gate bottom-contact configuration for the realisation of organic circuits. As described in Section 2.3.1, the top-gate structure is used to reduce the contact resistance and to have a relatively better performance. Given a top-gate structure, the top-contact configuration is the preferred choice when the source and drain contacts are photo-lithographically patterned. Photo-lithographically patterned source and drain contacts lead to a small dimension that is usually not feasible with the conventional printing techniques. The top-gate top-contact transistors are built using a four-layered process. A flexible polyester film was used as a substrate. On top of this, a 40 nm thick layer of gold was deposited as source and drain electrodes. Then an active layer consisting of a p-type soluble organic polymer, P3HT, was spin-coated on the substrate, containing

source and drain contacts. The resulting OSC layer had a thickness of approximately 50 nm. Subsequently, a soluble copolymer blend was applied over the OSC as a dielectric. The dielectric layer, which isolates the gate from the actual channel, was also spin-coated and resulted in a film thickness of approximately 500 nm. Finally, on top of the dielectric layer, a gate electrode was deposited. Both the gate and source/drain electrode layers were patterned using lithographic masks with a critical dimension of 5 μm giving rise to at least 40 nm thick gold lines. An additional cross-over layer is used to isolate two crossings or over-lapping of metal tracks. In order to protect the transistor against any contamination from air and moisture, an encapsulation layer may be applied over the whole transistor (and the chip). The current process can only fabricate p-type OTFTs. No self-alignment of gate contact with the underlying source and drain contact is possible. This produces a relatively large parasitic capacitances. Though the circuits were fabricated in a clean-room process, the technology is compatible with printing processes targeted for mass production. It is worthy of mentioning that all the OTFTs and organic circuits used in this work were fabricated by PolyIC GmbH using the above described organic process technology.

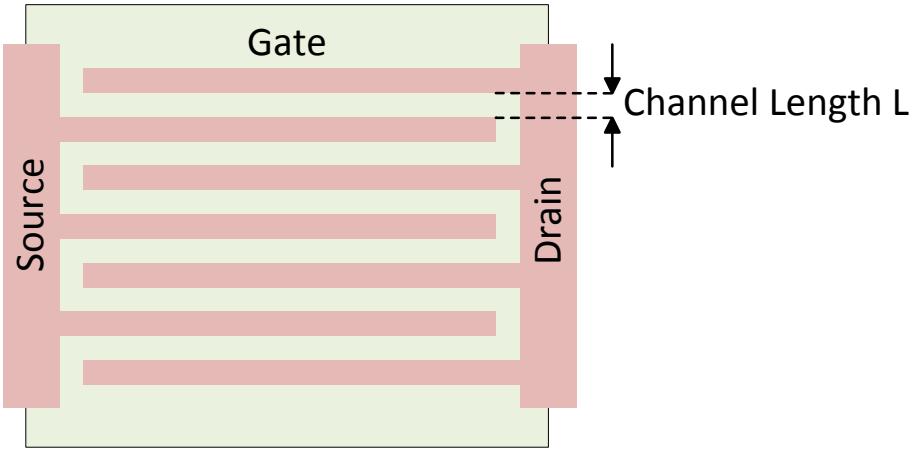


Figure 2.4: Schematic top-view of an OTFT with an interdigited finger structure.

2.4 OTFT Operation

OTFT is a three terminal device with no separate bulk connection. The TFTs and the conventional Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) share many common functional and structural features between them. However, there are also some key differences between them. First, the current enhancement in TFTs occurs through accumulation unlike MOSFET devices where it happens through inversion. This implies that the conduction channel, at the interface between the gate dielectric and OSC layer of an OTFT, is formed by accumulation of majority charge carriers. The other key difference is that there is no depletion region to isolate the conducting channel from the substrate. The depletion region in a conventional MOSFET isolates the device from the substrate and this results in a very low off-current. In OTFTs, the low off-current is guaranteed by the low conductivity of OSC. Since, there is no separate bulk connection, the drain-source current is a combination of the channel current and the bulk current. However, due to the low conductivity of the OSC region outside the accumulated channel,

the bulk current component is negligible. For a better understanding of the operation of an organic transistor, it is interesting to analyse the transistor behaviour under different bias conditions. For this reason, it is useful to define the meaning of V_{FB} for a Metal-Oxide-Semiconductor (MOS) structure. It should be mentioned that an OTFT operating in the accumulation regime is synonymous to a MOS structure. V_{FB} is the value of gate voltage for which the electric field inside the dielectric layer is zero. In this case, the energy bands are flat and the transistor is said to be in a thermodynamic equilibrium condition. Since the OTFTs are mostly undoped and since they have no depletion region, their threshold voltages (V_T) are equal to V_{FB} as shown in equation 2.3. This equation holds true under the assumption that there are no fixed charges and defect states.

$$V_T = V_{FB} \tag{2.3}$$

2.4.1 ON State

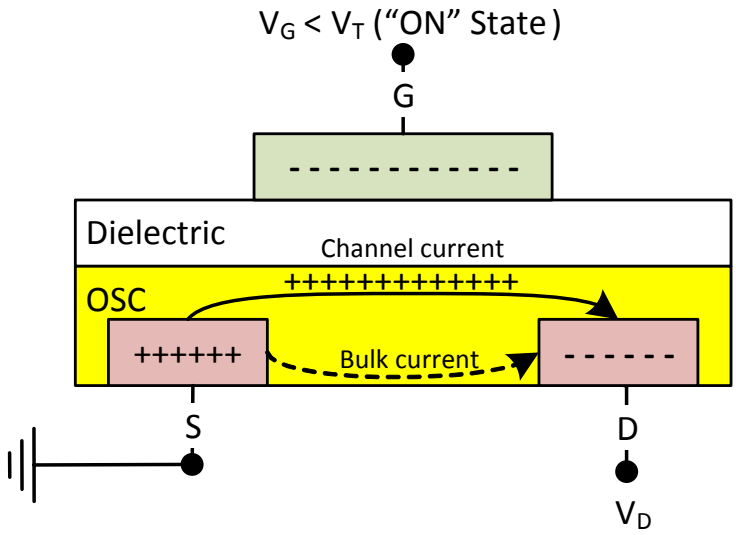


Figure 2.5: Simplified illustration of the operation of an OTFT during "ON" state. The total drain-source current is the sum of channel and bulk currents.

For a p-type OTFT, when a negative potential is applied to the gate terminal such that $V_G < V_T$, the transistor is said to be turned "on". This sets up an electric field in the dielectric layer that leads to an accumulation of the majority charge carriers at the interface between the dielectric and the semiconducting layers. This accumulation layer forms a conducting channel between the source and drain terminals. This channel allows a free flow of charges provided a potential difference exists between the source and drain terminals. In addition to the conduction current from the accumulated majority charge carriers, there is also a small amount of current flowing through the bulk. Therefore, the total drain-source current (I_{DS}) is given by the sum of the channel current and the bulk current, as shown in Figure 2.5. Additionally, the bulk current is a function of drain-source voltage (V_{DS}) and it is independent of the gate-source voltage (V_{GS}). This effect limits the maximum achievable gain [Mai13].

2.4.2 OFF State

When the gate voltage (V_G) is greater than V_T, the OTFT is said to be in the "OFF" state. The positive voltage at the gate terminal repels the positive charge carriers (holes) and attracts the negative charge carriers (electrons), as shown in Figure 2.6. This leads to a depletion of the majority charge carriers at the dielectric/semiconductor interface and there is no conducting channel in the semiconductor layer. This implies that, there is no current flow between the source and drain electrodes. However, a bulk current continues to flow between the source and drain terminals and it decreases with an increase in the gate voltage. As the gate voltage is increased, beyond a certain value when there are no charge carriers present within the semiconductor layer, the bulk current becomes zero and thus there is no current flow between the source and drain terminals.

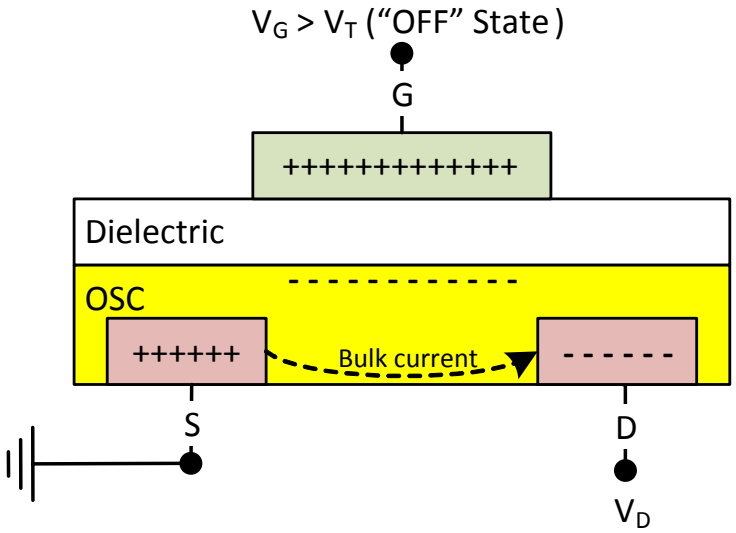


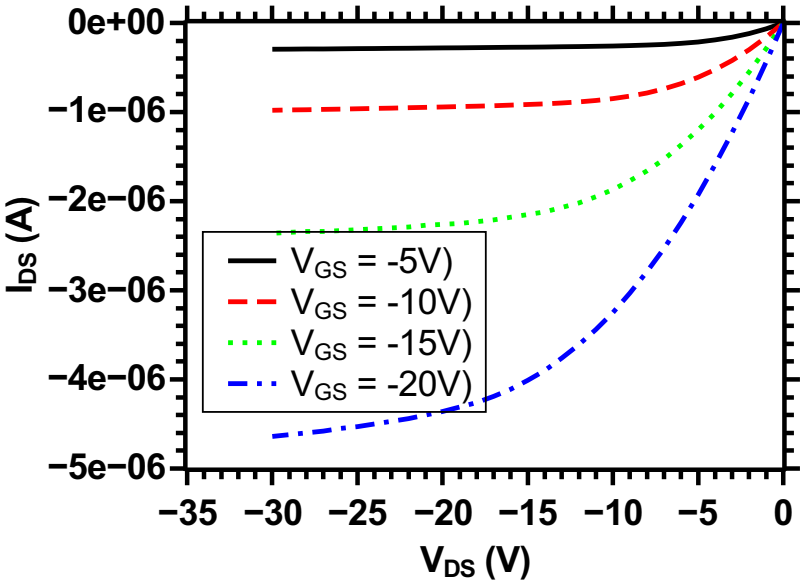
Figure 2.6: Simplified illustration of the operation of an OTFT during "OFF" state. The total drain-source current is nothing but the bulk current.

2.5 Electrical Characteristics of OTFTs

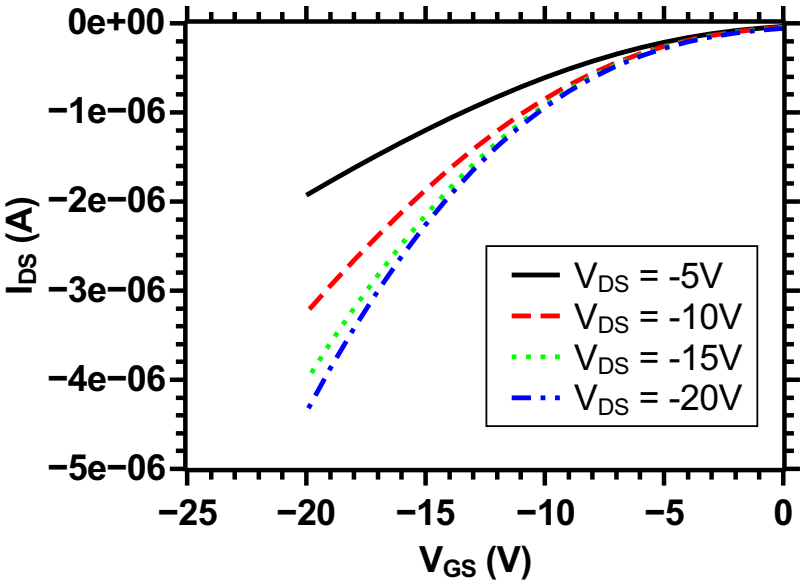
OTFTs are characterized by the same general principles as silicon MOSFETs. The voltage applied at the gate terminal modulates the width of the charge carrier channel and thus controls the current flow through the transistor [Tsi87]. For a gate potential (V_G) that is greater than the threshold voltage (V_T), the charge density Q inside the channel is dependent on V_{GS} by Equation 2.4

$$Q = -C_i (V_{GS} - V_T) \tag{2.4}$$

where C_i is the capacitance per unit area of the gate insulator. In Equation 2.4, the channel potential from the lateral electric field is assumed to be zero. Though the OTFTs share many common features with MOSFETs, OTFTs cannot be accurately described by the same set of analytical equations that are used to describe Silicon MOSFETs [HD91; Hor+99], among other things due to the differences in the conduction



(a) Output characteristics



(b) Transfer characteristics

Figure 2.7: Characteristics of a typical p-type OTFT.

process. However, as a first approximation, the classical Shichman-Hodges equations [SN06] of silicon MOS transistor can be used to describe the large-signal behaviour of an OTFT.

For $|V_{DS}| < |V_{GS} - V_T|$, the transistor works in linear regime and the drain-source current (I_{DS}) is given by the following equation:

$$I_{DS,lin} = -\frac{W}{L}\mu_{FE}C_i\left[(V_{GS} - V_T)\,V_{DS} - \frac{1}{2}V_{DS}^2\right](1 + \lambda|V_{DS}|) \tag{2.5}$$

where V_T is the threshold voltage, C_i is the dielectric capacitance per unit area and μ_{FE} is the effective charge carrier mobility of the OTFT. When $|V_{DS}| \geq |V_{GS} - V_T|$, the transistor works in saturation regime and the drain-source current is given by the following equation:

$$I_{DS,sat} = -\frac{W}{L}\mu_{FE}C_i\left[V_{GS} - V_T\right]^2(1 + \lambda|V_{DS}|) \tag{2.6}$$

Figure 2.7 depicts the output and transfer characteristics of a typical p-type OTFT. The current equations described in Equations 2.5 and 2.6, provide a basis for characterizing and comparing various OTFTs. The key electrical parameters that define the performance of an OTFT include: effective charge carrier mobility (μ_{FE}), threshold voltage (V_T), subthreshold swing (S_{sw}) and on/off current ratio (I_{ON}/I_{OFF}). The field-effect mobility (μ_{FE}) is proportional to the semiconductor conductivity and it describes how rapidly the charge carriers can move through the semiconducting material. This is directly responsible for determining the transistor performance metrics like maximum operating frequency, gain etc. and therefore they are often used as a figure of merit for comparing the performance of various organic semiconducting materials. The effective field-effect mobility is normally extracted from the transconductance value obtained when the transistor is operated in linear or saturation regime. In the linear regime, μ_{FE} can be calculated from transconductance ($g_{m,lin}$) by differentiating the Equation 2.5 and it is expressed as:

$$g_{m,lin} = \left.\frac{\partial I_{DS,lin}}{\partial V_{GS}}\right|_{V_{DS}=\text{Const.}} = \mu_{FE}C_i\frac{W}{L}V_{DS} \tag{2.7}$$

$$\implies \mu_{FE} = \frac{g_{m,lin}}{C_i V_{DS}}\frac{L}{W} \tag{2.8}$$

Similarly, in the saturation regime the field-effect mobility can be calculated by differentiating Equation 2.6 and it is given by the following expression:

$$g_{m,sat} = \left.\frac{\partial I_{DS,sat}}{\partial V_{GS}}\right|_{V_{DS}=\text{Const.}} = \mu_{FE}C_i\frac{W}{L}\left(V_{GS} - V_T\right) \tag{2.9}$$

By plotting $g_{m,sat}$ versus V_{GS}, the slope and intercept of the linear fit can be calculated that corresponds to the value of μ_{FE} and V_T respectively. Alternatively, the threshold voltage can also be evaluated from the plot of square-root of drain-source current (I_{DS}) versus the gate-source voltage (V_{GS}). The intercept point of its linear fit on the x-axis provides a rough estimation of V_T as shown in Figure 2.8. The term threshold voltage, originally used for MOSFETs, refers to the voltage where the onset of the inversion layer is established. Since, the OTFTs operate in accumulation mode, V_T in OTFTs refers to it's switch-on voltage, i.e. the gate-voltage which causes a significant increase in the drain-source current.

In a similar way, the I_{ON}/I_{OFF} and subthreshold swing (S_{sw}) can be easily deduced from the I_{DS}-V_{GS} curve. Due to the non-idealities present in the OTFT, there is a non-

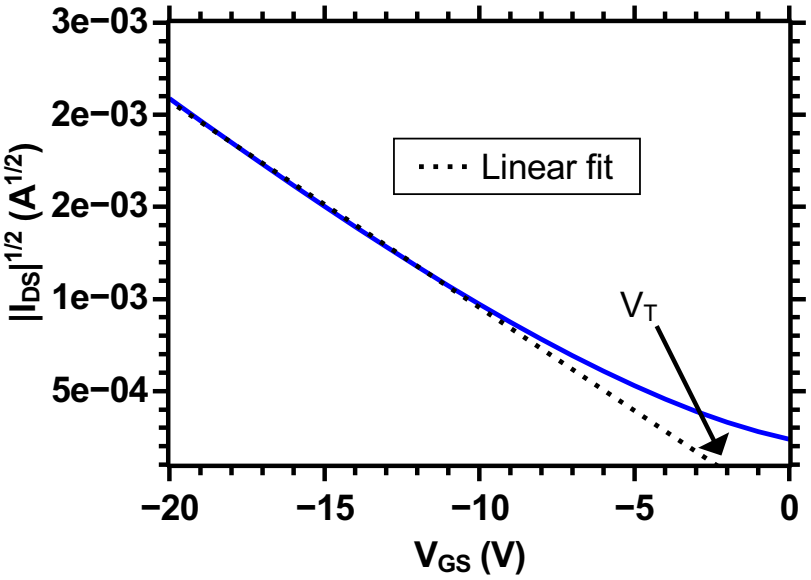


Figure 2.8: Illustration of the threshold voltage of a typical p-type OTFT in a plot of square-root of I_{DS} versus V_{GS}.

zero gate leakage current flowing between the source and gate terminal. Plot showing the gate-leakage current of a p-type OTFT is shown in Figure 2.9.

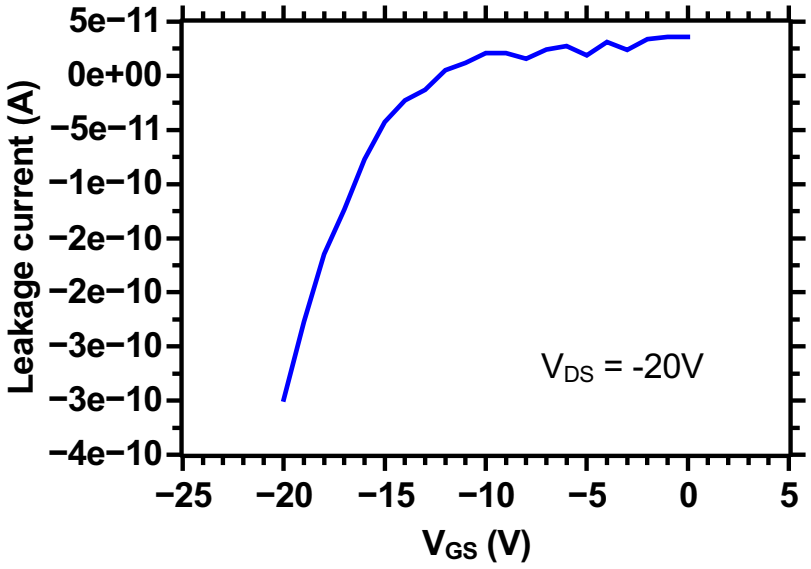


Figure 2.9: Gate-leakage current versus V_{GS} of a p-type OTFT for a V_{DS} = -20 V.

2.6 Modelling of OTFTs for Circuit Simulation

The current-voltage equations in 2.5 and 2.6 can satisfactorily represent the actual OTFT behaviour for basic theoretical analysis of organic circuits. However, their derivation is based on several approximations that are not always fulfilled by organic semiconductors. Thus, the device parameters extracted from this simple model are subject to error.

One of the key feature which is not accounted for by the model is the dependence of mobility on the gate bias voltage. An approach to overcome this model insufficiency is to introduce correction factors to the mobility that can represent its gate-voltage dependency. Charge transport in the conduction channel of an OTFT operating in the accumulation regime can be described by the VRH model [VM98] based on thermally activated tunnelling of holes between localized states in an exponential DOS, that is described in Section 2.2.3. The gate-voltage dependent field-effect mobility resulting from the VRH model, can be expressed in the form:

$$\mu_{FE} = \mu_0 \exp\left[V_{GS} - V_T\right]^{\gamma} \tag{2.10}$$

where γ is the mobility exponent factor coming from the exponential DOS distribution. Equation 2.10 is same as Equation 2.2 with γ equal to $2(T_0 - T)/T$. Using the gradual channel approximation, i.e. the electric field along the channel is much lower and does not significantly influence the perpendicular electric field across the channel, the drain current of an OTFT in the accumulation regime is of the form [Gel+06]:

$$I_{DS} = \begin{cases} \underline{\text{For } |V_{DS}| < |V_{GS} - V_T|:} \\ \quad -\dfrac{\mu_0 C_i W}{L\,(2+\gamma)}\left[(-V_{GS}+V_T)^{(2+\gamma)} - (-V_{GS}+V_T+V_{DS})^{(2+\gamma)}\right](1+\lambda|V_{DS}|) \\ \underline{\text{For } |V_{DS}| \geq |V_{GS} - V_T|:} \\ \quad -\dfrac{\mu_0 C_i W}{L\,(2+\gamma)}\left[(-V_{GS}+V_T)^{(2+\gamma)}\right](1+\lambda|V_{DS}|) \end{cases} \tag{2.11}$$

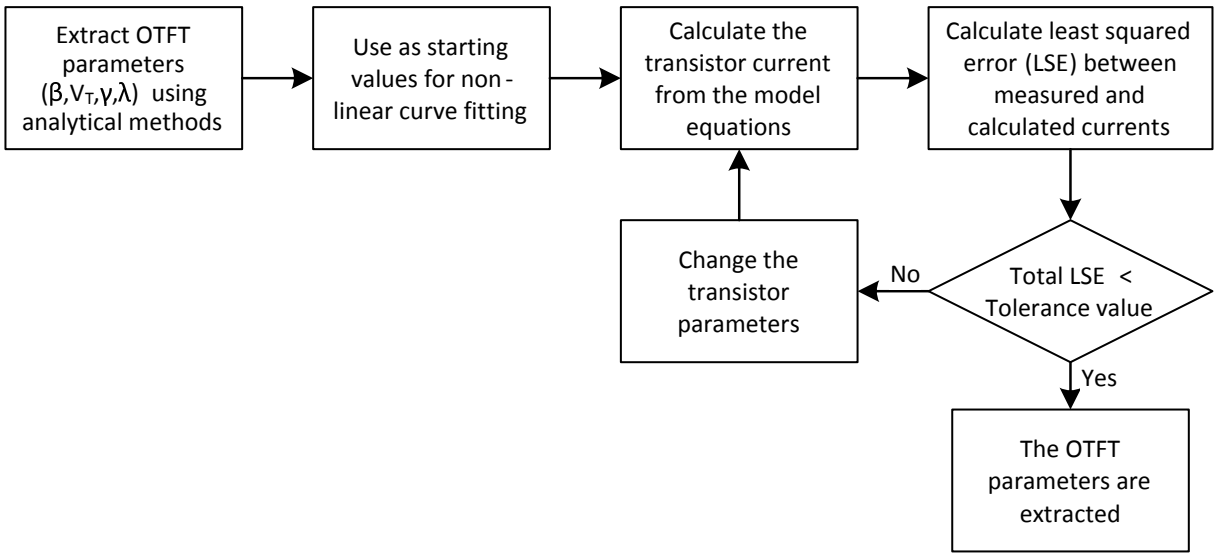


Figure 2.10: Flow-chart describing the various phases of the employed procedure for OTFT parameter extraction.

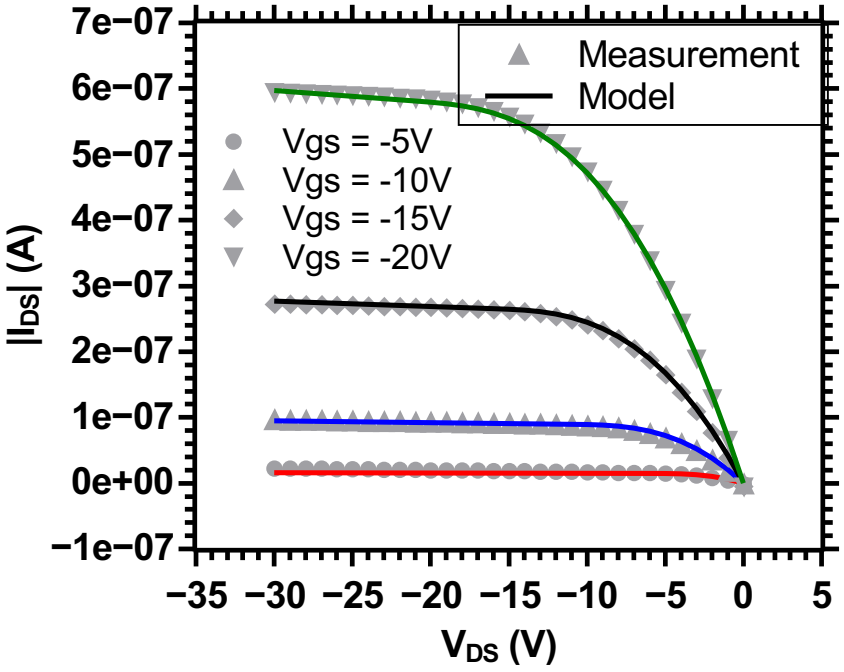


Figure 2.11: Measured and simulated output characteristics of an OTFT with a width of 800 μm and a length of 10 μm.

In the above model, W, L and C_i are process constants, and γ, V_T, μ_0 and λ are device parameters. The device parameters can be extracted from the measured data using analytical methods [Mar+14; KM13], as described in Section 2.5, or using non-linear least squares curve-fitting methods. Among other reasons, the non-quadratic dependence of the transistor current over the drain-source and gate-source voltages owing to the presence of γ in the power term of Equation 2.11, render the device parameters extracted using traditional graphical methods inaccurate. The non-linear least squares curve fitting or data-fitting is an iterative process which fits a mathematical function to a series of data points by varying the parameters of the function in a least square sense. The objective is to find the value for each of the parameter μ_{FE}, V_T, γ and λ that minimizes the total Least Square Error (LSE) between the modelled current and the measured current of an OTFT. The minimization function is shown below:

$$\underset{\mu,V_T,\gamma,\lambda}{\text{minimize}} \sum_{\forall V_{DS}} \sum_{\forall V_{GS}} \left[I_{DS,model}\left(\mu, V_T, \gamma, \lambda, V_{DS}, V_{GS}\right) - I_{DS,measured}\left(V_{DS}, V_{GS}\right) \right]^2 \qquad (2.12)$$

Non-linear optimization algorithm namely the Levenberg-Marquardt algorithm [Mor78] has been used to minimize the function given by Equation 2.12.

Figure 2.11 shows the comparison of the measured and simulated I_{DS} versus V_{DS} characteristics of an OTFT for various values of V_{GS}. The comparison of experimental I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics to those obtained from the simulations using Equation 2.11 shows very good agreement. Therefore, Equation 2.11 represents a more comprehensive model for OTFTs based on disordered/amorphous OSCs and can provide a more accurate extraction of the transistor parameters. Due to the growing understanding of

OSCs behaviour and OTFT physics, improved models for OTFT continue to evolve to this day.

2.7 Differences between Crystalline-Si MOSFET and OTFT

Table 2.1 provides a comparison between silicon-based MOSFET and OTFT.

Table 2.1: Comparison between silicon-based MOSFET and OTFT

Characteristic	Si-MOSFET	OTFT
Operation mode	Inversion	Accumulation
Charge transport	Band transport	Hopping, trap and release
Processing temperature	$> 800\,^{\circ}\mathrm{C}$	$<200\,^{\circ}\mathrm{C}$
Contact resistance	Negligible	Relatively large contact resistance
Environmental impact	Insignificant influence	Large influence
Charge carrier mobility	$> 100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$	$\leq 1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in disordered OSC
Typical channel length	$< 1\,\mu\mathrm{m}$	$> 1\,\mu\mathrm{m}$
Typical supply voltage	$< 5\,\mathrm{V}$	$> 10\,\mathrm{V}$
Typical V_T	$< 1\,\mathrm{V}$	$> 1\,\mathrm{V}$

2.8 Conclusion

A broad overview of organic semiconducting materials and their charge transport models have been discussed. The different architectures that are used to realize an OTFT have been introduced. Throughout this work, we will use, top-gate top-contact devices for circuit realization. From the operation point of view, OTFTs have more commonalities with crystalline-Si devices but with some differences mainly due to the non-band like hopping transport mechanism. Model equations that describe the behaviour of an OTFTs was presented and a methodology to extract the key transistor parameters using iterative non-linear optimization method was explained.

3 Variability in OTFTs

Contents

Most of the recent works in OTFTs have focused on enhancing the field-effect mobility of charge carriers in OSCs. However, for a successful commercialisation of products using organic electronics, the ability of OTFTs to sustain their electrical performance under continuous operation over a reasonable time period is very critical. In this chapter, the variability issues that affect OTFTs are studied in detail. This chapter is organized as follows. In Section 3.1, the sources of variation in organic transistors are discussed. In the next section (Section 3.2), the spatial variability i.e. process variations of an OTFT are discussed. Section 3.4 describes the bias-stress instabilities in an OTFT. Finally, the chapter concludes with a brief summary.

3.1 Sources of Variability

Organic thin-film transistors (OTFT) suffer significantly from parameter variations that severely affects the yield and reliability of organic circuits. A broad classification of the various sources of variation in OTFTs is shown in Figure 3.1. The parameter variations

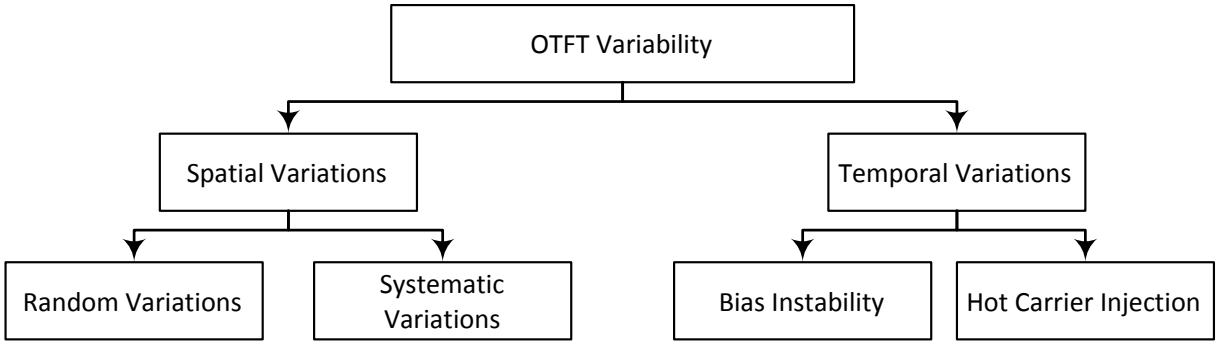


Figure 3.1: Overview of the classification of different sources of variations in OTFTs.

in an OTFT can be broadly classified into time-zero or instantaneous variations and variations that affect the circuit over a time period. The former type is also known as spatial variations and the latter type if also known as temporal variations.

3.1.1 Spatial Variations

The spatial variations are permanent variations that occur at time zero and are collectively responsible for the process variations occurring in organic technology. The major sources of instantaneous or spatial variations in an OTFT are summarized below:

- **Front-end Variability**: Generally, the intrinsic sources of variability in OTFT arise from random variability associated with the fabrication processing steps. Unlike the highly controlled optics based photo-lithographic fabrication process, the organic printing technology is a completely mechanical process that involves a lot of moving parts. These moving parts cause mechanical vibrations that lead to alignment inaccuracies. These alignment inaccuracies of the printing processes cause variations in the dielectric thickness, deviations in the width and length dimensions [Sir+06].
- **Back-end Variability**: Organic circuits use printed metal conductors as interconnections. The alignment accuracies and corner rounding adds to the process variability. Furthermore, due to the process variations, the via resistivity is also prone to vary from device to device.
- **Structural Defects**: Structural defects in amorphous organic polymers arising as a result of chemical synthesis, thermal and photo-induced defects cause inherent micro-structural disorder in thin films of polymers [SC06] and this has a significant effect in the electrical behaviour of OTFTs. In addition to these, the organic materials and the changes occurring in the semiconductor/dielectric interface also add to the process variations. These include variations in contact resistance [Pan+13b], dielectric roughness [Ste+04] and film morphology [DM02; LKL98].
- **Environmental Impurities**: Several experimental studies of P3HT-based OTFTs have demonstrated that oxygen present in air leads to an inadvertent doping of the semiconducting film. This leads to various noticeable effects that includes increased conductivity [Tay+91; Abd+97], decreased field-effect mobil-

ity [Abd+97], shift in threshold voltage (also referred to as switch-on voltage) [Mei+02] and a shift in the sub-threshold slope [Mei+02] of the transistor. The other commonly available environmental impurity comes from the water molecules present in the atmosphere. The water molecules are also known to have exacerbated the gate-bias instability in organic devices [Mat+99; Cha+06]. In addition to these factors, other environmental impurity atoms like dust particles also add to the statistical variation of electrical parameters in an OTFT.

3.1.2 Temporal Variations

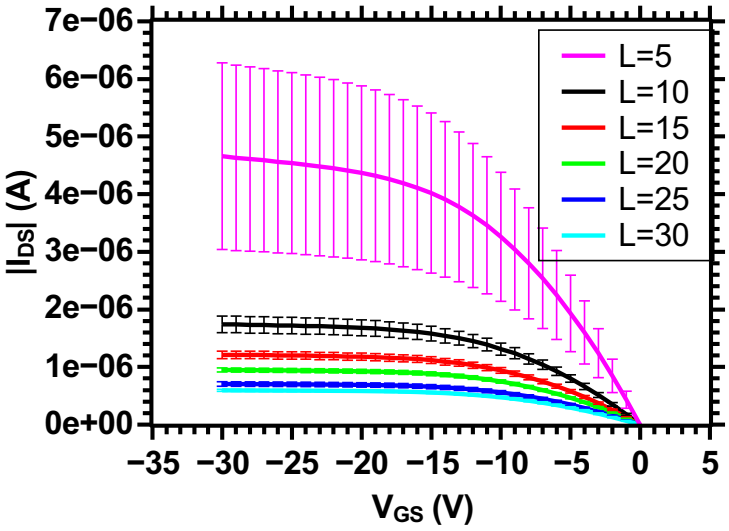
Unlike the spatial variations, temporal variations occur over a time for e.g. bias stress effects and hot carrier injection that are described in detail below:

- **Bias-Stress Instability**: Electrical instability, which has been extensively investigated and reported in a-Si semiconducting material [KWK08; LK93], manifests itself as a degradation of the output current with the prolonged operation of OTFTs. It is also referred to as bias stress effects. Bias stress effects can be due to the structural degradation of the organic semiconducting material in which case it leads to a decrease in the carrier field-effect mobility (μ_{FE}) of an OTFT. Bias stress effects can also be due to the trapping of mobile charge carriers in non-conducting states present in the dielectric, OSC or at the dielectric/OSC interface. In this case, it leads to a time-dependent shift in V_T [SC06] of an OTFT. The accumulation of the bias-stress effect induced instabilities over time is primarily accountable for the deterioration in the reliability of organic devices and circuits.
- **Hot-Carrier Injection**: Hot-Carrier Injection (HCI) is a phenomenon common to any solid-state electronic devices where the charge carriers (electrons or holes) gain sufficient energy and get injected into the gate dielectric leading to a permanent change in the V_T of a transistor.

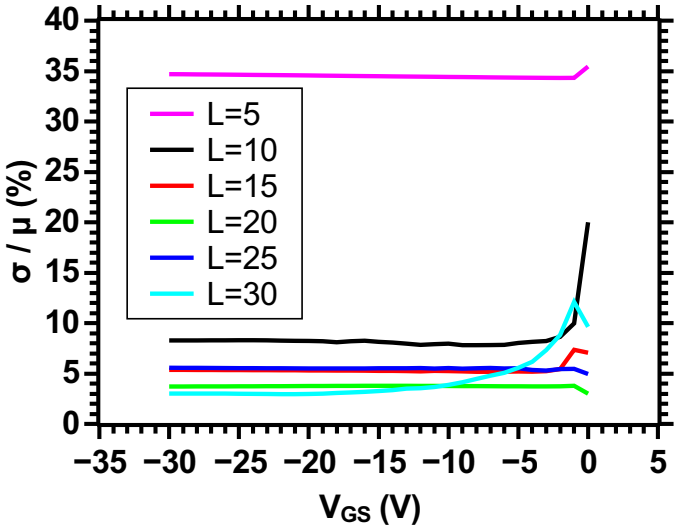
3.2 Spatial Variability

Spatial variability or process variability is of paramount concern as they lead to a deviation in the performance of organic circuits from its original intended performance. Process variations translate to variations in the key electrical parameters of OTFTs and consequently reduce the parametric yield of organic circuits. Process variability has been found to cause up to 25% variation in the drain-source current of an OTFT. The mean and standard deviation of the drain-source current of an OTFT for various length and width dimensions are shown in Figure 3.2 and 3.3 respectively. The variation in drain-source current of OTFTs with various lengths have been measured and the ratio between its standard deviation and mean is plotted in Figure 3.2(b). As the length of an OTFT is scaled down, the size of the impurities become comparable to the length dimensions and this leads to a relative increase in the variation of the drain-source current of the OTFT. This can be clearly observed in Figure 3.2(b) where the impact of process variations increase as the the channel length is scaled down. The width of the OTFTs are usually much larger in several millimetres and therefore, scaling the width

dimension is not as critical as scaling the length dimension. This general trend is shown in Figure 3.3(b).



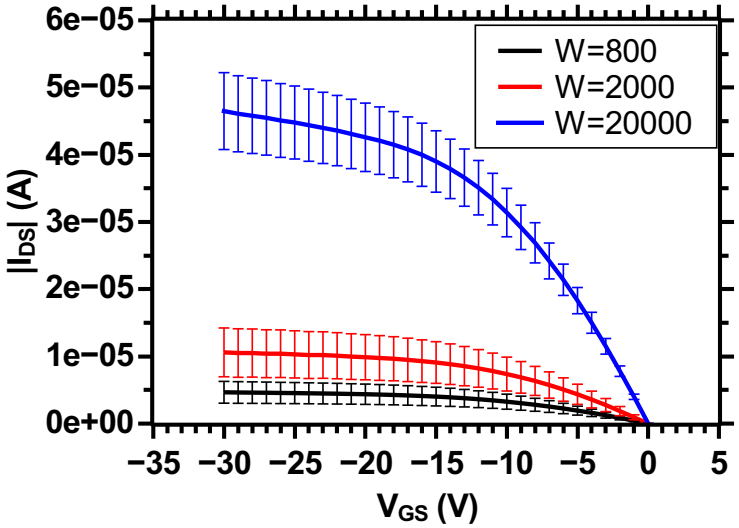
(a) Mean (μ) and standard deviation (σ) of the drain-source current of an OTFT



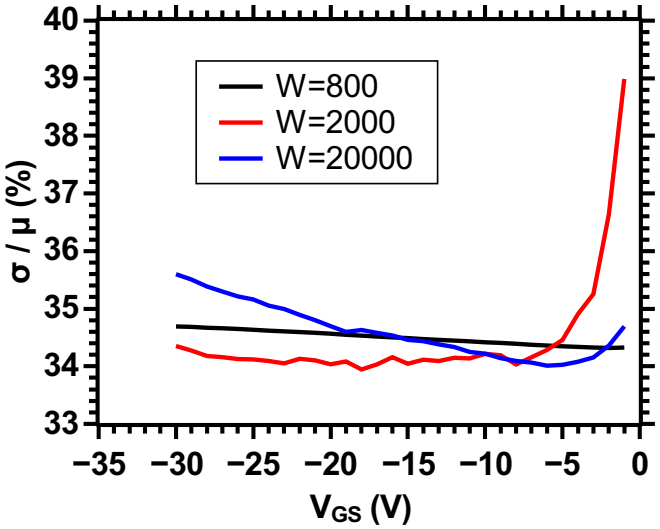
(b) Relative standard deviation of the drain-source current in percentage

Figure 3.2: Mean (μ) and standard deviation (σ) of the drain-source current of an OTFT with a fixed width (W = 800 μm) and various length (L) dimensions. The length dimensions are given in μm.

Process variations are typically divided into two components: systematic and random variations. The systematic variations also known as global variations have a larger spatial correlation distance and produce a systematic impact over a substrate or a batch. They, in general, cause a shift in the mean value of the electrical parameters of an OTFT. In contrast, the random variations also known as local variations are uncorrelated and accounts for variation in the electrical performance of the transistor with reference to an adjacent transistor on the same substrate. They are also called mismatch variations. The



(a) Mean (μ) and standard deviation (σ) of the drain-source current of an OTFT



(b) Relative standard deviation of the drain-source current in percentage

Figure 3.3: Mean (μ) and standard deviation (σ) of the drain-source current of an OTFT with a fixed length (L = 5 μm) and various width (W) dimensions. The width dimensions are given in μm.

mismatch variations can be sub-divided into short-range (between adjacent transistors) an across-chip (over a few transistors) variations. The short-range mismatch variations occur between adjacent transistors and the across-chip variations span over a few transistors. The global and local variations are also responsible for the inter-substrate and intra-substrate variations. Therefore, in an organic technology, two identical transistors placed side by side have different electrical characteristics owing to the process variability, resulting in intra-substrate device and circuit performance variability. Therefore, it is critical to characterize and accurately model process variability which can be then used to predict the statistical performance of organic circuits.

3.2.1 Characterization of Process Variations

In this section, we analyse the dependence of the process variations in an OTFT on its location in a given substrate. This can help in identifying the high impact regions that are much affected by process variations. This information will be handy in formulating a strategy for effective placement of organic circuits. It is not just important to find the magnitude of process variation but also to find the location of high impact on a given substrate. This will allow a circuit designer to avoid the region which is much affected by process variations particularly when it comes to analog circuits that demand high matching characteristics. To characterize the process variability in OTFTs, 100 identical OTFTs with a width (W) of 800 μm and a length (L) of 5 μm were fabricated on a single substrate. The OTFTs were laid out in 10 rows and 10 columns.

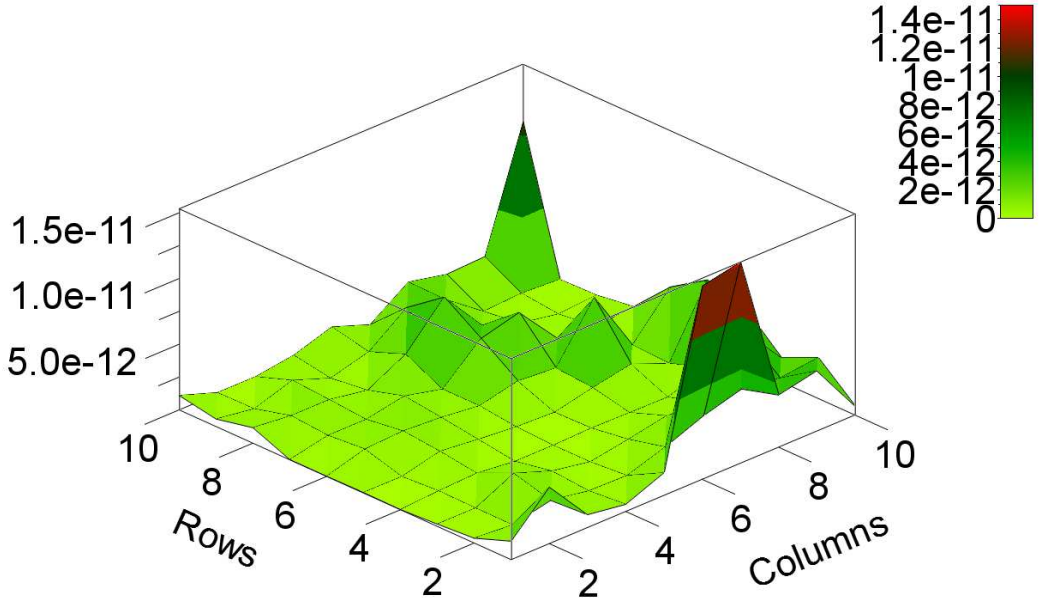
3.2.1.1 Intra-Substrate Distribution

All the OTFTs were measured and their respective output transfer characteristic curves were recorded. From the recorded output curves, the mean values were calculated. For a given V_{GS} and V_{DS} value, the square of the error between the measured current of an OTFT and the corresponding mean value is calculated. Similarly, the squared error is calculated for all V_{DS} from 0 V to V_{DD} with a fixed V_{GS} of V_{DD} and the sum of all squared error is calculated for a given OTFT. The sum of squared error (SSE) for i^{th} transistor is shown in Equation 3.1.

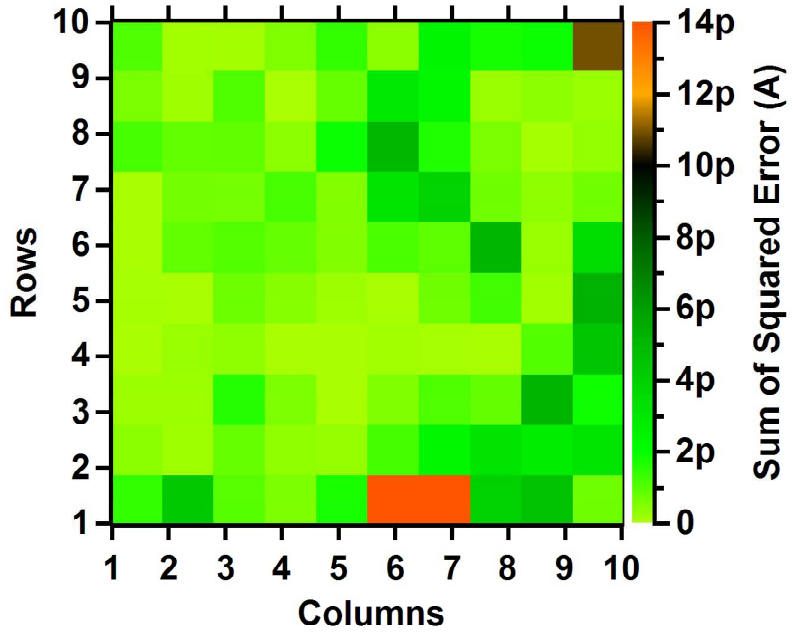
$$SSE_i = \sum_{V_{DS}=0}^{V_{DD}} \left(I_{DS,i}(V_{DS}, V_{GS}) - I_{DS,mean}(V_{DS}, V_{GS}) \right)^2 \tag{3.1}$$

The value of SSE is calculated for all the 100 OTFTs on a given substrate and this results in a matrix of 10x10 values. Such a matrix containing 100 SSE values was calculated for two substrates namely A and C. The sum of squared error (SSE) of all 100 OTFTs on substrate A and C is shown in Figure 3.4 and 3.5 respectively. In these figures, the maximum SSE values are clipped at a maximum of 14 pA. and such values are represented in red colour in the figures. The figures show that the sum of squared error is smaller at the centre and is higher at the periphery. This shows that the impact of process variations increases as we move from the centre of a substrate towards its edges. This increase in process variations, as we move from the centre towards the edges, could be explained by a radial gradient in the thickness of the spin coated dielectric and semiconductor layers.

To visualise the across-chip variations inside a given substrate, the row-wise and column-wise distribution of process variations in a given substrate are analysed. For the row-wise distribution, the mean and standard deviations of the output curves for all 10 OTFTs in each row were calculated. The procedure was repeated for column-wise distributions. The results are depicted in Figure 3.6. In this figure, the variation of the mean value across rows and columns represents the systematic variation component. The standard deviation denoted by bars represents the random variation component. The OTFT with the least variation lies more or less at the middle of the substrate.



(a) Side view

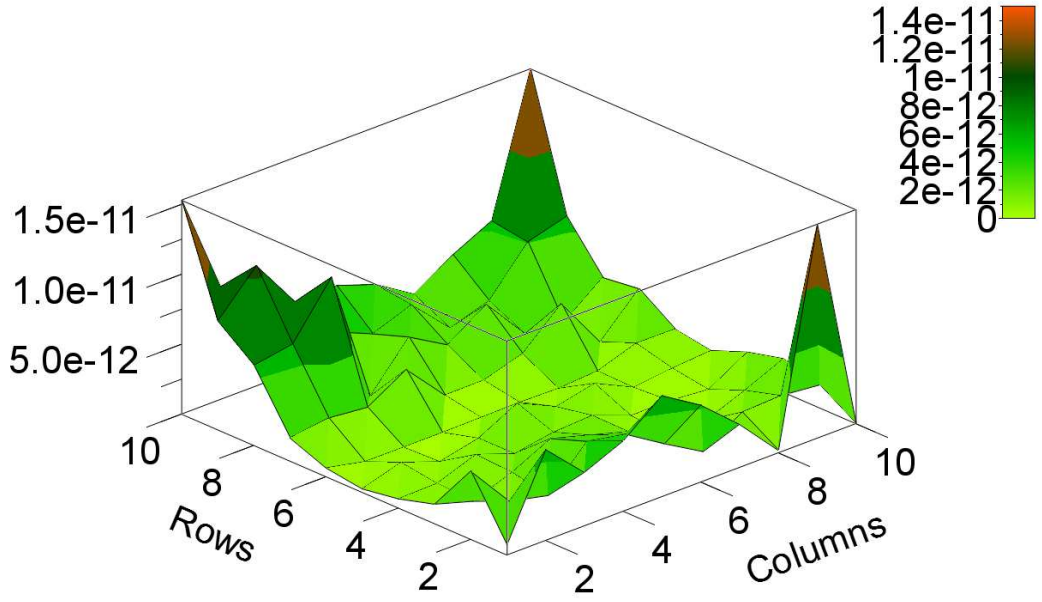


(b) Top view

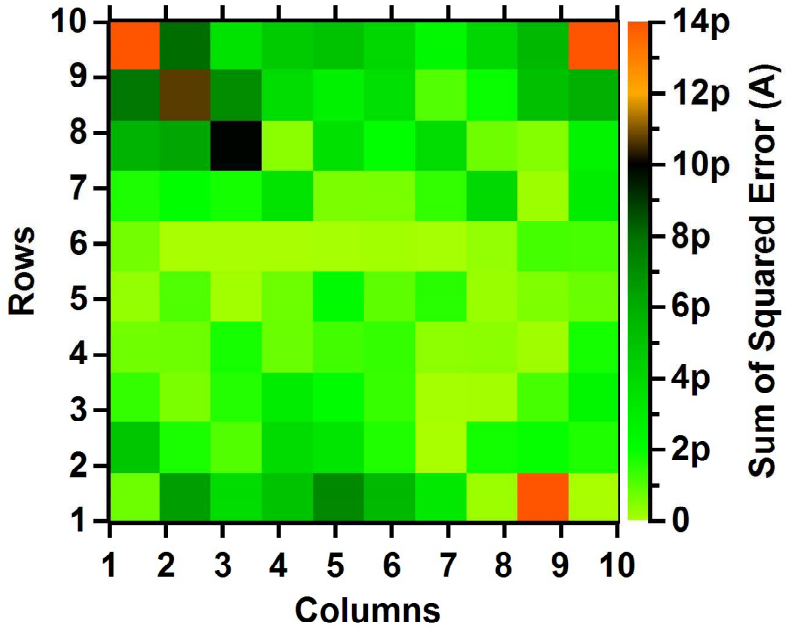
Figure 3.4: Colour plots showing the distribution of variation in the drain-source currents of 100 OTFTs on substrate A.

3.2.1.2 Inter-Substrate Distribution

To get an insight into the inter-substrate variation, the substrates A and C were compared. The SSE values for both the substrates, calculated in Sec. 3.2.1.1, were normalized. Then, the difference in the normalized SSE values between the two substrates



(a) Side view



(b) Top view

Figure 3.5: Colour plots showing the distribution of variation in the drain-source currents of 100 OTFTs on substrate C.

were determined and this value represents the variation in the drain-source current of any two OTFTs at a same location from two different substrates A and C. Any two OTFTs from the same location on substrates A and C are considered to be dissimilar when their difference in normalized SSE value is greater than 2 pA. The results are illustrated in

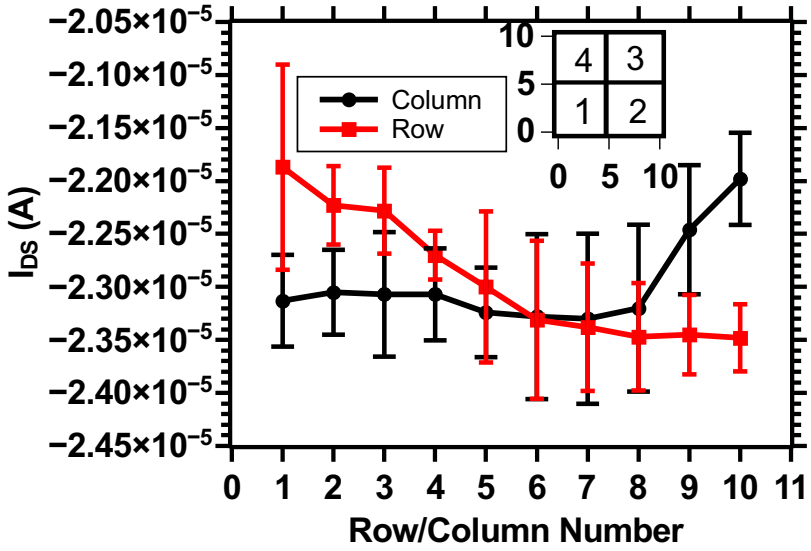


Figure 3.6: Measured row-wise and column-wise variation of the drain-source current for $V_{GS} = V_{DS} = V_{DD}$.

Figure 3.7. The green coloured pixels indicate the inter-substrate similarities. On the other hand, the black coloured pixels represent the inter-substrate dissimilarities.

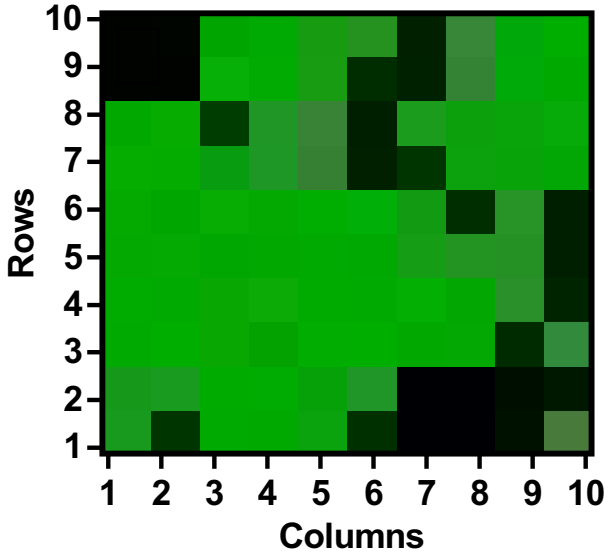


Figure 3.7: Colour plot showing the distribution of inter-substrate variation between substrates A and C. The green and black coloured pixels indicate the inter-substrate similarities and the inter-substrate variations respectively.

3.2.2 Statistical Model for Process Variations

The parameter variations in silicon devices have been extensively studied over the last two decades and there exists adequate information [PDW89; Ger89; MI92; PTV98; LHC86; FNSV94] to deal with these phenomena. With respect to organic electronics only a handful of work exists in this area. These works [Pan+13a; Gay07] initially

measure the current of a few identical transistors placed on the same substrate. They are then fitted with the OTFT current equations to extract the fitting parameters. The parameter extraction procedure used in this method is based on non-linear curve fitting methods. Then, the statistical distribution governing each of these model parameters is calculated. The Monte-Carlo simulations are carried out by statistically varying each of these OTFT model parameters and superimposing them to get the total variation in the current of the OTFT. This traditional approach is shown in Fig. 3.8. This approach has two main disadvantages. Firstly, it does not consider the correlation between different OTFT model parameters namely $\gamma, V_t, \beta, \lambda$. Secondly, it uses non-linear optimization methods to extract the model parameters which suffers from convergence issues and often leads to a solution that is not the global minimum. Thus the distribution of the extracted model parameters do not represent the measured process variations accurately. Moreover, these works do not make a distinction between global and mismatch variation. Since the design of analog circuits is based on transistor ratios rather than their absolute values, the mismatch variations are very critical for the analog circuits. The above issues can be best approached by directly finding the statistical parameters governing the global and mismatch variations in the drain current (I_{DS}) of an OTFT.

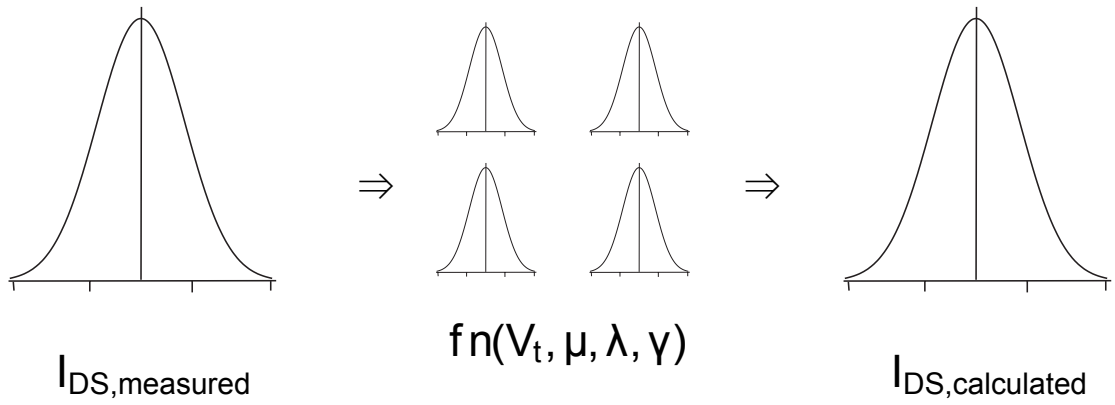


Figure 3.8: Overview of the existing statistical modeling approach

3.2.2.1 Generalized Statistical Model for OTFT Process Variability Modelling

Here, a statistical model of the drain-source current of an OTFT describing both global and local variation components is described. The process variations in an OTFT comprise of two components: (a) global variations that occur over an entire substrate and (b) local variations that are restricted to adjacent transistors or between transistors lying in a small area on a given substrate. Mathematically, let us assume that $\Delta_{glo,i}$ and $\Delta_{loc,i}$ are the random variables that represent the global and local variations in the drain-source current of i^{th} transistor respectively. The combined mean of the drain-source current of all the 100 OTFTs on a given substrate is denoted by $I_{DS,mean}$. In the ideal case, when there are no process variations, the current ($I_{DS,i}$) of i^{th} transistor is equal to the global mean $I_{DS,mean}$. Therefore, the ratio of $I_{DS,i}$ over $I_{DS,mean}$, represented by Equation 3.2, is equal to one. However, due to the process variations $I_{DS,i}$ may not be equal to $I_{DS,mean}$. It must be noted that since we compare the current of each transistor

with the global mean over the entire substrate, the ratio of $I_{DS,i}$ over $I_{DS,mean}$, represented by Equation 3.2, gives the amount of variation in the drain-source current of ith transistor due to the global component ($\Delta_{glo,i}$) of the process variation. Here, the local component of process variation is assumed to be negligible when compared to the global component.

$$\Delta_{glo,i} = \frac{I_{DS,i}}{I_{DS,mean}} \quad \Big| \quad i = 1 \cdots n \tag{3.2}$$

We assume that the process variations follow a Gaussian distribution. The distribution of the global variation component is shown in Fig. 3.9. This can be fitted with a Gaussian distribution. It can be observed from the figure that the mean of this distribution lies around unity.

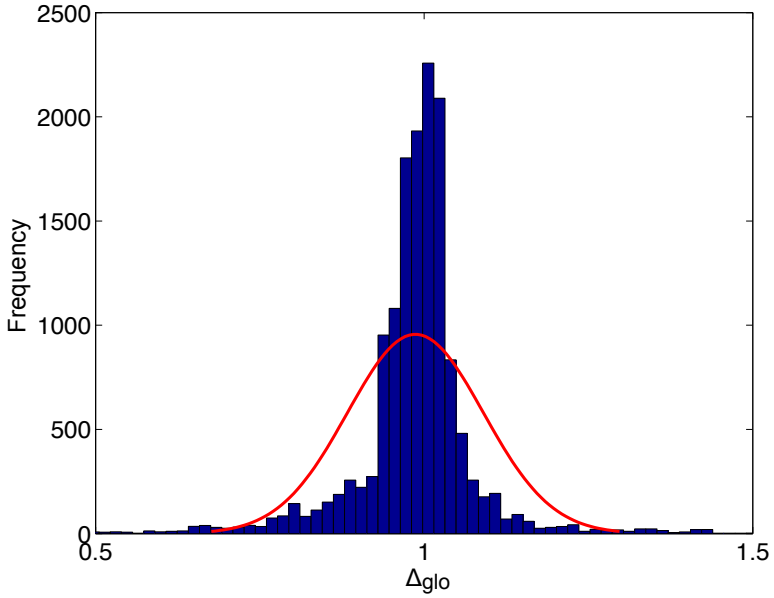


Figure 3.9: Histogram of process variation with Gaussian distribution envelope

Equation 3.3 provides the local variation component of the process variations.

$$\Delta_{loc,ij} = \frac{I_{DS,j}}{I_{DS,i}} - \frac{\Delta_{glo,j} + \Delta_{glo,i}}{2} \quad \Big| \quad i, j = 1 \cdots n \tag{3.3}$$

In the above equation, $\Delta_{loc,ij}$ represents the local component of process variations, $I_{DS,i}$ and $I_{DS,j}$ represent the drain-source current of jth and ith transistor respectively. $\Delta_{glo,j}$ and $\Delta_{glo,i}$ represent the local component of process variations for jth and ith transistor respectively. When the j^{th} transistor lies adjacent to the i^{th} transistor, $\Delta_{loc,ij}$ denotes the mismatch variations. When the j^{th} transistor lies far away from the i^{th} transistor, the value from Equation 3.3 corresponds to the across-chip random variation. The first term ($I_{DS,j}/I_{DS,i}$) represents the total variation between the two transistors. This includes both the global and local components of process variation. Therefore, to obtain the

corresponding local variation term, the average of the global component (second term in Eqn. 3.3) is subtracted from the total variation term ($I_{DS,j}/I_{DS,i}$). In the ideal case, when there are no local variations, the drain current $I_{DS,j}$ is equal to $I_{DS,i}$, and the global variation parameters $\Delta_{glo,i}$ and $\Delta_{glo,j}$ are equal to one. Thus the value of $\Delta_{loc,ij}$ is zero for the ideal case. The local (mismatch) variation between the i^{th} transistor and every other transistor on the substrate is calculated. This step is repeated for all i between 1 to n. The resulting values are fitted with a Gaussian distribution to find the mean (μ) and standard deviation (σ) of the random variation component. This includes both short-range and across-chip random variations.

The impact of process variations were compared on three different substrate samples namely A, B & C. To check the correctness of the statistical model, substrate sample B was fabricated using a different process and material compared to that used for fabricating samples A and C. All the samples contain 10×10 identical OTFTs with similar W and L dimensions. The mean and standard deviation of the statistical distribution corresponding to both the global and local variations for all the three samples are shown in Table 3.1. The values from substrate A and C closely match each other but differ from the values obtained from substrate B. The relatively large standard deviation for substrate B indicates that the process used for substrate B suffers from a relatively large process variation. The values shown in Table 3.1 represent the intra-substrate variation within the given substrate. One can also find the distribution governing the variation between different substrates which will give the inter-substrate variation component. Owing to the large number of substrates required to have a distribution with a decent accuracy, the distribution of inter-substrate variation is not calculated.

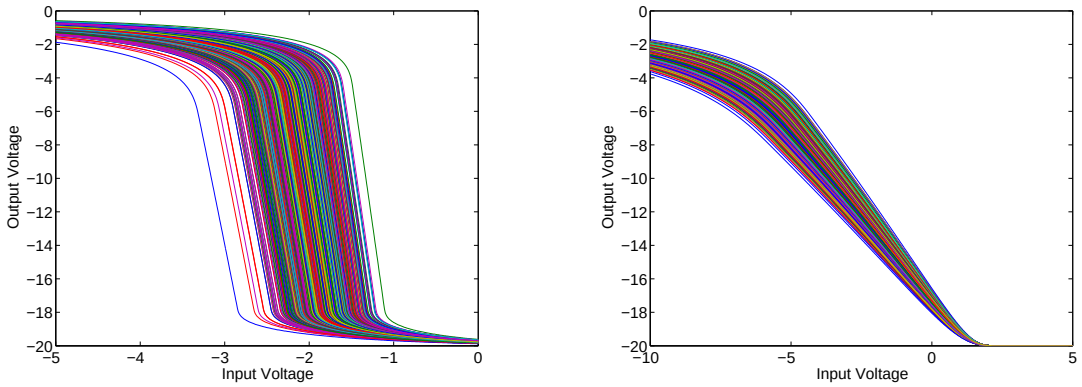
Table 3.1: Statistical distribution of process variations for different substrates

Substrate	Global Variation		Local Variation	
	μ	σ	μ	σ
A	0.98	0.10	0.0076	0.1072
B	0.95	0.22	-0.0115	0.2169
C	0.99	0.14	0.0077	0.0964

The drain-source current of an OTFT including the global and local variations can be modelled using Equation 3.4, where I_{DS0} is the drain-source current calculated from Equation 2.5 and Equation 2.6.

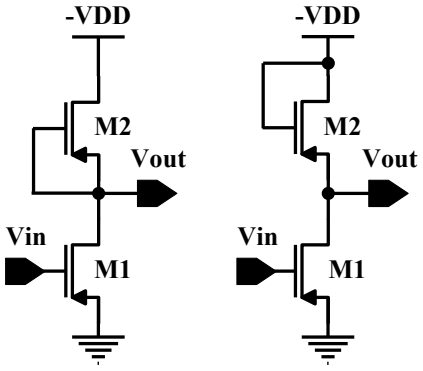
$$I_{DS} = I_{DS0} \cdot \Delta_{glo} \cdot (1 + \Delta_{loc}) \tag{3.4}$$

Figure 3.10 shows the Monte-Carlo simulations of zero-V_{GS} and diode load inverters. For the Monte-Carlo simulations, Δ_{glo} and Δ_{loc} in Equation 3.4 are varied according to the distributions that are specified in Table 3.1.



(a) Zero-V_{GS} load inverter (b) Diode load inverter

Figure 3.10: Monte-Carlo simulations showing the voltage transfer characteristics of (a) zero-V_{GS} load inverter and (b) diode load inverter extracted from 1000 iterations.



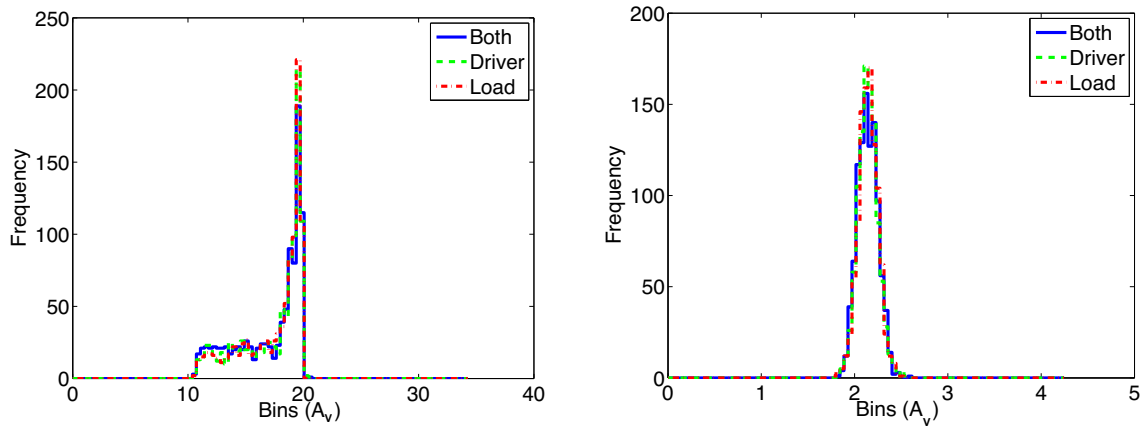
(a) (b)

Figure 3.11: Schematic of a) zero-V_{GS} load and b) diode load inverter circuit.

3.3 Impact of Process Variations on Organic Circuits

The statistical model describing the process variations, in addition to estimating the yield, can also be used to study the impact of process variations on various parts of a circuit topology. For instance, a simple circuit like an inverter consists of a driver and a load structure. The process variations can be used to find which of these are critical for a given performance specification like gain. Two commonly used inverter topologies namely zero-V_{GS} and diode load inverters were used for the analysis. The working of these inverters are explained in Chapter 4.

Monte-Carlo simulations were performed for both inverter types. The simulation model used both the global and local mismatch variations. We performed 1000 iterations of Monte-Carlo simulations for each of the three different configurations: when the global and mismatch variations were applied to a) driver alone, b) load alone and c) both driver and load. From the voltage transfer characteristic curves obtained from the Monte-Carlo simulations, the values of gain for each case were calculated. For a



(a) Zero-V_{GS} load inverter (b) Diode load inverter

Figure 3.12: Distribution of gain of (a) zero-V_{GS} load inverter and (b) diode load inverter extracted from 1000 iterations of Monte-Carlo simulations.

given inverter, the mean and standard deviation of the gain parameter for each of the cases was determined. Figure 3.12(a) and Figure 3.12(b) illustrate the distribution of the gain for zero-V_{GS} load inverter and diode load inverter respectively. The mean and standard deviation of the distributions are shown in Table 3.2 for zero-V_{GS} load inverter and in table Table 3.3 for diode load inverter. The Var values in Table 3.2 and Table 3.3 represent the variation in the mean value of a given parameter from that of the corresponding ideal case without process variations. This variable is used to measure the impact of process variations. When an inverter is used as an amplifier, the zero-V_{GS} load inverter provides a high gain. However, the variation in gain due to the process variations is higher in the case of a zero-V_{GS} load inverter compared to a diode load inverter. This is because the gain in the case of a zero-V_{GS} load inverter given by $A_V = -g_{m1}r_o$ is directly proportional to the current flowing through the inverter, whereas for a diode load inverter, the gain ($A_V = -g_{m1}/g_{m2}$) is independent of the current. It should be noted that the small signal gain (g_m) is directly proportional to the current flowing (I_{DS}) through the inverter i.e. $g_m = 2I_{DS}/V_{GS} - V_t$. Therefore, the gain is given by $A_V = -(V_{GS1} - V_t)/(V_{GS2} - V_t)$. Here, the change in V_t due to the process variations is very small compared to the gate-source voltages. Hence, the diode load inverters are least affected by process variations when considering to be used as amplifiers. This is clearly evident from the values in Table 3.3. The results in Table 3.2 shows that the variation in gain is larger when the process variations are introduced to the driver transistor compared to the load transistor.

3.4 Temporal Variability

Temporal variability leads to variations in the electrical behaviour of organic circuits and transistors after they have been fabricated. These variations become apparent after prolonged application of bias voltages. The impact of these variations on organic circuits can be temporary (reversible) or permanent (irreversible). The permanent irreversible factors complement the ageing effect in organic circuits. One of the key sources

Table 3.2: Mean and standard deviation of the Gaussian fit for the distributions shown in Figure 3.12(a) corresponding to the zero-V_{GS} load inverter. $\%Var$ denotes the variation in the mean value of gain from that of the corresponding ideal case with no process variations.

Configuration	μ	σ	$Var(\%)$
both	16.93	2.83	11.7
driver	17.18	2.71	10.4
load	17.28	2.62	9.8

Table 3.3: Mean and standard deviation of the Gaussian fit for the distributions shown in Figure 3.12(b) corresponding to the diode load inverter. $\%Var$ denotes the variation in the mean value of gain from that of the corresponding ideal case with no process variations.

Configuration	μ	σ	$Var(\%)$
both	2.12	0.11	0.2
driver	2.12	0.10	0.2
load	2.12	0.10	0.2

of temporal variability is the bias-stress instability. This is similar to the Bias Stress Instability (BTI) effect in crystalline Silicon devices. Unlike the BTI effect, which becomes significant at elevated temperatures, the bias-stress effects in OTFTs are prevalent even at normal operating temperatures. An OTFT operated under normal temperature conditions exhibits a gradual decrease or increase in its channel current even under constant bias conditions.

3.4.1 Charge Trapping in OTFTs

In an OSC, the band edges of HOMO and LUMO are not sharply defined and there exists trap levels between these bands. These traps can be classified into deep and shallow traps depending on whether their energy level, with respect to the LUMO (valence band), is far or near. As V_{GS} is made more negative, the fermi energy level (E_F) moves towards the LUMO. This leads to an accumulation of the mobile charge carriers and they start filling the deep traps. Though these charge carriers are mobile, they have a very low mobility as they need to overcome a high barrier to hop to other energy levels [Deb09]. Finally, when V_{GS} approaches V_T, the charge carriers fill the shallow traps. Now, the charge carriers can move relatively easily and hence contributes to a current flow.

Bias-stress instability is presumably due to the trapping of mobile charge carriers in pre-existing or stress-generated non-conducting states in the dielectric or at the dielectric/OSC interface and/or inside the organic semiconducting (OSC) layer [SSC03; Par+13; Sir09]. Bias-stress can also be due to a structural degradation of the semiconductor material which will also lead to a decrease in μ_{FE} [Deb09]. The trapping rate should be limited by either the defect creation rate or the barrier level that needs to be overcome to trap a carrier in an existing defect [Deb09]. The effect of the different

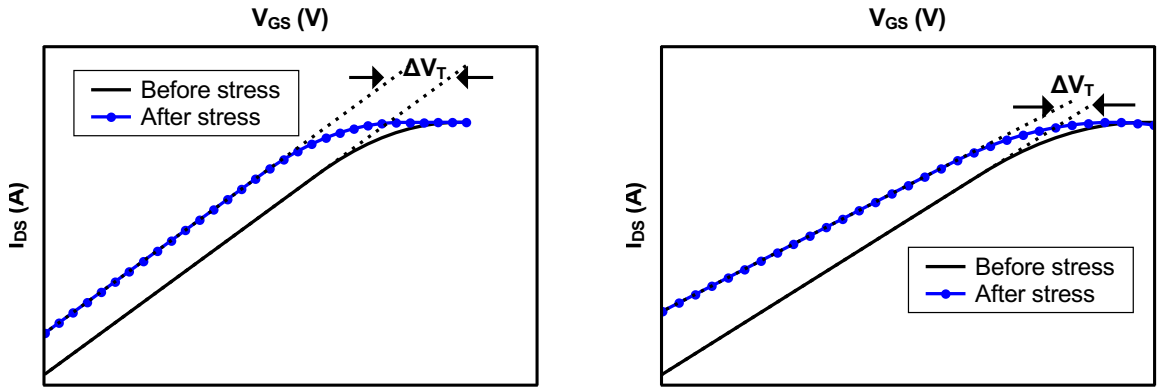
trapping processes can be clearly seen in the transfer characteristic curves by comparing their shapes before and after the application of bias-stress. Carriers trapped in the dielectric, in localized non-conducting states at the dielectric/semiconductor interface or in deep states in the OSC form an immobile charge density distribution which shields the gate voltage [SC06]. The transfer curve is identical to that of a pristine device when V_{GS} overcomes this electrostatic screening and this type of degradation gives rise to a shift in V_T that is given by:

$$\Delta V_T = N_{trap}/C_i \tag{3.5}$$

where N_{trap} is the density of the filled traps. The field-effect mobility and subthreshold swing are not changed and therefore, there is no change in the overall shape of the transfer characteristics as shown in Figure 3.13(a). On the other hand, if the bias-stress causes creation of new shallow trap states, the shape of the transfer characteristics of a transistor is affected in addition to causing a shift in its V_T. Subthreshold swing is an important parameter that can be used to study the subtle changes in the shape of a transfer characteristic curve. The subthreshold swing, given in Equation 3.6, is defined at the inverse subthreshold slope and corresponds to:

$$S_{sw} \approx \frac{k_B T}{q}\left(1 + \frac{q^2 N_{it}}{C_i}\right) \tag{3.6}$$

where N_{it} is the surface density of interface traps, $k_B T/q$ is the thermal voltage and C_i is the capacitance per unit area of the gate insulator. Since the subthreshold swing is inversely proportional to the interface trap density, the creation of new interface trap states, in addition to a shift in V_T of an OTFT, leads to a change in its subthreshold swing accompanied by a slight change in its field-effect mobility.



(a) (b)

Figure 3.13: Example of changes to the shape of the transfer curve obtained (a) when bias stress is due to the trapping of charge carriers in existing non-conducting states and (b) when bias stress is due to the trapping of charge carriers in the newly formed shallow donor-like states

In principle, both these bias-stress mechanisms may be observed in an OTFT. In contrast to a-Si devices, the exact trapping or defect creation mechanism is not well under-

stood in OSC devices. Moreover, different mechanisms might be active at different bias stress durations and for different polarities and magnitude of the gate field [SC06]. In the next section, the bias-stress effects are characterized for different stress durations and for different magnitudes of drain and source bias voltage.

3.4.2 Characterization of Bias-Stress Instability

In general, a threshold voltage shift possibly accompanied by a change in mobility has been an important indicator of bias-stress induced degradation in an organic TFT. This effect depends on the magnitude as well as on the time duration of the applied bias-stress voltages. The following section explains the measurement scheme used to characterize the bias-stress induced variations.

3.4.2.1 Measurement Scheme

In order to measure the time and bias dependence of the bias-stress induced shift in V_T of an OTFT, the measurement procedure described in Figure 3.14 is used. In this measurement procedure, firstly, the I_{DS}-V_{GS} (transfer) curves of the investigated OTFT are measured by sweeping its V_{GS} from 0 V to -V_{DD} with a constant V_{DS}. From the transfer characteristic curves, the initial threshold voltage (V_{T0}) of the OTFT is extracted. Then, the defined bias-stress voltage is applied to the drain-source terminal and gate-source terminal of the OTFT. The stress voltages are applied for a stress duration of T_{Stress}. After the time interval T_{Stress}, the stress voltages are removed and the I_{DS}-V_{GS} curves are recorded by momentarily sweeping V_{GS} from 0 V to -V_{DD} with a constant V_{DS}. Due to the bias-stress effects, the recorded I_{DS}-V_{GS} curves are different from those obtained before the application of stress voltages. The threshold voltage V_T is extracted from the I_{DS}-V_{GS} curves that were recorded after the stressing. This V_T when compared to V_{T0} will give a measure of the bias-stress induced shift in the threshold voltage of the OTFT. This process is repeated for various stress durations.

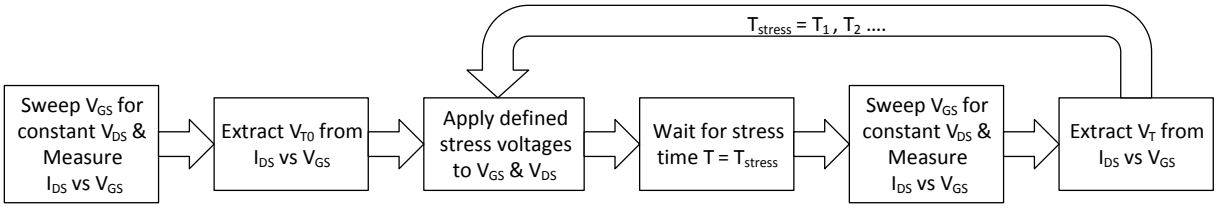


Figure 3.14: The typical measurement procedure applied to characterize bias-stress effects in an OTFT

3.4.2.2 Results and Discussion

The measurement procedure described in Section 3.4.2.2 is applied to an OTFT to study the effect of gate-bias stress voltage on its threshold voltage shift. Figure 3.15 compares ΔV_T as a function of T_{Stress} for various gate-bias stress voltages. The drain-bias voltage during the stress phase was held constant at -1 V. It can be observed from Figure 3.15

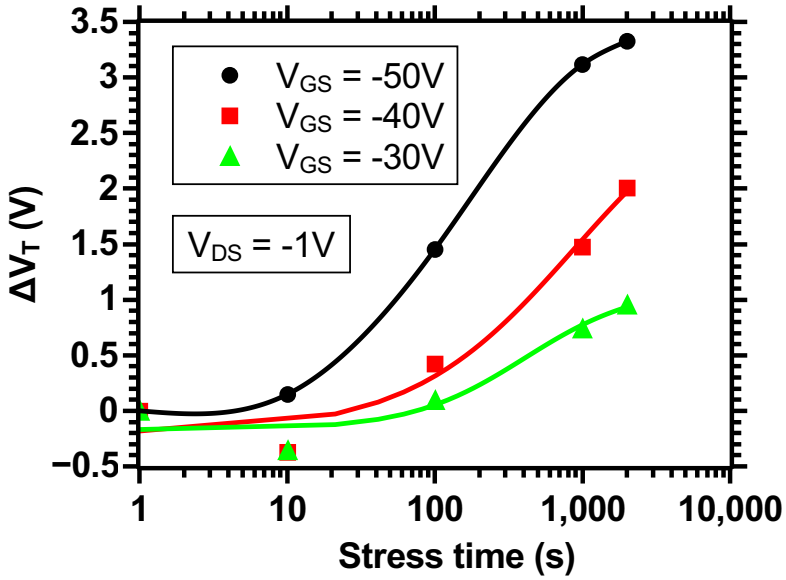
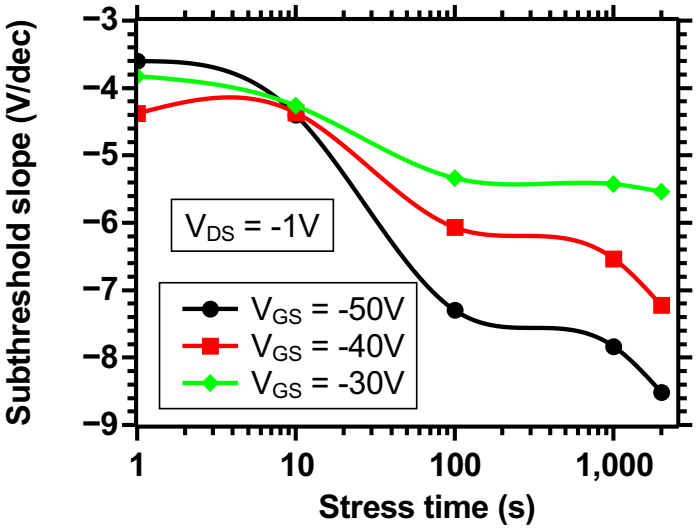


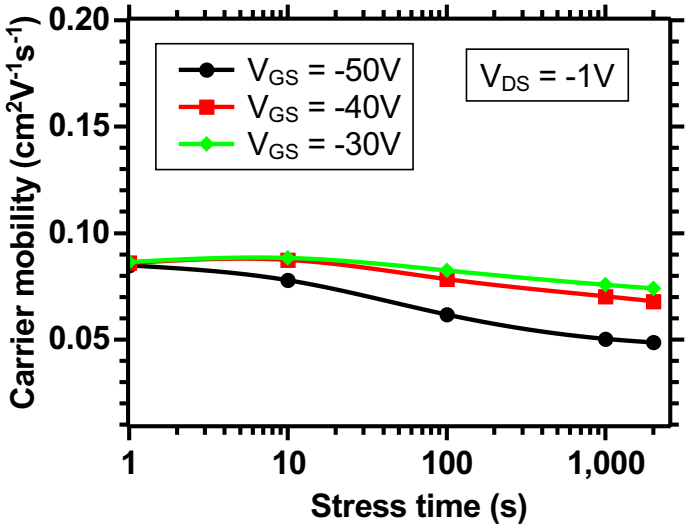
Figure 3.15: Shift in the threshold voltage as a function of stress time.

that the larger the magnitude of gate-bias stress voltage is, the larger the shift in threshold voltage. As explained in Section 3.4.1, the shift in threshold voltage results from the trapping of charge carriers in existing trap states or in newly created trap states. In addition, a larger gate-source voltage leads to a faster shift in threshold voltage. This is presumably because a larger gate-source voltage induces a larger density of charge carriers in the conducting channel. This increased charge carrier density, for a constant trapping rate increases the number of carriers trapped per unit time. Furthermore, the longer the gate bias is applied, the more carriers are trapped, and hence the larger shift in threshold voltage. It can also be noticed from Figure 3.15 that the ΔV_T tries to saturate beyond a stress duration of 1000 s. The subthreshold swing and field-effect mobility for the above stress measurements are shown in Figure 3.16(a) and 3.16(b). The shift in the subthreshold swing indicates that it involves creation of new defect states and the shift in V_T is caused by the trapping of charge carriers (holes) in these newly created defect states. It can also be noticed from Figure 3.16(a) that the shift in the subthreshold swing increases as the magnitude of gate-bias stress voltage becomes larger. This indicates that the defect creation increases with the magnitude of gate-bias stress voltage. The field-effect mobility for various gate-bias stress voltages shows a relatively small variation with the stress time.

To study the drain-source voltage dependence of the bias stress-induced threshold voltage shift, stress measurements were performed with a constant gate-source bias voltage of -15 V and with different drain-source bias voltages ranging from -1 to -25 V. The stress voltages were applied for a total stress time of 100 s. The results are illustrated in Figure 3.17 and it shows the bias-stress induced threshold voltage shift as a function of drain-source bias voltage. It can be seen from the figure that the bias-stress induced threshold voltage shift decreases as the magnitude of drain-source bias voltage is increased. This effect can be attributed to two primary reasons. First, a larger drain-source voltage decreases the charge carrier density in the vicinity of the drain contact and this reduces the number of carriers that are trapped in a given time dura-



(a)



(b)

Figure 3.16: (a) Shift in subthreshold-swing and (b) shift in field-effect mobility as a function of stress time when different gate biases (V_{GS} = -30, -40 and -50 V) was applied to the bias-stress measurement while the drain bias voltage was held constant at -1 V.

tion [ZK08]. Second, an increase in the magnitude of drain-source voltage with respect to the gate-source voltage lowers the barrier energy that needs to be overcome for the trapped charge carriers to get de-trapped[Zsc+09].

To determine the impact of bias-stress on OTFTs operated in a linear and a saturation regime, stress measurements were performed under two types of stress conditions namely high gate-field stressing and high drain-field stressing and their characteristics were compared.

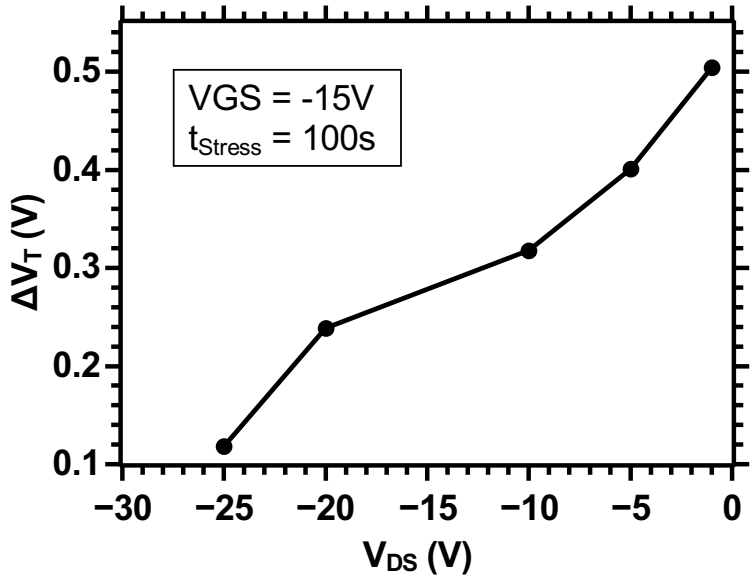


Figure 3.17: Shift in threshold voltage as a function of drain bias voltage for a stress time of T_{Stress} = 100 s. The gate bias voltage during the stress measurements was held constant at -15 V.

High Gate-field Stressing

A high gate-field stressing was performed by applying a relatively large gate bias with a very small drain bias as stress voltages to an OTFT. Characterisation of the OTFT was done before and after stressing at pre-selected time intervals. During the stressing phase, the gate bias V_{GS} was maintained at -30 V and the drain bias V_{DS} was maintained at -1 V. The OTFT was stressed upto 10000 s and then the OTFT was allowed to relax by removing all the stress voltages. The device was allowed to relax for 10000 s. Thus, the analysis was divided into two phases: a) stress and b) relaxation phases. Figure 3.18 shows the I_{DS}-V_{GS} characteristics of the OTFT before and after the application of high gate-field stress. The inset shows the magnified section of the I_{DS}-V_{GS} curve. Upon close examination, it can be observed that the nature of these curves is similar to that of Figure 3.13(b) which is characteristic of trapping in newly created defect states. The corresponding shift in threshold voltage is shown in Figure 3.19. The threshold voltage shift gets saturated beyond 1000 s and this is presumably due to the filling of all trap states, including pre-existing and newly created trap states. The relaxation phase is marked by two distinct regions: rapid decrease in ΔV_T followed by a gradual decrease in ΔV_T. The rapid decrease in ΔV_T that occurs immediately after the removal of stress conditions, is presumably due to the release of charge carriers trapped in shallow traps. The charge carriers trapped in deep states require a longer relaxation time or thermal annealing. The shift in the subthreshold swing and field-effect mobility of the OTFT for both the stress and relaxation phases are shown in Figure 3.20(a) and 3.20(b) respectively. The large variation in subthreshold swing corroborates our earlier observation of the creation of new defect states.

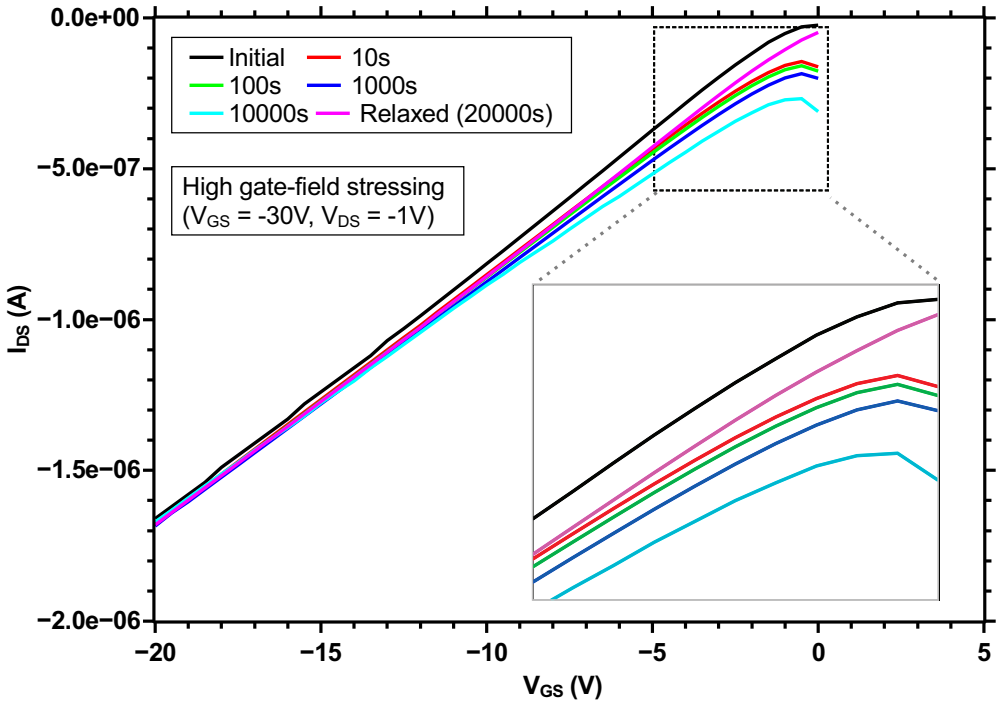


Figure 3.18: I_{DS}-V_{GS} (transfer) characteristics of an OTFT before and after application of bias stress during high gate-field stressing (V_{GS} = -30 V and V_{DS} = -1 V) at varying stress durations. The inset shows the magnified section of the curve lying between V_{GS} of 0 and -5 V.

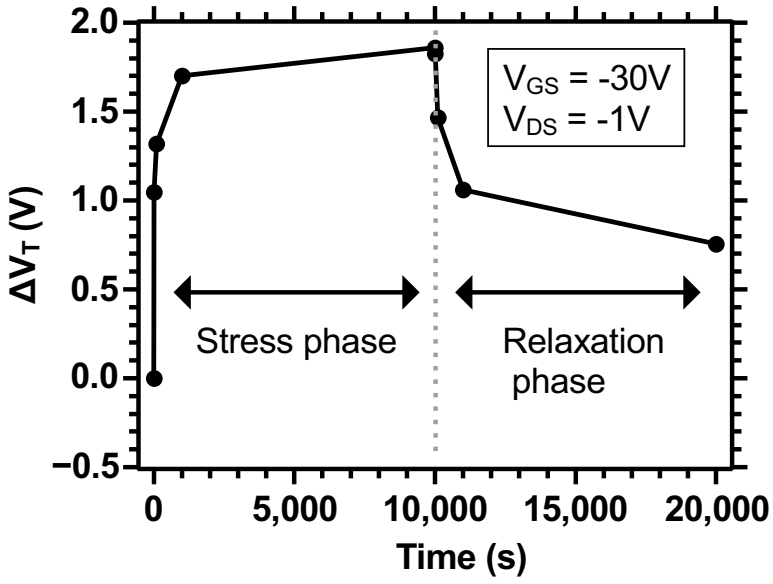
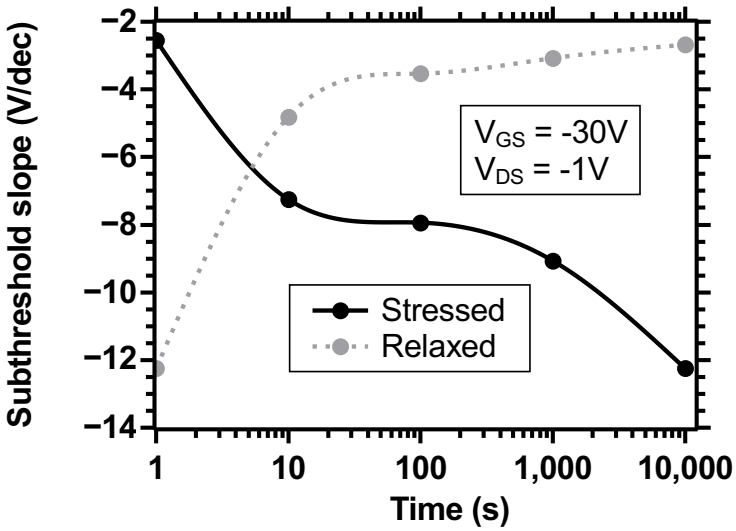
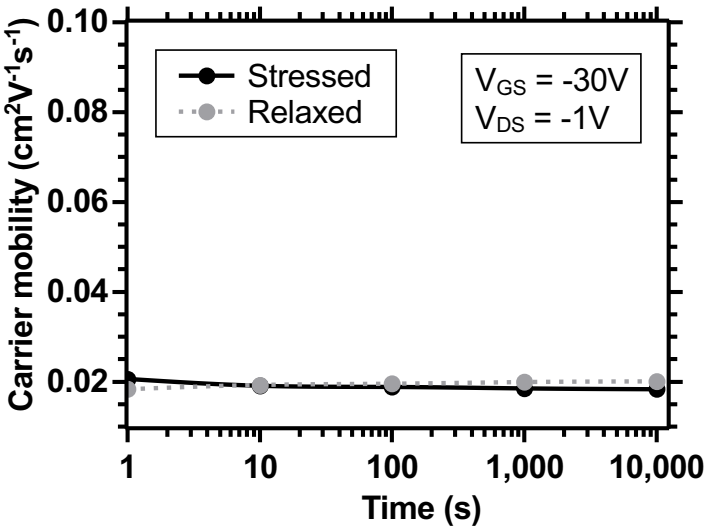


Figure 3.19: Shift in threshold voltage as a function of stress time for the case of a high gate-field stressing (V_{GS} = -30 V and V_{DS} = -1 V). The region from time t = 10000 s to 20000 s represents the relaxation phase where the stress conditions were removed and the OTFT is allowed to relax.



(a)



(b)

Figure 3.20: (a) Shift in subthreshold-swing and (b) shift in field-effect mobility of the OTFT as a function of stress time during the high gate-field stressing (V_{GS} = -30 V and V_{DS} = -1 V) for both stress and relaxation phases.

High Drain-field Stressing

Similar to the high gate-field stressing, a high drain-field stressing was performed by applying a drain bias that is relatively larger than the gate bias voltage. Characterisation of the OTFT was done before and after stressing at pre-selected time intervals. During stressing, the gate bias V_{GS} was maintained at -15 V and the drain bias V_{DS} was maintained at -25 V. Similar to the earlier measurement, the OTFT was stressed upto 10000 s and then the OTFT was allowed to relax for another 10000 s by removing all the applied stress voltages. Figure 3.18 shows the I_{DS}-V_{GS} characteristics of the OTFT before and after the application of high drain-field stress conditions. The inset shows the magnified section of the I_{DS}-V_{GS} curve. Upon close examination, it can be observed that the nature of the curves are similar to that of Figure 3.13(a) which is characteristic

of trapping in existing defect states. The comparison between the high gate-field and high drain-field stressing conditions are shown in Figure 3.22. It can be clearly observed that, compared to the high drain-field stressing, the high gate-field stressing produces large variation in the threshold voltage and subthreshold-swing. Thus, it can be concluded that devices operating in a saturation regime (high drain-field stressing) is less affected by bias-stress effects compared to an OTFT operated in a linear or a zero-V_{GS} regime (high gate-field stressing).

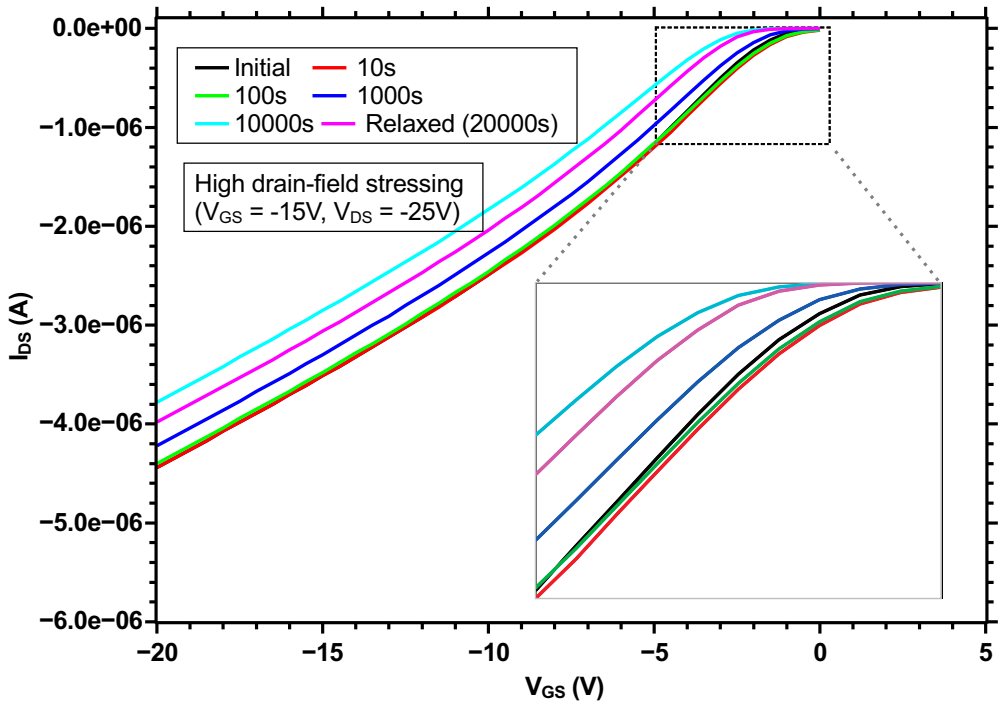


Figure 3.21: I_{DS}-V_{GS} (transfer) characteristics of an OTFT before and after application of bias stress during high drain-field stressing (V_{GS} = -15 V and V_{DS} = -25 V) at varying stress durations. The inset shows the magnified section of the curve lying between V_{GS} of 0 and -5 V.

3.4.3 Modelling Bias-Stress Instability

Despite the lack of a clear understanding of the physical mechanism responsible for the bias stress effects in OTFTs, experimental data can generally be well fitted with a stretched exponential function [Zsc+09; Kaw+06]:

$$\Delta V_T = \alpha \left[V_{T,final} - V_{T,initial} \right] [1 - exp\,(-(t/\tau)\,\beta)] \tag{3.7}$$

where $V_{T,initial}$ is the threshold voltage of an OTFT in the virgin state, $V_{T,final}$ is the final saturation value of the threshold voltage, α is the scaling constant, τ is the time constant, and β is the stretching parameter with values between 0 and 1. The stretched exponential function results in a faster-than-exponential response for time T_{Stress} less than time constant τ and a slower-than-exponential response for time T_{Stress} greater than the time constant τ. The degree of stretching depends on the parameter β. This

means the time required to reach the saturation value of the stretched exponential function depends on the value of β.

For the trapping of a mobile charge carrier, there needs to be a free mobile charge carrier and a free trap site. Therefore, the overall bias-stress induced shift in the threshold voltage depends on: a) the rate of creation of free mobile charge carriers, b) total trap density (both existing and created) and c) the rate of de-trapping of charge carriers. The charge carrier density is dependent on the value of V_{GS}. Intuitively, the shift in V_T of an OTFT can be considered to be either trap limited or carrier limited. If the concentration of charge carriers is more than the available trap states, the device is considered to be trap limited and the total trap density determines the final saturation value of its threshold voltage shift. On the other hand, if the concentration of charge carriers that are available to fill the traps are less than the total available trap states, then the device is considered to be carrier limited. In this case, the final saturation value of the threshold voltage shift is determined by V_{GS} and the saturation value increases with the magnitude of V_{GS}. The drain bias voltage exerts its influence by de-trapping of the trapped charge carriers. In our case, we assume that the device is charge carrier limited. Therefore, in Equation 3.7, $V_{T,final}$ is V_{GS} with $V_{T,initial}$ as V_{T0}. A comparison of modelled and measured shift in threshold voltage for various gate bias stress conditions are shown in Figure 3.23.

The values of α, β and τ are summarized in Table 3.4. As can be noticed, the value of β is approximately equal to 0.8. It can be observed that the time constant τ decreases with the increase in V_{GS}. This is because, for a larger V_{GS} there is an increased concentration of free mobile charge carriers and therefore, the shift in V_T occurs relatively faster.

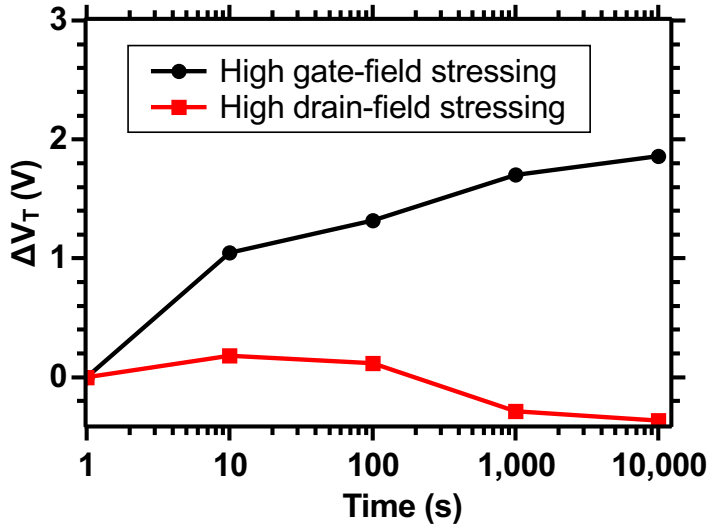
Table 3.4: Fitting parameters of the hysteresis model for different stress voltages. V_{DS} was held contant at -1 V.

Stress V_{GS} (V)	α	β	τ
-50	-0.07	0.88	1.9e+2
-40	-0.06	0.89	8.7e+2
-30	-0.04	0.88	1.2e+3

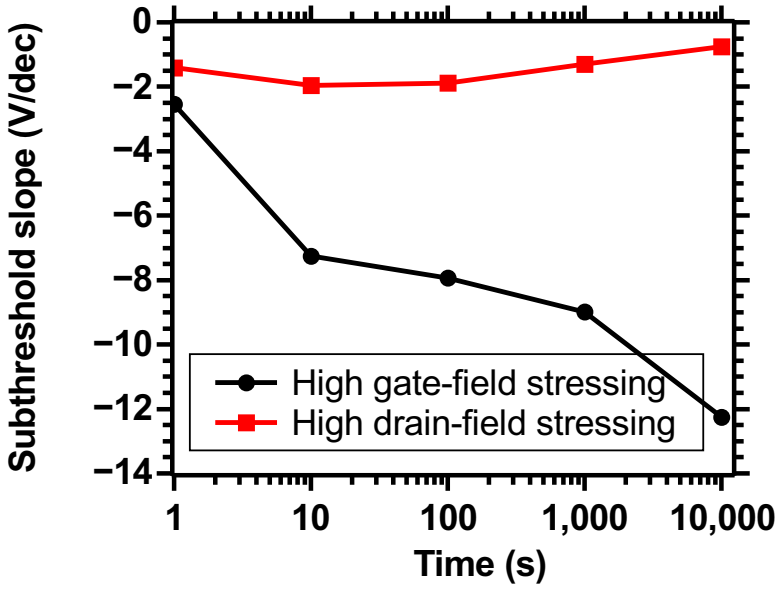
3.5 Conclusion

This chapter provides an overview of the various sources of variability in an OTFT. Substrates containing 100 identical OTFTs arranged in 10 rows and 10 columns were used to analyse the spatial distribution of the process variations including both the inter-substrate and intra-substrate variations. A statistical model taking into account both the global and local variations was developed. Thus, the process variations occurring in an OTFT were characterized and an appropriate statistical model was defined. Using this model, the impact of process variations on the electrical characteristics of basic organic circuits have also been analysed. In addition, the threshold voltage variation due to bias-stress effects in an OTFT has been investigated. It was observed that the threshold voltage variation is more pronounced for an OTFT operated in linear regime compared

to an OTFT operated in saturation regime. The dependence of the threshold voltage variation over V_{GS}, V_{DS} and time has been studied and a hysteresis model has been developed.



(a)



(b)

Figure 3.22: Comparison of the shift in threshold voltage and (b) shift in subthreshold-swing of the OTFT for high gate-field (V_{GS} = -30 V and V_{DS} = -1 V) and high drain-field stressing (V_{GS} = -15 V and V_{DS} = -25 V).

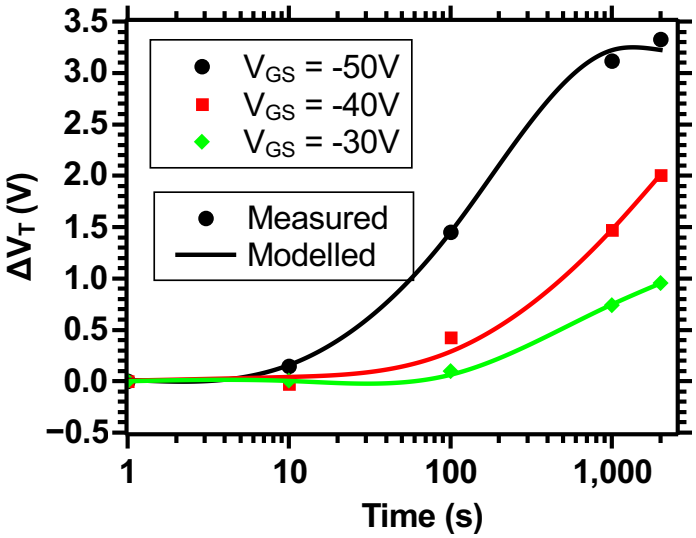


Figure 3.23: Calculated threshold voltage shift for V_{GS} = -50, -40 and -30 V and V_{DS} = -1 V.

4 Standard Cell Library of Organic Digital Circuits

Contents

This chapter describes a library of elementary organic circuits designed as standard cells. The focus is on digital logic gates and circuits. Therefore, we first introduce the basic digital gates, based on unipolar (PMOS) technology. We next discuss few basic digital circuits namely multiplexer and latches that use the previously designed digital gates. These standard cells will be used to design more complex circuitry, for e.g. the code generator circuit for a smart label system that will be described in detail in Chapter 6.

4.1 Design Considerations for Organic Circuits

- OFF Current: OTFTs are normally-on transistors, which means that the transistor cannot be switched off completely. This leads to a finite static current that always flows through any organic digital circuit increasing its power consumption.
- Reduced Voltage Swing: Due to the finite off resistance of the OTFT, there is always a voltage drop across the transistors which leads to a reduction in the output signal levels. This means that rail-to-rail output voltages are not possible with OTFTs.
- Operating Frequency: Due to the relatively large gate and parasitic capacitances, and large channel length, OTFTs have a low intrinsic cut-off frequency. In addition,

the large gate and parasitic capacitances reduce the operating frequency of organic circuits.

- Low Gain: The fact that just a single transistor type (p-type only) is used leads to a situation where the AC load impedance of a given circuit is reduced. Together with the fact that OTFTs have a low small-signal transconductance, the gain of organic circuits in general is low.
- Area: The fact that OTFTs have a low mobility leads to a decrease in the drain-source current and its small-signal transconductance. Therefore, to achieve a reasonable transconductance and drain-source current, the transistor dimensions must be significantly increased leading to large area circuits.
- Power Consumption: Due to the nature of the dielectric used, most often, a large voltage is required across the gate terminal to facilitate charge induction in the channel region. This usage of a large supply voltage leads to increased power consumption.

4.2 Standard Cell Configuration

The standard cell library of organic digital gates include Inverter, NAND, NOR, XOR, MUX and DFF. The basic digital gates namely inverter, NAND and NOR gates use either a diode or a zero-V_{GS} load topology. The standard cell library has two metal layers: a) one for the power rails (V_{DD} and GND) and b) the other for wiring connections. A type of 'Through via' is used to take the wiring across a cell cross section. The V_{DD} and GND rails are provided at the top and bottom of each standard cell respectively. The input and output ports for each standard cell are provided both at the top and bottom of the corresponding cell. The control signal port (for e.g. SEL in MUX) is provided either at the top or at the bottom of a standard cell. This choice of layout, for the standard cells, enables placing of cells side by side with efficient routing of V_{DD}, GND and wiring lines. All the cells have a fixed height of approx. 2000 μm but with varying widths. The minimum dimension for metal lines, inter-metal spacing and metal to cell spacing is 10 μm.

4.3 Mono-type Static Inverter

Although few organic circuits have been demonstrated using complementary logic [Bod+10; Xio+10b; Abd+12], the majority of the circuits reported in the literature use PMOS logic for various compelling reasons. A n-type OTFT is found to have inferior mobility and reliability compared to a p-type OTFT [Nau+11; TJK11; Ham+12]. Mono-type logic circuits are not completely new to the designer community. NMOS logic had been widely used for designing digital circuits using Si technology in 1980s before the advent of the modern CMOS logic [Fra+81; Bur+85; Erd85]. Several mono-type design styles have been proposed for designing organic digital circuits. Among them the most commonly used design styles are based on diode-load and zero-V_{GS} load topologies.

A static inverter is the simplest logic gate that consists of a driver transistor and an active load structure. They can be implemented in different ways depending on the type of the load topology used. The commonly used inverter types using mono-type PMOS transistors are shown in Figure 4.1. In Figure 4.1(a), a diode load inverter is shown where the load transistor has its gate terminal shorted to its drain terminal. Figure 4.1(b) shows a zero-V_{GS} load inverter where the load transistor has its gate terminal shorted to its source/output terminal. The other type of inverter shown in Figure 4.1(c) has a load transistor with a fixed bias voltage applied to its gate terminal. The working of these inverters will be discussed in detail in the next sections.

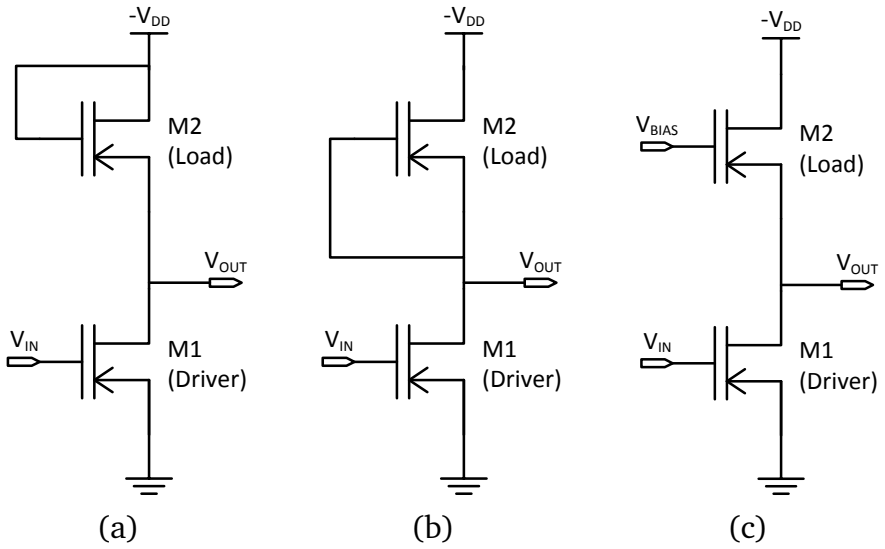


Figure 4.1: Schematic of commonly used (a) diode load, (b) zero-V_{GS} and (c) biased load inverter topologies using only PMOS transistors.

4.3.1 Diode Inverter

As shown in Figure 4.1(a), a diode inverter uses a diode-connected transistor as an active load. A diode-connected transistor has its gate terminal connected to its drain terminal. Thus its V_{GS} and V_{DS} are equal and its transfer and output characteristics exhibit a diode like behaviour as shown in Figure 4.2.

This implies that M_2 is always switched on and provides a strong pull-down force that pulls the output node to low (i.e. $-VDD$). When V_{IN} is low both M_1 and M_2 are conducting. For M_1 to pull-up the output node to high (i.e. GND), M_1 must have a larger width compared to M_2. In this work, the channel width (W) of the driver and the load transistor have been chosen to be 7000 and 800 μm respectively. However, this increases the gate capacitance of the input stage. Despite the large gate capacitance of the input transistor (M_1), the diode load inverter has a faster switching speed. This is mainly attributed to the strong pull-down force of the diode-connected load transistor (M_2). The key advantages of a diode load inverter are: 1) faster switching speed; and 2) robust to variations in the threshold voltage (V_T). On the other hand, its key disadvantages are: 1) poor noise margin due to its asymmetric transfer characteristics;

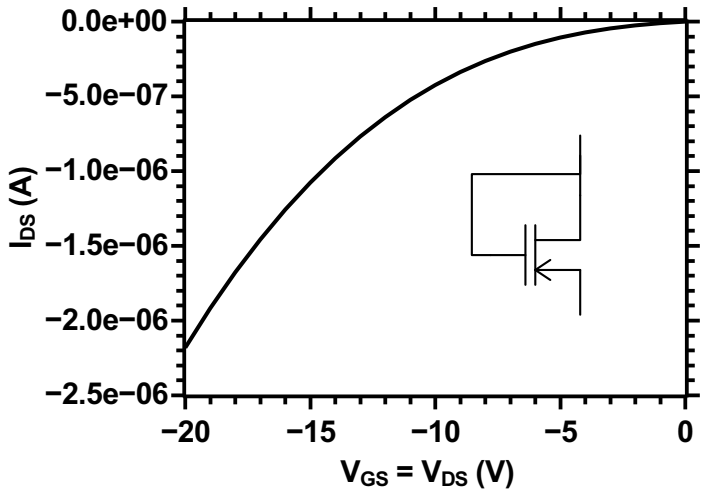


Figure 4.2: Transfer characteristics of a diode-connected transistor

2) greater power consumption as a result of the large pull-down current; 3) low output voltage swing; and 4) low gain.

4.3.1.1 DC Transfer Characteristics

Figure 4.3 shows the DC transfer characteristics of the diode load inverter. The transfer characteristics do not show two -1 slope points that is typical of a CMOS inverter. Nevertheless, the diode load topology can be used to design operating logic gates. The diode-connected load is a bad current source considering the fact that its drain-source current is dependent on its output voltage. This leads to a decrease in the output resistance which in turn reduces the gain of a diode load inverter. The low gain can be observed in Figure 4.3. This can also be explained using small-signal analysis. By performing a small-signal analysis, the equivalent output load resistance (R_L) and the voltage gain (A_V) can be determined using 4.1 and 4.3 respectively.

$$R_L = 1/g_{m2} \parallel r_{ds2} \tag{4.1}$$
$$\approx 1/g_{m2} \tag{4.2}$$
$$A_V = -g_{m1} \cdot (R_L \parallel r_{ds1}) \tag{4.3}$$
$$\approx -g_{m1}/g_{m2} \tag{4.4}$$

where g_{m1} and g_{m2} represent the small-signal transconductances of M_1 and M_2 respectively, r_{ds1} and r_{ds2} are the small-signal output resistances of M_1 and M_2 respectively. From the above small-signal analysis, the gain of a diode load inverter can be approximated by $-g_{m1}/g_{m2}$ which is nothing but ratio of two transconductances. As a consequence, the diode load inverter has a low gain.

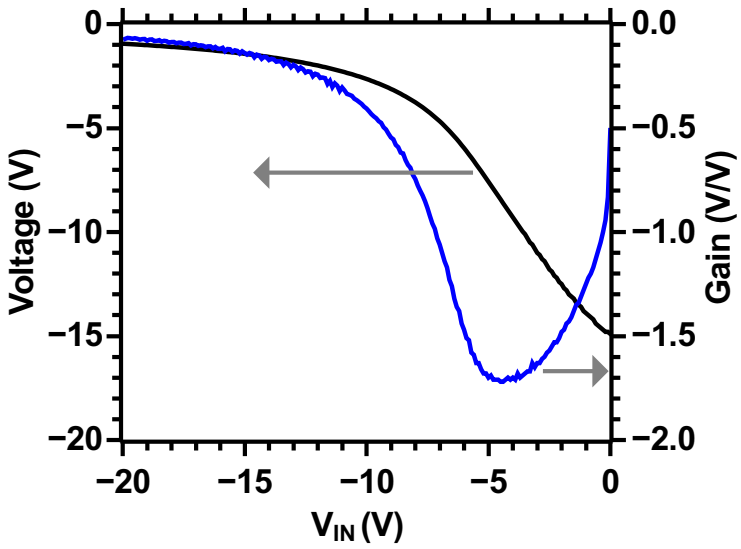


Figure 4.3: Measured DC characteristics of a diode load inverter.

4.3.1.2 Output Signal Levels

The output signal level of an inverter depends on the ratio of dimension of the driver transistor to that if the load transistor. Figure 4.4 shows the output level of a diode load inverter. Intersection points A and B represent V_{OL} and V_{OH} respectively. The values of V_{OL} and V_{OH} can be calculated analytically by equating the drain-source current flowing through the driver (M_1) transistor with the drain-source current flowing through the load (M_2) transistor. Since M_2 is diode-connected, V_{GS} is equal to V_{DS}. It must be noted that the OTFTs are usually depletion type devices i.e. normally on devices. This means that a PMOS transistor has a positive V_T. Therefore, transistor M_2 is always operating in a linear regime.

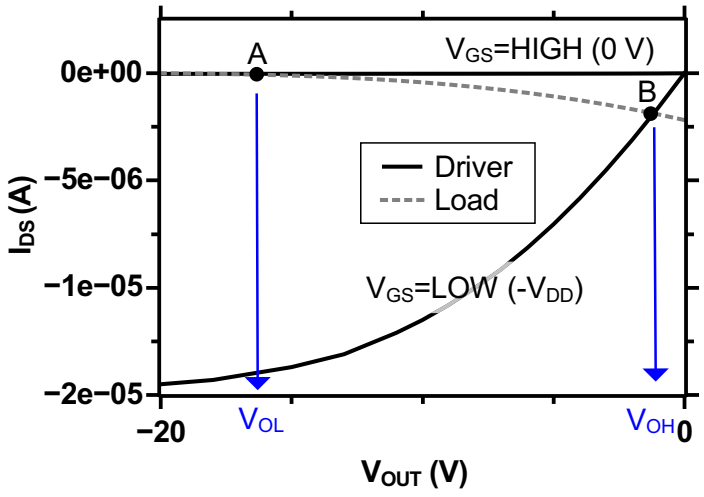


Figure 4.4: Output voltage levels of the diode load inverter.

Output Low

When the input voltage is set at high (0 V), M_1 is expected to be turned off and the output goes low (- V_{DD}). However, since the OTFTs are depletion type devices, the transistor is conducting with $V_{GS,eff} = -V_T$. In this case, M_1 is operating in saturation regime. The drain-source current (I_{DS1}) flowing through M_1 is given by:

$$\begin{aligned} I_{DS1} &= \frac{\kappa W_1}{2L_1}\left[(-V_T)^2\right] \qquad ; \text{where } \kappa = \mu_{FE} C_i \\ &= \frac{\kappa W_1}{2L_1}\left[{V_T}^2\right] \end{aligned} \tag{4.5}$$

Similarly the drain-source current flowing through M_2 operating in linear regime is given by:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[(V_{GS2} - V_T)\, V_{DS2} - \frac{V_{DS}^2}{2}\right] \tag{4.6}$$

For a diode-connected transistor, $V_{GS2} = V_{DS2}$. Substituting this in Equation 4.6 yields:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[\frac{V_{GS2}^2}{2} - V_{GS2} V_T\right] \tag{4.7}$$

Substituting $V_{G2} = V_{D2} = -V_{DD}$ and $V_{S2} = V_{OUT,L}$ in Equation 4.7

$$\begin{aligned} I_{DS2} &= \frac{\kappa W_2}{L_2}\left[\frac{\left(-V_{DD} - V_{OUT,L}\right)^2}{2} - \left(-V_{DD} - V_{OUT,L}\right) V_T\right] \\ &= \frac{\kappa W_2}{L_2}\left[\frac{V_{DD}^2}{2} + \frac{V_{OUT,L}^2}{2} + V_{DD} V_{OUT,L} + V_{DD} V_T + V_{OUT,L} V_T\right] \end{aligned} \tag{4.8}$$

Since the drain-source current through M_1 is equal to the drain-source current flowing through M_2, Equation 4.8 yields:

$$\begin{aligned} \frac{\kappa W_1}{2L_1}\left[{V_T}^2\right] &= \frac{\kappa W_2}{L_2}\left[\frac{V_{DD}^2}{2} + \frac{V_{OUT,L}^2}{2} + V_{DD} V_{OUT,L} + V_{DD} V_T + V_{OUT,L} V_T\right] \\ \frac{D_{12}}{2}\left[{V_T}^2\right] &= \frac{\kappa W_2}{L_2}\left[\frac{V_{DD}^2}{2} + \frac{V_{OUT,L}^2}{2} + V_{DD} V_{OUT,L} + V_{DD} V_T + V_{OUT,L} V_T\right] \end{aligned}$$

where $D_{12} = \frac{W_1 L_2}{W_2 L_1}$. Rearranging the terms and moving RHS to LHS:

$$V_{OUT,L}^2\left[\frac{1}{2}\right] + V_{OUT,L}\left[V_{DD} + V_T\right] + \frac{V_{DD}^2}{2} + V_{DD} V_T - \frac{D_{12}}{2}\left({V_T}^2\right) = 0 \tag{4.9}$$

The above equation (4.9) is of the form $Ax^2 + Bx + C = 0$ with $A = \frac{1}{2}$, $B = V_{DD} + V_T$ and $C = \frac{V_{DD}^2}{2} + V_{DD}V_T - \frac{D_{12}}{2}\left(V_T{}^2\right)$. Solving the above quadratic equation and finding its suitable root yields:

$$V_{OUT,L} = -(V_{DD} + V_T) + \left(\sqrt{1 + D_{12}}\right)V_T \approx V_{OL} \tag{4.10}$$

For the case when -V_{DD} is -20 V, V_T is 2 V and D_{12} is 9, V_{OL} is approximately equal to -15.68 V. This value closely follows the value observed from Figure 4.3. This value is significantly lower than that of a zero-V_{GS} load inverter as will be seen in coming sections.

Output High

When the input voltage is set to low (-V_{DD}), M_1 is turned on and the output goes high (0 V). In this case, M_1 is operating in linear regime. The drain-source current (I_{DS1}) flowing through M_1 is given by:

$$I_{DS1} = \frac{\kappa W_1}{L_1}\left[(-V_{DD} - V_T)V_{OUT,H} - \frac{V_{OUT,H}^2}{2}\right] \quad ; \text{where } \kappa = \mu_{FE}C_i \tag{4.11}$$

Similarly the drain-source current flowing through M_2 operating in linear regime is given by:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[(V_{GS2} - V_T)V_{DS2} - \frac{V_{DS}^2}{2}\right] \tag{4.12}$$

For a diode-connected transistor, $V_{GS2} = V_{DS2}$. Substituting this in Equation 4.12 yields:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[\frac{V_{GS2}^2}{2} - V_{GS2}V_T\right] \tag{4.13}$$

Substituting $V_{G2} = V_{D2} = -V_{DD}$ and $V_{S2} = V_{OUT,H}$ in Equation 4.13

$$\begin{aligned} I_{DS2} &= \frac{\kappa W_2}{L_2}\left[\frac{\left(-V_{DD} - V_{OUT,H}\right)^2}{2} - \left(-V_{DD} - V_{OUT,H}\right)V_T\right] \\ &= \frac{\kappa W_2}{L_2}\left[\frac{V_{DD}^2}{2} + \frac{V_{OUT,H}^2}{2} + V_{DD}V_{OUT,H} + V_{DD}V_T + V_{OUT,H}V_T\right] \end{aligned} \tag{4.14}$$

The drain-source current through M_1 is equal to the drain-source current flowing through M_2. Therefore, equating 4.11 and 4.14 yields:

$$V_{OUT,H}^2\left[\frac{1 + D_{12}}{2}\right] + V_{OUT,H}\left[(1 + D_{12})(V_{DD} + V_T)\right] + \frac{V_{DD}^2}{2} + V_{DD}V_T = 0 \tag{4.15}$$

where $D_{12} = \frac{W_1 L_2}{W_2 L_1}$. The above equation (4.15) is of the form $Ax^2 + Bx + C = 0$ with $A = \frac{1+D_{12}}{2}$, $B = (1 + D_{12})(V_{DD} + V_T)$ and $C = (V_{DD} + V_T) + \frac{V_{DD}^2}{2} + V_{DD}V_T$. Solving the above quadratic equation and finding its suitable root yields:

$$V_{OUT,H} = -(V_{DD} + V_T) + \sqrt{(V_{DD} + V_T)^2 - \frac{2}{1 + D_{12}}\left[\frac{V_{DD}^2}{2} + V_{DD}V_T\right]} \approx V_{OH} \qquad (4.16)$$

For the case when -V_{DD} is -20 V, V_T is 2 V and D_{12} is 9, V_{OH} is approximately equal to -1.12 V. This value closely follows the value observed from Figure 4.3.

4.3.2 Zero-V_{GS} Inverter

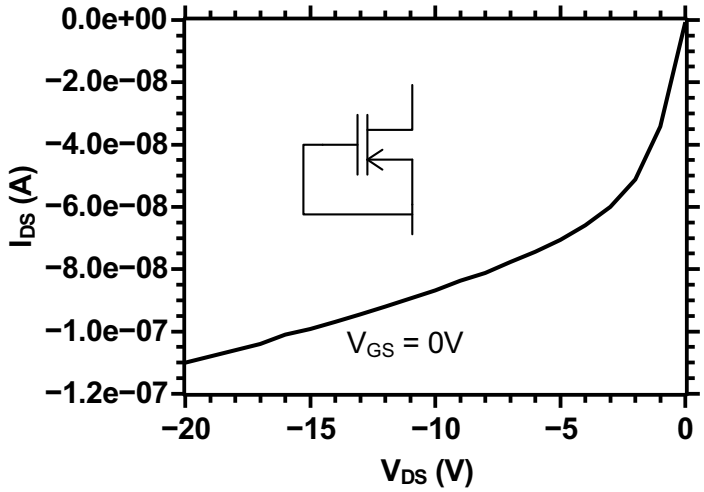


Figure 4.5: Output characteristics of a zero-V_{GS} load transistor

An inverter design using a zero-V_{GS} load, also known as cut-off load, is shown in Figure. 4.1(b). Unlike the diode load inverter, the gate terminal of the load transistor in a zero-V_{GS} load inverter is connected to its source terminal, which is also the output terminal of the inverter. A meaningful operation of the inverter is obtained only when the load uses a depletion-mode transistor (i.e. $V_T \geq 0$ V for a p-type OTFT). In this case the effective gate-source voltage is nothing but the V_T of the load transistor. Figure 4.5 shows the output characteristic of the load transistor with a V_{GS} of 0 V. As a result, zero-V_{GS} load inverters are greatly influenced by the variations in V_T. On the other hand, zero-V_{GS} load acts as a constant current source that results in a large small-signal output resistance. Consequently, the gain of the inverter that uses a zero-V_{GS} load is significantly larger. The load transistor, acting as a current source, operates in the sub-threshold regime producing a very low current. Therefore, to improve the noise margin and the output swing of a zero-V_{GS} load inverter, the width of the load transistor (M_2) must be chosen larger than the width of the driver transistor (M_1). For our design of the zero-V_{GS} load inverter, the driver and the load transistor have been chosen to have a channel width (W) of 800 and 7000 μm respectively. This type of inverter, although consumes relatively low power, operates at a slower speed. The key advantages of a

cut-off load inverter are: 1) large output swing; 2) good noise margin; 3) lower power consumption; and 3) relatively large gain. On the other hand, its key disadvantages are: 1) slower switching speed; and 2) greater sensitivity to variations in the threshold voltage (V_T).

4.3.2.1 DC Transfer Characteristics

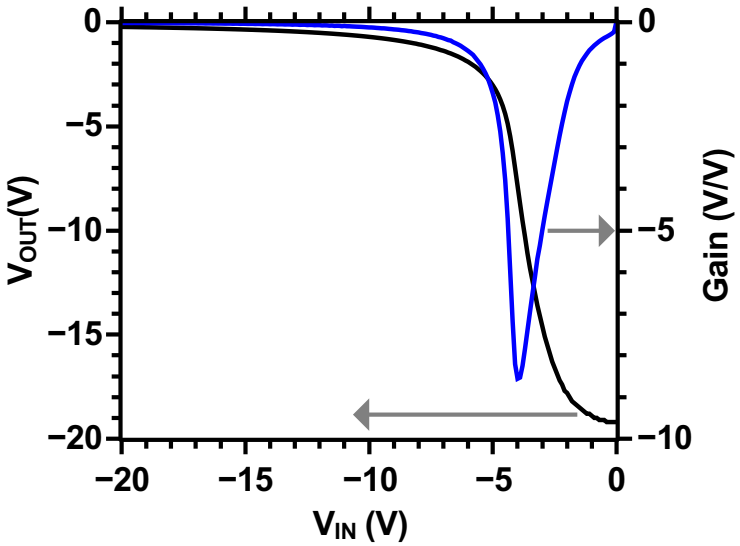


Figure 4.6: Measured DC (Gain and voltage transfer) characteristics of the zero-V_{GS} load inverter.

Figure 4.6 shows the measured DC transfer characteristics of the zero-V_{GS} load inverter. Unlike the diode load inverter, the transfer characteristics of the zero-V_{GS} load inverter shows two distinct -1 slope points. Since the zero-V_{GS} load acts as a constant current source with a relatively large small-signal output resistance (r_{DS}), gain of the inverter is higher compared to the diode load inverter. By performing small-signal analysis, the equivalent output load resistance (R_L) and the voltage gain (A_V) can be determined using 4.17 and 4.18 respectively.

$$R_L = r_{ds2} \tag{4.17}$$

$$\begin{aligned} A_V &= -g_{m1} \cdot (R_L \parallel r_{ds1}) \\ &\approx \frac{-g_{m1} r_{ds}}{2} \qquad \text{assuming } r_{ds1} = r_{ds2} = r_{ds} \end{aligned} \tag{4.18}$$

where g_{m1} represents the small-signal transconductance of M_1, r_{ds1} and r_{ds2} are the small-signal output resistances of M_1 and M_2 respectively. The above equation (4.18) explains the relatively high gain offered by the zero-V_{GS} load inverter in comparison to the diode load inverter.

4.3.2.2 Output Signal Levels

Figure 4.7 shows the output level of a zero-V_{GS} load inverter. Intersection points A and B represent V_{OL} and V_{OH} respectively. The values of V_{OL} and V_{OH} can be calculated analytically by equating the current flowing through the driver (M_1) and load (M_2) transistor.

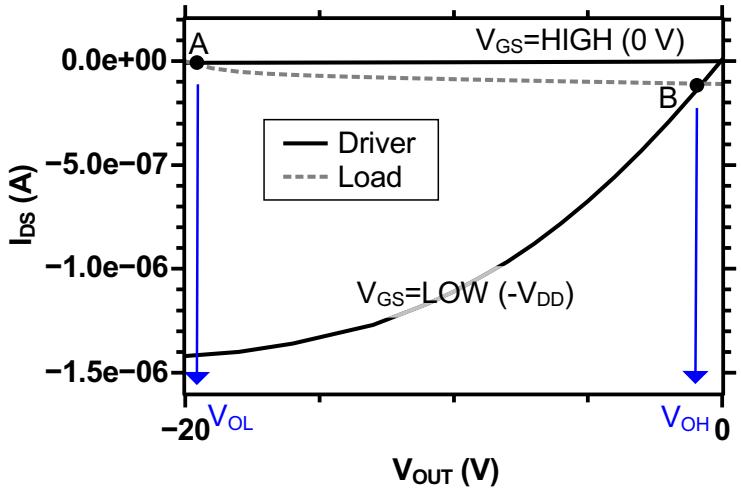


Figure 4.7: Output voltage levels of the zero-V_{GS} load inverter

Output Low

When the input voltage is set to high (0 V), the output goes low (- V_{DD}). Here, M_1 is operating in saturation regime and M_2 is operating in linear regime. M_1 operates with $V_{GS,eff} = -V_T$. The drain-source current (I_{DS1}) flowing through M_1 operating in saturation regime is given by:

$$\begin{aligned} I_{DS1} &= \frac{\kappa W_1}{2L_1}\left[(-V_T)^2\right] \qquad ; \text{where } \kappa = \mu_{FE} C_i \\ &= \frac{\kappa W_1}{2L_1}\left[{V_T}^2\right] \end{aligned} \tag{4.19}$$

Similarly the drain-source current flowing through M_2 operating in linear regime is given by:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[(V_{GS2} - V_T)\,V_{DS2} - \frac{V_{DS}^2}{2}\right] \tag{4.20}$$

For a zero-V_{GS} load transistor, $V_{G2} = V_{S2} = V_{OUT,L}$ and $V_{GS2} = 0$ V. Substituting this in Equation 4.20 yields:

$$I_{DS2} = \frac{\kappa W_2}{L_2}\left[(-V_T)\left(-V_{DD} - V_{OUT,L}\right) - \frac{\left(-V_{DD} - V_{OUT,L}\right)^2}{2}\right] \tag{4.21}$$

The drain-source current through M_1 is equal to the drain-source current flowing through M_2. Equating 4.19 and 4.21 and moving RHS to LHS yields:

$$V_{OUT,L}^2\left[\frac{1}{2}\right]+V_{OUT,L}\left[V_{DD}-V_T\right]+\frac{V_{DD}^2}{2}-V_{DD}V_T+\frac{D_{12}}{2}\left({V_T}^2\right)=0 \tag{4.22}$$

where $D_{12}=\frac{W_1L_2}{W_2L_1}$. The above equation (4.22) is of the form $Ax^2+Bx+C=0$ with $A=\frac{1}{2}$, $B=V_{DD}-V_T$ and $C=\frac{V_{DD}^2}{2}-V_{DD}V_T+\frac{D_{12}}{2}\left({V_T}^2\right)$. Solving the above quadratic equation and finding its suitable root yields:

$$V_{OUT,L}=-(V_{DD}+V_T)-\left(\sqrt{1+D_{12}}\right)V_T\approx V_{OL} \tag{4.23}$$

For the case when -V_{DD} is -20 V, V_T is 2 V and D_{12} is 1/9, V_{OL} is approximately equal to -19.8 V. This value closely follows the value observed in Figure 4.6.

Output High

When the input voltage is set to low (-V_{DD}), M_1 is turned on and the output goes high (0 V). In this case, M_1 and M_2 are operating in linear and saturation regimes respectively. The drain-source current (I_{DS1}) flowing through M_1 is given by:

$$I_{DS1}=\frac{\kappa W_1}{L_1}\left[(-V_{DD}-V_T)V_{OUT,H}-\frac{V_{OUT,H}^2}{2}\right] \quad ; \text{where } \kappa=\mu_{FE}C_i \tag{4.24}$$

Similarly the drain-source current flowing through M_2 operating in saturation regime is given by:

$$I_{DS2}=\frac{\kappa W_2}{2L_2}\left[{V_T}^2\right] \tag{4.25}$$

The current through M_1 is equal to the current flowing through M_2. Therefore, equating 4.24 and 4.25 and moving RHS to LHS yields:

$$V_{OUT,H}^2\left[\frac{D_{12}}{2}\right]+V_{OUT,H}\left[D_{12}(V_{DD}+V_T)\right]+\frac{{V_T}^2}{2}=0 \tag{4.26}$$

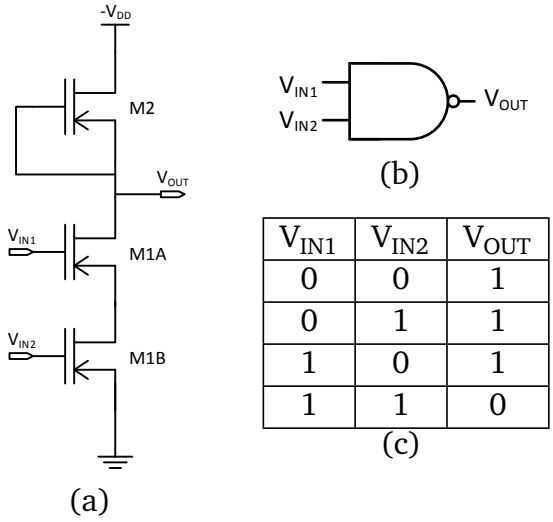
where $D_{12}=\frac{W_1L_2}{W_2L_1}$. The above equation (4.26) is of the form $Ax^2+Bx+C=0$ with $A=\frac{D_{12}}{2}$, $B=D_{12}(V_{DD}+V_T)$ and $C=\frac{{V_T}^2}{2}$. Solving the quadratic equation and finding its suitable roots yields:

$$V_{OUT,H}=-(V_{DD}+V_T)+\sqrt{(V_{DD}+V_T)^2-\frac{{V_T}^2}{D_{12}}}\approx V_{OH} \tag{4.27}$$

For the case when -V_{DD} is -20 V, V_T is 2 V and D_{12} is 1/9, V_{OH} is approximately equal to -0.8 V. This values closely follows the values shown in Figure 4.6.

4.4 NAND

NAND gate was designed using a zero-V_{GS} load structure. The schematic, symbol and the truth table of the NAND gate is shown in Figure 4.8. The dimensions of the transistors are given in Table 4.1. The input stage consists of two stacked transistors M_{1A} and M_{1B}. Therefore, to counter the increase in on resistance of the stacked transistors, the width of the input transistors are set at twice the width of the input stage of a NOR gate. The NAND gate was measured in air at ambient temperature/pressure condition. The transient characteristics of the NAND gate were measured at a supply voltage of -10 V. For this case, a HIGH represents 0 V and a LOW represents -10 V. The measured transient characteristics are shown in Figure 4.9. It demonstrates the correct functionality of the NAND gate. The output voltage exhibits a voltage swing of 6.6 V with a rise and fall time of 360 and 500 μs respectively (See Table 4.2).



V_{IN1}	V_{IN2}	V_{OUT}
0	0	1
0	1	1
1	0	1
1	1	0

(c)

Figure 4.8: Schematic, symbol and truth table of a static PMOS NAND gate.

Table 4.1: Transistor sizing of the static PMOS NAND gate.

Transistor	Width (μm)	Length (μm)
M1A, M1B	1600	5
M2	7000	5

Table 4.2: Performance metrics of the static PMOS NAND gate.

Parameter	Value
Voltage swing	6.6 V
Rise time	360 μs
Fall time	500 μs

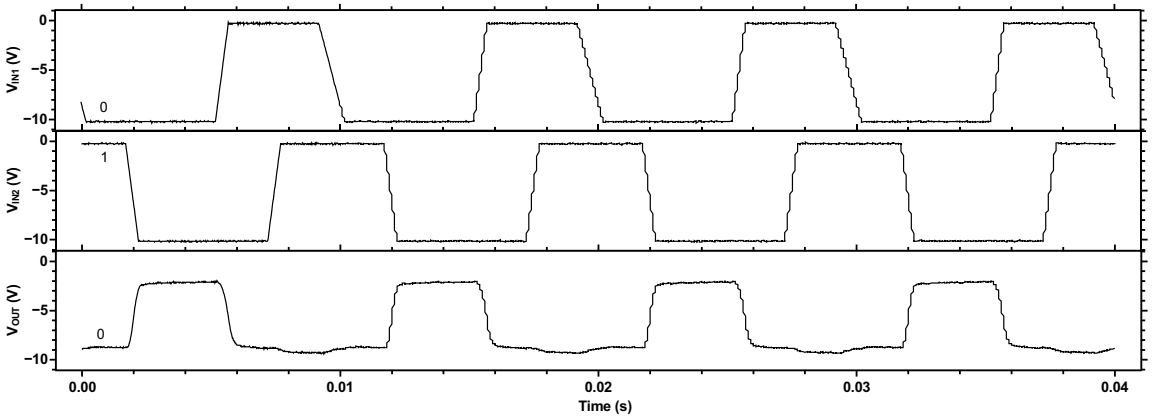
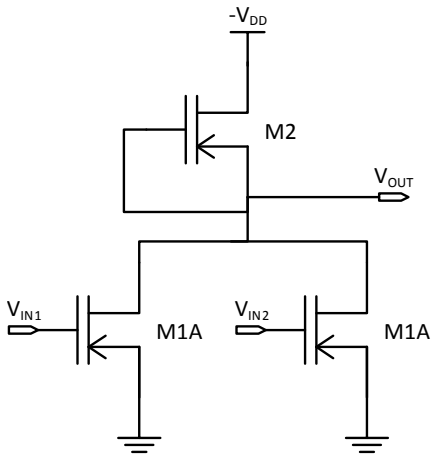


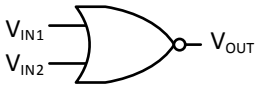
Figure 4.9: Measured transient characteristics of the NAND gate.

4.5 NOR

The design of NOR gate employs a zero-V_{GS} load structure. The schematic, symbol and the truth table of the NOR gate is shown in Figure 4.10. The transistor sizings are reported in Table 4.3. The transient characteristics of the NOR gate were measured at a supply voltage of -10 V. For this case, a HIGH represents 0 V and a LOW represents -10 V. The measured transient characteristics are shown in Figure 4.11 which demonstrates its correct functionality. The performance parameters are given in Table 4.4. The output voltage exhibits a voltage swing of 6.4 V with a rise and fall time of 450 and 510 μs respectively.



(a)



(b)

V_{IN1}	V_{IN2}	V_{OUT}
0	0	1
0	1	0
1	0	0
1	1	0

(c)

Figure 4.10: Schematic, symbol and truth table of a static PMOS NOR gate.

Table 4.3: Transistor sizing of the static PMOS NOR gate.

Transistor	Width (μm)	Length (μm)
M1A, M1B	800	5
M2	7000	5

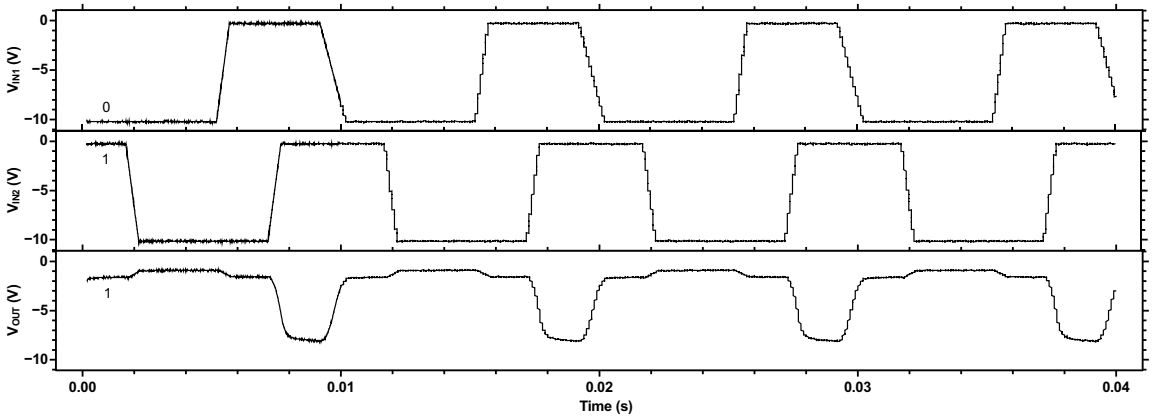


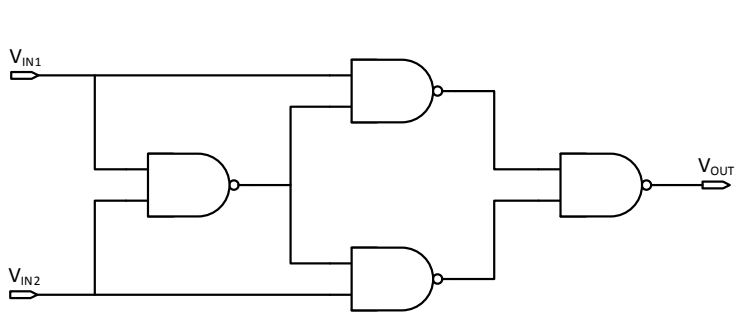
Figure 4.11: Measured transient characteristics of the NOR gate.

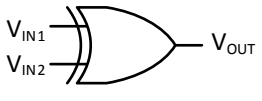
Table 4.4: Performance metrics of the static PMOS NOR gate.

Parameter	Value
Voltage swing	6.4 V
Rise time	450 μs
Fall time	510 μs

4.6 XOR

The XOR gate consists of four NAND gates. The schematic, symbol and the truth table of the XOR gate is shown in Figure 4.12. The measured transient characteristics of the XOR gate, measured at a supply voltage of -10 V, are shown in Figure 4.13 that demonstrates its correct functionality. The performance parameters are given in Table 4.5. The output voltage swing is reduced to 4.2 V owing to the fact that the input to the last NAND gate is applied after traversing through two NAND gates. The output voltage swing of the NAND gate observed from the measured results is approximately 6.6V. The rise and fall times of the output are observed to be 920 μs and 1.9 ms respectively. This represents a significant increase from the rise and fall times of the NAND and NOR gates. This is because, the input signal in a XOR gate passes through three consecutive NAND gates.





(b)

V_{IN1}	V_{IN2}	V_{OUT}
0	0	0
0	1	1
1	0	1
1	1	0

(c)

Figure 4.12: Schematic, symbol and truth table of a static PMOS XOR gate.

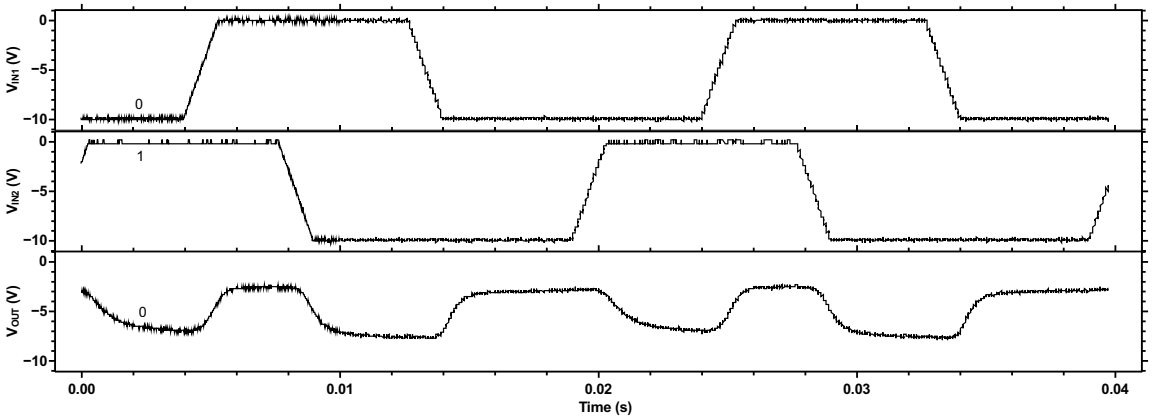


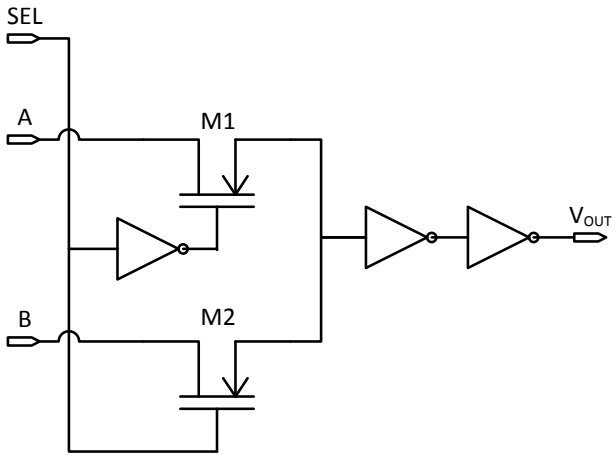
Figure 4.13: Measured transient characteristics of the XOR gate.

Table 4.5: Performance metrics of the static PMOS XOR gate.

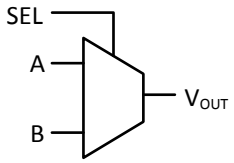
Parameter	Value
Voltage swing	4.2 V
Rise time	920 μs
Fall time	1.9 ms

4.7 MUX

The schematic, symbol and the truth table of a 2:1 multiplexer (MUX) is shown in Figure 4.14. The transistor dimensions are reported in Table 4.6. The transient characteristics measured at a supply voltage of -10 V is shown in Figure 4.15. The performance parameters of the multiplexer gate are given in Table 4.7. It has an output voltage swing of 5.9 V. The rise and fall times of the output were observed to be 470 μs and 1.1 ms respectively.



(a)



(b)

SEL	V_{OUT}
0	A
1	B

(c)

Figure 4.14: Schematic, symbol and truth table of a 2:1 MUX.

Table 4.6: Transistor sizing of 2:1 MUX.

Transistor	Width (μm)	Length (μm)
M1	800	5
M2	800	5

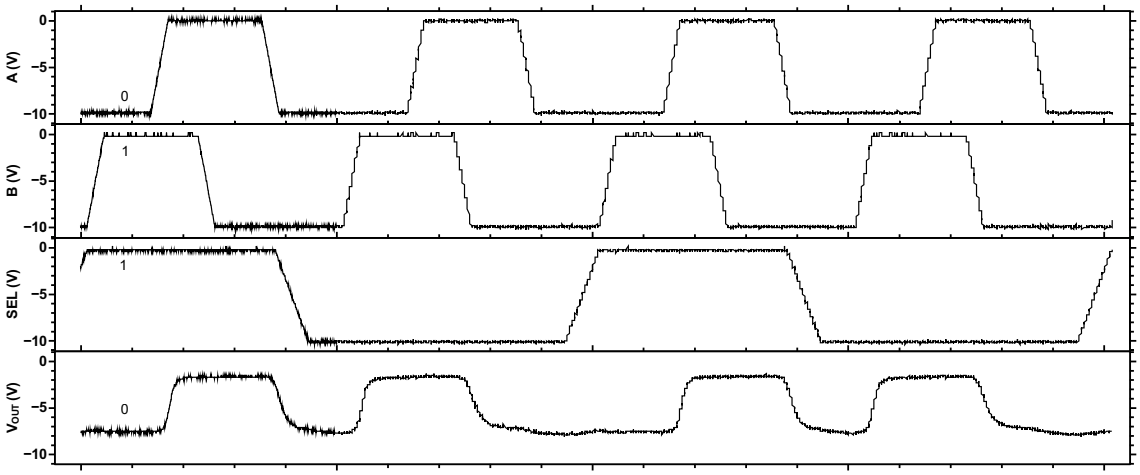


Figure 4.15: Measured transient characteristics of the 2:1 MUX.

Table 4.7: Performance metrics of the 2:1 MUX.

Parameter	Value
Voltage swing	5.9 V
Rise time	470 μs
Fall time	1.1 ms

4.8 D-Latch

D-latch is a basic constituent to realize a D-flip-flop. The circuit schematic of a D-latch is shown in Figure 4.16. The design uses a pass-transistor logic to reduce the transistor count. The transistor dimensions are reported in Table 4.8. The transient characteristics measured at a supply voltage of -10 V are shown in Figure 4.17 and its performance parameters are given in Table 4.9. It has an output voltage swing of 5.0 V. The rise and fall times of the output signal are observed to be 1.5 ms and 1.8 ms respectively.

Table 4.8: Transistor sizing of the D-latch cell.

Transistor	Width (μm)	Length (μm)
M1	800	5
M2	800	5

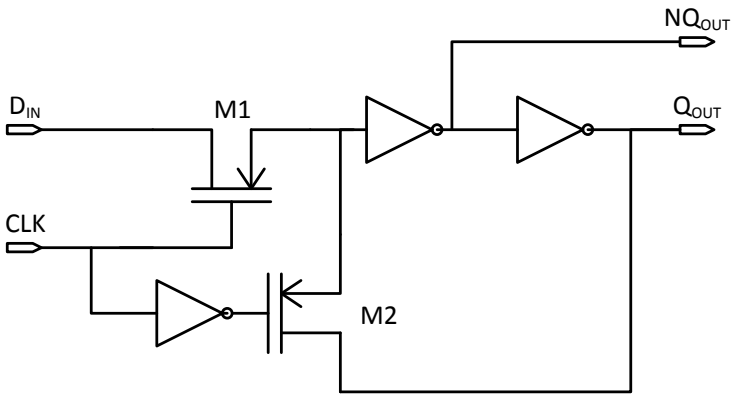


Figure 4.16: Schematic of a D-latch.

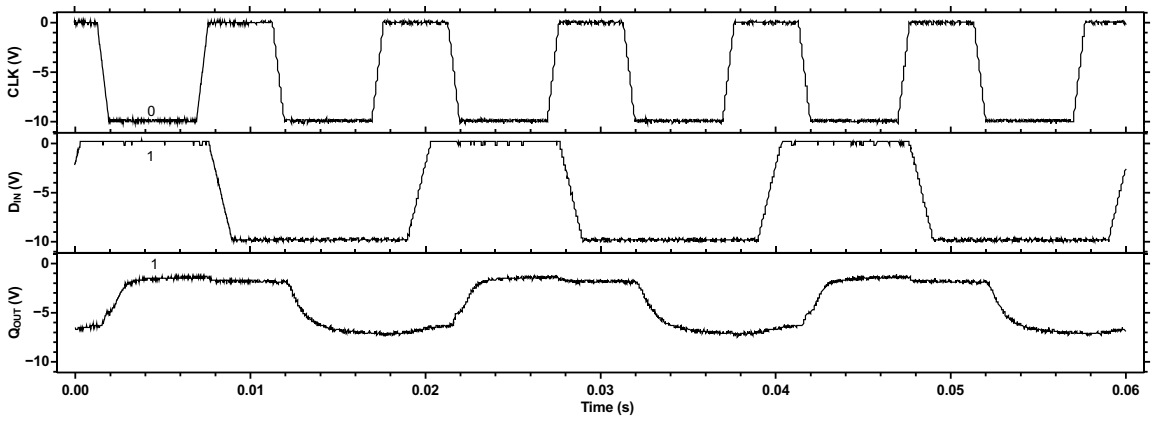


Figure 4.17: Measured transient characteristic of the D-Latch.

Table 4.9: Performance metrics of the D-Latch.

Parameter	Value
Voltage swing	5.0 V
Rise time	1.5 ms
Fall time	1.8 ms

4.9 Conclusion

A standard cell library of organic digital circuits was designed and measured. The library comprises basic inverters, NAND, NOR, XOR, 2:1 MUX and a D-Latch. The circuits were fabricated using organic PMOS technology. The measured transient results show that all the circuits are operating as expected. Owing to the large gate parasitic capacitances of OTFT, the circuits exhibit a large rise and fall time in the range of 300 μs to 1.5 ms. Due to the characteristics of the normally-on transistors and non-complementary PMOS only load, the output voltage swing is also significantly degraded. Though these circuits can not be used in applications that demand high performance, they can be used for low performance applications especially for low-cost smart label system. As will be discussed in Chapter 6, these standard cells were used to design the code generator block of a smart label system.

5 Design of Robust Organic Circuits

Contents

In this chapter, circuit techniques are presented to design digital and analog organic circuits using OTFTs that are tolerant to the threshold voltage (V_T) variation of an OTFT and as well as provides a better or a comparable performance compared to the state-of-the-art organic circuits. The design strategy consists of using enhanced load circuits for simple circuits and using digital based analog circuits for realising complex analog circuits like ADC. Section 5.1 provides a brief overview of key issues with the existing active load circuits using OTFTs. Among the state-of-the-art load circuits, zero-V_{GS} load circuit has a high gain but is less reliable whereas the diode load circuit is more reliable but has a low gain. Thus, a design solution that can combine the advantages of both topologies is very much necessary. This work proposes two techniques, one involving positive feedback (see Section 5.2) and the other using cascoded zero-V_{GS} transistors (see Section 5.3) for enhanced load structures. Inverter circuits using the proposed load topologies were fabricated and their performances were compared with that of the state-of-the-art inverter circuits in Section 5.4. The sensitivity of inverter circuits using various load topologies to the process and bias-stress variations are also investigated. Section 5.5 explains the design of organic differential amplifiers. Digital based ADC architectures namely VCO-based ADC and digital flash ADC are described in Section 5.8 and 5.9 respectively. A VCO-based ADC is a time-based ADC architecture that is highly digital with regard to its composition. In Section 5.8, the performance of an organic VCO employing different delay elements is analysed and their suitability for use in a VCO-based ADC is studied. An equation to calculate the theoretical limit of the resolution of a VCO-based ADC from its voltage vs. frequency characteristics is formulated. Using this equation various VCO architectures are analysed that can be used to

realise a VCO-based ADC. The impact of jitter and $1/f$ noise on the performance of the ADC is also investigated. Section 5.9 describes the design and measurement of the first all-digital flash A/D converter implemented using PMOS OTFT on a flexible substrate. For this design, a digital inverter based comparator is proposed and is used in the ADC circuit.

5.1 Existing Organic Mono-type Active Load Circuits

In circuit design, large AC load impedances are desirable to increase the AC gain of amplifier circuits. An active load is a circuit component made up of active devices, such as transistors, that are intended to provide a high small-signal impedance and at the same time do not drop a large DC voltage across it, as would occur if a large resistor were used instead. The most common prior-art active load circuits using OTFTs are diode-connected and zero-V_{GS} load circuits. Their design and characteristics are described in Section 4.3. These load circuits have some issues that needs to be addressed in order to improve the performance and reliability of organic circuits using them. The main challenge in organic circuit design arises from the fact that the OTFT suffers from large parameter and mismatch variation which were described in detail in Chapter 3. The changes in V_T due to the bias stress effect [Ryu+10; Mat+07] and process variations strongly undermine the reliability of the organic circuits. Therefore, sensitivity of organic circuits to V_T variation is of particular importance when designing reliable circuits and hence, a circuit designer has to take into account this sensitivity while designing organic circuits.

5.1.1 Issues with Diode Load Circuits

Looking at the diode load circuit shown in Figure 5.1, the effective gate-source overdrive voltage ($V_{GS,eff}$) of the load transistor is given by

$$\begin{aligned} V_{GS,eff} &= V_{GS} - V_T \\ V_{GS,eff} &= -V_{DD} - V_S - V_T \end{aligned} \tag{5.1}$$

where V_S is the voltage at the source terminal and V_T is the threshold voltage. The p-type OTFTs used in this work has a threshold voltage value in the range of 1 to 3 V. Since $|V_{DD}| >> |V_T|$, $V_{GS,eff}$ of the load transistor is less affected by any variation in its V_T. Therefore, the diode load inverter is less sensitive to any variation in the threshold voltage. But on the other hand, as described in Section 4.3.1, these circuits suffer from a low gain mainly due to the low AC impedance offered by the diode load transistor. Therefore, diode load circuits offer good reliability but offer a low gain that makes it unsuitable for amplifier applications that demands a decent gain.

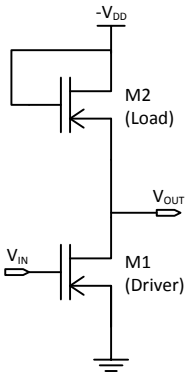


Figure 5.1: Schematic of an inverter using diode load

5.1.2 Issues with Zero-V_{GS} Load Circuits

In the case of a zero-V_{GS} Load Circuit, such as an inverter as shown in Figure 5.2, the gate-source voltage of the load transistor is zero. Therefore, the load transistor has an effective gate-source overdrive voltage ($V_{GS,eff}$) of $-V_T$ as given below.

$$\begin{aligned} V_{GS,eff} &= V_{GS} - V_T \\ V_{GS,eff} &= -V_T \end{aligned} \tag{5.2}$$

As given in Equation 5.2, $V_{GS,eff}$ is equal to V_T in magnitude. Hence, any variation in V_T causes a significant impact in the performance of the inverter. Therefore, circuits that uses a zero-V_{GS} load are more sensitive to the threshold voltage variations and thus they are relatively more unreliable compared to the circuits that uses a diode load. However, a zero-V_{GS} load offers a high AC output impedance (Refer Section 4.3.2). This leads to a relatively larger gain. Hence, zero-V_{GS} load circuits provide relatively better gain than the diode load circuits but are more susceptible to the threshold voltage variations.

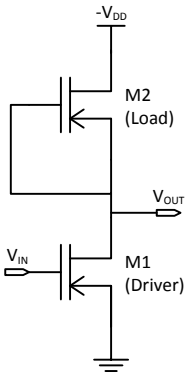


Figure 5.2: Schematic of an inverter using zero-V_{GS} load

5.1.3 Summary of Design Considerations

A summary of key advantages and disadvantages of the commonly used state-of-the-art load circuits is shown in Table 5.1. It can be clearly observed from Table 5.1 that the

existing load topologies need to be improved so that they can offer a decent gain and at the same time can be sufficiently reliable.

Table 5.1: Key davantages and disadvantages of prior-art load topologies.

Topology	Gain	Reliability
Diode	Low	High
Zero-V_{GS}	High	Low

5.2 Proposed Positive-feedback Load Circuit

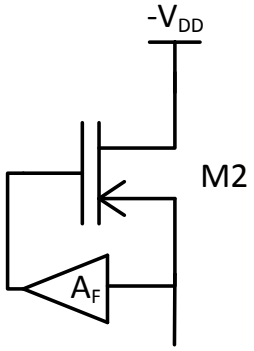


Figure 5.3: Schematic of a positive feedback load

To realize a load topology that has the combined advantages of both the zero-V_{GS} and diode load topologies, an output feedback mechanism is employed. The schematic of the proposed load topology is shown in Figure 5.3 where a part of the output is fed back to the gate terminal of the load transistor M_2. In the given schematic, A_F denotes the gain of the feedback amplifier whose output is used to bias the load transistor M_2. By performing small-signal analysis, the equivalent output load resistance (R_L) and voltage gain (A_V) can be determined using Equations 5.3 and 5.4 respectively.

$$R_L = [1/g_{m2}(1-A_F)] \,\|\, r_{ds2} \tag{5.3}$$

$$A_V = -g_{m1} \cdot (R_L \,\|\, r_{ds1}) \tag{5.4}$$

Here g_{m1} and g_{m2} represent the small-signal transconductances of M_1 and M_2 respectively, A_F is the gain of the feedback amplifier, r_{ds1} and r_{ds2} are the small-signal output resistances of M_1 and M_2 respectively. The schematic of an inverter using a feedback load is shown in Figure 5.4. In the given schematic, M_1 and M_2 form the inverter core, and M_3 and M_4 constitute a voltage follower circuit whose gain (A_F) is always less than unity. But for the purpose of analysis, different possible feedback conditions with A_F ranging from -1 to $+2$ is considered. The equivalent output load resistance R_L and the approximate voltage gain A_V of the inverter for various feedback conditions are shown in Table 5.2. It can be seen from Table 5.2 that the gain of an inverter using a negative feedback condition is half the gain of a diode load inverter. When the feedback gain becomes zero, the inverter circuit behaves like a diode load inverter offering a good reliability but with a low gain. For a unity gain positive feedback, the gain of the inverter

Table 5.2: Equivalent load resistance and voltage gain of a positive-feedback inverter for various A_F.

$A_F \rightarrow$	-1	0	+1	+2
R_L	$[1/2.g_{m2}]\|\|r_{ds2}$	$[1/g_{m2}]\|\|r_{ds2}$	r_{ds2}	$[1/-g_{m2}]\|\|r_{ds2}$
A_V	$-g_{m1}/2.g_{m2}$	$-g_{m1}/g_{m2}$	$-g_{m1}(r_{ds1}\|\|r_{ds2})$	g_{m1}/g_{m2}

is equal to that of a zero-V_{GS} load inverter. When A_F is increased beyond unity, the gain of the inverter starts decreasing and the gain becomes positive which means that the output is non-inverted. Hence, the unity gain feedback ($A_F = 1$) acts as an upper limit within which the feedback gain can be varied to improve the gain of the inverter. Therefore, A_F provides a control over the performance of the inverter through which one can trade-off gain for higher reliability and vice-versa. To avoid stability issues, A_F is always chosen to be less than unity. By having A_F around 0.8, one can achieve a decent gain for the inverter which is higher than that of a diode load inverter and also has a better reliability that a zero-V_{GS} load inverter.

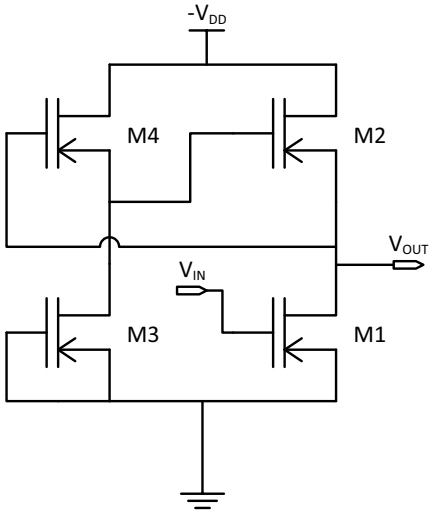


Figure 5.4: Schematic of an inverter using positive feedback load

5.3 Proposed Cascaded Zero-V_{GS} Load Circuit

It was described in Section 5.1.2 that although the zero-V_{GS} load offers high gain, it has low reliability owing to the operation of the zero-V_{GS} load transistor with $V_{GS,eff} = -V_T$. As a consequence, any change in V_T is completely translated to a variation in $V_{GS,eff}$. Therefore, zero-V_{GS} load inverters are relatively more unreliable. The reliability of the zero-V_{GS} load can be improved by employing a compensation mechanism that counteracts any variation in $V_{GS,eff}$ of the load transistor due to the changes in its V_T. Such a compensation mechanism can be achieved by connecting a resistor between the gate and the source terminal of the load transistor as shown in Figure 5.5(a).

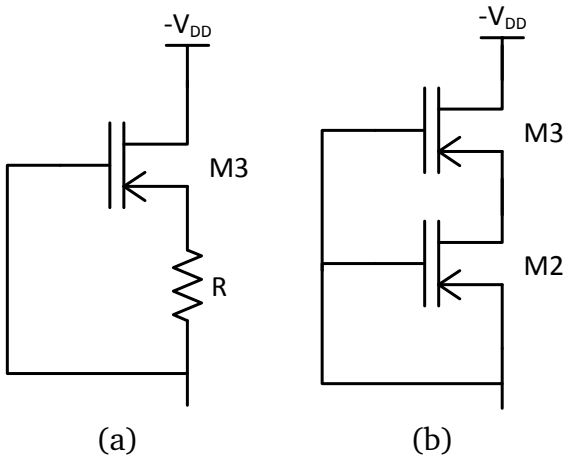


Figure 5.5: Schematics of a cascaded load structure

For the circuit shown in Figure 5.5(a), the gate-source voltage of the load transistor (M_3) is equal to the voltage drop across the resistor i.e. $V_{SG3} = -V_R$. The effective gate-source voltage is then given by Equation 5.5 as shown below.

$$V_{GS,eff} = V_R - V_T \tag{5.5}$$

where V_R is the voltage drop across the resistor R. Unlike the conventional zero-V_{GS} load structure, $V_{GS,eff}$ of the proposed load (Equation 5.5) has an apparent reduction in its dependence over V_T thereby reducing the sensitivity of the load to any variation in its V_T. Not only does the proposed load reduces the dependence of $V_{GS,eff}$ on V_T, but also compensates for the variation in V_T.

Since the OTFTs used in this work are p-type enhancement devices, their V_T is positive. This means that the transistor conducts a current when its $V_{GS,eff}$ is negative and for this condition to be satisfied, V_R should always be less than V_T. Now, let us assume that V_T changes due to the bias-stress effect. When V_T decreases, $|V_{GS,eff}|$ decreases and this causes a decrease in the drain-source current. This decrease in drain-source current leads to a proportional decrease in the voltage drop (V_R) across R. As a result, $|V_{GS,eff}|$ increases proportionally, which in turn compensates the previous decrease in $|V_{GS,eff}|$ due to the variation in V_T. Similarly, it also compensates for the case when there is an increase in V_T. Thus, the proposed load is able to compensate any variations in V_T arising due to both the process mismatch and bias-stress effects.

The schematic of the proposed load using a zero-V_{GS} transistor instead of the resistor is shown in Figure 5.5(b). This load has two load transistors connected in a cascade fashion. An inverter circuit using such a cascaded zero-V_{GS} load is shown in Figure 5.6. The transistors M_1, M_2 and M_3 have a width of 800 μm, 7000 μm and 7000 μm respectively. All these transistors have a uniform length of 10 μm. To determine the theoretical

gain of the inverter, small-signal analysis is performed. The equivalent load resistance and the gain of the inverter is given by Equations 5.6 and 5.7 respectively.

$$\begin{aligned} R_L &= r_{ds2} + r_{ds3} + r_{ds2} \cdot r_{ds3} \cdot g_{m3}, \quad g_m \cdot r_{ds} >> 1 \\ &\approx r_{ds2} \cdot r_{ds3} \cdot g_{m3} \end{aligned} \tag{5.6}$$

$$\begin{aligned} A_V &= -g_{m1} \cdot (R_L \parallel r_{ds1}), \quad R_L >> r_{ds1} \\ &\approx -g_{m1} \cdot r_{ds1} \end{aligned} \tag{5.7}$$

where g_{m1} is the small-signal transconductance of M_1, g_{m3} is the small-signal transconductance of M_3, and r_{ds1}, r_{ds2} and r_{ds3} are the small-signal output resistances of M_1, M_2 and M_3 respectively. It can be observed from 5.7 that the cascaded zero-V_{GS} load inverter offers a high gain compared to the conventional zero-V_{GS} load inverter. However, the cascading reduces the current that flows through the inverter particularly when the OTFTs have a very small V_T and this has a degrading effect on the AC characteristics and the gain of the inverter. Thus, a cascaded zero-V_{GS} load inverter offers a high gain along with a significant improvement in its reliability.

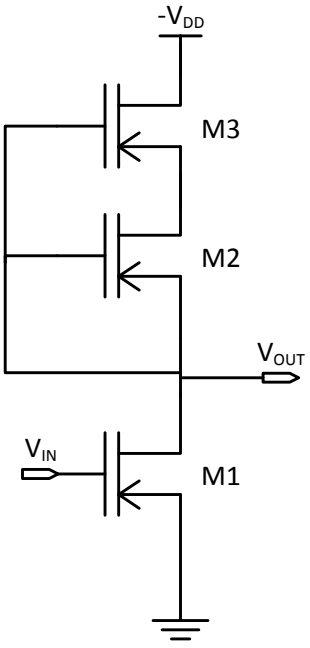


Figure 5.6: Schematic of an inverter using a cascaded zero-V_{GS} load

5.4 Performance Comparison of Various Load Circuits

To compare the performance of different load topologies, inverter circuits using diode, zero-V_{GS}, positive feedback and cascaded zero-V_{GS} load structures were designed and measured. Figure 5.7 shows the measured voltage transfer characteristics of the investigated inverters. The diode load inverter has the least output voltage swing whereas the zero-V_{GS} load inverter has the best output voltage swing. The positive-feedback inverter and the cascaded zero-V_{GS} load inverter has an output voltage swing that is in between that of the diode and zero-V_{GS} load inverter. The DC-gain of the inverters are shown in

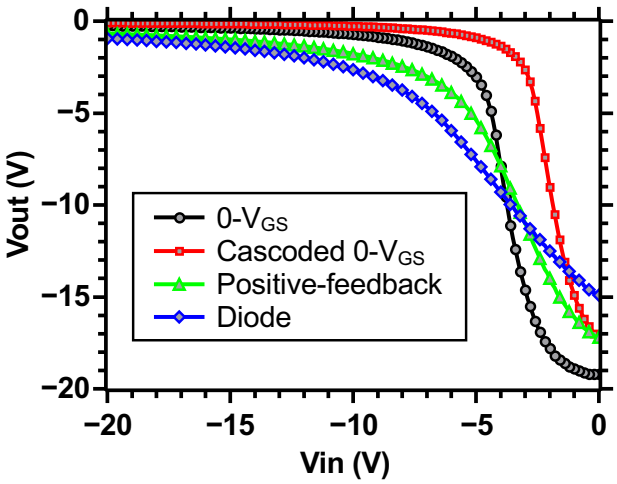


Figure 5.7: Measured voltage transfer characteristics of the investigated inverters.

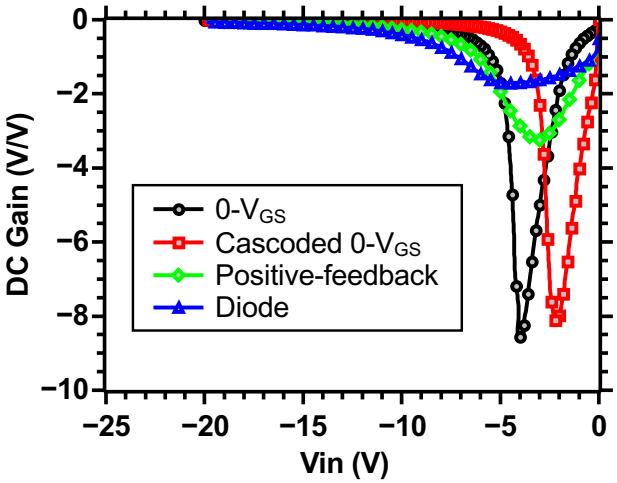


Figure 5.8: Measured DC gain versus V_{IN} characteristics of the investigated inverters.

Figure 5.8. As expected, the diode load inverter exhibits the least gain. The positive-feedback inverter provides a gain that is in between the gain offered by the zero-V_{GS} load and diode load inverters. Though the cascaded zero-V_{GS} load inverter has the potential to provide a gain that is higher than the conventional zero-V_{GS} load inverter, the experimental results (See Figure 5.8) show that the cascaded zero-V_{GS} load inverter offers almost the same gain as the conventional zero-V_{GS} load inverter. This inferior behaviour could be due to a low drain-source current flowing through the cascaded zero-V_{GS} inverter. The decrease in the drain-source current decreases the small-signal transconductance given by $g_m = 2I_{DS}/(V_{GS} - V_T)$ and therefore, the gain of the inverter is also reduced.

The AC characteristics of the investigated inverter circuits are shown in Figure 5.9. The positive-feedback and the cascaded zero-V_{GS} load inverters exhibit a zero-dB frequency of approximately 200 Hz. This is few hundred Hz less than the zero-dB frequency of the zero-V_{GS} load inverter. In the case of the positive-feedback inverter, the increase in the small-signal parasitic capacitance coming from the additional OTFT (M_4 in Figure 5.4) is responsible for the deterioration in the AC characteristics. In the case

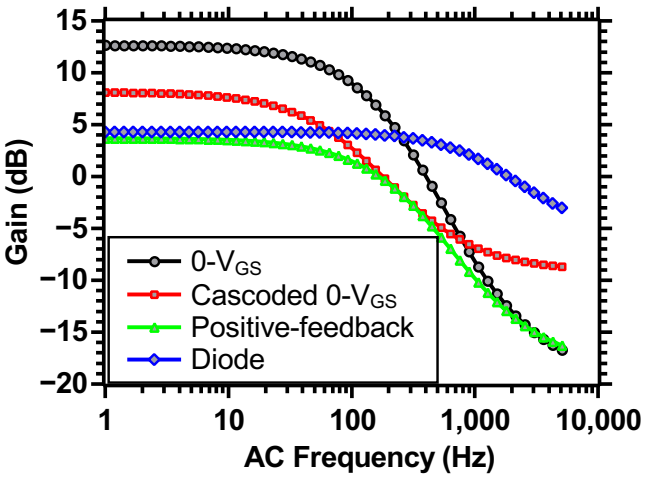


Figure 5.9: Measured AC characteristics of the investigated inverters

of the cascaded zero-V_{GS} load inverter, the deterioration in the AC characteristics is caused by the cascaded structure that increases the small-signal gate capacitance. The diode load inverter has a zero-dB frequecy in kHz range due to its strong pull-down current capability. Table. 5.3 shows the comparison of the performance metrics of all the investigated inverter topologies.

Table 5.3: Comparison of different inverter types.

Value	Diode	Zero-V_{GS}	Positive feedback	Cascaded zero-V_{GS}
Design Parameters (-VDD = -20 V)				
Width (μm) $M_1/M_2/$ ...	7000/800	800/7000	800/7000/ 800/7000	800/7000/ 7000
Length (μm)	10	10	10	10
Active Area (mm^2)	0.078	0.078	0.156	0.148
Performance Metrics				
Voltage swing (V)	-14	-19	-16.8	-17
Max. DC Gain (V/V)	-1.7	-8.5	-3.3	-8.1
Trip voltage (V)	-6	-4.5	-5	-2.9
Noise margin (V)	0.5	2.2	1	1.3
Unity-gain frequency (Hz)	2000	500	200	200

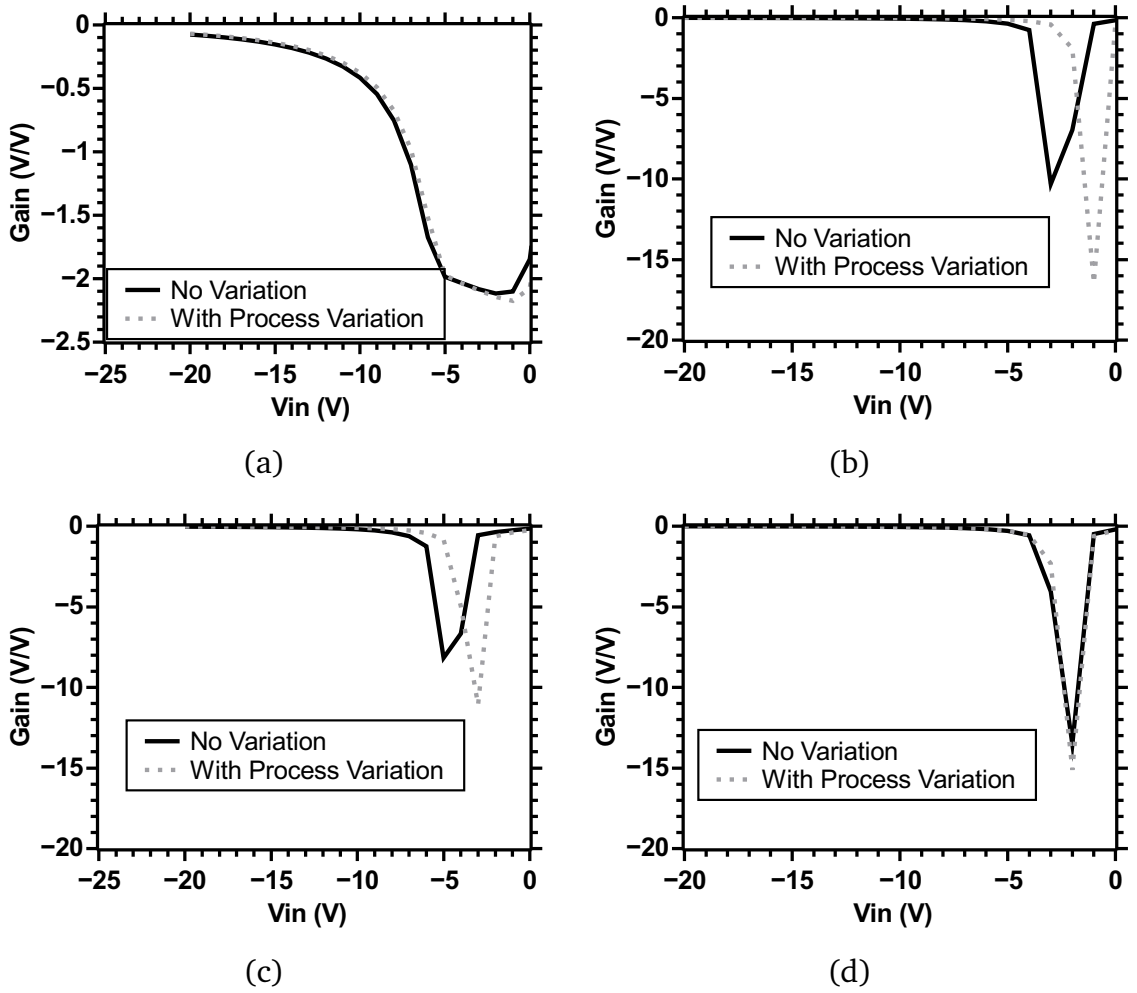


Figure 5.10: Simulated DC gain versus V_{IN} characteristics of (a) diode, (b) zero-V_{GS}, (c) positive-feedback and (d) cascaded zero-V_{GS} load inverter with and without process mismatch variation. The process mismatch variation was introduced to transistor M_2 by decreasing its V_T by 25 % of its original value.

5.4.1 Tolerance to OTFT Variations

To compare the reliability of the various inverter topologies, their tolerance towards process mismatch variations and bias-stress effect induced variations are tested. The process variations lead to a random mismatch in the drain-source current and V_T of an OTFT. These type of local variations are detrimental to analog circuits which usually requires a good amount of matching. The process variations are static in nature that is they occur only once at the time of fabrication and do not change after that. The bias-stress effects vary V_T of an OTFT and thus, further deteriorates the performance of organic circuits. Unlike process mismatch variations, the bias-stress effect induced variations [Ryu+10; Mat+07] are dynamically affecting the V_T of an OTFT.

5.4.1.1 V_T Variation due to Process Mismatch Variations

SPICE simulations were performed to compare the performances of the various inverter topologies in the presence of process variations. To be able to compare the impact of process and bias-stress induced variations, variation in the drain-source current was assumed to be zero for simplicity. Experimental data from several identical OTFTs fabricated on a same substrate indicated that the variation in V_T of an OTFT had a maximum variation around 25 % from its mean value. For the analysis, the inverters were initially simulated using mean value of all the transistor parameters that was extracted from the experimental data. Then, keeping all the other OTFT parameters namely γ, μ and λ unchanged, V_T alone was varied by 25 % from its previous value. For uniformity, the variations were only introduced to one of the load transistors i.e. M_2 in all the inverter circuits. From the output transfer characteristics, the gain of the inverters were calculated. Figure 5.10 depicts the gain of each of the inverter types with and without process variations.

It can be seen in Figure 5.10 that the diode load is less affected by the process variations. As explained earlier, the zero-V_{GS} load inverter is much affected by the process variation. The positive-feedback inverter has a variation of approximately 35 %. The cascaded zero-V_{GS} load inverter shows a significant resilience to process variations. Compared to the zero-V_{GS} load inverter, the cascaded zero-V_{GS} load offers around a 50 % reduction in the gain variation for a same amount of process variation. As described earlier in Section 5.3, this is mainly achieved by the reduction in the dependence of the effective gate-source voltage over V_T. The quantitative values are given in Table 5.4. It can be seen that the cascaded zero-V_{GS} load inverter exhibits a higher gain compared to a conventional zero-V_{GS} load inverter. The high gain of the positive-feedback load inverter is attributed to the close-to-unity feedback gain that was used for the simulations. The simulations were performed using a supply voltage of -20 V.

Table 5.4: Impact of V_T variation due to process variations on the maximum DC gain of different load types.

Load Type	DC gain w/o V_T variation (V/V)	DC gain with V_T variation (V/V)	Change in DC gain (|%|)
Diode	-2.1	-2.2	4.8
zero-V_{GS}	-10.3	-16.5	60.2
Positive-feedback	-8.2	-11.1	35.4
Cascaded zero-V_{GS}	-13.5	-15.1	11.9

5.4.1.2 V_T Variation due to Bias-Stress Effects

The bias-stress induced electrical instability in an OTFT is manifested by a shift in its V_T. This shift is dependent on time and bias-voltages (V_{GS} & V_{DS}). It is observed that the shift in V_T is minimum when the OTFT is operated in saturation regime and is maximum when the OTFT is operated in a linear regime [Ryu+10]. The fabricated inverters con-

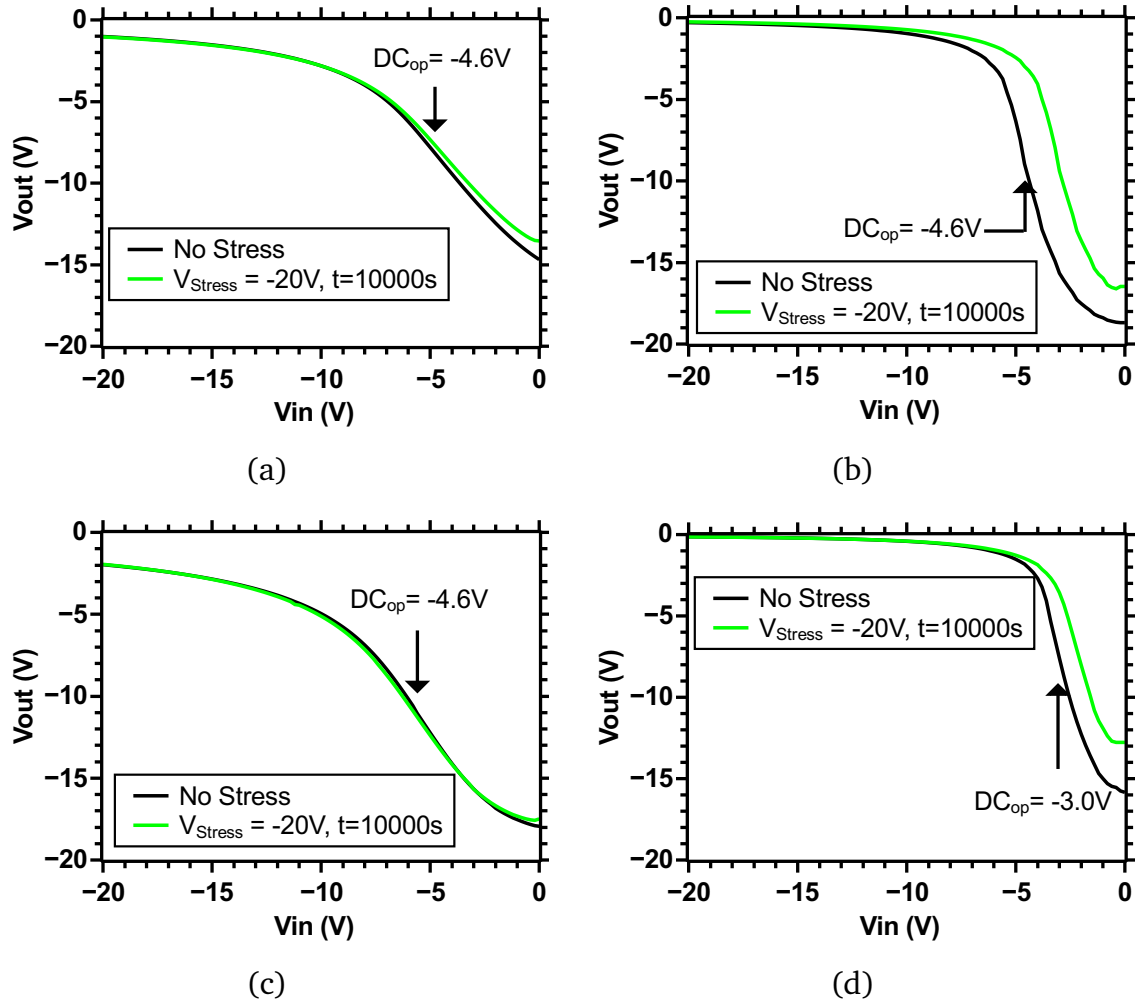


Figure 5.11: Voltage transfer characteristics of (a) diode (b) zero-V_{GS} (c) positive-feedback and (d) cascaded zero-V_{GS} load inverter for initial and stressed conditions.

taining diode, zero-V_{GS}, positive-feedback and cascaded zero-V_{GS} load structures were stressed by applying different stress voltages (V_{Stress}) and for different time intervals. The circuits were studied under both the DC and AC type of stress voltages.

DC Stress

The impact of the bias-stress effects on the AC gain of inverters when used as amplifiers was studied. The mid-point of the AC operating range of each inverter is chosen as its DC operating point. The chosen DC operating point of the investigated inverters are shown in Figure 5.11. The figure also shows the voltage transfer characteristics for both unstressed and stressed conditions. The AC gain of the investigated inverters for a sinusiodal input with a peak-to-peak voltage of 2 V was calculated. The AC gain was recalculated after the application of a stress voltage of -20 V for a time duration of 10000 s. The results are summarized in Table 5.5.

When the inverter is operated as a digital logic gate, the input signal level is confined to low (-20 V) or high (0 V). To find the impact of the bias-stress effects on inverters

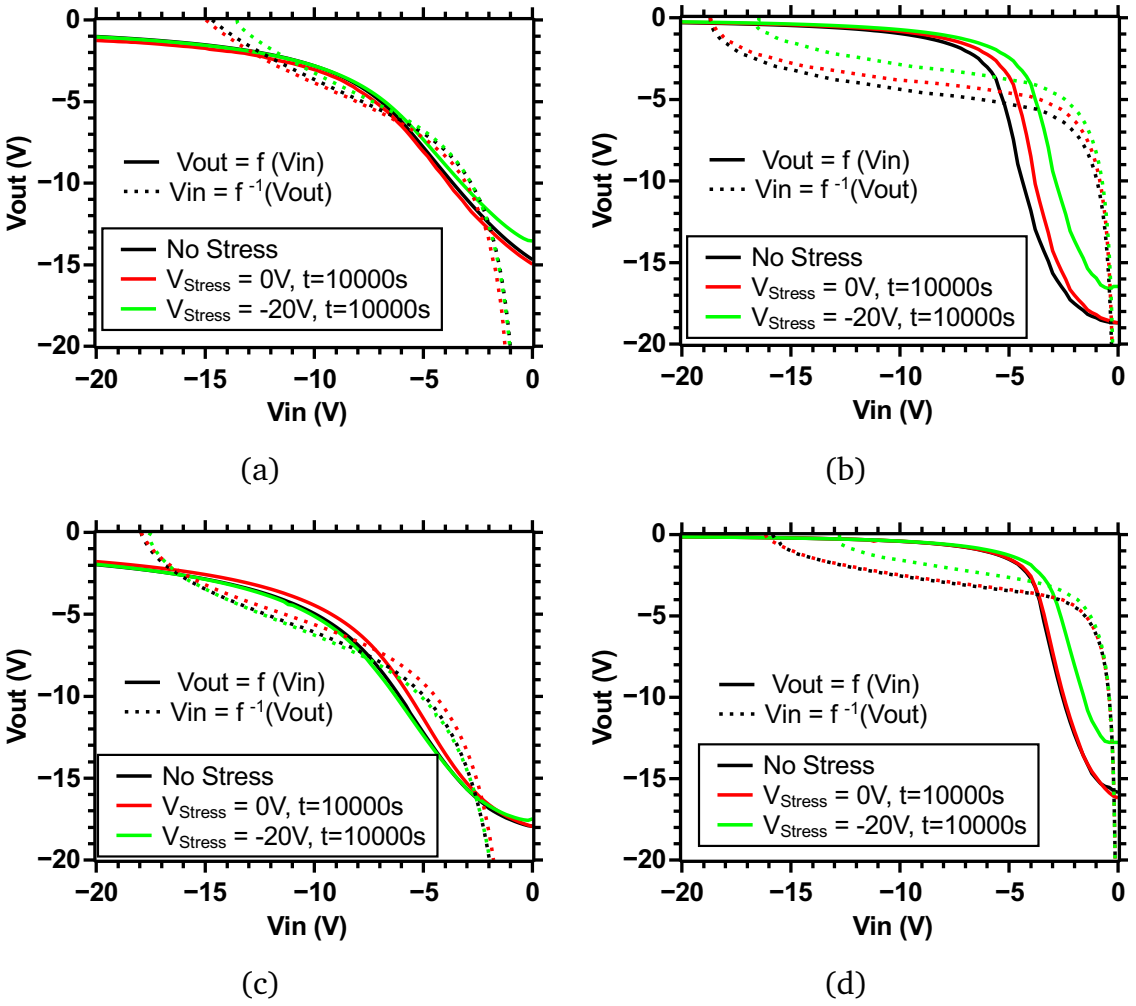


Figure 5.12: Voltage transfer characteristics and noise margin characteristics of (a) diode (b) zero-V_{GS} (c) positive-feedback and (d) cascaded zero-V_{GS} load inverter for various stress conditions.

Table 5.5: Impact of V_T variation due to bias-stress effects on the AC gain of different inverting amplifier circuits using different load structures.

Load Type	AC gain with no stress (V/V)	AC gain with V_{Stress}* = -20 V (V/V)	Change in AC gain (|%|)
Diode	-1.7	-1.5	12
zero-V_{GS}	-4.3	-1.9	55
Positive-feedback	-2.1	-1.9	11
Cascaded zero-V_{GS}	-4.6	-3.1	35

* The stress voltage was applied for a time duration of 10000 s.

when used as a logic gate, stress voltages (V_{Stress}) of 0 and -20 V were applied. First, the voltage transfer characteristics of the investigated inverters without any application of stress were measured. Then, a V_{Stress} of 0 V is applied to the input terminal for a

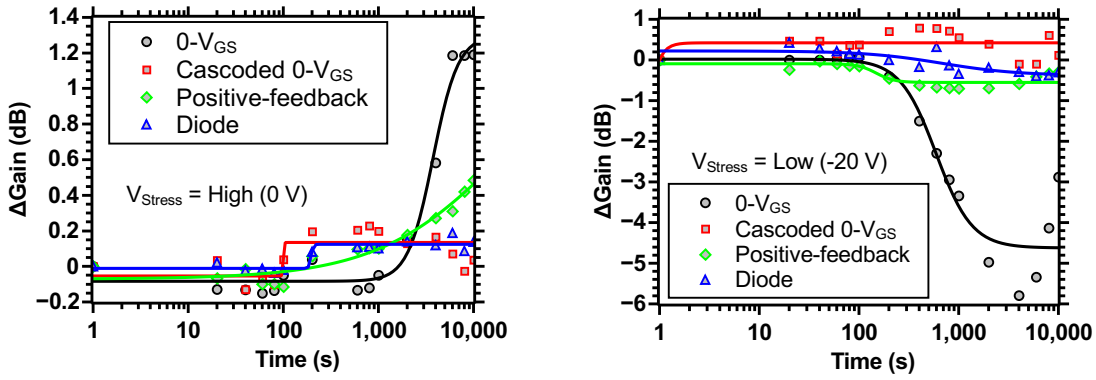


Figure 5.13: The changes in the DC gain of the investigated inverter types when stressed with (a) high and (b) low voltage signal levels.

time interval of 10000 s and the voltage transfer characteristics are measured. Similarly, the measurements were performed for a V_{Stress} of -20 V. The experimental results corresponding to a) no stress, b) V_{Stress} of 0 V and c) V_{Stress} of -20 V are shown in Figure 5.12. Looking broadly, the output of all the inverters is much affected when V_{Stress} is -20 V. The reason for this can be ascertained by analysing the operation regime of the input transistor (M_1). M_1 operates in saturation regime when a V_{Stress} of 0 V is applied to the input terminal (V_{in}). But, when a V_{Stress} of -20 V is applied to the input terminal, M_1 operates in linear regime. Since, the bias-stress induced shift in V_T of an OTFT operating in the linear regime is larger than the shift in the saturation regime, the output is much affected when V_{Stress} is -20 V.

To visualize the noise margin of the investigated inverters, functional inverse of their voltage transfer characteristics are added in Figure 5.12. The values of noise margin were extracted for all the curves from Figure 5.12. These values are shown in Table. 5.6. In accordance with our earlier explanation, the noise margin is much affected when V_{Stress} is -20 V. Among all the inverter topologies, the zero-V_{GS} load inverter offers the best noise margin value of 2.82 V. However, the zero-V_{GS} load inverter suffers the most due to the bias-stress induced variations. Due to the compensation mechanism involved in the cascaded zero-V_{GS} load inverter, compared to the conventional zero-V_{GS} load inverter, it fares better especially for the case with a stress voltage of 0 V. The most reliable among all the four inverters, for both the low and high stress voltages, is the positive-feedback inverter. In addition to the noise margin, the changes in the DC gain of the inverters were also studied. The inverters were stressed for a specific time and their DC gain was measured at the end of the stress period. The inverters were stressed in such a way that 5 data points were obtained for each decade upto a maximum stress time of 10000 s. The results for a high and low stress voltages are shown in Figure 5.13(a) and 5.13(b) respectively. It is evident, again, that the degradation in the performance of an inverter is much pronounced when the stress voltage is low. Furthermore, the compensation mechanism in the cascaded zero-V_{GS} load inverter decreases the gain-degradation compared to that of a conventional zero-V_{GS} load inverter.

Table 5.6: Impact of bias-stress on the noise margin of the inverter types.

Load Type	No Stress (V)	V_{Stress}* = -0 V (V)	Change (|%|)	V_{Stress}* = -20 V (V)	Change (|%|)
Diode	0.59	0.56	5	0.42	29
zero-V_{GS}	2.82	2.46	13	1.82	36
Positive feedback	0.87	0.86	1	0.81	7
cascaded zero-V_{GS}	1.82	1.78	2	1.23	32

* The stress voltages were applied for a time duration of 10000 s.

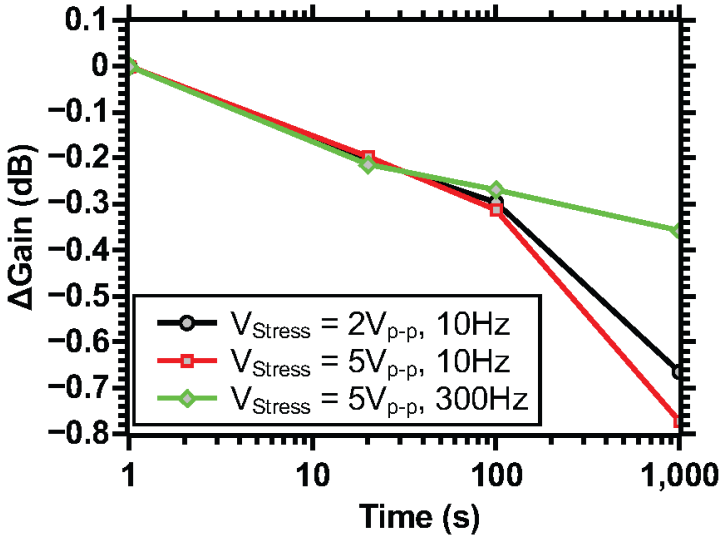


Figure 5.14: The changes in the DC gain of the zero-V_{GS} load inverter for a sinusoidal stress voltage.

AC Stress

To study the impact of bias-stress effects corresponding to an analog input signal, a sinusoidal stress voltage was applied to the input terminal of the zero-V_{GS} load inverter. A conventional zero-V_{GS} load inverter was chosen for this analysis because of its greater susceptibility to bias-stress induced V_T variation as we have seen in Section 5.4.1.2 . Three different cases were analysed: a) V_{Stress} with 2 $V_{p\text{-}p}$ at 10 Hz, b) V_{Stress} with 5 $V_{p\text{-}p}$ at 10 Hz, and c) V_{Stress} with 5 $V_{p\text{-}p}$ at 300 Hz. The results are shown in Figure 5.14. The results suggest that the degradation reduces as the frequency of the stress voltage is increased. This behaviour can be explained by the shorter effective stress time at higher frequencies. The application of an AC stress cycle involves both stress and relax phases which means for one half cycle the OTFT is stressed and for the second half cycle it is de-stressed. As the frequency of the stress signal increases, the effective time for which the OTFT is stressed reduces. This is because less charges are trapped at a higher frequency and variation in V_T is reduced. Therefore, as frequency of the stress signal is increased the stress time is reduced and hence, the degradation in an OTFT is reduced.

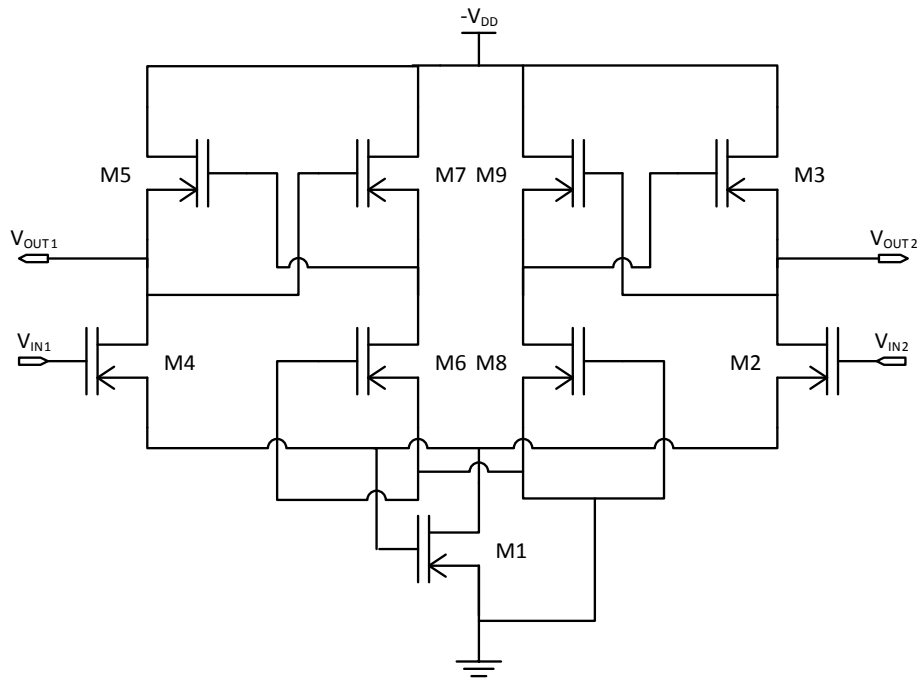


Figure 5.15: Circuit schematic of an organic differential amplifier using a positive feedback load.

5.5 Organic Differential Amplifiers

A differential amplifier is an electronic circuit that amplifies the difference between two input signals and suppresses what is common to both of them. This analog circuit block is a basic constituent of complex analog circuits like operational amplifiers and analog comparators. The differential amplifier converts the input voltages into two currents, subject to the condition that the sum of these currents must remain constant. In this work two differential amplifier circuits were designed using the proposed load topologies namely the positive feedback and cascaded zero-V_{GS} load topologies.

5.5.1 Differential Amplifier using a Positive Feedback Load

The schematic of a differential amplifier with a positive feedback load is shown in Figure 5.15. Transistors M_4 and M_2 are the input transistors corresponding to V_{IN1} and V_{IN2} respectively. Transistors M_3 and M_5 are the load transistors which are biased by a positive feedback circuit. In order to have a positive feedback, source follower circuits formed by M_6-M_7 and M_8-M_9 are used. The source follower circuit has a gain less than unity. Transistor M_1 acts as a current source that sets the total current flowing

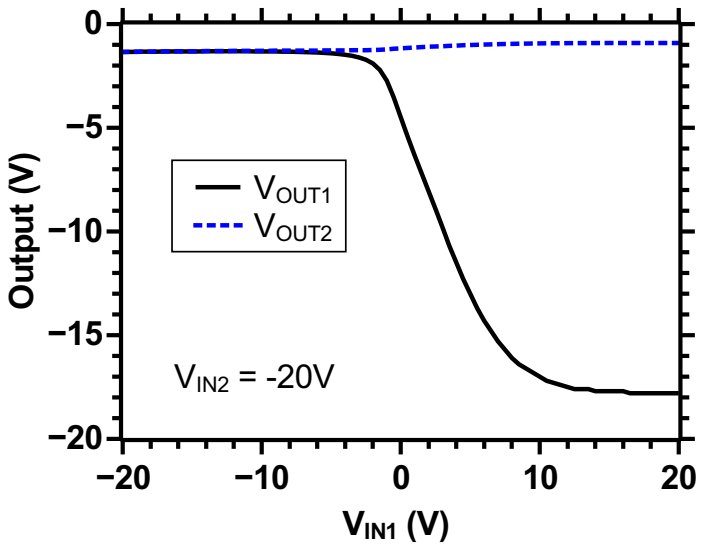


Figure 5.16: Measured output of the differential amplifier using a positive feedback load.

through both the paths of the differential amplifier. Performing small-signal analysis, the differential mode gain of the differential amplifier is given by:

$$A_{V,diff} = -g_{m2,4}\left[r_{ds2,4}||\left[\frac{1}{g_{m3,5}(1-A_F)}\right]\right] \tag{5.8}$$

$$\text{where} \qquad A_F = \frac{g_{m9,7}\left(r_{ds8,6}||r_{ds9,7}\right)}{1+g_{m9,7}\left(r_{ds8,6}||r_{ds9,7}\right)} \tag{5.9}$$

It can be observed that the differential gain is equal to the gain of a common-source amplifier but with the advantages of a differential pair i.e. common-mode rejection, differential-signal amplification and reduced distortion through suppression of even spectral components. It must be mentioned that the equations given above is valid for a differential pair having a strict symmetry. Similarly, the common mode gain of the differential amplifier is given by:

$$A_{V,CM} = -g_{m2,4}\left[r_{ds2,4}||\left[\frac{1}{g_{m3,5}(1-A_F)}\right]\right]\cdot\left[\frac{1}{1+2g_{m2,4}r_{ds1}}\right] \tag{5.10}$$

$$\text{where} \qquad A_F = \frac{g_{m9,7}\left(r_{ds8,6}||r_{ds9,7}\right)}{1+g_{m9,7}\left(r_{ds8,6}||r_{ds9,7}\right)} \tag{5.11}$$

It can be observed from Equation 5.10 that the common mode gain $A_{V,CM}$ can be reduced by increasing r_{ds1} and r_{ds1} is inversely proportional to W/L ratio. Therefore, the common mode gain can be reduced by increasing width or decreasing length of the current source transistor M_1. The measured results of the differential amplifier are shown in Figure 5.16. The measurements were performed using a supply voltage of -20 V. The input voltage V_{IN1} is swept from -20 V to +20 V and the output voltages are

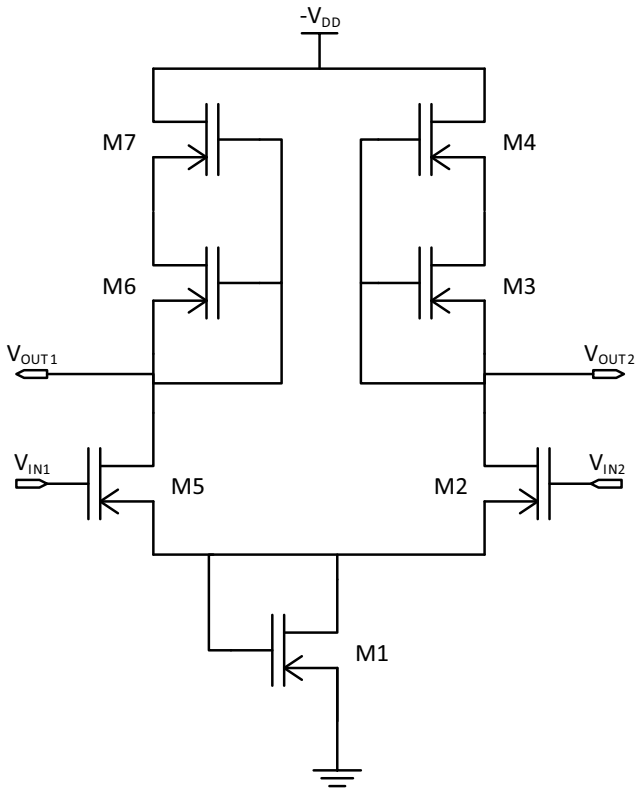


Figure 5.17: Circuit schematic of an organic differential amplifier using a cascaded zero-V_{GS} load.

plotted. Through out the measurement, V_{IN2} was held constant at -20 V. Since V_{IN2} is -20 V, V_{OUT2} is saturated and stays around 0 V. Only V_{OUT1} varies with the input sweep of V_{IN1}. The AC characteristics of the differential amplifier was also measured and the differential amplifier exhibited a maximum gain of 3.4 dB for a sinusoidal input with a peak-to-peak voltage of 0.5 V. The 3-dB cut-off frequency was measured to be around 80 Hz.

5.5.2 Differential Amplifier using a Cascaded Zero-V_{GS} Load

The schematic of a differential amplifier with a cascaded zero-V_{GS} load is shown in Figure 5.17. Transistors M_5 and M_2 are the input transistors corresponding to V_{IN1} and V_{IN2} respectively. Transistor sets M_3-M_4 and M_6-M_7 form the cascaded load structures.

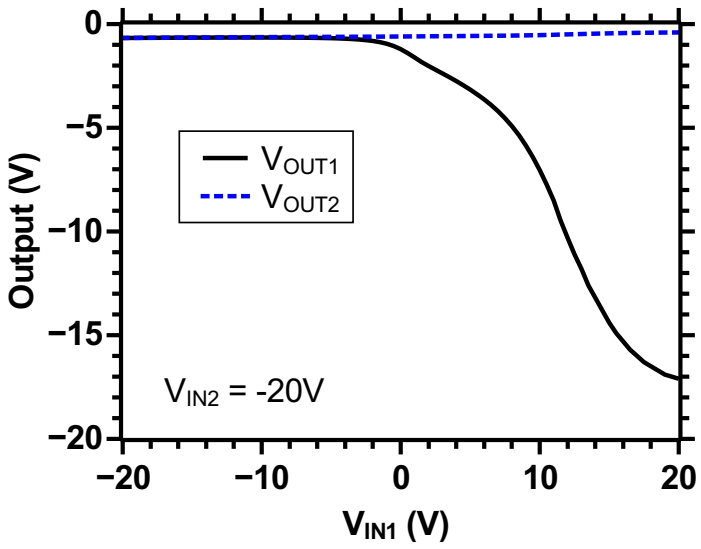


Figure 5.18: Measured output of the differential amplifier using a cascaded zero-V_{GS} load.

Performing small signal analysis, the differential mode gain of the differential amplifier is given by:

$$\begin{aligned} A_{V,diff} &= -g_{m2,5}\left[r_{ds2,5}||\left[r_{ds3,6}+r_{ds4,7}+g_{m2,5}r_{ds3,6}r_{ds4,7}\right]\right] \\ &= -g_{m2,5}\left[r_{ds2,5}||\left[g_{m2,5}r_{ds3,6}r_{ds4,7}\right]\right] \;;\; \text{when } g_m r_{ds} >> 1 \\ &\approx -g_{m2,5}\left[r_{ds2,5}\right] \;;\; \text{for } g_{m2,5}r_{ds3,6}r_{ds4,7} >> r_{ds2,5} \end{aligned} \tag{5.12}$$

(5.13)

Again, it can be observed that the differential gain is equal to the gain of a common-source amplifier but with the advantages of a differential pair i.e. common-mode rejection, differential-signal amplification and reduced distortion through suppression of even spectral components. Similarly, the common mode gain of the differential amplifier is given by:

$$\begin{aligned} A_{V,CM} &= -g_{m2,5}\left[r_{ds2,5}||\left[r_{ds3,6}+r_{ds4,7}+g_{m2,5}r_{ds3,6}r_{ds4,7}\right]\right]\cdot\left[\frac{1}{1+2g_{m2,5}r_{ds1}}\right] \\ &\approx -g_{m2,5}r_{ds2,5}\cdot\left[\frac{1}{1+2g_{m2,5}r_{ds1}}\right] \;;\; \text{for } g_{m2,5}r_{ds3,6}r_{ds4,7} >> r_{ds2,5} \end{aligned} \tag{5.14}$$

It can be observed from Equation 5.14 that the common mode gain $A_{V,CM}$ can be reduced by increasing r_{ds1}. The measured results of the differential amplifier using a cascaded zero-V_{GS} load are shown in Figure 5.18. The measurements were performed using a supply voltage of -20 V. The input voltage V_{IN1} is swept from -20 V to +20 V and the output voltages are plotted. Through out the measurement, V_{IN2} was held constant at -20 V. Since V_{IN2} is -20 V, V_{OUT2} is saturated and stays around 0 V. Only V_{OUT1} varies with the input sweep of V_{IN1}. The AC characteristics of the differential amplifier was also measured and the differential amplifier exhibited a maximum gain of 5.8 dB for an

input with a peak-to-peak voltage of 0.5 V. Thus a differential amplifier using a cascaded zero-V_{GS} load offers a relatively good gain compared to the differential amplifier using a positive feedback load. The 3-dB cut-off frequency was measured to be around 80 Hz.

5.6 Organic Analog-to-Digital Converters

In the recent years, organic electronics has gained popularity for their potential in realizing smart label systems that contain sensors integrated with the RFID tags on cheap and flexible substrates. Commercial applications of such intelligent RFID tags include item-level tagging solutions for cost-sensitive supply chain processes, for e.g. these smart tags provide a cheap and efficient means to monitor the vital parameters of the the food and pharmaceuticals throughout their logistics chain. Such smart tags are also expected to open-up cost sensitive sectors for the Internet-of-Things (IoT) by providing a low-cost holistic sensory monitoring [WD10]. Organic smart tags, also called as smart labels, will be discussed in detail in Chapter 6.4.

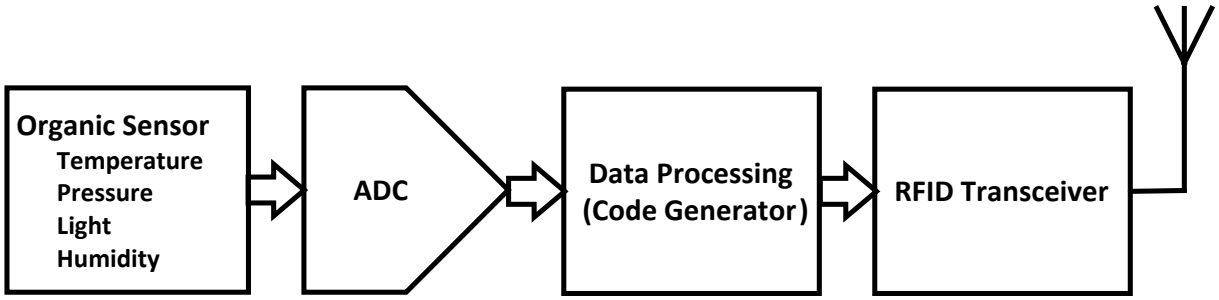


Figure 5.19: Schematic overview of a Smart label system.

The block diagram of a typical smart label system is shown in Figure 5.19. To realize any smart label it is very much essential to develop sensor interface circuits like ADCs. Few organic ADC circuits have been reported using $\Delta\Sigma$ [Mar+10], successive approximation register [Xio+10a] and counting ADC [Rai+13] architectures. These circuits use one or more analog components like operational amplifiers, comparators etc. which demand a high level of transistor matching for accuracy. As discussed in Chapter 3, fabrication of OTFT involves large process variations, often orders of magnitude higher than those in crystalline silicon processes [Can+03]. Thus designing an ADC using organic transistors is more challenging and this is the reason why very few organic ADC circuits have been reported till date. Although these variations also affect digital circuits, their effect on them is less pronounced since digital circuits do not require matching. In addition to this, designing an analog circuit is much more challenging compared to designing a digital circuit which is mainly due to the stringent tolerance requirements of any analog circuit. Therefore, an ADC architecture that is highly digital in composition is of high interest to the organic electronics community.

5.7 Digital Analog-to-Digital Converter Architectures

In this work we have chosen two digital ADC architectures namely a) VCO based ADC and b) a digital flash ADC. VCO based ADC architecture operates as a digital, time-

based circuit and it converts an analog input voltage to frequency domain and then converts the frequency to its corresponding digital output. It has a simple structure consisting of a voltage-controlled ring oscillator and an encoder logic. This property of having mostly digital composition makes it a potential candidate for realizing an organic ADC that is able to operate optimally even in the presence of relatively large parameter variations. The digital flash ADC uses a digital inverter based comparator circuit instead of the conventional differential amplifier based analog comparator. These circuits will be discussed in detail in the coming sections.

5.8 VCO-based Analog-to-Digital Converter

The VCO-based ADC comprises of a VCO and a Frequency to Digital Converter (FDC) as shown in Figure 5.20. The VCO converts the input voltage into frequency information and the FDC translates this frequency information into a binary code by integrating the VCO output over a time interval T_s. An overview of the ADC's operation is shown in Figure 5.20. A simple FDC, shown in Figure 5.21, consists of a counter and a register. The counter counts the edges in the VCO output within the given time interval T_s and stores the value in a register. Since this is a linear transformation, the linearity of the whole ADC can be easily estimated by knowing the linearity of the VCO's voltage-frequency characteristic. The output of the FDC can be calibrated further to yield the exact digital code corresponding to the analog input voltage. Since we use a Voltage Controlled Ring Oscillator (VCRO) consisting of inverter-based delay stages, the VCO-based ADC can be considered to be completely digital. Owing to its digital nature, the main advantages of the VCO-based ADC are lower power consumption, less area and robustness against parameter and mismatch variation. It must be noted that the maximum resolution of the VCO-based ADC is set by the VCO's resolution which means that if the FDC has ideal characteristics, the resolution of the whole VCO-based ADC equals the resolution of the VCO. Therefore a VCO is the most critical part of any VCO-based ADC architecture. The non-linearity in the VCO's voltage-to-frequency conversion severely limits the resolution of the VCO-based ADC [HS12]. So VCOs need to be thoroughly analysed with regard to its voltage-to-frequency conversion property.

Though the design of VCO-based ADCs [WMM03; HS12] using silicon transistors has been widely reported in the literature, it is yet to be explored as far as organic electronics is concerned. Furthermore, in the field of organic electronics there exists enough literature [CKJ12; Nau+10] pertaining to ring oscillator design using OTFTs. However, there is none that investigate various VCO circuits using different delay cells and their worthiness in building an organic VCO-based ADC. In this section, we have concentrated on this very issue and have analysed the performance of various organic VCO circuits based on different delay cells and their suitability for a VCO-based ADC design. The equations to calculate the maximum resolution of the VCO-based ADC from the V-f curve of the VCO was formulated in this direction. In addition the impact of jitter and $1/f$ noise of the VCO on the performance of the ADC was also investigated.

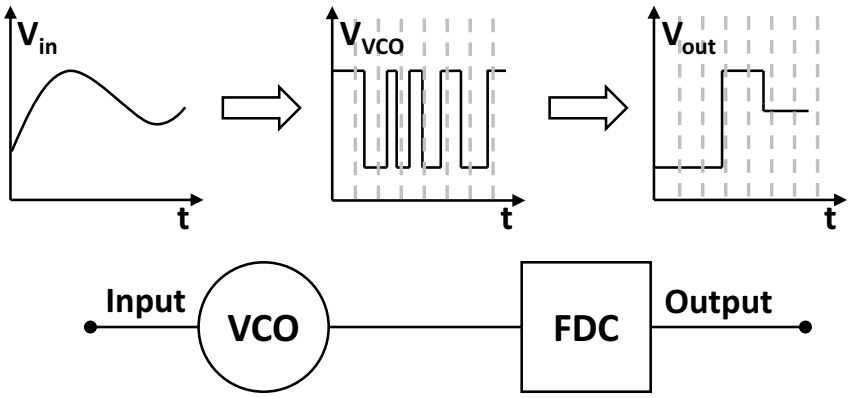


Figure 5.20: Block diagram of VCO-based ADC and overview of its operation

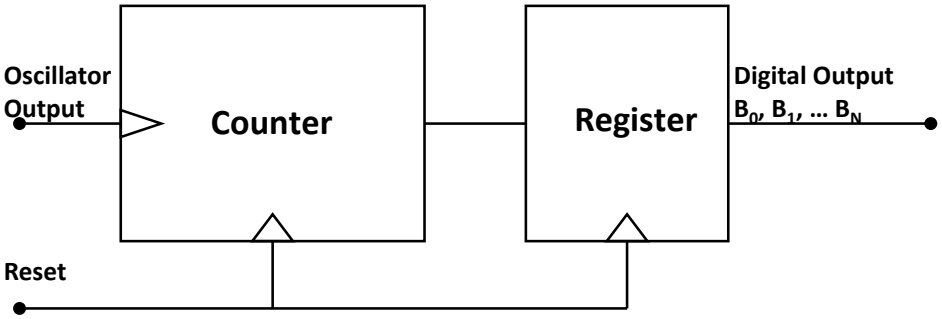


Figure 5.21: Schematic overview of a frequency to digital converter (FDC)

5.8.1 Voltage Controlled Oscillator

A voltage-controlled (ring) oscillator consists of a series of (tunable) delay stages connected in a loop in which output of the last stage is fed back as input to the first stage and the output of the intermediate stages is connected to the input of their succeeding stages. According to the Barkhausen's criterion, the ring oscillator must provide unity loop gain and a total phase shift of 2π to achieve an oscillating output. Here, each delay stage provides a phase shift of π/N, where N is the number of delay stages. The remaining π phase shift is provided by the DC inverted feedback and this necessitates a (single-ended) ring oscillator to have an odd number of delay stages. If we assume that each stage provides a delay of t_d, then the frequency of oscillation can be calculated using Equation 5.15. With each stage contributing a phase shift of π/N, the signal after passing through each of the N delay stages once will provide the first phase shift (π) in a time of Nt_d. Then, the signal must go through each stage a second time to obtain the remaining (π) phase shift, resulting in a total period of $2Nt_d$.

$$f = \frac{1}{2Nt_d} \tag{5.15}$$

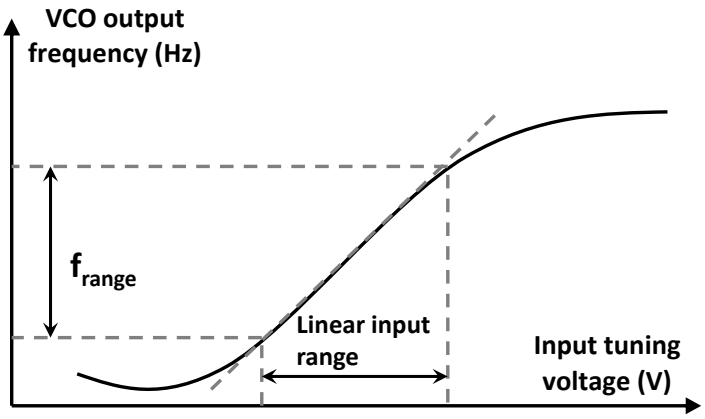


Figure 5.22: Input operating range of the VCO

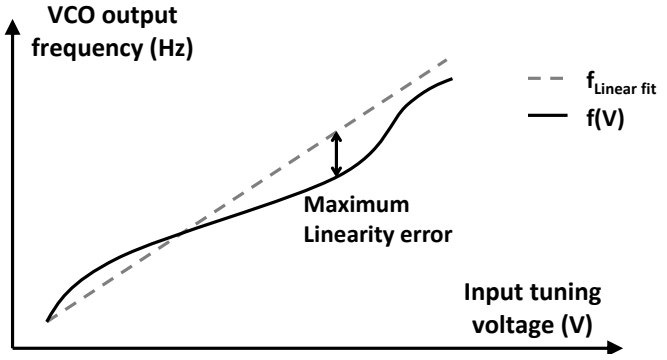


Figure 5.23: Determination of the maximum linearity error

The delay per stage (t_d) is defined as the ratio of its output voltage swing (V_{SW}) over its slew rate (I_{SS}/C_L). Thus, the delay per stage is given by $t_d = C_L V_{SW}/I_{SS}$. Here we assume that the output swings between rail-to-rail voltages. Substituting $V_{SW} = V_{DD}$ and t_d in Equation 5.15, the frequency of the output signal from the VCO becomes

$$f = \frac{I_{SS}}{2N C_L V_{DD}} \tag{5.16}$$

Here, I_{SS} is the tail current of a single delay cell, V_{DD} the supply voltage and C_L the equivalent load capacitance seen at the output of each delay stage.

One of the important metrics to evaluate an ADC is its resolution. As previously stated, the voltage-controlled oscillator is the most critical part of the ADC. It predominantly determines the critical performance metrics of a VCO-based ADC. Therefore, in this work, we have extensively investigated various delay cells and the corresponding VCO for realizing an organic VCO-based ADC. The bottleneck of a VCO-based ADC is the presence of non-linearities in its input voltage to frequency conversion scheme. Ideally, the voltage-to-frequency conversion is linear for the entire input range. However, real circuits do not show strictly linear behaviour. Hence, the range of input values for which the V-f curve remains more or less linear is taken as the input operating range of the VCO-based ADC. The nonlinearity associated with the output frequency of a VCO and the choice of desirable operating range is shown in Figure 5.22. Inside the chosen operating range,

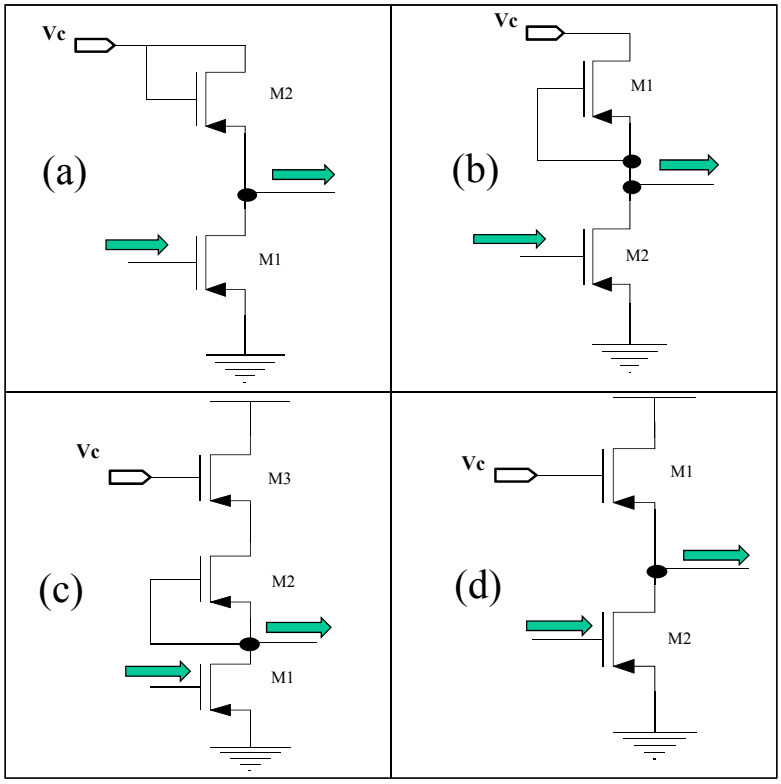


Figure 5.24: Schematic of a) diode load b) zero-V_{GS} (cut-off) load c) current-starved and d) biased load delay cell. The arrows pointing in and out denote the input and output of each delay stage.

the maximum difference between the V-f curve ($f(V\ )$) and its corresponding linear fit ($f_{linear}(V\ )$), shown in Figure 5.23, determines the minimum quantization step size of the VCO-based ADC. Thus the total number of quantization steps, which is equivalent to 2^N, is given by the ratio between the VCO output frequency range and the minimum quantization step size i. e. the maximum linearity error. The total number of quantization steps is given by Equation 5.17. Here $f(V\ )_{max}$ and $f(V\ )_{min}$ denote the maximum and minimum output frequency of the VCO for the chosen input range. Given the total number of quantization levels, the resolution (N) of the VCO-based ADC can be calculated using equation 5.18.

$$Quantization\ Steps\ (2^N) = \frac{f(V\ )_{max} - f(V\ )_{min}}{max\ (|\ f(V\ ) - f_{linear}(V\ )\ |)} \tag{5.17}$$

$$Resolution = \left| \frac{log\ (Quantization\ Steps)}{log\ (2)} \right| \tag{5.18}$$

5.8.1.1 Delay Cells

In this work, we have investigated four different inverter-based tunable delay cells namely zero-V_{GS} load, diode load, biased load and current starved load delay cells. The schematic of the investigated delay cells are presented in Figure 5.24. The fre-

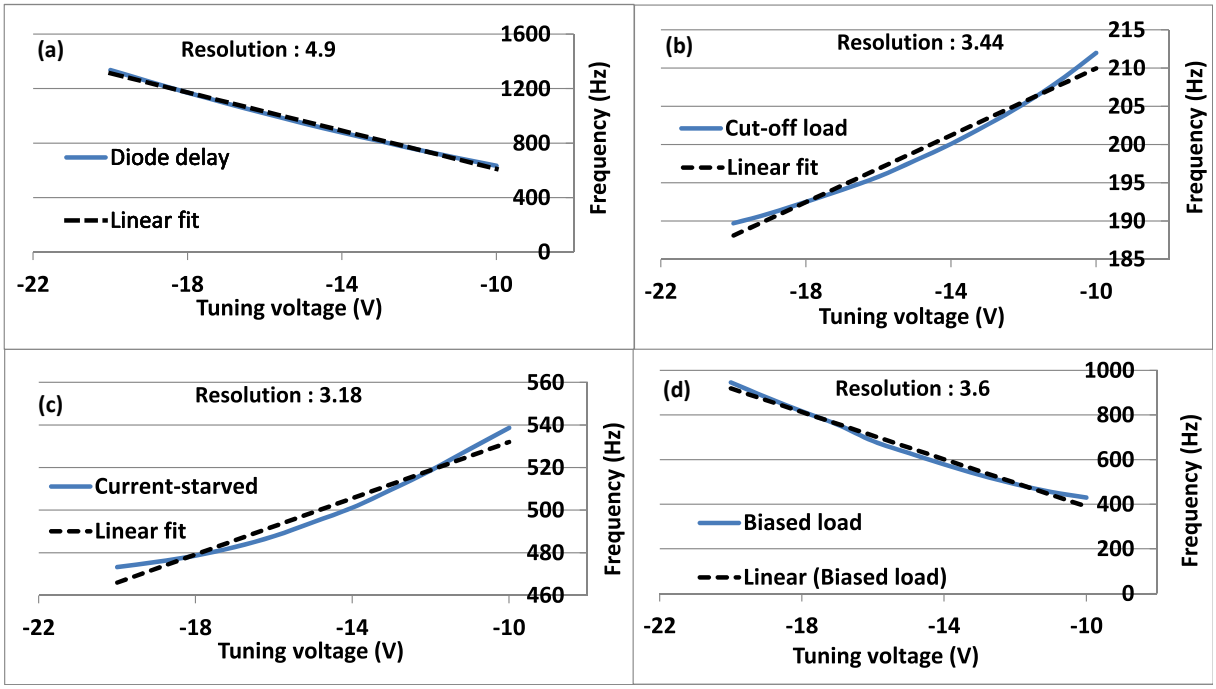


Figure 5.25: Simulated voltage versus frequency plot of the 11-stage VCO with a) diode load b) zero-V_{GS} (cut-off) load c) current-starved and d) biased load delay cell.

quency (f) of the output signal from a VCO can be controlled by varying either the equivalent load capacitance C_L or the power supply voltage V_{DD} or the tail current I_{SS} as observable from Equation 5.16. The investigated delay cells use one of the latter two methods to vary the frequency of the VCO's output. In the case of a biased load delay cell, the tuning voltage controls the gate bias of the load transistor M_1 which is shown in Figure 5.24d. Hence, as the tuning voltage changes, the effective gate-source voltage of M_1 changes and the charging/discharging current flowing through M_1 also changes. Thus, it uses the current to vary the output frequency. The current-starved delay stage uses a similar method as well.

In zero-V_{GS} and diode load delay cells, the tuning voltage is applied at the supply voltage rail and so the output frequency is changed according to the changes in the tuning voltage. In the case of a zero-V_{GS} load delay cell, the transistor M_1 (see Figure 5.24b) operates in the saturation region with a fixed effective gate-source voltage (i.e. $V_{GS}-V_T$) that is equal to the threshold voltage (V_T). The tuning voltage is applied at the drain of M_1. Any change in the tuning voltage (V_{tune}) will alter the drain-source voltage (V_{DS}) of M_1 and leads to a linear change in the current flowing through transistor M_1 with a linearity constant equal to the channel-length modulation parameter (λ). Therefore, the zero-V_{GS} load delay cell is expected to provide the best possible linear behaviour in the voltage-to-frequency conversion feature and eventually the best resolution for the VCO-based ADC. For a diode load delay cell shown in Figure 5.24a, the load transistor M_2 is operated in saturation regime with its drain and gate terminals shorted and exhibits a diode like transfer characteristics. Thus when the tuning voltage is applied at the drain/gate terminal of M_2, any change in the tuning voltage results in a non-linear

change in the current through M_2. This leads to an increased linearity error compared to the zero-V_{GS} load based delay cell.

Inverter Delay cell	Resolution (bits)	Tuning sensitivity (Hz/V)	Frequency range (Hz)
Diode load	4.90	-56.4	702.6
zero-V_{GS} load	3.44	1.3	22.3
Current starved	3.18	2.4	65.4
Biased load	3.60	-25.3	516.5

Table 5.7: Comparison of different inverter delay cells

Voltage-controlled ring oscillator circuits using the above four types of delay stages were designed and analyzed. The simulated frequency-vs-voltage curve and their resolution is shown in Figure 5.25. It can be observed that the sub-figure corresponding to the zero-V_{GS} (Figure 5.25b) and current starved (Figure 5.25c) delay cells have a decreasing slope unlike the others. For any delay cell, when the input tuning voltage is swept, its (absolute) tail current $|I_{SS}|$ increases and its equivalent load capacitance C_L even though assumed to be a constant increases slightly. Now, if the increase in the tail current is less than the increase in the load capacitance, the output frequency, given by Equation 5.16, shows a decreasing slope in the V-f plot. To confirm this, we have measured two different VCO circuits based on zero-V_{GS} load delay cell but using different width and length dimensions. The measurement results are discussed in Section 5.8.2. The performance metrics of the various delay cells are given in Table 5.7. It is clearly evident from the table that out of the four investigated delay cells, the diode-load delay cell offers maximum resolution, along with a good tuning sensitivity that is clearly better than that of a zero-V_{GS} load based delay cell. Tuning sensitivity (Hz/V) is defined as the change in the VCO output frequency for a unit change in the tuning voltage. Despite having a large linearity error (i. e. quantization step size), the diode load delay cells has a higher number of quantization steps (see Equation 5.17) due to its higher frequency range. Therefore the resolution of a VCO using diode load delay cells is high compared to that using zero-V_{GS} load delay cells.

5.8.2 Results and Discussion

To substantiate the results from the simulation, we fabricated and measured two VCO circuits containing diode-load (see Fig. 5.24a) and zero-V_{GS} load (see Fig. 5.24b) delay cell respectively. The measured frequency versus voltage characteristics of the voltage-controlled ring oscillator using zero-V_{GS} load delay cell is presented in Fig. 5.26a. The zero-V_{GS} load delay cell based VCO produces a resolution of 3.48 bits with a frequency range of 17 Hz. This goes well with the resolution and output frequency range obtained from simulation results (see Table.5.7). The transistors M_1 and M_2 of the zero-V_{GS} load delay cell, as shown in Fig. 5.24b, has a W/L ratio of 800 μm/5 μm and 7000 μm/5 μm respectively. As explained in section 5.8.1.1, the frequency of the output of the zero-V_{GS} load inverter based VCO is linearly dependent on the tuning voltage through the channel-length modulation parameter (λ) of M_1. Accordingly, the maximum difference between the measured V-f curve and the linear fit, in this case, was observed to be very

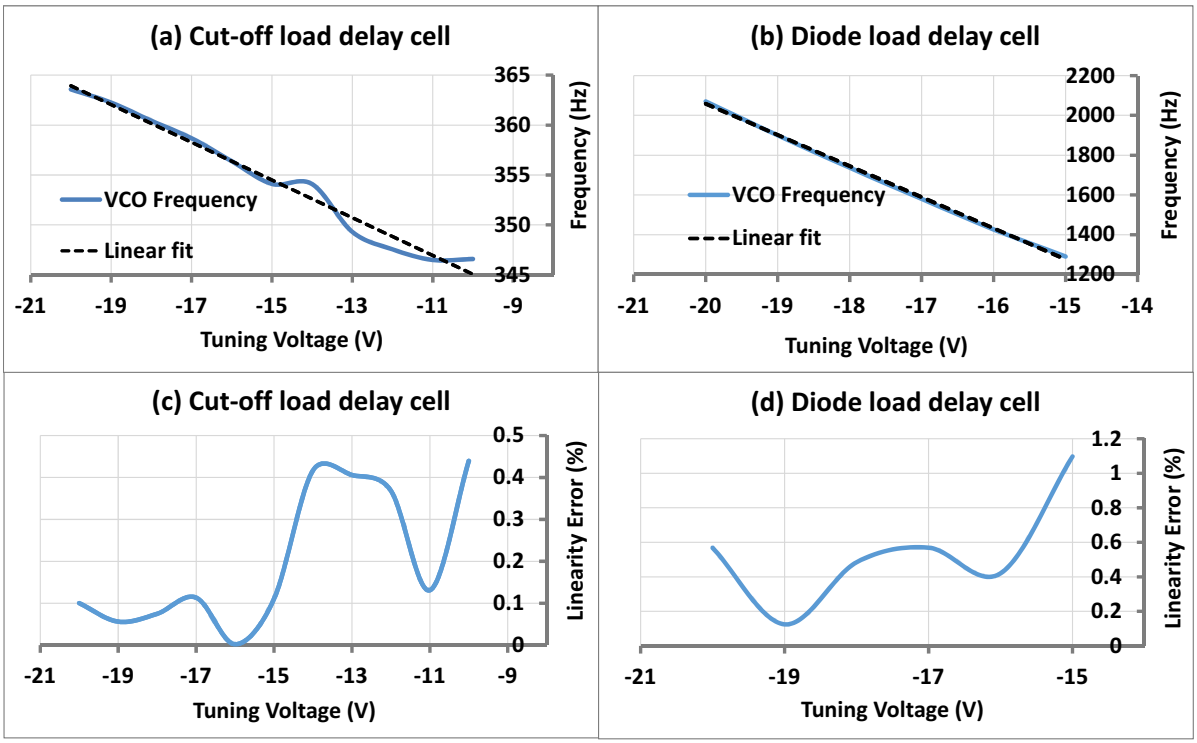


Figure 5.26: Measured (a, b) voltage versus frequency plot and (c, d) linearity error (in percentage) of the 11-stage VCO containing zero-V_{GS} (cut-off) and diode load delay cells respectively.

low around 1.5 Hz. The linearity error in percentage is shown in Fig. 5.26c, that is approximately within 0.5% for the zero-V_{GS} load delay cell. However, the frequency range of approximately 17 Hz is much lower since the drain-source current available to charge and discharge the load capacitance of a zero-V_{GS} load is much less. Therefore, the number of quantization levels which is directly proportional to the frequency range, as shown in Eqn. 5.17, is reduced which in turn reduces the resolution according to Eqn. 5.18. Thus, even though the cut-off load based delay stages exhibit a better linearity in their V-f characteristics, the resolution of the VCO using these delay cells is inferior compared to that using a diode-load based delay cell. We also measured a second VCO circuit based on zero-V_{GS} load delay cell but with different transistor dimensions. The transistor dimensions were chosen such that the increase in the tail current of a delay stage due to a change in the input tuning voltage is less than the marginal increase in the equivalent load capacitance at the output node of the corresponding stage. For this purpose, we used transistors M_1 and M_2 (see Fig. 5.24b) with a W/L ratio of 2000 μm/5 μm and 20000 μm/5 μm respectively. Their measured V-f plot as shown in Fig. 5.27 exhibits a decreasing slope that validates our arguement given in sec. 5.8.1.1.

The frequency versus tuning voltage curve and the linearity error percentage of the VCO using diode-load inverter delay cell is shown in Fig. 5.26b and Fig. 5.26d respectively. The linearity error is within 2%. The tuning voltage is swept from -10 V to -20 V. However, the voltage-controlled ring oscillator using diode load delay cells was observed to produce oscillations at the output only for tuning voltages below -15 V. The measured VCO circuits use 11 delay stages. The width of the transistors M_1 and M_2

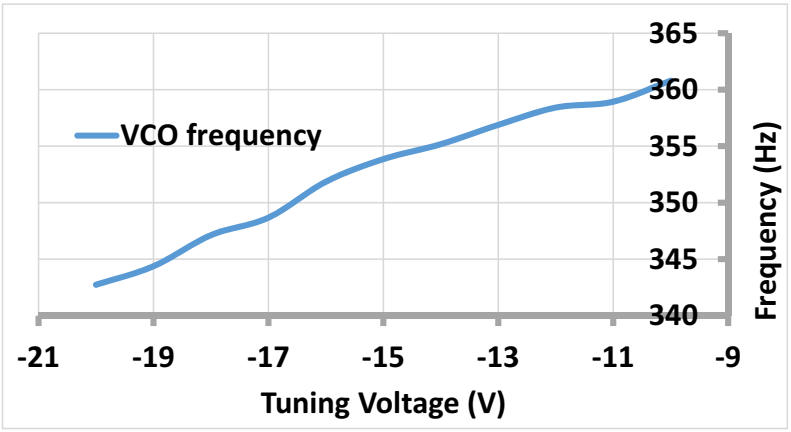


Figure 5.27: Measured output of a 11-stage VCO using zero-V_{GS} load delay cells showing a decreasing slope in their V-f characteristics. M_1 and M_2 have a W/L ratio of 2000 μm/5 μm and 20000 μm/5 μm respectively

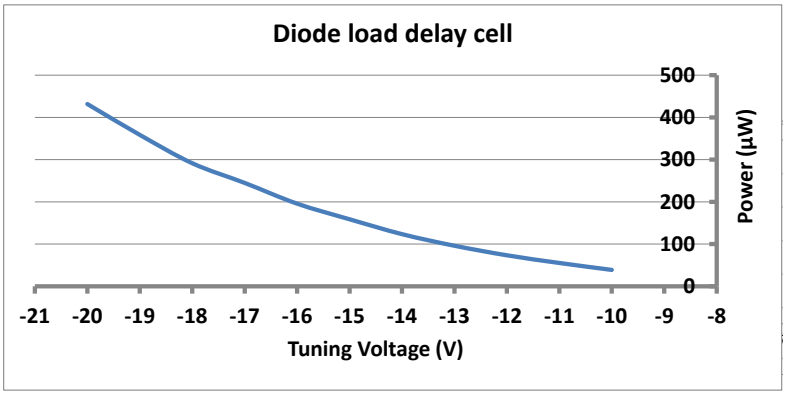


Figure 5.28: Measured power versus tuning voltage of the 11-stage VCO containing diode load delay cells.

of the diode load delay stage, as shown in Fig. 5.24a, is 10000 μm and 1250 μm respectively. The length of both the transistors is 5 μm. The measured resolution of the VCO, calculated according to Eqn. 5.17 & 5.18, was around 5.8 bits. The measured tuning sensitivity was observed to be around -170 Hz/V. The output frequency has a range of 783 Hz. The results clearly show that the VCO using diode-load based delay stage provide the best frequency range and tuning sensitivity. The maximum deviation of the V-f curve from the linear fit was 14 Hz. However, due to a large frequency range, the number of quantization levels and the resolution of the VCO is high. The power consumption of the diode-load delay stage based VCO is shown in Fig. 5.28.

5.8.2.1 Effect of Jitter and Phase Noise

Phase noise and jitter quantify the same phenomenon but in frequency and time domain respectively. Jitter is the time domain manifestation of the noise sources in oscillators that causes variation in the zero crossing times of the oscillation waveform. In the frequency domain, this appears as close-in sidebands around the fundamental frequency (f_0). For an ideal noiseless sinusoidal oscillator, this appears as an ideal pulse at the

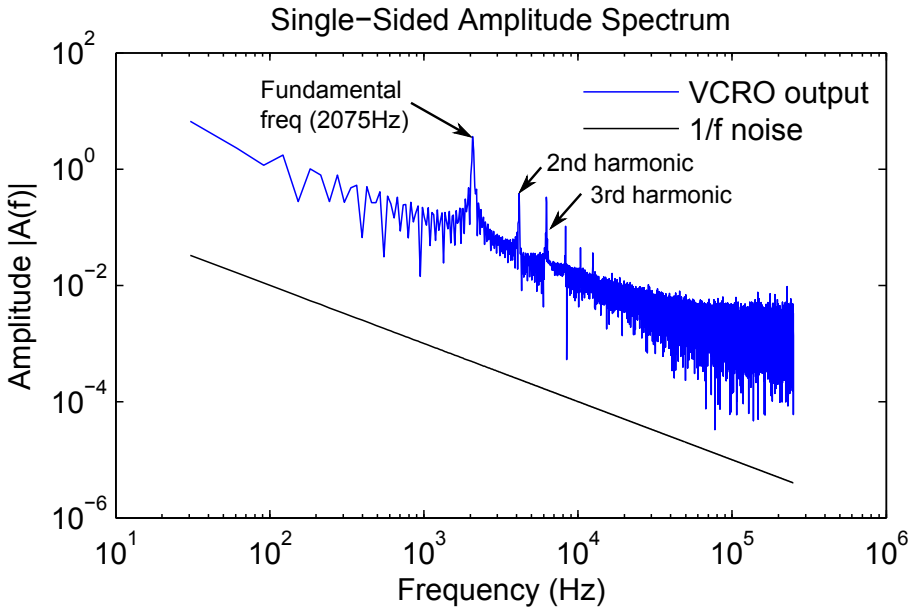


Figure 5.29: Measured amplitude spectrum of the diode load delay cell based VCO for a tuning voltage of -20V.

fundamental oscillation frequency (f_0). Phase noise is usually specified in dBc/Hz at a given offset frequency, where dBc is the level in dB relative to the fundamental. Due to the integrating nature of the VCO, the white noise is up-converted to $1/f^2$, and the device $1/f$ noise is up-converted to a $1/f^3$ noise region [HL98] in the noise-spectrum. The amplitude spectrum of the diode-load delay based VCO is shown in Fig. 5.29. We have used 16384 samples of the output sampled at 500 kHz to calculate the amplitude spectrum. The figure shows a very strong presence of 1/f noise in the VCO output which gets up-converted to $1/f^3$ noise. Thus to improve the resolution of the VCO-based ADC it is necessary to bring down the $1/f$ device noise. The impact of flicker noise is observed for the entire range of tuning voltage and the noise power was observed to be above the output power when the tuning voltages is less than -15 V.

5.8.2.2 Effect of Harmonics

The other major non-ideality affecting the performance of a VCO-based ADC is the harmonics. The harmonics occur at integer multiples of the fundamental frequency (f_0). The first harmonic occurs at a fundamental frequency of 2075 Hz for a tuning voltage of -20 V and is shown in Figure. 5.29 along with the higher harmonics. For a tuning voltage of -15 V, the lowest fundamental frequency of the VCO output occurs at 1290 Hz. The second harmonic for this occurs at 2580 Hz. For a given tuning voltage (V_{tune}), if the fundamental frequency exceeds this second harmonic frequency (2580 Hz) corresponding to the highest (or lowest in case of a positive voltage range) input tuning voltage, the VCO-based ADC cannot distinguish between the two input voltages. This introduces additional non-linearity in the V-f characteristics of the VCO and therefore reduces the resolution of the VCO-based ADC. The extrapolated measurement results from the diode-load delay cell based VCO show that for a tuning voltage (V_{tune}) of -24 V, the fundamental frequency exceeds the 2580 Hz limit. In the case of the zero-

V_{GS} load delay cell, it was observed that the VCO could theoretically operate up to an input tuning voltage of -200 V before the second harmonic of the higher tuning voltages interfere with the output. This is possible due to the low tuning sensitivity associated with the zero-V_{GS} load delay cell. The theoretical limit of the input tuning voltage range is given by

$$Tuning\ voltage\ range = \frac{2f_0(V_{tune,low})}{Tuning\ sensitivity} \tag{5.19}$$

where $f_0(V_{tune,low})$ corresponds to the fundamental frequency of the VCO output for a tuning voltage of $V_{tune,low}$. This equation shows a trade-off between the tuning sensitivity and the input tuning voltage range.

The power P1, P2, P3 and P4 corresponding to the 1st, 2nd, 3rd and 4th harmonics corresponding to the VCO using diode load delay cell are extracted from Fig. 5.29 and amounts to 13.18, 0.14, 0.11 and 0.01 respectively. The Total Harmonic Distortion (THD) of the VCO is observed to be approximately at 2 %. The comparison of the measurement and simulation results of the diode load delay cell based VCO is presented in Table.5.8. This table shows that the measurement results correspond with the simulation results.

	Resolution (bits)	Tuning sensitivity (Hz/V)	Frequency range (Hz)
Simulation	4.90	-56.4	702.6
Measurement	5.80	-170.7	780.8

Table 5.8: Comparison of measured and simulated performance metrics of the diode load delay cell based VCO

5.9 All-digital Flash Analog-to-Digital Converter

Flash ADCs have the highest operating speed, making them ideal for applications which require high bandwidth. In its entirety, a flash ADC is made up of three blocks: a linear voltage ladder, a comparator array, and an encoder. Figure. 5.30 shows the basic structure of a flash ADC. The linear reference voltages 1 to 2^N-1 can be designed using a resistor ladder. Input voltage is applied to each of the 2^N-1 comparators. These comparators compare the input voltage with the respective reference voltage, and generate a thermometer code. When the digital encoder is fed with this thermometer code, it generates the N bit digital value of the analog signal.

The conversion time for a flash ADC is one clock cycle that has two phase periods. During the first phase period, the analog input voltage is sampled and applied to the comparators. During the second phase period, the digital encoder determines the correct digital output code for the corresponding analog input. Since all the comparators work in parallel, the conversion time is independent of the resolution of ADC. On the contrary, the circuit complexity, die size, and the component matching requirements increase exponentially with the increase in resolution.

Of all the various ADC architectures, flash ADC provides a higher conversion speed. However, it requires $2^N - 1$ comparators for a N-bit resolution. Conventionally, com-

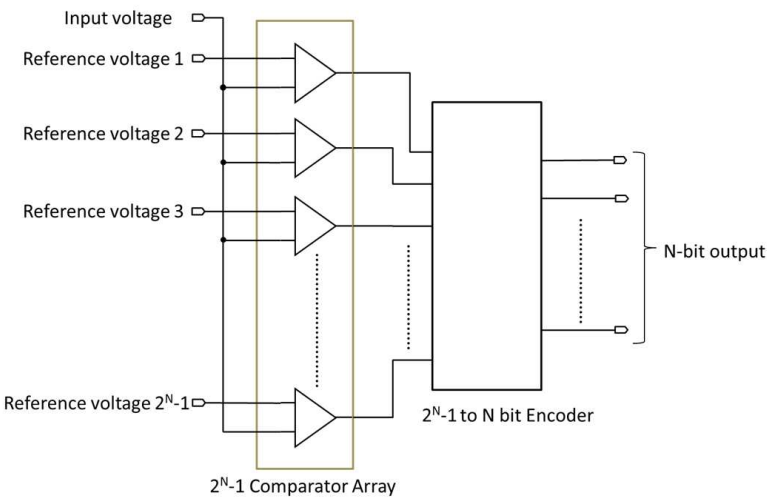


Figure 5.30: Basic structure of a flash ADC

parators are analog circuits and their linearity is limited by the poor matching typical of organic technologies. These non-linearities in turn severely deteriorate the INL and DNL errors of the ADC. We aim to address this deficiency by designing an all-digital flash ADC with INL and DNL errors below 0.5 LSB and whose linearity is not very much related to the matching of OTFTs.

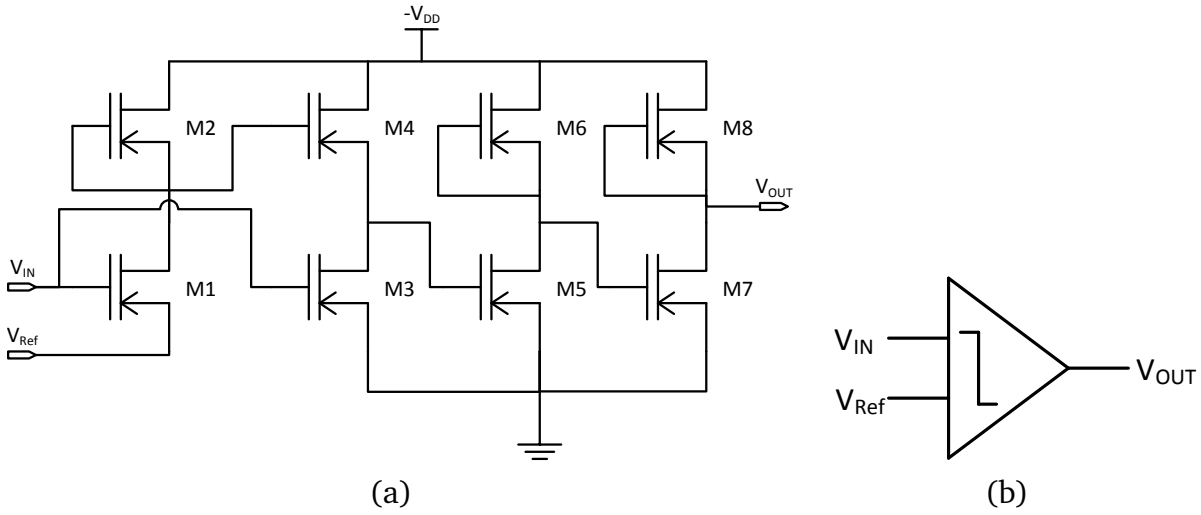


Figure 5.31: (a) Circuit schematic of the inverter based comparator and (b) its equivalent circuit symbol.

5.9.1 Design

In organic circuits, simplicity has an overbearing effect in minimizing the probability of hard faults. For this reason we used a flash ADC architecture which consists of a series of comparators and a priority encoder logic. Owing to their parallel structure, the flash ADCs offer the fastest way to convert an analog signal into a digital signal. The comparators act as a 1-bit ADC which compares the analog input voltage against

a given reference voltage. The reference voltage for each comparator exceeds the reference voltage of the comparator immediately below it by one Least Significant Bit (LSB). The output coming from the series of comparators is a thermometer code and the priority encoder logic converts this to a corresponding binary code. Since there are $2^N - 1$ comparators in a flash ADC, component matching requirements double with every bit increase in ADC resolution. Therefore, to overcome this problem we have used a mismatch-insensitive inverter based comparator. Additionally, the conversion speed of flash ADCs is limited only by the delay of comparators and the gate propagation delays. Since the comparators used are simple digital gates, their propagation delay is relatively less and this increases the conversion speed of the ADC as well.

An inverter is the simplest form of a digital comparator which switches its output when the input voltage approaches the inverter switching voltage. The switching voltage of a p-type inverter with a biased load can be expressed by Eqn. 5.20.

$$V_{SW} = \frac{V_{SS} + V_{td} + \sqrt{\frac{W_l L_d}{W_d L_l}}\,(V_b - V_{tl})}{1 + \sqrt{\frac{W_l L_d}{W_d L_l}}} \tag{5.20}$$

Here, V_{td}, W_d and L_d represent the threshold voltage, width and length of the driver transistor respectively. Similarly, V_{tl}, W_l and L_l denote the corresponding values for the load transistor. V_b represents the bias voltage applied to the load transistor. This switching voltage depends mainly on the threshold voltage, supply voltage and transistor sizing. By systematically varying one of these parameters, one can realize a series of inverters where the switching voltage of one inverter is one LSB apart from that of the previous inverter. Inverter based comparator using geometric scaling of transistor sizes and a subsequent flash ADC was designed in [TC04]. However, designing a comparator based on geometry scaling does not provide a promising solution for organic electronics, due to the large mismatch that is typical of any printing process. Hence, our design uses an inverter based comparator that varies its bias voltage (V_b) to change the switching voltage of the comparator.

The schematic of the inverter based comparator is illustrated in Figure 5.31(a). The comparator uses a non-differential mismatch-insensitive architecture. Transistors $M1$ and $M2$ form a level shifter with the rail-to-rail voltage given by $-V_{DD} - V_{ref}$. $M3$ and $M4$ are the load and driver transistor of the inverter respectively. The gate terminal of $M4$ is biased with the output of the level shifter. When V_{ref} changes, the output of the level shifter is shifted. This causes a proportional change in the current driving capability of the load transistor compared to that of the driver transistor. This is analogous to the effect achieved through geometric transistor sizing. The inverters formed by $M5$ to $M8$ act as buffers to bring the output voltage to rail-to-rail voltage levels.

5.9.2 Digital Encoder

The function of a digital encoder in a flash ADC is to convert the output of comparator array to a digital output. The code generated by comparator array in a flash ADC is a Digital Thermometer Code. This is called so because the code is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature

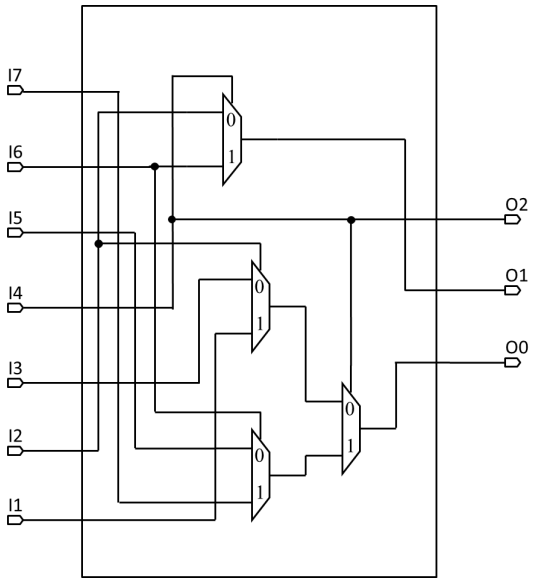


Figure 5.32: Implementation of digital encoder using multiplexers

and no mercury is present above that temperature. The inputs and outputs of digital encoder have been shown in Table. 5.9. This table considers the comparators in the comparator array to be non-inverting comparators.

Binary Input (Thermometer Code)								**Digital Output**		
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**	**O2**	**O1**	**O0**
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	1	1	0	1	0
0	0	0	0	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1

Table 5.9: Truth table for digital encoder

The following set of equations can be deduced after carefully analysing Tab. 5.9.

$$O2 = I4$$

$$O1 = \begin{cases} I2 & \text{if } I4 = 0 \\ I6 & \text{if } I4 = 1 \end{cases}$$

$$O0 = \begin{cases} \left.\begin{array}{ll} I1 & \text{if } I2 = 0 \\ I3 & \text{if } I2 = 1 \end{array}\right\} & \text{if } I4 = 0 \\ \left.\begin{array}{ll} I5 & \text{if } I6 = 0 \\ I7 & \text{if } I6 = 1 \end{array}\right\} & \text{if } I4 = 1 \end{cases}$$

These set of equations can be implemented by using a set of multiplexers. Figure. 5.32 shows the schematic for the implementation of priority encoder using multiplexers. The multiplexer gate uses a pass-transistor logic and is described in detail in Section 4.7. For the sake of maintaining proper rail-to-rail signal levels, two inverter buffers are used at the output of each multiplexer.

5.9.3 Experimental Results and Discussion

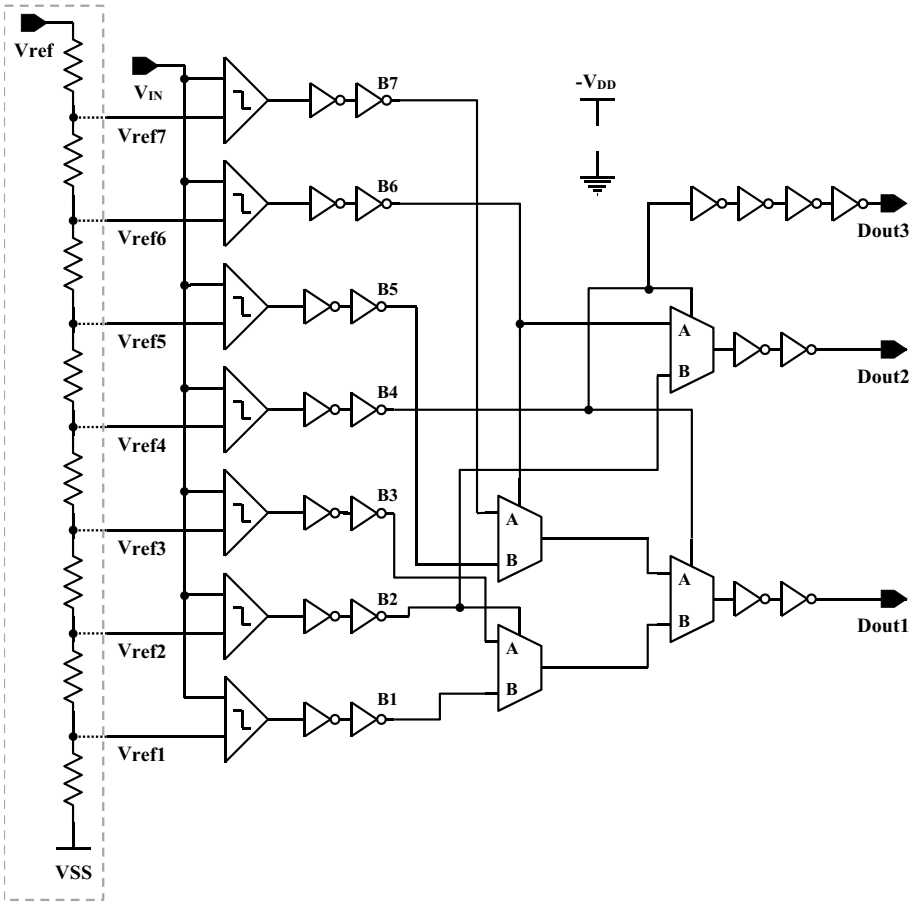
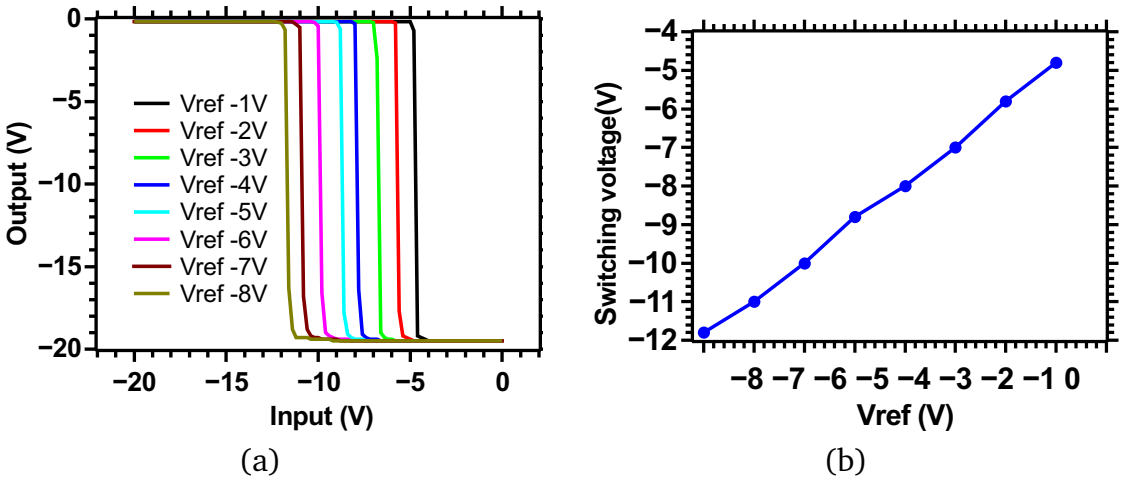


Figure 5.33: Detailed circuit schematic of the 3-bit flash ADC

A complete schematic of the 3-bit ADC is shown in Figure 5.33. The measured voltage transfer characteristics of the inverter based comparator is shown in Figure 5.34(a). The reference voltage is varied from -1 V to -8 V covering the full scale voltage range (V_{FSR}). Figure 5.34(b) depicts the linearity between the switching voltages extracted from Figure 5.34(a) and the applied reference voltages. The curve shows a good linearity and this will determine the non-linearity errors like INL and DNL error of the flash ADC. From the figure it can be observed that the comparator has an offset of approximately -5 V. This determines the minimum offset of the ADC. This high offset is mainly due to the large threshold voltage of the OTFT. The switching voltage determines the code transition point of the ADC output. For a 1 V change in reference voltage, the comparator yields a maximum difference of 1.2 V in the switching voltage. This makes the code



(a) (b)

Figure 5.34: Measured (a) voltage transfer curve and (b) the linearity of the switching voltage versus reference voltage of the inverter based comparator.

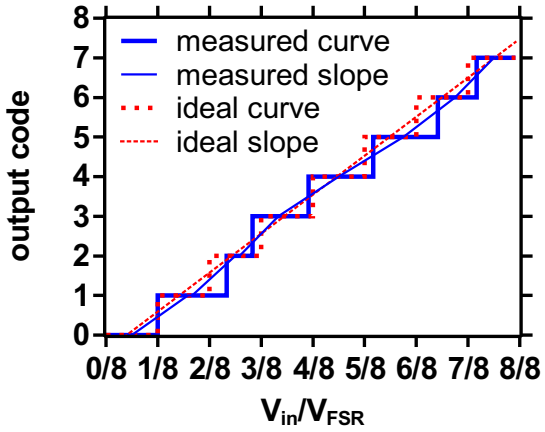


Figure 5.35: Measured transfer curve of the 3-bit flash ADC (after offset correction) for a full scale input voltage range

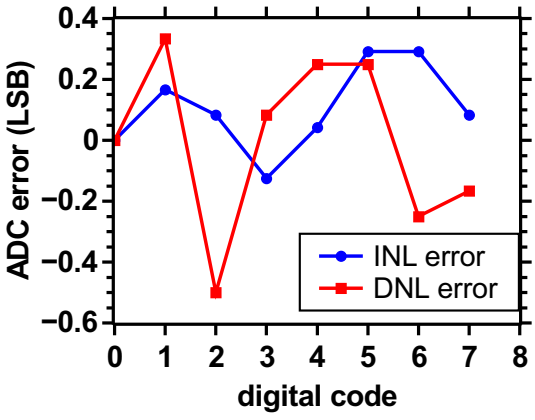


Figure 5.36: DNL and INL error of the ADC at 3-bit resolution.

width of the ADC to be 1.2 LSB instead of 1 LSB. Finally the full ADC functionality was tested using reference voltages generated from an external resistor ladder to simplify the experimental setup. Figure 5.35 illustrates the measured output code of the 3-bit

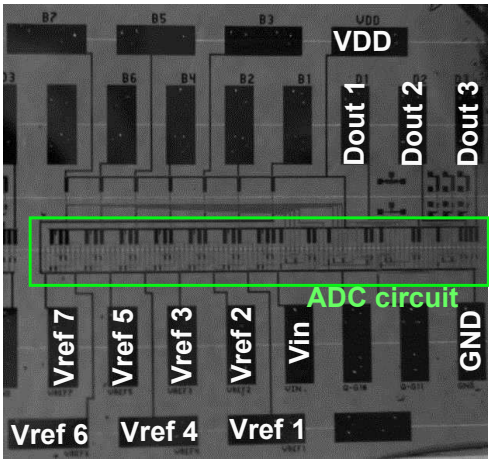


Figure 5.37: Chip photograph of plastic foil containing the organic flash ADC. The green enclosure depicts the active area of the circuit.

Table 5.10: Comparison with the state-of-the-art

	Architecture	Resolution (Bit)	DNL (LSB)	INL (LSB)	Area mm^2
[Mar+10]	$\Delta\Sigma$	4.1*	N.A.	N.A.	260
[Xio+10a]	SAR (C2C-DAC)	6	2.6**	3**	616
[Abd+13]	Counter (R2R-DAC)	4	0.24**	0.42**	2450
[Rai+13]	VCO-based	6	0.6	1	19.4
This work	flash	3	0.5	0.3	76

* ENOB evaluated from the SNR
** of the DAC before calibration

flash ADC after the offset and code width correction. The ADC output has an offset of -5.8 V and an average code width of 1.2 LSB. The measured values demonstrate that the comparator limits the linearity performance of the ADC. The difference between the ideal and the measured curves in Figure 5.35 is caused by the non-linearities present in the ADC. The critical non-linearity errors namely INL and DNL errors are shown in Figure 5.36. The measured INL and DNL error has a maximum of 0.3 LSB and 0.5 LSB respectively. The chip photograph of the presented circuit is shown in Figure 5.37. The comparison of this work with the state-of-th-art ADCs is shown in Table 5.10.

5.10 Conclusion

The following are the key summaries of this chapter.

- This chapter presents the design approaches required to design reliable circuits using OTFTs that are robust to threshold voltage variations without compromising on their performance. Two design approaches, one using positive-feedback and the other using cascaded zero-V_{GS} transistors as load structures, were proposed in

this chapter. Inverter circuits using the proposed load topologies were compared with the state-of-the-art inverter circuits namely diode and zero-V_{GS} inverters. The first approach employs a positive-feedback in the load structure and by varying the feedback gain one can trade-off gain for higher reliability and vice-versa. The second approach involving a cascaded zero-V_{GS} load is similar to the conventional zero-V_{GS} load but uses a compensation mechanism that reduces the sensitivity of the load to any variation in V_T. The measured results confirm that the cascaded zero-V_{GS} load inverter has a gain comparable to that of a zero-V_{GS} load inverter. The positive-feedback inverter has a moderate gain corresponding to the value of the feedback gain and the inverter gain can be increased further by making feedback gain close to zero.

- To understand the impact of variation on various load topologies, we examined the performance of various organic inverter circuits under the influence of process and bias-stress variations. With respect to the process variations, the simulated results show that the cascaded zero-V_{GS} load inverter offers good reliability (12% change in its gain) which is slightly less than that of the diode load inverter (5% change in its gain). For the analysis of the impact of bias-stress induced variations, both DC and AC stress voltages were applied. The experimental results show that both the proposed design topologies help in reducing the impact of V_T shift due to bias-stress effects. Thus, the proposed load topologies advance the state-of-the-art to realize robust digital and analog circuits using OTFTs without compromising much on their performance.

- The performance of the voltage-controlled oscillator circuits with respect to their suitability for the design of a VCO-based ADC circuit was analysed. For this analysis, four different tunable delay cells were used. The linearity of the V-f characteristics of the VCO determines the maximum limit of the VCO-based ADC's resolution and an equation relating the VCO's linearity with the ADC's resolution was derived. Based on this equation, the resolution of the ADC using different tunable delay cells were estimated and it has been found that the diode load based delay cell provides the highest resolution. Two VCO circuits, one using zero-V_{GS} load and the other with a diode load delay cell were fabricated and measured. The measurement results match with the results obtained from simulation. The diode-load delay cell based VCO provides a maximum resolution of 5.8 bits with a tuning sensitivity of -170 Hz/V. The effect of jitter and harmonics on the performance of ADC was also addressed and a relation between the input tuning range and the tuning sensitivity was established.

- In this chapter, a fully digital flash ADC was designed, fabricated and measured using organic technology on a plastic foil. The fabricated ADC has a good linearity. Even without calibration, the ADC has a DNL error of 0.5 LSB and an INL error of 0.3 LSB at 3-bit resolution. The area is 76 mm^2, which is significantly less compared to the previous work [Mar+10] with identical feature size (See Table. 5.10). Moreover, since we use a digital inverter based comparator, the ADC can be extended to achieve higher resolutions without any additional non-linearities.

6 System Design: Organic Smart Label System

Contents

In this chapter, an organic smart label electronic system using p-type organic thin film transistor (OTFT) for temperature sensing applications has been demonstrated. The electronic label consists of an organic temperature sensor, logic and interface circuits. It detects whether the critical temperature threshold value has been exceeded or not and records the data digitally in a write-once-read-many (WORM) form that can be transmitted to a reader through wireless communication. A comparator is used to interface the sensor to the logic part. The logic circuit block processes and bundles the sensor information along with the necessary additional protocol information that is required for a successful wireless transmission. We have demonstrated the operation of the reported organic smart label system using a silicon based modulator/rectifier circuit for Radio

Frequency (RF) communication. The organic logic circuit was built using standard cell design approach with approximately 180 p-type OTFTs.

6.1 Motivation

According to the UN Food and Agriculture Organization (FAO), it is estimated that one third of the food produced globally for human consumption is wasted, which amounts to 1.3 billion tons of food annually. This is a significant number given the fact that nearly 870 million people in the world do not get proper food. The temperature, being a key factor affecting microbial growth, is the most important factor impacting food safety and quality [Raa11]. Therefore, there is a need to employ temperature monitoring systems throughout the logistics industry to help achieve quality management standards and compliance with specified regulations and procedures for a range of goods. They can help identify if and when product damage occurred. Most importantly the data collected by these monitoring systems can help us to identify the faulty areas in the logistics so that immediate corrective measures can be taken to overcome the faults.

6.2 Introduction to Temperature Tracking Systems

Traditionally, there are many types of temperature monitoring systems used in the logistics. The commonly used types are the paper based temperature indicator labels [Pav13; Ros77; TL89], temperature data loggers [Kuc+05; Rog97; Woo00] and wireless technology based temperature tracking system [Fur06; Cro+04]. The paper-based temperature indicator label consists of one or more small spots of heat-sensitive materials sealed under transparent, heat-resistant windows. A variant of temperature indicator label namely time-temperature indicator (TTI) label shows the accumulated time-temperature history of a product. The temperature indicator labels are of two types namely reversible and non-reversible temperature labels. As the name implies, reversible temperature labels can change the temperature back and forth as long as the temperature does not exceed the maximum operating value. This implies that they can be re-used. On the contrary, non-reversible temperature labels are for one time use and they indicate that the specified temperature threshold has been reached. The main advantage with the non-reversible labels are that they store the temperature information inherently and are useful in a situation where a constant access to a product containing the label is not available. On the other-hand, since the reversible labels do not store the temperature information inherently, they require a dedicated storage mechanism. The information from the temperature labels are not directly machine readable. They require an optical inspection system which scans every product containing a label and converts the optical information into a corresponding digital information. This causes a significant delay in processing the goods containing these labels at a warehouse or in a distribution centre.

With the advent of the digital era, companies wanted a faster way to record the thermal readings. This led to the development of electronic data loggers [Kuc+05; Rog97; Woo00]. These systems typically use a microcontroller with one or more thermistors. The microcontroller collects and stores the digitized value of the temperature measurements on a data storage unit. They use a battery to operate the on-board electronic

circuits. All these components make the system bulky and costly. Furthermore, these temperature data loggers require a physical connection to transfer the data stored in the memory. This leads to a delay in processing the goods at the logistics centre. As far as the electronic data loggers are concerned, they are easily machine readable but they still have a processing delay due to the requirement of a physical connection for the data transfer.

During the last decade substantial technological progress has been achieved in the field of wireless communication technology. Crowley et al. developed a wireless temperature logger system [Cro+04]. The system contains an electronic data logger with an integrated RF transmitter. Not only did the use of wireless technology allowed a faster data transfer, it also allowed various data loggers to transfer data simultaneously. But, the usability of the system was limited by the run-time of the battery. The wireless data loggers were refined further by using an active RFID tag. Such an RFID-based temperature monitoring system was described in [Fur06]. The active RFID tag derives its power from the RF waves that are transmitted by the reader. Hence, they do not require a battery that saves the cost and increases the life time of the system.

6.3 Organic Smart Label System

One of the main proponents of research in organic RFID tag is the requirement for low-cost item-level tagging solutions. Baude et al. presented OTFT based RFID circuitry that uses external rectifier/modulator block[Bau+03]. Rotzoll et al. reported an organic transistor based rectifier operating at 13.56 MHz[Rot+06]. Further research resulted in building a complete organic RFID tag [Can+07; Myn+08; Myn+09] including the organic front-end circuitry for RF transmission.

Integration of functionality is one of the most compelling benefits of organic electronics that has the potential to create high volume markets. Therefore, it is advantageous to move further from the circuits in [Can+07; Myn+08; Myn+09] and to add sensory intelligence to these RFID tags to form smart electronic labels. Such an electronic label can be used to deliver item-level tracking of essential data for goods such as pharmaceuticals, perishable foods and hazardous chemicals. In this chapter, we have focused on the integration of functionality of various organic devices and circuits namely sensor, digital logic and interface circuit and these circuit blocks were shown to work together as a system that can sense, process and store the data for future retrieval. This smart label can be complemented with previously reported organic rectifier/modulator blocks [Rot+06; Can+07; Myn+08; Myn+09; Myn+12] to add RF wireless communication capability.

6.4 System Description

The organic electronic label consists of an organic temperature sensor, memory, interface and logic circuits. The interface circuit comprises of a simple inverter-based comparator and this along with the organic logic circuit performs the evaluation of temperature sensor. The organic temperature sensor used in this work is a Write-Once-Read-Many (WORM) type of sensor which means that the sensor once activated by

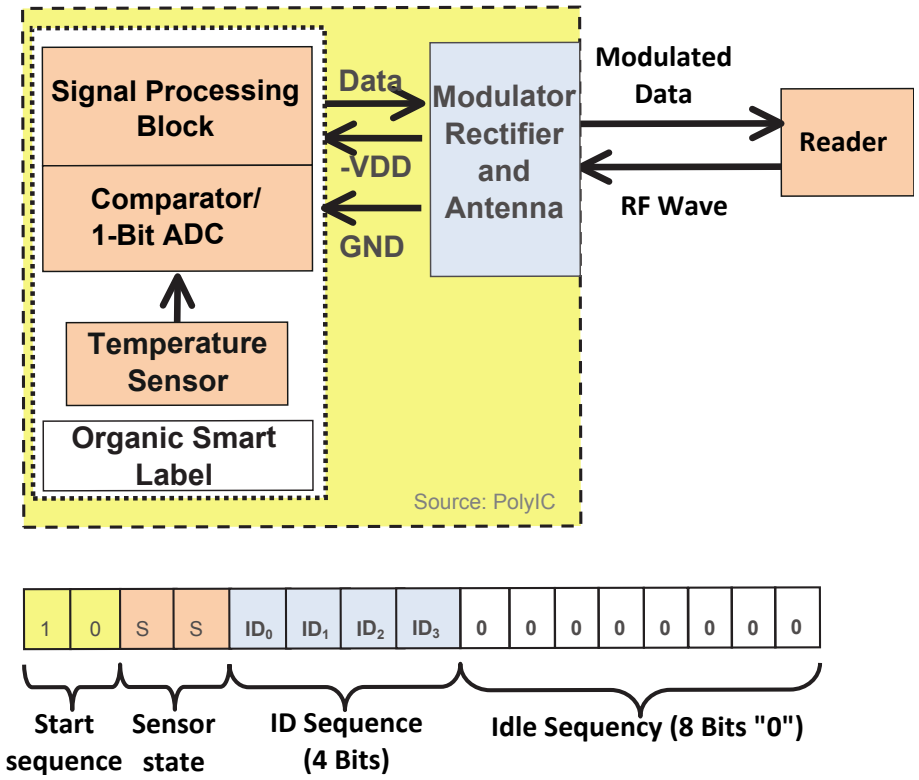


Figure 6.1: Block diagram (top) of the smart label system and description of the protocol bits (bottom).

exposing to a temperature above the critical threshold, remains in the activated state forever. The re-usable standard-cell library for digital gates, which is described in Chapter 4, has been used to design the organic logic circuits. Block diagram of a smart label system along with the RF communication circuitry is shown in Figure 6.1. The smart label system generally consists of a sensor, sensor interface circuit, signal processing block and the RF front-end for wireless communication. In this work, we focus on temperature sensing application and therefore the sensor used in our system is an organic temperature sensor. A simple inverter-based comparator is used to interface the sensor to the digital signal processing block. The data from the digital processing block is transmitted wireless to the reader using a silicon based RF front-end circuit that also provides the supply voltage to the organic circuitry. In this work, a silicon based RF rectifier/modulator circuit is used for the purpose of simplicity. The rectifier provides a -20 V DC supply to the organic sensor chip. The bottom of Figure 6.1 describes the transmission protocol used. It consists of a 2 start bits, 2 sensor bits, 4 ID bits and 8 idle bits. The start signal is predefined and are defined as a HIGH followed by a LOW. The sensor bits come from the temperature sensor and is represented twice for redundancy purpose. The ID bits is used for the identification of the smart label. The idle signal is represented as a bit stream containing eight LOW signals. The start and idle bits are hard-coded and are derived from two standard cells that generate HIGH and LOW signal levels. The ID bits are programmed mechanically. The defined protocol bit stream is generated by the signal processing or code generator circuit block.

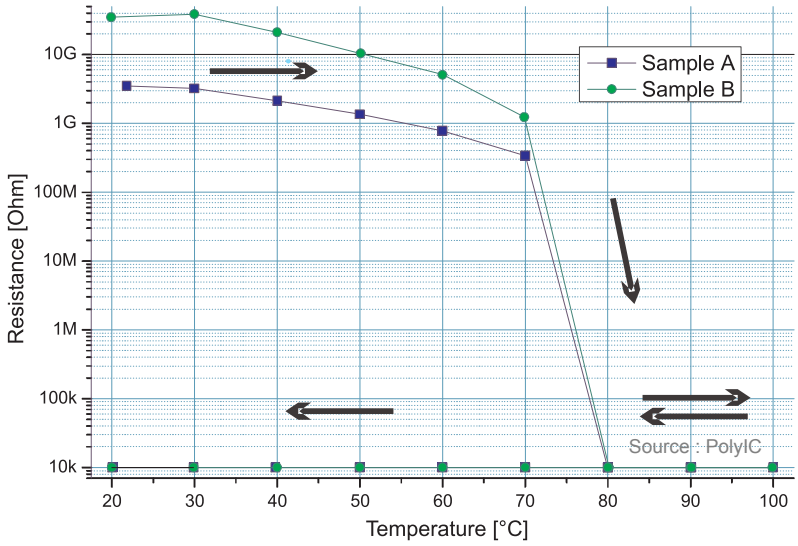


Figure 6.2: Measured resistance vs. temperature characteristics of the organic irreversible temperature sensor from samples A & B respectively. The temperature was first swept in a forward direction from 20 °C to 100 °C and then backwards from 100 °C to 20 °C.

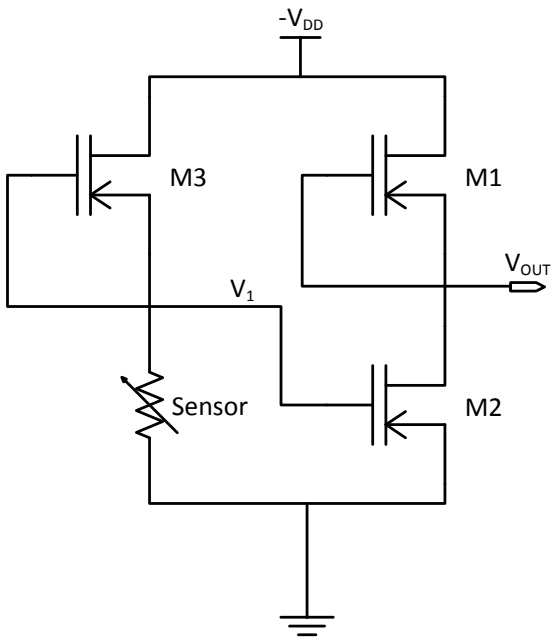
6.4.1 Sensor

The sensor is designed to be irreversible for a specific application scenario in logistics. The sensor is meant for temperature-tracking of goods during the logistic transportation where the goods have to be maintained always below the critical threshold temperature. This requires the goods to be continuously monitored throughout their transportation process. The goal is to have a low-cost and time effective solution to inspect every item and to separate the items that were exposed to temperatures above the threshold value. This is conventionally done using colour spots or temperature logger systems as mentioned in Section 6.2. In the case of a colour spot, a special thermally active material changes colour when the temperature exceeds the threshold. Though this is a cheap option, it is not easily machine readable. Every item has to be optically read and it is time consuming. The other method i.e. the temperature logger system uses a reversible temperature sensor. In this case, the sensor needs to be read and processed continuously throughout the transportation and that requires a battery for every sensor circuit which adds to the overall cost. An alternate option is to store the information on a separate non-volatile memory which would then require a constant power supply all time as the temperature has to be actively monitored. To overcome the above issues, we have uses an irreversible temperature sensor. When the temperature exceeds the threshold value, the sensor stores the temperature information in itself by changing its state permanently. Hence, this system does not need a battery to continuously track the temperature. Moreover, reading is easier and faster compared to colour spots due to the RF capability. Also the ID bits enable item-level identification that is difficult with colour spots. The temperature sensor is built using organic material and on exposure to temperatures above 80 °C, the electrical resistance of the sensor changes irreversibly from few GΩ to few kΩ. After reaching the critical threshold temperature, the resistance

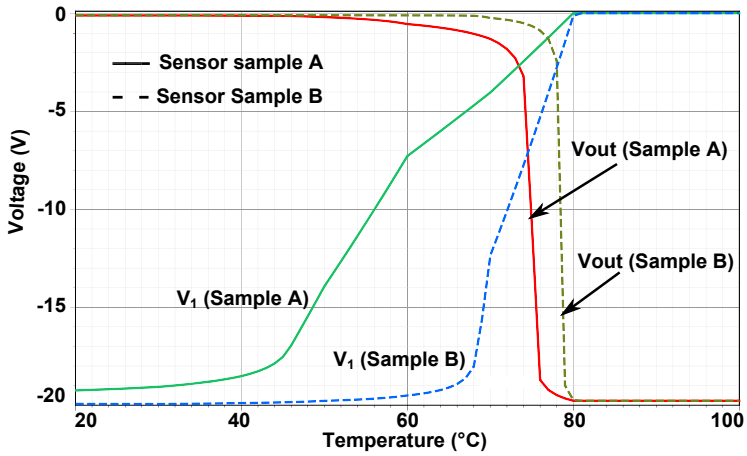
changes marginally only by few ohms for every 10 °C increase. The resistance vs. temperature characteristics of two different samples of the organic irreversible temperature sensor is depicted in Figure 6.2. The graph shows both the forward and reverse sweep of the temperature. It can be clearly observed that the resistance remains approximately at 10 kΩ for the reverse sweep of temperature. The sensor has an accuracy of +/- 10 °C. To protect the interface and the signal processing circuit from the influence of a high temperature applied on the sensor, they are fabricated on a separate substrate from that containing the temperature sensor. The used sensors were designed and fabricated by PolyIC GmbH.

6.4.2 Interface Circuit

Since it is only required to detect the temperature threshold crossing, a 1-bit ADC would suffice our requirement. A 1-bit ADC is nothing but a comparator and therefore a comparator is used as an interface circuit to realize the smart label. As discussed in Section 5.7, to overcome the typical issues associated with the process variations and bias-stress effects, the analog functionality needs to be realised using circuits having a highly digital composition. Therefore, to realize the comparator required for the smart label system, we have used an inverter based comparator which is completely digital. The schematic of the comparator is shown in Figure 6.3(a). It consists of two stages. The first stage is a voltage divider formed by transistor M_3 and the temperature sensor. The second stage is an inverter whose input is connected to the output (V_1) of the voltage divider. The inverter switches its output voltage (V_{OUT}) when its input voltage crosses the switching voltage of the inverter. When the temperature is well below the threshold, the resistance offered by the temperature sensor is large in the range of few giga ohms. This causes V_1 to be pulled down to -V_{DD} and this produces a high (GND) at V_{OUT} of the inverter stage. As temperature increases and approaches the temperature threshold value, the resistance offered by the temperature sensor decreases. This results in V_1 being pulled up to ground (GND). When V_1 equals the switching voltage of the inverter, the inverter output (V_{OUT}) switches from high to low. Thus, depending on the temperature value, output of the voltage divider varies and when it approaches the switching voltage of the inverter, the inverter output switches. The dimensions of transistor M_1, M_2 and M_3 are chosen in such a way that they make V_1 equal to the switching voltage of the inverter when the temperature reaches the threshold value. The widths of M_1, M_2 and M_3 are 7000 μm, 800 μm and 800 μm respectively. All the OTFTs have a length L=5 μm. The inverter uses a zero-V_{GS} load configuration. It is observed that the fabricated inverters have a switching voltage between -2.5 V and -4 V. This is taken into consideration to determine the W/L ratio of the transistors. Thus the voltage divider output V_1 changes from low to high when the sensor is irreversibly activated to its low resistive state when the temperature exceeds 80 °C. As seen in Figure 6.3(b), when the temperature crosses the threshold limit (80 °C), the inverter switches its output from high to low thus behaving like a 1 bit ADC. Since we have employed an irreversible temperature sensor, voltage V_1 will remain high even after bringing back the temperature to a normal value (i.e. <80 °C).



(a)



(b)

Figure 6.3: (a) Schematic of an inverter based comparator circuit. (b) Output of the comparator (V_{OUT}) and voltage divider part (V_1) when the temperature is swept from 20 °C to 100 °C (for two sensor samples).

6.4.3 Signal Processing Circuit

The schematic of the code generator circuit is shown in Figure 6.4. The signal processing block consists of memory and logic circuit that is built using standard cell design approach. The standard cell library of organic digital gates contains Inverter, NAND, NOR, XOR, MUX and DFF and are described in detail in Chapter 4. The schematic overview of the logic circuit is shown in Figure 6.4. It consists of a clock generator, a 4 bit counter, a set of multiplexers and an output buffer. The clock signal is generated using a 17 stage ring oscillator that produces a clock signal of 16 V_{pp} at 30 Hz signal

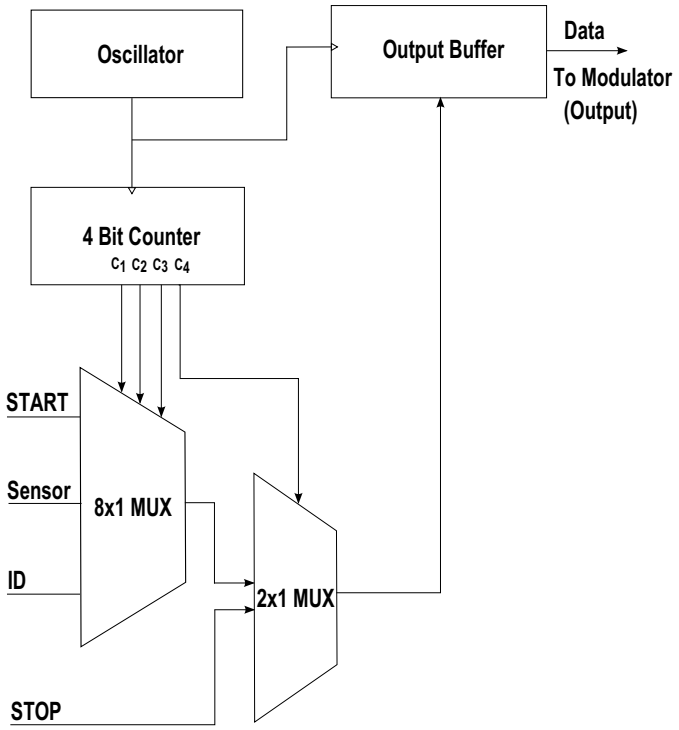


Figure 6.4: Block diagram of the signal processing (code generator) circuit.

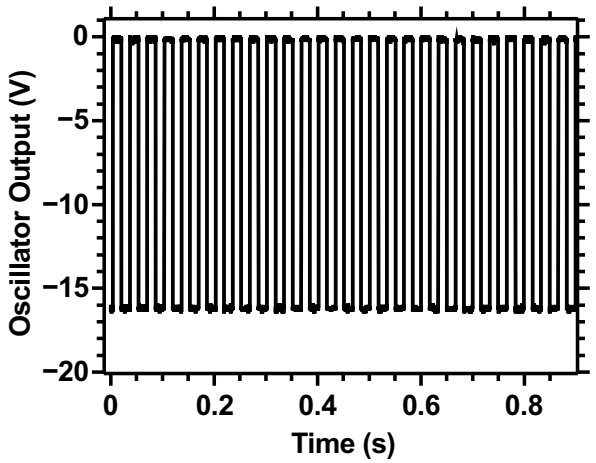


Figure 6.5: Output of the oscillator circuit.

frequency. The output of the oscillator is shown in Figure 6.5. The set of multiplexers along with the counter and the output buffer mimic the function of a shift-register. The truth table of the code generator circuit is given in Table 6.1. The code generator circuit uses a simple two bit write-once-read-many (WORM) memory that contains a high (GDS_HProg) and a low (GDS_LProg) signal. The start, idle and ID bits are derived from these two basic signal levels according to the defined protocol. Thus the start and idle bits are hard-coded, while the ID bits can be programmed mechanically externally.

Table 6.1: Relation between the output of the 4-bit counter and output of the signal processing block.

C_1	C_2	C_3	C_4	Output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	S
0	0	1	1	S
0	1	0	0	ID<1>
0	1	0	1	ID<2>
0	1	1	0	ID<3>
0	1	1	1	ID<4>
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

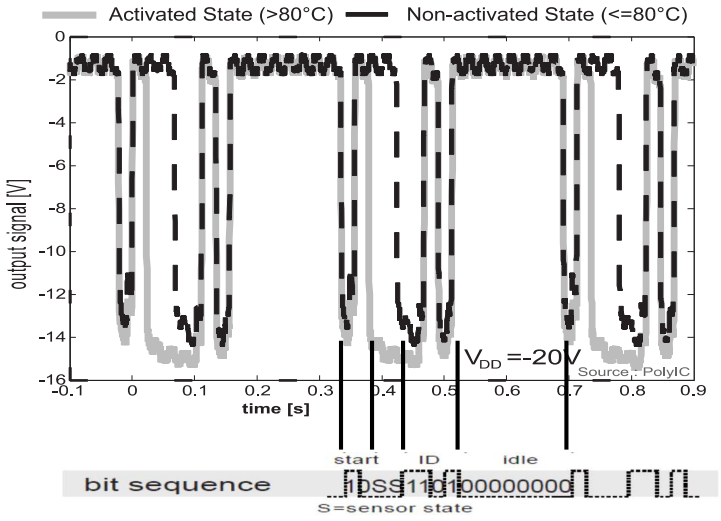


Figure 6.6: Measured internal signal of the sensor tag, tapped at the output of the organic sensor chip. The black and gray curves represent the measurement results when temperature on the sensor is below and above 80 °C respectively.

6.5 Results and Discussion

The measurement results of the individual standard cells are given in Chapter 4. Figure 6.7 shows the measured signal from the sensor tag, tapped at the output of the organic smart label. The bit stream from the electronic label for an activated (>=80 °C) sensor state is overlaid on that of a non-activated (<80 °C) sensor state. It shows the

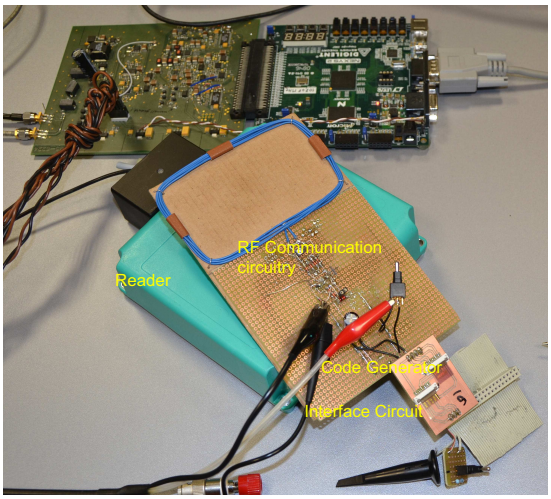
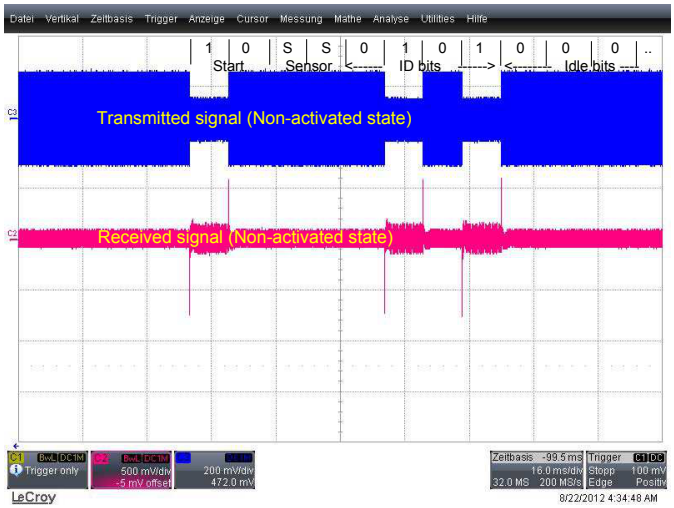


Figure 6.7: Photograph of the test set-up containing the organic smart label sensor chip with the RF communication circuitry and the reader (Source: Pepperl & Fuchs GmbH).

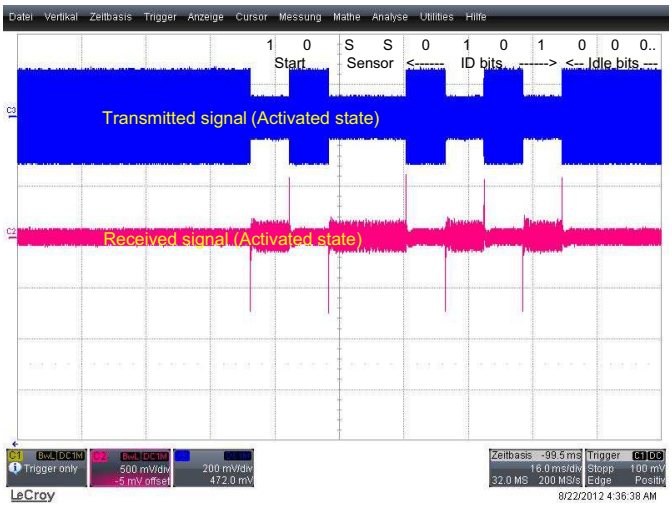
change in two identical sensor bits S from high to low when the sensor is activated. The sensor tag is operated by a 13.56 MHz carrier signal that is transmitted by the reader via inductive coupling to the silicon based RF front-end circuit. The rectified DC voltage is in the range of -20 to -25 V and supplies the organic smart label system. Photograph of the test set-up containing the reader and organic smart label with silicon based RF circuitry is shown in Figure 6.7. Figure 6.8(a) and 6.8(b) shows the transmitted signal from the smart label system and the received signal at the reader side for non-activated (<80 °C) and activated (>=80 °C) states respectively. The photographs of the organic chip containing the logic block and the interface circuit are shown in Figure 6.9(a) and 6.9(b) respectively.

6.6 Conclusion

To summarize, an organic smart label system combining a temperature sensor, sensor interface and code generator circuit have been developed. This way we have successfully demonstrated the integration of various individual organic circuits and devices having different functionalities to realize a relatively complex organic system. The organic logic circuit block was designed using standard-cell approach and thus, we have established a working design process using standard cells that enable structured and re-usable organic circuit design. We have tested the smart label's operation in a test system and were successfully able to transmit the sensor information to the reader using a silicon based RF communication circuitry. The presented results show a successful transmission of sensor states in the defined bit stream. In total, the organic part was constructed using approximately 180 OTFTs and operated at -20 V. For a prospective outlook, additional circuitry for the wireless communication capability needs to be realized using organic rectifiers and integrated with this electronic label to achieve its maximum commercial potential.

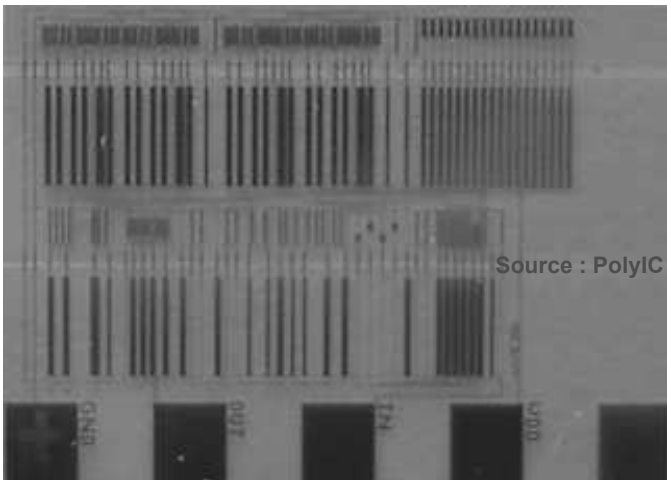


(a)

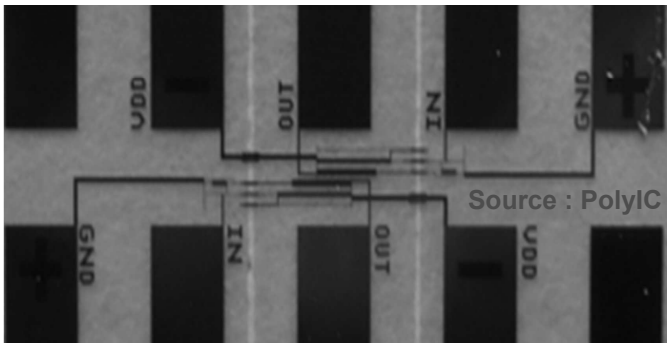


(b)

Figure 6.8: The transmitted signal of the RFID communication circuitry and the received signal at the reader side for (a) non-activated and (b) activated state (Source: Pepperl & Fuchs GmbH).



(a)



(b)

Figure 6.9: Chip photographs of (a) organic logic circuit and (b) organic interface circuit.

7 Overview and Conclusions

Contents

This chapter summarizes the work presented in this dissertation and discusses possible future extensions in the addressed directions.

7.1 Summary

Organic electronics has evoked keen interest in the research community due to its capability as a viable alternative to silicon electronics, mainly for low-cost, large-area and flexible application scenarios. The key advantage lies in the low cost fabrication using roll-to-roll printing techniques. The recent advances in the mobility of OTFT is very encouraging and the mobility has even surpassed the values of amorphous silicon TFTs. However, for successful commercialization of organic electronics the reproducibility of OTFT is much more important than just having higher mobility. The low-cost printing processes do not use a clean room facility and due to the material and printing properties, the printed layers are non-homogeneous. This causes differences in the electrical characteristics of the printed transistors even when they have identical dimensions. Furthermore, OTFTs suffer from bias-stress effects, that results in the dynamic shift of their threshold voltage (V_T) during the circuit operation. Unlike the process variations, which are static in nature occurring only once at the time of fabrication and does not change after that, the bias-stress induced variations are dynamically affecting the V_T of an OTFT during the operation of the circuit. Therefore, the investigation of the influence of process variations and bias-stress effects on OTFTs is very much essential for the exploitation of organic electronics. On a whole, the OTFTs generally suffer from relatively large process variations and bias-stress induced degradation, that results in poor long-term reliability in addition to the performance degradation. Furthermore, organic complementary circuits are still a distant reality due to the inferior performance of n-type OTFTs in comparison to p-type transistors. Therefore, it is highly desirable

to develop circuit design strategies which can 1) tolerate the relatively large parameter variation associated with the OTFTs and 2) advance the performance envelope of mono-type PMOS only organic circuits.

In the recent years, there has been a greater interest among the research community in realizing smart label systems that contain sensors integrated with the RFID tags on cheap and flexible substrates. Commercial applications of such intelligent RFID tags include item-level tagging solutions for cost-sensitive supply chain processes. For instance, these smart tags provide a cheap and efficient means to monitor the vital parameters of the the food and pharmaceuticals throughout their logistics chain. Such smart tags are also expected to open-up cost sensitive sectors for the Internet-of-Things (IoT) by providing a low-cost holistic sensory monitoring. Individual circuit components like rectifier, sensor and organic code generator blocks have been reported earlier, and as a next logical step it is necessary to integrate all the individual circuit blocks/components to form a smart label system.

The parameter variations in an OTFT are addressed in Chapter 3. In this, both the process and bias-stress induced variations are investigated. In the case of process variations, both global and local variations are addressed. Similarly, the temporal variability due to the bias-stress effects are characterized and measured. The variation of V_T is tested under high gate-field and high drain-field stressing experiments. The influence of bias-stress effects on V_T, mobility and subthreshold swing slope of OTFTs are also analysed and an appropriate model is developed.

On the circuit side, two new load circuits have been proposed to design reliable organic circuits like inverters, amplifiers and differential amplifiers. This forms a basic building block for any elemental circuit that uses active load in its schematic composition. The performance of the proposed load topologies in comparison to the prior-art load circuits were analysed using inverting amplifiers. As an example, differential amplifier circuits using the proposed load topologies were designed and measured. The differential amplifier circuit forms the basic elemental analog circuit component that is necessary to realise more complex analog circuits like operational amplifiers, comparators etc. Also, to have robust organic ADC circuits, two digital based ADC architectures were designed and evaluated.

Finally, as a design example for a smart label system, an RFID tag containing an organic temperature sensor, interface circuit and the code generator circuit was demonstrated. To realize the digital code generator circuit, a standard cell library containing various organic digital gates was developed. The measurement results demonstrate the intended operation of the organic smart label system and this is a promising step towards successful commercialisation of organic sensor tags.

Some of the key objectives of this work are given below:

- Investigation and understanding of the statistical distribution of parameters due to the process and material induced variations in an OTFT. These include both systematic and random variations. A generalized simulation model for statistical analysis was developed that includes components of both global and local variations.

- Investigation and understanding of the bias-stress induced threshold voltage (V_T) variation in an OTFT. The charge trapping mechanism is explained and a measure-

ment scheme to characterise the bias-stress effects is devised. The influence of the bias-stress effects on V_T, mobility and subthreshold-swing slope of an OTFT are analysed. The impact of both high gate-field and high drain-field stressing on the electrical characteristics of the OTFT is analysed.

- Designed and evaluated a standard cell library of basic digital gates using OTFTs. The standard cell library helps in re-usability of the design and is very much essential with the organic technology which is frequently changing as the technology is continuously evolving.

- Two design approaches required to design reliable circuits using OTFTs that are robust to threshold voltage variations without compromising on their performance are presented. The first approach uses positive-feedback and the other uses cascoded zero-V_{GS} transistors as load structures. Inverter circuits using the proposed load topologies were compared with the state-of-the-art inverter circuits namely diode and zero-V_{GS} inverters. In the first approach, that employs a positive-feedback in the load structure, one can trade-off inverter gain for higher reliability and vice-versa by varying the feedback gain. The second approach involving cascoded zero-V_{GS} load is similar to the conventional zero-V_{GS} load but uses a compensation mechanism that reduces the sensitivity of the load to any variation in V_T without compromising the gain of the inverter.

- The impact of V_T variation on various load topologies have been analysed by comparing the performance of various organic inverter circuits under the influence of process and bias-stress induced V_T variations. For the analysis of the impact of bias-stress induced variations, both DC and AC stress voltages have been considered.

- The performance of the voltage-controlled oscillator circuits with respect to their suitability for the design of a VCO-based ADC circuit has been analysed. For this analysis, four different tunable delay cells have been used. The linearity of the V-f characteristics of the VCO determines the maximum limit of the VCO-based ADC's resolution and an equation relating the linearity of VCO's V-f curve with the ADC's resolution was derived. Based on this equation, the resolution of the ADC using different tunable delay cells was estimated. Furthermore, the effect of jitter and harmonics on the performance of the ADC was also addressed and a relation between its input tuning range and its tuning sensitivity was established.

- A fully digital Flash ADC was designed, fabricated and measured. The fabricated ADC was observed to have a good linearity. Even without calibration, the ADC has a DNL error of 0.5 LSB and an INL error of 0.3 LSB at 3-bit resolution. The active area of the ADC was 76 mm^2, which is significantly less compared to the previous work [Mar+10] with identical feature size. Moreover, since we use a digital inverter based comparator, the ADC can be extended to achieve higher resolutions without any additional non-linearities.

- Successfully demonstrated the integration of various individual organic circuits and devices to realize a relatively complex organic smart label system for temper-

ature sensing application. The smart label system's operation was tested in a test system and was able to successfully transmit the sensor information to the reader.

7.2 Outlook

It is the author's hope that the present work may have contributed at least in a minimal way to realise reliable circuits using OTFTs. The organic electronics community is very much pre-occupied in improving the mobility of OTFT and reliability is less addressed. Through this work, the author would like to highlight that reliability is very much important for successful commercialisation of products based on organic electronics. The following sentences summarize the future outlook in this direction.

- Feedback to manufacturing engineer that can lead to variation-aware manufacturability. For e.g. the suitable combination of printing directions that can reduce the process variations
- Investigation and understanding of the correlation between the process and circuit parameters and development of design for manufacturing approaches
- Development of a process design kit for organic technology with improved models including a reliability and ageing model
- Investigation of noise in OTFTs and development of an appropriate noise model to simulate their behaviour

Appendix A: Verilog-A Code for OTFT Simulation Model

```
// VerilogA for printed_el, otft_mod3, veriloga
// With the Dynamic Model for Transistor
/*
File     :    otft_mod3.va
Author   :    Ramkumar Ganesan
Org :    TU Darmstadt
Date     :    11-Aug-10

Description:
     Implements the model for Organic TFT using VRH model with dynamic
    behaviour.
*/

`include "constants.vams"
`include "disciplines.vams"
//-------------------------------------------------------------------//
//                      Constants definition                         //
//-------------------------------------------------------------------//

`define NTYPE -1;
`define PTYPE 1;
`define EQN3;
`define DYNAMIC_MODEL 1;
//`define HYSTERESIS_MODEL 1;

//`define SAT_MODEL_1; // Given in Book.
`define SAT_MODEL_2; // Modified Saturation model from thesis(4.2.3.5)
`define MC_SIM; // Uncomment this for montecarlo simulations

//`define SUBTHRESHOLD_BEHAVIOUR;
//`define OFF_BEHAVIOUR;

//-------------------------------------------------------------------//
//                        Module definition                          //
//-------------------------------------------------------------------//

module otft_mod3( g, d, s);
 inout d, g, s;
 electrical d, g, s;

//electrical dd, gg;

//-------------------------------------------------------------------//
//                      Parameters definition                        //
//-------------------------------------------------------------------//
```

```
   parameter real Cox = 62.0e-6; // F per Sq.m
   parameter real sl = -0.44 from (-inf:inf);   //Inverse subthreshold
    slope. - V/decade
   parameter real sigma = 0.2 from (-inf:inf);  //subthreshold fitting
    parameter.
   parameter real roff = 10G from (0:inf);  //off resistance. - ohm
   parameter real i0 = 0.067 from (0:inf);  //subthreshold current
    parameter. - A
   parameter real beta = 29.162p; // from (0:inf);//beta=u0*w*ci/l
   parameter real gamma = 1.4380; //from (0:inf);//mobility exponent
   parameter real vth = 5.9347;// from (0:inf); //Threshold voltage. - V
`ifdef MC_SIM
   (* cds_inherited_parameter *) parameter real dIds_pro = 0;
   (* cds_inherited_parameter *) parameter real dIds_mis = 0;
`else
   parameter real dIds_pro=1; //Ids for process variation
   parameter real dIds_mis=0; //Ids for mismatch
`endif
   parameter real w = 400u from (0:inf);     //width. -m
   parameter real l = 20u from (0:inf); //length. -m

   parameter real w_ch = 2.94u;     // Correction to the width. Used for
    gate channel capacitance
   parameter real l_cor =1.8u;      // The correction to the channel length
   parameter real l_ov = 2.22u; //Overlap length of source and drain
   parameter real w_ov = -196.66u;
   parameter real ws_ov = 31.742u; // The width of source overlap area
    which is additional to that of gate drain overlap area
   parameter real ls_ov = 16.738u; // The length of source overlap area
    which is additional to that of gate drain overlap area

   parameter real lambda = 0.0239;// from (0:inf);  //Channel shortening
    parameter.
   parameter real k = 86u from [0:inf); //linear correction parameter.
    Inversely proportional to l.
   parameter integer trans_type = -1 from [-1:1] exclude 0; //type of
    device. n(1) or p(-1).

//-------------------------------------------------------------------//
//                  Variables definition                             //
//-------------------------------------------------------------------//
   //parasitic capacitors in the transistor
    real       C_DS;
    real       C_GS;
    real       C_GD;

    real       C_ch;  // Gate Channel Capacitance
    real       C_dov;  // Gate Drain overlap Capacitance
    real       C_sov;  // Gate Source Overlap Capacitance

    real       A_ch,A_sov,A_dov;
    real       v_DS, v_GS,v_GD,v_Gt;
    real       i_DS,i_DS_0;
```

```
    real      i_d,i_gd ;//current from C_DG
    real      i_g,i_gs ;//current from C_GS

    real      q_gd;//charge from C_DG
    real      q_gs;//charge from C_GS

    real      id_acc1,id_acc2,id_sub,id_off,id_acc1_sat,id_acc2_sat;
    real      id_acc3;
    integer   op_level;

    real vs;
    real cur_dir;

//-------------------------------------------------------------------//
//                 An analog function needed later                   //
//-------------------------------------------------------------------//
    analog function real double_sqr_brackets;
     input vx;
     real vx;
     real x_ret;
     begin
    x_ret = vx/2 + abs(vx)/2;
    double_sqr_brackets = x_ret;
     end
    endfunction

//-------------------------------------------------------------------//
//                 Main_Model from Statistic                         //
//-------------------------------------------------------------------//

analog begin

@(initial_step)
begin
  cur_dir = 1.0;

        id_acc1 = 0.0;
        id_acc1_sat = 0.0;
        id_acc2 = 0.0;
        id_acc2_sat = 0.0;
        id_acc3 = 0.0;
end

    vs = V(s);
//  if (vs != 0.0)
//  $strobe("Source /not connected to ground./n");

    v_DS = V(d, s);

    if (v_DS <= 0.0)
    begin
        mode = 1;
        v_GS = V(g, s);
        v_GD = V(g, d);
    end
```

```
    else
    begin
        mode = -1;
        v_GS = V(g, d);
        v_GD = V(g, s);
    end

v_Gt = v_GS - vth;  //added on 7.3.12

    id_acc1 = (beta*(pow(double_sqr_brackets(-v_GS + vth),(2.0+gamma)) -
   pow(double_sqr_brackets(-v_GS + vth + (mode*v_DS)),2.0+gamma)))/(2.0+
   gamma);
    id_acc1_sat = (beta*(pow(double_sqr_brackets(-v_GS + vth),2+gamma)))
   /(2.0+gamma);
    id_acc2 = id_acc1*min((1.0 +k*double_sqr_brackets(mode*v_DS)),(1.0 +k*
   double_sqr_brackets(-v_GS + vth)));
    id_acc2_sat = id_acc1_sat*min((1.0 +k*double_sqr_brackets(v_GS - vth))
   ,(1.0 +k*double_sqr_brackets(-v_GS + vth)));



`ifdef SAT_MODEL_1 // Given in Book.
    id_acc3 = id_acc2 + (lambda*pow((w/l),(1.0/3.0))*pow((
   double_sqr_brackets(v_GS + vth - (mode*v_DS))*abs(id_acc2_sat))
   ,(2.0/3.0)));
`endif

`ifdef SAT_MODEL_2 // Modified Saturation model from thesis(4.2.3.5)
    id_acc3 = id_acc2*(1.0 +(lambda*(-mode*v_DS)));
`endif

    if (v_GS <= vth)
//      id_sub = i0*pow(abs(mode*v_DS),sigma)*limexp(ln(10)*
   double_sqr_brackets(v_GS - vth)/sl);
        id_sub = 0.0;

    else
        id_sub = 0.0;

    id_off = (mode*v_DS)/roff;

    `ifdef EQN1     //Iacc1 //3/11 added cur_dir
    i_DS_0 = mode*trans_type*id_acc1*cur_dir;
    `endif
    `ifdef EQN2     //Iacc2
    i_DS_0 = mode*trans_type*id_acc2*cur_dir;
    `endif
    `ifdef EQN3     //Iacc3
//  i_DS_0 <+ absdelay(trans_type*id_acc3*cur_dir,1f);
    i_DS_0 = mode*trans_type*id_acc3*cur_dir;
    `endif
    `ifdef SUBTHRESHOLD_BEHAVIOUR       //Subthreshold model current is
   added
    i_DS_0 = mode*trans_type*id_sub;
    `endif
```

```
    `ifdef OFF_BEHAVIOUR    //Off current in the depletion regime is added
    i_DS_0 = mode*trans_type*id_off;
    `endif

i_DS=i_DS_0*dIds_pro*(1+dIds_mis);

// Add rout
//  I(d,s) <+ I(d,s) + V(d,s)/rout;


//Calculating Channel and overlap capaciatnces
A_ch = (w+w_ch)*(l+l_cor);
A_dov= (w+w_ov)*l_ov;
A_sov= A_dov + ws_ov*(l+ls_ov);

C_ch = Cox*(w+w_ch)*(l+l_cor);
C_dov = Cox*(w+w_ov)*l_ov;
C_sov = C_dov + Cox*ws_ov*(l+ls_ov);     // The gate source overlap area is
    larger than the drain source overlap area. The additional area is
   accounted by ws_ov*(l+ls_ov)

$discontinuity(0);
if (v_Gt >= 0) //cut-off region
 begin
 q_gs = C_sov*v_GS;
 q_gd = C_dov*v_GD;
 end
else if (v_Gt > (mode*v_DS) )  // linear region
 begin
 q_gs = (C_ch/2)*(v_GS-vth) + C_sov*v_GS;
 q_gd = C_ch/2*(v_GS-vth)+C_dov*v_GD  ;
 end
else        // saturation region
 begin
// q_gs = (1/2)*C_ch*(v_GS-vth) + (1/6)*C_ch*(v_GS-vth)*(1- pow((v_GS-vth)
   /(mode*v_DS),2.0)) + C_sov*v_GS;    // Made it continuous. Pow of 2 to
   make the transistion rapid once Vds crosses Vgs-vth
// q_gd = (1/2)*C_ch*(v_GS-vth) - (1/6)*C_ch*(v_GS-vth)*(1- pow((v_GS-vth)
   /(mode*v_DS),2.0)) + C_dov*v_GD;    // Made it continuous. Pow of 2 to
   make the transistion rapid once Vds crosses Vgs-vth

 q_gs = (1/2)*C_ch*(v_GS-vth) + (1/6)*C_ch*(v_GS-vth)*(1- exp(mode*v_DS-(
   v_GS-vth))) + C_sov*v_GS;    // Made it continuous. Exp has 1 when Vds=
   Vgs - vth and then decreases rapidly to 0.
 q_gd = (C_ch/2)*(v_GS-vth) - (1/6)*C_ch*(v_GS-vth)*(1- exp(mode*v_DS-(v_GS
   -vth))) + C_dov*v_GD;
 end

i_gd = trans_type*ddt(q_gd);
i_gs = trans_type*ddt(q_gs);

//Output
`ifdef DYNAMIC_MODEL
I(d) <+ i_DS + i_gd;
I(s) <+ -i_DS + i_gs;
```

```
I(g) <+ -i_gs - i_gd;
//   I(d,s)<+ i_DS ;
//   I(g,d)<+  mode*trans_type*ddt(q_gd);
//   I(g,s)<+  mode*trans_type*ddt(q_gs);
//   I(g,d)<+ C_GD*ddt(v_GD);
//   I(g,s)<+ C_GS*ddt(v_GS);
`else
    I(d,s)<+ i_DS;
    I(g,d)<+ 0.0;
    I(g,s)<+ 0.0;
`endif

end
end
endmodule
```

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Curriculum Vitae

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