Analysis of Current Conveyor based Switched Capacitor Circuits for Application in $\Delta\Sigma$ Modulators

Dem Fachbereich Elektrotechnik und Informationstechnik
der Technischen Universität Darmstadt
zur Erlangung des akademischen Grades eines
Doktor-Ingenieurs (Dr.-Ing.)
genehmigte Dissertation

von

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Tag der Einreichung:	15.09.2014
Tag der mündlichen Prüfung:	15.12.2014

D17
Darmstadt 2015

Erklärung laut §9 PromO

Ich versichere hiermit, dass ich die vorliegende Dissertation allein und nur unter Verwendung der angegebenen Literatur verfasst habe. Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient.

Plochingen, 16.02.2015

Acknowledgements

This thesis is a consequence of the work done as a teaching and research assistant at the Integrated Electronic Systems Lab of the Technische Universität Darmstadt. I would like to express my sincere gratitude to my Doktorvater, mentor and advisor Prof. Dr.-Ing. Klaus Hofmann for his continuous support, patience and motivation throughout my years of Ph.D study. I thank him for having confidence in my capabilities and giving me this wonderful opportunity of pursuing research under his guidance.

I would like to express my gratitude to Prof. Dr.-Ing. Roland Thewes for agreeing to become the Co-Referee for my thesis. His comments and observations were valuable and instrumental in improving the quality of the work. Besides my advisor and co-referee, I would like to thank the rest of my thesis committee for their thoughtful comments and advice, which helped improve the quality of my thesis.

My Ph.D would not have been enjoyable without the friendly atmosphere and camaraderie displayed by my colleagues. For this I would like to thank all my colleagues with whom I had the pleasure of carrying out interesting conversations regarding research, projects, conferences and administrative issues.

Last but not least I would like to thank my entire family, particularly my parents for their support and encouragement throughout my career. Without their best wishes and backing, I would not be in the position I am in today. A very special thanks to my wife Kamala for her love, understanding and assistance in proofreading this thesis!

Abstract

The reduction in supply voltage, loss of dynamic range and increased noise prevent the analog circuits from taking advantage of advanced technologies. Therefore the trend is to move all signal processing tasks to digital domain where advantages of technology scaling can be used. Due to this, there exists a need for data converters with large signal bandwidths, higher speeds and greater dynamic range to act as an interface between real world analog and digital signals.

The Delta Sigma ($\Delta\Sigma$) modulator is a data converter that makes use of large sampling rates and noise shaping techniques to achieve high resolution in the band of interest. The modulator consists of analog integrators and comparators which create a modulated digital bit stream whose average represents the input value. Due to their simplicity, they are popular in narrow band receivers, medical and sensor applications.

However Operational Amplifiers (Op-Amps) or Operational Transconductance Amplifiers (OTAs), which are commonly used in data converters, present a bottleneck. Due to low supply voltages, designers rely on folded cascode, multistage cascade and bulk driven topologies for their designs. Although the two stage or multistage cascade topologies offer good gain and bandwidth, they suffer from stability problems due to multiple stages and feedback requiring large compensation capacitors. Therefore other low voltage Switched-Capacitor (SC) circuit techniques were developed to overcome these problems, based on inverters, comparators and unity gain buffers.

In this thesis we present an alternative approach to design of $\Delta\Sigma$ modulators using Second Generation Current Conveyors (CCIIs). The important feature of these modulators is the replacement of the traditional Op-Amp based SC integrators with CCII based SC integrators. The main design issues such as the effect of the non-idealities in the CCIIs are considered in the operation of SC circuits and solutions are proposed to cancel them. Design tradeoffs and guidelines for various components of the circuit are presented through analysis of existing and the proposed SC circuits. A two step adaptive calibration technique is presented which uses few additional components to measure the integrator input output characteristic and linearize it for providing optimum performance over a wide range of sampling frequencies while maintaining low power and area.

The presented CCII integrator and calibration circuit are used in the design of a 4th order (2-2 cascade) $\Delta\Sigma$ modulator which has been fabricated in UMC 90nm/1V technology through Europractice. Experimental values for Signal to Noise+Distortion Ratio (SNDR), Dynamic Range (DR) and Figure Of Merit (FOM) show that the modulator can compete with state of art reconfigurable Discrete-Time (DT) architectures while using lower gain stages and less design complexity.

Kurzfassung

Analoge Schaltungen profitieren im Vergleich zu digitalen Schaltungen nur wenig von den Vorteilen moderner Technologien, da die abnehmenden Versorgungsspannungen deren Dynamikbereich reduzieren und gleichzeitig mehr Leistung zur Rauschminimierung benötigen. Es war und ist daher nur konsequent möglichst viele Signalverarbeitungsaufgaben in die digitale Domäne zu verlagern, in der die Vorteile moderner Technologien mit kleinsten Strukturgrößen zum Tragen kommen. Als weitere Konsequenz hieraus stieg der Bedarf nach schnellen Datenkonvertern mit großer Bandbreite und großem Dynamikbereich als Schnittstelle zwischen der analogen und digitalen Domäne rasch an.

Der Delta Sigma ($\Delta\Sigma$) Modulator ist eine der gebräuchlichsten Datenkonverterrealisierung mit hoher Abtastrate, ermöglicht eine hohe Auflösung im zu betrachtenden Spannungsbereich und bietet gleichzeitig die Möglichkeit einer effektiven Rauschunterdrückung. Der Modulator erzeugt einen pulsweitenmodulierten digitalen Datenstrom, ist darüber hinaus einfach aufgebaut und besteht im Wesentlichen aus analogen Integratoren und Komparatoren. $\Delta\Sigma$ Modulatoren werden häufig für schmalbandige Empfänger, Medizin- und Sensoranwendungen eingesetzt. Herkömmliche Operationsverstärker (Op-Amps oder OTAs) als eine Hauptkomponente dieser Datenkonverter limitieren jedoch zunehmend deren Leistungsfähigkeit. Aufgrund der niedrigen Versorgungsspannungen sind Entwickler zunehmend gehalten Folded-Cascode-, Multistage-Kaskaden- und Bulk-Driven-Topologien in ihren Schaltungsentwürfen einzusetzen. Die bei Multistage-Kaskaden sehr hohe Verstärkung und Bandbreite wird meist mit Stabilitätsproblemen aufgrund der hohen Anzahl von verstärkenden Stufen bzw. Rückkopplungen mit großen Kompensationskapazitäten erkauft. Es war daher nur konsequent, leistungseffiziente Switched-Capacitor (SC) Schaltungstechniken auf der Basis von Invertern, Komparatoren und Spannungsfolgern zu favorisieren.

In dieser Arbeit wird ein alternativer Ansatz zum Entwurf von $\Delta\Sigma$ Modulatoren unter Verwendung von Current Conveyor (CCII) der zweiten Generation untersucht. Bei diesen Modulatoren werden die herkömmlichen, auf Operationsverstärkern basierenden SC-Integratoren durch solche mit CCIIs ersetzt. Die auftretenden Entwurfsprobleme, wie beispielsweise die Nichtidealitäten der CCIIs werden in der Anwendung der SC-Integratoren diskutiert und Lösungen aufgezeigt. Weiterhin werden Entwurfsraumexplorationen zwischen verschiedenen Komponenten durch Analyse herkömmlicher und verbesserter SC-Schaltungen durchgeführt. Ferner wird ein adaptives Kalibrierungsverfahren mit nur wenigen zusätzlichen Komponenten beschrieben, das den Einsatz des Modulators über einen weiten Bereich von Abtastfrequenzen bei gleichzeitig optimaler Performanz, kleinem Silizium-Flächenbedarf und niedriger Leistungsaufnahme ermöglicht.

Die behandelten CCII Integratoren sind in einem Entwurfsbeispiel eines $\Delta\Sigma$ Modulators 4. Ordnung (2-2 Kaskade) in 90nm/1V UMC Technologie exemplarisch unter Verwendung des Europractice Services gefertigt worden. Messungen zeigen ein gegenüber herkömmlichen zeitdiskreten Architekturen vergleichbares Rausch/Störverhältnis (Signal to Noise+Distortion Ratio (SNDR)) sowie einen vergleichbaren Dynamikbereich (Dynamic Range (DR)), bei jedoch deutlich reduzierter Schaltungskomplexität und geringerer Anzahl der Verstärkerstufen.

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List of Abbreviations

$\Delta\Sigma$ Delta Sigma

ADC Analog to Digital Converter

BT Bluetooth

CBSC Comparator Based Switched Capacitor

CC Current Conveyor

CCCS Current Controlled Current Source

CCI First Generation Current Conveyor

CCII Second Generation Current Conveyor

CCIII Third Generation Current Conveyor

CCVS Current Controlled Voltage Source

CFOA Current Feedback Operational Amplifier

CT Continuous-Time

DAC Digital to Analog Converter

DEM Dynamic Element Matching

DR Dynamic Range

DT Discrete-Time

DVB-H Digital Video Broadcasting-Handheld

ENOB Effective Number of Bits

FOM Figure Of Merit

GPS Global Positioning System

GSM Global System for Mobile Communications

ICCII Inverting Second Generation Current Conveyor

ITF Integrator Transfer Function

LSB Least Significant Bit

MASH Multi-Stage Noise Shaping

MOM Metal-Oxide-Metal

MOS Metal-Oxide-Semiconductor

NTF Noise Transfer Function

Op-Amp Operational Amplifier

OSR Oversampling Ratio

OTA Operational Transconductance Amplifier

PCB Printed-Circuit-Board

PDF Probability Density Function

PDM Pulse Density Modulated

PSD Power Spectral Density

PSU Power Supply Unit

SC Switched-Capacitor

SI Switched-Current

SNDR Signal to Noise+Distortion Ratio

SNR Signal to Noise Ratio

SQNR Signal to Quantization Noise Ratio

SR Slew-Rate

STF Signal Transfer Function

UMTS Universal Mobile Telecommunication System

VCCS Voltage Controlled Current Source

VCVS Voltage Controlled Voltage Source

1 Introduction

Contents

1.1 Motivation and Research Scope

CMOS dominates the semiconductor market with each advanced technology node offering more transistors per unit area. New nodes offer transistors which work at low supply voltages consuming less power while providing higher operating frequencies [1]. Analog circuits unfortunately have not been able to take advantage of these new technology nodes because the reduction in supply voltages also decreases the dynamic range significantly, thus requiring more power and large sampling capacitors to scale circuit noise. Compounding this problem is the fact that analog circuit design techniques and development of new architectures have not been able to keep up the pace in innovation as their digital counterparts.

It is well known that signal processing tasks done in digital domain enable savings in power consumption and silicon area, increased robustness, faster design process, flexibility, programmability and greater possibilities for design reuse. For digital circuits, advanced technologies lead to more powerful and area efficient chips with greater functionality in the fields of electronics ranging from medical to wireless communications. Therefore the trend is to move all signal processing tasks to digital domain where technology scaling advantages can be properly harnessed.

Data converters are therefore required as they form a critical interface between the analog and digital domains. Because of the huge advantages in digital circuits provided by technology scaling, data converters with increasingly large bandwidths, higher speeds and greater dynamic range are needed to interface with the high performance digital circuits. The need for tight integration of all system components on a single chip, so called System-on-Chip (SoCs) additionally imposes the condition that data converters must be designed with the same technology as the digital circuits.

A fundamental building block used predominantly in data converter design is the Op-Amp. In advanced technology nodes where low supply voltage forms a critical road block, designing Op-Amp architectures which allow low noise, high bandwidth and linearity becomes an important issue. Because of low supply voltages, Op-Amp architectures which allow high gain such as gain boosting and cascode, high speed and low power such as telescopic cascode cannot be used. Instead designers have to rely on two stage, folded cascode and bulk input driven topologies for their designs. Although the two stage or multi-stage cascade topologies offer high gain and bandwidth, they suffer from increased stability problems due to multiple stages and feedback.

Technology scaling additionally aggravates the device leakage and mismatch issues due to variation in transistor threshold voltages, transconductance parameters which in the end requires some form of calibration/compensation technique to maintain acceptable performance.

In order to overcome design challenges in low voltage regimes, designers often look towards non Op-Amp based architectures to avoid the problems associated with Op-Amp in low voltage regime. Circuits such as dynamic amplifiers, unity gain buffers, comparators and inverters which are not restricted by low supply voltages are therefore gaining prominence in data converter design. The authors Sedra and Smith proposed different generations (First Generation Current Conveyor (CCI) and Second Generation Current Conveyor (CCII)) of a new building block analogous to the Op-Amp called the Current Conveyor (CC) in 1968 which has some inherent advantages.

Unlike the gain bandwidth limited Op-Amp, CCs are able to maintain independent control over gain and bandwidth separately thus allowing them to be used in high frequency applications. The CC is a circuit capable of working in both voltage mode and current mode while the Op-Amp is primarily operated in voltage mode. This allows the designer to expand his design space to include data converters working in current mode or as a combination or voltage mode and current mode together. Additionally stability problems commonly associated with Op-Amps can be avoided with CCs which primarily operate in open loop mode.

The objective of this thesis is to explore the feasibility of replacing Op-Amps based SC circuits with CCII based SC circuits. The thesis provides an introduction to the non-idealities of the CCII and analyzes the effect of the non-idealities on the SC operation. The important non-idealities of the CCII are identified from the analysis which are responsible for losses in the SC circuit. Different circuit and system design techniques are proposed to cancel the non ideal effects of CCIIs and make them useful for designing $\Delta\Sigma$ modulators. A simple two step adaptive calibration algorithm is introduced to correct non idealities of the SC circuit and improve its performance over a wide range of sampling frequencies.

To demonstrate the feasibility of the proposed CCII SC circuit, 2nd order $\Delta\Sigma$ and a 4th order (2-2 cascade) $\Delta\Sigma$ modulators are implemented and simulated in UMC 90nm CMOS process. Additionally, prototypes of the simulated modulator are fabricated through the same technology and measurement results of the chip are discussed. The simulations and measurements show the feasibility of circuit implementation and its efficiency in providing guaranteed dynamic range for different bandwidths.

1.2 Thesis Outline

The dissertation is organized into 6 chapters. Chapter 2 starts with a brief introduction to the operating principles of delta sigma modulators. Important performance metrics of the modulator such as the order, oversampling ratio and noise shaping are presented. This is followed with the description of various design strategies and modulator architectures to achieve high signal to noise ratios and dynamic range. The major design challenges designers face in delta sigma modulator design using Op-Amps are presented. Various delta sigma circuit architectures using inverters, comparators and other low voltage techniques are then introduced and compared with the traditional approach. Their advantages and disadvantages are touched upon in the course of their description. Finally the chapter presents a survey of the various published papers in the field of delta sigma modulators.

After covering the state of the art in low voltage delta sigma modulator design, chapter 3 gives an introduction to the history of CCs and presents a detailed analysis of SC circuits based on CCIIs. As the primary focus of this thesis is to find a replacement circuit for the Op-Amp in delta sigma modulators, the chapter gives a detailed look into this block and its characteristics. Different CC generations are described, along with their advantages and disadvantages. After introducing the various types of CCs, existing SC circuits proposed in literature are analyzed and compared with regards to feasibility of implementation, circuit behavior and performance. The main non idealities in CCII are then introduced and their effects on SC circuits are analyzed. The chapter proceeds with the discussion of the benefits and drawbacks of the existing approaches and then proposes a new approach to the design of the SC circuits using CCII. Adaptive calibration techniques to deal with the non idealities present in the CCIIs are presented in order to produce high accuracy SC circuits covering a wide sampling frequency range.

Chapter 4 presents the implementation details of 2nd order and 4th order delta sigma modulators using the CCII based SC circuit introduced in the previous chapter. The topology as well as circuit blocks are shown and discussed. The additional effects on the delta sigma modulator performance coming from the choice of circuit topology is also discussed. Simulation results obtained from MATLAB toolbox and Cadence AMS simulator using the UMC 90nm process at a supply voltage of 1V are given.

In order to verify the performance at chip level, Chapter 5 describes the measurement results obtained from the prototype of the 2nd order and 4th order delta sigma modulators fabricated through the UMC 90nm CMOS process. The chapter talks about the prototype, chip floor plan, layout and optimization techniques used during the design phase. The description of the test setup used to characterize the prototype is also described. The measured results are compared and analyzed with the simulation values obtained from the previous chapter. Finally the FOM of the modulator is compared with other state of the art implementations described in chapter 2.

Chapter 6 concludes the dissertation by giving a brief summary of the contributions of this work. Possible enhancements and design strategies to further improve the performance of the proposed circuit as well as directions for future work are presented.

2 Fundamentals and State of the Art in Low Voltage $\Delta\Sigma$ ADCs

Contents

The ADC is one of the most important blocks in communication systems. As an interface between analog signals and digital signals, the ADC is responsible for converting signals from one domain to another. Various ADC topologies exist depending on signal bandwidth, conversion speed and resolution needed for different applications. Among the ADC topologies, $\Delta\Sigma$ ADC is the most popular one featuring high resolution and high bandwidths without needing precision analog devices. This makes it useful in all application areas ranging from low bandwidth/high resolution needed for medical applications to high bandwidth/medium resolution needed for communication systems.

This chapter is intended as an introduction to the $\Delta\Sigma$ modulator and its plethora of architectures [2, 3]. The chapter presents the principles of $\Delta\Sigma$ conversion first, followed by introduction to various $\Delta\Sigma$ topologies. $\Delta\Sigma$ performance metrics are introduced in later sections followed by discussion on the state of the art designs in $\Delta\Sigma$ modulators. Finally the chapter concludes by presenting a survey of various delta sigma modulators published in literature by various authors.

2.1 Nyquist ADCs

Data converters can be classified into two types: Nyquist rate ADCs and Oversampling ADCs. Nyquist theorem governs the functioning of nyquist rate converters and it states that for a given input signal bandwidth of f_b and a sampling rate of f_s, the input signal can be reconstructed from its sampled values without loss of information if the sampling frequency is atleast two times greater than the input signal bandwidth ($f_s > 2f_b$).

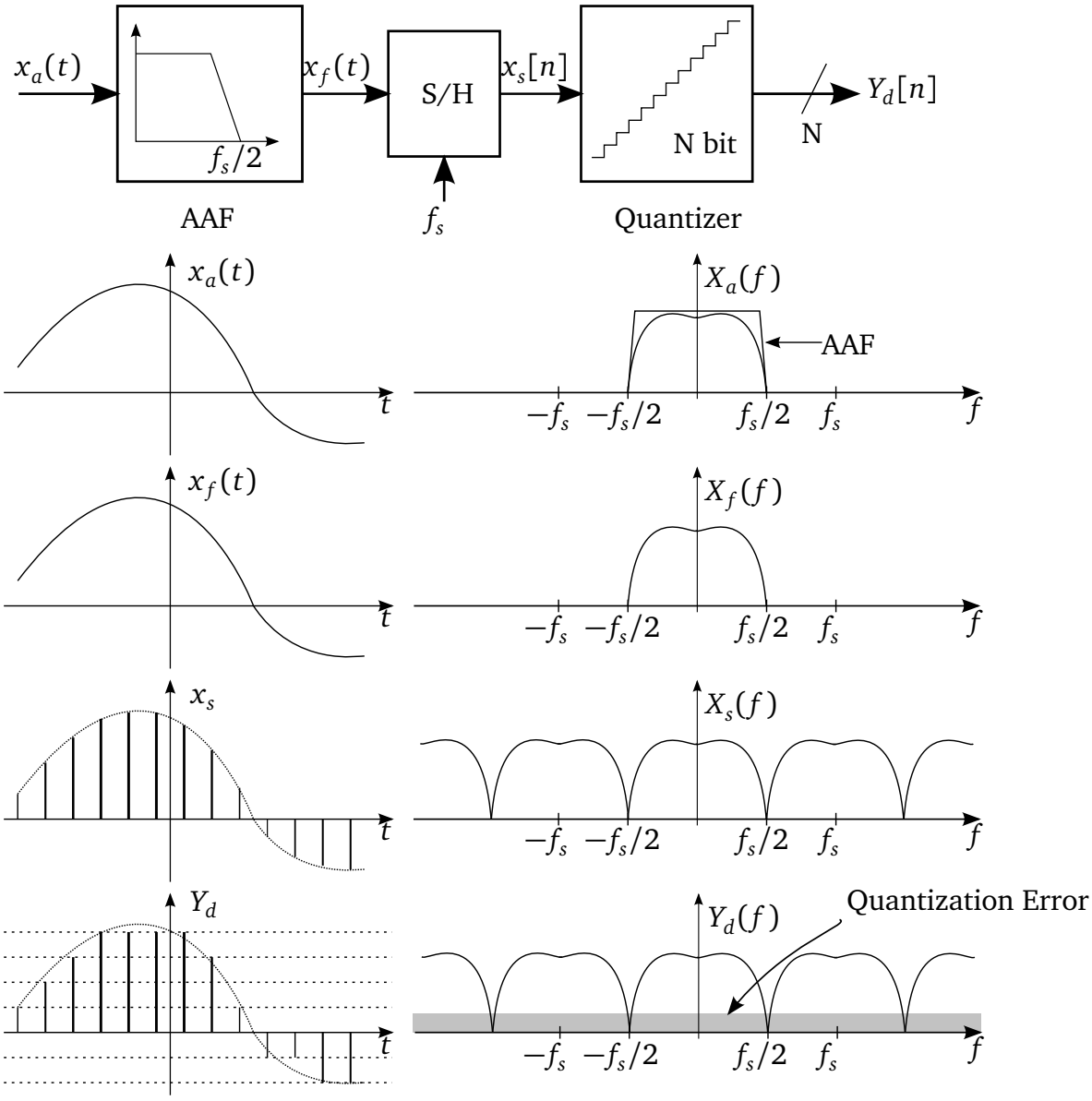


Figure 2.1: Generic Nyquist-rate ADC showing the signal processing steps. AAF denotes the anti-aliasing filter. S/H denotes the sample and hold block [2, 3].

Figure 2.1 shows the generic nyquist-rate ADC architecture [2, 3]. The figure also shows the various steps involved in processing of the input signal. The architecture processes the input signal by first bandlimiting it to frequency of f_b using an anti-aliasing filter and then sampling it in the time domain at frequency of f_s to create a discrete set of samples. This is then followed by quantization of each sample in the amplitude domain to generate a unique set

of digital outputs corresponding to each amplitude. In this conversion process, the nyquist rate converters introduce an error called the quantization error. This error appears due to fact that an infinite resolution input signal is being represented by set of finite digital values. Hence to lower the quantization error, the number of digital values used for representing the input signal, i.e. the resolution of the ADC needs to be increased.

The quantization error e_q of the nyquist ADC is smaller than its quantization step Δ, also called the Least Significant Bit (LSB). Assuming that the input signal changes by a large amount from sample to sample, it can be considered that the quantization error is largely uncorrelated to input signal and is evenly distributed over the quantization step $\pm\Delta/2$. Under such a condition, the quantization error can be modeled by a white random noise and its Probability Density Function (PDF) given by Figure 2.2a [2]. The quantization error power can be then calculated in relation to quantization step as:

$$P_q = e_q^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e_q^2 de_q = \frac{\Delta^2}{12} \tag{2.1}$$

Figure 2.2b shows the distribution of the quantization error power given in Equation 2.1 equally in the frequency band between [$-f_s/2, f_s/2$] [2]. For a nyquist converter with a sampling rate of $f_s = 2f_b$, it is seen that the total quantization error power appears within the signal band. Thus quantization error also called quantization noise is the limiting factor in reaching high resolution with nyquist rate ADCs. The Power Spectral Density (PSD) within the signal band is given as:

$$S_e(f) = S_e = \frac{\sigma_e^2}{f_s} = \frac{\Delta^2}{12f_s} \tag{2.2}$$

and the total quantization noise power within the signal band f_b is given by:

$$P_e = \int_{-f_b}^{f_b} S_e(f)df = S_e\int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} df = \frac{\Delta^2}{12} \tag{2.3}$$

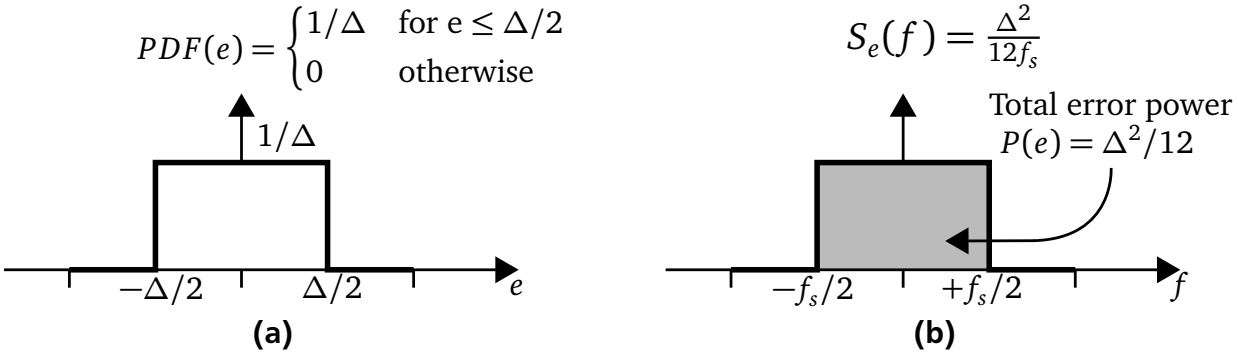


Figure 2.2: Quantization error (a) Probability density function and (b) Power spectral density.

From Equation 2.3, the maximum possible Dynamic Range (DR) of an ideal N bit nyquist converter can be calculated using Equation 2.4, where N is the finite resolution of the converter and

the peak input signal power given by $P_x = e_x^2 = 2^{2N-3}\Delta^2$. This equation is the well known formula for DR which states that for every additional bit increase in resolution, a DR improvement of 6dB can be observed.

$$DR_{dB} = 10\log\frac{P_x}{P_e} = 6.02N + 1.76dB \tag{2.4}$$

2.2 Principles of $\Delta\Sigma$ Modulators

In the previous section, a brief theory of nyquist rate ADCs was given. It is observed that the quantization error falls entirely within the signal band. This error needs to be reduced from the signal band and moved away so as to improve the resolution or the DR of the ADC. $\Delta\Sigma$ ADCs work on the two principles of oversampling and noise shaping to achieve this goal of noise reduction in the signal band.

2.2.1 Oversampling and Noise shaping

Equation 2.2 introduced the relation between error power and sampling frequency. It can be seen that as sampling frequency is increased beyond the nyquist rate of $f_s = 2f_b$, the quantization noise power spreads over a much larger sampling frequency band f_s. Thus the total quantization noise power within the signal band f_b is reduced. This process of reducing the noise power in the signal band is called oversampling. The OSR defines how many times over the nyquist rate the input signal is being sampled. It is given as:

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b} \tag{2.5}$$

where f_N is the nyquist rate sampling frequency.

The first advantage of oversampling is the relaxed design requirement of the anti aliasing filter. As seen from Figure 2.1, in nyquist rate ADCs the anti-aliasing filter needs to have a sharp roll-off due to the close placement of the in-band and out-of-band signal components. Using oversampling, the in-band and out-of-band signal components can have a much larger separation between them reducing the requirement of a sharp roll-off anti aliasing filter as shown in Figure 2.3 [3].

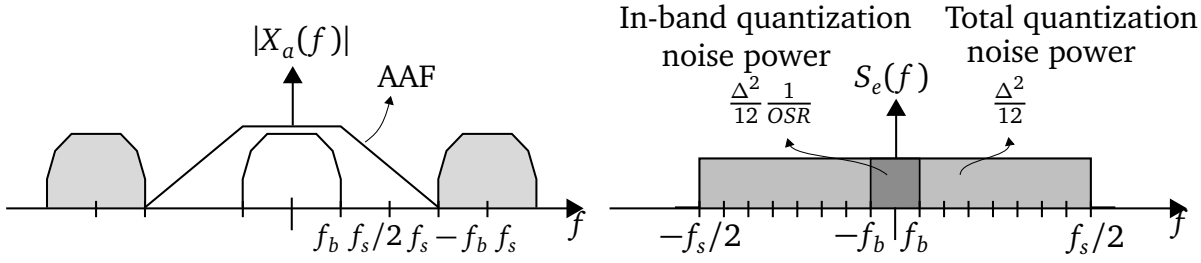


Figure 2.3: Anti-aliasing filter and Quantization error power spectral density distribution for an oversampled converter with OSR=8.

The second advantage of oversampling is the decrease of in-band quantization noise power as shown in Equation 2.6.

$$P_e = \int_{-f_b}^{f_b} S_e(f)df = S_e \int_{-f_b}^{f_b} df = \frac{\Delta^2 f_b}{6f_s} = \frac{\Delta^2}{12OSR} \tag{2.6}$$

The above equation states that the quantization noise power is inversely related to OSR. As the OSR increases, in-band noise reduces. Figure 2.3 shows the decrease in the overall in-band quantization noise power for an oversampling converter with a OSR of 8. The oversampling technique is an effective way to increase the DR and hence the ADC resolution. The peak DR of an oversampled ADC can be computed as before:

$$DR_{dB} = 10\log\frac{P_x}{P_e} = 6.02N + 1.76dB + 10\log OSR \tag{2.7}$$

where P_e is the in-band quantization noise power given in Equation 2.6.

Although the oversampling technique increases the effective DR of the system by 3dB for each doubling of the sampling frequency, the increase in the cost of system requirements in terms of speed of the circuit is more. Hence the meagre increase in DR of the system using oversampling alone does not justify its usage in circuit design. In order to increase the DR substantially, the noise in addition to being distributed over the wide sampling frequency range must additionally be shaped away from the input signal band to further increase the resolution.

The technique of processing the error power away from signal band is called Noise Shaping. Consider an N bit quantizer with large OSR such that the signal changes from sample to sample only by a small amount so that low frequency components of the quantization error between successive samples are similar. Taking the difference between two consecutive error samples and processing them results in:

$$q(n) = e(n) - e(n-1) \tag{2.8}$$

and the equivalent in Z domain becomes:

$$Q(z) = (1 - z^{-1})E(z) = NTF(z)E(z) \tag{2.9}$$

Equation 2.9 shows the noise being filtered by the function $NTF(z)$ which is called the Noise Transfer Function (NTF). The system applies high pass filtering to the noise component, allowing only high frequency components of the noise to pass through the ADC and reducing the in-band noise. This noise transfer function is responsible for pushing the noise away from the signal band and improving the DR of the ADC. Taking the squared magnitude of the NTF in frequency domain and plotting the equation results in the Figure 2.4.

$$|NTF(f)|^2 = |1 - e^{-j2\pi f/f_s}|^2 = 4sin^2(\pi f/f_s) \approx 4(\pi f/f_s)^2 \tag{2.10}$$

The previous equation shows the noise shaping of the first order. By extension of the first order noise shaping to higher order noise shaping of L^{th} order we get:

$$Q(z) = (1 - z^{-1})^L E(z) = NTF(z)E(z) \tag{2.11}$$

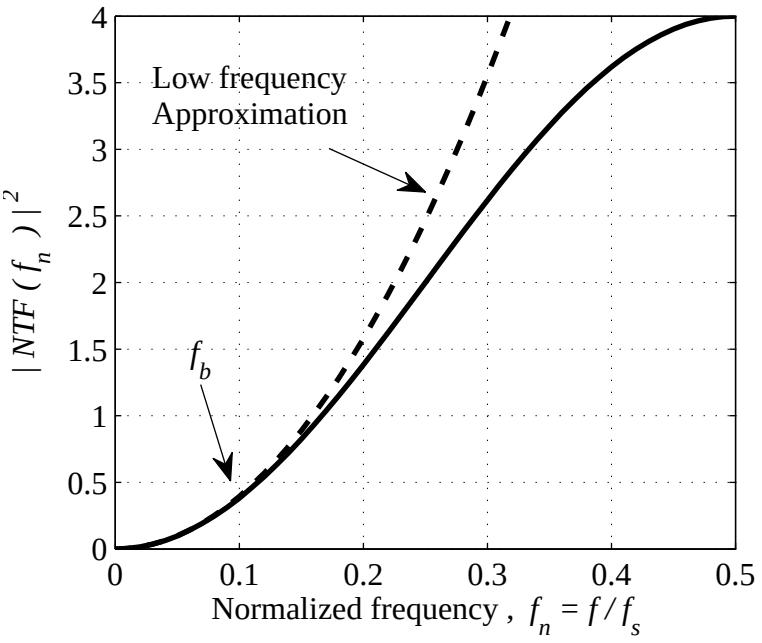


Figure 2.4: Noise shaping characteristics of an oversampled converter showing first order noise shaping.

$$|NTF(f)|^2 = |1 - e^{-j2\pi f/f_s}|^{2L} = 2^{2L} sin^{2L}(\pi f/f_s) \approx 2^{2L}(\pi f/f_s)^{2L} \tag{2.12}$$

The PSD of the nyquist converter was given in Equation 2.2. The PSD of a oversampling and noise shaping converter is given by:

$$S_q(f) = |NTF(f)|^2 S_e(f) \tag{2.13}$$

with $|NTF(f)|^2$ given by Equation 2.12.

The in-band quantization error can be derived for the oversampling and noise shaping converter as:

$$P_q = \int_{-f_b}^{f_b} S_q(f)df = S_e \int_{-f_b}^{f_b} |NTF(f)|^2 df = \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}} \tag{2.14}$$

where S_e is taken from Equation 2.2 and $|NTF(f)|^2$ is taken from Equation 2.12.

Therefore the peak DR of the oversampling and noise shaping converter can be calculated as:

$$DR_{dB} = 10\log\frac{P_x}{P_q} = 6.02N + 1.76dB + 10\log(2L+1) - 9.94L + (2L+1)10\log OSR \tag{2.15}$$

where P_q is the in-band quantization noise power given in Equation 2.14 and P_x is the input signal power.

Figures 2.5 and 2.6 show the plots for Equations 2.12 and 2.15 [2]. The plots show the decreasing noise within the signal band for various orders of the NTF and the improvement in the

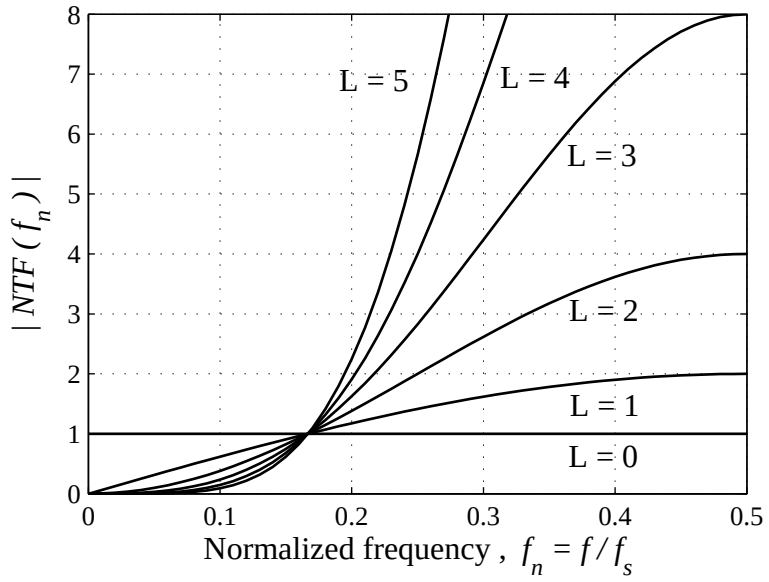


Figure 2.5: Illustration of $|NTF(f_n)|$ for different noise shaping orders(L).

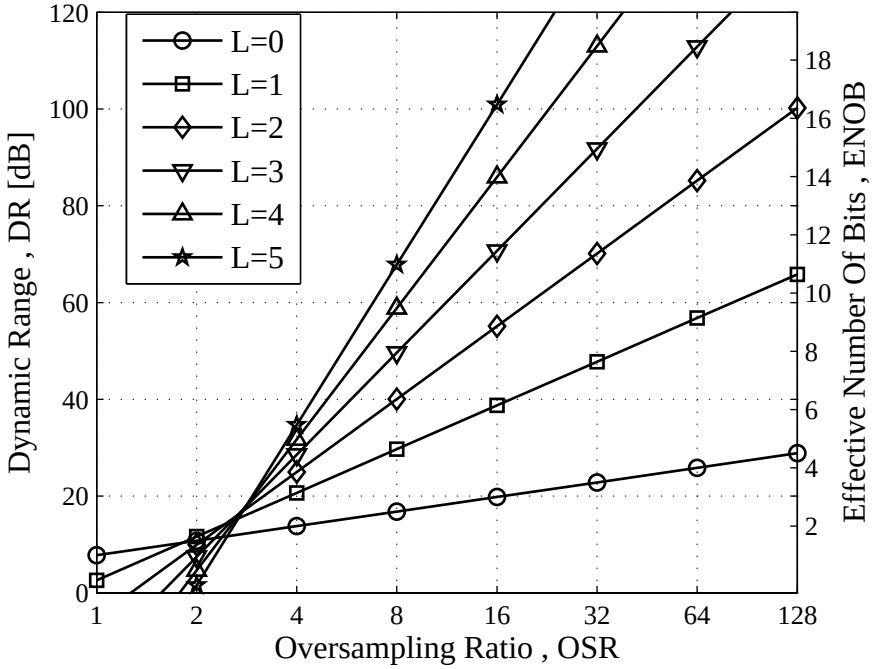


Figure 2.6: DR and ENOB versus OSR for different noise shaping orders of an oversampling(L=0) and oversampling and noise shaping converter.

peak DR for various orders and OSRs. The equation shows that the oversampling technique coupled together with an Lth-order noise shaping can increase the dynamic range of the converter by $3(2L+1)$ dB or $L+0.5$ bits per octave increase in OSR. The equation for a converter without noise shaping can be obtained from Equation 2.15 by setting the value for $L=0$. It is seen that noise shaping coupled with oversampling techniques allows much larger resolution extraction when compared to nyquist rate converters.

2.2.2 Basic ΔΣ Modulator Topology

The process known as oversampling and noise shaping forms the hallmark of ΔΣ converters. In order to achieve noise shaping, the converter must recognize which is the input and which is the noise in the signal band f_b. By introducing a loop filter before the quantizer and introducing feedback in the system as shown in Figure 2.7, the ΔΣ converter presents different signal and noise transfer functions to the input signal and the quantization noise respectively [2].

As shown the in the figure, the basic ΔΣ modulator consists of a loop filter, quantizer and a digital to analog converter inside the feedback loop. The output of the ΔΣ modulator is a B-bit digital stream at f_s sampling rate. The B-bit stream of digital bits is reduced by a digital processing block called the decimator. It reduces the rate of the ΔΣ modulator output bit stream to the nyquist rate while simultaneously increasing the resolution or word length of the converter from B-bits to N-bits.

The decimator in principle consists of a digital filter and a downsampler. The digital filter removes all frequency components outside the band of interest f_b and therefore removes most of the shaped quantization noise power. The ΔΣ block is the most important block as it directly influences the ADC performance directly.

2.2.2.1 Signal Processing in 1^{st}-Order ΔΣ Modulator

Figure 2.8 shows the basic scheme of a ΔΣ modulator [2]. The model shows a feed-forward path consisting of loop filter $H(z)$, a B-bit quantizer and a negative feedback path consisting of a DAC. The system works on the principle of presenting a large gain for H(z) inside the signal band and a small gain outside it. Due to this and the negative feedback, the differences between signals x and y are very small inside the signal band, thus pushing the differences between them to higher frequencies outside the signal band.

The figure also shows the linear model of the ΔΣM in which the DAC is assumed to be ideal and the quantizer has been replaced by a model using additive white noise approximation. The linear system has two input signals $x(n)$, $e(n)$ and one output signal y(n). The summer at the front of the system processes the difference signal between inputs $x(n)$ and $y(n)$. The relation between the three signals can be written in Z domain as shown below:

$$Y(z) = (X(z) - Y(z))kH(z) + E(z) \tag{2.16}$$

$$Y(z)(1 + kH(z)) = X(z)kH(z) + E(z) \tag{2.17}$$

$$Y(z) = X(z)\frac{kH(z)}{(1 + kH(z))} + E(z)\frac{1}{(1 + kH(z))} \tag{2.18}$$

$$Y(z) = H_x(z)X(z) + H_e(z)E(z) \tag{2.19}$$

where H_x is the Signal Transfer Function (STF) and H_e is the NTF given by:

$$H_x = \frac{kH(z)}{(1 + kH(z))} \tag{2.20}$$

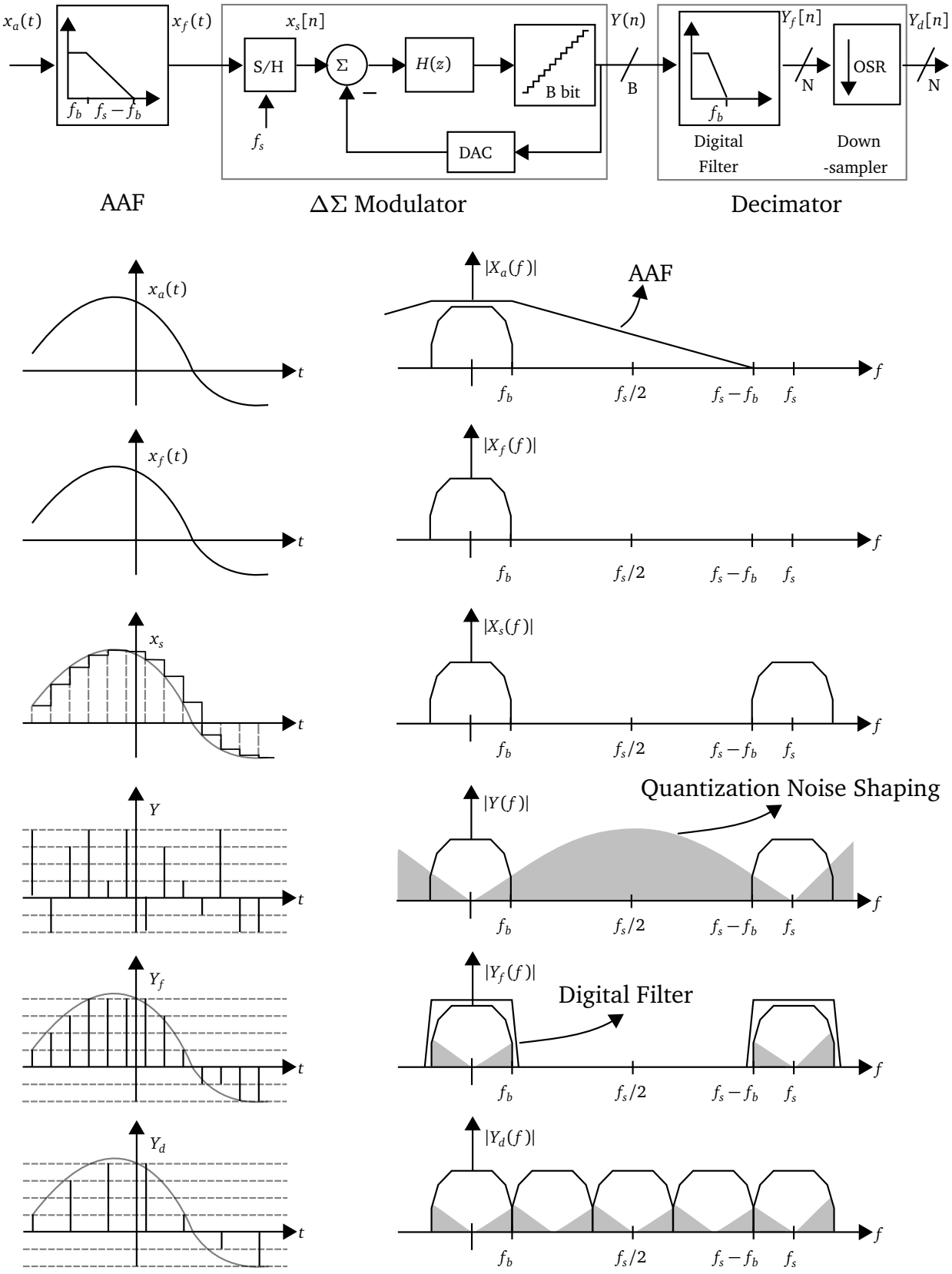


Figure 2.7: Generic $\Delta\Sigma$ architecture showing the various signal processing steps involved in time and frequency domain. AAF denotes anti-aliasing filter and S/H denotes sample and hold.

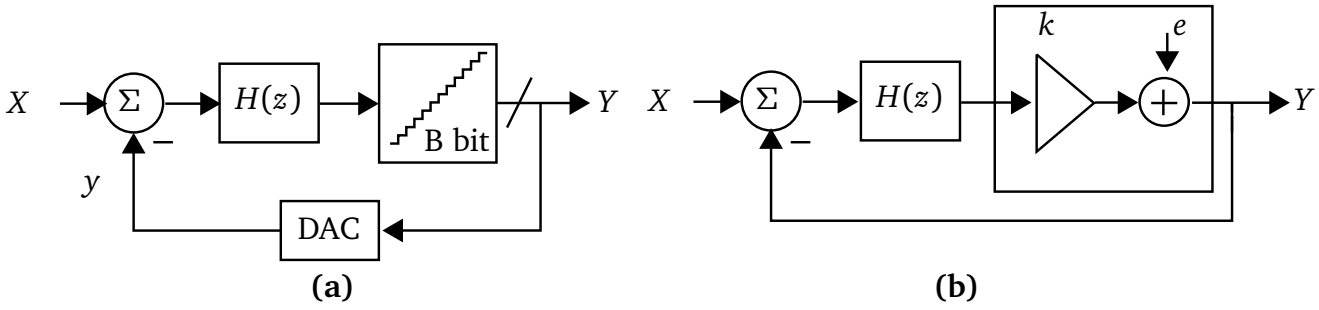


Figure 2.8: Basic scheme and Linear model of the $\Delta\Sigma$ modulator with B-bit quantizer, loop filter H(z) and feedback DAC.

$$H_e = \frac{1}{(1 + kH(z))} \tag{2.21}$$

As seen in Equations 2.20 and 2.21, the STF and NTF are different for the input signal and the error signal. By choosing loop filter H_z properly, input signal X_z through the $\Delta\Sigma$ modulator can be kept unchanged while suppressing noise signal E_z within the signal band f_b. If we assume that the loop filter provides a large gain for the input signal within the signal band and a small gain outside the signal band for out-of-band components then the STF and the NTF become:

$$H_x = \frac{kH(z)}{(1 + kH(z))} \approx 1 \tag{2.22}$$

$$H_e = \frac{1}{(1 + kH(z))} << 1 \tag{2.23}$$

Hence the noise is greatly suppressed while the signal is allowed to pass through relatively unchanged. The easiest loop filter that can implement these functions is a delaying discrete time integrator whose transfer function in the Z domain is given by:

$$H(z) = \frac{z^{-1}}{(1 - z^{-1})} \tag{2.24}$$

Assuming the quantizer gain is unity $k = 1$ yields:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2.25}$$

which is also called a 1st-order $\Delta\Sigma$ modulator referring to the first order noise shaping of the system. The integrator presents a STF which is merely a delay on the input signal while the NTF represents a differentiator which suppresses the noise within the signal band. Figure 2.9 shows loop filter $H(z)$, STF and NTF for the first order modulator [2].

In time domain, the modulator outputs a series of Pulse Density Modulated (PDM) digital signal whose average represent the input signal as shown in Figure 2.10. When the input signal is high the output signal contains higher density of +1's and when the input signal is low the output contains a higher density of -1's.

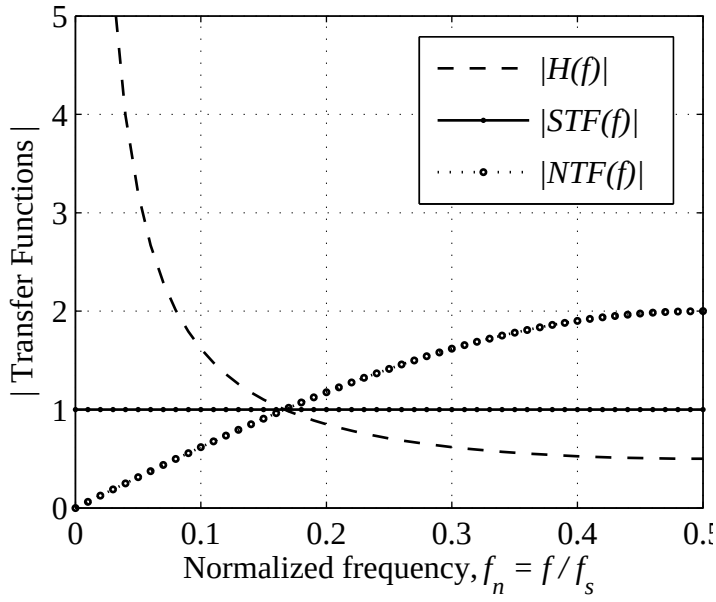


Figure 2.9: Transfer function H(f), STF(f) and NTF(f) of a first order modulator.

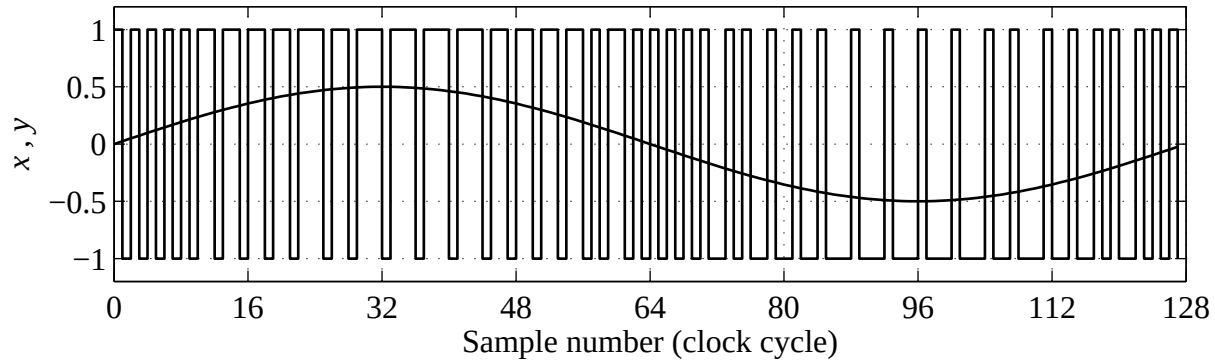


Figure 2.10: Time domain behavior of a first order $\Delta\Sigma$ modulator to a sinusoidal input signal with 1-bit quantizer.

2.3 Performance Metrics of $\Delta\Sigma$ Modulator

ADCs are evaluated against a set of standards which define how they perform in the presence of noise and non-idealities [2, 3]. For $\Delta\Sigma$ modulators the main parameters which define performance are:

- **Signal to Noise Ratio (SNR)**. It is the ratio of the output power at the frequency of the input signal to the uncorrelated in-band noise power. Noise sources in the modulator come from non-idealities of the circuits used to implement the modulator, quantization noise and other sources excluding harmonics and DC. It is the measure of linear performance of the modulator. SNR, taking into account just the quantization noise, is also sometimes referred to as Signal to Quantization Noise Ratio (SQNR). The SNR of the modulator can be given by:

$$SNR|_{dB} = 10\log\left(\frac{A^2}{2P_q}\right) \tag{2.26}$$

where A is the amplitude of the input signal and P_q is the quantization noise power.

- **SNDR**. The SNDR also called SINAD is the ratio of the signal power at the frequency of the input signal to the in-band noise including distortion and excluding DC. It is a measure of the dynamic performance of the modulator and its ability to suppress harmonics.

- **Dynamic Range (DR)**. It is defined as the ratio of the output power at the frequency of input signal with maximum amplitude to the output power at the frequency of the input signal for which $SNR = 0dB$. The DR defines the resolution of the converter and in an ideal case the input signal with amplitude of $X_{FS}/2$ will provide a output signal covering the full scale of the $\Delta\Sigma$M quantizer.

$$DR|_{dB} = 10\log\left[\frac{(X_{FS}/2)^2}{2P_q}\right] \tag{2.27}$$

- **Effective Number of Bits (ENOB)**. The DR defines the maximum resolution of the converter. Since the DR for the N-bit nyquist converter is given by: $6.02N + 1.76$, rearranging the DR equation for a nyquist converter yields the relation:

$$ENOB = \frac{DR|_{dB} - 1.76}{6.02} \tag{2.28}$$

where the ENOB represents the resolution needed by the $\Delta\Sigma$ converter to achieve the same DR as the nyquist converter.

- **Overload Level,** X_{OL}. In an ideal modulator the SNR increases monotonously for the input amplitudes in the range $[0, X_{FS}/2]$ where X_{FS} stands for the quantizer full scale. However in practice the quantizer overloads or starts to saturate at values close to $X_{FS}/2$ which causes an increase in the in-band error and a decrease in the peak SNR of the modulator. The value of the input level ($X_{OL} < X_{FS}/2$) at which this happens is called the overload level. Figure 2.11 shows the typical DR, SNR and SNDR curves as a function of the input signal amplitude X [2].

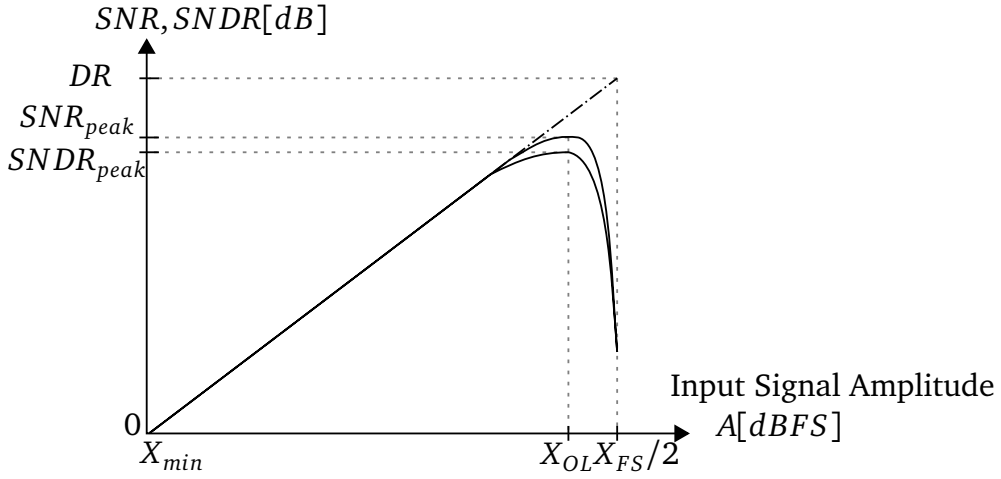


Figure 2.11: Performance metrics curves for a typical $\Delta\Sigma$ modulator.

2.4 Ideal Performance of $\Delta\Sigma$ Modulator

In the previous section, the basics of the $\Delta\Sigma$ modulator were given. The noise shaping characteristics of 1st-order $\Delta\Sigma$ modulator with 1-bit quantizer were illustrated. The discussion on the 1st-order noise shaping and 1-bit quantizer can be extended to the DR of a more general Lth-order and B-bit embedded quantizer based $\Delta\Sigma$ modulator as:

$$DR_{dB} \approx 10\log\left(\frac{3}{2}(2^B-1)^2.\frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}\right) \tag{2.29}$$

The equation shows that the DR of the modulator can be increased by increasing the order L, increasing the OSR and/or increasing the resolution B of the internal quantizer. The effect of increasing and decreasing these parameters on the DR is discussed below.

- **Increasing the order L** substantially improves the DR of the modulator due to increased attenuation of noise in the signal band and high pass filtering resulting from the NTF. The increase in the DR for each step increase in the order of the modulator can be written as:

$$\Delta DR_{dB} \approx 10\log\left[\frac{2L+3}{2L+1}.\left(\frac{OSR}{\pi}\right)^2\right] \tag{2.30}$$

  which states that for each step increase in modulator order the increase in the DR is dependent on the order L and the OSR. Assuming $L = 3$ and $OSR = 32$, the increase in the DR of a 4th-order modulator is found to be 21.3dB or 3.5bits. The calculation however does not take into account the stability considerations of higher order loops which usually prevent the modulator from reaching this increase in resolution.

- **Increasing the OSR** leads to direct reduction of the in-band quantization error as the overall noise power is spread over a wider sampling frequency band. Calculating the increase in DR for each doubling of the OSR leads to the equation:

$$\Delta DR_{dB} \approx 3(2L+1) \tag{2.31}$$

  which states that the DR increase for each doubling of the OSR is dependent only on the modulator order and not on the OSR itself. The expected increase in DR was already stated in the previous section which gave an increase of 3(2l+1)dB/octave for a Lth-order modulator. In practice the effect of increasing OSR translates to increased bandwidth requirements from the operating circuitry which leads to increased power consumption.

- **Increasing the quantizer resolution B** leads to an increase in DR of approximately 6dB (1bit) per extra bit in the quantizer. The DR increases because the in-loop feedback DAC, which usually has the same resolution as that of the quantizer, produces signal y which has a reduced step difference compared to input signal x. This leads to better tracking of the input signal by the $\Delta\Sigma$ modulator which pushes the quantization noise away from the signal band to higher frequencies. The increase in the DR for each additional bit increase in quantizer resolution can be written as:

$$\Delta DR_{dB} = 20\log\left(\frac{2^{(B+1)}-1}{2^B-1}\right) \tag{2.32}$$

which shows the improvement in DR to be independent of the modulator order and the oversampling ratio OSR. In practice however the increase in DR by increasing the quantizer resolution does not happen due to the presence of the multi-bit DAC which is present in the in-loop feedback of the modulator and whose non-linearities are added directly to the modulator input resulting in loss of resolution. In order to achieve a high resolution at modulator output, the linearity of the multi-bit DAC needs to reach the same resolution as that of the overall modulator.

Figure 2.12 shows the dependence of the DR and ENOB on the OSR of the modulator for various orders [2]. It is seen clearly that the increase in the DR for quantizer resolution above $B = 2$ is much less pronounced and the maximum difference occurs for change in quantizer resolution fronm $B = 1$ to $B = 2$.

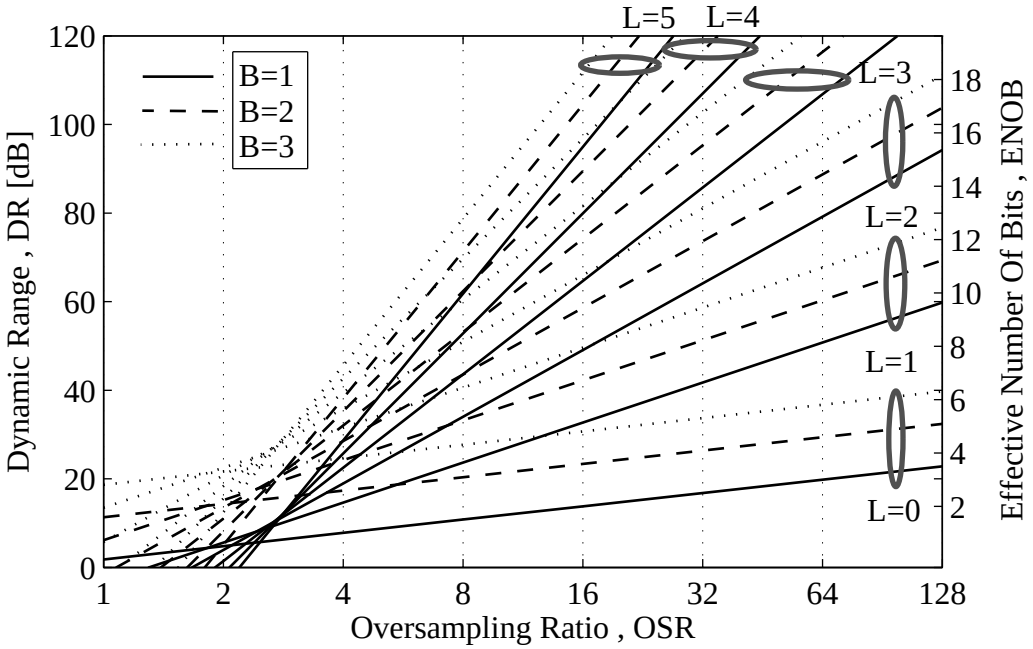


Figure 2.12: DR and ENOB versus the OSR for an ideal $\Delta\Sigma$ modulator with 1-bit,2-bit and 3-bit quantizers.

2.5 Types of $\Delta\Sigma$ Topologies

Previous sections introduced various strategies to improve the DR of the modulator. The strategies can be combined in a myriad of ways, leading to vastly different $\Delta\Sigma$ architectures. Various classifications exist according to which the modulators can be grouped, namely:

- The type of signal being converted: low-pass or band-pass.
- Implementation of loop filters: Traditional modulators used DT loop filters $H(z)$ to achieve noise reduction. Of late, Continuous-Time (CT) modulators are also implemented using CT loop filters but using discrete time quantizers.
- Number of stages/quantizers involved: Traditional topologies used single loop/single bit to convert the input signal. However in recent years multistage $\Delta\Sigma$ modulators using multi-bit quantizers have made their appearance.

- Types of circuitry involved: Most DT implementations use SC circuits but modulators are also designed using Switched-Current (SI) circuits.

Describing all topologies is beyond the scope of this thesis. Instead the thesis focuses on the topologies involving low-pass DT $\Delta\Sigma$modulators using SC techniques to which the thesis results contribute.

2.5.1 Single Loop $\Delta\Sigma$ Topology

The basics and fundamentals of $\Delta\Sigma$ modulators have already been discussed in previous sections. The architecture of the 1st-order modulator with 1-bit internal quantizer and its operation were presented in Section 2.2.2. It is the simplest architecture which however finds limited use in practice due to higher correlation of quantization noise with input signal. This section discusses higher order modulators with a single bit quantizer called single-loop $\Delta\Sigma$ modulators.

2.5.1.1 Second Order $\Delta\Sigma$ Modulator

The single loop second order modulator is an extension of the 1st-order modulator, wherein the quantizer is replaced by another 1st-order modulator resulting in two loop filters connected in series. Figure 2.13 shows such a modulator.

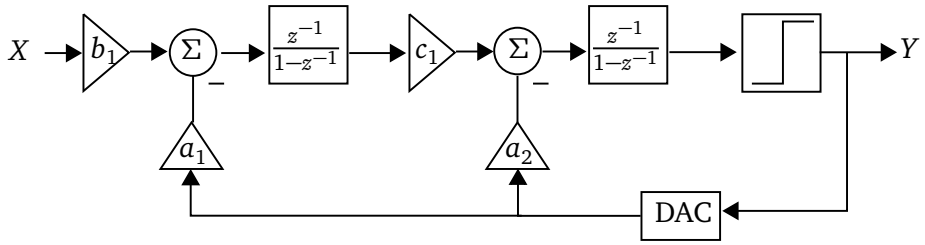


Figure 2.13: Second-order $\Delta\Sigma$ modulator with 1-bit quantizer using two delaying integrators.

Assuming white noise approximation and taking the linear model for the 1-bit quantizer we can write the relation between the input signal and the output signal as:

$$Y(z) = \frac{b_1 c_1 k z^{-2} X(z) + (1-z^{-1})^2 E(z)}{1 + (a_2 k - 2)z^{-1} + (1 + a_1 c_1 k - a_2 k)z^{-2}} \tag{2.33}$$

wherein to get 2nd-order NTF the previous equation must fulfill certain conditions namely:

$$\left.\begin{aligned} a_1 c_1 k &= 1 \\ a_2 &= 2 a_1 c_1 \\ a_2 k &= 1 \end{aligned}\right\} \tag{2.34}$$

Under these conditions and applying the usual case of equal gains for inputs $a_1 = b_1$, the output of the modulator becomes:

$$Y(z) = z^{-2} X(z) + (1-z^{-1})^2 E(z) \tag{2.35}$$

The conditions shown previously define the relationships between various coefficients and do not give the value themselves. The selection of coefficient values generally involve various tradeoffs at the circuit level, technology level and architectural level to ensure stability, increase in the overload level X_{OL}, reduction of the signal swing at integrator outputs, reduction of the overall power/area and matching of coefficients at the layout level. Compared to a first-order modulator the DR of the second-order modulator increases by 15 dB for each doubling of OSR. Additionally the sampling frequency needed to achieve the same level of DR as a first order modulator is substantially reduced by more than a factor of 10, which results in practically realizable circuits.

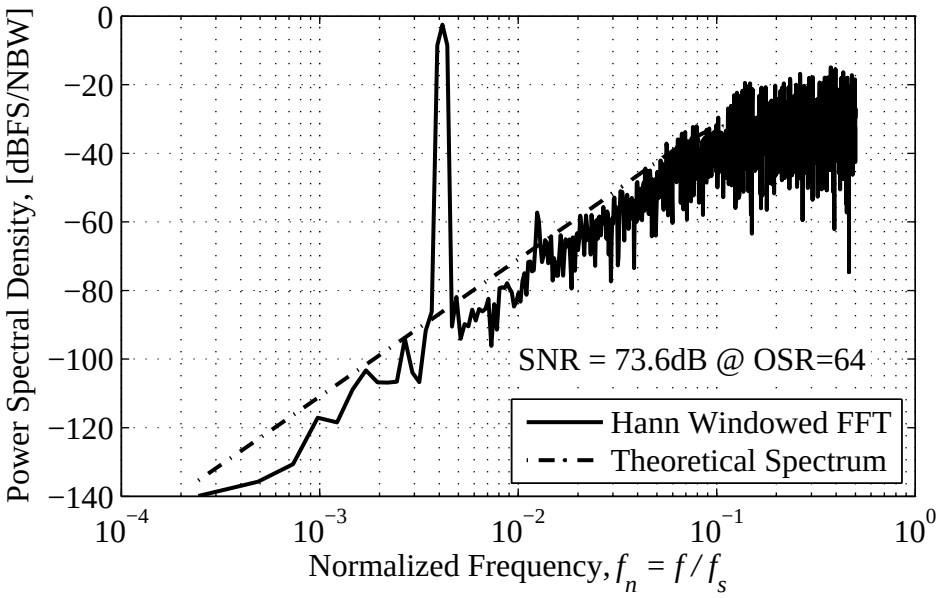


Figure 2.14: Power spectral density of a second-order modulator for a -3 dBFS input at OSR=64.

Figure 2.14 shows the example spectrum of a second order modulator for a -3 dBFS input signal, sampling at an OSR of 64 and having coefficients $b_1 = c_1 = a_1 = a_2 = 0.5$. The figure demonstrates the noise shaping in the modulator where the noise is being pushed away from the signal band to higher frequencies.

2.5.1.2 Higher Order $\Delta\Sigma$ Modulator

Higher order modulators can be constructed in a manner similar to the second order modulator by replacing successively the quantizer block in the first order modulators to form a long chain of filters $H(z)$. Figure 2.15 shows such a modulator which has the order L and uses a 1-bit quantizer at the end.

Analyzing the Lth-order modulator using the linear model as before, the output can be shown to be:

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^{L}E(z) \tag{2.36}$$

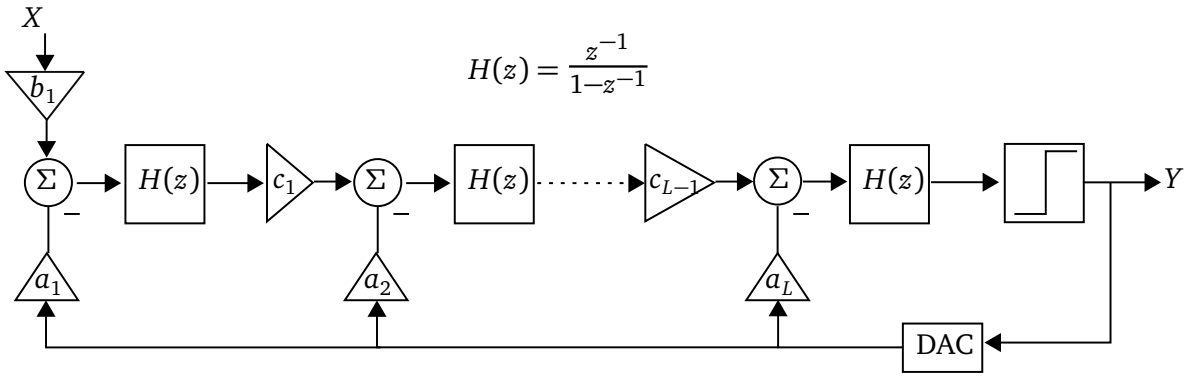


Figure 2.15: Lth-order ΔΣ modulator with 1-bit quantizer using L delaying integrators.

by satisfying the various conditions between the integrator coefficients similar to the 2nd-order modulator. For a single bit quantizer with B=1, the in-band error power is given by Equation 2.14 and the SNR and DR for this modulator are given by:

$$SNR_{dB} = 10(2L+1)\log OSR + 10\log\left(\frac{3}{2}\right) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) - 20\log\left(\frac{\Delta}{2A}\right) \tag{2.37}$$

$$DR_{dB} = 10(2L+1)\log OSR + 10\log\left(\frac{3}{2}\right) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) \tag{2.38}$$

The above equations state that the DR of the Lth-order modulator increases by 3(2L+1) dB for each doubling of the OSR. The previous equations for Lth-order modulator are under assumptions of ideal conditions, which in practice is not achievable. This is because as the number of loops increase, the input to the quantizer becomes large making it saturate. This can be seen by taking the equation for the quantizer input:

$$I(z) = STF(z)X(z) + (NTF(z) - 1)E(z) \tag{2.39}$$

where $(NTF(z) - 1)$ is the gain of the error signal.

As the number of the loops increase in the modulator the NTF while reducing the gain for low frequency components also presents increasingly higher gains for high frequency components of the error signal. This makes the small values of the error signal amplify quickly, saturating the quantizer input and introducing instability in the ΔΣ modulator. Hence in the design of higher order single loop ΔΣ modulators, various design techniques such as optimization of the NTF through optimal distribution of the NTF zeroes, placing signal limiters for the loop filters so that they do not exceed their safe operating limits must be used. By properly choosing coefficients of the integrator and automatically resetting the integrator on detection of instability, the modulator can be made stable across the entire input range. Although a generalized stability condition for higher order modulators has not been derived, higher order modulators have been successfully designed since the late 1980s.

2.5.2 Cascade Topology

The previous section introduced higher order single loop modulators. However as stated these higher order modulators pose more stringent design requirements in order to guarantee stability

while providing DR and SNR far from that of an ideal modulator. Hence as an alternative to implementing higher order modulators using single loops, the so-called Multi-Stage Noise Shaping (MASH) $\Delta\Sigma$ modulator architectures were introduced. These architectures, also referred to as cascade or multi-stage $\Delta\Sigma$ modulators, allow higher order noise shaping for quantization noise while preventing any instability concerns. As the name suggests, the modulator is built of a series of cascade of lower order modulators whose outputs are combined together to perform higher order noise shaping.

Figure 2.16 shows the generic scheme of cascade topology [2]. It consists of N stage cascade with each stage providing L_ith-order noise shaping. The first stage processes the input signal and the following stages process quantization noise of the previous stage. The outputs of all stages are subsequently passed through digital filters in order to cancel the quantization noise of all stages except the last one. The quantization error that enters the last stage is already processed by the preceding stages, hence when the quantization noise passes through the final stage, it is shaped by the NTF of order L.

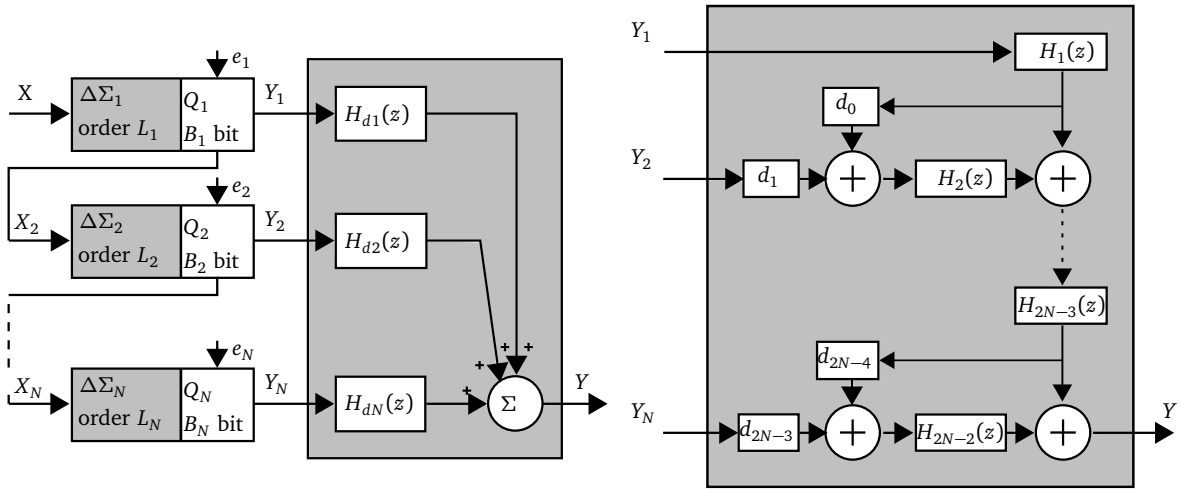


Figure 2.16: Generic N-stage cascade $\Delta\Sigma$ modulator and the structure of the digital cancellation logic.

The biggest advantage of this topology is evident from the fact that no feedback loop exists for the overall modulator but rather loops exist only for the stages used in the cascade. Hence the stability of the complete modulator is determined by the highest order modulator used in the cascade. Using modulators of order $L \leq 3$ for the cascade stages would result in a design that is unconditionally stable and provides higher order noise shaping with a performance comparable to that of an ideal modulator.

For an N stage cascade, by means of adequately processing the signal in digital domain results in the output signal:

$$Y(z) = STF(z) + NTF_N(z)E_N(z) = z^{-L}X(z) + d_{2N-3}(1-z^{-1})^L E_N(z) \tag{2.40}$$

where $L = L_1 + L_2 + ...L_N$ and d_{2N-3} is a scaling factor necessary to prevent overloading of the succeeding stages of the cascade. The total in-band quantization error of this cascade can be written as:

$$P_q \cong d_{2N-3}^2 \cdot \frac{\Delta_N^2}{12} \cdot \frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}} \tag{2.41}$$

with Δ_N being the quantization step of the last stage quantizer. The performance is similar to that of an Lth-order modulator, except for the scaling factor d_{2N-3} that increases noise in in-band frequencies. However this increase in noise is considerably lower than that resulting from optimized higher order single loop modulators. These benefits have led to the development of a large number of cascade $\Delta\Sigma$ modulators in various configurations.

2.5.2.1 Fourth Order Cascade

Figure 2.17 shows the topology of a 4th-order cascade $\Delta\Sigma$ modulator built from two 2nd-order single loop single bit topologies described previously [3]. The relationship between the various coefficients in a second-order modulator was derived in Equation 2.34. Applying those equations to the two second-order modulators found in the 4th-order cascade topology results in:

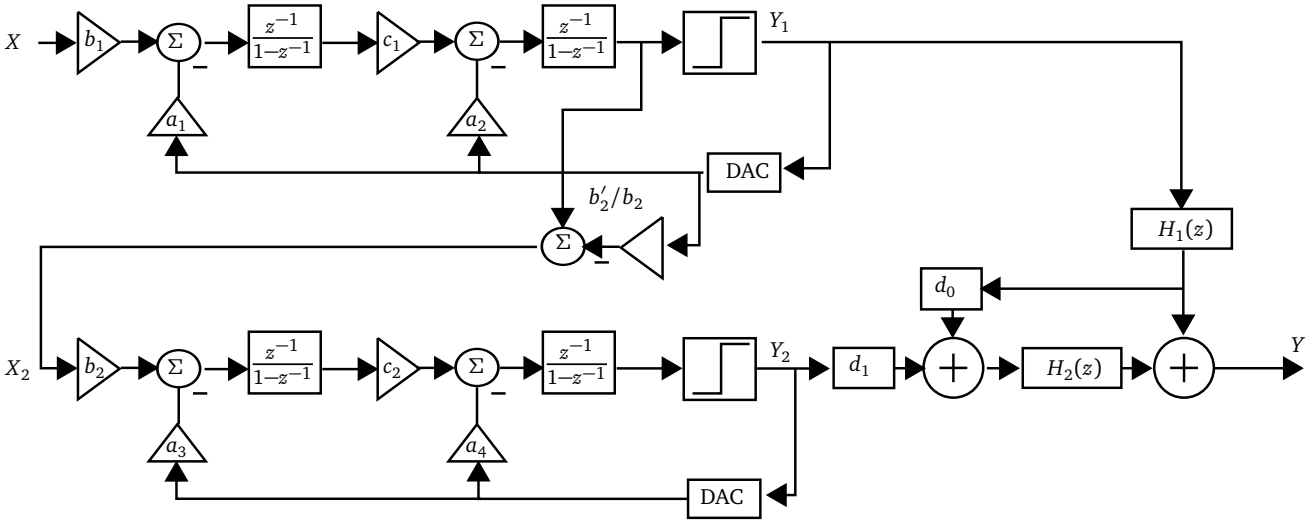


Figure 2.17: 4th-order cascade $\Delta\Sigma$ modulator with 1-bit quantizer.

$$Y_1(z) = \frac{b_1}{a_1} z^{-2} X(z) + (1 - z^{-1})^2 E_1(z) \tag{2.42}$$

$$Y_2(z) = \frac{b_2}{a_3} z^{-2} X_2(z) + (1 - z^{-1})^2 E_2(z) \tag{2.43}$$

where $Y_1(z)$ and $Y_2(z)$ are the modulator outputs going into the digital cancellation filters and X_2 is the second stage input given by:

$$X_2(z) = \left(a_1 c_1 - \frac{b_2'}{b_2} \right) Y_1(z) - a_1 c_1 E_1(z) \tag{2.44}$$

The outputs of the two second order modulators is processed using the digital cancellation filters to cancel the first stage noise completely as:

$$Y(z) = H_{d1}(z) Y_1(z) + H_{d2}(z) Y_2(z) \tag{2.45}$$

with functions and coefficients of the digital cancellation logic given by:

$$\left.\begin{aligned} H_{d1}(z) &= H_1(z)[1+d_0H_2(z)] = z^{-2}\left[1+\left(\frac{b_2'}{a_1c_1b_2}-1\right)(1-z^{-1})^2\right] \\ H_{d2}(z) &= d_1H_2(z) = \frac{a_3}{a_1c_1b_2}(1-z^{-1})^2 \\ d_0 &= \frac{b_2'}{a_1c_1b_2}-1 \qquad d_1 = \frac{a_3}{a_1c_1b_2} \qquad H_1(z) = z^{-2} \qquad H_2(z) = (1-z^{-1})^2 \end{aligned}\right\} \tag{2.46}$$

Applying the digital cancellation logic to the Equation 2.45 results in the output of the modulator as:

$$Y(z) = \frac{b_1}{a_1}z^{-4}X(z) + d_1(1-z^{-1})^4E_2(z) \tag{2.47}$$

which is similar to that of an ideal fourth order modulator that is unconditionally stable by design. The performance of this cascade modulator will be equal to that of an ideal modulator if $d_1 = 1$ is chosen. However, choosing $d_1 = 1$ usually results in larger peak to peak output swings of the integrator due to its dependence on the integrator coefficients. Hence a balance must exist in the choice of integrator coefficients so as to increase the overload level, and SNR while choosing a value for d_1 such that the increase in the noise of the modulator due to $d_1 > 1$ is not excessive.

Table 2.1 depicts some of the values for the integrator coefficients and digital cancellation logic chosen to design a 4th-order (2-2) cascade modulator. Many other high order architectures based on cascade topology have been reported in literature, such as three stage 4th order cascade (2-1-1 $\Delta\Sigma$M)[4], three stage 5th-order cascade (2-2-1 $\Delta\Sigma$M)[5], four stage 5th order cascade (2-1-1-1 $\Delta\Sigma$M)[6] and three stage 6th-order cascade (2-2-2 $\Delta\Sigma$M)[7].

Table 2.1: Coefficients reported for 4th-order cascade $\Delta\Sigma$M

Coefficients	[8]	[9]	[9]
b_1, a_1	0.25,0.25	0.5,0.5	0.5,0.5
c_1, a_2	0.5,0.25	0.5,0.5	0.5,0.5
b_2, b_2', a_3	0.5,0.125,0.25	1,0.5,0.5	0.5,0.25,0.5
c_2, a_4	0.5,0.25	0.5,0.5	0.5,0.5
d_0, d_1	1,4	1,2	1,4
ΔSNR (dB) comparing to ideal	-12	-6	-12
$X_{OL}/(\Delta/2)$ (dBFS)	-2	-5	-2

Cascade topology offers higher order noise shaping and in theory can be extended to any order with any number of stages. But practical circuit limitations prevent these higher order modulators from realizing their true performance. This is due to the imperfect or imprecise values of design coefficients, which results in ineffective cancellation of the noise present in intermediate stages by the digital cancellation logic and causes noise leakages of lower order to appear at the output.

2.5.2.2 L-0 Cascade

The cascade topology can not only be used to build architectures consisting of solely lower order $\Delta\Sigma$ modulators with smaller quantizers, but can also be used to combine lower order modulators with 1-bit quantizers and nyquist rate converters. The main idea behind this combination is to combine the advantages of noise shaping and linearity of 1-bit quantizers found in $\Delta\Sigma$ modulators with the lower quantization error found in nyquist rate B-bit quantizers. This sort of topology was first proposed by Leslie and Singh and is called L-0 cascade $\Delta\Sigma$ modulator [10], where L is the order of the first stage $\Delta\Sigma$ modulator and 0 refers to the nyquist converter. Figure 2.18 shows the general scheme of this L-0 cascade modulator [2].

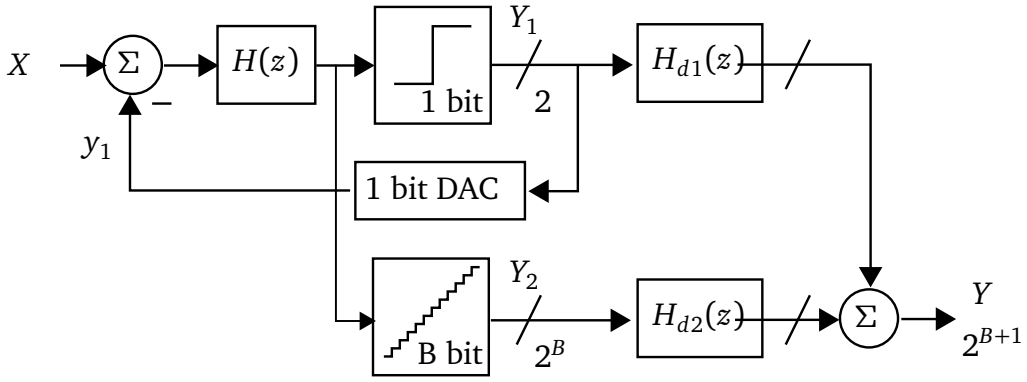


Figure 2.18: Leslie-Singh $\Delta\Sigma$ modulator with 1-bit and multi-bit quantizer.

Analogous to the previous case, the two outputs are combined using a digital cancellation logic to produce a lower error at the output within the signal band. Considering a second-order modulator for the first stage we can write the outputs as:

$$Y_1(z) = \frac{b_1}{a_1} z^{-2} X(z) + (1 - z^{-1})^2 E_1(z) \tag{2.48}$$

$$Y_2(z) = (-E_1(Z) + E_2(z)) z^{-k} \tag{2.49}$$

where z^{-k} is the overall delay of the second stage multi-bit quantizer and $E_2(z)$ is the second stage quantization error. The two outputs can be combined in the digital cancellation logic as:

$$\begin{aligned} Y(z) &= H_{d1}(z) Y_1(z) + H_{d2}(z) Y_2(z) \\ &= H_{d1}(z) \frac{b_1}{a_1} z^{-2} X(z) + \left[H_{d1}(z)(1 - z^{-1})^2 - H_{d2}(z) \right] E_1(z) + H_{d2}(z) E_2(z) \end{aligned} \tag{2.50}$$

where the digital filters should satisfy the conditions $H_{d1}(z) = z^{-k}$ and $H_{d2}(z) = z^{-k}(1 - z^{-1})^2$ respectively to get the final output as:

$$Y_1(z) = z^{-k} \left[\frac{b_1}{a_1} z^{-2} X(z) + (1 - z^{-1})^2 E_2(z) \right] \tag{2.51}$$

where the error term $E_2(z) << E_1(z)$ due to the use of the multi-bit quantizer. Thus the Leslie-Singh architecture combines the benefits of single bit lower order modulators with high resolution multi-bit quantizers. This architecture provides the benefits of multi-bit quantizers without

the need of multi-bit DACs in the feedback path which as in the later section is shown to need additional correction techniques to maintain high resolution. Different variations of this architecture utilizing the general Leslie-Singh principle were successfully implemented and verified [11, 12].

2.5.3 Multi-Bit Topology

The previous architectures discussed so far have used increase in OSR or increase in order L to improve the DR and SNR of the modulator. However the increase in the performance for higher order modulators is often limited or vanishes due to instabilities of single loops or due to noise leakages in cascade modulators. In the cascade modulators the concept of using higher resolution quantizers to reduce the noise was introduced. The L-0 cascade used higher B-bit quantizers for second stage and single-bit quantizer for the first stage to decrease the overall noise. As per the DR equation for Lth-order modulators, it is possible to use multi-bit quantizers instead of single-bit quantizers to improve the modulator performance. The main advantages of this approach are:

- decrease of 6dB in the quantization noise power for every additional bit increase in the embedded quantizer due to the smaller quantization step of the quantizer
- better fitting to the additive white noise approximation of quantization error when compared to single-bit quantizer.
- increased loop stability due to smaller quantization step size allowing for aggressive noise shaping.
- well defined quantizer gain allowing an increased overload level.
- nonlinear dynamics of modulators such as idle tones are much less pronounced due to weaker quantizer non-linearity.
- better suited for wide band applications due to the reduction in OSR obtained by using multi-bit quantizers leading to lower sampling frequency and power consumption.

Although multi-bit quantizers present many advantages they also come with some disadvantages namely:

- increase in the analog circuitry which requires more area and power and is difficult to design.
- requirements of a multi-bit DAC in the feedback path which unlike the 1-bit quantizer is not intrinsically linear due to the presence of component mismatch leading to non-linearities, errors and harmonics in the output of the modulator.

Figure 2.19 shows the general architecture and linear model of a multi-bit topology. Compared to the 1-bit quantizer model, this topology adds additional errors related to multi-bit conversion, namely: conversion errors coming from the ADC represented by e_{ADC} and conversion errors coming from the DAC represented by e_{DAC}. Deriving the relationship between the input and output in the z-domain results in:

$$Y(z) = \frac{kH(z)}{1+kH(z)}[X(z) - E_{DAC}(z)] + \frac{1}{1+kH(z)}[E(z) + E_{ADC}(z)] \tag{2.52}$$

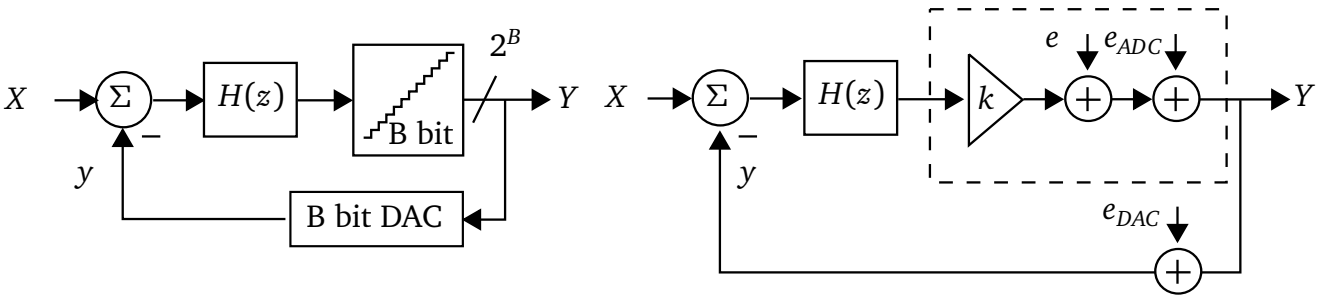


Figure 2.19: General scheme and linear model of $\Delta\Sigma$ modulator with B-bit embedded quantizer and B-bit feedback DAC.

which shows that errors added by the DAC are not noise shaped by the modulator and appear directly at the output leading to decrease in the DR of the entire system. Hence any non-linearities present in the feedback DAC causes distortion at the modulator output which necessitates an additional requirement in the multi-bit topologies namely:

- the multi-bit DAC should have the same linearity and resolution as that of the entire modulator. That is if the entire modulator needs to have N-bit resolution then the multi-bit DAC should also have the capacity to reach this N-bit resolution.

It is important to note that the above requirement only applies if the multi-bit DAC is used as feedback to feed the input of the first stage integrator. If the multi-bit quantizer is used to feed the second integrator or the second stage in the cascade topology, then the requirements on the linearity of the feedback DAC are not so stringent. This is because the non-linearity in the multi-bit DAC is noise shaped by the preceding integrators which leads to very little distortion appearing at the output.

Figure 2.20 shows the general implementation scheme for multi-bit quantizers and multi-bit DAC. As the number of bits usually employed in multi-bit topologies in less ($B \leq 6$), a full parallel implementation is used to derive the ADC and DAC outputs. This is done as follows:

- **For the ADC**: Utilizing a bank of $2^B - 1$ comparators (flash ADC) to generate thermometer code by digitizing the outputs of the loop filter and then passing it through a thermometer to binary conversion block to generate binary coded digital outputs.
- **For the DAC**: Utilizing a bank of $2^B - 1$ unitary elements (resistors, capacitors, current sources etc.) to generate the feedback analog signal by summing up their outputs and generating a signal equivalent to the ADC output.

2.5.3.1 Multi-Bit Correction Techniques

As stated previously, the use of multi-bit quantizers in $\Delta\Sigma$ modulators require multi-bit DAC which has the same resolution as that of the entire modulator. This is because DAC errors appear directly at the output without being noise shaped. The errors in the feedback DAC arise from the mismatch between unitary elements. Any variations between them cause imprecise analog levels to be generated which are then added to the output through the in-loop feedback summing node. In current technologies, as the size of unitary elements increases, the matching

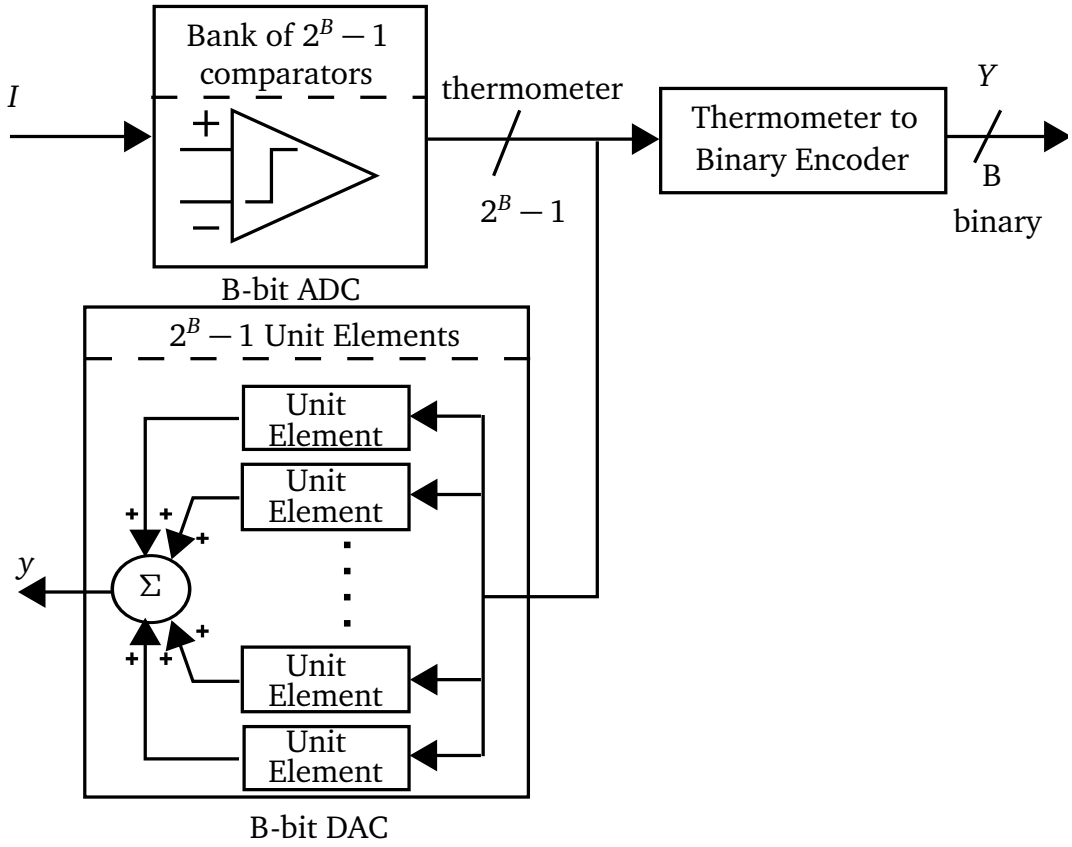


Figure 2.20: Internal architecture of a general B-bit parallel ADC and DAC in a $\Delta\Sigma$M.

between them also improves due to a lower mismatch factor. Hence it is possible to implement high resolution $\Delta\Sigma$ modulators with greater than 16 bits of linearity using larger unitary elements in the feedback DAC at the expense of increase in area. However if lower area is needed then one of the several alternatives stated below to improve the DAC linearity must be employed:

- Using dynamic or factory trimming of unitary elements after fabrication: This is a straight forward method wherein unitary elements are trimmed to the design values by lasers or by connecting on and off parallel and/or series combination of smaller elements to get a unitary element. This increases the costs due to the need of additional area for implementing dynamic trimming or additional fabrication/measurement steps.

- Using dual quantization techniques: This technique was already introduced in the Leslie-Singh architecture, wherein benefits of single-bit quantizer and multi-bit quantizer were combined to produce lower error at the output. A similar extension can be applied for multi stage or higher order loops where multi-bit quantizer and multi-bit DAC can be used to feed the second stage or higher integrators. This results in non-linearity of the multi-bit DAC being noise shaped by the preceding integrator stages.

- Using Dynamic Element Matching (DEM): This technique relies on randomizing fixed errors in the multi-bit DAC for each thermometer code, by selecting different unitary element combinations for the same thermometer code. Selecting different combinations of unitary elements for the same thermometer code results in fixed errors associated with each code transforming into time varying errors. Hence the average DAC error for each thermometer

code spread over time is the same, which in frequency domain translates to conversion of low frequency static DAC errors into wide-band white noise. This white noise can then be filtered and removed by the decimation filter. The effectiveness of the DEM depends on the type of the algorithm which is broadly classified into:

  - randomization algorithms where unitary elements paths are selected randomly to uncorrelate the DAC output with the thermometer code [13].
  - rotational algorithms where unitary elements are selected in a periodic fashion and not in some random fashion such as clocked averaging algorithm [14].
  - mismatch shaping algorithms where unitary elements are selected so as to shape the mismatch out of the signal band into higher frequencies such as data-weighted averaging [15], individual level averaging [16] and data-directed scrambling [17].

- Using digital calibration or correction of DAC non-linearities: This technique relies on calibrating the multi-bit DAC to determine where the non-idealities exist and correcting them using look-up tables in the digital domain. Acquiring digital equivalents of actual DAC values is done in the foreground or background mode [18, 19].

2.6 Low Voltage/Low Power Design Techniques for $\Delta\Sigma$ Modulators

The previous sections introduced the concept of $\Delta\Sigma$ modulators. Various architectures and strategies to improve the DR were presented. Ever since its introduction as a basic building block, Op-Amps have been used to build the vast majority of analog circuits in literature. This is due to the fact that a variety of topologies exist for Op-Amps, which can be tailored according to the needs of the application. Hence the vast majority of $\Delta\Sigma$ topologies continue to use the Op-Amp as their core building blocks to build the integrators for loop filters.

As technology scaled however, it bought with it lower supply voltages, increased parasitic effects and non idealities which proved not as beneficial for the Op-Amps. The decrease in supply voltage made the usage of Op-Amp configurations such as cascode and telescope difficult due to the reduction in available voltage swings. Designers relied more on the classic two stage and cascade topology of the Op-Amps to achieve their design requirements of high gain and low noise using large transistors and higher currents. However this also bought stability issues to the forefront which are more stringent in cascade topologies, necessitating the use of larger compensation capacitors. The increase in compensation capacitors in turn affected the achievable bandwidth due to the dependence of Op-Amps on fixed gain-bandwidth product. Hence various design approaches were developed for low voltage regimes to overcome difficulties associated with the use of Op-Amps. While some of topologies such as reset Op-Amp, switched-RC and switched-Op-Amp are used to tackle problems coming from the CMOS switches, this section will focus more on introducing alternate/replacement designs for Op-Amp based integrator circuits in $\Delta\Sigma$ modulators.

2.6.1 Dynamic Amplifiers

SC circuits based on dynamic amplifiers were introduced in the early eighties and were proposed as replacements to Op-Amps to reduce static power consumption and noise [20][21][22]. Figure 2.21 shows the architecture of a dynamically biased amplifier integrator and its clocking

scheme. The basic idea in this architecture is to dynamically bias the amplifier to provide higher currents during the charge transfer phase when the sampled input voltage on the sampling capacitor is transferred to the integration capacitor. This dynamic adjustment of current flowing through the amplifier which is directly related to the value of the input signal allows improved transient and settling response from the amplifier.

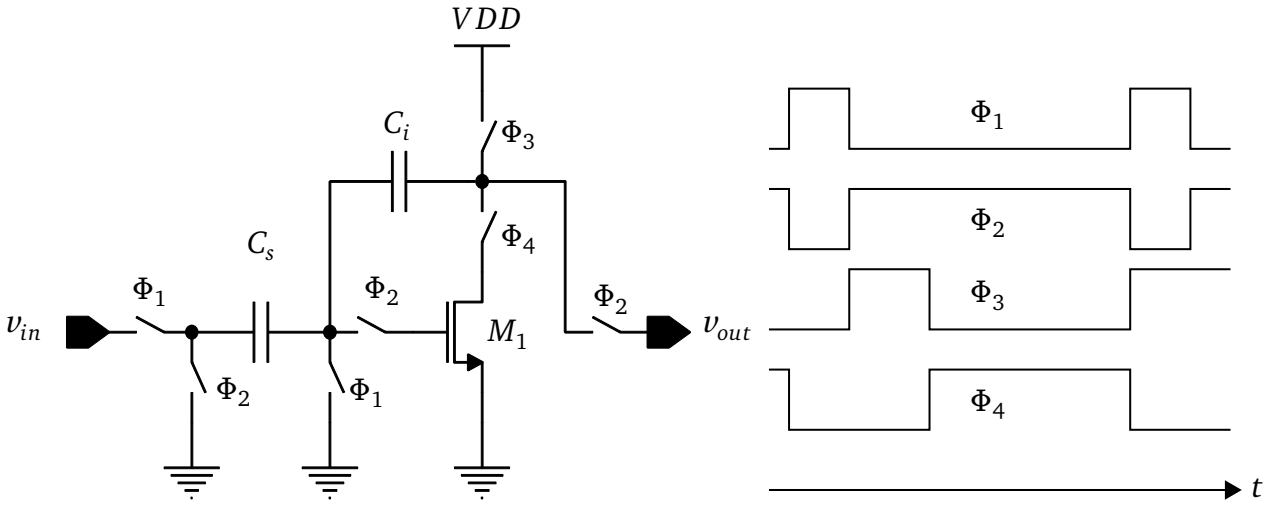


Figure 2.21: Switched capacitor circuit using dynamic amplifier and its clocking scheme.

The operation of the circuit is explained as follows. During phase Φ_1, input voltage is sampled onto sampling capacitor C_s, while the amplifier biasing circuits are disabled to reduce the power consumption. During the next phase, Φ_2 and Φ_3 are closed while Φ_1 and Φ_4 remain open. In this step the output is precharged to supply voltage V_{DD} and the input to transistor M_1 is precharged to a potential above its threshold voltage. The potential at input to M_1 depends on the charge from previous phase and charge from existing phase.

When Φ_3 is open and Φ_4 is closed, the output node starts to discharge from V_{DD} towards ground. Capacitive coupling from the output to the input of the transistor as the output voltage is lowered decreases the input gate voltage of the transistor. When the gate voltage reaches threshold voltage of the transistor, the discharge of output node stops as the transistor switches off. Any charge present on sampling capacitor C_s that is different from the threshold voltage of the transistor is transferred to integration capacitor C_i. It is similar to the virtual ground effect in Op-Amp where the charge transfer from input to output stops when input voltage of the Op-Amp reaches the common mode voltage.

The virtual ground condition in the dynamic amplifier circuit is reached when input voltage reaches its threshold voltage V_T. Hence by setting threshold voltage of the transistor V_T appropriately to half of the supply voltage, the dynamic range of input and output can be set symmetrical around the threshold voltage. An important consideration in dynamic amplifiers is that there be direct capacitive path between output and input virtual ground condition. Dynamic amplifiers have been used to realize low pass modulators with bandwidths upto few MHz [23][24][25]. One of the main disadvantages of this technique is the requirement of multiple clock phases.

2.6.2 Inverters

This circuit works similar to the dynamic amplifiers but uses inverters instead to perform the charge transfer as shown in Figure 2.22a [26][27]. However unlike dynamic amplifier where the virtual ground condition is set by the threshold voltage of the transistor, the inverter has no such possibility of virtual ground condition due to its single input terminal. Instead the input is maintained at the offset voltage due to the closed loop which is formed from output to input. Since the offset voltage depends on the process variations, transistor parameters, mismatch and also reduces the amount of charge transferred from input to output, offset cancellation schemes must be employed to produce predictable output.

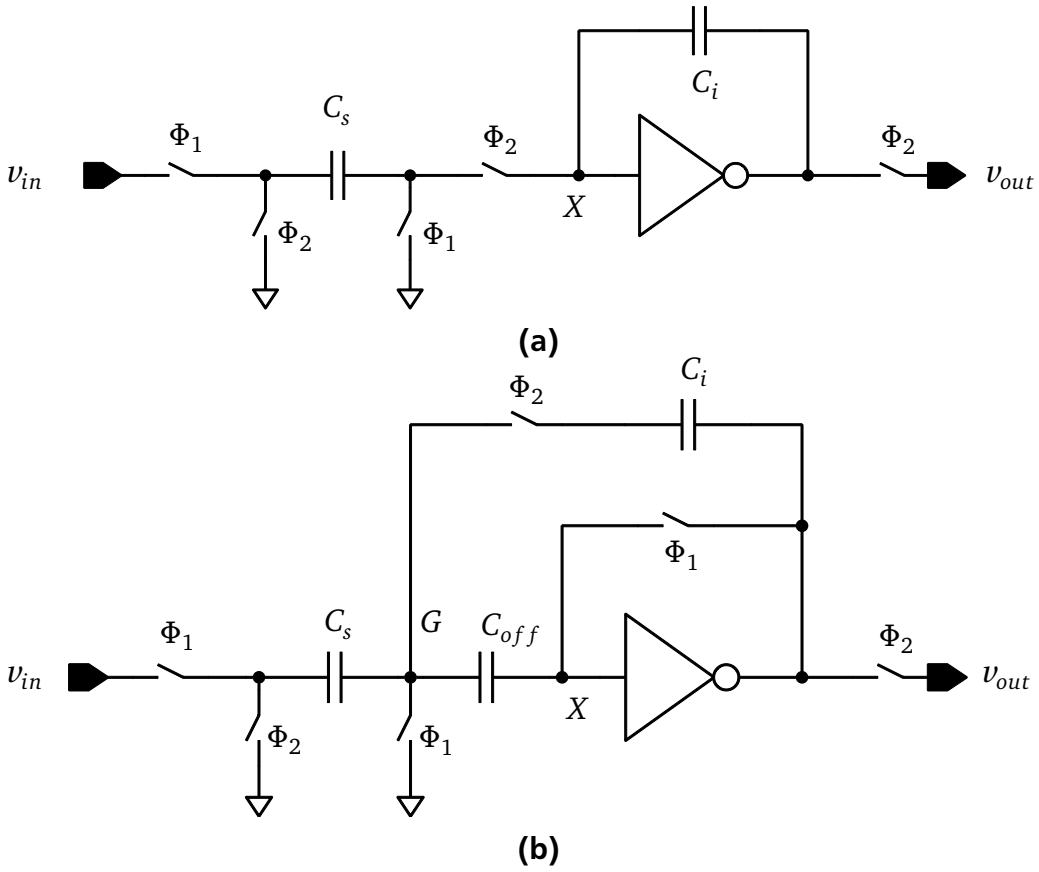


Figure 2.22: Switched capacitor using inverter (a) Basic architecture and (b) Practical architecture with offset cancellation.

Figure 2.22b shows an inverter based integrator employing a simple offset cancellation technique. The principle is to sample the offset voltage onto offset capacitor C_o during phase Φ_1 when the input is also being sampled onto capacitor C_s. During phase Φ_2, voltage V_X should be the offset voltage due to the feedback loop formed by capacitor C_i. However the presence of offset capacitor C_o which has the offset voltage with opposite polarity cancels this effect, thereby forcing node G to be the signal ground or equivalently the virtual ground. Thus the charge on C_s is transferred to C_i under the virtual ground condition. This technique has been successfully used to realize different $\Delta\Sigma$ modulators for medical and low frequency applications [28][29]. The main disadvantage is that this technique can be applied to only low sampling frequencies, which limits the application area to sub kHz bandwidths.

2.6.3 Comparators

Figure 2.23 shows the simplified schematic of a Comparator Based Switched Capacitor (CBSC) circuit implementing an integrator and its associated timing diagram [30]. In CBSC circuits the role of Op-Amp is performed by the comparator which detects the virtual ground condition at its inputs and enables or disables the charge transfer from input to output capacitors. The main blocks in this circuit are the comparators used for detecting the difference between its inputs and the current sources which are responsible for charging and discharging the integration and output capacitors.

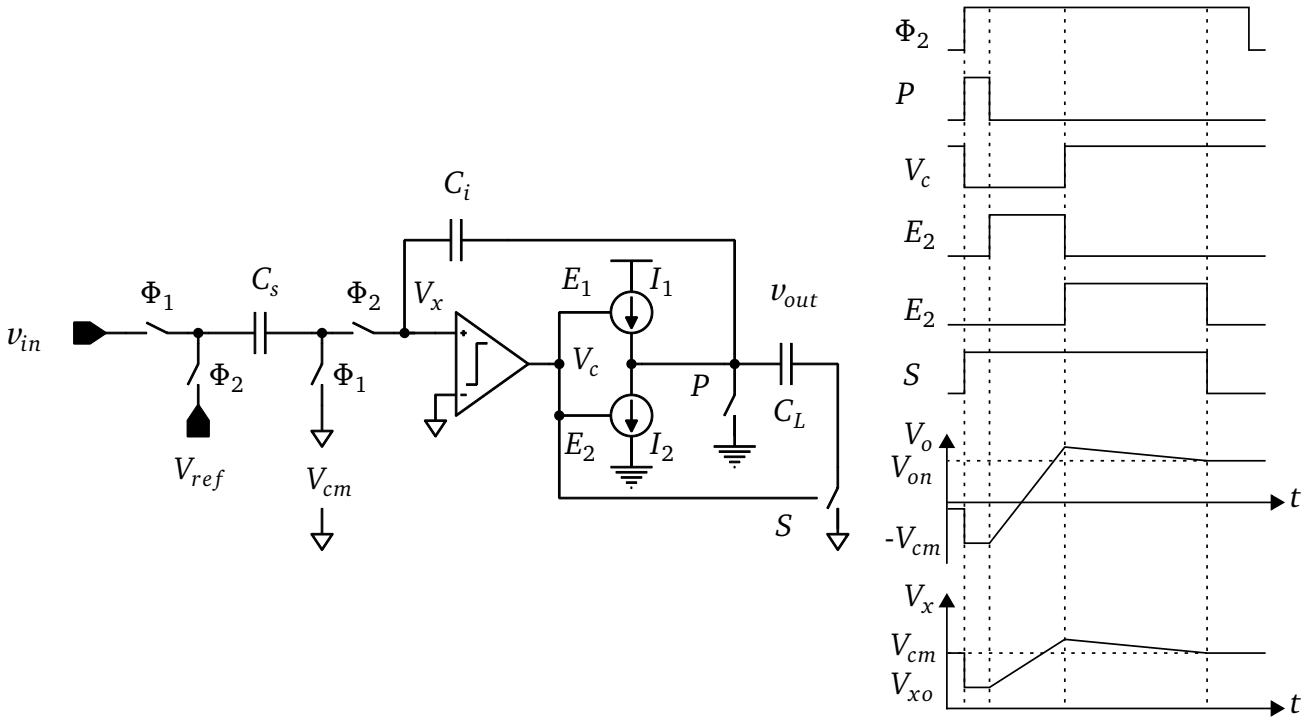


Figure 2.23: Comparator based switched capacitor and its associated timing diagram.

The operation of CBSC circuit is similar to that of a dynamic amplifier where the virtual ground condition was enforced by threshold voltage of the transistor. Here the virtual ground condition is enforced to the common mode voltage by using comparators to detect it. During sampling phase Φ_1, the input voltage is sampled onto sampling capacitor and the rest of the signals are set to low. At the beginning of charge transfer phase Φ_2, signal preset P is briefly enabled to clear the load capacitance by connecting it to ground potential and making sure the comparator input V_x starts well below its common mode voltage V_{cm}. After the preset, coarse charge transfer phase E_1 starts wherein the current source starts to quickly charge the output capacitor which leads to the comparator input crossing the V_{cm} level. The moment the comparator input detects a change in common mode voltage at its input, it turns off current source E_1 which stops the charging of the output load capacitor.

The output voltage on the load capacitor should ideally reach a voltage of V_{on} from $-V_{cm}$ at the end of E_1 signal. But due to the finite delay between the comparator detecting a change in its input levels and disabling current source E_1, an additional amount of charge is transferred into the load capacitor. To compensate and remove this additional charge, the comparator

immediately enables current source E_2 which slowly discharges the load capacitor. This phase E_2 is called the fine charge transfer phase during which the load capacitor voltage discharges towards voltage V_{on} and simultaneously the input of the comparator experiences its voltage V_x going again towards its common mode level. Once the comparator input crosses common mode voltage V_{cm} again, current source E_2 and sampling switch S are shut off. Due to the current source providing a slow rate of discharge compared to current source E_2, the final output voltage on the load capacitor reaches a value which is closer to the ideally required transfer voltage of V_{on}. This small overshoot is ideally independent of the input voltage if comparator delay and ramp rate of the current sources are constant.

CBSC circuits have been successfully used to realize data converters which include pipeline ADCs and $\Delta\Sigma$ modulators [31][32][33]. The accuracy of the circuit depends on the current source, which should provide a high output resistance to prevent loss of charge from integration and load capacitors. To maintain large output resistance, only small bias currents can be allowed to flow through current sources. This limits the maximum sampling frequency of the entire circuit and prevents its use in high bandwidth applications.

2.6.4 Switched Current Techniques

An altogether different technique is to use the current domain where the limitations of low voltage do not apply due to signal processing in the current domain. This method called SI circuits was proposed in the early eighties as an alternative to voltage mode processing of signals [34]. The core building block in SI integrator is called a current memory cell. Figure 2.24 shows the basic operational scheme of a second generation SI integrator. The current memory cell is shown in the dashed box and it is composed of only a few transistors. During Φ_2 the gate voltage of transistor M_2 is charged to a level V_{gs} which maintains a current flow of I_2 through it when phase Φ_2 is low.

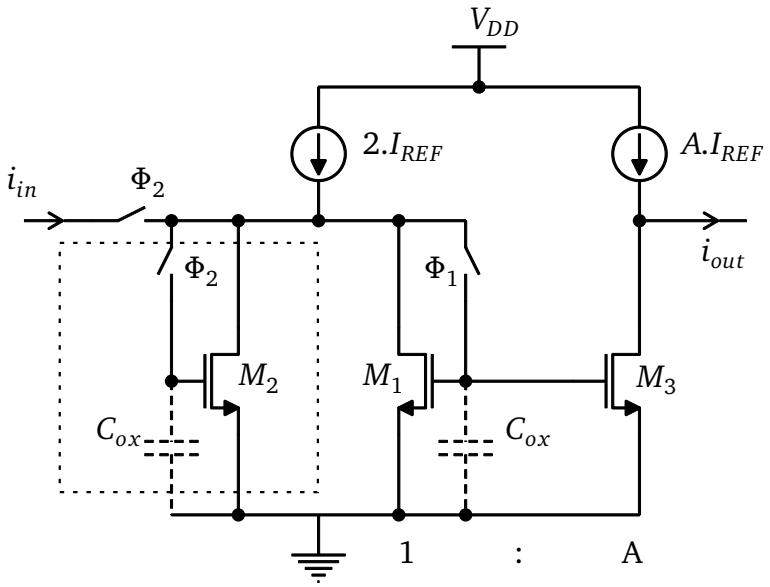


Figure 2.24: Architecture of a second generation switched-current integrator.

The integration of the input signal is performed by transistors M_1 and M_2. The third transistor M_3 which forms a current mirror together with transistor M_1 is used to buffer integrator current

I_1 to the output. A straightforward analysis of the integrator reveals the following relation between input and output currents $I_{out}(n) = I_{out}(n-1) + AI_{in}(n-1)$, where the coefficient of SI integrator is given by the current mirror ratio A. The maximum operating range of these integrators is set by the linear operating region of the transistors. Many variations of this SI concept have been used to realize $\Delta\Sigma$ modulators of various orders [35][36][37][38][39].

2.6.5 Digital Techniques

Analog circuits are more prone to errors in advanced technologies and are forced to reside on the same die as digital circuits in order reduce silicon area. However this can be an advantage due to the fact that low power and compact digital circuits can be used to digital assist the ADC in order to increase its performance. Digital blocks in combination with secondary analog blocks can be used to quantify the errors in analog blocks and apply correction to modulator outputs either at startup or during runtime.

Digitally assisted techniques were used to improve the DR, SNR performance of both nyquist and $\Delta\Sigma$ ADCs. In $\Delta\Sigma$ they were used to improve the multi-bit DAC performance. Digital calibration technique proposed in [40] uses adaptive line enhancers and least mean squares algorithm to estimate the signal of interest from the noisy input signal by updating digital cancellation filter coefficients, which results in the improvement of SNR by over 20dB.

The technique proposed in [41] corrects errors in integrators with low gain Op-Amps by determining its leakage in the digital domain and applying a correction in the analog domain. The process runs completely in the background without interrupting the normal operation of the integrator by injecting a separate calibration signal into the integrator. Some of the other techniques involve injecting pseudo random noise and dithering to estimate non linearities of the integrator as well as the entire system and apply correction either in digital domain or analog domain.

2.6.6 Comparison of the Low Voltage Design Techniques

The previous subsections introduced a variety of low voltage design techniques for $\Delta\Sigma$ modulators. Most of the techniques targeted the complete replacement of Op-Amp while some involved the correction of imprecise Op-Amp using digital and analog methods as a means to enhance performance. The performance comparison of non-Op-Amp based architectures reveals that none of the circuits described can be used at higher sampling rates without attracting heavy penalty from circuit parasitics and transistor non-idealities. Almost all non-Op-Amp circuits provide very good performance for lower sampling rates and lower bandwidths and hence find use in low frequency application areas such as medicine. However in order to truly challenge the dominance of Op-Amp, it is necessary to find alternate circuit design techniques which can operate at higher sampling rates and are able to provide higher performance without loss of accuracy. While it is possible to use time-interleaving techniques to combine two or more lower sampling rate modulators to generate a higher sampling rate and higher bandwidth, it comes however at the expense of larger power consumption and area requirements.

2.7 Survey of State of the Art $\Delta\Sigma$ Converters

This chapter presented different architectures of $\Delta\Sigma$ modulators and alternate integrator circuits. It can be concluded from the previous introduction that various combinations exist for the realization of DT low pass $\Delta\Sigma$ modulators. Although initially introduced for low frequency and high resolution applications, $\Delta\Sigma$ modulators have fast scaled up to the requirement of high frequency environments in recent years, covering bandwidths hitherto occupied by only nyquist rate converters. In this section a survey of the state of the art in $\Delta\Sigma$ modulator design is presented. Although the main focus of this thesis is related to the development of DT base $\Delta\Sigma$ modulators, CT based $\Delta\Sigma$ modulators are also included in this survey for comparison purposes.

Data converters are compared using a quantity called Figure Of Merit (FOM). FOM is used to measure or indicate the quality of the design through a combination of data converter specifications such as ENOB, signal bandwidth, power consumption, area etc. FOMs can be defined in a wide variety of ways out of which the following two equations for FOMs are used for comparison purposes.

$$FOM_1|_{pJ/conv} = \frac{Power(W)}{2^{ENOB}.2.f_b}.10^{12} \tag{2.53}$$

$$FOM_2 = a_5.\frac{a_1^{ENOB}.f_b^{a_2}.V_{DD}^{a_3}.L^{a_4}}{Power(W)} \tag{2.54}$$

FOM_1 relates the power consumption of the converter to the effective resolution obtained from it. A converter should ideally consume lower power as the resolution increases. Hence a smaller value for FOM_1 indicates a better converter. The disadvantage of FOM_1 is that the other important specifications of the data converter such as technology feature length, supply voltage are not taken into account. Hence in order to provide a more comprehensive comparison index , the FOM_2 was introduced to compare converters where V_{DD} is the supply voltage, L is the feature length and $a_i(1...5)$ are fitting parameters which are derived from actual implementations of several types of data converters published in literature [42]. For a $\Delta\Sigma$ converter the value of these parameters are $a_1 = 1.78, a_2 = 0.76, a_3 = 1.4, a_4 = 0.18$ and $a_5 = 0.006$ as derived in Equation 2.54. It should be mentioned that no single FOM can capture all the attributes of the converter since they are derived by greatly simplifying the design tradeoffs involved in data converter design to just a few parameters. Nonetheless the FOMs described here are widely used to identify the converter quality.

The survey includes data converter publications using CMOS and other similar technologies from important conferences [60-145]. Based on the collected data the survey classifies the plethora of $\Delta\Sigma$ modulators into three categories: Discrete-Time (DT), Continuous-Time (CT) and others (reconfigurable, hybrid, non-opamp).

Figure 2.25 plots the categories in the ENOB vs the signal bandwidth f_b plane. It is seen that the majority of DT implementations are used for signal bandwidths ranging from low frequencies of few Hz upto 10 MHz while the majority of CT implementations are used for signal bandwidths upwards of 10 kHz till 100 MHz.

For each of these converters, the values of FOM_1 and FOM_2 are calculated using the available data and plotted together to compare where they stand with respect to each other in the FOM versus the signal bandwidth plane, as well as in the FOM versus the technology feature length L plane.

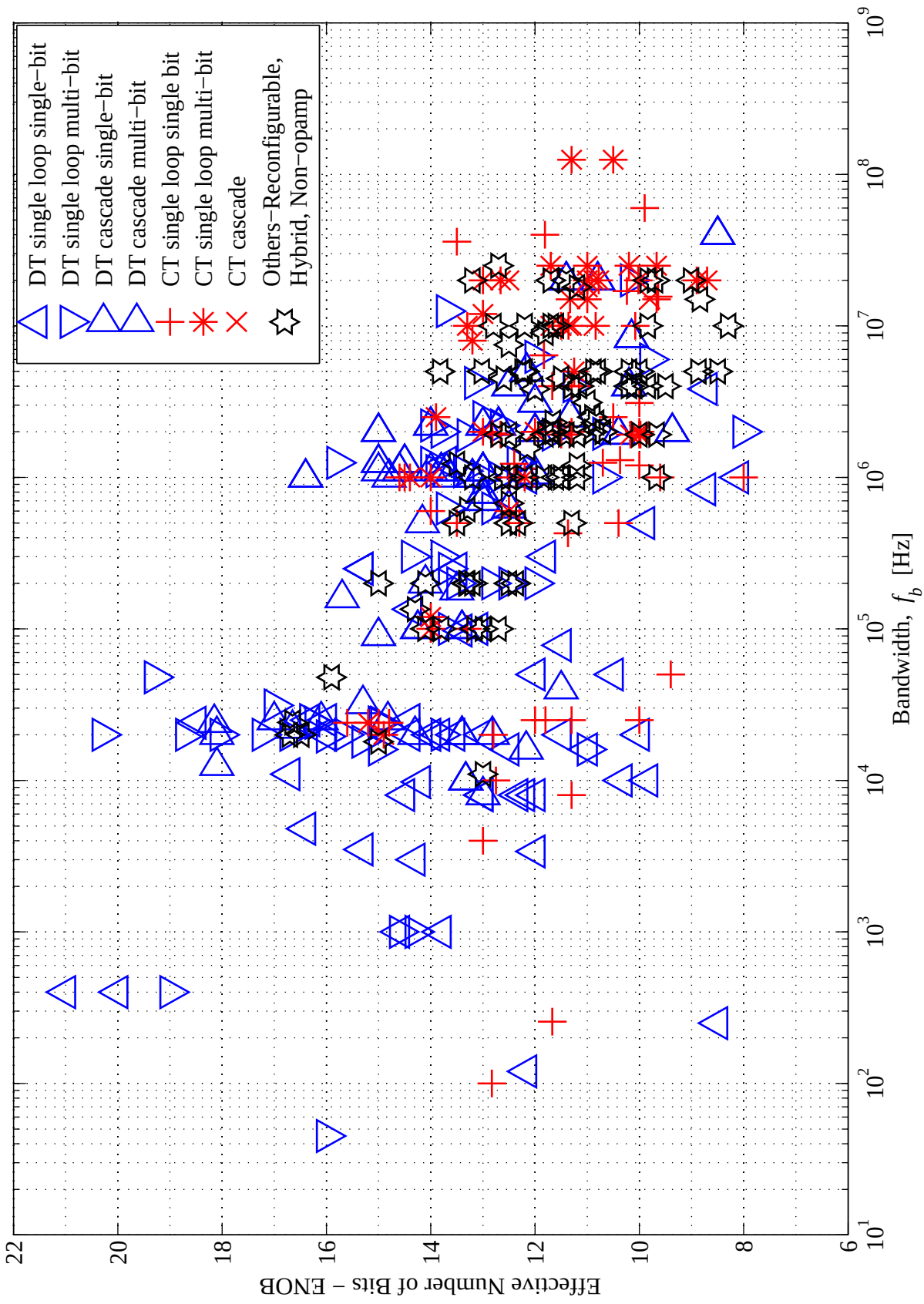


Figure 2.25: ENOB versus the signal bandwidth of surveyed modulators [60-145].

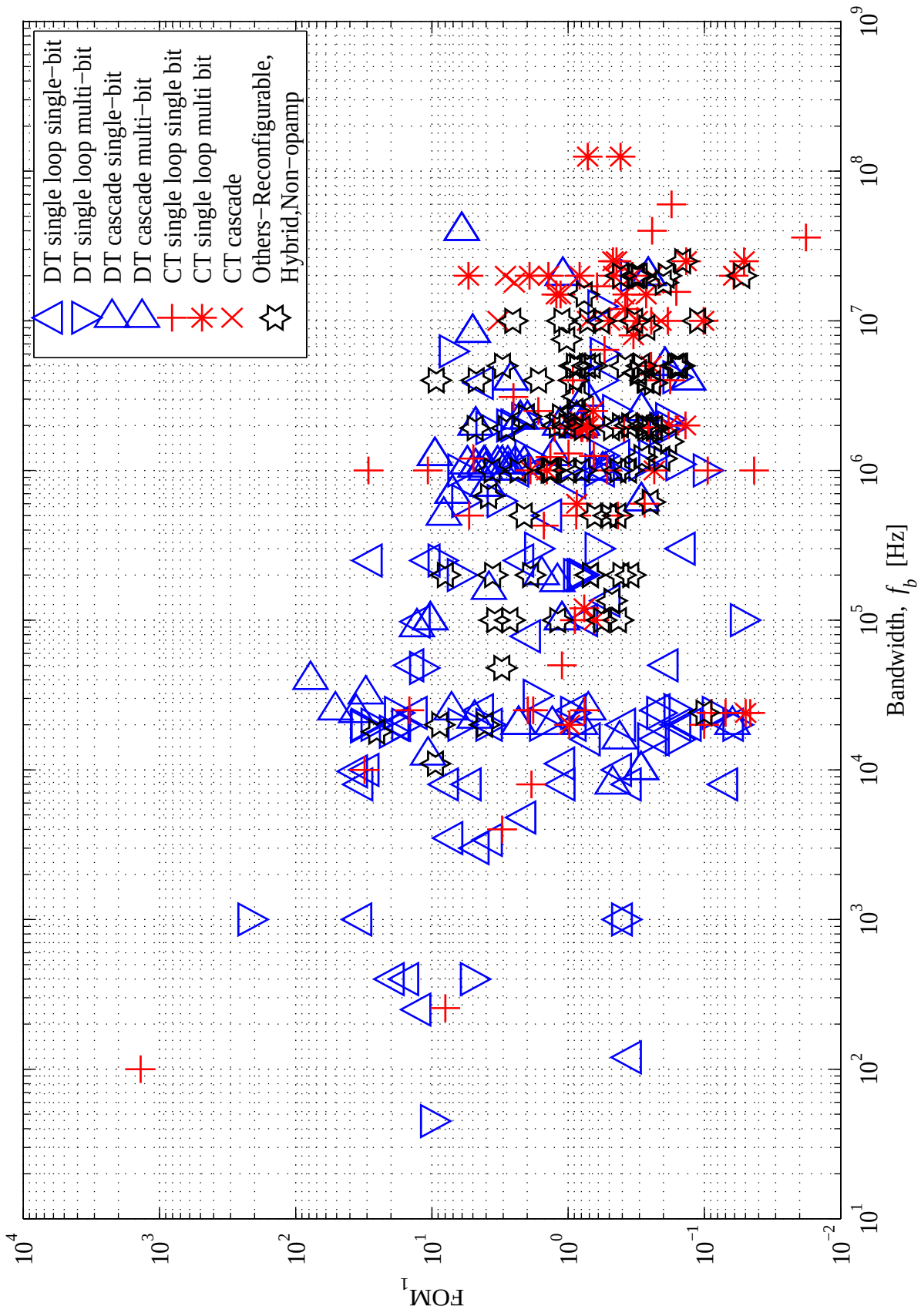


Figure 2.26: FOM_1 versus the signal bandwidth of surveyed modulators [60-145].

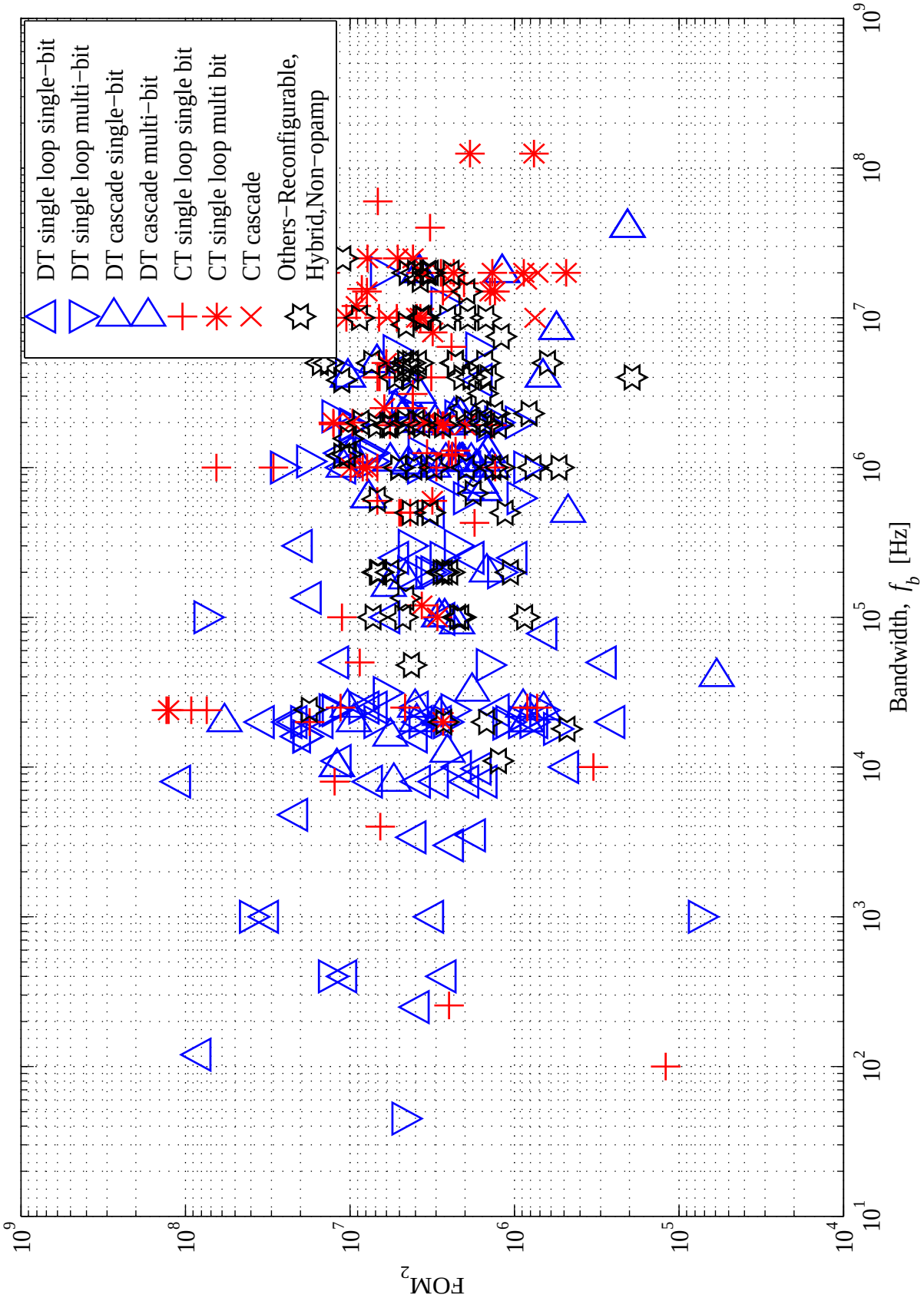


Figure 2.27: FOM_2 versus the signal bandwidth of surveyed modulators [60-145].

The following conclusions can be arrived at based on the survey and Figures 2.25 through 2.27:

- majority of the designs use DT modulators with SC techniques based on Op-Amps as the fundamental building block.
- other non-Op-Amp based architectures using inverters, comparators, as well as CT based modulators based on active-RC and GmC circuits also figure in this comparison but form a smaller part.
- early modulators were based on DT implementations and were used for the low frequency spectrum with only the recent entrants based on CT implementations targeting the high frequency spectrum of mobile communications standards such as WLAN, WiMAX and above.
- single loop DT implementations mostly use time multi-bit quantizers in combination with digital DAC correction techniques such as DEM instead of single-bit quantizers.
- cascade topologies normally use single bit or 1.5 bit quantizers avoiding multi-bit quantizers and associated digital correction techniques.

2.8 Summary

This chapter presented the operating principles of $\Delta\Sigma$ modulators. Various architectures and topologies were studied and compared with regards to performance parameters such as SNR, DR and ENOB. Different methods and approaches to implement the integrators in low voltage regimes were studied and a comparison of the state of the art in the $\Delta\Sigma$ modulators was given. From the survey it becomes clear that the CT implementations of the $\Delta\Sigma$ modulators tend to be favored when higher signal bandwidths are needed. Nonetheless DT implementations continue to be in wide use due to their usage of simple SC circuits which is more robust against process variations.

3 Analysis and Design of Current Conveyor based Switched Capacitor Circuits

Contents

The previous chapter introduced a variety of alternate circuit design techniques for $\Delta\Sigma$ modulators. Most of the techniques replaced the Op-Amp entirely with other circuits to maintain performance and keep power consumption low. The study of non-Op-Amp based circuits and their performance comparison reveals that barring the dynamic-amplifiers, none of the circuits described in the previous chapter can be used at higher sampling rates above 10 MHz. Almost all the circuits provide very good performance for lower sampling rates and lower bandwidths. These non-Op-Amp based circuits hence find use in low frequency application areas such as medicine. This chapter introduces SC circuits based on new class of building blocks called CCs. The Op-Amp as a core building block is completely eliminated and replaced with a simpler circuit which can be adjusted and adapted as per the needs of the application. The benefits,

drawbacks as well as non-idealities of this approach in combination with specific modulator topologies are discussed in this chapter. The need for CC calibration will be explained and the calibration technique itself will be introduced. Finally simulation results of the proposed approach will be discussed.

3.1 Introduction to Current Conveyors

A new building block analogous to the Op-Amp called the CC was introduced in late sixties, which brought with it some inherent advantages. Some of the main advantages of this block are as follows:

- Unlike the gain-bandwidth limited Op-Amp, CCs provide a nearly constant bandwidth independent of the value of the gain, thus allowing them to be used in high frequency applications.
- CC circuits are capable of working in both voltage mode and current mode regime while the Op-Amp is primarily voltage mode logic. This allows the designer to expand his design space to include designs working in current mode or as a combination of voltage mode and current mode together.
- CC circuits are typically open-loop circuits, which translates to better stability due to the lack of global feedback and huge compensation capacitors that are often needed as in the case of Op-Amps.
- CC circuits are typically less complex to implement due to their low to medium gains which are set by the circuit topology without the need for any external feedback as in the case of Op-Amps. Due to lack of feedback and lower complexity of the circuits, the transient performance of CC circuits is often better when compared to the Op-Amps.

In view of the above advantages CCs have been widely used to design various general purpose signal processing functions. While the lack of appropriate technology during the seventies for the design of CC prevented their proliferation, nonetheless since the late nineties a surge in the number of application based on CCs has been recorded. This section gives an brief overview of the principles of CCs, their basic implementations and some areas of application.

3.1.1 First Generation Current Conveyor-CCI

The concept of current conveyor was first introduced in 1968 and further developed two years later [43]. The CC was intended as a replacement to the Op-Amp in applications where the Op-Amp cannot be used. These applications where the mode of signal processing happens in the current domain, often referred to as current-mode processing, found use for the CCs. Before the introduction of the improved class of CCs a couple of years later, the first generation CC were referred to as simply CC. This name was later changed to CCI after the introduction of the second generation CC.

The CCI has three ports with terminals named X, Y and Z as shown in Figure 3.1 [44]. The operation of the CCI can be explained as follows. If a voltage is applied at port Y, the same voltage appears at port X. The application of voltage at port Y also causes a current flow at

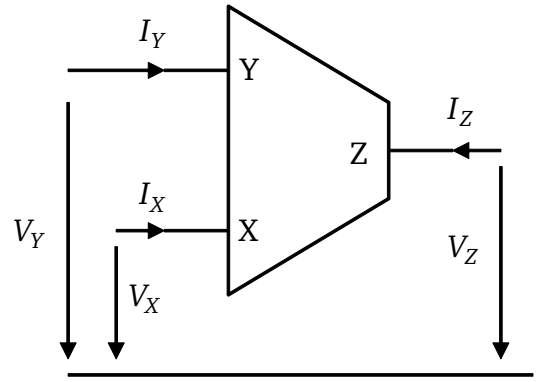


Figure 3.1: First generation current conveyor block diagram.

port X which in turn causes a current proportional to port X to be conveyed to port Z. The relationships between the various ports is given in the matrix form as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.1}$$

The currents at port Z can flow in the same direction as the X port or in opposite directions. Hence two classes of first generation current conveyors result, with each identified by the direction of flow of current in Z port relative to the X port as CCI±. The + sign refers the direction of current flow in the same direction and - sign refers to the direction of flow in opposite directions. The ideal CCI additionally presents the following impedances at its three ports. The X and Y ports ideally provide very low or zero impedance and Z port provides ideally infinite or very high impedance.

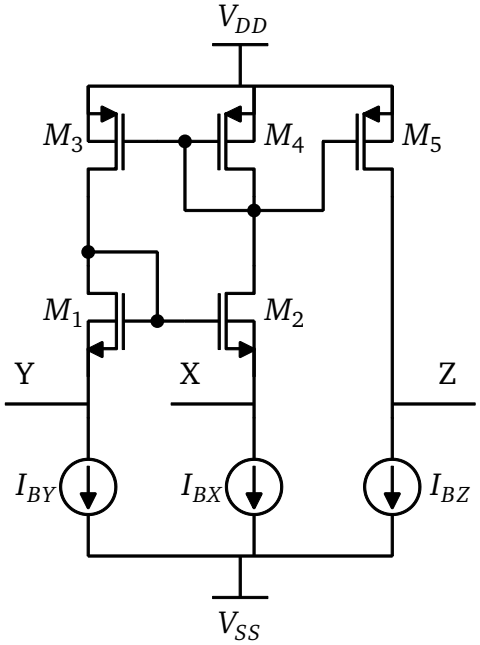


Figure 3.2: Class A implementation of first generation current conveyor.

The most common way to realize CCI is using current mirrors as shown in Figure 3.2 [45]. The illustrated circuit is a class A type CCI made from MOS transistors where the transistors

(M_1,M_2) and (M_3,M_4) form current mirror feedback loop, which forces the currents in the Y and X branches to be equal. At the same time, the current in the X port is mirrored to the Z port through the current mirror (M_4,M_5). The main disadvantage of this topology is the class A mode of operation, which reduces the linear operating range of voltages and currents.

The matrix shown in Equation 3.1 assumed ideal properties for the CCI. However transistors are not ideal and introduce non-idealities in the form finite output resistance, conductance and parasitics. Ideally the port X should present zero impedance. However a simplified analysis at the X port under no input condition at the Y port shows that the low frequency port impedance is given by:

$$Z_X|_{(f=0)} \approx \frac{(g_{ds1}+g_{m3}+g_{ds3})(g_{ds4}+g_{m2}+g_{ds2})-g_{m1}g_{m4}}{(g_{m1}+g_{ds1})(g_{m3}+g_{ds3})(g_{ds4}+g_{m2}+g_{ds2})} \tag{3.2}$$

which reduces by applying the following conditions for the matched current mirror transistors:$g_{mi} >> g_{dsi}$ where i=1,2,.. and $g_{m1}g_{m4} = g_{m2}g_{m3}$ to:

$$Z_X|_{(f=0)} \approx \frac{1}{g_{m1}}\left[\frac{g_{ds1}+g_{ds3}}{g_{m3}}+\frac{g_{ds2}+g_{ds4}}{g_{m2}}\right] \tag{3.3}$$

Similarly for the low frequencies (f=0), Z port impedance is given by:

$$Z_Z|_{(f=0)} \approx \frac{1}{g_{ds5}} \tag{3.4}$$

Although port X offers finite impedance, it is seen that the impedance is: $1/g_{m1}$ multiplied by a factor which is usually very small so that impedances of the order of few tens of ohm can be readily realized with current CMOS technologies. The non-linearity of class A CCI at low frequencies is generally very less due to the internal feedback among the four transistors $M_1..M_4$ and the only source of distortion arises from the threshold voltage mismatch among the current mirrors and the channel length modulation effects of the Z port transistor M_5 when it is driving high impedance loads. Using matched layout techniques and cascode transistors at the Z port, these distortions can be reduced.

A natural extension to the class A CCI is the class AB CCI, which provides increased dynamic range for the voltage and current signals at its three ports. Examples of such circuits are shown in Figure 3.3 [46, 47]. Figure 3.3a can be thought of as a combination of two class A CCIs described earlier with the top half symmetrical to the bottom half and the position of the PMOS and NMOS transistors interchanged. Similar to the class A CCI, this topology also introduces non-idealities in the form of finite port impedance and parasitics. The main advantage of this circuit is the increased dynamic range for small bias currents in the transistors. This can be seen by treating the upper half and lower half of the circuit independently. Each half circuit has a dynamic current handling capability equal to quiescent current. Both half circuits taken together can therefore handle currents up to two times the quiescent current and still stay in class A region of operation.

Although a straightforward analysis is quite tedious, nonetheless an approximation for the quiescent currents was derived in [46].

$$I_Q \approx \frac{1}{2}(I_Q^{'}+I_Q^{''}) \tag{3.5}$$

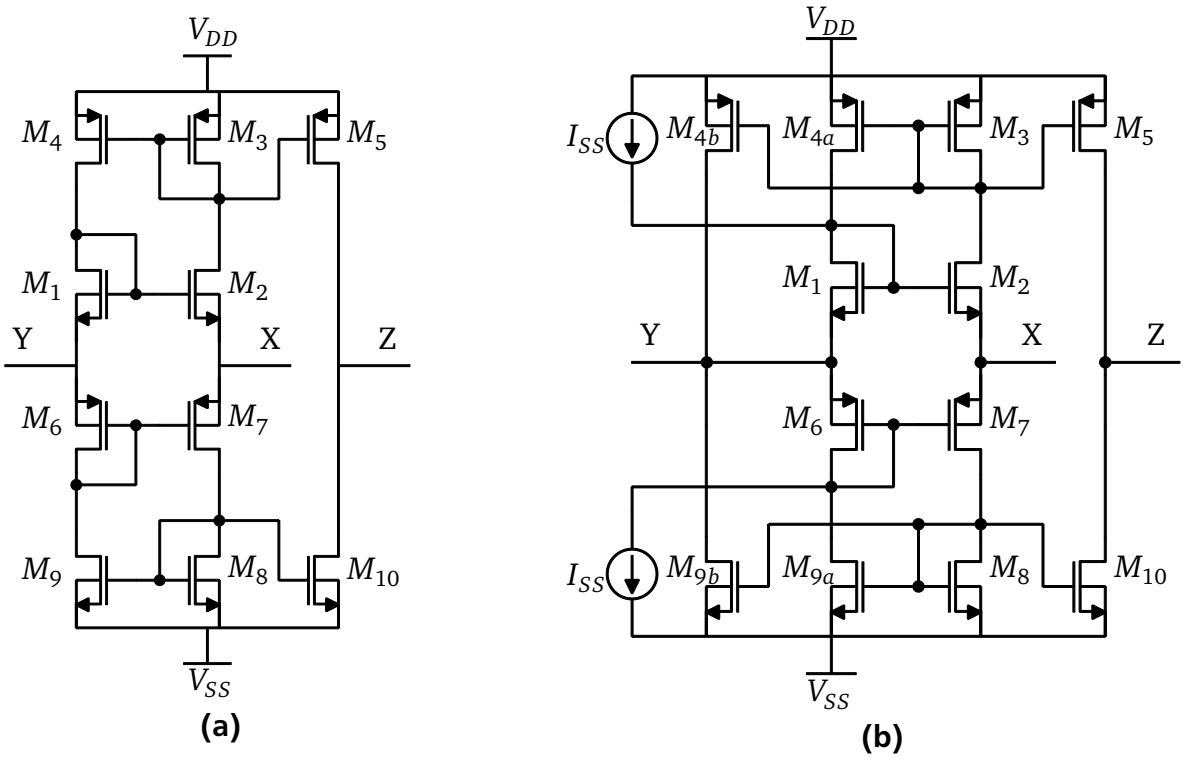


Figure 3.3: Class AB CCI (a) Uncontrolled Bias Current [46] and (b) Controlled Bias Current [47].

where

$$I_Q^{'} = \frac{K_2 K_3}{2[\sqrt{K_2} + \sqrt{K_3}]^2}(V_{DD} - V_{T2} - |V_{T3}|)^2 \tag{3.6}$$

$$I_Q^{''} = \frac{K_7 K_8}{2[\sqrt{K_7} + \sqrt{K_8}]^2}(V_{SS} - V_{T8} - |V_{T7}|)^2 \tag{3.7}$$

are the quiescent currents flowing in the upper half and lower half of the circuit when the port Y is connected to ground. These currents strongly depend on the supply voltage and are derived under assumption of ideal matching conditions. This leads to large variations in quiescent current and to bad biasing when transistor variations are included. A possible way to stabilize quiescent currents in the CCI topology involves adding current sources which provide the maximum fraction (1-λ_{FB}) of quiescent currents into the port Y while the X port provides only a small fraction λ_{FB} of the feedback current. Figure 3.3b shows such an arrangement.

Compared to class A CCI, the distortion in class AB CCI is greatly reduced. This is because of the symmetrical nature of the top half and bottom half of the circuit which leads to cancellation of the even order distortion components. Due to the class AB CCI staying in class A region of operation even in the presence of currents larger than its quiescent current, there is an improvement of typically 6dB for 2nd-order distortion and 12dB for 3rd-order distortion components [45]. Non-linearities due to channel length modulation are also not so significant as compared to class A CCI. However crossover distortion effects occur for currents greater than the quiescent current due to one half of the circuit turning off abruptly instead of gradually.

Some of the applications of CCI are shown in Figure 3.4. Due to low impedance at its input terminal it can be used as a negative impedance converter. A voltage controlled negative impedance converter results when the Z port is grounded, X port is connected to a resistor and

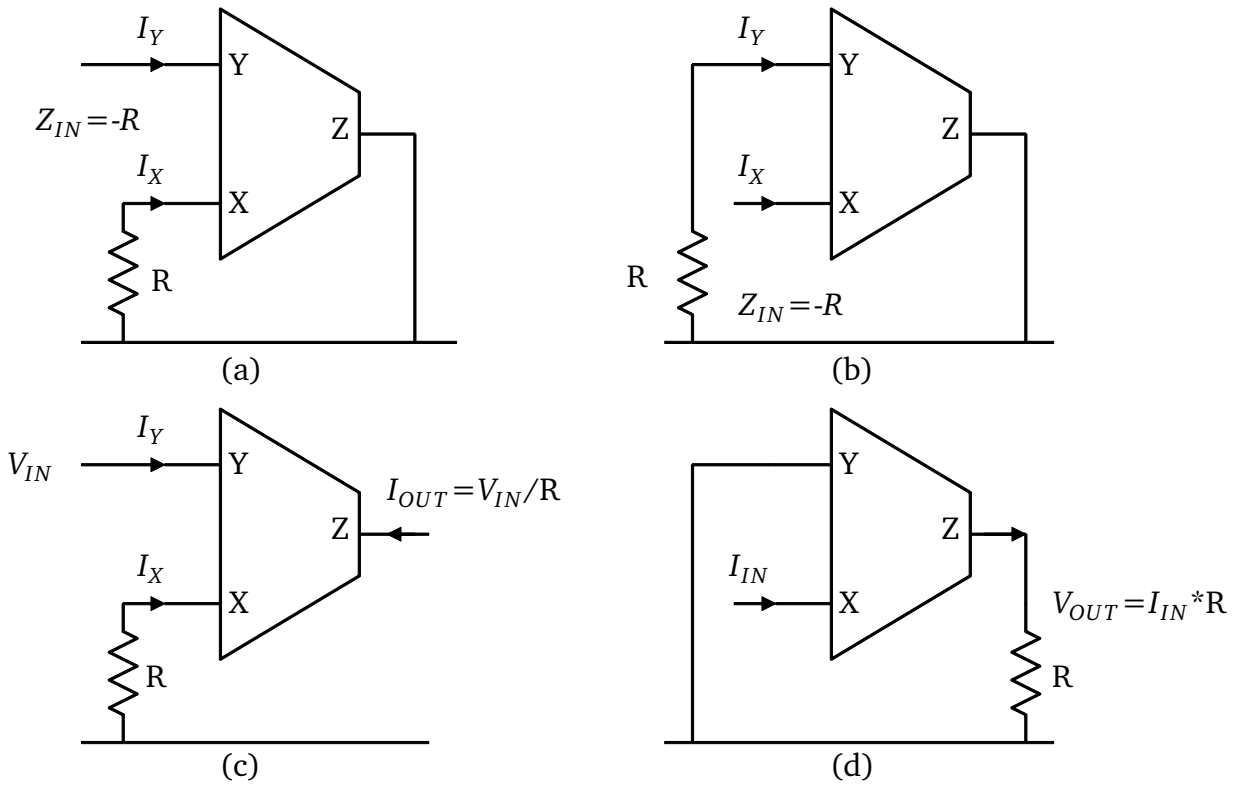


Figure 3.4: Applications of CCI (a) Voltage controlled negative impedance (b) Current controlled negative impedance (c) V-I converter (d) I-V converter.

voltage is applied at Y port. Similarly a current controlled negative impedance converter results when Z port is grounded, a resistor is connected to Y port and X port is given a current input. This negative impedance converter can be used to adjust the frequency response of amplifiers, filters and oscillators in order to improve their performance [48]. Some of the other applications of CCI include voltage-to-current, current-to-voltage converter, filter design and PTAT core for bandgap reference [49]. The main disadvantage that prevented the proliferation of CCI was that it had two low impedance ports Y and X and that all ports sunk currents. This meant that any preceding stage needed to be able to source the same amount of current in order to drive the low impedance ports of Y and X. Hence the CCI was not favored in many applications.

3.1.2 Second Generation Current Conveyor-CCII

The disinterest in CCI and the preference of high input impedance instead of low input impedance for various application led to the introduction of the CCII [50]. CCII is topologically similar to CCI, with the exception that it has one high impedance input and one low impedance input instead of two low impedance inputs like in CCI. The relation between three ports of CCII can be represented by the following matrix as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.8}$$

From the matrix it is clear that the Y port impedance is ideally infinite and sinks no current. The Y port is used as voltage input, Z port as current output and the X port for both voltage

output and current input. Similar to the CCI, the CCII is also classified as positive CCII (CCII+) or negative CCII (CCII-) depending on the direction of the current flow in the Z port relative to the X port. The CCII can be thought of as a combination of voltage-mode and current-mode device rolled into one block with the voltage-mode relation existing between Y and X ports and current mode relation existing between X and Z ports.

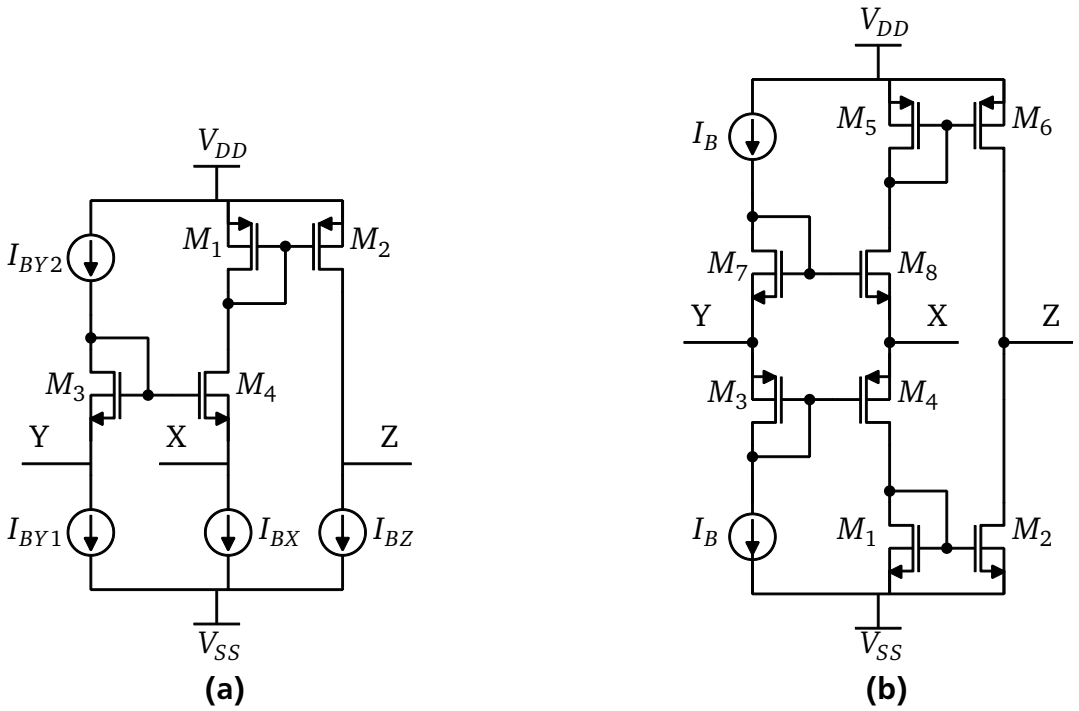


Figure 3.5: CCII (a) Type class A and (b) Type class AB.

Figure 3.5 shows class A and class AB CMOS realizations of CCII [44]. Comparing the two topologies to the CCI topologies described previously, it is seen that the major difference between the two is the removal of the feedback current mirror between X and Y ports and the inclusion of biasing current sources. Due to the lack of local feedback between X and Y ports, the impedance level at the port X increases slightly compared to CCI realizations. Also unlike the CCIs, the quiescent currents in the CCII are set by the biasing sources and not simply by the size and properties of the transistors.

Similar to class A CCI, analyzing the non-idealities of the class A CCII results in the following extended matrix which includes the finite transistor transconductances and output resistances.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} \approx \begin{bmatrix} g_{by1}+g_{by2} & 0 & 0 \\ 1-\frac{g_{dsp}+g_{bx}+g_{by2}}{g_{mp}} & \frac{1}{g_{mp}} & 0 \\ -g_{bx} & 1-\frac{g_{bx}}{g_{mp}}-\frac{g_{dsn}}{g_{mn}} & g_{dsn}+g_{bz} \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.9}$$

where g_{mn} and g_{dsn} are the matched transconductances and drain source conductances of the NMOS transistors M_1 and M_2, g_{mp} and g_{dsp} are the corresponding parameters for PMOS transistors M_3 and M_4, g_{by1} and g_{by2} and g_{bx} and g_{bz} are the limited output conductances of the current sources in the circuit. Through proper choice of transistor size and layout, the effect of these parameters can be adjusted so as to achieve a performance close to that of an ideal CCII.

Similar to the class AB CCI, the class AB CCII is also symmetrical. Comparing the upper half and the lower half of the class AB CCII, translinear loops can be seen which perform the action

of current conveying using current mirrors. Any current at port X is divided between the upper half and lower half. Then through current mirrors action, they are combined at the output port Z. If it is assumed that $\beta_3=\beta_4=\beta_p$, $\beta_7=\beta_8=\beta_n$, $V_{T3}=V_{T4}=V_{Tp}$ and $V_{T7}=V_{T8}=V_{Tn}$, the drain currents of the port X transistors M_4 and M_8 can be expressed as function of the input voltage v_x as:

$$i_{D4} = \begin{cases} I_B + v_X\sqrt{2\beta_p I_B} + \frac{1}{2}\beta_p v_X^2 & if\ v_X > -\sqrt{\frac{2I_B}{\beta_p}} \\ 0 & if\ v_X < -\sqrt{\frac{2I_B}{\beta_p}} \end{cases} \tag{3.10}$$

$$i_{D8} = \begin{cases} I_B - v_X\sqrt{2\beta_n I_B} + \frac{1}{2}\beta_n v_X^2 & if\ v_X > \sqrt{\frac{2I_B}{\beta_n}} \\ 0 & if\ v_X > \sqrt{\frac{2I_B}{\beta_n}} \end{cases} \tag{3.11}$$

Neglecting the small current flowing in either of the transistors during the short transition between weak inversion and shutoff, the total current at the X port can be expressed as linear function of the port X voltage v_X as:

$$i_X = i_{D4} - i_{D8} = v_X\sqrt{2I_B}(\sqrt{\beta_n} + \sqrt{\beta_p}) + \frac{1}{2}v_X^2(\beta_p - \beta_n) \tag{3.12}$$

when the condition $\beta_n=\beta_p$ and $|i_X|<4I_B$ is met.

Plotting the normalized drain currents show that the linear current handling capability of class AB CCII is four times the quiescent current flowing through it, when it is in class A region of operation [45]. Additionally the class AB CCII can operate beyond the current input levels of $4I_B$ in the class B region of operation, but with increasing non-linearity. If the currents in transistors M_4 and M_8 are plotted against the input current at port X, it would be observed that the X signal input current reaches almost four times the bias current I_B before either of the transistors come out of the saturation region and go into cutoff. Hence the class A region of operation of the class AB CCII is four times greater than the simple class A CCII. The important difference between this topology and the class AB CCI is the smooth transition between class A and class B region resulting in less crossover distortion. Similar to the class AB CCI this topology also reduces second order non-linearities and the distortion arising from channel length modulation due to the push pull symmetry of the PMOS and NMOS translinear loops.

The above discussion assumes matched symmetry between the upper half and lower half of the class AB CCII. Technology and process variations however introduce mismatches in threshold voltages, and transistors properties such that the upper half and lower half are not entirely matched resulting in increased distortion. By using proper layout and correction techniques these effects can be minimized. Additionally using differential structures such as differential amplifiers for the CCII construction, the above problems can be overcome at the cost of only class A region of operation.

Figure 3.6 shows some of the applications of the CCII [44, 45]. Due to voltage mode and current mode properties, the CCII can be used as voltage amplifier and current amplifier with gain ratios set by either passive resistors or capacitors. Hence the CCII can be used to replace Op-Amps in low to medium gain applications. The main source of gain error comes from the non-ideal finite impedance at X port for low frequency applications. At high frequencies similarly the parasitics at both the X and Z ports play an important role in determining the gain.

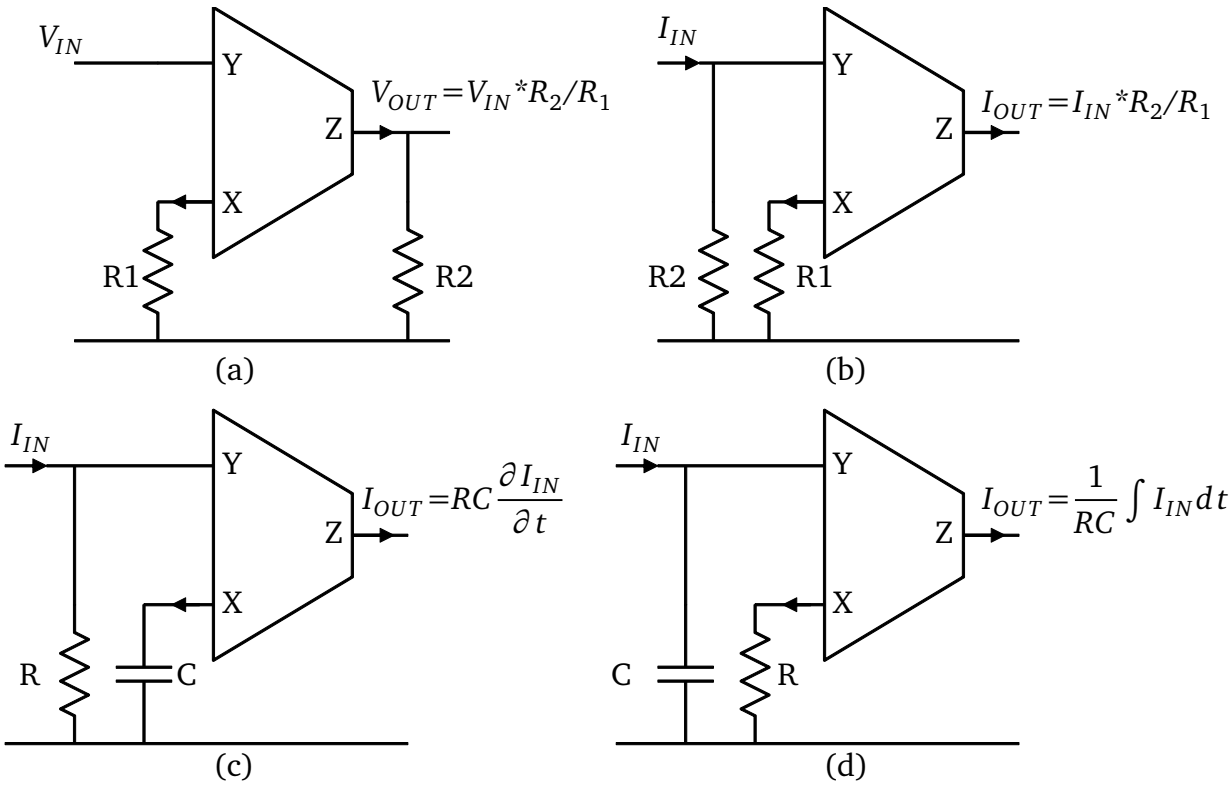


Figure 3.6: Applications of CCII (a) Voltage amplifier (b) Current amplifier (c) Current differentiator (d) Current integrator.

For example: Equations 3.13 and 3.14 show the voltage gain and current gain as a function of the parasitics C_z, C_x, C_y, impedance Z_x and resistors R_1, R_2 for the voltage and current amplifier in Figure 3.6.

$$A_v(s) \approx \frac{R_2}{(R_1+Z_x)} \frac{1+sR_1C_x}{(1+s(Z_x||R_1)C_x)(1+sR_2C_z)} \tag{3.13}$$

$$A_i(s) \approx \frac{R_2}{(R_1+Z_x)} \frac{1+sR_1C_x}{(1+s(Z_x||R_1)C_x)(1+sR_2C_y)} \tag{3.14}$$

Very high current or voltage gains typical for Op-Amps are not easily realized using CCII, due to the open loop mode of operation and the need for very large component ratios to set high gains. Hence CCIIs are typically used for signal processing functions where voltage to current and current to voltage conversions are needed, or voltage and current buffering with low to medium gains are needed. The lack of feedback and lower complexity of circuits in CCII, however, allow higher bandwidths without reduction of slew rate to be achieved. Compared to the Op-Amp where the use of feedback reduces inaccuracies arising from process and device variations, the CCII performance is directly affected by the accuracy of the voltage and current blocks which are influenced by technology, transistors, process and voltage variations. Hence proper design techniques and matching are needed to minimize their effects. Some of the other applications not shown in the figure are: Voltage Controlled Voltage Source (VCVS), Voltage Controlled Current Source (VCCS), Current Controlled Voltage Source (CCVS), Current Controlled Current Source (CCCS), capacitance multiplier, filters, Current Feedback Operational Amplifier (CFOA) and instrumentation amplifiers.

3.1.3 Other Current Conveyors

Many other configurations for current conveyors were proposed, with each providing a slightly different relation between the three ports. Although these CC might seem different in theory, at circuit level these configurations are derived from the CCI or CCII. Hence a detailed introduction to these configurations is omitted and instead they are briefly described here for the sake of completeness:

- A Third Generation Current Conveyor (CCIII) was introduced in 1995, which had properties similar to the CCI with the only difference being that the current in the Y port flows in the opposite direction to the current in X port. Its matrix was given by:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.15}$$

  Due to its low impedance node at Y and X ports, this CC found use in current probes to measure currents flowing through circuits.

- The Inverting Second Generation Current Conveyor (ICCII) was proposed with a inverting voltage relationship between Y and X ports. Any voltage applied to the Y port was buffered and inverted at its X port. Its matrix is represented as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.16}$$

3.2 Basic Principle of Switched Capacitor Integrator

In the previous section different CCs were introduced. Among the CCs, the CCII is undoubtedly the more versatile and powerful block. This can be observed by looking at the various applications where the CCII was applied extensively. This section introduces basic principles of the switched capacitor circuits. The operating principle of the Op-Amp based SC circuit and the CCII based SC circuit will be explained and the different approaches to realizing the Discrete-Time (DT) integrator for the $\Delta\Sigma$ modulators will be shown. The effect of the non-idealities will be dealt with in the next section.

3.2.1 Ideal Op-Amp Integrator

Discrete time loop filters are implemented by means of Switched-Capacitor (SC) circuits. Conventional SC circuits are made of Op-Amps, capacitors and switches. To control the loop filter response, two non-overlapping clock phases are used to switch the capacitors. Figure 3.7 shows the example of traditional SC integrator using Op-Amps.

As shown in the figure, the integrator consists of the input sampling capacitor C_{in} and integration capacitor C_{int} which help set the gain of the integrator stage. The input voltage is

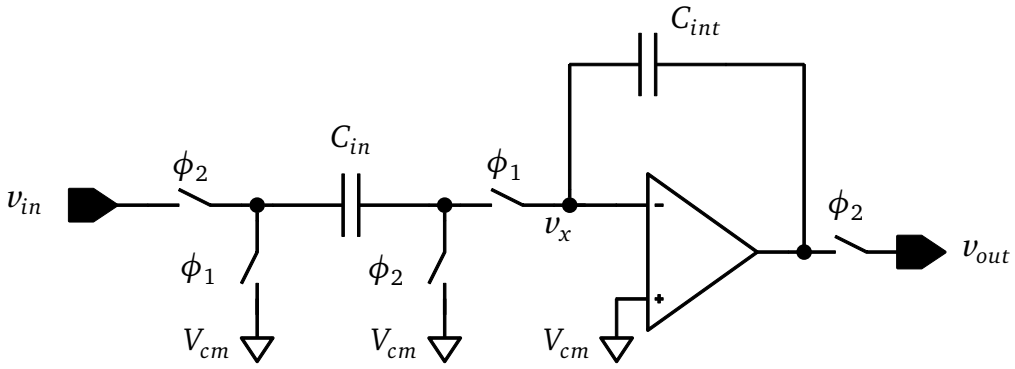


Figure 3.7: Traditional Op-Amp based SC integrator.

sampled onto capacitor C_{in} during the sampling phase denoted by clock ϕ_2 and the charge from C_{in} is transferred to capacitor C_{int} during the integration or charge transfer phase denoted by the clock ϕ_1.

The principle of charge transfer depends on the active enforcement of the virtual ground condition at input v_x by the Op-Amp. This means that the Op-Amp actively tries to bring any disturbance or change in its input voltage level back to its stable quiescent point by forcing the redistribution of charge from the C_{in} capacitor to the C_{int} capacitor using its feedback loop. Writing the charge balancing equation for the integrator at node v_x during the time instants, $\phi_2[(n-1)T_s]$, $\phi_1[(n-1/2)T_s]$ and $\phi_2[nT_s]$, and combining them we get:

$$C_{int}\, v_{out}[nT_s] = C_{int}\, v_{out}[(n-1)T_s] + C_{in}\, v_{in}[(n-1)T_s] \tag{3.17}$$

where $v_{out}[(n-1)T_s]$ is the charge existing on the C_{int} capacitor at the end of the (n-1)th clock cycle. Rearranging the equation and transforming the terms to the Z domain results in the following transfer functions for the integrator.

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} \frac{z^{-1}}{1-z^{-1}} \tag{3.18}$$

The gain coefficient of the integrator is given by the ratio of the capacitors C_{in}/C_{int}. This is an important advantage of the SC circuits because the gain depends on the ratio of capacitors and not on the absolute value of the components. Dependence on the absolute value of the components would make the gain coefficient more susceptible to variations due to the process and technology. Thus any large variations in the absolute value of the components of the same type results in only small relative variations between the same components.

3.2.2 Ideal CCII Integrator

In order to understand how the CCII can be used to replace the Op-Amp, we need to look at the integration process involved in the Op-Amp integrator. Figure 3.7 introduced the delaying Op-Amp integrator. The functionality of the opamp in the integration process can be narrowed down to two tasks, namely charge transfer or integration phase and hold phase. During charge transfer phase, the charge on the input sampling capacitor C_{in} flows as current into the integration capacitor C_{int}. This charge flow is possible due to the application of virtual ground condition

at Op-Amp input through the feedback loop formed by integration capacitor C_{int}. During hold phase, the charge present on C_{int} capacitor is held constant and the Op-Amp acts as a buffer to transmit this integrated voltage to the next stage sampling capacitor.

If we consider two separate blocks which can perform these two tasks, they are the current buffer for charge transfer phase and the voltage buffer for hold phase. As described in the introduction to CC, the CCII was introduced as a basic building block which combines the current mode logic and voltage mode logic into a single block. Hence the CCII can be used as a drop in replacement for Op-Amps to perform these two tasks. Assuming ideal blocks, Figure 3.8 shows an arrangement of the current conveyor based switched-capacitor integrator similar to the one described in Figure 3.7 [51].

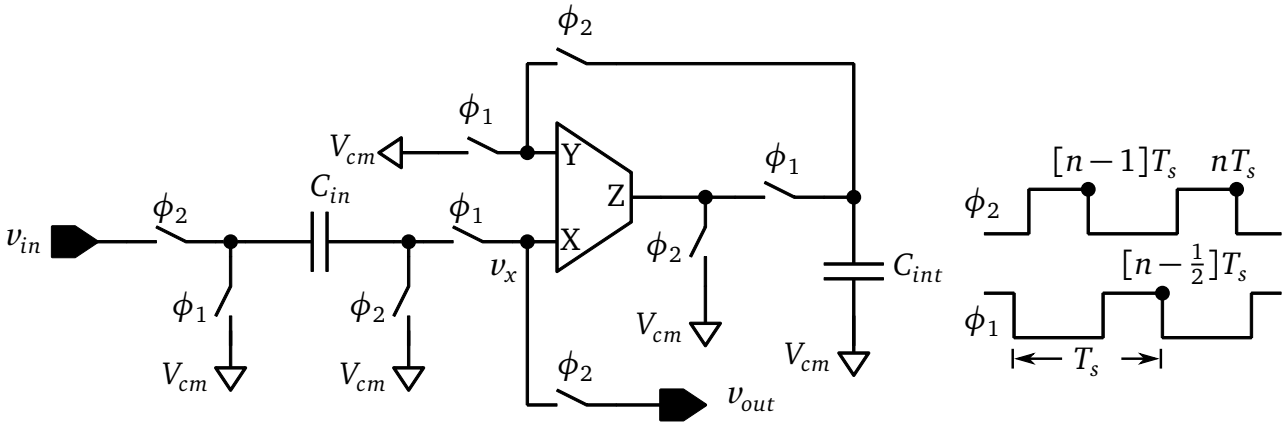


Figure 3.8: CCII SC integrator.

The operation of the CCII integrator can be described as follows. During the charge transfer phase ϕ_1, the current relation between the X and Z ports is utilized. The charge present on capacitor C_{in} is responsible for current flow in the X port, which causes a corresponding current to flow at the Z port. The Y port which is connected to the common mode voltage is used to enforce a virtual ground condition at the X port so that capacitor C_{in} discharges to the common mode voltage level. During hold phase ϕ_2, the voltage mode relation between Y and X ports is utilized. The voltage on C_{int} capacitor is buffered by the CCII and sent to the next stage sampling capacitor connected at the X port.

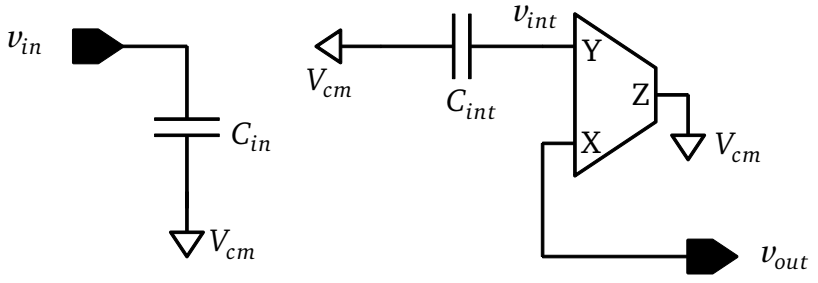


Figure 3.9: CCII SC integrator during sample and hold phase ϕ_2.

To analyze the input-output relationship of the CCII integrator, consider the circuit during ϕ_2 as shown in Figure 3.9. Assuming ideal CCII operation as shown in Equation 3.19, the following

equations can be written at the end of phase $\phi_2[(n-1)T_s]$ for the charge stored on C_{in} and the output voltage v_{out}.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.19}$$

$$Q_{in} = C_{in}(-v_{in}[(n-1)T_s]) \tag{3.20}$$

$$v_{out}[(n-1)T_s] = v_{int}[(n-1)T_s] = v_{int}[(n-3/2)T_s] \tag{3.21}$$

Next, consider the circuit during integration phase as shown in Figure 3.10. The Y port connected to the common mode voltage forces a virtual ground at X port, which causes C_{in} to discharge completely. This discharge causes a current flow which is replicated to the Z port and causes the change in charge of C_{int} capacitor. At the end of phase $\phi_1[(n-1/2)T_s]$, the following charge conservation equation can be written between X and Z ports.

$$\begin{gathered} \Delta Q_{int} = \Delta Q_{in} \\ C_{int}(v_{int}[(n-1/2)T_s] - v_{int}[(n-1)T_s]) = \pm(C_{in}(0-(-v_{in}[(n-1)T_s]))) \end{gathered} \tag{3.22}$$

where $v_{int}[(n-1/2)T_s]$ is the final value of integrated voltage at end of this phase. This voltage is buffered by the CCII and sent to the output as $v_{out}[nT_s]$ during the next hold phase $\phi_2[nT_s]$. The ± sign depends on the use of CCII+ or CCII- respectively.

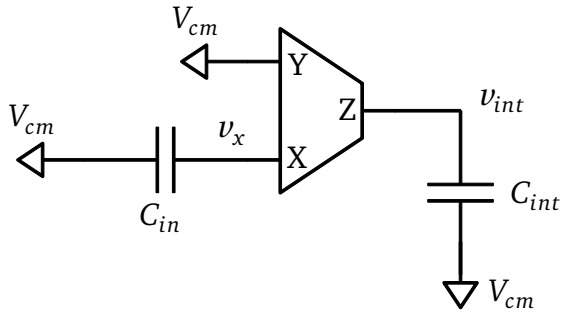


Figure 3.10: CCII SC integrator during charge transfer phase ϕ_1.

Replacing Equation 3.21 and $v_{out}[nT_s] = v_{int}[nT_s] = v_{int}[(n-1/2)T_s]$ in Equation 3.22, we get:

$$C_{int}(v_{out}[nT_s] - v_{out}[(n-1)T_s]) = \pm C_{in}(v_{in}[(n-1)T_s]) \tag{3.23}$$

which can be transformed to the Z domain to get the final transfer function of the CCII integrator.

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \pm \frac{C_{in}}{C_{int}} \frac{z^{-1}}{1-z^{-1}} \tag{3.24}$$

Equation 3.24 shows a transfer function of a delaying integrator whose gain coefficient is set by the ratio of capacitors C_{in}/C_{int}. This equation is equivalent to the delaying Op-Amp integrator described previously and hence can be used to replace it. Similar to this configuration, there

are other CCII SC configurations which result in a transfer function of half delaying and non-delaying integrators with different gain coefficients [52]. In the ideal analysis the CCII integrator is presented as a useful alternative to Op-Amp based integrator. It will however be seen in the next section, that the CCII integrator imposes stringent conditions on the CCII properties in order for it to give a performance comparable to that of Op-Amp integrator.

3.3 Non-Ideal Effects in Switched Capacitor Integrator

There are a number of non-idealities and non-linearities that degrade the performance of SC integrators, such as those coming from active blocks, switches, capacitors. This section will compare Op-Amp and CCII SC integrators with respect to the non-idealities of their main building blocks, that is the Op-Amp and the CCII. Design conditions will be derived for the CCII integrator in order for it to give comparable performance as an Op-Amp integrator. From the design analysis it will be shown that the existing integrator cannot be realized in advanced CMOS technologies, due to stringent requirements on the CCII properties and the size of associated components.

3.3.1 Op-Amp Integrator

Figure 3.11 shows the Op-Amp SC integrator which includes finite gain A_{DC} for the Op-Amp and the associated clocking sequence. C_p is the parasitic capacitance associated with Op-Amp input transistors and connecting switches.

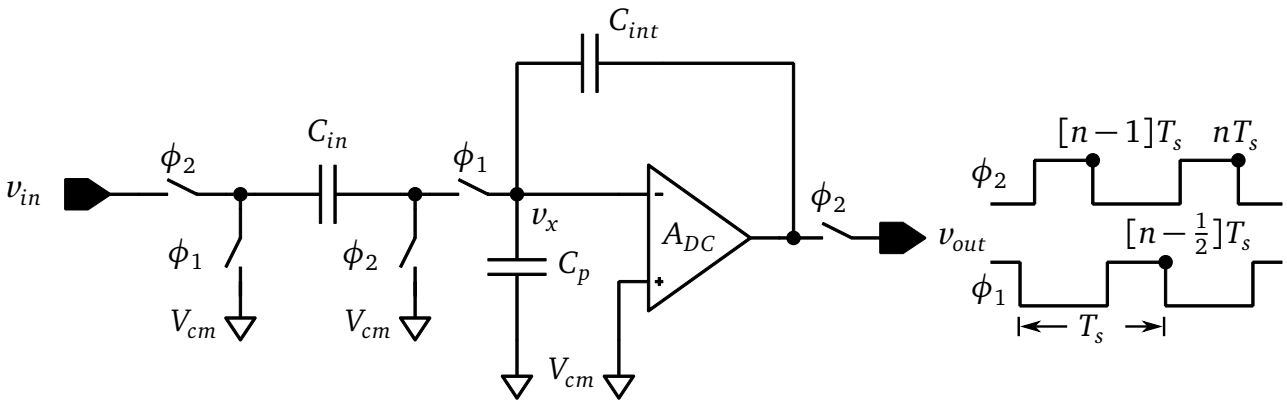


Figure 3.11: Traditional Op-Amp SC integrator with finite gain A_{DC} and parasitic C_p.

Analyzing the input-output relationship at $\phi_2[(n-1)T_s]$, $\phi_1[(n-1/2)T_s]$ and $\phi_2[nT_s]$, the following equation can be derived:

$$\begin{aligned} v_{out}[nT_s] = & \frac{1+\frac{1}{A_{DC}}\left(1+\frac{C_p}{C_{int}}\right)}{1+\frac{1}{A_{DC}}\left(1+\frac{C_p+C_{in}}{C_{int}}\right)} v_{out}[(n-1)T_s] \\ & + \frac{\frac{C_{in}}{C_{int}}}{1+\frac{1}{A_{DC}}\left(1+\frac{C_p+C_{in}}{C_{int}}\right)} v_{in}[(n-1)T_s] \end{aligned} \tag{3.25}$$

Applying Z domain transformation to the previous equation and identifying the two terms of the integrator namely, the gain coefficient and the Integrator Transfer Function (ITF) we get the transfer function:

$$H(z) = \frac{C_{in}}{C_{int}} ITF_{op}(z) \tag{3.26}$$

Thus the non-ideal transfer function of the integrator which is dependent on finite Op-Amp gain is given by:

$$ITF_{op}(z) = \frac{1}{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p + C_{in}}{C_{int}}\right)} \frac{z^{-1}}{1 - z^{-1}\left[\frac{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p}{C_{int}}\right)}{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p + C_{in}}{C_{int}}\right)}\right]} \tag{3.27}$$

Comparing the above equation to the ideal integrator transfer function of $z^{-1}/(1-z^{-1})$, it is seen that the finite Op-Amp gain introduces a gain error in the ITF and a phase error due to shift in the pole of the transfer function from DC ($z = 1$).

$$z_{op} = \frac{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p}{C_{int}}\right)}{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p + C_{in}}{C_{int}}\right)} \tag{3.28}$$

$$Gain_{op} = \frac{1}{1 + \frac{1}{A_{DC}}\left(1 + \frac{C_p + C_{in}}{C_{int}}\right)} \tag{3.29}$$

The net effect of the pole shift and the non-ideal ITF on the NTF of $\Delta\Sigma$ modulator is that the noise suppression in the signal band is reduced, resulting in more noise and lower SNR. Figure 3.12 illustrates the degradation in noise shaping for various Op-Amp gains by plotting the NTF of a second order $\Delta\Sigma$ modulator under assumption of $C_{in}/C_{int} = 1$ and $C_p \approx 0$

Similarly analyzing the integrator for finite unity gain bandwidth ($f_\mu = \omega_\mu/2\pi = A_{DC} f_d$) with the assumption of large DC gain A_{DC} and a low frequency dominant pole (f_d) for the Op-Amp results in just a gain error in the ITF [53]. This gain error is given by

$$Gain_{op} = 1 - e^{-k} \frac{C_{in}}{C_{in} + C_{int}} \tag{3.30}$$

where the factor k is related to the sampling frequency f_s and the unity gain bandwidth of the Op-Amp as

$$k = \frac{C_{int}}{C_{in} + C_{int}} \frac{\omega_\mu}{2 f_s} \tag{3.31}$$

As the previous equation shows, the gain error is dependent on the sampling frequency f_s. By making the unity gain bandwidth many orders larger when compared to the sampling frequency, the effect of the gain error can be minimized. This is why it is often advised in the design of Op-Amp SC circuits that the unity gain bandwidth be atleast 7-10 times higher than the maximum sampling frequency of the circuit.

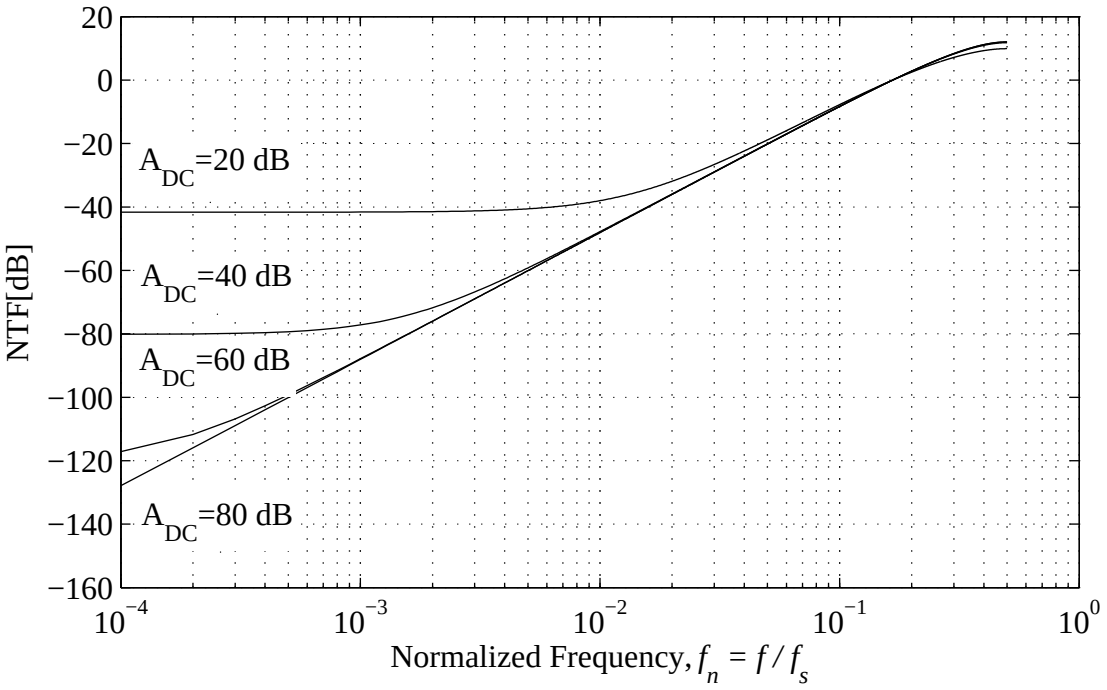


Figure 3.12: NTF of a second-order modulator for various Op-Amp gains.

3.3.2 CCII Integrator

The principles of CCII SC stage were introduced in the previous section, assuming ideal CCII properties at its three ports X, Y and Z. However it was shown in the section 3.1 when analyzing CC topologies, that transistor properties such as limited output resistance, transconductance and parasitics introduce non-idealities in the CCIIs. These non-idealities of CCII need to be analyzed with respect to its application in an SC integrator.

3.3.2.1 Non-ideal Macromodel of CCII for Analysis

In order to derive the non-ideal transfer function of CCII SC integrator, it is necessary to establish a macromodel for the CCII, describing its non-idealities. Different macromodels exist, varying in complexity and depending on the type and topology of the current conveyor [54, 55]. While complex models use more parasitic elements and sources to describe the circuit behavior accurately in order to reduce simulation times, the need here is to use to the macromodel to understand how the non-idealities of its three ports affect the operation of CCII integrator.

To this end, we use the macromodel of a non-ideal CCII shown in the Figure 3.13, which is derived from [56] and characterized by finite internal impedances of its ports and frequency dependent gains of the voltage and current follower. The three ports Y, X and Z contain an equivalent parallel impedance to the ground which along with the frequency dependent gains can be included in the non-ideal CCII matrix as:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 1/Z_Y & 0 & 0 \\ \beta(s) & Z_X & 0 \\ 0 & \alpha(s) & 1/Z_Z \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.32}$$

For describing the circuit behavior accurately, transistor level simulations are needed. However using the macromodel, important dependencies between the various CCII parameters and the performance of the SC integrator can be found out. These dependencies are useful for determining the minimum or maximum range of circuit parameters in relation to different components of the SC circuit, when designing the modulator at the transistor level. These dependencies will be discussed in detail in the design feasibility analysis.

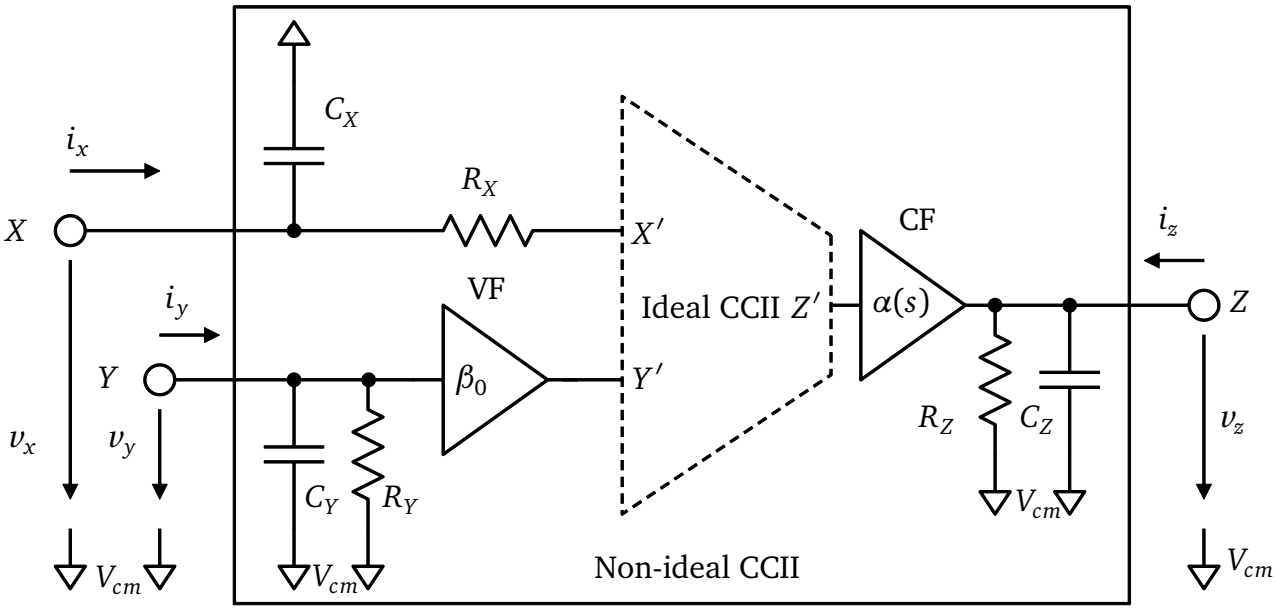


Figure 3.13: Non-ideal macromodel of CCII.

From the non-ideal CCII matrix, we observe five parameters. These parameters of the non-ideal CCII are defined as follows:

- $\beta(s)$: is the frequency dependent voltage transfer function of the CCII between Y and X ports. Depending on the topology, the voltage transfer response exhibits a first or higher order response. However since this thesis deals with simplified circuits such as the translinear class AB CCII presented in the introduction to CCs, therefore a first order approximation given below is sufficient for the non-ideal analysis. The first order single pole low pass response gives the maximum value at DC of β_0 and has -3dB bandwidth given by ω_β. In the following analysis we consider topologies which provide an approximate low frequency voltage gain of 1. That is $\beta_0 \approx 1$.

$$\beta(s) = \frac{v_x}{v_y} = \frac{\beta_0}{1 + s/\omega_\beta} \tag{3.33}$$

  The value of the 3dB frequency ω_β is determined by the value of parasitics at the X port and in the case of simple first order response it is given by:

$$\omega_\beta = \frac{1}{R_X C_X} \tag{3.34}$$

- $\alpha(s)$: is the frequency dependent current transfer function of the CCII between X and Z ports. Similar to $\beta(s)$, it is approximated by a single pole low pass type response with the

maximum value at DC given by α_0 and -3dB bandwidth given by ω_α. The low frequency current gain α_0 can be set to have any value by suitable design of the transistors in the CCII.

$$\alpha(s) = \frac{i_z}{i_x} = \frac{\alpha_0}{1 + s/\omega_\alpha} \tag{3.35}$$

- Z_Y: is the parasitic impedance at the Y port. At low frequencies the impedance is primarily resistive R_Y while at high frequencies it is capacitive C_Y. Depending on the type of circuit, the value of R_Y can become infinite as in the case when the gate of transistor is used as input or have a finite value as in the case of translinear CCII shown in Figure 3.5b. Taken together in parallel, the port Y impedance displays a first order low pass type frequency response. To determine the parasitic component values, an AC voltage source is applied at port Y while connecting an infinite load at port X and grounding the Z port. The impedance value Z_Y which is defined as the ratio of voltage to current is then plotted as a function of the frequency. The parasitics can be calculated from this curve as:

$$R_Y = Z_Y|_{(low\ f)} \tag{3.36}$$

$$C_Y = \frac{1}{2\pi R_Y f_Y} \tag{3.37}$$

  where f_Y is the -3dB frequency of the impedance plot.

- Z_Z: is the parasitic impedance at the Z port. At low frequencies the impedance is primarily resistive R_Z, while at high frequencies it is capacitive C_Z. Taken together in parallel, the port Z impedance displays a first order low pass type frequency response. The parasitics can be calculated using the procedure similar to that of port Y impedance as:

$$R_Z = Z_Z|_{(low\ f)} \tag{3.38}$$

$$C_Z = \frac{1}{2\pi R_Z f_Z} \tag{3.39}$$

  where f_Z is the -3dB frequency of the impedance plot.

- Z_X: is the parasitic impedance at the X port. At low frequencies the impedance is primarily dominated by the resistive component R_X and at high frequencies the impedance is dominated by the capacitive component C_X. The total parasitic impedance Z_X is hence a parallel combination of R_X and C_X components. In certain models an inductive component L_X is also added in series with the resistive component R_X to simulate the peaks that appears in the impedance plot and in the voltage gain plot. If the peak is however very small, then the inductive component can be neglected to simplify the analysis. The value of the R_X and C_X components can be found from the impedance plot as:

$$R_X = Z_X|_{(low\ f)} \tag{3.40}$$

$$C_X = \frac{1}{2\pi R_X f_X} \tag{3.41}$$

  where f_X is the -3dB frequency of the impedance plot.

3.3.2.2 Analysis of CCII Integrator using Macromodel

In this section the non-ideal macromodel of the CCII will be used to analyze the CCII SC integrator shown in Section 3.2.2 and repeated in Figure 3.14 for convenience. In order to derive the transfer function, Figure 3.14 needs to be analyzed at three time instants ($\phi_2[(n-1)T_s]$, $\phi_1[(n-1/2)T_s]$ and $\phi_2[nT_s]$). In the following analysis the SC integrator is assumed to be driven by a sampling clock which runs at a frequency of f_s or inversely has a time period of T_s. The circuit uses a two phase non-overlapping clock with pulsewidth of T_{s1} and T_{s2} respectively, where $(T_{s1}, T_{s2}) \approx T_s/2$. Furthermore, a positive CCII is assumed for the following analysis.

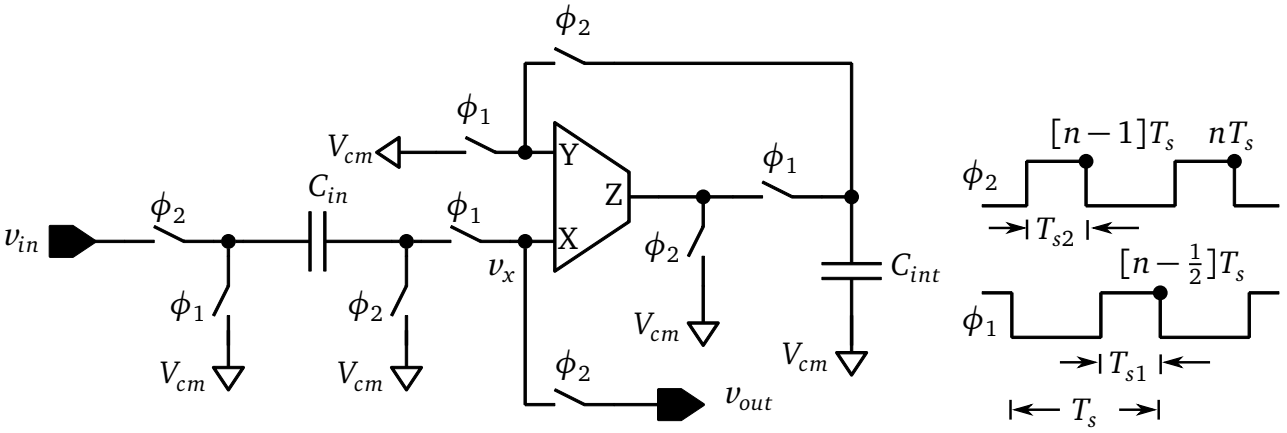


Figure 3.14: CCII SC integrator.

Time instant $\phi_2[(n-1)T_s]$:

The circuit is connected as shown in Figure 3.15. During this phase, also called the hold phase, the integrated voltage on C_{int} capacitor is sent to the output using the voltage buffer which multiplies its own frequency dependent gain $\beta(f_s)$. Thus the hold phase reduces the overall integrated voltage that appears at the output resulting in gain error. At the same time the input voltage is sampled onto the input capacitor C_{in}.

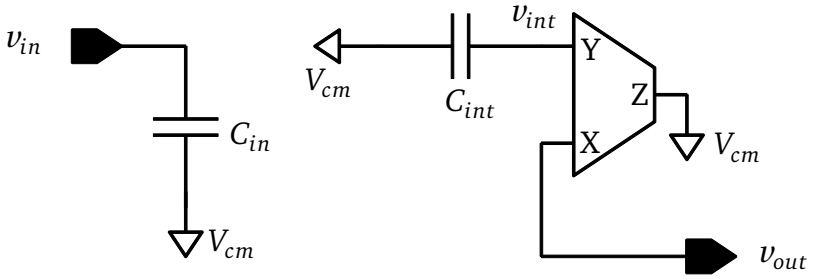


Figure 3.15: CCII SC integrator during the sample and hold phase $\phi_2[(n-1)T_s]$.

The equation for sampled charge Q_{in}, integrated charge Q_{int} and output voltage at the end of $\phi_2[(n-1)T_s]$ can be written as:

$$Q_{in} = C_{in}(-v_{in}[(n-1)T_s]) \tag{3.42}$$

$$Q_{int} = C_{int}\, v_{int}[(n-1)T_s] \tag{3.43}$$

$$v_{out}[(n-1)T_s] = |\beta(f_s)|\, v_{int}[(n-1)T_s] = \beta_0\, v_{int}[(n-1)T_s] \tag{3.44}$$

where $\beta(f_s)$ is the approximate magnitude of buffer gain at that specific sampling frequency. If we assume that the sampling frequency of SC integrator is less than the 3dB cutoff ($f_s << f_\beta$), then the voltage gain is simply given by the value at low frequency which is $|\beta(f_s)| = \beta_0$.

$$|\beta(f_s)| = \frac{\beta_0}{\sqrt{1+\left(\frac{f_s}{f_\beta}\right)^2}} = \beta_0 \tag{3.45}$$

As shown in Figure 3.15, integration capacitor C_{int} is disconnected from the Z port to prevent its discharge through the parasitic R_Z resistor. This is essential to maintain a constant voltage for the voltage buffer to be present at the output. However the parasitic C_Z capacitor is always connected and therefore continues to discharge through the R_Z resistor. The rate of discharge is controlled by the values of C_Z and R_Z which are defined by transistor properties and circuit topology. Since the transistor properties vary across different corners due to process and technology variations, the final value for R_Z and C_Z can change from the simulated values by large margins.

Additionally due to higher order effects which are not described in the macromodel, the rate of discharge also depends on the initial voltage of parasitic capacitor C_Z and other higher order circuit effects. The combined effect of the two causes the rate of discharge of C_Z to vary and introduce distortion on the integrated voltage during subsequent charge transfer cycles when parasitic C_Z and C_{int} capacitors are connected together. To avoid this and to make sure that C_Z capacitor is discharged completely, the entire Z port is autozeroed. Hence at the end of hold phase $\phi_2[(n-1)T_s]$, the charge on the parasitics at Z port becomes zero.

Time instant $\phi_1[(n-1/2)T_s]$:

The circuit is connected as shown in Figure 3.16. The Y port is connected to the common mode voltage V_{cm} and provides a forced virtual ground at X port due to the voltage relationship between Y and X ports. Since port Y is always connected to a constant voltage which is the common mode voltage, the parasitics of Y port do not affect charge transfer phase and therefore do not appear in the analysis below.

While the hold phase introduced just the gain error due to the voltage buffer, this phase introduces loss and gain errors both of which are caused by the CCII. The non-idealities responsible for these errors are:

- Current gain $\alpha(f_s)$: During the charge transfer phase input capacitor C_{in} is connected to the X port and due to the virtual ground enforced at the X port by the voltage mode relation between Y and X ports it starts to discharge, producing a current. The current flow generated at the X port is reflected on the Z port where it is multiplied by current gain $\alpha(f_s)$. The current gain $\alpha(f_s)$ reduces the conveyed current to the Z port and leads to gain error.

- Port X parasitics: The input capacitor C_{in} discharges through the port X parasitics namely the R_X and C_X components, producing a current. Depending on how big these parasitics

are relative to capacitor C_{in}, the rate of discharge varies. If the rate of discharge is very slow then at the end of the phase $\phi_1[(n-1/2)T_s]$, capacitor C_{in} is not completely discharged. An incomplete discharge translates to gain errors at the output which need to corrected.

- Port Z parasitics: Unlike the current gain and port X parasitics which introduce only gain error, the port Z parasitics introduce both gain and loss errors. This can be explained as follows. The integration capacitor C_{int} during this phase is connected to the Z port which was autozeroed previously during the hold phase. Since parasitics at the Z port have zero charge and integration capacitor C_{int} retains charge from the previous charge transfer cycle, connecting them together results in charge sharing between the two. Similarly the current flow generated at the Z port due to the discharge of C_{in} at X port is divided between the parasitics at Z port and the integration capacitor C_{int}. This charge sharing and division of the Z port current stabilizes the voltage levels across C_Z and C_{int} components initially, but is also responsible for decreasing the overall integrated voltage on the C_{int} capacitor. Additionally the overall charge present on capacitors C_{int} and C_Z is being slowly lost through the parasitic R_Z resistor during the entire charge transfer phase. This sharing and loss of charge on C_{int} leads to gain and loss errors.

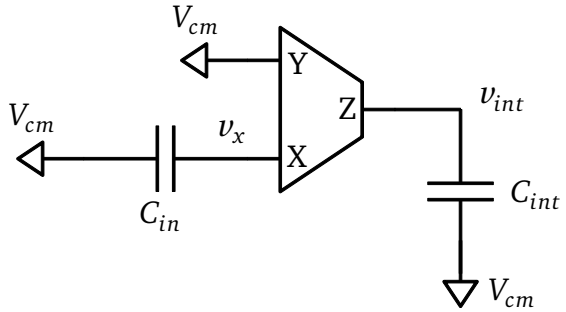


Figure 3.16: CCII SC integrator during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

To derive the total charge transferred from X to Z port during a time of T_{s1}, the circuit needs to be analyzed at port X and port Z independently to derive the various relationships. These relationships are then equated in the end to get the complete transfer function of the CCII integrator.

At Port X:

Figure 3.17 shows the connections at the X port, including the CCII parasitics during phase ϕ_1. To find the total charge lost by capacitor C_{in} during each half of the clock period, it is necessary to derive the voltage equation $v_x(t)$ over the time $t = (0 \rightarrow T_{s1})$. It is already known that at the end of previous sample and hold phase $\phi_2[(n-1)T_s]$, a voltage of $v_C = -v_{in}[(n-1)T_s]$ exists on the capacitor C_{in} which gets discharged over a total time of $t = T_{s1}$ during the phase $\phi_1[(n-1/2)T_s]$ through port X.

At the beginning of this phase the voltage on C_{in} is v_C and voltage on C_X is 0. Since the capacitors are connected in parallel, charge sharing takes place between the two. If switches connecting the capacitors have very low resistance, the charge sharing between the two capacitors can be assumed to be instantaneous, which results in stabilization of voltage level across the two capacitors at the beginning of this phase. The two capacitors with an initial common

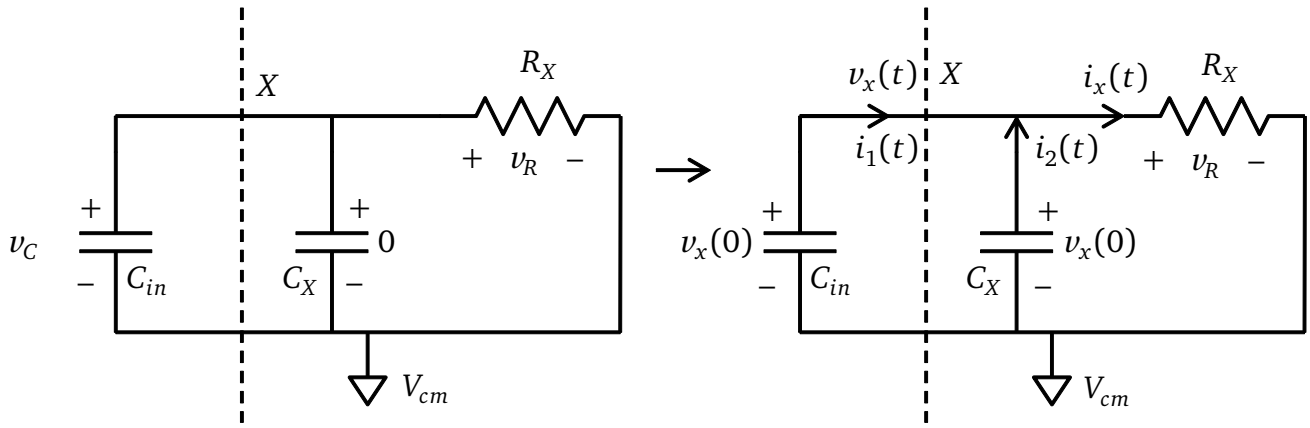


Figure 3.17: Connections at X port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

voltage level $v_x(0)$ then discharge over a time of T_{s1}, generating current $i_x(t)$ during this phase. Applying Kirchhoff law for the current at X we get:

$$i_x(t) = i_1(t) + i_2(t) \tag{3.46}$$

where $i_x(t)$, $i_1(t)$ and $i_2(t)$ are given in relation to the voltage $v_x(t)$ at X port as:

$$i_1(t) = -C_{in}\frac{\partial v_x(t)}{\partial t} \tag{3.47}$$

$$i_2(t) = -C_X\frac{\partial v_x(t)}{\partial t} \tag{3.48}$$

$$i_x(t) = \frac{v_x(t)}{R_X} \tag{3.49}$$

Substituting the currents $i_1(t)$ and $i_2(t)$ into the Equation 3.46 and rearranging the terms we get the following equation:

$$\frac{v_x(t)}{R_X} = -C_{in}\frac{\partial v_x(t)}{\partial t} - C_X\frac{\partial v_x(t)}{\partial t} \tag{3.50}$$

$$\frac{\partial v_x(t)}{\partial t} = -\frac{1}{R_X(C_{in}+C_X)}v_x(t) \tag{3.51}$$

Equation 3.51 is a derived from exponential function for the voltage $v_x(t)$ which has the form:

$$v_x(t) = Ae^{st} \tag{3.52}$$

where the term s is the solution of the Equation 3.51. To find s, we substitute Equation 3.52 in 3.51 and compare the terms to get the following:

$$\frac{\partial(Ae^{st})}{\partial t} = -\frac{1}{R_X(C_{in}+C_X)}Ae^{st} \tag{3.53}$$

$$s = -\frac{1}{R_X(C_{in}+C_X)} \tag{3.54}$$

To solve for A in Equation 3.52, we apply the initial conditions for the circuit. At the beginning of $t = 0$, the initial voltage on the capacitor C_{in} is $v_C = -v_{in}[(n-1)T_s]$. Therefore from Equation 3.52 we have:

$$A = v_x(0) \tag{3.55}$$

where $v_x(0)$ is the common voltage level given by:

$$v_x(0) = \frac{C_{in}v_C + C_X 0}{C_{in}+C_X} \tag{3.56}$$

$$v_x(0) = -\frac{C_{in}}{C_{in}+C_X} v_{in}[(n-1)T_s] \tag{3.57}$$

Applying the value of A and s into Equation 3.52, we get the final equation for the voltage variation at port X with respect to time as:

$$v_x(t) = v_x(0)e^{-\frac{t}{R_X(C_{in}+C_X)}} \tag{3.58}$$

$$v_x(t) = -\frac{C_{in}}{C_{in}+C_X} v_{in}[(n-1)T_s]e^{-\frac{t}{R_X(C_{in}+C_X)}} \tag{3.59}$$

From the voltage equation, the total charge transferred during a clock time of T_{s1} can be calculated using the following equation as:

$$\begin{aligned} \Delta Q_X|_{t=0}^{t=T_{s1}} &= Q_X(T_{s1}) - Q_X(0) \\ &= (C_{in}+C_X)v_x(T_{s1}) - (C_{in}+C_X)v_x(0) \end{aligned} \tag{3.60}$$

Applying Equation 3.59 to 3.60, we get the total charge lost at port X for the period of T_{s1} as:

$$\Delta Q_X = C_{in}v_{in}[(n-1)T_s](1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}}) \tag{3.61}$$

Equation 3.61 represents the total charge transferred from port X to port Z during the charge transfer phase $\phi_1[(n-1/2)T_s]$. Ideally the exponential term $e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}}$ in this equation should become zero at end of $\phi_1[(n-1/2)T_s]$. This can be achieved by choosing proper values for C_{in}, C_X and R_X in relation to charge transfer time T_{s1}.

Similar to the derivation for voltage $v_x(t)$, the equation for the current flowing through port X over time t due to the change in charge Q_X can be derived by applying Equation 3.59 to Equation 3.49. This gives:

$$\begin{aligned} i_x(t) &= C_{in}v_{in}[(n-1)T_s]e^{-\frac{t}{R_X(C_{in}+C_X)}}\left(-\frac{1}{R_X(C_{in}+C_X)}\right) \\ &= -\frac{C_{in}}{R_X(C_{in}+C_X)} v_{in}[(n-1)T_s]e^{-\frac{t}{R_X(C_{in}+C_X)}} \end{aligned} \tag{3.62}$$

At Port Z:
Equation 3.61 shows the total charge lost from C_{in} capacitor over a period of time T_{s1} during phase $\phi_1[(n-1/2)T_s]$. This charge is responsible for generating current $i_x(t)$ at X port as given in Equation 3.62. As shown in the macromodel any current at port X is conveyed to Z port, where it is multiplied by the frequency dependent current gain $\alpha(f_s)$ before it charges or discharges the C_{int} capacitor. This new charge (Q_{intn}) supplied to C_{int} capacitor from $i_z(t)$ current adds to the existing charge (Q_{inte}) on it from the previous charge transfer phase $\phi_1[(n-3/2)T_s]$. The newly added charge and the existing charge are affected by the Z port parasitics which lead to gain and loss errors.

In order to derive the final voltage on C_{int} capacitor at end of $\phi_1[(n-1/2)T_s]$, the causes leading to the losses in the newly added charge (Q_{intn}) and the existing charge (Q_{inte}) need to be analyzed. Then the equations for Q_{intn} and Q_{inte} can be derived independently and combined together in the end to get the final integrated voltage v_{int} on C_{int} capacitor. Figure 3.18 shows the connections at the Z port for the analysis below.

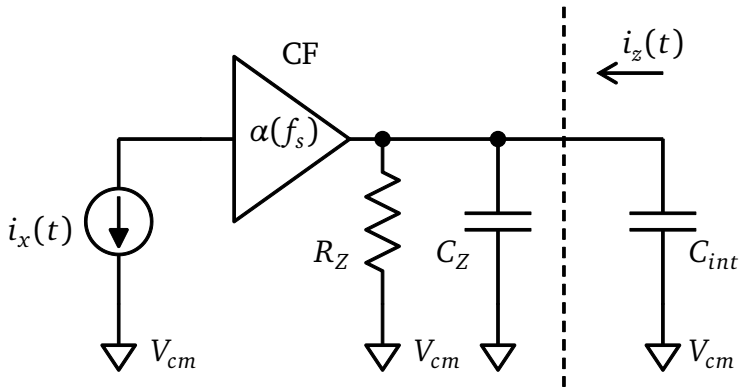


Figure 3.18: Connections at Z port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

- Errors in the existing charge Q_{inte}: The capacitor C_{int} carries some existing charge from the previous charge transfer phase. This existing charge is given by:

$$Q_{Z1} = C_{int}\, v_{int}[(n-1)T_s] \tag{3.63}$$

where $v_{int}[(n-1)T_s]$ is the voltage on C_{int} capacitor at the of the previous sample and hold phase $\phi_2[(n-1)T_s]$.

Similar to the analysis done in Figure 3.17 for the charged C_{in} capacitor which is connected in parallel with R_X and C_X, here we have a charged C_{int} capacitor connected in parallel with R_Z and C_Z. The equations derived for Figure 3.17 apply to this scenario as well, wherein the charge present on the C_{int} capacitor is lost through the R_Z resistor over the total charge transfer time of T_{s1}. Therefore the value of the existing charge at the end of this phase is given by:

$$\begin{aligned} Q_{inte} &= Q_{Z1} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \\ &= C_{int}\, v_{int}[(n-1)T_s] e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \end{aligned} \tag{3.64}$$

where Equation 3.63 has been substituted to get the final value of existing charge.

- Errors in the added charge Q_{intn}: Apart from the existing charge, an additional charge is added to the Z port in the form of current flow generated due to the current relation between X and Z ports. The relation between port Z current and X port current is given as:

$$i_z(t) = |\alpha(f_s)| i_x(t) = \alpha_0 i_x(t) \tag{3.65}$$

where $i_x(t)$ is given by Equation 3.62 and $|\alpha(f_s)|$ is the approximate magnitude of the current gain at sampling frequency. Similar to the voltage gain if we assume that the sampling frequency of the SC integrator is less than 3dB cutoff ($f_s << f_\alpha$), then the current gain is simply given by the value at low frequency which is $|\alpha(f_s)| = \alpha_0$.

$$|\alpha(f_s)| = \frac{\alpha_0}{\sqrt{1 + \left(\frac{f_s}{f_\alpha}\right)^2}} = \alpha_0 \tag{3.66}$$

As the current is directly to proportional to the rate of change of charge, the following charge relation can be established:

$$Q_{Z2} = \alpha_0 \Delta Q_X \tag{3.67}$$

where Q_{Z2} is the total new charge flowing into the Z port parasitics and the C_{int} capacitor. Similar to the existing charge, as this charge is being added to C_{int} and C_Z capacitors, a part of it is also lost through the R_Z resistor. This rate of loss is exponential and is controlled by the charge transfer time T_{s1} and the time constant formed by resistor R_Z and total capacitance $(C_{int}+C_Z)$ at Z port. Therefore the total new charge added during charge transfer phase within the time of $t = T_{s1}$, is given by:

$$\begin{aligned} Q_{intn} &= Q_{Z2} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \\ &= \alpha_0 \Delta Q_X e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \\ &= \alpha_0 C_{in} v_{in}[(n-1)T_s](1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}}) e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \end{aligned} \tag{3.68}$$

where Equations 3.61 and 3.67 have been substituted to get the final value of the newly added charge.

The total charge Q_{int} present on the parasitic C_Z and C_{int} capacitor at the end of charge transfer phase $\phi_1[(n-1/2)T_s]$ is given as:

$$Q_{int} = (C_{int} + C_Z) v_{int}[(n-1/2)T_s] \tag{3.69}$$

where $v_{int}[(n-1/2)T_s]$ is the final value of integrated voltage at the end of this phase.

Since the value of the total charge Q_{int} is given by the summation of newly added charge Q_{intn} and existing charge Q_{inte}, the Equations 3.64, 3.68 and 3.69 can be combined together to get the value of integrated voltage $v_{int}[(n-1/2)T_s]$ as:

$$Q_{int} = Q_{intn} + Q_{inte} \tag{3.70}$$

$$(C_{int}+C_Z)v_{int}[(n-1/2)T_s] = \alpha_0 C_{in} v_{in}[(n-1)T_s](1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} + C_{int} v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \tag{3.71}$$

$$v_{int}[(n-1/2)T_s] = \frac{\alpha_0 C_{in}}{(C_{int}+C_Z)} v_{in}[(n-1)T_s](1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} + \frac{C_{int}}{(C_{int}+C_Z)} v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \tag{3.72}$$

Time instant $\phi_2[nT_s]$:

During this sample and hold phase, the circuit is connected as shown in Figure 3.15. Figure 3.19 shows the connections including CCII non-idealities. Similar to the scenario where the charge present on C_{in} capacitor decays through the X port parasitics R_X and C_X during $\phi_1[(n-1/2)T_s]$, here the integrated voltage $v_{int}[(n-1/2)T_s]$ present on the capacitor C_{int} is lost through the Y port parasitics R_Y and C_Y over a time T_{s2}. Therefore applying Equation 3.59 to this scenario we get the voltage at Y port as:

$$v_y(t) = \frac{C_{int}}{C_{int}+C_Y} v_{int}[(n-1/2)T_s]e^{-\frac{t}{R_Y(C_{int}+C_Y)}} \tag{3.73}$$

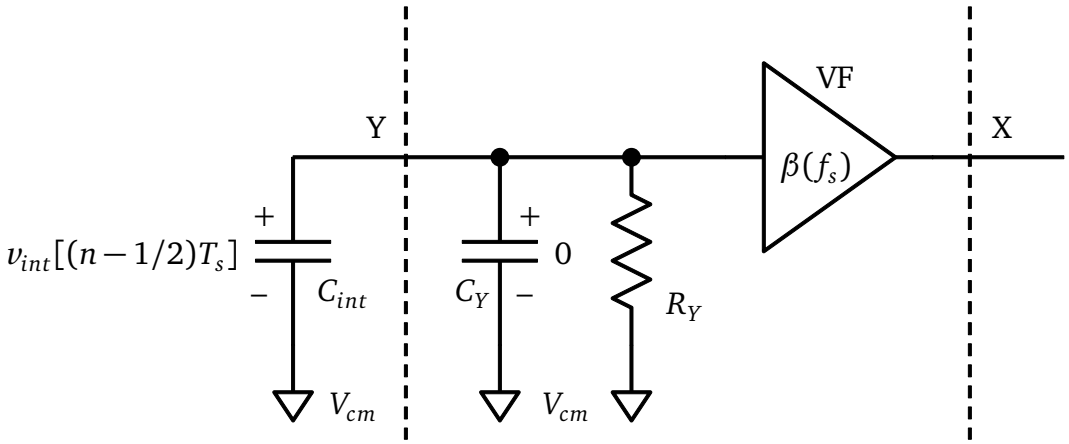


Figure 3.19: CCII SC integrator during the hold phase $\phi_2[nT_s]$.

The previous equation includes the effect of finite R_Y resistance at Y port which causes the charge from C_{int} to slowly discharge over a period of T_{s2}. It is possible to completely remove the exponential loss of the charge if the gate of MOS transistor is used as input. In this case the resistance R_Y becomes infinite. However for the purpose of presenting a complete analysis this exponential loss is included as it is in its current form. The final value of integrated voltage $v_{int}[nT_s]$ at the end of this phase $\phi_2[nT_s]$ is obtained by setting $t = T_{s2}$ to the Equation 3.73. Therefore we get:

$$v_{int}[nT_s] = v_y(T_{s2}) = \frac{C_{int}}{C_{int}+C_Y} v_{int}[(n-1/2)T_s]e^{-\frac{T_{s2}}{R_Y(C_{int}+C_Y)}} \tag{3.74}$$

This integrated voltage $v_{int}[nT_s]$ obtained from previous equation is sent to the next stage sampling capacitors through the CCII buffer which multiplies its own gain $|\beta(f_s)|$ given by Equation 3.45. Therefore, the final value of output voltage $v_{out}[nT_s]$ at the end of this phase is given by:

$$v_{out}[nT_s] = |\beta(f_s)| v_{int}[nT_s] = \beta_0 v_{int}[nT_s] \tag{3.75}$$

Substituting Equations 3.44, 3.72 and 3.74 in 3.75, we get the value of the integrated output voltage during this phase as:

$$\begin{aligned} v_{out}[nT_s] = \Bigg(& \frac{C_{in}}{C_{int}+C_Z}\beta_0\alpha_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})v_{in}[(n-1)T_s] \\ & + \frac{C_{int}}{C_{int}+C_Z}\beta_0 v_{int}[(n-1)T_s]\Bigg)\frac{C_{int}}{C_{int}+C_Y}e^{-\frac{T_{s2}}{R_Y(C_{int}+C_Y)}}e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \end{aligned} \tag{3.76}$$

$$\begin{aligned} v_{out}[nT_s] = & \left(\frac{C_{in}}{C_{int}}\beta_0\alpha_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})v_{in}[(n-1)T_s] + v_{out}[(n-1)T_s]\right)\times \\ & \left(\frac{C_{int}}{C_{int}+C_Y}e^{-\frac{T_{s2}}{R_Y(C_{int}+C_Y)}}\frac{C_{int}}{C_{int}+C_Z}e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}}\right) \end{aligned} \tag{3.77}$$

Applying Z domain transformation to the previous equation and writing the transfer function of the integrator in terms of its gain coefficient and the ITF gives:

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} ITF_{cc}(z) \tag{3.78}$$

where the non-ideal ITF which depends on the CCII and buffer non-idealities is given by:

$$ITF_{cc}(z) = Gain_{cc}\frac{z^{-1}}{1-z^{-1}z_{cc}} \tag{3.79}$$

Comparing the previous $ITF_{cc}(z)$ with the ideal integrator transfer function $(z^{-1}/(1-z^{-1}))$, it is observed that CCII non-idealities introduce a gain error and a shift in the pole of the transfer function from DC (z=1), similar to the Op-Amp, given by:

$$z_{cc} = \frac{C_{int}}{(C_{int}+C_Z)}e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}}\frac{C_{int}}{(C_{int}+C_Y)}e^{-\frac{T_{s2}}{R_Y(C_{int}+C_Y)}} \tag{3.80}$$

$$Gain_{cc} = \beta_0\alpha_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})z_{cc} \tag{3.81}$$

3.3.2.3 Design Conditions to get Comparable Performance with Existing CCII Integrator

The CCII SC integrator shown in Figure 3.14 was analyzed with respect to CCII non-idealities in the previous section. In order to check the design feasibility of the existing CCII integrator it is necessary to determine the set of conditions under which it gives comparable performance to Op-Amp based integrator. Comparison of the two ITFs gives us the following conclusions:

- Finite gain of the Op-Amp gives rise to gain and loss errors in the ITF. For a minimum gain of $A_{DC} \geq 45dB$, the finite gain of the Op-Amp gives rise to negligible gain and loss errors. This translates to good noise shaping characteristics for a 2nd-order modulator, as illustrated in Figure 3.12.

- Finite bandwidth of the Op-Amp gives rise to just gain error in the ITF, considering large gains A_{DC}. For unity gain bandwidths significantly larger than the sampling frequency ($f_\mu > 10f_s$), the finite bandwidth of Op-Amp gives rise to negligible gain error.

- Unlike the Op-Amp, the non-idealities of the CCII have a more significant impact on the CCII ITF. This as will be shown next, translates to more stringent requirements on the CCII properties and associated sampling and integration capacitors in order to achieve comparable performance.

- Unlike the Op-Amp where having a high gain reduces the effect of other parasitics such as C_p, there is no equivalent parameter for CCII, whose adjustment reduces the effect of other CCII non-idealities. Hence optimizing the CCII integrator requires simultaneous adjustment of all CCII properties to achieve comparable performance.

- In the case of the CCII, gain and loss errors depend on the sampling clock period ($T_{s1} = T_{s2} \approx T_s/2$) or inversely the sampling frequency (f_s) whereas in the case of Op-Amp with finite bandwidth, only the gain error depends on the sampling frequency.

- As the sampling frequency approaches the unity gain bandwidth of Op-Amp, the gain error increases as seen from the exponential term in Equation 3.30. A similar increase in sampling frequency of the CCII, assuming all other non-idealities remain the same, has the opposite effect of reducing loss errors as seen from the exponential terms in Equations 3.80 and 3.81.

In order to design a comparable CCII integrator similar to Op-Amp, it is necessary to compare the gain and pole location of the two ITFs. From this comparison the necessary minimum or maximum limits of capacitors C_{in}, C_{int}, CCII voltage and current gain and sampling frequency f_s can be found in relation to the CCII non-idealities.

For the design feasibility analysis, we assume that a noise floor above -90dB is required when the integrator is used in a 2nd order modulator. Considering this requirement and neglecting finite bandwidth effects, the Op-Amp needs a minimum gain of $A_{DC} > 45dB$ as seen in Figure 3.12 for a gain coefficient of $C_{in}/C_{int} = 1$. In order to achieve a similar noise floor with an CCII integrator, $Gain_{cc}$ and z_{cc} should have values similar to the Op-Amp $Gain_{op}$ and z_{op}.

In the case of Op-Amp, the pole of the Op-Amp ITF as shown in Equation 3.28 has a value of $z_{op} = (A_{DC} + 1)/(A_{DC} + 2) > 0.9944$ which is an error of 0.56% from the ideal value of 1.

Assuming a similar criterion for the pole of CCII ITF, we can derive the following conditions from Equation 3.80:

$$z_{cc} > 0.9944 \tag{3.82}$$

$$\frac{C_{int}}{(C_{int}+C_Z)} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \frac{C_{int}}{(C_{int}+C_Y)} e^{-\frac{T_{s2}}{R_Y(C_{int}+C_Y)}} > 0.9944 \tag{3.83}$$

In the analysis, the Y port is assumed to have a finite resistance if the translinear CCII is used. Further simplification of the design requirement can be done if it is assumed that the gate of a transistor is used as input, in which case the resistance R_Y approaches infinity. Thus Equation 3.83 can be reduced to:

$$\frac{C_{int}}{(C_{int}+C_Z)} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_Z)}} \frac{C_{int}}{(C_{int}+C_Y)} > 0.9944 \tag{3.84}$$

The location of the pole is determined by the ratio of integration and parasitic capacitors at Y and Z ports, as well as the exponential term which depends on Z port parasitics and integration capacitor. Out of the two terms in the pole equation, the exponential term is important as it also defines maximum limit on the charge transfer time for the CCII integrator. Rearranging Equation 3.84 further to derive an extended set of conditions we get:

$$T_{s1} < R_Z(C_{int}+C_Z)\log_e\left(\frac{C_{int}^2}{0.9944(C_{int}+C_Z)(C_{int}+C_Y)}\right) \tag{3.85}$$

Assuming the $C_{int} >> (C_Z C_Y)$ we get

$$T_{s1} < R_Z(C_{int}+C_Z)\log_e\left(\frac{C_{int}}{0.9944(C_{int}+C_Z+C_Y)}\right) \tag{3.86}$$

In order for the time T_{s1} to be a positive value greater than zero it becomes necessary that the $\log_e$ term on the right side is greater than zero or alternatively the term inside the $\log_e$ is greater than one. Therefore applying this condition we get from the $\log_e$ term:

$$\frac{C_{int}}{0.9944(C_{int}+C_Y+C_Z)} > 1 \tag{3.87}$$

$$C_{int} > 178(C_Y+C_Z) \tag{3.88}$$

The previous equation gives the minimum value for C_{int} capacitor when compared to parasitics C_Y and C_Z. From Equation 3.86, it is observed that a large value for C_{int} translates into larger charge transfer time which is useful when low sampling frequencies are used. However C_{int} cannot be made excessively large since it consumes too much area and requires more current handling capability from the CCII. Assuming a multiplying factor $g_c' > 1$ which is multiplied with the minimum value of C_{int} we get:

$$C_{int} = g_c' 178(C_Y+C_Z) \tag{3.89}$$

Substituting the value of C_{int} in Equation 3.86 and reducing it we get:

$$T_{s1} < R_Z(g_c'178(C_Y + C_Z) + C_Z)\log_e\left(\frac{g_c'178}{0.9944(g_c'178+1)}\right) \tag{3.90}$$

Assuming g_c' is large, the absolute maximum value of the $\log_e$ term in the previous equation can be derived as:

$$\log_e\left(\frac{g_c'178}{0.9944(g_c'178+1)}\right) \approx \log_e\left(\frac{1}{0.9944}\right) \approx \frac{1}{178} \tag{3.91}$$

Applying this reduction to Equation 3.90 we get the maximum upper limit of charge transfer time as:

$$T_{s1} < g_c'R_Z(C_Y + C_Z) \tag{3.92}$$

In the previous steps the conditions necessary for having a pole location similar to that of Op-Amp integrator were analyzed and derived in Equations 3.89 and 3.92. Using a similar principle, the gain error is analyzed next. The gain of the Op-Amp ITF, $Gain_{op}$ as shown in Equation 3.29 has a value of $A_{DC}/(A_{DC}+2) > 0.9889$ which is an error of 1.11% from the ideal value of 1. Assuming a similar criterion for the gain of CCII ITF, we get the following conditions from Equation 3.81:

$$Gain_{cc} > 0.9889 \tag{3.93}$$

$$\beta_0\alpha_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}})z_{cc} > 0.9889 \tag{3.94}$$

Applying Equation 3.82 to 3.93, we get:

$$\beta_0\alpha_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_X)}}) > 0.9944 \tag{3.95}$$

$Gain_{cc}$ depends on the values of current gain and voltage gain of the CCII as well as the exponential term which depends on X port parasitics and sampling capacitor. The exponential term in the previous equation signifies the error due to incomplete discharge of C_{in} and C_X capacitors. From the previous equation we observe that if the charge transfer time is very large such that $T_{s1} >> 10R_X(C_{in} + C_X)$, the exponential term vanishes and right side of the condition 0.9944 remains relatively unchanged. However assuming that this is not satisfied, the exponential term also contributes to gain error. Rearranging the terms in the previous equation we get the lower limit of the charge transfer time as:

$$T_{s1} > R_X(C_{in} + C_X)\log_e\left(\frac{\beta_0\alpha_0}{\beta_0\alpha_0 - 0.9944}\right) \tag{3.96}$$

In order for the charge transfer time to be positive it becomes necessary that the $\log_e$ term is greater than zero or alternatively the term inside $\log_e$ is greater than 1. This is true if the value of the denominator in the $\log_e$ term is positive. Therefore we have:

$$\beta_0\alpha_0 > 0.9944 \tag{3.97}$$

Equation 3.96 shows that the lower limit on the charge transfer time can be made very small, if the terms $\beta_0\alpha_0$ are larger than the minimum value given by Equation 3.97. However since the value of gains depend on transistor sizes, changing their sizes also changes the parasitics at Y, X and Z ports. For example, increasing $\alpha_0 = 2$ makes the port Z resistance approximately $R_Z/2$. Assuming simple topologies and a factor g_a' which is greater than 1 by a small margin we get:

$$\beta_0\alpha_0 = g_a' 0.9944 \tag{3.98}$$

Applying the previous equation and the value of C_{in} from the Equation 3.89 by using the coefficient condition $C_{in} = C_{int}$ to Equation 3.96 we get the lower limit of the charge transfer time T_{s1} in relation to the parasitics as:

$$T_{s1} > 178 g_c' R_X (C_Y + C_Z) \log_e \left(\frac{g_a'}{g_a' - 1} \right) \tag{3.99}$$

Equations 3.92 and 3.99 give lower and upper limits of charge transfer time which depends on the CCII parasitics. T_{s1} and T_{s2} are the pulse widths of the two phase non overlapping clock and they have a value of approximately ($T_{s1}, T_{s2} \approx T_s/2$) where $T_s = 1/f_s$ is the sampling clock period. Substituting ($T_{s1}, T_{s2} \approx T_s/2$) and combining Equations 3.92 and 3.99 we get:

$$178 g_c' R_X (C_Y + C_Z) \log_e \left(\frac{g_a'}{g_a' - 1} \right) < T_{s1} < g_c' R_Z (C_Y + C_Z) \tag{3.100}$$

$$356 g_c' R_X (C_Y + C_Z) \log_e \left(\frac{g_a'}{g_a' - 1} \right) < T_s < 2 g_c' R_Z (C_Y + C_Z) \tag{3.101}$$

$$\frac{1}{2 g_c' R_Z (C_Y + C_Z)} < f_s < \frac{1}{356 g_c' R_X (C_Y + C_Z) \log_e \left(\frac{g_a'}{g_a' - 1} \right)} \tag{3.102}$$

where $g_c' > 1$ and $g_a' > 1$.

Equations 3.89, 3.98, 3.101 and 3.102 need to be satisfied to achieve a performance comparable to Op-Amp integrator. Compared to the Op-Amp integrator where the sizes of C_{in} and C_{int} play no big role in defining gain and loss errors, the sizes of C_{in} and C_{int} capacitors need to be excessively large for CCII integrator in order to minimize these errors. Based on Equation 3.89 we observe that the value of C_{int} goes above few tens of pico farads for values of parasitics as small as few femto farads and using a multiplier g_c' larger than 1. As the parasitics increase, C_{int} becomes further high. Implementing such high value capacitors on chip requires huge area, while charging and discharging such capacitors in turn requires CCII with huge current source and sink capabilities.

Unlike the Op-Amp integrator which can work from near DC sampling frequencies upto its 3dB bandwidth, the CCII integrator gives good performance only when the sampling frequency lies in the range given by Equation 3.102. Ignoring the common terms in the equation, it is observed that the lower frequency limit depends on the inverse of Z port parasitic resistance and upper limit depends on the inverse of X port parasitic resistance. In order for the sampling frequency range to exist, the value of R_Z resistor must be many orders of magnitude higher than

R_X such that the condition ($R_Z >> 178R_X \log_e\left(\frac{g_a'}{g_a'-1}\right)$) is satisfied. If the CCII does not satisfy this requirement then there exists no sampling frequency where the CCII integrator can be used as an integrator.

The introduction of this additional requirement between R_Z and R_X poses a challenge to designers since achieving it is not so easy in advanced technology nodes. This can be explained as follows. In order for the sampling frequency to exist, the requirement is that resistance R_Z needs to have a high value and resistance R_X needs to have as small a value as possible. However this requirement is contradictory. For example, consider the equations given below for small signal parasitic resistances at X and Z ports of the translinear CCII topology given in Figure 3.5b.

$$R_X \approx \frac{1}{g_{mN} + g_{mP} + g_{dsN} + g_{dsP}} \approx \frac{1}{g_{mN} + g_{mP}} \propto \frac{1}{(I_{DSN}, I_{SDP})} \tag{3.103}$$

$$R_Z \approx \frac{r_{dsN} r_{dsP}}{r_{dsN} + r_{dsP}} \propto \frac{1}{(I_{DSN}, I_{SDP})} \tag{3.104}$$

where it is assumed that a tight matching constraint requires PMOS and NMOS transistors to have similar parameters g_{dsN}, g_{dsP}, g_{mN}, g_{mP} which are related to bias currents $I_{DSN} = I_{SDP}$, voltages $V_{GSN} = V_{SGP}$, $V_{DSN} = V_{SDP}$ and transistor parameters as:

$$g_{mN} = \frac{2I_{DSN}}{V_{GSN} - V_{TN}} \tag{3.105}$$

$$r_{dsN} = \frac{1}{g_{dsN}} = \frac{\frac{1}{\lambda_N} + V_{DSN}}{I_{DSN}} \tag{3.106}$$

$$g_{mP} = \frac{2I_{SDP}}{V_{SGP} + V_{TP}} \tag{3.107}$$

$$r_{dsP} = \frac{1}{g_{dsP}} = \frac{\frac{1}{\lambda_P} + V_{SDP}}{I_{SDP}} \tag{3.108}$$

The equations for transistor transconductance and output resistance show a direct and inverse dependence on bias current (I_{DSN}, I_{DSP}). Thus any increase or decrease in bias current also decreases or increases parasitics R_Z and R_X respectively. This applies to all the CCII topologies in literature. Assuming the CCII is used only at lower sampling frequencies in the range of few hundred kHz to few MHz, the main problem comes from R_Z resistance. This is because to achieve such low sampling frequencies, R_Z above few $M\Omega$ is needed. In advanced technology nodes of 130nm and beyond, it is very difficult to achieve such high R_Z values and high current handling capabilities at the same time to drive large capacitances, even when using cascode techniques at the Z port.

Equations 3.89, 3.98, 3.101 and 3.102 give the design conditions under which the CCII integrator gives a performance comparable to Op-Amp integrator. This derivation is valid under the assumption that the CCII has a wide linear operating range, bandwidth and slew rate for the currents and voltages. If slew rate effects are considered then the time (T_{s1}, T_{s2}) available for

settling of the input and output signals is reduced, which results in the reduction of sampling frequency range given by Equation 3.102. Similarly any non-linearity in the operating range of currents and voltages results in a non-linearity of current gain α_0 and voltage gain β_0 which introduces harmonics in the output.

If a better noise floor above -100dB is needed for low noise high resolution applications, then higher Op-Amp gains are needed. Following a similar procedure described in Equations 3.82 till 3.102, Table 3.1 shows the corresponding relations for integration capacitor, CCII gains and sampling frequency range for the CCII integrator in relation to different noise floors and equivalent Op-Amp gains.

Table 3.1: Design conditions for various noise floors

Op-Amp Gain (dB)	Noise Floor (dB)	Minimum C_{int}, C_{in}	Minimum $\beta_0\alpha_0$	Sampling Frequency f_s
40	-80	$101g_c'(C_Y+C_Z)$	0.9901	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{202g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$
45	-90	$178g_c'(C_Y+C_Z)$	0.9944	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{356g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$
50	-100	$318g_c'(C_Y+C_Z)$	0.99684	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{636g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$
55	-110	$564g_c'(C_Y+C_Z)$	0.99824	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{1128g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$
60	-120	$1001g_c'(C_Y+C_Z)$	0.9994	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{2002g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$
65	-130	$1780g_c'(C_Y+C_Z)$	0.99944	$\left[\frac{1}{2g_c'R_Z(C_Y+C_Z)}, \frac{1}{3560g_c'R_X(C_Y+C_Z)\log_e\left(\frac{g_a'}{g_a'-1}\right)}\right]$

Figure 3.20 shows the minimum value of the integration capacitor against various parasitics $C_Y + C_Z$ for achieving various comparable Op-Amp gains. It is seen that as better gains are needed the value of C_{int} increases. For very low sampling frequencies in the range of kHz the factor g_c or R_Z needs to very high, which makes the value of C_{int} not integrable in CMOS or leads to very strict requirements on CCII. Figure 3.21 shows the required values of R_Z for achieving various lower sampling frequency limits and varying parasitics $C_Y + C_Z$. As illustrated, the requirements on R_Z go into $M\Omega$ to achieve lower limits in the range of kHz.

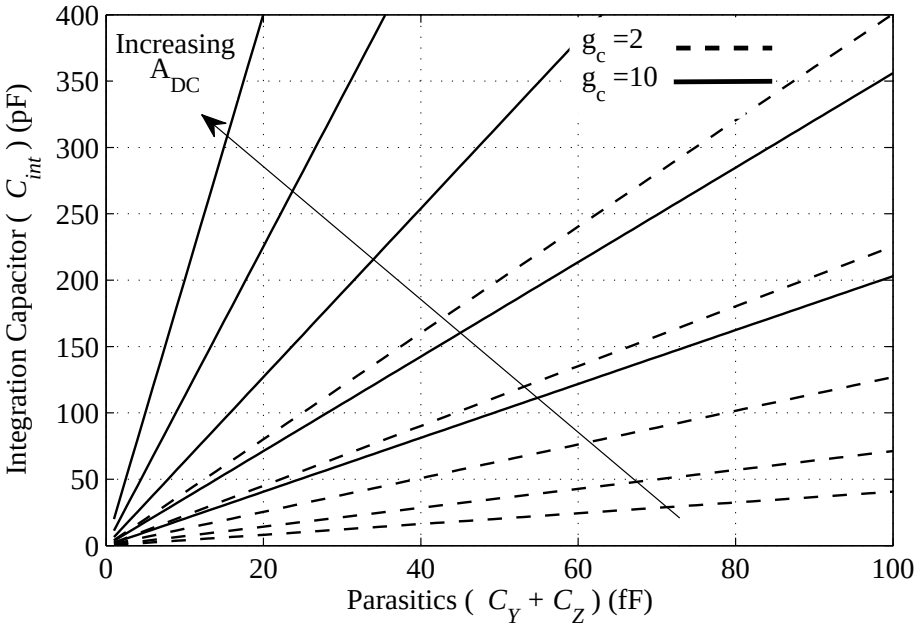


Figure 3.20: Required C_{int} for achieving comparable Op-Amp gain A_{DC}={40,45,50,55,60} plotted against different parasitics $(C_Y + C_Z)$ with g_c={2,10}.

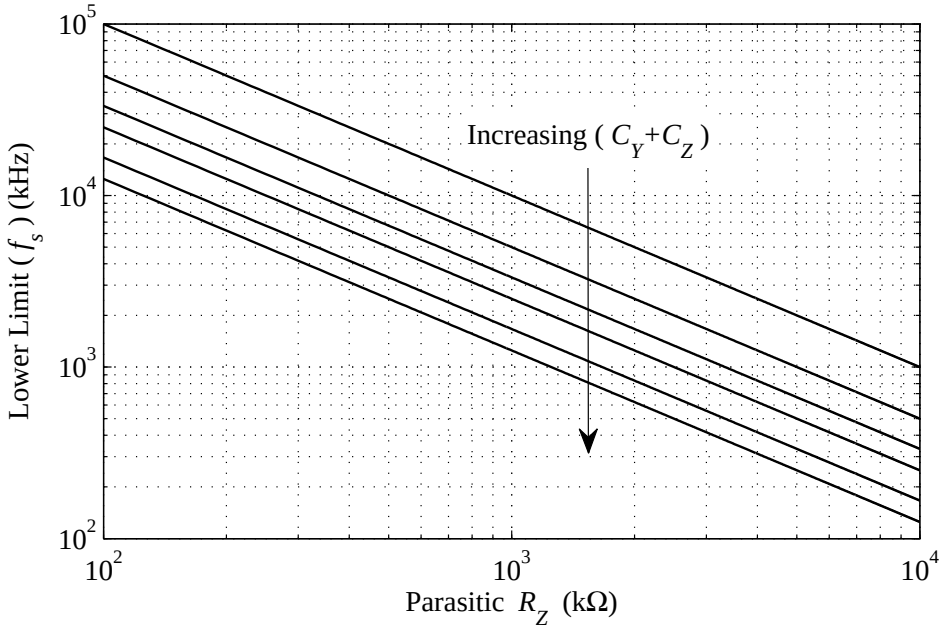


Figure 3.21: Sampling frequency lower limit plotted against various R_z for parasitic values of $(C_Y + C_Z)$={25f,50f,75f,100f,150f,200f}, $g_c = 2$ and comparable gain of $A_{DC} \geq 45$.

Figure 3.22 shows the required values of R_X for achieving various upper sampling frequency limits and varying parasitics $C_Y + C_Z$. As illustrated, the requirements on R_X go into few hundred Ω range to achieve upper limits in the range of MHz. If we consider for instance a sampling frequency of 2MHz and select lower and upper limits of 1MHz and 3MHz respectively, then this translates into maximum $R_X = (250\Omega, 500\Omega)$ and minimum $R_Z = (250k\Omega, 500k\Omega)$ for $C_Y + C_Z = (200f, 100f)$. While these CCII values can be achieved in practice, the values required for

$C_{int} = (720p, 360p)$ however make the existing CCII integrator unrealizable in integrated form in CMOS technologies. It is seen that lowering $g_c = 2$ to get lower $C_{int} = (140p, 70p)$ results in a more strict design requirement from the CCII that is a maximum $R_X = (450\Omega, 900\Omega)$, minimum $R_Z = (1.3M\Omega, 2.6M\Omega)$ for $C_Y + C_Z = (200f, 100f)$.

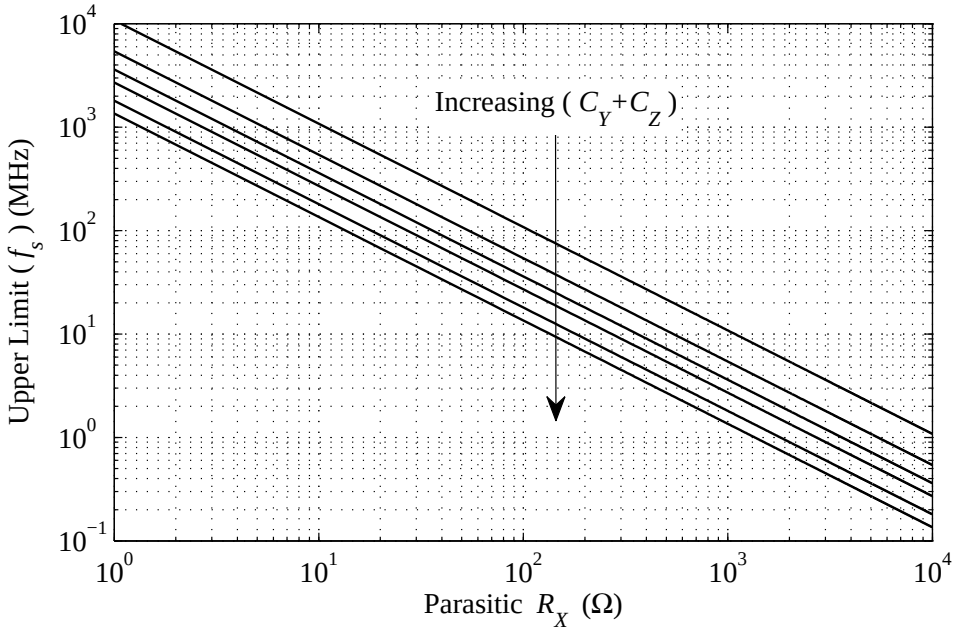


Figure 3.22: Sampling frequency upper limit plotted against various R_x for parasitic values of $(C_Y + C_Z)$={25f,50f,75f,100f,150f,200f}, $g_c = 2$, $g_a = 1/0.9944$ and comparable gain of $A_{DC} \geq 45$.

3.4 Proposed Fully Integrable CCII Integrators

In the previous section, an existing CCII integrator and its design feasibility were analyzed to achieve a performance comparable to an Op-Amp based integrator. It is observed that the existing architecture has some major drawbacks in the form of imposing severe requirements on the values of circuit capacitors, CCII non-idealities and parasitics, which are quite difficult to achieve. For example from Equation 3.102 it is observed that in order to achieve a lower sampling limit in the range of few hundred kHz, the value of parasitic R_Z needs to be in the range of few tens of MΩ assuming the parasitics $(C_Y + C_Z)$ are in the range of few femtofarads. In advanced technology nodes, it is very difficult to achieve such large values for R_Z resistance, unless transistor lengths are made extraordinarily large and widths small.

Even otherwise, assuming such large transistors can be implemented, a myriad of other problems arise such as the loss in the 3dB current and voltage bandwidth, higher R_X due to the interdependence of these parameters on the transistor width and length. Therefore it becomes necessary to find a means of delinking the CCII non-idealities from one another such that one CCII property can be improved without affecting the others significantly.

In this section a single ended and fully differential CCII integrator architecture will be introduced, which provides better performance in comparison to the existing CCII integrator. This will be shown by deriving the design conditions for the single ended and fully differential ar-

chitecture which are then compared with the design conditions of the existing integrator. The concept of predistortion and memory compensation will be introduced. It will be shown in the comparison that the design conditions for the proposed CCII integrators provide a more relaxed requirement on the non-idealities and parasitics of the CCII, making it realizable as an integrated circuit in advanced CMOS technologies.

3.4.1 Wideband Single Ended CCII Integrator

Figure 3.23 shows the single ended version of the proposed CCII integrator. Some of the main differences between the proposed integrator and the previous configuration are:

- Segregation of buffering and integration phases using two blocks. Unlike the existing configuration, the proposed integrator uses the CCII only for the charge transfer phase. For transferring the integrated voltage onto the next stage load capacitors, a separate buffer derived using the voltage mode property of Y and X ports of CCII is used.
- Use of a separate unity buffer to charge the next stage sampling and load capacitors. The buffer provides high current drive and very small output resistance, so that higher loads can be driven in shortest possible time.
- A separate buffer allows use of CCII with low power requirements. Low power CCII uses smaller transistors since they have small currents flowing through them. Smaller transistors and lower currents translate to smaller parasitics C_Y, C_X and C_Z as well as higher values for R_Z resistor. This is especially useful when the architecture is extended to a fully differential architecture in the next section where the circuit elements and power requirements also double.
- Capability to operate over a wide sampling frequency range due to the lower interdependence of the CCII non-idealities.
- Introduction of a new capacitor called C_{comp} for the memory compensation technique. It will be seen later from the design feasibility analysis of this integrator that C_{comp} capacitor substantially improves the CCII integrator performance by lowering loss errors and requirements on the CCII non-idealities.
- Predistortion of the C_{int} capacitor to correct gain errors.

Similar to the analysis done in the previous section, the proposed CCII integrator will be analyzed with respect to the CCII non-idealities. The analysis will be done as before at three time instants ($\phi_2[(n-1)T_s]$, $\phi_1[(n-1/2)T_s]$, $\phi_2[nT_s]$). All the conditions that were used for the earlier analysis apply to this scenario as well. Similar to the CCII non-idealities, the voltage buffer derived from the CCII Y and X ports used for buffering of integrated charge also presents a non-ideal voltage transfer function and a parasitic input capacitance C_{buf} which need to be considered during the analysis. If we assume a simple class AB topology for the voltage buffer, the frequency response of the buffer can be approximated by a single pole transfer function as:

$$\kappa(s) = \frac{v_{out}}{v_{int}} = \frac{\kappa_0}{1 + s/\omega_\kappa} \tag{3.109}$$

where κ_0 is the buffer gain at DC and $\omega_\kappa = 2\pi f_\kappa$ is the -3dB bandwidth.

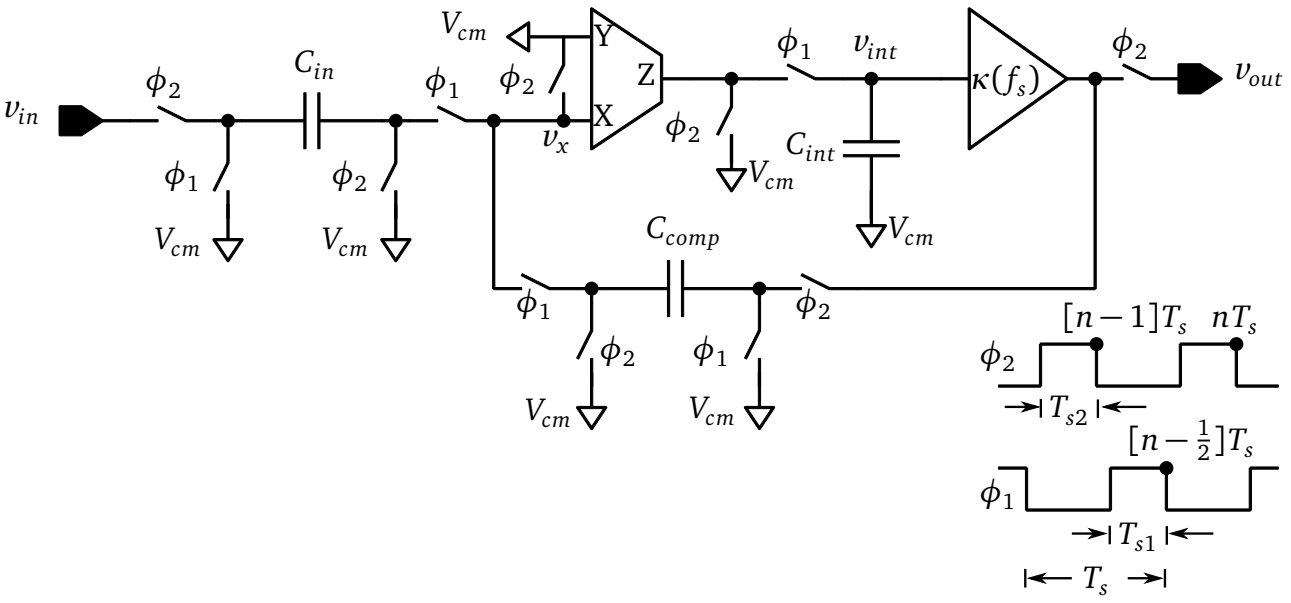


Figure 3.23: Proposed CCII SC integrator with separate unity buffer.

Time instant $\phi_2[(n-1)T_s]$:

The circuit is connected as shown in Figure 3.24. During this hold phase, the buffer multiplies its own frequency dependent gain $\kappa(f_s)$ with the integrated voltage and sends it to the output which consists of the next stage sampling capacitors and compensation capacitor C_{comp}. At the same time, the input voltage is being sampled onto input capacitor C_{in}.

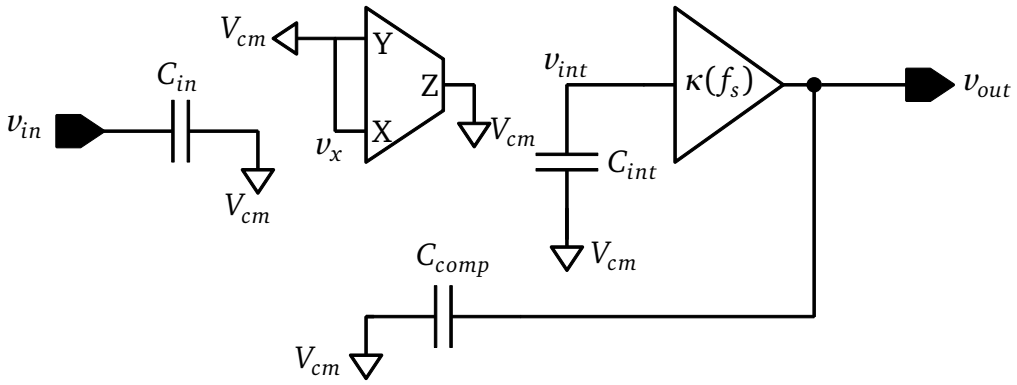


Figure 3.24: Proposed CCII SC integrator during the sample and hold phase $\phi_2[(n-1)T_s]$.

The equation for sampled charge Q_{in}, compensation charge Q_{comp}, integrated charge Q_{int} and output voltage at the end of $\phi_2[(n-1)T_s]$ can be written as:

$$Q_{in} = C_{in}(-v_{in}[(n-1)T_s]) \tag{3.110}$$

$$Q_{int} = (C_{int} + C_{buf})v_{int}[(n-1)T_s] \tag{3.111}$$

$$Q_{comp} = C_{comp}(-v_{out}[(n-1)T_s]) \tag{3.112}$$

$$v_{out}[(n-1)T_s] = |\kappa(f_s)|v_{int}[(n-1)T_s] = \kappa_0 v_{int}[(n-1)T_s] \tag{3.113}$$

where C_{buf} is the buffer input capacitance and $|\kappa(f_s)|$ is the approximate magnitude of the buffer gain at the sampling frequency. If we assume that the sampling frequency of the SC integrator is less than the 3dB cutoff ($f_s << f_\kappa$), then the voltage gain is simply given by the value at low frequency which is $|\kappa(f_s)| = \kappa_0$.

$$|\kappa(f_s)| = \frac{\kappa_0}{\sqrt{1+\left(\frac{f_s}{f_\kappa}\right)^2}} = \kappa_0 \tag{3.114}$$

Similar to the existing integrator, in the proposed integrator the integration capacitor C_{int} is disconnected from the Z port to prevent its discharge through parasitic R_Z resistor and to maintain a constant voltage for the voltage buffer to present at the output. All the three ports of the CCII are autozeroed to remove any stray charge on the CCII parasitics during the charge transfer or the integration phase.

Time instant $\phi_1[(n-1/2)T_s]$:

The circuit is connected as shown in Figure 3.25. The Y port is connected to common mode voltage V_{cm} and provides a forced virtual ground at X port due to the voltage relationship between Y and X ports. The Y port parasitics do not play any role since they are always connected to common mode voltage V_{cm}. Similar to the existing integrator this phase introduces loss and gain errors, both of which are caused by the CCII. The cause of these errors was explained in detail previously during the analysis of the existing integrator and they apply to this proposed integrator as well.

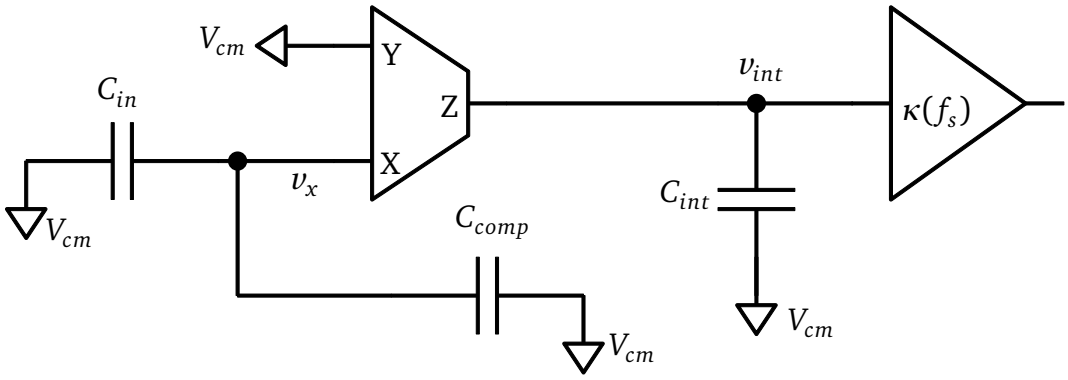


Figure 3.25: Proposed CCII SC integrator during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

To derive the total charge transferred from X to Z port during a time of T_{s1}, the circuit needs to be analyzed at port X and port Z independently to derive the various relationships. These relationships are then equated in the end to get the complete transfer function of the CCII integrator.

At Port X:

Figure 3.26 shows the connections at the X port including the CCII parasitics during phase ϕ_1. It is already known that at the end of previous sample and hold phase $\phi_2[(n-1)T_s]$, a voltage

of $v_{Ci} = -v_{in}[(n-1)T_s]$ exists on capacitor C_{in} and a voltage of $v_{Cc} = -v_{out}[(n-1)T_s]$ exists on capacitor C_{comp}. This charge present on the two capacitors is discharged over a total time of $t = T_{s1}$ during phase $\phi_1[(n-1/2)T_s]$ through parasitics R_X and C_X.

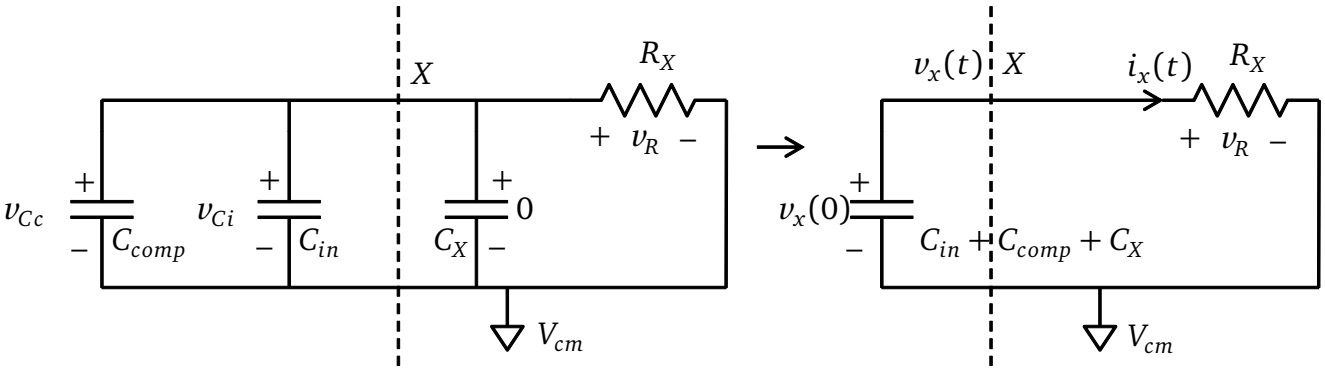


Figure 3.26: Connections at X port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

At the beginning of this phase the voltage on C_{in} is v_{Ci}, voltage on C_{comp} is v_{Cc} and voltage on C_X is 0. Since the capacitors are connected in parallel, charge transfer takes place between the three. Assuming very low resistance switches, the charge sharing can be instantaneous which results in stabilization of the voltage level across the three capacitors at the beginning of this phase. The three capacitors with an initial common voltage level $v_x(0)$ then discharge over a time of T_{s1}, generating current $i_x(t)$ during this phase. Using the same principles applied during analysis of the existing integrator, the rate of discharge of the voltage for the proposed integrator can be found to be:

$$v_x(t) = v_x(0)e^{-\frac{t}{R_X(C_{in}+C_{comp}+C_X)}} \tag{3.115}$$

where $v_x(0)$ is the common voltage level at the beginning of this phase given by:

$$v_x(0) = \frac{C_{in}v_{Ci} + C_{comp}v_{Cc} + C_X 0}{C_{in} + C_{comp} + C_X} \tag{3.116}$$

$$v_x(0) = -\frac{C_{in}v_{in}[(n-1)T_s]}{C_{in} + C_{comp} + C_X} - \frac{C_{comp}v_{out}[(n-1)T_s]}{C_{in} + C_{comp} + C_X} \tag{3.117}$$

Substituting Equation 3.117 in 3.115, we get the final equation for the voltage variation at port X with respect to time as:

$$v_x(t) = \left(-\frac{C_{in}v_{in}[(n-1)T_s]}{C_{in} + C_{comp} + C_X} - \frac{C_{comp}v_{out}[(n-1)T_s]}{C_{in} + C_{comp} + C_X}\right)e^{-\frac{t}{R_X(C_{in}+C_{comp}+C_X)}} \tag{3.118}$$

From the voltage equation, the total charge transferred during a time of T_{s1} can be calculated using the following equation as:

$$\begin{aligned}\Delta Q_X|_{t=0}^{t=T_{s1}} &= Q_X(T_{s1}) - Q_X(0) \\ &= (C_{in} + C_{comp} + C_X)v_x(T_{s1}) - (C_{in} + C_{comp} + C_X)v_x(0)\end{aligned} \tag{3.119}$$

Applying Equation 3.118 to 3.119, we get the total charge lost for half the clock period:

$$\Delta Q_X = (C_{in} v_{in}[(n-1)T_s] + C_{comp} v_{out}[(n-1)T_s])(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}}) \tag{3.120}$$

Equation 3.120 represents the total charge transferred from X port to the Z port during the charge transfer phase $\phi_1[(n-1/2)T_s]$. Ideally the exponential term $e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}}$ in this equation should become zero at end of $\phi_1[(n-1/2)T_s]$. This can be achieved by choosing proper values for C_{in}, C_{comp} capacitors in relation to C_X and R_X parasitic values.

The equation for the current flowing through port X over time t due to the change in charge Q_X can be derived by differentiating the Equation 3.118. This gives:

$$i_x(t) = -(C_{in} + C_{comp} + C_X)\frac{\partial v_x(t)}{\partial t} \tag{3.121}$$

$$i_x(t) = \left(-\frac{C_{in} v_{in}[(n-1)T_s]}{R_X(C_{in}+C_{comp}+C_X)} - \frac{C_{comp} v_{out}[(n-1)T_s]}{R_X(C_{in}+C_{comp}+C_X)}\right) e^{-\frac{t}{R_X(C_{in}+C_{comp}+C_X)}} \tag{3.122}$$

At Port Z:

Equation 3.120 shows the total charge lost from C_{in} and C_{comp} capacitors over a period of time T_{s1} during phase $\phi_1[(n-1/2)T_s]$. This charge generates current $i_x(t)$ at the X port as given in Equation 3.122 which is conveyed to the Z port where it is multiplied by the frequency dependent current gain α_0. This new charge (Q_{intn}) supplied to the $C_{int} + C_{buf}$ capacitor from the $i_z(t)$ current adds to the existing charge (Q_{inte}) on it from the previous charge transfer phase $\phi_1[(n-3/2)T_s]$. Figure 3.18 shows the connections at the Z port for the analysis below.

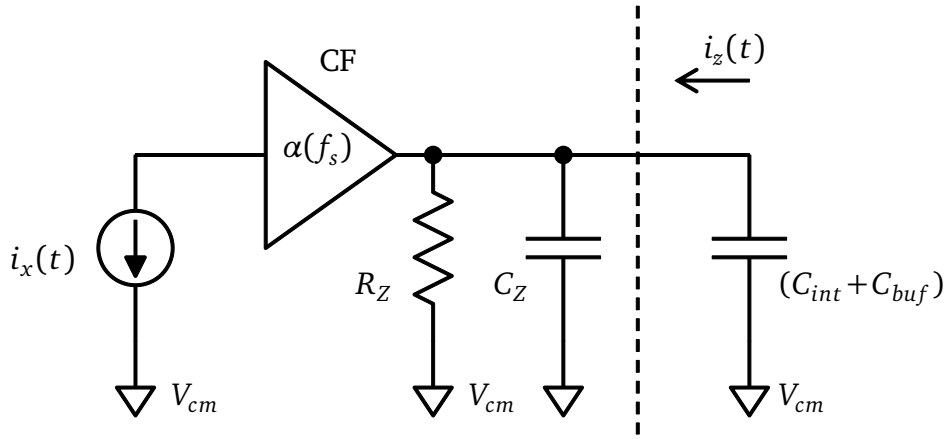


Figure 3.27: Connections at Z port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

The newly added charge and the existing charge losses due to the port Z parasitics are investigated individually below and then combined together as was done previously in the case of the existing CCII integrator.

- Errors in the existing charge Q_{inte}: The capacitors $(C_{int} + C_{buf})$ carry some existing charge from the previous charge transfer phase. This existing charge is given by:

$$Q_{Z1} = (C_{int} + C_{buf}) v_{int}[(n-1)T_s] \tag{3.123}$$

where $v_{int}[(n-1)T_s]$ is the voltage on C_{int} capacitor of the previous sample and hold phase $\phi_2[(n-1)T_s]$.

This charge present on $(C_{int}+C_{buf})$ capacitors is lost through the R_Z resistor over the total charge transfer time of T_{s1}. Therefore the value of the existing charge at the end of this phase is given by:

$$\begin{aligned} Q_{inte} &= Q_{Z1} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \\ &= (C_{int}+C_{buf}) v_{int}[(n-1)T_s] e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \end{aligned} \tag{3.124}$$

where Equation 3.123 has been substituted to get the final value of existing charge.

- Errors in the added charge Q_{intn}: Apart from the existing charge, an additional charge is added to the Z port in the form of current flow generated due to the current relation between X and Z ports. As the current is directly to proportional to the rate of change of charge, the following charge relation can be established:

$$Q_{Z2} = \alpha(f_s)\Delta Q_X = \alpha_0 \Delta Q_X \tag{3.125}$$

where Q_{Z2} is the total new charge flowing into the Z port parasitics and $(C_{int}+C_{buf})$ capacitors and $\alpha(f_s)$ is the approximate magnitude of the current gain at sampling frequency given. For low sampling frequencies such that $f_s << f_\alpha$ we get:

$$\alpha(f_s) = \frac{\alpha_0}{\sqrt{1+\left(\frac{f_s}{f_\alpha}\right)^2}} = \alpha_0 \tag{3.126}$$

As this charge is being added to C_{int}, C_{buf} and C_Z capacitor a part of it is lost through the R_Z resistor. This rate of loss is exponential and is controlled by the time constant formed by resistor R_Z and total capacitance $(C_{int}+C_{buf}+C_Z)$ at Z port. Therefore the total new charge added during the charge transfer phase within the time of $t = T_{s1}$, is given by:

$$\begin{aligned} Q_{intn} =& Q_{Z2} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \\ =& \alpha_0 (C_{in} v_{in}[(n-1)T_s] + C_{comp} v_{out}[(n-1)T_s]) \times \\ & (1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}}) e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \end{aligned} \tag{3.127}$$

where Equations 3.120 and 3.125 have been substituted.

The total charge Q_{int} present on parasitic C_Z, C_{int} and C_{buf} capacitors at the end of charge transfer phase $\phi_1[(n-1/2)T_s]$ is given as:

$$Q_{int} = (C_{int}+C_{buf}+C_Z) v_{int}[(n-1/2)T_s] \tag{3.128}$$

where $v_{int}[(n-1/2)T_s]$ is the final value of integrated voltage at the end of this phase.

Therefore combining Equations 3.124, 3.127 and 3.128 together to get the value of the integrated voltage $v_{int}[(n-1/2)T_s]$, we have:

$$Q_{int} = Q_{intn} + Q_{inte} \tag{3.129}$$

$$\begin{aligned}(C_{int}+C_{buf}+C_Z)v_{int}[(n-1/2)T_s] = &\left((C_{int}+C_{buf})v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\ &\left((C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s])\times\right.\\ &\left.\alpha_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.130}$$

$$\begin{aligned}v_{int}[(n-1/2)T_s] = &\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\ &\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\ &\left.\alpha_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.131}$$

Time instant $\phi_2[nT_s]$:

During this sample and hold phase, the circuit is connected as shown in Figure 3.24. The integrated voltage $v_{int}[(n-1/2)T_s]$ obtained from Equation 3.131 is sent to the output as shown by Equation 3.132. Therefore, the final value of output voltage $v_{out}[nT_s]$ at the end of this phase is given by:

$$v_{out}[nT_s] = \kappa(f_s)v_{int}[(n-1/2)T_s] = \kappa_0 v_{int}[(n-1/2)T_s] \tag{3.132}$$

Substituting Equations 3.113 and 3.131 in 3.132, we get the value of the integrated output voltage during this phase as:

$$\begin{aligned}v_{out}[nT_s] = &\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}(\kappa_0 v_{int}[(n-1)T_s])e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\ &\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\ &\left.\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.133}$$

$$\begin{aligned}v_{out}[nT_s] = &\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}v_{out}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\ &\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\ &\left.\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.134}$$

$$v_{out}[nT_s] = \left(\left(\frac{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}}{C_{int} + C_{buf} + C_Z} v_{out}[(n-1)T_s] \right) + \left(\frac{\alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{in}}{C_{int} + C_{buf} + C_Z} v_{in}[(n-1)T_s] \right) \right) \times e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.135}$$

Equation 3.135 shows the effect of C_{comp} capacitor. Due to the presence of R_Z, the previously held integrated voltage decreases by the factor $e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}$. The main purpose of C_{comp} capacitor is to sample a charge equivalent to the charge lost due to R_Z during the sample and hold phase and supply it back to C_{int}, C_Z, C_{buf} during the subsequent charge transfer phase. This compensation is called memory compensation.

Applying Z domain transformation to the previous equation and writing the transfer function of the integrator in terms of its gain coefficient and the ITF gives:

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} ITF_{cc}(z) \tag{3.136}$$

where the non-ideal ITF which depends on the CCII and buffer non-idealities is given by:

$$ITF_{cc}(z) = Gain_{cc} \frac{z^{-1}}{1 - z^{-1}z_{cc}} \tag{3.137}$$

Comparing the $ITF_{cc}(z)$ with the ideal integrator transfer function $(z^{-1}/(1-z^{-1}))$ the gain and pole location are given by:

$$z_{cc} = \frac{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}}{C_{int} + C_{buf} + C_Z} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.138}$$

$$Gain_{cc} = \frac{\alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{int}}{C_{int} + C_{buf} + C_Z} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.139}$$

The gain can be further modified as:

$$Gain_{cc} = Gain_{cc} \frac{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}}{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}} \tag{3.140}$$

$$Gain_{cc} = \frac{\alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{int}}{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}} z_{cc} \tag{3.141}$$

3.4.2 Design Conditions for Wideband Single Ended CCII Integrator

In order to derive the various conditions on the CCII parameters, we apply the same requirements used earlier to analyze the existing integrator. We use the same criteria such as requiring a noise floor of -90dB and a comparable gain of $A_{DC} > 45dB$, in order to derive the conditions given below. For this purpose we first consider the gain of the CCII integrator given in Equation 3.141.

$$Gain_{cc} > 0.9889 \tag{3.142}$$

Comparing Equations 3.80 and 3.81 derived for the existing CCII integrator with Equations 3.138 and 3.141, we observe that the pole contains an additional term in the numerator and the gain contains an additional term in the denominator related to C_{comp}. The main purpose of this capacitor is to reduce the loss errors by making the pole move closer to its ideal value of 1. In order to make the pole approach the ideal value of 1, C_{comp} needs to be increased. However it is seen that increasing C_{comp} has an opposite effect of making ITF gain $Gain_{cc}$ lower than the minimum value stated by Equation 3.142. An additional means of control is necessary in order to make the gain value high. Unlike the pole location, which has the C_{comp} capacitor to improve its value, gain $Gain_{cc}$ does not have an additional component in the numerator which can be used to improve its value.

From Equation 3.136, it is seen that a lower value of $Gain_{cc}$ in the ITF multiplies with the coefficient C_{in}/C_{int} and makes it lower than the desired coefficient value. $Gain_{cc}$ affects the overall coefficient of the integrator, therefore it is advantageous to improve the combined value of $(C_{in}/C_{int})Gain_{cc}$ so that the required coefficient can be achieved, instead of trying to improve $Gain_{cc}$ alone. In order to do so, predistortion is used wherein the ratio C_{in}/C_{int} is made larger than the desired coefficient such that the larger coefficient value and the lower $Gain_{cc}$ multiply together to give the desired coefficient value.

Therefore using the combined coefficient and the gain to derive the condition we get:

$$Gain_{cc}\left(\frac{C_{in}}{C_{int}}\right)_{distorted} > 0.9889\left(\frac{C_{in}}{C_{int}}\right)_{ideal} \tag{3.143}$$

Assuming that the ideal coefficient and the distorted coefficient are related using the predistortion factor $g_d > 1$, we get:

$$\left(\frac{C_{in}}{C_{int}}\right)_{distorted} = g_d\left(\frac{C_{in}}{C_{int}}\right)_{ideal} \tag{3.144}$$

Substituting ($z_{cc} > 0.9944$), Equation 3.141, 3.142 and 3.144 in 3.143 we get:

$$\left(\frac{g_d\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{int}}{C_{int}+C_{buf}+\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}}\right)z_{cc} > 0.9889 \tag{3.145}$$

$$\frac{g_d\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{int}}{C_{int}+C_{buf}+\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}} > 0.9944 \tag{3.146}$$

Rearranging the previous equation we get the lower charge transfer time limit as:

$$T_{s1} > R_X(C_{in} + C_X + C_{comp}) \log_e \left(\frac{g_d \alpha_0 \kappa_0 C_{int} - 0.9944 \alpha_0 \kappa_0 C_{comp}}{g_d \alpha_0 \kappa_0 C_{int} - 0.9944(C_{int} + C_{buf} + \alpha_0 \kappa_0 C_{comp})} \right) \quad (3.147)$$

$$T_{s1} > R_X(C_{in} + C_X + C_{comp}) \log_e \left(1 + \frac{0.9944(C_{int} + C_{buf})}{g_d \alpha_0 \kappa_0 C_{int} - 0.9944(C_{int} + C_{buf} + \alpha_0 \kappa_0 C_{comp})} \right) \quad (3.148)$$

The charge transfer time is positive if $\log_e$ is positive. This is true if the denominator inside $\log_e$ is positive. Therefore for a positive denominator we have the condition on C_{int} as:

$$C_{int} > \frac{0.9944(\alpha_0 \kappa_0 C_{comp} + C_{buf})}{g_d \alpha_0 \kappa_0 - 0.9944} \quad (3.149)$$

In order for the previous condition to be true the denominator needs to be positive. Equating the denominator gives the condition on the CCII gains as:

$$g_d \alpha_0 \kappa_0 > 0.9944 \quad (3.150)$$

Comparing the previous equation to Equation 3.97 we see that since g_d is greater than 1, the CCII gains for the proposed stage can have a value much smaller than 1. The predistortion technique lowers the requirement on the CCII gain by allowing the CCII gains to have a lower value. Assuming the factor $g_a > 1$ we get:

$$g_d \alpha_0 \kappa_0 = 0.9944 g_a \quad (3.151)$$

Substituting the previous equation and assuming a factor $g_c > 1$ over the minimum value for C_{int} capacitor given in Equation 3.149 we get the value of C_{int} as:

$$C_{int} = \frac{g_c(\alpha_0 \kappa_0 C_{comp} + C_{buf})}{g_a - 1} \quad (3.152)$$

Substituting Equation 3.152, 3.151 in 3.148 and assuming the ratio of $g_z = C_{int}/C_{buf}$, we get the lower time limit as:

$$T_{s1} > R_X(C_{in} + C_X + C_{comp}) \log_e \left(1 + \frac{0.9944(C_{int} + C_{buf})}{g_d \alpha_0 \kappa_0 C_{int} - 0.9944(C_{int} + C_{buf} + \alpha_0 \kappa_0 C_{comp})} \right) \quad (3.153)$$

$$T_{s1} > R_X(C_{in} + C_X + C_{comp}) \log_e \left(\frac{g_a}{(g_a - 1)} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)} \right) \quad (3.154)$$

where $g_z > 1$ since C_{int} is usually very large compared to input capacitance of buffer C_{buf}.

To find the upper charge transfer time limit we apply the condition on the pole Equation 3.138. The required value for the pole z_{cc} to achieve a comparable gain of 45dB is:

$$z_{cc} > 0.9944 \quad (3.155)$$

$$\frac{C_{int}+C_{buf}+\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})C_{comp}}{C_{int}+C_{buf}+C_Z}e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}>0.9944 \tag{3.156}$$

The factor $\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})$ is the overall error coming from non-ideal CCII current and voltage gains as well as the incomplete discharge of capacitors C_X, C_{int} and C_{comp} at the X port. To simplify the analysis we assume that these terms contribute an overall error of $g_x<1$ whose value is dependent on the chosen sampling frequency.

Substituting $g_x=\alpha_0\kappa_0(1-e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})$ and rearranging Equation 3.156 we get the upper limit on the charge transfer time as:

$$T_{s1}<R_Z(C_{int}+C_{buf}+C_Z)\log_e\left(\frac{C_{int}+C_{buf}+g_xC_{comp}}{0.9944(C_{int}+C_{buf}+C_Z)}\right) \tag{3.157}$$

$$T_{s1}<R_Z(C_{int}+C_{buf}+C_Z)\left(\log_e\left(\frac{1}{0.9944}\right)+\log_e\left(\frac{C_{int}+C_{buf}+g_xC_{comp}}{C_{int}+C_{buf}+C_Z}\right)\right) \tag{3.158}$$

$$T_{s1}<R_Z(C_{int}+C_{buf}+C_Z)\left(\log_e\left(\frac{1}{0.9944}\right)+\log_e\left(1+\frac{g_xC_{comp}-C_Z}{C_{int}+C_{buf}+C_Z}\right)\right) \tag{3.159}$$

In order for the charge transfer time to be positive, $\log_e$ should be positive or the term inside $\log_e$ should be greater than 1. The first $\log_e$ is unconditionally positive since the term inside is always greater than 1. The second $\log_e$ is positive if the term inside is greater than 1. Therefore applying this condition we get:

$$\left(1+\frac{g_xC_{comp}-C_Z}{C_{int}+C_{buf}+C_Z}\right)>1 \tag{3.160}$$

$$g_xC_{comp}>C_Z \tag{3.161}$$

Equation 3.161 gives the relation of the compensation capacitor in relation to the parasitic at Z port. The second $\log_e$ term becomes larger as the value of the compensation capacitor C_{comp} increases relative to C_Z capacitor. The main purpose of C_{comp} capacitor is to provide charge compensation equivalent to the charge lost by the port Z capacitors through the R_Z resistor as well as the finite gains and finite R_X which results in incomplete discharge of port X capacitors. Since the value of R_Z is in the range of few tens to few hundred kΩ in advanced CMOS technologies, the value of C_{comp} needed is usually many times over the minimum value given in Equation 3.161. Assuming a factor $g_l>>1$ exists, we get the value of the compensation capacitor as:

$$C_{comp}=\frac{g_lC_Z}{g_x} \tag{3.162}$$

Applying the previous equation to Equation 3.159 and neglecting the term $\log_e(1/0.9944)$ in relation to the larger second $\log_e$, we get the upper limit of the charge transfer time as:

$$T_{s1} < R_Z(C_{int} + C_{buf} + C_Z)\log_e\left(1 + \frac{(g_l - 1)C_Z}{C_{int} + C_{buf} + C_Z}\right) \tag{3.163}$$

Further reducing the equation by using the expansion series for natural logarithm we get approximate upper limit of the charge transfer time:

$$T_{s1} < R_Z(C_{int} + C_{buf} + C_Z)\left(\frac{(g_l - 1)C_Z}{C_{int} + C_{buf} + C_Z}\right) \tag{3.164}$$

$$T_{s1} < (g_l - 1)R_Z C_Z \tag{3.165}$$

Equations 3.154 and 3.165 give the lower and upper limits of the charge transfer time T_{s1}. Relating T_{s1} to the sampling clock as $T_{s1} = T_{s2} \approx T_s/2$, where $T_s = 1/f_s$, and combining the above equations we get:

$$R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{(g_a - 1)} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)}\right) < T_{s1} < (g_l - 1)R_Z C_Z \tag{3.166}$$

$$2R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{(g_a - 1)} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)}\right) < T_s < 2(g_l - 1)R_Z C_Z \tag{3.167}$$

$$\frac{1}{2(g_l - 1)R_Z C_Z} < f_s < \frac{1}{2R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{(g_a - 1)} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)}\right)} \tag{3.168}$$

where $g_l >> 1$, $g_a > 1$, $g_z > 1$, $g_c > 1$.

3.4.3 Wideband Fully Differential CCII Integrator.

In the previous section, a single ended CCII integrator was introduced and analyzed. In low voltage domains, fully differential architectures are preferred to suppress switching noise, common mode noise and increase the dynamic range of the circuit. Since the solution in the previous section is single ended, it is not capable of handling fully differential signals. One possible way to provide a fully differential signal is to use two single ended CCII integrators in parallel, with common mode feedback between the two single ended paths. However the charge transfer phase relies on currents as a means of integration, therefore implementing a common mode feedback scheme is not so easy.

It is observed in Figure 3.23, that port Y is always connected to common mode voltage. A fully differential architecture with some inherent common mode control can be implemented by using the Y port as a feedback input as shown in Figure 3.28. This cross coupled configuration allows a regenerative negative feedback to exist between the two CCII X and Y ports, which

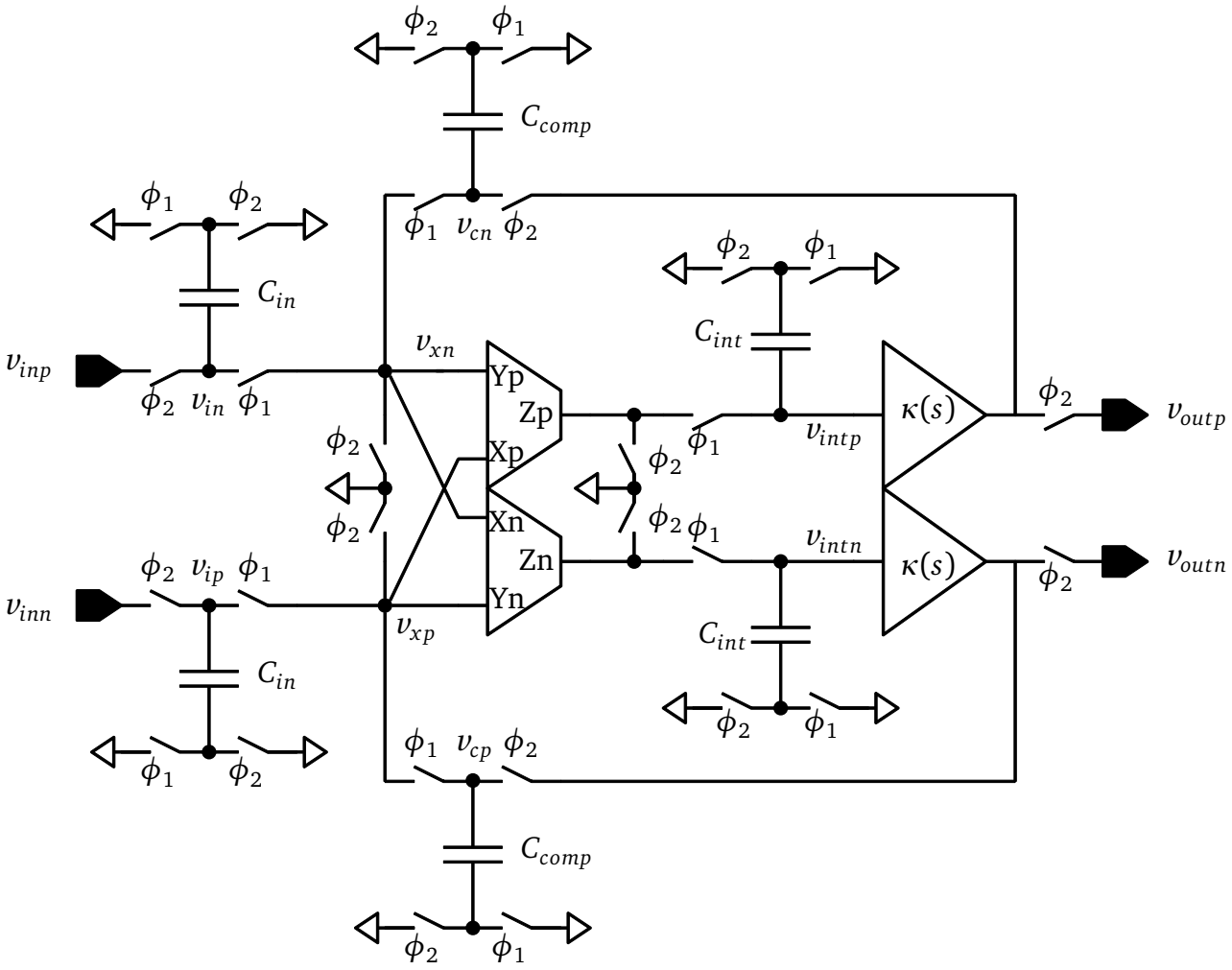


Figure 3.28: Fully differential CCII SC integrator.

allows a faster discharge of capacitors C_{comp} and C_{in} and consequently faster charge transfer to integration capacitor C_{int}. It will be shown in the following analysis that the improvement in speed is due to the factor $(1+\beta_0) \approx 2$ which relaxes the time available for discharge of port X capacitors.

This is shown by analyzing the fully differential circuit as before at three time instants, to derive the transfer function. In the following analysis the differential input signal is assumed to be $v_{inp} = v_{in}/2$, $v_{inn} = -v_{in}/2$. The two single ended elements are assumed to have similar properties so as to have good matching.

Time instant $\phi_2[(n-1)T_s]$:

In this phase the input voltage is sampled onto C_{in} and the integrated voltage is sent to the output using the buffer to C_{comp} as well next stage sampling capacitors. All the three ports of the CCII are autozeroed to remove any stray charge on the CCII parasitics during the charge transfer or integration phase. The corresponding equations at the end of $\phi_2[(n-1)T_s]$ can be written as:

$$\begin{aligned} Q_{in} &= C_{in}(v_{ip}[(n-1)T_s] - v_{in}[(n-1)T_s]) \\ &= C_{in}(v_{inn}[(n-1)T_s] - v_{inp}[(n-1)T_s]) \end{aligned} \tag{3.169}$$

$$\begin{aligned} Q_{int} =&(C_{int}+C_{buf})v_{int}[(n-1)T_s] \\ =&(C_{int}+C_{buf})(v_{intp}[(n-1)T_s]-v_{intn}[(n-1)T_s]) \end{aligned} \tag{3.170}$$

$$\begin{aligned} Q_{comp} =&C_{comp}(v_{cp}[(n-1)T_s]-v_{cn}[(n-1)T_s]) \\ =&C_{comp}(v_{outn}[(n-1)T_s]-v_{outp}[(n-1)T_s]) \end{aligned} \tag{3.171}$$

$$\begin{aligned} v_{out}[(n-1)T_s] =&\kappa(f_s)v_{int}[(n-1)T_s] \\ =&\kappa_0(v_{intp}[(n-1)T_s]-v_{intn}[(n-1)T_s]) \end{aligned} \tag{3.172}$$

Time instant $\phi_1[(n-1/2)T_s]$:

To derive the total charge transferred from X port to Z port during a time of T_{s1} , the circuit needs to be analyzed at port X and port Z independently to derive the various relationships. These relationships are then equated in the end to get the complete transfer function of the CCII integrator.

At Port X:

Figure 3.29 shows the connections at the X port, including the CCII parasitics during phase $\phi_1[(n-1/2)T_s]$. The resistance R_Y which comes in parallel to the capacitors takes away a small part of the charge from the capacitors. However since R_X is many order greater than R_Y, this charge is very small. Additionally if the gate of transistor is used as port Y input then the R_Y component is infinite. Therefore to make analysis simple, R_Y is neglected. It is already known that at the end of previous sample and hold phase $\phi_2[(n-1)T_s]$, a differential voltage of $v_{inn}[(n-1)T_s]-v_{inp}[(n-1)T_s]$ and a voltage of $v_{outn}[(n-1)T_s]-v_{outp}[(n-1)T_s]$ were sampled onto the C_{in} and C_{comp} capacitors. This differential voltage is discharged over a total time of $t=T_{s1}$ during the phase $\phi_1[(n-1/2)T_s]$ through the parasitics R_X at port Xp and Xn.

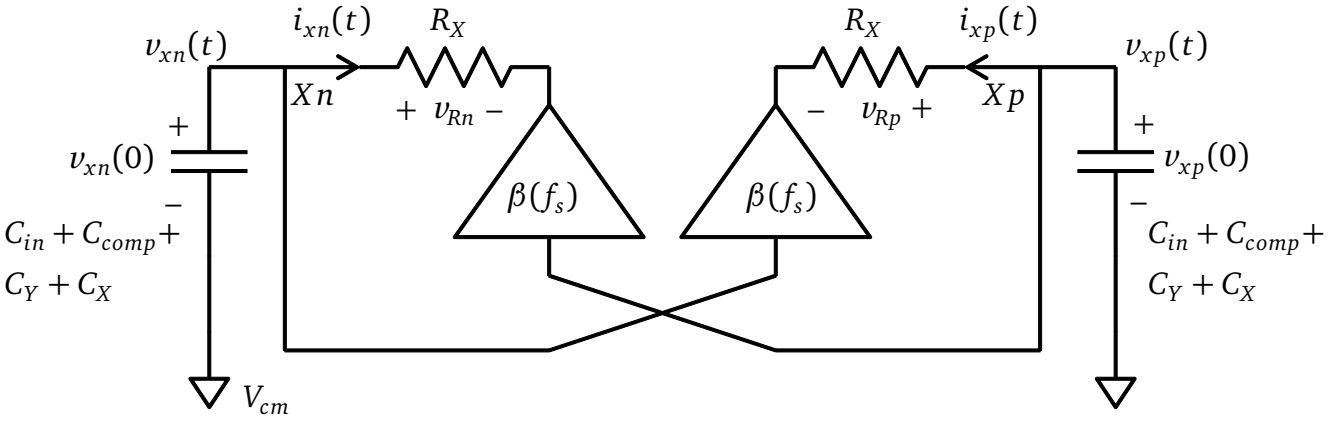


Figure 3.29: Connections at X port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

Assuming very low resistance switches the charge sharing can be assumed to be instantaneous between the four capacitors C_Y, C_{in}, C_{comp} and C_X at ports Xp and Xn, which results in stabilization of the voltage level at the beginning of this phase. This initial voltage of $v_{xp}(0)$, $v_{xn}(0)$

discharges over a time of T_{s1}, generating current $i_{xp}(t)$ and $i_{xn}(t)$ at ports Xp and Xn during this phase. The equation for the initial voltages are given by:

$$v_{xp}(0) = \frac{C_{in}v_{ip}[(n-1)T_s] + C_{comp}v_{cp}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} = \frac{C_{in}v_{inn}[(n-1)T_s] + C_{comp}v_{outn}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} \tag{3.173}$$

$$v_{xn}(0) = \frac{C_{in}v_{in}[(n-1)T_s] + C_{comp}v_{cn}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} = \frac{C_{in}v_{inp}[(n-1)T_s] + C_{comp}v_{outp}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} \tag{3.174}$$

The currents $i_{xp}(t)$ and $i_{xn}(t)$ are given by:

$$i_{xp}(t) = -(C_{in}+C_X+C_Y+C_{comp})\frac{\partial v_{xp}(t)}{\partial t} = \frac{v_{xp}(t)-\beta_0 v_{xn}(t)}{R_X} \tag{3.175}$$

$$i_{xn}(t) = -(C_{in}+C_X+C_Y+C_{comp})\frac{\partial v_{xn}(t)}{\partial t} = \frac{v_{xn}(t)-\beta_0 v_{xp}(t)}{R_X} \tag{3.176}$$

where β_0 is the value of the CCII voltage gain.

The total current flowing into the fully differential architecture is given by $i_x(t) = i_{xp}(t) - i_{xn}(t)$ and the total voltage that is discharged is given by $v_x(t) = v_{xp}(t) - v_{xn}(t)$. Taking the difference of the previous two equations we get

$$\frac{(1+\beta_0)(v_{xp}(t)-v_{xn}(t))}{R_X} = -(C_{in}+C_X+C_Y+C_{comp})\left(\frac{\partial v_{xp}(t)}{\partial t} - \frac{\partial v_{xn}(t)}{\partial t}\right) \tag{3.177}$$

Assuming an exponential decay for the voltage discharge $v_x(t) = v_{xp}(t) - v_{xn}(t) = Ae^{st}$ and applying it to the previous equation, we get the value of s as:

$$s = -\frac{(1+\beta_0)}{R_X(C_{in}+C_X+C_Y+C_{comp})} \tag{3.178}$$

Furthermore, applying the initial condition on the exponential decay at (t=0) and using Equations 3.173 and 3.174, we get the value of A as

$$A = v_x(0) = v_{xp}(0) - v_{xn}(0) = -\frac{C_{in}v_{in}[(n-1)T_s] + C_{comp}v_{out}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} \tag{3.179}$$

where $v_{in}[(n-1)T_s] = v_{inp}[(n-1)T_s] - v_{inn}[(n-1)T_s]$ and $v_{out}[(n-1)T_s] = v_{outp}[(n-1)T_s] - v_{outn}[(n-1)T_s]$.

Therefore the voltage decay at the differential input is given by:

$$v_x(t) = -\frac{C_{in}v_{in}[(n-1)T_s] + C_{comp}v_{out}[(n-1)T_s]}{C_{in}+C_{comp}+C_X+C_Y} e^{-\frac{(1+\beta_0)t}{R_X(C_{in}+C_X+C_Y+C_{comp})}} \tag{3.180}$$

From the voltage equation, the total charge transferred during a time of T_{s1} can be calculated using the following equation as:

$$\begin{aligned}\Delta Q_X|_{t=0}^{t=T_{s1}} &= Q_X(T_{s1}) - Q_X(0) \\ &= (C_{in} + C_{comp} + C_X + C_Y)v_x(T_{s1}) - (C_{in} + C_{comp} + C_X + C_Y)v_x(0)\end{aligned} \tag{3.181}$$

Applying Equation 3.180 to 3.181, we get the total charge lost for half the clock period:

$$\Delta Q_X = (C_{in}v_{in}[(n-1)T_s] + C_{comp}v_{out}[(n-1)T_s])(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_X+C_Y+C_{comp})}}) \tag{3.182}$$

Equation 3.182 represents the total charge transferred from X port to Z port during the charge transfer phase $\phi_1[(n-1/2)T_s]$. Ideally the exponential term $e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}}$ in this equation should become zero at end of $\phi_1[(n-1/2)T_s]$.

The equation for the total differential current flowing through port X can be derived by differentiating Equation 3.180. This gives:

$$i_x(t) = -(C_{in} + C_{comp} + C_X + C_Y)\frac{\partial v_x(t)}{\partial t} \tag{3.183}$$

$$i_x(t) = \left(-\frac{(1+\beta_0)C_{in}v_{in}[(n-1)T_s]}{R_X(C_{in}+C_{comp}+C_X+C_Y)} - \frac{(1+\beta_0)C_{comp}v_{out}[(n-1)T_s]}{R_X(C_{in}+C_{comp}+C_X+C_Y)}\right)e^{-\frac{(1+\beta_0)t}{R_X(C_{in}+C_{comp}+C_X+C_Y)}} \tag{3.184}$$

At Port Z:

The total charge lost at the differential input generates a current at Z port and charges C_{int}, C_{buf} and C_Z capacitors. Figure 3.30 shows the connections at Z port during the charge transfer phase.

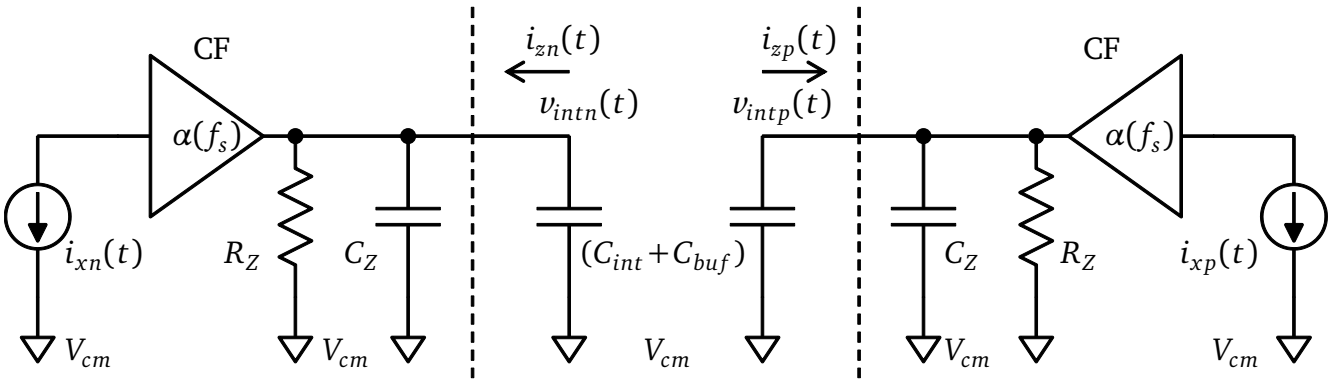


Figure 3.30: Connections at Z port during the charge transfer phase $\phi_1[(n-1/2)T_s]$.

The total additional charge added from the X ports to capacitors $C_{int} + C_Z + C_{buf}$ including the charge lost through R_Z during the charge transfer time of T_{s1} is given by:

$$\begin{aligned}Q_{inta} =& \alpha_0(C_{in}v_{in}[(n-1)T_s] + C_{comp}v_{out}[(n-1)T_s])\times \\ & (1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_X+C_Y+C_{comp})}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\end{aligned} \tag{3.185}$$

The total existing charge on $C_{int}+C_{buf}+C_Z$ at the end of the charge transfer phase including the losses through R_Z is given by:

$$Q_{inte}=(C_{int}+C_{buf})v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.186}$$

From Equations 3.185 and 3.186 the total integrated charge on $C_{int}+C_{buf}+C_Z$ capacitors at the end of this phase is given by:

$$Q_{int}=(C_{int}+C_{buf}+C_Z)v_{int}[(n-1/2)T_s]=Q_{inta}+Q_{inte} \tag{3.187}$$

and the value of the integrated voltage at the end of this phase is given by:

$$\begin{aligned}v_{int}[(n-1/2)T_s]=&\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}v_{int}[(n-1)T_s]e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\&\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\&\left.\alpha_0(1-e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.188}$$

Time instant $\phi_2[nT_s]$:

During this sample and hold phase the integrated voltage $v_{int}[(n-1/2)T_s]$ obtained from Equation 3.188 is sent to the output as shown by Equation 3.189. Therefore, the final value of the output voltage $v_{out}[nT_s]$ at the end of this phase is given by:

$$v_{out}[nT_s]=\kappa(f_s)v_{int}[(n-1/2)T_s]=\kappa_0 v_{int}[(n-1/2)T_s] \tag{3.189}$$

Substituting Equations 3.188 and 3.172 in 3.189, we get the value of the integrated output voltage during this phase as:

$$\begin{aligned}v_{out}[nT_s]=&\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}(\kappa_0 v_{int}[(n-1)T_s])e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\&\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\&\left.\alpha_0\kappa_0(1-e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.190}$$

$$\begin{aligned}v_{out}[nT_s]=&\left(\frac{C_{int}+C_{buf}}{C_{int}+C_{buf}+C_Z}v_{out}[(n-1)T_s])e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)+\\&\left(\frac{C_{in}v_{in}[(n-1)T_s]+C_{comp}v_{out}[(n-1)T_s]}{C_{int}+C_{buf}+C_Z}\times\right.\\&\left.\alpha_0\kappa_0(1-e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}}\right)\end{aligned} \tag{3.191}$$

where $v_{out}[(n-1)T_s] = \kappa_0 v_{int}[(n-1)T_s]$

$$v_{out}[nT_s] = \left(\left(\frac{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}{C_{int} + C_{buf} + C_Z} v_{out}[(n-1)T_s] \right) + \left(\frac{\alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{in}}{C_{int} + C_{buf} + C_Z} v_{in}[(n-1)T_s] \right) \right) \times e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.192}$$

Applying Z domain transformation to the previous equation and writing the transfer function of the integrator in terms of its gain coefficient and the ITF we get:

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} ITF_{cc}(z) \tag{3.193}$$

where the non-ideal ITF which depends on the CCII and buffer non-idealities is given by:

$$ITF_{cc}(z) = Gain_{cc} \frac{z^{-1}}{1 - z^{-1}z_{cc}} \tag{3.194}$$

Comparing the $ITF_{cc}(z)$ with the ideal integrator transfer function ($z^{-1}/(1-z^{-1})$), the gain and pole location are given by:

$$z_{cc} = \frac{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}{C_{int} + C_{buf} + C_Z} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.195}$$

$$Gain_{cc} = \frac{\alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{int}}{C_{int} + C_{buf} + C_Z} e^{-\frac{T_{s1}}{R_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.196}$$

The gain can be further modified as:

$$Gain_{cc} = \frac{\alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{int}}{C_{int} + C_{buf} + \alpha_0\kappa_0(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}} z_{cc} \tag{3.197}$$

3.4.4 Design Conditions for Wideband Fully Differential CCII Integrator

The main discharge happens through R_X and the Y port provides only negative feedback, therefore it is sufficient to use small transistors for the Y port which reduces the overall C_Y. The only change in the design conditions with respect to the single ended integrator is the replacement of capacitance C_X with $C_X + C_Y$ combination and the introduction of an additional factor $(1 + \beta_0)$.

From the Equation 3.141 and 3.197 it is observed that the fully differential term $(1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})$ approaches 1 better than the single ended term $(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})$.

This is attributed to the factor $(1+\beta_0) \approx 2$ present in the exponential. The presence of this factor makes the exponential $e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}} < e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}}$, assuming all the other values remain the same.

Alternatively it can also be thought that the factor $(1+\beta_0)$ reduces the requirement on R_X. Since the factor $(1+\beta_0)$ divides R_X resistance, a fully differential CCII integrator with port X resistance $2R_X$ discharges the capacitors at port X in the same time as a single ended CCII with port X resistance of R_X. The design conditions which are affected by C_Y and the factor $(1+\beta_0)$ are given below, while the rest remain the same as that of the single ended integrator. The value of C_{comp} capacitor is given by:

$$C_{comp} = \frac{g_l C_Z}{g_x} \tag{3.198}$$

where $g_x < 1$ and $g_x = \alpha_0 \kappa_0 (1 - e^{-\frac{(1+\beta_0)T_{s1}}{R_X(C_{in}+C_{comp}+C_X+C_Y)}})$

The limits of the charge transfer time and sampling clock are given by:

$$\frac{R_X(C_{in}+C_X+C_Y+C_{comp})}{1+\beta_0} \log_e\left(\frac{g_a}{(g_a-1)} + \frac{g_z+g_c}{g_z(g_a-1)(g_c-1)}\right) < T_{s1} < (g_l-1)R_Z C_Z \tag{3.199}$$

$$\frac{2R_X(C_{in}+C_X+C_Y+C_{comp})}{1+\beta_0} \log_e\left(\frac{g_a}{(g_a-1)} + \frac{g_z+g_c}{g_z(g_a-1)(g_c-1)}\right) < T_s < 2(g_l-1)R_Z C_Z \tag{3.200}$$

$$\frac{1}{2(g_l-1)R_Z C_Z} < f_s < \frac{1+\beta_0}{2R_X(C_{in}+C_X+C_Y+C_{comp}) \log_e\left(\frac{g_a}{(g_a-1)} + \frac{g_z+g_c}{g_z(g_a-1)(g_c-1)}\right)} \tag{3.201}$$

where $g_l >> 1$, $g_c > 1$, $g_a > 1$, $g_z > 1$.

3.4.5 Low Bandwidth Single Ended CCII Integrator

The architecture with a separate buffer is useful when the CCII integrator is also used at high frequencies, since it allows the use of an optimized CCII which focuses only on the charge transfer phase and an optimized buffer which focuses only on charging next stage sampling capacitors. If however the application requires just low sampling frequencies then a single dual X output CCII integrator such as in Figure 3.31 can be used.

In the dual output X CCII, any voltage at Y port is buffered by the two voltage output ports X and X' with a gain β_0. The only difference between X and X' is that current gain α_0 is determined by the currents flowing in X and Z ports alone. The X' port plays no role in determining current gain α_0. The advantage of this configuration is evident from the fact that since the port X' plays no role in determining the current gain, it can be designed to handle large currents and low resistance R'_X so as to drive the next stage sampling capacitors. Using dual X output ports of the CCII, different values for the port X resistance during the charge transfer phase and the sample and hold phase can be provided.

During the charge transfer phase the Z port needs to have high R_Z to reduce losses which require smaller transistors and smaller currents. Therefore during this phase the first port X

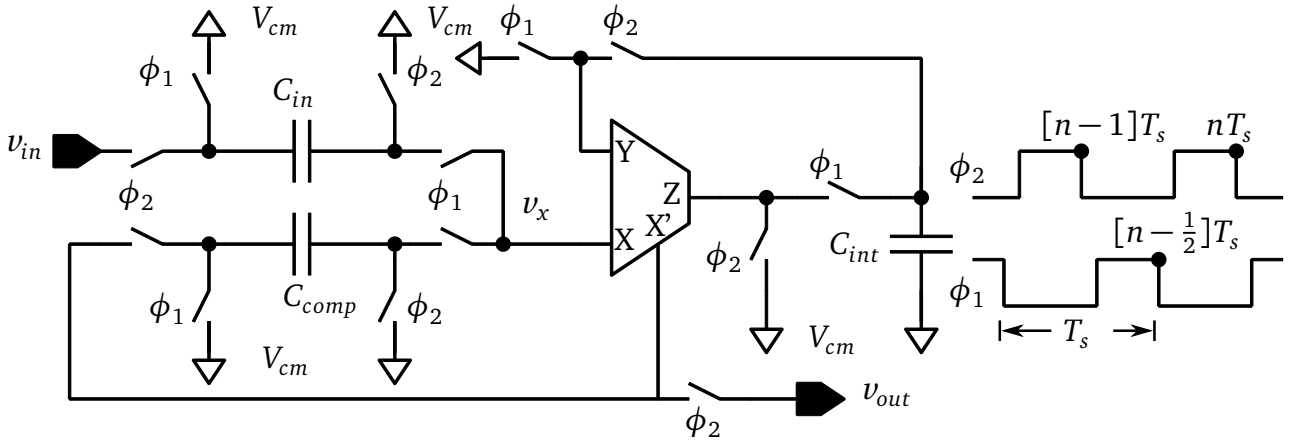


Figure 3.31: Low bandwidth single ended dual X output CCII integrator.

is used which although has a nominally higher R_X, is sufficient to discharge C_{in} and C_{comp} capacitors during the charge transfer phase. During the sample and hold phase the second port X' is used to charge the next stage sampling capacitors in a short time by providing higher current drive and lower R'_X. The integrator can be analyzed as before using predistortion in the gain equation and C_{comp} capacitor in the pole equation to improve the performance. One possible transistor implementation of a dual X output CCII is shown in Figure 3.32.

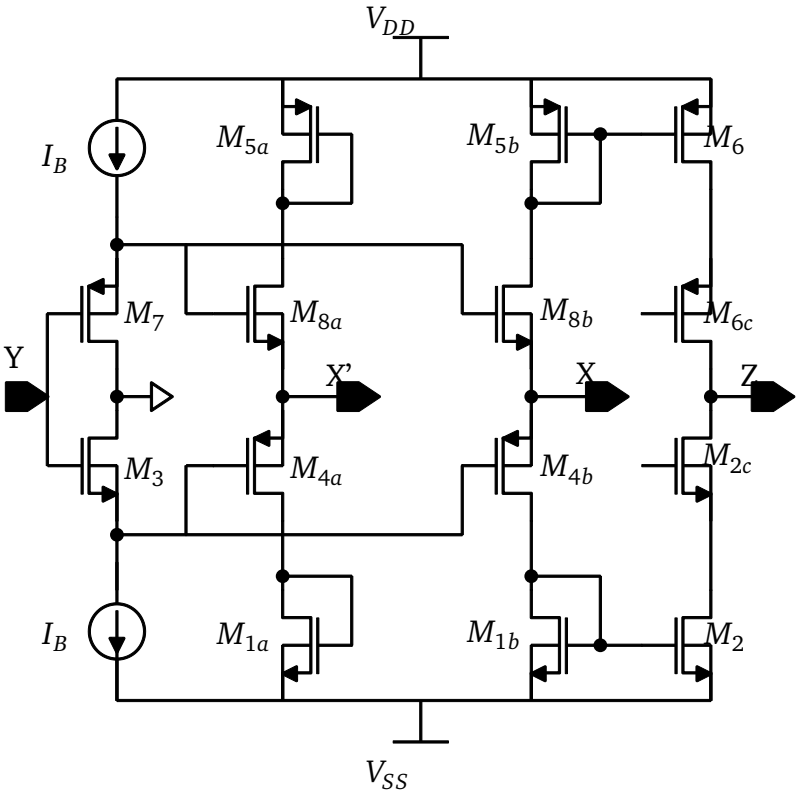


Figure 3.32: Transistor implementation of dual X output CCII.

The analysis can be done using the same methods as shown before to calculate the transfer function, ITF gain and pole location as shown in the equations below.

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} ITF_{cc}(z) \tag{3.202}$$

where the non-ideal ITF which depends on the CCII and buffer non-idealities is given by:

$$ITF_{cc}(z) = Gain_{cc} \frac{z^{-1}}{1 - z^{-1} z_{cc}} \tag{3.203}$$

Comparing the $ITF_{cc}(z)$ with the ideal integrator transfer function ($z^{-1}/(1-z^{-1})$), the gain and pole location are given by:

$$z_{cc} = \frac{C_{int}}{C_{int} + C_Y} \frac{C_{int} + \alpha_0 \kappa_0 (1 - e^{-\frac{T_{s1}}{R_X (C_{in} + C_{comp} + C_X)}}) C_{comp}}{C_{int} + C_Z} e^{-\frac{T_{s1}}{R_Z (C_{int} + C_Z)}} \tag{3.204}$$

$$Gain_{cc} = \frac{C_{int}}{C_{int} + C_Y} \frac{\alpha_0 \kappa_0 (1 - e^{-\frac{T_{s1}}{R_X (C_{in} + C_{comp} + C_X)}}) C_{int}}{C_{int} + C_Z} e^{-\frac{T_{s1}}{R_Z (C_{int} + C_Z)}} \tag{3.205}$$

The gain can be further modified as:

$$Gain_{cc} = \frac{\alpha_0 \kappa_0 (1 - e^{-\frac{T_{s1}}{R_X (C_{in} + C_{comp} + C_X)}}) C_{int}}{C_{int} + \alpha_0 \kappa_0 (1 - e^{-\frac{T_{s1}}{R_X (C_{in} + C_{comp} + C_X)}}) C_{comp}} z_{cc} \tag{3.206}$$

3.4.6 Design Conditions for Low Bandwidth Single Ended CCII Integrator

Analyzing the low bandwidth integrator to get a performance comparable to Op-Amp, we get the following design conditions:

$$\left(\frac{C_{in}}{C_{int}}\right)_{distorted} = g_d \left(\frac{C_{in}}{C_{int}}\right)_{ideal} \tag{3.207}$$

where $g_d > 1$.

The value of C_{int} is given by:

$$C_{int} = \frac{g_c \alpha_0 \kappa_0 C_{comp}}{g_a - 1} \tag{3.208}$$

where $g_c > 1$, $g_a > 1$.

Lower limit on the charge transfer time is given by:

$$T_{s1} > R_X (C_{in} + C_X + C_{comp}) \log_e \left(\frac{g_a}{g_a - 1} + \frac{1}{g_c - 1}\right) \tag{3.209}$$

where $g_a > 1$ and $g_a = g_d\alpha_0\kappa_0/0.9944$

The memory compensation capacitor value is given by:

$$C_{comp} = \frac{g_l(C_Y + C_Z)}{g_x} \tag{3.210}$$

where $g_l >> 1$, $g_x < 1$ and $g_x = \alpha_0\kappa_0(1 - e^{-\frac{T_{s1}}{R_X(C_{in}+C_{comp}+C_X)}})$

Upper limit on the charge transfer time is given by:

$$T_{s1} < (g_l - 1)R_Z(C_Y + C_Z) \tag{3.211}$$

Sampling frequency range limit is given by:

$$\frac{1}{2(g_l - 1)R_Z(C_Y + C_Z)} < f_s < \frac{1}{2R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{g_a - 1} + \frac{1}{g_c - 1}\right)} \tag{3.212}$$

where $g_l >> 1$, $g_c > 1$, $g_a > 1$.

3.4.7 Comparison of the Proposed and Existing CCII Integrator

In the previous sections, design conditions were derived for the existing architecture and proposed architecture of the CCII integrator. Table 3.2 summarizes the main design conditions of the two stages to achieve a coefficient of 1, noise floor of -90dB and a comparable Op-Amp gain of $Gain_{op} > 45dB$. Since the main scope of the thesis is to design wide band integrator, in the comparison the low bandwidth integrator is not considered. To show the advantages of the proposed solution with the existing architecture it is necessary to visualize the parameters in terms of values.

- C_{int}: Comparing the integration capacitor values for the existing and proposed stages, we observe the following. The predistortion factor ($g_d > 1$) which is greater than 1 makes the denominator large. Assuming that the predistortion factor g_d is chosen such that the denominator is $(g_a - 1) \approx 1$, we get the value of C_{int} for the proposed stage as $C_{int} = g_c(\alpha_0\kappa_0 C_{comp} + C_{buf})$. The size of C_{int} does not affect the lower sampling frequency limit, therefore $g_c > 1$ can be small such that for C_{comp} and C_{buf} in the range of few tens to few hundred femtofarads, the C_{int} value is in the range of few hundred femtofarads to few picofarads. The proposed solution which uses predistortion and memory compensation to lower the value of the C_{int} capacitor to less than few picofarads is useful way to make the integrator realizable in a compact layout and with less current consumption in the CCII. Figure 3.33a shows the plot of C_{int} for various g_l, C_Z and C_{buf}. We observe that the value of C_{int} does not cross 10pF even under high values of g_l. Figure 3.33b shows the C_{comp} for various g_l, g_b and C_Z. As illustrated, the value of C_{comp}, depending on the g_l, goes as high as 5pF. However unless the CCII integrator is to be used at very low sampling frequencies in the range of kHz, the g_l rarely crosses value of 20. This makes the value of C_{comp} to be in the range of max 1pF for sampling frequencies above few MHz.

  Comparing this with the C_{int} for the existing stage, we see that the factor $178g_c'$ where $g_c' > 1$ makes the value of C_{int} go into the range of few ten picofarads to few hundred picofarads.

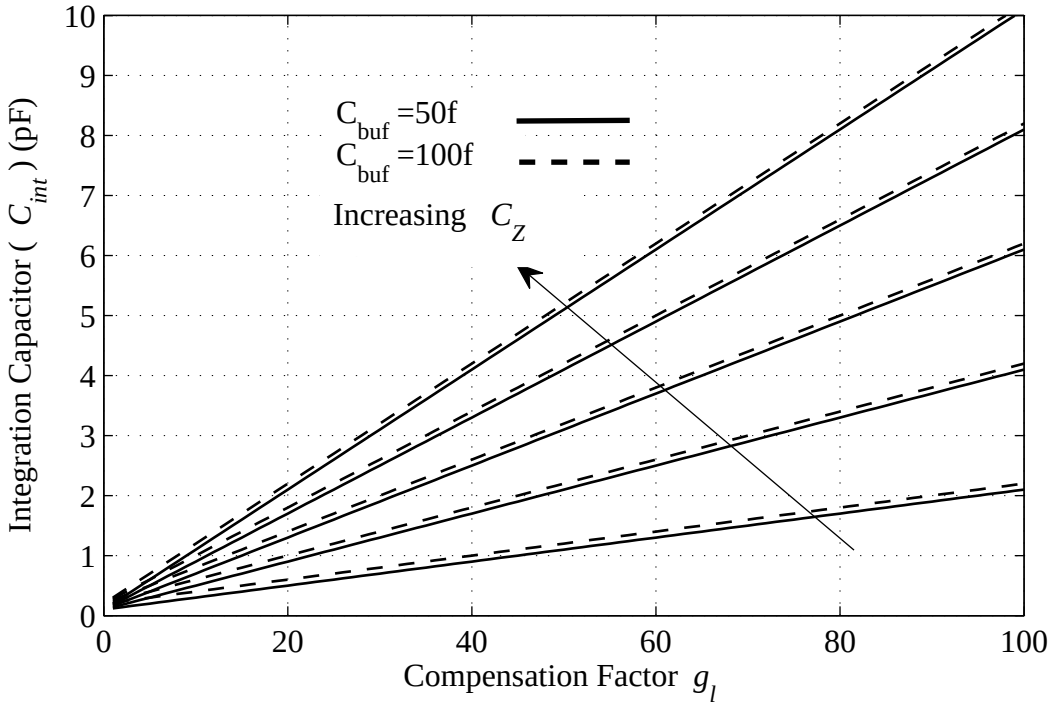
Table 3.2: Comparison of design conditions for achieving comparable gain of $A_{DC} \geq 45dB$

Parameters	Existing Architecture	Proposed Wideband Architecture Single Ended/Full Differential
C_{in}	C_{int}	$g_d C_{int}$
C_{int}	$178 g_c'(C_Y + C_Z)$	$\frac{g_c(\alpha_0\kappa_0 C_{comp} + C_{buf})}{g_a - 1} \approx \frac{g_c(g_l C_Z + C_{buf})}{g_a - 1}$
CCII gains	$\alpha_0\beta_0 = 0.9944 g_a'$	$\alpha_0\kappa_0 = \frac{0.9944 g_a}{g_d}$
Minimum f_s	$\frac{1}{2 g_c' R_Z (C_Y + C_Z)}$	$\frac{1}{2(g_l - 1) R_Z C_Z}$
Maximum f_s	$\frac{1}{2R_X(C_{in} + C_X)\log_e\left(\frac{g_a'}{g_a' - 1}\right)}$	$\frac{1}{2R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{g_a - 1} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)}\right)} / \frac{1 + \beta_0}{2R_X(C_{in} + C_X + C_{comp})\log_e\left(\frac{g_a}{g_a - 1} + \frac{g_z + g_c}{g_z(g_a - 1)(g_c - 1)}\right)}$
Others	$g_c' > 1,\ g_a' > 1$	$g_l >> 1,\ g_c > 1,\ g_d > 1,$ $g_z > 1,\ g_a > 1,\ \beta_0 \approx 1$

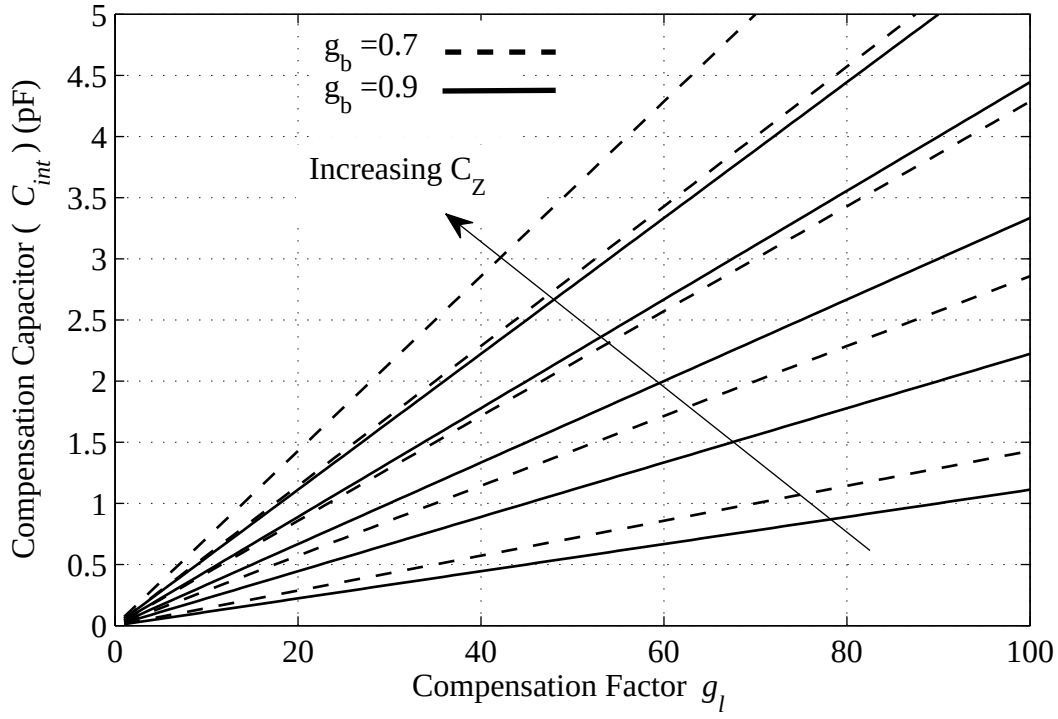
Having such large values increases the area substantially and makes the realization of the integrator difficult, since the capacitors will occupy a large area in relation to the active logic. With such large capacitors the existing stage will need CCII with high current handling capability, which in turn increases the parasitics and non-idealities due to the use of larger transistors. This has a cascading effect on the other parameters in the Table 3.2. Compared to the proposed solution the value of C_{int} for the existing integrator depends on the gain A_{DC} we want to achieve. For higher gains, the value of the C_{int} increases.

- C_{in}: For a coefficient value of 1, $C_{in} = C_{int}$ and therefore its value is also in the range of few tens to few hundred picofarads. With such high values of C_{in} capacitor, the existing stage needs very low values of R_X in order to discharge the C_{in} capacitor completely during the charge transfer phase. Additionally the next stage sampling capacitors have values similar to C_{in}, therefore the CCII port X must be able to drive high currents in order to charge them in a short time. This increases the power consumption substantially. However increasing current flow in port X also increases current flow in port Z in order to maintain current gain $\alpha_0 = 1$. High currents in Z port translates to large transistors and lower R_Z resistance values, which is detrimental to the performance of the CCII since it increases the losses.

  The proposed architecture on the other hand uses C_{in} capacitor which is marginally higher by the predistortion factor g_d. This makes the value of C_{in} capacitor to still remain in the range of few hundred femtofarads to few picofarads. For such low values of C_{in}, the CCII current handling capability need not be high. This improves the CCII performance, since lower currents in CCII need smaller transistors which lowers the parasitics and improves R_Z resistance as well. The separate buffer which drives next stage sampling capacitors needs



(a)



(b)

Figure 3.33: (a) C_{int} plotted against different g_l, parasitics C_Z={10f,20f,30f,40f,50f}, g_c=2, g_a=2 and C_{buf}={50f,100f}. (b) C_{comp} plotted against different g_l, parasitics g_b={0.7,0.9} and C_Z={10f,20f,30f,40f,50f}.

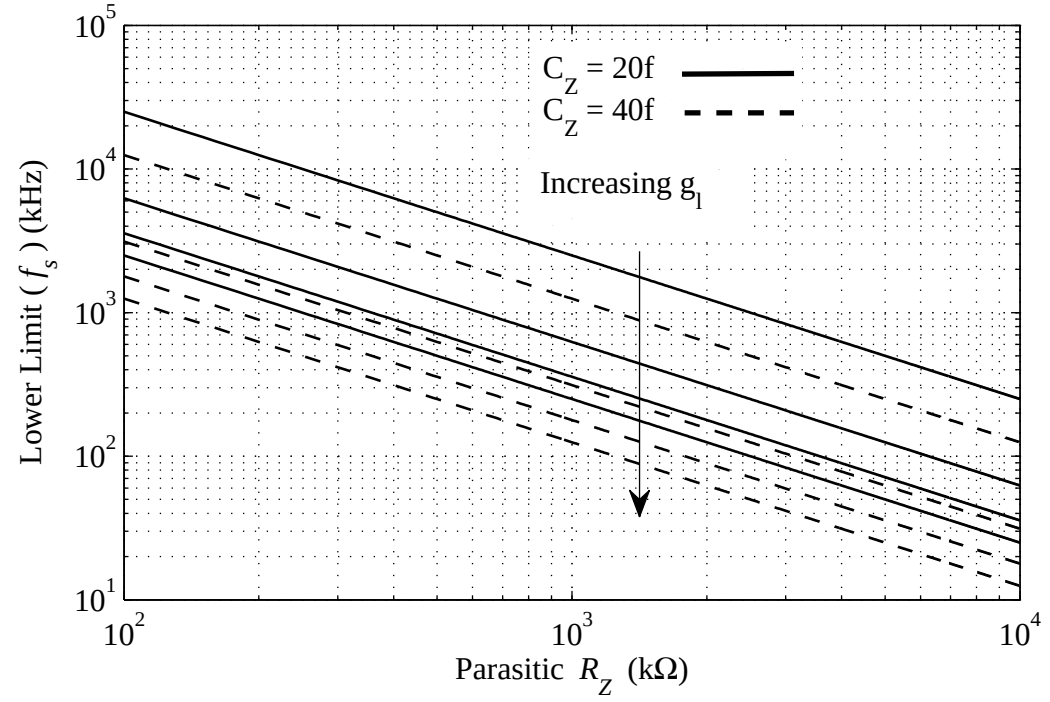
only small current drive capability to charge next stage sampling capacitors whose values are similar to C_{in}. Therefore the proposed solution lowers the overall power consumption of the CCII integrator by many orders, due to the reduction in the size of components.

- CCII Gains: The requirement on the existing CCII stage gain $\alpha_0\beta_0 > 0.9944$ is achievable in practice using more accurate and complex topologies. However a downside is that complex topologies in turn increase the parasitics and possibly lower the resistance R_Z. For example, assuming a CCII topology with $\alpha_0 = 2$, we see that this requires the port Z to have transistors which are twice the size of port X transistors in order to accommodate the larger current. Having larger transistors increases the parasitic capacitors and lowers the parasitic resistor by an approximate factor of 2 at Z port, which degrades the performance of the CCII integrator. Therefore it is preferred that the increase in the value of gains $\alpha_0\beta_0$ is kept to be marginal over the value of 0.9944 that is for example 1. This means the value of g_a' is marginally higher than 1.

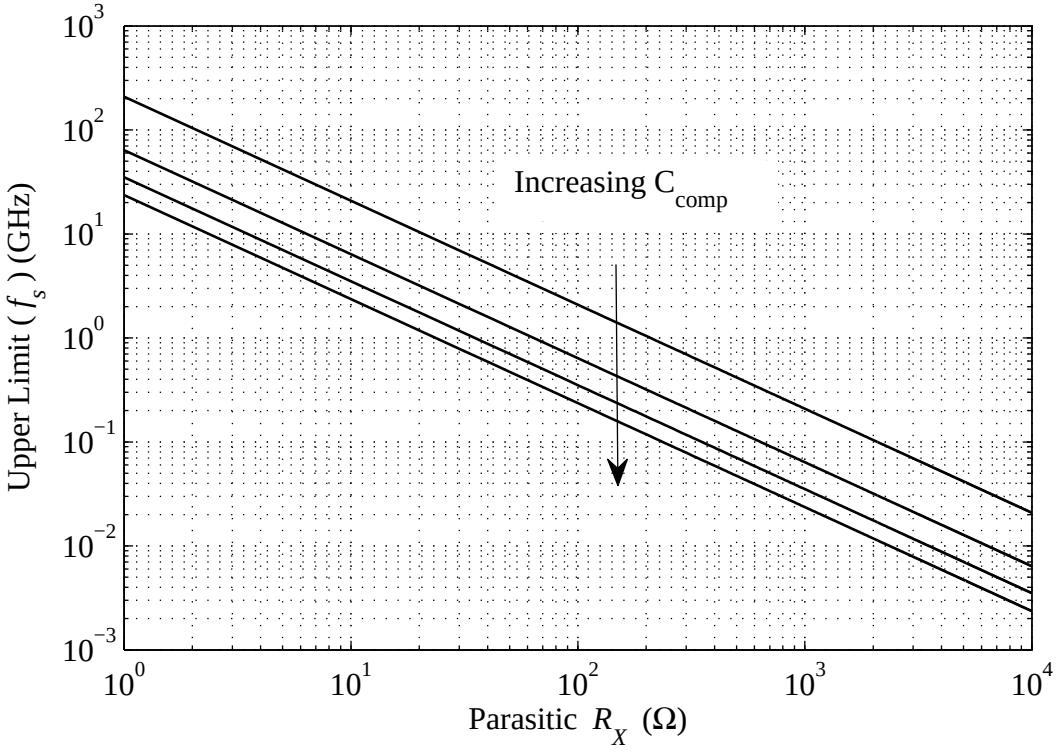
  In comparison, the requirement on the proposed CCII stage gain $\alpha_0\kappa_0 > 0.9944/g_d$ is less stringent and can be achieved quite easily with simple topologies. This is because the predistortion factor $g_d > 1$ lowers the requirement on the CCII gains. For example with predistortion factor of $g_d = 2$ we see that the condition on the gains becomes $\alpha_0\kappa_0 > 0.4972$. This condition is easily realized with simple topologies, without significant design effort. Additionally the value of g_a can be as high as the predistortion factor g_d, which improves the upper sampling frequency limit as well.

- Minimum f_s: For the existing integrator the lower sampling frequency limit depends on the inverse of R_Z, C_Y, C_Z and g_c'. In order to use very low sampling frequencies with the existing integrator, the lower limit needs to be very small, which requires R_Z to be very large above few $M\Omega$. While R_Z in the range of $M\Omega$ can be achieved using small transistors, the requirement of large C_{int} and C_{in} poses integration difficulties in CMOS technologies. Additionally, it is very difficult to design a CCII which provides both, a very large R_Z and a very high current handling capability required by the large C_{in} and C_{int} capacitors at the same time. This is because large currents require larger transistors which lowers the R_Z. The other factor g_c' can help lower the sampling frequency limit, but since it directly increases the size of C_{in} and C_{int} capacitors it cannot be increased substantially. Assuming that $(C_Y + C_Z)$ is in the range of few tens to few hundred femto farads due to larger transistors and $g_c' > 1$, that is for example $g_c' = 2$, and R_Z in the range of few hundred $k\Omega$, it is seen that the lower sampling frequency limit is in the range of MHz. In order to have a limit in kHz range, the value of R_Z has to be very high or alternatively at the expense of increase in C_{int} the value of g_c' can be made high.

  In comparison, for the proposed integrator, the lower sampling frequency limit depends on the inverse of C_Z, R_Z and g_l. Unlike g_c which cannot be excessively large, g_l can be made quite high such that $g_l > g_c$. The increase in g_l increases C_{comp} which in turn lowers the upper frequency limit. However, since the goal is to use the integrator at low frequencies, the decrease in the upper frequency limit is inconsequential. Additionally since smaller capacitors C_{in} and C_{int} are used due to predistortion and memory compensation, the current requirements on the CCII are greatly reduced. Therefore smaller currents and smaller transistors resulting in higher values for R_Z in $M\Omega$ can be easily realized. Assuming C_Z in the range of few tens of femto farads and $g_l > g_a$, that is for example $g_l = 50$, it is seen



(a)



(b)

Figure 3.34: (a) Sampling frequency lower limit plotted against various R_z, g_l={10,40,70,100}, C_Z={20f,40f}. (b) Sampling frequency upper limit plotted against various R_x for parasitic C_{comp}={100f,400f,700f,1000f}, C_X=100f, C_{buf}=100f, $g_c = 2$, $g_a = 2$ and $g_d = 2$.

that the lower sampling frequency limit can be in kHz range. For even lower limits below the parameters g_l can be increased as required, without substantially affecting the other parameters. Figure 3.34a shows the sampling frequency lower limit for various combinations of the parasitics and g_l. As illustrated, the sampling frequency in the range of kHz can be achieved without substantially increasing the C_{int} capacitors.

- Maximum f_s: For the existing integrator, it is observed that the upper sampling frequency limit is inversely related to R_X, C_{in}, C_X and g_a'. In order to use the integrator at high sampling frequencies, these values must be as small as possible. The value of C_{in} is already known to be in the range of few tens to few hundred picofarads and the value of g_a' is known to be marginally higher than the value of 1. Having a marginally higher value for g_a' makes $\log_e$ large. For example a $g_a' = 1.005$ gives the $\log_e$ a value of 5.3. Combined together with a resistance R_X which is in the range of few tens to few hundreds Ω, the maximum sampling frequency is in the range of MHz. As observed, the minimum and maximum sampling frequency limits are both in the range of MHz. A very careful design needs to be done in order to make sure that the lower limit is less than the upper limit, otherwise the exiting integrator cannot be used.

  In comparison for the proposed integrator, the upper sampling frequency limit is inversely related to R_X, C_{in}, C_X, C_{comp} and logarithm of g_z, g_c and g_a. It is given that the value of C_{in} is in the range of few hundred femto farads to few pico farads. C_X and C_{comp} are similarly in the range of few tens to few hundred femto farads. The $\log_e$ term of the existing stage is larger than the $\log_e$ term of the proposed stages due to the $g_a' < g_a$. Combining this and the smaller capacitances with R_X which is in the range of few tens to few hundred Ω, the maximum sampling frequency limit goes above few hundred MHz. Additionally for the full differential architecture it is seen that the factor $(1+\beta_0)$ improves the upper frequency limit by a factor of 2 approximately which is useful very high sampling frequencies need to be achieved. Figure 3.34b shows the sampling frequency upper limits. As illustrated the operating range of proposed integrator can lie between few kHz to above few hundred MHz depending on the CCII design and its parameters.

- Power Requirements: For the existing CCII integrator the power requirements are large. This is because of the higher currents required to drive the large sampling capacitors and integration capacitors.

  In comparison, for the proposed integrator the power requirements are small since the size of capacitances are reduced by many order in magnitude. If we assume a linear relationship between size of capacitance and power requirements, we observe that the power requirements of the proposed CCII integrator can be reduced by a factor of atleast 10, if not more.

- Equivalent Gain A_{cc}: While the straightforward derivation of the equivalent CCII SC gain from the transfer functions of the CCII integrator is difficult, nonetheless a liberal estimate of the gain can be derived as follows for the existing and proposed integrator. The dependency between comparable Op-Amp gain A_{DC} and equivalent CCII gain A_{cc} for the CCII integrator can be approximately derived as follows. Consider the input/output voltage equation for Op-Amp and CCII integrator using C_{in} and C_{int} capacitors. Assuming that

$\beta_A A_{DC} >> 1$, the gain A_{DC} of the Op-Amp is related to the input/output of the integrator as:

$$\frac{v_{out}}{v_{in}} \approx \frac{C_{in}}{C_{int}}\left(1-\frac{1}{\beta_A A_{DC}}\right) \tag{3.213}$$

where $\beta_A = C_{int}/(C_{int}+C_{in})$ is the Op-Amp feedback factor.

The input/output relationship of the existing CCII integrator for the sampling frequency f_s is given as

$$\frac{v_{out}}{v_{in}} = \frac{C_{in}}{C_{int}}\beta_0\alpha_0(1-e^{-\frac{1}{2f_sR_X(C_{in}+C_X)}})\left(\frac{C_{int}}{(C_{int}+C_Z)}e^{-\frac{1}{2f_sR_Z(C_{int}+C_Z)}}\frac{C_{int}}{(C_{int}+C_Y)}e^{-\frac{1}{2f_sR_Y(C_{int}+C_Y)}}\right) \tag{3.214}$$

Assuming the Y port has a MOS gate as input ($R_Y \to \infty$), $\beta_0\alpha_0 \approx 1$, capacitors at port X discharge completely during charge transfer phase and $C_{int} >> C_Z, C_Y$ we get the following approximation:

$$\frac{v_{out}}{v_{in}} \approx \frac{C_{in}}{C_{int}}\left(1-\frac{1}{2f_sR_ZC_{int}}\right) \tag{3.215}$$

Comparing Equations 3.213 and 3.214 we get the equivalent gain of the existing CCII integrator as:

$$A_{cc} = A_{DC} = \frac{2f_sR_ZC_{int}}{\beta_A} = \frac{2R_ZC_{int}}{\beta_A T_s} \tag{3.216}$$

As the equation shows, the equivalent gain of the CCII integrator is approximately defined by the port Z parasitics and the sampling frequency, both of which need to be high in order for it to give a high value. A disadvantage is that since the parasitic values cannot be accurately controlled during fabrication, the resulting gain can often vary by a large margin. The above equation shows that for low frequencies, the value of R_Z or the C_{int} needs to be high to realize high gains. As an example for realizing $A_{cc} = 400$ at $f_s = 1MHz$, we need a $R_Z = 1M\Omega$ and $C_{int} = 100p$. Similarly for realizing $A_{cc} = 400$ at $f_s = 100MHz$, we need $R_Z = 1M\Omega$ and $C_{int} = 1p$. As these liberal estimate of A_{cc} values show, realizing high R_Z at high frequencies or integrating high C_{int} at low frequencies is not practical in advanced CMOS technologies.

Similarly considering the input/output relationship of the proposed fully differential integrator we have:

$$\frac{v_{out}}{v_{in}} = \left(\frac{C_{in}}{C_{int}}\right)_{distorted}\left(\frac{\alpha_0\kappa_0(1-e^{-\frac{(1+\beta_0)1}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{int}}{C_{int}+C_{buf}+\alpha_0\kappa_0(1-e^{-\frac{(1+\beta_0)1}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}\right)z_{cc} \tag{3.217}$$

The memory compensation capacitor is used mainly to adjust the pole so that it approaches the value of 1 in the ITF of the integrator. Therefore assuming $z_{cc} \to 1$, and applying the same conditions as in the previous case, that is, $\alpha_0\kappa_0 \approx 1$, capacitors at port X discharge completely during charge transfer phase and $C_{int} >> C_Z, C_{buf}$ we get

$$\frac{v_{out}}{v_{in}} = \left(\frac{C_{in}}{C_{int}}\right)_{ideal}\left(\frac{g_d}{1+c_c}\right) \tag{3.218}$$

where $c_c < 1$ and $c_c = C_{comp}/C_{int}$ is the memory compensation factor.

Comparing Equation 3.218 and 3.213 we get the equivalent gain for the proposed integrator as:

$$A_{cc} = A_{DC} = \frac{1}{\beta_A}\frac{1+c_c}{1+c_c-g_d} = \frac{1}{\beta_A}\left(1+\frac{g_d}{1+c_c-g_d}\right) \tag{3.219}$$

As the previous equation shows, the value of the gain depends on the memory compensation factor and the predistortion factor, unlike the gain of the existing CCII integrator which depends on the the parasitics, sampling frequency and C_{int}. The value of the gain in the previous equation is made high by reducing the denominator to a very small value such that it is just positive above zero. Therefore we have:

$$0 < 1 + c_c - g_d < 1 \tag{3.220}$$

$$1 + c_c > g_d > c_c \tag{3.221}$$

where $g_d > 1$ and $c_c < 1$. By properly setting c_c and g_d the gain can be made high. For example assuming $g_d = 2$ and $1 + c_c - g_d = 0.02$ we have a gain above 200.

While the equivalent gain equation in 3.219 shows no direct dependence on the sampling frequency, nonetheless there exists an indirect dependence through c_c and g_d, both of which are defined by $Gain_{cc}$ and z_{cc} values which depend on the CCII parasitics and the sampling frequency. This makes the effect of sampling frequency on the proposed integrator to be marginally less. An advantage is that the required gain for the proposed integrator is far easier to adjust and realize, since it depends on the predistortion factor and memory compensation factor, both of which are under the designers control. Furthermore, it is easier to adjust these values post fabrication in order to account for changes in the CCII parameters than it is to adjust the CCII parasitics and C_{int} as in the case of the existing integrator.

A disadvantage of both the existing and proposed integrators is that if the CCII parameters are kept constant, the equivalent gains change as the sampling frequency changes. If the sampling frequencies are widely spaced apart, the gain varies widely. Therefore for both existing and proposed integrators equivalent gain remains relatively unchanged only for a specific set of closely spaced sampling frequencies and any wide variations in the sampling frequency need some sort of calibration.

From the above comparison, it is seen that using predistortion and memory compensation technique in the proposed CCII integrators not only improves the performance significantly by making the integrator usable over a wider sampling frequency range, but also reduces the size of the elements such as C_{in} and C_{int} by large factor such that they can be readily fabricated in advanced CMOS technologies.

3.5 Wide Sampling Frequency Coverage Using Adaptive Calibration Technique

In the previous section the non-idealities of CCII and their effects on the CCII integrator were analyzed. It was shown that the proposed integrator performs better with significantly low power consumption and lower design requirements on the CCII, due to the use of predistortion and memory compensation techniques. As long as the sampling frequency of the proposed integrators satisfies the conditions given by Equations 3.168, 3.201 and 3.212, the $\Delta\Sigma$ modulator performs as expected, providing high SNDR over the signal bandwidth. The limits are defined by the CCII parameters and circuit components, therefore for each circuit there exists only a small set of closely spaced sampling frequencies which can be used such that the sampling frequency limits given by the design equations are always satisfied.

If however there is a need to use the same CCII integrator over a much wider range of sampling frequencies while maintaining low power and robust performance, then calibration is needed. The necessity of the calibration can be explained as follows.

- Ideally the sampling frequency should lie within the two extreme limits given in Equations 3.168, 3.201 and 3.212 to guarantee good performance. The integrator needs to be designed such that sampling frequency is expected to be many orders lower than the upper limit and higher than the lower limit. This is necessary since the process and technology variations introduce additional effects such as parameter variations, offsets, mismatch and noise in the circuits which can shift the upper or lower sampling frequency limits. By having many orders difference between the limits and the sampling frequency, the operation of the integrator at the given sampling frequency is guaranteed. If however there is a need to use the same integrator at other sampling frequencies, calibration is necessary to make sure that the new sampling frequency still lies within the design limits. Without calibration the gain and loss errors can increase, causing loss of performance.

- One main disadvantage of the proposed integrator is that it cannot be used in applications where it is required to operate over a wide range of sampling frequencies ranging from few tens of MHz to few hundred MHz, such as in a reconfigurable $\Delta\Sigma$ modulator covering all the mobile communications standards. Since the upper and lower limits of the sampling frequency range are defined by the CCII parameters and circuit components which remain unchanged, changing the sampling frequency causes it to approach either of these frequency limits in such applications. As mentioned before, the sampling frequency should ideally lie in between the lower and upper limits to give best performance. In order to make sure that the new sampling frequency lies between these two limits, it is necessary to introduce a new distortion factor and compensation capacitor which can shift the upper and lower limits such that the new sampling frequency lies in between them. This is possible only through the use of calibration.

- In deriving the design conditions, it is assumed that the sampling frequency is many times lower than the 3dB bandwidth of the CCII and the voltage buffer, that is $f_s << f_\alpha, f_\beta, f_\kappa$. This is required so that the voltage and current gains present a constant value during the integration process. The main disadvantage of limiting the sampling frequency to less than the 3dB bandwidths is that it requires a wide bandwidth CCII when larger sampling frequencies are needed. Large CCII bandwidths require more power, which is not desirable in low power systems. In order to maintain low power for the CCII integrator when the

sampling frequency approaches or is greater than the 3dB bandwidths of the CCII and buffer, that is $f_s \rightarrow f_\alpha, f_\beta, f_\kappa$, calibration is needed. The calibration can respond to the changes in the properties of the CCII and the buffer with frequency such as the gains given by Equations 3.45, 3.66, 3.114 and apply correction with the help of programmable components.

3.5.1 Choice of Programmable Circuits

The proposed integrators use predistortion and memory compensation technique to cancel the effect of CCII non-idealities. In order to fulfill the requirement of wide operating sampling frequency range, these parameters need to be adjusted so that the errors in gain and pole for the chosen sampling frequency are minimized. To adjust the predistortion factor and the memory compensation capacitor, programmable circuit blocks are needed. The design equations derived for the fully differential integrator for a given sampling frequency f_s where $f_s \rightarrow f_\alpha, f_\beta, f_\kappa$, are produced below for convenience.

The relation between input and output of the integrator is given by:

$$v_{out}[nT_s] = \left(\left(\frac{C_{int} + C_{buf} + \alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_s R_X (C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}{C_{int} + C_{buf} + C_Z} v_{out}[(n-1)T_s] \right) + \left(\frac{\alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_s R_X (C_{in}+C_{comp}+C_X+C_Y)}})C_{in}}{C_{int} + C_{buf} + C_Z} v_{in}[(n-1)T_s] \right) \right) \times e^{-\frac{1}{2f_s R_Z (C_{int}+C_{buf}+C_Z)}} \tag{3.222}$$

The transfer function of the integrator in terms of its gain coefficient and the ITF is given as:

$$H(z) = \frac{v_{out}(z)}{v_{in}(z)} = \frac{C_{in}}{C_{int}} ITF_{cc}(z) = \left(\frac{C_{in}}{C_{int}} Gain_{cc} \right) \frac{z^{-1}}{1 - z^{-1} z_{cc}} \tag{3.223}$$

The pole and combined gain are given by:

$$z_{cc} = \frac{C_{int} + C_{buf} + \alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_s R_X (C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}{C_{int} + C_{buf} + C_Z} e^{-\frac{1}{2f_s R_Z (C_{int}+C_{buf}+C_Z)}} \tag{3.224}$$

$$Gain_{ct} = \left(\frac{C_{in}}{C_{int}} \right)_{distorted} \frac{\alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_s R_X (C_{in}+C_{comp}+C_X+C_Y)}})C_{int}}{C_{int} + C_{buf} + C_Z} e^{-\frac{1}{2f_s R_Z (C_{int}+C_{buf}+C_Z)}} \tag{3.225}$$

From the pole and gain equation we can identify four components which vary with the sampling frequency:

- $\alpha(f_s)$
- $\kappa(f_s)$

- $1 - e^{-\frac{(1+\beta(f_s))}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}}$
- $e^{-\frac{1}{2f_sR_Z(C_{int}+C_{buf}+C_Z)}}$

Assuming all the CCII parasitics and non-idealities remain the same, the first exponential term $(1 - e^{-\frac{(1+\beta(f_s))}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}})$ moves further away from the value of 1 as sampling frequency increases while the second exponential term $e^{-\frac{1}{2f_sR_Z(C_{int}+C_{buf}+C_Z)}}$ moves closer to the value of 1 as the sampling frequency increases. The gains $\alpha(f_s)$, $\kappa(f_s)$ and $\beta(f_s)$ decrease as the sampling frequency increases and approaches or goes beyond their respective 3dB bandwidths. The opposite happens when the sampling frequency decreases.

For a small set of closely spaced sampling frequencies, the changes in these errors are not that significant. If however the variation in the sampling frequency is considered to be wide, the errors associated with these terms also vary a lot. The combined gain of the CCII integrator is adjusted with the help of the predistortion factor g_d. Therefore in order to counter gain variations with increase or decrease in sampling frequency, the predistortion factor needs to be adjusted as well.

The predistortion ratio is determined by the distorted capacitors, therefore to create a new predistortion factor either of the two capacitors C_{in} or C_{int} needs to be made programmable. Similarly the pole location at a given sampling frequency is adjusted with the help of the memory compensation capacitor C_{comp}. In order to counter the pole variations with frequency, the memory compensation capacitor needs to be made programmable.

A $\Delta\Sigma$ modulator consists of many SC integrators which share a common circuit architecture, with the only difference being the variable coefficients. Therefore from the design point of view the optimum choice is to fix the size of C_{in} capacitors and make C_{int} as the programmable component to generate the different coefficients.

3.5.2 Calibration Architecture and Method

Figure 3.35 shows the calibration architecture used to calibrate the CCII integrator for different sampling frequencies. As illustrated, the main block used in the calibration process is the integrator itself with programmable C_{int} and C_{comp} capacitors and a high resolution low offset comparator capable of comparing the integrator output V_{out} with a known reference voltage V_{cmp}. The comparator needs to be accurate enough to amplify the differences at its input and detect small differences of less than 1 LSB. That is if the application demands a resolution of $100\mu V$, the comparator must have a resolution much smaller than this. This is necessary so that the integrator properties can be accurately set.

The calibration algorithm corrects the integrator errors in two steps. The first step involves setting the correct combined gain $Gain_{ct}$ for the integrator, by adjusting C_{int} in order to minimize the losses during the charge transfer from port X to port Z. Once the gain is corrected, the second step involves setting the correct value of C_{comp} to minimize the losses occurring at port Z due to C_Z and R_Z. The implementation details of the programmable capacitor blocks are explained in the next chapter. For explaining the calibration process they are assumed to be programmable and their values varied by addition or subtraction of binary weighted capacitances.

The calibration algorithm proceeds in two steps.

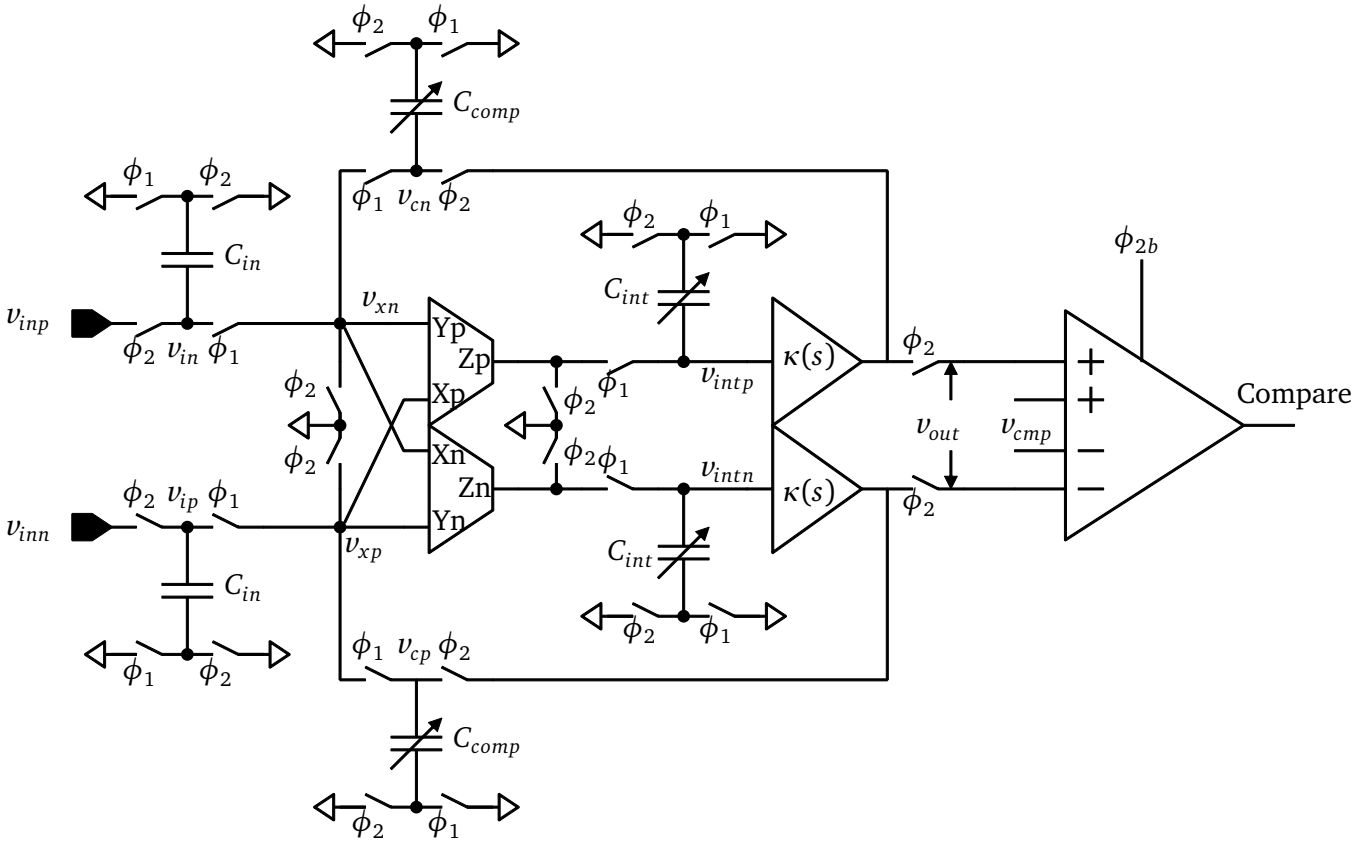


Figure 3.35: Calibration architecture setup for fully differential CCII integrator.

- Step 1 - Gain Calibration: Figure 3.36 shows the gain calibration waveforms during the first step of the calibration algorithm. During the first step of the calibration process the algorithm uses the following voltages v_{crefin} and $v_{crefout}$.

  Under steady state conditions when no inputs are applied, the integrator outputs are zero. Therefore we have $v_{out}[0] = 0$ at n=0. Applying this to the transfer function of the integrator given by Equation 3.222, we have $v_{out}[(n-1)T_s] = v_{out}[0] = 0$ at n=1. Due to this, the first term in the transfer function of the integrator becomes zero. In other words the C_{comp} capacitor does not add any charge to the C_{int} capacitor during the first charge transfer phase $\phi_1[(1/2)T_s]$. Therefore during the gain calibration, the C_{comp} capacitor is set to have a value of 0.

  Considering this, we have the output/input voltage relationship at the end of the first clock cycle that is (n=1) as:

$$\frac{v_{out}[T_s]}{v_{in}[0]} = \left(\frac{C_{in}}{C_{int}}\right)_{ideal} \times g_d \times \left(\frac{\alpha(f_s)\kappa(f_s)(1-e^{-\frac{(1+\beta(f_s))}{2f_sR_X(C_{in}+C_X+C_Y)}})e^{-\frac{1}{2f_sR_Z(C_{int}+C_{buf}+C_Z)}}C_{int}}{C_{int}+C_{buf}+C_Z} \right) \tag{3.226}$$

  The ratio of the voltages $v_{out}[T_s]/v_{in}[0]$ should ideally be equal to the integrator coefficient $\left(\frac{C_{in}}{C_{int}}\right)_{ideal}$ that we want to achieve. However as the equation shows, the presence of the CCII non-idealities lowers the overall coefficient ratio from the ideal value. By adjusting

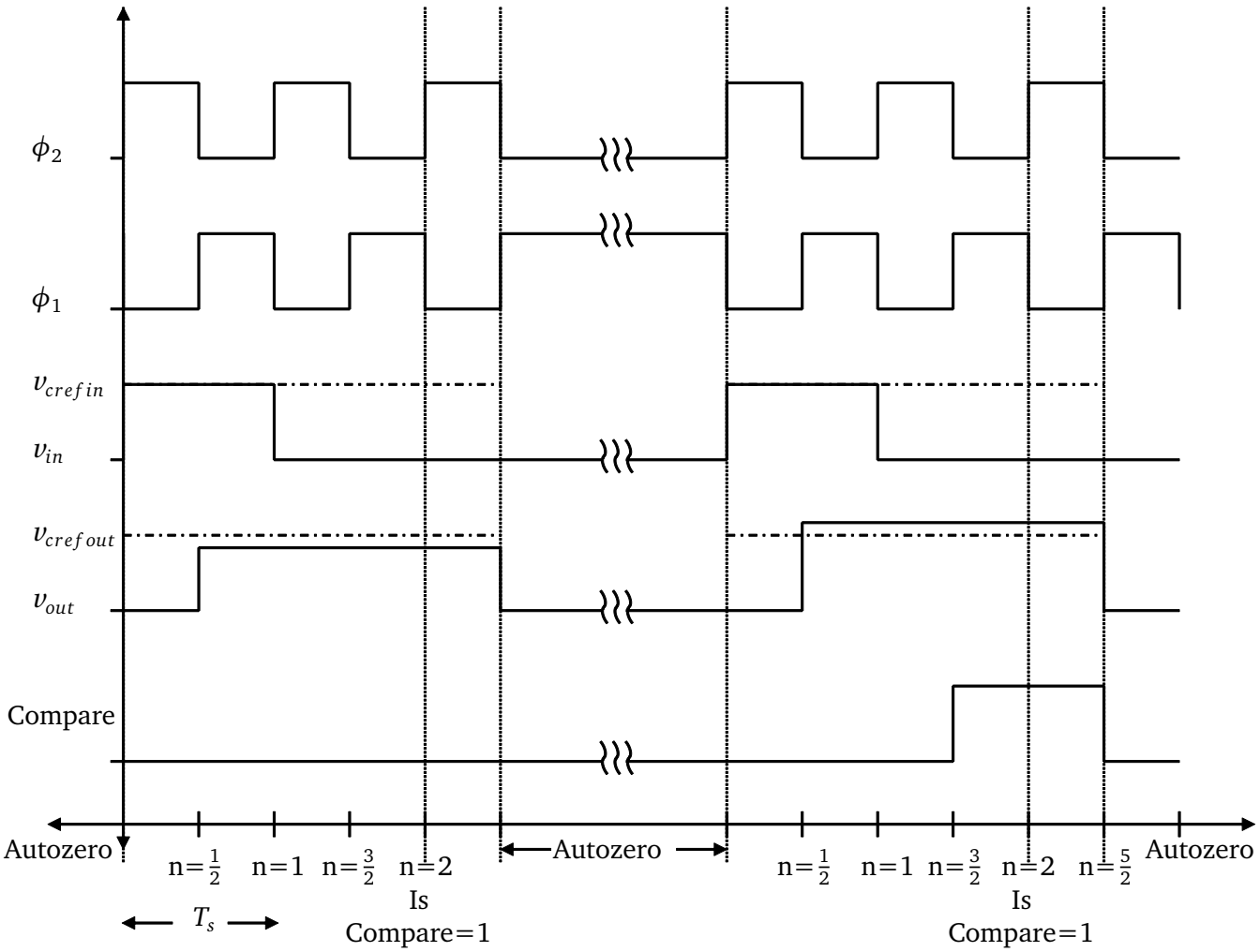


Figure 3.36: Gain calibration waveforms.

the predistortion factor g_d to a higher value using variable C_{int}, the ratio of output/input can be made approximately equal to the desired coefficient that we want to achieve.

The gain calibration process does this by first autozeroing all capacitors in the integrator so that all stray charges are removed. During the autozero phase the values of C_{int} and C_{comp} are set to C_{imax} and 0 respectively. C_{imax} is the maximum value of C_{int} when all capacitors in the programmable block are enabled. The autozero phase lasts a minimum of 8 clock cycles or more as the sampling frequency is increased.

After the autozero phase at the beginning of the first clock cycle, that is at (n=0), an input voltage of $v_{in} = v_{crefin}$ is applied to the integrator. During the first sample and hold phase $\phi_2[0]$, the C_{in} capacitor is charged to the calibration reference input voltage. Next during the first charge transfer phase $\phi_1[T_s/2]$, this voltage is sent to the Z port by the CCII. At the beginning of the second sample and hold phase $\phi_2[T_s]$, the output voltage $v_{out}[T_s]$ of the integrator shows a value. As mentioned before, the ratio of voltages $v_{out}[T_s]/v_{in}[0]$ should ideally give the desired coefficient. In order to check whether the desired coefficient is achieved, the output voltage is compared with $v_{crefout}$.

The ratio of voltages $v_{crefout}/v_{crefin}$ is the desired coefficient we want to achieve for the given integrator. The high resolution low offset comparator is used for this purpose of comparing the output of the integrator with $v_{cmp} = v_{crefout}$ and to check if the desired output voltage $v_{out}[T_s] = v_{crefout}$ is reached at the end of first clock cycle. If there are any errors such as the non-ideal gains, the non-ideal discharge of the capacitors at port X and charge losses at Z port through R_Z and C_Z as shown by the Equation 3.226, then the output of the integrator does not reach this value of $v_{crefout}$.

The example waveforms in Figure 3.36 initially show the comparator output as zero due to the output voltage not reaching above the level of $v_{crefout}$. Since the comparator produces a zero, the value of the binary weighted capacitor array C_{int} is decreased to increase the predistortion factor $g_d = (C_{in}/C_{int})_{distorted}/(C_{in}/C_{int})_{ideal}$ and the whole process repeats. The value of C_{int} is lowered until the desired output voltage is reached. When the correct value of C_{int} is found, the gain calibration process stops and the pole calibration process begins.

- Step 2 - Pole Calibration: Figure 3.37 shows the pole calibration waveforms during the second step of the calibration process. During the second step of the calibration process, the algorithm uses voltages v_{crefin}, $v_{crefout}$ and V_{cm}. The process of calibrating the pole location uses the same basic steps as before.

  The process starts by autozeroing all capacitors to zero charge state. The value of C_{int} is set to the value determined from the gain calibration phase and the value of C_{comp} is initially set to 0. After this, an input voltage of $v_{in} = v_{crefin}$ is applied for one clock cycle. The integrator coefficient is defined by the ratio of the voltages $v_{crefout}/v_{crefin}$. Since the predistorted coefficient is used, the output voltage of the integrator becomes $v_{out}[T_s] = v_{crefout}$ at the end of first clock cycle. Next an input voltage of $v_{in} = -v_{crefin}$ is applied for the second clock cycle followed by the $v_{in} = V_{cm}$ for the third clock cycle. Since an opposite input voltage is applied during the second clock cycle, the integrator output should ideally reach the common mode voltage V_{cm} at the end of second clock cycle. However if there are losses then the integrator output goes below the common mode voltage level.

  Writing the transfer equation for the second clock cycle we get:

$$v_{out}[2T_s] = \left(\left(\frac{C_{int} + C_{buf} + \alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{comp}}{C_{int} + C_{buf} + C_Z} v_{out}[T_s] \right) + \left(\frac{\alpha(f_s)\kappa(f_s)(1 - e^{-\frac{(1+\beta(f_s))}{2f_sR_X(C_{in}+C_{comp}+C_X+C_Y)}})C_{in}}{C_{int} + C_{buf} + C_Z} v_{in}[T_s] \right) \right) \times e^{-\frac{1}{2f_sR_Z(C_{int}+C_{buf}+C_Z)}} \tag{3.227}$$

  As the example waveforms illustrate in the pole calibration phase the output voltage of $v_{out}[T_s] = v_{crefout}$ is reached at the end of the first clock cycle since the predistortion factor g_d has been accurately set. However at the end of second clock cycle (n=2) the output voltage does not reach the value of V_{cm} initially due to the value of C_{comp} being 0 or too low. The comparator performs this comparison between the integrator output $v_{out}[2T_s]$ and $v_{cmp} = V_{cm}$ during the third clock cycle and gives a decision which is used

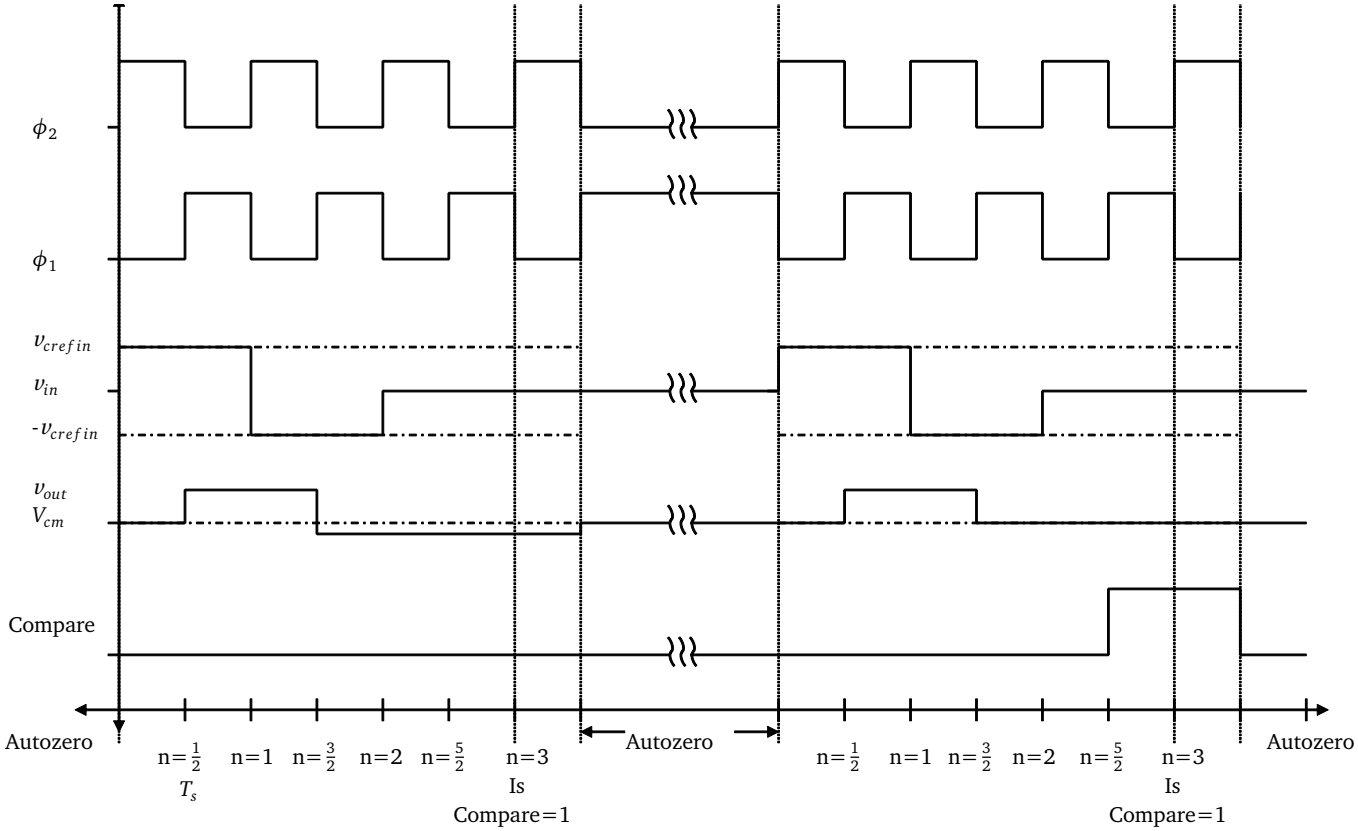


Figure 3.37: Pole calibration waveforms.

by the calibration algorithm to increase the C_{comp} value. As long as the output voltage of V_{cm} is not reached, the algorithm loops through pole calibration process, continuously increasing the value of C_{comp}. Once the correct value of the C_{comp} is found, the calibration process stops and the integrator is available to process input signals.

Figure 3.38 shows the calibration algorithm flowchart. The algorithm describes a linear iterative loop which cycles through all the values of C_{int} and C_{comp}, until the desired value is set. More efficient algorithms such as a successive approximation algorithm can also be implemented, which reduces the calibration time significantly. For example using a successive approximation algorithm the calibration cycles required for one integrator is about 160-200 clocks. Since the calibration circuits and the algorithm are simple, they are easily implemented with minimal design effort. The described algorithm is used to calculate the set of (C_{int}, C_{comp}) values for each given sampling frequency f_s, over which the integrator is supposed to operate in a $\Delta\Sigma$ modulator.

These sets of values can then be stored in a memory and be recalled as and when required. Additionally, any environmental variations such as change in temperature can also be accounted for using this calibration process. This is possible by simply running the calibration process whenever the modulator is not in use and whenever a change in the outside environment is detected that can cause the circuit components to behave differently. The only disadvantage of this algorithm is that the entire integrator is unavailable for use when it is being calibrated.

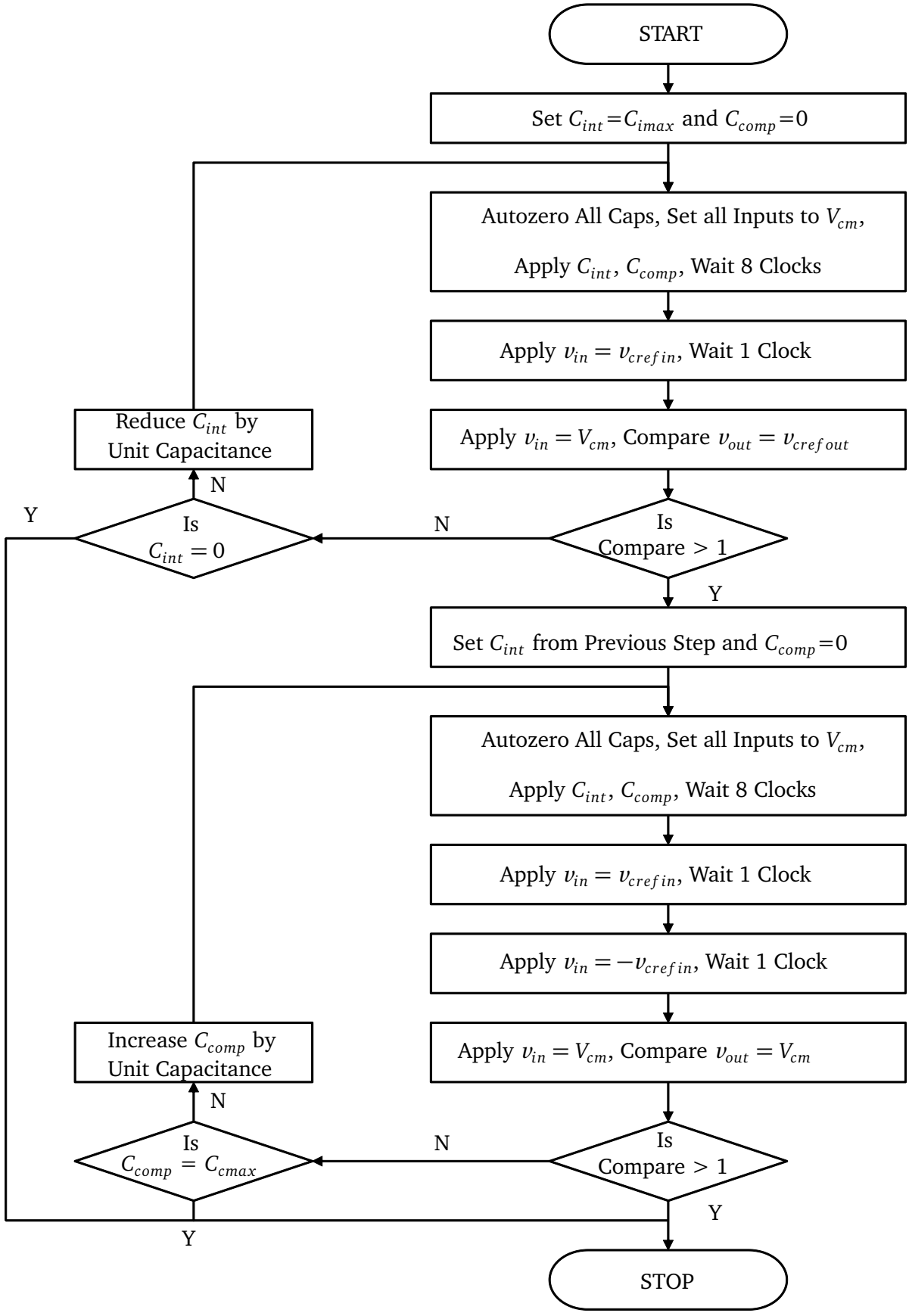


Figure 3.38: Calibration algorithm flowchart.

3.6 Simulation Results

In the previous section, three CCII stages using predistortion and memory compensation technique were proposed. It was observed that the proposed stages provide better performance in terms of reduction in power, size of components and reduced gain and loss errors due to use of predistortion and memory compensation techniques. In order to improve the integrator performance to cover a wider sampling frequency range as required by mobile communications, an adaptive calibration algorithm was introduced to correct CCII non-idealities. Figure 3.39 shows the Matlab behavioral model of the integrator where $Gain_{cc}$ and z'_{cc} are the uncompensated gain and pole of the integrator. The factor c_c is the compensation factor given by $c_c = C_{comp}/C_{int}$ and the factor g_d is the predistortion factor given by $g_d = (C_{in}/C_{int})_{distorted}/(C_{in}/C_{int})_{ideal}$.

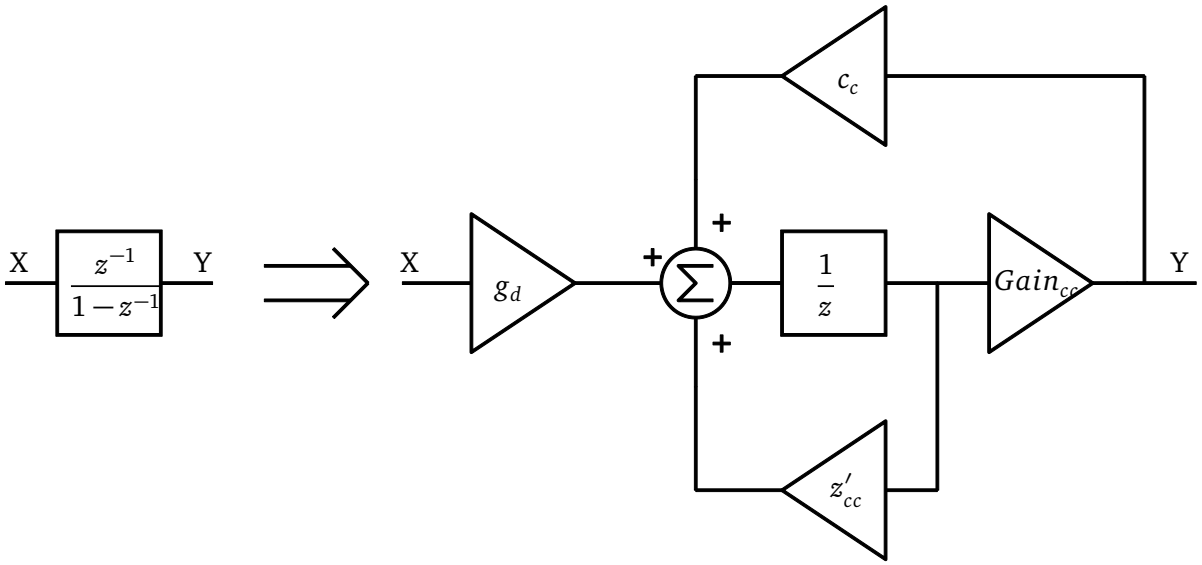


Figure 3.39: Matlab model of non-ideal integrator with gain and pole errors using predistortion and compensation.

The transfer function of the integrator is given by:

$$ITF(z) = \frac{Y(z)}{X(z)} = \frac{g_d Gain_{cc} z^{-1}}{1 - z^{-1}(z'_{cc} + Gain_{cc} c_c)} = \frac{g_d Gain_{cc} z^{-1}}{1 - z^{-1} z_{cc}} \tag{3.228}$$

where the value of the compensated pole $z_{cc} = (z'_{cc} + Gain_{cc} c_c)$ and gain $Gain_{cc}$ are given by Equations (3.80, 3.81), (3.138, 3.139), (3.195, 3.196) and (3.204, 3.205) respectively.

Based on the literature survey, the conservative value of the equivalent gains for the uncompensated and undistorted integrator is found to be in the range of $A_{cc} = 2 - 24$ for frequencies ranging from few MHz to above hundred MHz, depending on the CCII topology. Based on this A_{cc} approximation, the integrator model given previously is simulated at different frequencies using Matlab and Simulink. The first simulation test carried out on the integrator is to give it a square wave of known amplitude and frequency f_{in} and monitor the integrated output. The output of the integrator should correspond to that of a triangular wave when the sampling frequency $f_s << f_{in}$. In the presence of gain and pole errors, the integrator does not convert the waveform into a triangle wave but saturates after a certain number of integration cycles.

Figure 3.40 shows the waveform of the input square wave and integrated triangular wave for both the existing and proposed integrator at $f_{in} = 2MHz$ and $f_s = 80MHz$. The existing

integrator output is obtained by setting $g_d = 1$ and $c_c = 0$, whereas for the proposed integrator it was set according the value of $A_{cc} = 2-24$ used in the simulations. As shown in the figure, the existing solution starts saturating after a certain number of integration cycles, due to the low equivalent gains. Figure 3.41 shows the waveforms at $f_{in} = 1MHz$ and $f_s = 80MHz$. With the increase in the integration cycles for a given amplitude, we observe that the existing integrator stage produces a square wave rather than a triangular wave, whereas the proposed integrator produces a proper triangular wave due to the inclusion of g_d and c_c.

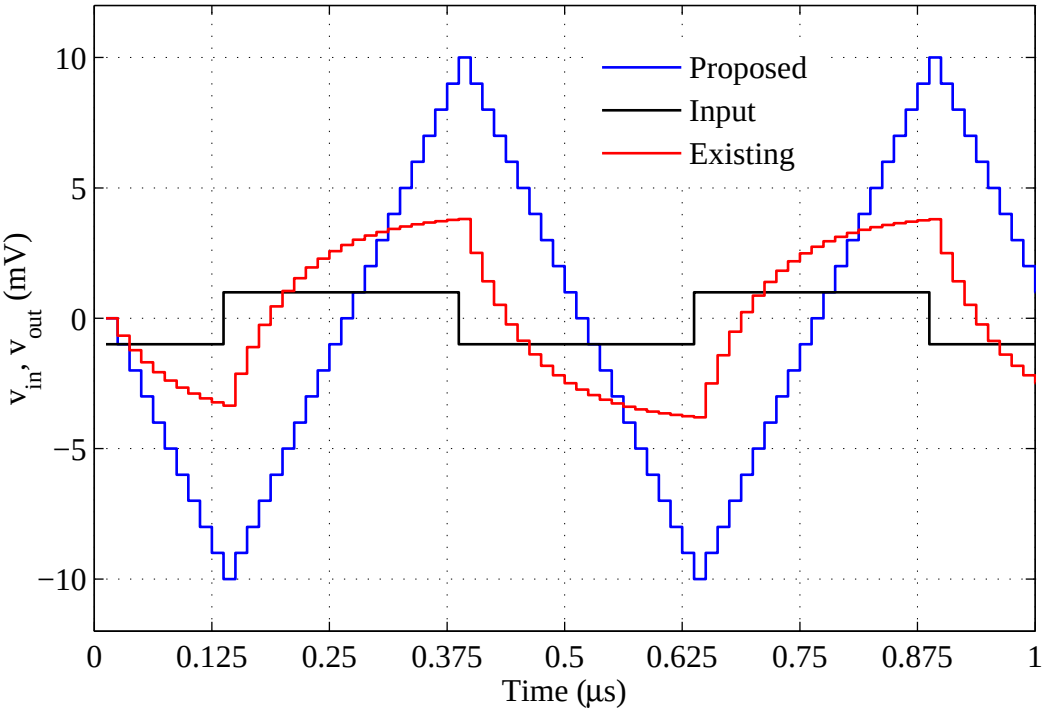


Figure 3.40: Comparison of input/output waveforms for integrator with and without predistortion/compensation techniques using input square wave of 2mV/2MHz and sampling frequency of 80MHz.

The above waveforms assume a complete cancellation of gain and pole errors which result in a perfect square to triangle wave generation from the integrator. However in practice, the presence of process variations changes the circuit properties such that the predistortion factor and compensation factor might not completely cancel the gain and pole errors. In order to check the effect of the circuit variations which result in loss of performance from the integrator, the SNDR variations for the 2nd order modulator based on the previously given integrator model are simulated. Figure 3.42 shows the 2nd order $\Delta\Sigma$ modulator based on unity-STF topology with 1.5bit ADC/DAC used for simulating the process variations. The advantage of this $\Delta\Sigma$ topology will be explained in the next chapter.

The given modulator was simulated at two different sampling frequencies and it is assumed that process variations change circuit parameters such that the actual g_d and c_c values change a maximum of -10% to +10% percent around the ideal g_d and c_c values. Figures 3.43 and 3.44 show the SNDR plots and variations against the g_d and c_c variations. As shown in the figure, without g_d and c_c, the SNDR shows a very low value while with use of g_d and c_c, the SNDR is improved substantially. Additionally it is observed that the variation in the SNDR is maximum of $\pm 5dB$ for ±10% variations in g_d and c_c. Thus it is seen that the change in the

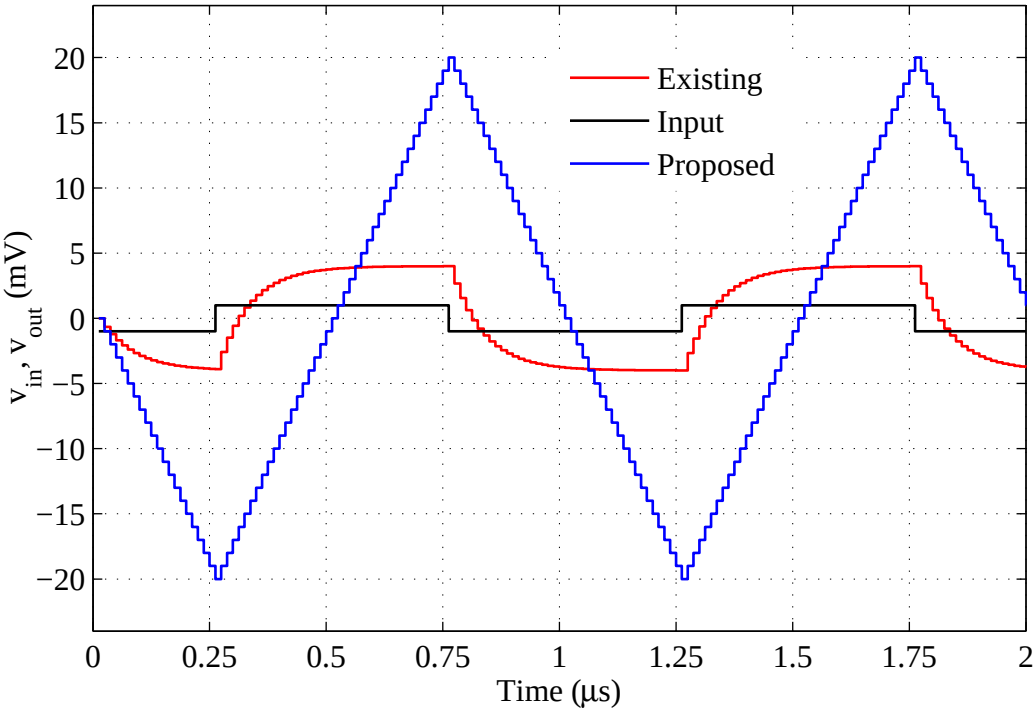


Figure 3.41: Comparison of input/output waveforms for integrator with and without predistortion/compensation techniques using input square wave of 2mV/1MHz and sampling frequency of 80MHz.

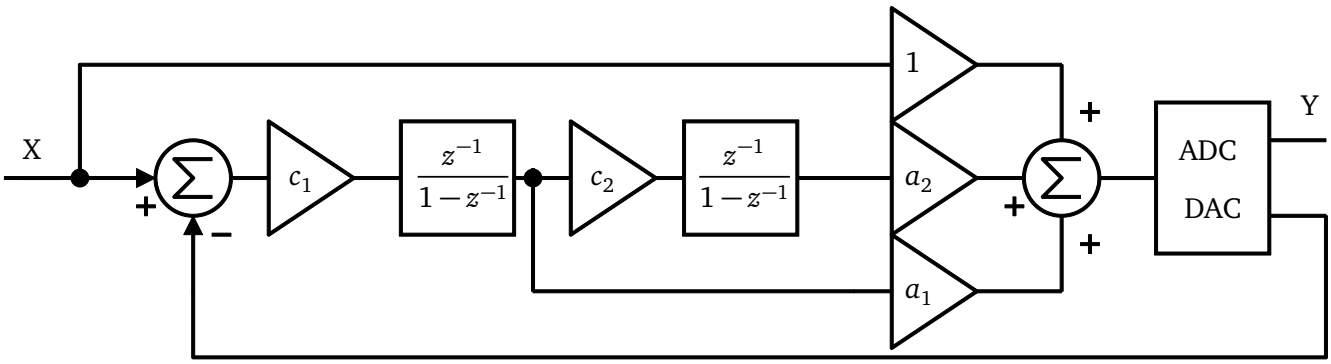
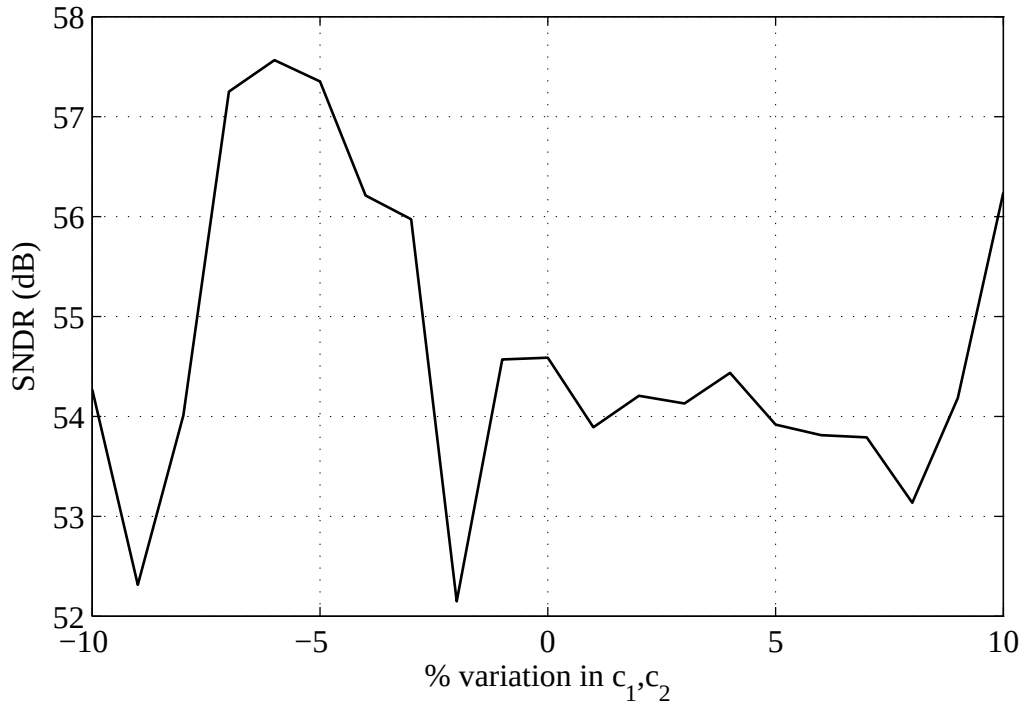


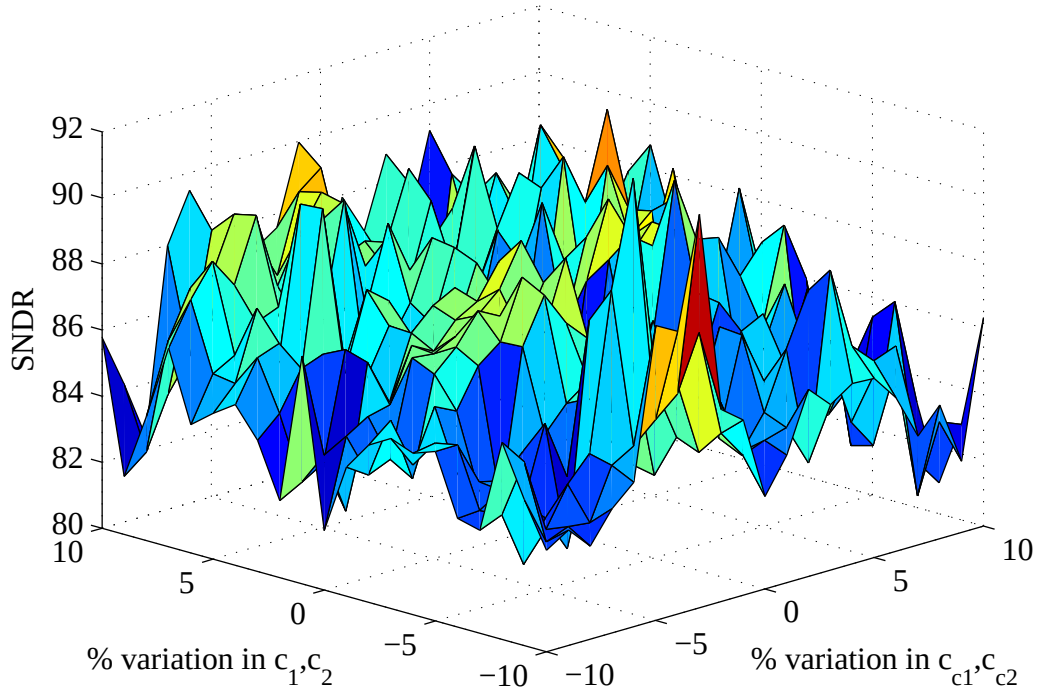
Figure 3.42: 2nd order unity-stf low distortion modulator topology using non-ideal integrator with 1.5bit DAC and ideal coefficients of c_1=0.25,c_2=1,a_1=8,a_2=4.

CCII properties during fabrication which changes the g_d and c_c, does not significantly affect the SNDR of the modulator. Normally the tolerances are well controlled during fabrication such that the maximum variation in g_d and c_c can be expected to be $\pm 1-2\%$. Thus the integrator in combination with the low distortion unity-STF topology is very suitable for the implementation of $\Delta\Sigma$ modulator.

Figures 3.45a and 3.45b show the PSD plots of the modulator for a sampling frequency of 40MHz and an input of -60dB at $f_{in} = 10.74kHz$. As the plots show, the uncompensated and undistorted integrator suffers severely from harmonics and noise leakages which cause the SNDR to come down. In contrast, the modulator using predistortion and memory compensation produces a clean spectra, thus improving the SNDR performance of the modulator. An

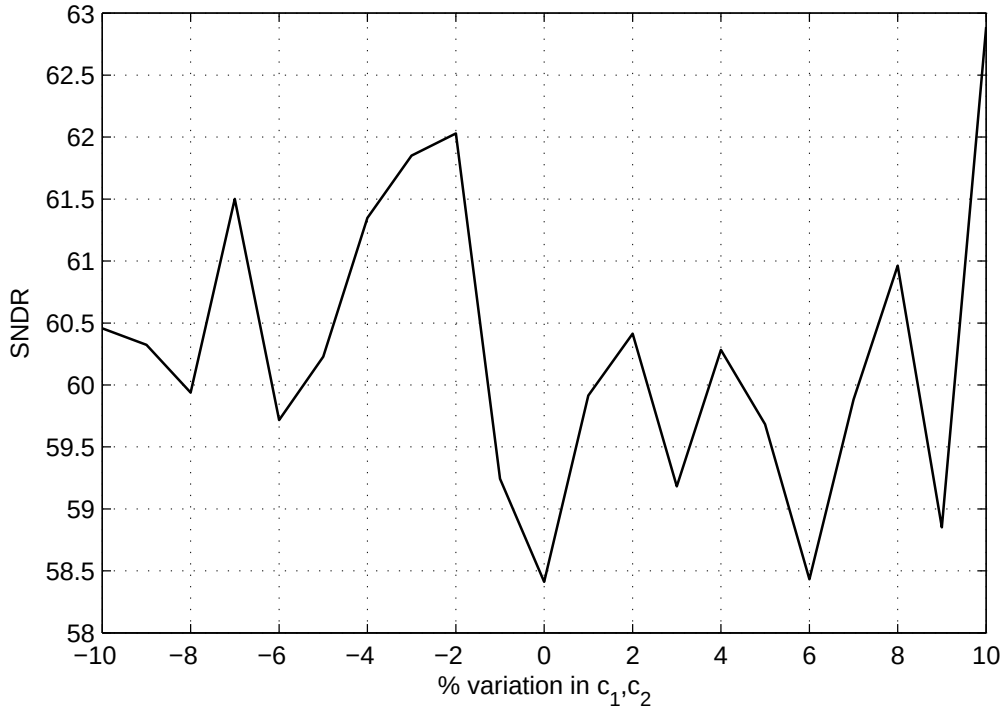


(a)

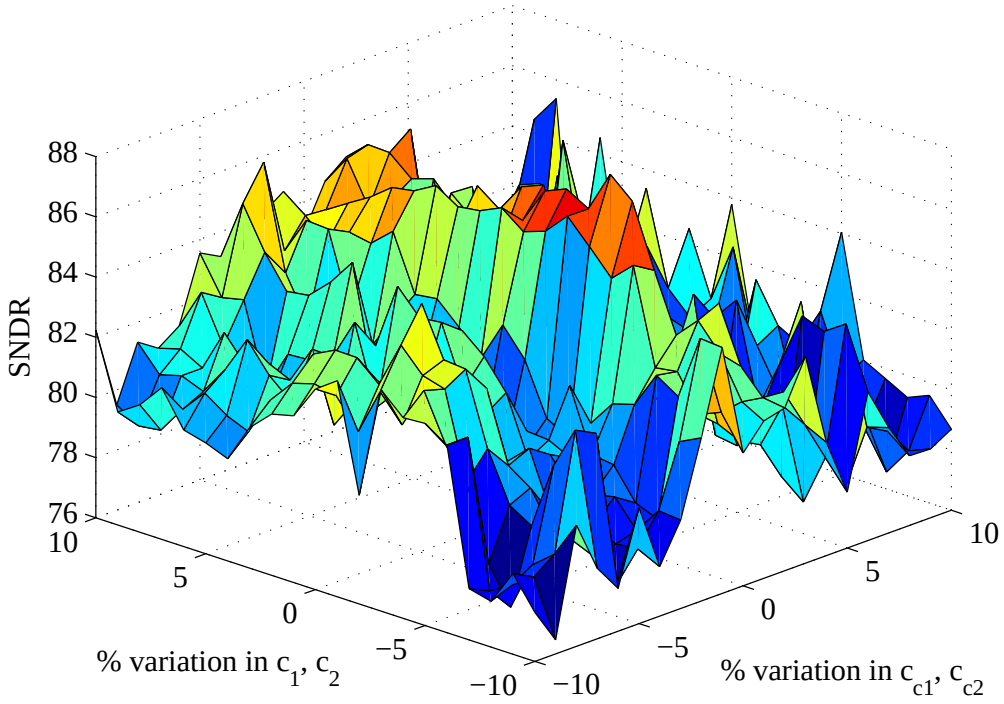


(b)

Figure 3.43: Modulator output taken at -6dBFS, f_{in}=107.4kHz, f_b=200kHz and f_s=40MHz. (a) SNDR plot for variations in the value of undistorted integrator coefficient (c_1, c_2) and no compensation factor. (b) SNDR plot for variations in the value of distorted integrator coefficient (c_1, c_2) and the compensation factor (c_{c1}, c_{c2}).

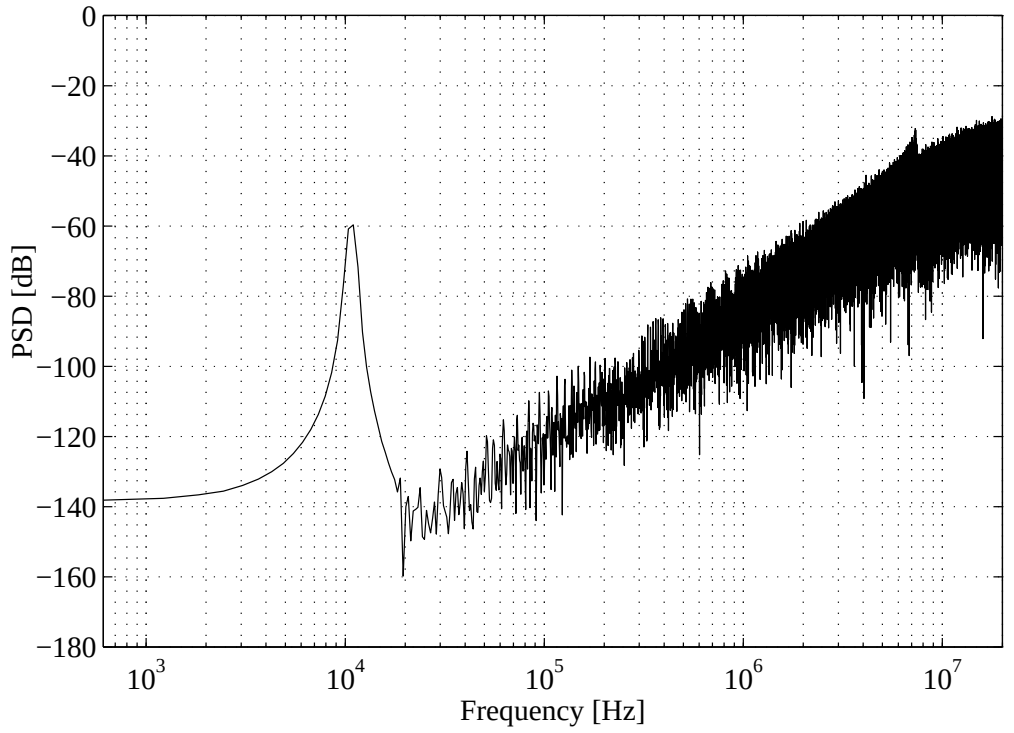


(a)

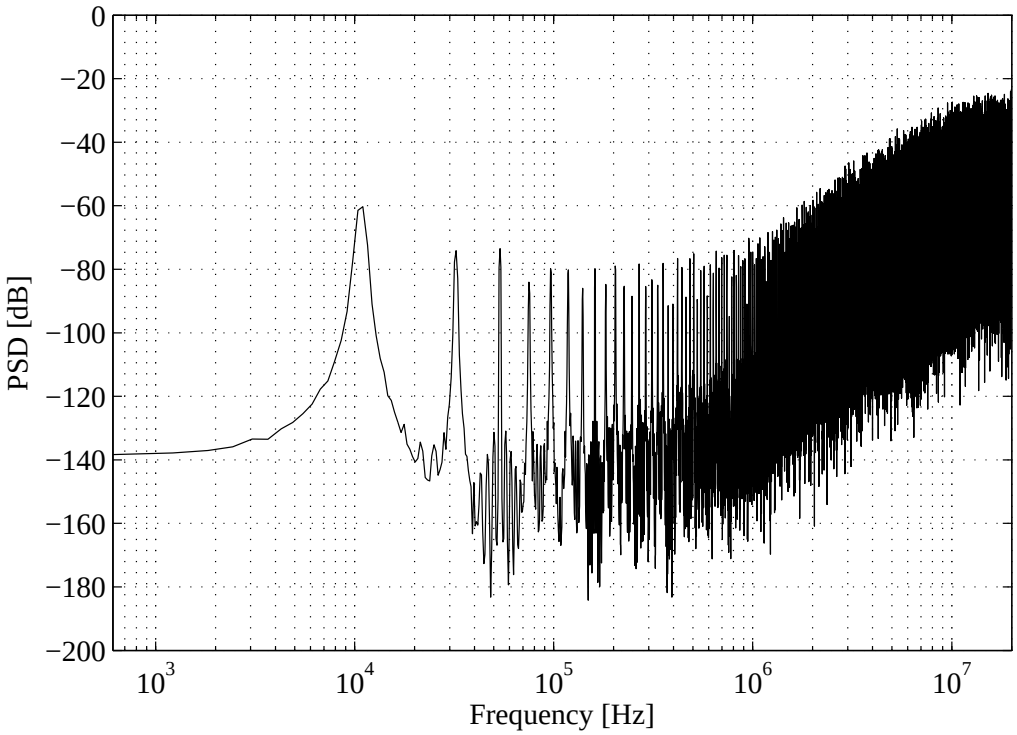


(b)

Figure 3.44: Modulator output taken at -6dBFS, f_{in}=253.9kHz, f_b=500kHz and f_s=80MHz. (a) SNDR plot for variations in the value of undistorted integrator coefficient (c_1, c_2) and no compensation factor. (b) SNDR plot for variations in the value of distorted integrator coefficient (c_1, c_2) and the compensation factor (c_{c1}, c_{c2}).



(a)



(b)

Figure 3.45: Modulator output taken at -60dBFS, f_{in}=10.74kHz, f_b=200kHz and f_s=40MHz. (a) PSD plot for distorted and compensated integrator. (b) PSD plot for uncompensated and undistorted integrator.

important difference is that in the simulation a more optimistic value for the equivalent gain A_{cc} is assumed. Assuming a more pessimistic equivalent gain results in a negative SNDR for the integrator without distortion and compensation.

3.7 Benefits and Drawback of the Approach

The main benefits of using a CCII is the design simplicity of the SC circuit. Unlike the Op-Amp which requires more design effort for achieving higher gains in advanced technology nodes, the CCII integrators rely on predistortion and memory compensation techniques to achieve the same performance. Since the reliance is on predistortion and memory compensation, the design of the CCII and the buffer becomes simple, requiring just unity voltage and current gains. This results in the use of simple circuits. Furthermore while the operating bandwidth of the Op-Amp is limited to many orders lower than the unity gain bandwidth, the CCII stages coupled with the calibration process have no such limitation and can operate at frequencies approaching its 3dB bandwidth.

Another advantage of the proposed approach is the complete removal of stability concerns. This is possible due to open loop mode of operation for the CCII integrator. There is no internal compensation required within the CCII to stabilize its performance, since the CCII operates in the open loop mode. Without internal feedback in the CCII there are less number of poles and zeros in the circuits, which results in better frequency response characteristics from the CCII integrator as a whole. This makes the proposed CCII integrators a viable option for implementing $\Delta\Sigma$ modulators in advanced technology nodes. The use of the adaptive calibration algorithm provides a more robust CCII integrator capable of operating over a wide range of sampling frequencies while requiring only few components such as a low offset comparator and a maximum of two references voltages for each integrator during the calibration phase.

There are however some challenges that still need to be addressed. Although the circuits are simpler and there exist no stability concerns, other challenges exist. Mismatch sensitivity between PMOS and NMOS transistors might affect the current gain, increase the offset and distortion. Lack of global feedback might also cause linearity problems and gain variations. These need to be controlled through tightly matched layouts and operating the CCII within its linear operating region.

3.8 Summary

In this section a class of SC circuits based on the CCII was studied. The novelty of the circuits presented here is the use of the building block called the CCII. Existing integrator architectures were studied for implementation in advanced CMOS technologies and it was observed that they were not realizable without a heavy penalty on power and area and strict design requirements. Three topologies for the CCII integrators using predistortion and memory compensation techniques were proposed and analyzed. It was shown that these topologies are viable due to the potential area and power savings they provided while not requiring any large design effort for the main active blocks, that is the CCII and the buffer. The CCII integrator provides comparable performance to Op-Amp integrator when used in combination with low distortion unity-STF topology, while reducing the design effort on the active blocks through the use of simpler architectures. The option of making it more robust through the use of an adaptive calibration to extend its performance makes the proposed integrators an attractive choice.

4 A 1V 90nm Reconfigurable 2-2 Cascade $\Delta\Sigma$ Modulator for Mobile Applications

Contents

This chapter presents the behavioral level and circuit level implementations of the 2-2 cascade $\Delta\Sigma$ modulator in 1V/90nm technology. The circuit topology as well as their properties of the individual CCII integrator are shown and discussed. Simulation results of the modulator using the MATLAB toolbox and transistor level designs in Cadence using the UMC 90nm technology and a supply voltage of 1 V are presented. The results of the modulator using a calibrated CCII integrator are also compared with the modulator using an uncalibrated version of the CCII integrator. The significant performance improvement obtained through the reduction of the harmonics and noise floor will be shown.

4.1 Specifications

In the previous section an adaptive calibration algorithm was introduced to mitigate the effects that arise from using the same CCII integrator over a wide sampling frequency range. An application area where such a calibration can be used is the field of mobile communications where the modulator needs to work at sampling frequencies ranging from few MHz to few hundred MHz to convert signal bandwidths ranging from hundreds of kHz to tens of MHz. Therefore in this chapter the design and implementation of a reconfigurable $\Delta\Sigma$ modulator intended for mobile communications is presented. The modulator will be used to convert the main mobile standards which are in use namely, Global System for Mobile Communications (GSM), Bluetooth

(BT), Global Positioning System (GPS), Universal Mobile Telecommunication System (UMTS) and Digital Video Broadcasting-Handheld (DVB-H). Based on a study of literature and other reconfigurable modulators, the bandwidth and SNDR requirements of these standards are given in Table 4.1.

Table 4.1: Modulator specifications

Standard	GSM	BT	GPS	UMTS	DVB-H
Signal Bandwidth (MHz)	0.2	0.5	1	2	4
Minimum SNDR (dB)	75	70	60	60	55

4.2 System Level Design

The previous section introduced the specifications that need to be achieved by the modulator. From the specifications it is clear that the modulator needs to provide high resolution for low bandwidths and high speed operation for large bandwidths. The technology and voltage are chosen to be 90nm/1V, therefore technology considerations such as increased parasitics, non-idealities and reduced dynamic range in transistors need to be taken into account during the selection of modulator topology. In literature there exist many modulator topologies such as Boser-Wooley Modulator, Silva-Steensgaard Structure and Error-Feedback Structure. While these structures provide some advantages, they are also more complex due to the presence of many feedback and feedforward paths.

4.2.1 Modulator Architecture

In order to process multiple mobile standards, the modulator architecture needs to be highly agile and configurable with minimal change at hardware level. In this situation, Figure 4.1 shows the block diagram of the 2nd order modulator that presents a good tradeoff in comparison to the previous architectures by providing less number of feedback and feedforward paths, reducing circuit complexity and using a almost linear 1.5 bit DACs without resorting to DAC calibration techniques such as DEM [57, 58].

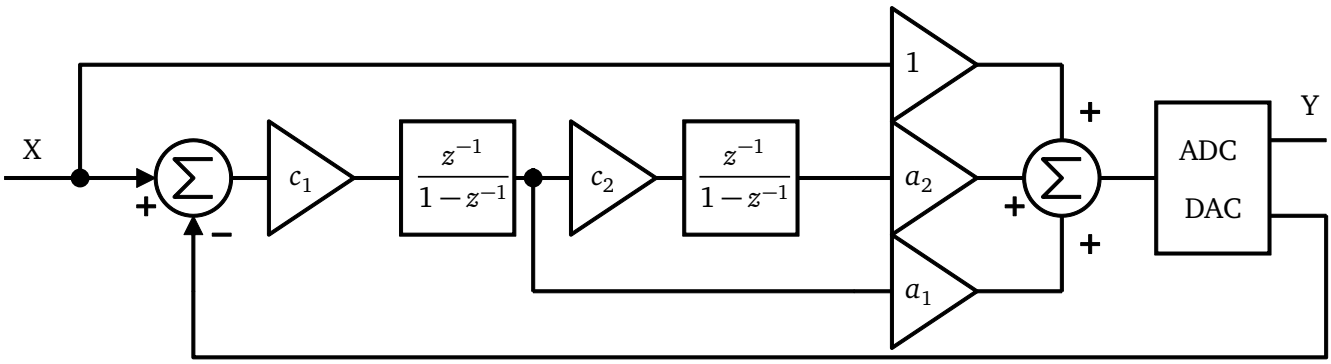


Figure 4.1: 2nd order unity-stf low distortion modulator topology using non-ideal integrator with 1.5bit DAC.

The input output relationship of the 2nd order modulator is given as:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{4.1}$$

where $E(z)$ is the quantization error and $X(z)$ is the input signal.

The STF and NTF of the 2nd order modulator are given by:

$$STF(z) = 1 \tag{4.2}$$

$$NTF(z) = \frac{(1-z^{-1})^2}{1 + z^{-1}(a_1c_1 - 2) + z^{-2}(1 + a_2c_1c_2 - a_1c_1)} \tag{4.3}$$

Setting the values of the feedforward coefficients as:

$$a_1 = \frac{2}{c_1} \tag{4.4}$$

$$a_2 = \frac{1}{c_1c_2} \tag{4.5}$$

and substituting in the Equation 4.3 we get the NTF of the 2nd order modulator as:

$$NTF(z) = (1-z^{-1})^2 \tag{4.6}$$

From Equations 4.1, 4.2 and 4.6 we see that ideally the modulator does not process the input signal and gives a 2nd order noise shaping under the conditions shown in Equations 4.4 and 4.5 for the feedforward coefficients. Furthermore for the given modulator the output taken at the 2nd integrator is given as:

$$X_2(z) = -c_1c_2z^{-2}E(z) \tag{4.7}$$

From the previous equation it is seen that the output of the second integrator is the quantization error itself, which is a useful feature of this modulator. If we want to extend the order of the modulator using multistage cascade, then the cascading stages can be directly fed the quantization error of the preceding stage using the second integrator output. This simplifies the circuitry to a great extent, as no further summing or differencing blocks are needed to extract the quantization errors from preceding stages.

Figure 4.2 shows the reconfigurable multistage noise shaping 2-2 cascade modulator using this technique. The presented modulator can work as a standalone 2nd order modulator converting low bandwidth signals and as a 4th order cascade modulator converting high bandwidth signals.

As before the feedforward coefficients in this modulator are given as:

$$a_1 = \frac{2}{c_1}, a_2 = \frac{1}{c_1c_2} \tag{4.8}$$

$$a_3 = \frac{2}{c_3}, a_4 = \frac{1}{c_3c_4} \tag{4.9}$$

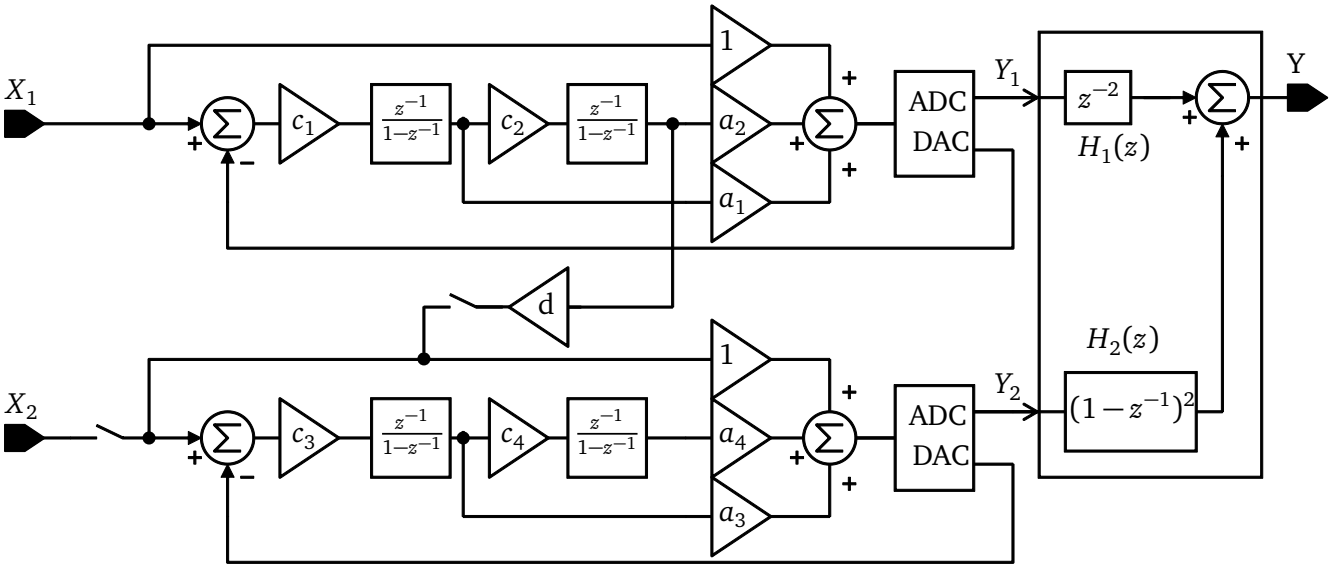


Figure 4.2: 4th order unity-stf low distortion 2-2 cascade modulator topology using non-ideal integrator with 1.5bit DAC.

The transfer function of the first stage, second stage in standalone mode is given as:

$$Y_1(z) = X_1(z) + NTF_1(z)E_1(z) = X_1(z) + (1-z^{-1})^2 E_1(z) \tag{4.10}$$

$$Y_2(z) = X_2(z) + NTF_2(z)E_2(z) = X_2(z) + (1-z^{-1})^2 E_2(z) \tag{4.11}$$

The transfer function in cascade mode is given as:

$$Y_1(z) = X_1(z) + (1-z^{-1})^2 E_1(z) \tag{4.12}$$

$$Y_2(z) = -dc_1c_2z^{-2}E_1(z) + (1-z^{-1})^2 E_2(z) \tag{4.13}$$

where the interstage scaling factor d is used to cancel the effects of the first stage coefficients c_1c_2.

Combining the two outputs in cascade mode using the digital cancellation filter we get the output as:

$$\begin{aligned} Y(z) =& Y_1(z)H_1(z) + Y_2(z)H_2(z) \\ =& (X_1(z) + (1-z^{-1})^2 E_1(z))z^{-2} + (-dc_1c_2z^{-2}E_1(z) + (1-z^{-1})^2 E_2(z))(1-z^{-1})^2 \\ =& X_1(z) + E_2(z))(1-z^{-1})^4 \end{aligned} \tag{4.14}$$

where $H_1(z) = z^{-2}$, $H_2(z) = (1-z^{-1})^2$ and the factor $d = 1/(c_1c_2)$ has been applied to cancel the first stage quantization error.

As seen from the previous equations, Unity-STF stages are advantageous in low voltage CMOS technologies, since they have less requirements from the active circuitry. This is due to the active

circuitry processing only the error signal while the input signal is sent unprocessed to the output. The modulator processes only the quantization error, hence the first stage quantization error can be readily extracted as shown in the previous figure at the output of the second integrator and sent to the second stage either directly or by multiplying it with the factor d. The main features of this architecture are [59]:

- Low sensitivity to non-idealities of the active circuit such as the CCII, the buffer and the switches. This is a useful feature since the CCII properties such as Slew-Rate (SR), non-linear gains and the large signal parameters have no significant effects on the signal conversion process. This leads to a more robust design when the modulator is used to convert large signal bandwidths where higher sampling frequencies are usually needed. Furthermore this architecture is useful for low to medium gain active blocks, such as the gain of the CCII integrator which is usually very low and defined by the port Z and port X parasitics.
- By appropriately setting the coefficients of the modulator, the internal voltage swings at the different nodes of the modulator are vastly reduced. Since the voltage swings are minimal, there is no requirement from the CCII such as wide linear operating range of currents and voltages. This simplifies the design and choice of the CCII and the buffer vastly as very simple circuits based on current mirrors, class AB structures can be used for the design. Furthermore huge power savings are possible due to the use of low swing requirements at internal nodes, which results in lower currents for the active blocks such as CCII and the buffer.
- Use of the Unity-STF enables higher overload levels compared to other architectures such as Boser-Wooley, Silva-Steensgaard. Therefore larger SNDR can be expected in this architecture.
- Compared to multiple in-loop feedback that are required in Boser-Wooley modulator, this structure requires only one in-loop feedback. Thus only one DAC is needed.
- The use of a 1.5bit DAC which provides decreased quantization error, output swings, power and area consumption compared to a 1-bit DAC. An almost inherently linear DAC is obtained while avoiding the multibit DAC calibration schemes such as DEM.
- Since the quantization noise is readily available at the output of the modulator, the second order modulator can be extended to higher orders through the use of cascade with the simple connection of the output of the first stage as the input of the second stage. This reduces the overall complexity of implementing higher order modulators and enables better matching and performance.

4.2.2 Matlab Modeling and Simulations

In order to choose the optimum coefficient values and sampling frequencies necessary for achieving the minimum SNDR shown in Table 4.1, Matlab simulations need to be performed. Based on these simulations the coefficients can be chosen such that the requirements on the active blocks, that is on the CCII and buffer are minimized. Furthermore Matlab simulations can also reveal the minimum and maximum tolerance of the CCII integrator to variations in the

predistortion factor and the compensation capacitor which results in a drop of the SNDR for the modulator. To this end, the model of the 4th order modulator shown in Figure 4.2 is used. The 4th order modulator is simulated for various combinations of the coefficients based on Equations 4.8 and 4.9 to check for output swing required from the active blocks of the integrator.

Since analyzing all combinations of coefficients is tedious, the variations are limited by the following conditions. The coefficient variations for c_1, c_2 upto 1 and resulting in powers of 2 for a_1, a_2 are considered. Furthermore it is assumed that both the 2nd order modulators in the cascade are similar in properties. That is $c_1 = c_3$, $c_2 = c_4$, $a_1 = a_3$ and $a_2 = a_4$. This makes the design space for exploring coefficients to a small subset. Table 4.2 and Figures 4.3, 4.4 shows the results of these simulations.

Table 4.2: Modulator coefficient variations and output swings

c_1,c_3	c_2,c_4	a_1,a_3	a_2,a_4	d	Int_1 (%)	Int_2 (%)	Int_3 (%)	Int_4 (%)
0.25	0.25	8	16	16	24.9	9.9	39.9	9.9
0.25	0.5	8	8	8	24.9	14.9	39.9	19.9
0.25	1	8	4	4	24.9	24.9	39.9	39.9
0.5	0.25	4	8	8	49.8	14.9	79.8	19.9
0.5	0.5	4	4	4	49.8	24.9	79.8	39.9
0.5	1	4	2	2	49.8	49.8	79.8	79.8
1	0.25	2	4	4	99.5	24.9	99.5	44.8
1	0.5	2	2	2	99.5	49.8	99.5	84.6
1	1	2	1	1	99.5	99.5	99.5	99.5

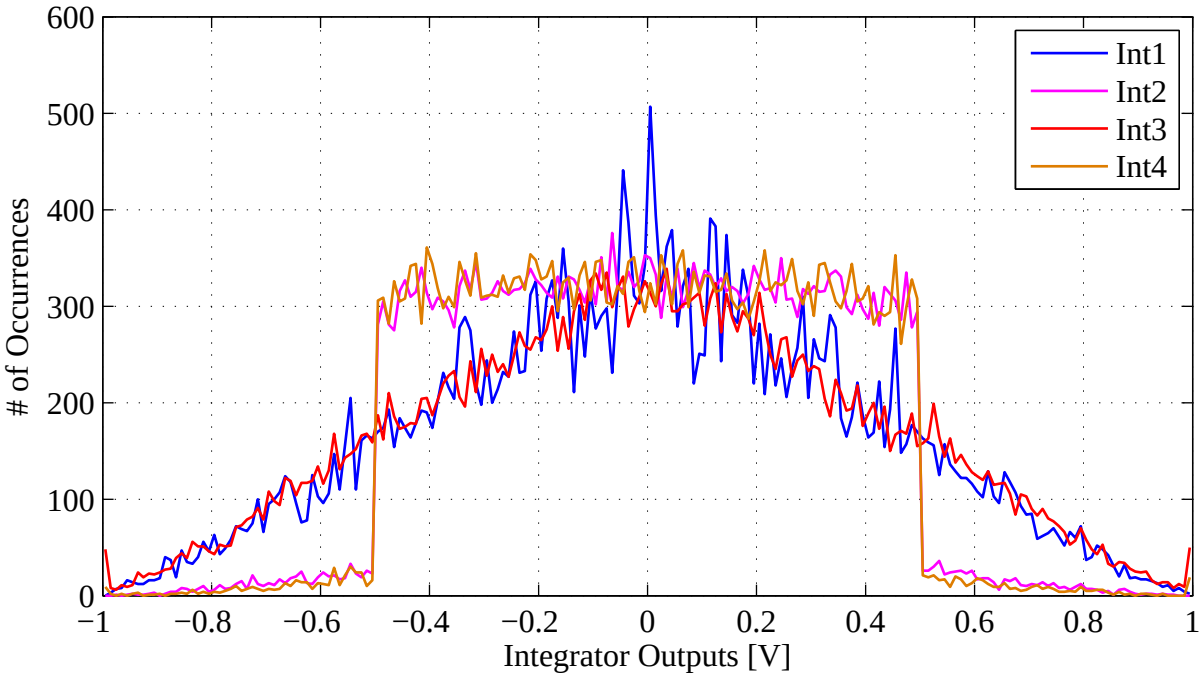


Figure 4.3: Output swings for -6dBFS input signal and $\{c_1, c_2, a_1, a_2\}$={1,1,2,1}.

From the table it is observed that smaller coefficients result in smaller output swings on the integrator. However smaller coefficients also require smaller unit capacitors and result in large

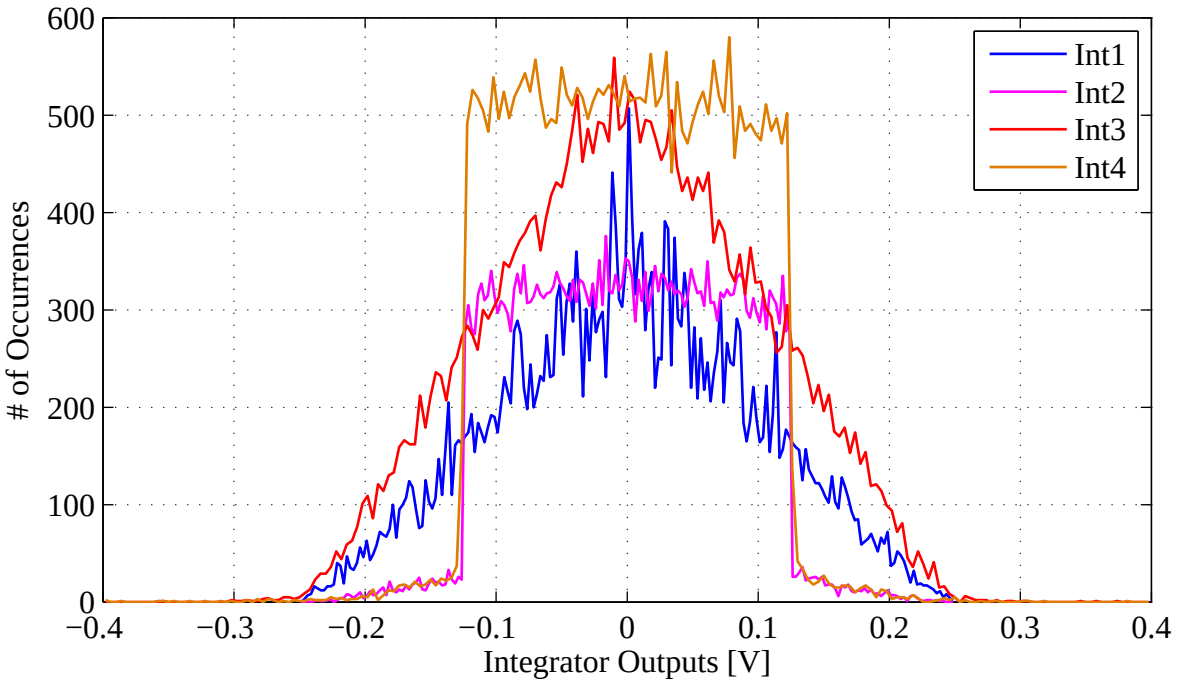


Figure 4.4: Output swings for -6dBFS input signal and $\{c_1, c_2, a_1, a_2\}$={0.25,1,8,4}.

variations between the size of capacitors used to realize the coefficients c_1, c_2, a_1, a_2. Therefore as a tradeoff between having smaller output swings and smaller variations between size of the capacitors the coefficients $c_1 = c_3 = 0.25$, $c_2 = c_4 = 1$, $a_1 = a_3 = 8$, $a_2 = a_4 = 4$ and $d = 4$ are chosen to implement the design. This combination results in the least number of unit capacitors at the expense of slightly larger output swings on the second, third, and fourth integrators.

Using the chosen coefficients, further simulations are carried for the various mobile standards in order to determine the minimum value of the sampling frequency, the OSR and the modulator order that are required to achieve the required SNDR given in Table 4.1. Assuming an equivalent gain of 45dB for the CCII integrator, Table 4.3 shows the minimum requirements and Figures 4.5, 4.6 show the plot of the PSD for -6dBFS input signal for the various standards. As illustrated, the chosen OSR and sampling frequency provide a SNDR performance well above the minimum requirements, leaving a large margin for the circuit design phase. The 2nd order modulator is sufficient for bandwidths upto 1MHz and 4th order modulator is used for bandwidth above 1MHz upto 4MHz. The behavioral models are simulated using the equivalent gains in the simulations and all other parameters such as SR are assumed to be ideal.

Table 4.3: Modulator extended specifications

Standard	GSM	BT	GPS	UMTS	DVB-H
Order	2	2	2	4	4
OSR	100	80	40	30	15
f_s (MHz)	40	80	80	120	120

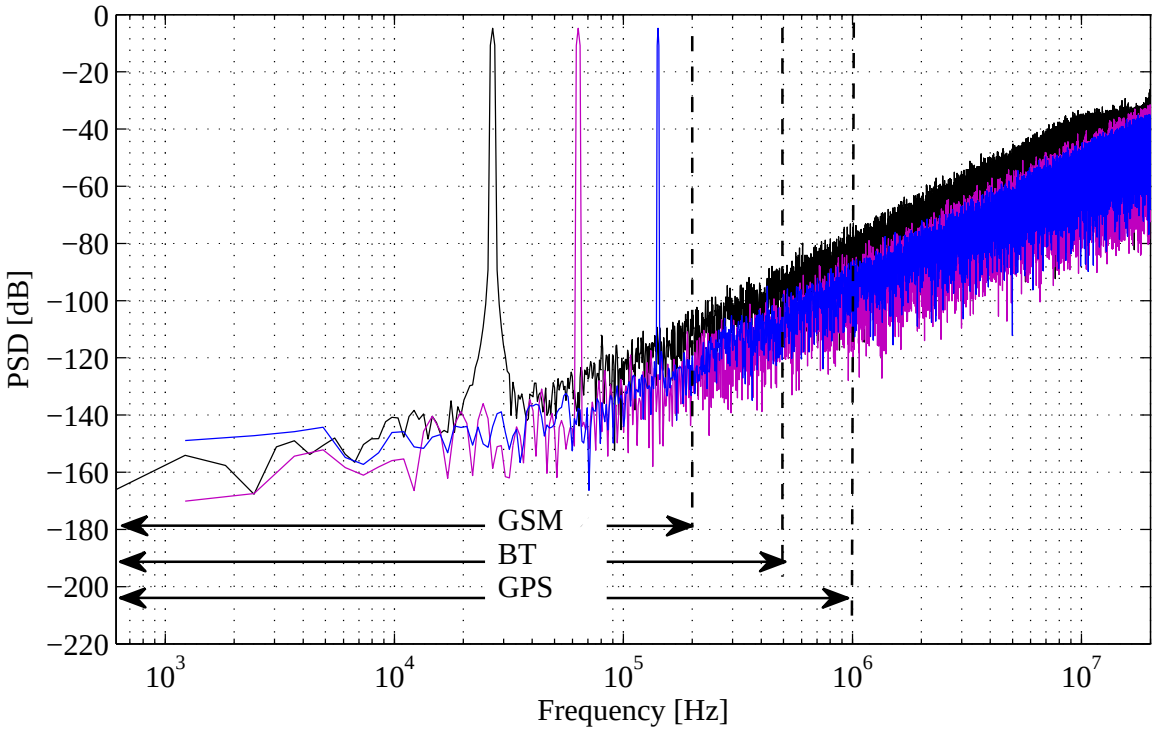


Figure 4.5: 2nd order modulator PSD for -6dBFS input signal at f_s={40MHz,80MHz,80MHz} and f_b={0.2MHz,0.5MHz,1MHz} respectively.

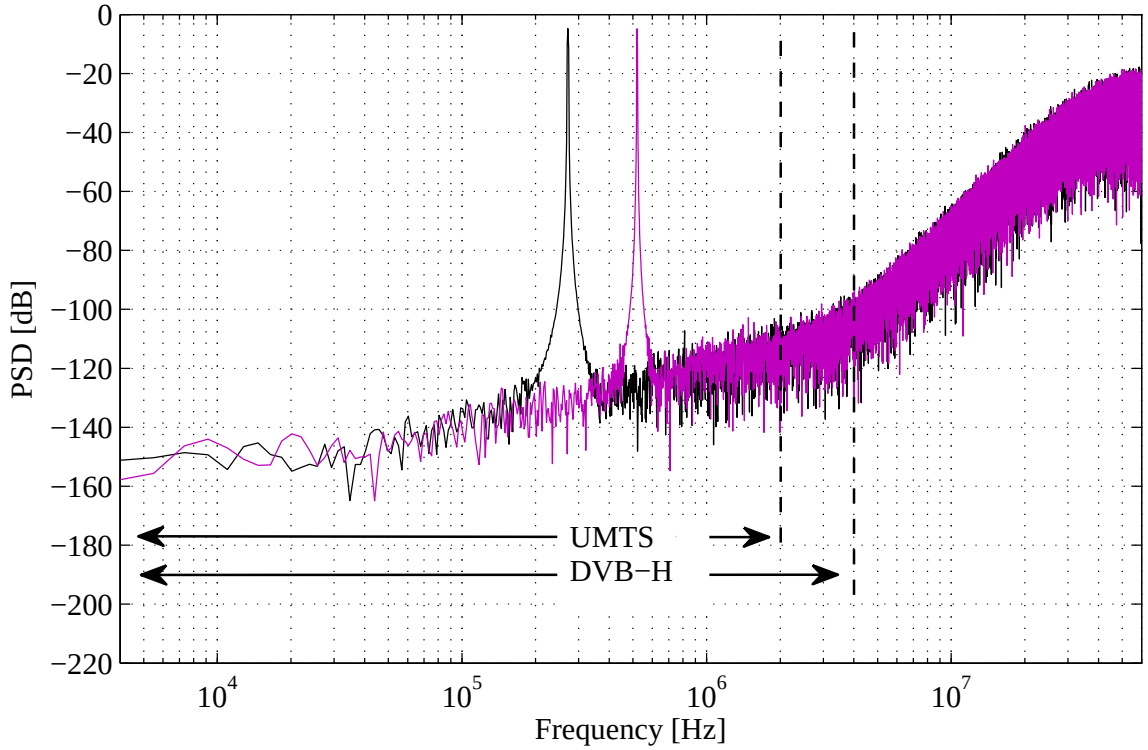


Figure 4.6: 4th order modulator PSD for -6dBFS input signal at f_s={120MHz,120MHz} and f_b={2MHz,4MHz} respectively.

4.3 Circuit Design

The extended specifications derived in the previous section form the starting point for the SC implementation of the modulator. The technology chosen is a UMC 90nm with 1V supply voltage, therefore a fully differential implementation is preferred over the single ended version in order to cancel out the even order effects such as switch charge injection, clock feedthrough, even order harmonics and to provide higher immunity to noise sources. Based on the results obtained from the previous section such as the output swings and bandwidths of the integrator, the CCII and the buffer can be designed to achieve low power consumption.

4.3.1 Fully Differential SC Modulator Implementation

Figure 4.7 shows the SC implementation of the 4th order reconfigurable 2-2 cascade modulator. The modulator consists of two similar 2nd order stages with each made up of two fully differential CCII integrators, passive analog adder before the ADC, 1.5bit ADC and DAC. As illustrated, the modulator is driven by a two phase non-overlapping clocks along with their delayed versions $\phi_1, \phi_{1d}, \phi_2, \phi_{2d}$. These clocks control the integration and sampling operations in the $\Delta\Sigma$ modulator. The sizes of the various capacitors are given in Table 4.4. The first and third integrators consist of three capacitors that are similar in size and are responsible for applying the input signal and the positive or negative reference depending on the feedback DAC outputs, A_1,B_1,A_2,B_2. Each of the 2nd order modulators can be driven separately using input signals and thus are able to operate in parallel if necessary. When En_c is enabled, the two 2nd order modulators are cascaded to form a 4th order modulator.

Table 4.4: Capacitance values in Figure 4.7

Capacitor	C_{i1}	C_{i2}	C_{i3}	C_{a1}	C_{a2}	C_{i4}	C_{i5}	C_{i6}	C_{i7}	C_{i8}	C_{a3}	C_{a4}
Value (fF)	250	1000	62.5	500	250	250	1000	62.5	750	187.5	500	250

The clock signals $\{M_{11}, M_{12}, M_{13}, M_{14}\}$, $\{M_{21}, M_{22}, M_{23}, M_{24}\}$, $\{M_{31}, M_{32}, M_{33}, M_{34}\}$ and $\{M_{41}, M_{42}, M_{43}, M_{44}\}$ are controlled by the digital logic using a 2-to-4 decoder. The 2-to-4 decoder and the programmable capacitors corresponding to each integrator are selectively enabled during the calibration phase using the enable signals $\{En_1, En_2\}$, $\{En_3, En_4\}$,$\{En_5, En_6\}$,$\{En_7, En_8\}$ so that each integrator can be calibrated separately. Using the enable signals and decoders, each integrator can be taken offline and calibrated by applying the calibration reference input signal $\{v_{crip}, v_{crin}\}$ and comparing the outputs of the integrator $\{Int_{1p}, Int_{1n}\}$, $\{Int_{2p}, Int_{2n}\}$, $\{Int_{3p}, Int_{3n}\}$ and $\{Int_{4p}, Int_{4n}\}$ with the calibration reference output signal $\{v_{crop}, v_{cron}\}$.

Tables 4.5 and 4.6 show the truth tables for the 2-to-4 decoders the cascade clock signals $\{M_{35}, M_{36}\}$. The decoders used for the first, second and fourth integrators are similar, while the third integrator has an additional control enable signal called En_c which is used to enable cascade mode of operation for the modulator. When En_c is enabled, the third integrator cannot be calibrated since its is always connected to the output of the second integrator.

The capacitors C_{i1}, C_{i2},C_{i4} and C_{i5} are used to sample the input signals and reference voltages respectively. A positive reference is applied if the DAC outputs A_1,A_2 are enabled and a negative

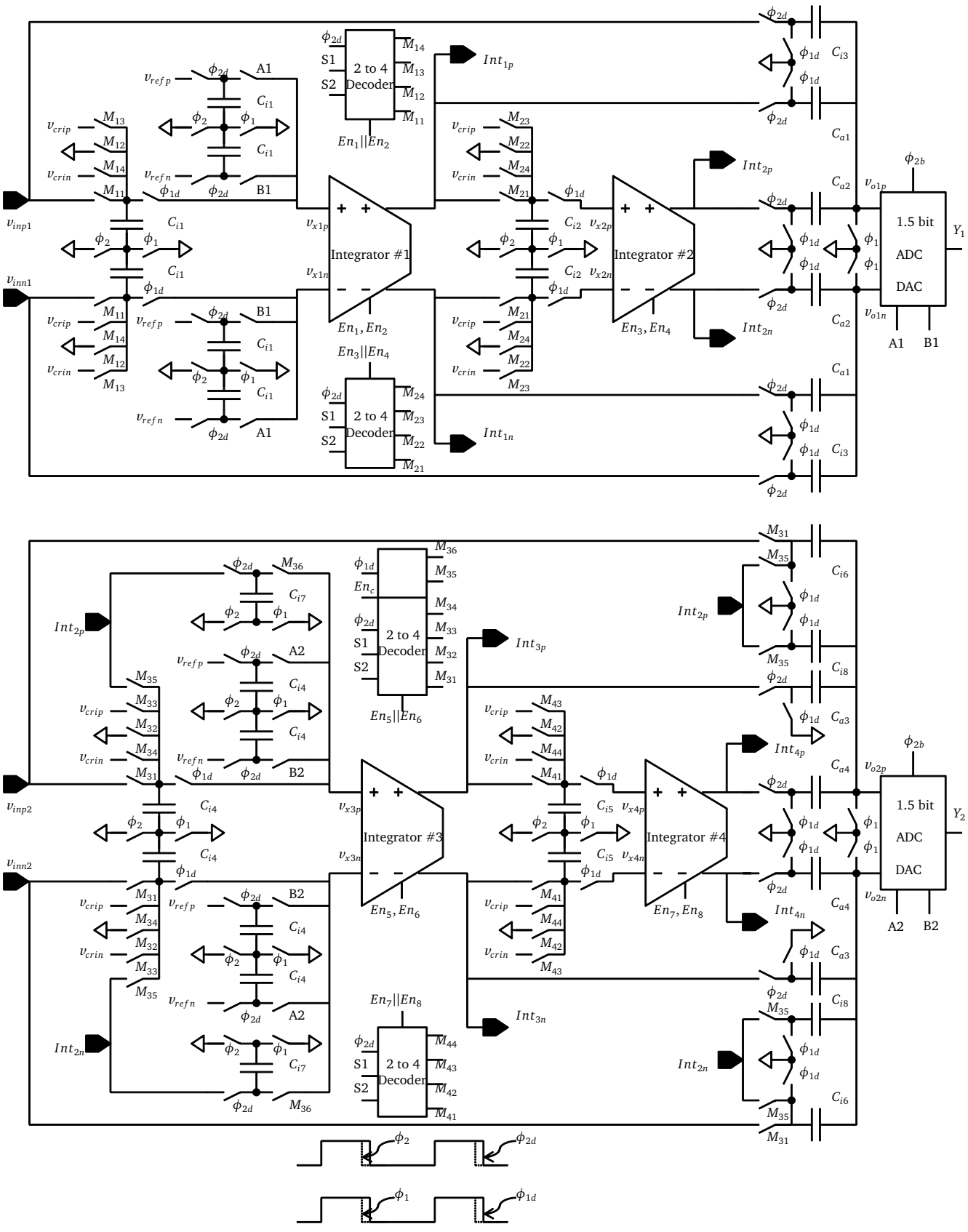


Figure 4.7: 4th order unity-stf low distortion 2-2 cascade modulator topology using passive analog adder and 1.5bit DAC.

Table 4.5: Truth table for 2-to-4 decoders of first, second, fourth integrator in Figure 4.7

$En_1 \| \| En_2, En_3 \| \| En_4$, $En_7 \| \| En_8$	S1	S2	M_{11}, M_{21}, M_{41}	M_{12}, M_{22}, M_{42}	M_{13}, M_{23}, M_{43}	M_{14}, M_{24}, M_{44}
0	X	X	ϕ_{2d}	0	0	0
1	0	0	ϕ_{2d}	0	0	0
1	0	1	0	ϕ_{2d}	0	0
1	1	0	0	0	ϕ_{2d}	0
1	1	1	0	0	0	ϕ_{2d}

Table 4.6: Truth table for 2-to-4 decoders of third integrator in Figure 4.7

En_c	$En_5 \| \| En_6$	S1	S2	M_{31}	M_{32}	M_{33}	M_{34}	M_{35}	M_{36}
1	X	X	X	0	0	0	0	ϕ_{2d}	ϕ_{1d}
0	0	X	X	ϕ_{2d}	0	0	0	0	0
0	1	0	0	ϕ_{2d}	0	0	0	0	0
0	1	0	1	0	ϕ_{2d}	0	0	0	0
0	1	1	0	0	0	ϕ_{2d}	0	0	0
0	1	1	1	0	0	0	ϕ_{2d}	0	0

reference is applied if the DAC outputs B_1, B_2 are enabled. The interstage scaling factor $d = 4$ during the cascade mode of operation for the modulator is achieved by enabling additional capacitors C_{i7} and C_{i8}. The combination of $(C_{i4} + C_{i7})$ and $(C_{i5} + C_{i8})$ together sample four times the signal from the second integrator in comparison to the reference voltage which is sampled only once using C_{i4}. Thus an interstage factor $d = 4$ is generated without the use of an interstage amplifier.

4.3.2 Fully Differential CCII Integrator Implementation

Figure 4.8 and 4.9 shows the SC implementation of the integrators and the programmable capacitor blocks. The integrator consists of two single ended CCIIs, two single ended buffers, two programmable capacitor blocks (C_{int}, C_{comp}) for adjusting the predistortion factor and compensation factor.

The integrators were chosen to have coefficients 0.25 and 1 based on which sizes 250fF and 1pF were chosen for the sampling capacitors. For a sampling capacitance of 250fF the integration capacitor should ideally have a value of 1pF. However as the non-ideal analysis showed, the buffer input and the port Z of the CCII also present certain capacitances which effectively get presented as integration capacitance in addition to C_{int}. Therefore taking this into consideration, the effective C_{int} that is required is less than 1pF. In this design including the buffer input capacitance, port Z parasitic capacitance and assuming a safe margin, the maximum value of C_{int} is chosen as approximately to be 850fF.

Based on the behavioral simulations in the previous chapter for a 2nd order modulator, it was observed that the change in SNDR was maximum $\pm 5dB$ for variations upto $\pm 10\%$ in the C_{int} values. In order to reduce the SNDR variation to within $\pm(1-2)dB$, we assume a variation of less than $\pm 2\%$ which results in the maximum unit capacitance size of 17fF. Using a unit capacitance,

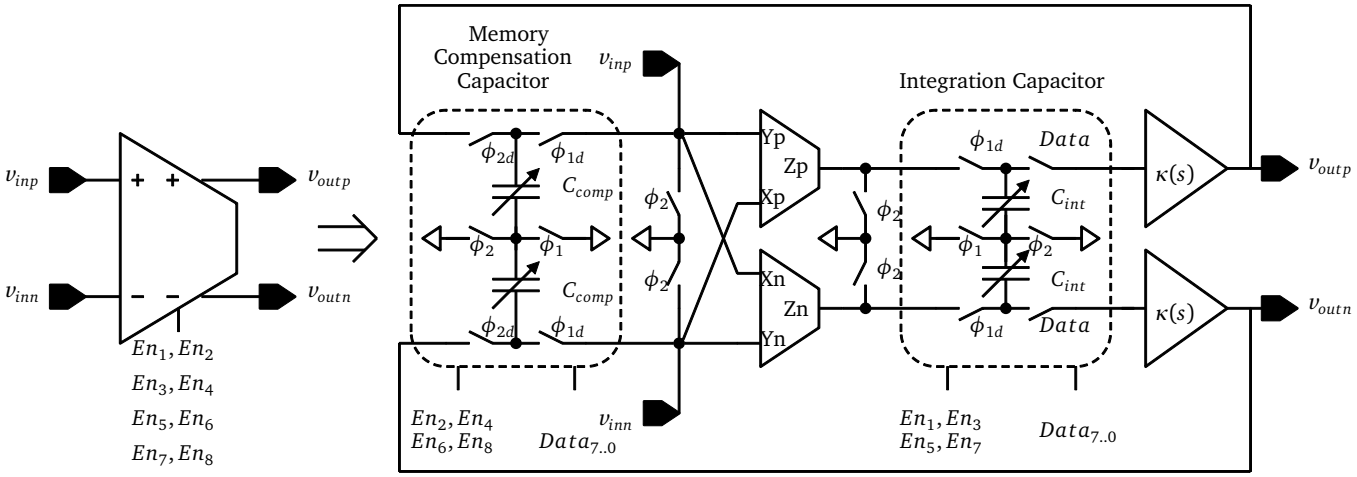


Figure 4.8: Integrator topology.

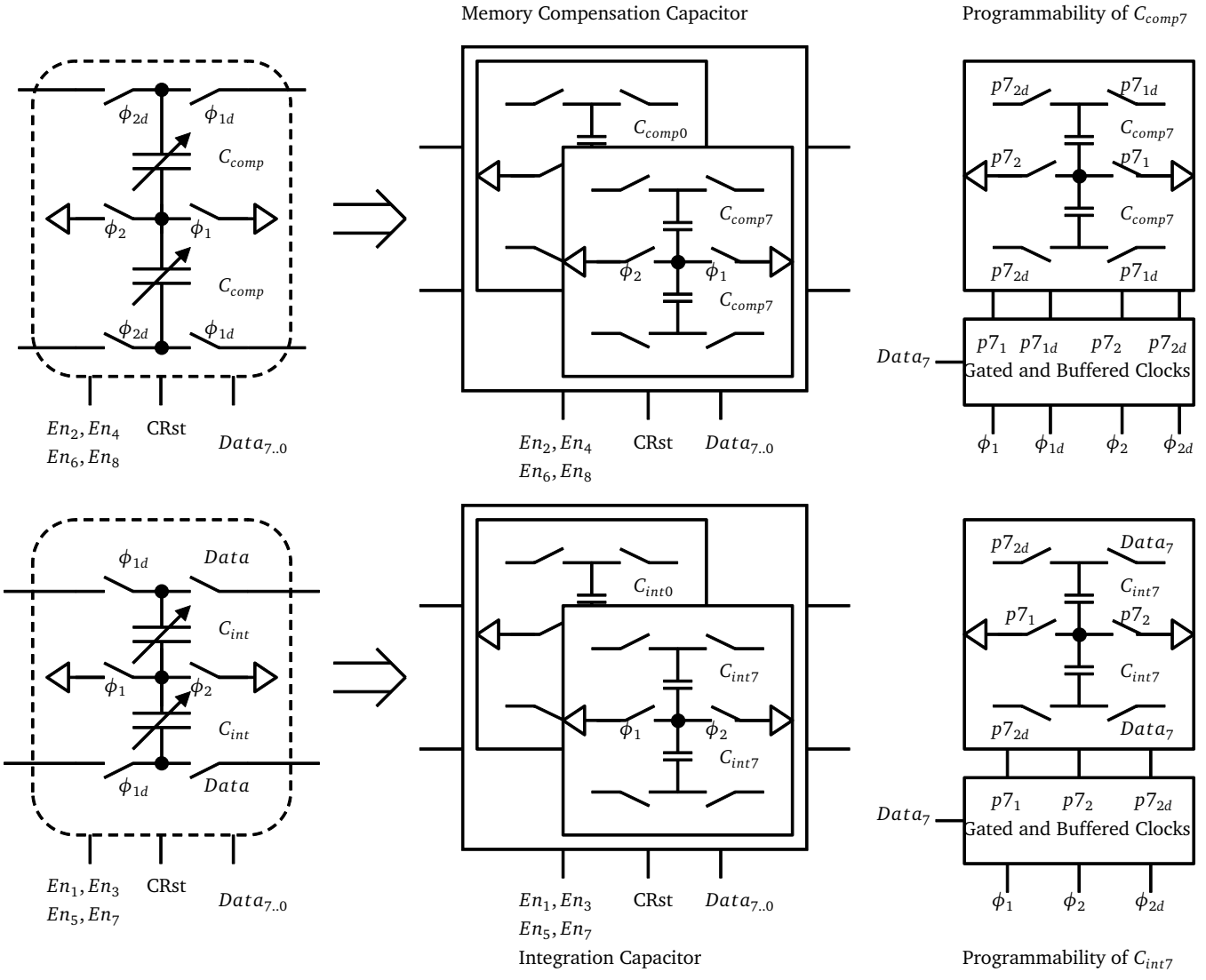


Figure 4.9: Programmable capacitor blocks.

that is four times lower than the maximum unit capacitance of 17fF for improved accuracy, we get 8 capacitances which can form the programmable capacitor C_{int} of the integrator. Although the memory compensation capacitor can be much smaller than C_{int}, it is also made up of the same 8 capacitances as C_{int} in order to simplify the design process and reuse the blocks where possible.

As illustrated in Figure 4.9, the compensation and integration capacitance of the integrator is programmed using a 8 bit digital word $Data_{7..0}$. During the calibration process, enable signals $En_1..En_8$ are used to select the respective programmable capacitor blocks in an integrator and then the 8 bit data is loaded into the capacitor array. Depending on whether the data bit is set or unset, the gated clock signals are either applied or not applied for that capacitor bit in the array. Thus the capacitor can be included or excluded during the conversion process.

The signal $CRst$ is used to drive the autozero switch which removes any charge from the programmable capacitor array during the calibration phase by providing a short between the two plates of the capacitors. The switch used to implement the autozero is sized to use the smallest possible transistors provided by the technology so as to reduce any additional parasitics coming from the switch itself. Figure 4.9 shows the example connections for bit 8 of the C_{comp} and C_{int} array. The buffers used to drive the switches in the capacitor array are kept the same for design simplicity and reducing the layout complexity. This however, as will be seen later in the results section, causes a higher digital power consumption. Scaling of the buffers according to the switch it drives should reduce substantially the digital power consumption of the modulator. The capacitor values in the programmable array are given in Table 4.7.

Table 4.7: Capacitance values in Figure 4.9

Capacitor	C_{int0}, C_{comp0}	C_{int1}, C_{comp1}	C_{int2}, C_{comp2}	C_{int3}, C_{comp3}	C_{int4}, C_{comp4}	C_{int5}, C_{comp5}	C_{int6}, C_{comp6}	C_{int7}, C_{comp7}
Value (fF)	4	8	16	32	62.5	125	250	350

All the capacitances are implemented using Metal-Oxide-Metal (MOM) capacitors. This type of capacitor was used due to the high capacitance per unit area that it offered, in addition to good matching tolerances of less than 0.1%, very small bottom plate parasitics less than 5% and very small voltage dependencies. This results in a highly linear capacitance which does not pass any additional non-linearity to the modulator. Although the smallest capacitor is 4fF, the additional parasitics coming from the layout increases its overall value.

4.3.3 Switch Sizing

Switches in the SC circuit are usually Metal-Oxide-Semiconductor (MOS) transistors operating in the triode region. The switches are designed such that they provide very high resistance during the OFF phase to prevent leakages and very low resistance during the ON phase so as to add very low distortion onto the incoming signal. The switches can be either NMOS or PMOS or a combination of both called CMOS. Due to the use of low supply voltages at 1V the use of NMOS or PMOS switch is not preferred as the overdrive voltage is already too low for these switches, thereby reducing the linear range of the switch. Therefore CMOS switches have been used for the SC implementation. The benefits are their higher linearity, cancellation of charge

injection and clock feedthrough effects while providing an almost constant ON resistance over the operating range.

Since there are parasitic capacitances associated with the source and drains of the switches, smaller transistor lengths are used to minimize these values. The switches used in the SC circuit are driven by the original clock and their delayed versions in order to prevent input dependent charge injection effects which arise from the dependence of the overdrive voltage on the gate to source voltage of the switch. This reduces the distortion effects due to the time varying input signal. The ON and OFF resistance of each switch connected to a particular capacitance is scaled according to the size of the capacitor such that the settling error produced is very small and well below 100dB for that capacitor. Care has been taken that the size of the switches are large enough to reduce the above mentioned effects but are not so high that they increase the charge injection and clock feedthrough effects.

To improve the performance of the modulator, other advanced techniques such as clock boosting and boot-strapping can be used for the first integrator. However since the CMOS switches are capable of providing the required linearity, they have not been used. Figure 4.10 shows the ON and OFF resistance variation for a CMOS switch connected to 250fF capacitance.

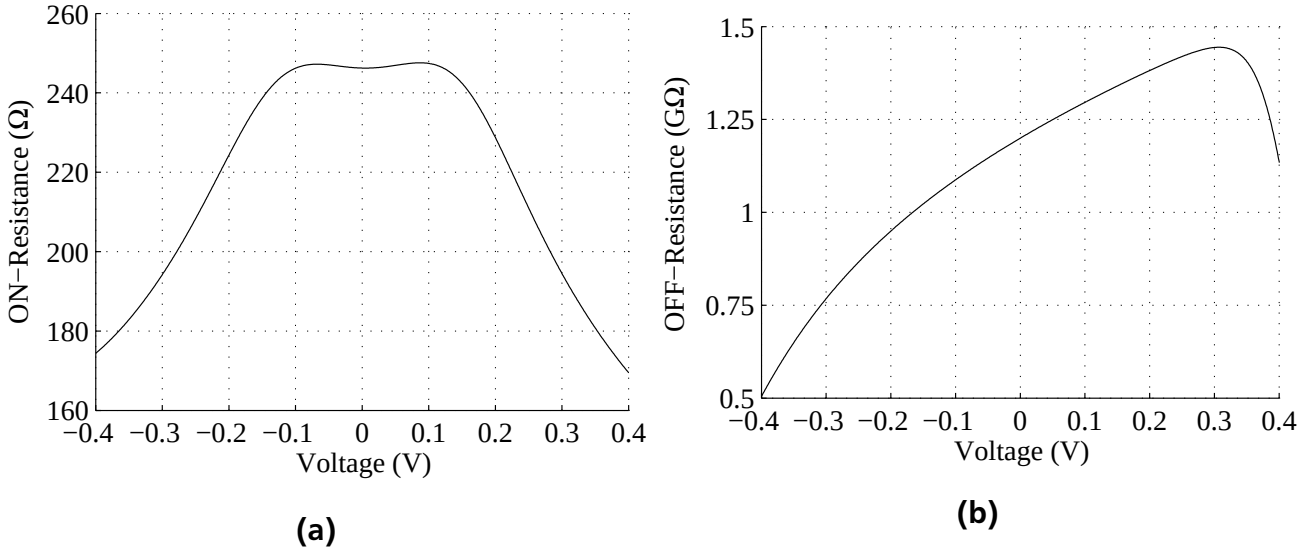


Figure 4.10: (a) ON-Resistance versus voltage level (b) OFF-Resistance versus voltage level.

Table 4.8 lists the size of the CMOS switches used in the modulator and the programmable capacitor array in relation to the capacitance value it drives.

Table 4.8: CMOS switch size versus the capacitance load

Capacitance (fF)		4,8	16	32	62.5	125	187.5	250,350	500	750	1000
PMOS	W (μm)	0.37	0.75	1.26	3	6	9	10	20	30	40
	L (nm)						80				
NMOS	W (μm)	0.12	0.24	0.44	1.2	2.4	3.5	4.1	7.8	12.4	15.6
	L (nm)						120				
ON-Resistance (kΩ)		5.8	2.8	1.8	0.8	0.41	0.27	0.25	0.125	0.08	0.06

4.3.4 CCII and Buffer Topology

Figure 4.11 shows the schematic of the class AB type CCII used in the integrator. Using class AB CCII instead of class A CCII, approximately four times the bias currents can be applied at port X without any of the transistors coming out of the saturation region. This is a useful property of class AB CCII which can be used to reduce the power consumption by using bias currents which are 1/4 of the maximum currents generated by the discharge of the capacitors C_{in}, C_{comp} at port X during the charge transfer phase.

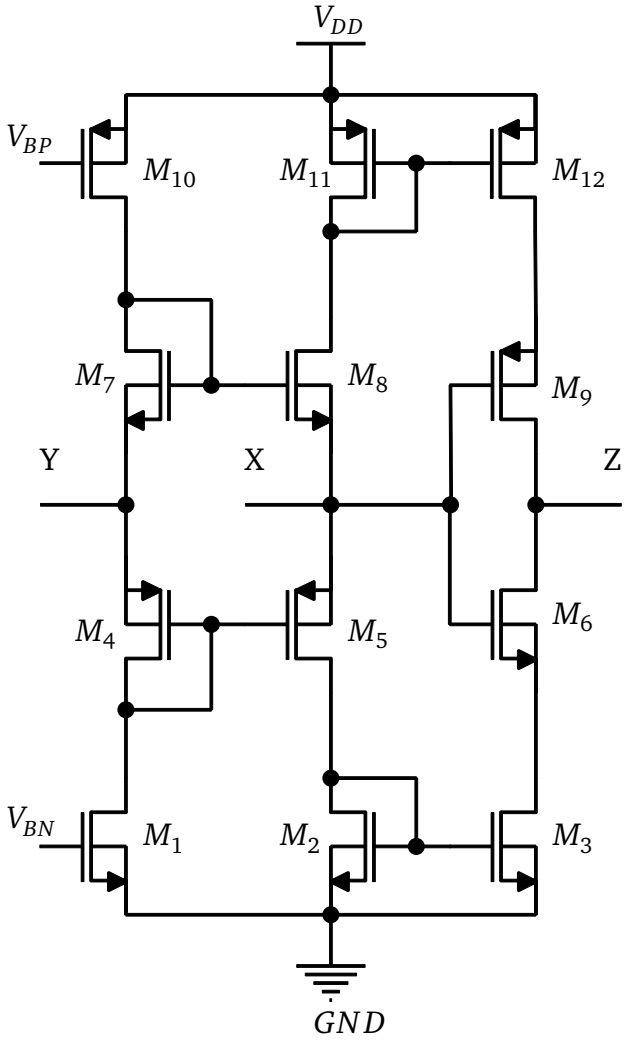


Figure 4.11: Translinear class AB CCII schematic.

The bias voltages for the CCII are generated externally off chip and can be used to control bias currents flowing through the CCII. However in this design the power consumption of the active blocks is chosen to be kept constant throughout all modes of operation in order to simplify the design. As illustrated, the CCII consists of translinear loops made from PMOS and NMOS current mirrors. Any current flowing in the port X is divided between the PMOS and NMOS paths and mirrored to the port Z where it is summed up. A mismatch between the PMOS and NMOS paths leads to offsets and non-linearities which can affect the modulator performance. The main cause of non-linearity is the variation in the port X resistance R_X due to the mismatch between the PMOS and NMOS transistor properties. To prevent this non-linearity, the port X

resistance needs to be made as small as possible, the PMOS and NMOS current mirrors need to be matched with a high degree of confidence and the transistors need to operate in strong inversion to provide good performance without any non-linearity.

In single well CMOS processes the possibility of matching the NMOS and PMOS paths is limited by the threshold voltage which can vary since the NMOS substrate is always connected to the ground, unlike the PMOS substrate where it can be connected to the source to remove threshold voltage variations due to the varying source-bulk voltages. However the chosen CMOS process UMC 90nm offers the option of using twin wells to provide an isolated substrate for the NMOS transistors too. Therefore the twin well option is used to put the NMOS transistors also in their own substrates, which can be then connected to the source of the NMOS transistors just as is done in the case of PMOS.

As mentioned in the analysis, port Z - R_Z needs to be as large as possible to reduce charge leakage and phase error of the integrator. Therefore cascoding is used at port Z to improve the R_Z value to hundreds of $k\Omega s$ range. To avoid extra bias sources for the cascode transistors M_6 and M_9, their inputs are connected to port X. This connection also serves to provide partial regulation of the current flowing through the cascode transistors with respect to the inputs applied at port X.

In order to determine the bias currents the following observation can be made for the chosen values of sampling capacitors C_{i1}, C_{i2}. Assuming a sampling frequency of 250MHz and peak sampled voltage of 0.25V around the common mode of 0.5V, it is seen that the average current produced by a capacitance of 1pF is $I = CVf = 62.5\mu A$. The previous estimation does not take into account the switch resistance and CCII parasitics, therefore for a safe margin we consider an average current that is three times, that is $200\mu A$. Since the class AB CCII can provide good linear performance upto four times its bias currents, the bias currents for the port X and port Z of the CCII are chosen to be $200/4 = 50\mu A$. The transistors are sized accordingly to satisfy this requirement of bias current $50\mu A$. To reduce the power further, port Y is biased at only half of the currents in port X and port Z, that is $25\mu A$. This is possible as port Y serves only to provide a cross coupled feedback and is not responsible for discharging the sampling capacitors.

Tables 4.9 and 4.10 show the size of various transistors used in the design of the CCII and the main properties of the CCII including the value of the its non-idealities as described in the macromodel. The CCII parameters are calculated using the method described in previous chapter.

Figure 4.12 shows the linear voltage and current range of the CCII for the nominal, best and worst case scenarios. As illustrated the CCII provides good performance over a voltage range of ±0.25V and a current range of ±0.25mA around common mode of 0.5V, assuming some non-linearity is tolerable at higher voltage and currents. For the worst corner that is the slow corner, the linear range is reduced, making the CCII produce more non-linearity if used above ±0.2mA. However overall the dynamic range is above the maximum output swings of the modulator as shown in Figure 4.4 which is ±40%.

Figure 4.13 shows the schematic of the class AB buffer which is derived by taking the Y and X ports of a translinear CCII and modifying them. The major changes are the removal of the Z port and the modification of the input port by using two level shifters to bias the output class AB stage. The removal of the Z port reduces the power, while the modification at the Y port serves to remove the parasitics R_Y by using the gate of the MOS as the input.

As discussed in the previous chapter, the buffer serves to provide a reduced output resistance so that high loads such as next stage sampling capacitors can be charged quickly. From the

Table 4.9: Transistor sizes for CCII

Transistor	Width (μm)	Length (nm)	Multiplier
M_1	4.61	200	2
M_2	4.61	200	4
M_3	4.61	200	4
M_4	5.72	200	2
M_5	5.72	200	4
M_6	4.61	200	4
M_7	4.61	200	2
M_8	4.61	200	4
M_9	5.72	200	4
M_{10}	5.72	200	2
M_{11}	5.72	200	4
M_{12}	5.72	200	4

Table 4.10: CCII Properties

Property	Value
Power (μW)	125
Supply (V)	1
Voltage Gain (β)	0.93
Current Gain (α)	0.96
3dB Voltage Bandwidth (GHz)	1.91
3dB Current Bandwidth (GHz)	0.86
Voltage Dynamic Range (V)	±0.25
Current Dynamic Range (mA)	±0.25
R_Y (kΩ) / C_Y (fF)	27 / 25
R_X (Ω) / C_X (fF)	504.2 / 99.27
R_Z (kΩ) / C_Z (fF)	360 / 26

values of the capacitors used in the modulator it is observed that the maximum capacitance load occurs at the output of the first and third integrators when used as a standalone 2nd order modulator and at the output of the second integrator when used in cascade mode. The average value of the load capacitance lies in the range of 1.5pF-2pF depending on the value of the memory compensation capacitor that is used. The fourth integrator however sees a smaller load than the other integrators due to it being the last stage of the cascade. The load seen by the fourth integrator lies in between 250fF-500fF, therefore the power required by the class AB buffer for the fourth integrator can be reduced by half in comparison to the other integrators.

Assuming a sampling frequency of 250MHz, output voltage of ±0.2V and worst case load of 3pF above the average, the value of the buffer output drive current can be determined as $I = CVf = 150\mu A$. As the previous calculation does not include the output resistance of the buffer, we take a value of 200μA for the output drive current. Based on this, transistor sizes are chosen to generate the required current flow in the output branch of the class AB buffer. The class AB buffer for the fourth integrator is sized to drive a current equal to half of this value

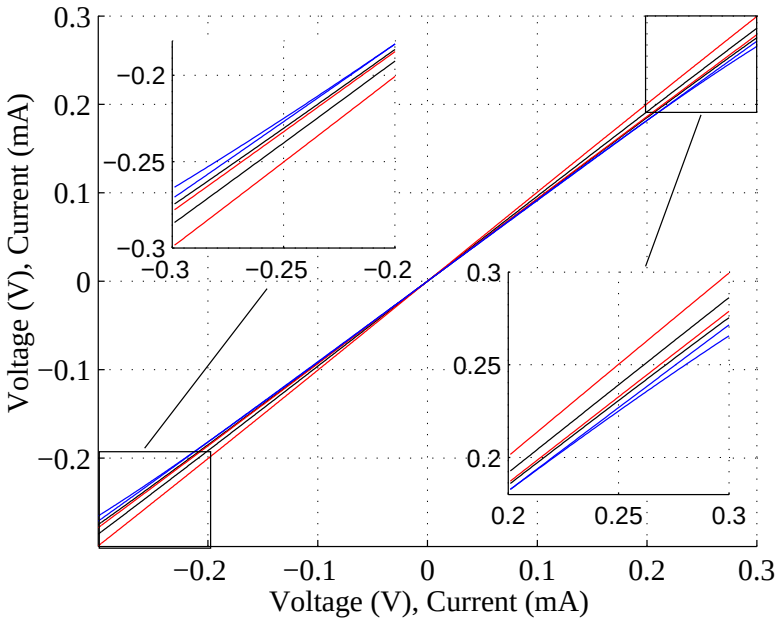


Figure 4.12: Plot of voltage relationship between Y/X and current relationship between X/Z.

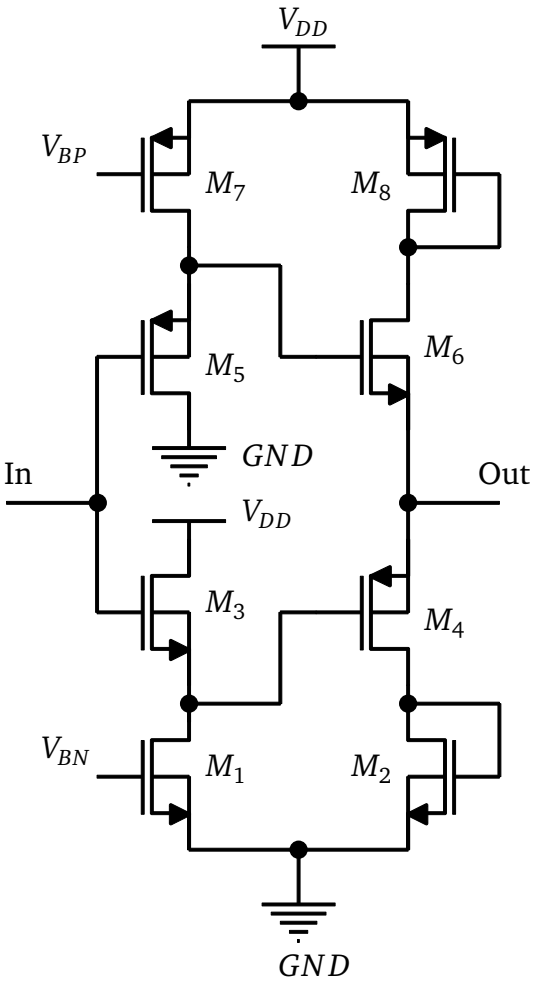


Figure 4.13: Class AB buffer schematic.

which is 100μA to reduce power. As in the case of the CCII, currents in the buffer output stage can be controlled by the bias voltage to reduce power at low sampling frequencies. However here the bias is maintained constant to keep the design simple. Tables 4.11 and 4.12 show transistor sizes and the buffer properties based on simulations with load of 3pF.

Table 4.11: Transistor sizes for buffer

Transistor Name	Width (μm)	Length (nm)	Multiplier Integrator #1/#2/#3	Multiplier Integrator #4
M_1	4.61	200	8	4
M_2	4.61	200	16	8
M_3	3.47	200	8	4
M_4	5.72	200	16	8
M_5	4.25	200	8	4
M_6	4.61	200	16	8
M_7	5.72	200	8	4
M_8	5.72	200	16	8

Table 4.12: Buffer Properties

Property	Integrator #1/#2/#3 $@C_{Load} = 3pF$	Integrator #4 $@C_{Load} = 1.5pF$
Power (μW)	400	200
Supply (V)	1	1
Voltage Gain (β)	0.903	0.903
3dB Voltage Bandwidth (MHz)	420	420
Voltage Dynamic Range (V)	±0.25	±0.25
C_{buf} (fF)	94	47
R_{out} (Ω)	126	252

4.3.5 Clock Generator

Figure 4.14 shows the schematic of the two phase non-overlapping and delayed clock generator. The integration and sampling phases are controlled by the output of the clock generator. The input clock is provided externally off chip and thus can be varied to generated the different sampling frequencies required by the modulator.

The delay inverters used to adjust the non-overlapping period between the two phases ϕ_1 and ϕ_2. Since the delay of the inverter can be controlled also by changing the supply voltage, these delay inverters are provided a supply voltage that is separate from the digital supply provided to other digital circuits. By adjusting the supply voltage externally, the non-overlapping periods can be adjusted by ±20% around the mean value. The nominal non-overlap time is set to 300ps between the two phases to ensure that charge transfer phase and sampling phase do not overlap.

The clock generator is replicated twice to adjust the sampling frequency of each 2nd order modulator independent of the other. Thus it is possible to use the 2-2 cascade modulator simul-

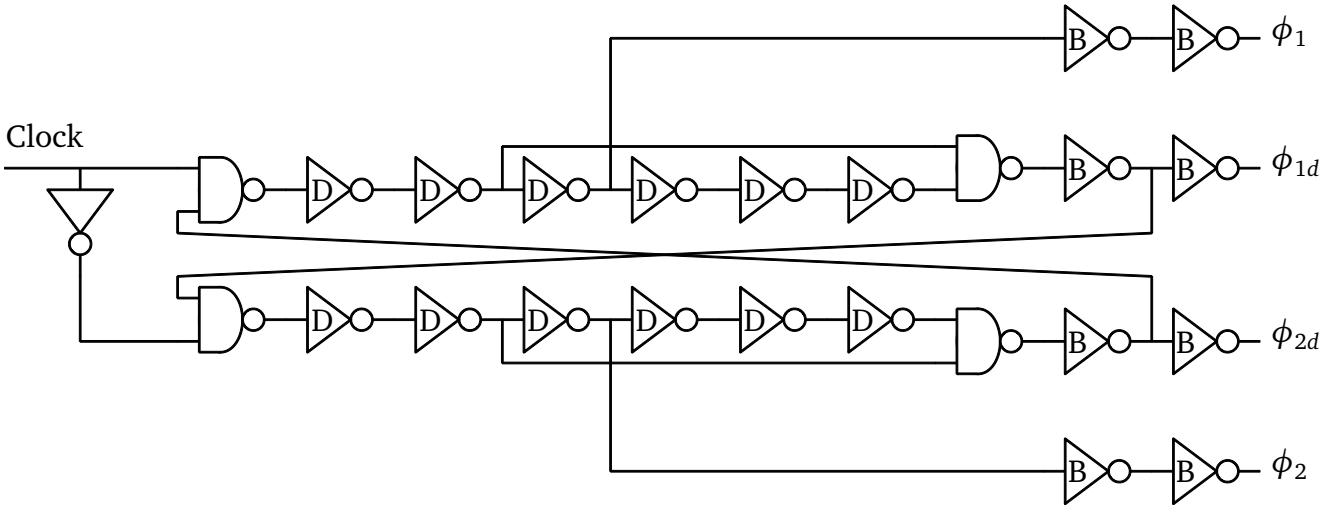


Figure 4.14: Clock generation circuit (D=Delay Inverter, B=Buffer Inverter).

taneously to convert two input signals of different bandwidths at different sampling frequencies. A drawback however is that the digital power consumption increases, since twice the required number of digital phase buffers are used.

4.3.6 Implementation of Analog Adders

An important feature of the modulator is the passive implementation of the analog adders before the 1.5bit ADC [59]. Using passive techniques, the use of an active block to sum the signals can be avoided thus saving power in the low voltage regimes. Figure 4.15 shows the analog adder implementation as well as its configuration during the sampling phase using capacitors C_{i3}, C_{a1}, C_{a2} for the first 2nd order modulator. As illustrated in the figure, the passive analog adder comes with certain constraints. The first constraint is the lack of virtual ground which results in greater influence of the parasitics and the input capacitive load of quantizer C_L. The second constraint is that the passive analog adder acts as a capacitive divider, which results in the input signal being scaled to a smaller value before it appears at the input of the 1.5 bit ADC. This results in the reduction of the full scale at the quantizer input which must be compensated for by scaling the quantizer references over a similar range as well.

Considering the circuit in the sampling phase we see that the effective input voltage at the input of the quantizer is given by:

$$v_o = \frac{C_{i3}\,v_{in}}{C_{i3}+C_{a1}+C_{a2}+C_L} + \frac{C_{a1}\,v_{int1}}{C_{i3}+C_{a1}+C_{a2}+C_L} + \frac{C_{a2}\,v_{int2}}{C_{i3}+C_{a1}+C_{a2}+C_L} \tag{4.15}$$

where C_L is the total parasitics coming from the quantizer input and other sources such as the switches and layout and v_{int1}, v_{int2} are the first and second integrator outputs.

As can be seen from the previous equation the input signal is being scaled by a factor:

$$\lambda = \frac{C_{i3}}{C_{i3}+C_{a1}+C_{a2}+C_L} \tag{4.16}$$

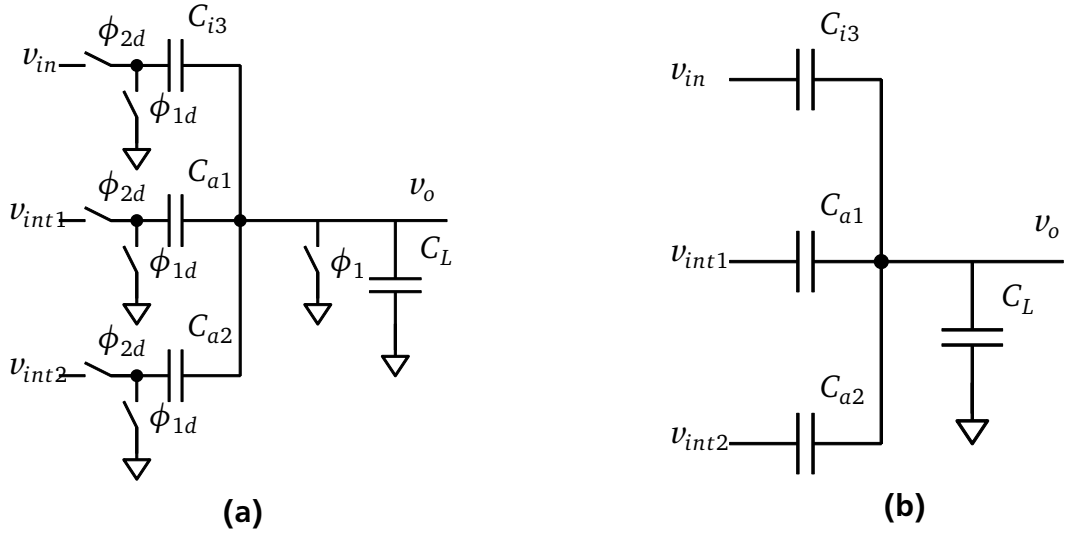


Figure 4.15: Passive analog adder (a) SC implementation (b) Connections during sampling phase.

Substituting the feedforward coefficients $a_1 = C_{a1}/C_{i3}$ and $a_2 = C_{a2}/C_{i3}$ in the previous equation we get the scaling factor as:

$$\lambda = \frac{C_{i3}}{13C_{i3} + C_L} \tag{4.17}$$

The upper limit on the scaling factor is obtained by neglecting C_L in relation to $13C_{i3}$, which results in a value of $\lambda = 0.0769$. However since the size of C_{i3} in relation to C_L is only marginally high, C_L cannot be neglected and must be included to obtain a more accurate estimate of the scaling factor. The size of C_L is determined by switch parasitics, layout parasitics and gate capacitance of the 1.5 bit quantizer. The 1.5 bit quantizer uses two comparators, therefore a first order approximation of the quantizer input capacitance C_q can be estimated from the simulations. This value is found to be equal to C_q =26fF for one comparator. Taking twice this value as the total quantizer input capacitance and recalculating the scaling factor gives a value of $\lambda = 0.0722$.

It needs to be mentioned that apart from the quantizer input capacitance there are additional capacitances which further lower the scaling factor, such as the switch drain and source parasitics, top plate parasitics of the capacitors C_{i3}, C_{a1}, C_{a2} and the parasitics of the metal layers used for routing in the analog adder. It is seen from the post layout extractions that the effective scaling factor comes down to a value in the range of 0.065. In order to compensate for the scaling of the input signal, the quantizer references also need to be scaled by the same factor λ so that the quantizer can produce correct outputs. The scaling of references can be implemented on chip using a resistive divider or provided externally off chip as is done in this design.

One disadvantage of the passive analog adder is that the comparator used in the quantizer must have very low offsets. Since the inputs and references are scaled to low values in the millivolts range, the comparator in the quantizer must provide an offset which is far lower than this value. Otherwise the quantizer will produce erroneous outputs for inputs that lie in the millivolts range. In order to reduce the input offset a preamplifier is used before the comparator, which amplifies the passive analog adder output to a range above its offset voltage. This prevents false toggles at the quantizer outputs by providing sufficient signal to offset margin for the quantizer. The maximum value of the comparator offset in a 1.5 bit quantizer for this

design is given as $\lambda * Vref/K \approx 20mV$, where K=3 is the number of levels in the quantizer and $Vref$ is taken to be 1Vpp.

The previous discussion holds true for the first stage 2nd order modulator operating alone. However if we consider the 4th order 2-2 cascade operation then for the second stage analog adder we observe that the presence of the interstage scaling factor $d = 4$ which is implemented with the help of additional capacitors C_{i7} and C_{i8} causes a change in the scaling factor λ. Ideally speaking it is necessary to use a different scaled quantizer reference for the second stage analog adder to account for the new λ. However in this design we use the same quantizer reference scaling for the 2-2 cascade due to the fact that the second stage 2nd order modulator errors are attenuated by the first stage which is more accurate. Hence the error increases due to the use of same same quantizer reference scaling for the second stage analog adder is negligible.

4.3.7 A/D/A Conversion

As illustrated in the modulator schematic, 1.5 bit ADC and DAC are employed for the purpose of generating the modulator outputs and providing in-loop feedback in the modulator. Figure 4.16 shows the implementation of the 1.5 bit ADC to digitize the analog adder outputs of the first stage 2nd order modulator. Although the connections are shown for first stage, the second stage uses a similar quantizer structure. It is made from two low offset comparators that generate the three bit outputs $Y_1[2:0]$ and $Y_2[2:0]$. The two comparators compare the differential output from the analog adders v_{o1} and v_{o2} with the scaled quantizer references $+v_{qr}$ and $-v_{qr}$. The topology of the comparators is described in the next section, where it is seen that the comparator is made from the differential preamplifier and a dynamic clocked latch to generate full scale outputs.

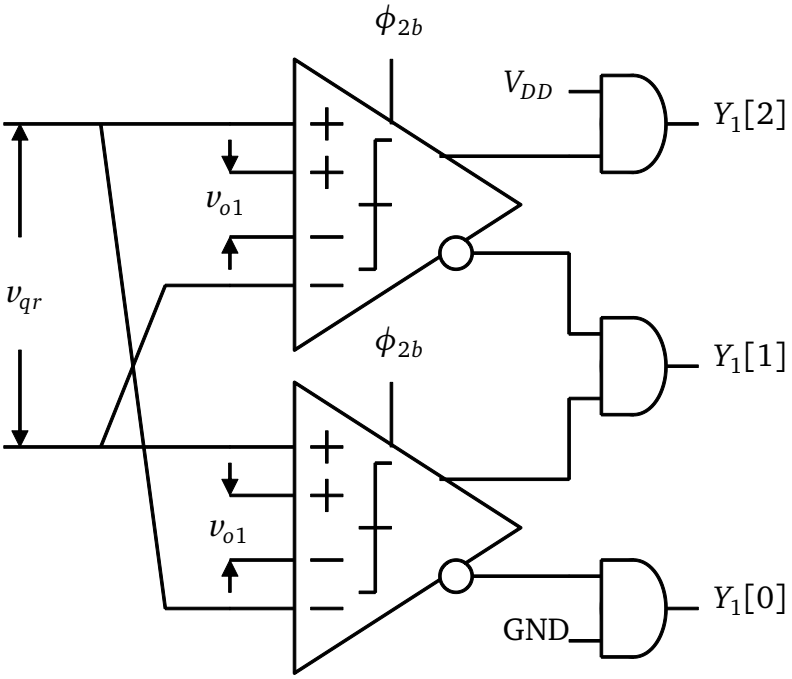


Figure 4.16: 1.5 bit ADC implementation schematic for the first stage second order modulator.

Figure 4.17 shows the implementation of the 3 level DAC used for the in-loop feedback in the first stage 2nd order modulator. The schematic is similar for the second stage 2nd order modu-

lator. The DAC works by presampling the reference voltages onto capacitors C_{i1}, C_{i4} during the sampling phase ϕ_2 and depending on which of the ADC outputs are enabled, the corresponding reference voltage $+V_{ref}$ (0.5V) or $-V_{ref}$ (-0.5V) is applied to the CCII during the charge transfer phase.

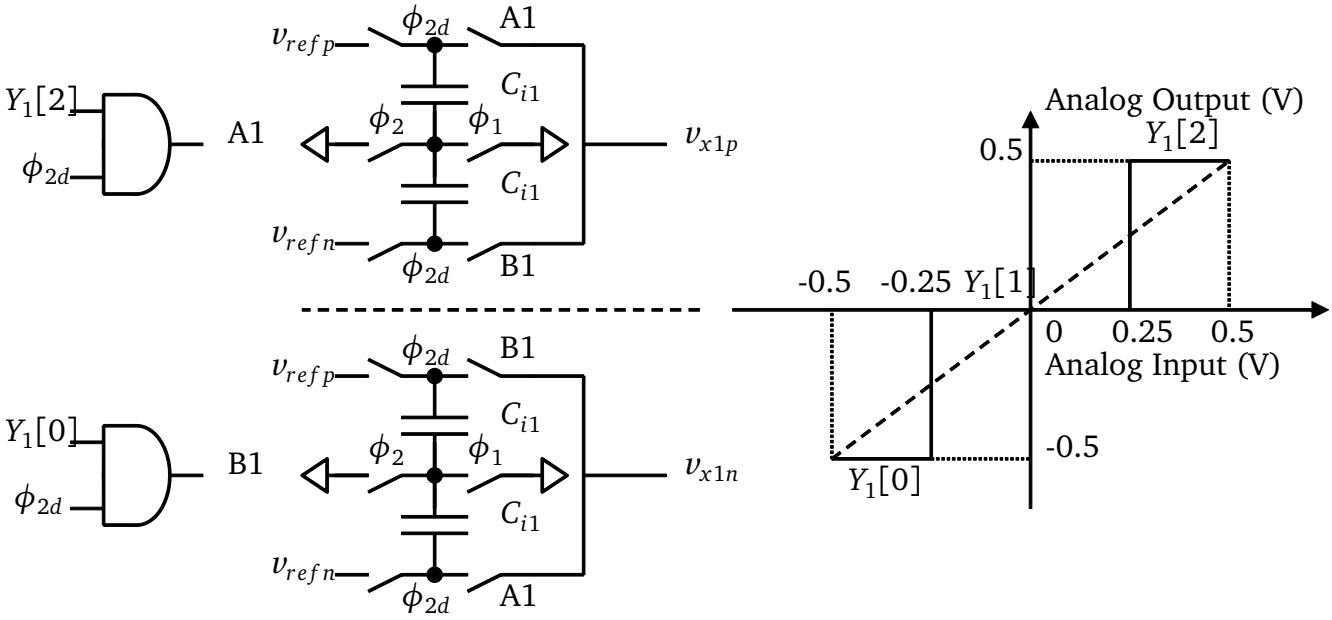


Figure 4.17: 1.5 bit DAC implementation schematic for the first stage second order modulator.

4.3.8 Calibration Comparator and Quantizer Comparator Design

Two types of comparators are used in the modulator. One comparator called the calibration comparator is used for the calibration phase to accurately set the integrator input output relationship and therefore requires ultra low offsets in the range of few tens of μV. The second comparator called the quantizing comparator is used by the 1.5 bit ADC to quantize the analog adder outputs and produce the outputs $Y_1[2:0]$, $Y_2[2:0]$.

The general architecture of these two comparators consists of a preamplifying stage followed by a dynamically clocked regenerative latch and a set-reset latch to maintain the output from the clocked latch constant for one clock cycle. Figures 4.18 through 4.23 show the schematic and architecture of the calibration comparator, quantizing comparator, preamplifiers, dynamic clocked latch and set-reset latch.

Table 4.13 shows the size of the various transistors used in the design of the comparator blocks. The value of the resistor Res is chosen as 25kΩ to obtain the necessary gain required for the low offset comparator.

The goal of the preamplifiers used in the calibration comparator is to reduce the offset of the overall comparator to a small value. The highest resolution provided by the modulator is for the GSM standard, where it gives a resolution of 12 bits at 40MHz sampling frequency. The lowest resolution is provided for the DVB-H standard, where it gives 9 bits. Assuming a 1 volt conversion range for the modulator, we get 1 LSB as 240μV for the GSM standard and 1.9mV for the DVB-H standard.

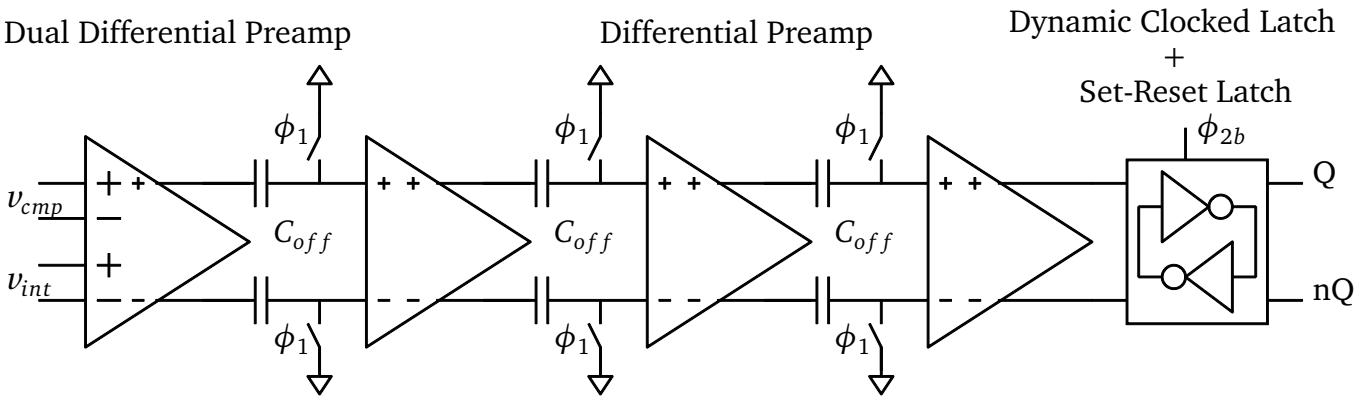


Figure 4.18: Calibration comparator schematic including the dynamic clocked latch and set-reset latch.

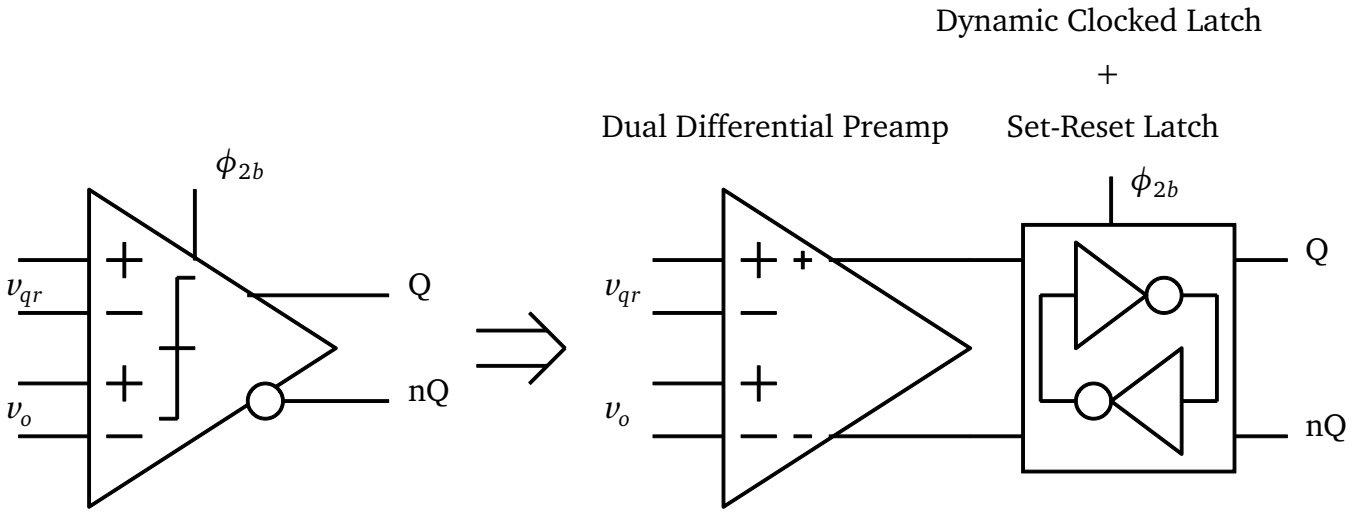


Figure 4.19: Quantizing comparator schematic including the dynamic clocked latch and set-reset latch.

In the order to set the integrator input and output response accurately to a value well below 1 LSB, the calibration comparator needs to have an offset that is much smaller than the 1 LSB resolution of the GSM and DVB-H standard at the sampling frequency of 40MHz of 120MHz respectively. In order to derive such low offsets, the calibration comparator uses four preamplifying stages before the dynamic clocked latch. The first preamplifier uses dual differential inputs to compare the output of the integrator with the calibration reference outputs and it provides gain of 15 dB at low frequencies which decreases to 11dB at high frequencies of 200MHz. The second, third and fourth preamplifiers use differential inputs and provide a gain of 20dB at low frequencies which decreases to 16 dB at high frequencies of 200MHz. Based on these gains it is observed that the total gain provided for the GSM standard is 75dB and the DVB-H standard is 67dB. Assuming that the dynamic clocked latch has an offset in the range of ±10mV, it is seen that the four preamplifying stages can theoretically amplify signals as small as few μV at low frequencies and few hundred μV at high frequencies to above ±10mV offset seen by the dynamic clocked latch.

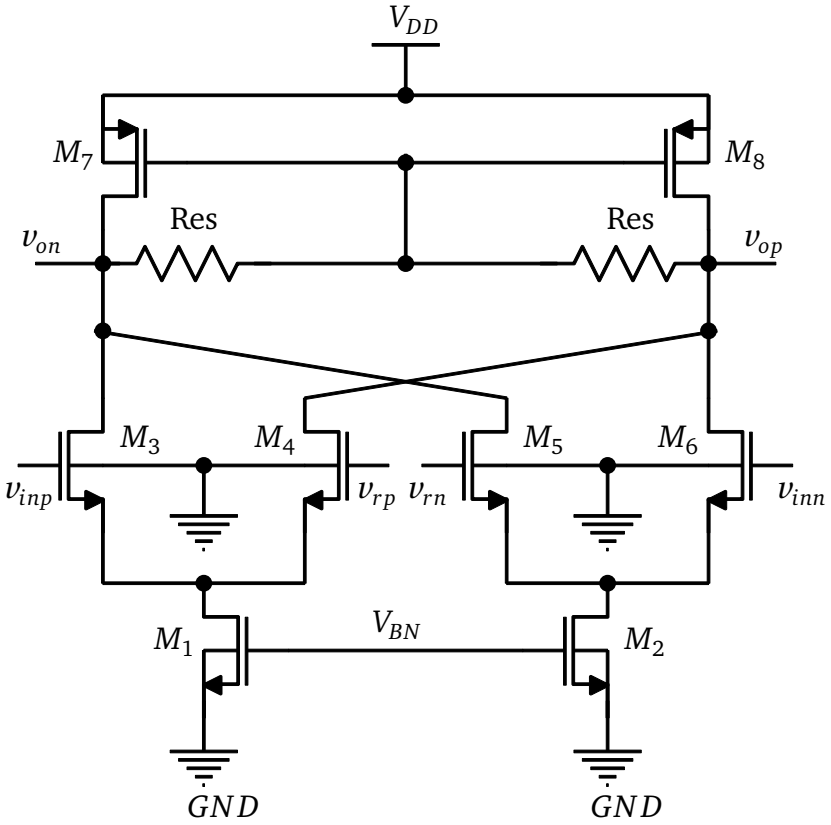


Figure 4.20: Dual differential preamplifier schematic which provides a low frequency gain of 15dB and high frequency gain of 11dB.

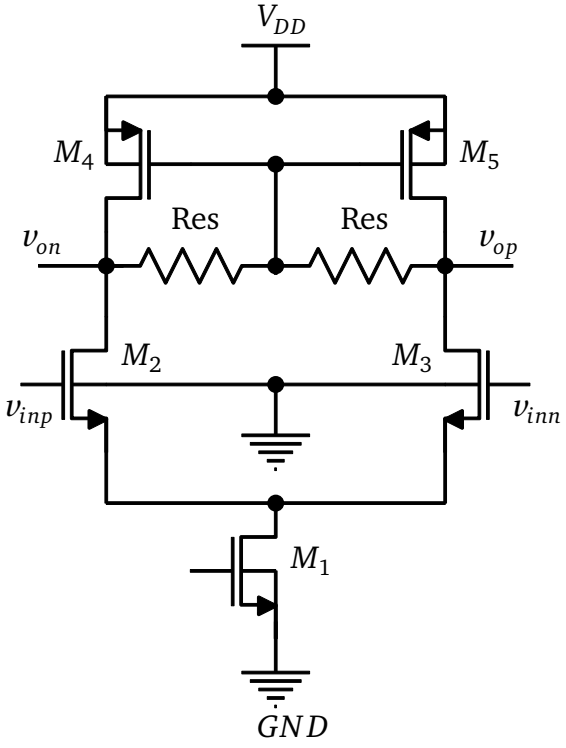


Figure 4.21: Differential preamplifier schematic which provides a low frequency gain of 20dB and high frequency gain of 16dB.

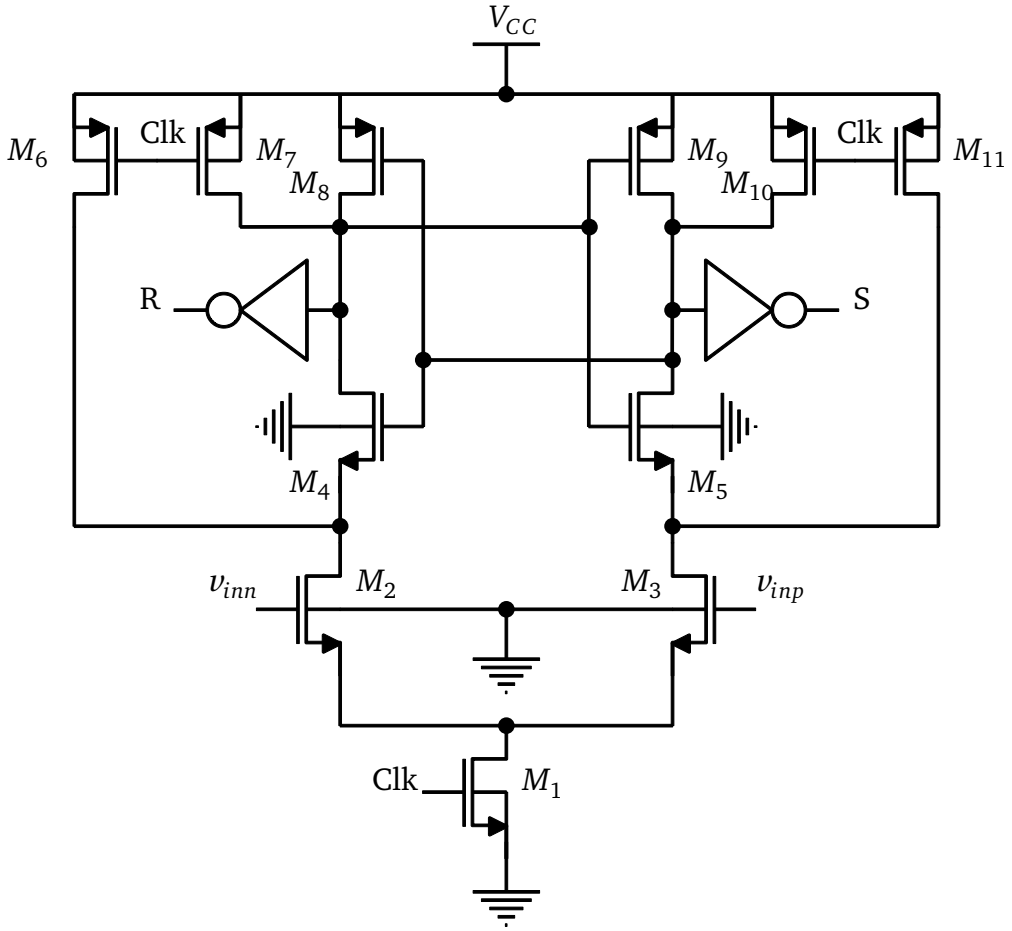


Figure 4.22: Dynamic clocked comparator schematic.

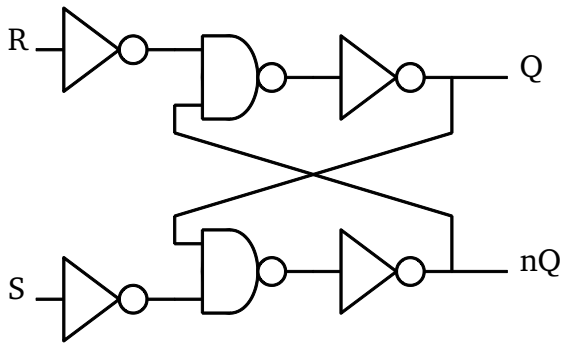


Figure 4.23: Set-Reset latch using NAND and inverters.

Although the offset of the dynamic clocked latch is reduced using preamplifiers, there exists an additional source of offset coming from the mismatch in the preamplifier itself. Hence in addition to canceling the dynamic latch offset, output offset cancellation techniques are employed to remove the preamplifier offsets. This is implemented by sampling the output referred offset of each preamplifier onto the interstage offset storage capacitor, which is then connected in series with the incoming signal to nullify the preamplifier offset.

Similar to the calibration comparator, the quantizing comparator also needs to have small offsets. However the offset requirements on the quantizing comparator are more relaxed. As discussed in the implementation of the analog adders, the offset of the quantizer needs to be

Table 4.13: Transistor sizes for the preamplifiers

Transistor Name	Dual Differential Preamplifer Width (μm)	Length (nm)	M	Differential Preamplifer Width (μm)	Length (nm)	M	Dynamic Clocked Latch Width (μm)	Length (nm)	M
M_1	4.61	200	8	4.61	200	16	5	80	16
M_2	4.61	200	8	5.925	200	8	5	80	8
M_3	5.925	200	4	5.925	200	8	5	80	8
M_4	5.925	200	4	2.88	400	8	4.45	80	2
M_5	5.925	200	4	2.88	400	8	4.45	80	2
M_6	5.925	200	4	-	-	-	5	80	2
M_7	2.88	400	8	-	-	-	5	80	2
M_8	2.88	400	8	-	-	-	3	80	4
M_9	-	-	-	-	-	-	3	80	4
M_{10}	-	-	-	-	-	-	5	80	2
M_{11}	-	-	-	-	-	-	5	80	2

smaller than 10mV in order for it to be used in a 1.5 bit ADC. This requirement is achieved by using just one preamplifying stage consisting of dual differential inputs, which provides gain of 15 dB at low frequencies and a gain of 11dB at high frequencies of 200MHz. Using this preamplifier input signals as 2mV at low frequencies and 3mV at high frequencies can be brought above the ±10mV offset.

The architecture of the dynamic clocked latch is shown in Figure 4.22. The dynamic latch can operate at very high clock frequencies and provide very low offsets in the range of ±10mV. The input differential pair in the latch serves to amplify the incoming signals. Depending on the inputs, one of the transistors in differential pair conducts lower current than the other. The back to back inverter pair senses this imbalance in the differential pair and provides positive reinforcement to the flow of the currents in the differential pair using the cross coupled feedback path. This positive reinforcement pulls one side of the differential amplifier to the ground while the other side reaches full scale. A set of PMOS and NMOS switches serve to strobe the differential inputs according to the positive edge of the incoming clock.

The set-reset latch is made from a combination of inverters and NAND gates, as simulations showed the NAND gate to perform faster producing smaller delays compared to the set-reset latch with NOR gates. The calibration comparator on the whole consumes 800μW of static power during the calibration phase and can be switched off when not in use. However in the present design due to the lack of IO pins, a power down switch was not included. Each of the quantizing comparators in the 1.5 bit ADC consumes about 200μW of static power.

4.3.9 Simulation Results

Circuit simulations are performed on the complete modulator to characterize its performance and check for problems related to timings, parasitics and other process related effects. Full post layout simulation for the entire modulator consumes a lot of time and memory due to the presence of many transistors and capacitors. Therefore only a limited number of full post layout simulations are carried out. To reduce simulation times and still provide good accuracy,

CADENCE AMS simulator is used to combine post layout analog blocks and schematic based digital blocks for simulation. Furthermore a rough estimation of parasitic capacitances that arise from metal routing and other sources in the layout are included in the CADENCE AMS simulator to make the simulation results correspond better with full post layout simulations.

The calibration algorithm is implemented as a Verilog model and interfaced with the chip during the calibration process. It controls the selection of integrators, programming of capacitors, synchronizing the application of the calibration reference inputs and processing the output of the calibration comparator to further adjust the programmable capacitors when necessary. The complete modulator is operated at a 1 V supply voltage and simulated at various sampling frequencies for different mobile standards.

The outputs of the modulator when operating as a standalone 2nd order modulator and when operating in cascade mode are saved and further processed by MATLAB. To estimate the power spectral density, a minimum of 4096 FFT points are taken and windowed using Hann window to minimize noise leakage and estimate the SNDR and DR performance of the modulator. The simulations are repeated for various input signal amplitudes between 0 and 1V around the common mode voltage of 500mV and different signal bandwidths to characterize the modulator.

Table 4.14 shows the complete modulator performance under nominal conditions and Figures 4.24 through 4.26 show the PSD and the DR of the modulator for all mobile standards. It is observed that with calibration the noise leakages and harmonics are suppressed, allowing the full performance of the integrator to be realized. As illustrated, the modulator provides excellent performance, giving a peak SNDR of 80.4/76.5/66/73/67 dB and a total DR of 92/86/78/81/76 dB for the GSM, BT, GPS, UMTS and DVB-H respectively. It is observed from the DR plot that the peak SNDR occurs at the -12dBFS input rather than at a higher input amplitude. This is direct consequence of using the CCII at the extreme end of its linear voltage and current range as shown in Figure 4.12 which introduces more distortion and noise leakage.

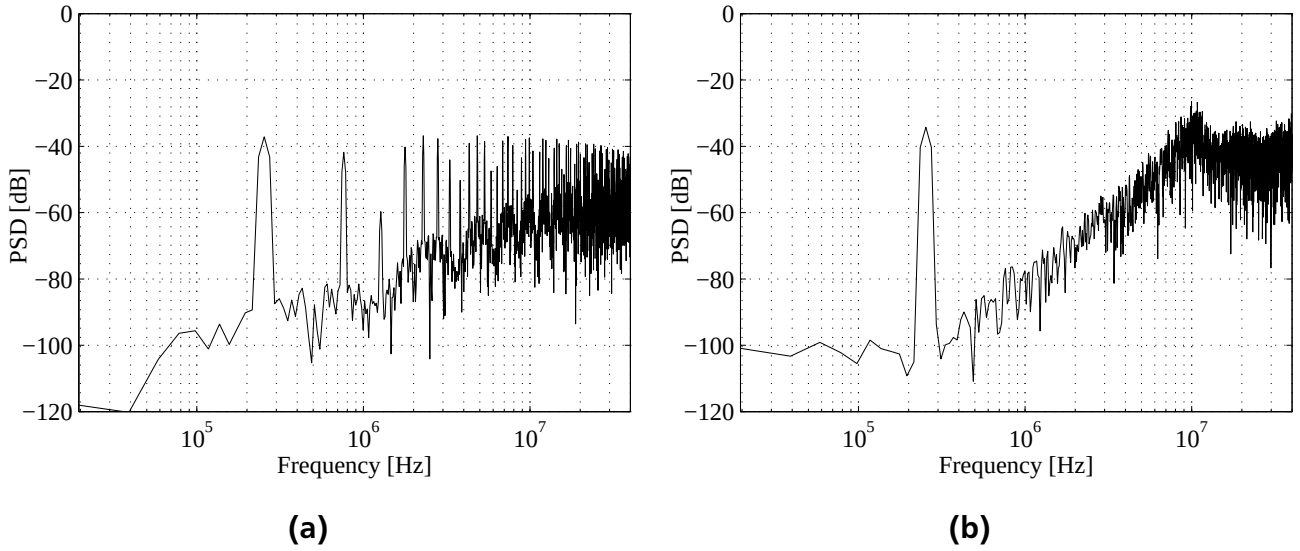


Figure 4.24: PSD plot of modulator output taken at sampling frequency of 80MHz (a) before calibration. (b) after calibration.

Figure 4.27 shows the power distribution of the modulator for various mobile standards after calibration has been performed and values of the C_{int}/C_{comp} capacitors have been set. Unlike other DT modulators present in literature which use adjustable bias voltages for analog blocks

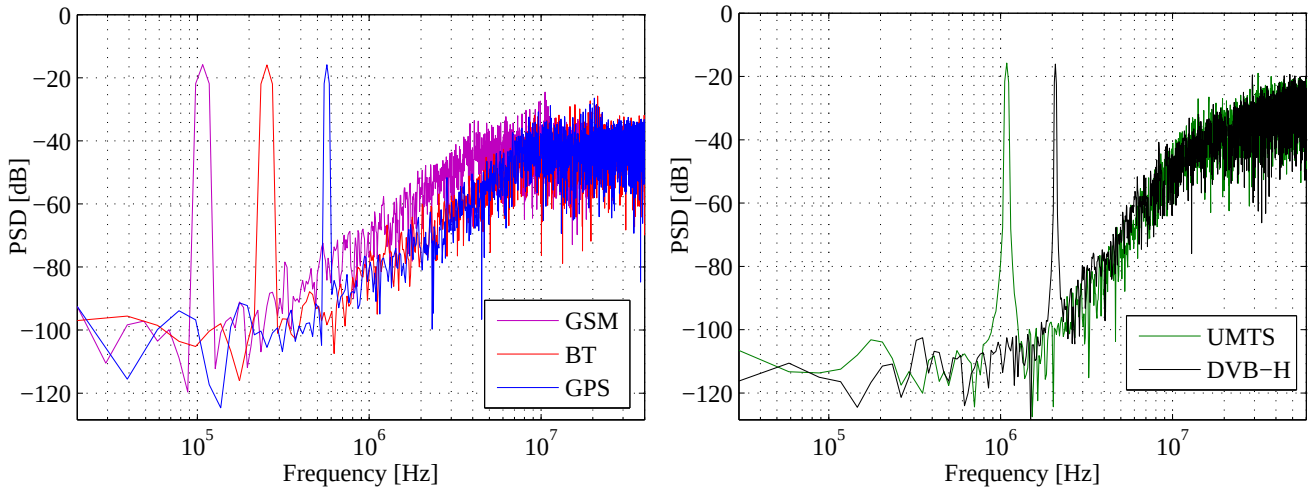


Figure 4.25: Simulated output spectra for all standards.

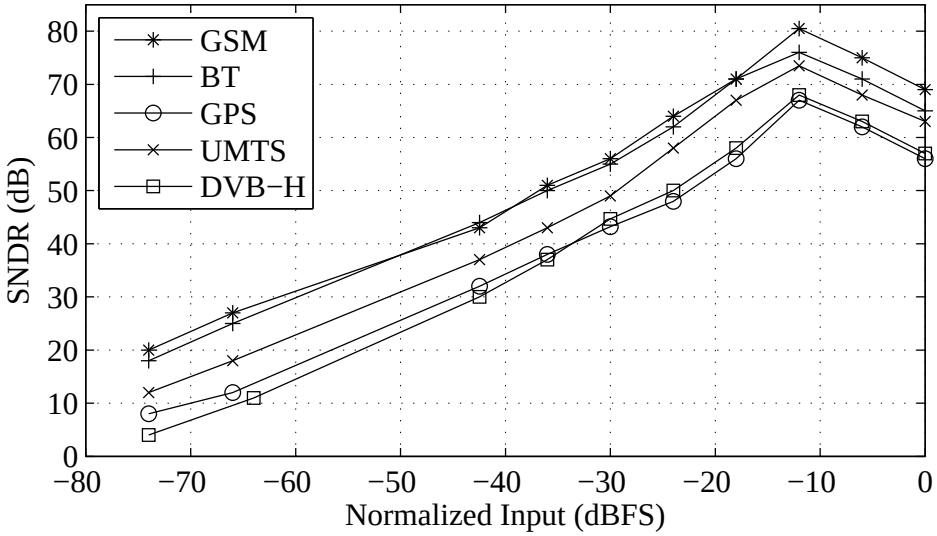


Figure 4.26: Simulated dynamic range for all standards.

Table 4.14: Modulator simulated performance summary

Property	GSM	BT	GPS	UMTS	DVB-H
Tech (nm) / Supply (V)			90 / 1		
Order	2	2	2	4	4
Sampling Rate (MS/s)	40	80	80	120	120
Signal Bandwidth f_b (MHz)	0.2	0.5	1	2	4
OSR	100	80	40	30	15
Power (mW)	4.4	6.98	6.98	17.1	17.1
SNDR (dB)	80.4	76.5	66	73	67
DR (dB)	92	86	78	81	76

to optimize power consumption, the bias voltages for the analog blocks in this design are maintained constant for all standards. This is done due to limited availability of IO pins. The digital power on the other hand is dependent on the sampling frequency. As sampling frequencies increase with higher signal bandwidths, the digital power consumption also increases.

It is observed that for the GSM standard which operates at 40MHz clock, the analog section consumes about 50% of the total power. For the rest of the standards which use a clock of 80MHz and 120MHz, the percentage of analog power goes down in comparison with the digital power. It is seen that for UMTS/DVB-H standards which operate at 120MHz clock and use the entire 2-2 cascade during conversion, the analog section consumes only about 25% of the total power, with the rest being consumed by the digital logic.

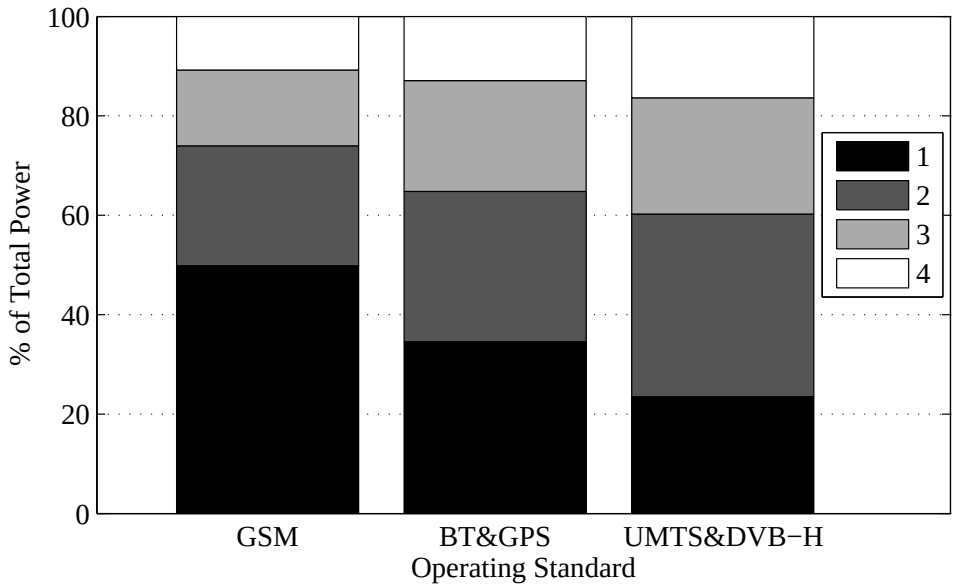


Figure 4.27: Power distribution in the modulator for different standards. (1) Analog section (2) Clock generator and buffer (3) Gated clock buffers for programmable C_{int}/C_{comp} (4) Rest of digital section.

The higher digital power consumption comes mainly from two blocks.

- Clock generator and driver: High strength digital clock buffers are used to drive the non-overlapping phases from the clock generator to the entire circuit. Due to reasons explained in the next paragraph, the clock buffers are overdesigned such that they can operate at clock frequencies above a few hundred MHz.
- Programmable C_{int}/C_{comp}: As illustrated in Figure 4.9, each unit capacitor in the programmable C_{int}/C_{comp} array has switches of varying sizes, which are driven by gated clock buffers. If a unit capacitor is enabled, the gated clock buffers transmit the clock phases to the switch in order to turn them on and off. The gated clock buffers used to drive the switches connected to each unit capacitor in the programmable capacitor array C_{int}/C_{comp} have the same buffer strength. This means that the power consumed by gated digital buffers connected to the smallest unit capacitor is the same as that consumed by gated digital buffers connected to the largest unit capacitor. Since many unit capacitors are enabled post calibration, many gated digital buffers are used, thereby increasing digital power consumption.

The reasons for the overdesign of the digital part which results in higher power consumption are explained as follows.

- Europractice offered only two additional opportunities for fabricating the chip in UMC 90nm/1V technology before it would be removed from their low cost multi project wafer mini@sic runs. The performance of the chip depends on the precision with which the clock phases arrive at various locations throughout the circuit. Errors in the clock arrival at different points in the chip lead to increased noise leakage and performance loss in the modulator. Due to limited number of attempts to redesign the chip in the event of such an error post fabrication, the decision was made to overdesign the digital part so that the clock phases arrive correctly as required.
- For the full custom design of the modulator, digital components such as inverters, buffers, digital gates and flip flops of varying properties and drive strengths were needed. However Europractice did not offer the schematic and layout views for the digital standard cells required to create a full custom ASIC. The main scope of the thesis was to prove the concept of wideband fully differential CCII integrator applied to the design of $\Delta\Sigma$ modulator and not to create a full fledged standard cell library. Therefore only a standard cell library consisting of limited number of digital cells with different properties and drive strengths was created from scratch. These digital cells were then used to drive switches in the programmable C_{int}/C_{comp} array. The digital buffers used to drive the switches in C_{int}/C_{comp} array were also overdesigned to make sure the clock arrives at the correct time as required by the chip.

From the previous discussion it becomes clear that the increase in power consumption is mainly due to the use of unoptimized digital blocks. It is observed from preliminary investigations that power savings of atleast 30-40% from the digital logic is possible by scaling and optimizing the digital buffers.

4.4 Summary

In this section modulator implementation details were presented. Various circuits used to design the integrator were explained in detail along with the transistor sizes. Discrete time 2nd order and 4th order $\Delta\Sigma$ modulators are realized using SC circuits based on the CCIIs proposed in the previous chapter. The performance of 2nd order and 4th order modulators were verified through simulations. The 4th order modulator is chosen for fabrication in UMC 90n technology, results of which are presented in the next chapter. The simulations show that the power consumption of the overall modulator is higher than expected, due to the overdesign of the digital blocks. However the FOM values in the next chapter reveal that the modulator performs excellently despite the higher digital power consumption when compared to state of the art reconfigurable discrete time $\Delta\Sigma$ modulators.

5 Experimental Prototyping and Test Results

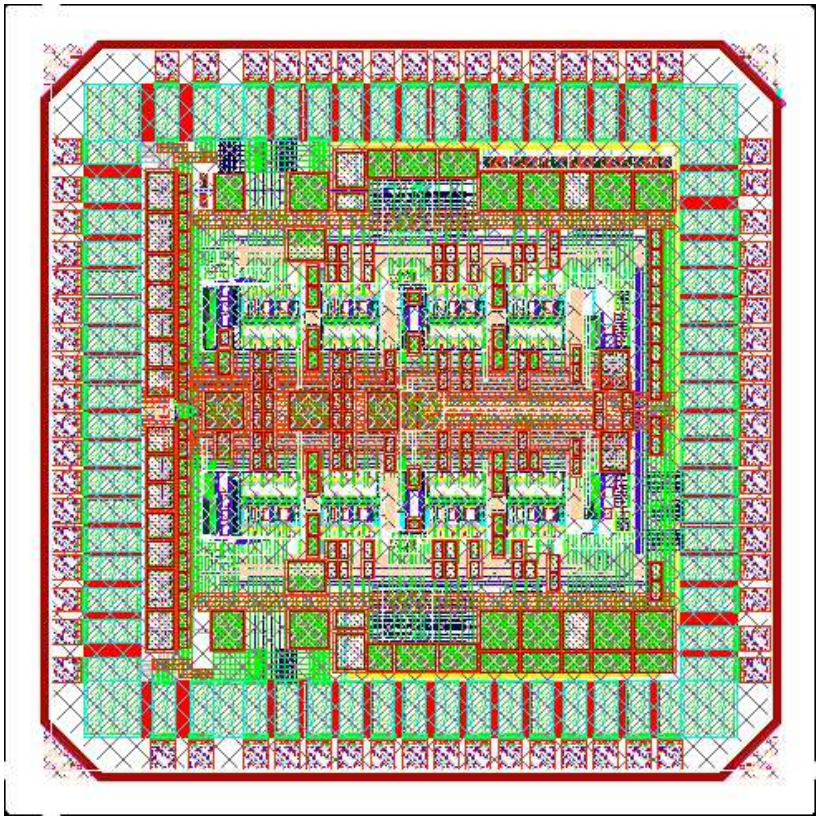
Contents

The 4th order modulator described in the previous chapter has been implemented in the UMC 90nm/1V technology and fabricated through the mini@sic runs offered by Europractice. This chapter describes the chip layout, floorplan, pin-description, the Printed-Circuit-Boards (PCBs) and the test setup used to characterize the performance of the fabricated chip. Finally the chapter also discusses the performance of the chip by comparing its FOM with other state of the art DT modulators.

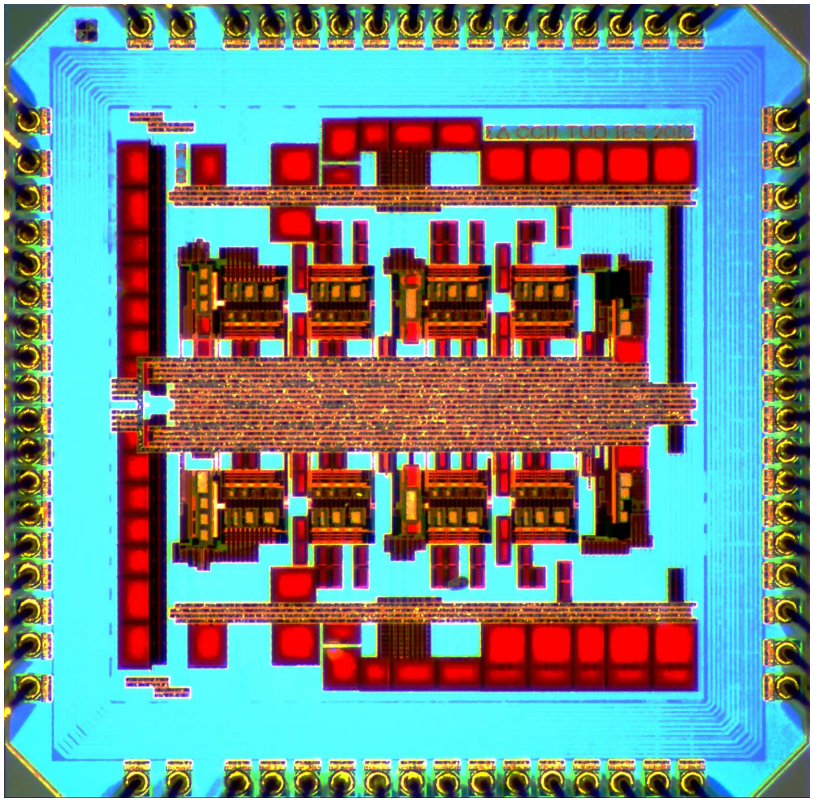
5.1 Chip Floorplan and Layout

The modulator has been designed and implemented in a UMC 90nm/1V technology. Figure 5.1 shows the complete chip layout as well as the chip microphotograph. The modulator occupies a total die area of approximately 1400x1400 μm^2 excluding IO pads. This area includes the main active die area itself, as well as additional components such as decoupling capacitors, IO routing and identification markers. The layout extensively follows translation of the schematic to layout design methodology, where the input signals come from the left and the modulator output is taken at the right. The layout applies tried and tested techniques laid down in literature for getting matched components. Common centroid and interdigitization techniques are extensively used to match similar components on the two single ended paths of the modulators. Thus each of the components in the single ended paths such as CCII, buffer, integration capacitor, sampling capacitor, compensation capacitors etc. is combined with its fully differential counterpart and laid together as if it is a single component. This allows tight matching of the two single ended paths to be achieved and also reduce effects such as gradient related mismatches. Dummy elements are used to improve matching where necessary.

All the capacitors in the modulator are constructed using MOMCAPS for better linearity, lower area and matching. Separate power supply lanes are created for routing analog and digital power supplies so as to minimize switching noise in the analog components. All the digital signals including the clocks are routed using a U shaped bus from the right side and all the analog signals including references are routed using a T shaped bus from the left side. Each digital and analog signal is further isolated from other neighbouring signals using grounded metal shields which surround the signal completely on all sides. Although this increases the capacitances, it



(a)



(b)

Figure 5.1: Chip implementation (a) Layout. (b) Die microphotograph.

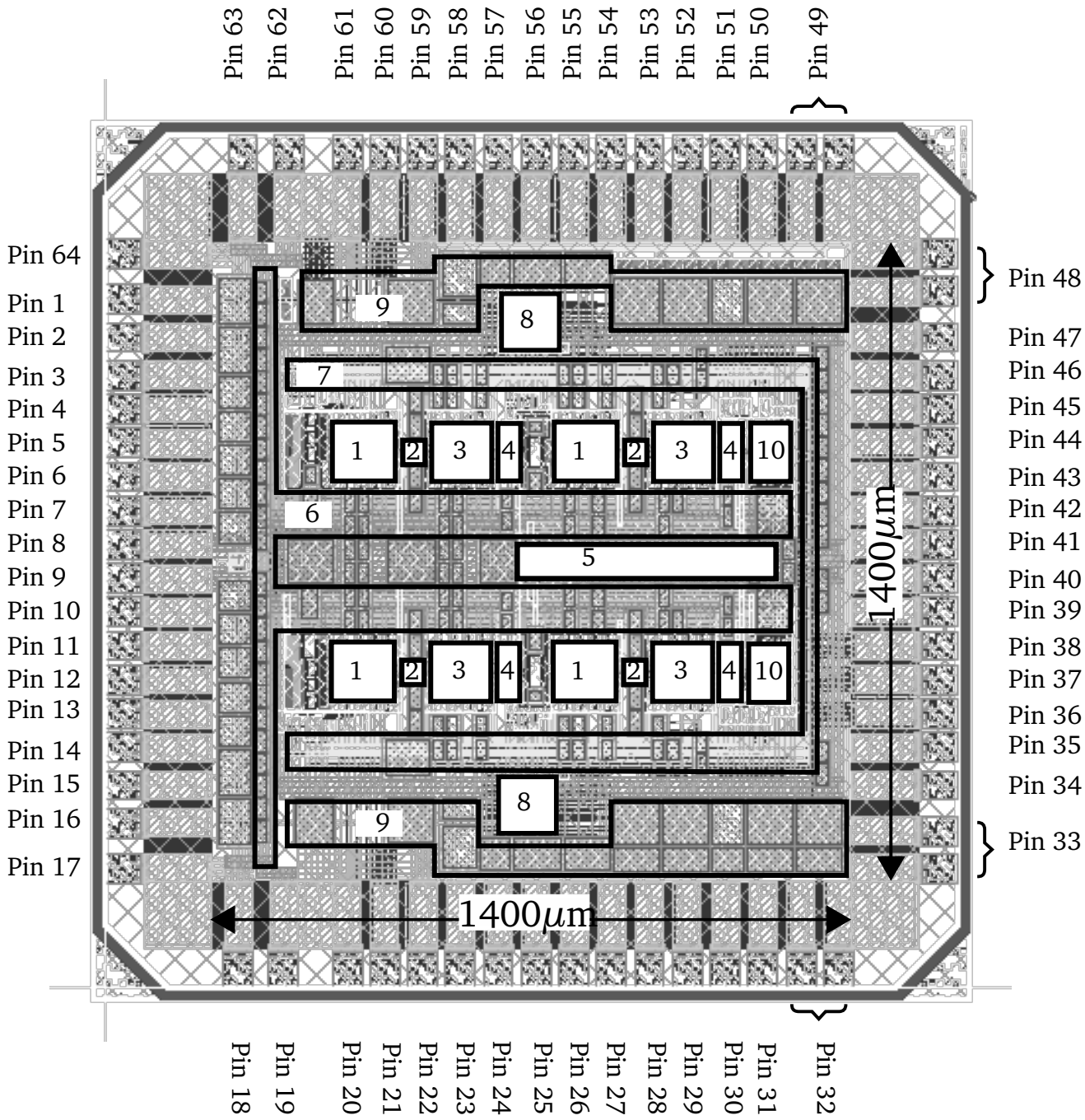


Figure 5.2: Chip floorplan. 1 - C_{comp}, 2 - CCII, 3 - C_{int}, 4 - Buffer, 5 - Calibration comparator, 6 - Analog signal bus, 7 - Digital signal bus, 8 - Clock generator and driver, 9 - Decoupling capacitors, 10 - Quantizer and analog adder

significantly reduces signal corruption due to crosstalk. Shielding is also applied to the blocks, CCII and buffer where a grounded metal covers the analog components so that any neighboring signals do not couple onto the active components. The IO pads are split to isolate the digital power supplies from the analog power supplies. Due to the references and calibration signals being generated externally, a quad-flat-no-lead(QFN64,8x8) package is used to accommodate the

large number of pins coming from the chip. Figure 5.2 shows the detailed floorplan identifying the locations of various components and Table 5.1 gives the pin descriptions.

Table 5.1: Pin Description

Pin	Label	Signal Type	Description
1,2,15,16	Vinp,Vinn	I	Differential input signal
3,4	TH_Vbiasp,TH_Vbiasn	I	Buffer bias
5,6	Vcomprefp, Vcomprefn	I	Differential quantizing comparator reference
7	VDD_Delay	I	Clock delay inverter supply
8,9	Vcm	I	Common mode voltage
10	Comp_Vbiasn	I	Comparator bias
11,12	INT_Vbiasn,INT_Vbiasp	I	Integrator bias
13,14	Vrefn,Vrefp	I	Differential DAC reference
17,64	Analog_Shield	I	Analog bus shield voltage
18,62	AGND	I	Analog ground
19,63	VDD	I	Analog supply
20,22,36, 38,59,61	DGND	I	Digital ground
21,37,60	VCC	I	Digital supply
23,26,27,28, 53,54,55,58	Data[7:0]	I	Digital code for programmable components
25,43,57	Clk	I	Clock
24	Cascade_EN	I	Cascade mode enable
29,30,31	Y_2[2:0]	O	Second modulator outputs
32,49	DGNDIO	I	Digital ground for IO drivers
33,48	DVCCIO	I	Digital supply for IO drivers
34,35	Stg_Sel[2:0]	I	Stage select pin to select first or second stage for calibration
39,40	Vcompref_Sel[1:0]	I	Calibration comparator reference select for comparison
41,42	Calib_Compp,Calib_Compn	O	Calibration comparator outputs
44,45	Vintout_Sel[1:0]	I	Calibration comparator integrator select for comparison
46,47	Cap_Sel[1:0]	I	Programmable capacitor select pin to program capacitor data
56	Cap_Rst	I	Programmable capacitor autozero signal
50,51,52	Y_1[2:0]	O	First modulator outputs

5.2 PCB Design and Test Equipment Setup

To test and characterize the chip, a set of PCBs (Mainboard, Power Supply Unit (PSU) Board, Reference Board) was developed. Figures 5.3 and 5.4 show the PCB schematic and photo of the test setup used to characterize the chip. The main features of the PCBs and test setup are summarized as follows:

- The complete test setup consists of the Mainboard interfaced with a Xilinx Virtex-5 FPGA which communicates with a computer using a serial interface. The PSU and Reference PCBs are pluggable modules designed to connect to the Mainboard. The calibration algorithm to calibrate the chip on the Mainboard, the I2C control interface for configuring the Reference PCB and the PSU PCB as well as the UART interface to communicate with the computer are implemented using Verilog on the Virtex-5 FPGA. The UART interface allows serial commands to be sent from the computer to the FPGA which performs tasks such as performing proper powerup sequence for the chip, programming references and supply voltage levels to correct value, performing calibration on the chip, reading calibration/modulator data from the chip and debugging the entire system if necessary.

- The input signal to the chip is generated from a single ended external source and fed to the fully differential low distortion ADC driver (ADA4927-1) from Analog Devices on the Mainboard PCB using SMA connectors. The differential output of the ADC driver is filtered by a programmable second order RC filter network before being sent into the main chip which is housed in a QFN64 socket for easy access. The supply voltage for the ADC driver is generated on the Mainboard using linear regulators (TPS7A3001DGN and TPS7A4901DGN). The programmable second order low pass RC filter network allows different values of cutoff for input bandwidth to be selected depending on the operation of the modulator. The Mainboard is a 4 layer board which has separate regions for routing digital and analog signals so that they do not overlap.

- There are two PSU boards responsible for generating the 1V analog and digital supplies needed by the chip. All voltages going into the PSU board are filtered to remove any noise from the power lines. The PSUs have onboard programmability to adjust their output voltage between 0.5V-1.5V using a programmable linear regulator (LT3085EMS) from Linear Technologies. Additionally a current measurement capability is added to measure the supply currents consumed by the analog and digital circuits in the ASIC using a Texas instruments current measurement IC (INA219). The programmability of the PSU board is implemented through an I2C interface which is connected to the Virtex-5 FPGA. Large decoupling capacitors are employed very close to the chip to provide stable supply voltages with minimum rippling.

- The bias voltages and references needed for the active blocks in the chip are generated using the References PCB. This PCB consists of many 16 bit monotonic programmable DACs (AD5669/AD5696) from Analog Devices which generate the required voltages with high precision and low noise. An onboard buffer additionally serves to drive DAC outputs to decoupling capacitors on the Mainboard. The DACs outputs are programmed using an I2C interface which is controlled by the Virtex-5 FPGA.

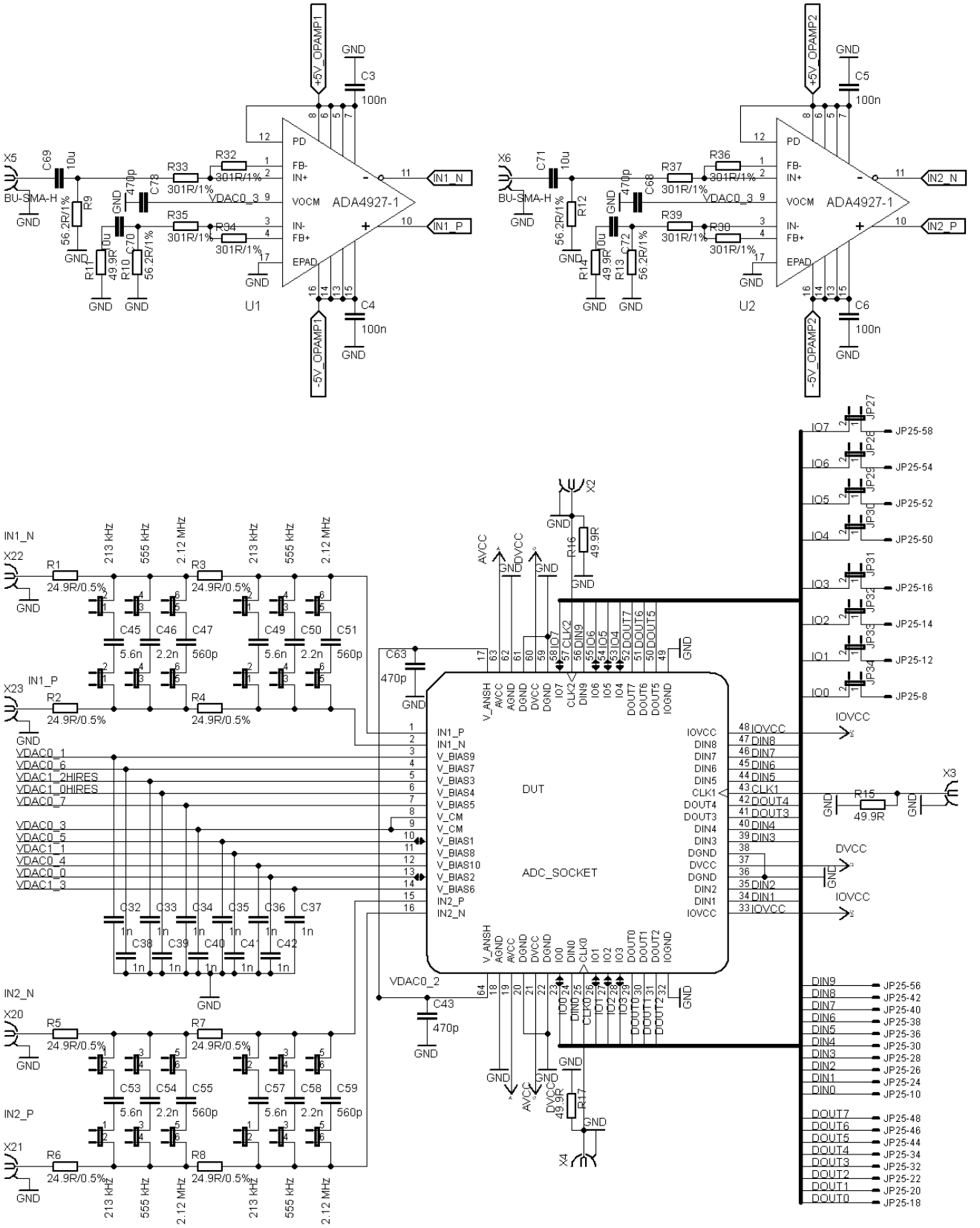


Figure 5.3: Mainboard PCB schematic.

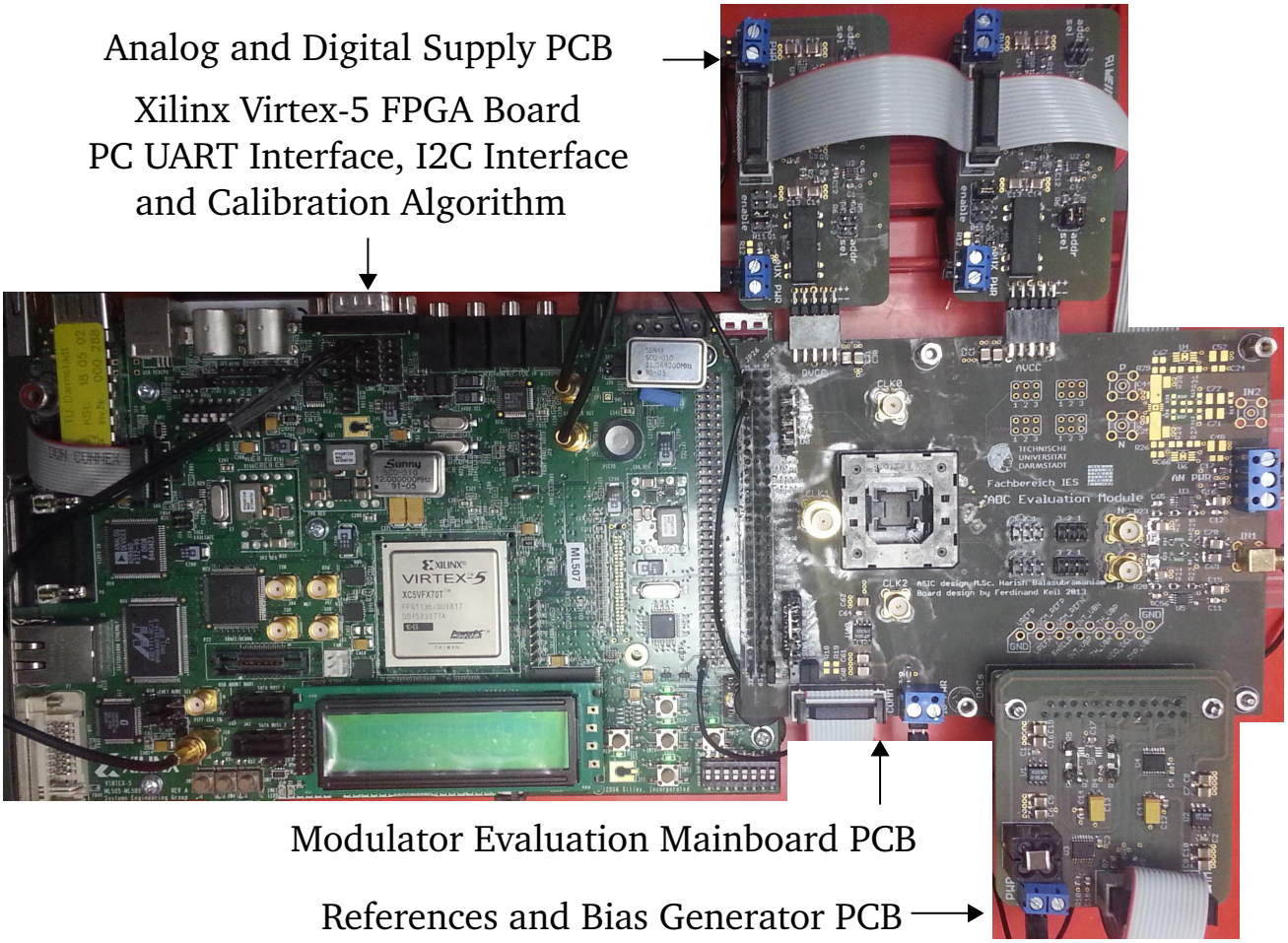


Figure 5.4: Complete test setup.

- The various clock frequencies for the modulator are generated using a clock generator present onboard the Xilinx Virtex-5 FPGA board and fed using shielded SMA connectors. Additionally the PCB traces for the clocks on the Mainboard are shielded from other analog/digital signal lines to prevent any switching noise and crosstalk effects.

5.3 Experimental Results

The performance of the chip is evaluated using the test setup described previously. Inputs signals using the same frequencies as in the previous chapter are applied for evaluating the SNDR and DR performance of the modulator. Different clock frequencies used in simulations are generated using the programmable clock generator onboard the Virtex-5 evaluation board. The outputs from the modulator are captured by the FPGA and later transferred to the computer for generating PSD plots using Matlab. To compute the PSD of the modulators, their outputs are windowed using a Hann window. Figure 5.5 shows the measured output spectra corresponding to the GSM, BT, GPS, UMTS and DVB-H standards considering an input sine wave with an amplitude of -18dBFS.

Figure 5.6 shows the DR of the modulator plotting the SNDR for various input signal amplitudes. Measuring the supply currents, it is observed that the chip is operating in the slow-typical

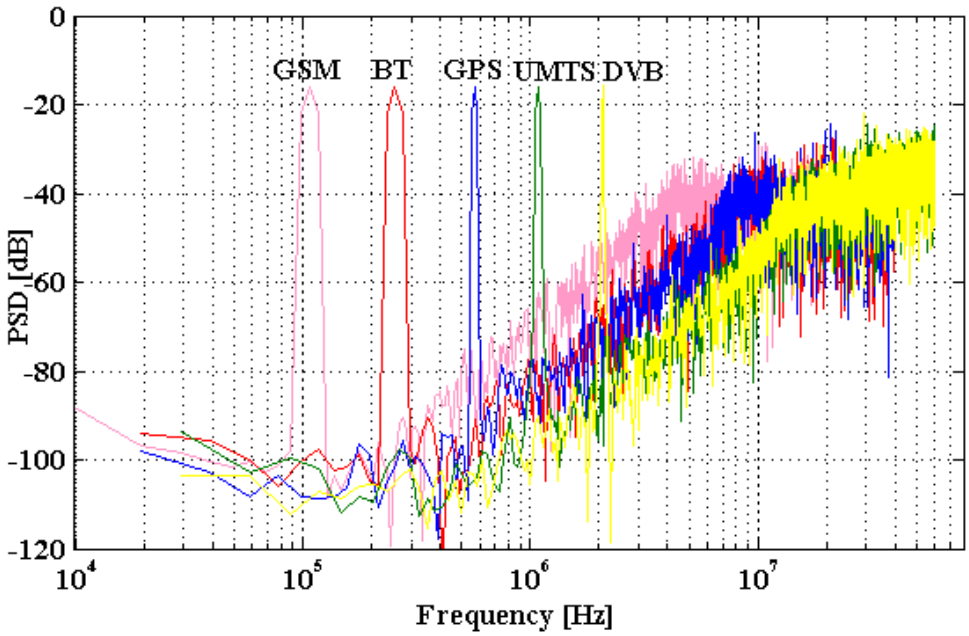


Figure 5.5: Measured output spectra for GSM, BT, GPS, UMTS, DVB-H modes

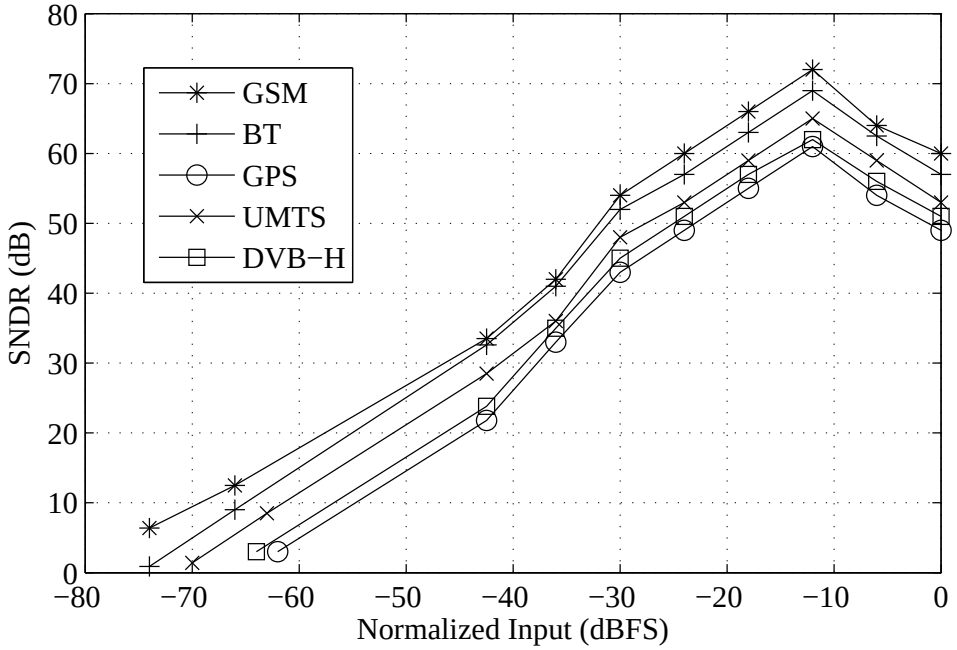


Figure 5.6: Measured dynamic range for GSM, BT, GPS, UMTS, DVB-H modes

corner due to which there is a loss in the linear operating range of the CCIIs and buffers. Additionally it was explained in the previous chapter that CCII and the buffers were shown to have increased non-linearities when used near the maximum of its input/output voltage and current range. Hence between the simulations and measurements the DR degrades by 10dB due to these two effects. The results can be improved further by using regulated stages for the CCII X and Z ports as well as designing a more linear class AB buffer. The complete performance results are summarized as before in Table 5.2 for the different operating modes.

Table 5.2: Modulator measured performance summary

Property	GSM	BT	GPS	UMTS	DVB-H
Tech (nm) / Supply (V) / Total Area (mm^2)			90/1/1.96		
Order	2	2	2	4	4
Sampling Rate (MS/s)	40	80	80	120	120
Signal Bandwidth f_b (MHz)	0.2	0.5	1	2	4
OSR	100	80	40	30	15
Power (mW)	4.85	7.3	7.3	17.8	17.8
SNDR (dB)	72	69	61	65	62
DR (dB)	80	75	64	71	66
FOM_1	1.48	1.58	2.7	1.53	1.36
FOM_2	1.28M	1.06M	0.625M	0.85M	0.89M

Table 5.3: Comparison with other modulators

	Standard	Tech (nm)/ Supply (V)	Clock (MHz)	f_b (MHz)	Power (mW)	DR (dB)	FOM_1
[60]	GSM	90/1.2	50	0.1	3.4	84.8	1.2
2-1 Cascade	BT		90	0.5	3.7	77	0.64
	UMTS		80	2	6.8	66.2	1
[61]	GSM	90/1.2	40	0.1	4.6	78.2	3.5
2-2 Cascade	BT		80	0.5	5.35	69.7	2.1
	GPS		120	1	6.2	71.6	1
	UMTS		120	2	8	66.2	1.2
	DVB-H		120	4	8	62.5	0.9
This work	GSM	90/1	40	0.2	4.85	80	1.48
2-2 Cascade	BT		80	0.5	7.3	75	1.58
	GPS		80	1	7.3	64	2.7
	UMTS		120	2	17.8	71	1.53
	DVB-H		120	4	17.8	66	1.36

While a strict one to one comparison cannot be made due to use of different architectures, signal bandwidths and sampling frequencies, nonetheless Table 5.3 shows the comparison of the presented modulator with two other reconfigurable DT $\Delta\Sigma$ modulators designed in 90nm technology. As shown in the table, the modulator achieves good performance for GSM and BT modes while providing acceptable performance in other operating modes. The presented modulator provides good performance for upto 200kHz GSM bandwidth in comparison to 100kHz GSM bandwidth provided by the other two modulators.

The achieved FOMs show that the presented modulator can indeed compete with other state of art implementations surveyed in Chapter 2. The active die area of the modulator is larger compared to the 2-2 cascade in [61]. The reasons for this are many fold such as the use of unoptimized high strength buffers resulting in larger layout for digital cells, use of memory compensation capacitor which has the same size as the integration capacitor and replicating the layout of 2nd order modulator twice to create the 2-2 cascade without employing any opti-

mization to reduce overall layout area. Since the presented modulator also omits many of the optimizations which are normally done to reduce power such as using adjustable bias voltages for the active blocks and using scaled digital buffers, there is clearly a huge scope for improving the power consumption and area of the modulator. Applying these optimizations would lead to further improvement in the overall FOM of the modulator making it an attractive option for converting higher signal bandwidths.

5.4 Summary

An experimental prototype of the 4th order (2-2 cascade) $\Delta\Sigma$ modulator has been fabricated in UMC 90nm/1V technology through Europractice. This chapter described the prototype, layout, floorplan, pin description, PCB, test setup and the experimental results used to verify and characterize the modulator. The experimental results indicate that the modulator performs as expected and achieves the necessary resolution and performance, similar to the simulations. It is shown that the presented modulator can compete with other similar state of the art reconfigurable architectures and also has the possibility of further improving its FOM by optimizing the power consumption of analog and digital blocks.

6 Conclusion and Future Work

Contents

6.1 Contributions of the Work

The main contributions of the thesis are summarized as follows:

- This thesis presents the behavioral analysis, modeling and design of $\Delta\Sigma$ modulators based on CCII integrators. It is shown through analysis that the existing CCII integrator topologies are not capable of operating at high sampling frequencies and are not suitable for integration in advanced CMOS technologies due to the presence of parasitics and frequency dependent non-idealities of the active blocks.

- To overcome the problems, various SC integrator topologies based on CCII are proposed. It is shown that predistortion and memory compensation techniques substantially reduce the area and power requirements of the SC integrator circuit, allowing practical realizations of the integrator at the transistor level. Furthermore it is shown that using low distortion unity-STF modulator topologies that place less stringent requirements on the active blocks, it is possible to realize $\Delta\Sigma$ modulator using the proposed integrators that can compete with similar Op-Amp based counterparts.

- The thesis also introduced a simple adaptive calibration routine to increase the operating range of the proposed integrator. Using the calibration routine which consists of few additional programmable components and digital logic, the integrator was able to cover a wide range of sampling frequencies, thus making it useful in applications such as mobile communications.

- A prototype chip was implemented in UMC 90nm/1V technology to validate the concept. The DT 2nd order and 4th order cascade $\Delta\Sigma$ modulator have been experimentally verified to provide a SNDR of 72/69/61/65/62 dB and DR of 80/75/64/71/66 dB for signal bandwidths of 0.2/0.5/1/2/4 MHz and clock frequency of 40/80/80/120/120 MHz respectively. FOM calculations show that the modulator can compete with state of art reconfigurable DT architectures while using lower gain stages and less design complexity. Experimental results indicate the performance of the chip is in line with the simulations and comparable to state of art DT modulators in literature based on the obtained values for the FOM.

- The modulator is shown to perform well without applying any design optimizations normally employed by other modulators. Therefore for the presented modulator there is scope for significant improvement in the chip power consumption and area using the following optimization techniques. Adjusting the power consumption of the analog active blocks according to the sampling frequency using programmable bias. Optimizing the power consumption of the digital buffers by adjusting it according to the load it drives. Reducing the maximum size of the programmable memory compensation capacitor based on corner simulations instead of using the same values as the programmable integration capacitor. Use programmable current gains instead of programmable integration capacitor to reduce area and power.

6.2 Future Research Paths

The following topics related to the thesis are worth investigating with an aim of achieving better performance, power consumption and reduction in area.

- **Implementing offset cancellation schemes in the active blocks**. The proposed integrator architectures have been analyzed without including the offsets coming from mismatches in the singled ended paths. Future works might consider how these mismatches affect the output of the modulator, as well as analyze methods and techniques to reduce these offsets by applying already established techniques for offset cancellation in Op-Amps to the CCIIs.

- **Decrease digital power**. As stated in the previous chapter, the digital drivers used for routing clocks throughout the chip and driving switches in the programmable capacitor blocks have a higher driving strength than is necessary. Preliminary simulations show that the driving strength of the buffers can be reduced by 30-40% without significantly affecting the modulator performance. This results in further improvement of the modulator FOMs which would make the presented modulator the best in its class.

- **Explore regulated CCII to make the charge transfer more linear**. The presented modulator uses simpler translinear loops to achieve charge transfer and maintain low power consumption. However this results in increased non-linearity when the CCII and the buffer are used near the upper end of operating range. To improve the operating range, simple regulation schemes such as those used to design highly linear regulated current mirrors can be explored and applied to the design of the CCII.

- **Explore dual output ccii**. It was shown that a dual X output CCII can be used for lower sampling frequencies. Further investigation in this area can be done to apply the modulators in medical applications.

- **Explore automated shutoff of the Z port as soon as input X port is discharged to prevent charge loss during the charge transfer phase**. In comparator based SC circuits the current sources and sinks connected to the capacitors are disconnected as soon as the comparator detects the virtual ground at its inputs. This is done so as to prevent discharge of the capacitors through the finite resistance of the current sources. A similar principle can be applied here by using a variable charge transfer time with lower duty

cycle depending on the sampling frequency to reduce the charge losses and improve the integrator performance.

- **Explore alternative CCII topologies**. The translinear CCII depends on tight matching of the NMOS and PMOS paths to achieve higher linearity and reduce offsets. However as we go further in deep submicron technologies this becomes a problem. Hence alternative topologies, which can achieve class AB operation without using PMOS and NMOS transistors at same time, need to be explored.
- **Application of CCII SC circuit to other circuits**. The presented circuits can be further investigated for application in other circuits such as dual slope ADC, Ramp ADC and pipeline ADCs.

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[155] Ferdinand Keil. “Design of an Evaluation Platform for an Analog-to-Digital Converter ASIC”. Student Research Project. TU Darmstadt, Aug. 2012.

[156] Tanfer Alan. “Design of Temperature Sensor in SiGe 130nm Process”. Student Research Project. TU Darmstadt, May 2014.

[157] Tanfer Alan. “Design of Precision Current Reference For Laser Diode in SiGe 130nm Process”. Student Research Project. TU Darmstadt, May 2014.

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2000–2002	Board of Intermediate Education, "Ratna Junior College", Hyderabad, India
2002–2006	Student at the Department of Electrical Engineering, Jawaharlal Nehru Technological University, Hyderabad, India Degree:Bachelor of Technology in Electronics and Communications
2006–2009	Student at the Department of Electrical Engineering and Information Technology, Technische Universität Hamburg-Harburg, Germany Degree: Master of Science in Microelectronics and Microsystems
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Februar 2015