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DEVELOPMENT OF DC/AC POWER CONVERTERS FOR APPLICATIONS REQUIRING HIGH EFFICIENCY

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Preface

DC to AC converters are widely used in industrial applications, such as motor drives, harmonic compensators, active filters and inverters for renewable energy systems.

Efficiency of motor drives is often sacrificed in order to lower the price of the converters and to increase the power density of the systems. The development of power converters for renewable energy generation, instead, is mainly driven by efficiency requirements. Higher cost of the converters is in fact paid back by energy efficiency policies, and by larger energy production over the long term.

Silicon-based power devices have dominated power electronics applications over the last decades. Research and development in microelectronics have pushed the performance of power devices to face some fundamental limitations of silicon material. Wide bandgap semiconductors, such as silicon carbide, offer a solution to the pressing performance requirements of power electronic systems. Silicon carbide power devices can operate at higher temperatures, higher frequencies, and generate less power losses as compared to traditional silicon-based technologies. In the last few years, several silicon carbide devices have become commercially available on the market at reasonable cost, thereby offering great benefits for efficiency demanding applications.

The use of wide bandgap transistors, however, is not the only way to increase the efficiency of the converters. Special DC to AC topologies, named soft switching converters, can be adopted as well in order to reduce the switching losses of transistors. Several soft switching inverters and control strategies have been proposed in literature. The price that has to be paid to increase the efficiency, is a greater hardware and control complexity the converter.

The aim of this thesis is the development of DC to AC power converters for applications requiring high efficiency. Silicon and silicon carbide based inverters, as well as soft switching inverters, have been analyzed and fabricated for performance comparison.

The dissertation is organized as follows.

Chapter 1 presents the state of art on silicon and silicon carbide power devices.

Chapter 2 explores the power loss generation in power switches.

Chapter 3 presents a topology review of DC/AC soft switching converters. Particular attention is given to the operating principle and to the design guide lines of the Zero Voltage Transition converter with Two Coupled Inductors (ZVT2CI). The performances of a ZVT2CI prototype are compared to that of hard switching converters, based on latest silicon and silicon carbide technologies.

Chapter 4 explores inverter topologies for low power, single phase photovoltaic (PV) systems. In the first part of the chapter is presented the diffusion of photovoltaic systems in Italy and a review on the requirements for grid connected distributed generators. Particular attention is then given to the leakage current issue in transformerless PV system and to inverter topologies that can mitigate the problem. Eventually, the experimental performances of two single-phase transformerless inverters are presented, one built using high performance silicon switches, and one using high switching speed silicon carbide devices.

The last chapter presents a summary of the results obtained during the Ph.D. research activity.

Chapter 1

Trends in Power Transistors Technology

1.1 State of the art of silicon transistors

Efficiency of power electronic systems is strongly related to advances in power semiconductor technologies since large portion of the losses are dissipated by power transistors and diodes. Semiconductor power device technologies have evolved over the last decades improving the efficiency and lowering the cost of power converters [1].

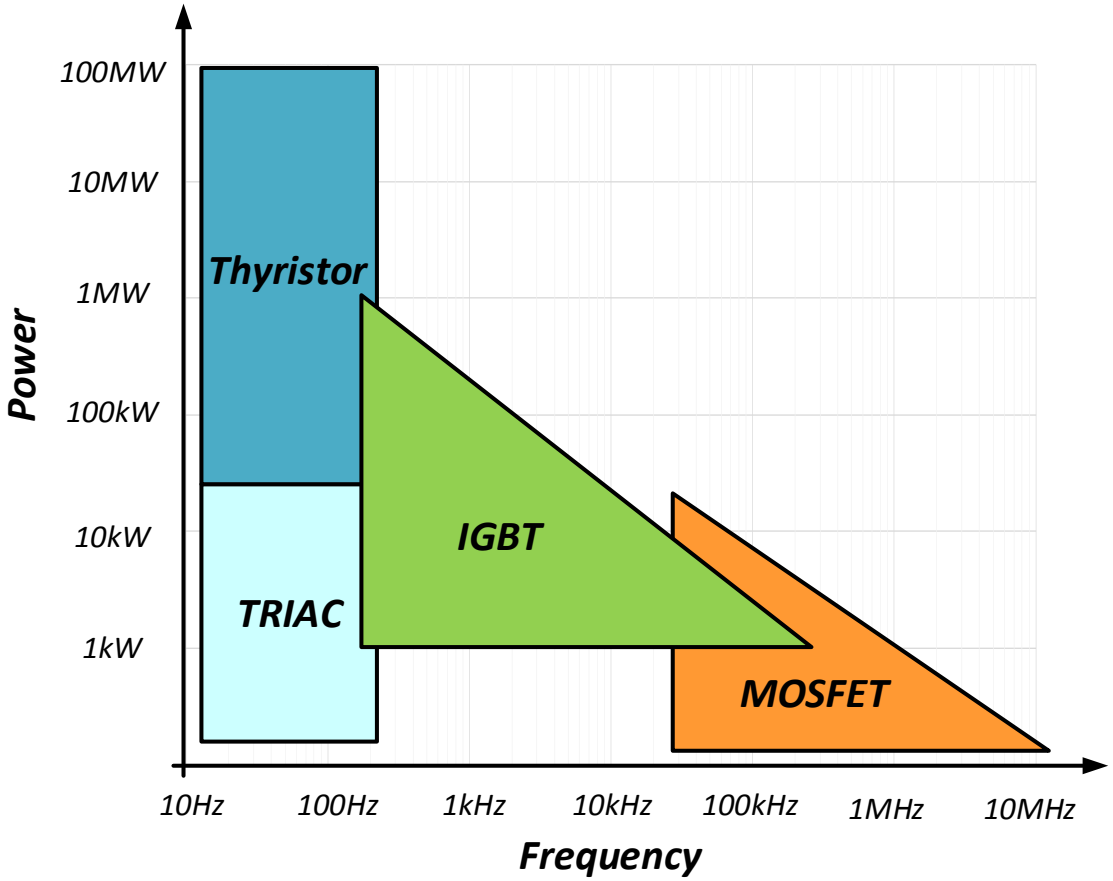


Figure 1.1 - Application of discrete power semiconductors.

Nowadays, power converters are mainly based on the mature and reliable silicon technology [2]. Power devices can be classified in two categories: controlled power switches and rectifiers. The controlled device family can be further divided in bipolar-based devices,

FET-based devices and devices, such as the IGBT, that combine a bipolar and a FET transistor.

Bipolar devices such as BJTs (Bipolar Junction Transistor), MCTs (Metal-Oxide Controlled Thyristor), GTOs (Gate Turn-off Thyristor) and IGCTs (Insulated Gate Controlled Thyristor) were the only power switches available before 80s [3]. The earlier power converter topologies of the silicon transistor era, e.g., bridge controlled rectifiers and cycloconverters, were developed around the characteristics of thyristors. The first real fully controllable power switch was the BJT. However, its slow turn-off characteristics (tail current) and the complexity required for the base driver circuitry, limited the diffusion of BJTs to low power and low frequency applications. Nowadays only IGCTs are still used, since they are the only feasible option for high voltage, for high power applications such as HVDC power stations and static synchronous compensators (STATCOMs) [4].

The commercial availability of power MOSFETs in the 70s, and IGBTs in the 80s represented an important breakthrough in power semiconductor device technology [5]. These new devices replaced bipolar transistors and thyristors for industrial applications, allowing the development of efficient power electronic systems.

The aim of this thesis is the development of DC to AC power converters for applications requiring high efficiency, such as photovoltaic inverters, motor drives, active filters and harmonic compensators. For these applications, the typical DC voltage level is in the range from 400Vdc to 800Vdc. As can be seen in Figure 1.2, IGBTs are the only feasible choice for applications above 1000V, while MOSFETs are the best devices for applications below 200V. In between 200V to 1000V the choice between IGBT and MOSFET is application dependent [6]. Requirements on cost, size, speed, reliability and efficiency contribute to select of the most suitable device.

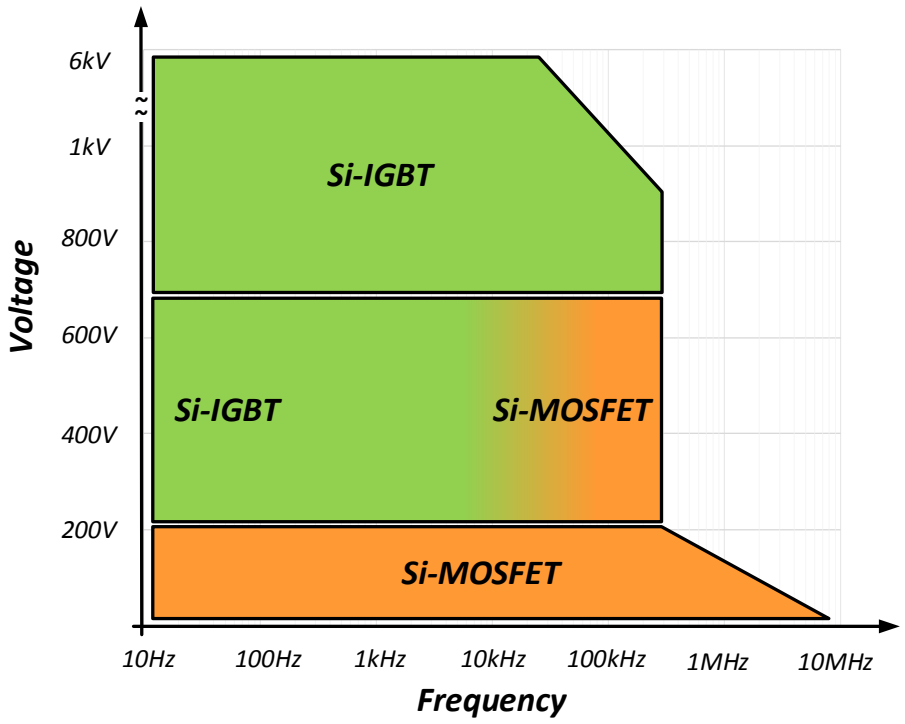


Figure 1.2 - Typical MOSFETs and IGBTs selection as a function of blocking voltage and switching frequency.

1.1.A Power MOSFETs

More than 30 years of research and development in microelectronics have led to silicon power switches with outstanding electrical performances, several classes of devices were developed following the requirements demanded by different kind of converter topologies.

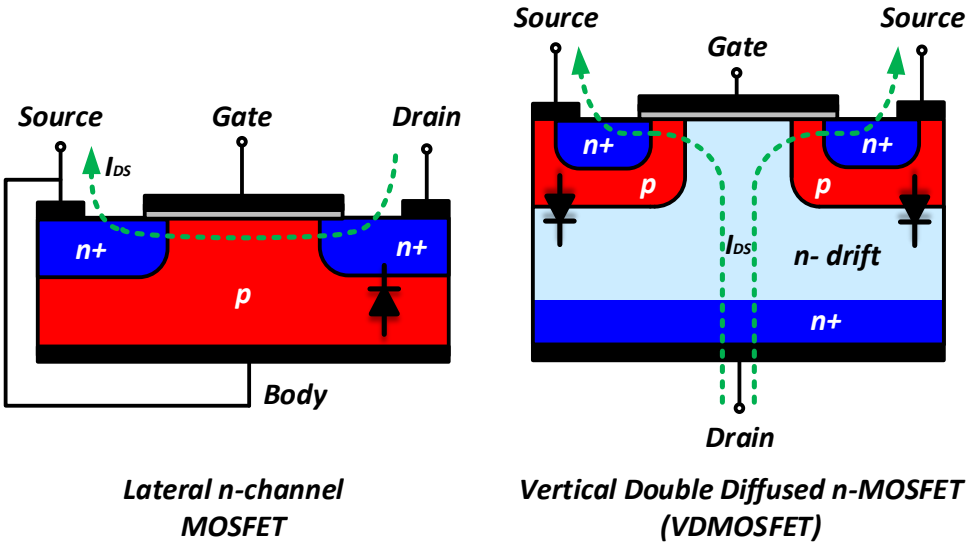


Figure 1.3 – Lateral and vertical MOSFET structures.

The earlier power MOSFET developed was a lateral device since, as depicted in Figure 1.3, the current flows along the plane of the device from the drain to the source. Lateral MOSFET have low on-resistance since the current flows in highly doped silicon region, however, the length of the channel increases with the increase of blocking voltage capability of the device, requiring larger silicon area [7]. For economic and power density reasons, the lateral MOSFET structure was replaced by the Vertical Double Diffused MOSFET (VDMOSFET). In this device, as can be observed in Figure 1.3, the current flows vertically from the top to the bottom through the silicon wafer [8]. The VDMOSFET structure includes an intrinsic body diode, therefore the operation in the first and in third quadrants of the V-I characteristic is allowed without the need of an external freewheeling diode. The drift region is a low-doping region of the MOSFET, which is required to support the block voltage when the device is off. Its thickness increases as the break down voltage (V_{BD}) rating of the device increases. As can be seen in Figure 1.4, for high voltage VDMOSFET the main contribution to the on state resistance is due to the drift region, therefore, the only way to reduce the overall on-resistance is to use larger silicon area, increasing the cost of the device. The minimum contribution of the drift region to the specific on-resistance per surface unit (R_{ON-SP}) is proportional to $V_{BD}^{2.5}$, which is known as 1D-Silicon limit of power MOSFETs [9]:

$$R_{ON-SP} = 6 \cdot 10^9 \, {V_{BD}}^{2.5} \, [\Omega/mm^2]. \tag{1.1}$$

Another weakness of power MOSFETs is the fact that, as the voltage rating increase, the reverse recovery characteristics of the parasitic body diode deteriorates causing the increase of switching losses [10]. For the technical and economic reasons above, power MOSFETs are hardly ever selected for applications above 200V.

VDMOSFET layout is still used today, power transistor companies have invested resources to improve the dynamic behavior of the device and to increase its power density. At the same pace of the improvement in VDMOSFET technology, other device structures were born in response to the demand of devices specifically optimized for low voltage and high voltage applications.

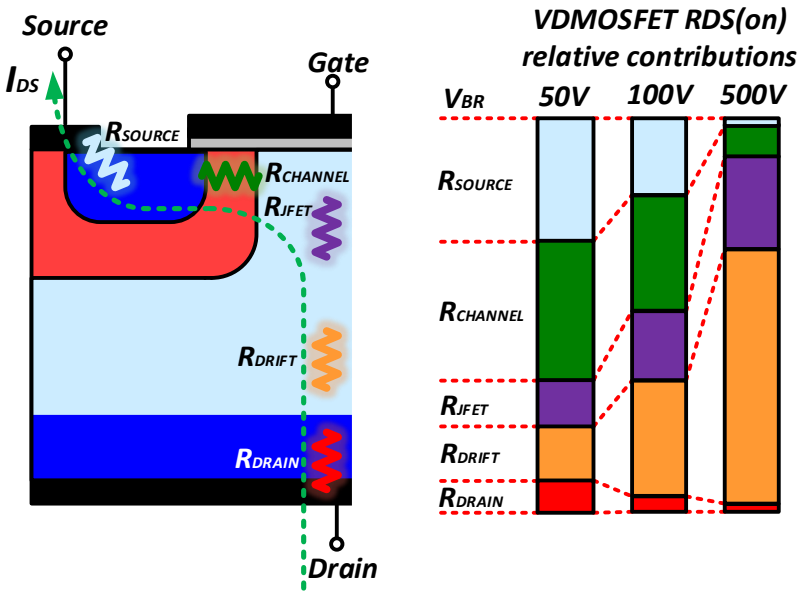


Figure 1.4 - Contribution to the on state resistance of a VDMOSFET as function of the blocking voltage

The trench gate MOSFET was introduced in order to reduce the conduction losses of the transistor in low voltage applications. As depicted in Figure 1.5, the gate of the trench MOSFET does not lay on the surface of the chip like in VDMOSFET, but it expands vertically inside the wafer. For this device, the induced channel in the P well region in the on-state is arranged vertically, so that the overall distance covered by the electrons is shorter than in the case of VDMOSFET. This solution reduces significantly the $R_{DS(on)}$ of the transistor [11].

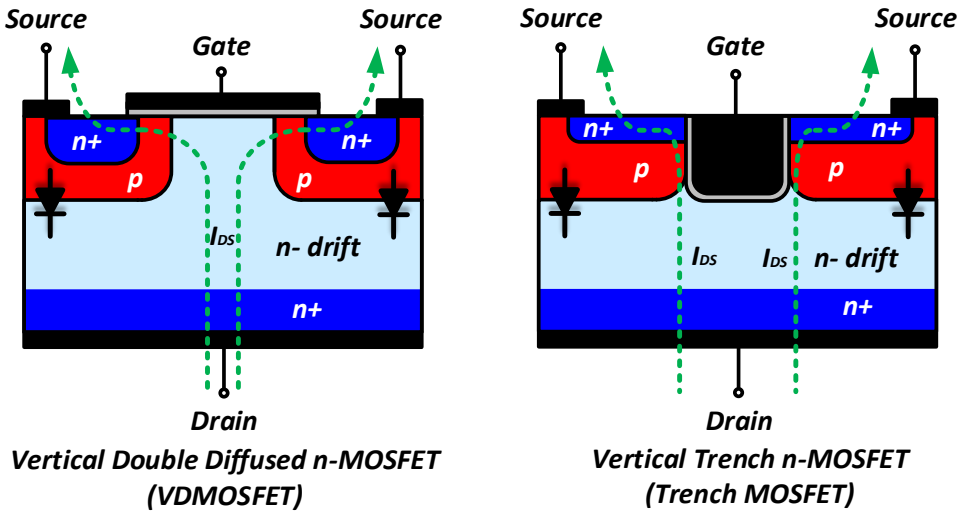


Figure 1.5 – VDMOSFET and trench MOSFET structures.

Regarding high voltage MOSFETs, a breakthrough in the technology was the introduction in the late 90's of a device structure that broke the 1D-limit of power MOSFETs [12]. The concept was based on the charge compensation effect, known as super-junction principle [13], a special structure that allows a significant reduction of the drift region resistance. Super-junction power devices were commercially introduced in 1998 by Infineon (CoolMOS) [14], and are now available from 500V to 900V. The theoretical R_{ON-SP} limit of VDMOSFETs and SJ MOSFETs are depicted in Figure 1.6. It can be seen that the super junction technology can potentially achieve higher power density than VDMOSFET. However, super junction MOSFETs, for physical reasons, are more prone to have a low performance body diode. In DC to AC inverter topology i.e. half bridge, full bridge and three phase inverter, the presence of the freewheeling diode in parallel to the transistor is essential for the proper operation of the converter. Several applications reported the failure of the transistors under hard turn off of the diode due to its reverse recovery characteristic [15] [16] [17]. As reported in the section 2.2, for half bridge-based converters under inductive load, the reverse recovery current of the diodes increases the turn-on losses of the power transistor and is seen as a temporary shoot-trough of the DC source.

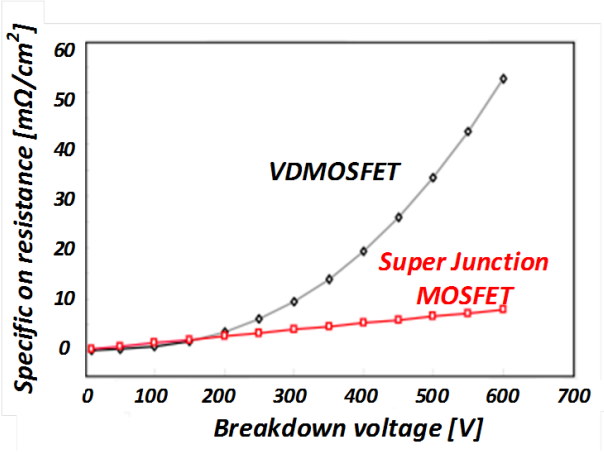


Figure 1.6 – 1D-Silicon limits of VDMOSFETs and SJ MOSFETs

Although SJ MOSFETs are hardly ever selected for DC to AC inverters, they are widely used in DC to DC power conversion. In topologies such as buck, boost, PFC and Flyback the body diode never conducts, so all the benefits of the power MOSFETs can be exploited.

1.1.B Power IGBTs

The technological evolution of the power transistors has affected also IGBTs family. During the last two decades significant advances were achieved in the fabrication of IGBTs.

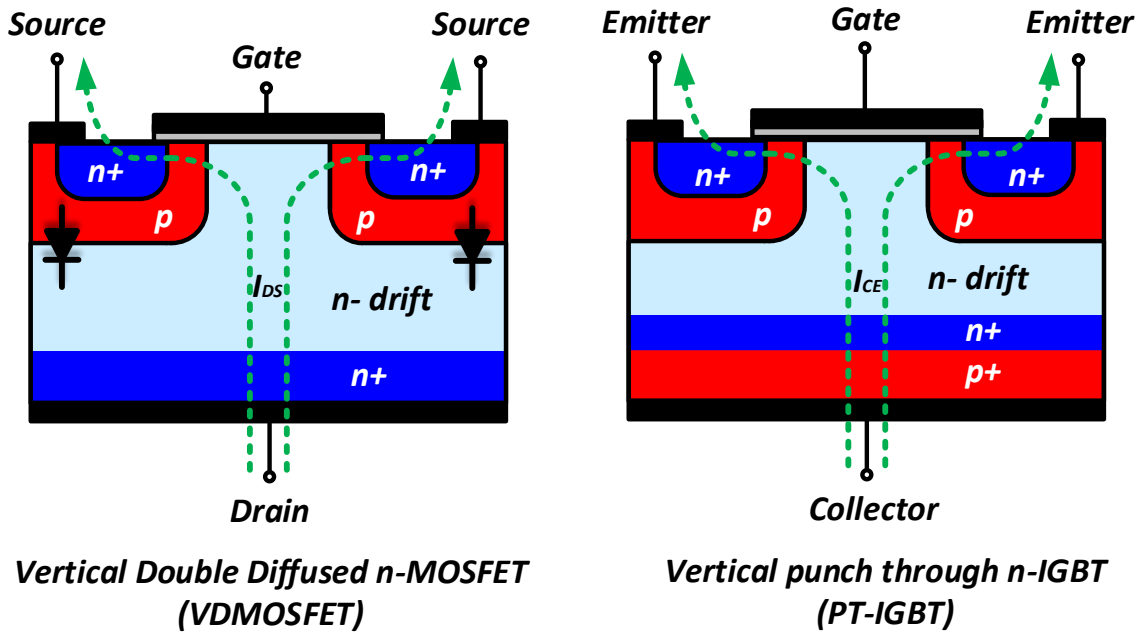


Figure 1.7 – Comparison of the structure of a VDMOSFET and of a PT IGBT.

The basic layouts of a power MOSFET and of a IGBT look very similar. The cross section of the firstly commercialized Punch Through (PT) IGBT and the one of the VDMOSFET are depicted in Figure 1.7. It can be notice that an IGBT is a power MOSFET with the addition of a P layer under the N substrate. However, in spite of the similarity, the physical operation of the IGBTs is closer to that of bipolar transistors rather than that of power MOSFETs. During the on-state, the P layer injects holes into the highly resistive n- drift layer increasing its conductivity. The overall effect is the reduction of the on-state voltage drop of the device. For this reason, IGBT is sometimes called conductivity modulated metal oxide field effect transistor [18]. For the reasons above, the IGBT merges the high current handling capability of a bipolar transistor with the ease of control of a MOSFET.

Another important characteristic of IGBTs is the absence of a parasitic body diode typical of MOSFETs. This feature gives the freedom and the flexibility to choose an external fast recovery diode to match the target application [19].

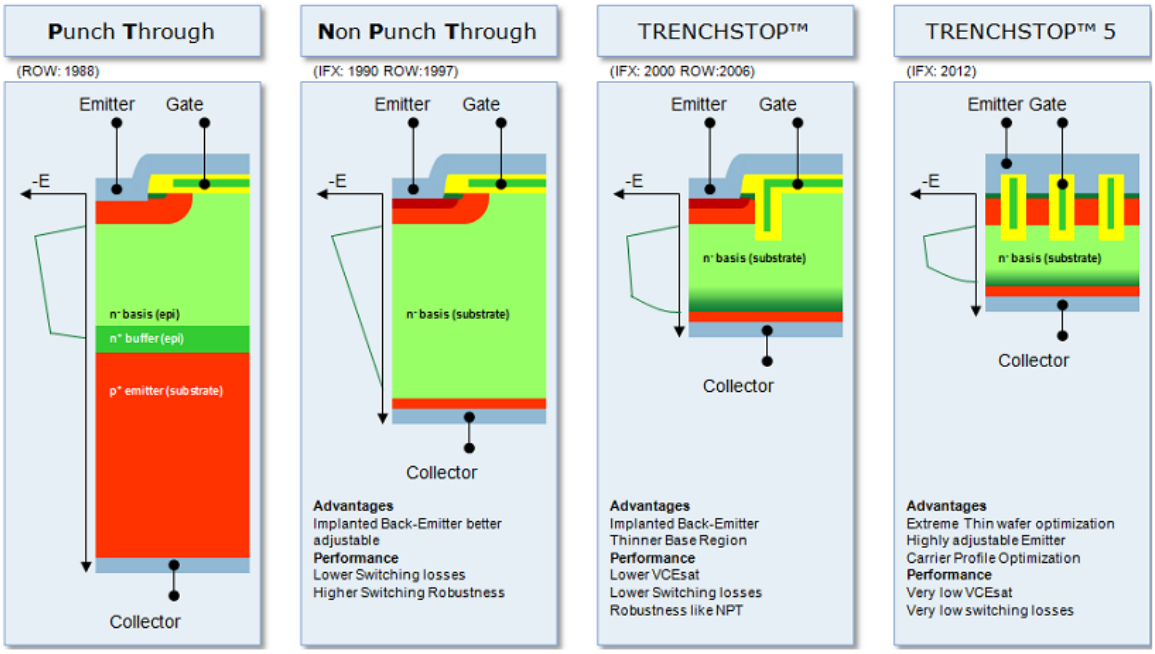


Figure 1.8 - Evolution of Infineon IGBTs, from Punch Trough to TRENCHSTOP™ 5 technology

Early versions of IGBTs suffered severe limitations. First of all, they could potentially loose ability to be turned-off (latch up) in some dynamic conditions [20], furthermore, the negative temperature coefficient of IGBTs made the parallel operation of devices hard to achieve [21]. The problems above are no longer present for the latest generations of IGBTs, moreover, improvement in the switching performances have narrowed the gap between IGBTs and MOSFETs. Figure 1.8 compares the cross sections of different IGBT technologies, namely planar Punch Through (PT), planar Non Punch Through (NPT), Trench Field Stop, and their historical introduction on the market [22].

1.2 Wide bandgap materials – Silicon Carbide

The development of power semiconductor devices has always been a driving force for power electronics systems. For a long time, silicon-based power devices have dominated the power electronics applications [23]. As the needs and requirements for electric energy continuously grow nowadays, silicon devices are coming to face some fundamental limits in performance due to the inherent limitations of silicon material properties.

Wide bandgap materials, such as Silicon Carbide (SiC) offer a long term solution to the pressing requirements on dynamic performance and efficiency requirements of power electronic systems [2] [24] [25] [26] [27].

In a solid material, electrons exist at energy levels that combine to form energy bands [28]. The top level band is called the conduction band and the lower is called valence band. The region between the valence band and the conduction band is a forbidden state where ideally no electron exists. If the electrons in the valence band are excited externally, they can jump to the conduction band. For a conductor, like copper, the forbidden band does not exist and the energy bands overlap completely. For an insulator, on the other hand, this band is so wide that the electrons need large amount of energy to move from the valence band to the conduction band. For the semiconductors conversely, the forbidden gap exists and is smaller than that of an insulator. At a certain temperature, electrons have enough energy to move spontaneously to the conduction band, this generate an uncontrolled conduction mode that must be avoided. In silicon transistors, the temperature at which the devices start to behave like a conductor is around 170°C. Wide bandgap semiconductors have the advantage of high temperature operation as the thermal energy required to promote electrons in the valence band is higher than the one of silicon materials (1.12 eV). The energy bandgap level is not the only propriety that make SiC superior material for power electronics devices. The main physical property of Si and SiC semiconductors are reported and compared in Table 1.1.

Table 1.1 - Material properties of silicon and silicon carbide.

Property	***Si***	***SiC***
Breakdown Field (MV/cm)	0.3	2.2
Energy Bandgap (eV)	1.1	3.3
Thermal conductivity [W/cm K]	1.5	4.9
Saturated electron drift velocity [cm/s]	1	2
Electron mobility ($10^{\wedge 3}$ cm^2/V sec)	1.5	1

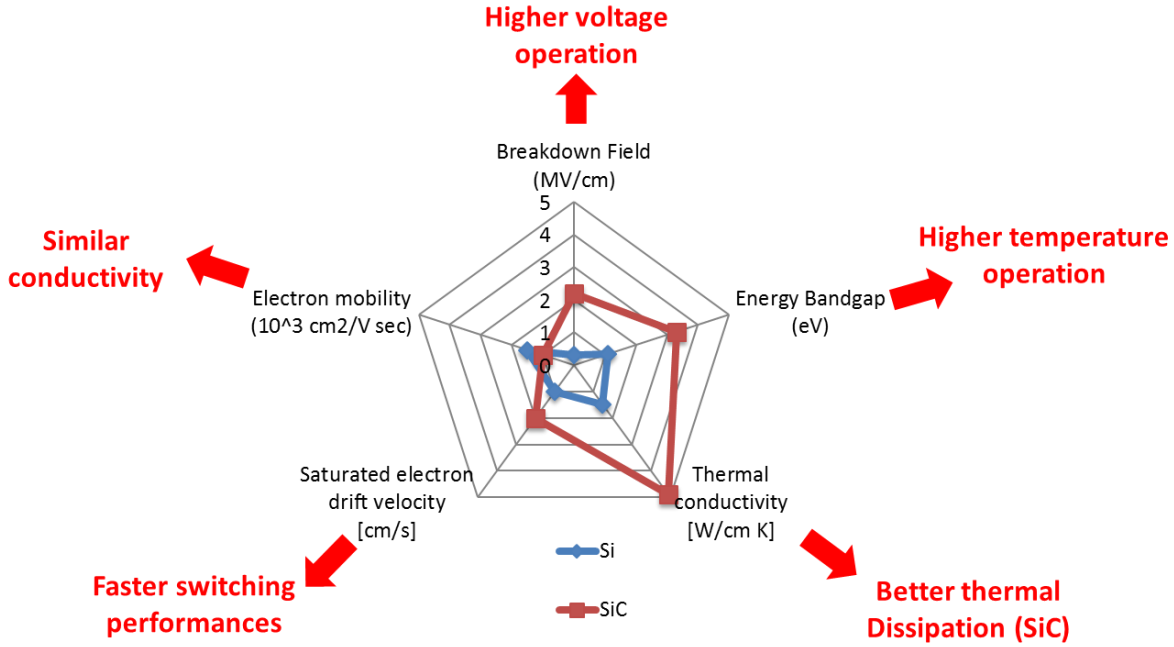


Figure 1.9 - Material properties of silicon and silicon carbide.

As can be seen in Figure 1.9, SiC presents greater thermal conductivity, higher critical electric field, higher saturated electron drift velocity, and slightly lower electron mobility than Si [29].

SiC offers a critical electric field that is more than seven times higher than Si. This property increases the voltage blocking capability of power devices and allows the reduction of the drift layer thickness of power MOSFETs, reducing significantly the on-state resistance. Furthermore, the higher thermal conductivity of SiC makes it superior to Si in terms of heat dissipation, while the wider bandgap energy (3.3 eV) allows high-temperature operation above 300 °C. The superior electron drift velocity also makes SiC devices capable of extremely fast commutation.

Infineon Technologies and Cree Inc. introduced the first commercial SiC power devices in 2001 and 2002, which were 600V SiC Schottky diodes [30], [31]. Schottky diodes are majority carrier devices, therefore they do not exhibit the reverse recovery phenomena, a very favorable characteristic for high-voltage applications [32]. SiC technology extended the breakdown voltage of Schottky diodes above 1000 V, which was previously limited below 200 V for Si technology. Another important characteristic of the SiC Schottky diodes is their positive thermal coefficient, which allows a stable parallel connection of diodes in order to handle high currents. The success of the SiC Schottky diodes pushed the development and

commercialization of the first junction field-effect transistor (JFET) by SemiSouth Laboratories in 2008 [33]. In 2011, three years after the release of the SiC JFET, Cree commercialized the first SiC Vertical Double Diffused MOSFET (SiC VDMOSFET) [31].

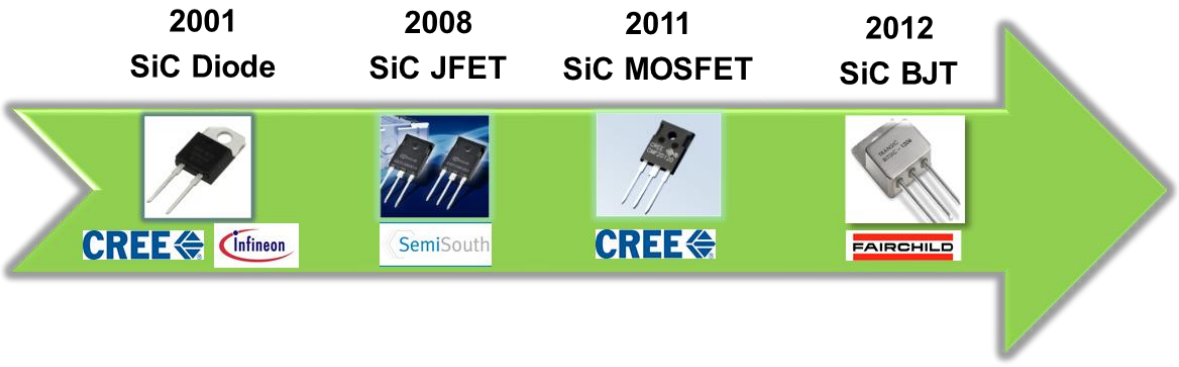


Figure 1.10 - History of the commercialization of SiC devices.

Today, several manufacturers produce SiC MOSFETs, including General Electric (GE), ROHM Semiconductor, Mitsubishi Electric, Microsemi, GeneSiC, and United Silicon Carbide. In 2012 the first SiC bipolar junction transistor (BJT) was presented by Fairchild [34].

SiC PN diodes [35], IGBTs [36] and thyristors [37] are still under development, and are targeted at high voltage systems (> 10 kV).

Chapter 2

Power Loss Mechanism in Power Transistors

2.1 Introduction

Understanding the power loss mechanism of power transistor is essential for the development of efficient power converters.

Device losses can be divided in two main contributes, the conduction losses and the switching losses [10]. Conduction losses are defined as the energy dissipated by a transistor or diode is in the conduction state (on-state). This loss contribution is related to the static characteristic of power switches, i.e., unipolar and bipolar devices but is independent to the switching frequency of the converter. As described in the previous chapter, many generations of MOSFETs and IGBTs have been developed during the last 30 years with the aim of the reduction of the forward voltage drop.

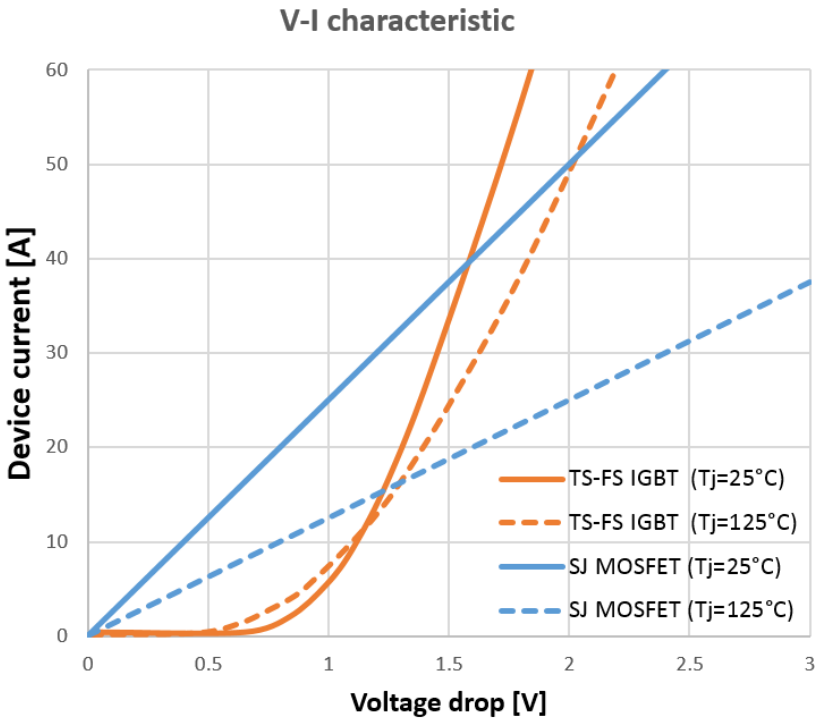


Figure 2.1 – V-I characteristic two typical 650 V IGBT and SJ MOSFET rated for the same current

Generally, power MOSFETs have a linear forward voltage drop whereas IGBTs, being bipolar devices, show a diode like exponential characteristic. For example, the forward characteristics of two best in class devices are reported in Figure 2.1; the first is a 650V, 40A trench-field stop IGBT (TS-FS IGBT) and the second is a 650 V, 40A, 40 mΩ Super Junction MOSFET (SJ MOSFET). It can be seen that the two 25°C characteristics match at 40A. Below the nominal current, the voltage drop of the MOSFET is lower than the voltage drop of the IGBT, making the device more efficient during low load conditions. On the other hand, the forward characteristic of the MOSFET deteriorates more than the one of the IGBT when the junction temperature is 125 °C, making the IGBT more suitable for overload and high temperature operations.

The choice of the best device suited for the target application cannot be done only on the basis of the conduction behavior, switching losses must be considered as well. Switching losses are defined as the energy dissipated by the device during the transition from the on-state to the off-state, and vice versa, due to the overlap of the applied voltage and the conducted current.

In first analysis, switching losses depend on the dynamic performance of the devices, on the voltage applied in the block state, on the switching frequency and on the converter topology. Several families of MOSFETs and IGBTs have been developed with the aim of reducing the conduction losses, switching losses or a tradeoff of them.

2.2 Losses in AC to DC power converters

The world most diffused architectures of DC to AC power conversions are based on the half bridge two levels converter, also known as inverter leg, which consists of two power transistors in a totem pole configuration [10]. Single phase, three phase and, more in general *m*-phase DC to AC two level converters can be obtained connecting together *m* inverter legs, as illustrated in Figure 2.2.

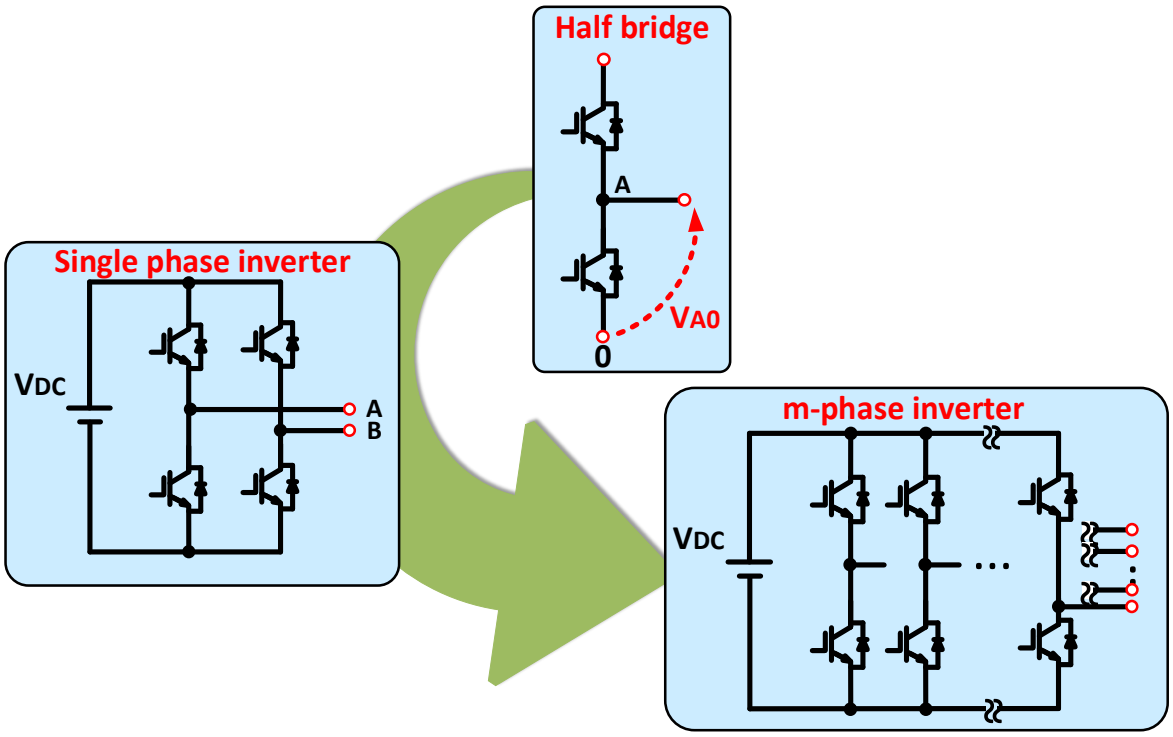


Figure 2.2 – multi phase DC/AC converters based on the half bridge leg.

The half bridge topology, controlled by pulse width modulation (PWM), is widely adopted in industrial applications, especially with an ohmic-inductive load connected to the output. In this configuration, during the switching transient, the output inductance maintains nearly constant the load current, which commutates from a transistor to the complementary freewheeling diode and vice versa. Since this commutation mechanism is the most diffused operation mode in power electronics converters, manufactures provide the turn on and turn off losses of their transistors using a simplified operation of the half bridge under inductive mode operation, called double pulse tester (DPT) [38]. Basically the double-pulse tester is an inductive load buck converter, containing one device under test (DUT), one freewheeling diode (usually the same diode endowed in the DUT) and a load inductor (See Figure 2.3).

A two pulse train is sent to the gate of the DUT, the widths of both pulses and the interval in between them is adjustable.

During the first pulse, V_{DC} is applied to the inductor L_0 and current I_0 rises linearly:

$$\frac{dI_0}{dt} = \frac{dI_C}{dt} = \frac{V_{DC}}{L_0}. \tag{2.1}$$

Since in this condition the load current flows through the DUT, the duration of the fist gate pulse T_1 is adjusted in a way to obtain the desired value for the current $I_{C\,TEST}$:

$$T_1 = \frac{L_0\, I_{C\,TEST}}{V_{DC}}. \tag{2.2}$$

The falling edge of the first pulse corresponds to the turn off of the device, then the turn off switching energy E_{OFF} at the current $I_{C\,TEST}$ and voltage V_{DC} can be evaluated.

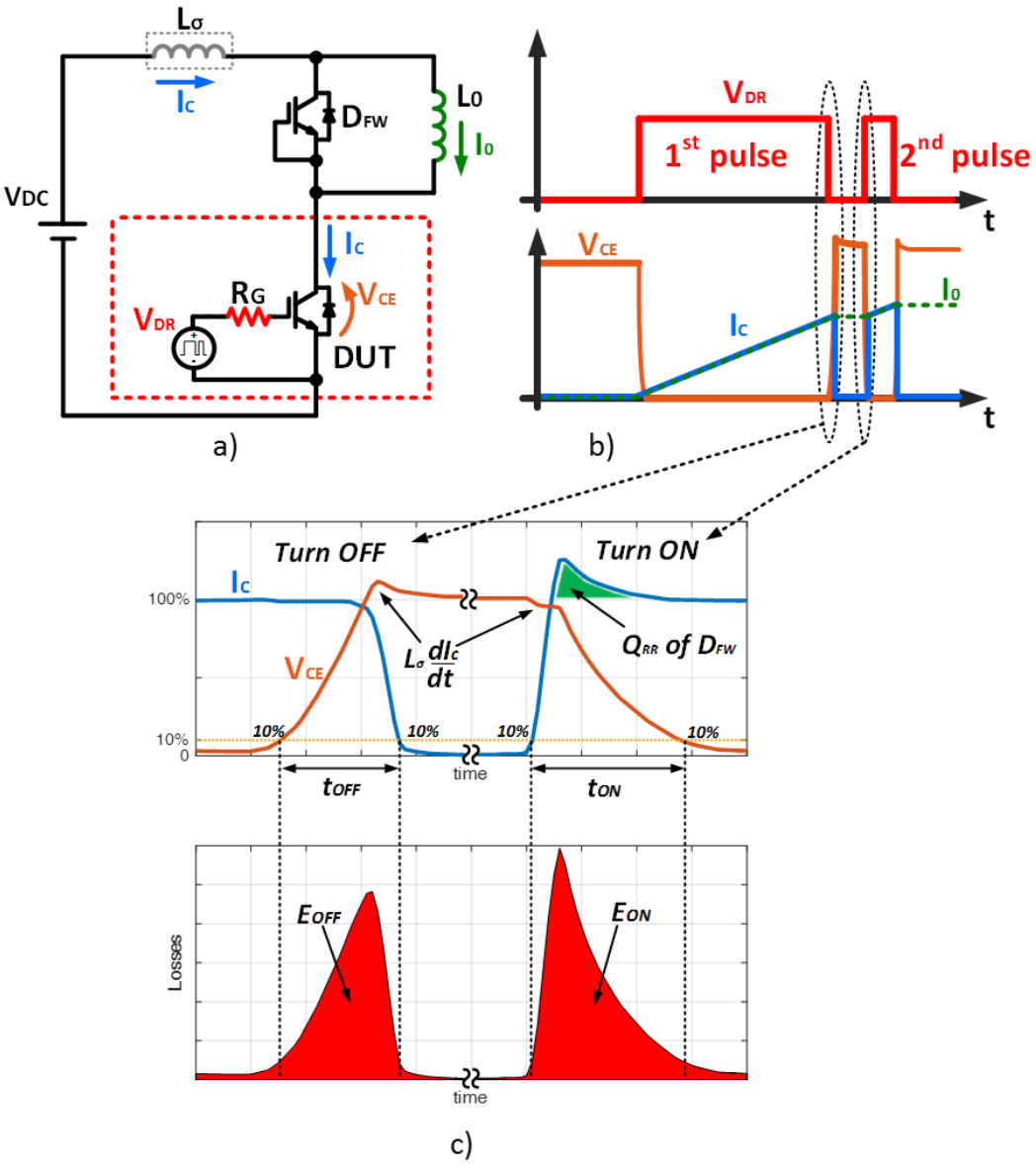


Figure 2.3 – Switching characterization test power switches. a) double pulse tester. b) gate-emitter voltage, collector-emitter voltage and collector current of the DUT. c) switching waveforms during turn-on and turn-off.

Between the fist and the second gate pulse, the load current flows through the top freewheeling diode D_{FW} and remains nearly unchanged at the value $I_{C\,TEST}$. The rising edge of the second pulse corresponds to the turn on of the device at current $I_{C\,TEST}$ and voltage V_{DC}, then turn on switching energy E_{ON} can be evaluated.

The typical voltage and current switching waveforms of a power switch in the DPT are depicted in Figure 2.3. The turn-on time t_{ON} is defined as the time between the moment at which the conducted current (I_C) rises to 10% of the $I_{C\,TEST}$ current to the moment at which the applied voltage (V_{CE}) falls to 10% of the steady state blocking voltage V_{DC}. The turn-off time t_{OFF} is defined as the time from the moment at which the applied voltage (V_{CE}) rises to 10% of the steady state blocking voltage V_{DC} to the moment at which the conducted current (I_C) falls to 10% of the test current $I_{C\,TEST}$. The turn-on switching energy E_{ON} and the turn-off switching energy E_{OFF} are defined as the integrals of the product of V_{CE} and I_C over t_{ON} and t_{OFF} respectively.

The switching speed of the transistor, i.e., $\frac{dI_C}{dt}$ and $\frac{V_{CE}}{dt}$, can be varied, within the safe operation limits of the device, changing the value of the gate resistance R_G. Faster switching speed reduces the overlap time of V_{CE} and I_C, hence, reducing the switching losses.

The junction temperature T_j of the DUT influences the switching energy as well. The DUT junction temperature during the test can be regulated by using a temperature controlled heatsink.

It's important to mention that the reverse recovery charge Q_{RR} of the freewheeling diode takes part to the switching loss generation increasing the carried current of the DUT during the turn on. Silicon Fast Recovery Diodes (FREDs) are usually chosen as a freewheeling diode of IGBTs due to their low reverse recovery charge. In the case of Si-MOSFET, the freewheeling diode coincides with the intrinsic parasitic body diode. However, the reverse recover performance of the body diode of MOSFETs degrades as the voltage rating increases. For high voltage MOSFETs ($V_{BD} > 250V$), the reverse recover characteristics of the body diode is usually so poor that the transistor can easily fail due to the excessive heat generation. The introduction in 2001 of the first 600V zero reverse recovery charge SiC Schottky diode made possible the fabrication of hybrid Si-IGBT + SiC-Schottky devices for efficiency demanding applications. Differently from silicon SJ MOSFETs, silicon carbide MOSFETs

counterpart are suited for the operation in totem pole configuration since the parasitic body diode has dynamic behavior similar to a FRED diode.

Another important parameter that affects the switching losses of the DUT is the parasitic inductance in the power loop of the double pulse tester. The DUT current I_C flows also through the stray inductance L_σ, increasing the transient blocking voltage on the DUT at the turn on ($L_\sigma \frac{dI_D}{dt} > 0$) and reducing the applied voltage at the turn off ($L_\sigma \frac{dI_D}{dt} < 0$), therefore increasing E_{OFF} and reducing E_{ON}.

In fist approximation, switching losses of a transistor operating in a half bridge configuration are function of:

$$E_{sw} = f(V_{DC}, I_C, R_G, T_j, L_\sigma, Q_{RR}). \tag{2.3}$$

Device manufacturers provide in the datasheet of their devices the switching energies obtained in the DPT, varying the key parameters that influence the switching losses i.e., V_{DC}, I_C, R_G and T_j. The switching losses obtained in the DPT of a commercial IGBT (Infineon IKW30N60T) are depicted in Figure 2.4 and Figure 2.5.

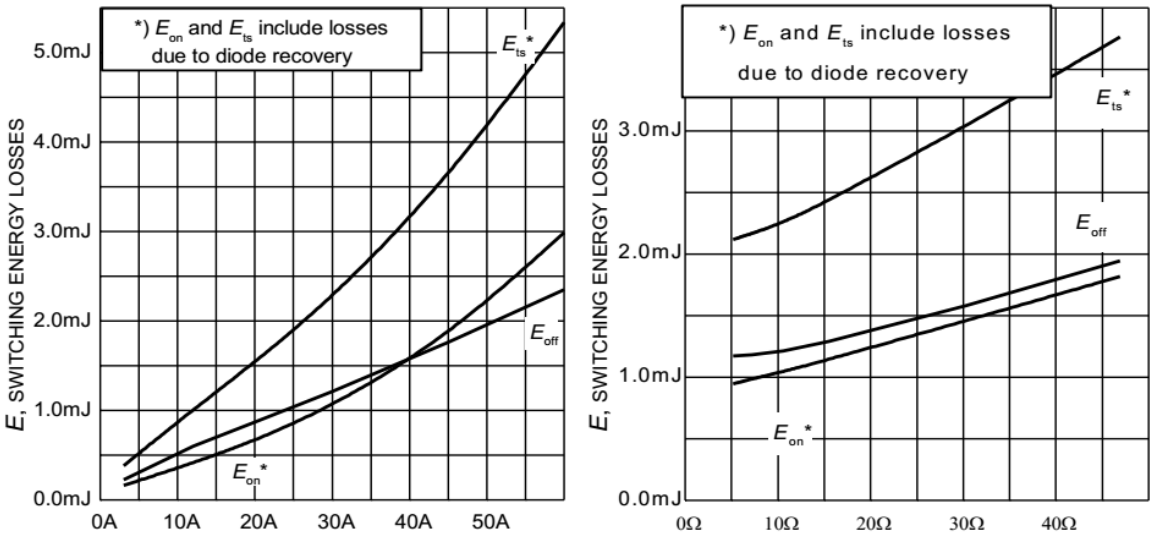
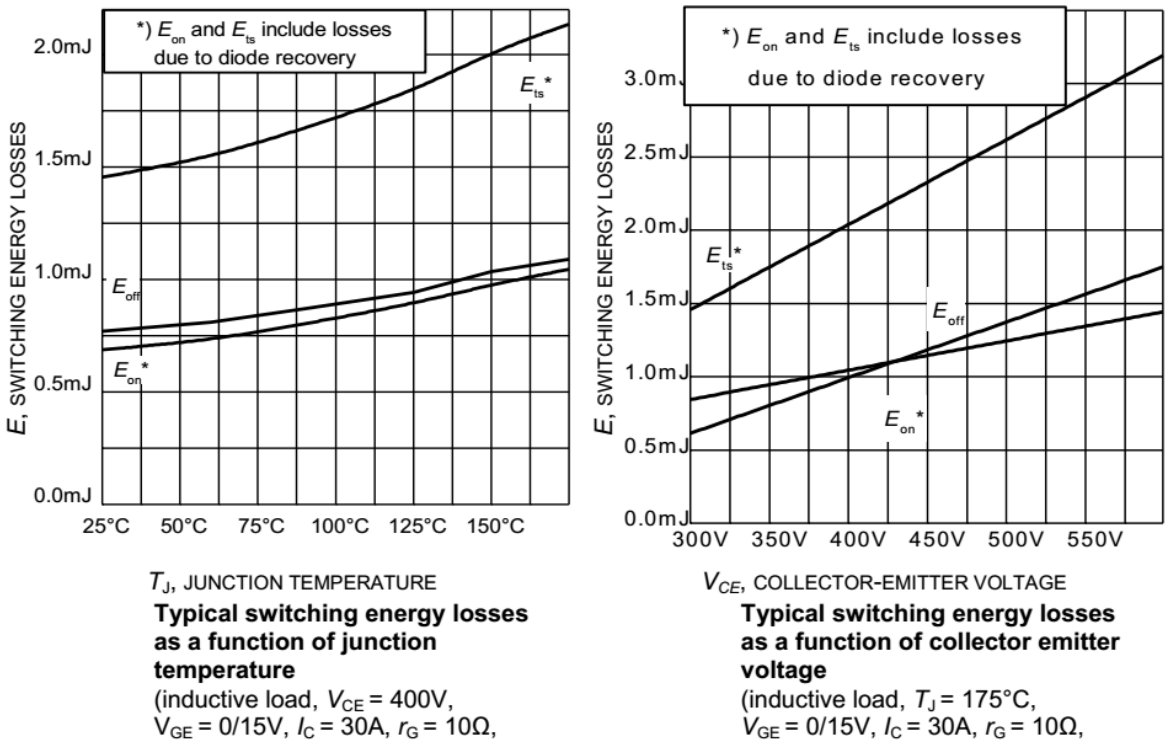


Figure 2.4 – Switching energies of the IGBT Infineon IKW30N60T as function of collector current (left figure) and of gate resistance (right figure)



Typical switching energy losses as a function of junction temperature
(inductive load, V_{CE} = 400V, V_{GE} = 0/15V, I_C = 30A, r_G = 10Ω,

Typical switching energy losses as a function of collector emitter voltage
(inductive load, T_J = 175°C, V_{GE} = 0/15V, I_C = 30A, r_G = 10Ω,

Figure 2.5 - Switching energies of the IGBT Infineon IKW30N60T as function of the junction temperature (left figure) and of collector-emitter voltage (right figure)

In half bridge based converters, given the switching frequency and the modulation technique, the only way to reduce the switching losses is to select fast transistors, low reverse recovery diodes and minimize the parasitic inductance of the power loops.

Topologies in which power losses are generated during the turn on and off of the transistors are called hard switching converters, all the DC to AC converters based on the 2L half bridge topology are part of the hard switching family.

A different way to improve the overall efficiency of AC to DC power converters is to use topologies that reduce the switching losses, avoiding the simultaneous presence of high voltage and high current during the commutation of the transistors. Such kind of topologies are called soft switching converters [10].

Switching trajectory is a graphical way to see the switching behavior of a transistor by superimposing the voltage V_{CE} and the current I_C in a X-Y plot. The switching trajectories of the DUT previously presented in Figure 1.1, are depicted on the left side of Figure 2.6. It can be clearly seen that hard switching commutations appear as rectangular square trajectories. The soft switching locus in the V_{CE}-I_C plane instead, appear completely different. As can be

seen in the right side of Figure 2.6, the transition from the on state to the off state and vice versa moves along the axes of the graph, avoiding then the overlap of high voltage and high currents i.e. reducing the switching losses.

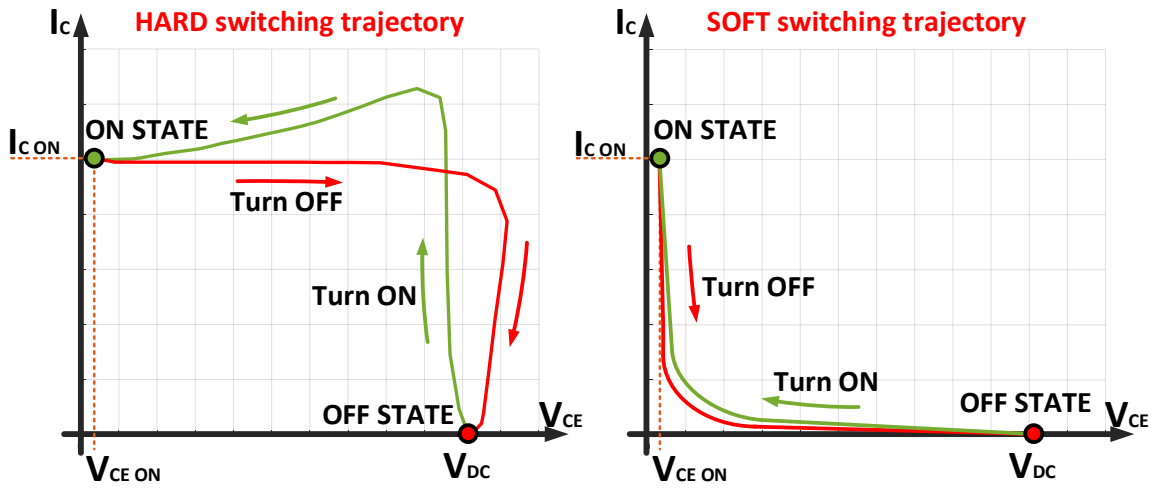


Figure 2.6 – Comparison of hard and soft switching trajectories.

Inevitably, to archive the soft switching operation, the complexity of the converter is increased when compared to a standard hard switched inverter.

Power electronic designers are called to choose the converter topology and select power devices that can satisfy the constraints on cost, efficiency, performance and power density of the converter. For applications requiring high efficiency, the higher complexity and cost of a soft switching converter can be justified only if the overall efficiency is higher than the efficiency obtainable with a simpler structure, e.g., half bridge based converter, using the best power transistors available on the market.

Further details about soft switching converters are presented in chapter Chapter 3.

Chapter 3

Soft Switching in DC to AC Converters

3.1 Introduction

Developments in power electronics of the last two decades involved not only power switches, but also circuit topologies and control strategies. Since the 70s, the most diffused control technique for power converters is the Pulse Width Modulation (PWM). Ideally, power switches are operated only in two low-loss conditions, the interdiction state (fully off) and the saturated state (fully on). When a switch is in the off state and high voltage is applied to the device, practically no current is allowed to flow. Instead when the switch is on, the current can flow through the device with a very low internal voltage drop (<2 V). Power losses, being the product of voltage and current, are thus in both cases extremely low. However, during the commutation between the on-state and the off-state, transistors could be subjected to the simultaneous presence of high voltage and high current, which lead to high levels of power losses.

Converter topologies in which power losses are generated during the commutations are called *hard switching* converters.

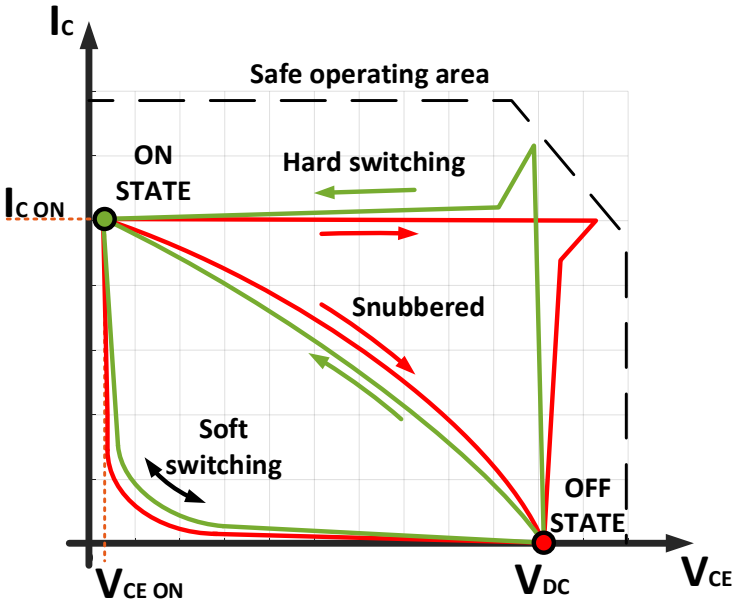


Figure 3.1 – Comparison of typical hard, snubbered and soft switching trajectories of an IGBT or BJT.

A typical trajectory in (V_{CE}, I_C) plane of a switch, operated in hard switching conditions is shown in Figure 3.1 for an IGBT (V_{CE} is the collector-emitter voltage, I_C is the collector current). It is important to mention that the switching trajectory must be inside the Safe Operating Area (SOA) prescribed by the manufacturer for the device, operation outside this limit leads to the failure of the device. A possible solution to relieve the stresses of the component is the addition a snubber circuit (suppressor), which reduces the overlap of high values of current and voltage and consequentially the power dissipated by the device. However most snubber circuits divert the part of energy that would be dissipated by the transistor to an external dissipative circuit, e.g., RC snubber and RCD snubber, hence it is clear that the global efficiency of the system is not increased.

In the 80's, considerable research efforts were directed toward the use of resonant topologies to increase efficiency of converters [39]. The basic idea was to include reactive elements in converters, in order to induce sinusoidal oscillations that create the conditions for a zero-voltage (ZVS) or zero current (ZCS) switching of the transistors. This behavior corresponds, in the (V_{CE}, I_C) plane, to a switching trajectory that avoids the simultaneous presence of high voltage and high current. Such kind of topologies were firstly called *soft switching* converters. The drastic reduction of the switching losses and the technological improvement of the devices made possible to achieve switching frequencies of hundreds of kHz (typically 100-200 kHz). However, resonant converters had several drawbacks in comparison to conventional PWM converters, e.g., higher peak current and higher voltage stress, leading to higher conduction losses and requiring devices with higher voltage and current rating. Furthermore, resonant converters where controlled by means of frequency modulations techniques (FM) rather than PWM, making this new class of converters more suited for DC to DC applications rather than for DC to AC inverters.

In the late 80s and during the 90s, new generations of soft-switching converters that combined the advantages of conventional PWM converters with those of resonant converters were proposed. Unlike full resonant converters, the resonance phase is used in a controlled way, during the on and off transition of the switches, creating the conditions for zero voltage and zero current switching. Apart from the resonant transition, these converters behaved like traditional PWM converters.

3.2 Overview of DC to AC soft switching inverters

Soft-switching techniques offer a substantial reduction of the losses, allow high frequency operation and avoid the use of the dissipative snubbers. Many soft switching inverters and control strategies have been proposed, a general classification of soft switching inverter proposed in [40] is shown in Figure 3.2.

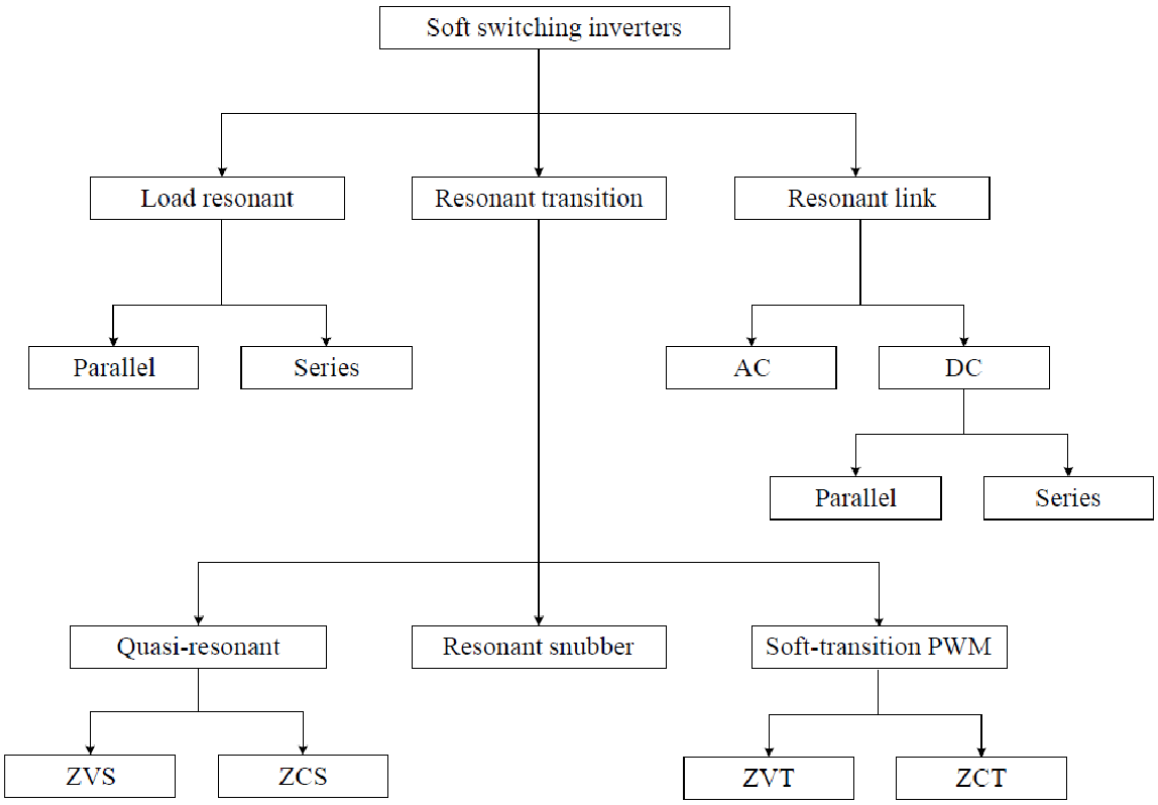


Figure 3.2 – Classification of soft switching DC/AC converters

Since in soft switching converters commutations have to happen when the voltage or the current of the switches are zero, measurement circuits are required to detect the ZV and ZC conditions and to trigger the gate driver of transistors; high bandwidth measurement circuits are hence required. Voltage measurement is quite easy to implement, whereas high bandwidth current measurement is more complicated. The simplest method for current measurement is the use of a shunt resistors, which acts as a linear current to voltage transducer, although power losses are introduced by the resistor as well as stray inductance in the power loop. For the reasons above, zero voltage switching operation is generally preferred to zero current switching.

Regarding zero voltage switching converters, it is possible to follow two different approaches to achieve soft switching.

Resonant DC-Link family:

- Resonant DC-link inverter [41];
- Actively-clamped resonant DC-Link inverter [42];
- Resonant inverter with minimum voltage stress [39];

Resonant Pole family:

- Auxiliary resonant pole inverter [43];
- Auxiliary resonant commutated pole inverter [43];

The Resonant DC-link inverter, depicted in Figure 3.3, was proposed by Deepakraj M. Divan in 1989 [41]. The basic idea is to introduce a resonance on the DC link of the inverter so that the voltage at the input of the inverter periodically drops to zero, therefore the configuration of the inverter can be changed under ZVS conditions. However, to control this type of converters, it is required an Integral Pulse Density Modulation (PMID) strategy since the switching can occur only at the instants at zero voltage, which are determined by the resonant frequency of the DC link [44]. Despite the potential advantages of this family of converters, too many drawbacks prevented its diffusion. In [45] [46] [47] is concluded that resonant DC link inverters, compared to traditional hard switched inverters, have a significantly higher harmonic distortion caused by the IPDM modulation. In addition, the peak voltage of the DC link is two times higher than the voltage of the DC link of a conventional inverter. Although auxiliary circuits can be used to reduce the peak voltage to 1.3-1.5 time the input voltage, the blocking capability of the transistor of the inverter (topologies in Figure 3.4 and Figure 3.5) is increased in comparison to a traditional hard switched converter. Furthermore, the power entirely passes through the resonant inductor of the DC link, thus reducing the efficiency and limiting the use of these converters only for low power applications.

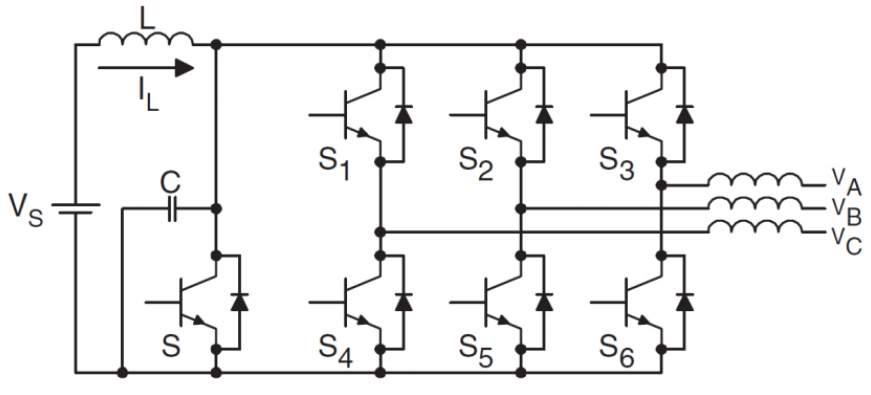


Figure 3.3 - Resonant DC-Link Inverter.

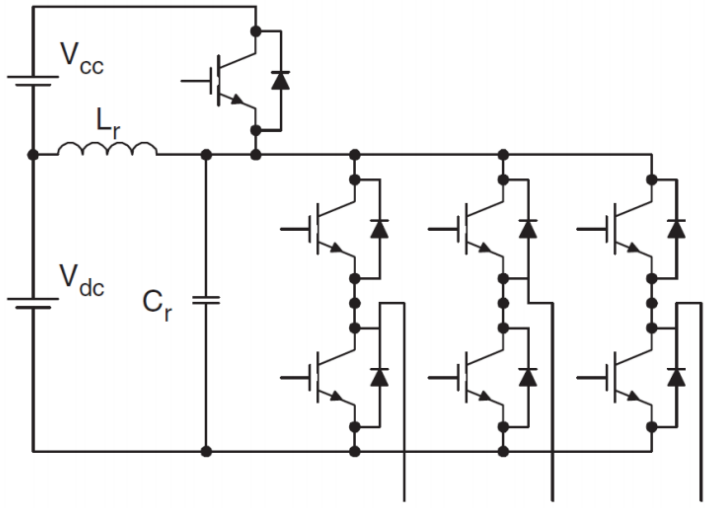


Figure 3.4 - Active-Clamped Resonant DC-Link Inverter.

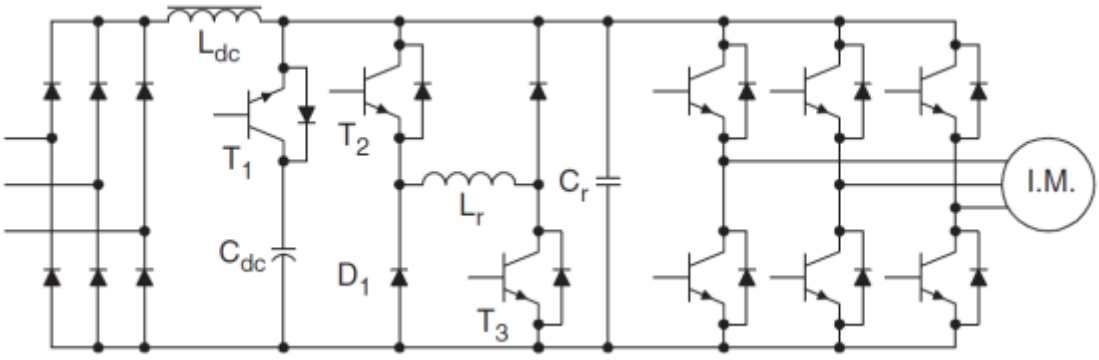


Figure 3.5 - Resonant Inverter with Minimum Voltage Stress.

The resonant pole family was proposed by Rik W. De Doncker in 1990 to overcome the limitations of the DC link converters [43]. The basic configuration, depicted in Figure 3.6, uses auxiliary resonant circuits on the load side of each inverter branch to force to zero the voltage whenever it is required to switch a transistor. The auxiliary branches are constituted of a bidirectional switch connected in series with an inductor, which ensures the zero current switching operation of the bidirectional switch and the zero voltage switching of the transistor of the main branch.

Differently from DC link inverters, this approach does not cause over voltage spikes higher than the DC link voltage, therefore the blocking voltage of the power switches equal to that of hard switched DC/AC converters. Furthermore, the full power of the system does not flow through the auxiliary circuits, making this converter suitable for high power applications.

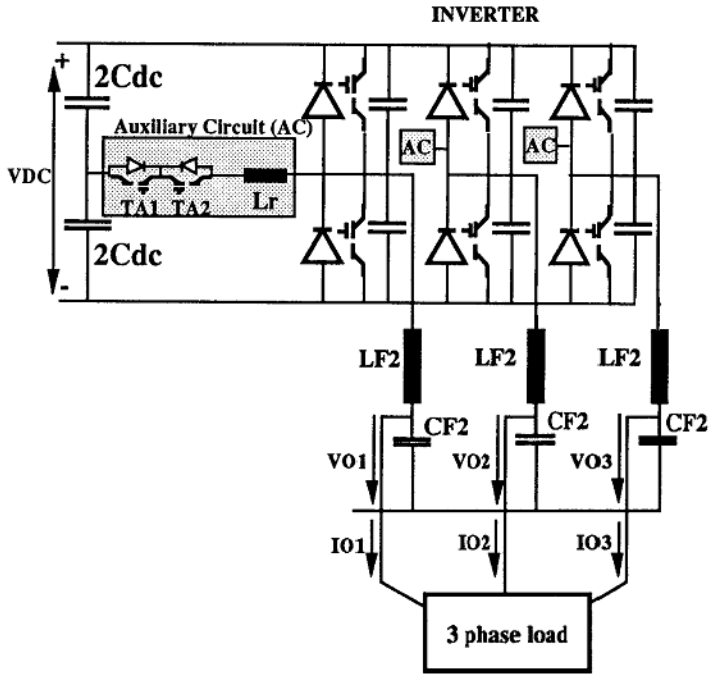


Figure 3.6 - ARCP DC to AC converter.

The control of the auxiliary branches, however, is very complicated since it depends on the amplitude and sign of the load current [43]. Several auxiliary circuit variations have been proposed to improve the efficiency of the first version of ARCP converter, to make the control easier and to reduce the current rating of the devices. Among them it is worth mentioning:

- Zero Current Transition converter (ZCT) [45];

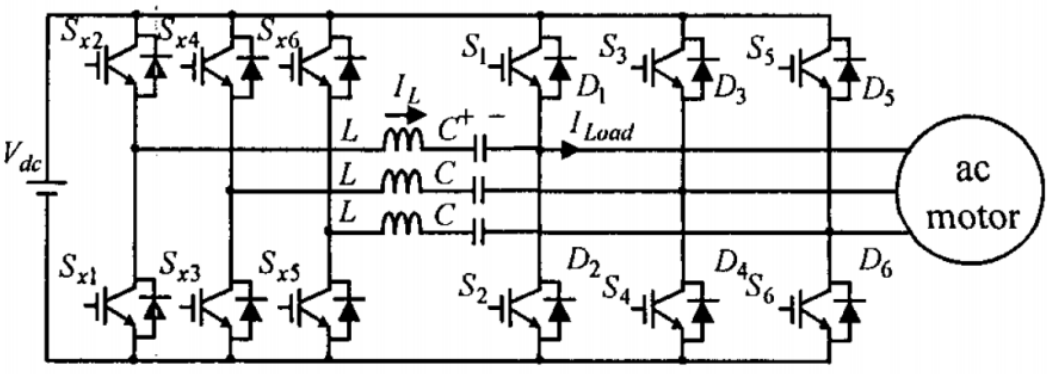


Figure 3.7 – Schematic of a three phase ZCT.

- Zero Voltage Transition with a Single Switch converter (ZVTSS) [45];

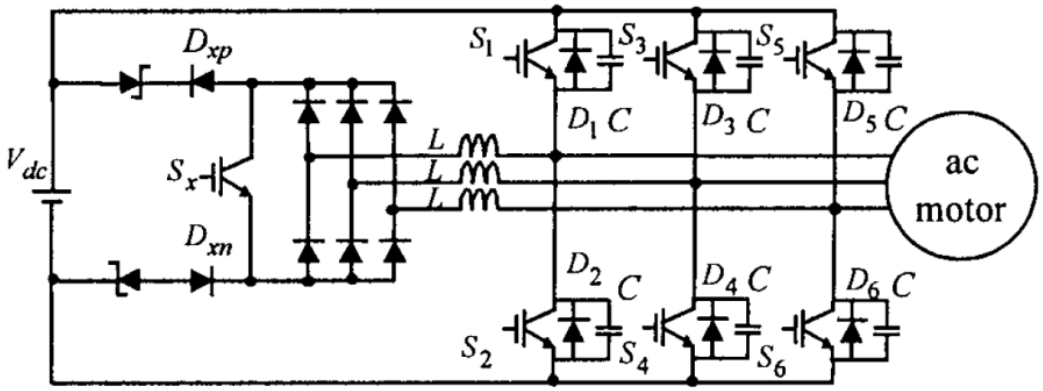


Figure 3.8 - Schematic of a three phase ZVTSS.

- Zero Voltage Transition with a Single Inductor converter (ZVTSI) [45];

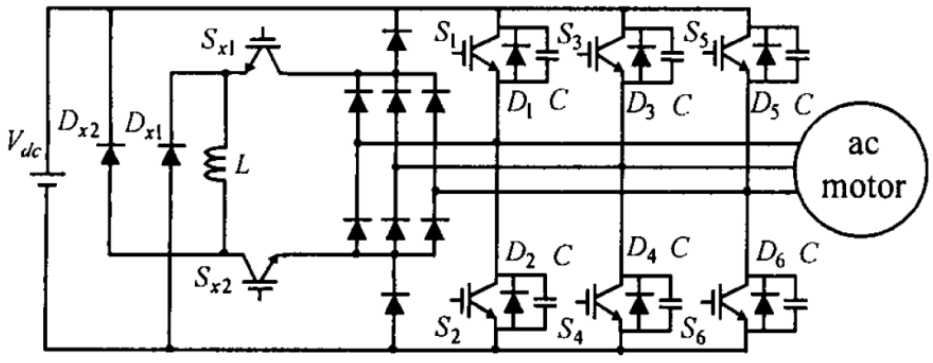


Figure 3.9 - Schematic of a three phase ZVTSI.

- Zero Voltage Transition with a Coupled Inductor converter (ZVTCI) [48];

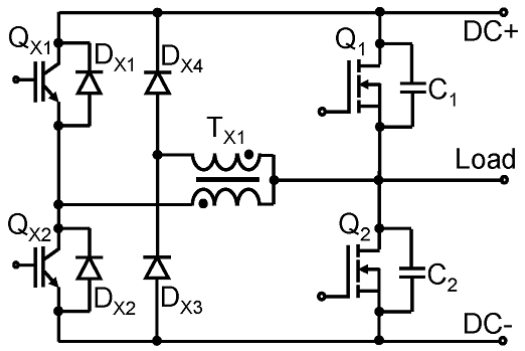


Figure 3.10 - Schematic of a ZVTCI inverter leg.

- Zero Voltage Transition with two Coupled Inductor converter (ZVT2CI) [49];

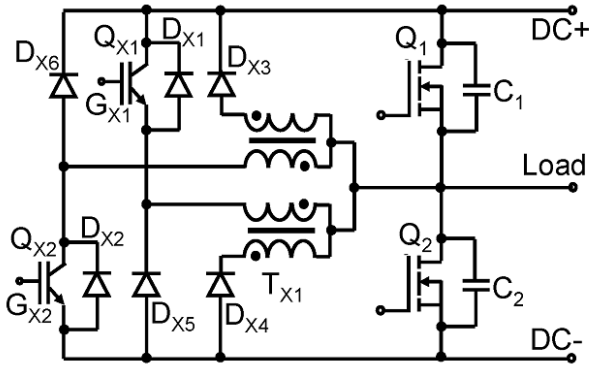


Figure 3.11 - Schematic of a ZVT2CI inverter leg.

The Zero Voltage Transition with two Coupled Inductor (ZVT2CI) is the latest evolution of the Resonant Pole family [49]. The detailed analytical model of this topology is presented in section 3.3.B whereas the design procedures of a 2 kW, 400 Vdc single phase converter are presented in section 3.3.C. An efficiency comparison between the soft switching converter and a hard switched counterpart using the latest transistor technology is presented in section 3.3.D.

3.3 Zero Voltage Transition Converter with two Coupled Inductors

Among the soft-switching inverter presented in section 3.2, in this thesis attention has been given to the auxiliary pole family due to the higher efficiency [45] and relatively simple control. The converter selected for a performance comparison with hard switched converters is the zero voltage transition converter with two coupled inductors in one resonant pole [49]. This topology solves the main drawbacks of the transformed-based ZVS converters, i.e., the saturation of the core of the inductors [48], by resetting the magnetizing current each switching cycle.

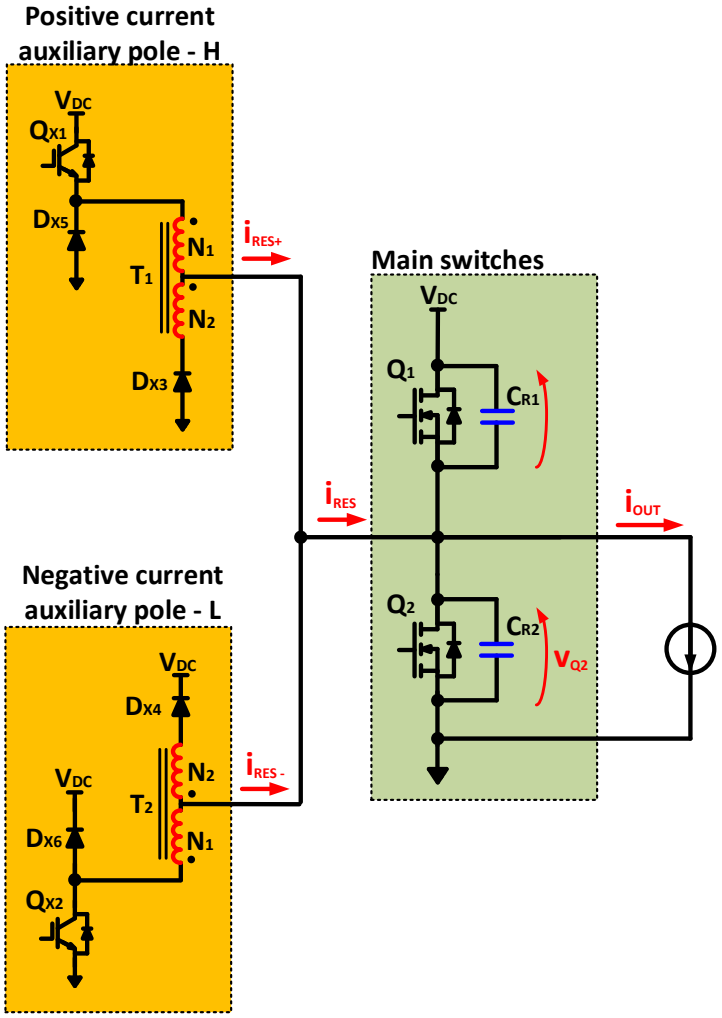


Figure 3.12 - Schematic of a ZVT2CI inverter leg feeding an highly inductive load, approximated by a current source.

3.3.A Topology description

A branch of a zero voltage transition converter with two couple inductor in one resonant pole is shown in Figure 3.12. As in a conventional inverter, two switches (Q_1 and Q_2) with freewheeling diodes (D_1 and D_2) form the main leg of the converter. Connected in parallel to the two main switches there are the resonance capacitors C_{R1} and C_{R2}, which play a key role to archive the zero-voltage turn-on of Q_1 and Q_2 and to reduce the turn-off losses. Two auxiliary branches are connected to the central point of the main leg. Each one consists of an autotransformer ATR, an auxiliary switch ($Q_{X1,2}$) and two auxiliary diodes ($D_{X3,4}$) and ($D_{X5,6}$). The auxiliary resonant current can be established by turning on the auxiliary switch, which conducts the resonant current through the respective coupled magnetics. The upper auxiliary branch takes part to the commutation only if the load current is positive while the second one operates only in case of commutation under negative load current. The switches of the main branch switch under zero voltage (ZVS) conditions, while the switches of the auxiliary branches under zero current (ZCS) conditions.

3.3.B Operating principle of the converter

In order to simplify the analysis and obtain an analytical description of the converter, the following assumptions have been made:

- power switches and diodes have zero forward voltage drop in the on-state and are open circuits in the off-state;
- the output capacitance of the transistors is negligible;
- diodes have no reverse recovery charge;
- the switching time of the power switches is zero, i.e., commutations are instantaneous;
- autotransformers and capacitors have zero losses;
- the load is highly inductive, then the load current can be considered constant over a switching cycle. Therefore, the load can be modelled as a DC current source.

The control adopted for the converter, originally proposed in [49], requires four independent PWM signals G_{X1}, G_{X2}, G_1 and G_2 to control the switches Q_{X1}, Q_{X2}, Q_1 and Q_2 respectively.

G_{X1} and G_{X2} are complementary signals with a dead time in between them, exactly as they were the gate signals of a half bridge converter.

The turn-on rising edge of the main switch gate signal G_1 is controlled adaptively by a zero voltage detector logic, which checks the drain-source voltage of Q_1 and ensures soft switching turn-on under any load current and any source voltage condition. Instead, the turn-off falling edge of G_1 is controlled by a fixed time delay from the falling edge of the PWM command G_{X1}, the delay time ensures the complete reset of the magnetizing current of the transformer T_1 every switching period.

In the same way, the turn ON rising edge of the main switch gate signal G_2 is controlled adaptively by a zero voltage detector logic, which checks the drain-source voltage of Q_2 and ensures soft switching turn ON. The turn OFF falling edge of G_2 is controlled by a fixed time delay from the falling edge of the PWM command G_{X2}, the delay time ensures the complete reset of the magnetizing current of the transformer T_2 every switching cycle.

In the analysis of a period, it is assumed that the load current is positive. Therefore, in the following description the auxiliary pole *L*, which operates only in case of negative output current, is not considered. The circuit considered in the next analysis is re-drawn in Figure 3.13.

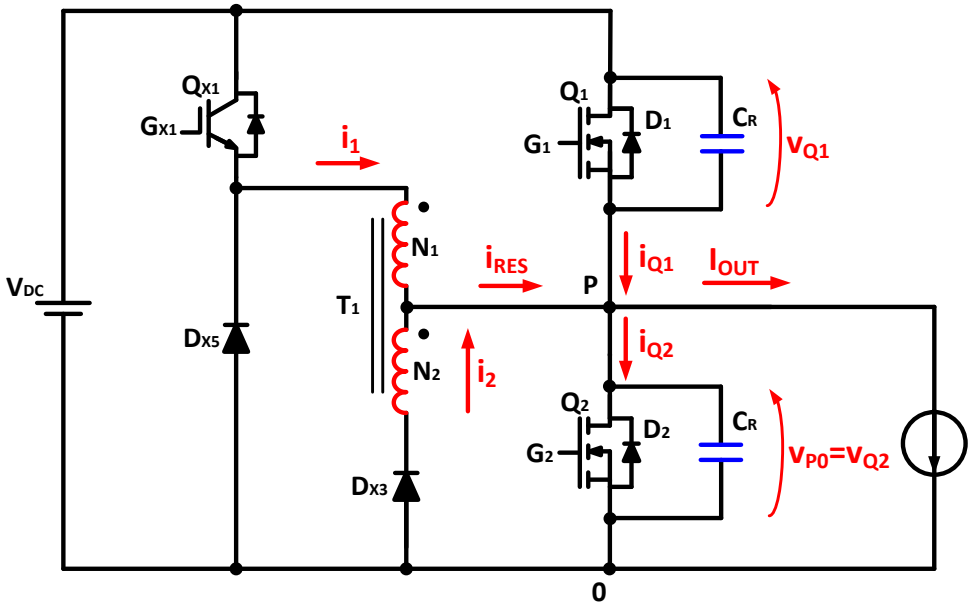


Figure 3.13 - Schematic of the ZVT2CI converter, considering only the main bridge and the positive current auxiliary pole.

One operating cycle of the converter can be subdivided in nine phases as shown in Figure 3.14, each phase can be analyzed using an equivalent circuit of the converter. The duration of each phase has been increased for the sake of clarity. The sign convention for voltages and currents follows the notation of Figure 3.13.

The stating point of the analysis is the end of the interval [t_0-t_1], which corresponds to the freewheeling circulation of the output current through the diode D_2.

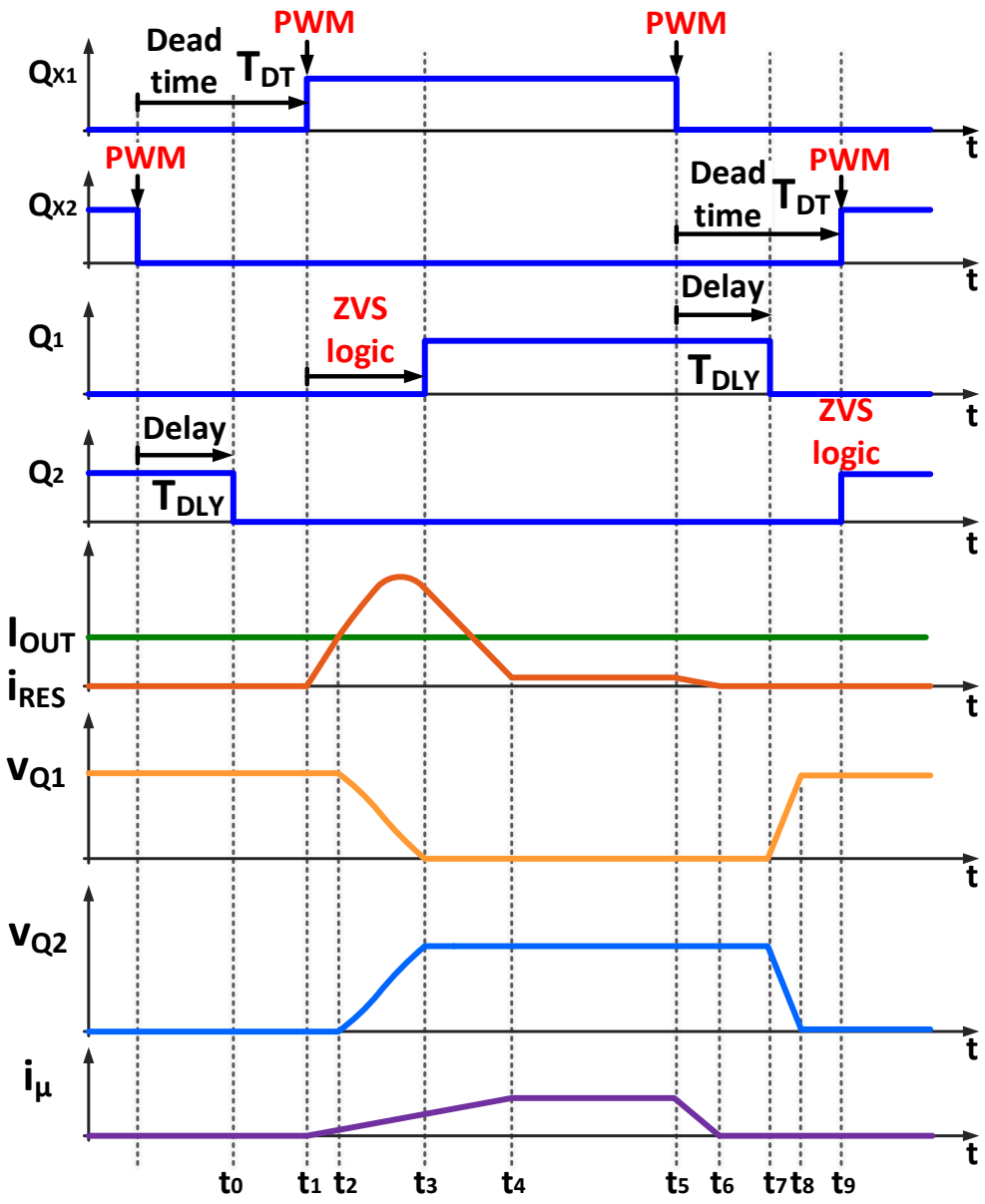


Figure 3.14 - Timing diagram of the ZVT2CI inverter.

Phase 0 - [t_0, t_1]

At $t = t_0$, the main switch Q_2 is turned off under ZVS conditions, the current I_{OUT} that was flowing through the channel of the MOSFET (third quadrant operation) is diverted to the body diode D_2. Therefore:

$$i_{Q2} = -I_{OUT}. \tag{3.1}$$

The turn-off action does not change the output voltage and current waveforms. All the gate signals are low and the resonant current i_{RES} is zero.

The resonant capacitors across Q_1 and Q_2 respectively are fully charged and discharged:

$$v_{Q1} = V_{DC} \tag{3.2}$$

$$v_{Q2} = 0\,. \tag{3.3}$$

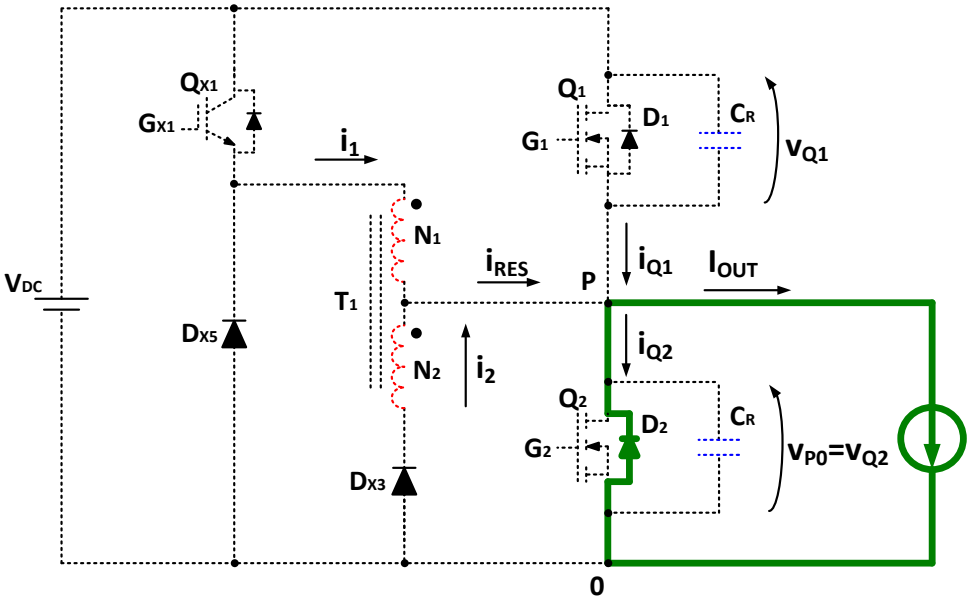


Figure 3.15 –Detail of the ZVT2CI converter during time [t_0, t_1].

Phase 1 - [t_1, t_2]

At $t = t_1$, the auxiliary switch Q_{X1} is turned-on by the PWM signal G_{X1}. The input voltage V_{DC} is applied to the primary side of the autotransformer and then the diode D_{X3} is forced in conduction mode, the components that take part to this phase are highlighted in Figure 3.16.

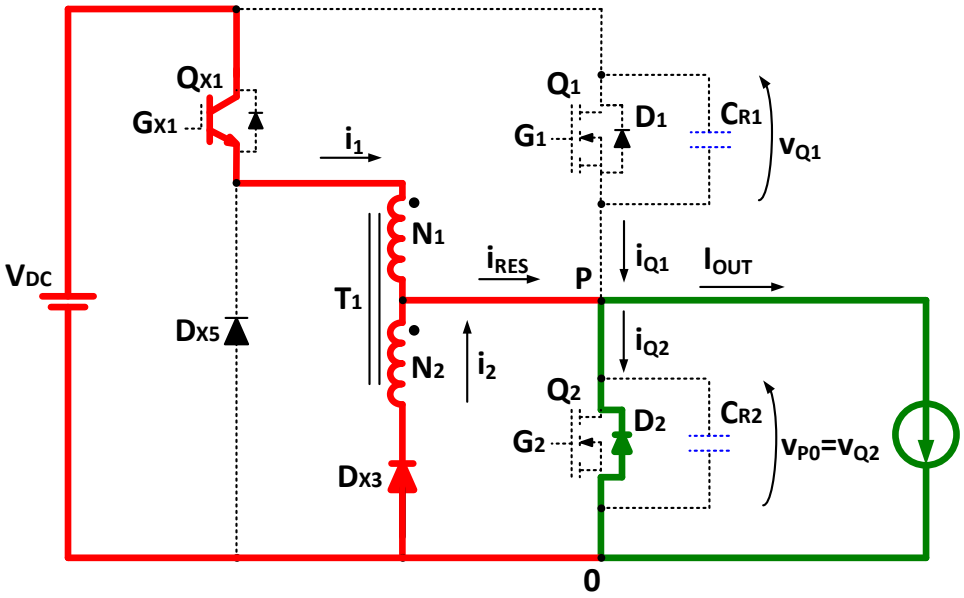


Figure 3.16 - Detail of the ZVT2CI converter during time [t_1, t_2].

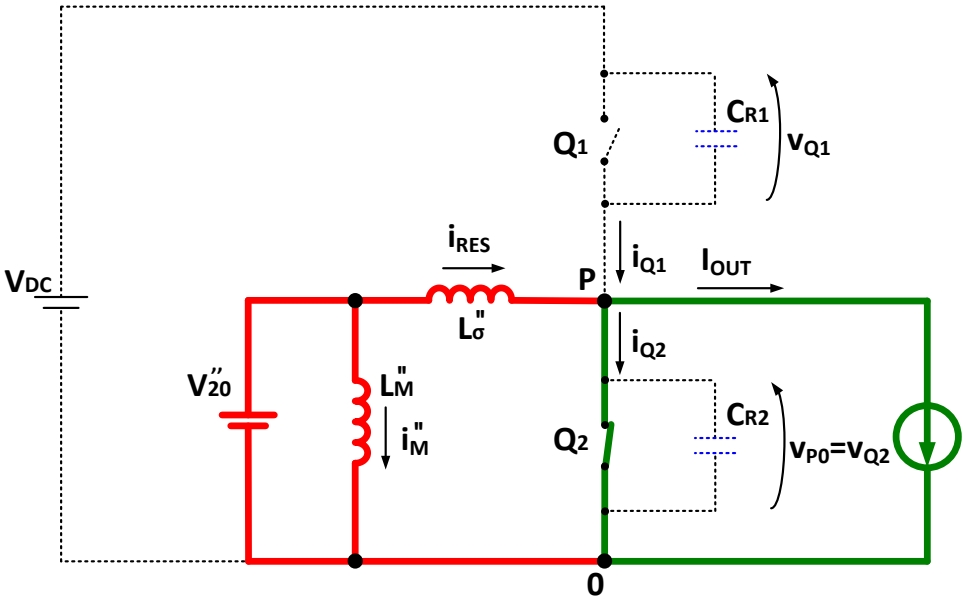


Figure 3.17 – Equivalent circuit of the ZVT2CI converter during time [t_1, t_2].

To simplify the analysis, the equivalent circuit of the auto transformer depicted in Figure 3.17 is introduced. The equivalent electrical parameters of the autotransformer, i.e., the no-load voltage V_{20}'', the magnetizing inductance L_M'' and leakage inductance L_σ'', are referred to the secondary side. The autotransformer behaves then like a DC voltage source of amplitude

$$V_{20}'' = \frac{N_2}{N_1 + N_2} V_{DC} = kV_{DC}. \tag{3.4}$$

Initially, the load current I_{OUT} is freewheeling through D_2, keeping the pole voltage v_{P0} to zero. The secondary side of the autotransformer is then short circuited and voltage kV_{DC} is completely applied to the leakage inductance L''_{σ} and to the magnetizing inductance L''_{M}.

Let us define $t' = t - t_1$. The resonant current i_R rises linearly as follow:

$$i_R = \frac{kV_{DC}}{L''_{\sigma}} t'. \tag{3.5}$$

Simultaneously, a magnetizing current i''_M is established:

$$i''_M = \frac{kV_{DC}}{L''_M} t'. \tag{3.6}$$

Phase 1 ends at $t = t_2$, when the resonant current i_R reaches the value of the output current I_{OUT} and the diode D_2 is forced to turn-off. Therefore, phase 1 lasts:

$$T_{12} = t_2 - t_1 = \frac{L''_{\sigma}\, I_{OUT}}{kV_{DC}}. \tag{3.7}$$

The real currents in the windings of the autotransformer can be calculated as follow:

$$i_1 = k(\, i_{RES} + i''_M\,) \tag{3.8}$$

$$i_2 = \, i_{RES} - i_1 = (1-k) i_{RES} - k i''_M\,. \tag{3.9}$$

It can be seen from equations (3.10) and (3.11) that the resonant current i_{RES} is shared between the transistor Q_{X1} and the diode D_{X3}.

Phase 2 - [t_2, t_3]

At $t = t_2$, the resonant current i_{RES} exceeds the load current: the diode D_2 is forced in blocking mode and the resonant transition that leads to the ZV turn-on of Q_1 begins. The excess of current $i_{RES} - I_{OUT}$ charges and discharges the resonant capacitors C_{R2} and C_{R1} and the pole voltage V_{P0} start rising.

The Figure 3.18 illustrates the topological configuration of the circuit of phase 2, while Figure 3.19 shows the equivalent circuit.

If we assume that the resonant capacitor C_{R1} and C_{R2} have the same capacity C_R, then the circuit of Figure 3.19 can be further simplified as in Figure 3.20.

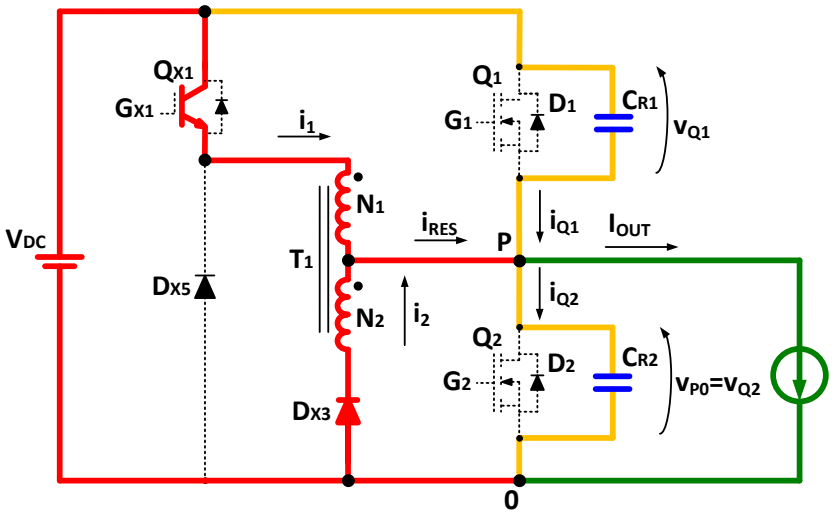


Figure 3.18 - Detail of the ZVT2CI converter during time [t_2, t_3].

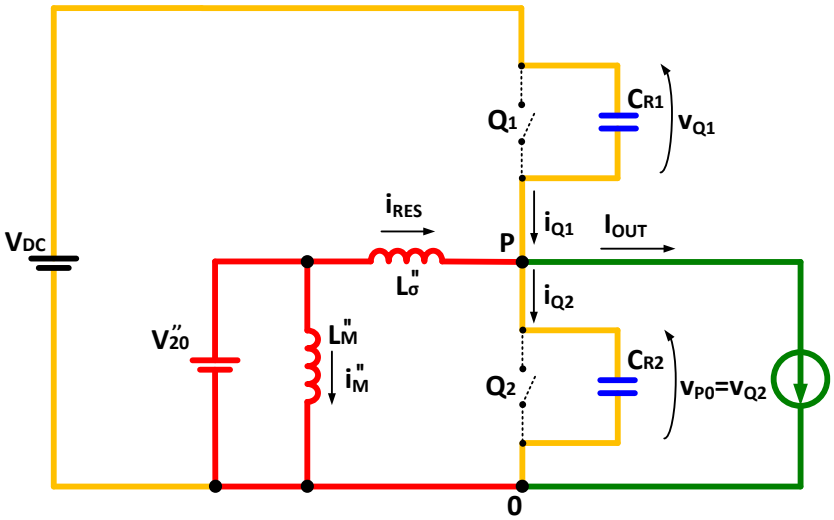


Figure 3.19 - Equivalent circuit of the ZVT2CI converter during time [t_2, t_3].

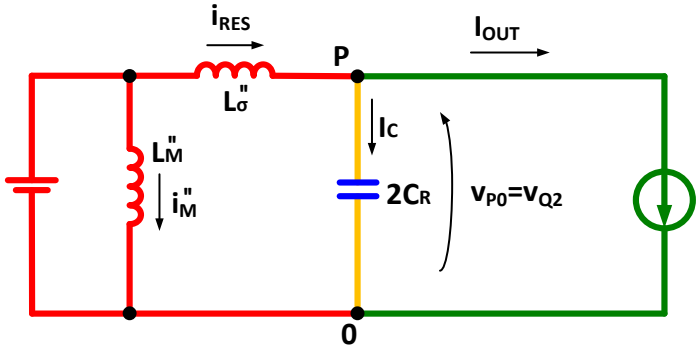


Figure 3.20 - Equivalent circuit of the ZVT2CI converter during time [t_2, t_3].

Let us define $t' = t - t_2$. The following differential equations can be written:

$$\frac{di_{RES}}{dt'} = \frac{d(i_c + I_{OUT})}{dt} = \frac{di_c}{dt'} \tag{3.10}$$

$$kV_{DC} - L''_{\sigma}\frac{di_c}{dt} - v_{P0} = 0 \tag{3.11}$$

$$i_c = 2C_R\frac{dv_{P0}}{dt'}. \tag{3.12}$$

Equations (3.10), (3.11) and (3.12) can be combined to obtain a second order differential equation:

$$\frac{d^2v_{P0}}{dt'^2} + \frac{1}{2C_R}v_{P0} = \frac{1}{2C_RL''_{\sigma}}kV_{DC}. \tag{3.13}$$

The solution of (3.13) for the given initial conditions

$$v_{P0}|_{t'=0} = 0 \tag{3.14}$$

$$\left.\frac{dv_{P0}}{dt'}\right|_{t'=0} = \left.\frac{i_c}{2C_R}\right|_{t'=0} = \left.\frac{i_{RES} - I_{OUT}}{2C_R}\right|_{t'=0} = 0 \tag{3.15}$$

is

$$v_{P0} = kV_{DC}[1 - \cos(\omega_R t')] \tag{3.16}$$

where

$$\omega_R = \frac{1}{\sqrt{2C_RL''_{\sigma}}} \tag{3.17}$$

is the natural resonant frequency of the L-C series circuit. The equation (3.16) states that the pole voltage rises following a cosine shape evolution, whose peak voltage is:

$$V_{P0_{MAX}} = 2kV_{DC}. \tag{3.18}$$

The voltages across Q_1 and Q_2 are obtained from v_{P0} as follows:

$$v_{Q_1} = V_{DC} - v_{P0} = \mathrm{V_{DC}} - kV_{DC}[1 - \cos(\omega_R t')] \tag{3.19}$$

$$v_{Q_2} = v_{P0} = kV_{DC}[1 - \cos(\omega_R t')]. \tag{3.20}$$

The time evolution of v_{Q_1} and $v_{Q_2}$for several values of k are depicted in Figure 3.21. If the turn ratio k of the autotransformer is greater than 0.5, the voltage $v_{Q_2} = v_{P0}$ could rise

above V_{DC}. Actually, the freewheeling diode D_1 of the to switch Q_1 prevents the pole voltage to be greater than the input voltage, therefore v_{P0} is clamped to V_{DC}. In this condition the ZV logic of the upper main switch turns Q_1 on, since V_{Q1} is zero, archiving a zero switching losses commutation.

The autotransformer turn ratio k must be strictly greater than 0.5 to obtain a ZVS transition. Practically, k is selected between 0.55 and 0.6 in order to ensure a safe operation margin, since the real peak of V_{P0} during the resonant transition is reduced by the equivalent series resistance in the resonant loop, which includes the resistance of the transformer and the forward voltage drop on transistors and diodes.

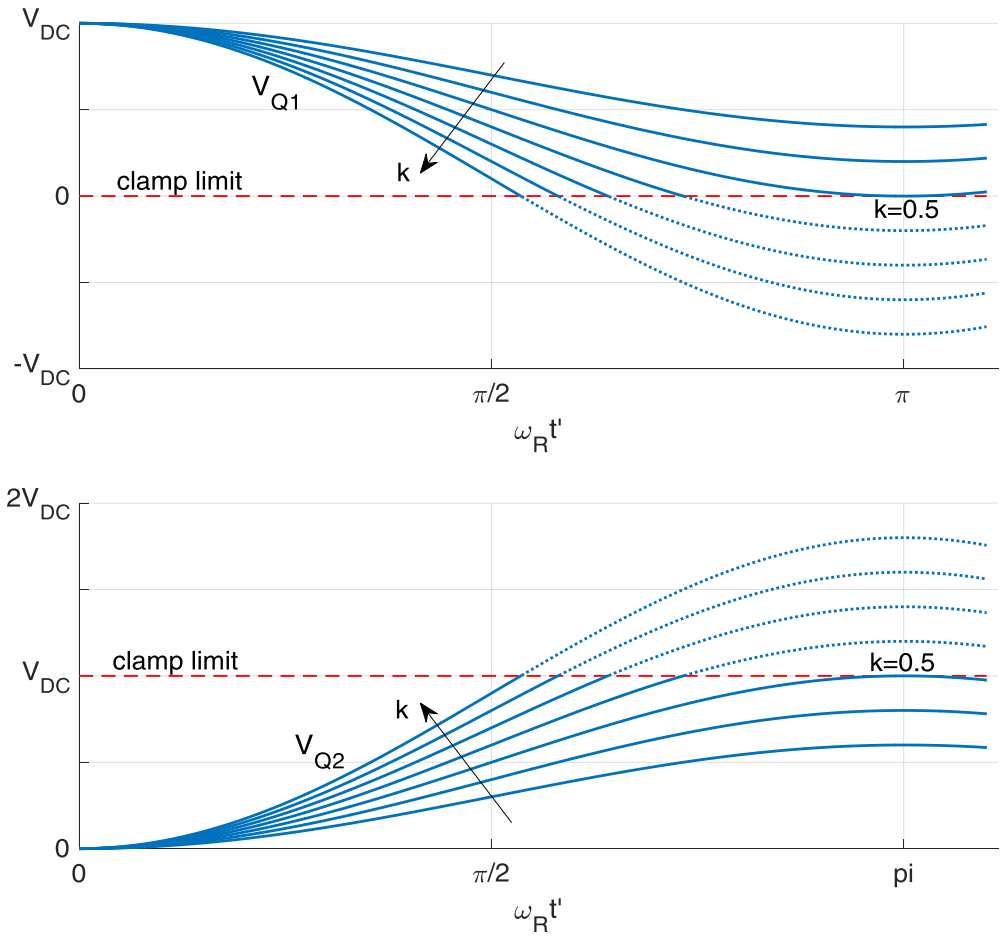


Figure 3.21 – Resonant transition of voltages V_{Q1} and V_{Q2} during time [t_2, t_3].

Assuming that $k > 0.5$, phase 2 ends when at $t = t_3$, when v_{PO} reaches V_{DC}. The duration of phase 2 can be obtained by assuming $v_{PO} = \mathrm{V_{DC}}$ in (3.16):

$$T_{23} = t_3 - t_2 = \frac{1}{\omega_R}\cos^{-1}\left(\frac{k-1}{k}\right). \tag{3.21}$$

Thus, the turn-on delay time between the main switch Q_1 and the auxiliary Q_{X1} switch can be obtained as follows:

$$t_3 - t_1 = \frac{L''_\sigma\, I_{OUT}}{kV_{DC}} + \frac{1}{\omega_R}\cos^{-1}\left(\frac{k-1}{k}\right). \tag{3.22}$$

This expression indicates that the delay time is variable and dependent on the load current. Therefore, a ZV detector is required to automatically adapt the turn-on of Q_1 to different load and source conditions [50].

The resonant current i_{RES} can be expressed as follows:

$$i_{RES} = i_C + I_{OUT} = 2C_R\frac{dv_{P0}}{dt'} + I_{OUT} = \frac{kV_{DC}}{Z_R}\sin(\omega_R t') + I_{OUT} \tag{3.23}$$

where Z_R is the resonant impedance:

$$Z_R = \sqrt{\frac{L''_\sigma}{2C_R}}. \tag{3.24}$$

The peak of the resonant current happens when v_{P0} is equal to kV_{DC}, because:

$$\frac{di_{RES}}{dt} = \frac{kV_{DC} - v_{P0}}{L''_\sigma}. \tag{3.25}$$

Assuming $\frac{di_{RES}}{dt} = 0$ the peak value of i_R can be obtained:

$$I_{RES_{MAX}} = I_{OUT} + \frac{kV_{DC}}{Z_R}. \tag{3.26}$$

It can be seen that $I_{RES_{MAX}}$ is greater than I_{OUT}, but the resonant contribution that takes part to the charge and discharge of C_{R1} and C_{R2} is constant for any load current. At the end of phase 2, the resonant current reaches the following value:

$$I_{RES-t_3} = I_{OUT} + \frac{kV_{DC}}{Z_R}\sin(\omega_R T_{23}). \tag{3.27}$$

During the entire phase 2 the voltage kV_{DC} is applied to L''_M, so the magnetizing current increases linearly and in t_3 it reaches the value:

$$I''_{M-t_3} = \frac{kV_{DC}}{L''_M}(T_{12} + T_{23}). \tag{3.28}$$

Phase 3 - [t_3, t_4]

At $t = t_3$, the capacitor C_{R1} is fully discharged, while the capacitor C_{R2} is charged at the voltage V_{DC}. Diode D_1 prevents the pole voltage V_{P0} from rising above V_{DC} and conducts the excess current $i_R - I_{OUT}$ back to the source. As long as the resonant current is greater than the output current, D_1 is forward biased and V_{Q1} is clamped to zero. Therefore, switch Q_1 can be turned-on under ZV conditions. The configuration of the converter during phase 3 is depicted in Figure 3.22, while Figure 3.23 shows the equivalent circuit.

Let us define $t' = t - t_3$. The resonant current decreases linearly subjected to the voltage $(1-k)V_{DC}$:

$$i_{RES} = I_{RES-t_3} - \frac{(1-k)V_{DC}}{L''_\sigma} t'. \tag{3.29}$$

The ZV logic circuitry must detect the ZV condition and turn Q_1 on before i_{RES} falls below the load current, otherwise the ZV switching condition is lost. The time window for the ZV turn-on can be evaluated introducing (3.26) into (3.29) and solving t' for $i_{RES} = I_{OUT}$:

$$\Delta T_{ZVS} = \frac{1}{\omega_R}\frac{k}{1-k}\sin(\omega_R T_{23}) = \frac{1}{\omega_R}\sqrt{\frac{2k-1}{(1-k)^2}}. \tag{3.30}$$

The equation (3.30) states that the ZV time window is an intrinsic property of the converter, which depends only on the transformer turn ratio, on the transformer leakage inductance and on the resonant capacitors.

When switch Q_1 is turned on, the current i_{Q1} that was flowing in the diode D_1 is diverted to the channel of Q_1. After the time ΔT_{ZVS}, the current of Q_1 becomes positive and continues to increase linearly, diverting the load current from the auxiliary circuit to the main switch:

$$i_{Q1} = i_{RES} - I_{OUT}\,. \tag{3.31}$$

The magnetizing current keeps rising since kV_{DC} is still applied to L''_M:

$$i''_M = I''_{M-t_3} + \frac{kV_{DC}}{L''_M} t'. \tag{3.32}$$

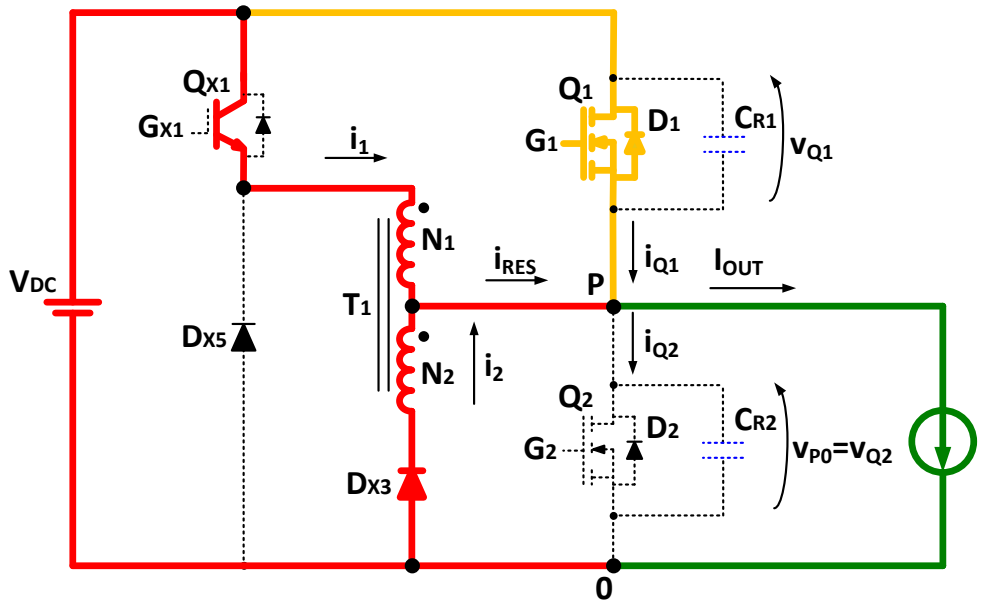


Figure 3.22 – Detail of the ZVT2CI converter during time [t_3, t_4].

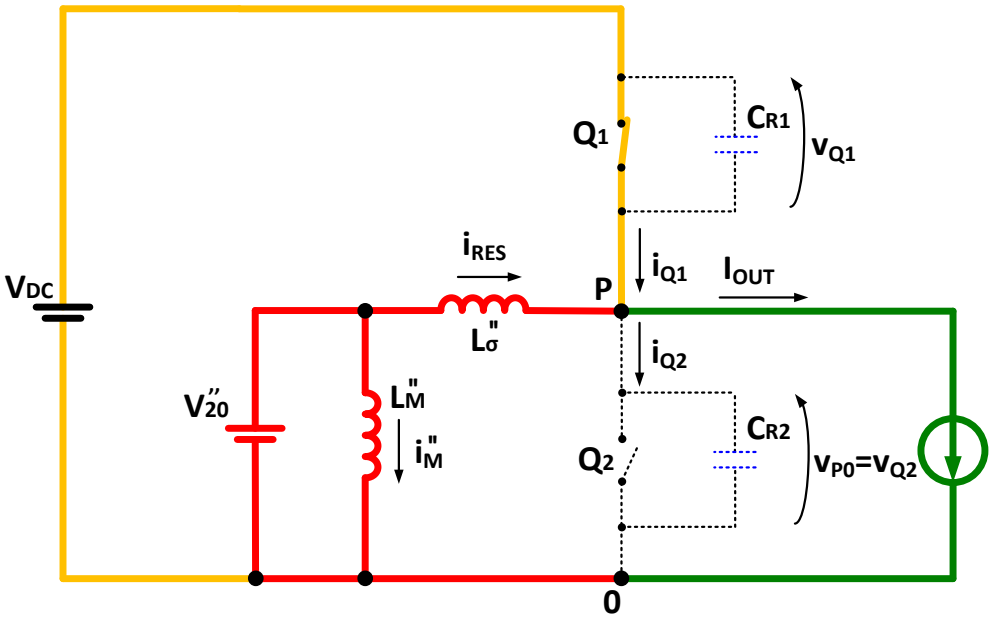


Figure 3.23 - Equivalent circuit of the ZVT2CI converter during time [t_3, t_4].

Phase 3 ends when the current i_2 that flows through D_{X3} falls back to zero, forcing the turn-off of the diode. By using (3.8), (3.29) and (3.32) the current i_2 can be written as:

$$i_2 = (1-k)\left(I_{RES-t_3} - \frac{(1-k)V_{DC}}{L''_\sigma}t'\right) - k\left(I''_{M-t_3} + \frac{kV_{DC}}{L''_M}t'\right). \qquad (3.33)$$

The duration of phase 3 can be obtained imposing $i_2 = 0$ and solving for $t' = T_{34}$:

$$T_{34} = t_4 - t_3 = \frac{(1-k)I_{RES-t_3} - kI''_{M-t_3}}{V_{DC}\left(\frac{k^2}{L''_M} + \frac{(1-k)^2}{L''_\sigma}\right)}. \tag{3.34}$$

Since in a transformer the magnetizing inductance is much larger than the leakage inductance, (3.34) can be approximated as follows:

$$T_{34} \cong \frac{L''_\sigma}{(1-k)V_{DC}} I_{RES-t_3} \ . \tag{3.35}$$

From time t_1 to t_4 the transformer is supplied. Therefore, the magnetizing current i''_M rises linearly and its final value in t_4 can be calculated as:

$$I''_{M-t_4} = \frac{kV_{DC}}{L''_M}(T_{12} + T_{23} + T_{34}) \ . \tag{3.36}$$

It has been shown that at the end of phase 3 the current i_2 has dropped to zero. Figure 3.24 helps to understand the relations between the currents of the transformer in t_4. By using (3.8), (3.9) and (3.33),the resonant current I_{RES-t_4} and the primary current of the autotransformer I_{1-t_4} can be calculated as:

$$I_{1-t_4} = I_{RES-t_4} = \frac{k}{1-k} I''_{M-t_4} \ . \tag{3.37}$$

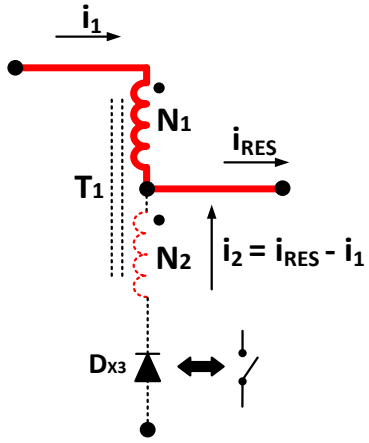


Figure 3.24 – Relation between the resonant current and the currents in the windings of the autotransformer.

Phase 4 - [t_4, t_5]

Phase 4 starts in $t = t_4$ when the current i_2 of the transformer falls to zero and the diode D_{X3} is forced to turn-off therefore, the secondary winding becomes an open circuit. Therefore, the autotransformer behaves just like an inductor , which is formed by N_1 primary turns wounded around the core of the transformer. The equivalent inductance L_{N1} can be calculated as follows:

$$L_{N1} = L''_M \left(\frac{N_1}{N_2}\right)^2 = L''_M \left(\frac{1-k}{k}\right)^2 . \tag{3.38}$$

It can be seen in Figure 3.25 and in the equivalent circuit of Figure 3.26 that a low resistance loop is formed by Q_{X1} (which is still on), Q_1 and the primary winding N_1. Therefore the current $I_{1-t_4} = I_{RES-t_4}$ calculated in (3.37) can freewheel without attenuation, since the voltage applied to L_{N1} is zero. The current carried by Q_1 is:

$$i_{Q1} = I_{OUT} - I_{RES-t_4} \cong I_{OUT} . \tag{3.39}$$

Phase 4 lasts as long as the PWM signal of $G_{X1}$is high.

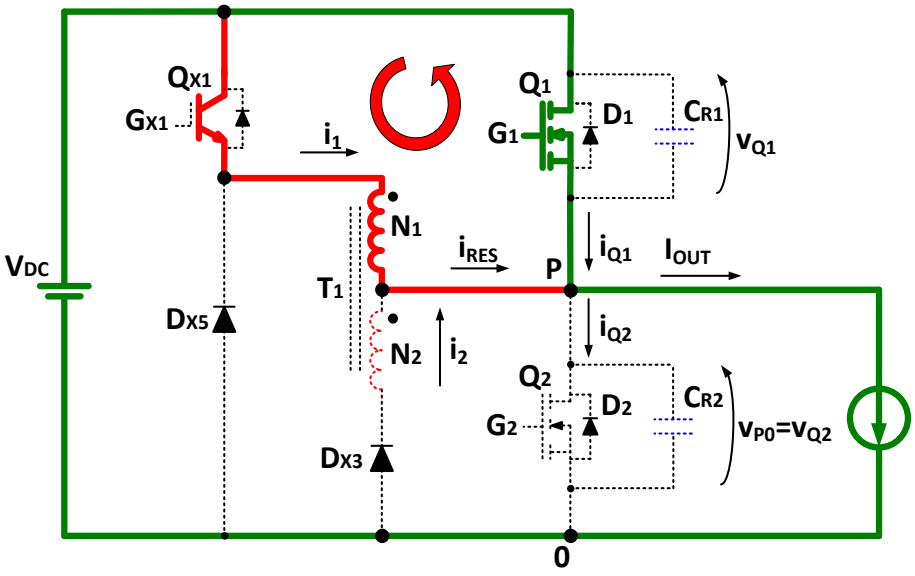


Figure 3.25 - Detail of the ZVT2CI converter during time [t_4, t_5].

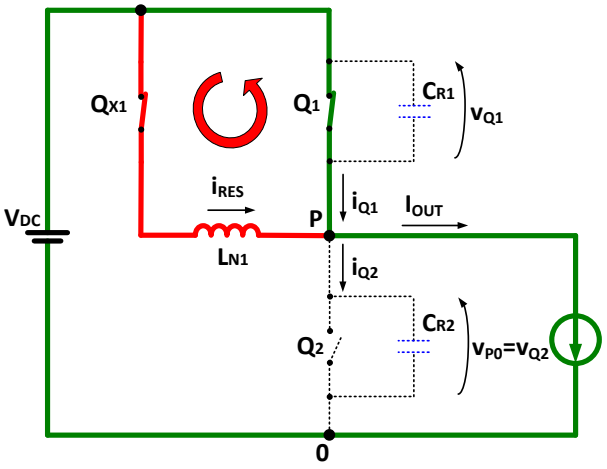


Figure 3.26 - Equivalent circuit of the ZVT2CI converter during time [t_4, t_5].

Phase 5 - [t_5, t_6]

At $t = t_5$, the PWM signal G_{X1} goes to zero and turns-off the switch Q_{X1}. At the same time the current i_1, since is flowing through the inductor L_{N1}, forces the turn on of the diode D_{X5}.

Therefore, it begins the resetting phase of the current i_{RES}.

Let us define $t' = t - t_5$:

$$i_{RES} = I_{RES-t_4} - \frac{V_{DC}}{L_{N1}} t'. \tag{3.40}$$

Figure 3.27 illustrates the topological configuration of the circuit, while Figure 3.28 shows the equivalent circuit.

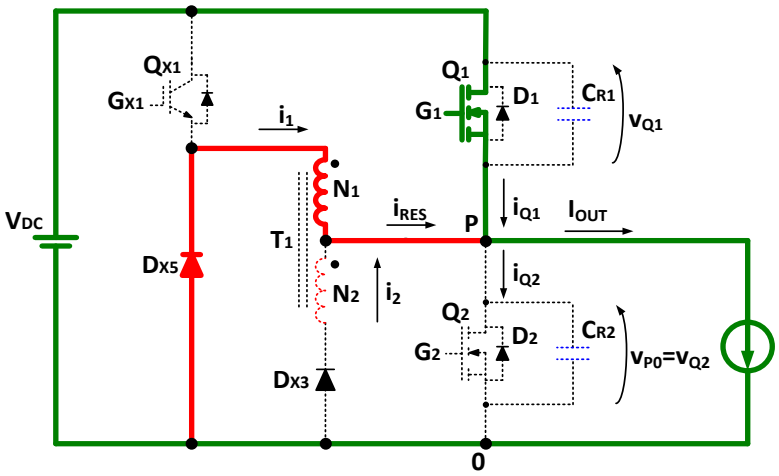


Figure 3.27 - Detail of the ZVT2CI converter during time [t_5, t_6].

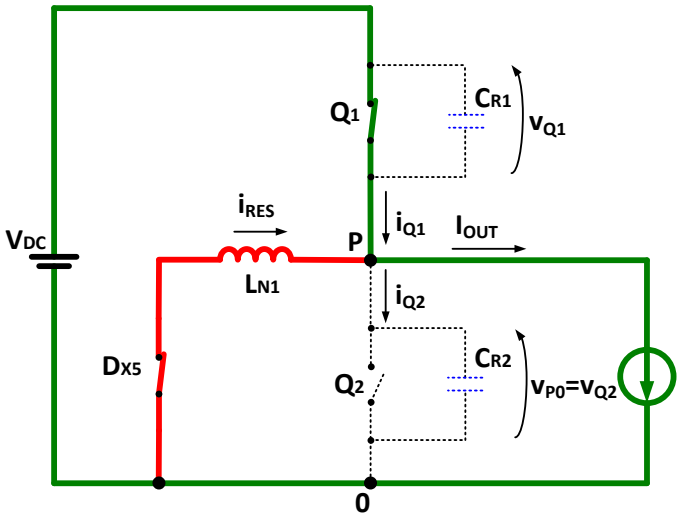


Figure 3.28 - Equivalent circuit of the ZVT2CI converter during time [t_5, t_6].

During the resetting of i_2, the diode D_{X3} is reverse biased by the voltage induced in N_2:

$$v_{DX3} = V_{DC} + \frac{N_2}{N_1} V_{DC} = \frac{1}{1-k} V_{DC} \,. \tag{3.41}$$

For values of turn ratio greater than 0.5, it appears that D_{X3} has to withstand a voltage greater than $2V_{DC}$. This phenomenon must be taken seriously into account during the design of the converter.

Phase 5 ends at $t = t_6$, when the resonant current i_R falls to zero and the diode D_{X5} is forced to turn-off. Therefore, the duration of phase is:

$$T_{56} = t_6 - t_5 = \frac{L_{N1} I_{RES-t_4}}{V_{DC}} . \tag{3.42}$$

The delay time T_{DLY} introduced between the falling edges of the PWM signals G_{X1} and G_1 (see Figure 3.14) must guarantee the complete reset of the resonant current each switching cycle. An incomplete reset leads to the bias of i_{RES}, which increases cycle by cycle, leading to the saturation of the autotransformer and to the possible failure of the converter. Therefore, the delay time must greater than T_{56} calculated at the maximum output current of the converter:

$$T_{DLY} > T_{56}|_{I_{OUT\,MAX}} \,. \tag{3.43}$$

Phase 6 - [t_6, t_7]

Phase 6 starts at $t = t_6$ when the resonant current has been fully reset and the output current flows only through switch Q_1.

Figure 3.29 illustrates the topological configuration of the circuit.

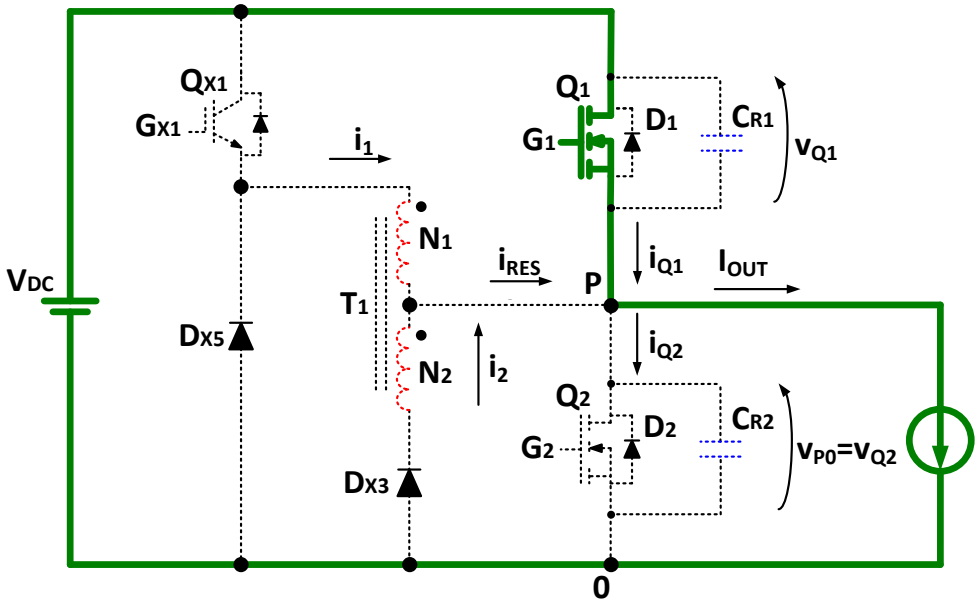


Figure 3.29 - Detail of the ZVT2CI converter during time [t_6, t_7].

Phase 7 - [t_7, t_8]

At $t = t_7$, the main switch Q_1 is turned-off by the PWM signal G_1. Ideally, Q_1 interrupts instantly I_{OUT}, which continues to flow through the capacitor C_{R1}. Therefore, C_{R1} is being charged by I_{OUT} while C_{R2} is being discharged. Figure 3.30 illustrates the configuration of the circuit during phase 7.

Let us define $t' = t - t_5$, the pole voltage can be expressed as:

$$v_{P0} = V_{DC} - \frac{I_{OUT}}{2C_R} t'. \tag{3.44}$$

The pole voltage decreases linearly to zero, with a slope proportional to the load current, phase 7 ends when v_{P0} reaches zero.

$$T_{78} = t_8 - t_7 = \frac{2C_R V_{DC}}{I_{OUT}}. \tag{3.45}$$

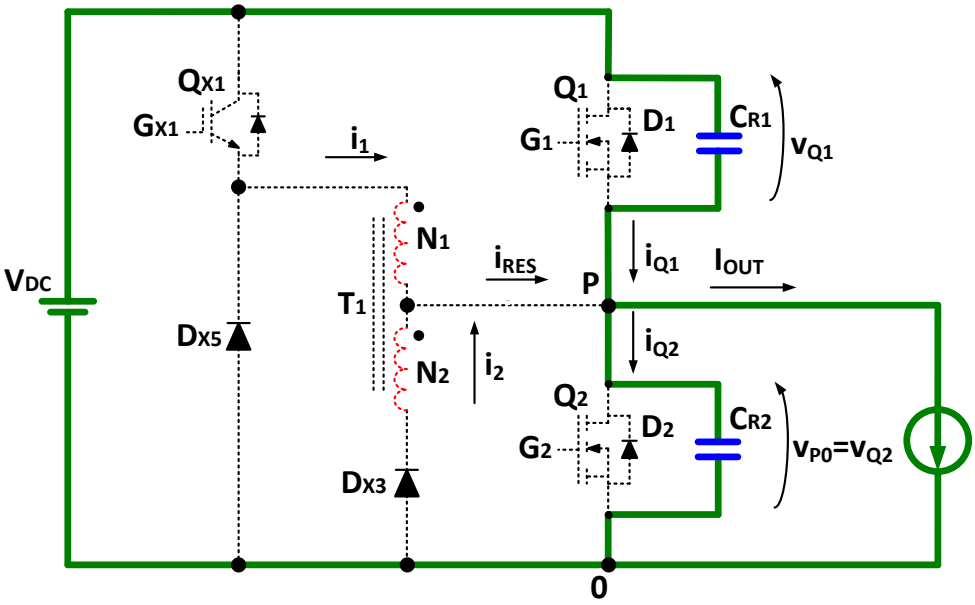


Figure 3.30 - Detail of the ZVT2CI converter during time [t_7, t_8].

Phase 8 - [t_8, t_9]

At $t = t_8$ the pole voltage v_{P0} reaches zero, diode D_2 is forced to turn-on and the load current I_{OUT} freewheels through D_2 (see Figure 3.31).

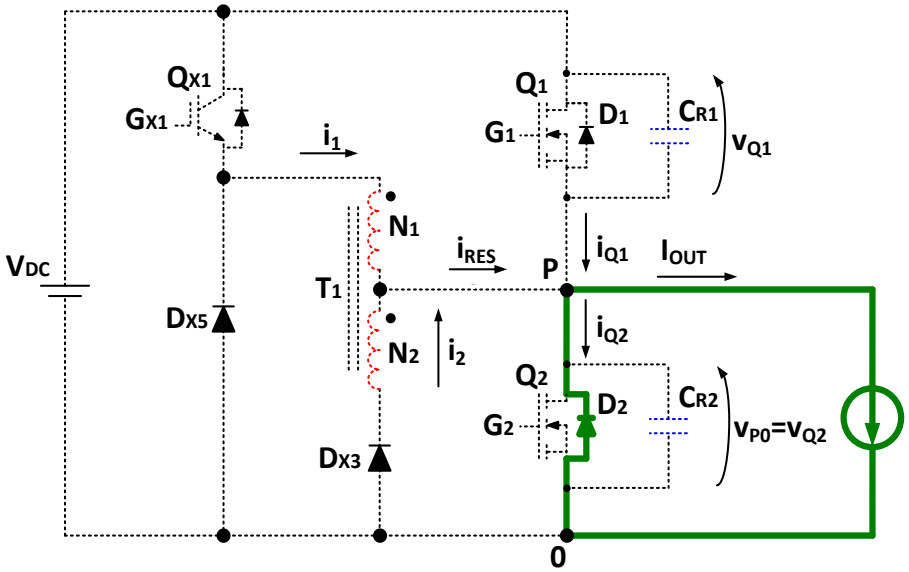


Figure 3.31 - Detail of the ZVT2CI converter during time [t_8, t_9].

In this condition, since D_2 keeps the voltage v_{Q2} to zero, the ZV logic can turn-on Q_2 without the generation of switching losses. Then, the current I_{OUT} that was flowing through diode D_2 is diverted to the channel of Q_2, resulting in a third quadrant operation as depicted in Figure 3.32.

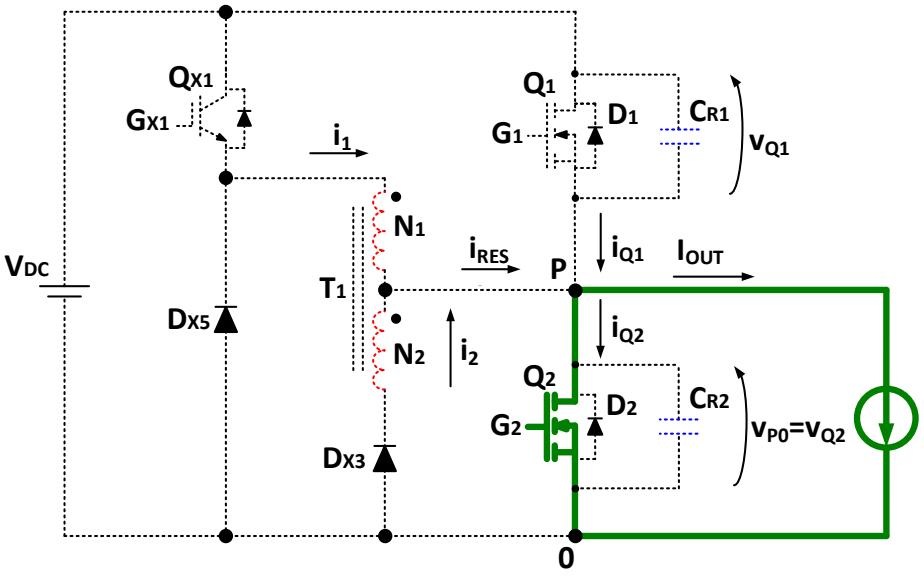


Figure 3.32 - Detail of the ZVT2CI converter during time [t_8, t_9].

Phase 8 is the last mode of operation, and it continues until the beginning of the next switching cycle, which is described in phase 0.

The operation of the converter in the case of a negative output current involves the negative current auxiliary pole *L* and is similar to the analysis presented so far, therefore it will be not considered.

3.3.C Converter design

Design specifics

The design procedures of one leg of ZVT2CI inverter are presented in the following subsections. The specifications of the converter are as follows:

Table 3.1 – Design specifications of the ZVT2CI inverter.

Design Specifics	*Value*
DC link voltage V_{DC}	400 V
Phase current $I_{OUT-MAX}$	16 A_{RMS}
Switching frequency F_{SW}	Up to 20 kHz

Main transistor selection

As discussed in section 1.1, IGBTs are usually selected for applications above 200 V_{DC} in hard switched DC to AC inverters. The use MOSFETs could potentially increase the efficiency of converters due to the fact that the majority carrier devices can switch much faster than bipolar transistors. However, power MOSFETs present an inherent parasitic diode whose dynamic performance and di/dt ruggedness deteriorates dramatically with the increase of the blocking voltage, generating switching losses and leading to potential failure of the device. Typical di/dt ruggedness for the largest part of 600V SJ MOSFET body diodes is below 100A/µs, while the di/dt during the hard turn off of diode in DC to AC converters can easily reach 1500A/µs, far above the inherent limit of SJ MOSFETs.

For the ZVS2CI Inverter described in 3.3.A, instead, the di/dt of the current during the turn off of the diode D_2 (phase 1) is controlled by the leakage inductance and the turn ratio of the auxiliary autotransformer, accordingly to the equation:

$$\frac{di_Q}{dt} = \frac{di_R}{dt} = \frac{kV_{DC}}{L''_\sigma}. \tag{3.46}$$

Therefore, the leakage inductance of the auxiliary autotransformer can be designed to limit the di/dt to less than 50 A/µs, making the use of SJ MOSFETs possible and safe for the main switches Q_1 and Q_2 of the inverter. However, even if di/dt is limited below the physical limit

of the SJ MOSFETs, the reverse recovery charge of the body diode of MOSFETs could affect the ideal operation of the converter during the resonant transition.

A short introduction to reverse recover phenomena is required for best understanding of the power switches selection criteria.

It is well known that when a diode is switched from the conducting state to the blocking state, the stored charge in the PN junction must be recombined before that the diode can recover the ability to block the reverse voltage. The recombination takes a finite amount of time, known as Reverse Recovery Time, or t_{rr}.

The reverse recovery time can be divided into two parts, corresponding to the duration of two distinct consecutive steps:

1. the storage time t_S, which is defined as the time between the instant when the current crosses the zero, and the instant when the current reaches the peak of reverse recovery I_{RRM};
2. the fall time t_f, which is defined as the time necessary for the current to fall from I_{RRM} to 10% I_{RRM}.

During the storage phase, the current decreases linearly, whereas during the second phase the current drops back to zero following an exponential law.

In general, t_s, t_f and I_{RRM} are functions of the current I_F at the turn off, of the fall rate $\frac{di_F}{dt}$ during t_S, of the reverse blocking voltage and of the junction temperature of the diode.

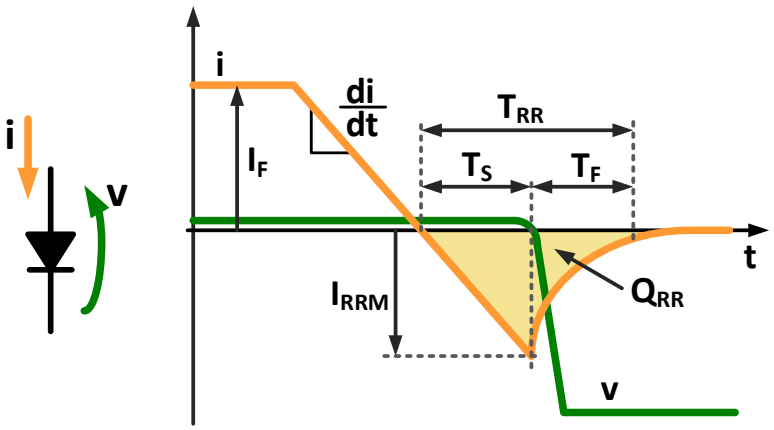


Figure 3.33 - Reverse recovery waveforms and definitions.

Regarding the ZVS2CI inverter, the reverse recovery charge of D_1 and D_2 can cause an increase in the resonant current during the resonant phases.

The switching cycle of the converter, described in section 3.3.B, begins when the load current flows through the freewheeling diode D_2. The aim of the auxiliary pole is to bring the pole voltage v_{P0} to V_{DC} allowing the ZV turn-on of the upper switch Q_1. In doing so, a current pulse i_{RES} higher than I_{OUT} is injected in the point P of the converter. The first part of the pulse has the aim of turning off the freewheeling diode D_2, while the second part charges and discharges the resonant capacitors across the transistor Q_1 and Q_2, therefore increasing the pole voltage.

Assuming an ideal behavior of diodes, the pole voltage starts rising exactly when the resonant current reaches the load current, forcing the diode D_2 in block mode. This case is analytically described in section 3.3.B and is reported in Figure 3.34 for the sake of clarity.

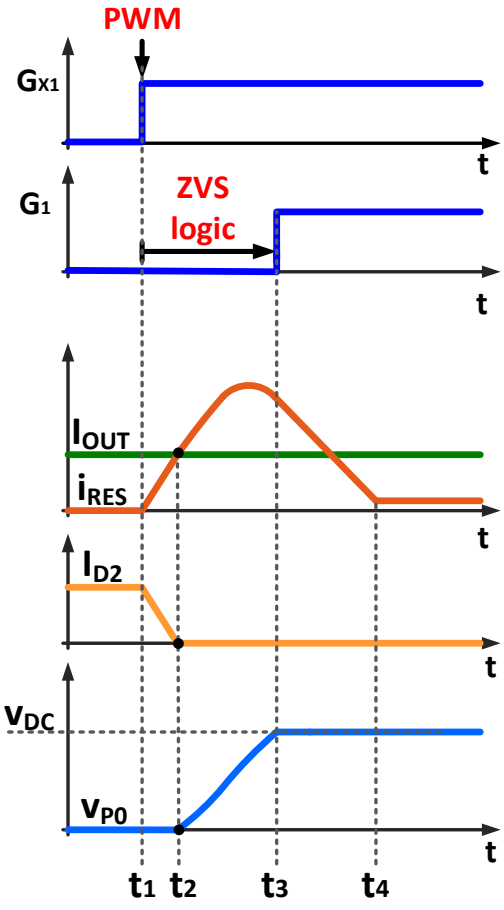


Figure 3.34 - Resonant transition of the converter if ideal diodes are considered.

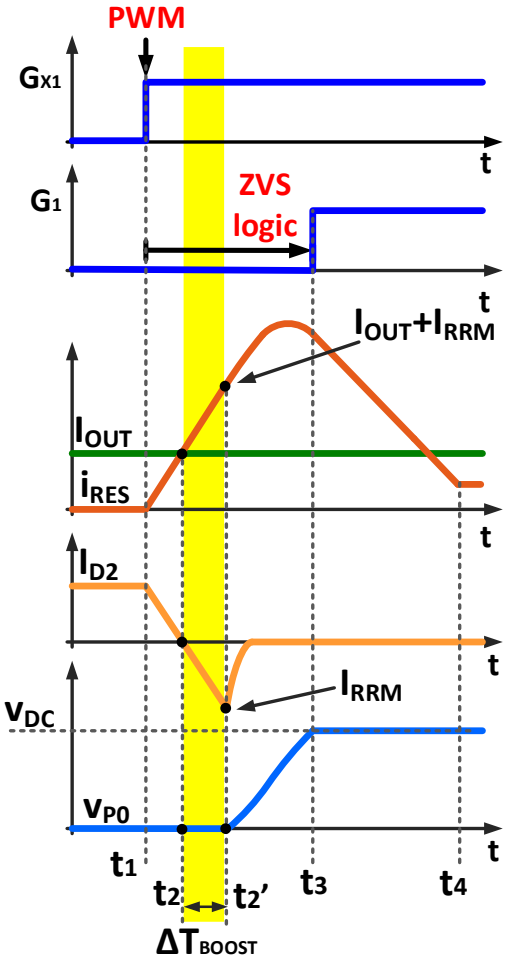


Figure 3.35 - Resonant transition of the converter if real diodes are considered.

However, real diodes, can recover the blocking capability only when the charges stored in the PN junction have been completely recombined, therefore higher resonant current than in the ideal case is required to turn-off D_2. The resonant transition of the converter in the case of real diodes is depicted in Figure 3.34. It can be seen that the pole voltage is kept to zero until $t_{2'}$, when the resonant current is equal to:

$$I_{RES-t2'} = I_{OUT} + I_{RRM} \,. \tag{3.47}$$

Therefore, the total time required to fully turn off the diode D_2 is larger than in the ideal case and lasts:

$$T_{12'} = (t_2 - t_1) + (t_{2'} - t_2) = T_{12} + \Delta T_{BOOST} = \frac{L''_\sigma \, I_{OUT}}{kV_{DC}} + \frac{L''_\sigma \, I_{RRM}}{kV_{DC}}. \tag{3.48}$$

The time delay introduced by the reverse recovery characteristic of the diode is called boost time ΔT_{BOOST}, since the resonant current i_{RES} is boosted above the load current I_{OUT}.

The presence of the boost phase has negative effects on the operation of the converter, including:

- increase in the peak value of the resonant current;
- longer duration of the resonant transition;
- increase in the conduction losses of the auxiliary circuits due to the larger RMS value of the resonant current;
- increase in the magnetizing current and therefore longer reset time is required.

Then the main switches Q_1 and Q_2 should be selected in such a way that the freewheeling diodes D_1 and D_2 are endowed with a low recovery current. IGBTs are usually co-packed with fast recovery diodes, therefore they are potentially suitable to operate as main switches in the ZVS2CI inverter. Instead not all power MOSFETs are suited for this application; only MOSFETs with a fast body diode should be selected for the use in the ZVS2CI inverter.

Given the above, both MOSFETs and IGBTs could be selected as main switches of the converter as long as theirs freewheeling diodes have proper dynamic performance. A second requirement that make a difference in the performance of the converter, is the turn-off characteristic of bipolar and majority carrier devices. Although the turn-on losses of Q_1 and Q_2 are negligible due to the zero-voltage switching, the turn-off loss can be only reduced, but

not fully eliminated, by the resonant capacitors C_{R1} and C_{R2}, acting as voltages snubbers. The shorter is the current fall time of the switch, the lower are the turn off losses. A detailed analysis of the resonant capacitor selection criteria is reported in the next section.

For the reasons above, and giving that the converters efficiency is the main focus of this thesis, power MOSFETs have been chosen due to the fast switching characteristics of majority carrier devices i.e., current fall time and absence of tail current.

An Infineon IPW65R080CFD super junction MOSFET with fast body diode, designed specifically for resonant converter topologies, was selected for the switches Q_1 and Q_2. Its main static and dynamic parameters are listed in Table 3.2.

Table 3.2 – Main electrical parameters of IPW65R080CFD SJ MOSFET.

Parameter	*Value*
Continuous drain current	*43.3 A @ 25 °C* *27.4 A @ 100°C*
Switching rise time	*18 ns @ (400 V, 26.3 A)*
Switching fall time	*6 ns @ (400 V, 26.3 A)*
R_{TH} (junction-case)	*0.32 K/W*
Diode forward voltage	*0.9 V @ (26.3 A , 25 °C)*
Diode reverse recovery time	*180 ns @ (400 V, 26.3 A, 100 A/µs, 25°C)*
Diode reverse recovery charge	*1 µC @ (400 V, 26.3 A, 100 A/µs, 25°C)*
Diode peak of recovery current	*10 A @ (400 V, 26.3 A, 100 A/µs, 25°C)*

Resonant capacitor selection

The resonant capacitors C_{R1} and C_{R2} play a key role to archive the ZV turn ON of the switches Q_1 and Q_2 of the converter. They affect the duration of phases 2-7 and define the peak of the resonant current i_{RES}. However, the most important role of resonant capacitors is to mitigate the turn-off losses of the main switches Q_1 and Q_2.

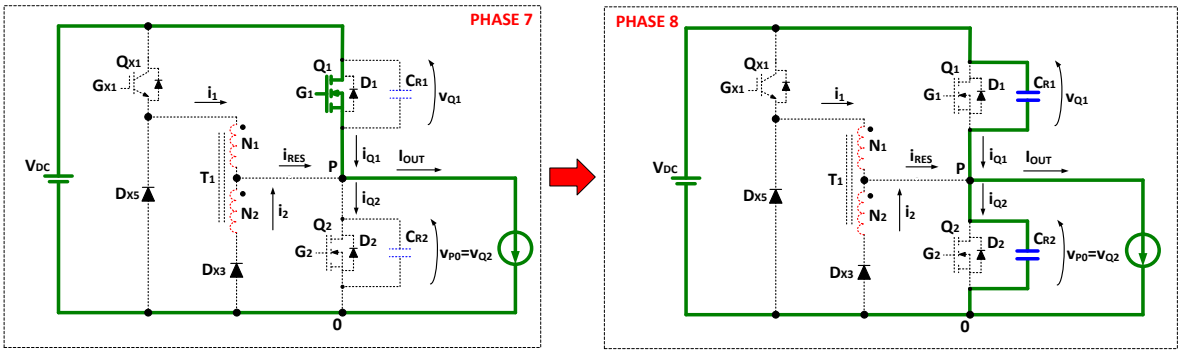


Figure 3.36 – Turn-off of Q_1 considering ideal switches. ZVS is achieved since the load current commutate instantly from the transistor to the capacitor C_{R1}.

The turn-off of Q_1 described in the phase 7 appears to be a ZV tur-off, since C_{R1} keeps to zero the voltage v_{Q1} across the switch during the instantaneous commutation of Q_1. However, in a real transistor the interruption of the current is not instantaneous; the current in Q_1 starts shifting out to charge C_{R1}, whose voltage starts increasing. Given that the transistor conducts current while the voltage is rising, power losses are generated. The correct design of the capacitor C_R can retain the voltage across the switch near zero during the turn-off of the switch, reducing significantly the turn-off losses.

The rigorous calculation of the switching losses requires a complete dynamic model of the transistor, of the gate driver and in general of the whole converter leg; this approach is possible only numerically using Spice models.

A simplified analysis can be carried out by assuming that the current in the switch Q_1 decreases linearly to zero in a time t_{fall}. As a first approximation, it can be considered t_{fall} as the time provided by device manufacturers for the double pulse test. The turn off mechanism of the upper switch Q_1 is depicted in Figure 3.37.

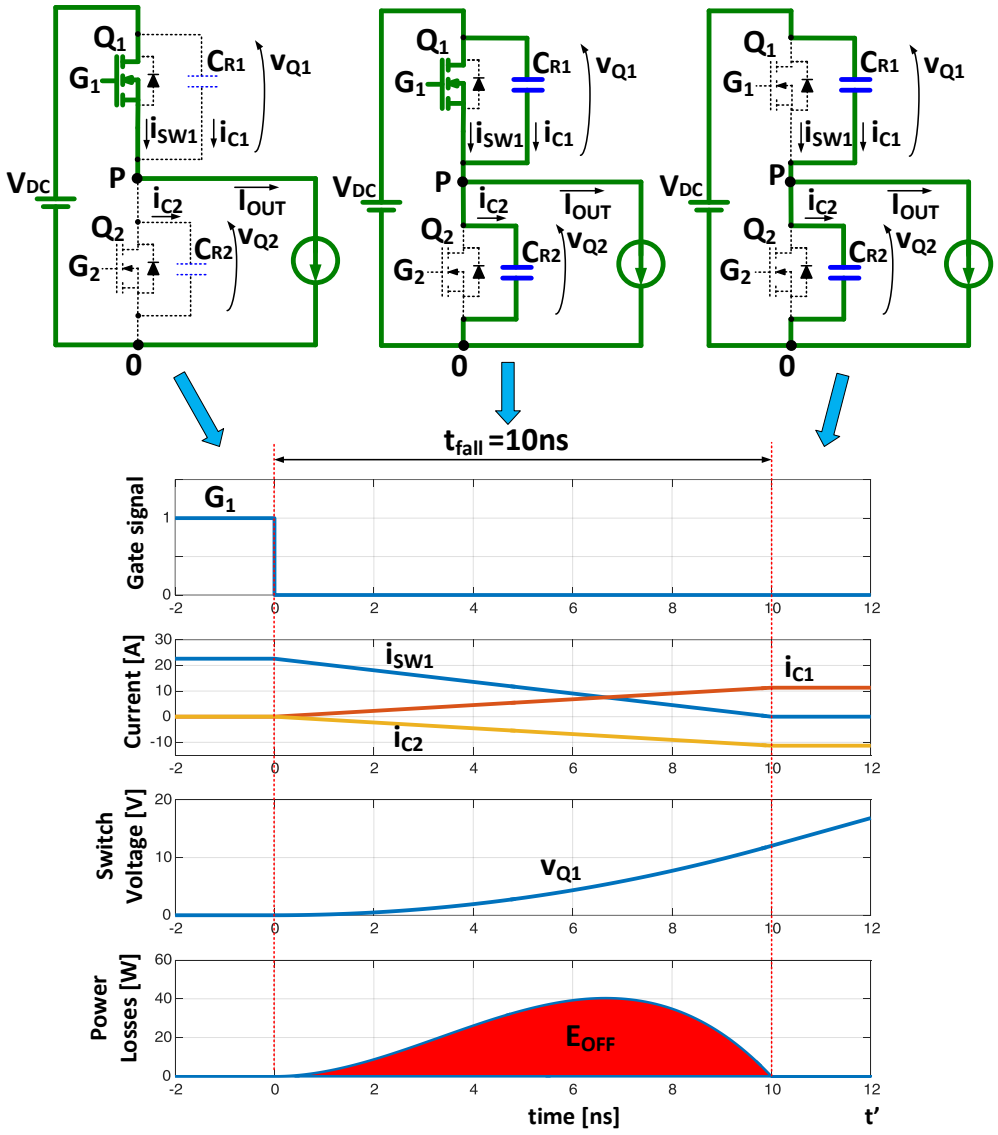


Figure 3.37 - Turn-off loss generation of Q_1 considering a real power transitor.

Let us define $t' = t - t_1$. The analysis illustrated hereafter starts in $t' = 0$ when the PWM signal G_1 commands the turn off of Q_1.

The following equations can be written:

$$i_{SW1} = I_{OUT} - \frac{I_{OUT}}{t_{fall}} t' \tag{3.49}$$

$$i_{C1} = C_{R1} \frac{dv_{Q1}}{dt} \tag{3.50}$$

$$i_{C2} = C_{R2} \frac{dv_{Q2}}{dt} = C_{R2} \frac{d(V_{DC} - v_{Q1})}{dt} = -C_{R2} \frac{dv_{Q1}}{dt} \tag{3.51}$$

$$i_{SW1} + i_{C1} = I_{OUT} + i_{C2}\,. \tag{3.52}$$

If the resonant capacitor are equals $C_{R1} = C_{R2} = C_R$, equations (3.49), (3.50), (3.51) and (3.52) can be combined to obtain the following differential equation:

$$\frac{dv_{Q1}}{dt'} = \frac{I_{OUT}}{2C_R t_{fall}} t' . \tag{3.53}$$

The initial condition of (3.53) is the forward voltage of Q_1 in conduction mode, which can be assumed negligible. Therefore, imposing $v_{Q1}\big|_{t=0} = 0$, the voltage across transistor Q_1 during the turn off can be calculated as:

$$v_{Q1} = \frac{1}{2}\frac{I_{OUT}}{2C_R t_{fall}} t'^2 . \tag{3.54}$$

The voltage across transistor Q_1 when the current has fully extinguished is:

$$V_{Q1}\big|_{t_{fall}} = \frac{1}{2}\frac{I_{OUT} t_{fall}}{2C_R} . \tag{3.55}$$

Therefore, the turn off energy can be calculated as the integral of the instantaneous power:

$$E_{off} = \int_0^{t_{OFF}} v_{Q1}\, i_{SW1} dt = \frac{1}{24}\frac{I_{OUT}^2}{2C_R} t_{fall}^2 = \frac{1}{12} I_{OUT}\, V_{Q1}\big|_{t_{fall}}\, t_{fall} . \tag{3.56}$$

Relation (3.50) states that the snubber capacitor can be selected in order to reduce the switching energy. Furthermore, the quadratic dependence of E_{off} upon t_{fall} of the transistor justifies the selection of fast switching power devices such as power MOSFET.

A criteria for the selection of resonant capacitors is to limit the voltage $V_{Q1}\big|_{t_{fall}}$ (calculated for the maximum output current) to a small percentage of the DC link voltage V_{DC}, usually below 10%:

$$V_{Q1\,max-pu} = \frac{V_{Q1}\big|_{t_{fall}} (@I_{OUT\,max})}{V_{DC}} < 0.1 . \tag{3.57}$$

An excessive snubber effect has the drawback of over-extend phase 7, indeed the derivative of the pole voltage v_{P0} is:

$$\frac{dv_{P0}}{dt} = -\frac{I_{OUT}}{2C_R} . \tag{3.58}$$

Several values of $V_{Q1\,max-pu}$ calculated for different fall time t_{fall} and resonant capacitors C_R are depicted in Figure 3.38. The DC link voltage has been considered equal to 400 V and $I_{OUT\,max}$ equal to $22.6A$, i.e., the design specifications of the converter.

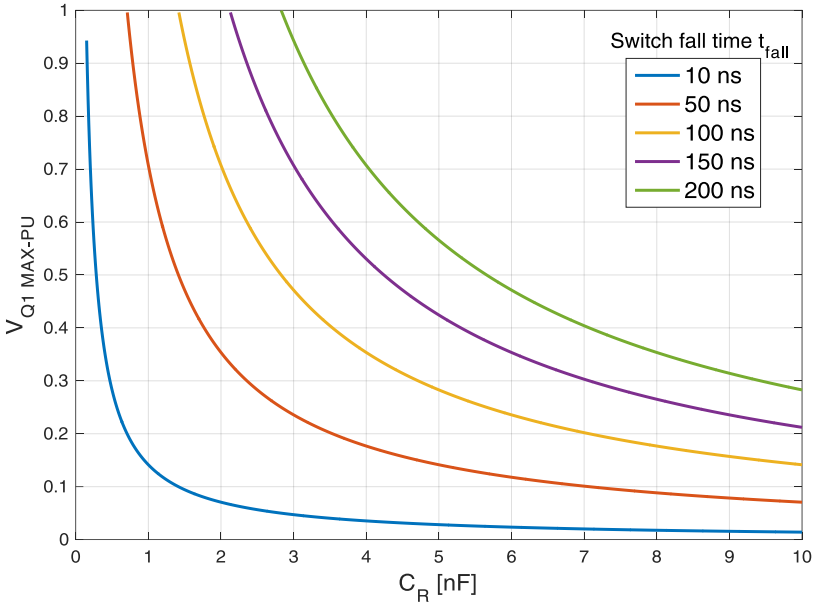


Figure 3.38 – Voltage across switch Q_1 versus snubber capacitor C_{R1} as a function of the fall time of the transistor. Curves are calculated for a load current of $22.6A$.

It should be considered that power transistors have an inherent parasitic nonlinear output capacitance C_{OSS} between drain and source (collector-emitter). This capacitance is in parallel to the external capacitor C_R and takes part to the resonant transition phases of the converter. Therefore, C_R should be selected at least one order of magnitude above C_{OSS}, in order to mitigate the nonlinearity of C_{OSS} and to make the frequency shift caused by of C_{OSS} negligible.

The parasitic output capacitance of the SJ MOSFET selected for the converter is shown in Figure 3.39, it can be seen the strong nonlinearity of C_{OSS} over the drain source voltage.

For $V_{DS} < 50V$, the output capacitance of the transistor is higher than 1 nF, therefore it has the effect of helping C_R to reduce the turn off losses of the switch while for $V_{DS} > 100V$, C_{OSS} is lower than 200 pF. Therefore the resonant capacitor C_R should be selected higher than 2 nF.

For the reasons above, and considering that the fall time of the selected SJ MOSFET is 6ns (@ 26.3A), a 4.7nF capacitor was selected for C_{R1} and C_{R2}.

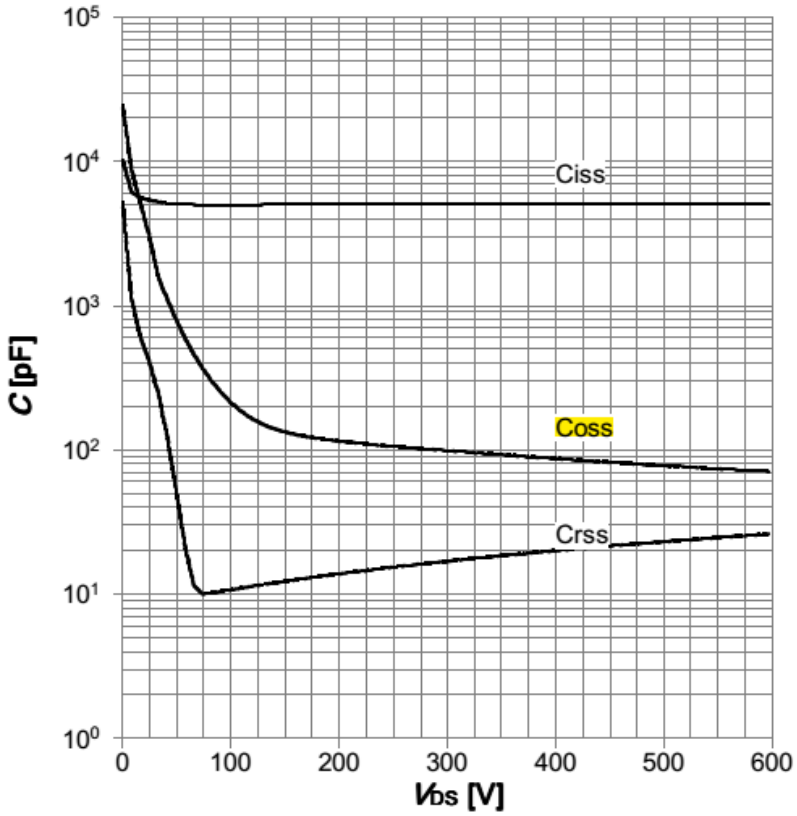


Figure 3.39 - C-V characteristics of IPW65R080CFD super junction MOSFET.

Autotransformer turn ratio section

The transformation ratio k of the autotransformer affects the duration of the resonant transitions of the converter. In fact, the derivative of current in phase 1 is proportional to k:

$$\frac{di_R}{dt} = \frac{kV_{DC}}{L''_\sigma} \tag{3.59}$$

while in phase 3 is proportional to $1-k$:

$$\frac{di_R}{dt} = -\frac{(1-k)V_{DC}}{L''_\sigma}. \tag{3.60}$$

Figure 3.40 shows the effect of the turn ratio on the resonant current i_R. The following operating conditions and parameters have been considered:

- $V_{DC} = 400\ V$
- $I_{OUT} = 22.6\ A\ (16Arms)$

- $L''_\sigma = 6.8\ \mu H$
- $C_{R1} = C_2 = 4.7\ nF$
- no magnetizing inductance.

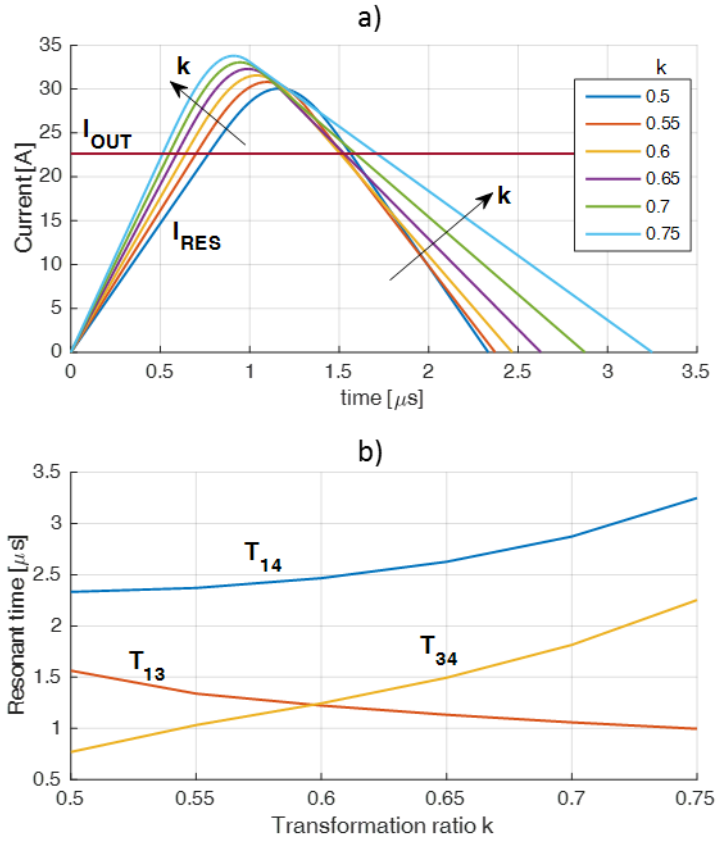


Figure 3.40 - a) Auxiliary current as a function of the transformation ratio of the autotransformer. b) Duration of phases 1, 2, and 3 as a function of the transformation ratio of the autotransformer.

It can be seen in Figure 3.40 that the increase of k leads to an increase in the peak value of i_{RES} and a reduction in time T_{13} (resonant phases 1 and 2). Therefore, ZV condition for Q_1 can be reached in shorter time. On the contrary, the descending phase of i_{RES} takes a longer time T_{34}, increasing the overall time T_{14} required to complete a resonant cycle and increasing RMS value of the current i_{RES}. Since there are no benefits in the reduction of T_{13} i.e., main switches Q_1 and Q_2 are turned on under ZV in any case, it is recommendable to keep the turn ratio as close as possible to 0.5.

Practically, k is selected between 0.55 and 0.6 in order to guarantee a safe margin of operation since the equivalent series resistance of the resonant loop reduces the theoretical peak of the voltage V_{P0} during the resonant phase 2.

For the reasons above, the transformation ratio selected for the prototype is:

$$k = \frac{N_2}{N_1 + N_2} = 0.6\,. \tag{3.61}$$

Resonant inductance selection

The resonant inductance L''_σ plays a key role in the design of the converter since it determines the duration of the resonant phases 1 to 3 and the peak of the resonant current i_{RES}. Figure 3.41 shows the effect of the variation of L''_σ, where the following operating conditions and parameters are considered:

- $V_{DC} = 400\ V$
- $I_{OUT} = 22.6\ A\ (16Arms)$
- $C_{R1} = C_2 = 4.7\ nF$
- $k = 0.6$
- no magnetizing inductance.

It can be observed in Figure 3.41 that the resonant transition time is almost a linear function of the resonant inductance L''_σ; small value of L''_σ reduces the transition time T_{14} but causes high values of i_{RES} and of $\frac{di_{RES}}{dt}$. As explained in the previous section, high level of $\frac{di_{RES}}{dt}$ may introduce an unwanted boost phase of i_{RES} caused by the reverse recovery characteristics of D_1 and D_2. A reasonable $\frac{di_{RES}}{dt}$ value that makes negligible the reverse recovery effect on the converter behavior is between 10 and 50 A/µs.

For the reasons above, and considering the dynamic characteristic of the body diode of the selected power switch, the following resonant inductance has been chosen:

$$L''_\sigma = 6.5\ \mu H \tag{3.62}$$

which correspond to a $\frac{di_{RES}}{dt}$ of 37 A/µs and to a transition time of 2.4 µs at the maximum output current I_{OUT} of $22.6\ A$.

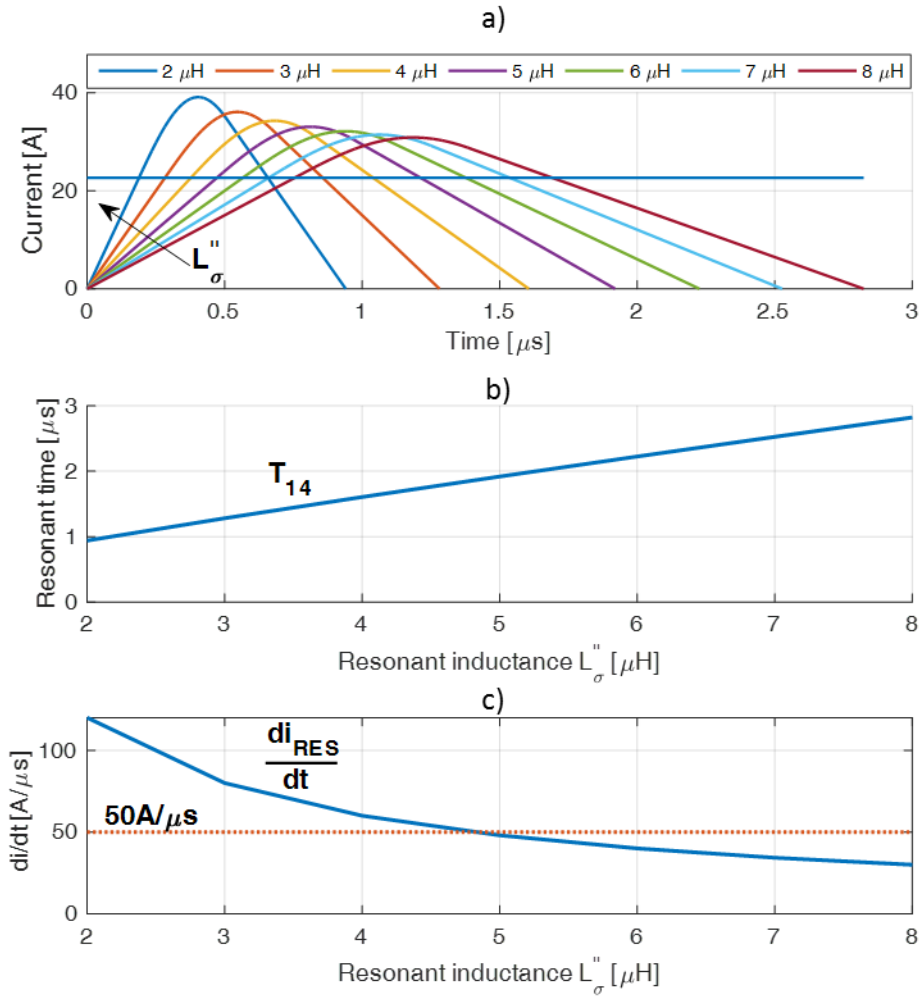


Figure 3.41 - a) Auxiliary current as a function of the leakage inductance of autotransfomer. b) Duration of the transition time T_{14} as a function of the leakage inductance of autotransfomer. c) Maximum resonant current variation as a function of the leakage inductance of autotransfomer.

Autotransformer design and FEM simulation

The autotransformer of the ZVT2CI inverter has two main functions; it generates the voltage kV_{DC} and it incorporates the inductance that take part to the LC resonant transition of the converter. The design specifics and the constraints obtained in the previous paragraphs can be summarized as follows:

Table 3.3 – Design specifics of the autotransformer.

Design Specifics	*Value*
Primary side voltage	400 V
Autotransformer turn ratio $k = \frac{N_2}{N_1+N_2}$	0.6
Secondary side leakage inductance L''_σ	6.5 µH
Maximum transition time T_{14-MAX}	2.4 µs ($@I_{OUT\ MAX}$)

It has been shown in section 3.3.B that the DC link voltage is applied to the primary winding of the autotransformer $N_P = (N_1 + N_2)$ for the time T_{14}, thus the cross section area A_e of the transformer and the primary winding turns N_P should be selected in such a way that the iron core saturation is avoided. If we assume the proper operation of the converter, then the magnetizing current of the transformer is completely reset each switching cycle. The magnetic flux linked with the primary coil can be obtained as:

$$\emptyset_{MAX} = V_{DC} T_{14-MAX} \,. \tag{3.63}$$

Assuming a linear BH characteristic of the ferromagnetic material of the core, the turn number of the primary coil can be calculated as follows:

$$N_P = \frac{\emptyset_{MAX}}{B_M A_e} = \frac{V_{DC} T_{14-MAX}}{B_M A_e} \tag{3.64}$$

where B_M is the flux density and A_e is the cross section area of the iron core.

For high frequency applications, ferrites are usually adopted since sintered materials can significantly reduce eddy currents losses compared to laminated iron steels. For the project, a TDK N87 ferrite material has been selected, its B-H characteristic is depicted in Figure 3.42. It can be seen that the saturation flux density at 100°C is around 360 mT, therefore (3.64) is reasonably accurate if the maximum flux density is limited below the saturation knee of the material.

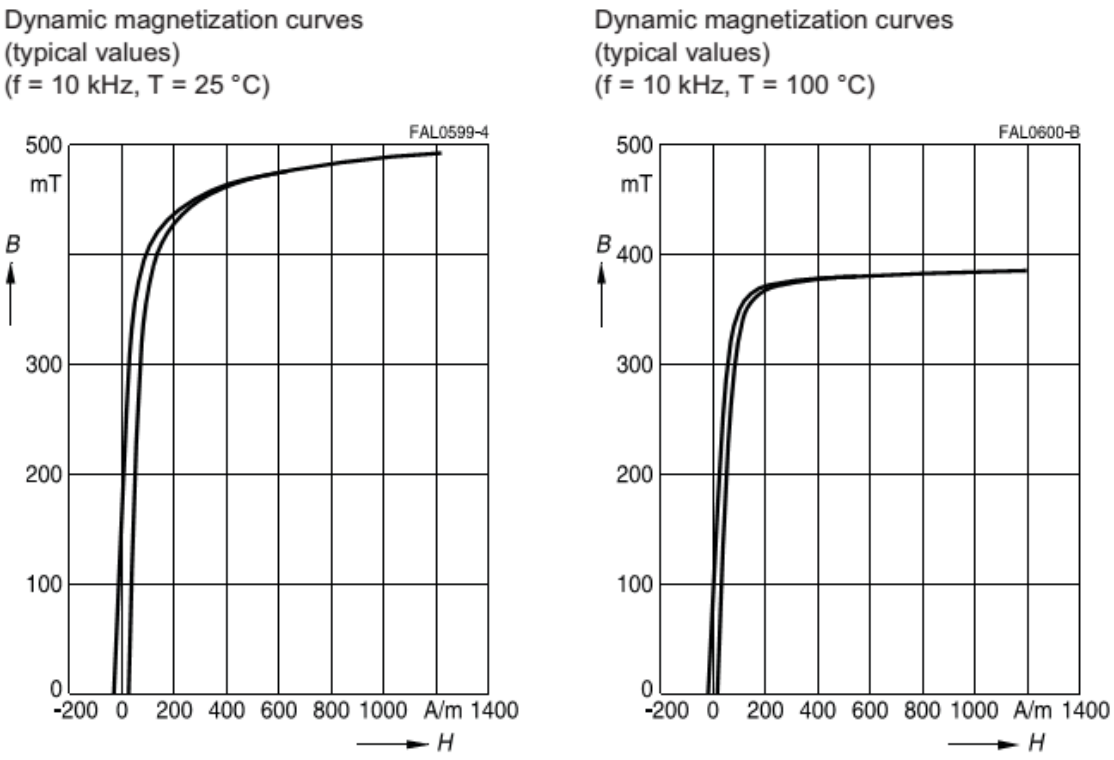


Figure 3.42 – Magnetic hysteresis loop of N87 ferrite.

The number of turns of the two coils of the autotransformer can be easily calculated imposing the required transformation ratio k:

$$N_1 = (1 - k)\, N_P \tag{3.65}$$

$$N_2 = k\, N_P\,. \tag{3.66}$$

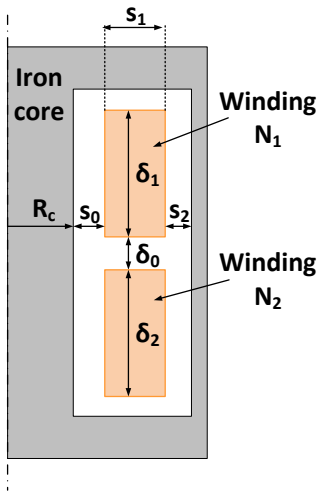
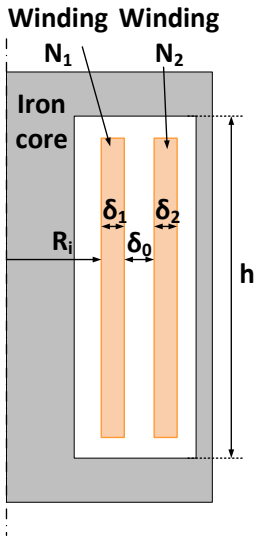
The inductance L''_σ can be controlled by varying the mutual position of the windings N_1 and N_2. The leakage inductance referred to the secondary side of the autotransformer can be evaluated using the approximated geometrical relations reported in

Table 3.4 and the following formula:

$$L''_\sigma = N_2^2 \left(\frac{1-k}{k}\right)^2 \lambda_\sigma\,. \tag{3.67}$$

In general, concentric disposition of N_1 and N_2 reduces the leakage flux, while a split arrangement has the effect to reduce the coupling coefficient.

Table 3.4 - Leakage permeance coefficients of split and concentric windings.

	Leakage permeance coefficient of split windings: $\lambda_\sigma \cong \mu_0 \frac{2\pi\left(R_C + \frac{s_0+s_1+s_2}{2}\right)}{s_0+s_1+s_2}\left(\delta_0 + \frac{\delta_1+\delta_2}{3}\right)$
	Leakage permeance coefficient of concentric windings: $\lambda_\sigma \cong \mu_0 \frac{2\pi\left(R_i + \frac{\delta_0+\delta_1+\delta_2}{2}\right)}{h}\left(\delta_0 + \frac{\delta_1+\delta_2}{3}\right)$

The last design constraint is the maximum current density J_{CU} of the windings of the transformer. Common values of J_{CU} that guarantee a safe thermal operation of an air cooled transformer are below $2A_{RMS}/mm^2$.

The RMS currents in the winding N_1 and N_2 depend on the load current I_{OUT} and on the switching frequency of the converter. If the magnetizing current is neglected, I_{1RMS} and I_{2RMS} can be calculated as:

$$I_{1RMS} = \sqrt{F_{SW} \int_0^{T_4} (k\, i_{RES})^2\, dt} \tag{3.68}$$

$$I_{2RMS} = \sqrt{F_{SW} \int_0^{T_4} \left((1-k) i_{RES}\right)^2 dt}\,. \tag{3.69}$$

A numerical design procedure has been implemented in order to design the autotransformer. The range of variation of the design parameters and the constraints are listed in Table 3.5 and Table 3.6.

Table 3.5 – Design specifics of the autotransformer.

Design Specifics	*Value*
Primary side voltage	*400 V*
Autotransformer turn ratio $k = \frac{N_2}{N_1+N_2}$	*0.6*
Secondary side leakage inductance L''_σ	*6.5 µH*
Maximum transition time T_{14-MAX}	*2.4 µs (@*$I_{OUT\ MAX}$*)*
Switching frequency F_{SW}	*30 kHz*

Table 3.6 - Design constraints of the autotransformer.

Design constraints	*Value*
Maximum iron core flux density B_{MAX}	*350 mT*
Maximum error on turn ratio k	*< 2%*
Maximum current density J_{CU-MAX}	$< 2A/mm^2$
Utilization factor of the transformer window	$K_U < 0.45$
Distance between N_1 *and* N_2	*0.5mm to 5mm*
Winding configuration	*Split or concentric coils*
Ferrite core shapes	*ETD34 , ETD39 , ETD43*

The preliminary design result of the transformer has been simulated by using 3D Finite Element Analysis in order to adjust the mutual position of the windings. In Table 3.7 are listed the electrical characteristics of the final design of the transformer, while in Figure 3.43 are depicted the rendering of the transformer and a FEA field map.

Table 3.7 – Final design results.

Design results	*Value*
Ferrite core shape	*ETD39*
Maximum iron core flux density B_{MAX}	*300 mT* ($@T_{14} = 3.5\mu s$)
Winding N_1	*15 turns*
Winding N_2	*22 turns*
Turn ratio $k = \frac{N_2}{N_1+N_2}$	*0.595*
Primary winding composition	10 *wires x* 0.35*mm diameter*
Secondary winding composition	7 *wires x* 0.35*mm diameter*
Primary winding DC resistance	*18m*Ω @25°C
Secondary winding DC resistance	*39m*Ω @25°C
Distance between N_1 *and* N_2	*4 mm*

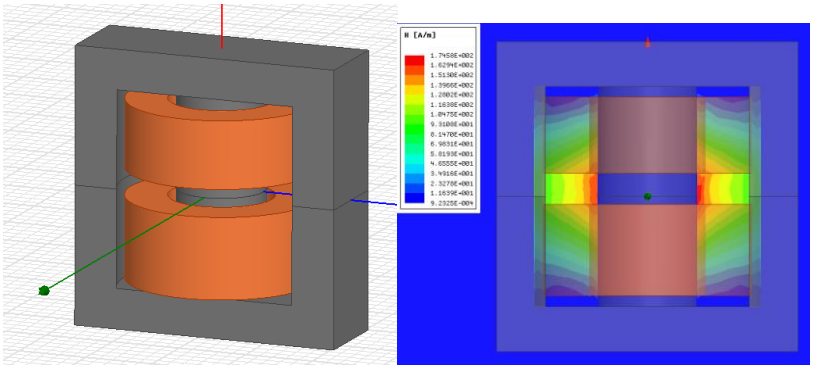


Figure 3.43 – Detail of the FEA model of the autotransformer.

The finite element analysis provides only the inductance matrix between the coils N_1 and N_2 of the autotransformer:

$$\begin{vmatrix} L_{11} & M \\ M & L_{22} \end{vmatrix} = \begin{vmatrix} 0.734 & 1.062 \\ 1.062 & 1.577 \end{vmatrix} mH. \tag{3.70}$$

The magnetizing and leakage inductance referred to the secondary side of the auto-transformer can be obtained by means of (3.70) and imposing the series connection of coils N_1 and N_2:

$$L''_{\sigma} = k^2 L_{11}\left(1 - \frac{M^2}{L_{11}L_{22}}\right) = 6.8\,\mu H \tag{3.71}$$

$$L''_{M} = \left(\frac{k}{1-k}\right)^2 \frac{M^2}{L_{22}} = 1.54\,mH. \tag{3.72}$$

Auxiliary switches and selection of diodes

The components used for the auxiliary switches Q_{X1} and Q_{X2} are composed of an IGBT (Infineon IGP50N60T) and a Schottky diode (Infineon IDH04G65C5XKSA1). This IGBT offers high switching speed and a low collector-emitter saturation voltage, whereas the diode is a SiC part specifically designed for high-frequency applications. Infineon IDH04G65C5XKSA1 is used also for diodes D_{X5} and D_{X6}. Finally, the Schottky SiC diode Cree C4D05120A is used for D_{X3} and D_{X4}, because it provides a negligible reverse recovery current.

Active ZVS gate driver design

As described in the section 3.3.B, load current and source voltage influence the duration of phases 1 to 3 of the converter. Adaptive gate driver circuits have been implemented in order to ensure the ZV turn-on of the main switches under any load current and source voltage conditions [50].

The details of the ZVS gate driver for switch Q_1 are depicted in Figure 3.44. The circuit is composed by a gate driver, a decoupling diode, a Schmitt trigger, a logic AND gate, an optocoupler and an isolated power supply that generates the voltage V_{CC} referred to the source of Q_1. The same block is replicated for switch Q_2.

The voltage V_{DS1} across Q_1 is sensed through a blocking diode, which guarantees that no voltage higher than V_{CC} can be applied to the logic circuit. If V_{DS1} is lower than a threshold value (few volts), the Schmitt trigger enables the transmission of the PWM control signal to the gate driver circuit. Therefore the ZV turn-on of Q_1 is ensured.

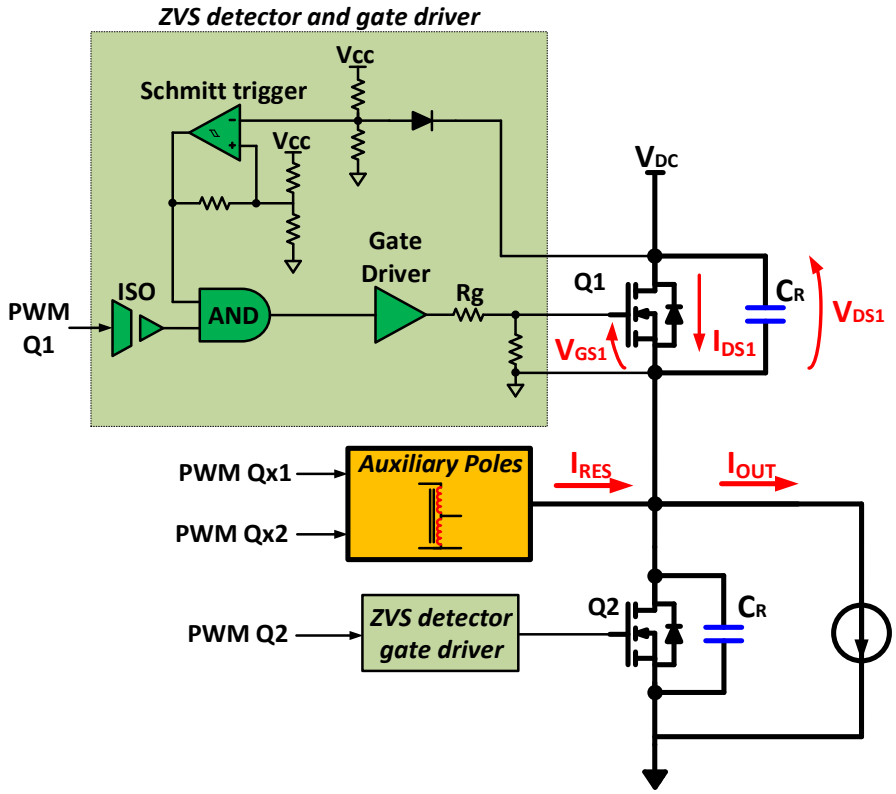


Figure 3.44 – Details of the Zero-voltage detection circuit and gate driver.

3.3.D Experimental results

For the sake of simplicity, only one leg of the inverter has been fabricated. The same board can be reconfigured to a hard switching leg for performance comparison.

The schematic and the 3D rendering of the prototype are depicted in Figure 3.45. The converter is controlled by means of an external control board, which implements the control algorithm and generates the PWM signals.

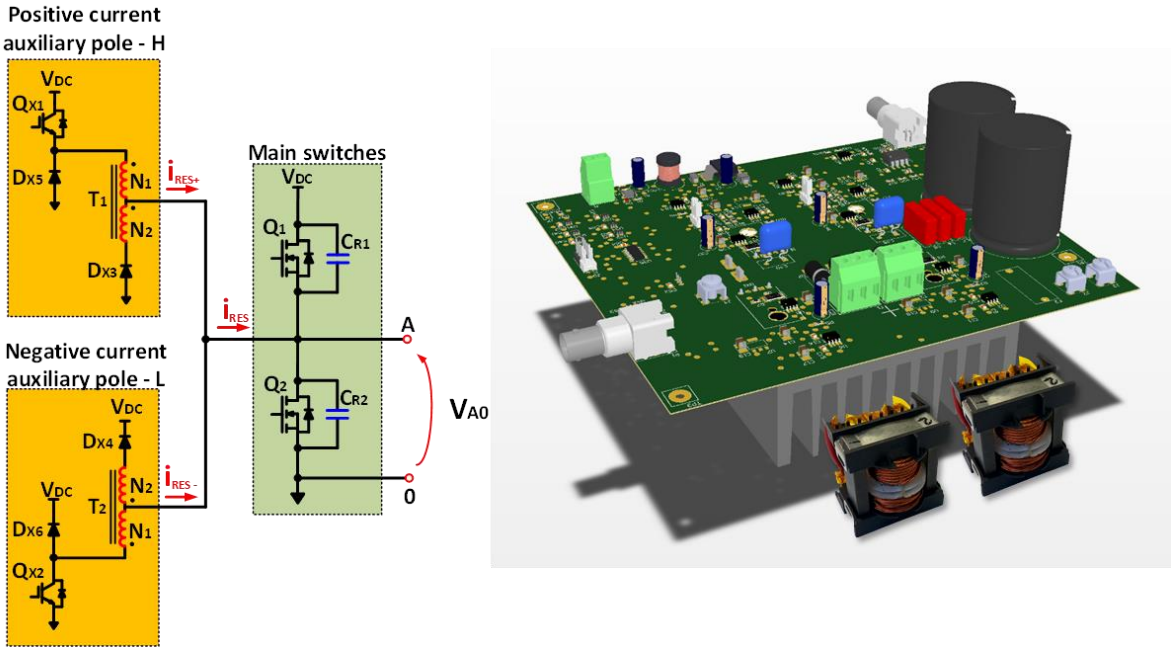


Figure 3.45 – Schematic and 3D rendering of the prototype of ZVT2CI converter.

Functional tests of the converter

The ZVT2CI prototype was firstly tested in order to verify the proper operation of the converter, the test circuit implemented is depicted in Figure 3.46.

Switches Q_{X1} and Q_{X2} are controlled according to the principle of the sinusoidal pulse width modulation. The dead-time interval, T_{DT}, is equal to 1.5 µs, while the delay time T_{DLY} between the fall edge of Q_{X2} and Q_1 has been chosen equal to 1 µs in order to guarantee the complete reset of the magnetizing current of the autotransformer each switching cycle.

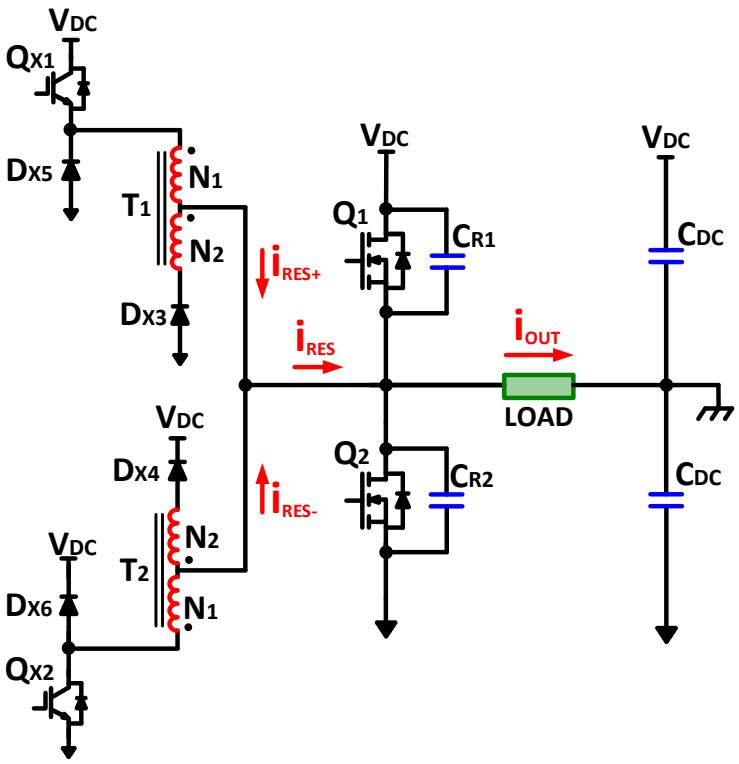
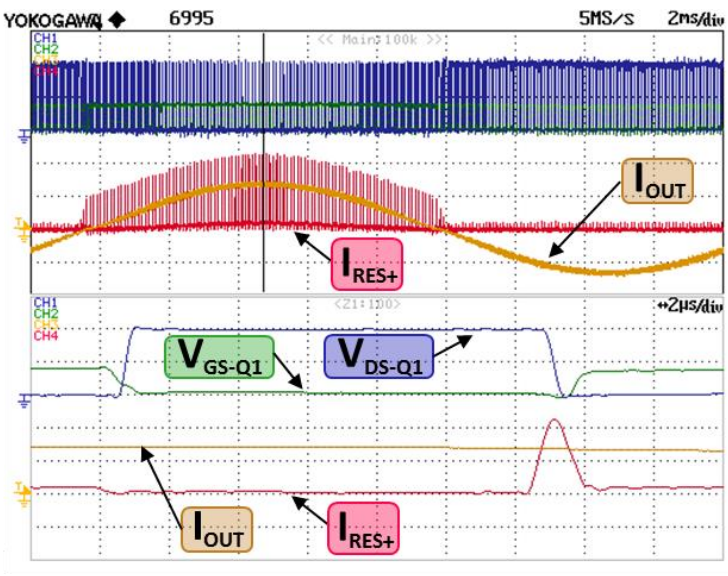


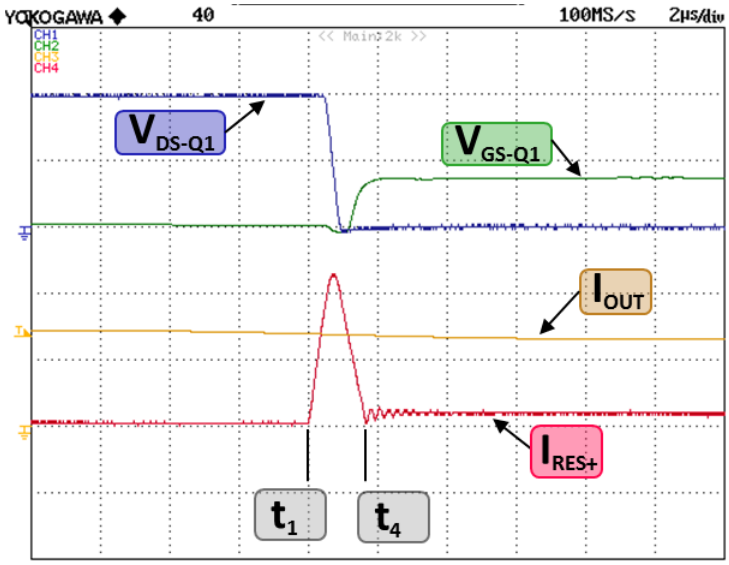
Figure 3.46 - Schematic of a leg of the ZVT2CI inverter.

Figure 3.48 shows the waveforms of the load current, I_{OUT}, the positive component of the resonant current, i_{RES+} , the drain-source voltage V_{DS-Q1} of Q_1, and the gate-source voltage V_{GS-Q1} of Q1 over a time interval of 20 ms. The lower part is a zoomed view of the same waveforms during one switching cycle of Q_1. The inverter is controlled by means of a sinusoidal PWM, therefore the load current is nearly sinusoidal. It can be noted that the resonant current is zero during the negative half-period of the load current since only i_{RES+} is sensed. Therefore, the auxiliary RMS current stress is very low. In the zoomed view of the same picture, it can be clearly seen that the load current is approximately constant over a switching period, and the waveforms of the variables depicted are very similar to those shown in the theoretical timing diagram of Figure 3.14. The turn-on command of Q_1 is applied when its drain-source voltage V_{DS-Q1} is zero, i.e., in zero-voltage switching condition.



V_{GS-Q1} [20 V/div], V_{DS-Q1} [100 V/div]
I_{OUT} [10 A/div], I_{RES+} [10 A/div]

Figure 3.47 - Behavior of the ZVT2CI inverter controlled by means of sinusoidal modulation.



V_{GS-Q1} [20 V/div], V_{DS-Q1} [100 V/div]
I_{OUT} [10 A/div], I_{RES+} [10 A/div]

Figure 3.48 – Detail of the zero-voltage turn-on of switch Q_1.

Figure 3.48 shows in details the turn-on phase of Q_1. It can be observed that the turn-on command of Q_1 is applied when its drain-source voltage is zero, therefore the ZV switching is achieved. In addition, the same figure shows the waveform of the resonant current during

the time interval $t_1 - t_4$. The resonant current is zero before t_1, while is equal to the magnetizing current of the transformer after t_4, this fact confirms the correct de-magnetization phase of the autotransformer in each switching cycle.

The upper part of Figure 3.49 shows the waveforms of the drain-source voltage V_{DS-Q1} and the current I_{DS-Q1} carried by the device during the turn-on phase. I_{DS-Q1} starts to flow through the device only when V_{DS-Q1} falls to zero, therefore, soft switching operation is achieved since the instantaneous power dissipated by the device is minimized. The soft switching operation is confirmed by the turn-on trajectory depicted in the lower part of Figure 3.49.

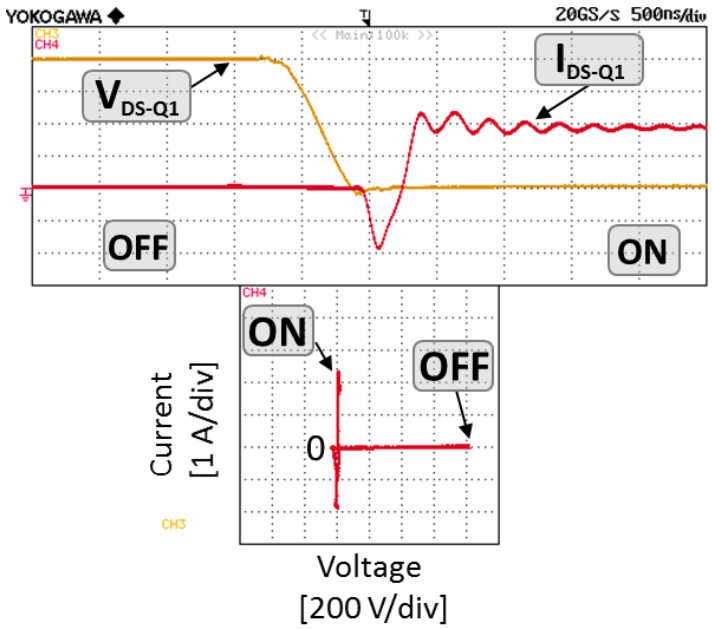


Figure 3.49 - Detail of the zero-voltage turn-on of switch Q_1 and switching trajectory.

Figure 3.50 shows the experimental verification of the main switch ZVS operation with load current adaptability. As Q_{X1} is turned on, the resonant current start increasing. Voltage V_{DS-Q1} decreases to zero when the resonant current exceeds the load current and diode Q_2 turns off. It can be noted that the reverse recovery current of the diode causes a small delay between the instant at which I_{RES} is equal to I_{OUT} and when voltage V_{DS-Q1} starts falling. Although the duration of the resonant process depends on the amplitude of the load current,

the zero-voltage detection circuit of Figure 3.44 always ensures that Q_1 is turned on only when its drain-source voltage is zero.

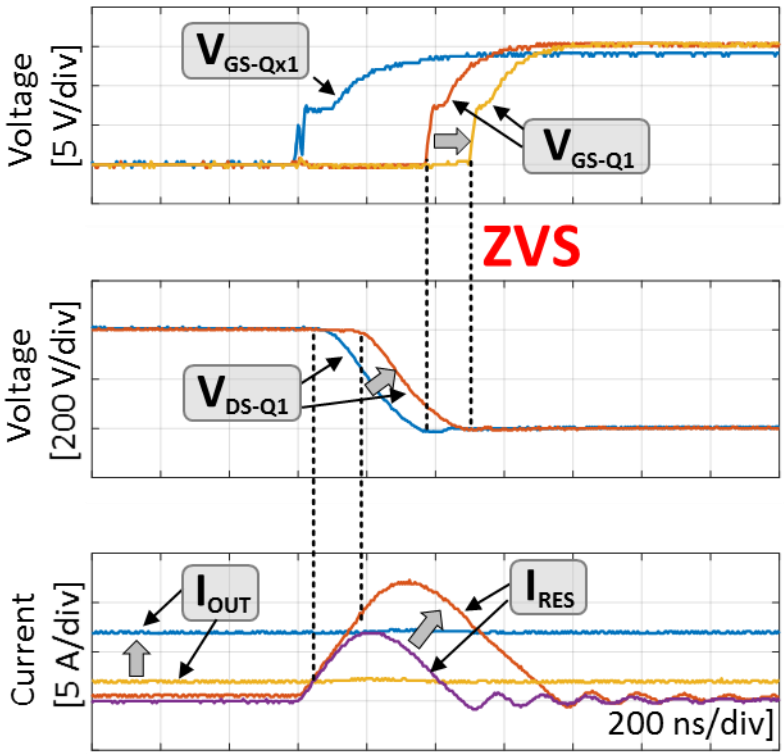


Figure 3.50 - Behavior of the ZVT2CI inverter as the load current increases.

The effect of the reverse recovery characteristic of D_2 on the resonant transition of the converter is reported in Figure 3.51. The left part of the figure is obtained using for Q_1 and Q_2 SJ MOSFETs endowed with body diodes that have large reverse recovery charge Q_{RR}, while the right part of the figure is obtained using the MOSFETs endowed with a fast body diode selected in section 3.3.C. Both experiments were carried out at the same input voltage V_{DC} and output current I_{OUT}. It can be observed that the reverse recovery charge of D_2 can introduce a boost phase of the resonant current, which causes negative effects on the operation of the converter. It is worth mentioning that the longer duration of the resonant phase $t_1 - t_4$ and the higher peak value of the resonant current lead to an increase in the conduction losses of the auxiliary circuit.

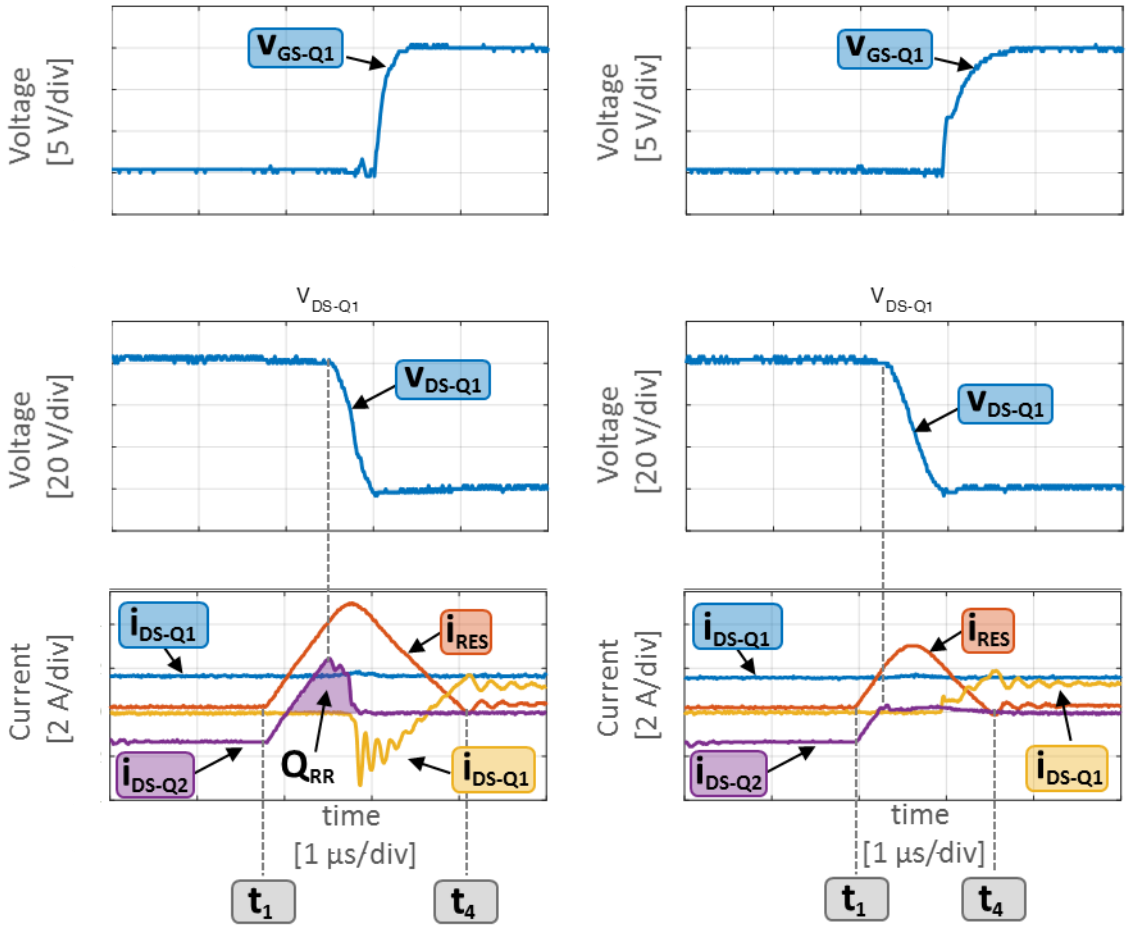


Figure 3.51 – Effect of the reverse recovery of diodes on the behaviour of the converter.

Efficiency comparison of ZVT2CI inverter and HS inverters

The efficiency of the ZVT2CI inverter developed has been compared to hard switched inverters built with the latest transistor technologies. This comparison is crucial since the hardware and control complexity of the ZVT2CI inverter is justified only if the reduction in the overall losses of the converters is appreciable. In fact, the reduction of the switching losses of the main power switches is obtained in spite of additional losses introduced by the auxiliary circuits to achieve ZVS.

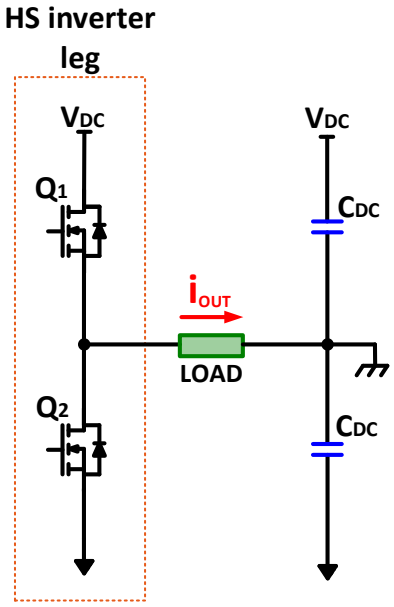


Figure 3.52 - Schematic of a leg of the hard-switching inverter.

For comparison purposes, the ZVT2CI inverter has been re-arranged in a conventional hard switching inverter, as shown in Figure 3.52. Two versions of the converter have been tested, which differ from each other only in the power switches Q_1 and Q_2. The transistor chosen for the efficiency comparison are listed in Table 3.8. The first device is a silicon high-performance IGBT (Infineon IKW40N65H5), designed for best-in-class efficiency in hard-switching and resonant converter topologies. The second device selected is a high-switching speed SiC MOSFET (C2M0080120D), produced by CREE. As can be observed in Table 3.8, the blocking voltage of the SiC switch (1200V) is almost twice that of the Si counterpart (650V). This choice is due to the absence of SiC devices with lower blocking voltages on the market.

It is worth mentioning that the Si SJ MOSFET selected for the operation in ZVT2CI configuration cannot be tested under hard switching condition. Indeed, the reverse recovery characteristic of the body diode would generate very high levels of switching losses, which would damage the components.

Table 3.8 – Main parameters of the Si IGBT and SiC MOSFET selected.

Parameter	*Si IGBT*	*SiC MOSFET*
Breakdown voltage	*650V*	*1200V*
DC continuous current	*46A @100°C*	*20A @100°C*
Nominal on-state voltage drop/resistance	*1.65 V*	*80 mΩ*
R_{TH} (junction-case)	*0.60 K/W*	*0.60 K/W*
Case package	*TO247*	*TO247*
Part number	*Infineon*	*Cree*
	IKW40N65H5	*C2M0080120D*

The forward voltage drop of the Si IGBT and SiC MOSFET are compared in Figure 3.53, whereas the turn-on and turn-off switching energies are depicted in Figure 3.54.

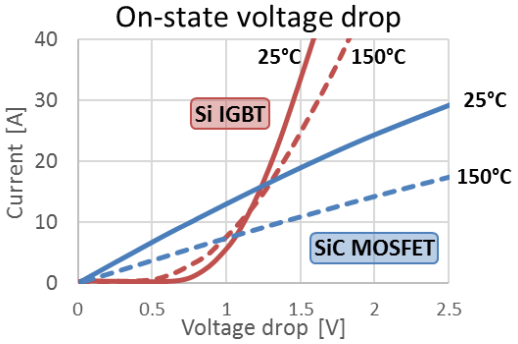


Figure 3.53 – V-I characteristic of the Si IGBT and SiC MOSFET selected.

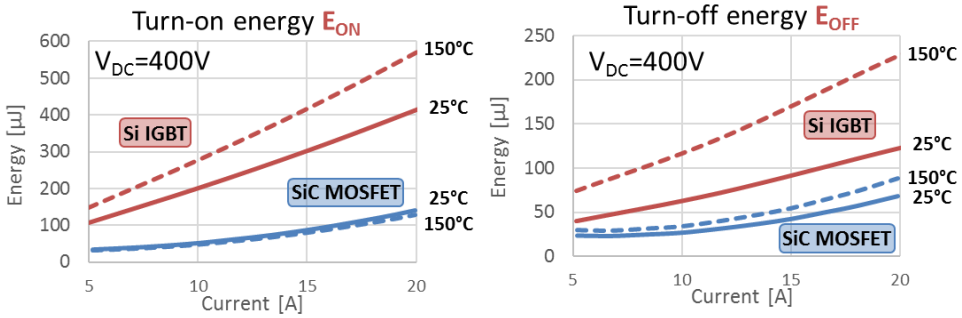


Figure 3.54 – Switching energies of the Si IGBT and SiC MOSFET selected.

Three prototypes were tested in the same operating conditions in order to compare their efficiency. For the sake of clarity the converters that were tested are listed in Table 3.9.

Table 3.9 – List of tested converters.

	Inverter configuration	*Power switch*	*Switch part number*
Prototype 1	*Hard switching (HS)*	*Si IGBT*	*IKW40N65H5*
Prototype 2	*Hard switching (HS)*	*SiC MOSFET*	*C2M0080120D*
Prototype 3	*ZVT2CI*	*Si SJ MOSFET*	*IPW65R080CFD*

All the tests were carried out at constant modulation index, equal to 0.8, and at an output frequency of 50 Hz. The converters fed an R-L load, whose inductance was 2 mH, whereas the resistance was adjusted to change the load point. Due to the low value of the load inductance, the load power factor was nearly unity in all tests.

During the tests, the dc voltage, equal to 400 V, was kept constant by the dc generator TDK Lambda GEN600-5.5, which also limited the output power to about 2200 W. The efficiency was measured by means of a digital power meters Yokogawa WT2030, since the wide frequency ranges of the instrument makes possible the direct efficiency measure of switching converters.

The sink of the prototypes was thermally controlled and its temperature was kept at about 25°C for all whole duration of the tests. The test setup is show in Figure 3.55.

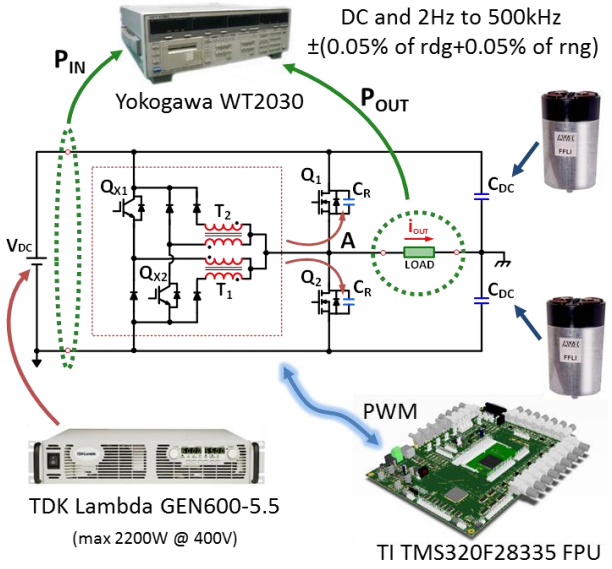


Figure 3.55 – Experimental test setup.

The efficiency of the three prototypes are shown in Figure 3.56, Figure 3.57 and Figure 3.58 as a function of the output power at three switching frequencies, i.e., 10 kHz, 20 kHz and 30 kHz.

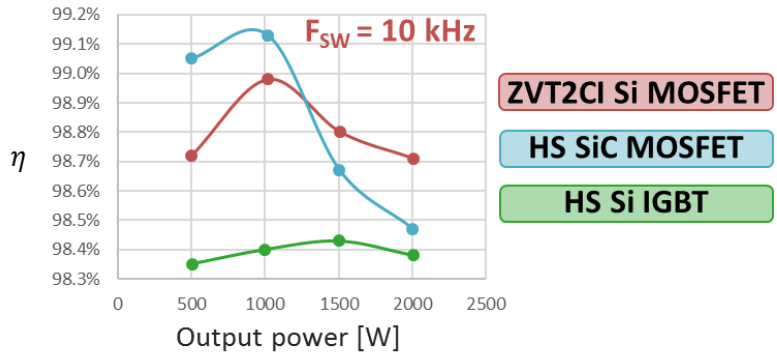


Figure 3.56 – Efficiency of prototypes as a function of output power at a switching frequency of 10 kHz.

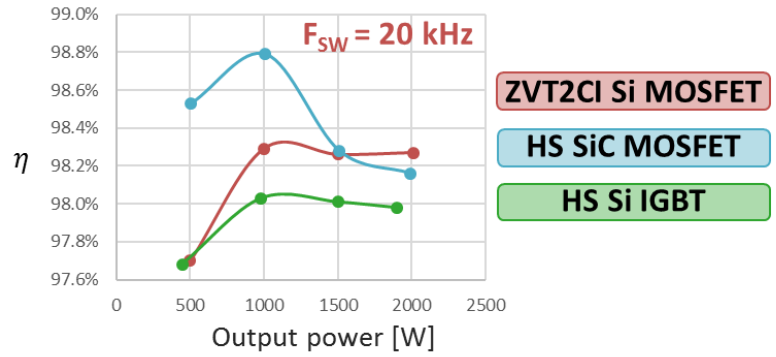


Figure 3.57 - Efficiency of prototypes as a function of output power at a switching frequency of 20 kHz.

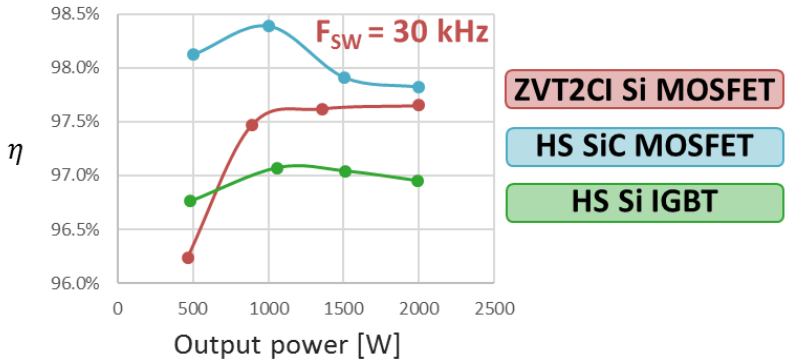


Figure 3.58 - Efficiency of prototypes as a function of output power at a switching frequency of 30 kHz.

The efficiency of all prototypes is plotted in Figure 3.59 as a function of the switching frequency when the output power is equal to 500 W, 1000 W, 1500 W and 2000 W.

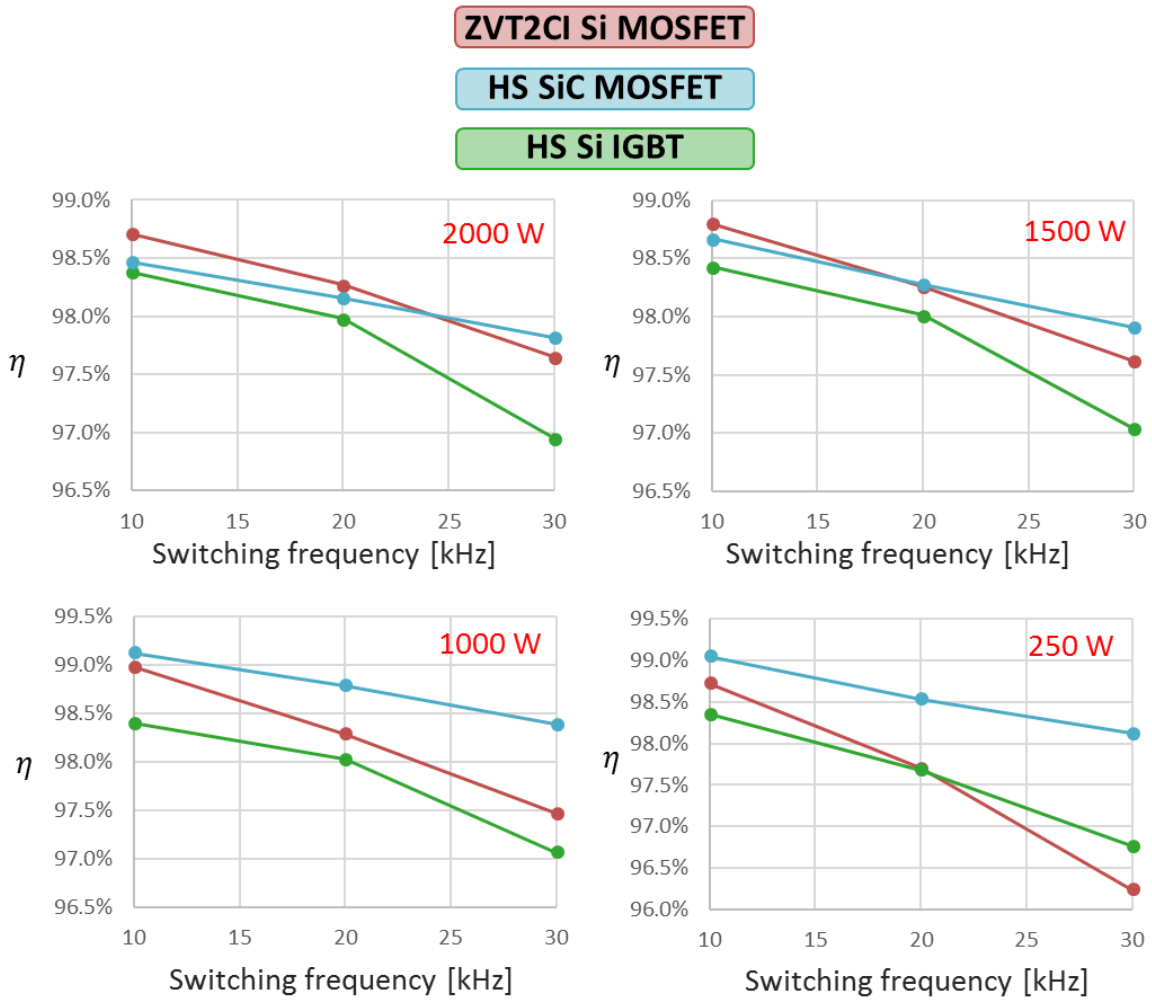


Figure 3.59 - Comparison of the efficiency of prototypes as a function of the switching frequency for different output power.

It can be noted from the graphs that the efficiency of the ZVT2CI converter is always greater than the efficiency of the HS Si IGBT inverter. The higher efficiency is due to several factors. First of all the use of the ZVT2CI topology avoids the turn-on losses and reduces the turn-off losses generated by the main switches of the converter. In addition, the ZVT2CI converter allows the use of SJ MOSFET that otherwise would not be possible to use for issues related to the reverse recovery characteristic of the body diode. The last advantage is the increase in efficiency of the converter at low load, which is due to the resistive V-I characteristic of MOSFET.

The comparison between the ZVT2CI converter and the HS SiC MOSFET converter deserves a special discussion. Conduction losses of the main leg of the two converters are similar since both uses devices with the same nominal R_{DS-ON} of 80 mΩ. Therefore, the efficiency difference is mainly due to the switching losses and to the losses introduced by the auxiliary circuits of the ZVT2CI converter. It can be noted that the efficiency at low load of the ZVT2CI converter is lower than that of SiC inverter, even at low switching frequency. This behavior is due to the loss bias of the auxiliary circuits, which become dominant at low output currents.

As the frequency increases, it can be noted that the efficiency of the SiC inverter tends to be higher than that of the ZVT2CI converter, for any load current value. Again, this behavior is due to the losses of the auxiliary circuits of the ZVT2CI, which increase as a function of the frequency more than the switching losses of the SiC converter, thus making the efficiency improvement less appreciable. For switching frequencies above a threshold value, between 20 and 30 kHz, the SiC converter becomes more efficient than the ZVT2CI converter for any load current.

It is worth mentioning that the SiC prototype have higher efficiency even though the power transistors are rated for a blocking voltage much higher than the silicon transistor.

Chapter 4

Single Phase Inverters for Transformerless PV Applications

4.1 Short introduction on solar energy conversion

Photovoltaic (PV) energy has grown at an average annual rate of 60% in the last five years, and has become an important part of the energy mix of power systems [51]. Global PV power installed has had a significant growth from 1.2 GW in 1992 to 177 GW in 2014 [52]. Europe has led the PV development until 2012, when its cumulative PV installed power was the 70% of the global installations [53]. Since 2012, European PV installations has slowed down while Asian PV installations have been increasing rapidly.

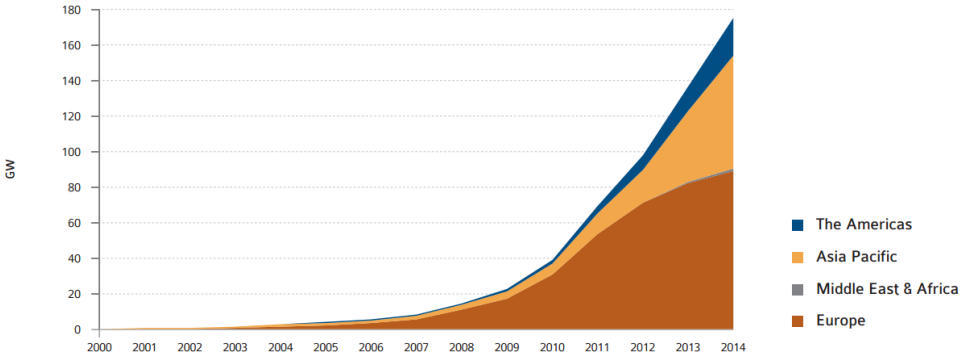


Figure 4.1 – Evolution of regional PV installations.

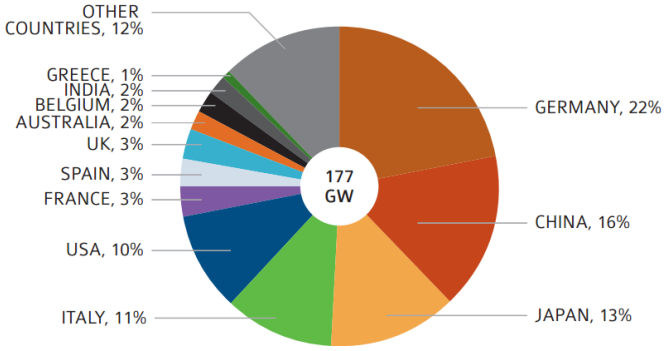


Figure 4.2 – Cumulative installed PV capacity at the end of 2014.

The contributions of individual countries to the cumulative PV power installed at the end of 2014 are depicted in Figure 4.2, the statistical results were published in 2014 PV Annual Report of the European Photovoltaic Industry Association (EPIA) [54]. It can be observed that over 50% of the global PV power installations (89 GW) are within the European Union territory.

At the end of 2014, the installed PV capacity in Italy was 18.5 GW. The PV penetration in the national power system is very important considering that 24 TWh of energy were generated by PV on a total energy demand of 309 TWh.

The largest part of the photovoltaic power is generated by large photovoltaic plants connected to the medium voltage (MV) network (61%), low voltage (LV) installations contributes to the 33% of national production while only the 6% is generated by plants connected to the high voltage (HV) grid. Even though low voltage systems contribute only for one third to the national energy production, they are the majority part of installed systems. In fact, 97% of PV installations are connected to the LV grid and consist of residential and commercial PV plants.

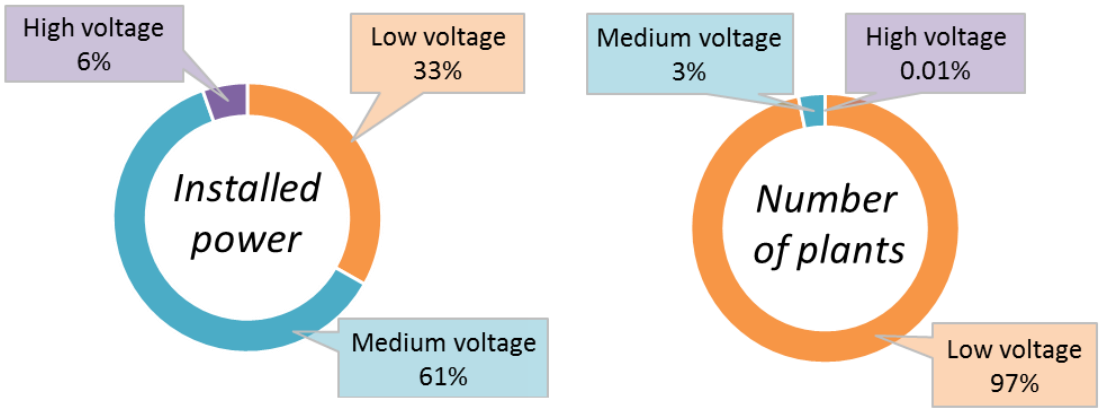


Figure 4.3 –Statistic of italian PV systems.

All the energy generated by PV systems is injected in the electrical power system by DC/AC converters. Therefore, considering the high cost of solar panels, great attention has been given to the development of highly efficient PV inverters by researcher and companies. Several inverter topologies have been proposed to increase the efficiency of converters in compliance with national safety regulations for grid connected systems.

In Italy, LV grid connected photovoltaic systems are regulated by the standard CEI 82-25.

For power levels above 20kW, the standard requires a galvanic isolation between the DC side and the AC side of the PV system. Galvanic isolation can be performed using an isolation transformer. This solution has the main goal of prevent the injection of DC current into the grid by DC/AC converters. DC currents in AC system must be avoided since may lead to the iron core saturation of MV/LV distribution transformers. Isolation can be achieved either by high frequency and low frequency transformers.

If the installed power is below 20 kW, the galvanic isolation may be replaced by an active protection that senses the phase currents and disconnects the PV system within:

- 200 ms if the DC component is higher than 1A;
- 1 s if the DC component is higher than 0.5% of the rated current of the converter.

Furthermore, the standard imposes a three phase connection to LV grid for all PV systems above 6 kW, below this power level, PV inverters can be single phase units.

Given that LV PV systems are the largest part of the PV installations, the focus of this thesis has been given to single phase PV converters.

Figure 4.4 shows the schematic of a single phase PV system connected to the LV grid through an isolation transformer. The overall conversion efficiency of this solution can be written as:

$$\eta_{TOT} = \eta_{INV}\,\eta_F\,\eta_T \tag{4.1}$$

where η_{INV} is the combined efficiency of the Maximum Point Tracker (MPPT) and inverter, η_F is the efficiency of the decoupling filter, and η_T is the efficiency of the transformer.
The opportunity given by CEI 82-25 to remove the insolation transformer (transformerless) has the aim of increasing the overall efficiency of low power PV systems. Although the transformer reduces the efficiency of the system, its low coupling capacitance between primary and secondary windings strongly attenuates the circulation of any hazardous leakage current generated by the DC/AC converter, also known as Common Mode (CM) currents [55] [56] [57]. Figure 4.5 shows the schematic of a single phase transformerless PV system connected to the LV grid. The common mode current is generated by the inverter and flows in a loop composed by the coupling capacitance of the transformer, the LV grid, the ground connection of the MV/LV transformer and the parasitic capacitance to ground of the PV modules.

PV systems are sensitive to CM current issue more than any other energy generation system due to the parasitic capacitance between PV modules and ground. PV silicon solar cells are usually encapsulated in a structure composed of glass, thermoplastic elastomers like Ethylene Vinyl Acetate (EVA), protective back sheet, and a metallic frame. In order to guarantee the personal protection against indirect contacts, all the exposed metallic frames must be electrically connected to the grounding system of the plant. The proximity of grounded metallic frames to PV cells creates a distributed capacitance between the DC link of the PV system and the ground, i.e., a path for leakage currents is created. The total capacitance to ground depends on the module fabrication, on the surface of the PV strings and on weather conditions. Typical values of capacitance to ground are in the order of 50-150 nF/kWp [55].

The respect of national safety requirements for PV transformerless inverters (CEI 64-8), is then more critical to achieve than for transformer-based inverters. Special converter topologies, modulation strategies and common mode line filters are generally required to be compliant with standards [58] [59] [60].

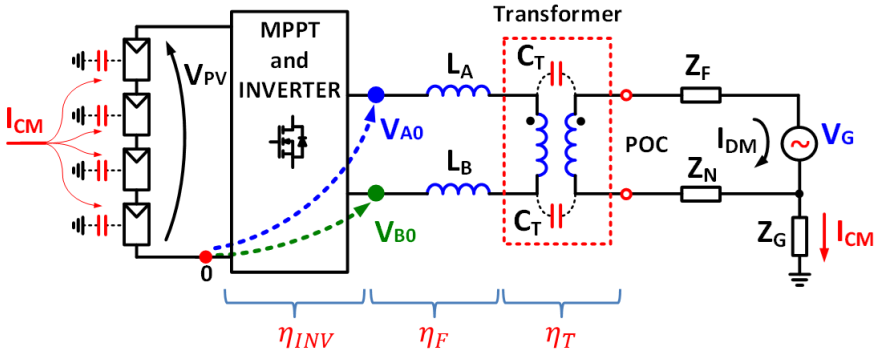


Figure 4.4 – Single phase PV system with isolation transformer.

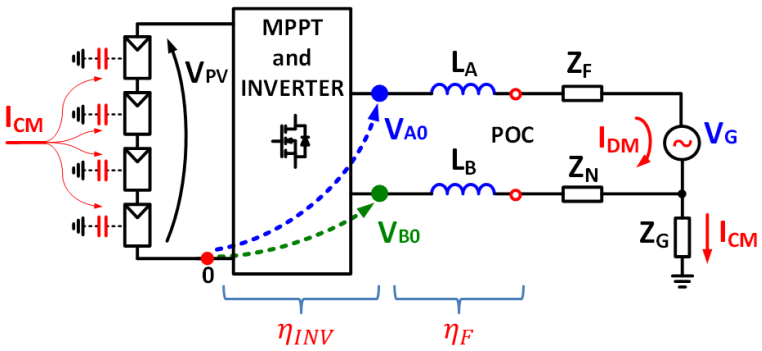


Figure 4.5 - Single phase transformerless PV system.

4.2 *Common mode model of single-phase transformerless inverters*

The aim of this section is to show how the leakage current can be calculated as a function of the output voltage generated by the inverter.

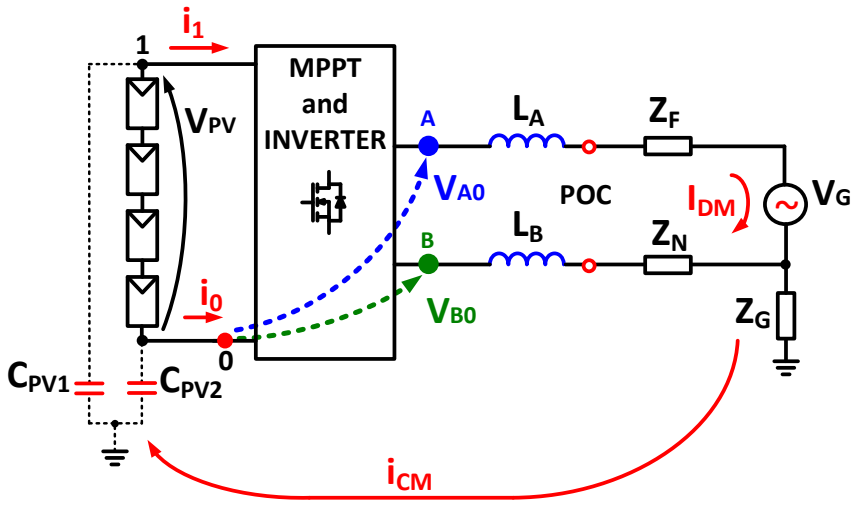


Figure 4.6 – Transformerless PV system schematic showing the leakage loop.

Let us consider the schematic of a typical single phase transformerless PV system depicted in Figure 4.6. The elements of the system can be described as follows:

- Z_G is the ground impedance of the MV/LV transformer of the grid;
- Z_F and Z_N are the line and neutral impedance of the electrical line between the MV/LV transformer and the Point of Connection (POC) of the PV system;
- L_A and L_B are the decoupling inductors between the grid and the inverter. The converter is a voltage controlled source, and therefore, a short-circuit condition appears whenever it is directly connected to other voltage source like the grid. Consequently, decoupling inductors are required to limit the current injected into the grid.
- C_{PV1} and C_{PV2} are the equivalent capacitances to ground of the PV system;
- V_{A0} and V_{B0} are the voltages generated by the front-end inverter;

- i_{DM} is the differential mode (DM) current, which is related to the power generated by the PV system;
- i_{CM} is the common mode current generated by the front-end inverter.

As reported in previous paragraph, the total capacitance of the PV system to ground can be estimated in 50-150 nF/kW. If we consider a 6 kW PV system, the maximum level allowed by standards for single phase connections, the capacity to ground C_{PV} can be calculated as:

$$C_{PV} \cong 900\ nF\ . \tag{4.2}$$

The voltage across C_{PV} presents a low frequency component due to the grid voltage source, and a high frequency component due to the voltage modulation of the front-end inverter, typically from 10 kHz to 30 kHz. The impedance of C_{PV}, opposing to the circulation of the leakage current, can be calculated as:

$$Z_{PV}(@50\ Hz) = 3.5\ k\Omega \tag{4.3}$$

$$Z_{PV}(@20\ kHz) = 9\ \Omega\ . \tag{4.4}$$

Given that C_{PV} acts as a high-pass filter, the grid influence on the common mode behavior of the system can be neglected. For the same reason, the voltage variation on the PV panels can be neglected as well.
A second reasonable approximation comes from the fact that grid impedances Z_F and Z_N depend on the short-circuit power of the grid at the point of connection of the PV system. Weak distribution grids have high impedances, which help to reduce the leakage current. PV systems, however, must be compliant with safety standards independently of the short-circuit power at POC, hence, even in the worst case of ideal grid (Z_F=Z_N =0).

In light of the above, the model of Figure 4.6 can be simplified to that of Figure 4.7. The inverter has been substituted by two equivalent controlled voltage sources V_{A0} and V_{B0}.

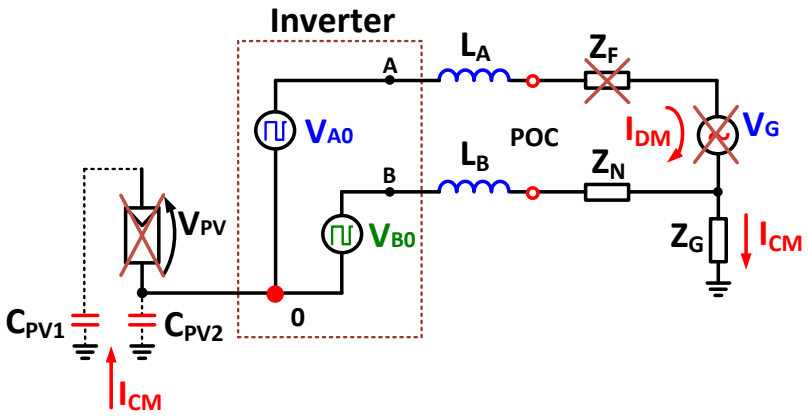


Figure 4.7 – Simplified model of the PV system.

Circuit depicted in Figure 4.7 can be redrawn as in Figure 4.8, capacitors C_{PV1} and C_{PV2} have been reduced to the single lumped capacitor calculated in (4.2).

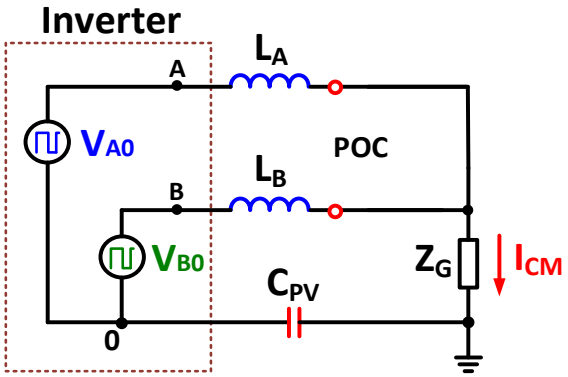


Figure 4.8 - High frequency model of the PV system

The leakage current can be calculated solving the circuit of Figure 4.8:

$$I_{CM}(s) = \frac{sC_{PV}}{1 + sC_{PV}Z_G + s^2 C_{PV} L_{AB}} \left(\frac{L_B}{L_A + L_B} V_{A0}(s) + \frac{L_A}{L_A + L_B} V_{B0}(s) \right) \quad (4.5)$$

where L_{AB} is the parallel of the decupling inductances L_A and L_B.

Relation (4.5) can be further simplified introducing the concept of common mode and differential mode voltage. The common mode voltage is defined as the average value V_{A0} and V_{B0}:

$$V_{CM} = \frac{V_{A0} + V_{B0}}{2}. \quad (4.6)$$

The differential mode voltage is defined as the difference between the pole voltages:

$$V_{DM} = V_{AB} = V_{A0} - V_{B0}\,. \tag{4.7}$$

The voltages V_{A0} and V_{B0} can be written as:

$$V_{A0} = V_{CM} + \frac{V_{DM}}{2} \tag{4.8}$$

$$V_{B0} = V_{CM} - \frac{V_{DM}}{2}\,. \tag{4.9}$$

By using (4.8) and (4.9), leakage current I_{CM} can be written as:

$$I_{CM}(s) = \frac{sC_{PV}}{1 + sC_{PV}Z_G + s^2C_{PV}L_{AB}}\left(V_{CM}(s) + V_{DM}(s)\frac{L_B - L_A}{2(L_A + L_B)}\right). \tag{4.10}$$

The terms that sustain the circulation of leakage current can be grouped in one equivalent quantity called *total common mode voltage* V_{TCM}, defined as:

$$V_{TCM}(s) = V_{CM}(s) + V_{DM}(s)\frac{L_B - L_A}{2(L_A + L_B)} \tag{4.11}$$

Equation (4.11) can be rewritten as follows:

$$I_{CM}(s) = \frac{sC_{PV}}{1 + sC_{PV}Z_G + s^2C_{PV}L_{AB}}V_{TCM}(s) \tag{4.12}$$

Figure 4.9 shows the equivalent common mode circuit on the PV system. It is worth mentioning that V_{DM} may contribute to the total common mode voltage if decoupling inductors L_A and L_B are unbalanced.

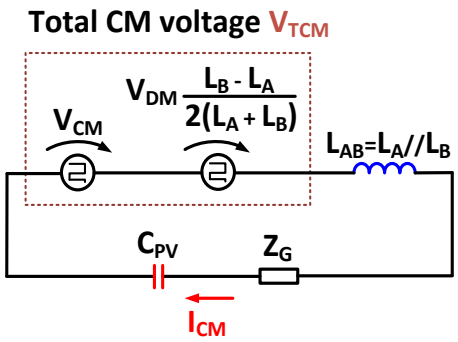


Figure 4.9 - Simplified model of the PV system showing the total common mode voltage V_{TCM}.

Equation (4.12) shows that I_{CM} can be reduced by increasing the decoupling inductance (adoption of CM filters), or by reducing the high frequency components of voltage V_{TCM}. If

voltage V_{TCM} does not vary with time ($\frac{dV_{TCM}}{dt} = 0$), then leakage current is minimized. Several converter topologies and modulation techniques have been proposed to address the leakage current issue of transformerless PV systems. Proposed converters can be classified into two categories, which are different for the implemented approach.

The aim of the first category is to keep constant V_{TCM} over the time. Topologies that exploit this approach are [61] [62]:

- Full bridge converter with bipolar modulation (H4 bipolar inverter);
- Three Level Neutral Point Clamped inverter (NPC inverters);
- T-type Three Level inverter (T-NPC inverters);
- H6 inverter;

The aim of the second group is a bit different from what has been explained so far. Rather than keeping V_{TCM} constant, the DC side of the inverter is disconnected to the grid every time a zero configuration ($V_{A0} = V_{B0}$) is applied by the inverter. As described in section 4.3.B, this solution has the effect of an evident reduction in the leakage current [62]. The main topologies that implement CM current interruption are [61]:

- H5 inverter
- Highly Efficient and Reliable Inverter Concept (HERIC)

In this thesis only the configurations derived from the full bridge converter have been analyzed, i.e., H4, H5, and H6 converters.

4.3 Single phase transformerless inverters derived from full cridge converter

In the following sections are presented the latest DC/AC converters employed for transformerless PV systems. For each converter the possible modulation techniques are described and the results of numerical simulations obtained with PLECS, a software developed by Plexim GmbH for the simulation of power electronic systems, are presented. Particular emphasis is given to the total common mode voltage V_{TCM} generated by each converter.

Simulations have been performed under the assumption that the parameters listed in Table 4.1. The symbols are referred to the general schematic of Figure 4.10.

Table 4.1 – Parameter of the PV system used for the simulations.

Parameter	*Value*
Grid voltage V_G	*230* V_{RMS} *, 50 Hz*
DC link voltage	*400 V (800V for 3L converters)*
Total decoupling inductance $L_A + L_B$	*2 mH*
Switching frequency F_{SW}	*20 kHz*
C_{PV}	*900 nF*
Z_G	*20 Ω (ohmic)*
Z_F *and* Z_N	*0 Ω (ideal grid)*

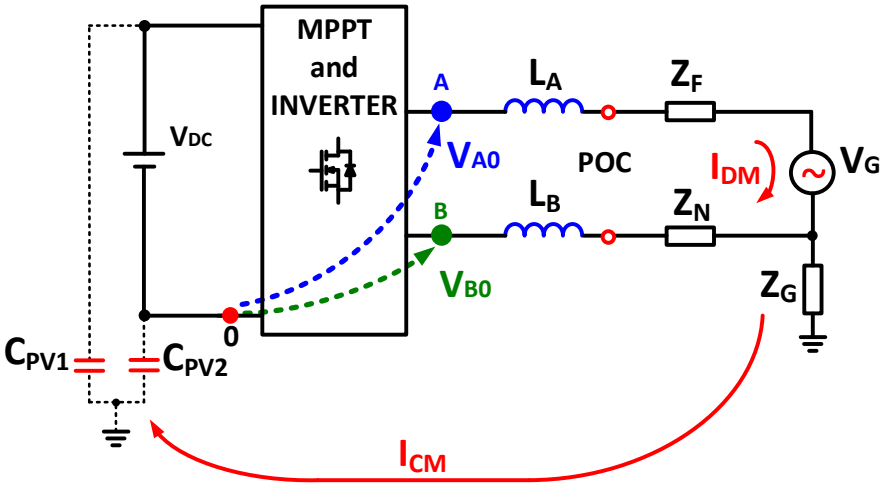


Figure 4.10 – Circuit simulated in PLECS.

All the modulation strategies presented are based on the concepts of switching function and modulation index. The instantaneous value of the output voltages V_{A0} and V_{B0} is defined by binary switching functions s_A and s_B:

$$\begin{cases} V_{A0} = s_A V_{DC} \\ V_{B0} = s_B V_{DC} \end{cases} \tag{4.13}$$

where s_A and s_B can assume only values (0,1).

The average value of V_{A0} and V_{B0} can be controlled each switching cycle T_{SW} by means of the switching functions s_A and s_B:

$$\begin{cases} \overline{V_{A0}} = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_A V_{DC}\, dt = m_A V_{DC} \\ \overline{V_{B0}} = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_B V_{DC}\, dt = m_B V_{DC} \end{cases} \tag{4.14}$$

where m_A and m_B are the leg modulation functions:

$$\begin{cases} m_A = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_A\, dt \\ m_B = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_B\, dt \end{cases}. \tag{4.15}$$

Instantaneous values of s_A and s_B that satisfy relation (4.15) can be generated by well-known Pulse Width Modulation (PWM) strategy. In PWM, a modulation signal is compared with a triangular carrier wave, and the intersections define the switching instants of the output function s. Several waveforms can be adopted for the triangular carrier.

Direct and homopolar modulation functions can be introduced in order to simplify the implementation of the control system:

$$m_D = m_A - m_B \tag{4.16}$$

$$m_O = \frac{m_A + m_B}{2}. \tag{4.17}$$

By using (4.16), (4.17) the leg modulation functions can be written as:

$$m_A = m_O + \frac{m_D}{2} \tag{4.18}$$

$$m_B = m_O - \frac{m_D}{2}. \tag{4.19}$$

Direct modulation function m_D is closely related to the differential output voltage generated by the converter, therefore, it controls the power injected in the electrical grid:

$$V_{AB} = V_{A0} - V_{B0} = (m_A - m_B)V_{DC} = m_D V_{DC}\,. \tag{4.20}$$

Homopolar modulation function m_O is a degree of freedom whose value defines different modulation strategies, it can be used along with PWM carrier to vary the common mode voltage generated by the converter.

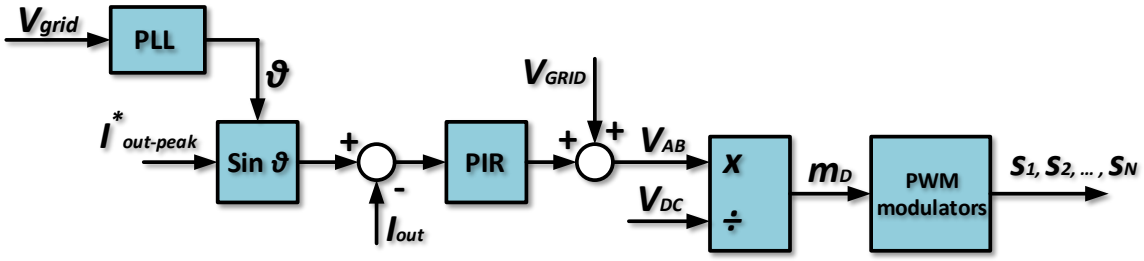


Figure 4.11 - Output current control scheme.

The reference voltage V_{AB} is generated by the current control loop depicted in Figure 4.11. A reference sinusoidal current, synchronized with the grid voltage by means of a single phase PLL module [63], is compared with the phase current of the converter. The current error signal enters in proportional resonant controller (PIR) [64], which generate the reference voltage V_{AB}. The controller is tuned is order to guarantee a stable operation of the converter and a good dynamic response.

4.3.A Full bridge converter (H4)

World most diffused DC/AC power converters are based on the half bridge leg, indeed single phase, three phase and more in general *m*-phase DC to AC two level converters can be obtained connecting together m-half bridge legs.

Figure 4.12 shows a transformerless PV system connected to grid by means of a full bridge converter.

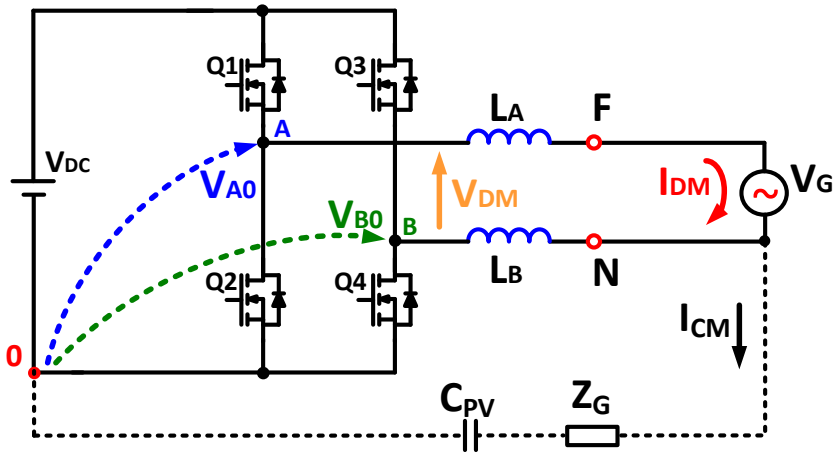


Figure 4.12 – Grid connected full bridge converter.

The converter can be controlled by means of four well known modulation strategies [65]:

- Bipolar modulation.
- Unipolar modulation
- Discontinuous modulation
- Hybrid modulation.

Each modulation strategy has its own advantages and disadvantages as discussed in the following sections.

Bipolar modulation

Bipolar modulation is the simplest modulation strategy that can be used to control the full bridge converter, indeed it requires only one PWM modulator. The switching function s_A is used to control the converter while s_B is substituted by the logical complement of s_A:

$$\begin{cases} V_{A0} = s_A V_{DC} \\ V_{B0} = (1 - s_A) V_{DC} \end{cases}. \tag{4.21}$$

Functions m_A and m_B defined in (4.15) can be written as:

$$\begin{cases} m_A = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_A \, dt \\ m_B = 1 - m_A \end{cases}. \tag{4.22}$$

The differential mode voltage generated by the inverter can be obtained as follows:

$$V_{AB} = V_{A0} - V_{B0} = (m_A - m_B) V_{DC} = (2m_O - 1 + m_D) V_{DC}\,. \tag{4.23}$$

If the homopolar component m_O is equal to 0.5, equation (4.23) becomes:

$$V_{AB} = m_D V_{DC}\,. \tag{4.24}$$

It has been shown that bipolar modulation controls the average value of the output voltage V_{AB} using only one PWM modulator.

The total common mode voltage can be calculated using equation (4.11). If decoupling inductors L_A and L_B are balanced, V_{TCM} can be simplified as:

$$V_{TCM} = V_{CM} = \frac{V_A + V_B}{2}\,. \tag{4.25}$$

Table 4.2 lists the values of V_{A0}, V_{B0}, V_{AB}, V_{CM} and the state of the switches of the converter as function of s_A.

Table 4.2 – Configurations of the converter.

	Switching function	**Switch states**							
	s_A	Q_1	Q_2	Q_3	Q_4	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
Active	1	1	0	0	1	V_{DC}	0	V_{DC}	$\frac{V_{DC}}{2}$
	0	0	1	1	0	0	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$

The table above shows that V_{AB} can only assume the values $+V_{DC}$ and $-V_{DC}$, hence the name bipolar modulation. Table 4.2 shows also that this control strategy has the benefit of maintaining V_{TCM} constant to $V_{DC}/2$.

The full bridge converter with bipolar modulation technique has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A.

The simulation results are presented in Figure 4.13. The waveforms of m_A, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from the top to the bottom. The left part shows one fundamental period of modulating signals (20 ms), while, the right part is a zoomed view of the same waveforms during four switching cycles. The peak of the output current is set to 20A by the high-level control loop. It is worth noting that bipolar modulation maintains constant the total common mode voltage V_{TCM} over the time, therefore, it can limit the circulation of leakage current in PV systems. Even though V_{TCM} is constant, the harmonic content of V_{AB} is worse than the one generated by all the other converters presented in this chapter. Figure 4.14 shows the harmonic content of V_{AB}, it can be noted that all the harmonics multiple of the switching frequency are present. In order to reduce the output current ripple, H4 converter with bipolar modulation requires higher switching frequency or larger decoupling inductors than the other solutions. The usage of a higher switching frequency or larger inductors have the drawback of reduce the overall efficiency of the converter, therefore, it should be avoided.

However, even at the same switching frequency, bipolar modulation generates more losses than unipolar modulations on reactive components of the inverter:

- Bipolar voltage variation ($V_{DC} \rightarrow -V_{DC} \rightarrow V_{DC}$) across the inductor leads to larger minor hysteresis loops than for unipolar case ($V_{DC} \rightarrow 0 \rightarrow V_{DC}$). Thus higher iron core losses are generated.
- In unipolar modulation, the output current freewheels on two transistor during the freewheeling phase ($V_{AB} = 0$). On the contrary, in bipolar modulation, the output current is forced back to the source, increasing then the DC link capacitor losses.

The FB with bipolar modulation, despite it generates a constant V_{TCM}, is generally avoided for use in transformerless PV applications due to the low efficiency [61].

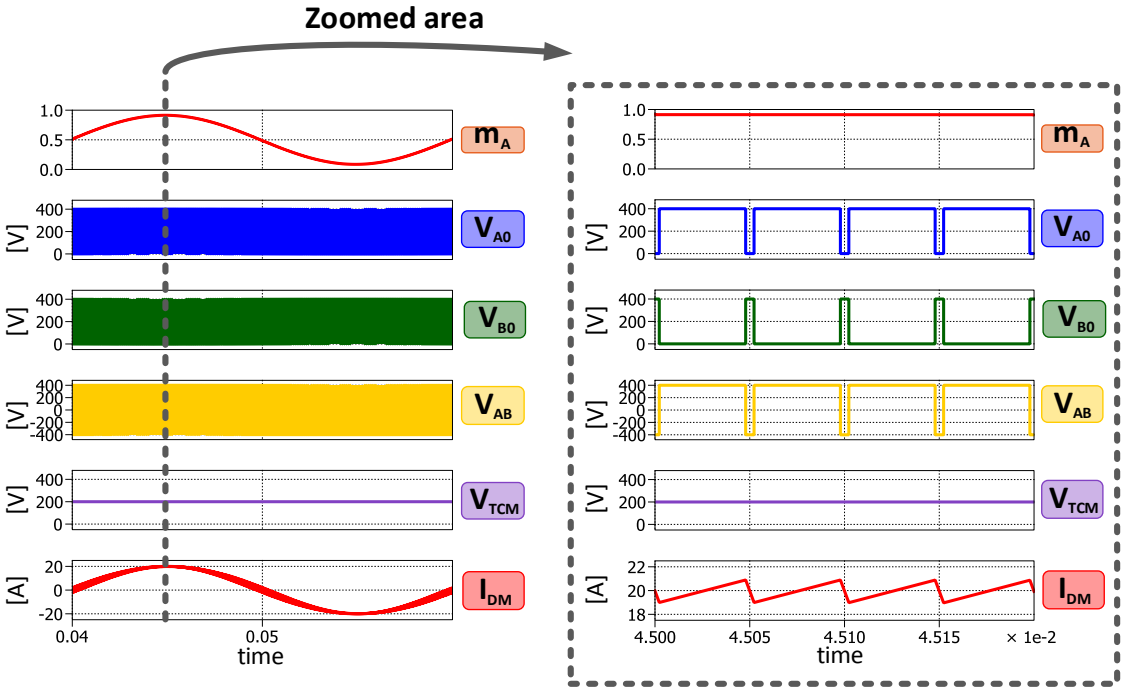


Figure 4.13 – Simulation results of full bridge converter controlled by means of bipolar modulation.

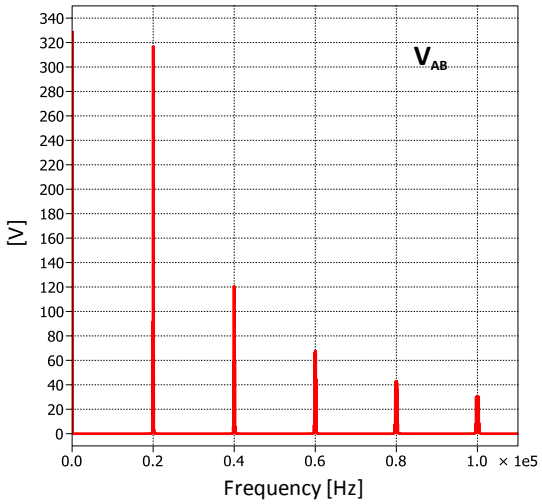


Figure 4.14 – Harmonic content of the output voltage V_{AB} generated by bipolar modulation.

Unipolar modulation

Unipolar Modulation (UM), unlike bipolar modulation, generates three output voltage levels i.e., V_{DC}, 0, and $-V_{DC}$. The two leg of the converter are controlled in such a way that the equivalent switching frequency of V_{AB} is twice the frequency F_{SW}. With the same input voltage V_{DC} and switching frequency F_{SW}, the output voltage V_{AB}, generated by unipolar modulation, has better harmonic content than the one generated by bipolar modulation. Moreover, compared to bipolar modulation, unipolar modulation reduces the iron core losses in the output filter and prevents the reactive power exchange between output filter and DC link capacitor. These properties make unipolar modulation the most diffused modulation strategy for DC/AC FB converters in industrial applications.

The modulation strategy can be obtained imposing m_O equal to:

$$m_O = \frac{1}{2}. \tag{4.26}$$

The leg modulating signals can be obtained as:

$$m_A = \frac{1 + m_D}{2} = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_A \, dt \tag{4.27}$$

$$m_B = \frac{1 - m_D}{2} = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_B \, dt \,. \tag{4.28}$$

The total common mode voltage V_{TCM} can be calculated by using equation (4.11). If decoupling inductors L_A and L_B are balanced, V_{TCM} can be simplified as follows:

$$V_{TCM} = V_{CM} = \frac{V_A + V_B}{2}. \tag{4.29}$$

Table 4.3 shows the switching configurations that can be generated by unipolar modulation each switching cycle. It can be noted that V_{TCM} assumes three voltage levels (0,V_{DC} / 2, V_{DC}), thus this modulation strategy do not keep the common mode voltage at a constant value.

Table 4.3 – Configurations of the converter.

	Switching function		***Switch states***							
	S_A	S_B	Q_1	Q_2	Q_3	Q_4	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
Active	*1*	*0*	*1*	*0*	*0*	*1*	V_{DC}	*0*	V_{DC}	$\frac{V_{DC}}{2}$
	0	*1*	*0*	*1*	*1*	*0*	*0*	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$
Zero	*1*	*1*	*1*	*0*	*1*	*0*	V_{DC}	V_{DC}	*0*	V_{DC}
	0	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*

The full bridge converter with unipolar modulation technique has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A. Figure 4.15 shows the simulation results. The waveforms of m_A, m_B, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from top to bottom.

The simulation confirms that FB converter with unipolar modulation is not suitable for the use in transformerless PV application due to the high frequency harmonic content of the total common mode voltage.

Harmonic content of the output voltage V_{AB} is shown in Figure 4.16, unipolar modulation has the unique feature to cancel the odd voltage harmonics multiple of the switching frequency F_{SW}.

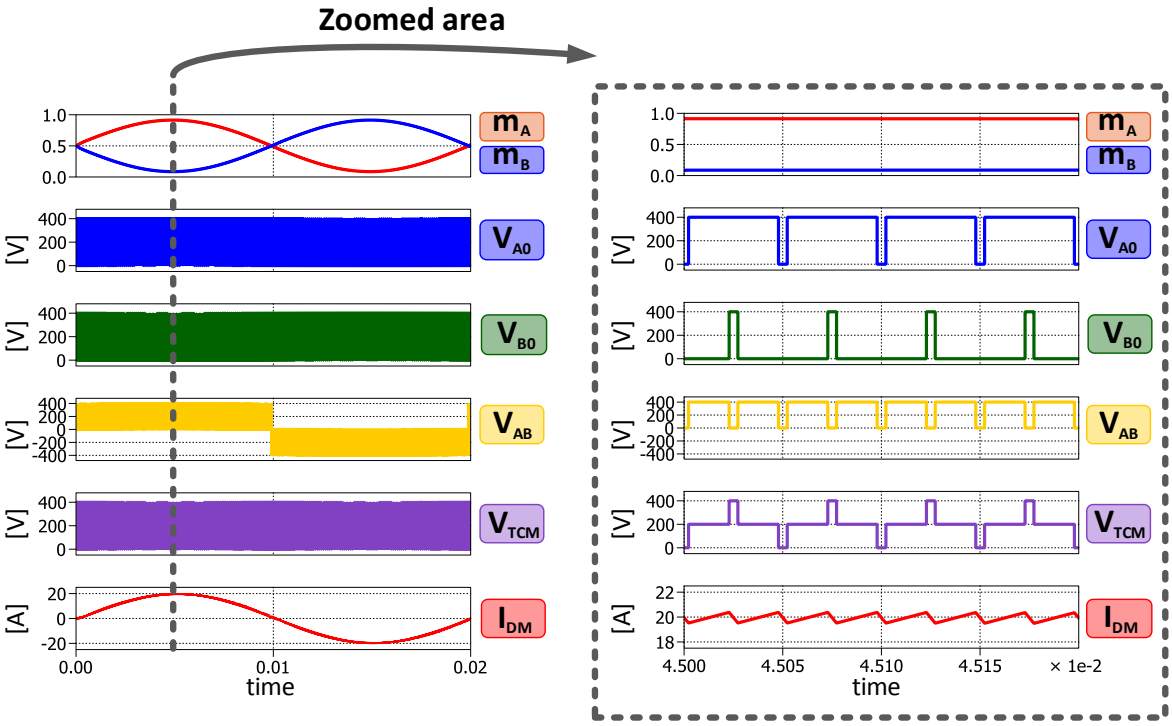


Figure 4.15 - Simulation results of full bridge converter controlled by means of unipolar modulation.

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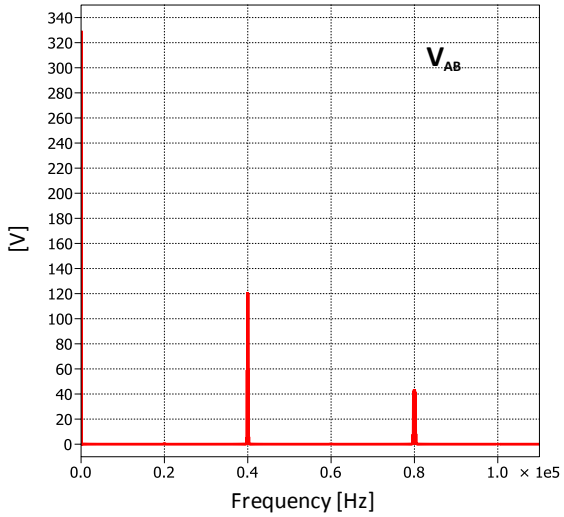


Figure 4.16 - Harmonic content of the output voltage V_{AB} generated by unipolar modulation.

Discontinuous modulation

A common feature of bipolar and unipolar modulations is that, during each switching cycle, both inverter legs are used to modulate the reference voltage V_{AB}^{*}. Discontinuous modulation instead, depending on the sign of V_{AB}^{*}, modulates the output voltage with only one leg while the configuration of the other one remains unchanged for the whole switching cycle. Two modulation strategies can be implemented depending on whether the switching function is kept to zero or one, i.e., high-side or low-side discontinuous modulation. Only the low-side case has been analyzed since both of them generate the same common and differential mode voltages.

The modulation strategy can be obtained by imposing m_O equal to:

$$m_0 = \left|\frac{m_D}{2}\right|. \tag{4.30}$$

The leg modulating signals are can be calculated as:

$$m_A = \frac{|m_D| + m_D}{2} \tag{4.31}$$

$$m_B = \frac{|m_D| - m_D}{2}. \tag{4.32}$$

Depending on the sign of the reference voltage V_{AB}^{*}, modulating signals can be calculated as follows.

$$V_{AB}^{*} > 0 \rightarrow\ m_D > 0 \begin{cases} m_A = m_D \\ m_B = 0 \end{cases} \tag{4.33}$$

$$V_{AB}^{*} < 0 \rightarrow\ m_D < 0 \begin{cases} m_A = 0 \\ m_B = -m_D \end{cases}. \tag{4.34}$$

The total common mode voltage V_{TCM} can be calculated using equation (4.11). If decoupling inductors L_A and L_B are balanced, V_{TCM} can be simplified as:

$$V_{TCM} = V_{CM} = \frac{V_A + V_B}{2}. \tag{4.35}$$

Table 4.4 reports the switching configuration applied by discontinuous modulation. Also in this case, the common mode voltage is not kept constant; it varies between two voltage levels every switching cycle, i.e., 0 and $V_{DC}/2$.

Table 4.4 - Configurations of the converter

		Switching functions		***Switch states***							
		S_A	S_B	Q_1	Q_2	Q_3	Q_4	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
$m_D>0$	*Active*	*1*	*0*	*1*	*0*	*0*	*1*	V_{DC}	*0*	V_{DC}	$\frac{V_{DC}}{2}$
	Zero	*0*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*
$m_D<0$	*Active*	*0*	*1*	*0*	*1*	*1*	*0*	*0*	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$
	Zero	*0*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*

The full bridge converter with discontinuous modulation technique has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A.

Figure 4.17 shows the simulation results, the waveforms of m_A, m_B, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from top to bottom. The left part shows one fundamental period of operation (20 ms), while the right part is a zoomed view of the same waveforms during four switching cycles. The peak of the output current is set to 20A by the high level control loop.

It is worth noting that each leg of the converter commutates at high frequency only for half period (10 ms), hence the name discontinuous modulation.

As in the case of unipolar modulation, the common mode voltage V_{TCM} is not kept at a constant value, however the peak to peak voltage V_{TCM} is reduced from V_{DC} to $V_{DC}/2$. Even though the harmonic content of V_{TCM} is lower, this modulation technique should be avoided for transformerless PV applications too.

The harmonic content of V_{AB} is shown in Figure 4.18, differently than unipolar modulation, all the harmonics at frequencies multiple of the switching frequency are present. However, the high frequency harmonic content of V_{AB} is lower than that generated by bipolar modulation.

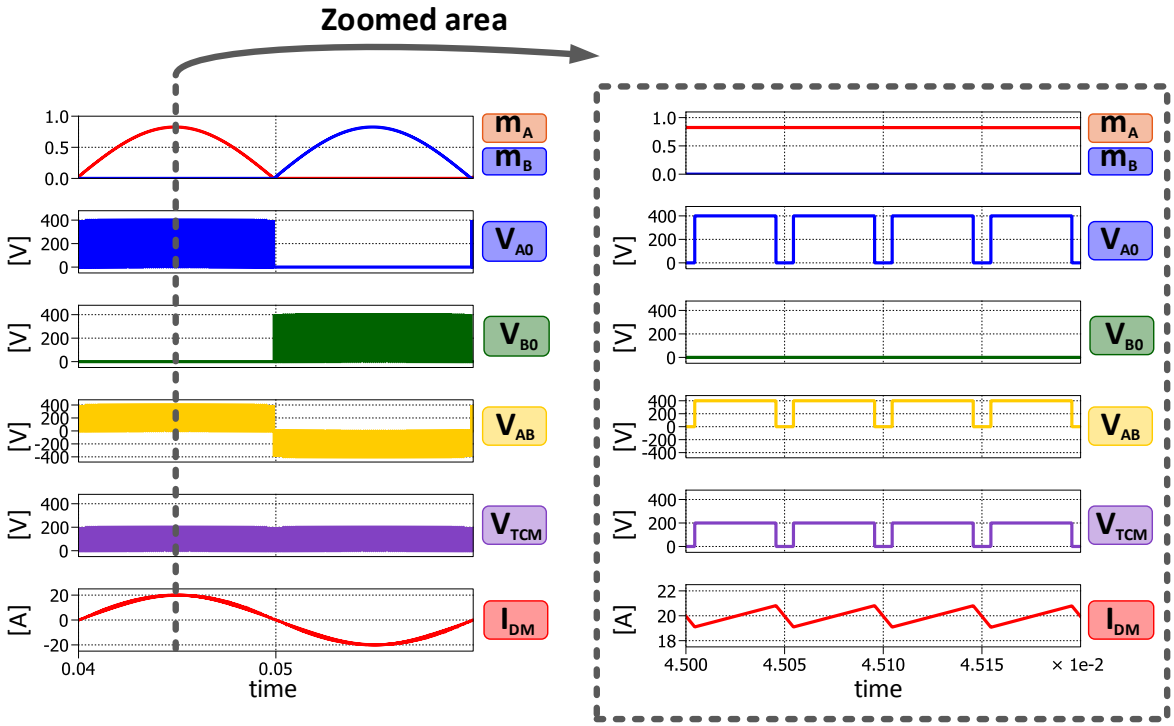


Figure 4.17 - Simulation results of full bridge converter controlled by means of low side discontinuous modulation.

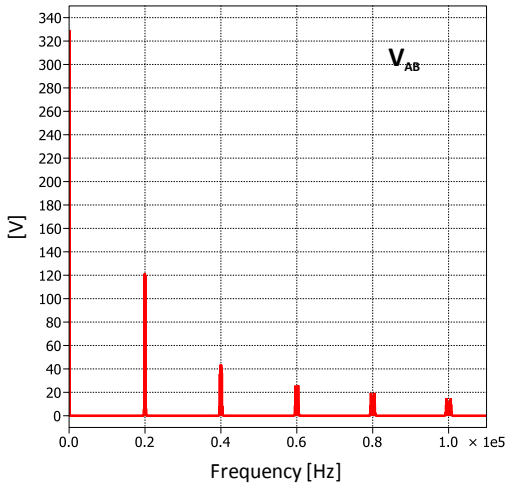


Figure 4.18 - Harmonic content of the output voltage V_{AB} generated by low side discontinuous modulation.

Hybrid modulation

Hybrid modulation is a special case of discontinuous modulation. Leg A of the converter is switched at high frequency while leg B is switched at grid frequency. This modulation scheme requires a specific connection scheme to the grid in order to reduce the common mode voltage generated. Figure 4.19 shows a grid connected full bridge converter controlled by means of hybrid modulation. It can be noted that decoupling inductances L_A and L_B have been grouped on the phase side of the converter. Therefore, no inductance is present between point B and the neutral conductor.

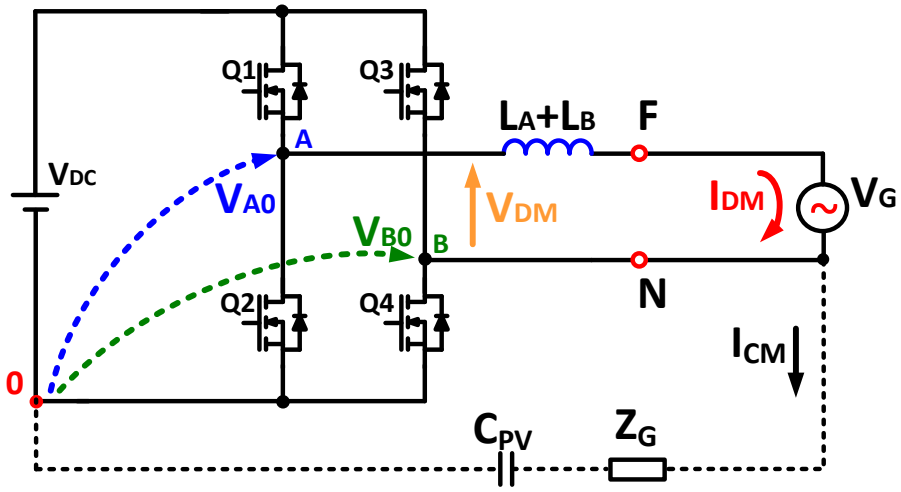


Figure 4.19 - Grid connected full bridge converter controlled by means of hybrid modulation.

The hybrid modulation strategy can be obtained imposing two different m_O, depending on the sign of the reference voltage V_{AB}^*.

$$V_{AB}^* > 0 \rightarrow m_0 = \frac{m_D}{2} \tag{4.36}$$

$$V_{AB}^* < 0 \rightarrow m_0 = 1 + \frac{m_D}{2}. \tag{4.37}$$

Modulating signals can be calculated as follows:

$$V_{AB}^* > 0 \rightarrow m_D > 0 \rightarrow \begin{cases} m_A = m_D \\ m_B = 0 \end{cases} \tag{4.38}$$

$$V_{AB}^* < 0 \rightarrow m_D < 0 \rightarrow \begin{cases} m_A = 1 - |m_D| \\ m_B = 1 \end{cases}. \tag{4.39}$$

The total common mode voltage V_{TCM} can be calculated using equation (4.11). In this case, since decoupling inductors L_A and L_B are unbalanced ($L_B = 0$), V_{DM} contribute to the total common mode voltage too.

$$V_{TCM} = V_{CM} + V_{DM}\frac{L_B - L_A}{2(L_A + L_B)} = V_{CM} - \frac{V_{DM}}{2} = V_{B0}\,. \qquad (4.40)$$

Table 4.5 reports the switching configurations applied by hybrid modulation. It can be noted that the common mode voltage is maintained to V_{DC} if the reference V_{AB}^{*} is positive, while V_{TCM} is maintained to zero if V_{AB}^{*} is negative. Therefore, the total common mode voltage V_{TCM} changes its level at grid frequency.

Table 4.5 - Configurations of the converter.

		Switching functions		***Switch states***							
		S_A	S_B	Q_1	Q_2	Q_3	Q_4	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
$m_D>0$	*Active*	*1*	*0*	*1*	*0*	*0*	*1*	V_{DC}	*0*	V_{DC}	*0*
	Zero	*0*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*0*	*0*
$m_D<0$	*Active*	*0*	*1*	*0*	*1*	*1*	*0*	*0*	V_{DC}	$-V_{DC}$	V_{DC}
	Zero	*1*	*1*	*1*	*0*	*1*	*0*	V_{DC}	V_{DC}	*0*	V_{DC}

The full bridge converter with hybrid modulation technique has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A.

The simulation results are presented in Figure 4.20, the waveforms of m_A,m_B, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from top to bottom during one fundamental period of the grid.

It is worth noting that only leg A of the converter switches at high frequency, while leg B changes its configuration at grid frequency. The total common mode voltage V_{TCM} has a square wave variation at grid frequency, therefore its harmonic content is lower than that generated by unipolar and discontinuous modulation. As discussed in 4.2, not only the common mode voltage determines the leakage current but also the common mode impedance of the decoupling filter of the converter. Figure 4.21 shows the CM equivalent circuit of the PV system, the common mode impedance of decoupling inductors is zero since all the

inductance is on the phase side of the converter. Each time leg B changes configuration, a voltage step of V_{DC} determine an high leakage current peaks, which is limited only by the ground impedance of the system. This drawback prevents the use of hybrid for transformerless PV applications.

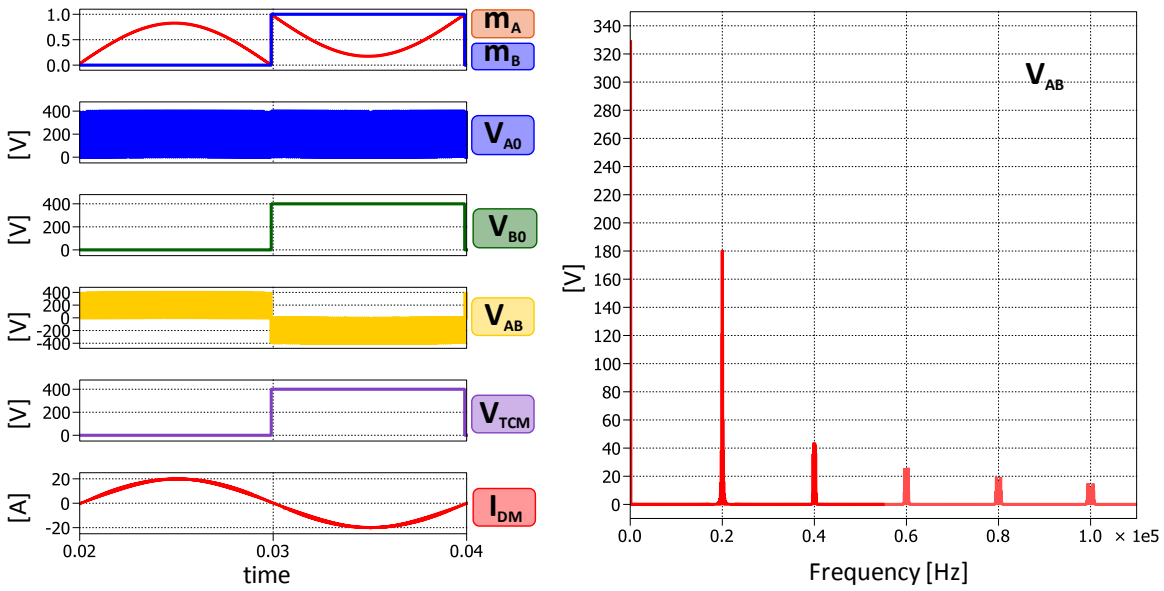


Figure 4.20 - Simulation results and harmonic content of the output voltage V_{AB} in case of full bridge converter controlled by means of hybrid modulation.

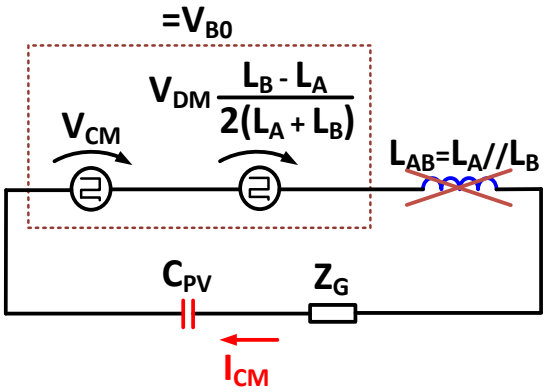


Figure 4.21 – Simplified CM circuit of the full bridge converter controlle by means of hybrid modulation. The total common mode voltage is equal to V_{B0}.

4.3.B H5 converter

It has been shown, in the previous section, that bipolar modulation is the only modulation strategy of the full bridge converter suited for transformerless applications. However, in comparison to unipolar modulations, the output voltage V_{AB} has only 2 levels ($-V_{DC}$, $+V_{DC}$) and the absence of the freewheeling phases ($V_{AB} = 0$) reduces the efficiency of the converter. In order to limit the ripple of the current, high switching frequency or bulky inductors are required, but both solutions further reduce the overall efficiency of the PV system.

H5 topology was proposed and patented in 2005 by SMA to overcome the limitations of H4 inverter [66].

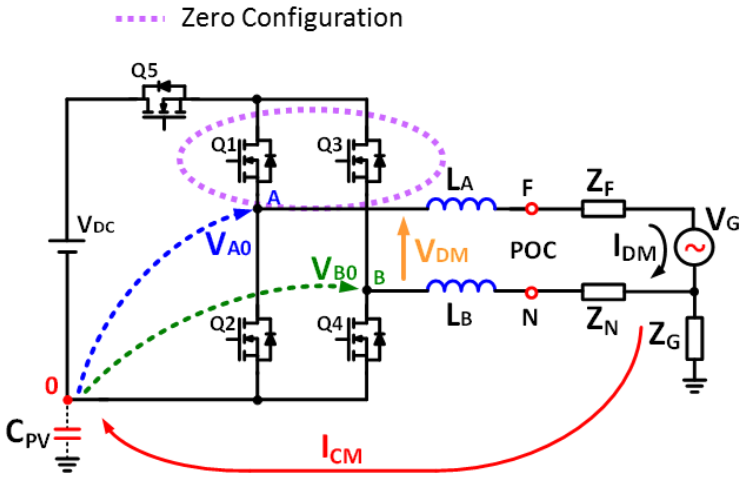


Figure 4.22 - Grid connected H5 converter.

Figure 4.22 shows the H5 inverter, it consists of a full bridge converter with an extra switch Q_5 on the positive side of the dc-link. During active configurations, the operation of H5 inverter is similar to H4 converter. The additional switch Q_5 is closed while diagonal switches of the bridge are controlled in order to generate $V_{AB} = \pm V_{DC}$. The zero voltage configuration $V_{AB} = 0$, instead, is obtained shorting the output by means of switches Q_1 and Q_3, while Q_2, Q_4 and Q_5 are kept open. Left part of Figure 4.23 shows the equivalent circuit of PV system during the active configurations, while the right part, during the zero output configuration. The aim of the fifth switch, along with Q_2 and Q_4, is to disconnect the PV panels from the electric grid during freewheeling phases of the converter. Actually, the prefect disconnection is not possible due to the junction capacitance of power switches, which

is in the range from tens to few hundreds pF. However, a large impedance is inserted in the common mode circuit that reduces the high frequency leakage current.

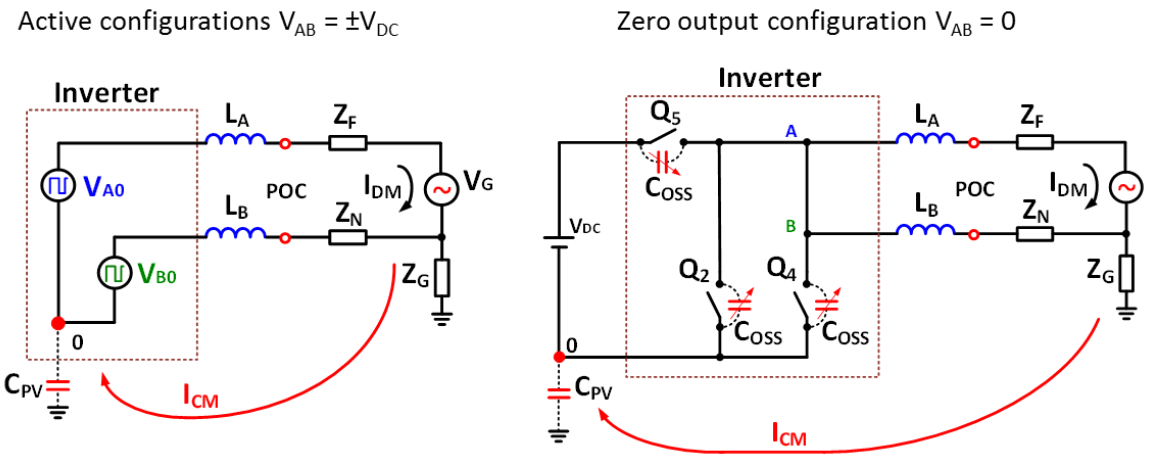


Figure 4.23 – Simplified circuit of the H5 converter during active configurations (left) and zero output configurations (right).

The main bridge is controlled by means of high side discontinuous modulation, while the switching function of Q_5 can be derived as a logic combination of s_A and s_B.

Homopolar component m_O is equal to:

$$m_0 = 1 - \left|\frac{m_D}{2}\right|. \tag{4.41}$$

The leg modulating signals can be calculated as:

$$m_A = 1 - \frac{|m_D| + m_D}{2} \tag{4.42}$$

$$m_B = 1 - \frac{|m_D| - m_D}{2}. \tag{4.43}$$

Depending on the sign of the reference voltage V_{AB}^*, modulating signals can be calculated as follows.

$$V_{AB}^* > 0 \rightarrow\ m_D > 0 \begin{cases} m_A = 1 - m_D \\ m_B = 1 \end{cases} \tag{4.44}$$

$$V_{AB}^* < 0 \rightarrow\ m_D < 0 \begin{cases} m_A = 1 \\ m_B = 1 - |m_D| \end{cases}. \tag{4.45}$$

Switching functions of legs A and B are obtained by means of PWM modulation:

$$m_A = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_A \, dt$$
$$m_B = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_B \, dt \ . \tag{4.46}$$

The switching function s_5 of the additional switch Q_5 can be obtained by means of a logic NAND operation on s_A and s_B:

$$s_5 = \overline{s_A \cdot s_B} \ . \tag{4.47}$$

Table 4.6 shows the switching configuration of the H5 converter.

Table 4.6 - Configurations of the converter.

	Switching function			***Switch states***								
	S_A	S_B	S_5	Q_1	Q_2	Q_3	Q_4	Q_5	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
Active	*1*	*0*	*1*	*1*	*0*	*0*	*1*	*1*	V_{DC}	*0*	V_{DC}	$\frac{V_{DC}}{2}$
	0	*1*	*1*	*0*	*1*	*1*	*0*	*1*	*0*	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$
Zero	*1*	*1*	*0*	*1*	*0*	*1*	*0*	*0*	-	-	*0*	-

The H5 converter has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A.

The simulation results are presented in Figure 4.20. The waveforms of m_A,m_B, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from top to bottom during one fundamental period of the grid.

As discussed before, during the zero output configuration, the grid is connected to DC side of the converter only by means of stray junction capacitance of power switches. Thus the total common mode voltage V_{TCM} is hardware and application dependent, since V_{A0} and V_{B0} are not actively set by the converter.

With respect to bipolar modulation of H4, H5 reduces the losses in reactive components of the converter and generates an output voltage V_{AB} with lower harmonic content. The voltage spectrum of V_{AB}, as depicted in Figure 4.25, is identical to the one generated by discontinuous modulation for full bridge converters. However, higher conduction losses in

power transistors are generated since the output current flows through three switches during the active configurations.

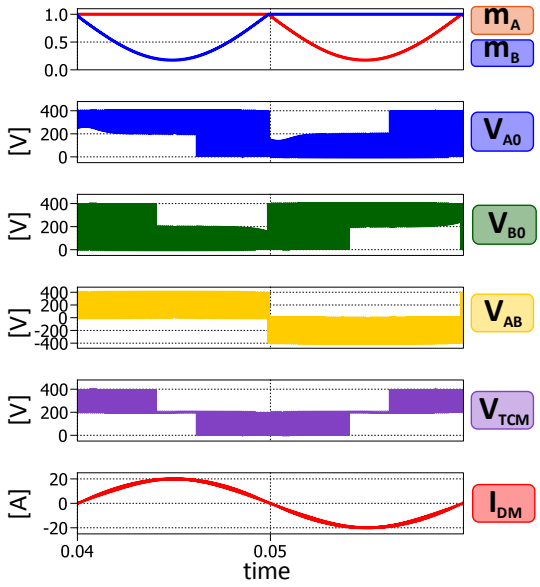


Figure 4.24 - Simulation results of H5 converter controlled by means of high side discontinouos modulation.

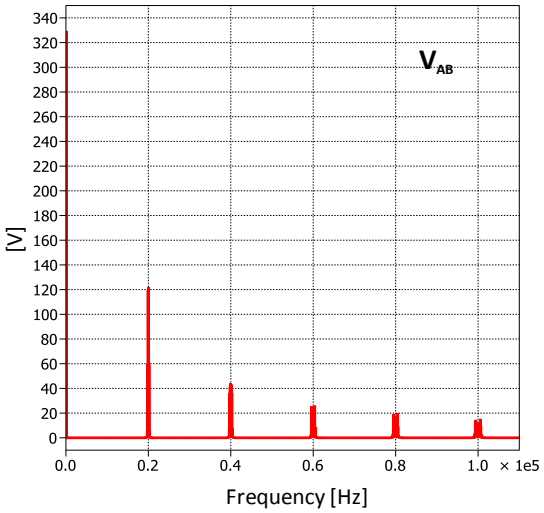


Figure 4.25 - Harmonic content of the output voltage V_{AB} generated by high side discontinouos modulation.

4.3.C H6 converter

In the previous section, it has been shown that H5 converter addresses the problems of the leakage current disconnecting the PV panels to the electric grid during zero output state of the inverter. Therefore, the approach followed is to interrupt the leakage current rather than keeping the total common mode voltage constant.

H6 converter, instead, is an inverter that can be used to actively keep the common mode voltage to a constant value, $V_{DC}/2$. It has been patented by Ingeteam [67] and published in reference [60]. H6 topology is depicted in Figure 4.26. It is composed by a full bridge (H4) with two extra switches Q_5 and Q_6 on the upper and lower side of the DC link. Moreover, the DC link capacitor is split into two parts. The potential of the midpoint is $V_{DC}/2$. Two diodes D_7 and D_8 are connected between the center tap of the capacitors and the input of the bridge. Several modulation strategies have been proposed in literature [68] [69] [70] [71].

During active configurations, the operation of H6 inverter is similar to H4 converter. The DC link switches Q_5 and Q_6 are closed while diagonal switches of the bridge are controlled in order to generate $V_{AB} = \pm V_{DC}$. The total common mode voltage V_{TCM} in both cases is $V_{DC}/2$.

During zero output voltage configuration $V_{AB} = 0$, instead, Q_5 and Q_6 are switched off while all the switches of the bridge are turned on. In this condition, the diodes D_7 and D_8 clamp the voltages V_{A0} and V_{B0} to $V_{DC}/2$, therefore the leakage current is reduced since V_{TCM} is maintained to a constant value. It is worth mentioning that the short circuit of the bridge guarantee that V_{TCM} is clamped to $V_{DC}/2$, regardless the sign of the output current.

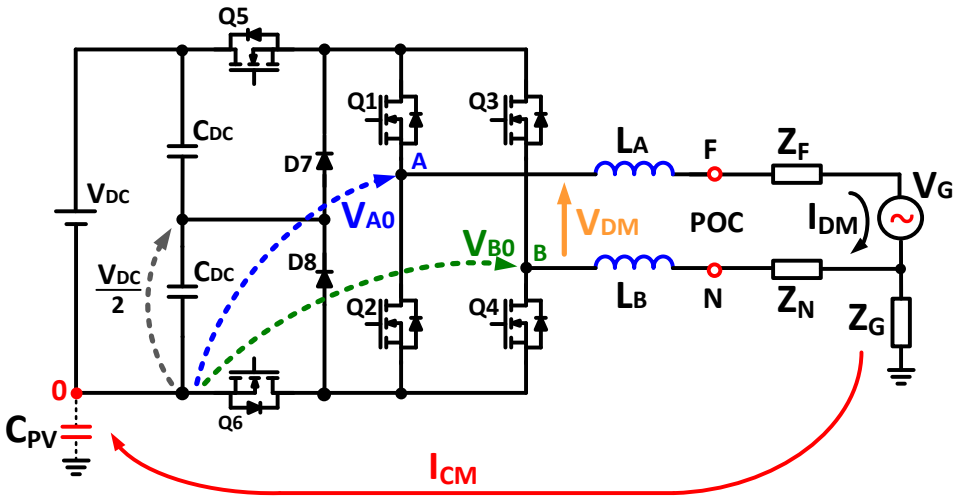


Figure 4.26 - Grid connected H6 converter.

The proper operation of the converter requires the possibility to close all the switches of the bridge. This situation is not allowed using one switching function per leg since only one switch at time can be turned on i.e., the top or the bottom switch. In order to control the converter, a different mathematical approach has to be defined. Switches Q_1 and Q_4 are controlled by the same modulating signal m_{14}, while Q_2 and Q_3 are controlled by the modulating signal m_{23}:

$$m_{14} = 1 - \frac{|m_D| + m_D}{2} \tag{4.48}$$

$$m_{23} = 1 + \frac{|m_D| + m_D}{2}. \tag{4.49}$$

The switching function of the switches of the bridge can be obtained by means of two PWM modulators, which generate s_{14} and s_{23}:

$$\begin{cases} m_{14} = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_{14}\, dt \\ m_{23} = \dfrac{1}{T_{SW}} \displaystyle\int_0^{T_{SW}} s_{23}\, dt \end{cases}. \tag{4.50}$$

Switches Q_5 and Q_6 are controlled by the same switching function s_{56}, which can be obtained by means of logic NAND operation on s_{14} and s_{23}: Configurations of the converter

$$s_{56} = \overline{s_{14} \cdot s_{23}} \tag{4.51}$$

Table 4.7 shows the switching configuration of the H6 converter. It can be noted that the common mode voltage is equal to $V_{DC}/2$ for all active and zero configurations of the converter, i.e., the leakage current is reduced.

Table 4.7 - Configurations of the converter

	Switching function			***Switch states***									
	$S_{1\text{-}4}$	$S_{2\text{-}3}$	$S_{5\text{-}6}$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
Active	1	0	1	1	0	0	1	1	1	V_{DC}	0	V_{DC}	$\frac{V_{DC}}{2}$
	0	1	1	0	1	1	0	1	1	0	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$
Zero	1	1	0	1	1	1	1	0	0	$\frac{V_{DC}}{2}$	$\frac{V_{DC}}{2}$	0	$\frac{V_{DC}}{2}$

The simulation results carried out by PLECS are presented in Figure 4.27. The waveforms of m_{14},m_{23}, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from the top to the bottom during one fundamental period of the grid. It is worth noting that the clamping diodes make V_{A0} and V_{B0} to commutate by the voltage step $V_{DC}/2$ instead of the full DC link voltage, as in a standard H4 converter. This characteristic of operation reduces the switching losses of the main switches of the converter. However, higher conduction losses in power transistors are generated since the output current flows through four switches during the active configurations.

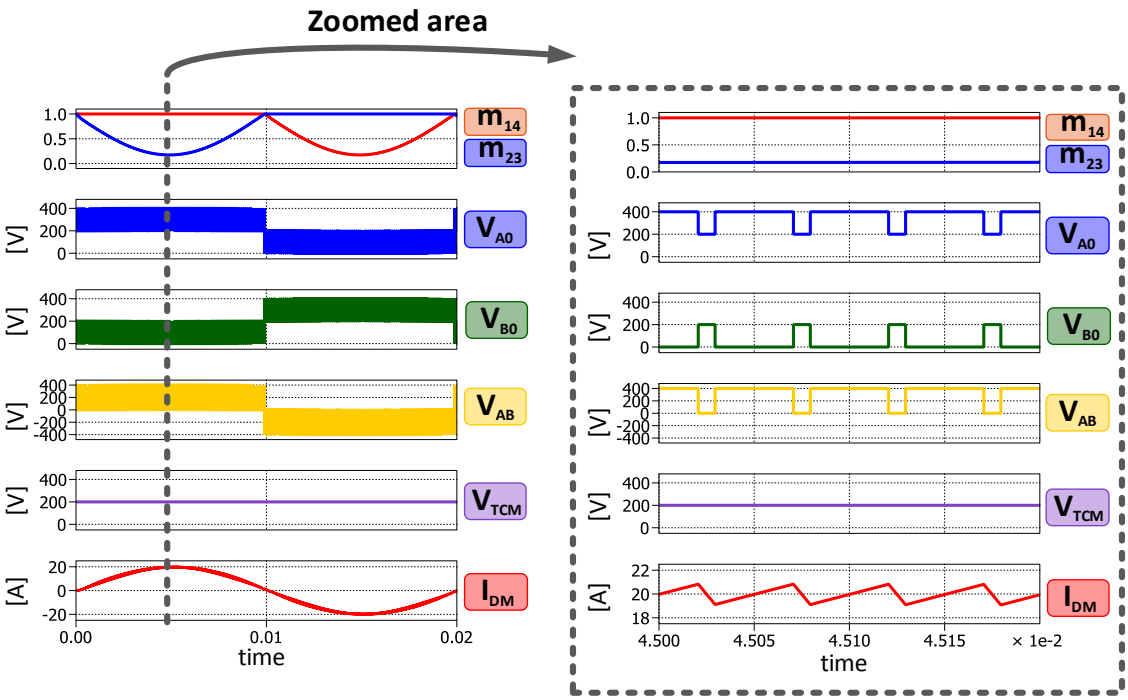


Figure 4.27 - Simulation results of H6 converter.

With respect to bipolar modulation of H4, the H6 reduces the losses in reactive components of the converter and generates an output voltage V_{AB} with lower harmonic content. The voltage spectrum of V_{AB}, as depicted in Figure 4.28 is identical to the one generated by discontinuous modulation of full bridge converter.

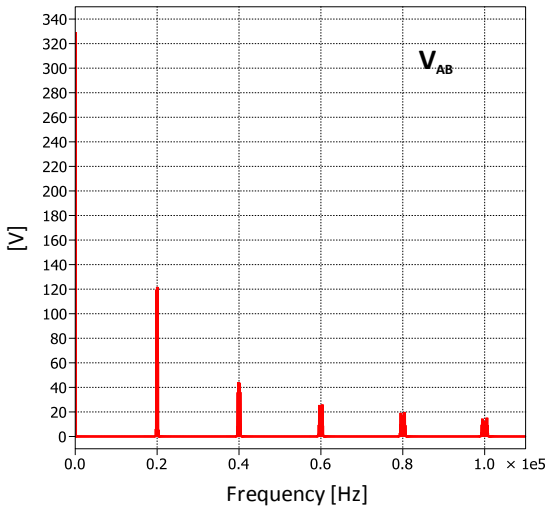


Figure 4.28 - Harmonic content of the output voltage V_{AB}.

4.3.D H6 converter – unipolar modulation

The control technique of H6 presented so far guarantees a constant common mode voltage regardless the sign of the output current. H6 topology can be also controlled by a modulation technique that combines the advantages of the unipolar modulation of H4 (equivalent switching frequency of V_{AB} is twice the frequency F_{SW}), with the leakage current reduction of the H5 converter.

Legs A and B of the bridge are controlled by means of the unipolar modulation presented in paragraph 4.3.A. The switch Q_5 is turned off every time the main bridge applies an high side null configuration, and the PV panels has to be disconnected from the grid. In the same way, Q_6 is turned off every time the bridge applies a low side null configuration. Similarly to the case of H5 converter, the common mode voltage during zero configurations depend on the stray junction capacitance of the switches, however, the diodes D_7 and D_8 may clamp V_{TCM} to $V_{DC}/2$, depending on the sign of the output current.

The main bridge is controlled by means of unipolar modulation, while the switching function of Q_5 can be derived as a logic combination of s_A and s_B.
Homopolar component m_O is equal to:

$$m_0 = \frac{1}{2}. \tag{4.52}$$

The leg modulating signals can be calculated as:

$$m_A = \frac{1 + m_D}{2} = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_A \, dt \tag{4.53}$$

$$m_B = \frac{1 - m_D}{2} = \frac{1}{T_{SW}} \int_0^{T_{SW}} s_B \, dt \, . \tag{4.54}$$

The switching function s_5 and s_6 of the addition switch Q_5 can be obtained by means of logic operation on s_A and s_B:

$$s_5 = \overline{s_A \cdot s_B} \tag{4.55}$$

$$s_6 = s_A + s_B \, . \tag{4.56}$$

Table 4.8 - Configurations of the converter.

	Switching function				Switch states									
	S_A	S_B	S_5	S_6	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	V_{A0}	V_{B0}	V_{AB}	V_{TCM}
Active	1	0	1	1	1	0	0	1	1	1	V_{DC}	0	V_{DC}	$\frac{V_{DC}}{2}$
	0	1	1	1	0	1	1	0	1	1	0	V_{DC}	$-V_{DC}$	$\frac{V_{DC}}{2}$
Zero	1	1	0	1	1	0	1	0	0	1	-	-	0	-
	0	0	1	0	0	1	0	1	1	0	-	-	0	-

The H6 converter with unipolar modulation technique has been simulated using PLECS, the parameters of the model and the implemented control loop are described in section 4.3.A. Figure 4.29 shows the simulation results, the waveforms of m_A, m_B, V_{A0}, V_{B0}, V_{AB}, V_{TCM} and I_{DM} are plotted from the top to the bottom.

Harmonic content of the output voltage V_{AB} is shown in Figure 4.30. Unipolar modulation has the unique feature to cancel the odd voltage harmonics multiple of the switching frequency F_{SW}, which in this case is 20kHz.

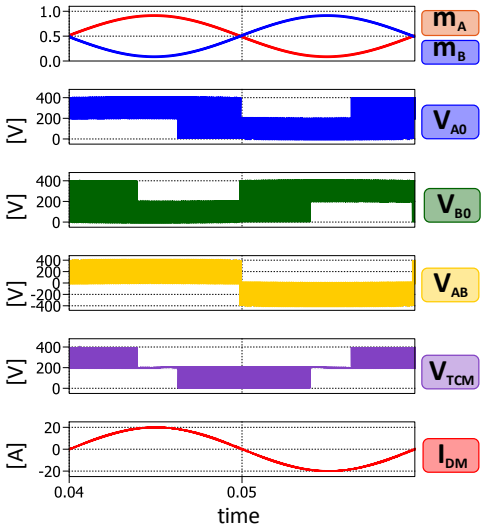


Figure 4.29 - Simulation results H6 converter controlled by means of unipolar modulation.

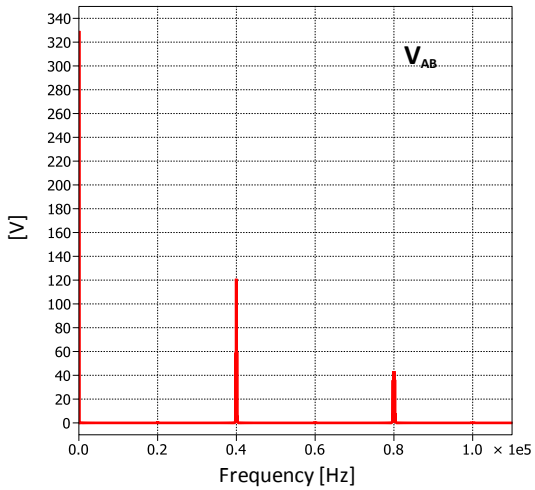


Figure 4.30 - Harmonic content of the output voltage V_{AB} generated by unipolar modulation.

4.4 Experimental results

H6 converter is the most complex topology described in section 4.3. It includes all the elements of full bridge and H5 converters. Giving that H6 can be reconfigured as three different converters, a H6 prototype has been designed and fabricated in order to experimentally compare the efficiency and the leakage current generated by different modulation strategies.

4.4.A Design of a H6 converter

Figure 4.31 shows the H6 prototype. The converter is rated for a DC link of 400 V and a phase current of 16 A_{RMS}. The power stage consists of discrete power components mounted on an exposed heatsink. Therefore, during experimental tests, the accurate measure of the temperature of the power switches is possible by means of an infrared (IR) camera. This feature allows to evaluate the effect of the different modulation techniques on the thermal stress of each component. The thermal resistance of the heatsink, under natural cooling condition, is nearly 1.4 ÷ 1.5 °C/W. Such a large value has been selected so that small variation of the dissipated power leads to a variation of the temperature of the heatsink appreciable by IR measurements.

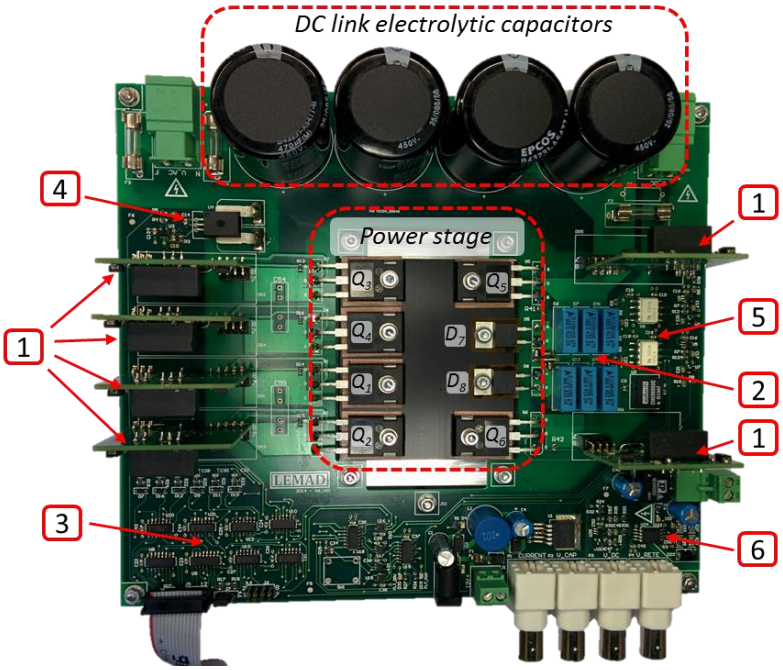


Figure 4.31 – Picture of the H6 converter prototype.

The prototype has been designed also with the aim to be a test bench platform for different power switch technologies, thus, reconfigurable gate driver circuits have been adopted. Labels "1" of Figure 4.31 identify the six gate driver circuits of the converter. Each one consists of the standalone circuit depicted in Figure 4.32.

Two versions of the converter have been built, one using high-performance Si IGBTs (Infineon IKW40N65H5), and one using high-switching speed SiC MOSFETs C2M0080120D, produced by CREE [72]. These two devices require a different driving voltage and gate resistance in order to maximize their static and dynamic performances, thus, two different gate driver boards have been built.

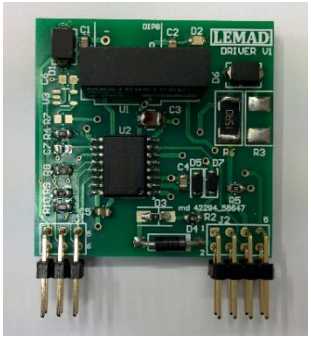


Figure 4.32 – Picture of the gate driver board.

The DC bus is composed of electrolytic capacitors and metallized polypropylene film capacitors, as shown in Figure 4.31. In single phase PV systems, the DC link capacitor decouples the constant power generated by PV panels, to the pulsating AC power injected in the grid. This situation, for the sake of clarity, is depicted in Figure 4.33. The DC bus voltage and its second harmonic ripple are computed by the balance of input and output powers in the inverter, and may be approximated by the following expression, given in [73] [74]:

$$v_{DC}(t) = \overline{V_{DC}} + \frac{P_{PV}}{2\omega_G C_{DC} \overline{V_{DC}}} \sin(2\omega_G t) \tag{4.57}$$

where $\overline{V_{DC}}$ is the average DC bus voltage, P_{PV} is the power generated by the PV panels, ω_G is the frequency of the grid, and C_{DC} is the DC link capacitance. The maximum ripple of v_{DC} can be controlled by properly selecting the capacity of the DC link:

$$\frac{P_{PV,max}}{2\omega_G C_{DC} \overline{V_{DC}}} < \frac{V_{PP,max}}{2}. \tag{4.58}$$

A total capacity of 560 µF has been selected in order to limit the peak to peak voltage ripple below 30V, when the converter operates at 400V and the input power is 2000W:

$$C_{DC} > \frac{P_{PV,max}}{\omega_G \overline{V_{DC}}\, V_{PP,max}} = 530\ \mu F\ . \tag{4.59}$$

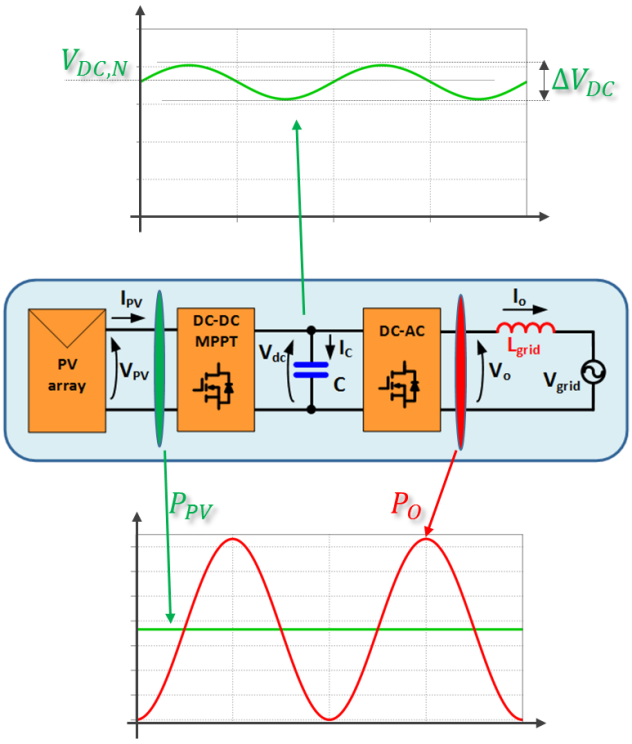


Figure 4.33 – Power balance on the DC link capacitor of a single phase PV system.

The converter is controlled by an external DSP board, therefore, it is designed for the reception of the PWM signals, and for the transmission of analog feedback measures.
The PWM receiver module of the converter is pointed out by label 3 of Figure 4.31. Labels 4, 5, and 6 of the same figure show, respectively, the isolated measurement circuits of the output current, of the DC link voltage, and of the grid voltage.

4.4.B Leakage current test

In section 4.3, different modulation techniques for H4, H5, and H6 inverters have been presented. Each strategy generates a common mode voltage that may or may not be suited for the use in transformerless PV systems. Moreover, converters that reduces the leakage current disconnecting the PV panels from the electric grid during zero output configuration,

cannot be accurately simulated using system level programs, like PLECS. For this reason, the leakage current generated by each inverter has been measured experimentally for comparison purpose.

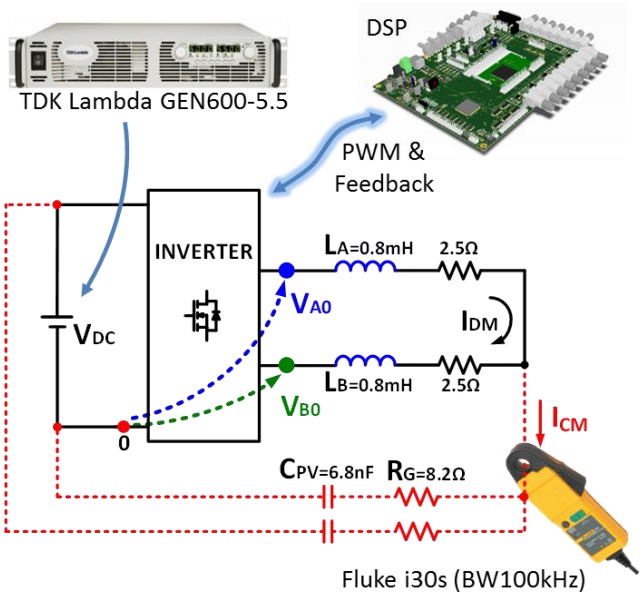


Figure 4.34 – Experimental test setup.

Figure 4.34 shows the test setup used to compare the modulation strategies presented in section 4.3. The tests have been carried out at reduced DC link voltage of 70 V. In order to make results reproducible and independent from the POC of the system, the power grid has been replaced by an ohmic inductive load.

The common mode current generated flows back to the DC side of the converter by means of two R-C circuits, which simulate the ground resistance and the capacitance of the PV panels.

A Fluke i30s current probe, which has a bandwidth of 100 kHz, has been used to measure the CM current. Thus, the RMS value of the leakage current has been calculated considering only spectral components below 100 kHz.

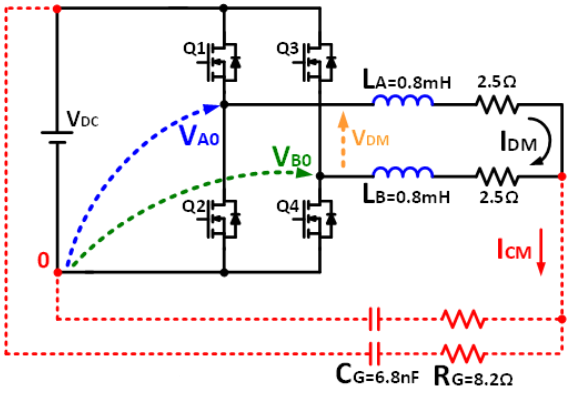
The control algorithm depicted in Figure 4.11 has been implemented, in discrete time [75], on a control board based on a floating point Digital Signal Processor (DSP) TMS320F28335. The switching frequency is the same for all the tests, 20kHz, and the output peak current is set to 5 A – 50 Hz.

The converter endowed with Si IGBTs has been used for the leakage current test.

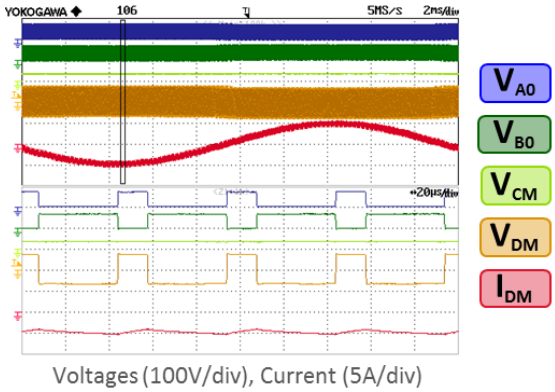
H4 converter with bipolar modulation

Figure 4.35 shows the test set setup and the experimental results obtained. In b) it can be noted that the output voltage V_{AB} generated by the bipolar modulation has only two levels. The output current I_{DM} has the higher ripple among all the tested solutions.

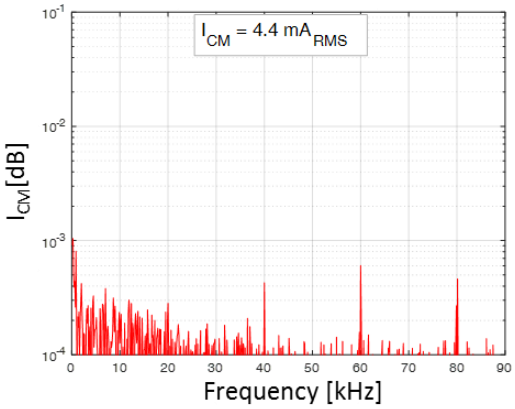
Figure a) shows the test setup, it can be noted that the load is symmetric, therefore, V_{TCM} is equal to V_{CM}. In d) it can be observed that the bipolar modulation keeps nearly constant V_{CM}, therefore, the leakage current is extremely low. This is confirmed by the spectral analysis of the leakage current depicted in graph c), the RMS value of I_{CM} is 4.4 mA_{RMS}.



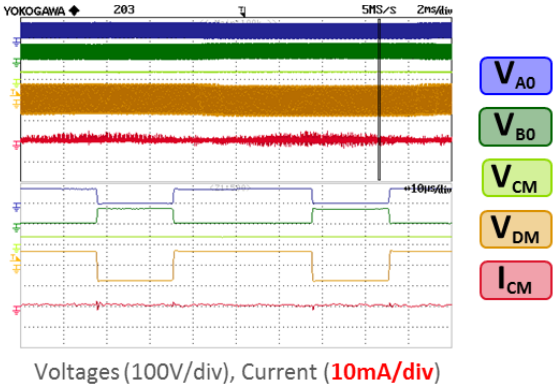
a) Test setup



b) Differential mode results



c) Harmonic content of the leakage current



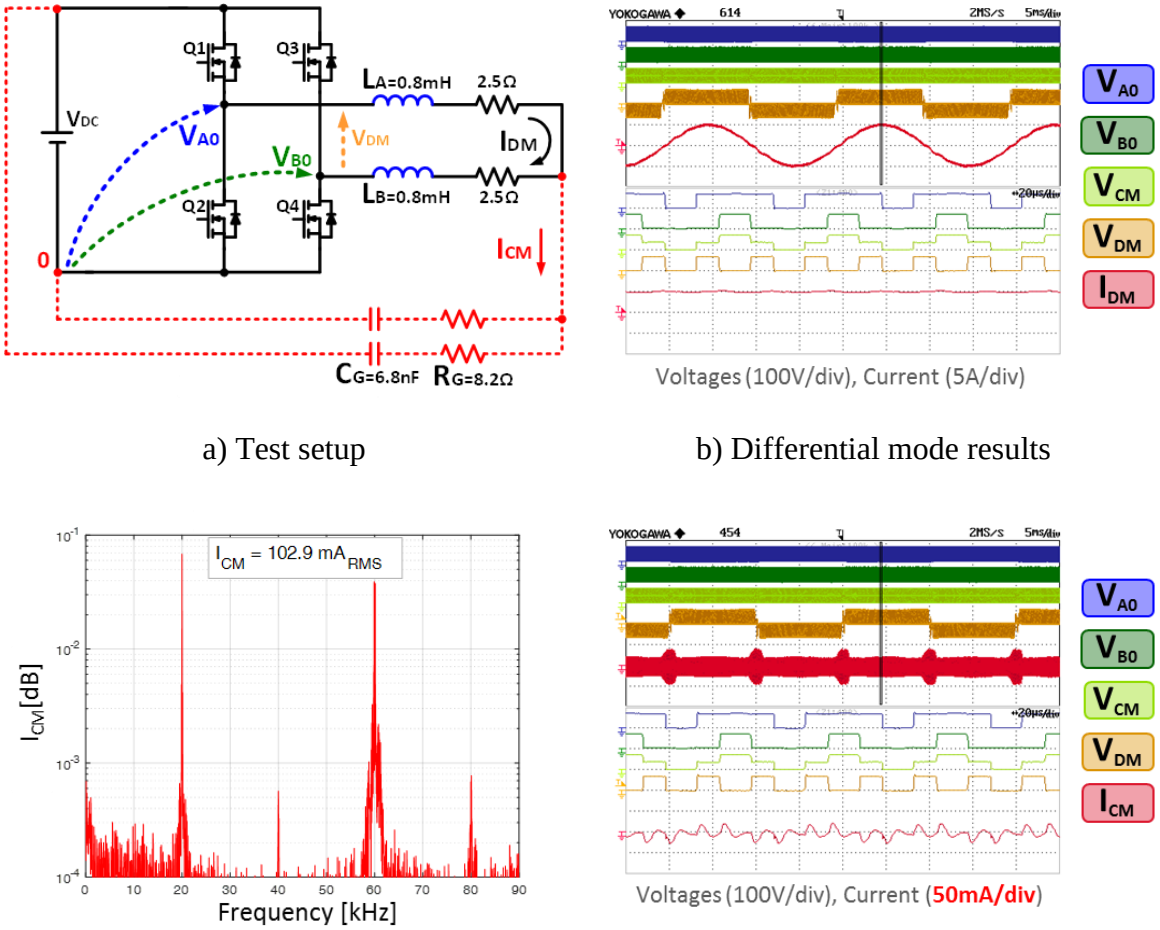
d) Common mode results

Figure 4.35 – Experimental results of full bridge converter controlled by means of bipolar modulation.

H4 converter with unipolar modulation

Figure 4.36 shows the test set setup and the experimental results obtained. In b) it can be noted that the output voltage V_{AB} has three levels and its equivalent switching frequency is twice that of V_{A0} and V_{B0}.

Also in this case, the load is symmetric, therefore, V_{TCM} is equal to V_{CM}. In d) it can be observed that the common mode voltage has a high frequency harmonic content, therefore, large leakage current is generated. This is confirmed by the spectral analysis of the leakage current depicted in graph c), the RMS value of I_{CM} is 102.9 mA_{RMS}.



a) Test setup

b) Differential mode results

c) Harmonic content of the leakage current

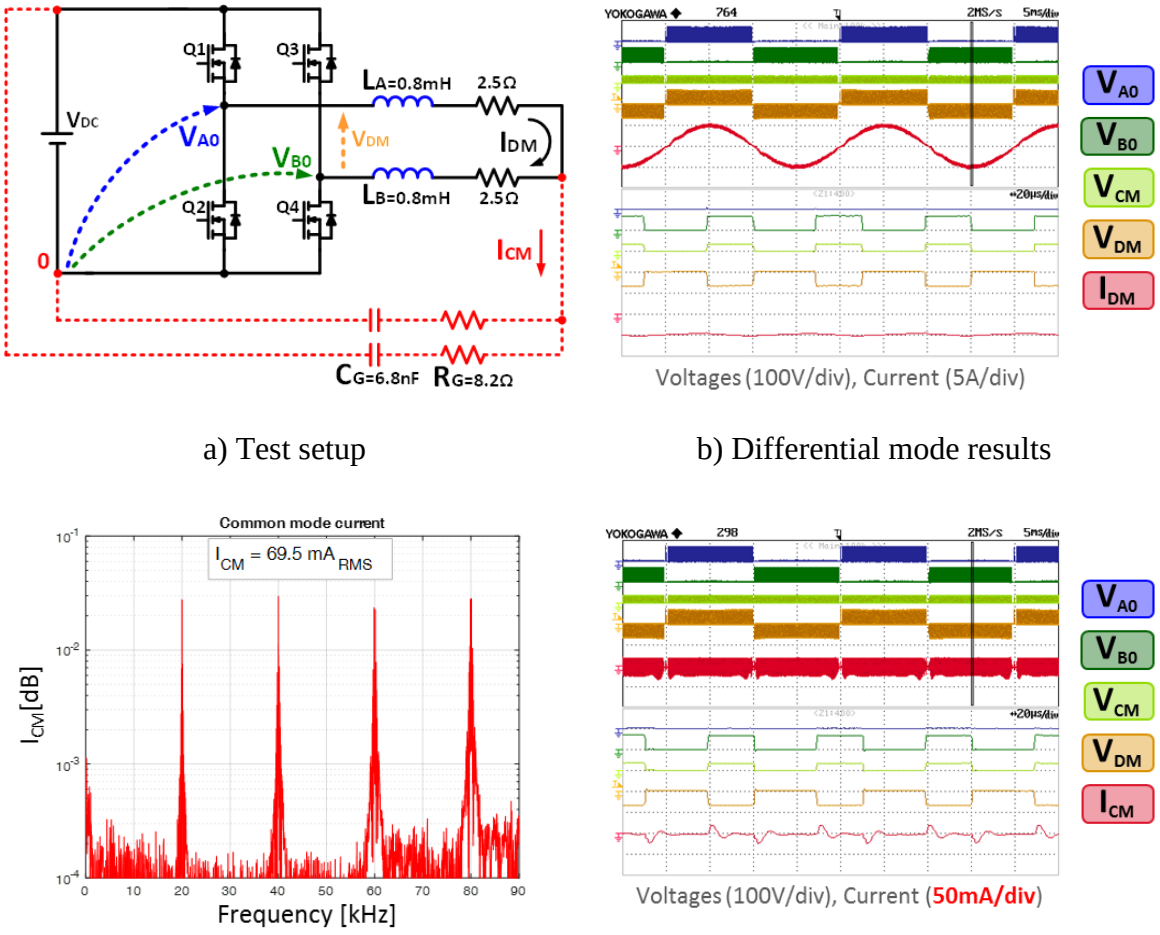
d) Common mode results

Figure 4.36 - Experimental results of full bridge converter controlled by means of unipolar modulation.

H4 converter with discontinuous modulation

Figure 4.37 shows test set setup and the experimental results obtained. In b) it can be noted that the output voltage V_{AB} has three levels, and that legs A and B modulate once at time.

Also in this case, the load is symmetric, therefore, V_{TCM} is equal to V_{CM}. In d) it can be observed that the common mode voltage has a high frequency harmonic content, therefore, large leakage current is generated. This is confirmed by the spectral analysis of the leakage current depicted in graph c), the RMS value of I_{CM} is 69.5 mA_{RMS}.



a) Test setup

b) Differential mode results

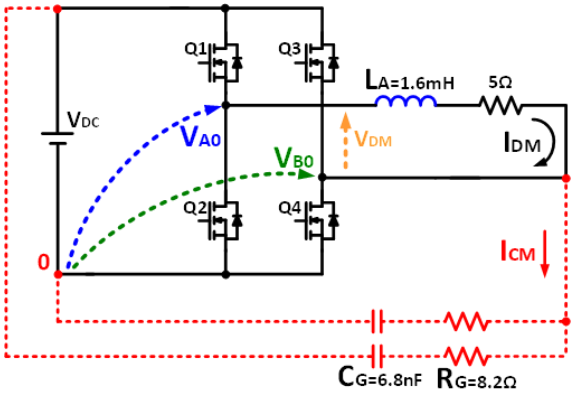
c) Harmonic content of the leakage current

d) Common mode results

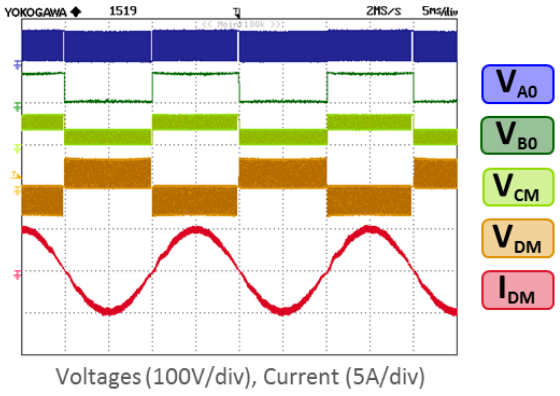
Figure 4.37 - Experimental results of full bridge converter controlled by means of discontinuous modulation.

H4 converter with hybrid modulation

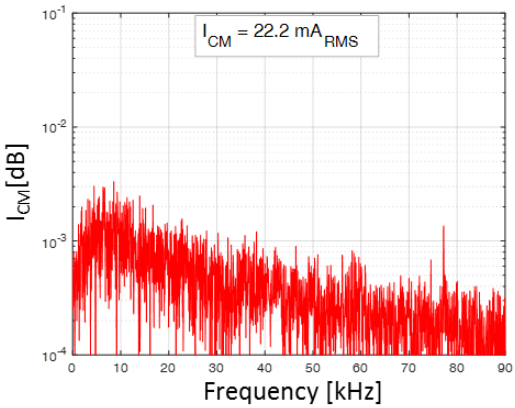
Figure 4.38 shows the test set setup and the experimental results obtained. Hybrid modulation has the unique characteristic of modulate leg A at high frequency, and leg B at grid frequency. It can be noted in figure a) that decupling inductors and load resistances have been grouped on the phase side of the converter. This specific arrangement, as discussed in paragraph 4.3.A, makes V_{TCM} equal to V_{B0}. The total common mode voltage appears as a square wave, varying at grid frequency. Figure d) confirm that every time leg B changes configuration, a voltage step V_{DC} determine leakage current peaks higher than 1 A, which are limited only by R_G and the parasitic inductance of the circuit. The spectral analysis of the leakage current is depicted in graph c), its RMS value is 22.2 mA_{RMS}.



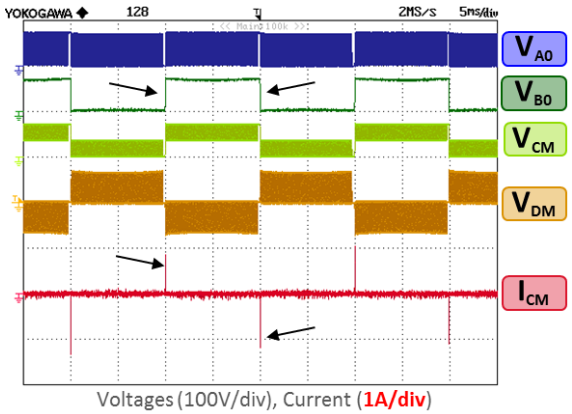
a) Test setup



b) Differential mode results



c) Harmonic content of the leakage current

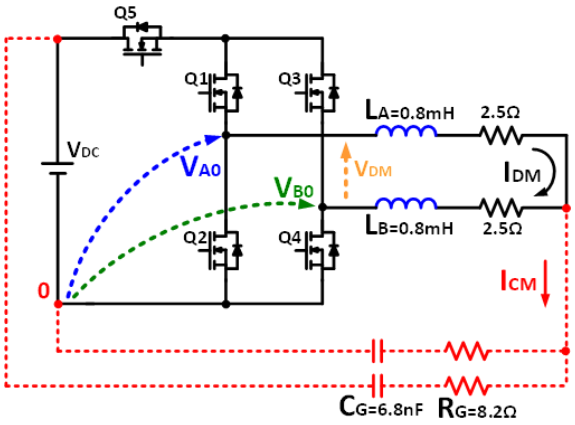


d) Common mode results

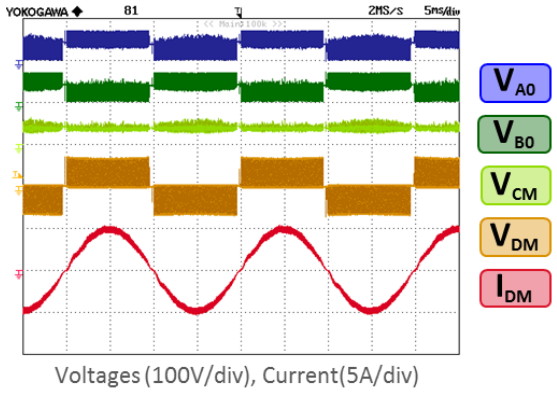
Figure 4.38 - Experimental results of full bridge converter controlled by means of hybrid modulation.

H5 converter

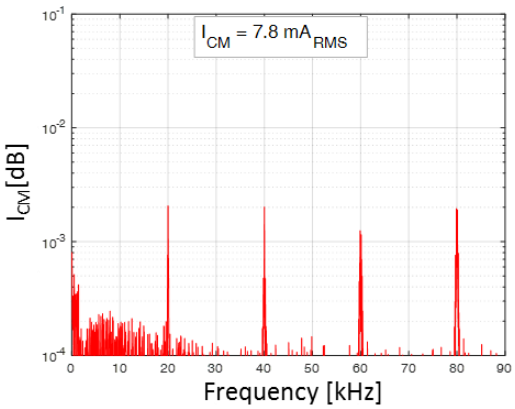
Figure 4.39 shows the test set setup and the experimental results obtained. The bridge of the converter is controlled by means of high side discontinuous modulation, while switch Q_5 disconnects the DC side from the AC side during zero output configurations. The output voltage has the same characteristic of discontinuous modulation of H4, whereas the common mode voltage is hardware dependent. In d) it can be noted that voltage V_{A0} and V_{B0}, when V_{AB} is zero, are not actively imposed by the converter to any value. The effectiveness of this converter is shown in graph c), the RMS value of the leakage current is reduced to 7.8 mA_{RMS}. The H4 converter controlled by means of the same discontinuous modulation strategy generates a leakage current that is 9 times higher.



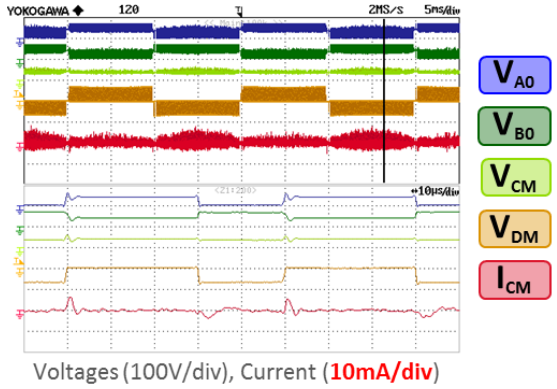
a) Test setup



b) Differential mode results



c) Harmonic content of the leakage current

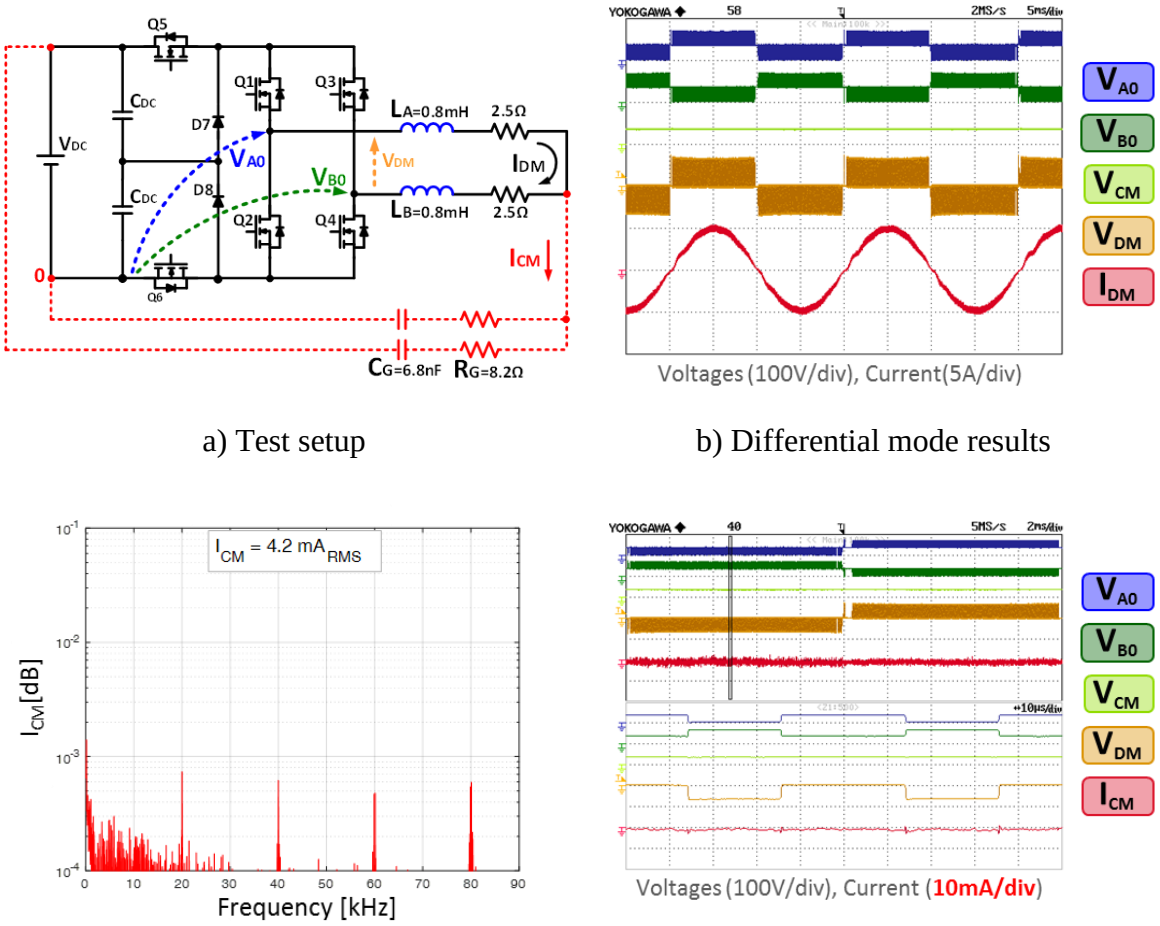


d) Common mode results

Figure 4.39 - Experimental results of H5 converter.

H6 converter

Figure 4.40 shows the test set setup and the experimental results obtained. The aim of H6 converter is to actively keep the common mode voltage to a constant value $V_{DC}/2$. This characteristic is confirmed by the waveforms depicted in plot d). Since V_{TCM} is nearly constant over time, the RMS value of the leakage current is greatly reduced. The spectral analysis of the leakage current is depicted in graph c). The RMS value of I_{CM} is 4.2 mA_{RMS}, a value that is close to that obtained by bipolar modulation of H4 converter.



a) Test setup

b) Differential mode results

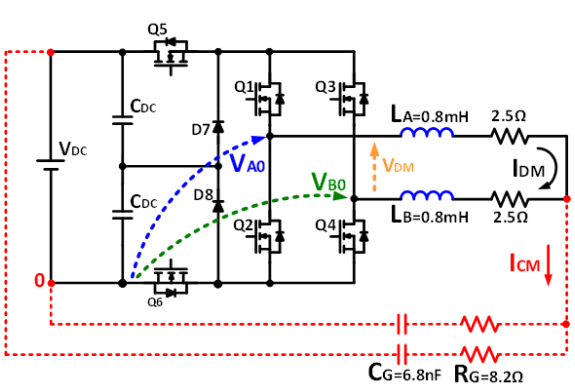
c) Harmonic content of the leakage current

d) Common mode results

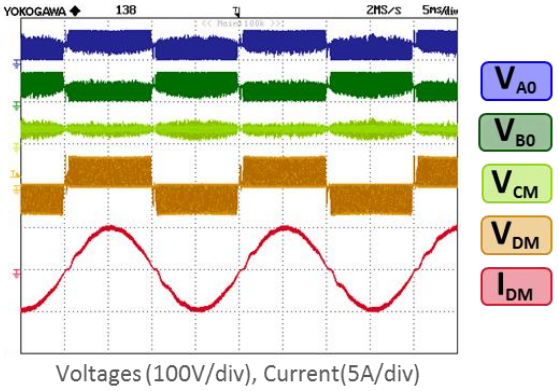
Figure 4.40 - Experimental results of H6 converter.

H6 converter with unipolar modulation

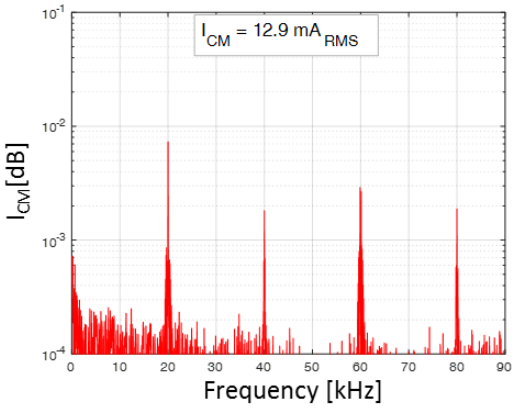
Figure 4.39 shows the test set setup and the experimental results obtained. The bridge of the converter is controlled by means of unipolar modulation, while switches Q_5 and Q_6 disconnect the DC side from the AC side during zero output configurations. The output voltage has the same characteristic of unipolar modulation of H4, while the common mode voltage is hardware dependent. In d) it can be noted that voltage V_{A0} and V_{B0}, when V_{AB} is zero, are not actively imposed by the converter to any value. The effectiveness of this converter is show graph c), the RMS value of the leakage current is reduced to 12.9 mA_{RMS}. The H4 converter controlled by means of the same unipolar modulation strategy generates a leakage current 8 times higher.



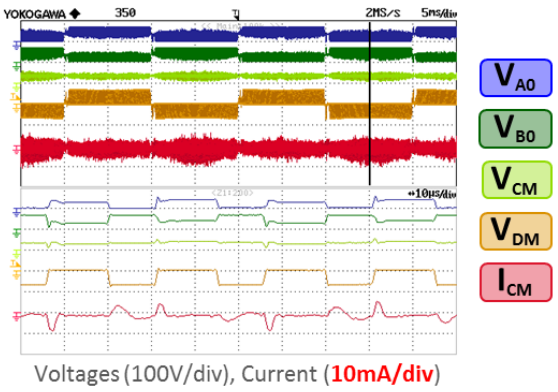
a) Test setup



b) Differential mode results



c) Harmonic content of the leakage current



d) Common mode results

Figure 4.41 - Experimental results of H6 converter controlled by means of unipolar modulation.

Leakage current comparison

Figure 4.42 combines the results of the leakage current tests. The figure is subdivided into seven columns, one for each modulation technique. Four graphs are depicted from top to bottom. The first one shows the total common mode voltage during a period of the grid frequency. The second graph shows the total common mode voltage during two switching cycles. The third graph depicts the leakage current during a period of the grid frequency, whereas the last graph shows the RMS of the leakage current, expressed as a percentage of the maximum value obtained in the tests.

Figure 4.42 shows that bipolar modulation is the only modulation technique of the H4 converter that strongly reduces the leakage current. In fact, the total common mode voltage is maintained at a constant value of $V_{DC}/2$. On the contrary, unipolar and discontinuous modulations determine and high-frequency variation of V_{TCM}, hence, high leakage current.

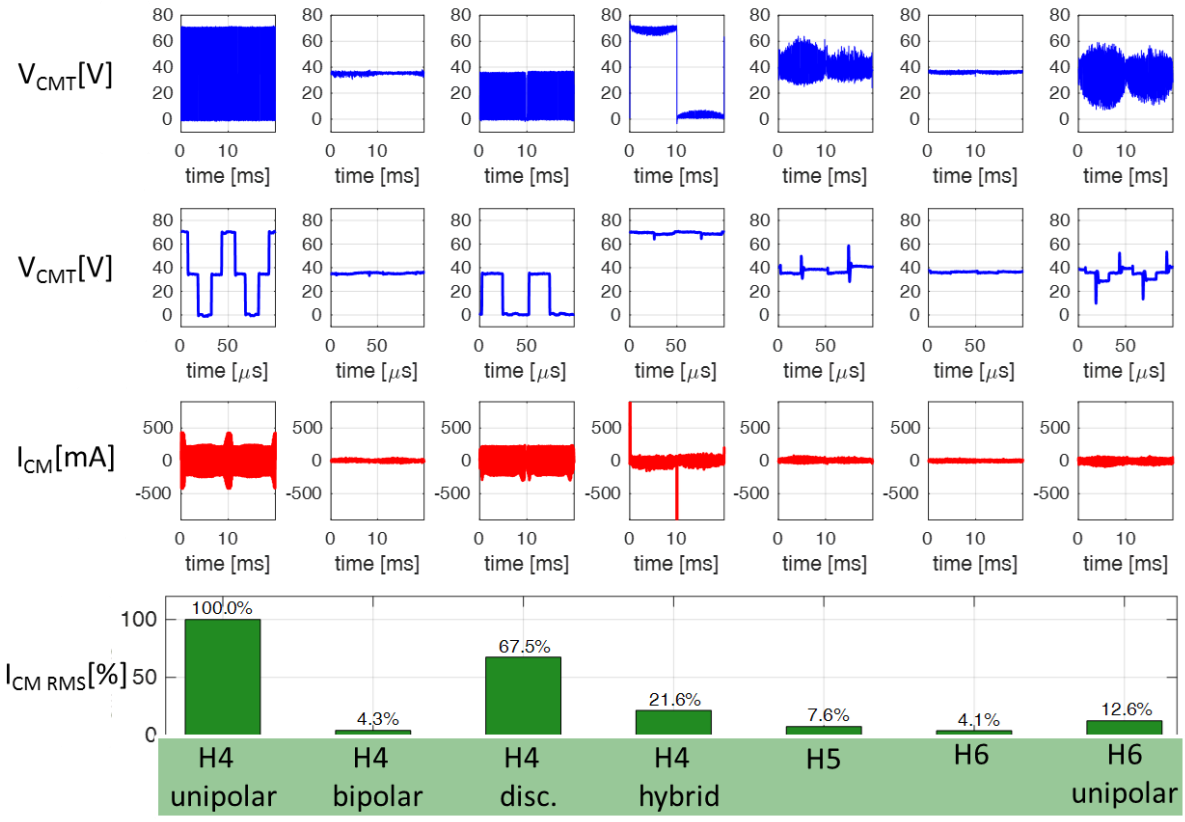


Figure 4.42 – Comparison of the total common mode voltage and leakage current generated by the tested modulation strategies.

The total common mode voltage generated by hybrid modulation of H4 converter has a low frequency square wave variation. However, high leakage current peaks are generated due to the fact that the common mode impedance is composed only by the ground resistance and by the parasitic inductance of the circuit.

The H6 converter generates a very low leakage current level, similar to that obtained by the H4 converter controlled by bipolar modulation. Indeed, the aim of the H6 topology is to actively maintain the common mode voltage to $V_{DC}/2$.

H5 converter and H6 converter controlled by unipolar modulation, have the common characteristic of interrupt the leakage current during zero output configurations. It can be noted in Figure 4.42 that the common mode voltage is not actively kept to $V_{DC}/2$ as in the case of H6 converter. A voltage transient appears every time the converter applies a zero output configuration, i.e., common mode behavior is hardware dependent. Both topologies greatly reduce the leakage current. Therefore, they are very suitable for transformerless PV applications.

The common mode voltage generated by the converter, however, is not the only requirement of PV systems, and the efficiency has to be considered as well. In the next section the efficiency evaluation of the converters presented so far is assessed, using silicon and silicon carbide power devices.

4.4.C Efficiency tests

The Si IGBT prototype and the SiC MOSFET prototype of the converters previously described have been tested and compared for all the modulations strategies presented in section 4.3.

The transistor chosen for the efficiency comparison are the same used in chapter 3.3.D. For the sake of clarity the main electrical parameters of the devices are listed in Table 4.9. The first device is a silicon high-performance IGBT (Infineon IKW40N65H5), designed for best-in-class efficiency in hard-switching and resonant converter topologies. The second device selected is a high-switching speed SiC MOSFET C2M0080120D, produced by CREE. As can be observed in Table 4.9 the blocking voltage of the SiC switch (1200V) is almost twice of that of the Si counterpart (650V). This choice is due to the absence of SiC devices with lower blocking voltages on the market.

Table 4.9 - Main parameters of the Si IGBT and SiC MOSFET selected.

Parameter	*Si IGBT*	*SiC MOSFET*
Breakdown voltage	*650V*	*1200V*
DC continuous current	*46A @100°C*	*20A @100°C*
Nominal on-state voltage drop/resistance	*1.65 V*	*80 mΩ*
R_{TH} (junction-case)	*0.60 K/W*	*0.60 K/W*
Case package	*TO247*	*TO247*
Part number	*Infineon IKW40N65H5*	*Cree C2M0080120D*

The forward voltage drop of the Si IGBT and SiC MOSFET is compared in Figure 4.43, whereas the turn-on and turn-off switching energies are depicted in Figure 4.44.

All the tests were carried out at constant modulation index, equal to 0.8, and at output frequency of 50 Hz. The converters fed a R-L load, whose inductance was 2 mH, whereas the resistance was adjusted to change the load point. Due to the low value of the load inductance, the load power factor was nearly unity in all tests.

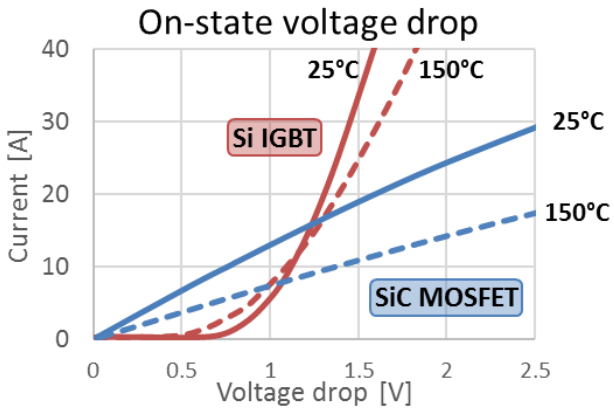


Figure 4.43 - V-I characteristic of the Si IGBT and SiC MOSFET selected.

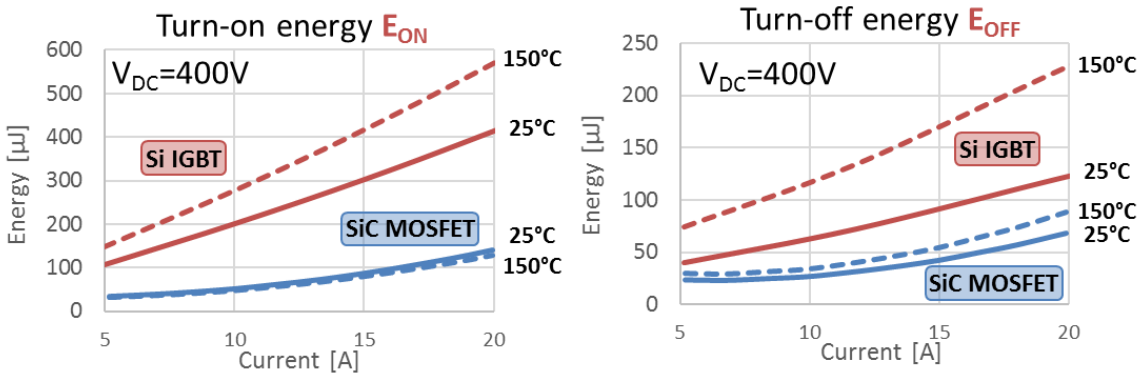


Figure 4.44 – Switching energies of the Si IGBT and SiC MOSFET selected.

The experimental test setup is depicted in Figure 4.45. During the tests, the dc voltage, equal to 400 V, was kept constant by a dc generator TDK Lambda GEN600-5.5, which also limited the output power to about 2200 W. The efficiency was measured by means of a digital power meter Yokogawa WT2030. The wide frequency range of the instrument allows the direct measure of the converter efficiency.

The control algorithm depicted in Figure 4.11 has been implemented, in discrete time, on a control board based on a floating point Digital Signal Processor (DSP) TMS320F28335. The switching frequency was kept constant at 20 kHz for all the tests.

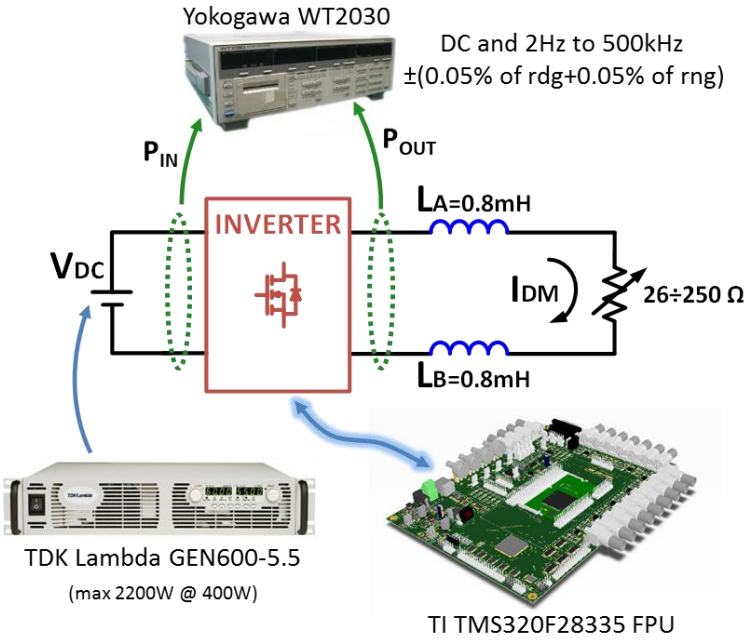


Figure 4.45 – Experimental test setup.

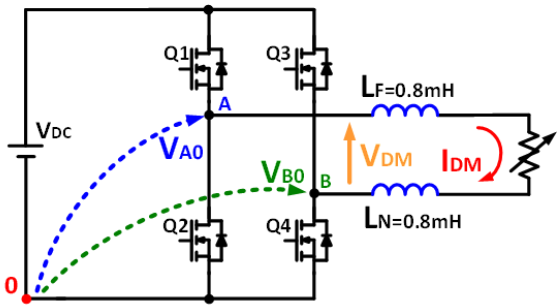
H4 converter with unipolar modulation

Figure 4.46 shows the results of the efficiency tests of the H4 converters controlled by means of unipolar modulation. The efficiency curves of Si and SiC prototypes are shown in Figure b), each point was measured at the end of the thermal transient of the heat sink.

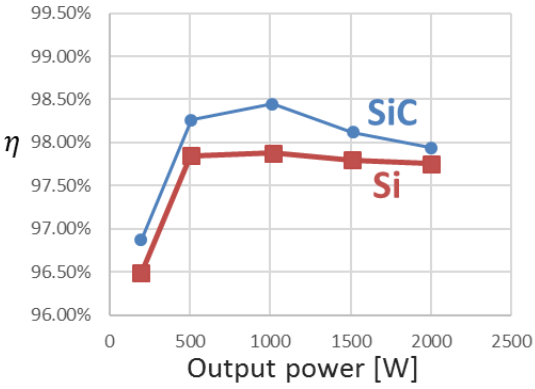
The efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference is 0.5% at half load. The difference between the two converters decreases as the output power increases. This behavior is due to the forward voltage characteristics of IGBT and MOSFET. As can be seen in Figure 4.43, SiC MOSFET is favored for low load conditions.

The minimum difference between the two efficiencies, 0.19%, is reached at the maximum output power of 2000 W. Given that the thermal resistance of the heat sink is 1.3 ÷ 1.5 °C/W, the difference of temperatures between the two prototypes can be roughly estimated in 4.9 ÷ 5.7 ° C.

The infrared thermal analysis of the two converters, at the output power of 2000 W, is depicted in Figures c) and d). The difference of temperature between the two heatsink is 4.9 ° C, thus confirming the consistency of the measure of efficiency.

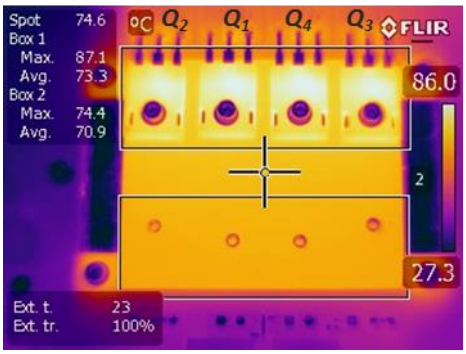


a) Test setup.



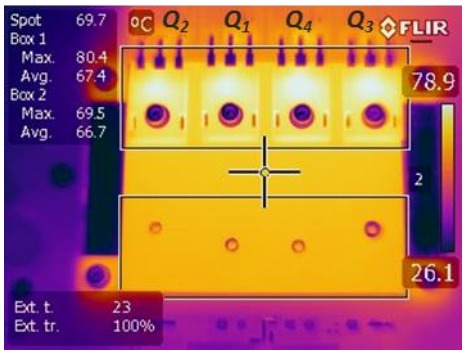
b) Efficiency comparison of SiC and Si prototypes.

T_{MAX} = 87.1°C , $T_{HEATSINK}$ = 74.6°C



c) IR picture of the Si prototype at output power of 2000 W.

T_{MAX} = 80.4°C , $T_{HEATSINK}$ = 69.7°C



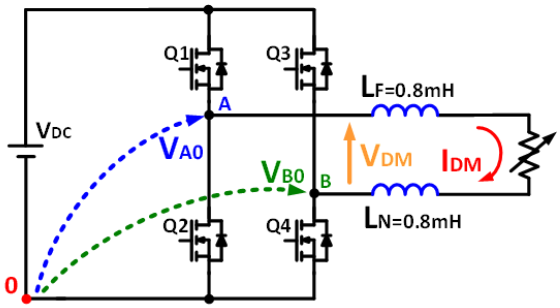
d) IR picture of the SiC prototype at output power of 2000 W.

Figure 4.46 - Experimental results of full bridge converter controlled by means of unipolar modulation.

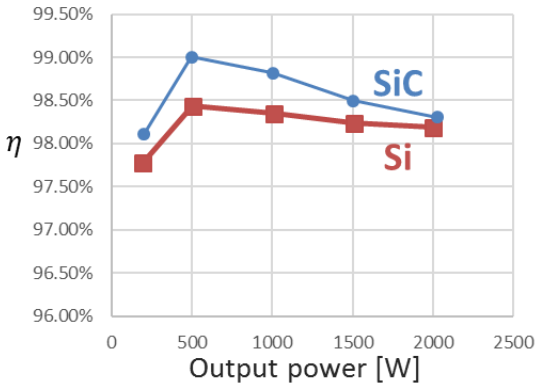
H4 converter with discontinuous modulation

Figure 4.47 shows the results of the efficiency tests of the H4 converters controlled by means of discontinuous modulation. The efficiency curves of Si and SiC prototypes are shown in Figure b), it can be seen that the efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference is 0.6% at 25% of load. The minimum difference between the two efficiencies, 0.12%, is reached at the maximum output power of 2000 W.

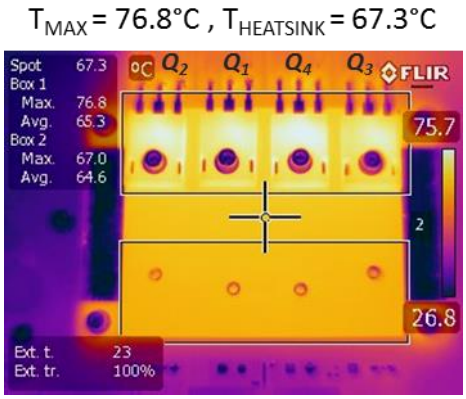
The infrared thermal analysis of the two converters, at the output power of 2000 W, is depicted in c) and d). It can be noted that switches Q_1 and Q_3 are hotter than Q_2 and Q_4. This behavior is due to the asymmetric use of the converter by the discontinuous modulation. Indeed, the zero output voltage configuration is always generated by the upper switches of the bridge, therefore they generate more conduction losses. The difference of temperature between the two heatsink is 6.3 ° C, whereas the maximum temperature of the transistors is 87.1 °C, for Si IGBTs, and 80.4 °C for SiC MOSFETs.



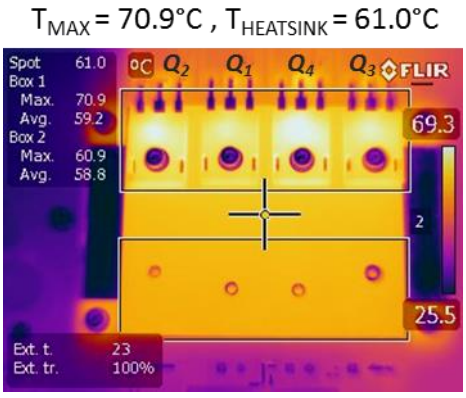
a) Test setup.



b) Efficiency comparison of SiC and Si prototypes.



c) IR picture of the Si prototype at output power of 2000 W.

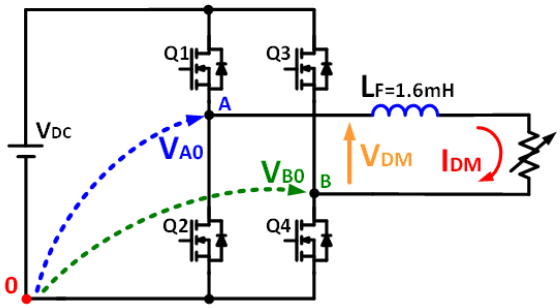


d) IR picture of the SiC prototype at output power of 2000 W.

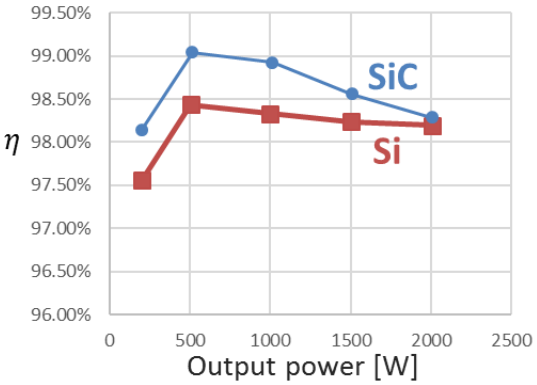
Figure 4.47 - Experimental results of full bridge converter controlled by means of discontinuous modulation.

H4 converter with hybrid modulation

Figure 4.48 shows the results of the efficiency tests of the H4 converters controlled by means of hybrid modulation. The efficiency curves of Si and SiC prototypes are shown in Figure b). The efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference is 0.6% below 50% of load. The minimum difference between the two efficiencies, 0.1%, is reached at the maximum output power of 2000 W.

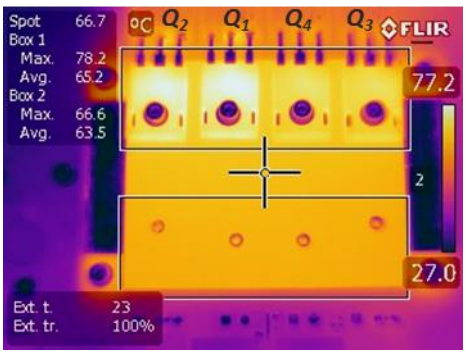


a) Test setup.



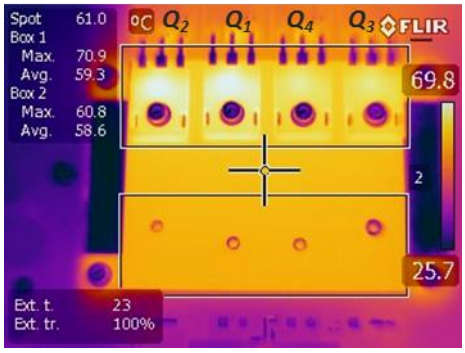
b) Efficiency comparison of SiC and Si prototypes.

T_{MAX} = 78.2°C , $T_{HEATSINK}$ = 66.7°C



c) IR picture of the Si prototype at output power of 2000 W.

T_{MAX} = 70.9°C , $T_{HEATSINK}$ = 61.0°C



d) IR picture of the SiC prototype at output power of 2000 W.

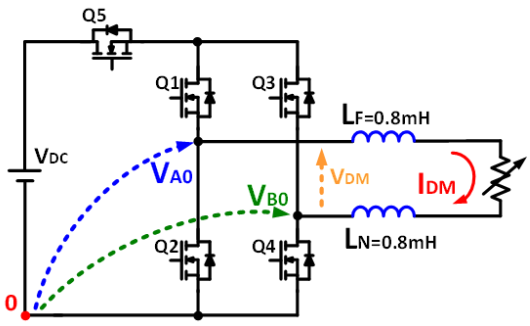
Figure 4.48 - Experimental results of full bridge converter controlled by means of hybrid modulation.

The infrared thermal analysis of the two converters, at the output power of 2000 W, is depicted in Figure c) and d). It can be noted that switches Q_1 and Q_2 are hotter than Q_3 and Q_4. This behavior is due to the asymmetric use of the leg of the converter by the hybrid modulation. Indeed, leg A is switched at high frequency while leg B is switched at grid frequency. The difference of temperature between the two heatsink is 5.7 ° C, whereas the maximum temperature of the transistors is 78.2 °C, for Si IGBTs, and 70.9 °C for SiC MOSFETs.

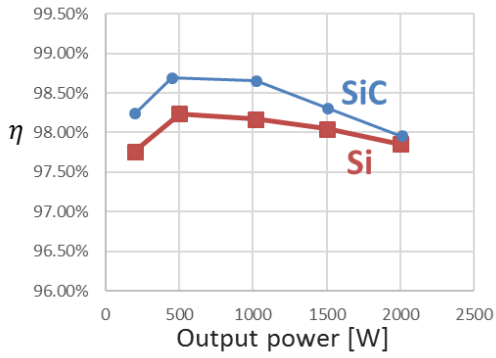
H5 converter

Figure 4.49 shows the results of the efficiency tests of the H5 converters. The efficiency curves of Si and SiC prototypes are shown in Figure b), each point was measured at the end of the thermal transient of the heat sink. The efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference is 0.6% below 50% of load. The minimum difference between the two efficiencies, 0.1%, is reached at the maximum output power of 2000 W. The infrared thermal analysis of the two converters, at the output power of 2000 W, is depicted in Figure c) and d).

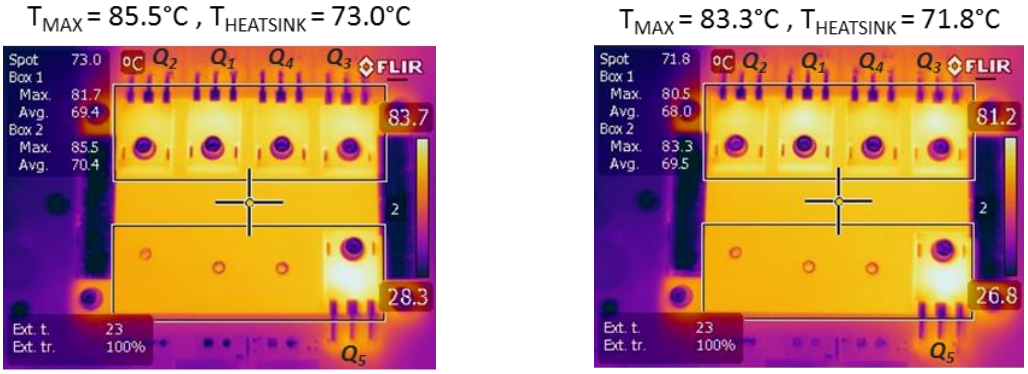
The difference of temperature between the two heatsink is 1.2 ° C, whereas the maximum temperature of the transistors is 85.5 °C, for Si IGBTs, and 83.3 °C for SiC MOSFETs. For both converters, the hottest switch is Q_5. This characteristic is due to the fact that all the load power flows through the DC link transistor.



a) Test setup.



b) Efficiency comparison of SiC and Si prototypes.



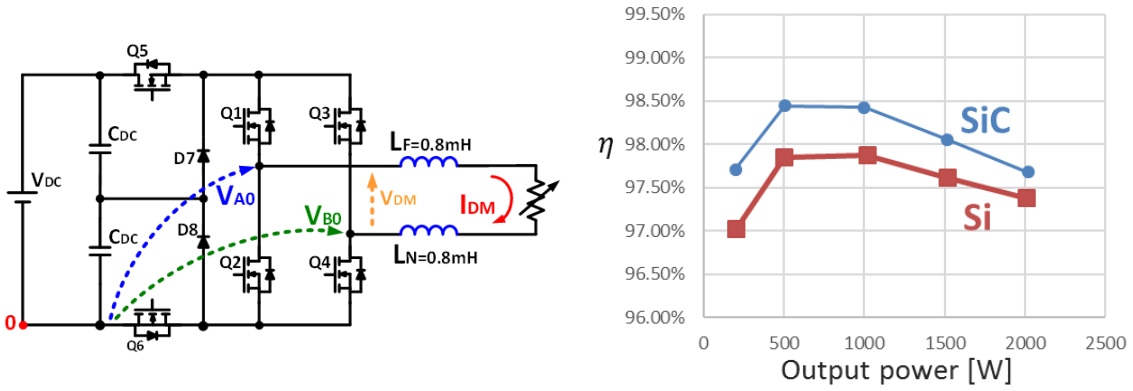
c) IR picture of the Si prototype at output power of 2000 W.

d) IR picture of the SiC prototype at output power of 2000 W.

Figure 4.49 - Experimental results of H5 converter.

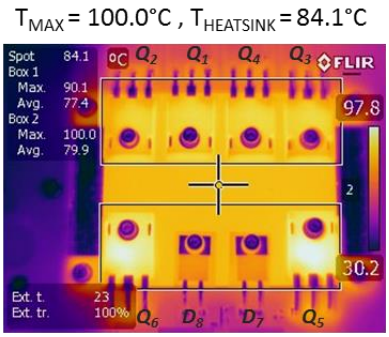
H6 converter

Figure 4.50 shows the results of the efficiency tests of the H6 converter. The efficiency curves of Si and SiC prototypes are shown in Figure b). The efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference is 0.55% below 50% of load. The minimum difference between the two efficiencies, 0.3%, is reached at the maximum output power of 2000 W. The infrared thermal analysis of the two converters ia depicted in Figure c) and d). The difference of temperature between the two heatsink is 6.7 ° C, whereas the maximum temperature of the transistors is 100 °C, for Si IGBTs, and 92.5 °C for SiC MOSFETs. For both converters, the hottest switches are Q_5 and Q_6. This characteristic is due to the fact that all the load power flows through the DC link transistors.

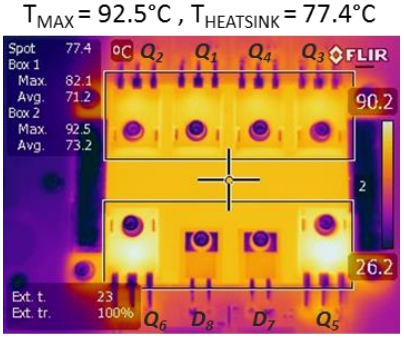


a) Test setup.

b) Efficiency comparison of SiC and Si prototypes.



c) IR picture of the Si prototype at output power of 2000 W.

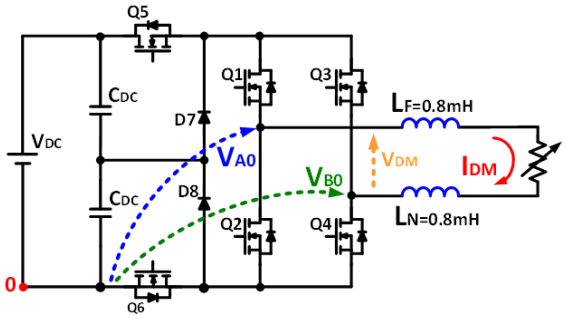


d) IR picture of the SiC prototype at output power of 2000 W.

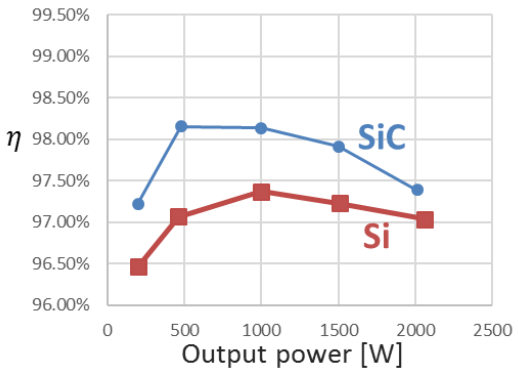
Figure 4.50 - Experimental results of H6 converter.

H6 converter with unipolar modulation

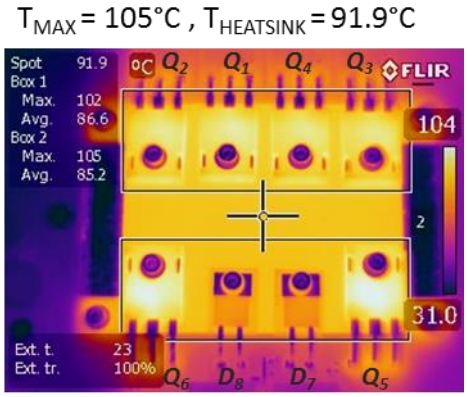
Figure 4.51 shows the results of the efficiency tests of the H6 converter controlled by means of unipolar modulation. The efficiency curves of Si and SiC prototypes are shown in b). The efficiency of the SiC converter is always greater than the Si counterpart, and the maximum difference 1% at 25% of load. The minimum difference between the two efficiencies, 0.35%, is reached at the maximum output power of 2000 W. The infrared thermal analysis of the two converters is depicted in figures c) and d). The difference of temperature between the two heatsink is 7.7 ° C, whereas the maximum temperature of the transistors is 105 °C, for Si IGBTs, and 95.3 °C for SiC MOSFETs.



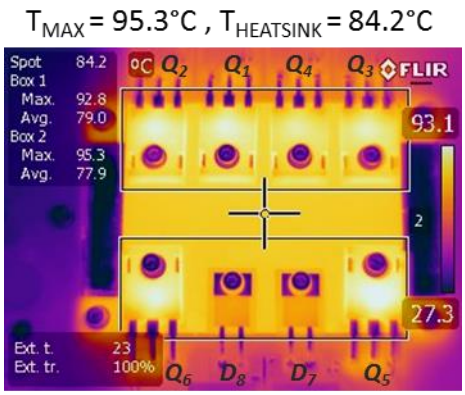
a) Test setup.



b) Efficiency comparison of SiC and Si prototypes.



c) IR picture of the Si prototype at output power of 2000 W.



d) IR picture of the SiC prototype at output power of 2000 W.

Figure 4.51 - Experimental results of H6 converter controlled by means of unipolar modulation.

Efficiency comparison

Figure 4.52 shows the efficiency of Si and SiC inverter prototypes as a function of the output power, whereas the maximum temperature reached by the converters is reported in Figure 4.53.

Full bridge converter, controlled by means of hybrid and discontinuous modulation, is the most efficient topology tested. This result is due to the fact that both conduction and switching losses are minimized. Conduction losses are related to the number of components present in the converter, thus full bridge is favored respect to H6 and H5. Switching losses, instead, depend on the number of commutation per switching cycle, thus discontinuous modulations are more efficient than unipolar and bipolar techniques. Even though hybrid and discontinuous modulation of full bridge lead to higher efficiency, they cannot be used for transformerless PV applications, as shown in section 4.4.B

The only modulation technique of H4 converter that strongly reduces the leakage current is the bipolar one. Unfortunately, it was not possible to test the efficiency of bipolar modulation as the power meter could measure differential voltages up to 600V, while bipolar modulation generates a differential output voltage of 2 V_{DC}, i.e., 800 V. Nevertheless, H4 converter controlled by bipolar modulation requires high switching frequency and large

decoupling inductors in order to reduce the output current ripple, thus, reducing the overall efficiency of the converter.

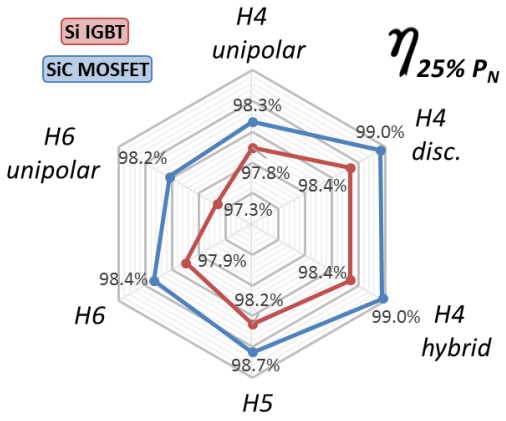
Among all the converters that reduce the leakage current, the H5 topology shows the best efficiency. Instead, H6 converter controlled by unipolar modulation technique shows the lowest efficiency. However, it generates an output voltage that has a fundamental switching frequency at $2F_{SW}$, thus it requires smaller decoupling inductors.

It is worth mentioning that the DC link switches of H5 and H6 converters, from the thermal point of view, are more stressed than the switches of the main bridge. The maximum output power of the converters is thus limited by the maximum junction temperature of the DC power switches. An accurate design of the cooling system may help to uniform the thermal stress among the transistors, therefore increasing the maximum power of the inverter.

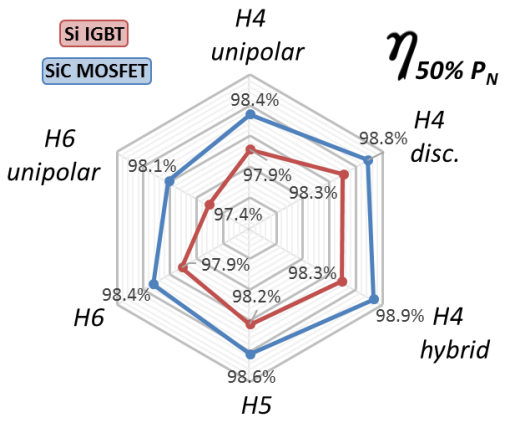
The efficiency of the SiC converters is always greater than that of the Si counterpart, for any value of the output power. The gain of efficiency is more appreciable at reduced load and decreases as the output power increases. This behavior is due to the forward voltage characteristics of IGBT and MOSFET. High efficiency at low load is particularly advantageous for PV installations, which rarely operate at full power since the solar radiation depends on weather conditions and on the position of the sun in the sky. It may be noted also that the advantage in the use of SiC is greater for unipolar modulation than for discontinuous techniques. This behavior is due to the fact that the SiC MOSFET has lower switching energy than the Si IGBT, as depicted in Figure 4.44.

It is also important to remind that SiC prototypes show higher efficiency even if the MOSFETs are rated for 1200 V, whereas silicon prototypes use 650 V IGBTs. A fair comparison among devices with the same blocking voltage, would have resulted in a greater difference in terms of efficiency.

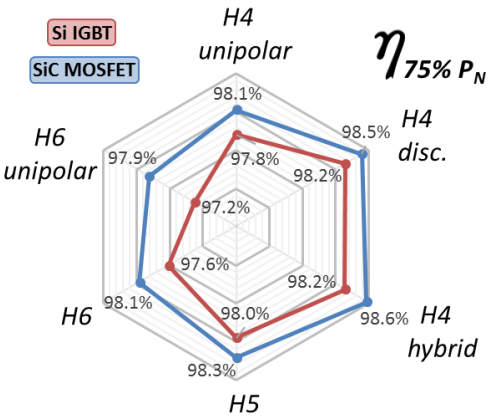
In conclusion, among the topologies examined, the H5 converter offers the best tradeoff between efficiency and reduction of the leakage current. Moreover, the superior switching characteristics of SiC technology can be advantageously used in PV systems, where the economic return in the long term operating can justify the higher cost of SiC devices.



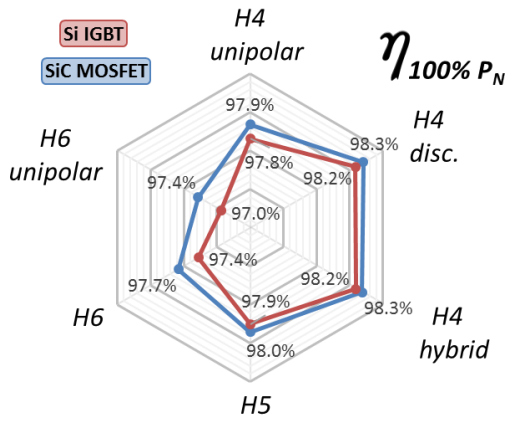
a) Efficiency at 25 % of power.



b) Efficiency at 50 % of power.



c) Efficiency at 75 % of power.



d) Efficiency at 100% of power.

Figure 4.52 – Efficiency comparison of Si and SiC prototypes as a function of the output power.

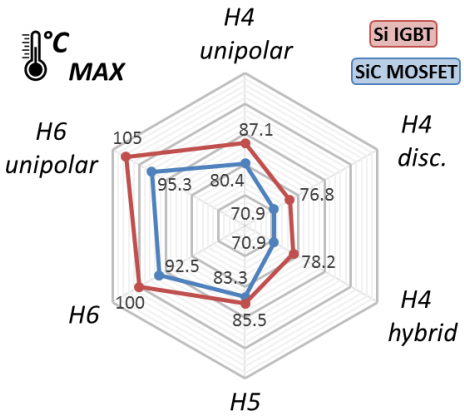


Figure 4.53 – Maximum temperature of the power switches at output power of 2000 W.

Conclusions

In this thesis, high-efficiency DC to AC power converter have been investigated. The state of the art on transistor technologies and on converter topologies has been presented too.

In the first part of the dissertation, soft switching and hard switching topologies have been presented. Silicon and silicon carbide prototypes have been built for efficiency comparison.

The soft-switching silicon prototype has shown better efficiency than hard-switching silicon counterparts, for any value of the output power and switching frequency. Higher efficiency is however achieved to the price of higher hardware and control complexity of the converter. Soft-switching silicon converter, however, compared to hard switching silicon carbide converter, has shown marginal benefits in terms of efficiency. For switching frequencies below 20 kHz, soft switching converter is slightly more efficient than SiC prototype only at high power level. While for switching frequencies above 25 kHz, the silicon carbide prototype is the most efficient for any value of the output power.

The first conclusion of the thesis is that the use of the latest SiC technologies in hard switching DC/AC converters guarantee higher efficiency with respect to the use of silicon devices, even using complex soft switching topologies.

The second part of the dissertation have shown inverter topologies for low power, single phase photovoltaic (PV) systems. When no transformer is included in a PV system, the DC/AC front-end converter may generate high level of leakage current, leading to potential hazards for the personal electric safety. Inverter topologies that can mitigate the leakage problem, and at the same time guarantee a high level of efficiency, have been presented.

Full bridge, H5 and H6 converters prototypes have been realized in order to experimentally compare their efficiency and their common mode behavior. Each converter has been realized in two different versions, one using high-performance Si IGBTs, and one using high-switching speed SiC MOSFETs.

The conclusion of the tests is that, among the topologies examined, the H5 converter offers the best tradeoff between efficiency and reduction of the leakage current. Moreover, the superior switching characteristics of SiC technology can be advantageously used to increase the efficiency of PV systems.

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