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NANO-FABRICATION OF COMPLEX FUNCTIONAL STRUCTURES USING NON- CONVENTIONAL LITHOGRAPHY

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ACKNOWLEDGEMENTS

DEDICATION

Dedicated to those who loved me and supported me most, my family:
my lovely mum and dad,
for taking the time to teach me the value of humanity and education, and
my lovely sisters, brothers and nieces,
for their continues support every day even from a long distance.

PREFACE

Parallel local oxidation as an unconventional lithography technique is proposed for nanopatterning and device fabrication. The inherent simplicity of this process with the *in-situ* growth of SiO_2 provides the possibility of the fabrication of novel devices with the nanojunction configuration. By this method a new family of resistive switch devices introduced in the technology of silicon without any special processing in pristine silicon. This nanofabrication method enable us the possibility of studying the biomolecules by nanopatterning and more application in device, and biosensor fabrications.

In this thesis I will describe a novel approach for the nanofabrication and device properties of inorganic nanostructures, as well as the self-organization of organic and biological matter. My research activity is focused on the application of local electrochemical methods for nanofabrication and the development of new devices based on resistive switching behavior including inorganic structures and also organic molecules as Graphene. I developed the fundamental process of local oxidation soft-lithography also in the surface architecture applicable in the biotechnology.

In **Chapter 1** I will present a brief introduction on the state of art of nanotechnologies, nanofabrication techniques and unconventional lithography as a technique to fabricate the novel electronic device as resistive switch so-called memristor is shown. In **Chapter 2** a detailed description of the main fabrication and characterization techniques employed in this work is reported. **Chapter 3** parallel local oxidation lithography (pLOx) describes as a main technique to obtain accurate patterning process. All the effective parameters has been studied and the optimized condition observed to highly reproducible with excellent patterned nanostructures. The effect of negative bias, calls local reduction (LR) studied. Moreover, the use of AC bias shows faster patterning process respect to DC bias. In **Chapter 4** (metal/ e-SiO_2/ Si nanojunction) it is shown how the electrochemical oxide nanostructures by using pLOx can be used in the fabrication of novel devices call memristor. We demonstrate a new concept, based on conventional materials, where the lifetime problem is resolved by introducing a “regeneration” step, which restores the nano-memristor to its pristine condition by applying an appropriate voltage cycle. In **Chapter 5** (Graphene/ e-SiO_2/ Si), Graphene as a building block material is used as an electrode to selectively oxidize the silicon substrate by pLOx set up for the fabrication of novel resistive switch device.

In **Chapter 6** (surface architecture) I will show another application of pLOx in biotechnology is shown. So the surface functionalization combine with nano-patterning by pLOx used to design a new surface to accurately bind biomolecules with the possibility of studying those properties and more application in nano-bio device fabrication. So, in order to obtain biochips, electronic and optical/photonics devices Nano patterning of DNA used as scaffolds to fabricate small functional nano-components.

Chapter 1

Introduction

In this chapter, the main topic of this research report biased on Nanotechnologies and Nanofabrication methods as unconventional lithography for several application such as electronic devices fabrication like resistive switch or memristor and surface architecture are reviewed.

1.1 Nanotechnology

Nanotechnology has been developed as an incredible way during the last decades in a variety of applications. Beyond miniaturization, which is anyway a strong issue of nanotechnology, It makes nanotechnology more effective technology, rather than miniaturization, that nanostructured materials have physical and chemical properties extremely different from those of bulk materials. In the bulk materials we associate some properties which are the averaged properties, such as the density and the elastic modulus in mechanics, the resistivity and the magnetization in electricity and magnetism and the dielectric constant in optics. It is notice at nanoscale dimensions the properties of materials are not longer depend solely on the composition and the structure. Nanomaterials involve new phenomena affiliated with quantized effects and with the excellence of the surfaces and interfaces. Its effects outcrop in the nanometric regime because the throughout dimensions of the objects are comparable to the characteristic wavelength for fundamental excitations in materials. Such excitations include the wavelength of electrons, photons, phonons, and magnons; for example, electron wave functions in semiconductors are typically of the order of 10 to 100 nanometers. These excitations carry the quanta of energy through materials and thus determine the dynamics of their propagation and transformation from one form to the other. When the size of structures is comparable to the quanta themselves, the effect of the excitations moving through and interacting with material structures, is no more negligible, with the effect of bringing into play quantum mechanical selection rules not apparent at larger dimensions [1,2,3,4].

In 1959, the promise of nanotechnology was outlined by Nobel Prize laureate Richard Feynman in his famous talk, “There's Plenty of Room at the Bottom”. Since then, the concepts of molecular nanotechnology have extended to such as “molecular engineering” by Eric K. Drexler [5] and “molecular electronics” by Mark A. Ratner [6]. Recently, the area of molecular nanotechnology has rapidly developed because enormous possibilities have opened to manipulate the molecular synthesis and movement. A lot of devices and applications have been demonstrated [7]. It is now not an impractical dream to fabricate molecular devices and molecular machines with atomic precision. In figure 1-1, I show the effect of nanotechnology in a variety of innovative application such as Nano device, Nano-biotechnology, Bio engineering, Medicine and drugs, Nano fabrics, Energy, Optical engineering and cosmetics.

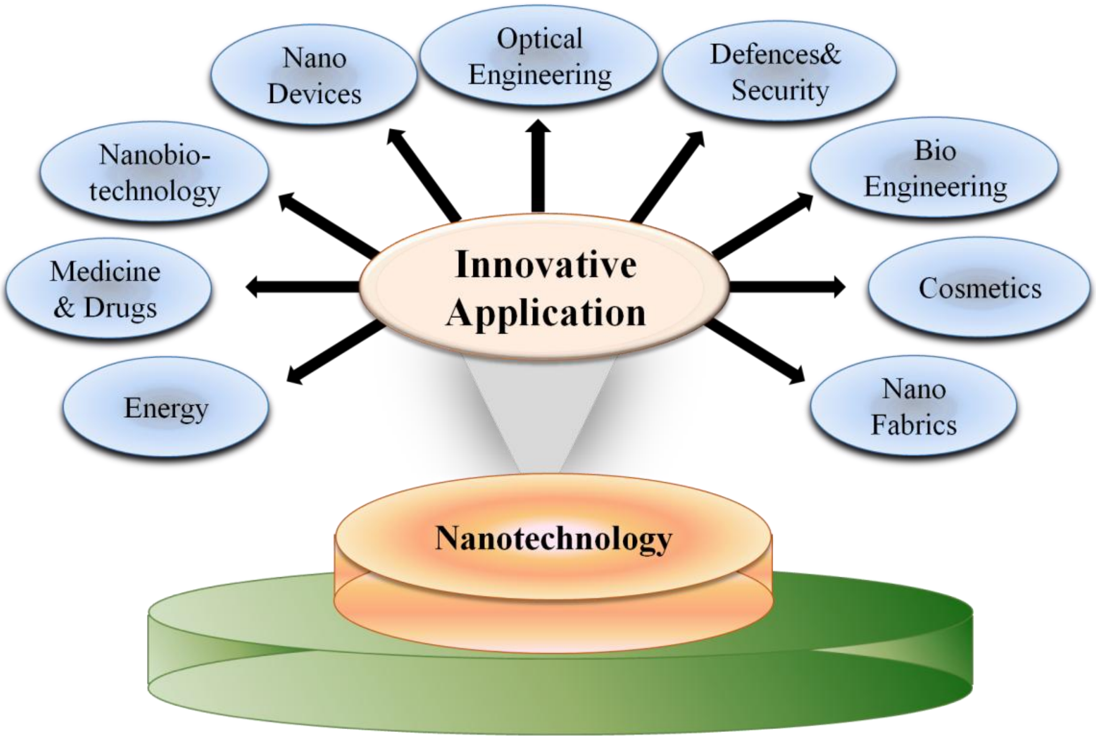

Figure 1- 1- The effect of Nanotechnology in developing of innovative application

1.2 Nanofabrication

In order to exploit the advantages of nanotechnology the nanostructures must be connected with the outside world, therefore nano-objects must fabricated or placed in controlled and defined positions. One of the most important issue of nanotechnology is the nanofabrication that allow the building and positioning of the nanostructure in precise positions.

Traditionally, micro/nanostructured materials can be obtained following two different approaches: “top-down” and “bottom-up” (Figure 1-2). In the top-down process a macroscopic object is progressively cut and shaped in order to obtain a functional smaller architecture. This methodology is characteristic of the conventional lithographic techniques (e.g. photolithography) , which have been used in microelectronics since many years to produce microchips and hardware components. However the resolution of photolithography, being an optical fabrication technique, is limited by the wavelength of the light. Features smaller than few microns are not achievable with this technique. To overcome this, several complex top-down techniques have been developed in the last decade, still based on light as X-ray Lithography (XRL) [8] and Deep X-ray lithography (DXRL) [9], or on De Broglie wavelength of the electrons as Electron Beam Lithography (EBL) [10]. All this technique allow to achieve a very high resolution (few tens of nanometer) but require very expensive equipment and are not applicable to a large range of materials.

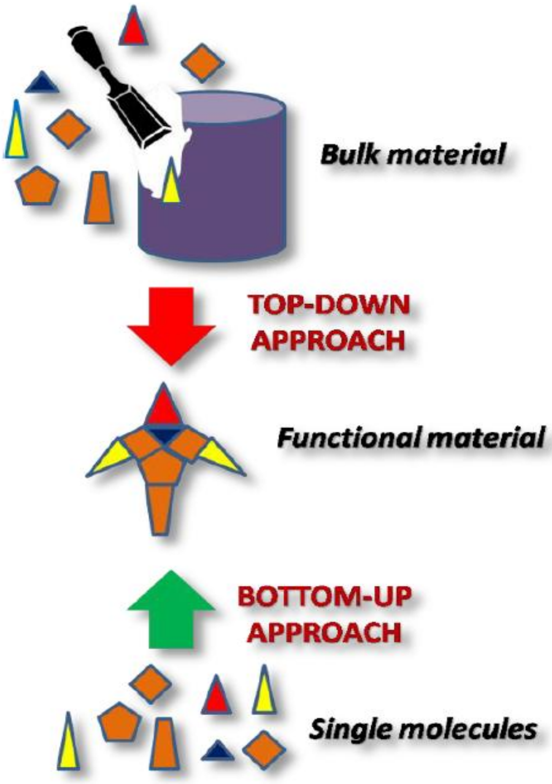

Figure 1- 2- Schematic representation of the two typical fabrication approaches

The bottom-up approach starts directly from the molecules, and is based on the their capability to self-assembly into regular structures under specific conditions. The driving forces of this self-organization are specific and non-specific supramolecular and intermolecular interactions[11,12]. The forces responsible for the spatial organization may vary from weak interactions (electrostatic and magnetic forces or hydrogen bonding) to strong interactions (covalent and ionic bonding). Non-covalent bonds are critical in maintaining the three-dimensional structure of large molecules, such as proteins, nucleic acids and artificial supramolecular structures, and are involved in many biological processes in which large molecules bind specifically but transiently to one another. The energy released in the formation of non-covalent bonds is usually in the order of 1-5 kcal/mol. There are four commonly mentioned types of non-covalent interactions: hydrogen bonds, ionic bonds, van der Waals forces, and hydrophobic interactions. Examples of bottom-up techniques exploiting molecular self-organization are: Dip-pen Lithography (DPL) [13], Local Oxidation Nanolithography (LON) [14], Nanoimprint Lithography (NIL) [15] and Soft-lithography [16]. Thank to their flexibility and cheapness bottom-up techniques have found more and more space in these decades for applications in many scientific fields, ranging from electronics, optoelectronics to biotechnology and medicine.

1.3 Unconventional lithography

"Nanofabrication" is the process of making functional structures with arbitrary patterns having sizes of 100 nm or less in at least one dimension. Scanning-beam techniques, such as electron beam lithography (EBL) and focused ion beam lithography (FIB) writing, are the principal methods of generating arbitrary nanoscale patterns (mastering); photolithography is the principal method of transferring these patterns from one substrate to another (replication). These techniques, while the workhorses of nanofabrication, come with high capital and operating costs, limited accessibility to general users (and users of materials considered incompatible with electronics fabrication). They are generally only applicable to the two-dimensional patterning of resist materials on planar substrates.

The limitations of these conventional approaches when applied to innovative problems - high capital and operating costs, the difficulty in accessing the facilities necessary to use them, and their restricted applicability to many important classes of problems - motivated scientists' exploration and development of new, or "unconventional" nanofabrication techniques.

Unconventional techniques have the potential to be the ultimate, low-cost method for certain types of nanomanufacturing; approaches based on reel-to-reel processing are particularly attractive for low-cost processes. Unconventional approaches are also operationally much simpler to use than are conventional techniques, and thus help to open nanoscience and nanotechnology to exploration by a wide range of disciplines, especially those historically only weakly connected to electrical engineering and applied physics. The successful unconventional techniques, which have been extensively reviewed recently in the literature, as a bottom-up techniques are soft lithography [12], nanoimprint lithography [11], nanoindentation lithography [17], edge lithography [18] and scanning probe lithography (local oxidation) [10]. The main lithography techniques used in this work are based on local oxidation nanolithography and soft lithography.

Most of the soft lithographic techniques use mold formed of a master template which the process begins with the master fabrication, usually made by replica molding (RM) (see chapter 2, section 2.2). RM includes transfer of topographical features from a rigid master or soft mold, referred here as the master and by the end could make available a soft stamp to be used for our patterning procedures. Patterning by local oxidation includes scanning probe lithography and parallel local oxidation (pLOx). In our research, the patterning process is performed by pLOx (see **chapter 2** and **chapter** 3) where it used a soft metalized stamp performed by RM as an electrode, instead of conductive tip used by scanning probe lithography, to oxidize the silicon substrate and fabricate nanostructures. This nanopatterning process was optimized to pattern silicon (see **chapter 3**) with different possible features, fabrication of novel electronic devices named resistive switch or memristor (see **chapter 4** and **chapter 5**) and more application in selectively bind biomolecules (see **chapter 6**).

Patterning by following RM abilities are involves also another techniques such as lithography control wetting (LCW), micromolding in capillaries (MIMIC), microtransfer Molding (μTM), and Ultraviolet-molding (UV-molding). In our work the pattern film of graphene which used for fabricating of novel resistive switch devices that will explain in the chapter 5 was performed by LCW (see chapter 2, section 2.3)

In this work we use several kind of introduced techniques for fabricating several kind of nanpatterns on technological relevant surfaces and to demonstrate the bottom-up nanofabrication of a memristors and surface driving for biomolecules.

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Chapter 2

Experimental Materials

In this chapter, the main techniques used for patterning, device fabrication and characterization are reviewed.

Fabrication techniques

2.1 Parallel electrochemical Local Oxidation (pLOx)

The Local Oxidation of silicon is the main fabrication technique used in this thesis. Local oxidation firstly has emerged by a robust and versatile lithographic technique based on scanning probe microscopy (SPM), namely local anodic oxidation. This technique has demonstrated the possibility to prototype ultra-small silicon oxide nanostructures with lateral size <50 nm and 1–4 nm height, with results comparable to state-of-the-art electron beam lithography [1]. This approach has been proven to be useful to fabricate nanoscale devices [2,3,4] or templates[5,6], and to investigate electrochemical reactions in an attoliter environment [2]. Local oxidation exploits the water meniscus formed between a conductive tip of an AFM and the substrate, when the tip is brought to a few nanometers above the surface. The tip,–water meniscus (electrolyte) and substrate cell that yields a nanometric sized oxidation of the substrate upon the application of a voltage bias across (Figure 2.1).

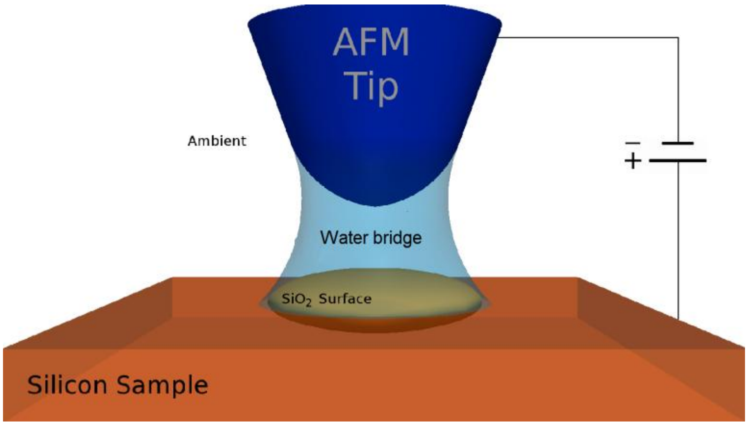

Figure 2- 1. Oxidation driven by AFM tip, which are generated due to the presence of the strong electric field, interacting with the silicon surface.

Local anodic oxidation has the typical limitations of the SPM techniques, namely maximum scan size of the piezoelectric actuator (generally hundreds of microns) and the serial fabrication being dependent on the scan frequency. In order to overcame this problem, recently, several authors have scaled up the local oxidation process using a conductive stamp with multiple protrusions as a cathode. They follow the original idea of Jacobs [7] to increase the writing rate of the scanning probe lithography (serial process) by using a metalized stamp to oxidize a large surface area and fabricate more nanostructures at the same time (concept of parallel process). M¨uhl et al [8] used a stamp with few protrusions to demonstrate the feasibility of parallel oxidation, Cavallini et al [9] transferred the bits of a metalized digital videodisk (DVD) to the silicon surface, and Martinez et al [10] used silicon stamps, modified by electron beam lithography, to generate arrays of parallel lines separated by 100 nm over cm^2 regions. In the above experiments, the areas oxidized are as large as 1 cm^2, and the heights of the oxide nanostructures are about 3 nm, namely comparable to the ones fabricated by local anodic oxidation performed by SPM.

Here, the parallel local oxidation as a main procedure in device fabrication and surface architecture is developed by using a press (figure 2-2). The press for pLOx is composed of three main parts; part 1 is a micro screw driver that would move up and down the movable holders, part 2 is the movable holder with conductive flat plate that by means of silver paste the metalized stamp will get connect to the wires to have the electrical connection to the power supply, and part 3 is a fix holder with conductive flat plate to electrically keep in contact the silicon substrate into the power supply. To bring the stamp in contact with the substrate it is fixed on a stamp-holder and moved downward by a micrometric screw while, the substrate, is fixed to a rigid sample-holder (figure 2-2). The PDMS stamps and the substrate are electrically connected to a voltage source (ELIND Model 3232). The machine was inserted inside a box (Tupperware, USA) with feed through for bias and hygrometer's probe (PCE 313-A), where the Relative Humidity (RH) is increased and controlled by bubbling pure water with nitrogen (water purified by a Milli-Q system ELGA PURELAB UHQ). When RH reached 90%, the stamp and the sample are gently placed in contact by means the downward motion of the micrometric screw. The system stamp/water/silicon substrate is an electrochemical cell where the stamp is the cathode, the silicon substrate is the anode and the pure water layer, adsorbed on silicon and stamp surfaces, generates the electrolyte. When a bias voltage is applied between stamp and substrate the anodic oxidation takes place at the anode. At the end of the oxidation process, a pattern of oxide lines is formed. Parallel-local anodic oxidation works also for stamps composed by motives with different length-scale as arrays of parallel lines with different periodicity (e.g. a replica of a blank DVD) and objects of different nanometric size (replica of a recorded DVD).

The high reproducibility of this method is due to the breaking strength of the stamp that not shows any relevant degradation after several operations (up to 20). This is an important peculiarity property in order to repeat the process several times on the same sample and make more complex patterns. The details of the procedure is described in the **Chapter 3**.

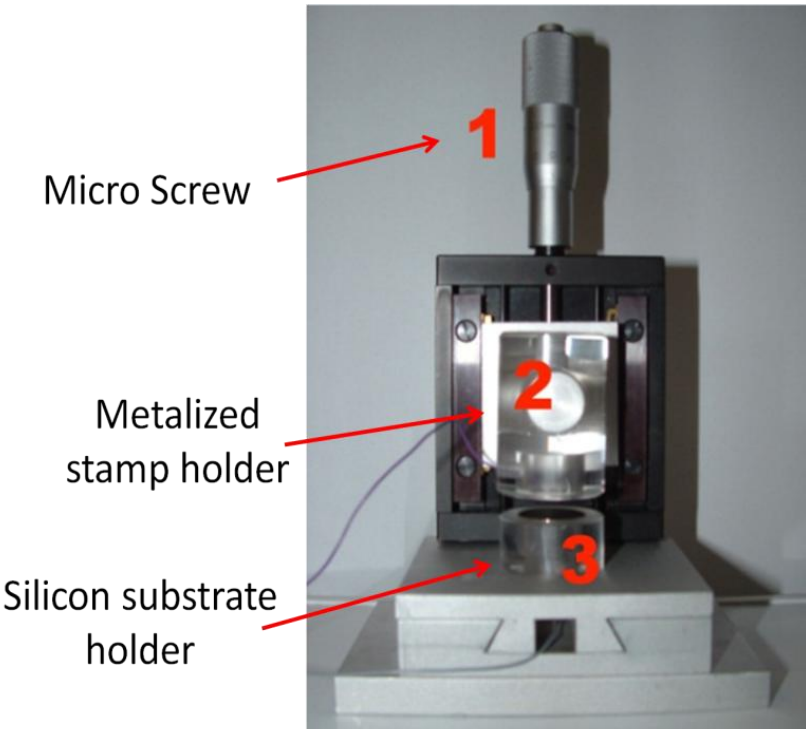

Figure 2- 2 - Home-made machine with a micro-screw(1), stamp holder (2), substrate holder (3), (d) Parallel Local Oxidation set up.

2.2 Replica Molding (RM) and metalized stamp

“Replica molding” (RM) allows a faithful duplication of the topographic information present in a master, even if three-dimensional. This technique with an appropriate material such as Polydimethylsiloxane (PDMS) enables replicating highly complex master structures with nanometric features in a simple, reliable and inexpensive way. In fact the fidelity of this process is largely determined by Vander Waals interactions, wetting, and capillary forces that are short range interactions and allow more accurate replication of small features (<100 nm) than Photolithography. Thermally or UV-curable pre-polymers, have a shrinkage of less than 3% on curing as they usually do not contain solvent; the cured polymers, therefore, possess almost the same dimensions and topologies as the channels in the PDMS mold. In Figure 2.2 the general replication procedure is reported. The molds are prepared by casting against rigid masters a mixture of PDMS with a curing agent (generally in a ratio 10:1). The PDMS/master is put in a oven at $70°^{C}$ for 1 hour to complete the curing process (Figure 2-3).

Figure 2- 3 Replica molding of the master with PDMS

Then the mold is peeled off and it is covered by 100nm of Au layer in spattering chamber under vacuum condition and it is ready to be use as a metalized stamp.

Figure 2- 4 Spattering chamber under vacuum condition for Au deposition on PDMS

There are the other types of the metalized stamp which are made of metal layer of Compact Disk (CD). In this case, the mold are prepared by casting in front metal cover of CD of PDMS and then curing the agents at 70°^{C} for 1 hour. Then the mold including the metal layer of CD is peeled off and simply a metalized stamp is obtained.

Figure 2- 5 Replica molding of the CD with PDMS

2.3 Lithographically Controlled Wetting

In order to pattern some nanostructure of graphene flakes we used an unconventional method called "Lithographically Controlled Wetting" (LCW). This technique has been developed by researchers of ISMN-CNR of Bologna [11]. LCW is a micro/nanofabrication process particularly attractive for soluble materials because it allows one to exploit self-organization of soluble functional materials with the spatial control provided by the stamp features. The stamp can be made of either rigid materials, such as metals, ceramics or rigid polymers, or by soft materials, such as polycarbonates or PDMS. LCW is suitable for large-area nanopatterning and is sustainable because of its simplicity and high transfer rate. LCW represents a valid alternative and often a finer route to obtain nanosized structures with respect to MIcroMolding In Capillaries (MIMIC) : in fact, while the latter is based on capillary forces that under specific surface tension conditions do not allow the filling of extremely small channels, the former is based on wetting-dewetting processes. Dewetting, which is not used in this work, is the opposite of the process of the spreading of a liquid on a substrate (wetting): it describes the rupture of a thin liquid film on the substrate (either a liquid itself, or a solid) and the formation of a discontinuous film made of droplets. The factor determining the wetting and dewetting is the so-called spreading coefficient S, which is defined as:

$$S = \gamma_{SO} - \gamma_{SL} - \gamma$$

where γ_{SO} is the surface tension substrate/air, γ_{SL} is the surface tension film/substrate and γ is the surface tension film/air. LCW general operation is represented in Figure 2-6.

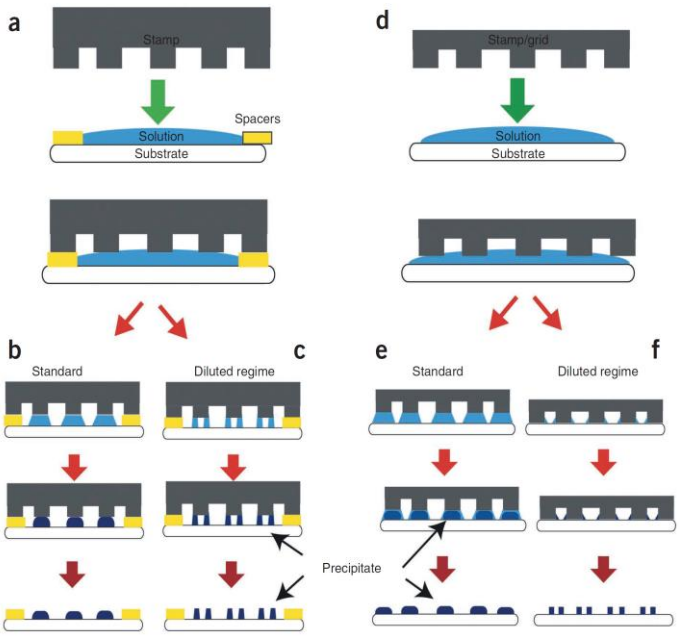

Figure 2- 6 Scheme of LCW. (a–c) Scheme of printing using prefabricated spacers (a) in the standard (b) and diluted (c) regime. (d–f) Scheme of printing using a floating stamp (d) in the standard (e) or diluted (f) regime. Whereas in standard conditions features with size comparable to the stamp protrusions are printed (b,e), in the diluted regime a split of the printed features with reduced size takes place (c,f).

When a stamp features is placed in contact with a liquid thin film spread onto a substrate (Figure 2.6a), the fluid layer develops instabilities, where the capillary forces pin the solution to the stamp protrusions, giving rise to an array of menisci (Figure 2.6b). As the critical concentration is reached, the solute precipitates from the solution onto the substrate within the menisci, giving rise to a structured thin film that replicates the protrusions of the stamp (Figure 2.6c, e). In particular low concentration regimes (Figure 2.6d), the menisci can be splitted under the same protrusion thus obtaining smaller structures (Figure 2.6f, g).

The interplay of protrusion size with the physical length scales of self-organization and growth phenomena gives rise to the deposition of a material into domains whose lateral dimension ranges from micrometers to nanometers. Since the concentrations of the solutions used in LCW are usually low (thus the quantity of deposited material is small), the nanostructures often end up with a thickness equivalent to a few molecular layers. In this regime, growth phenomena are less prone to develop defects due to roughening, secondary nucleation, and orientational transitions. Thus, LCW allows to deposit highly ordered low-dimensional small-size domains, which can be used to tailor the properties of the material by size[12,13].

Since the described process does not rely on specific interactions between the molecules and the surface, LCW is of general application in a large variety of soluble materials such as rotaxanes [14], discotic liquid crystals [15], molecular magnets [16,17,18], and organic semiconductors [19,20,21]. Using suitable stamps, this technique can be used also with aggressive chlorinated and fluorinated solvents.

2.4 Atomic Force Microscopy

In 1982 G. Binning, H. Rohrer, C. Gerber and E. Wiebel developed the scanning tunneling microscope, opening a new area in the surface science field. The limitation of this technique is the possibility to scan only conductive surfaces. The introduction of the Atomic Force Microscope (AFM), based on the atomic interactions rather than on the tunneling current, overcame this problem allowing the investigation of almost all the materials with physically relevant surface morphology. In more recent years other scanning probe techniques directly related to AFM have been introduced to probe also electrical, magnetical and elastic properties.

AFM is a relatively compact instrument, especially if compared to electron microscopies. It does not require vacuum to operate and can be placed on any stable workbench in a laboratory.

The key elements of an AFM are: 1) a local probe interacting with the surface; 2) a piezoelectric actuactor which allows sample or probe (stand alone configuration) motion; 3) an electronic system for detecting and amplificating the signal resulting from the probe-sample interaction; 4) a feedback system allowing to keep the probe-sample interaction stable by the definition of an appropriate setpoint; 5) a system to insulate the microscope from external noise, either mechanical or electrical. The basic operation mode is common to all the scanning probe techniques: a very sharp tip is attached to a cantilever spring which moves over a sample surface. When the tip is moved near the surface, different kind of interactions can take place, ranging from Van Der Waals and dipole-dipole up to magnetic forces. The resulting cantilever spring displacement, acting as a small dynamometer, is recorded as relevant physical signal by an optical lever. A laser beam is focused on the cantilever with an incidence angle θ and reflected via one or more mirrors to a four segment Position Sensitive Detector (PSD), after an optical path L (Figure 2-7).

Any small variation $\Delta\theta$ of the incidence angle will produce a Δz shift of the reflected spot in the photodiode, amplifying the angle variation as $\Delta z = L\Delta\theta$. This movement is detected by the PSD comparing the intensity of the signal from each segment, with a sub-Angström resolution. Two pairs of segments (upper and lower) give the values of vertical deflection of cantilever, known as topography or Z-signal. Another pair of segments (left and right ones) supplies the so called lateral force signal, related to the tilting of the cantilever due to torsional forces during scan.

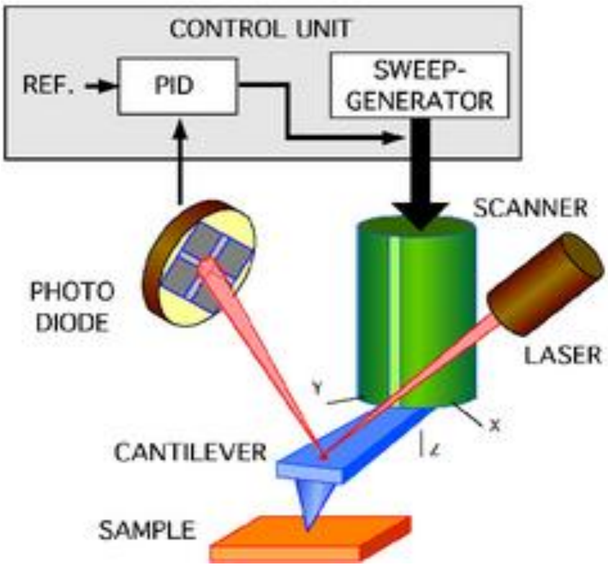

Figure 2- 7 Schematic representation of AFM equipment.

The piezoelectric can contract or elongate under the application of an electric bias with the direction of the elongation that is perpendicular to that of the applied voltage, thus allowing the movement in the x-y-z space. The Z signal goes to the Feedback electronics, which controls the piezoelectric scanner and regulates the interaction strength moving the piezoelectric in order to minimize the difference between the measured value and the required one.

2.4.1 The cantilever

As already mentioned, the probe of an AFM (Fig. 2.5) is the crucial part of the instrument and is made of a sharp tip (with a curvature radius in the order of nanometers) attached to a cantilever type-spring (in the order of microns).

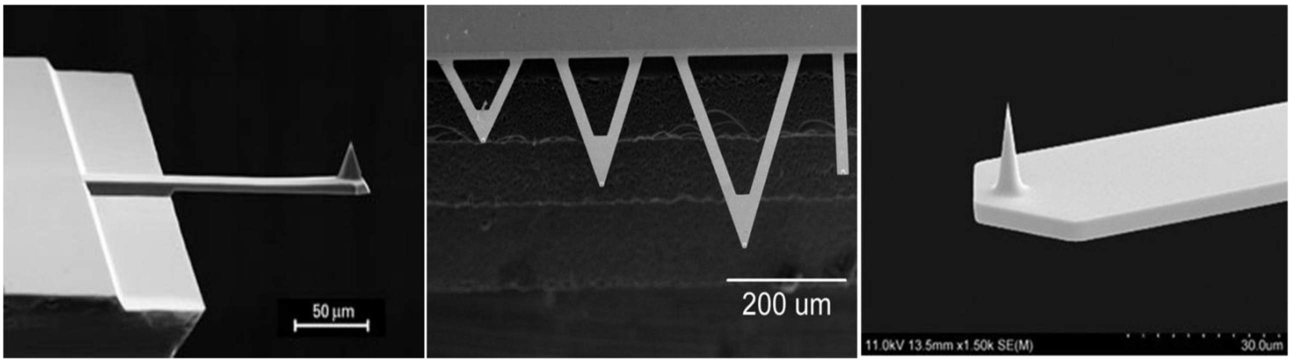

Figure 2- 8 Images of different cantilevers taken by Scanning Electron Microscope

The side of the cantilever opposite to the tip is fixed to a millimiter sized chip, which can be easily handled. The cantilever behaves as a dynamometer, hence subjected to Hook’s law, allowing to translate small forces into detectable displacements:

$$F = -k\Delta z$$

The resonance frequency of the cantilever is:

$$W_0 = \sqrt{\frac{k}{m}}$$

For a rectangular cantilever the spring constant k is calculated from the equation:

$$k = \frac{Ewt^3}{4l^3}$$

where *E* is the Young’s modulus of the cantilever and *l*, *w* and *t* its length, width and thickness respectively. For example, to obtain a resonance frequency in the range 10-100 KHz with a cantilever spring constant of ~0.1-1 N/m it is necessary a lever approximately 100 μm long and 1 μm thick. Such sizes are nowadays achievable by means of common microfabrication techniques.

To be effective the force sensor has to fulfill several requirements:

i) The spring constant *k* has to be small enough to detect small forces.

ii) The resonant frequency *w*0 has to be high enough to minimize sensitivity to mechanical vibrations.

iii) The tip has to be sharp enough to achieve high lateral resolution (of the order of 10^{-10} m).

The tip curvature is the real radius of the tip in the approximation that it is spherical and determines the size of the details that the AFM will be able to resolve. The aspect ratio instead is a measure of the opening angle of the cone representing the full tip, and establishes how deep the tip will penetrate between two adjacent structures on the surface.

2.4.2 Operating modes

Many forces are involved in the interaction between tip and surface. However the most relevant are dipole-dipole attractive interactions and ion core repulsive interaction (viz. Van Der Waals). These forces are described by the Lennard-Jones potential:

$$V(r) = c_1 \frac{1}{r_{12}} - c_2 \frac{1}{r_6}$$

where r is the distance from the surface, c_1 and c_2 are appropriate constants, the term to the sixth power of r represents the attractive Van Der Waals potential while the term r_{12} represent the strong repulsive potential when the tip is too close to the surface. In Fig. 2.9 the Lennard-Jones potential curve is represented.

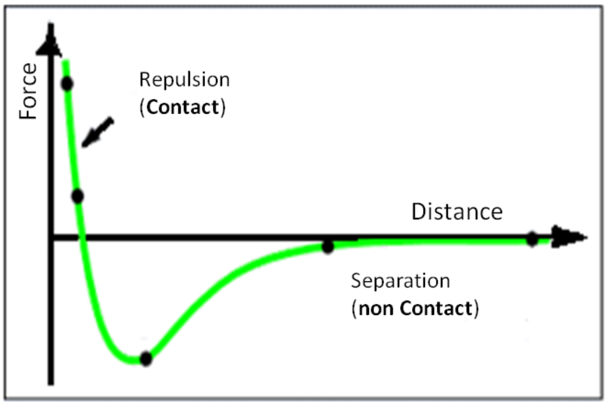

Figure 2- 9 Typical force-curve for a tip surface interaction.

When the cantilever is far from the surface, the cantilever is in the separation force regime and the potential varies slowly: the AFM operation mode is called “non-contact mode”. A stiff cantilever is forced to oscillate at a certain distance to the sample, without touching it. The forces between the tip and sample are quite low, of the order of pN (10^{-12} N). The detection scheme is based on measuring changes of the resonant frequency or of the oscillation amplitude of the cantilever.

On the contrary, if the cantilever works in the repulsive force regime, viz. very near to the surface, the operation mode is called “contact mode”. This mode enables a very high resolution but it enhances the probability to damage the cantilever. In contact force mode, the tip is constantly adjusted to maintain a constant deflection, and therefore constant distance from the surface. It is this adjustment that is displayed as topographic data. Because the tip is in hard contact with the surface, the stiffness of the lever needs to be less that the effective spring constant holding atoms together, which is on the order of 1 - 10 nN/nm. Most contact mode levers have a spring constant of < 1N/m.

There is a third operation mode that is “tapping mode”, and that is the one used in this thesis.

In this mode the cantilever is excited externally with constant excitation amplitude at a constant frequency near its resonance frequency. While scanning the surface, a feedback loop controls the cantilever-sample distance in order to maintain the amplitude constant. Typical oscillation amplitudes are in the range of 10 to 100 nm, thus encountering a wide range of tip-sample interactions within each cycle, including both attractive as well as repulsive forces.

The feedback system detects also the oscillation shift (phase signal), which can provide information about the surface composition and viscoelastic properties.

In this thesis a Smena (NT-MDT, Zelenograd, Russia) scanning probe microscope has been used. This microscope consists of standalone head, where the piezo scanner is positioned inside the head. The geometry of the piezo consists of three blocks of piezoelectric ceramic, they allow the movement of the tip in three orthogonal directions x, y, z. The sample is placed on a special sample holder, and the head is the only moving part. The microscope is equipped with a camera and often with a vibration insulator.

2.5 Electrical characterization

The electrical characterization by I-V curve is a finger print characteristic of our type of device. So in order to characterize the electrical performance of our devices we used a Keithley 2612 Source Meter for ISD measurements, controlled by a dedicated home-made acquisition software. For electrical testing, the bias was applied to the silicon electrode, while the top metal electrode was grounded. The electrical characteristics were measured on devices with 10^6 cross-points in parallel.

In order to test the quality of our junction we used our set-up on a Si/SiO_2 (native oxide)/Metal junction which confirms the results that can be found in the literature [22].

2.6 Optical Microscopy

Optical microscopy exploits UV-visible light to image objects. The simplicity of the technique and the minimal sample preparation required are significant advantages. The resolution limit is set by the Raleigh diffraction limit of the wavelength of the light, so objects spaced less than 0,2 micrometers are not distinguished.

The optical components of a modern microscope are shown in Figure 2.10. The optical path has to be very accurately set up and controlled. Despite of this, the basic operating principle of a microscope is quite simple. An objective lens with very short focal length (few millimeters) is used to form a highly magnified real image of the object. This magnification is carried out by means of two lenses: the objective lens which creates an image at infinity, and a second weak tube lens which forms a real image in its focal plane. The resulting image can be detected directly by the eye, imaged on a photographic plate brought onto the array detector of a digital camera.

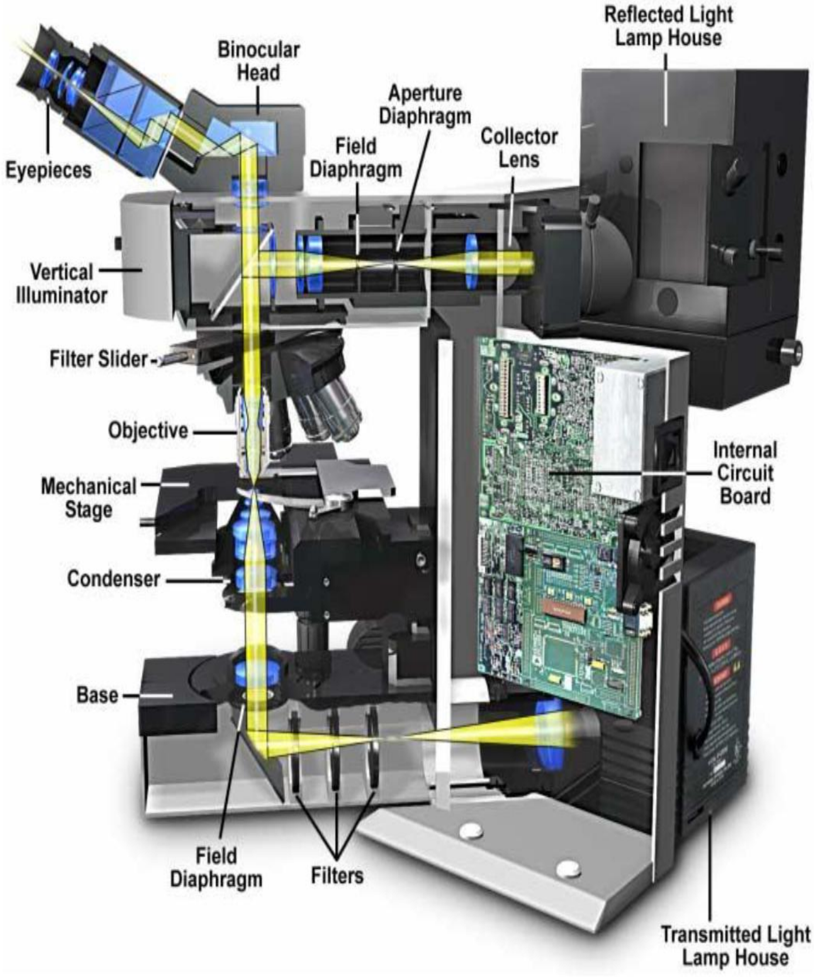

Figure 2- 10 Components of a modern microscope configured for both transmitted and reflected light.

Techniques working with different illumination modes have been developed such as Bright field, Dark field, Phase contrast, Polarized light, Hoffman modulation contrast, Differential interference contrast, Fluorescence [23].

Bright field microscopy is the simplest, with the sample being illuminated by transmitted white light. It presents however some limitations such as it can only image dark or strongly refracting objects effectively. Dark field microscopy is an illumination technique used to enhance the contrast in unstained samples. To view a specimen in dark field, an opaque disc is placed underneath the condenser lens, so that only light that is scattered by objects on the slide can reach the eye. Instead of coming up through the specimen, the light is reflected by particles on the slide. This produces the classic appearance of a dark, almost black, background with bright objects on it. In this work, optical microphotographs have been recorded both in bright/dark field using 5x, 10x, 20x and 50x short working distance objectives and a digital camera (Nikon High-speed Live Display Color Camera HeadDS-2Mv).

2.7 Scanning Electron Microscopy

2.7.1 Working principle

An electron microscope is a microscope that uses an electron beam for imaging objects, thus allowing an increase in resolution of several orders of magnitude. The development of the electron microscope was based on theoretical work done by Louis de Broglie, who found that wavelength is inversely proportional to momentum. In 1926, Hans Busch discovered that magnetic fields could act as lenses by causing electron beams to converge to a focus. The first operational electron microscope was presented by Ernst Ruska and Max Knoll in 1932, and 6 years later Ruska had a first version on the market. In 1986 Ruska received a Nobel Prize in physics for his "fundamental work in electron optics and for the design of the first electron microscope". The original form of the electron microscope was a Transmission Electron Microscope (TEM), which uses high energy electrons to image the sample, while Scanning Electron Microscope (SEM) collects secondary electrons to get an image. Figure 2.11 shows the basic components of a SEM: (1) the electron column, (2) the specimen chamber, (3) the vacuum pumping system and (4) the electron control and imaging system.

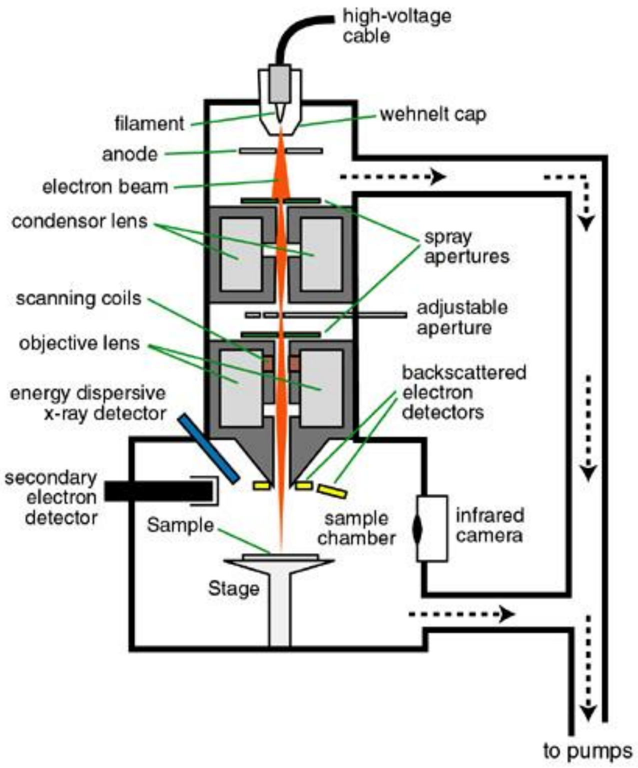

Figure 2- 11 Schematic representation of SEM instrument.

In a typical configuration, an electron beam is thermionically emitted from an electron gun fitted with a tungsten filament cathode. Tungsten is normally used in thermionic electron guns because it has the highest melting point and lowest vapor pressure of all metals, thereby allowing it to be heated for electron emission, and because of its low cost. Other types of electron emitters include lanthanum hexaboride (LaB6) cathodes, which can be used in a standard tungsten filament SEM if the vacuum system is upgraded, and field emission guns (FEG), which may be of the cold-cathode type using tungsten single crystal emitters or the thermally-assisted Schottky type, using emitters of zirconium oxide. The field emission source provides higher resolution; high stability and high current in a small spot size and generates high x-ray fluxes for chemical analysis at high resolution conditions. The electron beam, which typically has an energy ranging from 0.5 keV to 40 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in the final lens, which deflect the beam in the x and y axes so that it scans in a raster fashion over a rectangular area of the sample surface.

When the electron beam strikes a sample, these electrons will scatter through the sample within a defined area called the interaction volume (Figure 2-12).

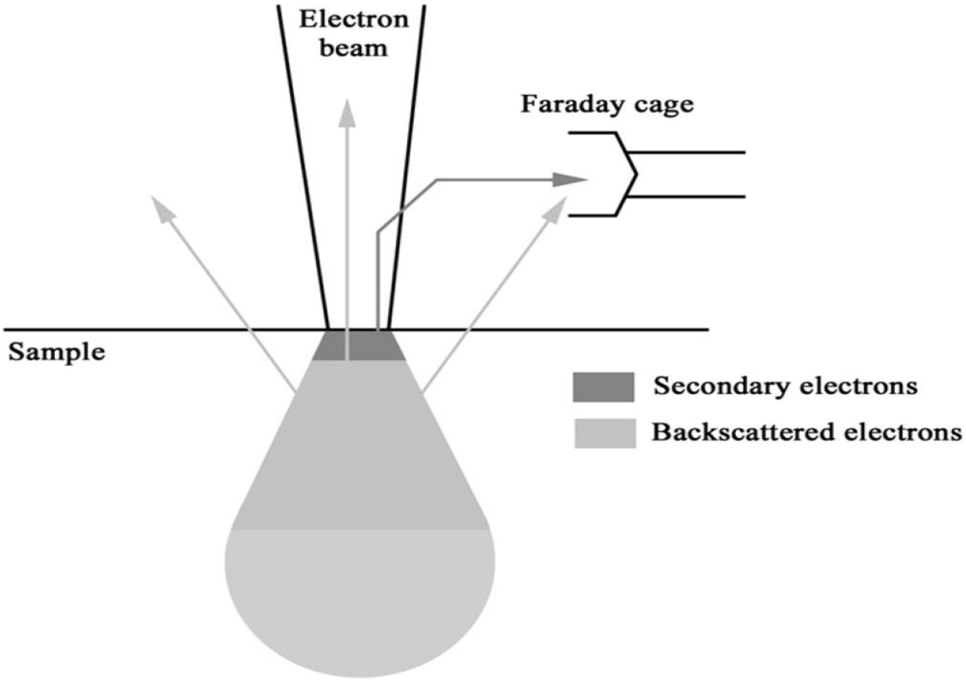

Figure 2- 12 Scheme of the interaction between an accelerated electron beam and the sample.

During the electron beam-specimen interactions, many signals are produced, like transmitted electrons (TEM), secondary electrons (SEM), backscattered electrons (BSE) diffracted backscattered electrons (EBSD, that are used to determine crystal structures and orientations of minerals), photons (characteristic X-rays that are used for elemental analysis and continuum X-rays), visible light (cathode luminescence-CL), and heat. Secondary electrons are low energy electrons and when produced deeper within the interaction volume, will be absorbed by the sample. Only secondary electrons close to the surface will be able to escape the specimen. The weakly negative secondary electrons will be deflected by a positive pull exerted by the Faraday cage surrounding the secondary electron detector and therefore will contribute to the image formation. Backscattered electrons are also produced deep within the sample but have a much higher energy and because of this, are able to escape from deeper within the interaction volume. Because of their high energy, backscattered electrons will not be deflected by the Faraday cage and therefore not contribute to the image formation. Only a few backscattered electrons will interfere with the signal for secondary electrons. The SEM used in this work is an Hitachi-S4000 FEG-SEM (Figure 2.11; max resolution: 1.5 nm; acceleration voltage: 0.5kV-30kV; magnification: 20X-200.000X; filament: cold-cathode field emission).

2.7.2 Sample coating

For SEM imaging, samples must be electrically conductive and grounded to prevent electrostatic charge accumulation at the surface. Metal specimens require little preparation apart from a good conventional cleaning procedure. Instead, non-conductive specimens are usually coated with an ultrathin layer (few nm) of an electrically-conducting material (commonly gold, but also platinum, osmium, tungsten and graphite) deposited by low vacuum sputtering or high vacuum sublimation. Other than preventing charge accumulation, there are two reasons for coating: to increase signal and surface resolution, especially with samples containing low atomic number elements. The improvement in resolution arises mainly from the enhancing of the backscattering and secondary electron emission near the surface. Depending on the instrument, the resolution ranges between less than 1 nm and 20 nm. For SEM analysis, the sample is normally required to be completely dry, since the specimen chamber is at high vacuum; thus living cells and tissues usually require chemical fixation to preserve their structure.

2.8 Wettability Measurements

In many applications the wet ability of a surface or ability of liquids to wet surfaces can be a key factor in a product s performance or be a significant issue in a manufacturing process, for examples cleaning of glassware, lubrication, crop spraying, photographic processing, coating surfaces, etc.

Wetting refers to the study of how a liquid deposited on a solid (or liquid) substrate spreads out. When a drop is placed down on very clean glass, it spreads completely. By contrast, the same drop deposited on a sheet of plastic remains stuck in its place. The conclusion is that two regimes of wetting can be identified: total and partial wetting (Figure 2.13a), according to the difference between the surface tension, viz. the surface energy per unit area Esub of the dry substrate and that of the wet substrate. The parameter distinguishing the two regimes is called spreading parameter S [24]:

$$S = [E_{sub}]_{dry} - [E_{sub}]_{wet} = \gamma_{SV} - (\gamma_{SL} + \gamma)$$

where the three coefficients γ are the surface tensions at the solid-air, solid-liquid and liquid-air interfaces respectively. In total wetting the parameter S is positive and, as a result of the competition between molecular and capillary forces, the liquid spreads completely forming a continuous thin film with contact angle $\theta=0$. In partial wetting, S is negative and the liquid does not spread forming at equilibrium a hemi-spherical cap resting on the substrate with a non-zero contact angle. Depending on the contact angle, the liquid is "mostly wetting" when $\theta \leq \pi/2$ whereas is "mostly non-wetting" when $\theta > \pi/2$ (Figure 2.13b) [37].

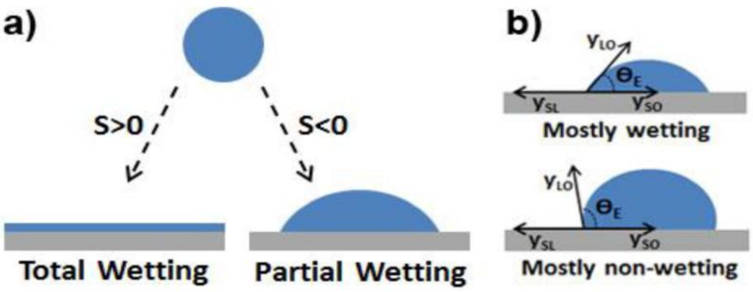

Figure 2- 13 Schematic drawing of (a) the two wetting regimes, and (b) drops of "mostly wetting" and "mostly non-wetting" liquids on a solid substrate.

The contact angle is a measure of the ability of a liquid to spread on a surface. The method consists to measure the angle between the outline tangent of a drop deposited on a solid and the surface of this solid. The contact angle is also linked to the surface energy.

A contact angle measurement gives some different information:

• the affinity of a liquid to a solid surface. If water is used to measure the contact angle one can deduce the hydrophobic ($\theta > 90°$) or hydrophilic ($\theta < 90°$) character of the surface;

• if several reference liquids are used, the surface energy of the solid can be calculated, discriminating between polar and dispersive components.

• the measure of the hysteresis between advancing angle and recessing angle give informations on non-homogeneity of the surface (roughness, contamination, etc).

One approach commonly used to measure contact angles of solid substrates is the optical tensiometry (goniometry). Optical tensiometry involves the observation of a sessile drop of a liquid on the substrate. Analysis of the shape of a drop of test liquid placed on a solid is the basis for optical tensiometry. The basic elements of an optical tensiometer include a light source, sample stage, a siring to make the droplet, lens and image capture device (Figure 2.14). The contact angle instrument used all along this work is a contact angle meter DGD - DX model (DIGIDROP).

Contact angle can be accessed directly by measuring the angle formed between the solid and the tangent to the drop surface. With this technique it is possible to use a great variety of solid substrates provided they have a relatively flat portion for testing, and can fit on the stage of the instrument. Testing can be done using very small quantities of liquid.

The assignment of the tangent line that defines the contact angle is a factor which can limit the reproducibility of contact angle measurements. Conventional optical tensiometry relies on the consistency of the operator in the assignment of the tangent line. This can lead to significant error, especially subjective error between multiple users. In some case it is possible to analyze the drop by using computer analysis of the drop shape to generate consistent contact angle data.

In addition the amount of surface sampled for each measurement is limited and multiple measurements should be used to characterize a surface.

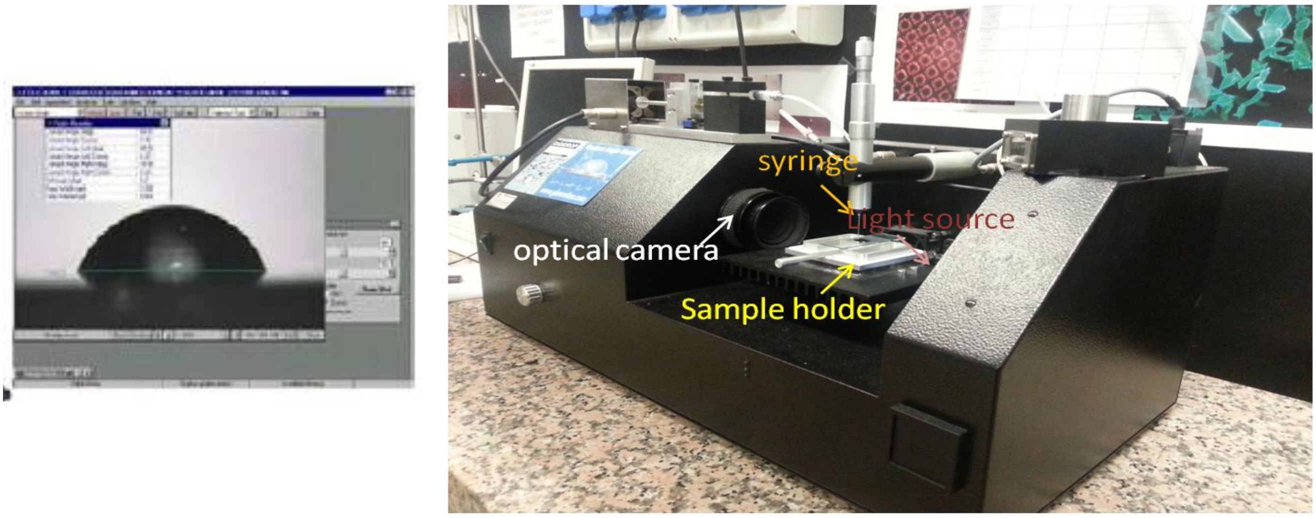

Figure 2- 14 Photo of a contact angle instrument.

2.9 Impedance Spectroscopy

Since impedance spectroscopy (IS) deals directly with complex quantities, its history really begins with the introduction of impedance into electrical engineering by Oliver Heaviside in the 1880s. His work was soon extended by A.E. Kennelly and C.P. Steinmetz to include vector diagrams and complex representation. It was not long before workers in the field began to make use of the Argand diagram of mathematics by plotting immittance response in the complex plane, with frequency an implicit variable. Electrical engineering examples were the circle diagram introduced by C.W. Carter [25] and the Smith-Chart impedance diagram of P.H. Smith [26]. These approaches were soon followed in the dielectric response field by the introduction in 1941 of the Cole-Cole (or Nyquest curve) plot: a plot of ε'' on the y (or imaginary) axis vs. ε' on the x (or real) axis. Such complex plane plots are now widely used for two-dimensional representation of the response of all four immittance types. Finally, three-dimensional perspective plots that involve a log-frequency axis were introduced to the IS area by the author and his colleagues in 1981[27]; these plots allow complete response at a given immittance level to be shown in a single diagram. Because IS analysis generally makes considerable use of equivalent circuits to re-present experimental frequency response, the whole history of lumped-constant circuit analysis, which particularly flowered in the first third of the century, is immediately relevant to IS. Since then, much work has been devoted to the development of theoretical physicochemical response models and to the definition and analysis of various distributed circuit elements for use in IS-equivalent circuits along with ideal, lumped elements like resistance and capacitance. The preferred analysis method for fitting of IS data to either equivalent circuits or to a mathematical model is complex nonlinear least squares fitting (CNLS), introduced to the field in 1977 by Macdonald and Garber [28]. In this procedure, all the parameters of a fitting model are simultaneously adjusted to yield an optimum fit to the data.

2.9.1 Definitions and Distinctions

Impedance Spectroscopy is the measure of the opposition that a circuit presents to a current when a voltage is applied. In quantitative terms, it is the complex ratio of the voltage to the current in an alternating current (AC) circuit. Impedance extends the concept of resistance to AC circuits, and possesses both magnitude and phase, unlike resistance, which has only magnitude. When a circuit is driven with direct current (DC), there is no distinction between impedance and resistance; the latter can be thought of as impedance with zero phase angle.

It is necessary to introduce the concept of impedance in AC circuits because there are two additional impeding mechanisms to be taken into account besides the normal resistance of DC circuits: the induction of voltages in conductors self-induced by the magnetic fields of currents (inductance), and the electrostatic storage of charge induced by voltages between conductors (capacitance). The impedance caused by these two effects is collectively referred to as reactance and forms the imaginary part of complex impedance whereas resistance forms the real part.

The symbol for impedance is usually Z and it may be represented by writing its magnitude and phase in the form $|Z|\angle\theta$. However, complex number representation is often more powerful for circuit analysis purposes. The term impedance was coined by Oliver Heaviside in July 1886. Arthur Kennelly was the first to represent impedance with complex numbers in 1893.

Impedance is defined as the frequency domain ratio of the voltage to the current. In other words, it is the voltage–current ratio for a single complex exponential at a particular frequency ω. In general, impedance will be a complex number, with the same units as resistance, for which the SI unit is the ohm (Ω). For a sinusoidal current or voltage input, the polar form of the complex impedance relates the amplitude and phase of the voltage and current. In particular,

- The magnitude of the complex impedance is the ratio of the voltage amplitude to the current amplitude.
- The phase of the complex impedance is the phase shift by which the current lags the voltage.

The reciprocal of impedance is admittance (i.e., admittance is the current-to-voltage ratio, and it conventionally carries units of siemens, formerly called mhos) [29].

2.9.2 IS measurements

The impedance spectroscopy measurements were carried out using a FRA2 µAutolab; TYPE III, and the measurements frequency was swept from 0.1 Hz–100 kHz with 0.2V of amplitude.

2.10 Raman spectroscopy

Raman spectroscopy owes its name to the discoverer of the homonymic effect, the Indian scientist Chandrasekhara Venkata Raman (1888-1970), among the founders of scientific research in India, and Asia’s first Nobel Prize winner in science. Early in 1928, after years of accurate experiments on the scattering of light, came his discovery of a “new radiation” as he simply called it, which was soon to be recognized as an entirely new phenomenon and named after him. C. V. Raman was then awarded the Nobel Prize in physics in 1930, remarkably soon after his discovery [30] (Miller and Kauffman 1989).

Raman spectroscopy probes molecular and crystal lattice vibrations and therefore is sensitive to the composition, bonding, chemical environment, phase, and crystalline structure of the sample material. These characteristics make it an exceptional method for unambiguously identifying materials in any physical form: gases, liquids, solutions, and crystalline or amorphous solids. Raman spectroscopy has thus become an established technique for the study of cultural heritage materials over the past 20 years.

2.10.1 The Raman effect

The basic theory of the Raman effect was developed long before its discovery; anomalies in the fluorescence emissions had in fact been described as early as 1878. Later on the effect itself had been repeatedly predicted by applying quantum mechanics to molecules [31] . When light quanta of energy $h\nu_0$ hit matter, a small fraction of the incident radiation is scattered, either elastically (Rayleigh scattering, fig. 2.15a) or inelastically, giving rise to emitted photons of energies either higher or lower than that of the incoming radiation: this is what is called the Raman effect. The photons emitted at the lower energy, $h\nu_0 - h\nu_1$, are called Stokes Raman photons (fig. 2.15b). The energy difference $h\nu_1$ arises from the energy lost from the incoming photon to promote the molecule into an excited vibrational level of the ground electronic state. Anti-Stokes Raman photons (fig. 2.15c) appear at the same energy difference in relation to the excitation line, but on the high-energy side of the Rayleigh photons. The intensities of anti-Stokes Raman bands are very weak, and temperature dependent (following the Boltzmann law). Consequently, Raman spectra reported in the literature commonly include only the Stokes portion.

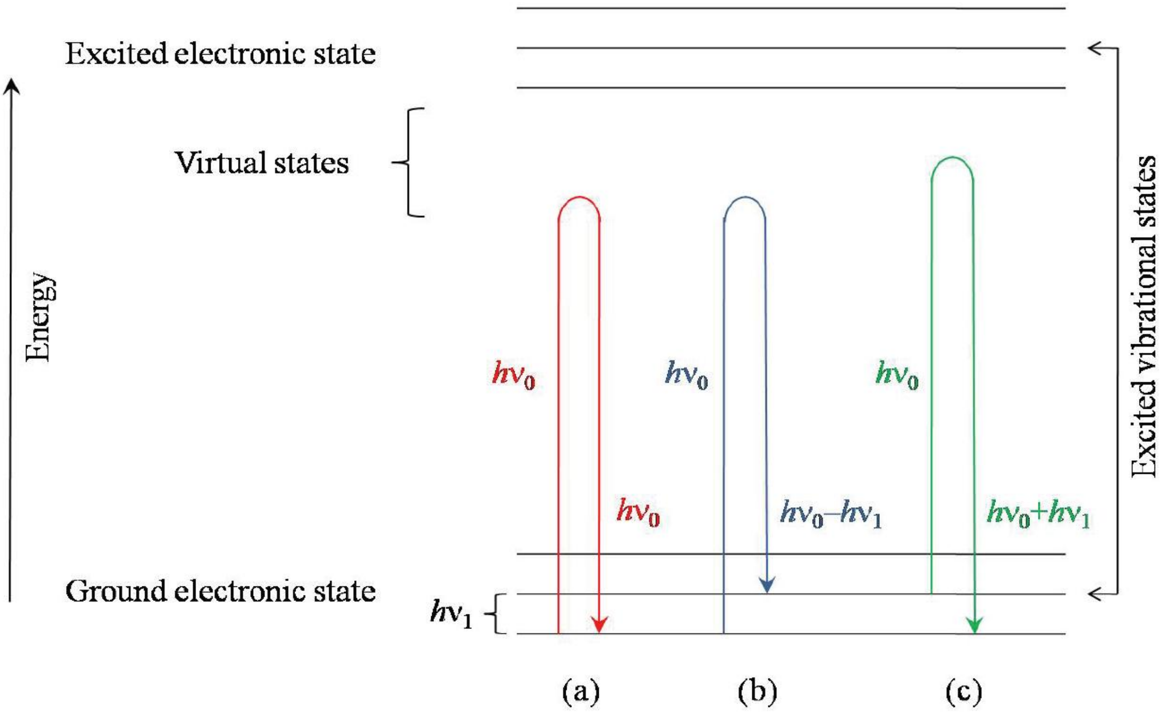

Figure 2- 15 Schematic representation of the (a) Rayleigh, (b) Stokes Raman and (c) anti- Stokes Raman scattering effect

Figure 2-15 describes a single vibrational mode of a diatomic molecule. Other photons of potentially different energies, $h\nu_i$, will be generated by a polyatomic molecule for each of its i normal vibrational modes meeting the selection rules for Raman scattering. By spectrally sorting the Raman scattered photons generated from these Raman-active modes, a highly characteristic vibrational spectrum can be obtained for the molecule under study. In order to make Raman spectra easier to evaluate, frequency or even better wavenumber1 shifts are usually recorded; the exciting radiation defining the zero of this recorded variable. The wavenumber[1] shift for a Raman band is in fact constant, regardless of the excitation line used (which might affect only the relative intensity of lines), and it directly relates to the energy of the vibrational level being probed, $h\nu_i$. It is therefore analogous to the vibrational information provided by IR absorption spectroscopy, but complementary to it rather than identical, owing to the different selection rules governing Raman scattering (mandatory change in polarizability) and IR absorption (mandatory change in dipole moment). Further explanations of the physical laws governing Raman scattering, and exact

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[1] wavenumbers are commonly used to tabulate spectroscopic data, and can be defined in terms of wavelenghts ($\tilde{\nu} = 1/\lambda$) as well as in terms of frequencies ($\tilde{\nu} = \nu/c$, with c the velocity of light). They are measured in cm^{-1}.

calculations of the wavenumber positions and relative intensities of Raman bands can be found in a variety of reference books (e.g. Schrader 1995), and will therefore not be detailed here.

Here the confocal micro-Raman spectra were recorded in backscattering geometry with a Renishaw RM 1000 system using the 488 nm (2.54 eV) Ar+ laser line focused on the sample through a ×80X objective lens forming a laser spot of approximately 1 μm. The laser power was kept low enough to avoid damaging and heating of graphene (70 μW that corresponds approximately to 1 kW/cm2). In order to obtain a good signal-to-noise ratio, the spectrum acquisition time was typically 30 min. The spectrometer resolution (grating 2400 l/mm) is about 2 cm^{-1} for the laser line used.

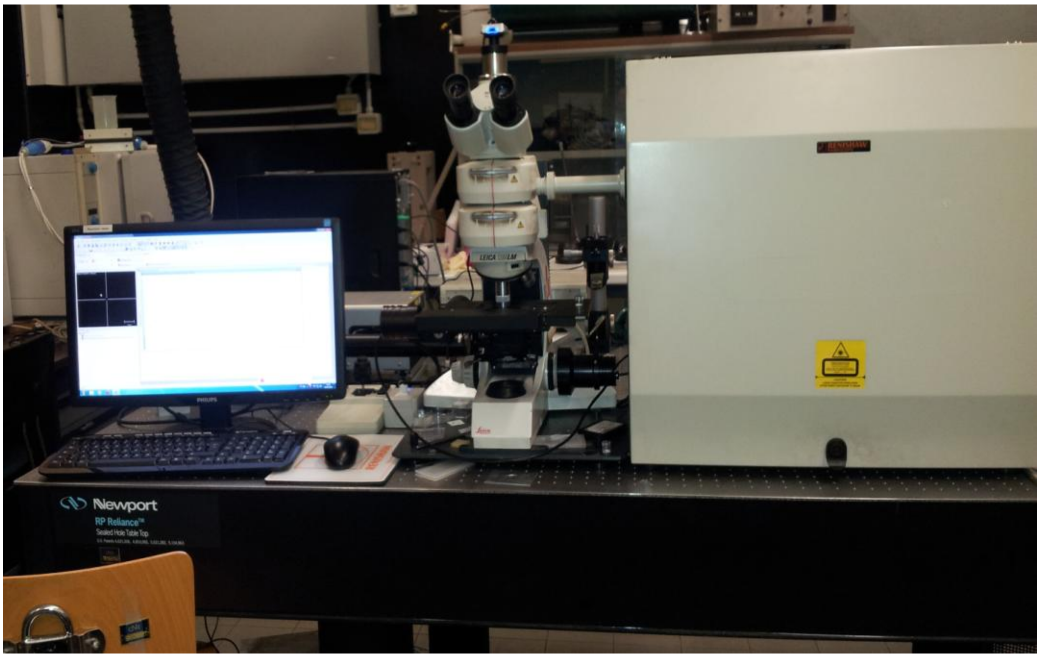

Figure 2- 16 Photo of the Raman Spectra machine

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Chapter 3

Parallel Local Oxidation lithography (pLOx)

This chapter describes pLOx procedure in detail as nanopatterning procedure, applicable in device fabrication and surface architectures. The effect of several parameters in pLOx process has been studied.

3.1 Introduction

Local Oxidation Nanolithography of Silicon has been developed since **1990** with the scanning tunneling microscope (STM) [1,2,3]. However, the versatility of the atomic force microscope (AFM) for operating with conducting and non-conducting samples alike has prompted its application for the local oxidation of surfaces to fabricate nanometer-scale structures and devices. Nano-oxidation has been applied to yield patterns made of dots and lines of controlled size and positions that have been used to demonstrate bit writing with areal densities of about 1 terabit/in. [2,4,5] to generate sets of interdigitated lines with a periodicity of 13 nm,[6] and to fabricate submicrometer gratings [7] and optical waveguides with subwavelength cross sections [8]. Local oxidation nanolithography has also been applied to fabricate several electronic devices with critical features in the nanometer range, such as single electron transistors, [9] superconducting interference devices, [10] or antidot lattices [11]. Local oxidation has also been proven useful to seed defects acting as nuclei for crystallization or anchoring sites for receptors of biomolecules, [12] to modify self-assembled monolayers, [13] or to fabricate templates to orient growth of molecular thin films [14]. Moreover, negative features, such as nanosized holes and trenches, can be achieved by anisotropic etching of the oxide layer [15].

Local oxidation is compatible with ambient operation, microelectronic processing, and does not require masks or lift-off. In terms of resolution and writing speed, it is comparable to state-of-the-art electron-beam lithography, with the advantage of being more sustainable in terms of cost and being based on a widespread microscopy technique. The shortcomings arise from the strictly serial nature of the process that hinders its technological implications and by the limited area in which fabrication can be performed. The patterned area is limited by the maximum scan size of the piezoeletric scanner, usually in the 10^{-3} mm^2 range. It would be therefore extremely desirable to transfer the same process developed for AFM into a parallel fabrication method capable of similar performance in terms of positioning and feature definition, but covering centimeter-square regions. Although parallel local oxidation was demonstrated by using an array of 50×1 parallel cantilevers [16], current technical limitations in the fabrication and operation of arrays of parallel cantilevers have slowed down this approach. Nano-oxidation has strong similarities with conventional anodic oxidation. The AFM tip is used as a cathode and the water meniscus formed between tip and surface is the source of the oxyanions species. The strong localization of the electrical field lines within the meniscus gives rise to a nanometer-sized oxide dot [17,18]. The physics and chemistry of individual local oxidation processes are rather general and do not imply the use of an AFM tip as a cathode to perform the oxidation. Consequently, a setup can be envisioned in which the cathode is an array of metallic protrusions grown, deposited, or attached onto a solid support.

Recently Cavallini et all. [19] demonstrated the possibility of local oxidation from single to parallel local oxidation. They showed that local oxidation can be effectively used with stamps brought into intimate contact with a silicon oxide surface. Figure 3-1 shows the development of local oxidation from single (figure 3-1A) to parallel local oxidation (figure 3-1B) Where the stamps are made of a metallic films grown onto a polymeric support with the groves made of lines or dots.

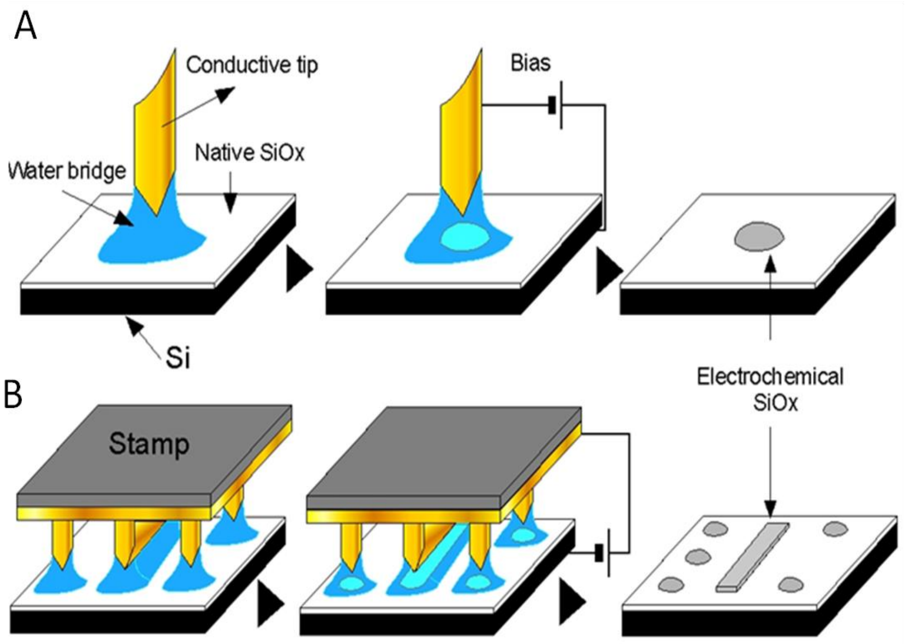

Figure 3- 1 Scheme of local oxidation. (A) Single electrochemical local oxidation of silicon substrate as a tip-based process. (B) Parallel electrochemical local oxidation of silicon made by metalized soft stamp.

By replacing the metalized stamp instead of SPM tip we became able to grow many oxide structures in parallel in the same time in a large scale, up to 1cm^2 area. The facilities which is needed to perform the local oxidation by using stamp is much cheaper since here it is used an home-built machine which was introduced in chapter 2 as a main tool, a power supply as a source for applying the bias, and a simple chamber to control the humidity, all these make the Parallel local oxidation much faster, easier and cheaper than local oxidation lithography.

As it is indicated in the figure 3-1B, while the set up is kept under humidity controlled ambient, due to the capillary force between the features of the metalized stamp and substrate the water bridge will occur and simply an electrochemical cell is created where silicon acts as anode, metalized stamp as cathode and water bridge as an electrolyte therefore, by applying an adequate bias under optimized condition an electrochemical reaction can occurs.

The accepted explanation of the oxidation of silicon surfaces requires the formation of a water meniscus between metalized stamp and the sample. Oxygen ions (OH^{-},O^{-}) are produced by the hydrolysis of the water within the meniscus. The ions are driven through the oxide by the electrical field. At the Si/ SiO_2 interface they react with holes h+. So, the local oxidation as a well known and promising procedure to grow the e-SiO2 nanostructures followed the electrochemical oxidation reaction which can be written as;

$$Si + 2H_2O \longrightarrow SiO_2 + 4H^{+} + 4e^{-} \quad \text{Anodic reaction (Oxidation)} \quad (1)$$

$$4H^{+} + 4e^{-} \longrightarrow 2H_2 \quad \text{Cathodic reaction (Reduction)} \quad (2)$$

Moreover the aging effect on the fabricated oxide nanostructures was investigated. It is identified that the height of the fresh nanostructures decreased by almost 40% within a few weeks and reaches the mean thick of ~2 nm. This effect could be explained due to collapsing of the SiOx which results much porous than conventional thermal SiO_2.

3.2 Effective experimental parameters on pLOx

The nanopatterning by pLOx performed via a simple set up and under optimized experimental parameters of applied voltage *V*, oxidation time *t*, *RH*, and the applied force *F*. To make the oxidation procedure as reproducible as possible, these parameters were systematically investigated.

Firstly the effect of bias by taking *variable V* and *t* (2 *min),* and *RH* (90%) has been studied. A constant voltage (DC) was applied across the electrodes and the flowing current was measured by an amperometer (Digital multimeter Fluke 112) in series with the electrodes [20,21] The oxidation occurs when the stamp and the silicon are in contact and a voltage ≥ 30 V is applied. For these voltages circulates a current density ≥ 25 μA cm^{-2}, that is the minimum current useful observed to oxidize the silicon. Usually we applied 30 V with a circulating current varying, for different experiments, from 150 to 230 μA cm^{-2}.

The second parameter was *variable t*; while *V* (30 *V*), *and RH (* 90%) . The high current density flowing between the stamp and substrate makes the oxidation process fast and, therefore, the nanostructures are produced in less than 1 min [22].

The effect of *variable RH*; by keeping *V* (36 *V)* , and *t* (2 *min)* , has been investigated . The oxidation process occurs over all the range $10 \leq RH \leq 95\%$, but the *RH* values affect the height of the oxide lines. The detailed investigation also by C. Albonetti [23] shows by increasing in RH% the height of oxide structures is increased (figure 3-2). This behavior is related to the thickness of the water layer adsorbed on the stamp and the silicon substrate.

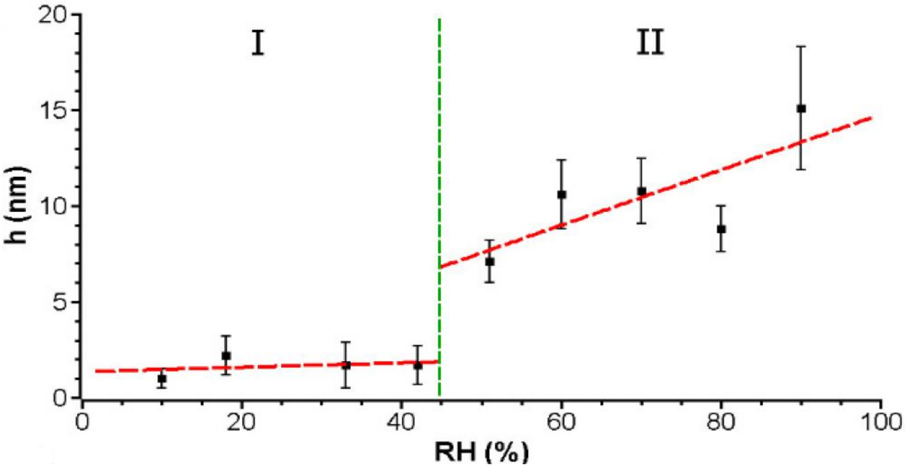

Figure 3- 2 Height of the oxide lines with respect to the relative humidity. In the range $10\% < RH < 40\%$ the height is fixed at ≈2 nm with a growth factor 0.01 nm/% (slope of the linear fit). In the range $40\% < RH < 90\%$, the height of the oxide lines increases from 7 to 15 nm with growth factor 0.35 nm/%. The error bars of the measurements are overestimated using the FWHM of the height distribution graphs [23].

The quality of the contact between metalized stamp and silicon substrate was studied by monitoring the resistance in between stamp and substrate. This parameter as an applied force (F measurements) was studied also by C. Albonetti [23] . For instance, a load cell [24] (RS-components 632-736) was used to measure the force applied by the stamp to the substrate. We fixed a conductive substrate (silicon substrate covered by 50 nm of Au) on the load cell cantilever, we brought the stamp (fixed on the stamp-holder) in contact with the substrate by the micrometric screw, and we measured the variation of the electrical resistance between the stamp and the substrate with respect to the displacement of the micrometric screw. At the same time, the downward movement of the micrometric screw bends the load cell cantilever (deflection of the cantilever expressed in *V*), so we are able to correlate the displacement of the micrometric screw with the force applied on the surface. The resistance–voltage–position graph (figure 3-3) shows two different regions (I and II) separated by a dashed line. In region I, the resistance roughly follows an exponential decay, in agreement with the conformal adjusting of the PDMS stamp on the surface, while the deflection of the cantilever increases with a power law trend. When the stamp is conforming to the substrate (region II), the resistance graph shows a flat region (indicating a good electrical contact). The deflection of the cantilever is proportional to the force and follows a linear trend versus the displacement of the micrometric screw. Usually, the oxidation process has been realized when we are inside this flat resistance region. Here, the force applied from the stamp to the substrate ranges from 0.5 to 20 N[1].

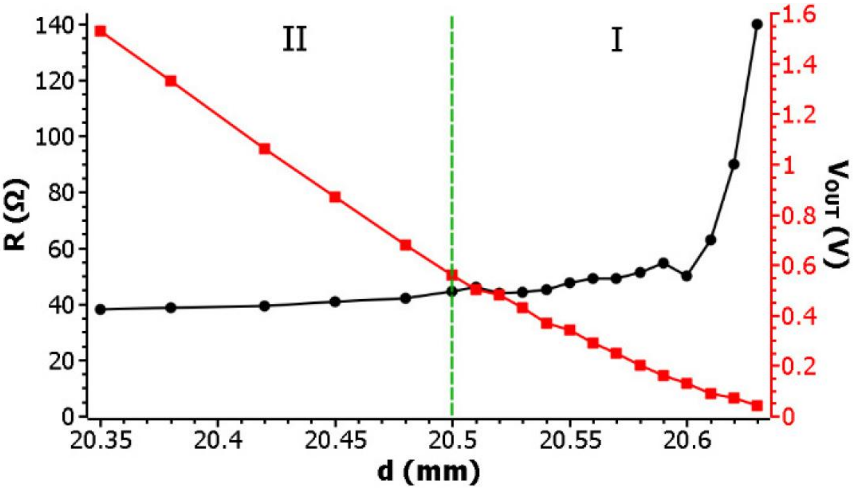

Figure 3- 3 Electrical resistance (*Ω*) between the stamp and the substrate measured by varying the displacement of the micrometric screw (mm) and corresponding output voltage of the load cell [20].

Chemical analyses are necessary to verify the quality of the oxide. We used two techniques: etching of the samples by means of a fluoridric acid (HF) solution [25], and analysis of the surface chemical composition by x-ray photoemission spectroscopy (XPS). The oxide lines etched by HF solution (Sigma Aldrich) indicate that the nanostructures are made of silicon oxides. It was found that the etching rate of anodic oxide (64 A° s−1) is much larger than that of thermal oxide (4 A° s−1). In addition, measurements with a spectrophotometer have been performed to measure the anodic oxide thickness and its porosity. The average of the measured oxide thickness was 128 ± 2 A° , while its estimated refractive index was 1.3 (1.5 for thermal oxide [22]). As a consequence, the anodic oxide exhibits 30% more porosity than the thermal oxide. The XPS measurements (Mg Kα source; hν =

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[1] The load cell measures a voltage $VOUT$ (V) proportional to the displacement of four strain gauges in a Wheatstone bridge (WB) configuration. $VOUT = VSk\varepsilon$, where $VS = 12$ V is the WB voltage supply, $k = 2$ is the gauge factor and ε is the strain. ε is related to the stress σ by the Young's modulus E ($EPDMS = 0.4$ MPa), $\sigma = E\varepsilon$. σ is a pressure $\sigma = F \cdot A{-}1$, where F is the force (to measure) and A (stamp's area 7 mm × 7 mm) the surface under pressure. Finally $F = AEVOUT(VSk)$

1253.6 eV) were performed on patterned and unpatterned surfaces to understand how the pure water anodic oxidation process changes the chemical composition of the surface. Wide scan XPS spectra (figure 3-4(a)) clearly reveal the presence of C, O and Si at the surface.

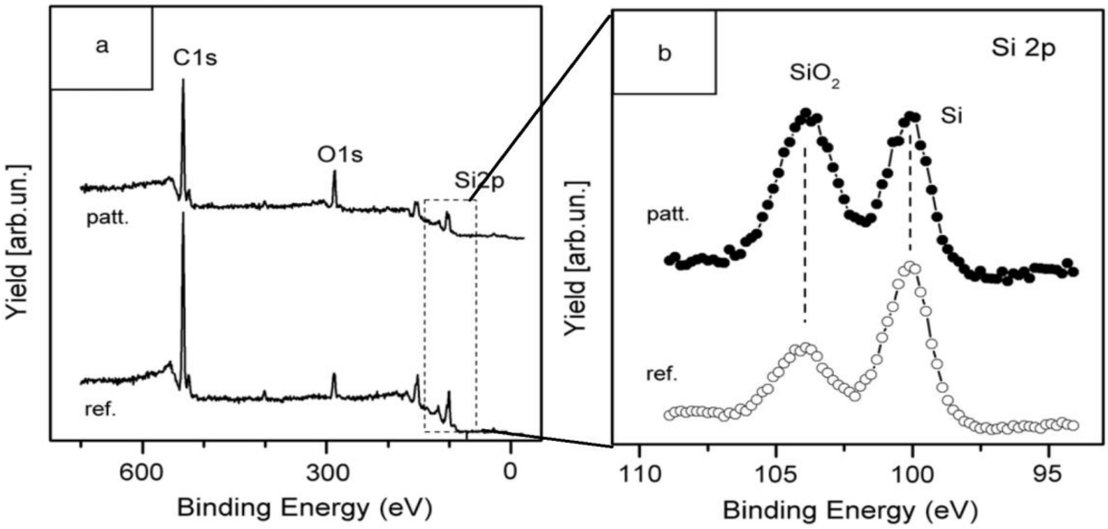

Figure 3- 4 (a) XPS spectra measured with a Mg Kα source (1253.6 eV). Panel (a): XPS wide scans of a reference silicon wafer with native surface oxidation and the patterned sample prepared by means of the PDMS stamp. Both XPS spectra show the contribution of carbon, oxygen and silicon. Panel (b): detail of the silicon 2p peak line shapes. The binding energies of the two peaks indicate the presence of different silicon chemical states, namely pure Si (BE 99.8 eV) and SiO2 (BE 104 eV). The intensity of the SiO2 peak for the patterned sample (filled circles) is roughly twice the one of the unpatterned silicon wafer (open circles).

The presence of C is typical of samples not produced in ultra-high vacuum and is due to carbonaceous contamination. The peak of Au is absent, indicating that the stamp does not release gold clusters to the surface. In particular, the detailed Si 2p spectra (figure 3-4(b)) evidence the chemical states of the Si atoms. The binding energies (BE) of the two peaks coincide with Si^{0+} (BE ~ 100 eV) and Si4+ (BE ~ 104 eV) valence states [26]. They indicate that the material probed by XPS is mainly composed of silicon and silicon dioxide (SiO_2). Comparing the patterned and unpatterned silicon surfaces, the intensity of the Si peak is roughly halved, as expected from a sample with the surface covered approximately for the 50% by oxide lines high 10 nm. In fact, the typical XPS depth sensitivity to the chemical composition of the sample is of the order of ~3λ, where λ is the attenuation length of the photoelectrons escaping from the surface. For the Si 2p signal (λ ~ 3 nm) the depth sensitivity is ~9 nm or lower than the height of the oxide lines (10 nm); therefore, in the patterned sample, the oxide lines screen the underlying Si signal. The surface coverage (50%) of the oxide lines is responsible for halving the Si contribution. Further, the SiO2 peak of the patterned sample exhibits a mild broadening with respect to the unpatterned sample, suggesting small contributions also from other Si chemical states (Si^{3+}, Si^{2+} , Si^{1+}). In conclusion, silicon oxides composed the nanostructures analyzed.

3.3 Nanopatterning by using *Single* and *Multiple steps* of pLOx

Under these optimized conditions I was able to fabricate oxide nanostructures as stripes which was highly reproducible with considerable quality. Reaching to this level, I got the possibility of device fabrication and surface architecture by e-SiO_2 stripes using *single step* of pLOx and Complex nanostructures by using *Multi steps* of pLOx. The scheme of the process is shown in Figure 3-5.

As it is indicate in this scheme e-SiO_2 stripes is fabricated when the process is used in a single step, (Figure 3-5a -5c) and in the other hand the ability of the sample holder give us the possibility to rotate the silicon substrate about 90°, so when the first pLOx process took place stamp is lift up by moving the micrometer screw and the sample holder is rotated 90° and again it goes in contact by approaching metalized stamp to the silicon substrate and then the second step of pLOx performs (Figure 3-3d, e), in this step a complex structure of oxide stripes as grid are fabricated.

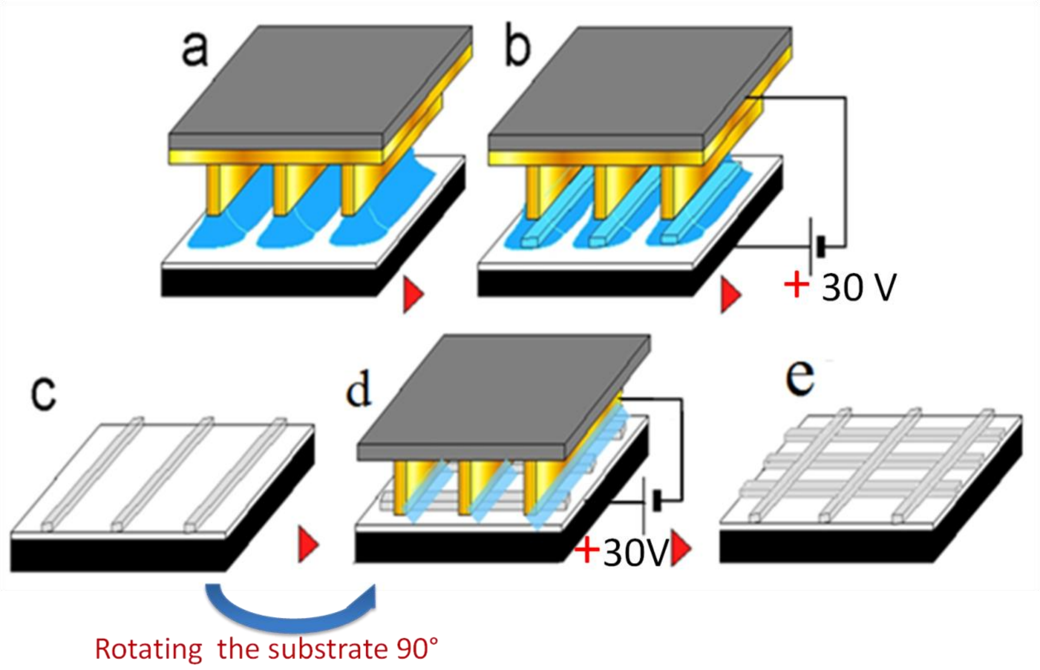

Figure 3- 5 The scheme of pLOx. (a) While two substrates are kept in contact due to capillary force between the features of the metalized stamp and Si substrate water bridge occurs. (b) Local oxidation process is performed under optimized conditions while already an electrochemical cell performed. (c) E-SiO_2 stripes grown in a single step of pLOx onto the silicon surface. (d) The patterned E-SiO_2 stripes substrate is rotated 90° and second step of pLOx by keeping the same condition performed. (e) a grid nanostructure of E-SiO_2 is fabricated.

Figure 3-6 shows AFM images of the sample which patterned e-SiO_2 stripes are produced by a *single step* of pLOx (Figure 3-4a) and a patterned e-SiO2 grid are produced by two steps of pLOx (Figure 3-3b). These nanostructures were highly reproducible with the height of 2-4 nm and the width of 200 nm in the large area of about $1cm^2$ that were the upper size of our machine.

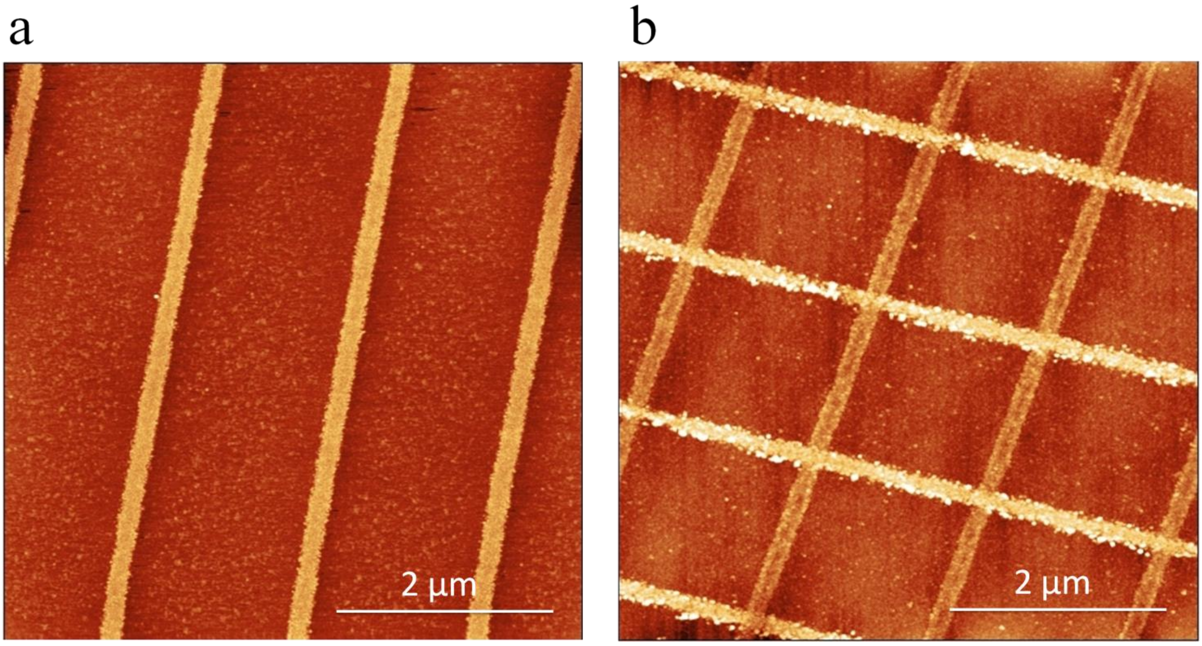

Figure 3- 6 Morphological characterization of (a) patterned e-SiO2 stripes using a single step of pLOx and (b) patterned e-SiO_2 grid using multiple steps of pLOx.

The inherent simplicity of *in-situ* fabrication combined with formation of the electrochemical cell limited to the contact area (> $1cm^2$) in our optimized set up of pLOx in DC mode, proposed us to investigate the effect of different applied bias types on the process in order to enlarge the application of local electrochemistry.

3.4 The effect of negative DC (Local electrochemical reduction- LR)

The effect of negative bias was studied by applying negative DC bias in the same optimized experimental set up. So, experimentally on a pristine silicon substrate the pLOx procedure has been performed and patterned e-SiO_2 stripes are grown, then simply by using micrometer screw the stamp was lift up and the substrate was rotated about 90 °. Then it is approached onto the substrate again and under optimized condition, negative bias is applied which calls parallel local reduction (plR). The scheme of the process is shown in the Figure 3-7.

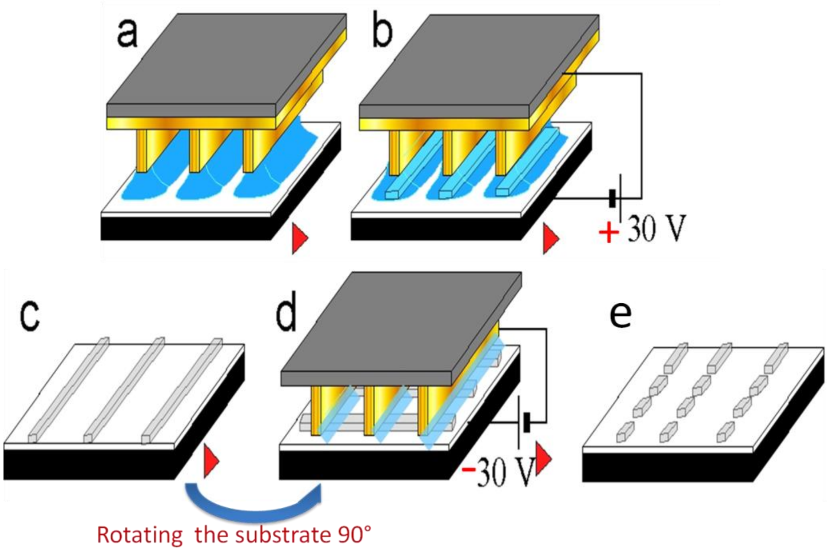

Figure 3- 7 The scheme of pLR after pLOx. (a) While two substrates are kept in contact due to capillary force between the features of the metalized stamp and Si substrate water bridge occurs. (b) Local oxidation process is performed under optimized conditions while already an electrochemical cell performed. (c) e-SiO2 stripes grown in a single step of pLOx onto the silicon surface. (d) The patterned e-SiO2 stripes substrate is rotated 90° and second step of pR by keeping the same condition performed. (e) A cross-point structure obtained

Figure 3-8a shows the morphology of the Silicon substrate after applying a negative DC bias for 60s at about 90° respect to the direction of e-SiO_2 stripes that produced by applying positive bias before. The effect of negative bias on the nanostructure of SiO_2 made by pLOx, appear as the cross-points which is reduced or removed, this effect is illustrated in the line profiles graph (figure 3-8b).

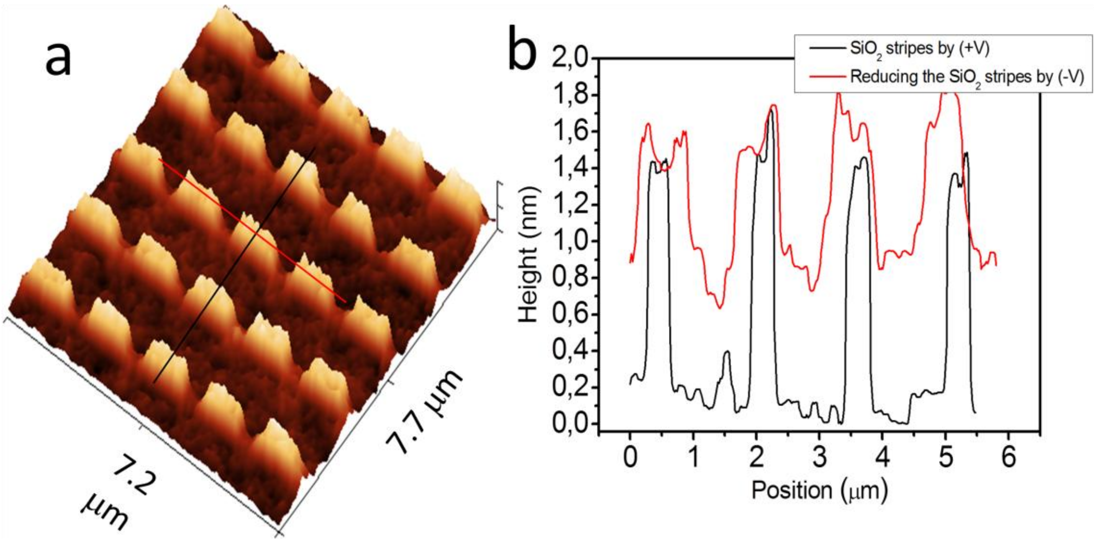

Figure 3- 8 (a) 3D AFM (Smena, NT-MDT) image of the cross-points Silicon oxide stripes obtained over a silicon sample using a PDMS stamp after applying negative DC bias (V= -30V) for 60 sec onto the sample which already applied positive DC bias for 60 sec to grow e-SiO2 before, (b) Line profiles of the AFM image (Silicon oxide stripes by applying positive bias in black solid line and reducing the stripes by applying negative bias red solid line).

Since the application of positive bias on the stripes fabricated by LOx does not alter the patterned structures nor traces of material was observed in the samples or on the stamp, we excluded that during the application of negative bias the SiO_x could be removed mechanically. Applying negative bias the possible electrochemical reduction of not fully oxidized e-SiO_x which results in a local decreasing of the height of the pre-fabricated stripes, can occurs. The reducing thickness of e-SiO_x varied almost 1 nm. It is noticed that for some cases after applying negative DC bias, the morphology of the substrate underneath of the stamp protrusion changed even by applying negative bias and some nanostructures are growth underneath of stamp protrusion, morphologically similar to structures fabricated by applying positive bias. In order to understand the chemical properties of nanostructures fabricated applying positive and negative bias, the samples were etched by HF (16%, for 10 min), which is able to dissolve SiO_2 while it does not alter the Si. Figure 3-9 (a) shows the morphology of the silicon substrate, obtained by applying first a positive bias, than rotating the stamp 90° and applying negative bias. The sample results in parallel stripes ~2nm thick obtained along the direction of “oxidation” and in parallel stripes 1nm thick obtained along the direction of “reduction”.

Figure 3-9 (c) shows the same sample after chemical etching by HF. While in correspondence of the stripes obtained by Oxidation an indentation depth of 1 nm appears as expected in pLOx [27]. The surface in correspondence of the stripes obtained by electrochemical reduction, remains almost smooth and flat as the original substrate.

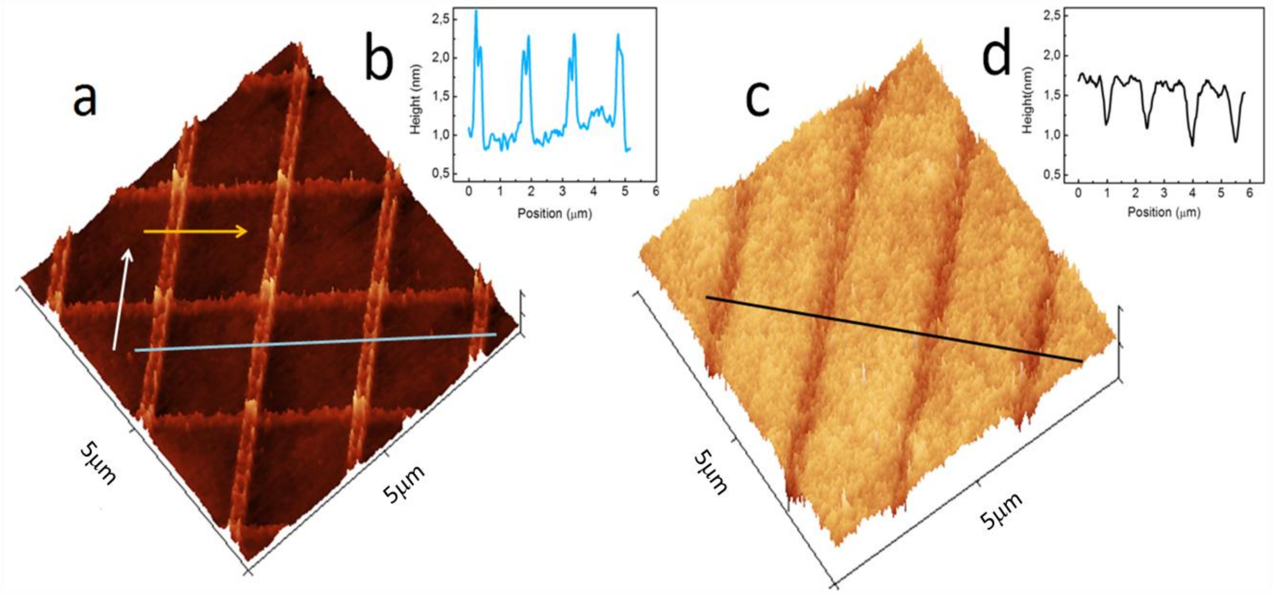

Figure 3- 9 (a) 3D AFM (Smena, NT-MDT) image of the e-SiO2 stripes obtained over a silicon substrate using a PDMS stamp after applying +30 V for 60 s in the direction of white arrow (pLOx) and -30 V for 60s in the direction of yellow arrow (pLR), (b) The line profile of AFM image in the direction of pLOx. (c) 3D AFM (Smena, NT-MDT) image of the same sample after chemical etching by HF (16%) for 10 min., (d) The line profile of AFM image in the direction of pLOx after chemical etching.

The results suggest that the chemical properties of the fabricated features are different by applying positive bias respect to the electrochemical reduction reaction where negative bias was applied. We interpreted these results as a partial electrochemical reduction to Si of the not fully oxidized native SiO_2 that is immediately transformed in SiO_2 when at the end of the process (i.e. when the sample is exposed to air)

3.5 Effect of AC bias compare to DC on the nanopatterned e-SiO_2 stripes

In view of the previous results, we demonstrate the possibility of the parallel local oxidation by using an alternative bias (AC) instead the DC bias. We show how it is possible to fabricate e-SiOx using AC bias and the increase the aspect ratio of the oxidation in the pLOx by bias modulation. The effect of the main parameters as voltage applied range in AC, applied time, and the varying frequency of the AC voltage have been systematically studied.

We performed the parallel local oxidation by AC by keeping the same set up and just switching the applied voltage from direct bias into alternative bias .

The procedure is identical to the DC case. For instance, silicon substrate is kept in contact with the metalized stamp (compact disk feature) by using a press . While they are electrically connected to a power supply, and the water bridge is formed due to humidity control atmosphere, a voltage pulses in AC mode is applied between the stamp and the substrate.

In the figure 3-10a, the parameters that define the AC waveform are illustrated. T_{ox} is oxidation time, where the total oxidation time is T_{ox} multiplied by the number of pules, and V_{ox} the applied voltage, $T^{'}$ is the rest time (V' is usually negative).

AC mode results more efficient than DC mode since the micrometric stripes of SiO_2 were fabricated applying lower bias. Figure 3-10b shows the morphology characterization of the silicon substrate after the application of 8 V DC bias versus to AC voltage and the corresponding line profile is also illustrated in Figure 3-10c. It is observed that the silicon substrate under AC conditions presents an electrochemical SiO_2 (e-SiO_2) stripes while is not formed any features under DC conditions at that bias. According to the obtained results, it confirms that the oxidation rate for AC voltage pulses is higher than DC bias. This effect has been obtained by other authors as well under AFM cantilever condition [28, 29].

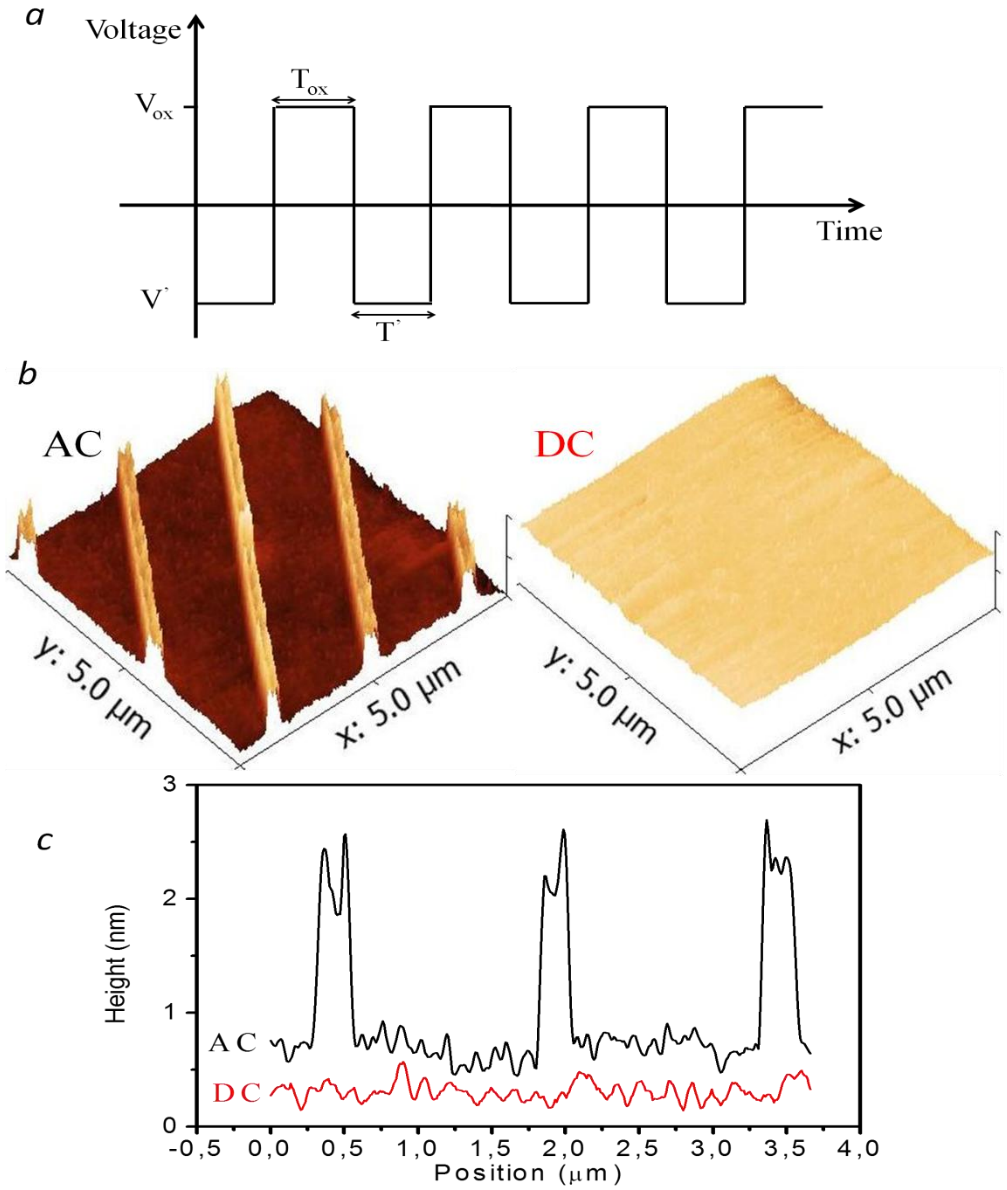

Figure 3- 10 (a) Waveform voltage applied to the surface with respect to the metal stamp when performing the pLOx under AC conditions: T_{ox} is the time when the oxidation is performed (V_{ox}, the voltage applied to oxidize the substrate which usually is between 6V and 12V), and $T^{'}$ is the rest time ($V^{'}$, the negative voltage applied), (b) 3D AFM (Smena, NT-MDT) image of the oxide lines obtained over a silicon sample using a PDMS stamp after applying 8V in AC mode ($T_{ox} = T^{'} = 10$ ms, $V_{ox} = 8$ V, $V^{'} = -8$ V) for 60 sec and after applying 8V in DC mode for 60 sec, (c) Line profiles of the AFM images.

3.5.1 Effect of voltage

pLOx in AC mode results efficient applying bias larger than 6V. We investigate the effect of varying AC voltage, from 6 V to 12 V maintaining constant time and relative humidity, we used the same stamp used in DC configuration which consist of protrusion with 200nm width and the groove of 900nm in between. Figure 3-11a shows the AFM image of the e-SiO_2 stripes obtained over a silicon substrate using a PDMS stamp, V_{ox} (+8 V) and V' (-8V) at 50Hz, for 60 s and figure 3-11b corresponded line profile.

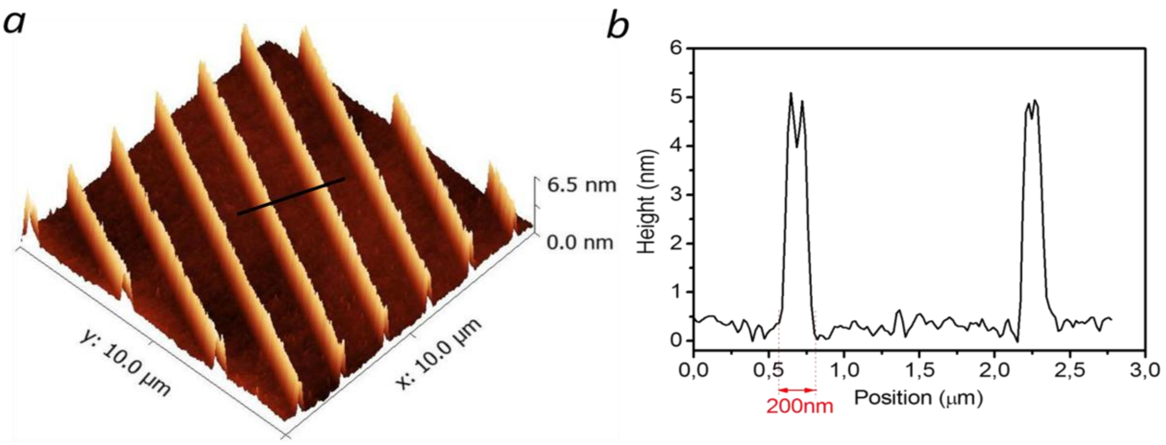

Figure 3- 11 (a) 3D AFM image of the e-SiO_2 stripes obtained over a silicon substrate using a PDMS stamp after applying V_{ox}= +8 V and V' = -8V at 50Hz, for 60 s. (b) The line profile of AFM image.

The oxide lines height has been measured statistically by the height distribution graph (figure 3-12a), in which the difference between the positions of the peaks is the height of the oxide lines. Figure 3-12b shows that the height of growth SiO_x nanostructures in the range of 6- 8 V increases from 1 to ~3.5 nm with growth factor of 0.93 /%, which simply extracted as a slope of the linear fit, y= Ax+ B; A= 0.93, B= - 4.61, and then from 8.5 V to 12 V it reaches to an almost saturation level of ~2 nm which is little be lower than e-SiO_x fabricated at lower bias. The study of aging effect shows that the e-SiO_x fabricated at bias larger than 8 V is stable and not sign of collapse was observed also one year from its fabrication. We explain this behavior as a stabilization of the e-SiO_x, which already occurs during the process.

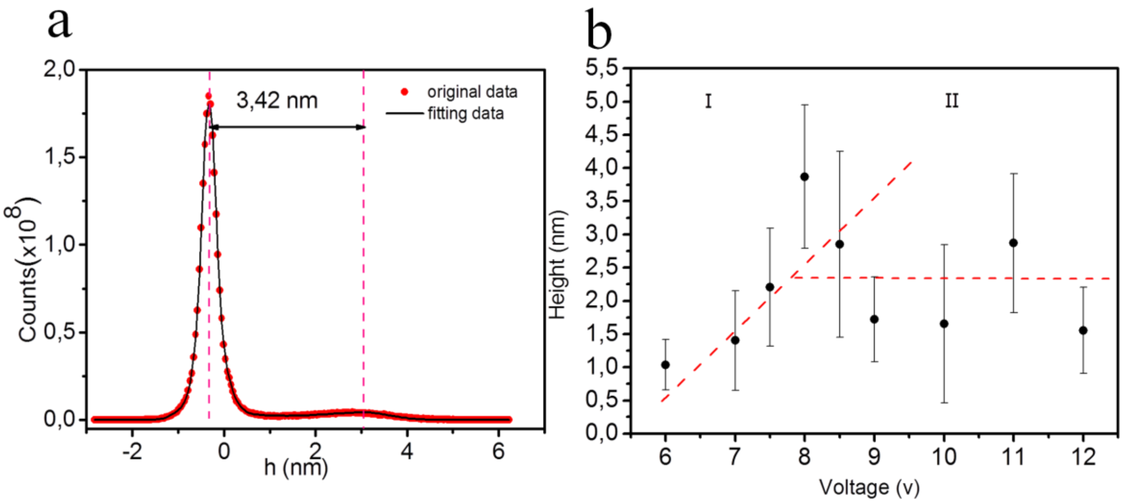

Figure 3- 12 (a) Height distribution graph of the topographic image (analysis done using the open source SPM software Gwyddion-www.gwyddion.net). The difference between the two peaks is the height of the oxide lines (~3 nm). (b)Height of the oxide lines with respect to the relative applied bias. In the range 6 ≤ V ≤ 8 the height increases from 1 to ~3.5 nm with growth factor 0.93/% (slope of the linear fit). In the range 8.5 ≤V ≤ 12, the height of the oxide lines is fixed at ≈2 nm. The error bars of the measurements are overestimated using the FWHM of the height distribution graphs.

3.5.2 Effect of time

The effect of different applied time in AC bias from 30s to 600s under constant AC bias of 8 V at 50Hz and relative humidity has been studied. Figure 3-13 shows the effect of time on the height of the e-SiO_2 stripes, which is extracted by height distribution of the AFM images using the open source SPM software Gwyddion-www.gwyddion.net. It is observed that the height of the e-SiO_2 by increasing the time from 30s to 160s increases from 1.5 to ~ 4.4 nm with the average value of ≈ 3nm), after that by increasing the time up to 600s, the height of the oxide lines is almost constant at ≈ 2.5 nm which obviously the process is reached to a saturation regime. As in the case of the effect of bias voltage We attribute the effect of collapsing of oxide structures during the process (viz. after 200s), this interpretation is confirmed by the observation of the fact that not change of stripes thickness was observed after one year in the sample prepare in times longer than 200s.

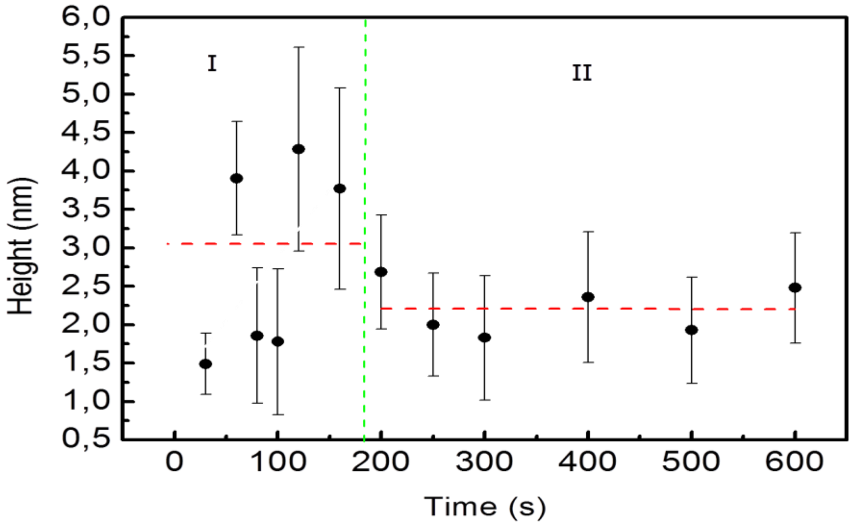

Figure 3- 13 Height of the stripes versus varying applied time, total T, from 30 s up to 600 s, at 8V, f = 50Hz, RH = 90%. b) (Height distribution graph of the topographic image (analysis done using the open source SPM software Gwyddion-www.gwyddion.net)). In the range $30 \leq t \leq 160$ s the height increases from 1.5 to ~ 4.5 nm with the average of ≈3nm and in the range $200 \leq t \leq 600$ s, the height of the oxide lines is fixed at ≈2.5 nm. The error bars of the measurements are overestimated using the FWHM of the height distribution graphs.

3.5.3 Raman characterization

The fresh patterned oxide nanostructures were studied by Raman scattering measurement to investigate the integrity of fabricated nanostructures by AC bias.

Figure 3-14a shows The Raman spectrum obtained under 15 mW at 532 nm laser 10 sec exposure time, 0.7 NA 100x 1800 lines/m showing clearly the peak of Silicon oxide at 522 cm^{-1} and often a quite high intensity peak at 475 cm^{-1} which might be corresponded to the silicon Nanoribbons [30], while in sample prepared by DC mode only the typical intense peak of bulk silicon at 522 cm^{-1} (figure 3-14b) is observed.

To support this interpretation a detailed study is reported in chapter 4 were the electrical properties of e-SiOx were investigated directly in resistive switching devices.

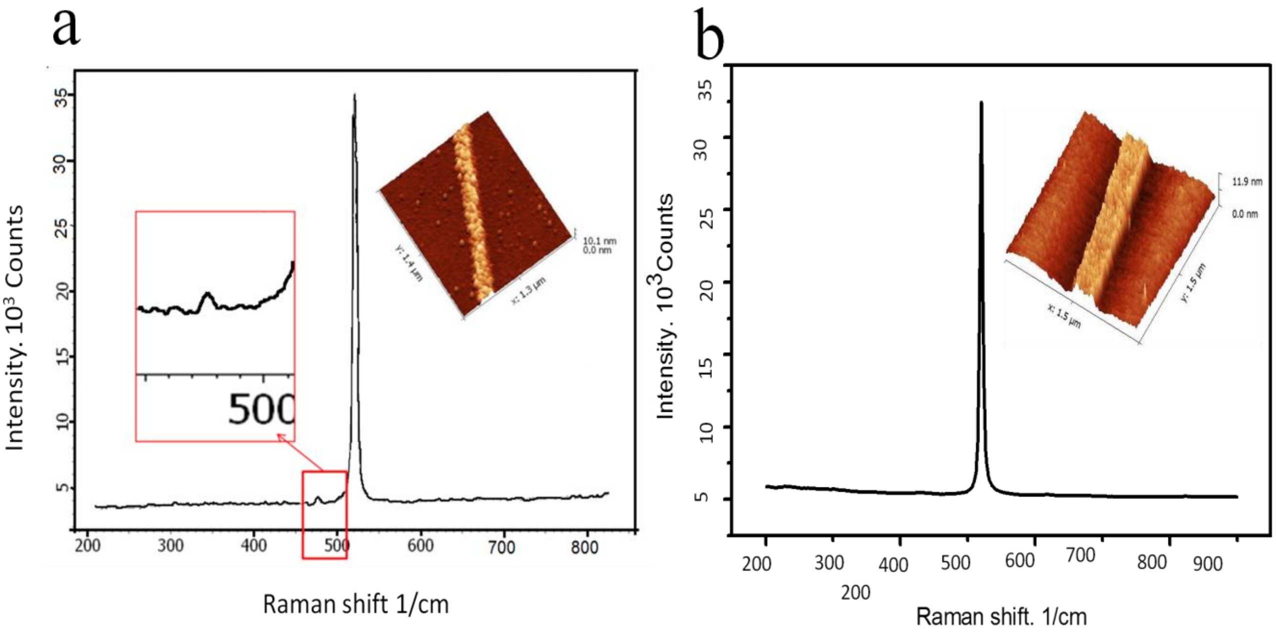

Figure 3- 14 (a) The Raman spectra of corresponded area with e-SiO$_2$ stripes made by AC bias shows a peak at 522 cm^{-1} corresponding to SiO$_2$ structure and also an almost high intensity peak at 475 cm^{-1}which can correspond to Silicon nanoribbons (inset is the corresponded AFM in 3D). (b) The Raman spectra of corresponded area with e-SiO$_2$ stripes made by DC bias shows a peak at 522 cm^{-1} corresponding to SiO2 structure (inset is the corresponded AFM in 3D).

3.6 Conclusion

In conclusion in this chapter we demonstrated parallel local oxidation (pLOx) soft-lithography as a friendly and additive procedure to fabricate different type of nanostructure at the technology of silicon. The effective parameters on the procedure have been systematically studied and the optimized conditions obtained for nanaopatterning of silicon. We observed that by applying AC bias the rate of oxidation process is higher than DC bias. Furthermore we observed that applying negative bias the nanostructures fabricated by pLOx can partially reduced or removed. Moreover, Raman scattering measurements confirmed that local oxidation of silicon in AC mode can grow in-*situ* silicon filament formation which is one of the main issue in resistive switch device fabrication. The highly reproducibility with excellent quality combined with inherent simplicity of this procedure gave us the possibility of surface architecture in the fabrication of electronic devices as resistive switch nanojunction which will present in the **chapter 4** and **chapter 5**. Moreover this technique is used to study the bio-molecules by selectively positioning and confinement of molecules as DNA (**Chapter 6**).

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Chapter 4

Memory resistive properties of Si/e-SiO_2/ Metal Nanojunction

This chapter describes the applications of pLOx procedure in device fabrication by using silicon native as a substrate and metalized PDMS soft stamp as an electrode.

4.1 Introduction

Metal-insulator-Metal (MIM) junction is very important for many applications in electronics, however due to intrinsic porosity of SiO_2 fabricated by anodic oxidation the use of e-SiOx is not usable for traditional application in nano/micro electronic. In recent years the use of MIM junction in the so called “memristors” been proposed. In principle e-SiOx has ideal characteristic for this kind of application.

Memristor theory was formulated and named by Chua L. [1] in his seminal paper on the memristor's concept and its connection to the nonlinear circuit theory [2]. Chua (1971) predicted that there is a solid-state device, which defines the missing relationship between four basic variables. In the 1960s, Simmons [3] published the very first report on the Metal-insulator-Metal (MIM) I-V curve, illustrating the hysteresis effect associated with a MIM structure, that characterized tunneling current behavior. In 2008, almost forty years later, a team at HP Labs announced the development of a switching memristor based on a thin-film of TiO_2[4]. The rational for choosing the name 'memristor' is the same as the memristor, a resistor with memory, and also resistive switch devices. The memristor, *memory-resistor*, is a two-terminal nano-device that can be made as thin as a single-atom-thick insulator layer or semiconductor between two electrodes and has become of tremendous interest for its potential to revolutions electronics, computing, computer architectures, and neuromorphic engineering. It is a relatively unexplored device in terms of modeling, applications, design methodologies, and underlying physics of its switching mechanism(s) between two or more stable state is yet to be understood. Resistance switching memories, which is the main device which will be described in this chapter, can be classified as memristor-based memories [5]. It has a capacitor-like structure composed of insulating or semiconducting materials sandwiched between two electrodes (Figure. 4a). Its function is fairly simple. Two values, Turn "OFF" and Turn "ON", are assigned to its Low Resistance State (LRS) and High Resistance State (HRS), respectively. The resistance is changed by applying a voltage across the device (Figure. 4b). Because of its simple structure, highly scalable cross-point and multilevel stacking memory structures have been proposed [6]. In the resistive switching phenomenon, a large change in resistance (>1000%) occurs on applying pulsed voltages, and the resistance of the cell can be set to a desired values by applying the appropriate voltage pulse [7]. A recent study has shown that the switching speed can be faster than several nanoseconds [8].

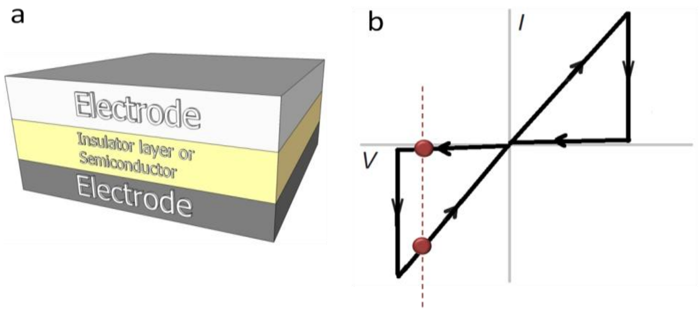

Figure 4- 1- (a) Schematic configuration of a resistive switch memories, (b) The ideal I-V cure which indicate the Low Resistance State (LRS) and High Resistance State (HRS) in a single bias.

Among the materials that exhibit a resistive switching phenomenon, oxide materials have been studied intensively. In 1962, Hickmott [9] first reported hysteretic current–voltage (I–V) characteristics in metal insulator- metal (MIM) structures of Al/Al_2O_3/Al, indicating that resistive switching occurs as a result of applied electric fields. Resistive switching has subsequently been reported in a wide variety of MIM structures composed of binary metal oxides, such as SiO_x [10,11] and NiO_x [12].

The resistive switching phenomenon has been observed in a wide variety of transition metal oxides, such as PCMO [13], Cr-doped $SrZrO_3$ [14], $SrTiO_3$ [15], NiO_2 [43], TiO_2 [16], and Cu_2O [17], and also SiO_x [18]. However, the observed switching behavior seems to differ depending on the material. On the basis of I–V characteristics, the switching behaviors can be classified into two types: *unipolar* (nonpolar) and *bipolar*, for which typical I–V curves are shown in Figures 4-2a and 4-2b, respectively.

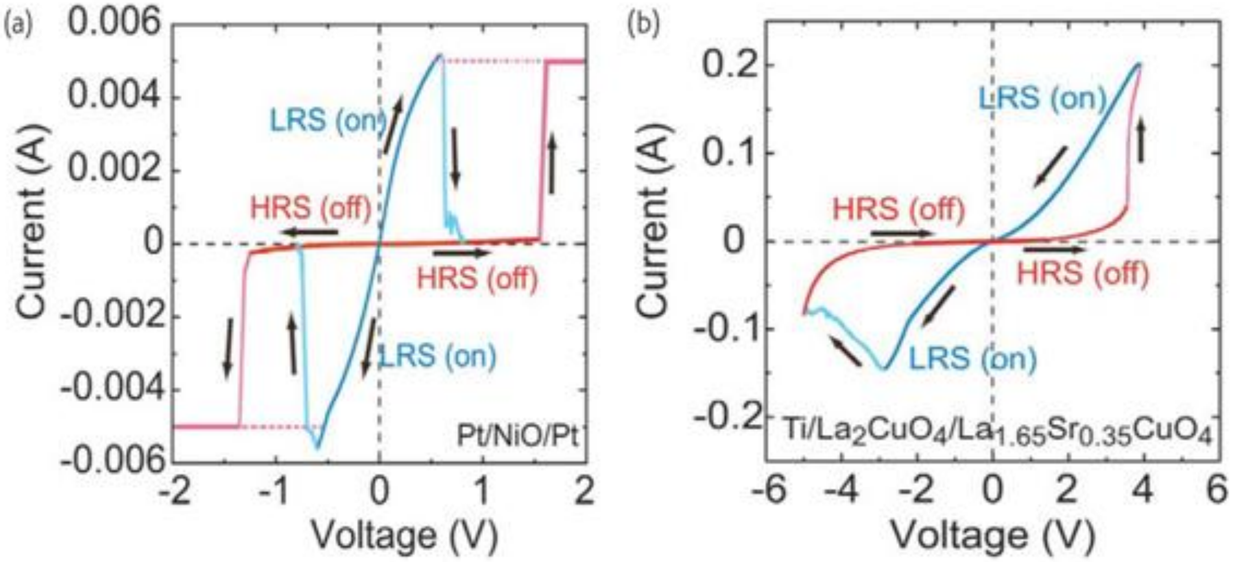

Figure 4- 2- I-V curves for (a) *unipolar* (nonpolar) switching in a Pt/NiO/Pt cell and (b) *bipolar* switching in a Ti/La_2CuO_4/La1.65Sr0.35CuO_4 cell. In unipolar switching, the switching direction depends on the amplitude of the applied voltage. Bipolar switching shows directional resistance switching according to the polarity of the applied voltage.

In unipolar resistive switching, the switching direction depends on the amplitude of the applied voltage but not on the polarity. An as-prepared memory cell is in a highly resistive state and is put into a low-resistance state (LRS) by applying a high voltage stress. This is called the ‘forming process’. After the forming process, the cell in a LRS is switched to a high-resistance state (HRS) by applying a threshold voltage (‘reset process or OFF state’). Switching from a HRS to a LRS (‘set process or ON state’) is achieved by applying a threshold voltage that is larger than the reset voltage. In the set process, the current is limited by the current compliance of the control system or, more practically, by adding a series resistor. In the other word in unipolar switch, two different threshold exist, hence, there is a need to exceed those threshold to force the device to switch from one state to another. This type of switching behavior has been observed in many highly insulating oxides, such as binary metal oxides [19].

Bipolar resistive switching shows directional resistive switching depending on the polarity of the applied voltage (Figure 4-2b). So in a bipolar switch, a negative voltage should be applied across the device to force the device switch back. This type of resistive switching behavior occurs with many semiconducting oxides, such as complex perovskite oxides [20].

In addition to classification in terms of switching behavior, the type of conducting path is also used to categorize the resistive switching. One class shows a filamentary conducting path, in which the resistive switching originates from the formation and rupture of conductive filaments in an insulating matrix (Figure 4-3a). This can be associated with both unipolar and bipolar switching behavior.

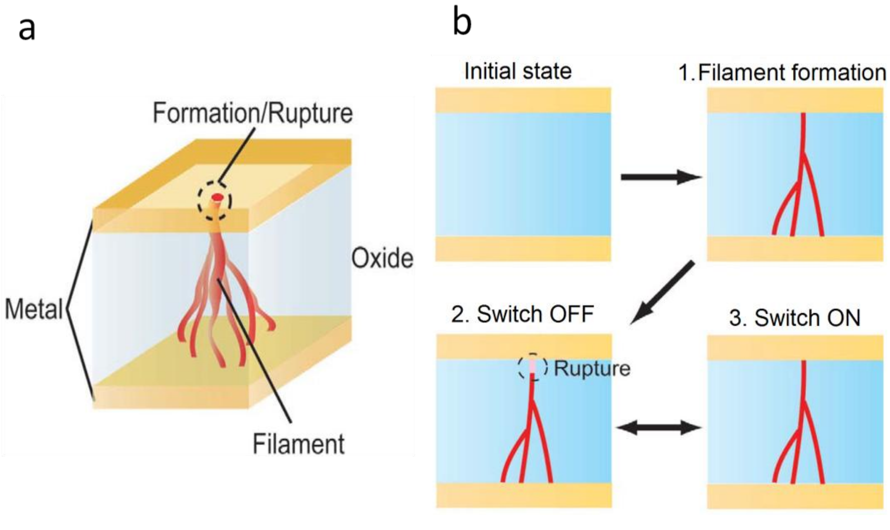

Figure 4- 3 (a) Proposed models for resistive switching based on the formation of filamentary conducting path (b) Schematics of the initial state (as-prepared sample) and (1) filament formation, (2) switch OFF (reseat), and (3) Switch ON (set) processes for a unipolar resistive switch.

Figure 4-3b shows a possible driving mechanism for filament formation-type resistive switching that shows unipolar switching behavior which was observed in a polycrystalline CuO film between Pt electrodes during the forming process, after which the cell switches into a LRS. They have also shown that the cell resistance returns almost to the original value when a part of the filament-like structure is cut with a focused ion beam, indicating that the filamentlike structure is the conducting path in the cell [21]. In the filament formation process (1), filamentary conducting paths form as a soft breakdown in the dielectric material. Rupture of the filaments takes place during the switching OFF (reset) (2) process, and filament formation during the switching ON (set) process (3). Thermal redox and/or anodization near the interface between the metal electrode and the oxide is widely considered to be the mechanism behind the formation and rupture of the filaments [22,23]. In contrast, in bipolar-type switching, electrochemical migration of oxygen ions is regarded as the driving mechanism [24] .Clear visualization of the conducting filaments in insulating oxides has not been achieved.
Although there are several suggested mechanisms for the resistive switch devices but still the mechanism of this type of devices are not well-known and it is an open problem to be studied.

Here, we propose an original system based on nano-memristors that offers several crucial technological and scientific breakthroughs compared to conventional devices: i) the possibility to regenerate or repair the junction upon the application of an appropriate voltage cycle; ii) the spatially controlled patterning of the insulating layer, which is fabricated in situ, preventing the problems of cross-talk through the thin film; iii) the usage of removable top electrodes, which allow the unique possibility to expose the two sides of the metal/thin film interface after switching for subsequent investigation.

4.2 The fabrication of Si/ SiO_2/ Metal junction

We demonstrated our approach on a Si/ SiO_2/ Metal junction where the SiO_2 is fabricated *in-situ* by parallel local oxidation lithography (pLOx), as described in the previous chapters in details ;[25,26,27] these materials are commonly used in silicon-based technology. SiO2 is normally used as an insulating layer. However, it is known that defective SiO_x thin films ($x < 2$) [28], in which some structural defects are induced by a locally high electrical field, up to the stage of breakdown, can exhibit memory effects [29]. Intrinsic resistive switching in SiO_2 was observed in several (non) Metal/ SiO_2/ (non)Metal systems both using thermal and native oxide [42,30,31]; all these systems have excellent switching speeds and durability. Despite the poor electric properties of electrochemically-fabricated SiO_x (e-SiO_x) thin films for conventional applications in micro-(nano) electronics, e-SiO_x has appealing characteristics for (Ref. 42,43). e-SiO_x is more porous than the thermal oxide (this can help metal filament formation), it contains a high density of defects and charges trapped in it [32], and it grows in conformity to the electrodes [33]. A schematic drawing of our system is depicted in Figure 4-4, which at the end of our procedure a layer of electrochemical SiO_2 (e-SiO_2) is sandwich between metalized stamp and doped silicon.

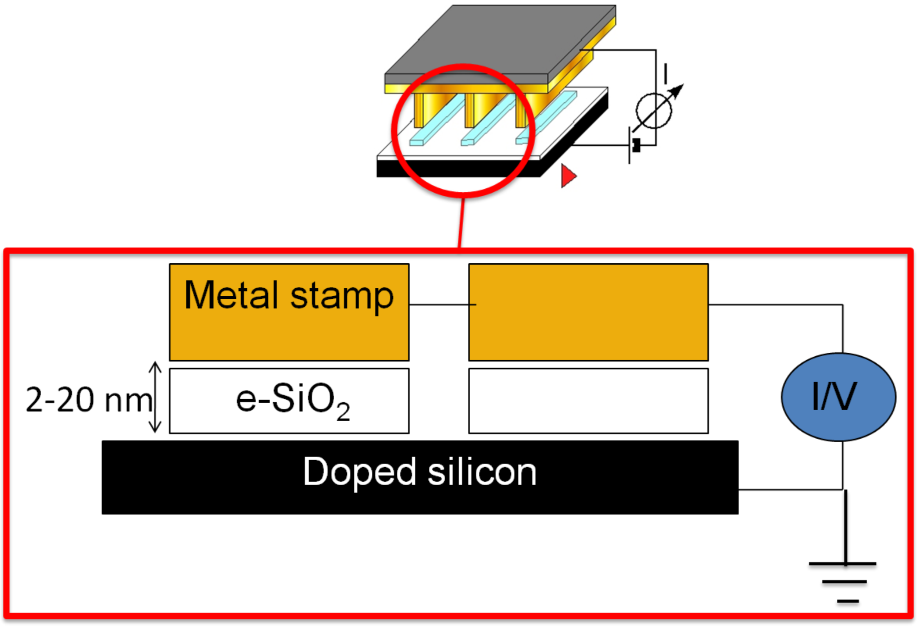

Figure 4- 4 Schematic drawing of the system. The nano-electrochemical cell was formed in an environment rich in water vapor (RH>80%) by placing a stamp in contact with a Si surface. B) The Si is oxidized by applying to it a positive bias. It growth in conformity with the stamp protrusions. C) Parallel nanostripes of electrochemical SiO_2 (SiO_x) were formed. D) A cross-bar like device is fabricated by rotating the stamp by 90°. The inset shows the detail of the Metal/e-SiO_2/Si junction.

The main device fabrication step is based on pLOx procedure where a metalized stamp is placed in contact with the doped Si surface in a high-humidity environment. By applying a bias voltage the sample surface is oxidized, forming an oxide film that perfectly adapts to the stamp features [47]. The process takes place only underneath of the stamp protrusions to fabricate the SiO_2 nanostructures during the process [34] The cross-bar-like configuration could also obtain by rotating the stamp 90° after the oxidative process (see chapter 3). Typically, we are able to fabricate the e-SiO_2 stripes with a width of 200 nm and a thickness of 2-10 nm. By the end of pattering procedure of pLOx, simply by moving the patterning stage out from the humidity chamber control, an array of nano-junctions $200 \times 200 \times 10$ nm^3 are obtained.

4.3 Electrical characterization

The electrical characterization of the fabricated junction is proposed to investigate its properties. So the electrical behavior of the Si/ e-SiO_2/ Metal nano-junctions is studied by following the I/V curve. The I–V curve of the device shows a diode-like rectifying behavior (Figure 4-5a) [35], and after a forming step [36], which consists in the application of a large negative bias (usually <–10 V), the I–V curve exhibits a large hysteresis and a sharp resistive switch at a negative bias (Figure 4-5b) [49]. Our device behaves as a bipolar memristor, forasmuch as it is clear from different resistance state for each single bias, viz. it can switch ON (i.e., switched in the low-resistance state) only by applying a negative bias and can be switched OFF (i.e., switched in the high-resistance state) only by applying a positive bias.

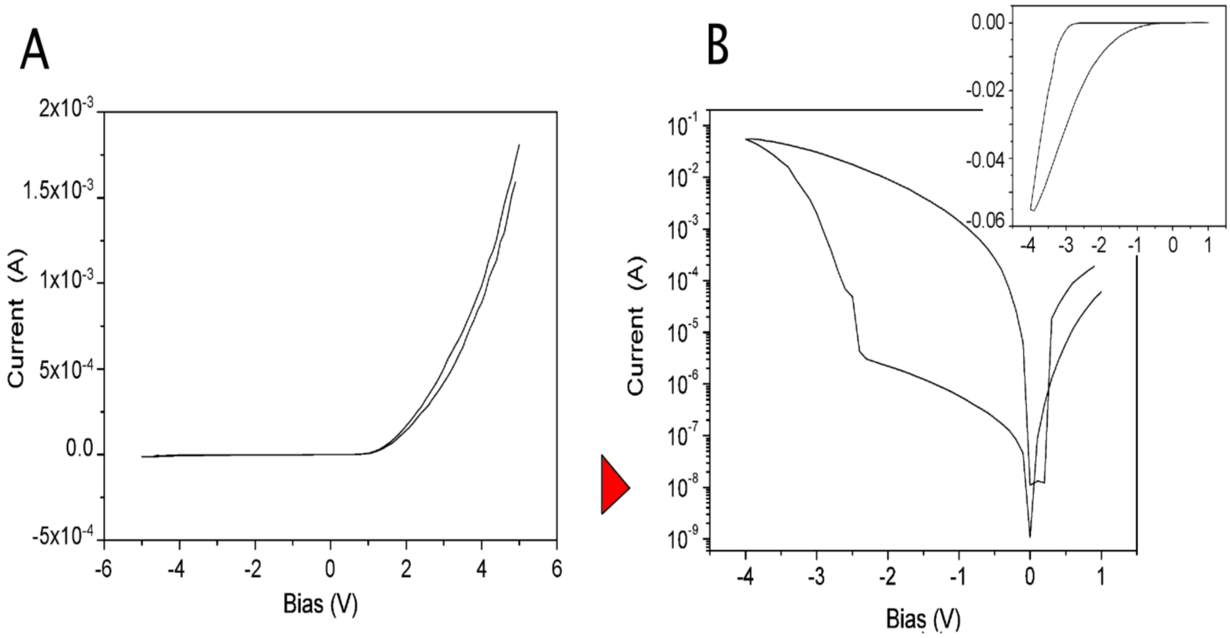

Figure 4- 5 Electrical characterization of e-SiO_2 pattern, before and after the forming step. A) I–V curve of Si/SiO2/Al device fabricated by local oxidation. B) Hysteretic I–V curve after the forming step (semi-logarithmic scale). The inset shows the same curve in linear scale.

The nonvolatile character of our devices were tested by measuring the current at the reading bias in the low-resistance state. The device was kept in a short-circuit state between the reading measurements. **Figure 4-6** shows the scheme of the program applied for resistive switching characterization. In this case a cycling bias program of writing, reading and erasing is applied to the device and the output current as a corresponded signal is recorded to monitor its memory characteristic.

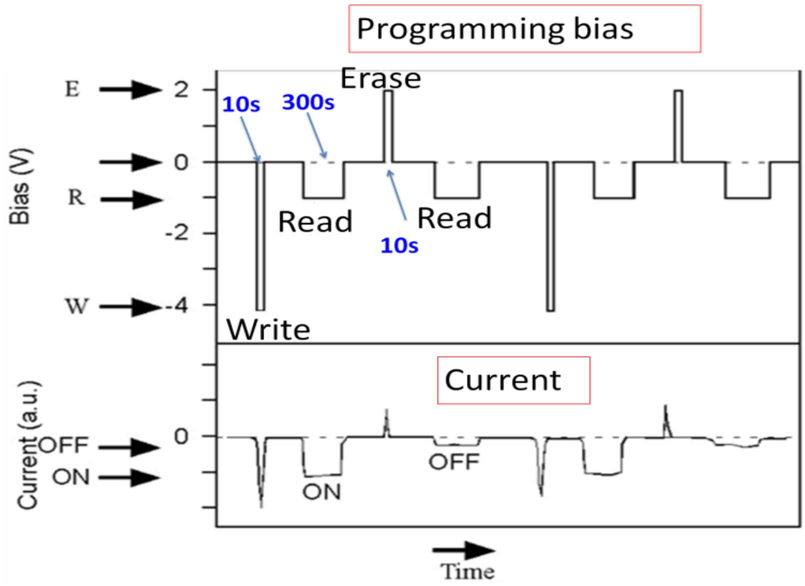

Figure 4- 6 Scheme of memory characterization program. The cycling program by using a potential of –4 V for 10s pulses to switch the device ON (writing bias), a potential of -1V for 300s to monitor the output current (reading bias), and a potential of +2V for 10s pulses to switch it OFF (erasing bias)

To elucidate the memory properties of our device, **Figure 4-7a** shows its resistance measured by using a potential of -1 V for 300s after each one of a series of –4 V for 10s pulses to switch the device ON and +2 V for 10s pulses to switch it OFF; we observed a retention time of at least one day.

The endurance tests of the memory devices were conducted by cycling the voltage between 1 to –3 V. For optimized devices with a low programming voltage bias (>-4 V during the write process), we observed an excellent stability over more than 10^5 cycles without any sign of degradation in the devices. The current of the ON-state tends to decrease by ~10% in the first 100 cycles, after which it remains stable over more than 10^5 cycles. The inset in Figure 4-7a demonstrates the stability and the high degree of repeatability of the I–V curve after more than 10^5 cycles.

The endurance is generally less robust (i.e. hysteresis curve becomes unstable) in the samples where the programming bias is <–4 V (about 40% samples, if prepared under non-optimized conditions, exhibited rapid degradation of the hysteresis curve).

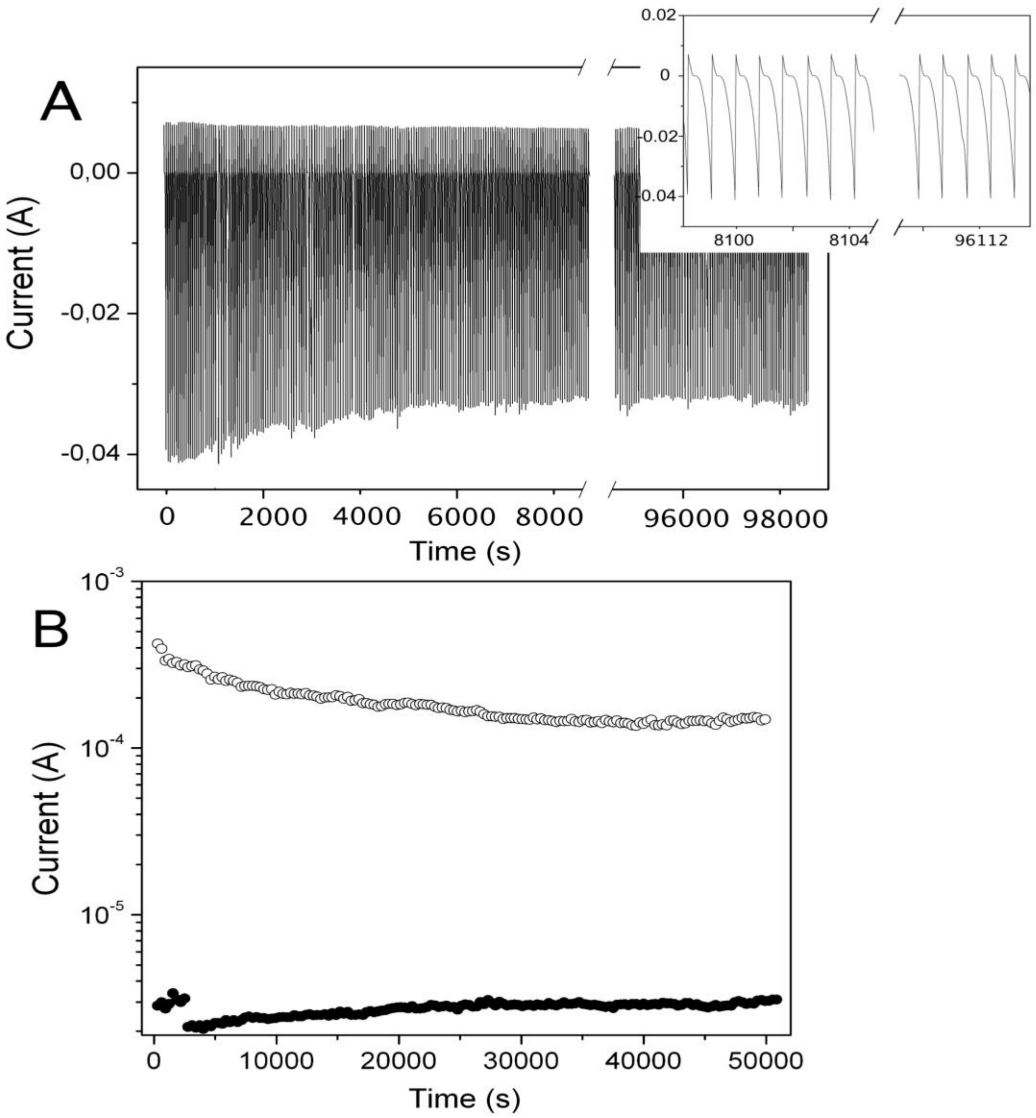

Figure 4- 7 Memory and endurance characterization. A) Endurance tests. Demonstration of I–V cycle reproducibility after ~10^5 cycles. The inset shows a few cycles in detail. B) Memory properties tested by using a potential of -0.2 V after a pulse of –4 V to switch ON the device and +4 V to switch OFF.

Since the configuration of our memristor is the same used for the fabrication of the e-SiO_2 nanostructures, the system offers the possibility to be regenerated without the need to disassemble the device. **Figure 4-8** shows an example of a device-regeneration of a device exhibiting fast degradation. The black curve shows the first I–V characteristic after the forming step, while the blue curve shows the I–V characteristic after 1000 cycles. Here the device is regenerated by the application of a positive voltage higher than +15 V for 500 ms, which establishes again the condition for Si oxidation [37, 38]. After the application of the regenerative voltage, the device is almost completely regenerated to the original state (Figure 4-8, red curve).

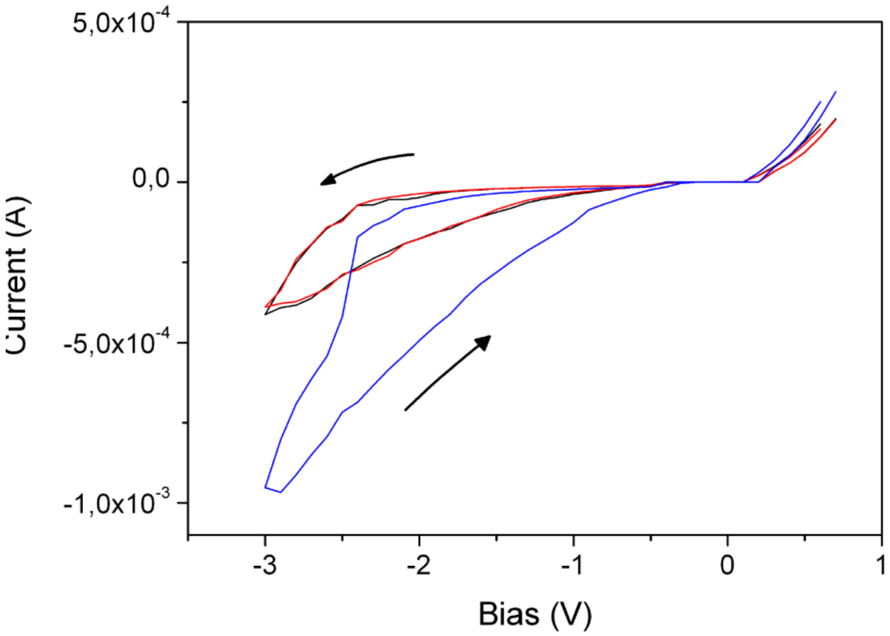

Figure 4- 8 Device regeneration. This non-optimized device exhibits a small hysteresis (black curve), which rapidly degrades after a few cycles (blue curve), here after 1000 cycles. The device can easily be restored by applying a +15 V bias, which re-oxidizes the semi-permanent silicon filaments (red curve).

In order to exclude possible artifact due to particular configuration the proposed we tested behavior of our system the Si/SiO_2 (Native) /Metal (figure 4-9a) confirming the results of similar system in literature by S. M. Sze, it is observed a clear hysteresis for poly Si/ SiO_2 (native)/ poly Si junction (figure 4-9b) [49].

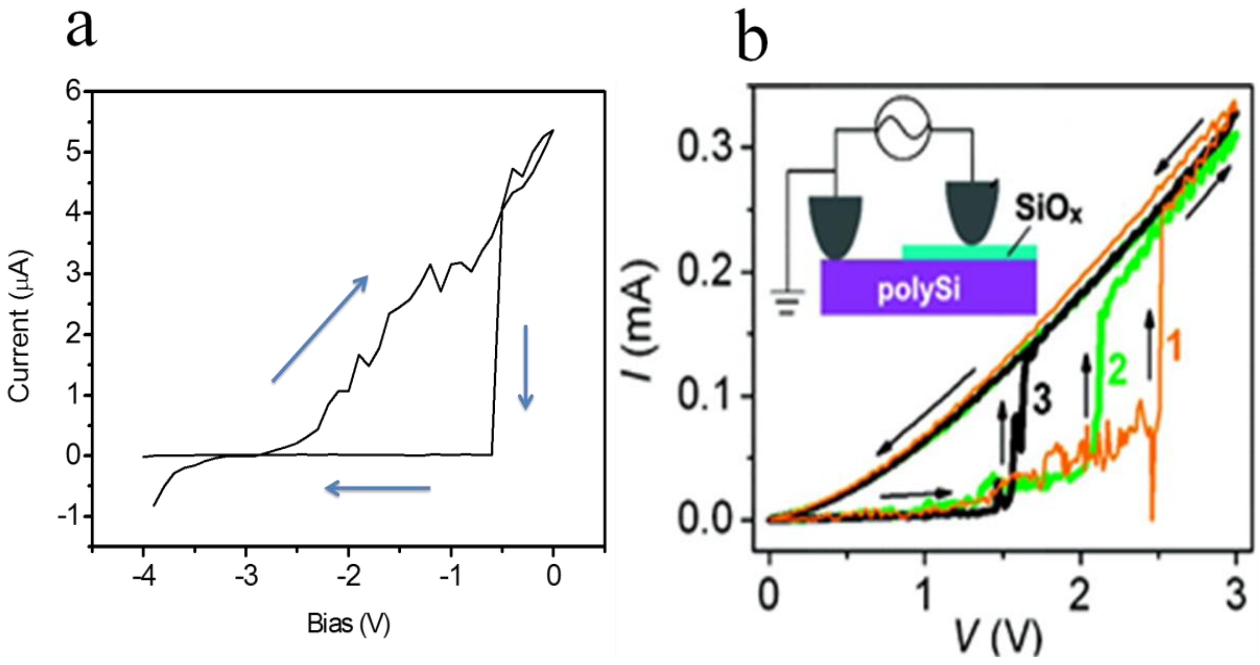

Figure 4- 9 (a) I-V curve of Si/SiO_2/Metal devices fabricated using native SiO_2 keeping our set up (b) I-V curve of Poly Si/SiOx (native) / Poly Si .

Figure 4-10 shows the thermal stability of this nano-junction which was studied by heating up the device at 200 ^{oC} for 10 min. The Comparison between the I/V curve characterization before and after thermal annealing did not show any relevant effect and it confirms the stability of this resistive switch device.

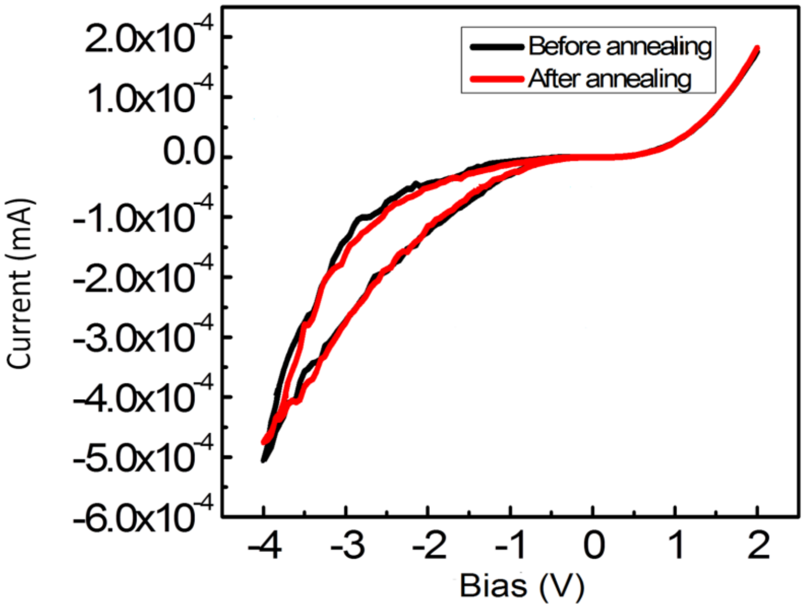

Figure 4- 10 Device thermal stability.This device exhibits almost stable hysteresis (red curve) after thermal annealing at 200 °C for 10 min , which had no relevant difference with the original hysteresis (black curve).

4.4 Morphology characterization

The proposed configuration offers a unique possibility to investigate the interface after operation by simply removing the top electrode that coincides with the stamp.

The silicon substrate before and after electrical stress was studied morphologically by AFM and SEM. Figure 4-11a and 4-11b show the morphological characterization of the e-SiO_2 stripes before and after applying 10 write/ erase cycles (here without rotating the stamp). Scanning electron microscopy (Figure 4-11b) and Atomic force microscopy (Figure 4-11d) show the formation of some outgrowths. No traces of metal contaminants were observed in printed structures by scanning electron microscopy microanalysis, nor by X-Ray photon electron spectroscopy performed by syncrotron radiation (sensitivity <1%) which can confirm that the formation of these outgrowths are related to the process of our device.

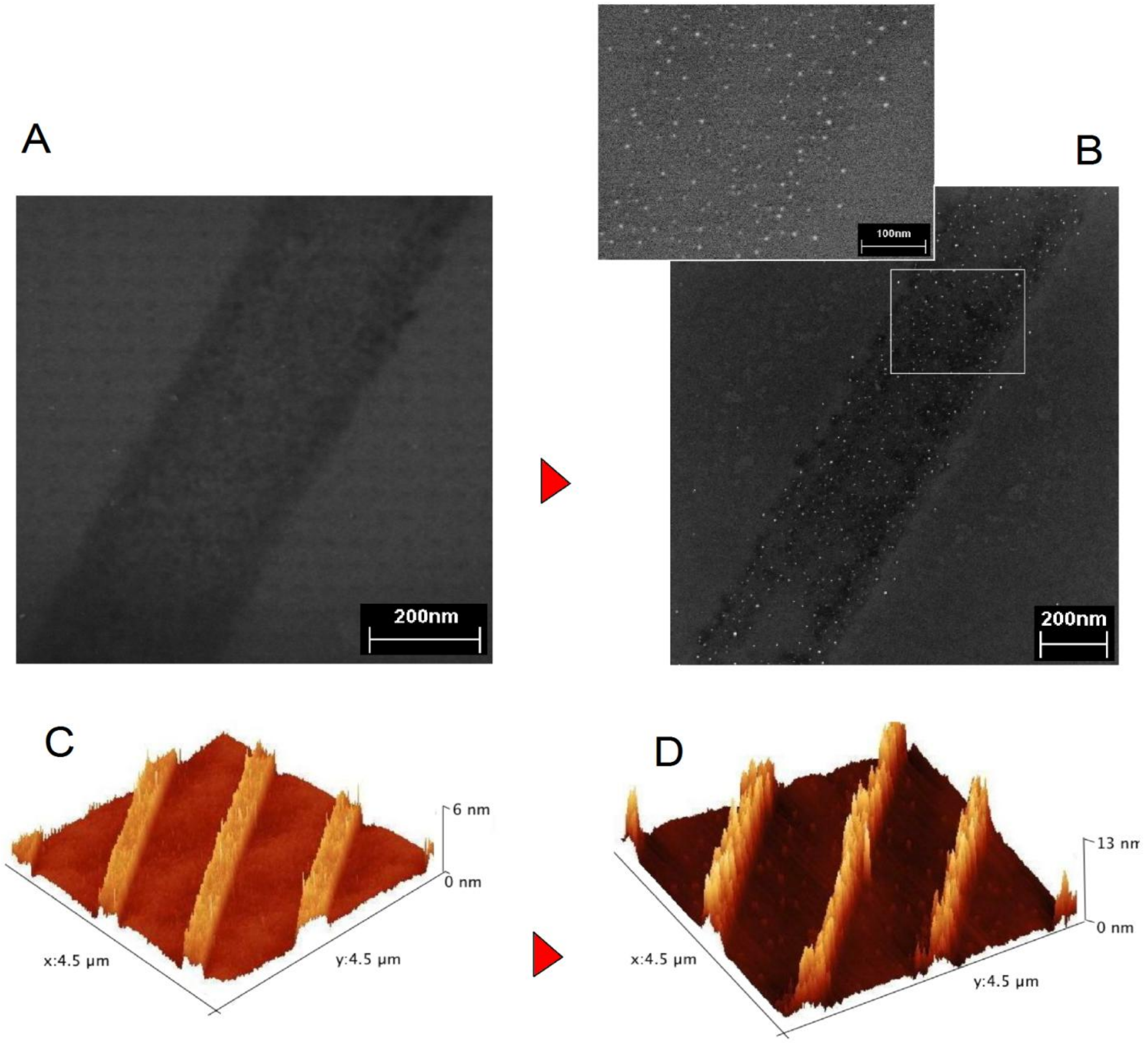

Figure 4- 11 Morphological characterization of e-SiOx pattern, before and after the resistive switching. A) SEM image of e-SiO_2 stripes as prepared; B) InLens Secondary Electrons SEM image after the application of 10 write/erase cycles without stamp rotation. The inset shows a detail of the same sample region, observed with the Everhart-Thornley detectors, therefore reducing the contribution of the surface morphology to enhance the presence of the outgrowths. The image shows the clear formation of outgrowths smaller than 7 nm in width. D) Corresponding AFM image of A. D) Corresponding AFM image of B.

Moreover, the Morphological and Electrical evolution in cross-bar configuration has been studied . **Figure 4-12** shows the AFM morphology of e-SiO_x surface before and after applying 100 write/erase cycles in cross-bar configuration. In correspondence of the cross-point the local roughness increases from 1.9 nm to 3.1 nm and some outgrowths clearly appear. We identify the outgrowths as evidence of the filament formation. The effect of cross-bar-like configuration (i.e. stamp rotation) in I/V curve showed the absolute value decrease of about 80% corresponding to the effective area of the electrodes due to rotating the metal stamp.

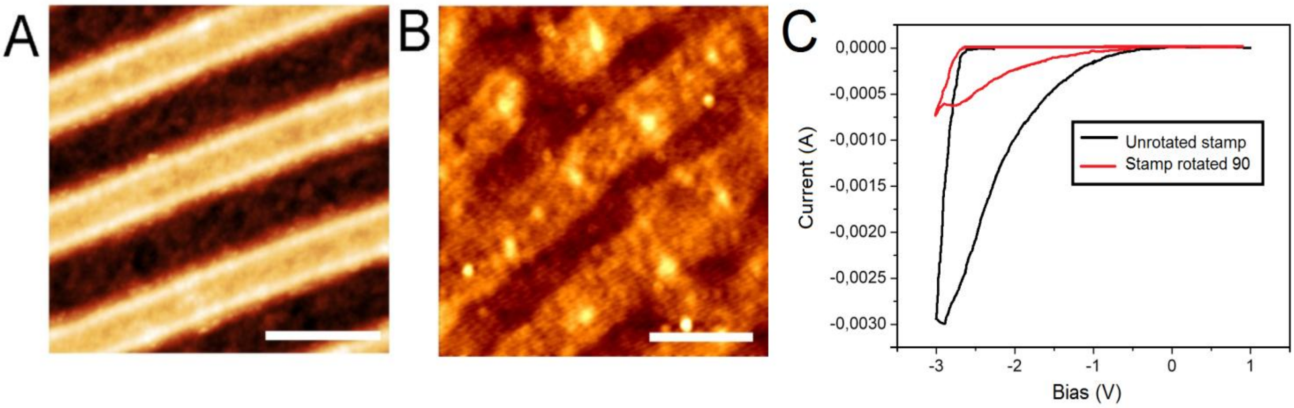

Figure 4- 12 Morphological and electrical evolution in cross-bar configuration, AFM morphology of e-SiO_2 surface (A) before and (B) after applying 100 cycles. The image shows a local increase of the roughness due to the Si filament formation (Z scale 0-8 nm), the scale bar of AFM images is 2μm. (C) Current reduction associated to the stamp rotation, the hysteresis after decreasing of about 80% corresponding to the effective area of the electrodes by rotating the metal stamp about 90 ° (red curve) in comparison of the totally 100% effective area (black curve).

4.5 Proposed Mechanism

The results and the peculiar architecture gives access to important information about the fabricated Si/ e-SiO_2/ Metal nano-junction and more investigation about the details of the switching mechanism. Compared with carrier trapping memory devices and metallic filament based devices, which show no polarity dependence and a crucial dependence on the electrode material respectively, our devices show a polarity dependence but are not influenced by the material of the top metal electrode (we tested Al, Au and Ag). Significantly, the hysteresis cycle remained unaltered, even when $AgNO_3$ or other dopant salts were embedded in the e-SiO_2 during the fabrication process [39] In addition, by applying the writing bias in non-optimized or electrically stressed samples, the current increases until it reaches a saturation value after 1000 seconds (~30% of the initial value in the first 2000 ms and a further ~2% within 10^3 s. **Figure 4-13** shows the current evolution, applying the writing bias (-4 V) for 1000 s. The increasing on the current value can explain the formation of conductive filament of Si.

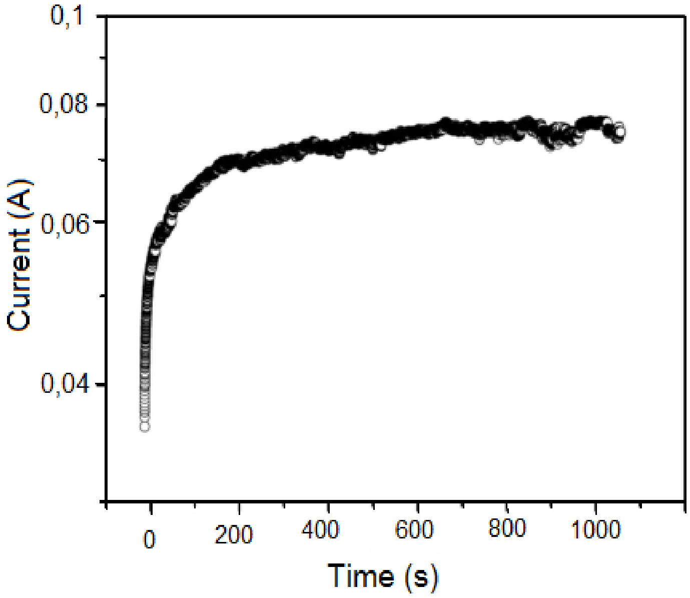

Figure 4- 13 Current evolution maintaining the memristor at the bias of writing bias (-4V), the current increases until it reaches a saturation value after 1000 seconds.

The scheme of proposed mechanism based on filament formation of Si is shown in the **figure 4-14** which the filaments of Si are formed by applying negative bias (Figure 4-14B) and are destroyed by applying positive bias (Figure 4-14C) which could return to the pristine junction by keeping positive bias (Figure 4-14A).

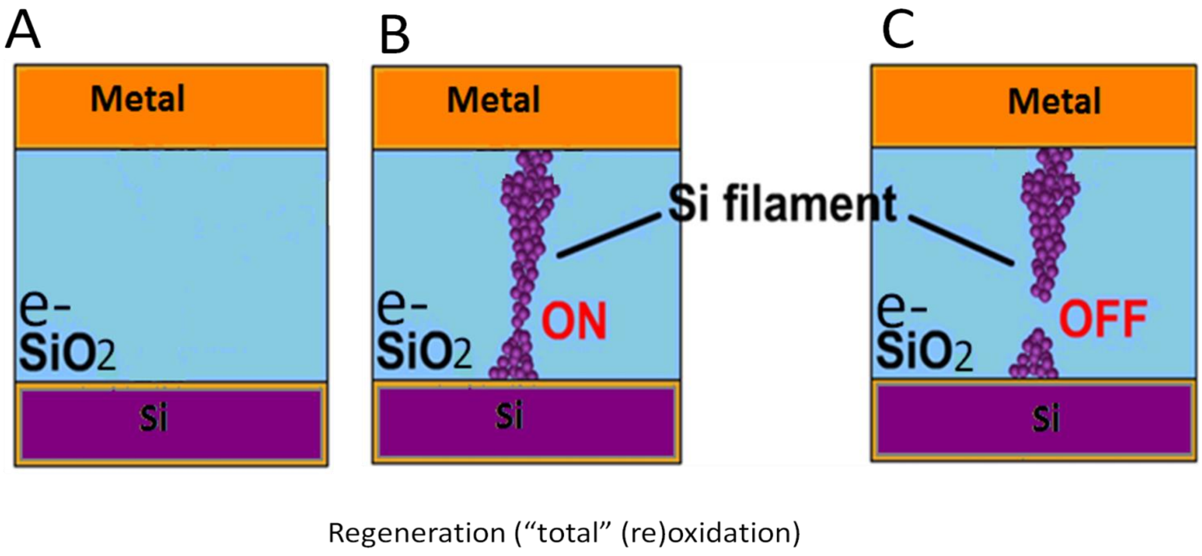

Figure 4- 14 The proposed mechanism for resistive switching behavior of Si/ e-SiO2/Metal nano-junction based on filament formation of Si, (A) Pristine Si/ e-SiO_2/Metal nano-junction after *in-situ* growth of e-SiO_2. (B) The formation of Si filaments by writing on device and keeping negative bias (ON state). Si filaments are partially destroyed (or disconnected) by oxidation in positive bias (OFF state).

The observed behavior and the formation of the outgrowths upon a few write/erase cycles obtained in the AFM and SEM images, indicates that the resistive switching is caused by an electro-reductive/electromechanical process inducing silicon filament formation, which form after e-SiO_2 breakdown, as previously observed in the case of poly-Si/ SiO_x/ poly-Si junction [42] and carbon nanotube/ SiO_2/ carbon nanotube systems.[43,44,40] The filaments are destroyed by oxidation when a positive bias is applied to the Si electrode. The increase in current observed by applying the writing bias was mainly caused by uncorrelated increases in both ON and OFF-currents and may be explained by a semi-permanent formation of silicon islands inside the e-SiO_2 matrix after repeated application of large driving voltages. This interpretation is supported by the raman characterization of e-SiOx after the application of alternate bias (see **chapter 3**, Raman characterization) which have similar condition used in resistive switching characterization.

4.6 Impedance spectroscopy

Resistance switching is a phenomenon by which some electrical insulators display a change in resistance upon application of a bias voltage. Such a phenomenon was observed several decades ago [41] and has been widely studied in1970s [42]. As described before resistance switching has been observed in several classes of oxides, including binary metal oxides (NiO, TiO_2, ZrO_2, CuxO, etc.), perovskites ($BaTiO_3$, $SrTiO_3$, etc.), manganites (Pr1−xCaxMnO3, La1−xSrxMnO3, etc.) and SiO_2. Several models were proposed to explain the effect, and the switching mechanisms such as charge-trap model [43], field-driven Mott insulator-metal transition, Schottky barrier modification at electrodes, or formation of conducting filaments upon field enhanced migration of cations or anions across the film’sthickness (filamentary model). Despite several years of research efforts, the origin of resistance switching is still uncertain. Impedance spectroscopy is one the powerful technique which can give us more details about the real mechanism of the interface state of these junctions.

Y. Hirose considered an equivalent circuit model of metal/ insulator (oxide)/ semiconductor [44] and the situation is illustrated by an equivalent circuit superimposed on a corresponding band diagram and he suggested a (RC)R and (RC)(RL)R circuit for the actual experimental results of this MOSTD which there is metal/SiO_2/ Si interface configuration (**Figure 4-15**).

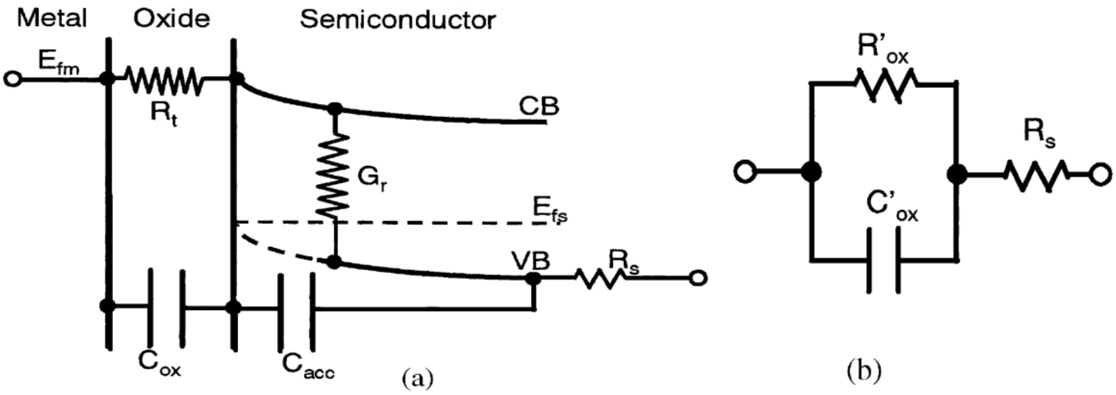

Figure 4- 15 (a) An equivalent circuit model of p-type biased in accumulation superposed on the band diagram: R_t, electron tunneling current path through the oxide; G_r, recombination conductance; E_{fm}, the Fermi level in the metal ; E_{fs}, the fermi level in the semiconductor; C_B, Si conduction band; V_B, Si valance band. (b) The simplified equivalent circuit. (c)

P. Zhao et. al. reported a study of influence of charging and discharging in Si nanocrystals (nc-Si), which are embedded throughout the gate oxide in metal-oxide-semiconductor (MOS) structures, on the current-voltage and capacitance-voltage characteristics of the MOS structures and he suggested a (CC)C circuit for the MOS structure with nc-Si embedded in the gate oxide. Charge could be stored in the three elements, *i.e.*, the nanocrystals (C_{nc}), the remaining gate oxide capacitor (C'_{ox}), and the Si depletion (C_D) layer as shown in figure 4-16 [45]. In this study it is observed that charge transport via the nc-Si can strongly modify the current conduction and the capacitance of the MOS structures. The charge trapping in the nanocrystals can reduce both the current and the capacitance dramatically. The trapped charges can also tunnel out from the nc-Si under a bias, leading to the recovery of both the current and the capacitance. The current reduction is attributed to the breaking of the nc-Si tunneling paths due to the charge trapping in the nc-Si, while the capacitance reduction is explained by an equivalent circuit in terms of the change of the nc-Si capacitance as a result of the charge trapping.

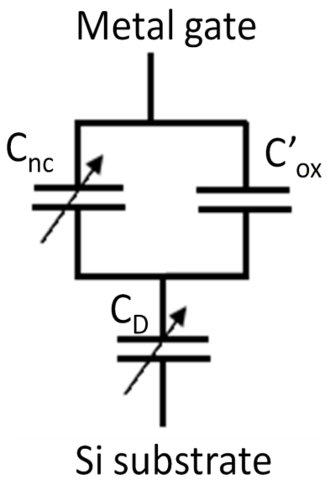

Figure 4- 16 Equivalent capacitance circuit for the MOS structure with nc-Si embedded in the gate oxide.

In this study the resistive switching behavior of our device was studied in the metal/electrochemical-SiO_2(e-SiO_2)~2-10 nm/Si devices, where e-SiO_2 is fabricated in situ by local oxidation lithography (LOx) [46] , we described before the concept and application of a new memristor, based on e-SiO_2, which is fabricated in situ with spatial control at the nanoscale. The proposed system exhibits peculiar such as the possibility to be regenerated after being stressed or damaged and the possibility to expose the metal and the oxide interfaces by removing the top electrodes (see the electrical characterization section). We demonstrated the feasibility of the method using silicon as a substrate without any process optimization.

We demonstrate the use of the impedance spectroscopy to find the right physical model of our system and to gain more information about the mechanism of the resistance switching behavior. So, we studied the metal/e-SiO_2/Si junction by using forward bias I–V characteristics and recording impedance spectroscopy measurements after each step.

4.7 Impedance characterization of the fabricated Si/ e-SiO_2/ Metal nano-junction

In these experimental report the impedance spectroscopy characterization is recorded for Si native oxide (metal/ Si native oxide/ Si), electrochemical SiO_2 (e-SiO_2) fabricated by parallel local oxidation (metal/ e-SiO_2/Si), stressed device in low resistance state (ON state) by applying a bias at -5V(metal/e-SiO_2/Si) and stressed device in high resistance state (OFF state) at +5V.

So firstly as a reference measurement simply two electrodes (silicon native and stamp) are kept in contact by moving the micrometric screw in the home-made apparatus and then it is electrically connected to FRA2 µAutolab, I-V characterization was perform to study its properties (see electrical characterization) and then the impedance measurement (stamp is connected to WE and substrate to CE+RE), was recorded in an ambient atmosphere for Si native oxide sandwiched between two electrodes (figure 4-17a, curve a). Then the device is fabricated by parallel local oxidation (LOx) which e-SiO_2 has grown on Si native oxide by applying +30V in an ambient with controlled relative humidity of ~ 90% and limited current of 0.2A. After fabrication of e-SiO2 in between the metal electrode and Si substrate, the impedance spectroscopy of this junction has been recorded in the atmosphere (figure 4-17a, curve b). According to I/V characterization of this device [64] , the switching characterization followed by cycling of potential at -5 V for 10s to switch the device ON (Writing bias), and the impedance spectroscopy with the measurements frequency was swept from 0.1 Hz–100 kHz with 0.2V of amplitude (figure 4-174, curve c), and then applying a potential of +5V for 10s to switch it OFF (Erasing bias). The impedance spectroscopy measurement of our device in the high resistance state is illustrated in figure 4-17a, curve d.

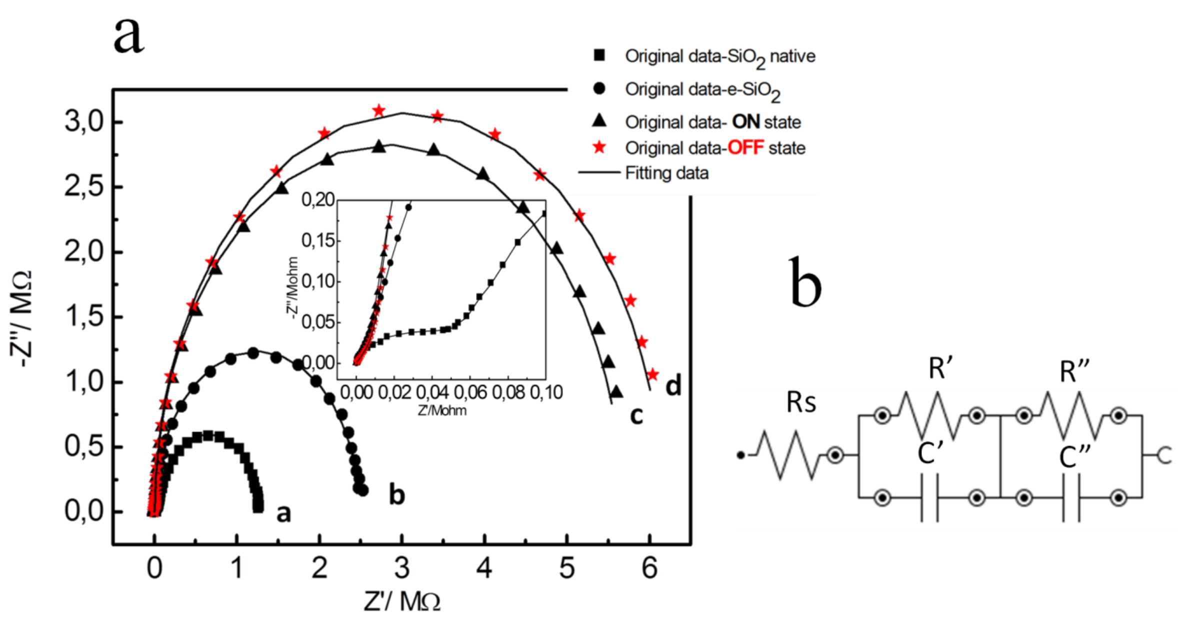

Figure 4- 17 (a) The representative Nyquist plot from the impedance spectroscopy measurements in different configurations, before e-SiO_2 fabrication, after e-SiO_2 fabrication, stressed e-SiO_2 by writing at -5V (ON state), and stressed e-SiO_2 by erasing at +5V. (b) An equivalent circuit taking account of the observed data for Si native oxide (non-fabricated e-SiO_2), fabricated e-SiO_2 and stressed device after writing at -5V and erasing at+5V. The inset is the zoom in of impedance in the high frequency range.

The native silicon oxide showed a very small semicircle (curve a, Rs =239 Ω) from the high frequency range semicircle) followed by a larger semicircle (curve a, R'= 5.62×10^3 Ω in the low frequency range). The relevant semicircle diameter at the high frequencies range, corresponding to the charge transfer resistance at the electrode surface, increased upon pristine e-SiO_2 layer and moreover electrical stressed layer of e-SiO_2 (curve b, R"= 2.45×10^6± 0.13 Ω and curve c, R"=5.83×10^6± 0.22 Ω, and curve d, R"= 6.14×10^6± 4.71 Ω). The formation of silicon filament (see suggested mechanism) on the e-SiO_2 layer caused a larger barrier to the interfacial charge transfer that was depicted by increasing the diameter of the semicircle in the spectrum. The EIS results were supported the formation of silicon filament. The main results here are confirming the physical concept of our junction by means of introduced equivalent circuit (figure 4-17b) including the resistance and capacitance which observed for all the condition of fabricated device, stressed device in ON and OFF state. It is also investigate that average resistance of device in the OFF state is bigger than ON state which confirms the suggested mechanism based on filament formation of silicon (see **suggested mechanism**).

The actual experimental results is plotted as a dots with different shapes and colors and the solid lines are the calculated spectra (Figure 4-17a) using above model (Figure 4-17b) with the parameter listed in Table1.The zoomed in snapshot of Nyquist plot showed different behavior for Si native oxide in the high frequency which has different equivalent circuit model too compare to e-SiO2 fabricated by LOx.

Table 4- 1 The parameters used for fitting the experimental data

Active layer	EIS				
	Rs/Ω	R'/ Ω	C'/nf	R"/ Ω	C"/nf
Si (Native oxide)	239± 4	5.62×10^3± 0.11	0.45± 0.01	1.21×10^6± 0.02	3.05± 0.06
Pristine e-SiO_2	128± 6	10.08×10^3± 0.61	4.64±0.19	2.45×10^6± 0.13	3.75± 0.10
Stressed e-SiO_2 (ON state)	134± 21	7.10×10^3± 1.35	7.09± 3.88	5.83×10^6± 0.22	4.64 ± 0.47
Stressed e-SiO_2 (OFF state)	266± 51	9.24×10^3± 1.04	2.23± 0.78	6.14×10^6± 4.71	4.06± 0.27

4.8 Conclusion

In summary, we demonstrated the concept and application of a new memristor, based on e-SiO_2, which is fabricated in situ with spatial control at the nanoscale. The proposed system exhibits peculiar properties such as the possibility to be regenerated after being stressed or damaged and the possibility to expose the metal and the oxide interfaces by removing the top electrodes. We demonstrated the feasibility of the method using silicon as a substrate without any process optimization, therefore a significant improvement on the device performance is expected by optimizing the process and by embedding specific dopants and/or nanoparticles in the e-SiO_2[53].

The proposed system is compatible with the current (silicon) technology, the resolution of the nanopatterning process can be further downscaled to the spatial resolution of lithography based on local oxidation [46,18] and extended to many other systems,[47,4831,32] including magnetic manganites,[49,50, 33,34] where the magnetic and conducting properties are closely related to the oxidation state. This will lead to the development of a new generation of memory devices based on resistive switching, where the active, re-generable layer is fabricated in situ.

Impedance spectroscopy as a complex method here is used to investigate the physical concept related to our junction. The nyquist curve shows an equivalent circuit involve resistance and capacitance that in the OFF state respect to ON state show higher resistance. The results could confirm the relation between the switching of our system and formation of Silicon filament.

4.9 Experimental Section

Sample preparation: Si/e-SiO2/Metal junctions were fabricated using a home-made apparatus as described in ref. 21 in the main text. In order to put the stamp in contact with the substrate, we placed the sample holders at the bottom of the apparatus, so that the stamp was fixed on stamp holder in the top-side and moved downward by a micrometric screw. The substrate was fixed on a rigid sample holder on the bottom side.

The substrate and replica stamps were connected electrically to the voltage source (ELIND Model 3232). Then in order to check the quality of the contact, the resistance between these two electrodes was measured while increasing the applied force. The system was inserted inside the sealed chamber (Tupperware, USA) with feedthroughs for the voltage leads and hygrometer’s probe (PCE Model 313-A). The relative humidity (RH) was kept stable by fluxing moist nitrogen. When the RH reached to 90%, the stamp and substrate were put in contact by the downward motion of the micrometric screw. During this process, the resistance between the two electrodes was monitored while the humidity was kept constant. In this configuration, the silicon substrate/water/metal stamp system is an electrochemical cell, with the silicon substrate acting as the anode, the pure water layer between silicon and stamp as the electrolyte and the metal stamp as the cathode. Then the bias voltage of 32 V DC with limited current (typically 200 mA) was applied between the electrodes for 30 seconds. The oxidation reaction took place at the anode electrode and at the end of this electrochemical reaction a pattern of parallel oxide lines was formed (Ref. 21 in the main text). The SiO2 thickness could be varied between 2 and 25 nm depending on the bias voltage, application time and relative humidity[18,21]).

Typically, we fabricated oxide lines between 200 nm and 10 nm in width, obtaining cross-junctions with a volume of $200 \times 200 \times 15$ nm^3.

Stamps: see **chapter 2**.

The stamp motif consists of parallel lines with a periodicity of 1.4 μm, a width at the apex of 200 nm and a depth of 200 nm. In some experiments the coating of commercial blank compact disks was directly used as stamp.

Substrates: The substrates were 1 × 1 cm^2 pieces of Si p- and n- doped, covered with a native silicon oxide layer (Siltronic, type n and p, 0.5 mm thick, orientation [100], resistivity of n-type: $\rho = 0.0015\ \Omega$ cm and p-type: $10 < \rho < 20\ \Omega$ cm). The substrates were cleaned by sonication for 2 min. in electronic-grade water (milli-pore quality), 2 min. in acetone (Aldridch chromatography quality) then 2 min in 2-propanol (Aldridch spectroscopic grade quality).

Scanning Electron Microscopy: The scanning electron microscopy (SEM) images were obtained with a ZEISS 1530 SEM equipped with a Schottky emitter and operating at 10 keV. The instrument was equipped with an Energy Dispersive X-Ray Spectrometer (EDX) for X-Ray microanalysis, and two different Secondary Electrons (SE) detectors, the InLens (IL) and the Everhart-Thornley detectors (ETD). The IL detector collected a secondary electrons component (the so-called SE1) generated by the primary incident beam in a small region around the beam impinging point, and for this reason it shows an higher sensitivity to surface morphology. The ETD collects the complete SE spectrum, the SE1 component, but also the SE generated by the back scattered electrons (BSE) emitted by the specimen (SE2) and the SE generated by the BSE colliding with the chamber of the instrument (SE3). In addition ETD acts also as a BSE detector with a rather low efficiency. Therefore the detected signal shows a reduced sensitivity to the local surface morphology, but a higher sensitivity to the density and/or compositional variations.

Atomic Force Microscopy: All the AFM images were recorded with a standalone AFM (SMENA NT-MDT Moscow) operating in air, in intermittent contact mode at room temperature with a relative humidity 55%. Si cantilever (NT-MDT NSG10, with typical curvature radius of a tip of 10 nm and typical resonant frequency of 255 KHz) were used. The topographic images were corrected line-by-line for background trend effects by removal of the second-order polynomial fitting.

Electrical measurements: We used a Keithley 2612 SourceMeter for ISD measurements, controlled by a dedicated home-made acquisition software. For electrical testing, the bias was applied to the silicon electrode, while the top metal electrode was grounded. The electrical characteristics were measured on devices with 10^6 cross-points in parallel. No relevant difference in the behavior was observed by measuring our memristor without stamp rotation (thus in configuration as in Figure 1B), except for a reduction of the absolute value of the current.

In order to test the quality of our junction we used our set-up on a Si/SiO_2 (native oxide)/Metal junction which confirms the results that can be found in the literature.

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Chapter 5

Memory resistive properties of Si/ e-SiO_2/ Graphene Nanojunction

This chapter describes the applications of pLOx procedure in device fabrication by using silicon native as a substrate and Graphene as building block material which acts as an electrode.

5.1 Introduction

Graphene is a two-dimensional material consisting of carbon atoms tightly arranged in an hexagonal lattice. In the last decade, it has been widely studied both for fundamental physics and technological applications. The key factors of such an intense research effort are properties such as high charge carriers mobility, large current-carrying capacity and high thermal conductivity combined with mechanical robustness and excellent chemical stability [1,2,3]. Due to its excellent properties, it became a very appealing material for scientist in a variety of applications. Graphene has been used as an active functional material (e.g. as channel of field effect transistor, sensors, active layer of memristors, etc.) [4,5,6,7] or passive component (e. g. electrode) [8,9] in a variety of applications.

Graphene retain the potential for being integrated in the so called “memory resistors” or “memristors” (see chapter 4) which are one of the most likely candidates for the post-CMOS technology in nanoscale memory-bit cells [10]. In such devices, graphene can act either as active layer [11,12,13] or as electrode [14,15].

Here we demonstrate that graphene flakes (GFs) and patterned graphene films can be used as electrodes for nanofabrication by *in-situ* parallel local oxidation. In particular, we demonstrate the fabrication of structures made of SiO_2 on silicon that replicate the GFs/films morphology. Eventually, we demonstrate that these structures can be used as memristors.

5.2 Oxidation through graphene flakes

Graphene flakes were prepared by micromechanical cleavage [16] onto silicon substrates and were identified by a combination of optical microscopy [17], Raman spectroscopy and morphological characterization by AFM.

After that GFs were moved onto silicon substrates by means of a transfer process, based on a PMMA sacrificial layer. Success of the transfer was confirmed by Raman spectroscopy.

In order to contact GFs deposited on doped silicon we used the experimental set-up for parallel local oxidation [18,19] that is described in the **chapter 2**[20,21]. The process is based on, a conductive stamp, which is placed onto the Graphene/ Si surface in moist air environment (Relative humidity >90%). Under these conditions a water meniscus forms between the stamp and the surface, resulting in an electrochemical cell, where graphene and the stamp constitutes the electrodes.

Good conformal and electrical contact between stamp and surface was guaranteed by the use of metallized soft stamps (see Replica Molding (RM) and metalized stamp, **chapter 2**), as shown in figure 5-1. By applying an appropriate bias of 16 V the surface is oxidized. The process acts only under the stamp protrusions and at the GFs/ substrate interface, which is accessible to oxygen or water [22, 23] that work as features of the stamp (Figure 5-1). It is noteworthy that GFs does not require any lithographic manipulation of the GF, which can be directly deposited either on the stamp or onto the surface.

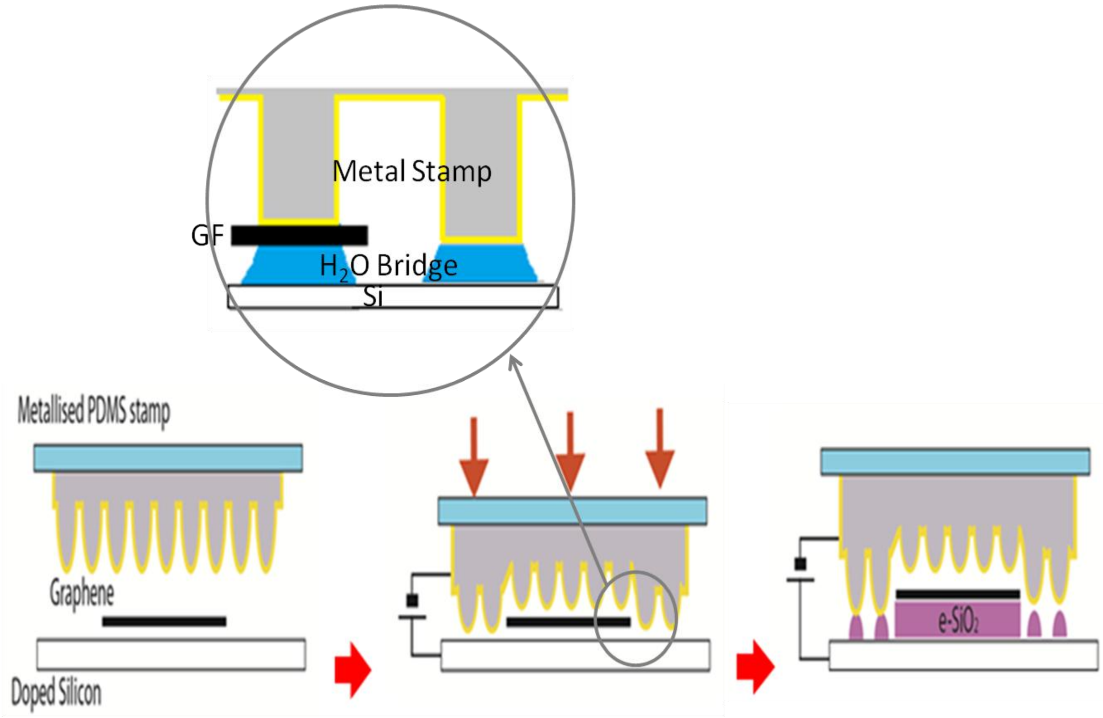

Figure 5- 1 Scheme of the processes. a) Parallel local oxidation using a soft stamp applied to graphene flakes deposited on the silicon surface.

By applying a bias larger than 15 V (Si positive), both the silicon under the stamp protrusions and under the GFs, is oxidized and grows conformal to the stamp protrusions and to the GFs.

The e-SiO_2 thickness can be regulated by time and bias voltages in the range of 0-20 nm [18]. Its control depends on the effective area of the stamp features and GFs in contact with the surface. Figure 5-2a and 5-2b show a GF before and after the process described in figure 5-1 using a stamp made of parallel lines (here we applied 30 V for 60 s). Figure 5-2c shows the zoom of the same flake after local oxidation process. In this condition the increase of the mean thickness of GFs at about 3.1±0.5 nm (comparing pre and post topography processing) and the formation of the SiO_2 stripes out of the GFs confirm the success of the experiment.

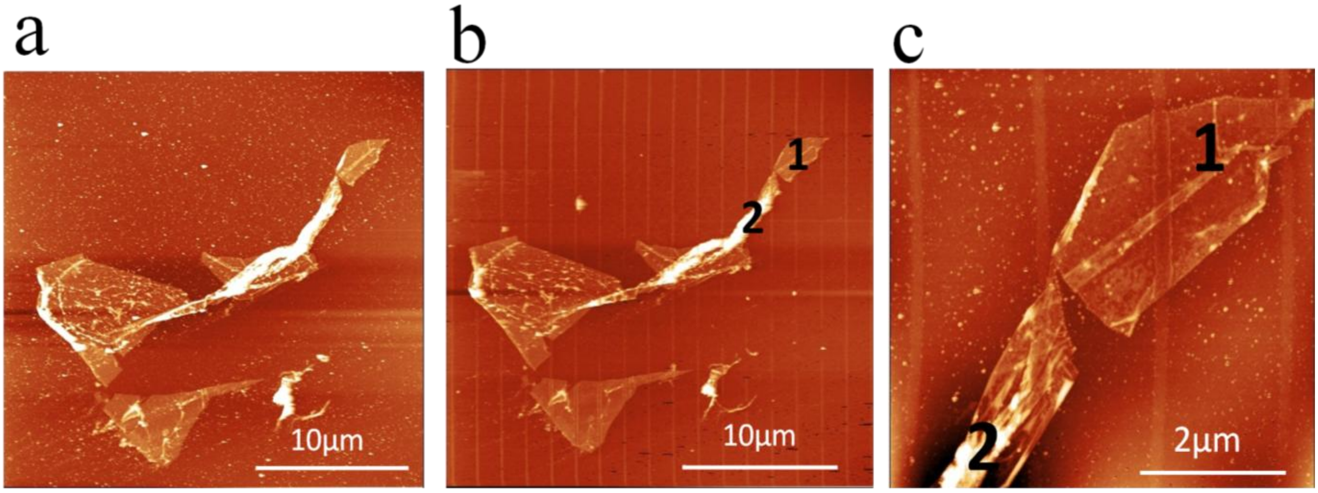

Figure 5- 2 (a) AFM image of graphene flakes (GFs) deposited on doped silicon. (b) AFM image of the same zone after local oxidation using a stamp made of parallel lines and (c) Zoom of b with flake deformation.

In order to investigate the integrity of GFs, samples were investigated by µ-Raman scattering [24] . This technique allows counting the number of layers [25], as well as monitoring and quantifying doping [26,27], defects [28] and strain [29].

Figure 5-3 shows Raman scattering measurements in different zones which is collected by mapping records within the area of the investigated GF after the parallel oxidation process. The Raman spectrum obtained from the single layer GF (position 1 in Figure 5-2) shows only a sharp single 2D peak at 2695.6 cm^{-1} (figure 5-3, blue line). G peak is below detection limit, which implies a very high I(2D)/I(G) ration and therefore low doping. The spectra collected from the zone 2, show a broad D' mode at about 2710 cm^{-1}, a G mode at 1582 cm^{-1} (figure 5-3, red line) almost of the same intensity, which is compatible with the multilayer of GFs. The shape and position of the detected Raman mode at position 1 are consistent with single layer GF. Also, no D peak is detected, proving that the parallel oxidation process does not induce structural defects.

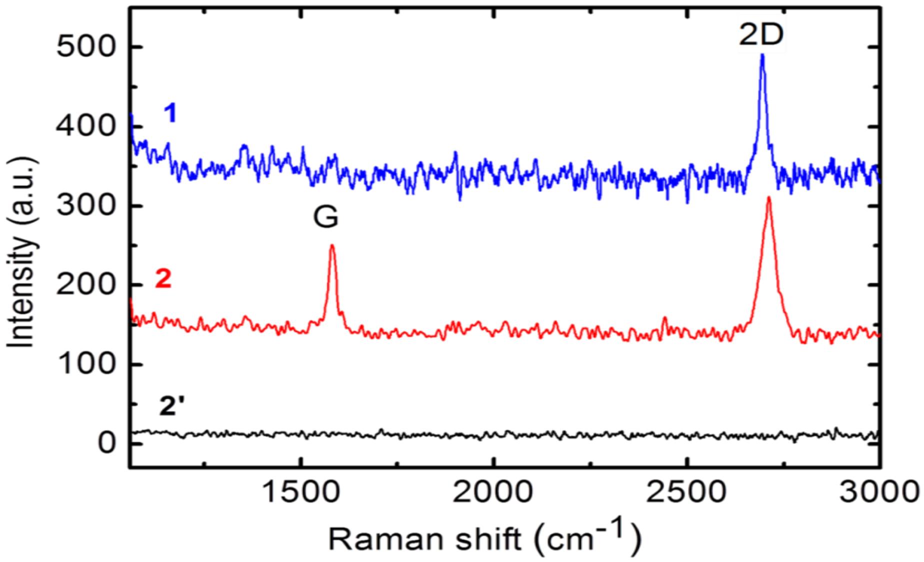

Figure 5- 3 The Raman spectra of GF, corresponding to zone 1 (blue line) and zone 2 (red line) of figure 2. The Raman spectra of zone 1 shows only a sharp single 2D peak at 2695.6 cm^{-1}, typical of graphene single layer while the spectra in zone 2 shows a broader 2D peak at 2711.67 cm^{-1} and a G mode at 1583.92 cm^{-1}. Black line shows the Raman spectra of recorded in zone 2 after O2 plasma etching.

In order to investigate the SiO_2 grown underneath of graphene flakes, the sample was treated by oxygen plasma exposure. The treatment by oxygen plasma, which is performed for 10min and 75W intensity, does not affect on the e-SiO_2 (except a possible slight reduction of its thickness, typically <20%), therefore the structures fabricated by local oxidation remain almost unaltered on the surface as confirmed by AFM images (Figure 5-4a, 5-4b). It is worth to note that the e-SiO2 structures replicate the GFs, including the morphological defects (e.g. the wrinkles, fold and rolling), which works as stamp motif [30]. The recorded Raman spectra in the zone 2 after O2 plasma etching confirms the removal of graphene, as no carbon peak is detected (figure 5-3, black line) , it is corresponded to the zone 2' in the AFM image (figure 5-4).

Figure 5-4a shows a GF after O_2 plasma treatment, which used to remove the layer of GF and investigate the silicon surface underneath of GFs. Figure 5-4b shows the zoom of the same flake after O2 plasma treatment.

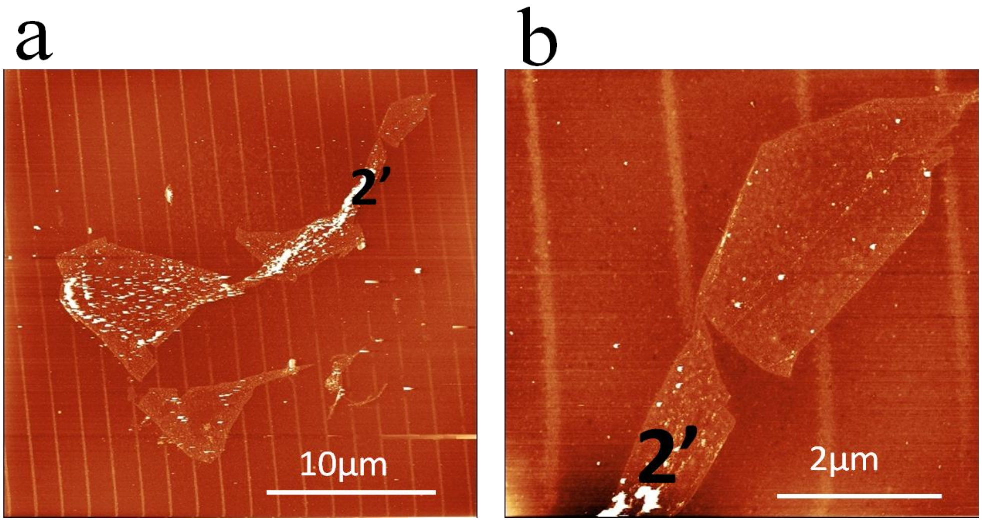

Figure 5- 4 (a) AFM image of graphene flakes (GFs) deposited on doped silicon proceed by local oxidation and after plasma etching in oxygen atmosphere. (b) Zoom of the same zone after plasma etching. At position 1 is indicated a single layer of GF, at position 2 multilayer of GF where Raman spectra were recorded.

During the process GFs can be "molded" by the stamp: in this case the stamp features are reproduced on the GF (Figure 5-5a) as happens in nanoimprint lithography. Normally these deformations are small and do not affect the oxidation process (i.e. the deformations are not transferred on SiO_2) (Figure 5-5b) however, applying on the stamp a pressure greater than ~100 kPa (estimated value, which depends on the features and the nature of the stamp) these artificial modifications can also be transferred to the e-SiO_2 structures allowing the fabrication of more complex structures.

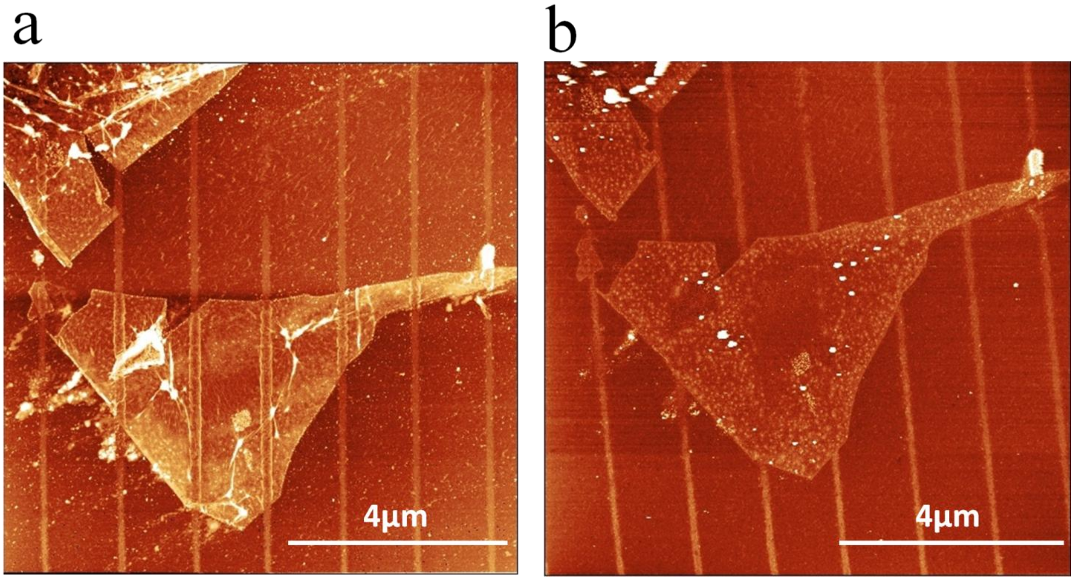

Figure 5- 5 (a) AFM image of graphene flakes (GFs) deposited on doped silicon after local oxidation using a stamp made of parallel lines and (b) after plasma etching in oxygen atmosphere.

This investigations confirm, while GFs is deposited on silicon surface under parallel local oxidation and making electrical contact from the top metalized stamp, it can act as an electrode and silicon can be selectively oxidized underneath of GFs independently from the shape of the stamp. Moreover it is observed for the samples treated by oxygen plasma etching that e-SiO2 growth underneath of GFs are quite stable and not aging effect was observed.

5.3 Fabrication and characterization of GFs / e-SiO_2/ Si junction

As recently demonstrated, SiO_2 [31,32,33] can exhibit electrical bistability and can be used as the active layer in memristors. Our process allows a facile-fabrication of memristor structures. Indeed, as result of the oxidation process, we obtain a GF/ e-SiO_2/ Si stack.

In order to fabricate a GFs/ e-SiO_2/Si junction where only the area of the substrate with GFs contributed to the electrical transport, some spacers were deposited in between the GFs (**Figure 5-6**). When the stamp is placed on top of the sample it is in electrical contact only with GFs. So the spacers prevent the formation of the meniscus outside the GFs area, and therefore the direct oxidation of the silicon outside the GF. Thus, the silicon substrate will be oxidized just under GFs.

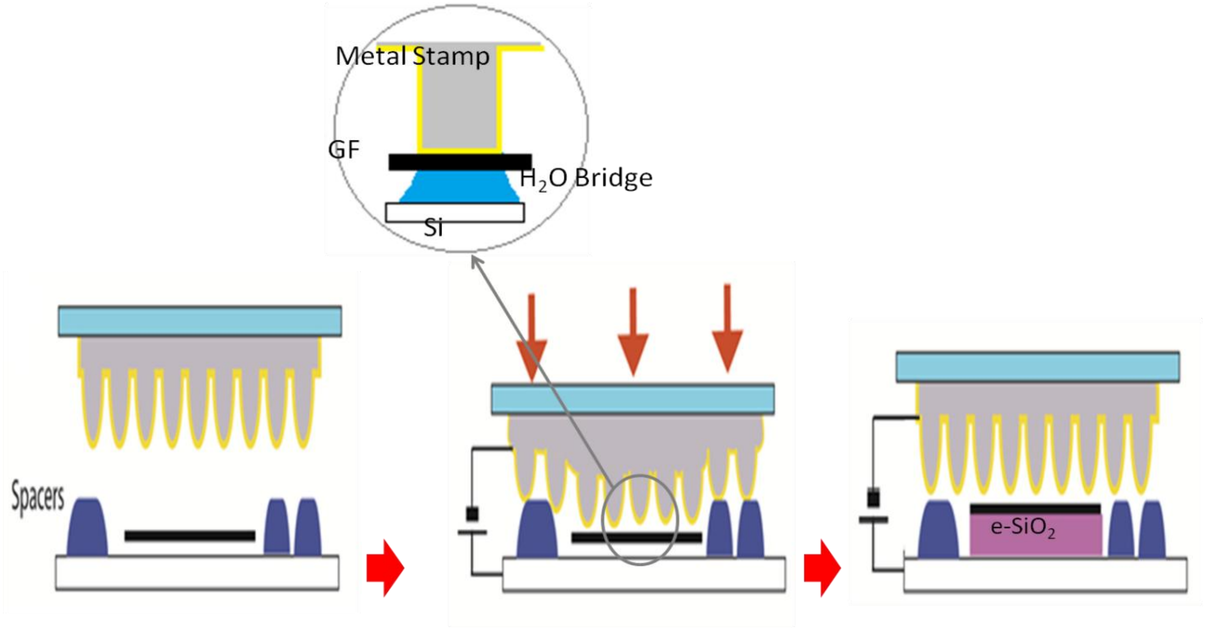

Figure 5- 6 Scheme of the processes. a) parallel Parallel local oxidation using a soft stamp applied to graphene flakes deposited on the silicon surface using fabricated spacers between the GFs.

AFM imaging confirmed that no oxidation occurs outside the GF as we could not detect any sign of SiO_2 stripes in the topography characterization (**Figure 5-7**). Therefore, by this experimental set up we could reach to the configuration of GFs/ e-SiO_2/ Si junction which suggest the possibility of resistive switching behavior that obtained for the previous device (see **chapter 4**).

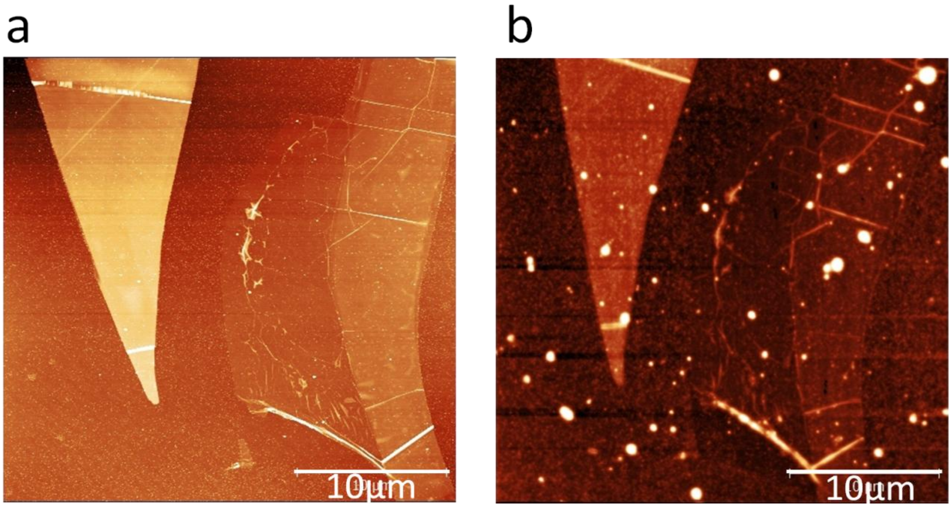

Figure 5- 7 (a) AFM image of graphene flakes (GFs) deposited on doped silicon with the spacers deposited in between . (b) AFM image of the same zone after local oxidation using a stamp made of parallel lines

So the electrical characterization of the fabricated junction is proposed to investigate its properties. I-V characteristics of our junction were measured by applying the bias to the silicon (the stamp/graphene is grounded) in a two-probe configuration. **Figure 5- 8** shows a typical curve with bias sweep between -13 V and +10 V. A hysteresis is clearly visible.

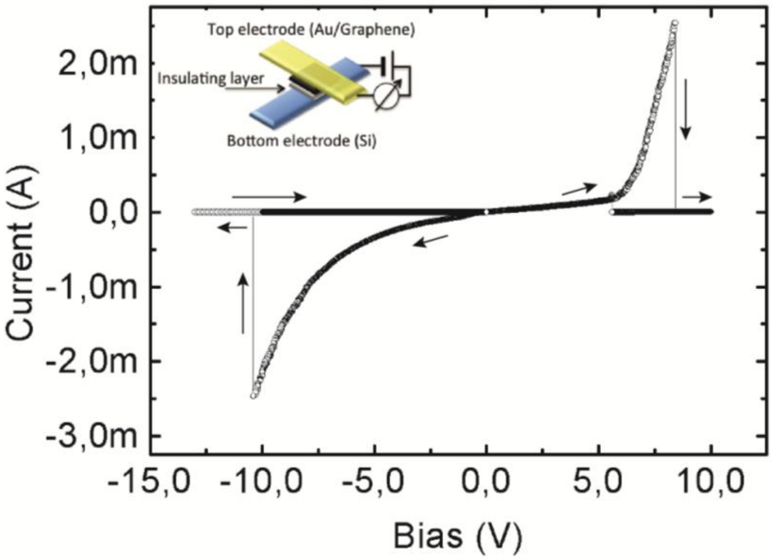

Figure 5- 8 Hysteretic **unipolar** switching I−V curves for a ~4 nm thick e-SiO_2 thin film. The voltage ramp is applied to the silicon from negative to positive values and back to complete the cycles as indicated by the arrows. The inset shows a schematic picture of the memristor.

The device always starts in the low resistance state (R_{on}) and once a positive voltage threshold is reached it switches to the high resistance state (R_{off}). The R_{on}/ R_{off} ratio is more than 7000 at 1 V, going from 53 μA to 7.3 nA at reading voltage (-1 V). The effect is volatile, which is more visible in the positive branch of the I-V, where on the way back to zero bias, at 5V the device switches back to low resistance and the negative branch starts in the low resistance state. The symmetric current thresholds and volatility could indicate that the resistive switching is due to thermal effects [11], while the slightly different life time of the high resistance state between the positive and negative branches could indicate that charged species are involved in the switching process [11]. However we cannot exclude other possible contributions to the switching. The low resistance I-V appears asymmetric above 1 V, indicating that the resistance drops mainly at the interfaces. On the contrary, the high resistance state is symmetric, which is more characteristic of low mobility bulk transport. Unfortunately, in GF based devices this bistability is reproducible only for a few cycles, eventually leaving the sample in a high-resistance state. This is probably due to a rupture on GF since the device becomes non-regenerable as observed in conventional metal/e-SiO2/Si memristors [34].

5.4 Fabrication and characterization of graphene / e-SiO_2/ Si junction

As the stability of GFs-base device was very poor and just for few cycles, patterned graphene-based devices are proposed to improve the stability of our junction. Some microstructure of graphene were obtained patterning a solution of suspended graphene [35] on silicon wafer. The microstructures consist of square pads with ~10 μm width, ~505 nm thick which are separated by 12μm from each other. The microstructure of graphene were molded by lithographically controlled wetting (LCW) [36], which is a powerful technique for the manipulations of several functional materials, colloids and nanoclusters in a single step and large area [37,38,39] . In LCW a stamp is gently placed in contact with a liquid thin film spread on a substrate, the fluid layer develops instability where the capillary forces pin the solution to the stamp protrusions, forming an array of menisci. As the critical concentration is reached by solvent evaporation, the solute precipitates from the solution onto the substrate inside the menisci, giving rise to a structured thin film that replicates the protrusion of the stamp. The solvent, the interaction among the molecules of solute and the interaction between solute and substrate determine the morphology of the printed features. In this case, silicon substrate was treated by O_2 plasma for 1 min in order to have best contraction between the graphene solution and the substrate. **Figure 5-9a** shows a scheme of LCW and the device fabrication by parallel local oxidation (figure 5-7b). A detailed description of LCW protocol is reported in **chapter 2** and ref 40.

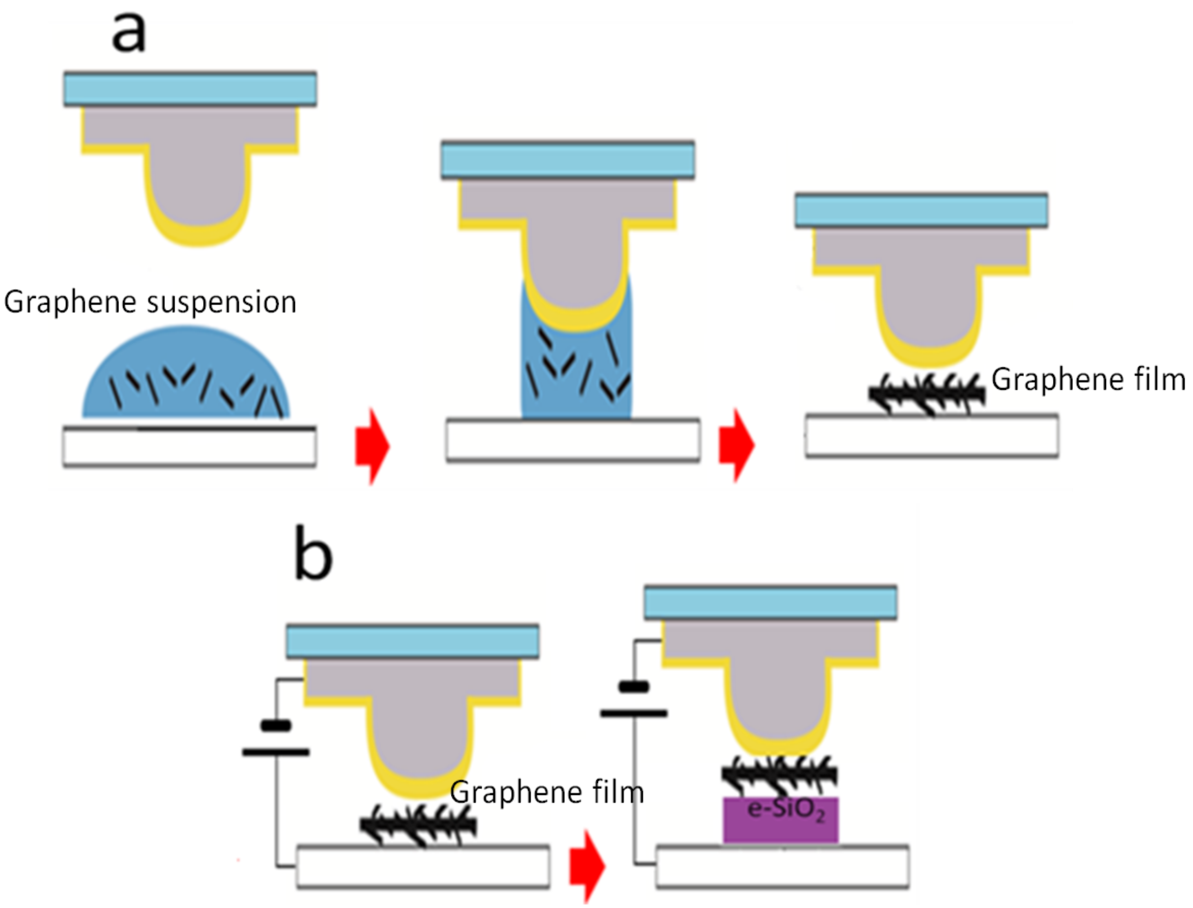

Figure 5- 9 Scheme of the processes. a) Patterning a film of graphene by LCW, b) parallel local oxidation using a soft stamp applied to graphene film deposited on the silicon surface.

Graphene solutions were patterned into parallel electrodes 10.5± 1.2 µm width and 505± 15 nm tick. The electrodes were electrically contacted from the top using the same procedure described for GF. In printed films the distance between the stamp and the surface which is the thickness of the electrodes, prevent the formation of the meniscus directly under the stamp protrusions, therefore the oxidation of silicon occurs only underneath of graphene. **Figure 5-10** shows the morphology characterization of pristine patterned graphene film by LCW (Figure 5-10a) and the same sample after device fabrication, electrical stress and removing the graphene film by oxygen plasma (Figure 5-10b).

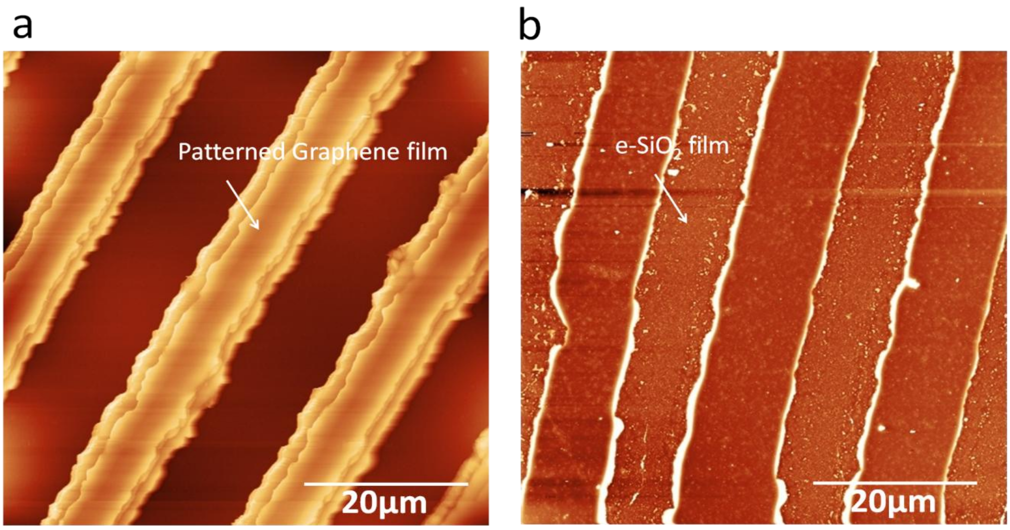

Figure 5- 10 (a) AFM image of pristine patterned graphene film by LCW into parallel electrodes of 10.5±1.2 µm width and 505±15 nm tick. (b) AFM image of fabricated device by using the same sample, after plasma etching in oxygen atmosphere with the thickness of ~10nm e-SiO2.

The e-SiO2 growth underneath of patterned graphene film with the thickness of ~10nm confirmed our strategy in device fabrication here the fabrication of graphene/ e-SiO$_2$/ Si junction too. I-V characteristics of our junction were measured by applying the bias to the silicon (the stamp/graphene is grounded) in a two-probe configuration. **Figure 5-11** shows a typical curve with bias sweep between -20 V and +10 V. An hysteresis is clearly visible in the negative branch of the curve.

Patterned graphene-based devices show remarkably different properties: although the shape of I-V curve is also different but these devices are much more stable under stressful conditions and posses durable non-volatile memory characteristics.

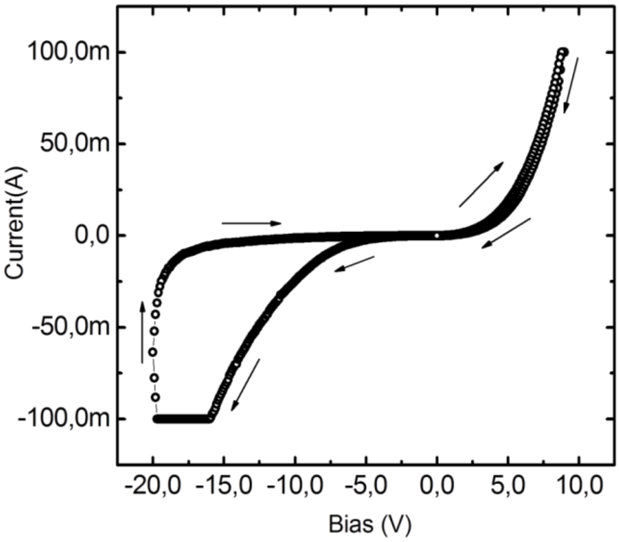

Figure 5- 11 Hysteretic unipolar switching I−V curves for a 10 nm thick e-SiO2 thin film. The voltage ramp is applied to the silicon from positive to negative values and back to complete the cycles as indicated by the arrows.

To elucidate their memory properties and their stability, we applied a series of programming cycles consisting in a 1s, -17 V write pulse, followed by 10 cycles of 1s, -1 V reading voltage pulses and 1s short-circuiting 0 V pulses, followed by a 1s, 9 V erase pulse and 10 cycles of the reading/short circuit sequence (**Figure 5-12**). The non-volatile resistive states were retained for at least one day.

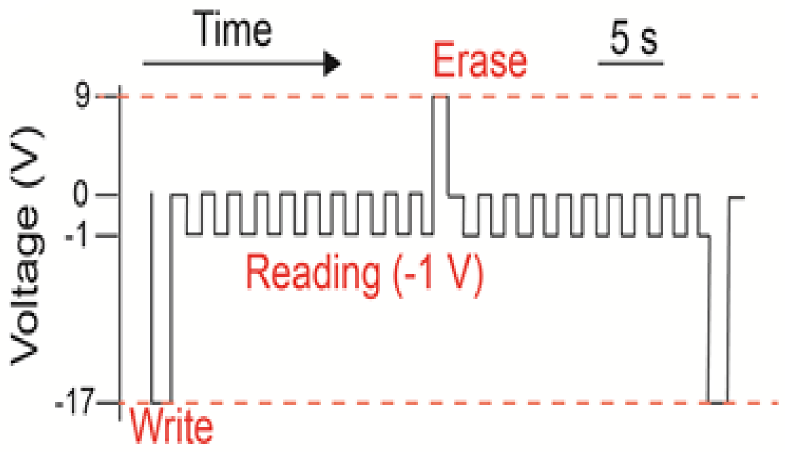

Figure 5- 12 The scheme of the sequence of applied potential to write, read and erase the device and corresponding current.

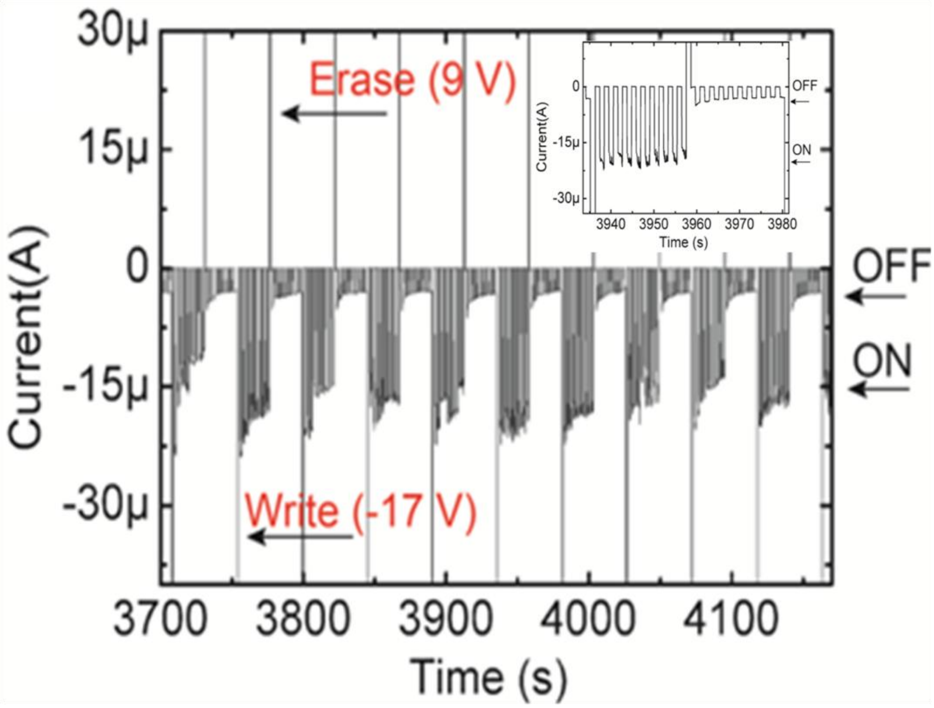

Figure 5- 13 Memory characterization of patterned graphene based memristor. Memory properties read by using a potential of -1 V after a pulse of -17 V to switch ON the device and +9 V to switch OFF. The device is stable over more than 10^4 cycles without any signs of degradation. The inset shows the zoom in one switching cycle.

Although in these devices the ON/OFF ratio is not improve and get less than device based on GFs we observed an excellent stability over more than 10^4 cycles without any signs of degradation (**Figure 5-13)**. The current of the ON-state tended to decrease by ~10% in the first 100 cycles, after which it remained stable over more than 4×10^4 cycles (note that we did not test longer number of cycles).

5.5 Conclusion

In conclusion we demonstrated selective oxidation of Si, where graphene acts as a template electrode. By applying a voltage between a conductive stamp and graphene in a humid atmosphere, we showed that oxide is grown underneath the whole graphene area, independently from the pattern of the stamp. So the grown e-SiO_2 film is conformal to the graphene, and allows the fabrication of novel devices. As proof of concept we realized graphene/ SiO_2/ Si junctions that exhibited electrical bistability and can therefore be used as memristors. The in-situ fabrication takes place only where the electrode is located. This allows us to by-pass a series of fabrication steps that often limit the application of graphene, addressing what had been a significant obstacle to the use of graphene in future generations of high-performance electronic devices. In forthcoming works the spatial resolution of the nanopatterning process can be further downscaled to the spatial resolution of lithography based on local oxidation and extended to many other systems, including magnetic manganites, where the magnetic and conducting properties are strictly related to the oxidation state. This will lead to the development of a new generation of devices based on graphene, where the active layer is fabricated in-situ.

5.6 Experimental Section

Graphene flakes preparation:

Graphene flakes are prepared by micromechanical cleavage [41] onto silicon substrates. Graphene flakes are identified by a combination of optical microscopy [42], Raman spectroscopy and Morphology characterization by AFM. Graphene is subsequently moved onto silicon substrates by means of a transfer process, based on a PMMA sacrificial layer. Success of the transfer is confirmed by Raman spectroscopy, which also allows excluding process-induced defects.

Graphene solution:

Graphite flakes (NGS Naturgraphit) are ultrasonicated (Decon bath, 20W) inNMP for 9 h. The decanted dispersions are then ultracentrifuged using a TH-641 swinging bucket rotor in a Sorvall WX 100 ultracentrifuge at 10 000 rpm (~15000g) for an hour and filtered to remove flakes >1 μm, which might clog the nozzle. The suspended graphene solution characterized by optical absorption spectroscopy (OAS), high resolution transmission electron microscopy (HRTEM), electron diffraction, and Raman spectroscopy.

Parallel oxidation : GF/e-SiO_2/Metal junctions were fabricated using a home-made apparatus described in ref. [43] (see also **chapter 2**), which consists of a press where the stamp approach to the sample holder by a micrometric screw and an electrical bias can be applied between samp and sample holder. The Si substrate with graphene was firstly glued on a sample holder by means of conductive silver paint, and then the holder was placed at the bottom of the chamber. The stamp was fixed on a rigid holder with the grooves side facing down. A micrometric screw allowed precise motion of the stamp towards the sample.

More details described in experimental section chapter 4. So the oxidation reaction took place at the anode electrode and at the end of this electrochemical reaction a layer of SiO_2 was formed under the stamp protrusions and under the GFs. So-deposited SiO_2 covers the whole area underneath graphene, while it follows the shapes of the stamp outside of it. The SiO_2 thickness can be varied within 2 and 20 nm depending on the bias voltage, time and relative humidity. The exact parameters depend on the percentage of the surface covered by the GFs.

Atomic Force Microscopy: see experimental section, **chapter 4**.

Raman: Confocal micro-Raman spectra were recorded in backscattering geometry with a Renishaw RM 1000 system using the 488 nm (2.54 eV) Ar^+ laser line focused on the sample through a 80X objective lens forming a laser spot of approximately 1 μm. The laser power was kept low enough to avoid damaging and heating of graphene (70 μW that corresponds approximately to 1 kW/cm^2). In order to obtain a good signal-to-noise ratio, the spectrum acquisition time was typically 30 min. The spectrometer resolution (grating 2400 l/mm) is about 2 cm^{-1} for the laser line used.

Electrical measurements: DC measurements were carried out using a Keithley 236 Source-Meter controlled by dedicated home-made acquisition software. For electrical testing, the bias was applied to the silicon (bottom) electrode, while the top metal electrode was grounded. The voltage ramp was applied starting from 0 going to a positive voltage then going to a negative one with a rate of 50 mV/s.

In order to tests the quality of our junction we used our set-up on the Si/SiO_2 (native oxide)/Metal junction confirming the results that can be found in the literature [44].

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Chapter 6

Surface driving the selective adsorption of molecules (Bio-molecules as DNA)

This chapter describes the application of pLOx procedure on surface for driving the selective adsorption of bio-molecules.

6.1 Introduction

Nano patterning of DNA can be used as scaffolds to fabricate small functional nano-components. Functional nanoscale objects, such as metallic nanoparticles, quantum dots, semiconductor nanowires, and carbon nanotubes, display unique electronic, optical, and magnetic properties, mostly as a result of quantum confinement [1,2,3,4]. Exploiting their properties has been challenging because they are not readily amenable to organization on surfaces in interconnected circuits, networks, and arrays. So patterned DNA nanostructures [5,6,7] that can be made large enough that they may be accessible to conventional lithographic techniques are excellent candidates for bridging the gap between the minimum size reached by photolithography and that of nanoscale functional objects, which are typically only a few nanometers in size. Therefore, the application of DNA in this area takes advantage of the placement of DNA on substrates and thus a selected positioning of DNA molecules is required. Recently, patterned features to bind DNA were made by nanoimprint lithography [8,9,10,11], dip-pen nanolithography (DPN) [12,13], nanomolding [14,15], and soft lithography [16].

Placing DNA on surfaces relies upon the fact that DNA is a charged molecule. The environment for DNA synthesis and manipulation is generally an aqueous buffer solution; positive ions complex the negatively charged backbone of the DNA, making it highly interactive with hydrophilic surfaces or positively charged substrates. Lithographic patterning of hydrophilic areas has been used to selectively attach organic compounds [17], single- and double-stranded DNA molecules [18,19], or DNA nanostructures [20,21,22]. So two main issues are required to selectively bind DNA; nanopatterned structures and hydrophilic or positively attractive properties of nanostructures.

Here I present a process which is combining parallel Local Oxidation (pLOx) as an unconventional soft lithography with surface functionalization to selectively bind single stranded DNA molecules. Hexamethyldisilazane (HMDS) is used as a passivation layer on the native silicon oxide to prevent DNA attachment. DNA adhesive areas, were fabricate by patterned electrochemical SiO_2 (e-SiO_2) stripes which were covered by a layer of 3-aminopropyltriethoxylsinale (APTES), an amino terminated molecule well known to induce a strong DNA adsorption. The use of this process, as a low cost and high reproducible patterning technique enables a high precision driving and orienting of a single strand DNA molecules on a surface over large areas.

6.2 The fabrication of the designed surface for binding the bio-molecules

The surface functionalization and nano-patterning by pLOx are following requirement steps to design a driving surface for the selective binding of biomolecules such as DNA. For this purpose the substrate has to be protected from the binding of the biomolecules everywhere. The Methyl group terminated molecules (-CH_3) is one the best option which has no any interaction with bio-molecules. Here one of the best organosilicon candidate that could have a full covered surface with lowest polymerization and preferentially with the low r.m.s. roughness for the next patterning step is hexamethyldisilazane (HMDS at 99%) [5,23,24]. So firstly to promote the binding of HMDS to the silicon substrate, the Si Oxide has to be converted into silicon hydroxyl groups. Thus, a clean substrate was treated by Oxygen plasma for 10 min and then immediately used for functionalization step. A monolayer of HMDS, as a methyl (-CH_3) terminated group, was deposited on silicon substrate by using chemical vapor deposition (CVD). Through this method, a highly hydrophobic monolayer of HMDS (i.e., water contact angle of 96.5°± 1.5) was deposited on a reactive Si/SiO_2 (native) surface (i.e., contact angle of 48.2°± 0.9) which transforms the surface hydroxyl (-OH) groups into an inert film of $Si(CH_3)_3$ groups.

Then the pattern stripes of e-SiO_2 with 200 nm width, ~2nm height and the r.m.s. roughness of 0.43 nm were grown by pLOx [25,26,27,28,29] on the hydrophobic surfaces which changed slightly the hydrophobicity of the surface. This step is particularly critical for our process, for fabricating the smooth sites for binding the DNA molecules. In this case, the effective parameters are the smoothness of the substrate and also the metalized stamp. It is noticed that the patterned stripes are the printed effect of the stamp protrusions on the substrate, so it is necessary to have a quite flat features metalized stamp and substrate to obtain an ideal position. In our experimental procedure, thanks to the properties of the metal layer of the stamp and the substrate and the highly reproducibility of nanostructures, we became able to pattern the e-SiO_2 stripes with low r.m.s roughness.

In order to have electrostatic interaction between the specific position on the surface (along the stripes) and bio molecules, the patterned e-SiO_2 stripes were functionalized by a monolayer of 3-aminopropyltriethoxylsinale (APTES) [30]. This step insures the amino terminated group on the patterned position by keeping almost the same r.m.s. roughness which provide a selectively amino group along the stripes. The scheme of surface functionalization combine with the nano-patterning is illustrated in the figure 6-1.

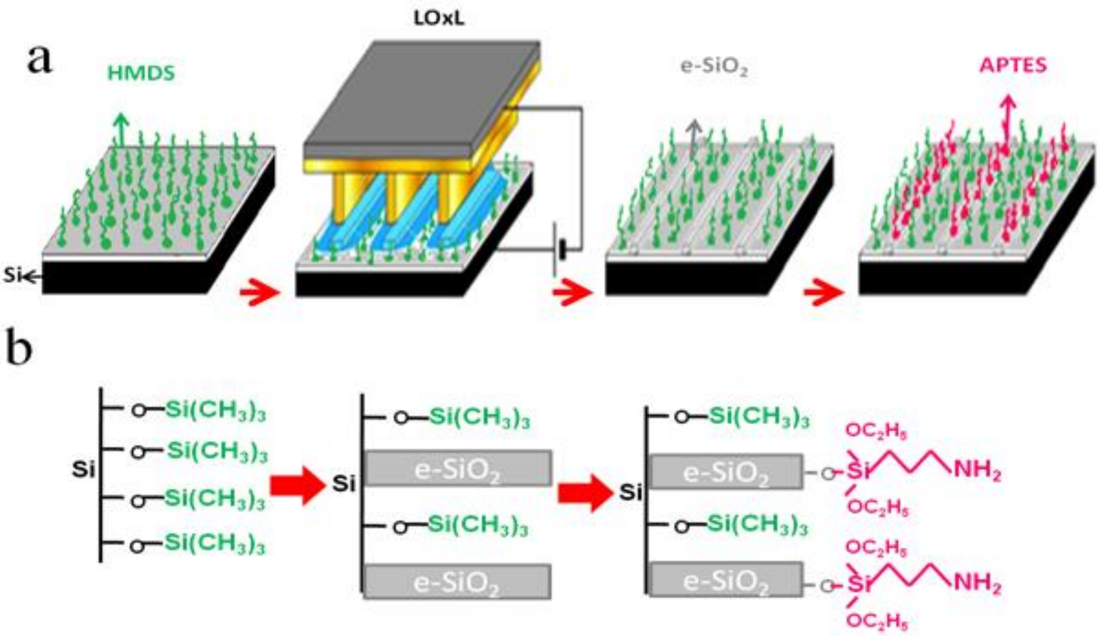

Figure 6- 1 Surface designing for bio-application by combining parallel Local Oxidation nanolithography (pLOx) and surface functionalization. a) The scheme of the major steps of the nano-patterning process. b) The chemical view of the process.

The surface characterization by contact angle measurements of water drop after each step is reported in Table 1.

Substrate	Native SiOx	SiO_x treated by Pirania	SiO_x Functionalized by HMDS	e-SiO_2 Stripes Fabricated by LOxL	e-SiO_2 Stripes Functionalize by APTES
Images					
CA /°	50.7°± 0.3	48.2°± 0.9	96.5°± 1.5	94.3°± 0.5	93.3°± 0.4

The contact angle measurement confirm that the hydrophobicity of the functionalized substrate slightly decreased by growing e-SiO_2 stripes due to the hydrophilic property of SiO_2 either by APTES functionalization, which is also due to its hydrophilic property (APTES ~ 66°) respect to HMDS. This emphasizes the authenticity of our surface designing method.

Surface characterization for each step was studied also by AFM morphology and showed that in most cases a smooth surface is obtained by deposition of an HMDS monolayer with an r.m.s.

roughness of 0.37 nm. After the nano patterning by pLOx and APTES deposition, we achieved almost smooth stripes features with the r.m.s. roughness of 0.49 nm. Figure 6-2a shows the AFM image of functionalized substrate by HMDS and the patterned substrate made by pLOx and functionalized by APTES is shown in the figure 6-2b.

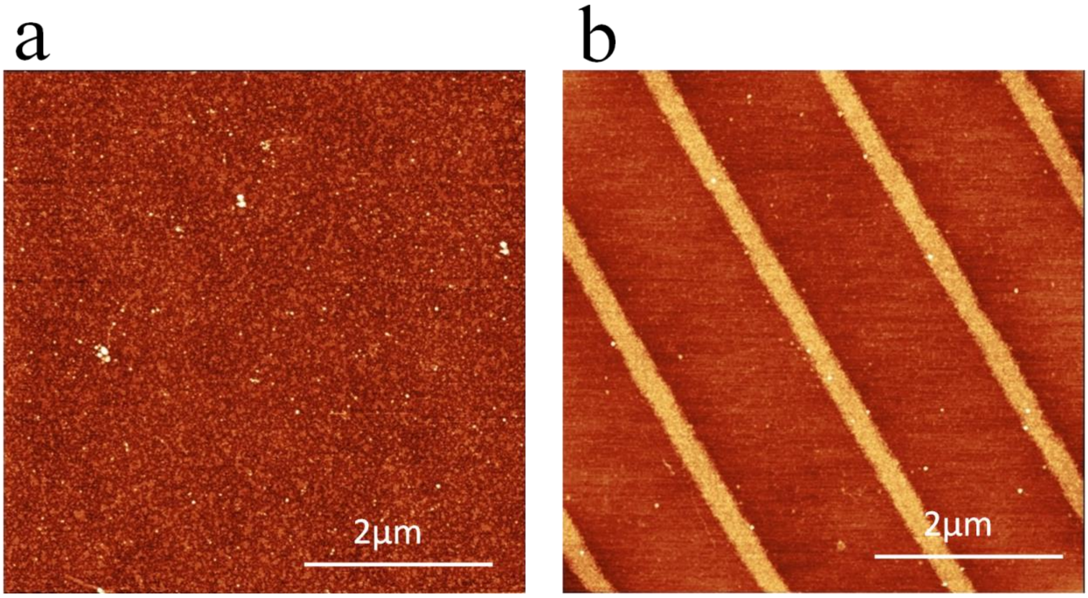

Figure 6- 2 Morphological characterization (a) AFM image of silicon substrate functionalized by HMDS following CVD, (b) AFM image of the same sample after fabrication of e-SiO_2 stripes on Si/HMDS substrate and functionalization of the e-SiO_2 stripes by APTES.

This designed surface is an excellent device to selectively bind the biomolecules in a specific position over a large area and to study their properties. Different properties of the patterned surface that along the stripes are adhesive and in between the stripes are non-sticky gives us the possibility of confining biomolecules such as DNA in a nano scale at about 200nm width of the patterned stripes. It can expand the application of our system to attach the smaller functional nanomaterials, such as carbon nanotubes or semiconducting nanowires, on the DNA scaffolds, enabling the formation of dense, ordered arrays of working devices.

6.3 DNA positioning

Our surface design, an application of pLOx, provide us with the possibility of DNA positioning. Therefore, Following the previous steps, a drop of buffer solution containing a double stranded linear DNA obtained by cutting the DNA plasmid pBR322 (4361 nucleotide pairs long = 1483 nm) was placed on the samples patterned area. Figure 6-3a shows the scheme of the DNA binding onto the stripes. The Chemical view of the interaction between DNA and patterned substrate is shown in figure 6-3b.

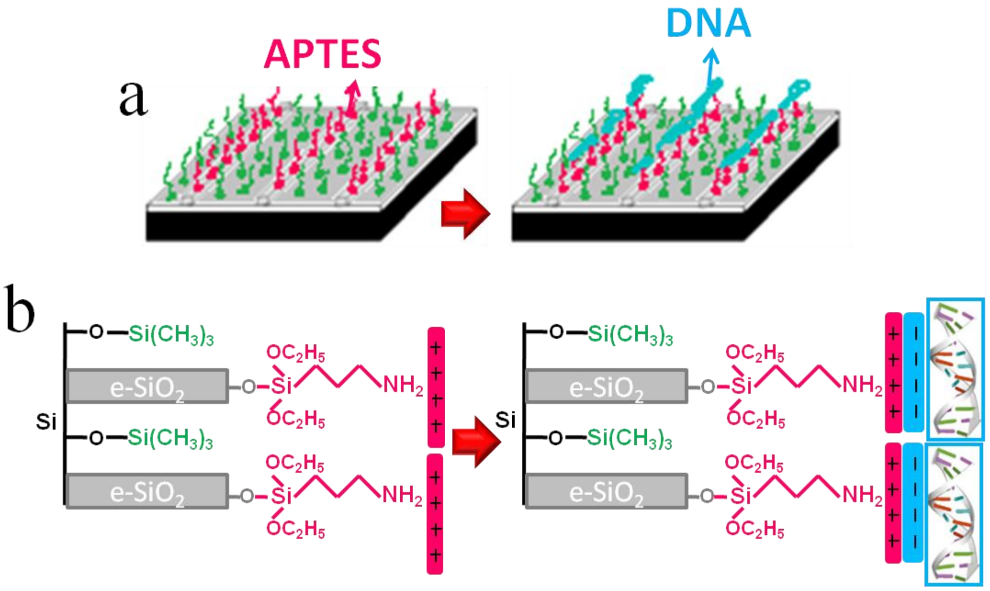

Figure 6- 3 Surface designing for bio-application. (a) The scheme of the major steps of the nano-binding of DNA. b) The chemical view of the process in the liquid phase with the pH=7.6.

As it is indicated in the scheme, placing DNA on surfaces relies upon the fact that DNA is a charged molecule and it interacts favorably with the APTES functionalized surface which in a buffer solution of pH=7 is positively charged The comparison between the nano-patterns before and after deposition of DNA illustrates both the preferentiality and the selectivity of the adsorption process (figure 6-4a and 6-4b).

We achieved a very high yield (more than 90%) of DNA attachment just in the specific location of the surface with lateral size comparable with its persistence length, and for a very few cases a single DNA molecule was bind also in between the stripes which was protected by HMDS. This could be due to some oxidation effect during the nano-patterning by LOx which may remove a part of monolayer as a points or not well covered substrates by HMDS during the functionalization. In particular, we can mention that one of the most advantages of our process is the ability of nanopattering in a very large area up to 1cm^2.

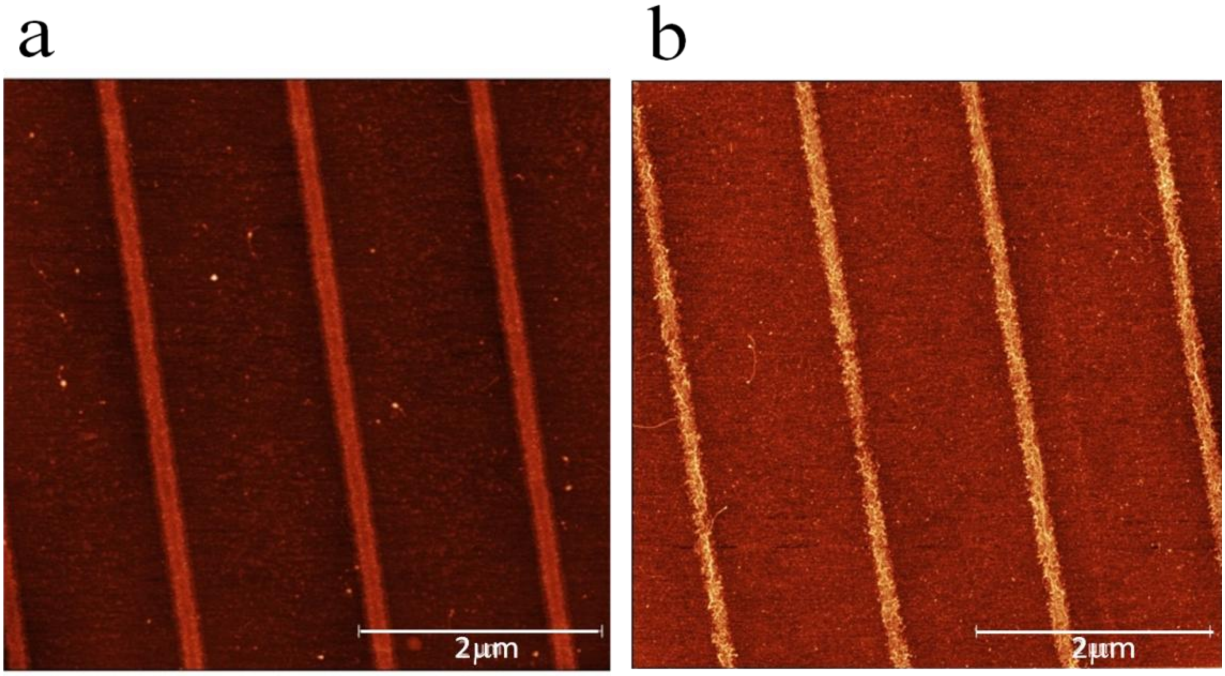

Figure 6- 4 AFM characterization of the nanopattern substrate. a) e-SiO_2 pattern stripes fabricated by pLOx before DNA deposition. b) AFM image of the distribution of the DNA on the nanopattern.

Two different diluted DNA solutions with the concentration of 5×10^{-2} μg/ μl and 5×10^{-3} μg/ μl were deposited onto the substrate by drop casting. Figure 6-5a shows an AFM image of a single SiO_2 stripes where DNA is fully confined, while a single deposited molecule can be achieved by taking diluted DNA solution over the nanopatterned surface (figure 6-5b).

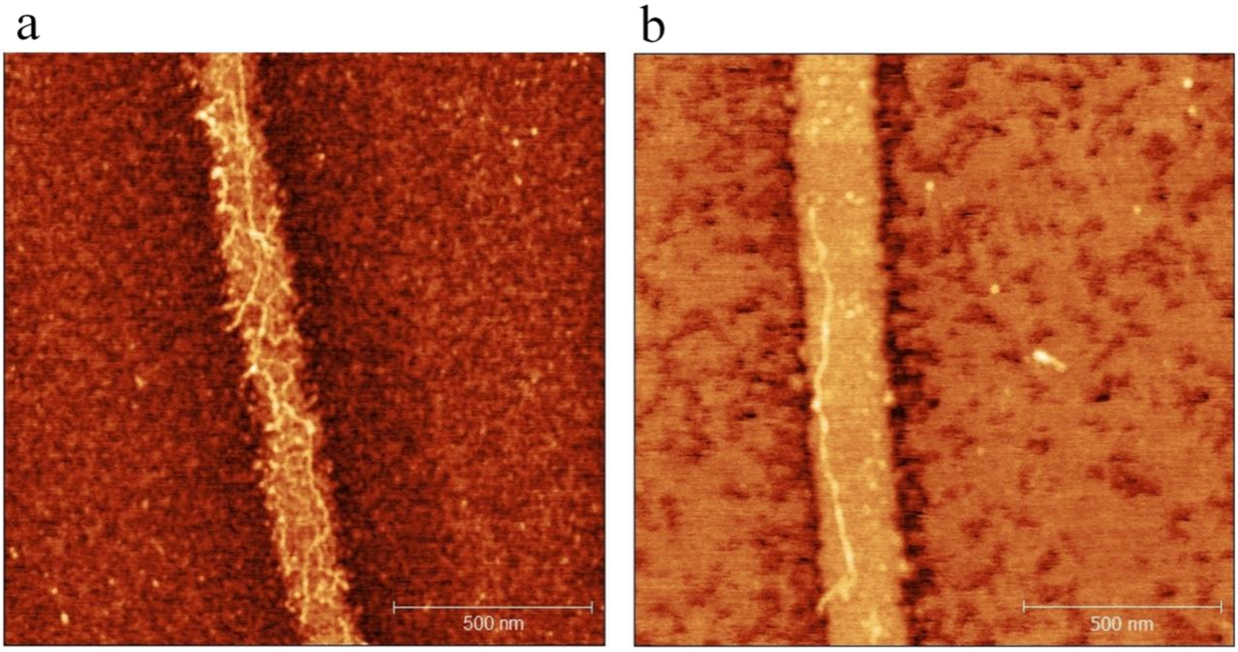

Figure 6- 5 AFM characterization of the nanopattern substrate. a) Topography AFM image of DNA deposited on a single nano stripe which performed with more concentrated DNA solution. b) AFM image of a single DNA on a single nano stripe which performed with a diluted DNA solution.

6.4 Complex nanostructure patterning

As it was described in the chapter 3, pLOx has the possibility of being used as multi step process. This ability enables us to pattern SiO_2 stripes with the variety of distance gap. Thanks to our fabrication set up, we became able to study if there is any relation between the width of the attractive stripes, the distance gap size in between, the length of DNA chain and the probability to be confined in a single adhesive stripe. In this case pLOx was performed 2 times onto the functionalized surface by HMDS. So after the first oxidation process that SiO_2 stripes growth on the substrate, the metalized stamp was lifted up and it moved slightly to approach again to the substrate and produce the second SiO_2 stripes onto the same sample (see chapter 3, section 3-3). Figure 6-6 shows the AFM image of patterned substrates with different distance gap.

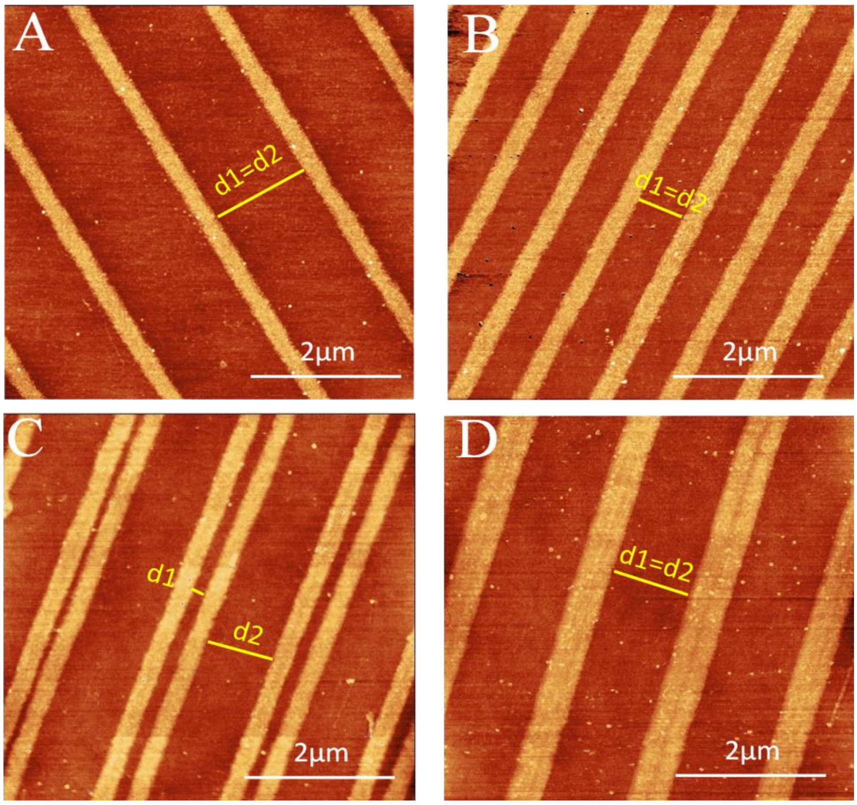

Figure 6- 6 AFM image of the nanopattern SiO_2 made by (A) one step of pLOx (distance gap of 1242nm). (B) 2 times of pLOx (distance gap of 593nm). (C) 2 times of pLOx (2 different distance gap of 141nm and 841nm). (D) 2 times of pLOx where 2 stripes are attached to each other and performed more width pattern stripes.

Table 6-1 shows the distance gap and the width of the stripes corresponding to the AFM images (figure 6-6) which were obtained by the line profile analysis (Gwyddion-www.gwyddion.net). Sample A is a patterned structure fabricated by a single pLOx which consists of stripes with 230nm width and an identical distance gap of 1242nm. Sample B is a patterned structure fabricated by two pLOx which consists of stripes with 230nm width and an identical distance gap of 593nm. Sample C consists of stripes with 230nm width and different distance gap of 147nm and 841nm. In sample D two stripes are attached to each other and create wider stripes, 450nm, with the distance gap of 1057nm. The thickness of the fabricated stripes in all cases are ~2nm.

Table 6- 1 shows the patterned nanostructures dimension (distance gap and width of the stripes)

AFM image	Distance gap/nm		Width of the stripes/nm
	d1	d2	
A	1242	1242	230
B	593	593	230
C	147	841	230
D	0	1057	450

6.5 DNA bridging

The patterned complex nanostructures on Si/ HMDS and functionalized by APTES have been used to bind linear DNA. Morphology characterization of sample A (figure 6-6) after DNA deposition is illustrated in figure 6-7.

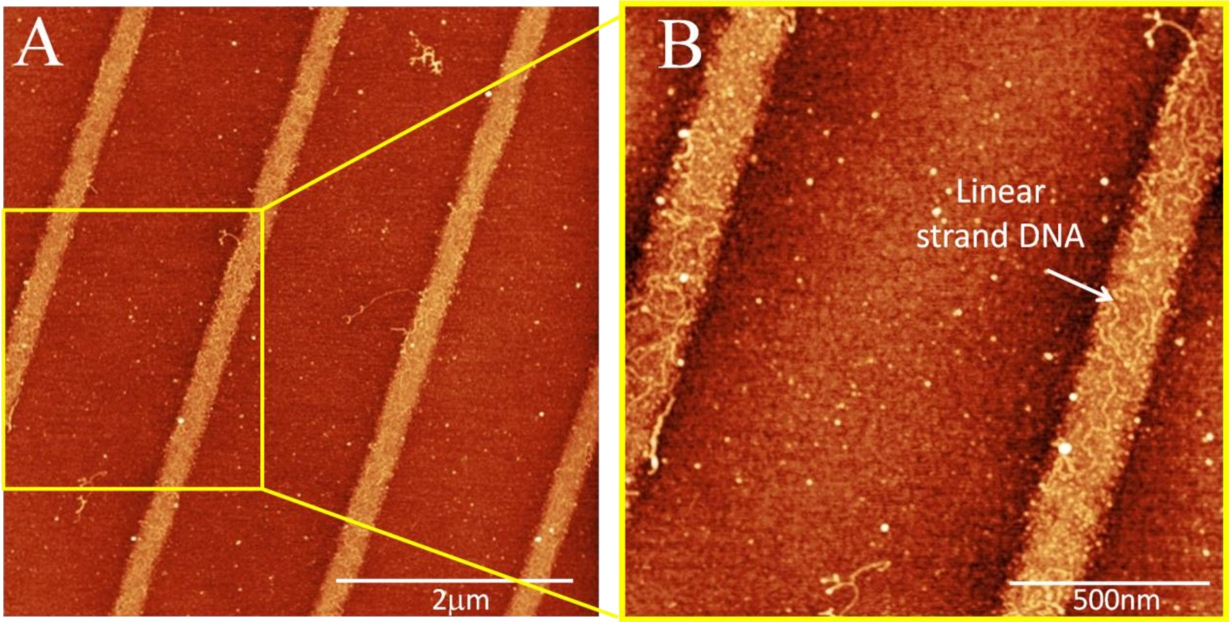

Figure 6- 7 (A) AFM image of deposited DNA on the sample with 1247nm distance gap and 230nm width. (B) Zoom of the same zone.

It is confirmed that we achieved a surface able to selectively bind DNA over a large scale and due to big distance gap, the DNA was always confined on the adhesive stripes. We confined plasmid DNA on the stripes of 200nm width and more width nanostructures of 450nm (figure 6-8).

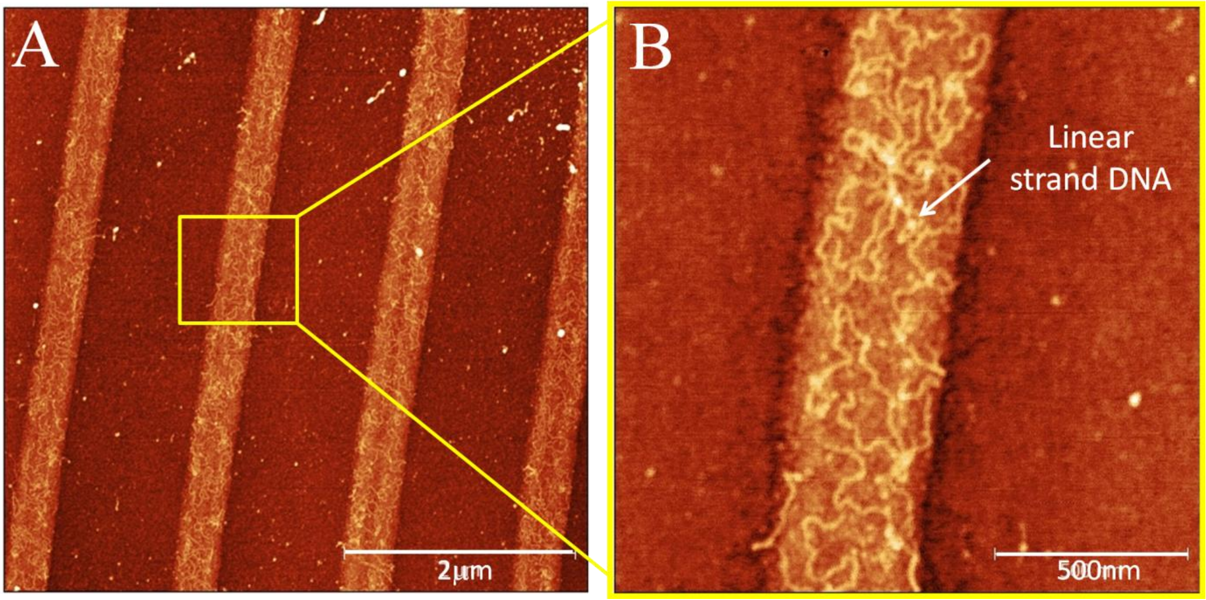

Figure 6- 8 (A) AFM image of deposited DNA on the sample with 1057nm distance gap and 450nm. (B) Zoom of the same zone .

It is noticed that for the samples with distance gaps of 147nm and 841nm, linear strand DNA 1483nm long had the possibility of bridging on adhesive structures across the antifouling areas (figure 6-9).

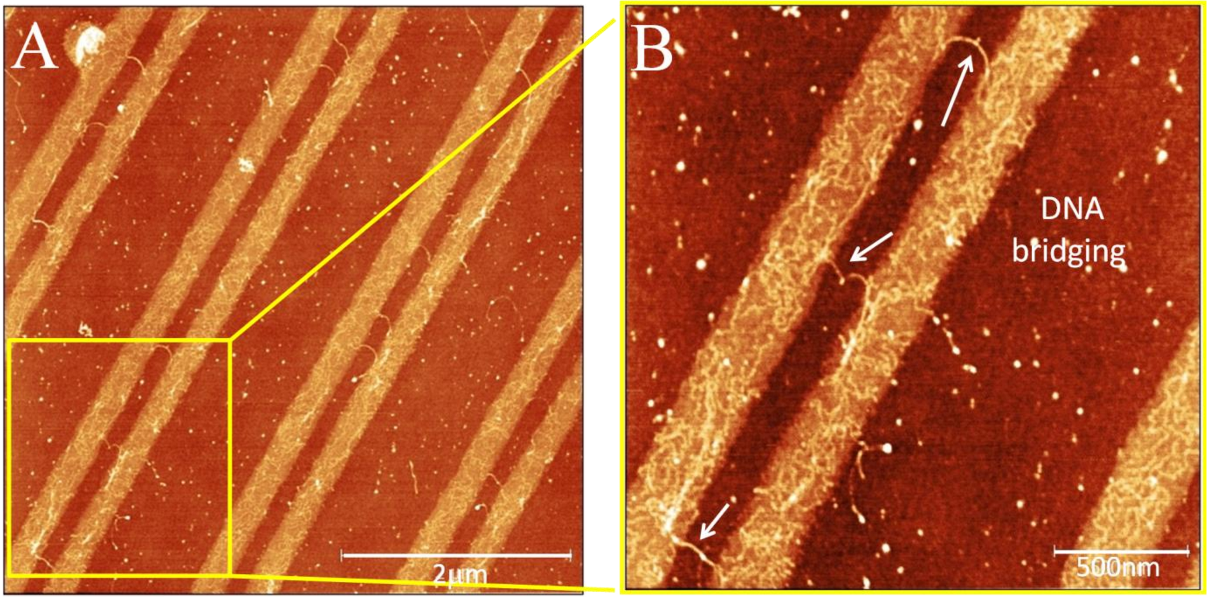

Figure 6- 9 (A) AFM image of deposited DNA on the sample with 147nm and 841nm distance gap and 230nm width. (B) Zoom of the same zone .

This is due to the fact that upon adsorbing on the surface the DNA might have an end-to-end distance that allows to two far enough portion to bind onto two different stripes, and this can take place only if the ratio of the DNA size and the stripe gap distance is sufficiently large. If the DNA bind on an adhesive surface and the rest does not encounter another adhesive area, the thermal agitation will pull the remaining part of DNA away from the antifouling region onto the stripe where it firstly bound. Figure 6-10 shows the number of bridging DNA molecules versus different distance gap. The statistic comes from counting the number of bridging DNA in 12 AFM images 5 μm X 5μm. The maximum number of DNA bridging of 2 μm^{-1} was observed with a gap distance of about ~ 150nm between attractive stripes and quickly decreasing with increasing stripe gap distance.

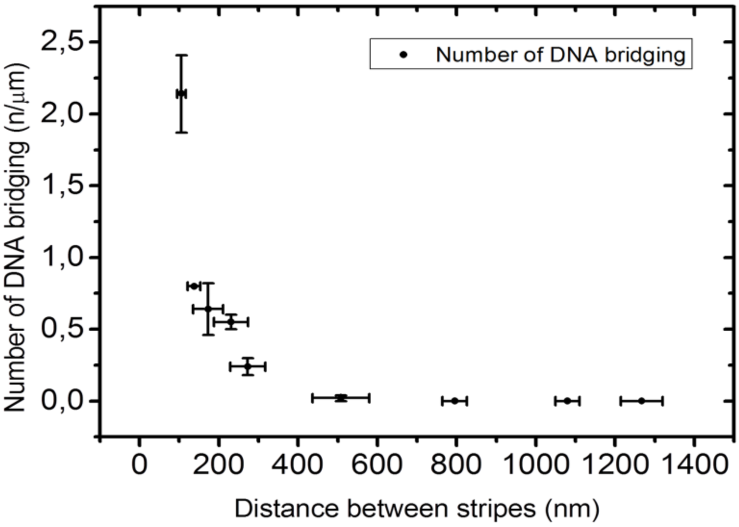

Figure 6- 10 The number of linear strand DNA bridging versus different distance gap. The error bars are the standard deviation of 10 measurements.

6.6 Conclusion

We have implemented pLOx as a nanofabrication process combined with surface functionalization to selectively position DNA molecules on substrates. We achieved a very high yield of confinement of DNA into the single stripes, with very few nonspecific binding, and a good control of the orientation of DNA in a large area up to $1cm^2$. Different patterned gaps between the attractive stripes enable us to study how DNA can form bridges according to its contour length. Our nanopatterning provide the possibility of binding also single DNA onto a single stripe of 200nm width thus opening the way to the binding of functional materials such as as carbon nanotubes or semiconducting nanowires, on the DNA scaffolds, enabling the formation of dense, ordered arrays of working devices and their connection into circuits. Moreover this process can be extended to the attachment of other biomolecules proteins and etc. for many different applications.

6.7 Experimental section

Substrate fabrication: The substrates were 1 × 1 cm^2 pieces of Si p-doped, covered with a native silicon oxide layer (Siltronic, 0.5 mm thick, orientation [100], and resistivity of $10 < \rho < 20$ Ω cm). The Si substrates were cleaned by sonication three times each for 2 min. in electronic-grade water (Millipore quality), 2 min. in acetone (Aldridch chromatography quality) then 2 min in 2-propanol (Aldridch spectroscopic grade quality). Then the substrates were heated at 80°C in a solution of H2SO4/H2O2 (3:3 v/v) for 15 min and then etched for 5 sec in 0.2% diluted HF solution. This treatment gives a hydrophilic surface and assures that the Si surface is OH-terminated. Immediately a monolayer of hexamethyldisilazane (HMDS at 99%, was acquired from Sigma-Aldrich and used as received) was deposited by exposing the OH-terminated silicon wafer to HMDS vapor (pure HMDS was kept in a thermal bath of 80°C for few hours) and transformed the surface hydroxyl (OH) groups into an inert film of $Si\ (CH_3)_3$ groups.

The patterned substrates were performed by pLOx process which was described in the chapter 3. This process assures the e-SiO_2 stripes with the width of 200nm and the height of ~ 2nm onto the functionalized silicon by HMDS.

In the last step of surface fabrication a monolayer of 3-aminopropyltriethoxylsinale (APTES at 99%, was acquired from Sigma-Aldrich and used as received) was deposited onto the e-SiO2 stripes. To prepare a 1mM solution, 2.2 µl of the starting solution was mixed with 10ml of ethanol. The back side of the substrate which was contaminated by silver pain due to pLOx process was carefully cleaned. Then the patterned substrate was immersed in the solution for 45min., then rinsed, successively in ethanol and ultrapure water and finally was blown dry with N_2. This process assures that the e-SiO_2 stripes are NH_2-terminated groups and it is a great position to drive the biomolecules.

DNA binding: Samples were obtained by depositing DNA pBR322 (E. Coli (dam+, dcm+), Fermentas, FL5SD0041, 4361 bp = 1483 nm, MW = 2.83 x 106 Da) on the patterned substrate with

NH_2-terminated groups. The initial concentration was 0.5μg/ μl in 10 mM Tris-HCl (pH 7.6) and 1 mM EDTA. About 10 μl of 5×10-2 and 5×10-3 μg/ μl DNA solution was deposited on the substrates patterned area. The samples were washed with ultrapure water and dried with pure nitrogen after 20 min.

Sample Characterization

Water Contact Angle Measurements:

The static water contact angles of the sample surfaces were measured at 25 °C in air using a contact angle meter (GBX Digidrop instrument) on the basis of the sessile drop method. All of the contact angles were determined by averaging values measured at three different points on each sample surface after each steps of surface fabrications. The volume of the DI water used for these measurements was 1μl. The equivalent diameter of the spherical droplet is presumed to be 1.8 mm in the air.

Morphological characterization.

The morphological properties of the samples have been extensively investigated by atomic force microscopy (AFM) after each step of fabrication. All the AFM images were recorded with a standalone AFM (SMENA NT-MDT Moscow) operating in air, in intermittent contact mode at room temperature with a relative humidity 55%. Si cantilever (NT-MDT NSG10, with typical curvature radius of a tip of 10 nm and typical resonant frequency of 255 KHz) were used. The topographic images were corrected line-by-line for background trend effects by removal of the second-order polynomial fitting in comparison with non- polynomial. Image analysis was done using the open source SPM software Gwyddion-www.gwyddion.net.

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CONCLUSION

In this thesis, I demonstrated the concept and application of *in-situ* fabrication of e-SiO_2 by pLOx as an unconventional lithography with spatial control at the nanoscale. This research was focused to provide novel process for nanopatterning and electronic devices fabrication by using local electrochemical methods including inorganic structures and also organic molecules as Graphene and more application in biotechnology.

Initially, I presented (pLOx) soft-lithography as a friendly and additive procedure to fabricate different types of nanostructure at the technology of silicon. The effective parameters on the procedure have been systematically studied and the optimized conditions obtained for nanaopatterning of silicon highly reproducible with superior quality. I observed that by applying AC bias the rate of oxidation process is higher than DC bias. Moreover, by applying negative bias the nanostructures fabricated by pLOx can be reduced or removed partially. Moreover, Raman spectra measurement confirmed the formation of silicon filament by local oxidation of silicon in AC mode which is one of the main issue in the mechanism of resistive switch devices.

The *in-situ* fabricated e-SiO_2 by our procedure, as an insulator layer, is used to develop novel memristor at the nanoscale. Our device which has nanojunction structure with resistive switching properties exhibits peculiar properties such as the possibility to be regenerated after being stressed or damaged and the possibility to expose the metal and the oxide interfaces by removing the top electrodes. This study proposed the formation of silicon filament by writing on device at ON state and deformation of the filaments at OFF state. Additionally, the impedance spectroscopy measurements confirmed the properties of our system in switching states by proposing an equivalent circuit which involves resistance and capacitance that in the OFF state respect to ON state has higher resistance value.

As the further application of pLOx, I demonstrated selective oxidation of Si, where graphene as building block materials acts as a template electrode. So the grown e-SiO_2 film is conformal to the graphene allows the fabrication of graphene/ SiO_2/ Si junctions as the novel devices which showed resistive switch properties. This enables us to by-pass a series of fabrication steps that often limit the application of graphene, addressing what had been a significant obstacle to the use of graphene in future generations of high-performance electronic devices.

Finally, I have demonstrated the application of pLOx combine with surface functionalization to develop novel surface architecture for binding biomolecules. In particular, our nanopatterning process provides us the possibility of positioning single strand DNA accurately onto the stripe nanostructures of 200nm width. We also showed a relation between the distance gap of adhesive nanostructures and the length of DNA, which the molecules could bridge between 2 stripes when it has a distance gap of around 150nm.

In conclusion, this work highlights the versatility and impact of nanotechnology on the performance of local oxidation in the Silicon technology and fabricating of novel electronic devices using inorganic and organic molecules. This study has also some implication for bio-engineering and bio-nano devices.

CONFERENCES AND WORKSHOPS

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- Workshop on POLIMERI DA FONTI RINNOVABILI POLIMERI BIODEGRADABILI, CNR, Area della Ricerca di Bologna Via Gobetti 101 - Sala 216, Bologna, 29 Novembre 2013.

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- “Workshop in honour of Carlo Taliani”. Organized by Professor Fabio Biscarini. Sponsor: Nikon, Organic Spintronic and Scriba Nanotecnologie2011.

PUBLICATIONS

- Francesca Lugli, Giulia Fioravanti, Denise Pattini, Luca Pasquali, M. Montecchi, Denis Gentili, Mauro Murgia, **Zahra Hemmatian**, Massimiliano Cavallini, Francesco Zerbetto, "And yet it moves! Microfluidics without channels and troughs", Advanced functional Materials (2013), (DOI: 10.1002/adfm.20130091).
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- **Zahra Hemmatian**, Stefano Chiodini, Cristiano Albonetti, Massimiliano Cavallini, Fabio Biscarini, "Template growth of Pentacene on the patterned e-SiO2 substrate", (in preparation).

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