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Size-Dependent Metal-insulator Transition in Pt-Dispersed Sio2 Thin Film: A Candidate for Future Non-Volatile Memory

Albert B. Chen
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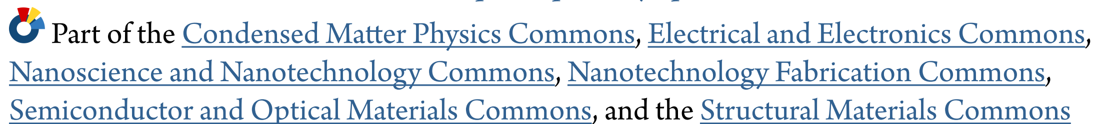
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Size-Dependent Metal-insulator Transition in Pt-Dispersed Sio2 Thin Film: A Candidate for Future Non-Volatile Memory

Abstract

Non-volatile random access memories (NVRAM) are promising data storage and processing devices. Various NVRAM, such as FeRAM and MRAM, have been studied in the past. But resistance switching random access memory (RRAM) has demonstrated the most potential for replacing flash memory in use today. In this dissertation, a novel RRAM material design that relies upon an electronic transition, rather than a phase change (as in chalcogenide Ovonic RRAM) or a structural change (such in oxide and halide filamentary RRAM), is investigated. Since the design is not limited to a single material but applicable to general combinations of metals and insulators, the goal of this study is to use a model material to delineate the intrinsic features of the electronic metal/insulator transition in random systems and to demonstrate their relevance to reliable memory storage and retrieval.

We fabricated amorphous SiO_2 thin films embedded with randomly dispersed Pt atoms. Macroscopically, this random material exhibits a percolation transition in electric conductivity similar to the one found in various insulator/metal granular materials. However, at Pt concentrations well below the bulk percolation limit, a distinct insulator to metal transition occurs in the thickness direction as the film thickness falls below electron's "diffusion" distance, which is the tunneling distance at 0K. The thickness-triggered metal-to-insulator transition (MIT) can be similarly triggered by other conditions: (a) a changing Pt concentration (a concentration-triggered MIT), (b) a changing voltage/polarity (voltage-triggered MIT), and (c) an UV irradiation (photon-triggered MIT).

The resistance switching characteristics of this random material were further investigated in several device configurations under various test conditions. These include: materials for the top and bottom electrodes, fast pulsing, impedance spectroscopy, static stressing, retention, fatigue and temperature from 10K to 448K. The SiO_2-Pt RRAM exhibits fast switching speed (~25 ns), high resistance ratio (>100), long retention time/write time ratio ($>10^{12}$), multi-bit storage and extraordinary performance reproducibility. The device switches by a purely electronic mechanism: electron trapping makes it an insulator; charge detrapping returns it to a metal. The switching voltages are low, ~ 1 V, and are independent of size, thickness, composition, temperature and write/erase time. The insulator state has a conductance that exponentially decays with the thickness.

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Size-dependent metal-insulator transition in Pt-dispersed SiO_2 thin film:

a candidate for future non-volatile memory

Albert B. K. Chen

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Professor I-Wei Chen

Supervisor of Dissertation

____

Professor Russell J. Composto

Graduate Group Chairperson

Dissertation Committee

Peter K. Davies, Professor of Materials Science and Engineering

Ritesh Agarwal, Professor of Materials Science and Engineering

Cherie Kagan, Professor of Electrical and System Engineering

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To Mom, Dad, Erik,

and my loving and ever-supportive wife, Mimi.

Abstract

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Albert B. K. Chen

Dr. I-Wei Chen

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Chapter 1 Background and Introduction

I. Amorphous Materials

An amorphous material is built upon a nonperiodic structure. It is conventionally termed “glass”, originally referring to a material that is being quenched into a solid phase without having a volume discontinuity during freezing. Amorphous solids have been discovered in all the material classes (oxide glass, organic polymer, amorphous chalcogenide, amorpohous semiconductor, and metallic glass) with every bonding type (covalent, metallic, ionic, hydrogen, and van der Waals)[1]. However, it is not to say that the atomic positions in an amorphous solid are completely randomly distributed in space (that would be a gas); the essential key point of an amorphous solid that distinguishes it from a crystalline solid is the absence of long-range order.

In an amorphous material, inborn structural defects and impurities induce disorder of electronic states. The electron wave function does not extend far and the electrons are somehow localized. Traditional band theory does not satisfactorily apply to disordered materials. The band structures are less distinct than those of a periodic system and the concept is subtle. The gap between the conduction band and the valence band often appears as a “pseudogap”, scattered with various small density of states. The near edge states are discrete and localized, usually with a very small density of state, n(E). These “tails”, which refer to the top of the valence band and the bottom of the conduction band, obscure the definition of a metal and an insulator in amorphous materials. Instead, a “mobility edge” near both bands separates the localized and non-localized states.

These findings have led to the notion of Anderson's localization, which explains the origin of wave interference between scattering paths caused by randomly placed scatters. It is this exotic explanation put forth on a single electron "diffusion" picture in a random insulator that has motivated this thesis. To set the background, the remaining part of this chapter will provide a brief overview of the experimental techniques, materials, technology, current understanding and issues that pertain to this work.

II. Sputter Deposition

Sputtering is extensively used in this work for material preparation. Sputtering is a technique of physical vapor deposition (PVD) method commonly used in industry[2,3]. The first sputtering deposition was reported by Grove in 1852. However, it was not until the development of magnetron sputtering source that sputtering deposition finally becomes popular. Sputtering process is known for its capability for large area coatings and its wide adaptability for depositing almost every kind of condensed material. A basic schematic is shown in Fig. 1. It consists of a cathode facing toward a substrate holder typically a few cm away in distance. A target composed of the depositing source material is mounted on the cathode and provided with either a constant voltage (direct current, or DC mode) or a radio frequency voltage excitation (RF mode). With a process gas (typically argon) backfilled into the vacuum chamber, a sufficiently large voltage between cathode (target) and anode (chamber or substrate) will ignite glow discharge (plasma). The ionized gas ions are pulled toward the cathode, hitting the target surface inducing ejections of target atoms and ions.

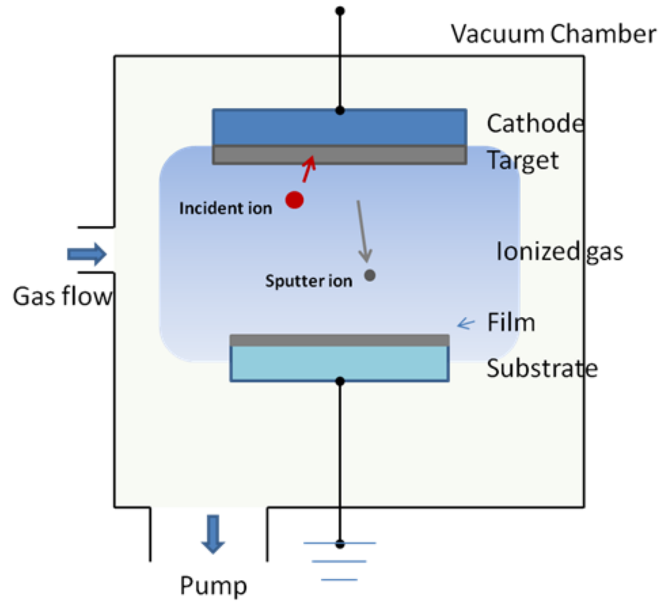

Fig. 1 Schematic of sputtering deposition

In DC discharge mode, a constant current is flowing to the cathode, which only allows sputtering of conducting materials. For deposition of insulating or poorly conducting materials, RF sputtering is required. This allows plasma excitation with no net current flow. A major difference between the DC and the RF mode is the sputtering rate: the DC mode is much faster. This is mainly due to the potential drop between cathode and anode. A high deposition rate of dielectric films can be achieved by the so-called reactive sputtering process, however. This process sputters pure metallic targets under a mixture of process/reaction gases like Ar/O_2 or Ar/N_2, which allows the formation of oxides or nitrides. However, this process requires high precision control. Otherwise, the film may not not fully oxidize if oxygen pressure is not enough, or the target may oxidize (so-called "poisoned") if the oxygen pressure is too high. Under suitable conditions, though, sputter deposition does offer the capability of high-rate film deposition for a wide variety

of materials, which is suitable for not only commercial processes but also research and discovery of multicomponent materials.

III. Non-volatile Memory

The device studied in this work is potentially suitable for non-volatile digital memory. Non-volatile random access memory (NVRAM), as opposed to volatile memory, is a solid state memory device which can hold information without power. The increasingly higher requirements for write/erase speed, storage capacity, and data reliability has motivated intensive NVRAM research to replace tradition hard drive disk (HDD) technology[4]. NVRAM has many advantages over tradition magnetic storage devices, such as fast writing/erase speed and good reliability[5,6,7]. Today, flash memory[8] is the most popular and mature NVRAM technique. The basic structure of flash memory, shown in Fig. 2, consists of four terminals: floating gate, source, drain and bulk, which constitute one bit. The floating gate acts like a regulator of the current, and therefore it defines 1 and 0 when the bit read by the drain/source. However, flash memory has not yet fully replaced magnetic memory storage devices (hard drives) and may not meet future technology demands because of its higher cost per Giga-bytes, relatively poor retention limit, slower write speed, and some scalability issues[5] .

Recently, several new NVRAM devices (as listed in Table 1) have shown promise for future memory applications. These include phase-change memory (PCRAM)[9,10], ferroelectric memory (FeRAM)[11], magnetic memory (MRAM)[12], and racetrack memory[13,14]. These next generation NVRAMs could potentially provide high scalability,

fast writing speed, long retention and low price, and they may be amenable to top-down integration of DRAM and storage systems. Resistive switching random access memory (RRAM or ReRAM), discovered in 1960s in amorphous chalcogenide semiconductors (similar or same as PCRAM) and binary oxides such as NiO[15], TiO_2[16] and SiO[17], is another candidate for future NVRAM devices. Recently, RRAM has also been studied in colossal magneto resistance (CMR) oxides and doped perovskite oxides in addition to binary oxides. Much literature exists to demonstrate RRAM's promising features such as fast write/erase speed, low cost and high density, which has in turn drawn further attention to this field[18].

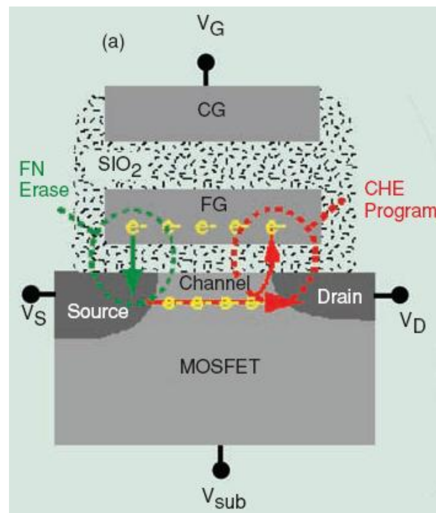

Fig. 2 Schematic of Flash memory

Table 1. Comparison of different memory devices

	Hard Drive	Flash	PRAM	RRAM
Read time	~ms	fast	fast	fast
Program Power	Non	High	Low	Low
W/E time	~ms	1μs/1ms	<100ns	<50ns
Multi-Bit	No	Yes	Yes	Yes
Cost	Low	High	Low	Low
Storage density	Low	High	High	High
Scalability	Low	Low	High	High
Endurance	Good	Poor	Good	Poor
Retention	--	>10years	>10years	>10years

IV. Resistive Switching Random Access Memory

The basic structure of RRAM consists of three layers: bottom electrode (BE), active layer, and top electrode (TE), as shown in Fig. 3. The bottom and top electrode are usually metals, and the active (e.g. an oxide) layer a nominal insulator, forming a metal-insulator-metal (MIM) structure. The significance of the resistive behavior is that this MIM structure can hold two stable resistance states: a high resistance (HR) state and a low resistance (LR) state, which can be switched back and forth by a voltage or current pulse. Typically, the cell initially has a high resistance. The set voltage is therefore defined to be the voltage when the resistance state is switched from the HR state to the LR state, and the reset voltage is defined to be the one when the LR state is returned to

the HR state. (In our device, the initial cell is a LR state, so at the set voltage it switches to the HR state, and later at the reset voltage it reverts to the LR state.) The read voltage can be applied anywhere between the set and reset voltage to distinguish the present state of the device, as shown in Fig. 4. Differing from a flash memory which has four terminals, RRAM device needs only two terminals, the top electrode itself behaves both as a floating gate and a drain, whereas the bottom electrode plays the role of both source and bulk. This simplification greatly increases the capacity of the memory device, benefiting the fabrication process and cost.

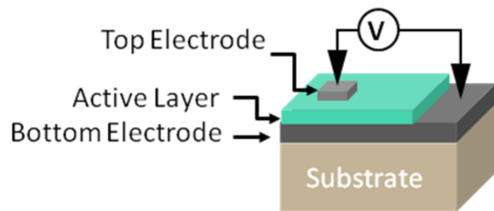

Fig. 3 Schematic of RRAM.

There are two types of switching behavior with respect to the bias polarity (i.e., positive or negative bias): unipolar and bipolar. In unipolar switching, the set voltage and the reset voltage have the same bias polarity, they only differ in magnitude. In bipolar switching, the two voltages come in opposite polarity[19]. Examples of unipolar switching are found in Fig.4(a), and bipolar switching in Fig. 4(b). Some systems, such as NiO, exhibit both: its polycrystal is unipolar whereas single crystal is bipolar[5].

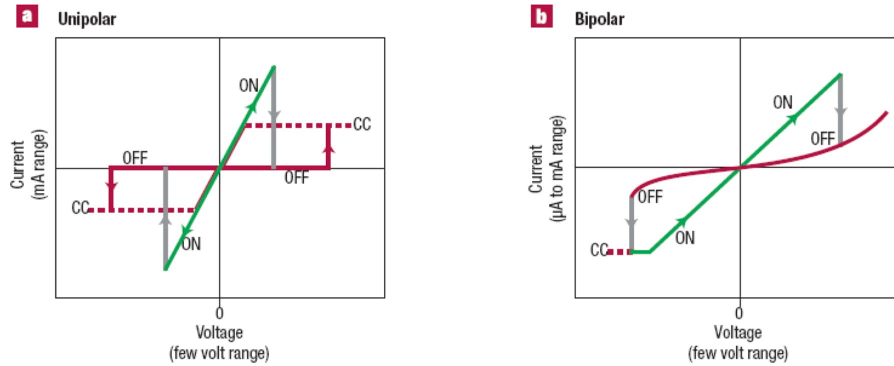

Fig. 4 (a) Unipolar switching, (b) Bipolar Switching.

A common characteristic, the so called "forming process" (shown in Fig. 5), has been mentioned in most of the RRAM literature. This process is performed in order to initiate the switching phenomenon. The as-fabricated device has a high resistance even higher than that of the HR state. During forming, a large bias (usually higher than the set or reset voltage) is applied to the as-fabricated cell and held for a certain time, during which the initial high resistance "breaks down" and the LR state is attained, after which the normal switching behavior ensues. The phenomenon is explained by field-induced ion (or metal) migration from the anode into the insulator layer forming a conducting filament[20]; this filament is subsequently broken due to Joule heating under a higher bias (unipolar) or reverse migration under a reverse bias (bipolar) thus reverting to the HR state. Some researchers explained forming in terms of the breakdown of the Schottky barrier at the interface[6].

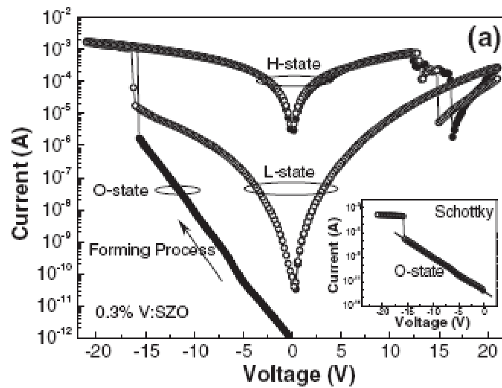

Fig. 5 An example of "forming process".

V. RRAM Materials

A. Binary oxides

Binary oxides were first investigated as resistive switching memory in 1960's. Various oxides such as TiO_2[21,22,23], NiO[24], Al_2O_3[25], ZrO_2[26], MoO_x[27], CuO_x[28], CoO[29], WO_3[30], Cr_2O_3[31] and SiO_2[32,33] have been discovered to exhibit resistive switching behavior. In recent years, most of the research has been focused on TiO_2, NiO, and ZrO_2 in the family of transition metal oxides. Oxygen vacancy migration can induce oxidation/reduction of metal cations in these transition metal oxides. The reduced (nonstochiometry) phases usually have a higher conductivity, which is the main reason for resistance switching in these materials. For these materials, both bipolar and unipolar switching can occur between electrodes of Pt, Ag, Au and Cu, and this phenomenon was mostly explained by the filamentary effect[34,35,36,37,38]. Illustration of filaments induced resisance switching is

shown in Fig. 6. They have been observed using conducting atomic force microscopy (C-AFM): conducting spots appear in C-AFM mapping when the cell is switched into the LR state, indicating conducting paths have formed during this process[34,35]. Further characterization of TEM and EDX results also showed diffusion of anode ions into active layer[36].

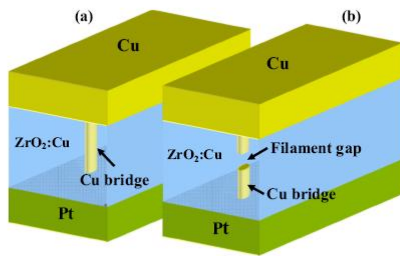

Fig. 6 Filamentary effect of a RRAM device.

For NiO, Son & Shin directly probed the conducting filaments by using a Hg top electrode[35]. The Hg electrodes were removed after switching two cells, one to HR and the other to LR. Then, C-AFM mapping reveals high leakage current in several regions when the cell is in the LR state, whereas minor leakage current was observed when the cell is in the HR state. The size and density of the filaments were then simulated by Monte Carlo calculations. The calculations were done using very small electrodes, namely nanospheres[39]. The simulated electrode diameter is as small as 10nm and switching probability was found to decreases significantly as the cell size decreases. Yoshida et al. suggested that these leakage sites were Ni deficient NiO phases[40]. A time-of-flight-secondary ion mass spectrometry (TOF-SIMS) mapping of a HR region and another LR region shows different ratio of ^{16}O and ^{18}O. The voltage-driven oxygen migration can trigger the formation of a stoichiometry NiO phase (insulating, HR state)

and another non stoichiometry $Ni_{1-\delta}O$ phase (semiconducting, LR state), as shown in Fig. 7. A study of different electrode materials effecting NiO switching performance also suggested that switching voltage is related to the contact potential between the metal electrode and NiO interface[41].

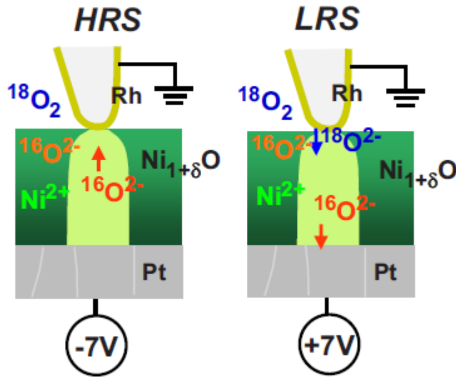

Fig. 7 Indication of oxygen migration in NiO RRAM.

In the TiO_2 RRAM device, the redox mechanism has also been proposed. Oxidation/reduction reactions near the cations site are suggested to occur at the interfaces with active metals electrodes or near the filaments inside the active layer. Insulators, in this case TiO_x[18,21,42], serve as oxygen reservoirs, and the HR state is obtained when an anode-metal-oxide layer forms between the metal and the insulator. Under an opposite bias or a lower voltage, the layer is reduced back to the metal, so the LR state is recovered. Recently, the formation and disruption of a Ti_nO_{2n-1} oxygen-deficient phase of a nanofilament form extending throughout the film was identified using high-resolution transmission electron microscopy (HRTEM) during in-situ current-voltage measurements[37]. The TEM image (Fig. 8) also revealed another crystalline phase, a Magneli phase, at the blown-out region under in-situ current voltage measurements. A

direct measurement performed on these two phases shows that the Magneli phase is more conducting than the original TiO_2 phase. Jeong et al.[43] states that the oxygen migrates to the interface between the top electrode (TE) and TiO_2, and such resistive switching can be enhanced by adding an inert metal above the TE to prevent oxygen out-diffusion. It was further confirmed by electron energy loss spectroscopy (EELS) that the oxygen atoms accumulate at the first couple layers near the interface.

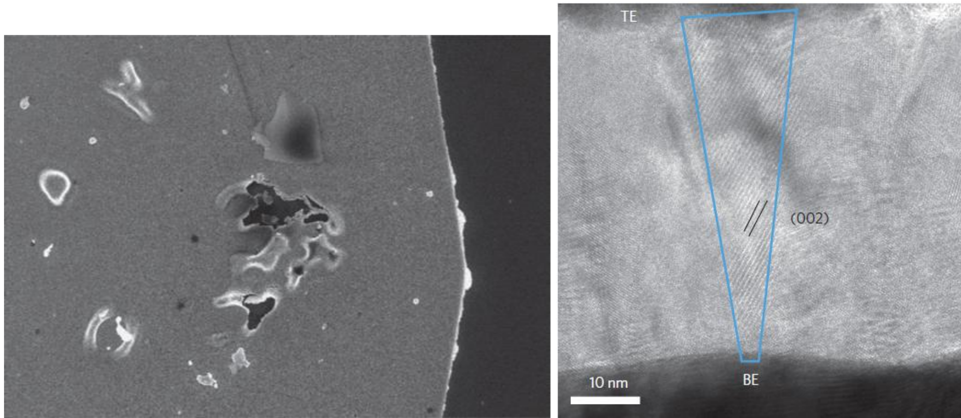

Fig. 8 Blown-out region on a Pt/TiO_2 RRAM and its HRTEM image.

A memristive switching device was reported in anisotropic TiO_2[21], as illustrated in Fig. 9. The device consists of two active layers: an oxygen rich region and an oxygen poor region, connected in series. Strukov et al. demonstrated that the resistance of the device is a function of a state variable w controlled by the boundary of the two regions; i.e., $v/i = R(w)$, and $dw/dt \sim i$. The state can be modulated by electric current to achieve atomic rearrangement, such as oxygen migration, which triggers resistance switching.

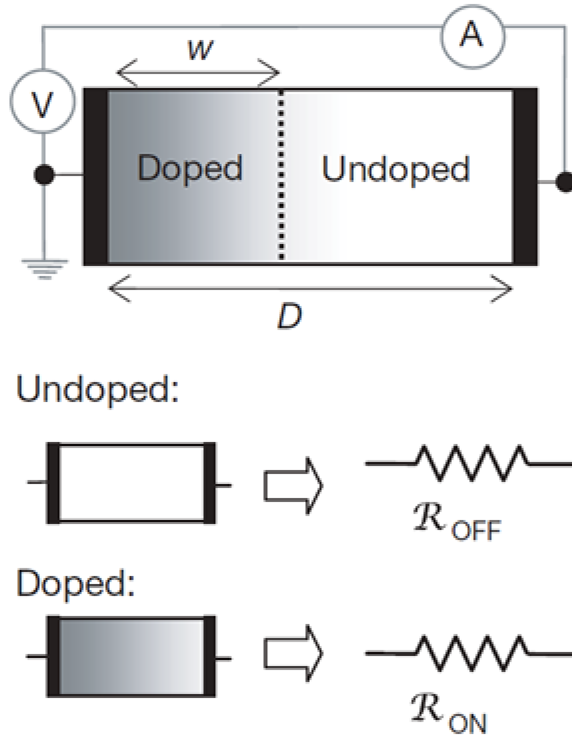

Fig. 9 Illustration of a memristive RRAM device.

Recent attention to HfO[44,45] and TaO_x[46,47] RRAM devices has also been paid in view of their outstanding endurance limit. Switching of 10^9 cycles was achieved in HfO by Lee et al.[45] and a TaO_x RRAM device investigated by Yang et al.[47] has successfully switched over 10^{10} cycles. The switching mechanism proposed for HfO and TaO_x is similar to that for TiO_2: oxygen vacancies migration creating filaments with highly conducting non-stochiometric HfO and TaO_x phases. HfO and TaO_x are known to exhibits better thermal stability[47] compare to other transition metal oxide RRAM and this is believed to be the main reason of their excellent endurance property.

In ZrO_2 films, Zr^+ ions, serving as trap sites distributed across the active layer, have been implanted to investigate the space-charge-limit-conduction (SCLC) mechanism.[48]

When the set voltage is reached, electrons are injected and they occupy the trap sites, switching the device to the LR state. A reverse bias de-traps the electrons from the trap sites, returning the state to the HR state. A structural study using X-ray photoelectron spectroscopy (XPS) on ZrO_2 supports this mechanism[49]: near the top electrode, the film is stoichiometric and has a high resistance, whereas near the bottom electrode, the film is oxygen deficient and conducting.

Another redox resistance switching material is Al_2O_3[25,50,51]. However, since Al_2O_3 is not a transition metal oxide, the redox reaction is believed to only occur at the interface, usually with the top electrode, such as Ti forming TiO_x that accompanies Al^{3+} reduction.

Another binary oxide that is not a transition metal oxide is SiO_x. SiO_x-based RRAM devices have drawn attention since 1960's[16,32,33,38,52,53] because of its CMOS compatibility in the silicon based semiconductor industry. The earliest report was that of Simmons *et al.*[16] using gold electrode on top of SiO_2. Resistance switching can be triggered after forming the device. It is believed that Au ions are driven into the SiO_2 film, creating localized states that facilitate charge trapping. Schindler et al.[32,38] and Jo et al.[52,53] reported filamentary switching in pure SiO_2 or SiO_x using low melting metal electrodes. Again, resistance switching requires a forming process in order to drive metal ions from the electrode into the dielectric layer. In the work of Yao et al.[33], cross-section transmission electron microscopy revealed Si nanocrystal formation in the SiO_x matrix. It is determined that switching takes place through the voltage-driven formation and modification of silicon nanocrystals embedded, with SiO_x serving as the source of Si along this pathway.

B. CMR materials

CMR (colossal magenetoresistance) oxides are materials that substantially change electric resistance in the presence of a magnetic field. Liu *et al.*[54] were the first to explore this type of materials for memory devices. Using a 600 nm thick $Pr_{0.3}Ca_{0.7}MnO_3$ (PCMO) thin film between a $YBa_2Cu_3O_{7-x}$ (YBCO) and a Ag electrode, they observed a switching effect by applying an electric pulse of 100 ns duration and ±5V magnitude, with a resistance change of more than 1700%, as shown in Fig.10. Electric pulse induced resistance (EPIR) switching can be achieved at room temperature and zero magnetic field. This is surprising because CMR is usually observed at not far from the Curie temperature (well below 100K in this system), and with the aid of a magnetic field. Other manganites including $La_{1-x}Sr_xMnO_3$ (x=0.3 [55], 0.33 [56]), $La_{1-x}Ca_xMnO_3$ (x=0.3 [57,58], 0.5 [59]) and $Sm_{0.7}Ca_{0.3}MnO_3$[60] have also been reported for EPIR observations, however, PCMO is still the most prominent material in CMR-type RRAM devices[61,62,63,64].

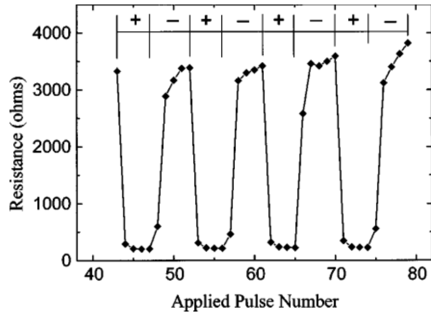

Fig. 10 EPIR switching by ±5V and 100ns electric pulse.

Several explanations have been proposed to explain the switching phenomenon in CMR materials. Originally, Liu *et al.* hypothesized a metallic cluster formation/removal mechanism[54]. However, this hypothesis suffers from insufficient evidence. Sawa later

proposed a Schottky-like barrier with a barrier height that can be altered by charge trapping at the interface[64], as illustrated in Fig. 11. This interface effect was further verified by gradually increasing the thickness of the active layer ($Sm_{0.7}Ca_{0.3}MnO_3$)[60], causing the $\Delta R/R_L$ ratio to saturated after inserting 5 SCMO layers (approximately 2~3 nm). This suggests charge trapped at the interface can raise the barrier height to form a HR state.

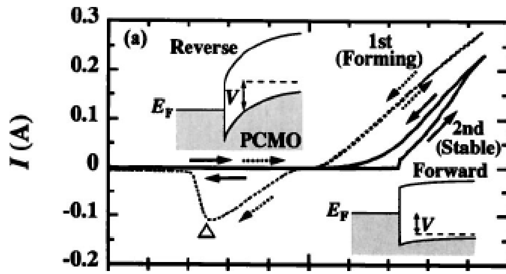

Fig. 11 Schottky-like barrier height altered by charge trapping.

Another mechanism proposed for the CMR materials is Mott transition[65]. In this mechanism, the resistance states are regulated by electron localization and de-localization. Specifically, altering the Mn^{4+}/Mn^{3+} ratio triggers a change of conduction mechanism. When electrons are localize along the $Mn^{4+} – O – Mn^{3+}$ chain, a $Mn^{3+} – O – Mn^{3+}$ chain forms and the conduction mechanism switches from double exchange to superexchange, which results in a HR state. This was supported by evidence such as the lost of resistive switching properties after inserting a $PrMnO_3$ or $CaMnO_3$ in between the PCMO layer; or the increase of Mn^{4+} concentration by oxygen annealing enhancing the resistance ratio. This suggests that the Mn^{4+}/Mn^{3+} ratio plays an important role in resistive switching in CMR materials.

Another theory for the Mn – O – Mn conduction chain considers electrochemical migration of oxygen ions and vacancies, instead of electrons[66]. As a sufficiently large negative bias drives oxygen vacancies to the interface, the Mn – O – Mn chain is broken and the layer switches to a HR state. A positive voltage drives the oxygen atoms back and switches the layer back to the LR state.

Shono *et al.*[67] suggested that, when active top electrodes such as Al and Ti are used, resistance switching is caused by oxidation/reduction at the interface. The Ti/PCMO interface was inspected by TEM and a thin amorphous TiO layer was observed as shown in Fig. 12. The HR state was achieved when a positive bias is applied to the Ti top electrode. The PCMO active layer serves as an oxygen reservoir which supplies oxygen ions to the top electrode. Further investigation of different TE shows that the switching behavior strongly depends on the TE material, and the junction resistance sequence is consistent with the Gibbs free energy for the formation of corresponding TE oxides[68].

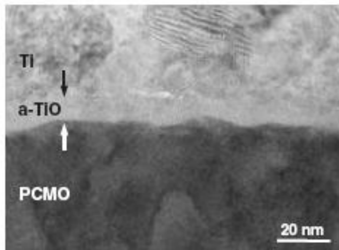

Fig. 12 Thin amorphous TiO_x layer formed between active top electrode and PCMO.

C. Doped perovskites

In addition to PCMO, other perovskite structure oxides such as $SrZrO_3$[69], $SrTiO_3$[70,71], and $(Ba,Sr)TiO_3$[72] with Cr, V, or Mo doping have demonstrated good switching properties in the past few years. The active layer usually has a thickness from 20 nm to

300 nm, and is typically grown on a $SrRuO_3$ (SRO) or $LaNiO_3$ (LNO) bottom electrode to ensure epitaxial growth. A noble metal, typically Au or Pt, is used as the top electrode.

A filamentary mechanism has also been proposed for the perovskite RRAM. Filaments consisting of electrode metals transported into the insulator under a bias form a conductive pathway which lowers the resistance. A reverse bias pushes the metal ions backward and returns the cell to its original state. Filamentary structures have been observed in samples of macroscopic size under optical microscope[71], also verified by TEM and conducting atomic microscopy (C-AFM)[73]. For such macroscopic samples, the proposed filamentary mechanism relies on oxygen vacancy migration along dislocation lines[73], as found in $SrTiO_3$ (STO) single crystals via conducting AFM and optical microscopy. The on/off state was explained by oxygen electro-migrating out/in of the conducting path, rendering Ti reduction/oxidation causing resistance changes. Spectroscopic evidence was also provided by X-ray absorption fine structure (EXAFS) data indicating oxygen atom removal during switching[71].

The Schottky barrier model has also been explored for doped perovskite. According to Fujii *et al.*[74,75] , the interface junction of $SrRuO_3/SrTi_{0.99}Nb_{0.01}O_3$ exhibits rectifying *I-V* characteristics similar to that between a high work function metal and an n-type semiconductor.

Charge carrier storage and release at defects was inspected in a Cr-doped $SrZrO_3$ single crystal by electron beam induced current (EBIC) mapping collected during scanning electron microscopy (SEM)[76]. More bright spots were revealed in the LR state, presumably associated with conducting pathways rich in defects. Here, Cr cations may

act as local trap sites, along with the intrinsic defects, forming a broad band of localized states.

D. Organic/Polymer materials

Interesting findings of resistive switching have also been reported in organic and polymer materials[77-83]. The advantages of using organic materials including polymers is the ease of fabrication, mechanical flexibility, and low cost. The earlier work reported by Ouyang *et al.*[79], demonstrated resistive switching in polystyrene film with gold nanoparticles sandwiched between two Al electrodes. More recent work in this field was summarized by Bozano et al. [78] They demonstrated that spin-coated films of a semiconducting polymer, embedded with metallic or organic nano-particles presumably allowing charge trapping at the nano-particle site, exhibit resistive switching behavior. By examining different combinations of polymer materials and nano-particles, Bozano et al. concluded that conduction is mainly by direct tunneling and that the switching characteristic very much depends on the particle size and distribution rather than the energy level of the matrix. A similar material was investigated by White et al., but in the macroscopic size [79] . A certain portion of silver nanowires was incorporated into polystyrene in the bulk dimension. It is believed that breaking/connecting of the conducting bridges between silver nanowires is the mechanism which induces resistive switching phenomenon. Kim et al. [80] using poly[(9,9-bis((6'-(N,N,N-trimethylammonium)hexyl)-2,7-fluorene)-alt-(9,9-bis(2-(2-methoxyethoxy)ethyl)-fluorene)] dibromide (denoted as WPF-oxy-F) as the polymer active layer demonstrated

stable long-term resistive switching after forming conducting filaments, presumably from the electromigration of top electrode metals. Other observations of resistance switching in organic materials [81, 82, 83] were explained in terms of the oxidation/reduction of the interface oxide layer, such as Al_2O_3.

E. Ionic conductors

Ionic conductors have also been studied for resistance switching, In this type of resistive switching memory [84-90], the metal electrode again plays an important role. Typically, a solid electrolyte is sandwiched between metal electrodes, such as Ag or Cu. With a large forming voltage, metal cations migrate towards cathode, forming a metal filament that turns on the switch. The earliest work was reported by Faraday using Ag_2S as electrolyte. However, at that time, the resistive switching behavior was relatively unstable and always required a gigantic voltage. In 2002, Mitkova *et al.*[86] demonstrated a low voltage resistive switching phenomenon using a Ge-Se electrolyte and silver metal electrodes. The device exhibits low voltage switching below 1 V and a resistance ratio well above 10^2. Since then, extensive studies following Mitkova's work have been reported in systems such as Ag-Ge-S[85], Cu-Ge-S[87], Cu-Ge-Se[86], and Ag-Ge-Se[87]. The Aono group then extended these observations into an "atomic switch" resistive switching memory[88,89,90] by incorporating a nanometer sized gap in between the metal electrode and the electrolyte. In Fig. 13, a 1 nm Ag layer was deposited between Ag_2S and Pt wires; by applying a voltage pulse for a long time, the Ag ions were ionized and then incorporate

into the Ag_2S crystal, thus creating a gap. The Ag ions can then migrate across the gap under a voltage bias, triggering resistant switching.

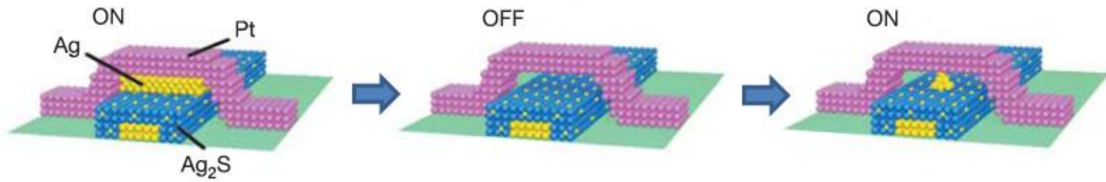

Fig. 13 Switching mechanism of an atomic switch RRAM.

VI. Summary of Switching Mechanisms

Switching mechanisms proposed in the recent literature, some of them reviewed above, can be broadly divided in two types, bulk or interface phenomenon, each subdivided into two categories, ionic or electronic mechanism. A summary of the RRAM structures and their switching mechanisms is provided in Table 1.

A. Interface/Bulk

The differentiation of interface or bulk like mechanisms can be determined by where the resistive switching behavior takes place. One method to verify interface/bulk effect is by studying switching voltage or HR/LR ratio as a function of thickness. Several reports found such effect of thickness depending on the set/reset voltage and resistance ratio, providing information on whether the resistive switching is bulk related or interface

related. Others techniques such as TEM, EDX, XPS, or EELS have been used to directly probe the resistive switching sites, such as the observation of TiO_x Magneli phase[37], or EELS analysis of oxygen concentration across the films.

Typically three types of interface mechanisms have been proposed: Schottky barrier[20,64,69,70,74], surface oxidation[91,92] , and interface oxygen migration[93].

For bulk mechanism, the most popular model is the filamentary effect [94]. This filamentary can be categorized into two types, metal ion filaments or oxygen vacancies filaments, depending on the predominant elements. Others mechanisms such as Mott transition[61] and charge trapping are also classified as the bulk type resistive switching memories.

B. Electronic/Ionic

1. Electronic

The electronic charge trapping mechanism was first discussed by Simmons and Verderber in Au-SiO_2 system[16]. Since then, it has been mainly used to explain Schottky barrier type memory[20,60,65,66,70], such as $SrTiO_3$ and $SrRuO_3/SrTi_{0.99}Nb_{0.01}O_3$, where electrons can be trapped at the interface, thus regulate the height of the Schottky barrier.

Other proposed electronic switching mechanisms such as Mott transition state that the electrons injected into certain (e.g., Mn^{4+}) sites induce electron localization thus resulting in a high resistance state[65]; conversely, the removal of electrons from the (Mn^{3+}) sites can cause delocalization, thus returning to the low resistance state.

2. Ionic

Unlike electronic mechanisms, which are specifically proposed for certain CMR or doped perovskites materials, filamentary mechanisms have been proposed for almost every kind of RRAM materials. The creation of filaments can be caused by (1) electromigration of top/bottom metal ions into the active layer, and (2) creation of oxygen vacancies or oxygen deficient phases in the active layer[94]. The former type of switching mechanism has been proposed for almost every material, since it always seems possible (indeed quite commonly observed in electronic devices such as capacitors and resistors(that conducting paths (shorts) can be created by metal electrode (Au, Ag, or Cu) ingress. Materials prone to nonstoichiometry such as TiO_2, NiO, and other transition metal oxides are more likely to exhibit type (2) mechanism by forming TiO_x or NiO_x phases that facilitate electron conduction.

Another popular ionic mechanism is redox reaction[94]. Several oxide interfaces were found to exhibit redox reactions during resistance switching at electrodes, e.g., reactions at the interface between Al top electrode and Al_2O_3 film[25,48,49]. The redox mechanism proposed for TiO_2 memristor is another example: in this case, it concerns a shifting buried interface between TiO_2/TiO_{2-x} phases.

A summary of these observations in a tabulated form is provided next.

VII. List of RRAM System

Insulator/ Active Layer	RRAM Structure	Type	Category	Mechanism	Polarity
Binary Oxides	Pt/NiO/Pt	Bulk	Ionic	Filamentary	Uni
	Au/Cr/Zr^{+}:ZrO_2 /Si[50]	Bulk	Electronic	Electron trapping	Bi
	Al/TiO_x/Al	Interface	Ionic	Redox reaction	Bi
	Pt/TiO_2/Pt	Bulk	Ionic	Filamentary	Uni
	Pt/TiO_{2-x} /TiO_2/Pt[21]	Interface	Ionic	Memristive	Bi
	Pt/MnO_x/Pt or Al	Bulk	Ionic	Filamentary	Bi
	Pt/CoO/Ta[29]	Interface	Ionic	Redox	Uni
	Al/CuO_x/Cu[28]	Bulk	Ionic	Filamentary	Bi
	TiN/HfO/TiN[44,45]	Bulk	Ionic	Redox	Bi
	TaO_x[46,47]	Bulk	Ionic	Redox	Bi
	Pt/WO_x/Cu[30]	Bulk	Ionic	Filamentary	Bi
	Al/Al_xO_y/Al[48,49] Ti/Al_2O_3/Al	Interface	Ionic	Redox	Bi

	TiN/ZnO/Pt	Bulk	Ionic	Oxygen vacancies migration	Bi
	Au/SiO/Al[16]	Bulk	Electronic	Charge trapping	
	Cu/SiO_2/W[32,38]	Bulk	Ionic	Filamentary	Bi
	Poly-Si/SiO_x/Poly-Si[33]	Bulk	Ionic	Formation of Si nanocrystals	Uni
	Ag/a-Si/Poly-Si[52,53]	Bulk	Ionic	Filamentary	Bi
	Ti/PCMO/SRO[64]	Interface	Electronic	Schottky barrier	Bi
CMR	Au/PCMO/Pt[65]	Bulk	Electronic	Mott Transition	Bi
	Ag/PCMO/Pt[66]	Bulk	Ionic	Oxygen atoms/vacancies migration	Bi
	Ti/PCMO/Pt[67]	Interface	Ionic	Redox reaction	Bi
	Ag/LSMO[56]	Interface	Electronic	Chrage trapping	Bi
	Ti/SCMO[60]	Interface	Electronic	Schotkky barrier	Bi
	Ag/LCMO/Pt[57]		Electronic	Charge injection	Bi
	Au/SRO/Nb:ST	Interface	Electronic	Schottky barrier	Bi

	O[74]				
Doped-Perovskites	Cr:STO[71]	Bulk	Ionic	Oxygen vacancy migration	Bi
	Au,Pt/STO[70,73]	Bulk	Ionic	Oxygen vacancy migration along dislocation	Bi
	Pt/Cr:SZO/SRO[69]	Bulk	Electronic	Charge carriers storage and release	Bi

VIII. Challenges for RRAM

A. Comparing unipolar and bipolar RRAM, two issues related to their operation stand out. Unipolar RRAM has an advantage in simpler system configurations, but a disadvantage in endurance and reliability. These issues are briefly described below.

B. Memory cells in an RRAM are organized in a cross bar matrix. The rows and columns in this array are called word lines and bit lines, which are connected to some circuit amplifier for reading. This type of matrix will suffer a so-called "parasitic-path-problem," when signal bypasses (or sneaks through) the cells that are already in the LR state[94,95]. In a unipolar RRAM switching device, this parasitic-path can be overcome with a diode connected in series with the RRAM

device[94], which allows current passing in one direction only. A bipolar switching device needs to operate under both polarities, making a diode not effective. In this case, a transistor need to be used to prevent the parasitic-path problem[94]. The gate of the transistor is connected to the word line, and the drain /source connected to the bit line/cell, so that the only cell operating is the one that senses the applied voltage on the gate and that allows a current to follow from the drain to the source. Unfortunately, the addition of a diode or a transistor will largely decrease the operation speed; it also lowers the storage density.

C. Although unipolar switching RRAM requires a simpler system configuration, compared to bipolar switching RRAM it suffers from poorer endurance, slower reset speed, and more switching instability. The main reason is that unipolar switching experiences continuous ion (metal, oxygen, or oxygen vacancy) movements toward one electrode in the filamentary mechanism. The accumulation of ions or their defects at one end/electrode will eventually lead to permanent breakdown/failure[96]. The switching process of unipolar switching also requires a longer switching time and a higher current because thermal effects are often required to activate filamentary switching.

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Chapter 2 Nanostructures

I. Introduction

Random materials of interest to this study are composites of finely dispersed mixtures of insulators and conductors at various length scales. These types of systems were considered by Maxwell-Garnett in 1904[1,2]. However, due to the inherent instability of composite films, fabrication difficulties were not overcome until the 1960's. Granular materials prepared by co-evaporation or co-sputtering techniques with different volume fractions of metallic particles, with a size ranging from 1-20 nm could finally be controlled. These granular materials stimulated diverse areas of interests for potential applications in microelectronics, ferroelectrics and optics[3,4]. Granular materials, their structural or electrical properties exhibiting a percolation behavior, can fall into three distinct regimes[5,6]: (1) metallic region, where the volume fraction f of the metal is larger than the percolation limit and, where metal forms a continuum across the sample; (2) dielectric region, when f is smaller than the percolation limit and each of the metallic particles is dispersed in an insulator continuum; and (3) transition region, where the metal connectivity lies between metallic and dielectric regions. Crossover through the three regions have been studied[4]. Figure 1 shows resistivity as a function of the volume fraction f in

fW-(1-f)Al_2O_3 systems[6], delineating the three regions: insulating when f<0.3, conducting when f> 0.4, and a transition region in between.

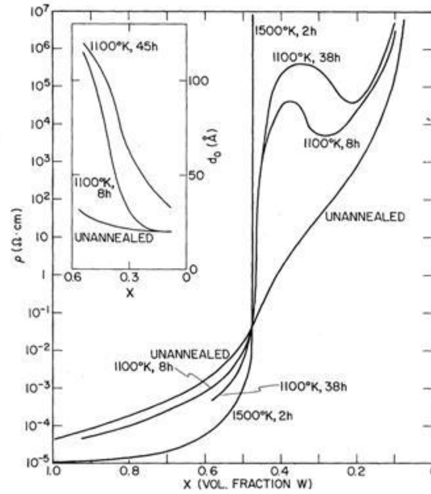

Fig. 1 Percolation of a W-Al_2O_3 granular film[6].

Studies in the transition region in 1970's have focused on metal to insulator transitions (MIT) and electron localization in disordered systems[7,8,9,10,11,12]. The materials studied included granular metals containing distinct phases, for example, some oxygen co-deposited with Al forming a thin oxide layer between metallic islands[8]. They also included amorphous solid solution such as Si co-deposited with Nb (becoming metallic above a certain concentration)[7]. They have led to important findings such as superconductivity and conduction mechanisms in disordered medium. Electron to electron correlation (such as correlation gap) and its effect on tunneling have been probed within this transition region. Importantly, these studies concern

macroscopic properties: localization of electronic states was studied in macroscopic samples and their properties were determined as a function of temperature, pressure, impurity concentration and applied magnetic field.

Unlike the above studies, our work concerns nanoscale random samples which, as will be shown in later chapters, exhibit a size effect and phase transitions entirely unforeseen by the above literature. In this chapter, we report a solid solution that consists of an atomically mixed SiO_2 and Pt mixture. (Pt is finely dispersed at the sub-1 nm scale.) The microstructure is partially confirmed by various methods including X-ray diffraction and transmission electron microscopy. The electronic carrier concentration, distributions and responses are further studied by optical spectroscopies and found to be unlike those of conventional Pt metal. Electrical measurements of macroscopic samples as a function of Pt concentration and temperature confirm the normal percolation phenomenon in these SiO_2-Pt films[4], thus setting the stage for the size effect study which will be conducted at compositions well below the percolation threshold — that is the focus of this thesis.

II. Experimental Procedures

A. Sample preparation

Highly doped p-type (100) single crystal silicon wafers with resistivity < 1 ohm-cm were used as substrates. The Si wafer was first cut into small pieces of a size approximately 4mm × 4mm. The divided wafers were next cleaned by Acetone and DI water in an ultrasonic bath for several minutes and then directly put into vacuum. The morphology (Fig. 2) of the substrate scanned by atomic force microscopy (AFM, Nanoscope IIIA Dimension, Digital Instruments, Santa Barbara, CA) showed a root mean square (RMS) roughness of about 0.75 nm, indicating a good surface flatness.

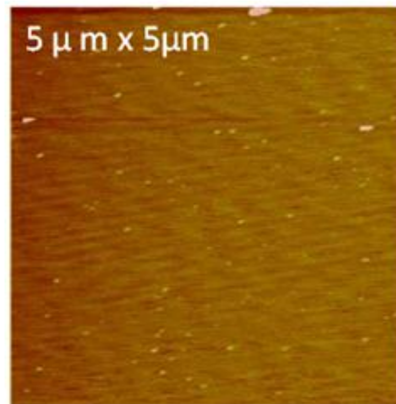

Fig 2. AFM image of a Si wafer surface showing root mean square roughness < 1 nm.

A SiO_2 target (99.5%) was used as the sputtering source operating under the Radio frequency (RF) mode. An argon gas (purity 99.999%) flow of 12 sccm was introduced to the chamber (without oxygen) during the sputtering process. The working pressure was maintained at 15 mtorr and the sputtering power was fixed at 205 W to maintain a stable deposition rate. The deposition rate on the Si wafer was measured by AFM and x-ray reflectometry (XRR, D8 Discovery, Bruker AXS, Madison, WI). Pt deposition

was made under the same RF condition and working pressure in order to allow Pt and SiO_2 co-sputtering later. The deposition rate of Pt was measured for a target bias from 45V to 85V.

Co-sputtered SiO_2:Pt films on both Si wafers and single crystal MgO (100) substrates were obtained at various compositions and thickness. By adjusting the Pt target power, mixture films of various compositions were obtained. The composition of the mixture film was calibrated using energy-dispersive X-ray spectroscopy analysis (EDX, JEOL 7500F FEG HRSEM) and Rutherford backscattering (RBS, NEC Minitandem Ion Accelerator). Here, thin films on MgO substrates were used in order to avoid Si atom over-count that would have occurred with Si substrates. The thickness of these films was around 100 nm to ensure sufficient counts in EDX and RBS measurements. The morphology and crystallinity of the film were measured by AFM and x-ray diffractometry (XRD, Rigaku, The Woodlands, TX).

B. Rutherford Back Scattering (RBS)

In RBS, a film is bombarded with particles of a known energy, and the measured intensity of backscattered particles as a function of their energy is shown, as in Fig. 3, reflects the spatial distribution of scattering atoms in the film, which vary in nucleus mass and charge. The data were then simulated by software

"SIMNRA"(Max-Planck-Institute, Germany) to acquire the number of Si and Pt atoms per cm^2. Raw data and the simulated curves were plotted in Fig. 3. The Pt atomic concentration can then be calculated by

$$\text{Pt concentration} = f = \frac{N_{Pt}}{N_{Si}+N_{Pt}} \qquad \text{Eq. 2-1}$$

where N is the number of counts of each atoms.

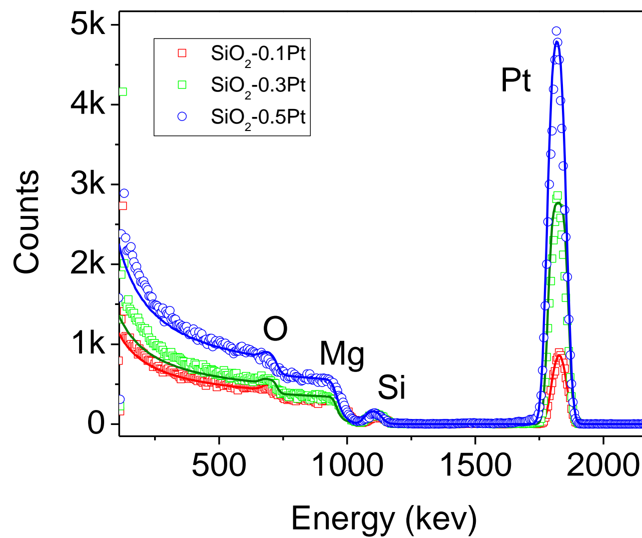

Fig. 3 Measured (symbols) and simulated (curves) RBS data of SiO_2-Pt films with *f*=0.1, 0.3, and 0.5.

C. Optical measurements

Transmission and reflection spectra in the ultraviolet-visible-near infrared (UV-Vis-NIR, 200 ~ 3000 nm) range were measured using a spectrophotometer (Varian Cary 5000 spectrometer from Agilent Technologies), and in the far infrared

range (FIR, 2500 ~ 25000 nm) by a Fourier transform infrared spectrophotometer (FT-IR, Nexus 470, Thermo Nicolet, International Equipment Trading Ltd. Vernon Hills, Illinois, USA). A calibrated Al mirror (Newport Corp., Irvine, CA) with a known reflectance spectrum was used in the reflection measurements of both UV-Vis-NIR and FT-IR, using the setup shown in Fig. 4. Fused SiO_2 was used as

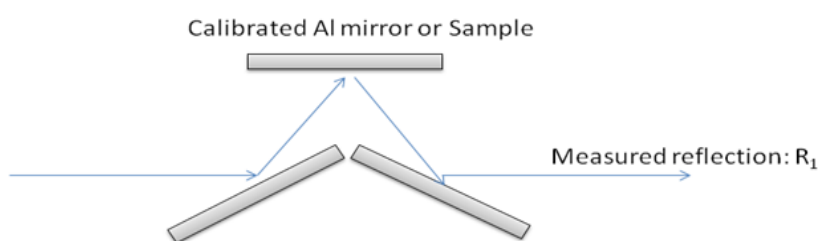

Fig. 4 Reflection measurement setup schematic.

the substrate for UV-Vis-NIR range measurements; KBr crystals (International Crystal Labortories, Garfield, NJ) were used as the substrates for FT-IR measurements. The films for UV-Vis-NIR experiments were typically 40 nm in thickness, while the films for FT-IR experiments were above 200 nm. The films thickness in the UV-Vis-NIR measurement is limited by the interference from reflections from the interfaces[13]. Single-side-polished substrates were used in reflection measurements to prevent interference and double-side-polished substrates were used in transmission measurements. The reflection data were calibrated by the following equation to obtain sample reflectance::

$$(R_1 / R_m) \times R_{Al} = R_r \qquad \text{Eq. 2-2}$$

Here, R_1 stands for the measured (raw) reflection signal, R_m for the (blank) reflection signal with the sample replaced by the calibrated mirror, R_{Al} for the reflectance of the calibrated Al mirror, and R_r for the reflectance of the sample. This method was used in order to remove the influence of the unknown reluctances of the two (uncalibrated) mirrors in the configuration. Both the transmission and the reflection data were analyzed using the simulation package -TFcompanion Thin films Optical Analysis software (RE standard version, Semiconsoft Inc., Southborough, MA)

D. Four point electric measurement

Four point measurement of the film resistance was performed by a multimeter (Hewlett Packard 3457A, Palo Alto, CA, USA). Si wafers with a 200 nm SiO_2 thermal oxide coating were used as substrates to exclude the Si wafer conductivity from affecting the apparent conductivity in the measurement. The substrates were cut into a size of 10 mm x 10 mm. A shadow mask with four electrodes, spaced at 0.79 mm from each other, was used. The measurement was performed in a Joule Thompson cryostat (JT90) from room temperature down to 90K.

E. Pair distribution function

Measurements of the atomic pair distribution function (PDF) were performed at a synchrotron (Argonne Photonic Source or APS, Argonne, Chicago, IL). These measurements used a series of 100 nm films, including Pt and SiO_2-Pt mixtures, deposited on Kapton tapes (Kapton polyimide, Dupont, Wilmington, Delaware, USA). During deposition, the Kapton tape was glued to the stainless steel stage by vacuum grease mixed with Al powder to improve thermal conductivity. The samples prepared in this way did not show any Pt peaks at 50% Pt composition, whereas the samples not glued to the stage as above showed a very weak signal of Pt peaks, as shown in Fig. 5. Measurements were collected in the transmission mode with the synchrotron source energy at 99 kV, with the radiation first calibrated by passing through a CeO_2 sample. Data were processed using a software (Fit2D) to acquire I(Q) from the raw data, then analyzed by PDFgetX2 (Dept. of Physics and Astronomy, Michigan State Univ.) to obtain S(Q) and G(r).

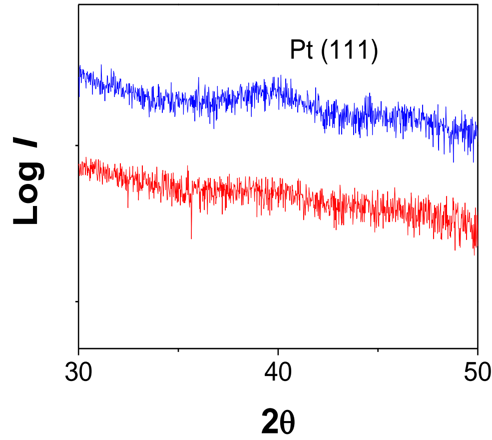

Fig. 5 XRD pattern of SiO_2-0.5Pt deposited on Kapton tape with red: Al powder vacuum grease glued to sputtering stage, blue: without glue to stage.

III. Results and Discussion

A. Morphology and crystallinity

The deposition rate of pure SiO_2 measured by AFM is approximately 2 nm/min. The diffraction pattern (XRD) of SiO_2 films shows an amorphous background with no peaks other than those of the Si substrate. Images of AFM reveal a smooth surface (roughness root mean square < 1nm) similar to that of the underlying substrate, indicating an amorphous non-granular film. Pure Pt films are polycrystalline with a somewhat (111) texture according to the XRD shown in Fig. 6 (Power = 30W, voltage=72V, deposition rate =1nm/min).

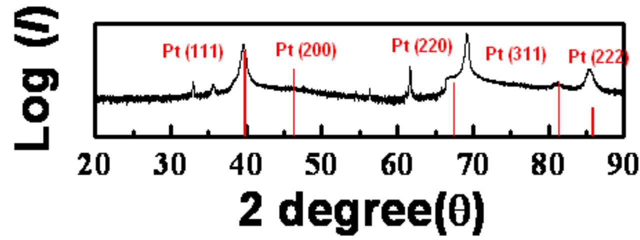

Fig. 6 Pt film on Si substrate showing only Pt peaks and Si background.

According to AFM the mixture films on Si wafer substrates have a root mean square (RMS) roughness < 2 nm, which is relatively smooth. Their composition as a function of deposition power of the Pt target was measured using energy-dispersive X-ray spectroscopy analysis (EDX, JEOL 7500F FEG HRSEM) and Rutherford backscattering, as shown in Fig. 7. In these measurements, 100 nm thick films were used to ensure sufficient counts in EDX and RBS measurements.

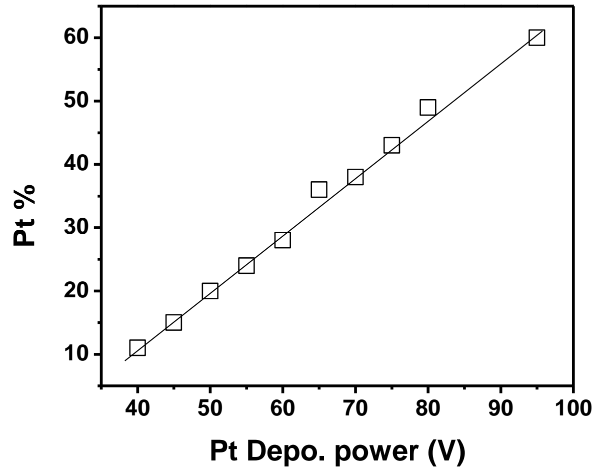

Fig 7. Pt concentration measured by RBS as a function of Pt power, under fixed SiO_2 power of 205W.

The crystallinity of the mixture films was studied by XRD, Fig. 8, which shows only reflections of the Si substrate in all cases below 50% Pt consistent with an amorphous nature. This also holds for samples before and after annealing, for 1 hr at 550°C. When the Pt concentration exceeds 50%, a weak Pt (111) peak appears[14,15], indicating crystalline Pt clusters have formed.

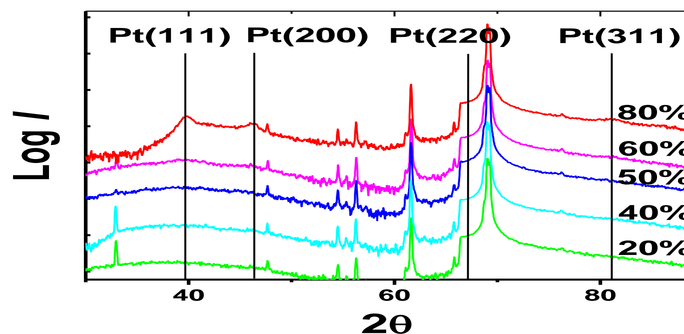

Fig. 8 XRD patterns of SiO_2-Pt with f ranging from 0.2~0.8, all sample have a thickness around 200 nm.

B. Density

Film densities measured by X-ray reflectometer (XRR) gave 4.44 g/cm^3 for a SiO_2-0.3 Pt film, versus 2.52 g/cm^3 for a SiO_2 film. (For dense SiO_2, the density should be 2.2 g/cm^3). For pure Pt, the film density decreases from 21 g/cm^3 to 12 g/cm^3 as the sputter pressure increases from 5 mtorr to 15 mtorr. Independent density measurements were also made using RBS.

Pt concentration and film density are related by the following equation:

$$\text{Film density} = \frac{(N_{Pt} \times w_{Pt} + N_{Si} \times w_{SiO_2})}{100nm \times 1cm^2} \qquad \text{Eq. 2-3}$$

for N = number of atoms, and w = atomic mass. The density measured by XRR is obtained by fitting the simulation and the data as shown in Fig. 9. (In these films, the Pt concentration is proportional to the Pt deposition power (Fig. 7). So the Pt weight fraction can be read from the power used.) These results are in agreement with the RBS concentration, as shown in Fig. 10(a). As shown in Fig. 10(b), the results are also in agreement with Abeles empirical relation for the density of random materials

$$S = S_I / [1 - y\,(1 - S_I/S_M)], \qquad \text{Eq. 2-4}$$

where S, S_I, and S_M denote the density of the mixture material, insulator, and the metal, respectively, with y being the weight fraction of the metal. The actual measured density is slightly lower than the calculated density, which, according to Abeles , is due to voids in the medium that lower the mixture density[4].

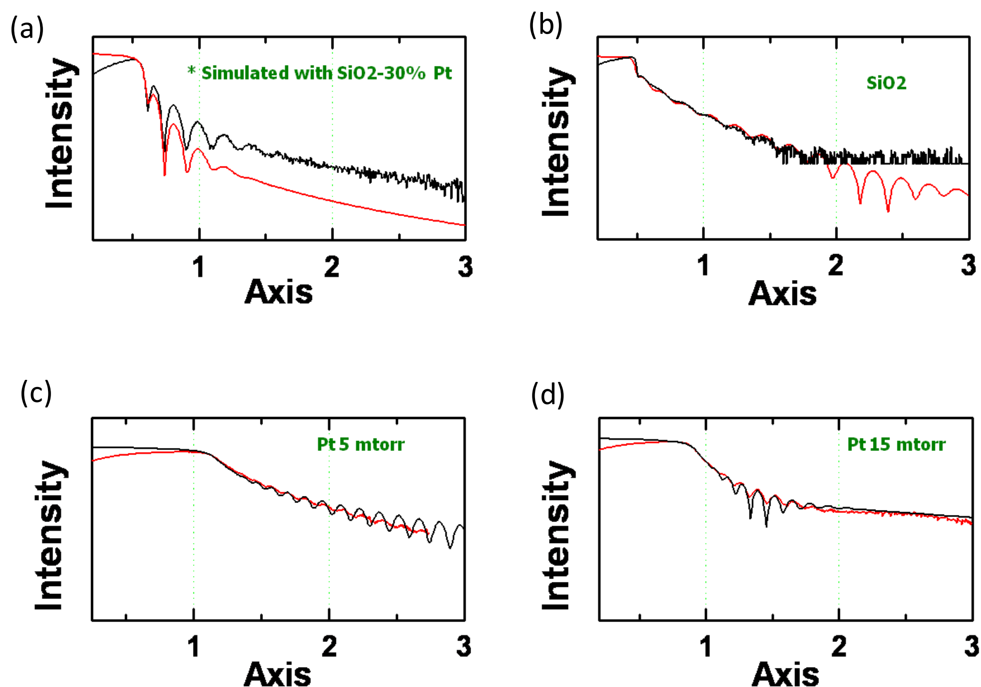

Fig. 9 XRR measurements and simulations of (a) SiO_2-0.3Pt mixture film, (b) pure SiO_2 films, (c) Pt films under 5 mtorr working pressure, (d) Pt films under 15 mtorr working pressure.

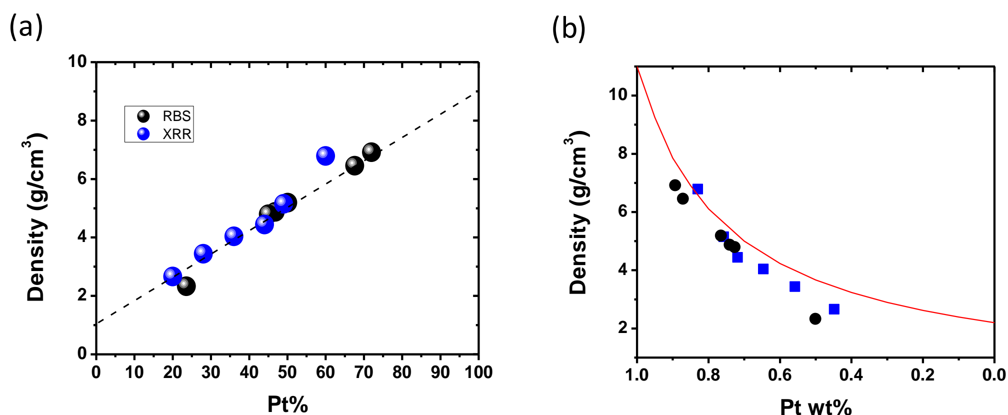

Fig.10 Density measured by RBS and XRR, (1) plotted versus Pt atomic concentration, showing linear correlation, and (2) plotted versus Pt weight percentage, showing agreement with Abeles prediction (red curve) for granular materials.

C. TEM

Nanostructure of the mixture films was examined using transmission electron microscope (TEM Joel 2010). For this experiment, a 10 nm thick layer of SiO_2-0.2 Pt was deposited onto a carbon coated TEM grid and its plan view TEM images were obtained, as shown in Fig. 11. Both in bright field and dark field, the TEM images reveal a worm-like structure with some dark regions smaller than 1 nm in diameter evident. However, no diffraction contrast of the crystalline type was found from these regions at less than 30% Pt, in agreement with other researcher's observation that the Pt particles did not show any lattice fringes when they are below 2nm in diameter[16]. The electron diffraction patterns of several regions show a set of diffuse rings that are typically seen in amorphous metals[17]. At a higher Pt concentration (f=0.3), the TEM image again reveals an amorphous background; the dark regions still lacking crystalline features.

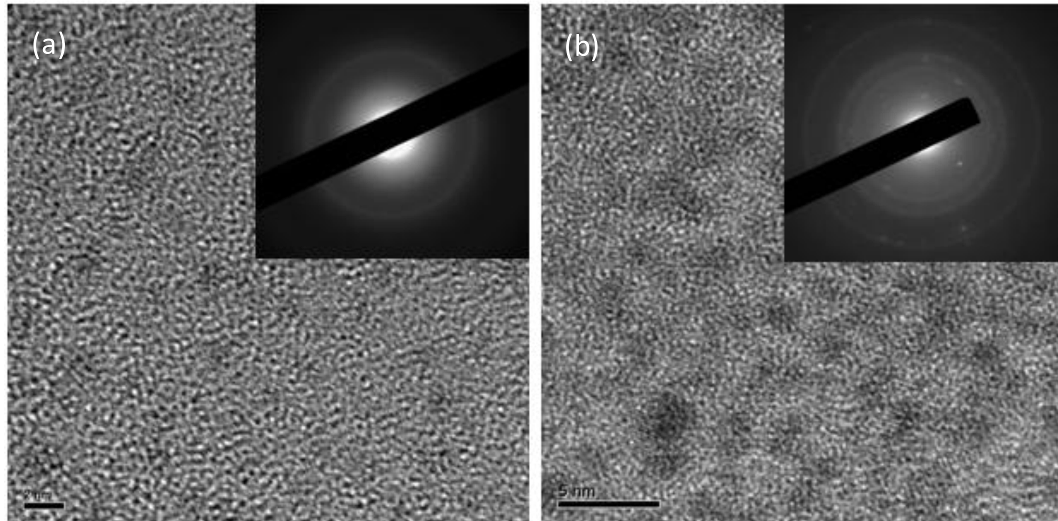

Fig. 11 Plan view TEM image (bright field) of (a) SiO_2-0.2Pt film showing worm-like amorphous structure, inset: electron diffraction pattern of the same area revealing only amorphous rings. (b) SiO_2-0.3Pt also showing amorphous structure with minor crystalline regions.

Figure 12(a) shows a plan-view scanning transmission electron microscopy (STEM) dark field Z contrast image of a SiO_2-0.2Pt film. The white dots having a diameter around 1~2 nm can be identified with Pt-rich regions, although the contrast is not as sharp as those of (Au) nanoparticle systems[18,19]. Similar white regions are seen in the image of a SiO_2-0.3Pt film. Although the density of the white regions is higher, surprisingly each region appears to be of a similar size (~ 1nm) as the one in the other film.

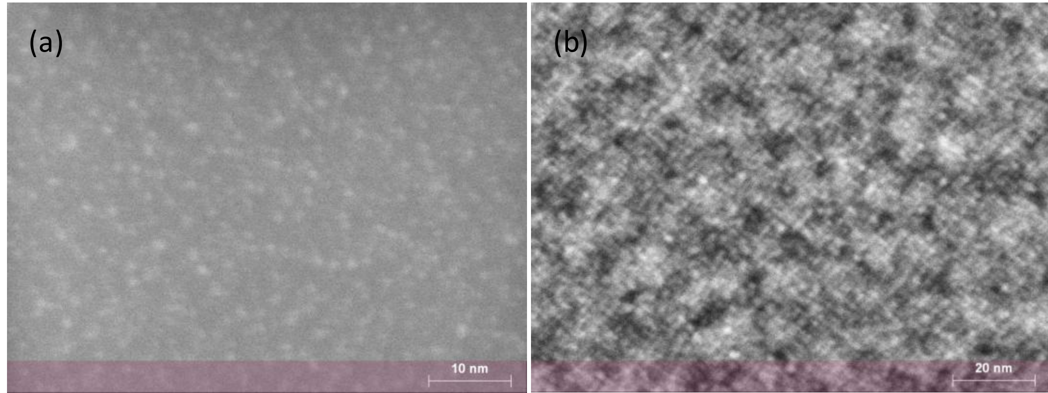

Fig 12. Z-contrast (dark field) by STEM of (a) SiO_2-0.2Pt film, and (b) SiO_2-0.3Pt film.

D. Optical measurements

1. Plasmon resonance

Optical measurement has been commonly used to identify metallic nanoparticles in various nanoparticle systems. The excellent sensitivity of this technique comes from the plasmon resonance of metallic particles, which can be detected against a large non-resonant background even at low particle concentrations such as the ones encountered in nanoparticle suspensions. Because of the large sample volume the light beam travels, this technique also provides statistically meaningful information over a large region. Since amorphous Pt (metallic glass) is still metallic, it is possible that Pt-rich clusters in our films are metallic without being crystalline. Such metallic clusters, if they exist, will decisively impact the electric conductivity of our films.

Therefore, it is important to ascertain whether they are metallic or not using optical measurements.

The Maxwell-Garnett (MG) model was first used to simulate the transmission and reflection data. Dielectric functions of bulk SiO_2 and Pt were used as input parameters for the simulation, and Pt is assumed to behave as bulk-like metallic particles embedded in the SiO_2 matrix, giving rise to a surface plasmon resonance (describe by the Mie theory) in the UV range. According to the Mie theory, the polarizability of an isolated particle with a dielectric function ε, embedded in a matrix with a dielectric function ε_m, has an effective polarizability

$$A = 4\pi e_o R^3(\varepsilon - \varepsilon_m)/(\varepsilon + 2\varepsilon_m), \qquad \text{Eq. 2-3}$$

Resonance then occurs when the polarizability is infinite, which is possible if $\varepsilon<0$, which only happens for metallic particles for a radiation energy below the plasma edge. The MG model was used in order to account for the interparticle interactions and particle aggregation, which are not considered in the Mie theory. Indeed, in our simulation a surface plasmon resonance peak appears at around 300 nm in Fig. 13. This peak red-shifts to higher wavelengths at higher Pt concentrations,[20,21] because of (a) aggregation of metallic clusters causing a broadening of the plasma resonance, and (b) particle-particle interaction. The simulation also finds that the peak appears at all concentrations, even at f=0.05, indicating that the resonance is a strong effect that

would be difficult to miss.

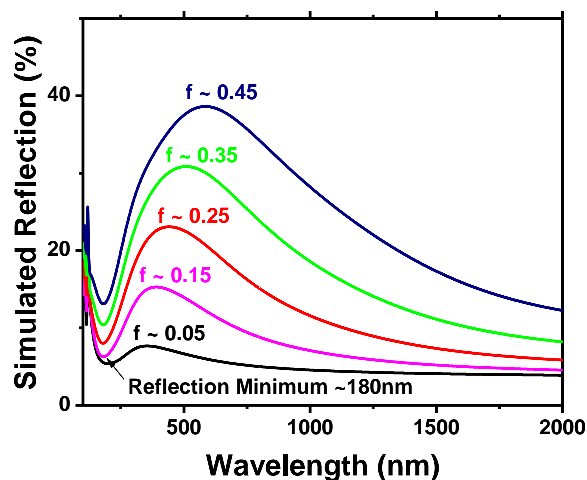

Fig. 13 Optical simulation done by TFcompanion showing metallic nanoparticle surface Plasmon resonance peak around 300nm.

For comparison, the data from our films, shown in Fig. 14, also contain well defined surface plasmon peaks at around 300 nm, and as predicted they red-shifts to longer wavelengths at higher Pt concentrations. However, at Pt concentrations below 0.3, the peak suddenly disappears. This can only be interpreted as the absence of metallic nanoparticles, which exist at f>0.3 but not at f<0.3. (Metallic nanoparticles here refer to particles that share the dielectric function of bulk Pt.) This provides the strongest evidence that the Pt-rich clusters in SiO_2 are not metallic in the conventional sense. In other words, such low f films are "optically" amorphous since metallic Pt would have been resonating.

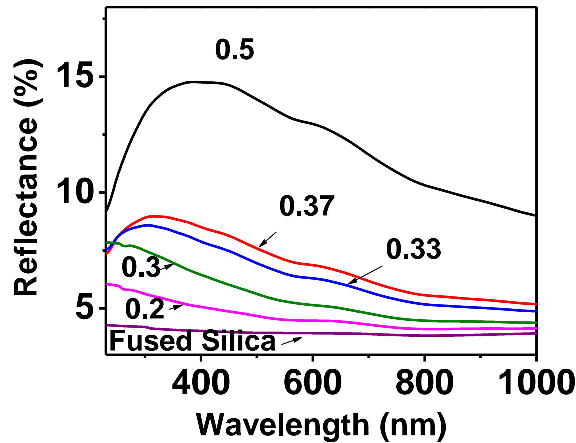

Fig. 14 Optical measurements (UV-Vis) of SiO_2-f Pt with f ranging from 0.2 ~0.5. Surface Plasmon resonance peak appearing after f=0.33 indicating formation of nanoparticles.

2. Optical conductivity

Although UV-vis spectroscopy did not reveal metallic features at low Pt concentrations, it is still possible that Pt does provide mobile carriers that contribute to DC conductivity, which is the subject of the study in the next section. This is because UV-vis measurements pertain to high frequencies,so they do not exclude DC (and quasi-DC electric measurements performed in our work scanning over a voltage range at a frequency less than 1 GHz) conductivity. If so, the electrons provided by Pt may still form a Fermi gas, albeit with very low carrier concentrations. The electron oscillations of this Fermi gas in the background of (positively charged) nuclei are like plasma excitations and are usually described by the Drude model, but here the plasma

edge is downshifted from the UV range (for the high density Fermi gas of Pt metal) to the IR or far IR range due to the low electron concentration. In Fig. 15, the optical measurements in the IR range confirm this expectation: they show SiO_2 vibration modes with a superposed Drude-like electron response, which appears as a background that increases with wavelength.

The FT-IR data were simulated by including (a) the vibrational modes of amorphous SiO_2, which are described by a Lorenz model, and (b) a Drude tail according to the Drude model, which contributes to the background. To fit the data of the pure SiO_2 film, three Lorentz oscillations (equation 2-4) corresponding to the three peaks in Fig. 15 were used. These are the stretching mode (~9,500 nm), bending mode (~12,500 nm), and rocking mode (22,500 nm), respectively. The Drude tail corresponding to the free electron contribution to reflectivity of Fig. 15 was fitted using the Drude formula (equation 2-5) for the dielectric function, $\varepsilon = 1 - \omega_p^2 / \omega (\omega + i/\tau)$, where ω_p is the plasma frequency that can be used to determine the carrier concentration (proportion to ω_p^2).

Lorentz Model

$$\varepsilon(E) = 1 - \frac{E_r^2}{E^2 - iE/r\Gamma} + Ae^{-i\theta}\left(\frac{1}{E+E_0+i} - \frac{1}{E-E_0+i\Gamma}\right) \qquad \text{Eq. 2-4}$$

Drude Model

$$E(w) = 1 - \frac{E_p^2}{w(w+i/T)} \qquad \text{Eq. 2-5}$$

The fitting results are summarized in Table 1. Both plasma frequency and carrier concentration increase as the Pt concentration increases. The carrier concentration is around $10^{17}/cm^3$ indicating that the SiO_2-Pt film is more like a sparsely doped semiconducting material than like a conventional Pt metal (its electron density = $10^{22}/cm^3$)[22]. This contribution is responsible for the increase in the IR reflectivity (>20,000nm), in a Pt concentration-dependent manner, in Fig. 15. (Note the stretching mode remains constant.)

Some representative values of the fitted parameters are: for a film of f=0.2, the fitted plasma energy of the mixture film is about 0.053 eV, associated with a plasma frequency f_p of 1.6×10^{13}/s, with a carrier (free electron) concentration about $8.4\times10^{16}/cm^3$. These plasma frequency and the carrier concentration are too small compared to those of metallic Pt meaning the optical conductivity[23] in the Drude tail cannot give rise to any surface plasmon resonance in the UV-Vis region in Fig. 15. Indeed, the film at lower wavelength (< 10,000 nm, or higher frequency) behaves like SiO_2[24]. The carrier concentration and the associated plasma energy increase with Pt concentration, as shown in Fig. 16.

Combining results from UV-Vis and FT-IR, we deem the SiO_2-Pt glasses as insulating at high frequency but conducting at low frequency. In other words, the low-Pt material behaves like a transparent conductor, with a transparency edge in the IR range.

However, as will be shown in the next section, even the low frequency conductivity only survives in the nanoscale. Therefore, it is a conductor only in the sense of its response to optical excitations, and not in the measurements that probe longer transport distances.

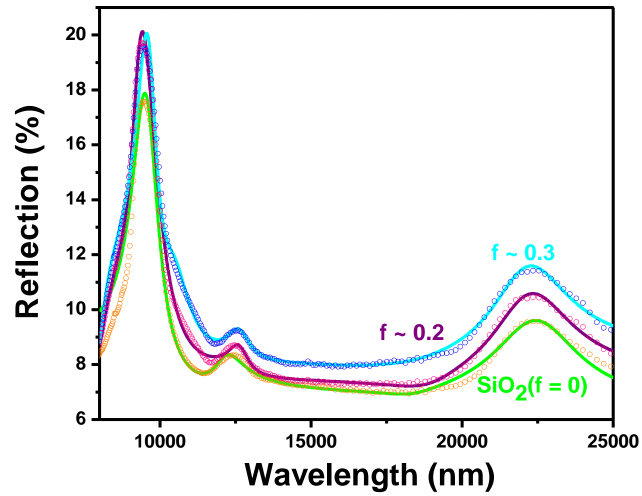

Fig. 15 Optical measurements (FT-IR) and fitting results of SiO_2 and SiO_2-Pt films showing three SiO_2 oscillation modes and a Drude tail at the far end.

Table 1. FT-IR measurements and fitting results of various SiO_2-Pt films.

Sample ID	Deposition condition (SiO_2: 205W)	Thickness (nm)	E_p^2/A^* (eV)	Carrier Concentration ($1/cm^3$)	Deposition rate (nm/min)
S185	205W	179	0	0	1.98
SP238	Pt: -45V (f~0.2)	334.4	0.5277	8.4E+16	3.7
SP222	Pt: -50V (f~0.25)	191.26	0.7171	1.325E+17	3.13
SP239	Pt: -55V (f~0.3)	375.33	1.039	1.467E+17	4.155
SP172	Pt: -54V (f~0.29)	251.5	1.254	2.08E+17	2.24
SP282	Pt: -60V (f~0.33)	229.07	0.878	1.465E+17	4.242
SP240	Pt: -65V (f~0.37)	435.63	1.265	1.529E+17	4.823
SP246	Pt: -65V (f~0.37)	442.49	1.279	1.686E+17	4.9
SP168	Pt: -67V (f~0.39)	189.4	1.374	2.957E+17	2.6
SP247	Pt: -75V (f~0.45)	484.58	1.487	2.085E+17	5.365
SP170	Pt: -88V (f~0.55)	188.8	1.666	3.412E+17	3.78

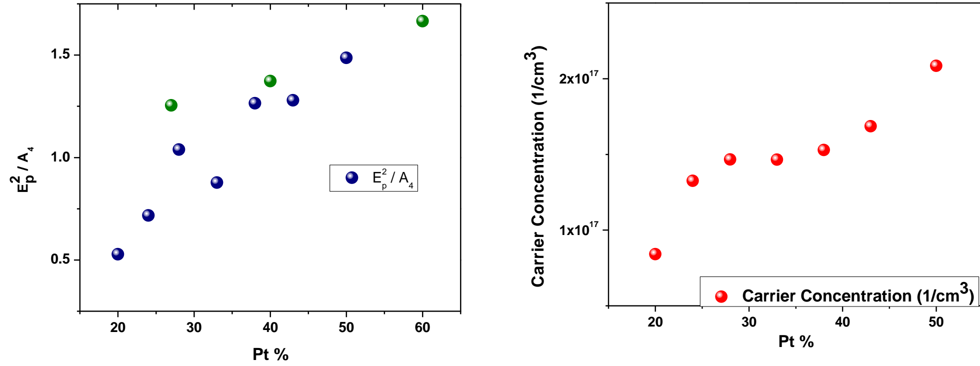

Fig. 16 (a) Plasma frequency and (b) carrier concentration obtained by simulation and fittings to FT-IR measurements.

E. Four point measurements: Percolation threshold

The resistivity ρ of the SiO_2- f Pt mixture films measured from f =0.2 to f =0.8 is shown in Fig. 17(a). The resistivity is calculated by

$$\rho = 4.5324 \text{ x } t \text{ x } (V/I)\ f_1 \text{ x } f_2 \qquad \text{Eq. 2-6}$$

with t representing the film thickness, and f_1 and f_2 representing the correction factor related to the size of the sample and the distance between probes. The resultant ρ decreases from 322 Ω-cm to 10^{-3} Ω-cm as f increases from 0.2 to 0.8 undergoing a transition at approximately f=0.4. The overall trend is very similar to the one exhibited by the resistivity measured in other unannealed disordered granular systems[25,26].

To more accurately locate the composition at the metal-insulator transition, the temperature coefficient of resistivity (TCR) was also measured down to 90K. The f =0.3 film shows a negative TCR, indicating that this mixture film is an insulator. The films with f =0.4 and f =0.45 both show positive TCR (the TCR of the f=0.4 film is very small) indicating that the percolation limit has been reached and the mixture films are now metallic. Similar evidence was found in 2 point current-voltage measurements. In Fig 17, both f =0.36 and f=0.28 film shows non-ohmic behavior, whereas the f =0.49 films show ohmic I-V behavior. These results indicate that the (bulk) percolation limit of the SiO_2-Pt film is around 40% of Pt, similar to the reported percolation limit for this system [26].

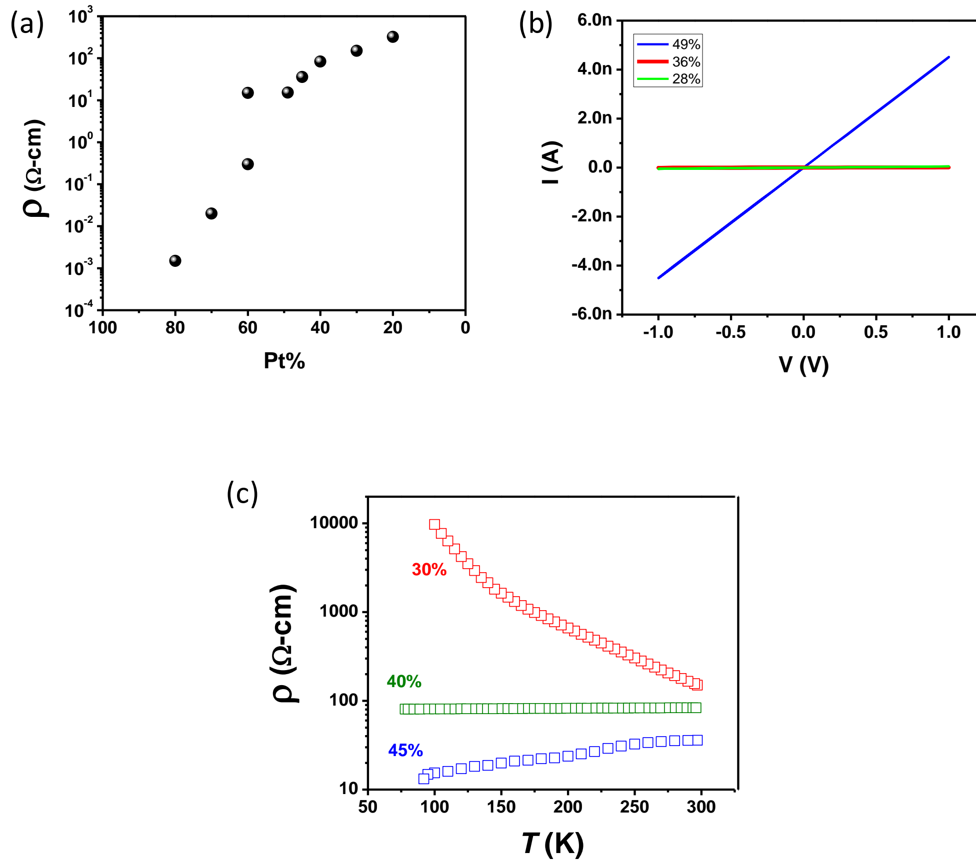

Fig. 17 (a) Four point resistivity of SiO_2- f Pt with f ranging from 0.2 ~ 0.8 showing a change of more than 5 orders of magnitude, (b) two point I-V measurement showing percolation between f=0.49 and f=0.36, (c) four point temperature dependence measurement showing metal to insulator transition around f=0.4.

F. Pair distribution function

All-atom pair distribution functions (PDF)[27,28] were investigated in order to probe the Pt structure. The PDF of a Kapton tape was first measured for calibration. The measurements were performed twice for 600 seconds each, and the data were averaged. Next, a Kapton-backed 100 nm Pt film was measured. The measured

signals were normalized by the beam counts per minute, then the Kapton tape signal was subtracted from the normalized signal to obtained the signal of the film material. After processing, the intensity as a function of Q is plotted in Fig. 18, showing strong peaks. The d-spacing of these peaks can be obtained by conversion using

$$d=2\pi/Q, \text{ where } Q = 4\pi\sin\theta/\lambda \qquad \text{Eq. 2-7}$$

They are listed in Table 2 for the first five peaks. From these data, the lattice parameter calculated is around 3.94 A, which is close to the ideal Pt polycrystalline phase[29].

After that, S(Q) was processed by software "PDFgetX2" to normalized the background, substrate absorption, and fluorescence. Then by Fourier transform, the data were converted to the atomic pair distribution function, G(r), using equation 2-8, which provides information about the spacing between Pt atom and its neighbors: G is the number of atoms in a spherical shell of a unit thickness at a distance r from a reference atom. This function is plotted in Fig. 14(b) for Pt.

$$G(r) = \frac{2}{\pi}\int_0^{\infty} Q[S(Q) - 1]\sin(Qr)\,dQ \qquad \text{Eq. 2-8}$$

Next, a 100 nm SiO_2-20%Pt was measured. Unfortunately, after (Kapton tape) background subtraction, there was almost no signal left (Fig. 18(a)); G(r) did not reveal any correlation that can be definitely associated with a Pt crystal. (The main oscillatory feature in G(r) is due to the fourier component of the (only) peak in Fig,

18(a), at 3 A^{-1}. Assuming this peak is real, it can be due to the first or the first two coordination shells of either a crystalline Pt or an amorphous Pt. Because of poor resolution it is not possible to further differentiate the two. Therefore, this experiment is inconclusive regarding whether the SiO_2-20%Pt film is crystalline or amorphous.

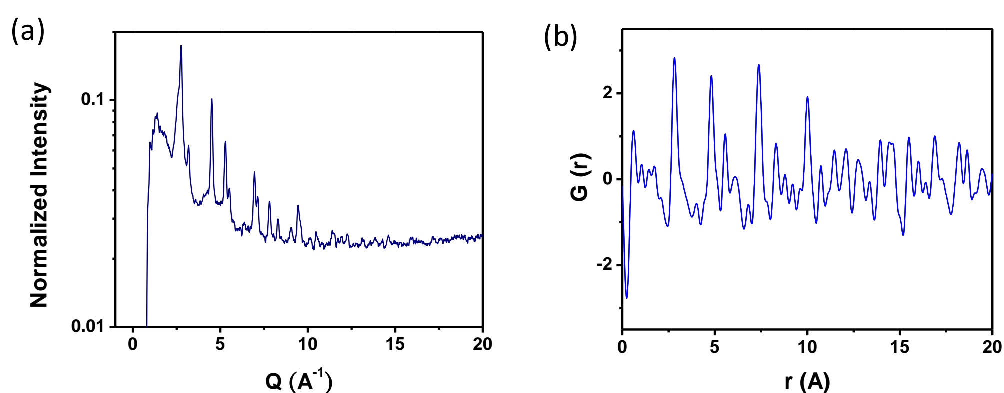

Fig. 18 (a) Calibrated Intensity of 100nm Pt films, (b) Atomic PDF G(r) showing Pt regular d-spacing.

Table 2. Calculation of D-spacing and lattice parameter of the first 5 peaks.

Q (nm^{-1})	27.526 (111)	31.865 (200)	44.174 (220)	52.897 (311)	55.198 (222)
D-spacing (A)	2.28	1.97	1.39	1.19	1.14
Lattice parameter (A)	3.95	3.94	3.93	3.95	3.94

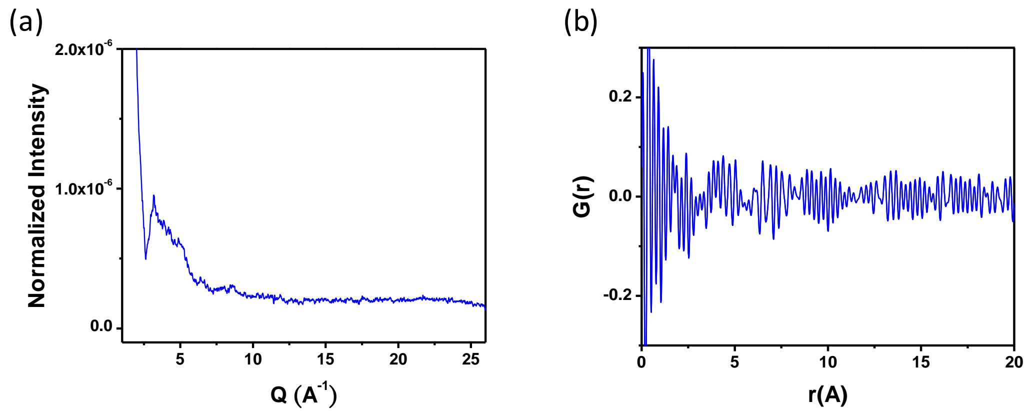

Fig. 19 (a) Calibrated intensity of SiO_2-0.2Pt films of 200nm and, (b) Atomic PDF G(r) showing no ordering of Pt phases.

IV. Conclusions

1. We have successfully fabricated amorphous SiO_2-Pt mixture film with a co-sputtering technique.
2. The bulk properties of the mixture film have a percolation type of behavior similar to those granular materials reported by Abeles.
3. The density of the film fits well with Abeles' empirical equation for other types of (porous) granular materials. XRD, TEM and PDF evidence does not provide evidence that the films at low Pt concentrations ($f < 0.3$) contain any crystalline Pt.
4. More importantly, optical measurements reveal that Pt atoms in SiO_2 do not provide any characteristic metallic (plasmon) oscillation when Pt

concentration f is less than 0.3. However, at low Pt content, increasing f causes an increase in the Drude tail of the far IR background, indicating increasing carrier concentrations albeit still at a very low level ($10^{17}/cm^3$).

5. These results suggest that the film is porous, the Pt is relatively uniformly dispersed at the atomic level, the low-Pt-content film is macroscopically insulating, but optically (far IR) and probably nanoscopically conducting, which fits the schematic picture of Fig. 20 and Anderson's picture of a random insulator with a finite "diffusion" length to be described in the remaining part of this thesis.

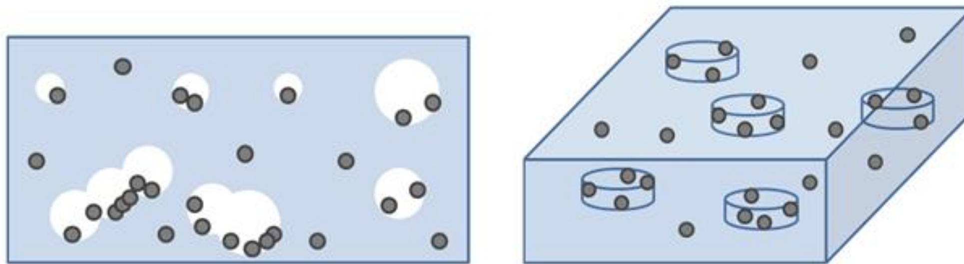

Fig. 20 Illustration of a cheese-like structure of mesoporous SiO_2 film with Pt dispersed inside and outside the pores.

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Chapter 3 Composition and the δ-*f* Map

I. Introduction

In the preceding chapter, we discussed the electronic and structural properties of random materials. Unlike insulators and conductors with a periodic structure, which can be readily distinguished by their distinctly different band structures, the band structures of insulators and conductors in random materials are less well defined. In a doped semiconductor crystal, narrow bands formed by impurity centers disturb the band structure of the undoped crystal. Electrons at these impurity centers are localized, and they form discrete energy states within the band gap. These localized states, which have energies near the band edges, are examples of the features that may be expected in random materials. As the structure becomes more random, these states are more numerous and are more randomly scattered in the energy-momentum space, having less correlation with each other. These states cannot be treated as groups like true energy bands spanning a continuum of energy. Neither do they have distinct edges in energy, as in the case for valence bands and conduction bands in a periodic system. Instead, in a random material, at some critical point in energy, the wave-function of the electron (of this energy) undergoes a change of character from a localized one to a delocalized one. This point is called the mobility edge. On one side

of the mobility edge, all electronic states are delocalized; on the other side, they are localized. A conductor, for example, is one in which the Fermi level is high enough so that it allows electron filling beyond the mobility edge, accessing delocalized states. Conversely, an insulator is one in which the Fermi level falls below the mobility edge accessing only localized states. The above features of energy (and momentum) are evaluated for wave functions in a sample of essentially an infinite size. For nanoscopic samples, these features become less well defined as they will strongly depend on the boundary condition.

In 1958, Anderson provided a straightforward real-space criterion for distinguishing insulators and conductors in disordered materials based on the "diffusion" distance δ of an electron[1]. At 0K, a material in which an electron has a finite ζ is an insulator; conversely, a material in which an electron has an infinite ζ is a conductor. Aided by the scaling argument, this concept has led to major advances in the understanding of disordered electronic systems. For example, it explains why the electrical resistivity of "dirty" metals always rises toward 0K[2,3,4]. Surprisingly, though, there has been no attempt to use such size dependence to experimentally engineer metal insulator transition (MIT) in random materials for technological applications. Indeed, the most convincing experimental verification of the scaling theory in connection to Anderson localization came from the predicted temperature, pressure, concentration, and

magnetic field dependencies of properties of macroscopic samples, and not from the size dependence of conductivity which is obvious from the criterion. Yet the size-dependent metallicity in random materials should be of great interest to nanotechnology since ζ typically approaches the nanoscale.

In this chapter, we report a size-triggered metal-insulator transition (MIT) in the SiO_2:Pt system. Together with the thesis of Yudi Wang who studied a similar problem in perovskite thin films, this is the first time the size-triggered MIT is reported. By engineering the thickness δ to reach the nano-size level, we found an insulator to metal transition can occur well below the bulk percolation limit, giving rise to what we term "nanometallicity". We also observed an external voltage stimulated MIT when $\delta \sim \zeta$. The latter behavior naturally leads to the application of memory devices baed on this nanometallicity concept.

II. Experimental Procedures

A p-type (100) single crystal silicon wafer was used as sample substrate. The wafer was first cut into small pieces of a size about 4 mm × 4 mm, then cleaned by acetone and Di water in an ultrasonic bath for several minutes. After cleaning, the substrate was placed in a pulse laser deposition (PLD) or a sputter chamber. Films of $SrRuO_3$ (SRO) by PLD or Mo by sputtering were deposited on the substrate as the bottom

electrode (BE).

The SRO film was deposited at temperatures ranging from 350℃ to 550℃ with the laser energy fixed at 300 mJ and the chamber backfilled with oxygen of 100 mtorr. The film morphology was examined by atomic force microscopy (AFM, Nanoscope IIIA Dimension, Digital Instruments, Santa Barbara, CA). The film structure was analyzed using a high-resolution x-ray diffractometer (HXRD, D8 Discovery, Bruker AXS, Madison, WI), and the film thickness measured by the same diffractometer in the x-ray reflection (XRR) mode. Electrical properties measured in the continuous voltage-sweep mode were performed using a Keithley 237 high voltage/source measuring unit (Keithley Instruments, Cleveland, OH) with the sample mounted on a probe station (S-1160, Signatone Corporation, Gilroy, CA).

The XRD pattern of the SRO target is presented in Fig. 1. The peaks show a phase-pure perovskite structure. The target has high density (~95%) and is suitable for PLD deposition.

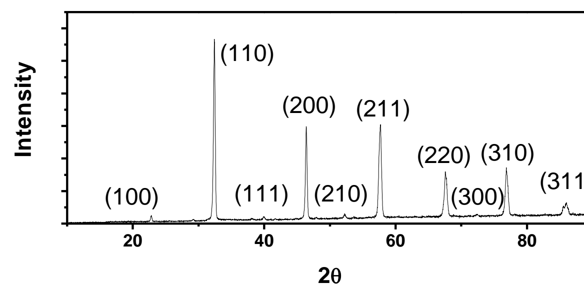


Fig. 1 XRD pattern of a $SrRuO_3$ target.

In Fig. 2, AFM images of SRO films deposited at different substrate temperatures are shown. These images indicate that SRO is unable to crystallize below 400℃at a laser energy of 300 mJ. The crystallized SRO reveals a (110) peak[5], as shown in Fig. 3. The roughness of the surface is strongly related to the film thickness and deposition condition, as is the resistivity. The best combination of smoothness and resistivity was obtained at 30 nm. For this thickness, as the temperature increases from 450℃ to 550℃, the grain size increases, which causes an increase of surface roughness and a decrease of resistivity[6], as shown in Fig. 4. Therefore, the optimal temperature was chosen to be 500℃ in order to obtain a RMS roughness < 2 nm and a two point resistance of about 200 Ω for a 30 nm bottom electrode across a substrate of 4 mm × 4 mm. This film was deposited at 100 mTorr oxygen; at a higher or a lower pressure an insulating film was obtained[6]. We also used n-type Si substrates of (110) and (100) orientations. No orientation effect on SRO deposition was found according to AFM and XRD examinations. This may be explained by the presence of a thin amorphous native SiO_2 film on all Si substrates[7].

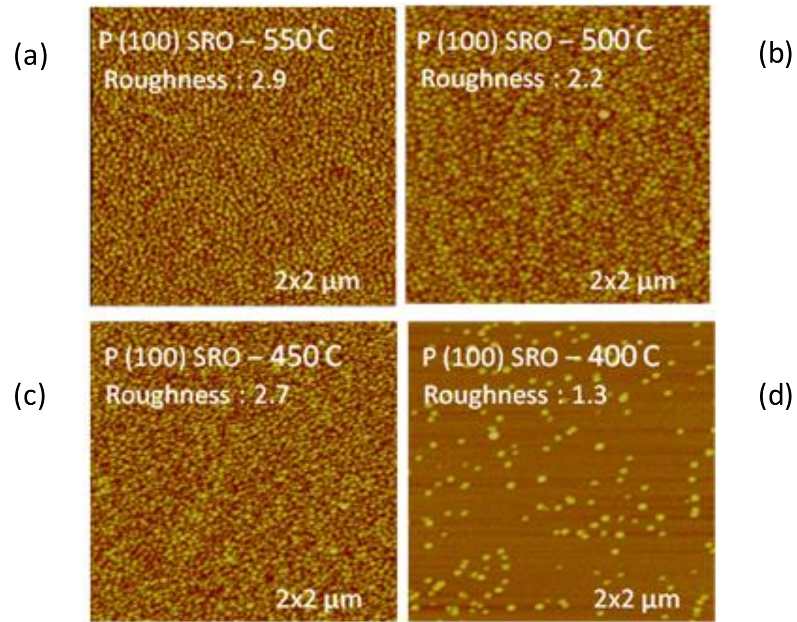


Fig. 2 2 × 2 µm AFM image of 30 nm SRO film with deposition temperature ranging from 400℃ to 550℃.

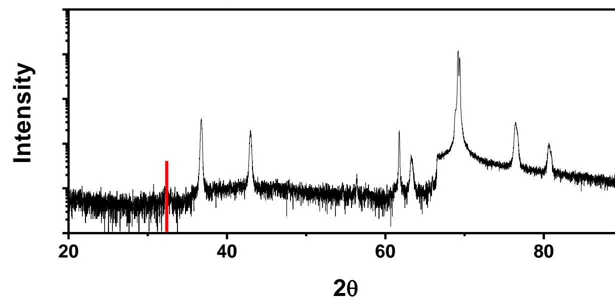


Fig. 3 SRO deposited on P-Si (100) showing (110) orientation.

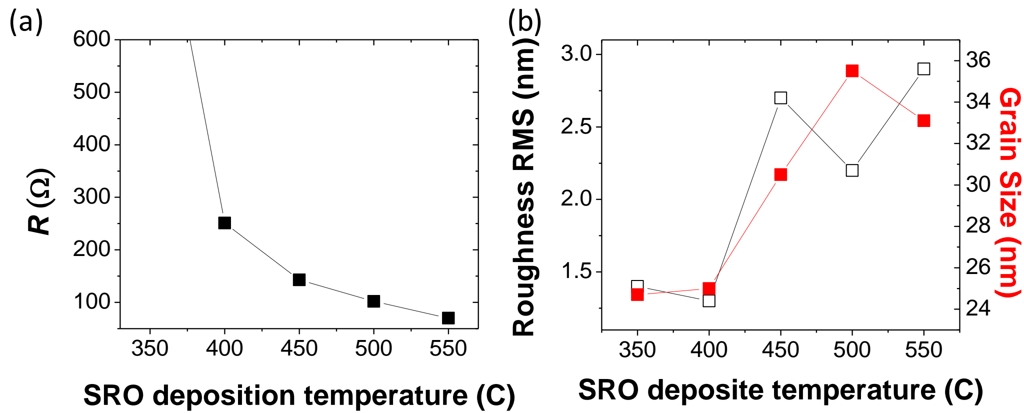


Fig 4 (a) 2 point resistance of SRO film under different deposition temperature, (b) roughness and grain size of SRO film with different deposition temperature.

Mo films as BE were deposited on thermal oxide coated Si wafers by a direct current (DC) sputtering method, as shown in Fig. 5(a). A Mo target (99.95%, Williams Advanced Materials, Brewster, NY) was used as the sputtering source. The base vacuum pressure was 1×10^{-7} in order to avoid Mo oxidation. Figure 5(b) shows the XRD patterns of the Mo films under various deposition conditions. At higher power, 200 mA, Mo (110) reflection is evident indicating crystallization and the preferred orientation[8,9]. When the deposition power is lower, e.g., 100 mA, the (110) peak diminishes and an oxide peak appeares. This results in a non-linear I-V behavior of the film, which indicates the film is insulating. In our practice, a long pre-sputter time (during which sample being shielded by a shutter) and a fast sputtering rate were used to minimize Mo oxidation[10]. Under the “standard” condition (a working pressure of 5

mtorr and a direct current of 200mA), the deposition rate was at least 5nm per minute. The "standard" film has a thickness about 50 nm and a resistance typically 100-200 ohms across the 4 mm square wafer.

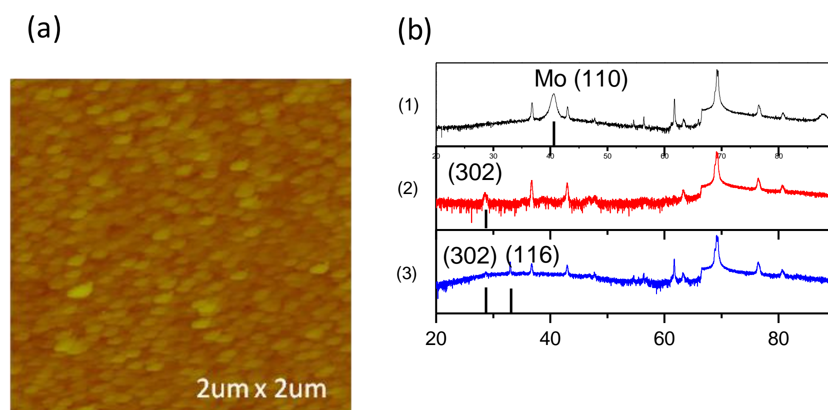


Fig. 5 (a) AFM image of Mo film morphology showing RMS roughness ~1.4nm, (b) XRD pattern of Mo film under various sputtering conditions: (1) 5 mtorr, 200mA DC current, (2) 5 mtorr, 100mA DC current, and (3) 12 mtorr, 200mA DC current.

To avoid contamination, the SRO coated samples, once removed from the PLD chamber, were immediately placed into the sputter chamber for mixture layer deposition. (The Mo coated samples were left in the sputtering chamber until mixture layer deposition.) For the latter, a SiO_2 target (99.995%, Kurt Lesker Company, PA) was used as the sputtering source. Deposition rates of SiO_2 and Pt on unheated substrates were first determined for the following conditions: 120 W and 205 W for the SiO_2 target at 15 mtorr of flowing argon; 14W to 31W (40V ~ 65V) for the Pt target at the same working pressure. With these data, mixture films of various

compositions were co-sputtered by varying the power of the Pt target. The composition of the mixture film was calibrated using energy-dispersive X-ray spectroscopy analysis (EDX, JEOL 7500F FEG HRSEM) and Rutherford backscattering (RBS, NEC Minitandem Ion Accelerator). AFM micrographs in Fig. 6 show a smooth morphology (RMS roughness < 3 nm) for such mixture layers on the Si (100) and SRO/n-type Si (110) substrates.

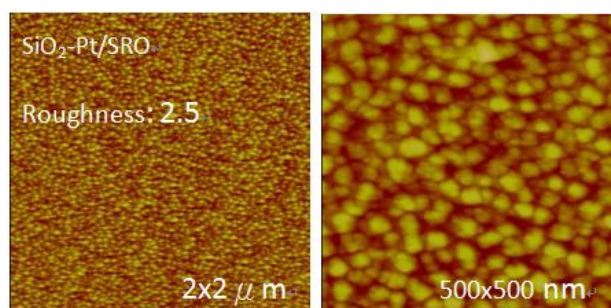


Fig. 6 Morphology of SiO_2-Pt on SRO BE.

Finally, Pt top electrodes (TE) of approximately 50 nm thick were deposited on the SiO_2-Pt mixture film. A shadow mask with circular openings ranging in diameter from 70μm to 168μm was used to define electrode areas. Figure 7 shows a schematic device; each circular electrode defines a “cell.”

Similar device structures were also obtained by replacing SiO_2 of the mixture layer with Si_3N_4. An un-doped Si target (99.999%, Williams Advanced Materials, Brewster, NY) was used as the sputtering source, and 12 sccm of gaseous N_2 and Ar, with the total pressure maintained at 20 mtorr, was introduced for reactive sputtering. The top

and bottom electrodes were Pt and SRO. The Pt to Si_3N_4 ratio was also calibrated by EDX.

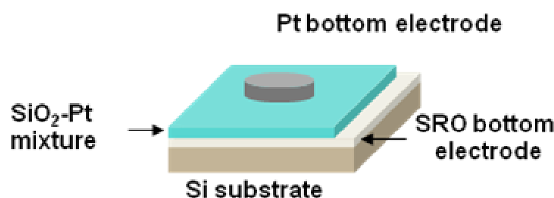


Fig. 7 Schematic of the Pt/SiO_2-Pt/SRO RRAM device.

Pt/SiO_2-Pt/$SrRuO_3$ (SRO) and Pt/SiO_2-Pt/Mo devices with different mixture thicknesses (δ) and Pt concentrations (f, the molar fraction of Pt in a mixture of Pt+SiO_2) were investigated to determine the metal/insulator behavior and the transition. Typically, the electrical properties were investigated using the following voltage sequence: 0V → -4V → 0V → 4V → 0V, as shown in Fig. 8. Positive bias is defined as current flowing from top electrode (Pt) to the mixture film and then to the bottom electrode (SRO or Mo). A similar study was conducted for the Si_3N_4 containing devices.

The electrical properties were further investigated by using different TE/BE including Pt, Ta, Ni, Ag, Mo, and SRO. Pt, Ta, and Mo were deposited by either DC or RF sputtering. Ni and Ag were deposited using a thermal evaporator (VE-90, Thermoionics Inc. Sunnycale, CA). The samples were loaded into an evaporator

chamber immediately after mixture film deposition to avoid contamination by air-borne species. After prolonged pumping to achieve a base pressure of 10^{-7} torr, a power is applied to maintain a deposition rate of 0.1 nm/sec measured by a quartz crystal thickness monitor. To improve adhesion with SiO_2, a 1 nm thin Cr film was deposited prior to Ag deposition. All electrodes deposited through a shadow mask that defines circular electrodes of 80 μm in diameter have a thickness around 50 nm.

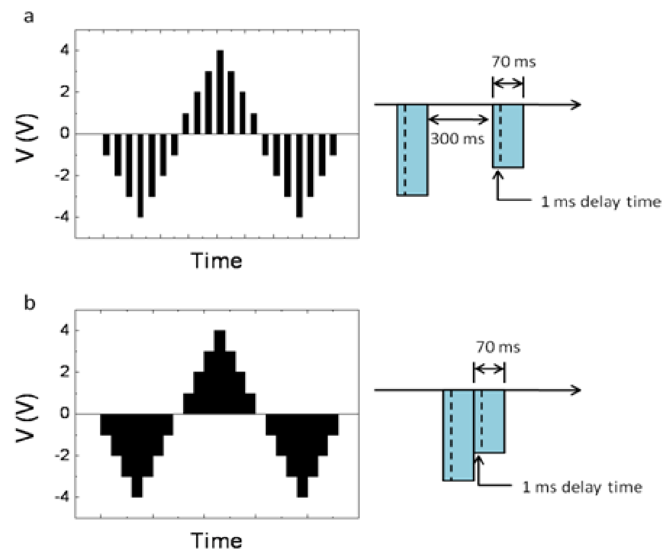


Fig. 8 Electric measurement sequence.

III. Results

A. The δ–f map and resistance switching properties

Electrical behavior of films of various thickness and composition is summarized in Fig. 9. Triangles denote films which switch, exhibiting a distinct high resistance (HR)

and a low resistance (LR) state. Filled circles represent films that are always in the HR state, and the open circles represent films that are always conducting, i.e., in the LR state. Clearly, switching is limited to a window of certain thickness (δ) and Pt (f) concentration combinations. Both SRO and Mo BE devices shared the same f-δ map. Notably, when the Pt concentration of the mixture film exceeds 40%, which is the bulk percolation limit established in the preceding chapter, there is no more HR/LR transition regardless of thickness. Below this composition, thinner films are metallic, thicker films are insulating, and between the two regions a voltage-triggered metal to insulator (MIT) transition is observed, as shown in Fig. 10 for two devices, one with a SRO BE and the other a Mo BE. Here, a positive voltage V refers to having a current I flowing across a test cell from top to bottom, with a resistance R=V/I. Note that the film is initially in the LR state and ohmically conducting.

The two distinct states, HR and LR, can be read with a low voltage (~0.2V). At a characteristic positive bias, the cell switches from the LR state to the HR state. This process is termed set process (or off switching) and the critical voltage that triggers this transition is called set voltage (V_{set}). At a characteristic negative polarity, the cell switches back from the HR state to the LR state, which is termed reset process (or on switching) and the critical negative voltage is called reset voltage (V_{reset}). Note that reset takes place in multiple stages. Hence, in the following, V_{reset} refers to the voltage

at the first reset resistance drop. Meanwhile, since reset can apparently be continuously triggered at a higher negative bias, the maximum (negative) voltage used will be referred to as the maximum reset voltage, max V_{reset}. Note that this definition of set and reset transitions differs from the one used in the literature because the as-fabricated state of our device is in the LR state whereas most, if not all, other resistance-switching devices start in the HR state (or in an even higher HR state).

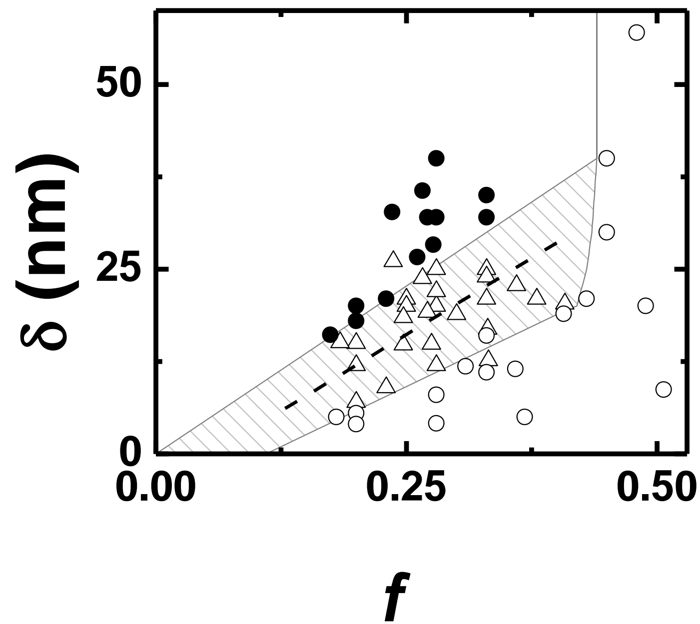


Fig. 9 δ-f map of SiO_2-Pt device, filled circles: insulating, open circles: conducting, triangles: resistance switching.

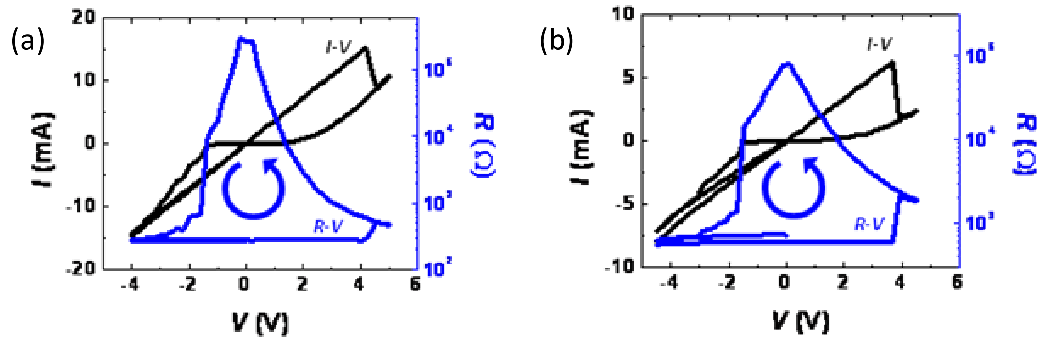


Fig. 10 Voltage triggered resistance switching in (a) Pt/SiO_2-0.25Pt/SRO device and (b) Pt/SiO_2-0.3Pt/Mo device.

Figure 11 shows the HR-LR transition and its *f* and δ dependence. With f=0.2, as δ decreases in Fig. 11(a), the film begins to switch at 12 nm, switching continues through 7 nn, and finally at 5.5 nm switching is lost and the film is always in the LR state. With δ= 20 nm, as *f* increases in Fig. 11(b), the film begins to exhibit switching at 25%, which continues through 36%, and finally at 42% switching is lost and the film is always in the LR state.

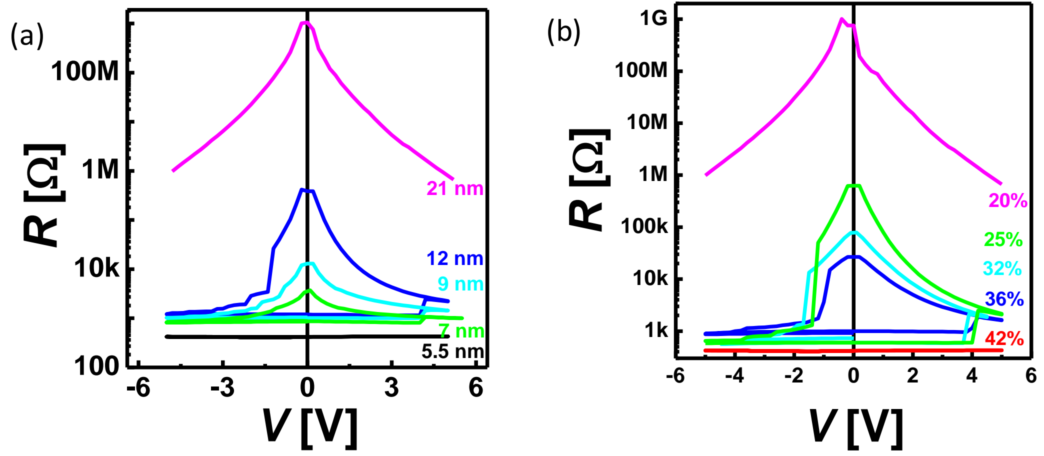


Fig. 11 (a) δ-triggered MIT, *f*=20% and (b) f-triggered MIT, δ=20nm, both with voltage-triggered MIT in between.

B. Switching voltage

Remarkably, the set voltage in Fig. 11 is independent of both *f* and δ. The voltage to trigger resistance switching is summarized in Fig. 12. For all the thickness, concentration, and cell size, the voltage to trigger resistance set transition is always the same. Later, in Chapter 5, we will also show that the switching voltage is temperature independent.

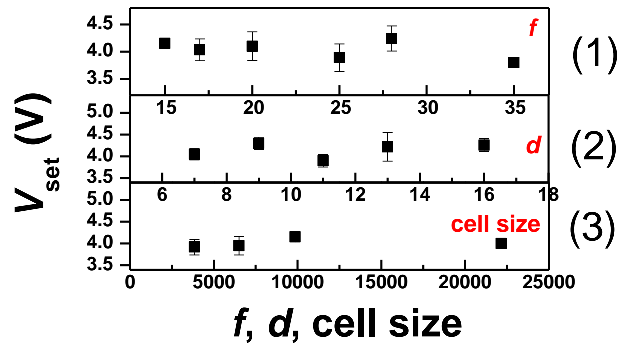


Fig.12 Switching voltage as a function of (1) Pt concentration, (2) film thickness, and (3) cell size.

C. Electrode dependence

Beside Pt/SiO_2-Pt/Mo and Pt/SiO_2-Pt/SRO structures, other electrode combinations using different materials for different electrodes were also investigated. All of them show reproducible resistive switching behavior and all are bipolar switching. Two distinct resistance states with a resistance ratio of at least 100 were demonstrated in these structures. In the cases shown in Fig. 13(a) and (b), the switching “loops” are counter-clockwise, similar to those of Pt/SiO_2-Pt/Mo and Pt/SiO_2-Pt/SRO. In the cases shown in Fig. 13(c) and (d), the switching loops are clockwise.

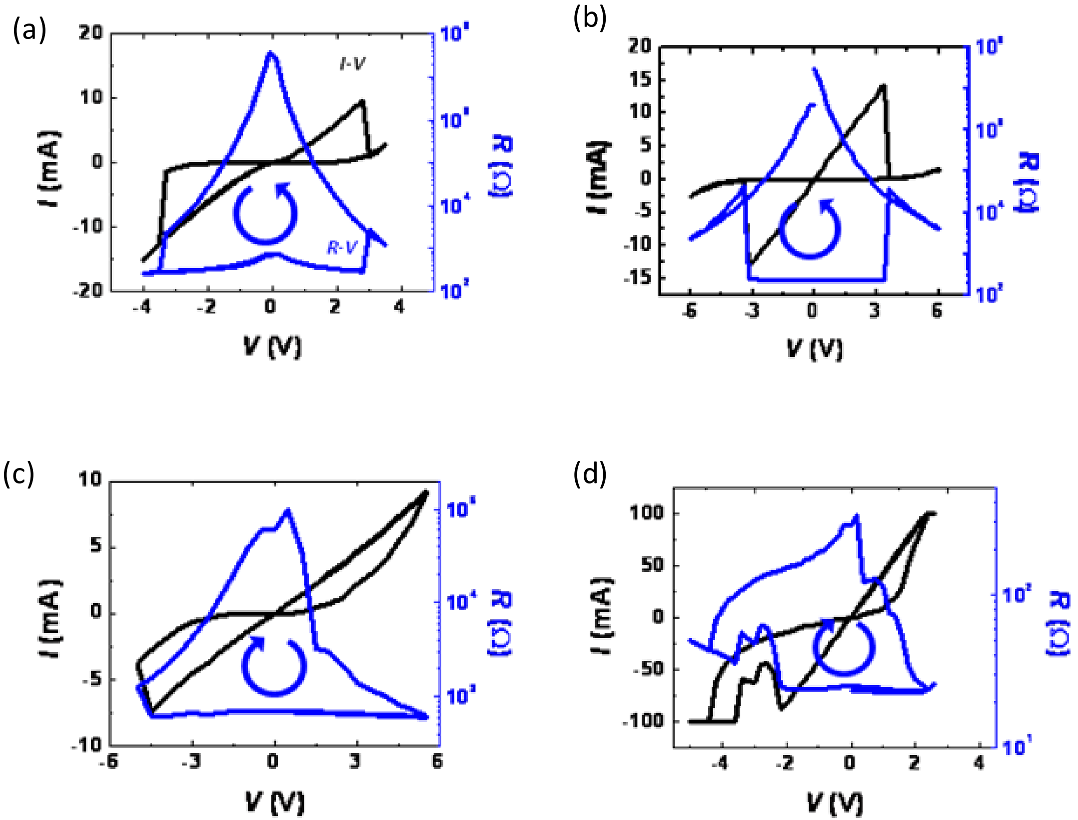


Fig. 13 I-V curve (Black) and R-V curve showing resistance switching of different combination of TE/BE, (a) Pt/Ta, (b) Pt/Ni, (c) Mo/SRO, (d) Ag/Pt.

Highly p-doped Si wafer is known to have a work function around 4V. In principle, the p-doped state (commonly referred to as p++) can be directly used as the BE in our design. The device, however, exhibits a very high initial resistance, generally over 10 MΩ. The I-V curve shows a Schottky barrier-type behavior. As shown in Fig. 14(a), although it exhibits certain resistive switching behavior between two states, HR and LR, the latter not Ohmic unlike the LR in devices described earlier, after some 20 cycles, the device breaks down from the high resistance state (HR) to a very low

resistance state (LR’). Subsequent “switching” occurs when a very high voltage was applied, switching between the LR’ to the LR that actually has a higher resistance than LR’. In addition, the HR state exhibits a highly asymmetric I-V behavior. Figure 14(b) show the I-V curve of this device before the cycling test in Fig. 14(a); clearly the I-V is asymmetric and appears to be akin to certain Schottky barrier-like behavior in the literature[11]. The device can switch at a higher voltage of +8 V/−7 V, switching between two asymmetric insulating state. After the then breakdown (or forming) in about 20 cyles, the I-V curve shown in Fig. 14(c), has a symmetric LR state and an asymmetric HR state.

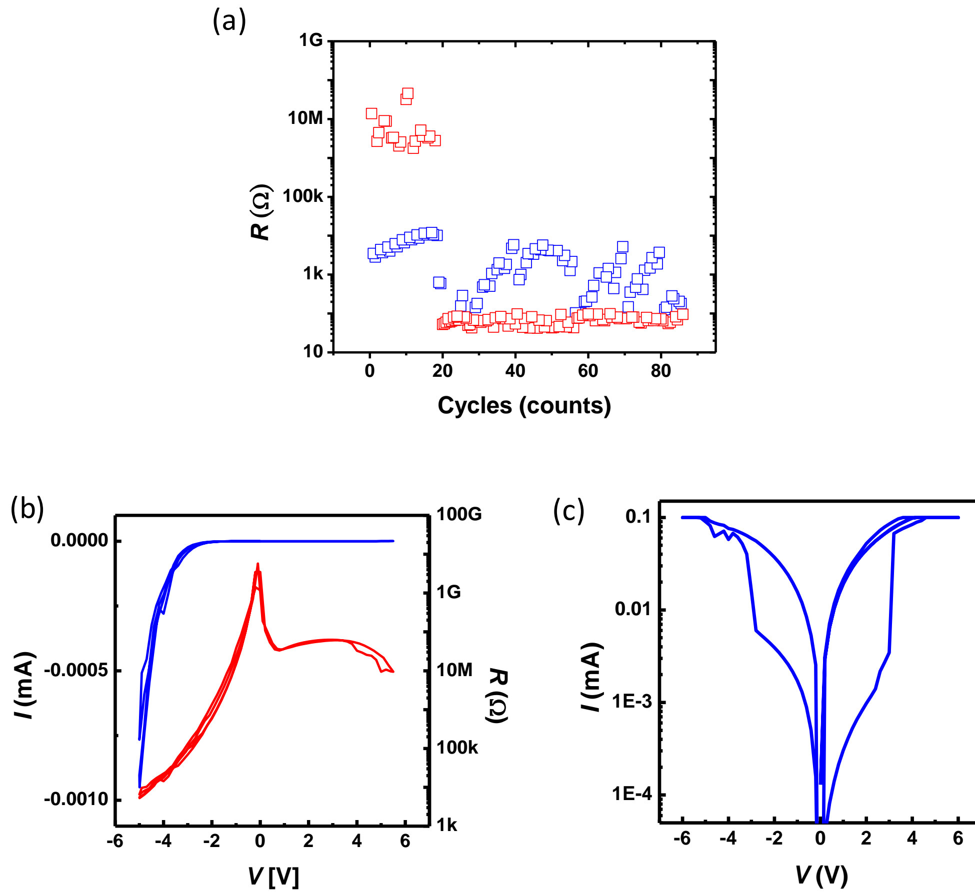


Fig. 14 (a) Resistance switching behavior in a Pt/SiO_2-Pt/P-Si device using cycling test, red : resistance after -7V pulse; blue : resistance after +8V pulse; (b) Schottky-type I-V and R-V curves of the as-fabricated state; no resistance switching is evident; (c) resistance switching I-V curves after forming.

Furthermore, symmetric electrode configurations were also investigated. Devices with the Pt/SiO_2-Pt/Pt and Mo/SiO_2-Pt/Mo configurations were fabricated by sputtering; neither shows resistive switching. The two devices behave differently. In the case of Mo/SiO_2-Pt/Mo, the film is always in the LR state and cannot be switched to the HR state. In the Pt/SiO_2-Pt/Pt case, the film initially is in the LR state, but

switches to an HR state at a relatively small voltage of either positive or negative polarity, after that it remains in the HR state regardless of the voltage magnitude or polarity. However, the HR state can be switched back to the LR state by a UV light (wavelength: 300-420 nm, energy: 4.2-3.0 eV, ELC-403, Electro-Lite Corp., Bethel, CT), just like all other switchable devices described in our work which all can be switched from the HR to the LR by similar UV irradiation (see Chapter 4 for more details). These contrasting I-V behaviors are shown in Fig. 15 for the Pt/SiO_2-Pt/Pt device (Fig. 15(a)) and for the Mo/SiO_2-Pt/Mo device (Fig. 15(b)).

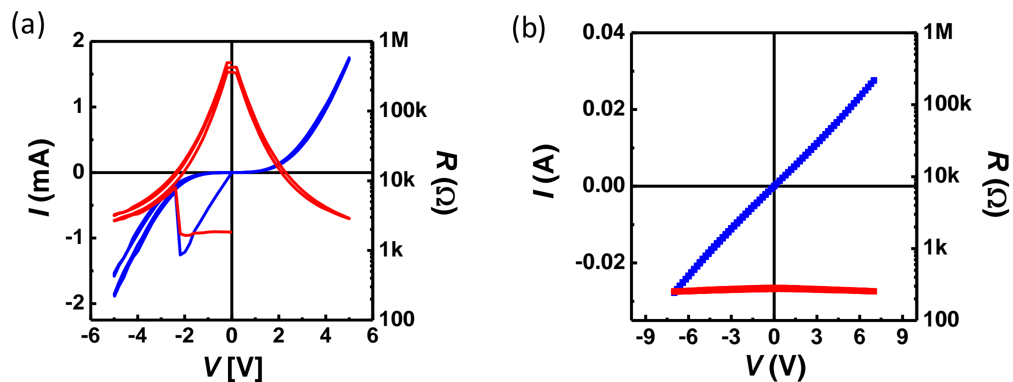


Fig. 15 I-V and R-V curves of (a) Pt/SiO_2-0.25Pt/Pt, and (b) Mo/SiO_2-0.25Pt/Mo electrodes showing different electrical properties.

D. Silicon nitride system

Resistance switching similar to that observed in Pt/SiO_2-Pt/SRO was observed when SiO_2 is replaced by Si_3N_4, as shown in Fig. 16.

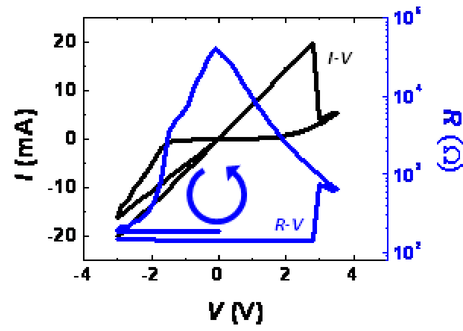


Fig. 16 I-V and R-V of resistance switching behavior in a Pt/$SiN_{3/4}$-0.25Pt/SRO device.

E. Thickness dependence

The thickness dependence of the HR (read at 0.1 V) was found to follow an exponential dependence, which violates Ohm's law. As shown in Fig. 17, this dependence holds for all three Pt concentrations despite different slopes. The slope becomes steeper as the Pt concentration is lowered. Because of the exponential dependence, the HRS increases dramatically as the thickness increases, varying by five orders of magnitude when the thickness increases by mere 10 nm in the case of 20% Pt. When the Pt concentration is higher, the HR increases less, though the dependence is still apparently exponential and much faster than seen in the conventional resistors ($R \propto$ thickness).

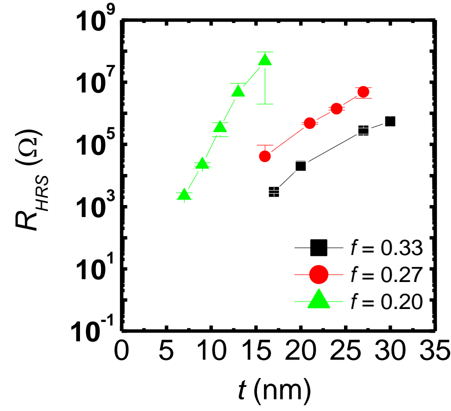


Fig.17 Dependence of HR on Pt concentration (f) and film thickness (δ).

IV. Discussion

A. Nanometallicity

The insulator to metal transition in thick films occurs at f=0.4 in Fig. 9, which coincides with the percolation limit seen in the bulk measurements described in the preceding chapter (Chapter 2, Fig. 17). However, for thinner films, the transition to the metallic-like behavior occurs well below f=0.4, such metals may be regarded nanometallic and their metallicity may be termed "nanometallicity." In Anderson's picture, the sample gains nanometallicity as it shrinks below electron's diffuse length ζ. Consequently, as the thickness of the film δ is greater than this diffuse length ζ, it behaves like a non-Ohmic insulator. Conversely, when δ is less than ζ, the film

becomes an Ohmic conductor. According to Fig. 9, we may define this diffuse length ζ as the dashed line which is the bisect of the switching region, which is sandwiched between the insulating region and the conducting region.

The films with $\delta \sim \zeta$ are initially in the LR state but can undergo a metal to insulator transition triggered by a voltage pulse, and the transition is reversible by a reverse voltage trigger. The polarity of the switching direction is dependent on the relative work function of the two electrodes. (Work functions of the electrodes used here are listed in table 1.) Without exception, there is a perfect correlation between the direction of the switching loop and the relative work functions of the top and bottom electrodes. The result indicates that switching polarity can be predicted and engineered.

Table 1. List of work function and the switching polarity (blue color indicate higher work function electrode; positive: counter-clockwise, negative: clockwise).

Mixture Film	$\varnothing_{TE}$ (eV)	$\varnothing_{BE}$ (eV)	V_s Polarity
SiO_2-Pt	Pt 5.65	SRO 5.0	+
	Pt 5.65	Mo 4.6	+
	Mo 4.6	SRO 5.0	-
	Ag 4.26	Pt 5.65	-
	Pt 5.65	Ta 4.25	+
$SiN_{3/4}$-Pt	Pt 5.65	SRO 5.0	+

When the BE has a work function smaller than the TE, charge injection from the BE side is possible during the positive voltage sweep. This appears to trigger the LR to HR transition. Under a reverse bias, the HR to the LR transition then corresponds to the removal of the injected charge, presumably trapped until this stage, flowing from the film back to the bottom electrode, if the above picture of electron injection is correct. On the other hand, if the same material is used for both electrodes, then the above picture of charge trapping/removal obviously is not applicable. This seems to be consistent with the observations that, (a) in the case of Mo electrodes, the device remains in the LR state regardless of polarity and voltage; and (b) in the case of Pt electrodes, the device, once switched to the HR state, remains in the same state regardless of polarity and voltage. The different behavior between (a) and (b), however, cannot be explained simply by the above argument, and further considerations are needed.

B. Resistance thickness dependence

The HR's thickness dependence of the mixture film is particularly interesting. In a conventional insulator, resistance is proportionally to the thickness as described by Ohm's law. Such behavior does not exist in our devices. In the SiO_2-20%Pt films of ~ 10 nm, the resistance level increases by one order of magnitude as the thickness

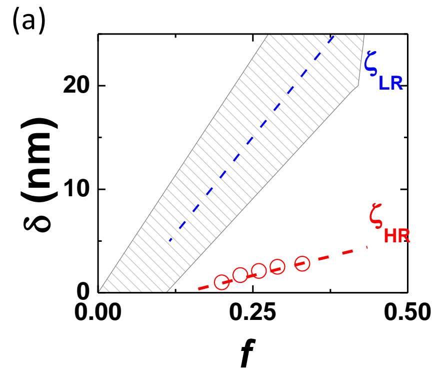
increases by only 2.5 nm. This confirms that the SiO_2-Pt device is not a conventional resistor. Instead, its behavior follows the prediction of the scaling theory for disordered medium[12]:

$$R_{HRS} \sim \exp(-\delta/\zeta)$$

Here, ζ is a localization length of electrons. Comparing ζ of the HR state with the diffusion distance of electrons in the LR state, we see an order of magnitude decrease (see Fig. 18). This drastic decrease accounts for the entirely different R(V) behavior of the two states, being linear in the LR state and highly non-linear in the HR state. It also confirms that the two states are in entirely different regimes of localization. The LR state is not localized since δ is below the diffusion distance, the HR state is definitely localized since δ far exceeds ζ. From Fig. 18, it is also clear that the localization length increases from 1.0 nm to 2.80 nm as the Pt composition increases. This is reasonable since an increase of Pt concentration favors metallicity, thus reducing the electron localization distance.

For a cube size of δ^3, the predicted pre-exponential factor is about 8 kΩ[13]. The extrapolated pre-factor obtained from Fig. 10 at δ=0 is about 10Ω, which is about 10^{4-5} smaller than 8 kΩ. We believe this is due to the many parallel conducting paths existing across the film, resulting in a lower total resistance. This is reasonable since the SiO_2-Pt thin film has a lateral dimension much larger than the thickness. Indeed,

we find the product R and area of different cell sizes follows the same exponential dependence, giving about the same t_o, suggesting that the pre-factor is about inversely proportional to the area.



(b)

f	0.2	0.23	0.26	0.28	0.33
ζ_{HR} (nm)	1.0	1.7	2.1	2.5	2.8
ζ_{LR} (nm)	10.8	13.5	15.9	17.5	20.5

Fig.18 (a) Fitted localization length as a function of Pt concentration plotted against original diffuse length in virgin films, and (b) comparison of ζ_{HR} and ζ_{LR}.

C. Possible switching and charge trapping model

Wang used epitaxial thin films of perovskites on (001) $SrTiO_3$ substrates to demonstrate a metal insulator transition and a reversible, voltage-induced LR-HR transition [14,15]. These films are random alloys containing a conductor ($SrRuO_3$ or $LaNiO_3$) and an insulator ($CaZrO_3$ or $LaAlO_3$). In the above conductors, electrons of Ru^{4+} ($4d^4$) and Ni^{3+} ($3d^5$) form a conduction band of a narrow bandwidth (having a

high density of states). In a random alloy, some bandwidth B of such electrons may still exist when their concentration is high enough. In particular, if B exceeds the (weak) disorder W due to alloying, then metallicity is maintained. On the other hand, if $W>B$, then the alloy is an insulator. Near the critical state of $W \sim B$, charge trapping that creates additional strong disorders may tilt the balance so that the initially conducting film ($W<B$) loses metallicity above a certain set voltage. This picture is also due to Anderson and the transition is sometimes referred to as Anderson localization/transition[4, 16]. Such films can recover metallicity later, when, upon reaching a reset voltage of a reverse bias, charge trapping is removed, and so are strong disorders.

The above picture is applicable at all length scales. Therefore, it can be used to explain the metal insulator transition in the macroscopic sample. However, Wang also observed size-dependent nanometallicity of the same nature as we do here. Therefore, the above picture needs to be modified to reconcile with Anderson's picture of diffusion distance. One possibility is that W is size dependent: in larger samples, W is larger if it refers to the worst disorder that can cause electron localization. Conversely, as the size decreases, W is smaller so even samples with a composition well below the bulk conduction limit can become metallic. In this way, Anderson localization/transition implies an implicit size effect that is made explicit in

Anderson's diffusion picture.

Presumably, the above picture also applies to amorphous insulators that contain electron sources, such as an amorphous insulator SiO_2 with atomically dispersed Pt. In theory, electrons of metallic Pt ($5d^9$ $6s^1$) could have a larger bandwidth than those of Ru^{4+} and Ni^{3+} in the perovskite structure. However, in the amorphous SiO_2 the distance between Pt atoms is possibly larger, which may substantially reduce B. Meanwhile, the disorder of the amorphous surrounding is certainly very considerable giving a larger W. This may explain the relatively large Pt fraction, compared to some compositions (such as $CaZrO_3$:5%$SrRuO_3$), required to render our films metallic.

A picture of nanometallic paths and the effect of trap charge is shown in Fig. 19. Nanometallicity initilaly provides a passage for electron flow in the vertical direction, for a distance ζ that exceeds the film thickness δ. This is despite the presence of possible trap sites (T1, T2, T3) nearby, as long as such sites are electrically neutral thus not providing any potential barrier. Later, when electrons are trapped, possibly via Fowler-Nordheim tunneling (FNT) or by other mechanisms that are likewise voltage sensitive, an electric field is erected which lifts the Coulombic potential (W*). These new and strong disorders block the current on the conducting path: they reduce the diffusion distance ζ to a value less than δ. In terms of Anderson localization/transition, this corresponds to W*>B; B does not change since the

composition remains the same. In this way, the LR to HR transition is achieved and is understandable in both the Anderson localization/transition picture and the Anderson diffusion picture.

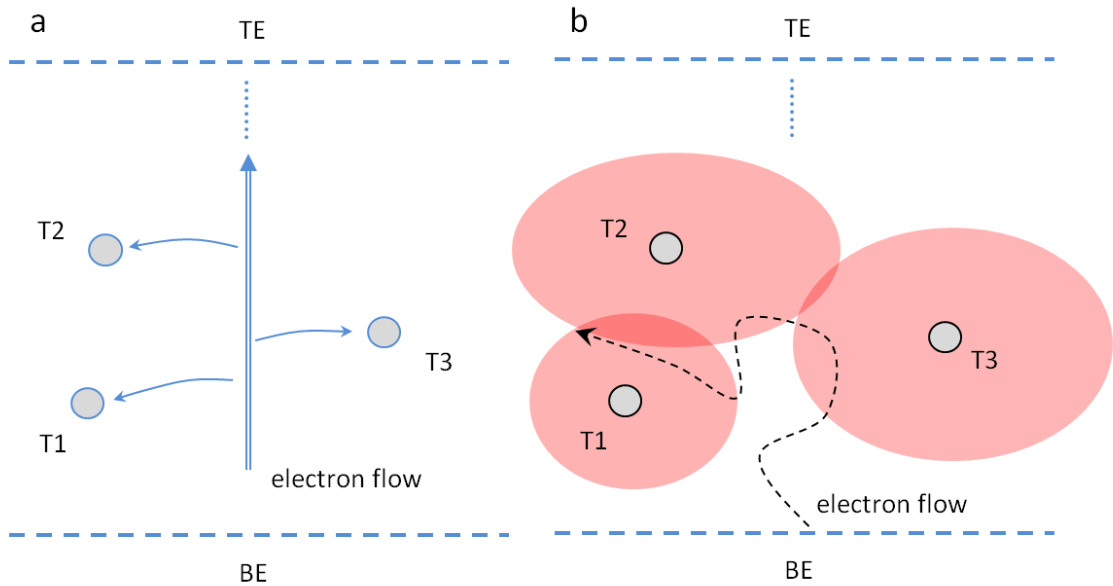


Fig. 19 (a) Nanometallic path allowing electron diffussion through the film. (b) charge-trapped states that scatters electrons so much that the electrons becomes localized.

V. Conclusions

1. Nanometallicity is achieved by shrinking the sample dimension to less than the electron diffuse length.
2. When the composition of the conductor in the mixture layer is near the critical value for electron transport over a distance of the sample dimension (thickness), the pathway can be easily gated off or gated on by introducing or withdrawing a trap-charge-mediated strong disorder, using a voltage.

3. Electrode dependence tests suggest that the voltage-triggered MIT is work function dependent.

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Chapter 4 Device Properties

I. Introduction

A. State of the art

Non-volatile random access memory (NVRAM) is a type of storage device that holds information without power. Recently, flash memory [1] has been replacing magnetic storage devices especially in portable electronics. Its high read/write speed and excellent mechanical stability have also allowed NVRAM to make inroad in non-portable computers. Resistive switching random access memory (RRAM), being one of the strongest candidates for future NVRAM, has drawn significant attention from industry. Materials for RRAM include amorphous/crystalline chalcogenides which have been under study since the 1960's[2,3,4]. More recent research has also focused on oxides thin film, especially transition metal oxides including binary oxides and ternary and quarternary oxides such as perovskites: for examples, TiO_2[5,6], NiO[7], Al_2O_3[8], ZrO[9], SiO_2[10] $SrTiO_3$[11], and $(Pr,Ca)MnO_3$[12]. Polymer composites[13] were also reported to exhibit resistive switching. A review of these materials and their switching mechanisms was given in Chapter 1.

A typical RRAM device can hold two resistance states, a high resistance (HR) and a low resistance (LR). The two states can be switched back and forth via a voltage pulse or a current pulse[14,15]. A common characteristics of RRAM devices is that the as-fabricated cells require a so-called "forming process" to activate the device's switching behavior[16]. In most cases, the as-fabricated cells usually have a resistance higher than that of the HR state and cannot be switched to either HR or LR. The "forming process" is performed under a high voltage, usually higher and lasting much longer than the switching voltage pulse, which "breaks" the initial high resistance. This process, although its detail is still under debate, appears to cause either ion migration from the electrodes into the insulating film[3] or oxygen vacancies to form creating states that facilitate electron hopping[17,18].

The thus "formed" cell enables resistance switching between two stable states. In such a device, conduction in the LR state depends on a few filaments that were initially formed in the forming process. This results in a relatively area-insensitive resistance state for both the HR and LR[15,19]. It is also conceivable that switching may not be possible when the cell area approaches or even falls below filaments' dispersion limit[20].

Referring to the performance of the state-of-the-art Flash memory which sets a benchmark for the RRAM[21,22], the proposed performance requirements for RRAM are

listed in Table 1: long retention time (≥ 10 years), short read/write time (t ≤ 100 ns), high density (area ≤ 100 x 100nm^2) and low applied voltage (≤ 1V). According to the calculations of Schroeder et al.[23], such criteria cannot be satisfied in devices that operate via Simmons & Verderber's mechanism[3] of electronic switching. Properties of long retention time, short read/write time and low operating voltage are mutually incompatible. This has been referred to as the "voltage-time dilemma."

Feature	Range
Cell size, A	<100 x 100 nm^2
Store time, t_s	> 3 x 10^8 s (= 10yrs)
Write time, t_w	< 10^{-7} s
Read time, t_R	< 10^{-7} s
Read voltage, V_R	< 1V
Read current, I_R	~10^{-6} A
Resistance Ratio, R_{off}/R_{on}	~10
$t_{retention}/t_{write}$	>10^{16}

Table 1. Performance requirements.

In this chapter, we describe prototype devices fabricated using the materials described in the preceding chapter. The properties of these devices are evaluated to compare with the above performance requirements. Special attention will also be

made to verify that their switching behavior is purely electronic. We find that they satisfy most if not all of the above listed requirements including a low operating voltage (as low as 1V), long retention time, fast switching, low power, and high resistance ratio, indicating that they do not suffer from the voltage-time dilemma as discussed in Schroeder's paper. Some of the above aspects (retention and dynamic switching) will also be examined in more detail in later chapters

II. Experimental Procedures

Most of the experimental procedures used here have been described in detail in the preceding chapter. Briefly, a mixture film of about 20~30 nm, consisting of an insulator (SiO_2 or Si_3N_4) and a conductor (Pt), was deposited by cosputtering over a 20 nm bottom electrode (SRO or Mo) on a Si substrate. The Pt concentration f ranges from 20% ~ 30%, and Pt was also used as the top electrodes patterned by a shadow mask with a diameter of 80 μm and an electrode spacing over 100 μm. Since f is below the bulk percolation limit, these electrode pads are electrically isolated from each other across the mixture film surface. Electrical properties of the device were measured either by a continuous voltage sweep or by voltage pulses using a Keithley 237 (Keithley Instruments, Cleveland, OH) with samples mounted on a probe station (S-1160, Signatone Corporation, Gilroy, CA).

Additional samples were fabricated using lithography, lift-off, and baking processes (Fig.1) to acquire smaller electrode sizes down to 1 μm. For lithography, two types of photo masks (Advance Reproductions Corporation, North Andover, MA), Fig. 2, in conjunction with samples with an initially continuous Pt top electrode coverage were used. First, a positive photo-resist (PR) was applied and spin coated (Spinner CEE100/CEE200X, Brewer Science) on the sample. The samples were then baked on a hot plate at 200°C. After that, the PR film was UV-exposed (in a Mask aligner, MA4, Karl Suss) using mask #1, and the sample was next developed in a PR develop solution (PR developer MF319). After development, the sample was dry etched by a reactive ion etcher (RIE, ICP, Trion, Phantom III) to remove the area of unexposed PR and the mixture film underneath it. PR stripping in a solution (Remover PG) was then processed to remove the remaining PR, and the sample was rinsed in DI water to clean the sample surface.

The cleaned sample next received a coat of SiO_2 dielectric deposited by sputtering. It then underwent another round of processes similar to the above mentioned in order to define the top electrode area and to provide connecting circuitry. First, a negative PR was spin coated onto the sample, the exposed region (defined by mask #2) was developed using a solution PR developer (RD6) and then dry etched by RIE. After PR stripping and rinsing, another PR was deposited on top of the dielectric layer to isolate

the top electrodes from each other. Finally, Au was deposited for connection to the top electrode pads or to the bottom electrode, and the remaining PR was removed. A set of cells fabricated in this way is shown in Fig. 3.

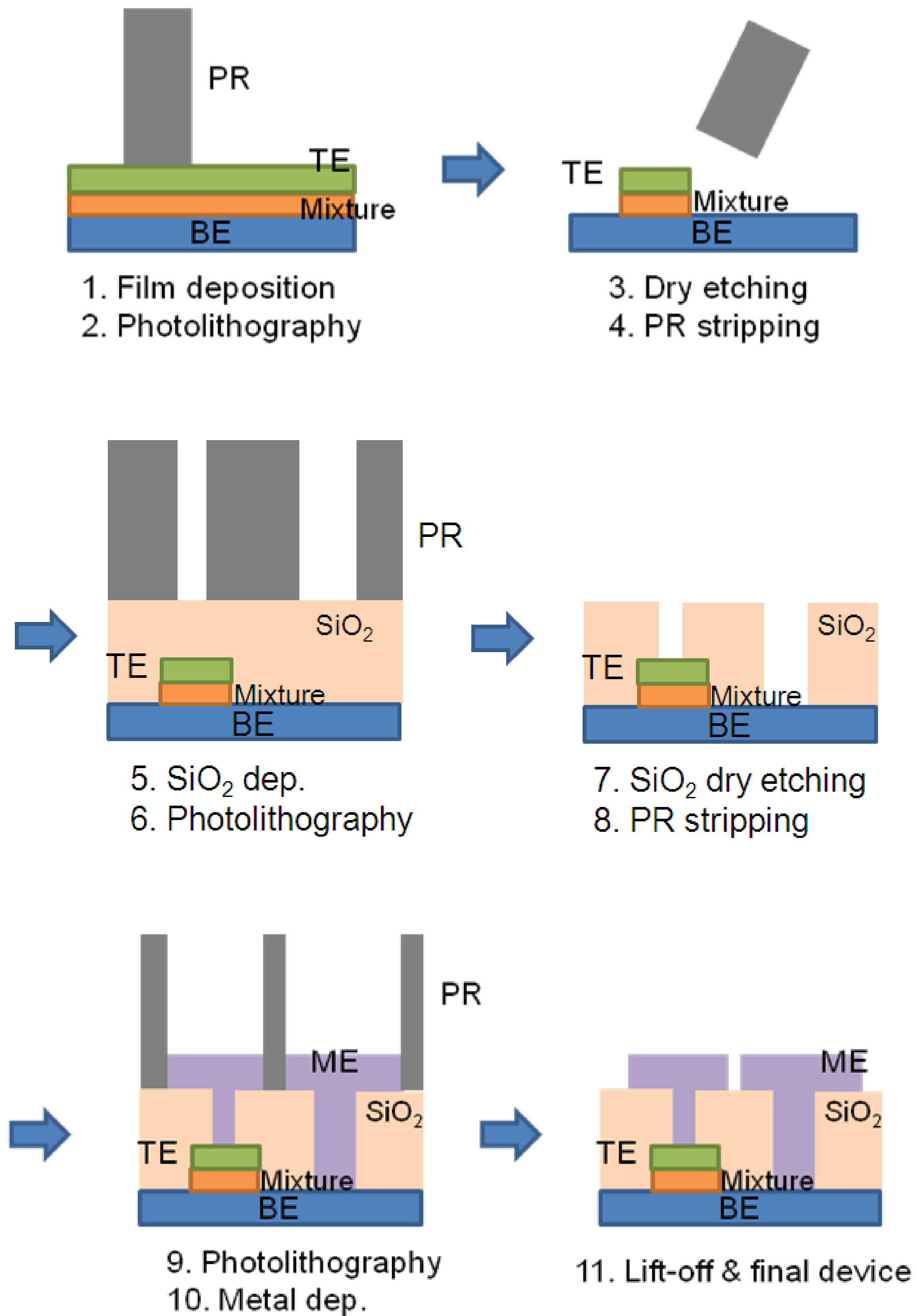

Fig. 1 Micro-fabrication process and structure schematic of device.

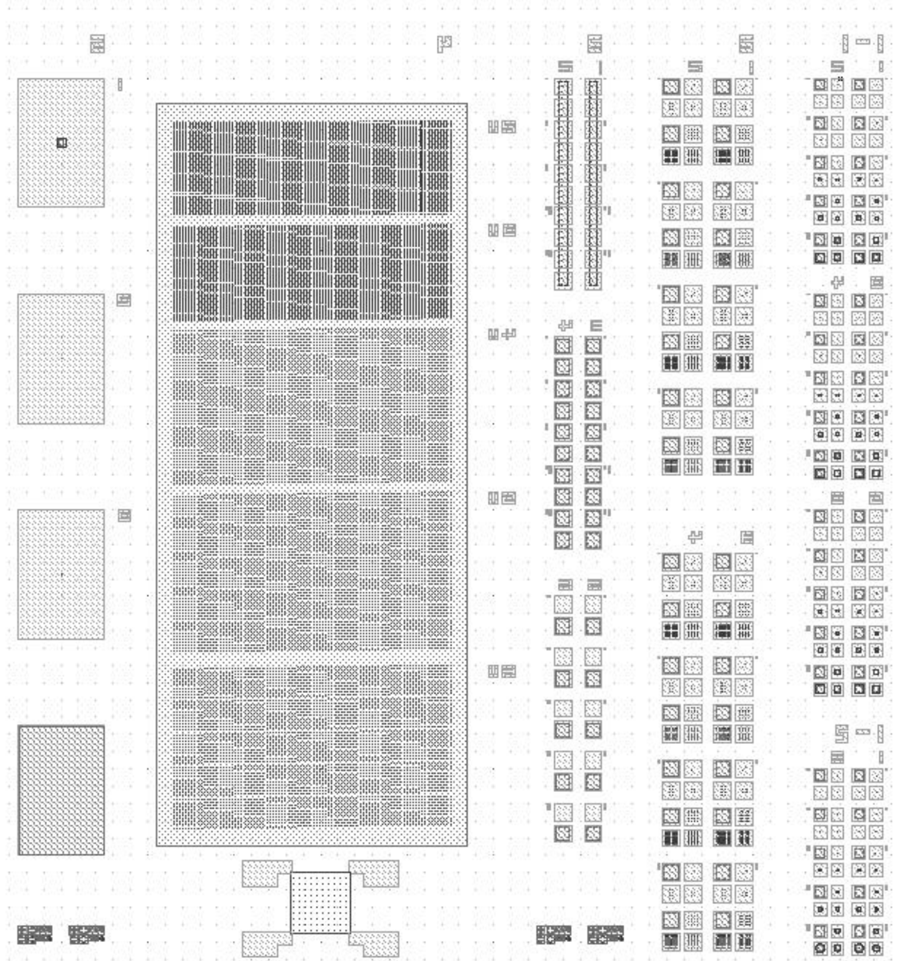

Fig. 2 An illustration of lithography mask used in micro-fabrication process.

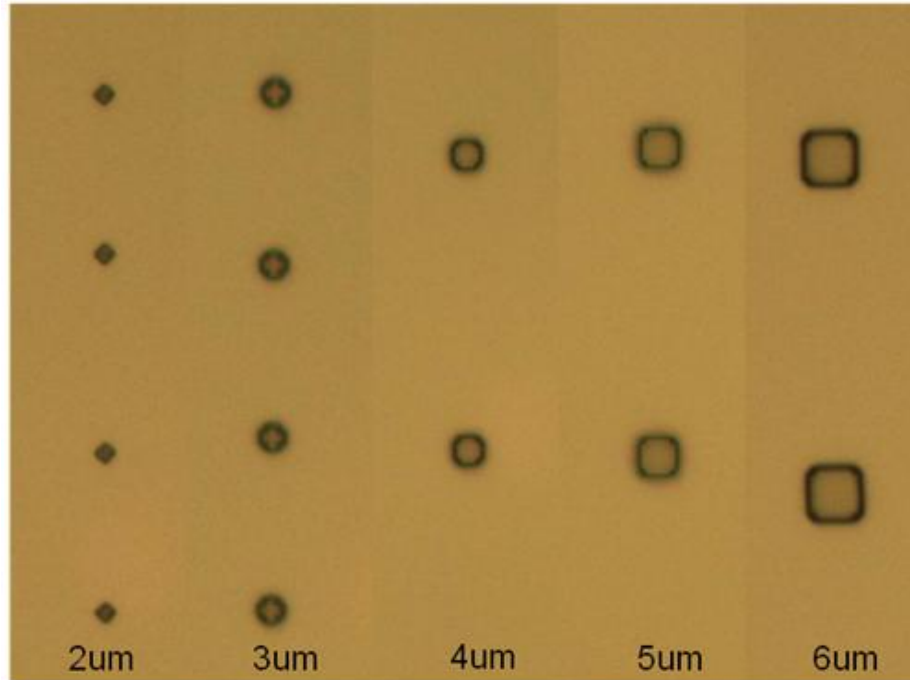

Fig. 3 Cell size of micro-fab patterned device.

III. Results

A. Resistance and yield

In the previous chapter, a map of film thickness δ and Pt fraction *f* was used to delineate the switching zone. In the center of the zone, 100% switching yield is achieved. (The yield was determined by randomly measuring 10~20 cells across the sample, and dividing the number of cells that can reproducibly switch by the total number of cells tested.) In Fig. 4, the HR and LR values (read at 0.1V) are plotted against δ and *f*. The HR increases with increasing thickness or decreasing Pt

concentration, whereas the LR almost remains constant. The device yield and V_{set} (define as the switching voltage from LR to HR) are plotted versus δ and *f* as shown in Fig. 5. The switching yield of a Pt/SiO_2-0.2 Pt/Mo device increases as *f* increases, reaches its highest yield around 12 nm, then decreases. Remarkably, V_{set} (and LR) remains unchanged over all the δ-*f* throughout the switching zone.

In the following sections, samples with a mixture film of SiO_2-0.25 Pt sandwiched between a Pt TE and a SRO or Mo BE are described to evaluate other switching characteristics.

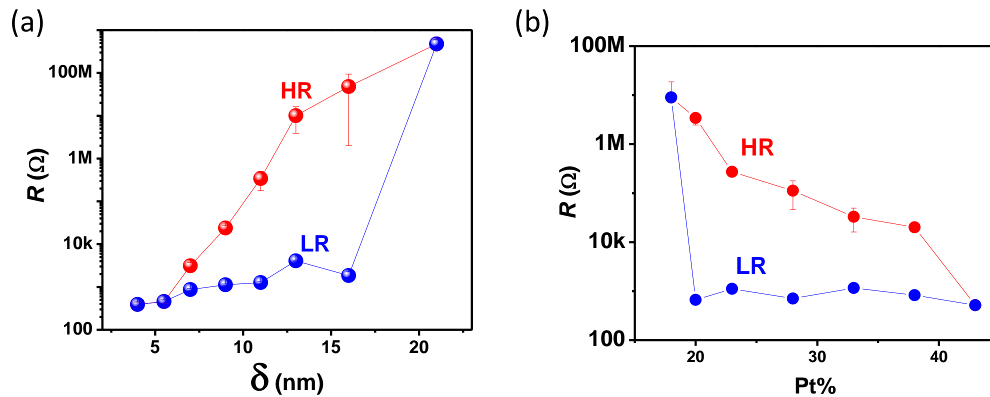

Fig. 4 HR and LR as a function of (a) thickness, and (b) Pt atomic concentration.

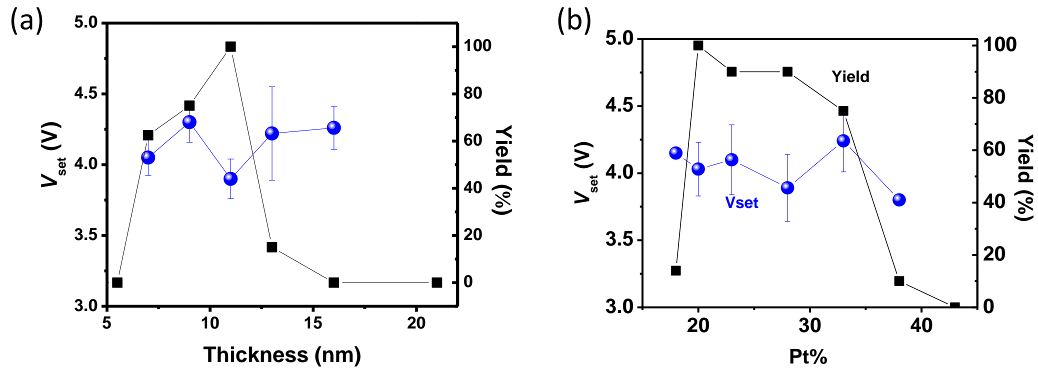

Fig. 5 Yield and V_{set} as a function of (a) thickness, and (b) Pt atomic concentration. Blue symbols denote V_{set}, black symbols denote yield.

B. Retention

The standard voltage-current-sweep test uses voltage segments with a rest (0 V) internal of 300 ms between them. From such test, we are certain that resistance remains stable during the rest period of 300 ms. The following retention test was conducted to further probe the resistance stability over a longer time. In Fig. 6, two cells in the same sample (Pt/SiO_2-0.25Pt/Mo) are first switched, one to the HR state and the other to the LR state, and their resistances are continuously read with a small voltage of 0.2V. (The low reading voltage ensures no disturbance to the resistance state.) To avoid Mo oxidation, these tests were conducted at room temperature. The results shown in Fig. 6(a) confirm that both the HR state and the LR state can be held for at least 300 hours; the LR state is especially stable having almost no change in the resistance value. (In the figure, extrapolation to 100 ks corresponds to 10 years.)

Accelerated retention tests at elevated temperatures were also conducted. In these

tests, the sample is heated to either ~150˚C (for Pt/SiO_2-0.25Pt/SRO) or 85˚C (for Pt/SiO_2-0.25Pt/Mo) for a certain time, then the resistance is measured at 0.2 V at the ambient temperature after the sample is removed from the heater. This heating/measuring procedure is then repeated up to 1,000 hours. As shown in Fig. 6, both the HR and the LR states can hold resistance during the accelerated test. The HR state begins to decay after 20~30 hours when SRO is the BE, but the opposite is observed when Mo is the BE. Meanwhile, the resistance of the LR state remains almost constant for both. From these tests, we may conclude that there is no indication that 10 year retention may be problematic for our devices.

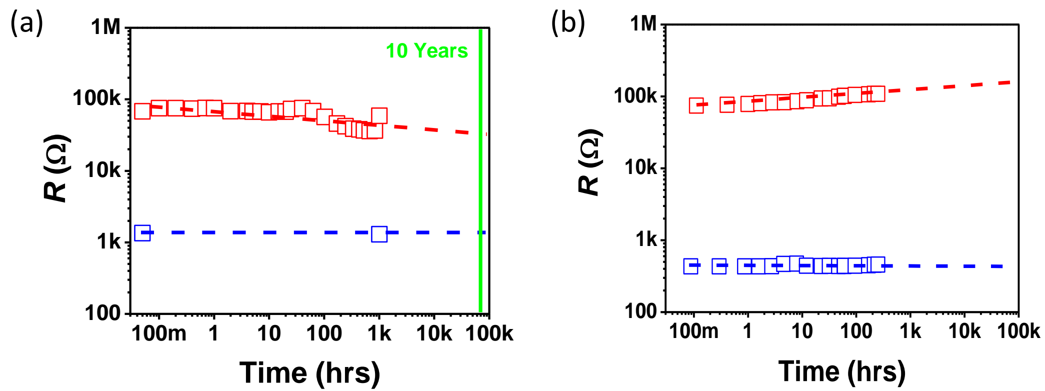

Fig. 6 Retention properties of (a) Pt/SiO_2-0.3Pt/SRO under 150˚C, and (b) Pt/SiO_2-0.3Pt/Mo under 85˚C.

C. Fatigue

Fatigue endurance was evaluated by the following method: an alternating positive +5V pulse and a negative -4V pulse are applied, designed to cause set and reset switching, respectively, and between these two pulses the resistance was measured at a small sensing voltage (0.2V). Here, each write-and-erase combination counts as one cycle. The results in Fig. 7 shows little fatigue of the HR state after 16000 cycles in both SRO and Mo BE cases. Although there is resistance fluctuation, it is much smaller than those reported for RRAM in most literature[24,25,26].

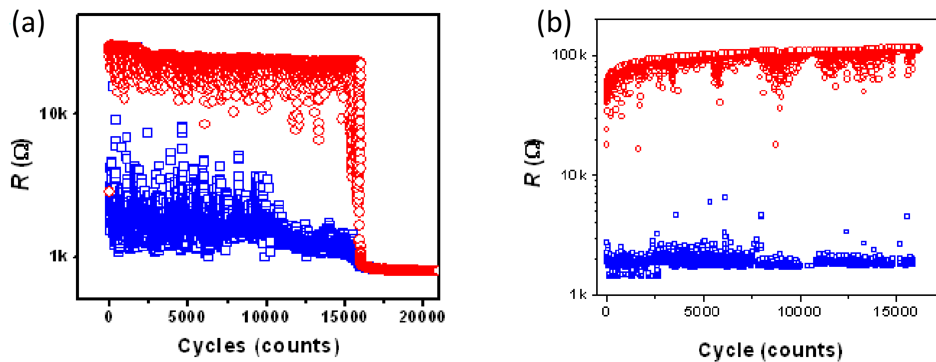

Fig. 7 Fatigue test of (a) Pt/SiO_2-0.3Pt/SRO, and (b) Pt/SiO_2-0.25/Mo devices.

D. Cell area

Cells with various top electrode sizes were examined to determine the area dependence of the HR and LR values. Our shadow mask has four different diameters: 70 μm, 91 μm, 112 μm, and 168 μm. Lithography further provides cell areas ranging

from 1 μm to 100 μm. For each cell size, 10 cells are measured, those that exhibit stable resistance switching are selected and their resistances are read at 0.1V. The HR of both Pt/SiO_2-Pt/SRO and Pt/SiO_2-Pt/Mo samples shows a linear dependence on the reciprocal cell area, Fig. 8. However, the LR state has a relatively weak area dependence. The cell size dependence of the Pt/SiO_2-Pt/Mo device shows better statistics than that of the Pt/SiO_2-Pt/SRO device. This may be attributed to the surface roughness: Mo BE is smoother than SRO BE. Overall, our SiO_2-Pt devices exhibit a much stronger cell size dependence than that of the filamentary type RRAM[15,27,28], which shows almost constant HR and LR resistance over a wide range of cell area.

The reason that the LR resistance is insensitive to the cell area is that the true LR state has a resistance much less than the apparent resistance. The latter is mostly attributed to the BE and the spreading resistance, which has a weak (logarithmic) area dependence. In addition, since the as-fabricated cells are in the LR state, most cells are "short circuits" to their top electrodes, further weakening the "single cell area" dependence of the spreading resistance.

The switching voltages as well as the yield of the device are constant independent of the cell size.

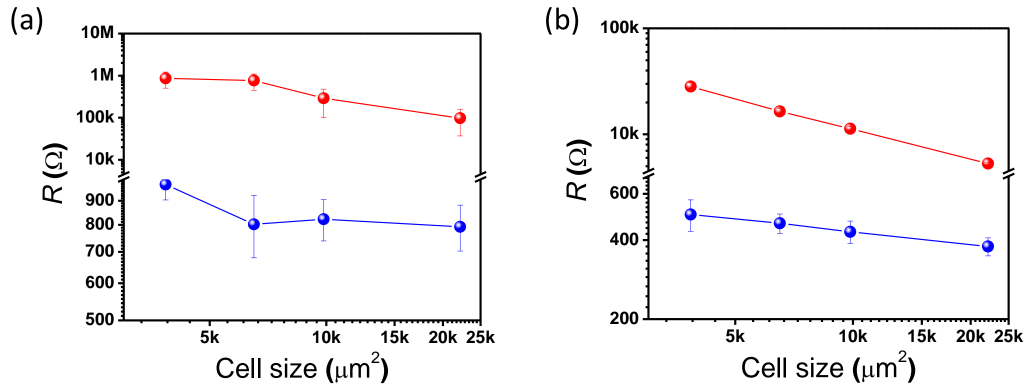

Fig. 8 HR and LR cell size dependence in (a) Pt/SiO_2-0.25Pt/SRO, and (b) Pt/SiO_2-0.3Pt/Mo.

Similar results were obtained for samples with lithographically fabricated top electrodes, Fig. 9: the HR shows a linear dependence on the reciprocal cell area, the LR shows negligible dependence, even weaker than seen in the previous samples. The latter observation may be attributed to oxidation of Mo BE during the microfabrication process, which further increases the ratio of the BE/spreading resistance to the LR resistance. The resistivity calculated for these cells shows a constant resistivity for the HR state, suggesting sample uniformity. Over these cell sizes, the switching voltage remains constant. As a result, the R-V curves expand vertically as the cell size decreases, with no changes to switching voltage and to the LR value.

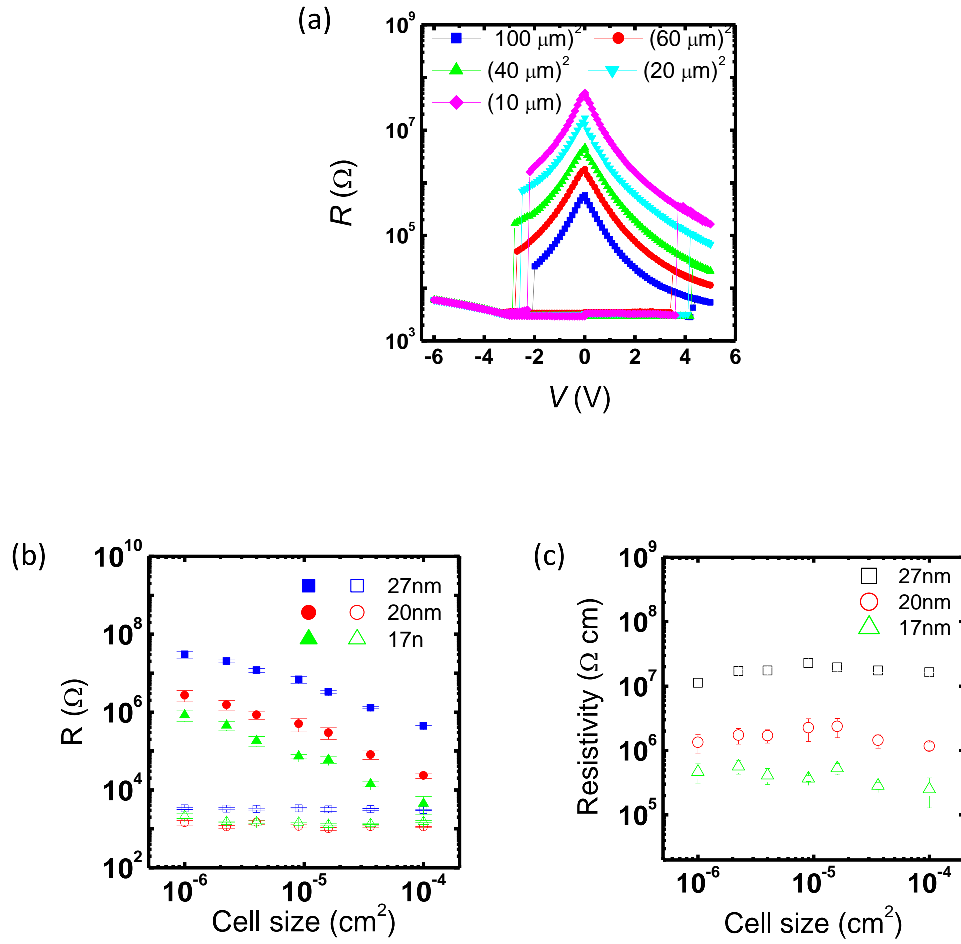

Fig. 9 (a) R-V curves of different cell size of a Pt/SiO_2-0.3Pt/Mo device with micro-fabricated cells, (b) HR and LR cell size dependence in Pt/SiO_2-0.3Pt/Mo device, and (c) HR state resistivity as a function of cell size.

E. Switching speed

Switching triggered by voltage pulses (Agilent 81104A, Pulse Pattern Generator) of different widths was performed to determine the write/erase speed of the memory device. A series of voltage pulses of increasing amplitude in either the positive or the negative polarity is applied, and switching is monitored by measuring the resistance at

0.2 V after each pulse. This procedure is used to find the switching voltage for each pulse duration starting with 10 ms pulses. After a set of the switching voltages is found, the pulse width is reduced by a factor of 10 after the cell switches, and the search for the switching voltages continues, and the procedure repeats itself until the pulse width is reduced to 25 ns. Figure 10(a) shows the R-V plots of three such cycles, at three pulse widths, in a Pt/SiO_2-0.3Pt/SRO cell. Another example for a Pt/SiO_2-0.2Pt/Mo cell is shown in Fig. 10(b) for comparison. The plots has a rectangular R-V shape due to (a) abrupt switching within one pulse after the voltage increment, and (b) constant R values read at 0.2 V. The fastest switching time is 25 ns for Pt/SiO_2-0.25Pt/SRO device and 50ns for Pt/SiO_2-0.25Pt/Mo device.

Figure 11 shows the set/reset voltage dependence on the pulse width. These voltages show little increase until the pulse width is shorter than 100 ns, below that the set/reset voltage increases with decreasing pulse width. This sudden increase is probably related to the RC time constant of the circuit. As shown in Fig. 11(c) for a pulse profile programmed to be a square pulse lasting 100 ns, there is a distortion/delay during much of the first 100 ns, reaching the programmed value after 75 ns.

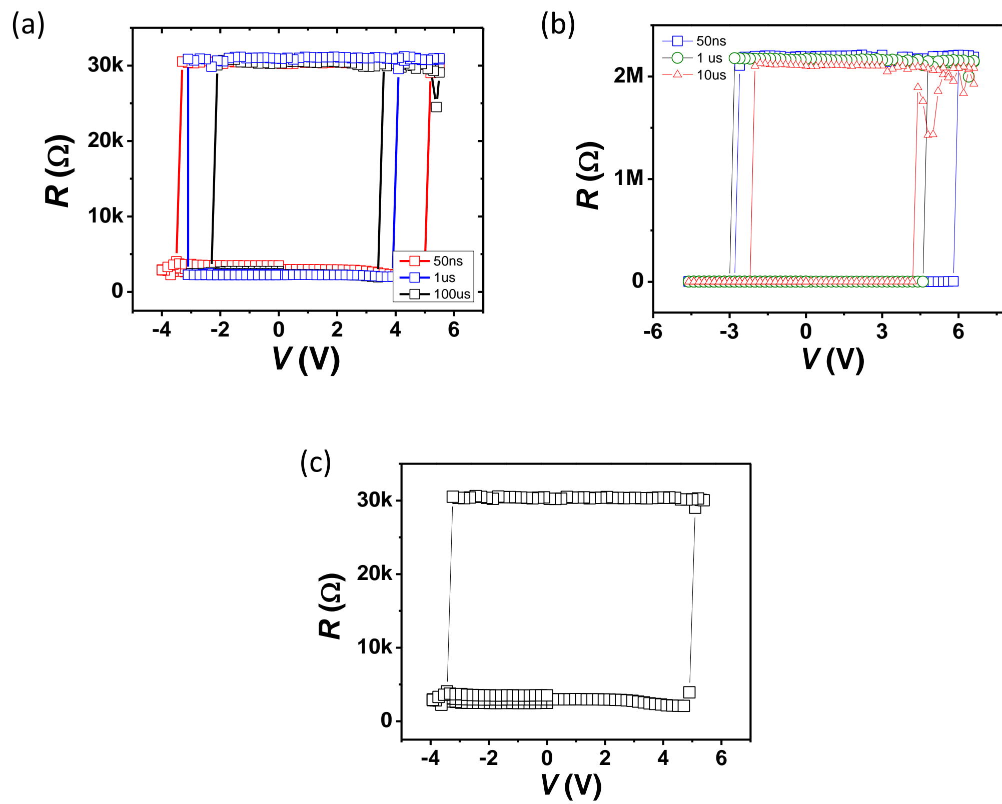

Fig. 10 R-V curves of different pulse width for (a) Pt/SiO_2-0.3Pt/SRO, (b) Pt/SiO_2-0.2Pt/Mo, and (c) fastest switching speed obtained in Pt/SiO_2-0.3Pt/SRO, using 25 ns voltage pulses.

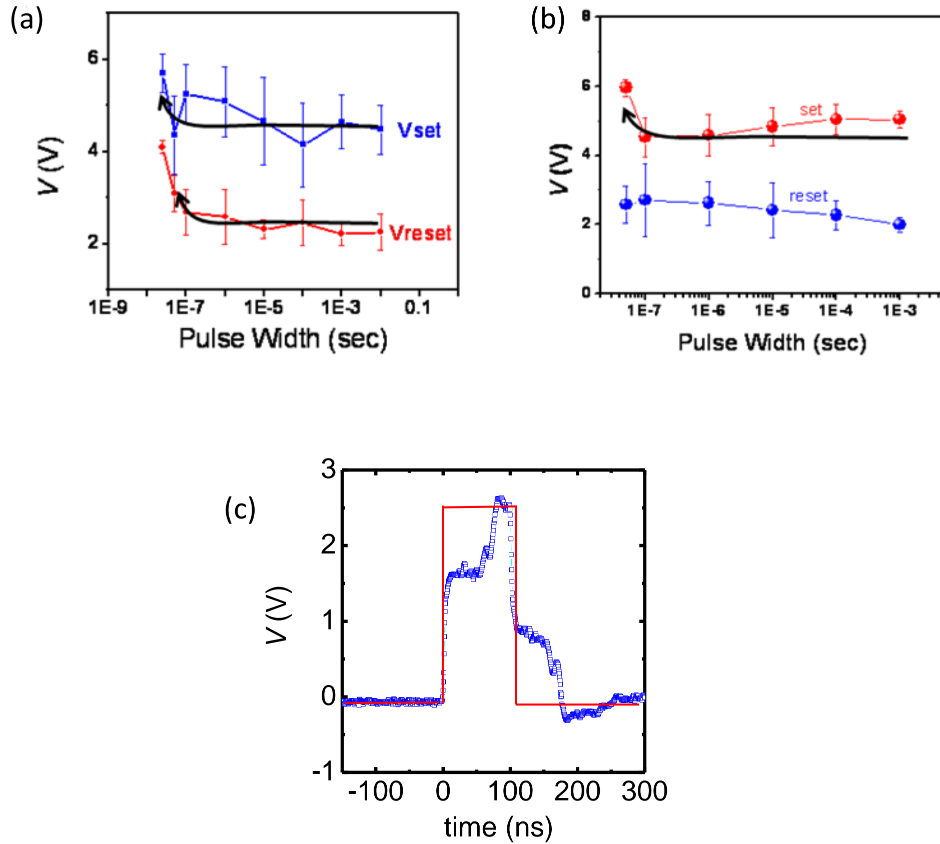

Fig. 11 Switching voltage as a function of pulse width for (a) Pt/SiO_2-0.3Pt/SRO, and (b) Pt/SiO_2-0.2Pt/Mo devices; (c) a standard electric pulse showing distortion due to RC time delay in the first 100 ns.

F. UV irradiation effect

In thin films, even a small voltage can lead to a large field (~10^6V/cm in our case), which could trigger ionic and (metallic) atomic migration. To avoid such a field, which is required to trigger ion movement, UV experiments were performed on a Pt/SiO_2-Pt/SRO device. The UV light source (ELC-403, Electro-Lite Corp., Bethel,

CT) used has a wavelength of 300-420 nm (4.2-3.0 eV), with an output power of at least 70 mW/cm^2 at 3.4 eV. Since Si is opaque to UV, fused SiO_2 was used as the substrates so that UV could be shone from below. The films deposited on quartz and fused SiO_2 show no structural differences compared to those on a Si wafer. The device also has the same switching I-V behavior as the standard device on Si. A cell is first switched to a HR/LR state, monitored for 20 seconds to ensure no fluctuation of resistance. Next, the UV light is turned on for ~120 seconds before it is turned off, and the resistance is monitored using four configurations: (1) the cell is connected to a Keithley 237 meter providing a reading voltage of 0.2 V; (2) the cell is externally shorted between the top and the bottom electrode by a connecting wire; (3) the cell is floated without any connection; and (4) the top or the bottom electrode is grounded with the other one floated. The four configurations show the same phenomena: the LR state shows no change after UV irradiation, whereas the HR state switches to the LR state after the UV irradiation. Therefore, electronic switching is confirmed. (In configuration (1), an instant resistance change is confirmed. In other configurations in which the cell is not connected to the measurement circuit, the resistance change is confirmed after the 120 s irradiation.) The same results were also observed in a Pt/SiO_2-Pt/Mo device (Fig. 13). To avoid the influence of persistent photocurrent[29,30], which can also lowers the resistance but only transiently, we continued to monitor the

resistance up to 200 hours after the UV experiment. No return to the HR was found (Fig. 13(b)) . This confirms that there is indeed an UV-triggered HR to LR transition. The UV energy used is centered in the range of 3.0 – 4.2V, which is less than the work function of Pt (5.6 eV), Mo (4.6 eV), SRO (5.0 eV) and the band gap of SiO_2 (8.9 eV). However, the highest energy emission of a Hg lamp is 184 nm or 6.7 eV. Therefore, there is a weak component of the UV light that is capable of exciting electrons in Pt, Mo, and SRO from their Fermi level to the vacuum. (It is not sufficient to excite electrons in SiO_2 from its valence band to the conduction band.)

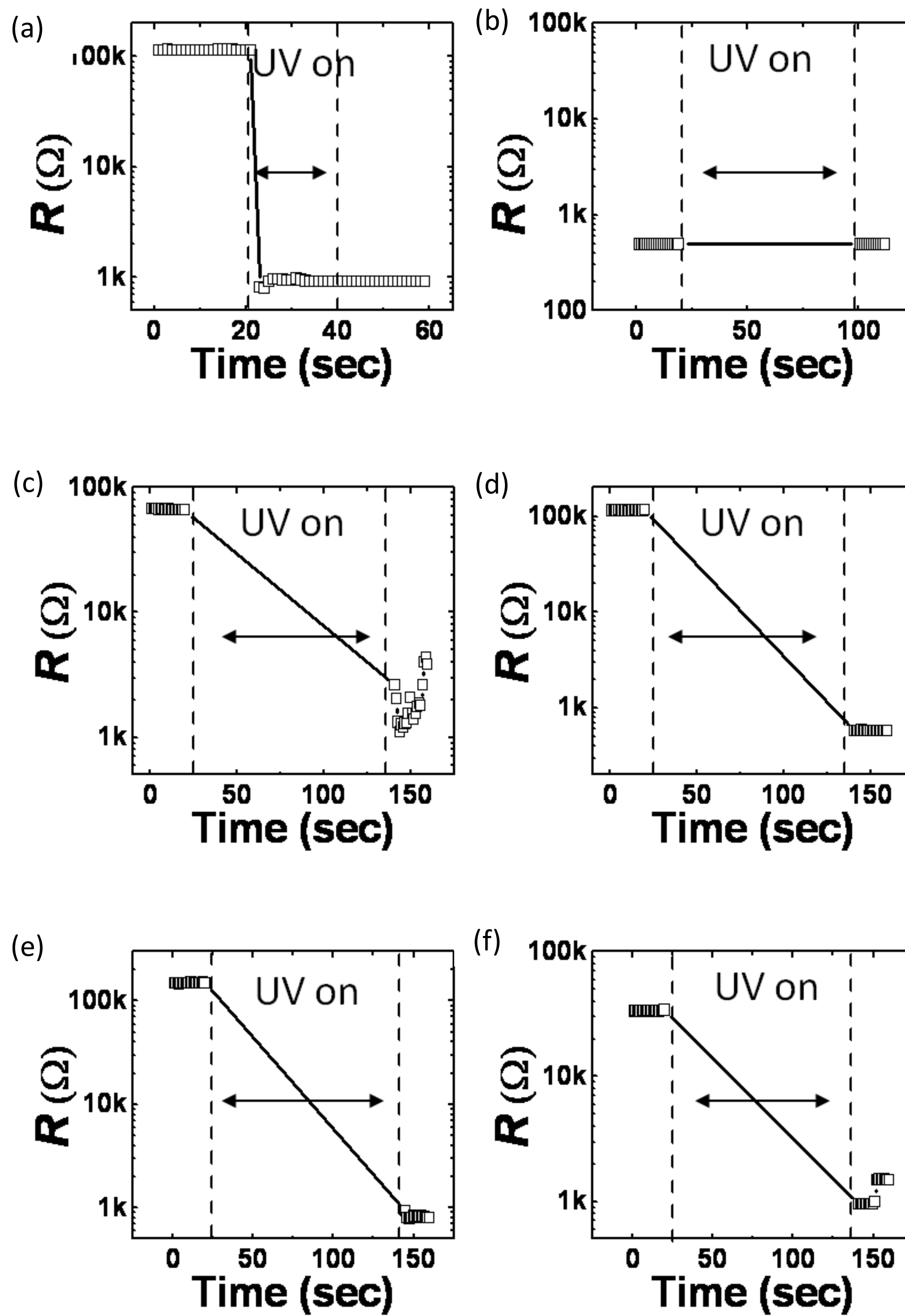

Fig. 12 UV experiment of Pt/SiO_2-0.25Pt/SRO HR state and LR state under different configurations, (a) initially HR state: TE/BE in series with Keithley, (b) initially LR state, (c) initially HR state: TE/BE shorted, (d) initially HR state: TE/BE floated, (e) initially HR state: TE floated, BE grounded, (f) initially HR state: BE floated, TE grounded.

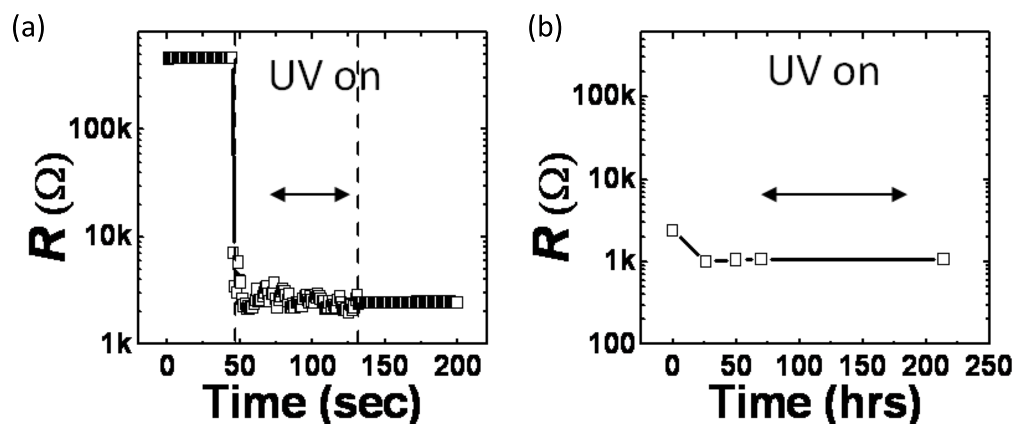

Fig. 13 (a) UV experiment of Pt/SiO_2-0.25Pt/Mo HRS, (b) photocurrent has no effect on resistance after 200 hours of waiting.

We also investigated the effect of UV irradiation on the Pt/SiO_2-Pt/Pt device. In the preceding chapter, we reported observing Pt/SiO_2-Pt/Pt switching to the HR state but not switching back to the LR state. This is shown in Fig. 13: the device has a low initial resistance (IR) and it switches to the HR state at a negative "set" voltage (Fig. 14(a)). The device is confirmed to be stuck at the HR state and cannot be switched back to the LR state by a voltage (Fig. 14(b)). Next, UV irradiation is turned on. The device promptly returns to the LR state (Fig. 14(b)), and the LR state can be switched to the HR state again (Fig. 14 (c)).

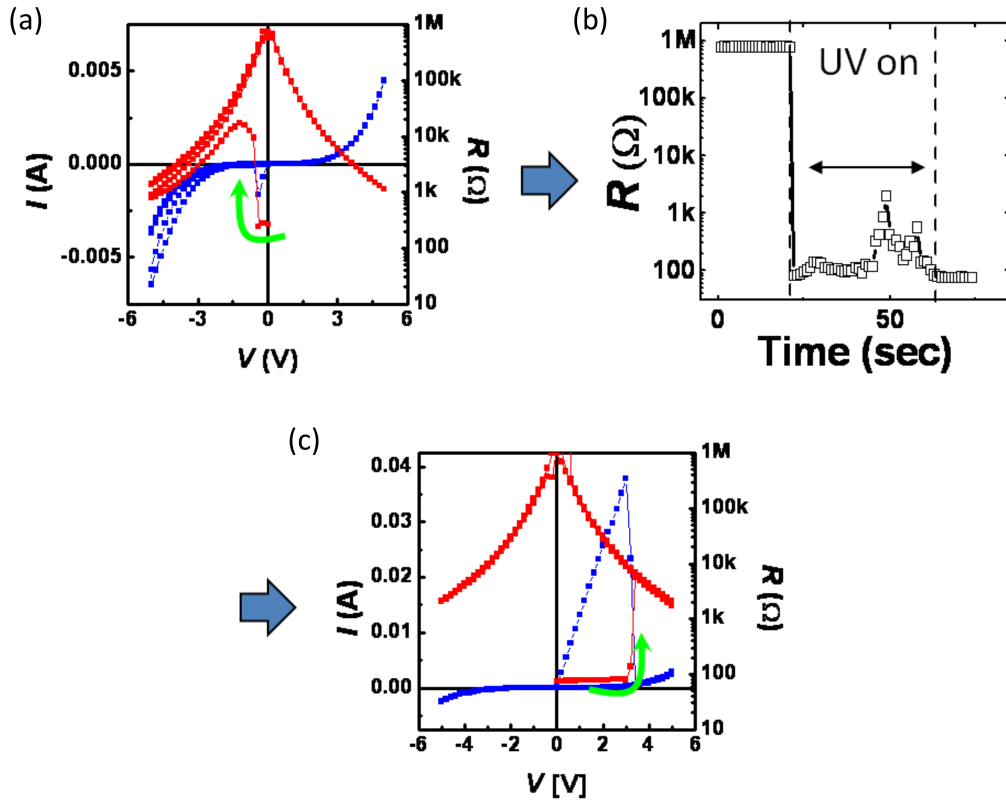

Fig. 14 (a) Voltage-triggered resistance switching from LR to HR (negative bias) in Pt/SiO_2-0.25Pt/Pt device, (b) UV-triggered resistance switching from HR back to LR, (c) voltage-triggered resistance switching again in the same cell from LR to HR by positive bias.

G. Annealing

The effect of annealing was examined by annealing the samples at various temperatures, 150, 250, 400 and 550℃, for one hour. After annealing, sample thickness was found to slightly decreased (Fig. 15), the set voltage and the LR changed little (Fig. 16(c)), but the HR significantly decreased (Fig. 16(b)). This might be due to the removal of defects allowing more conducting paths in the cell and fewer

sites for charge trapping. (If the trapping sites are associated with locations of dangling bonds or of metastable configurations of SiO_2 polyhedra, then it is likely that their density will decrease during annealing, especially in view of the density increase/thickness decrease.) The switching voltage, however, remains almost constant (Fig. 16(a)). These results are very different from those reported for filamentary- or redox- based RRAM, which shows a large increase of the HR or switching voltage with increasing annealing temperature or annealing time[31,32].

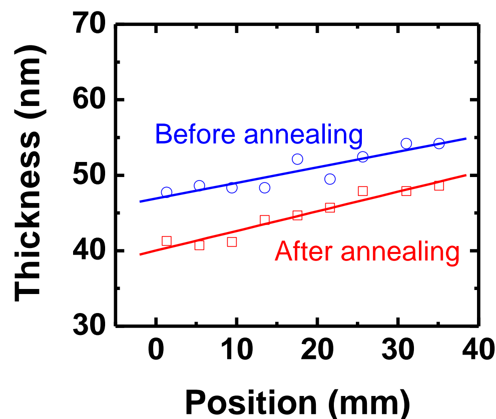

Fig. 15 Sample thickness before and after annealing (annealing condition: 550°C for 1 hour), position indicating measurement from one end of the sample to the other end.

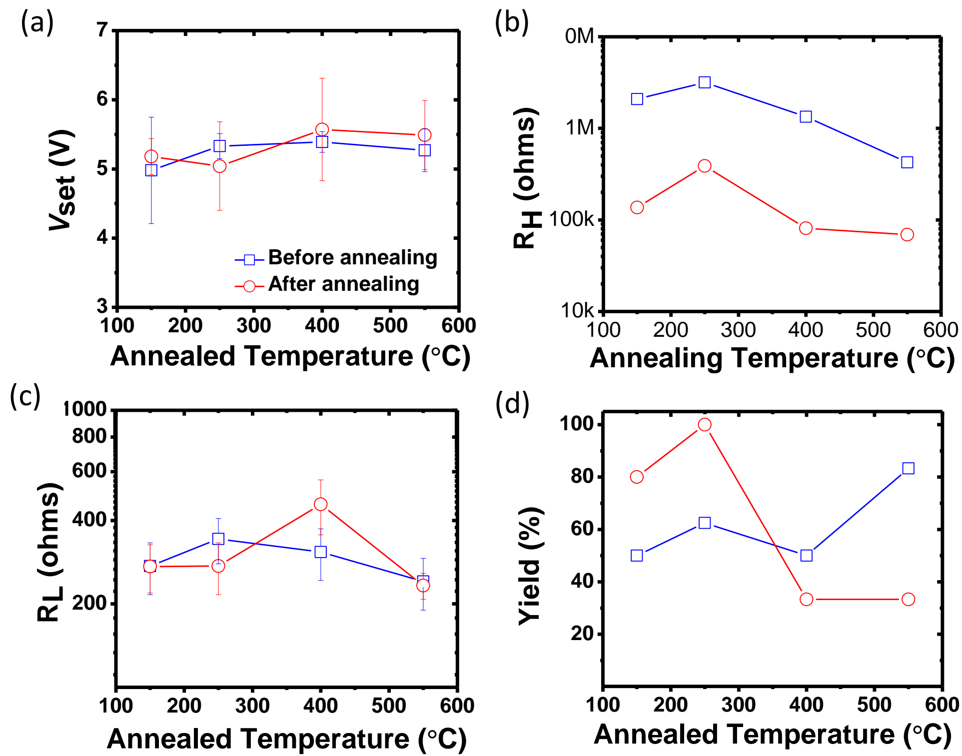

Fig. 16 Annealing effects on (a) V_{set}, (b) HR, (c) LR, and (d) yield.

H. Breakdown

Breakdown is expected at high voltages. Because of set switching, at a large positive voltage only the HR state remains. Conversely, because of reset switching, at a large negative voltage, only the LR state remains. Therefore, voltage (V_{BD}) was measured under a negative bias for the LR state, and a positive bias for the HR state. Breakdown occurs at about 10 V in either polarity (Fig. 17) for a *f*=0.30 film of 20 nm thickness. Breakdown was often accompanied by visible physical damages of the cell, such as bursting of the top electrode. Fig. 18 is a secondary electron microscopy

(SEM) image of the burst electrode; the cell, during breakdown, experiences bubble formation and becomes dark. After breakdown, the cell appears shorted with a resistance even lower than that of the LR state. (Not surprisingly, it cannot be switched anymore.)

The breakdown voltage appears to increase as the film thickness increases. However, despite the voltage increase, the breakdown field actually decreases. This is not surprising since it is common that the breakdown strength increases as the film thickness decreases. (It is commonly explained in terms of defect statistics, which is scarcer in smaller volume.) Since the breakdown voltage much exceeds the operating voltage, it does not present any limitation to the normal RRAM operation.

The observation that breakdown is usually accompanied by certain darkening or bubbling of the top electrode, as shown in Fig. 18, suggests a possible role of gaseous species. If so, it might be prevented if an hermetic seal is incorporated to isolate the device from the atmosphere. Indeed, we found that breakdown/bubbling will not occur when a thin Al_2O_3 (or AlOx) capping layer is deposited on top of the device. This suggests that breakdown is caused by the external atmosphere (for example creation of oxygen vacancies or the supply of H_2O)—though it requires a voltage to operate, it is not an intrinsic property, and it can be prevented.

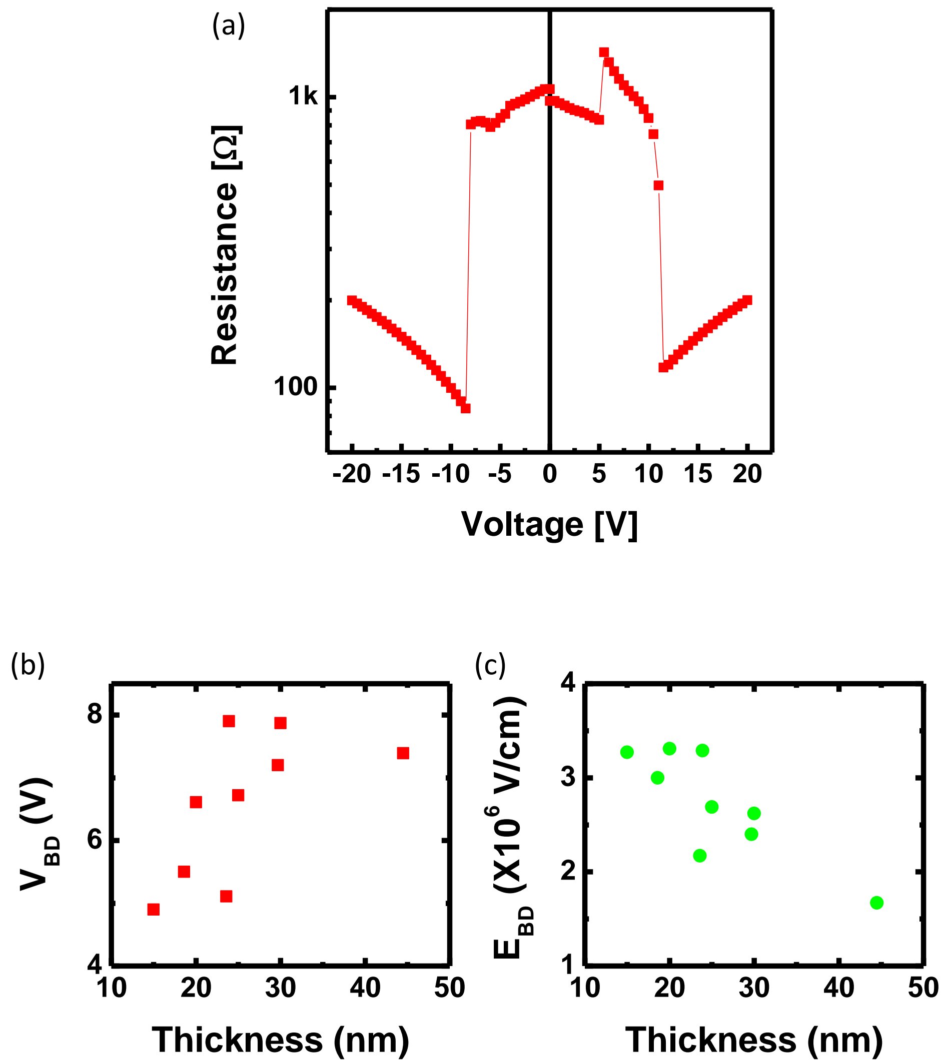

Fig. 17 (a) Breakdown phenomenon of a Pt/SiO_2-Pt/SRO device in both positive and negative bias, (b) negative breakdown voltage as a function of film thickness, (c) negative breakdown field as a function of film thickness.

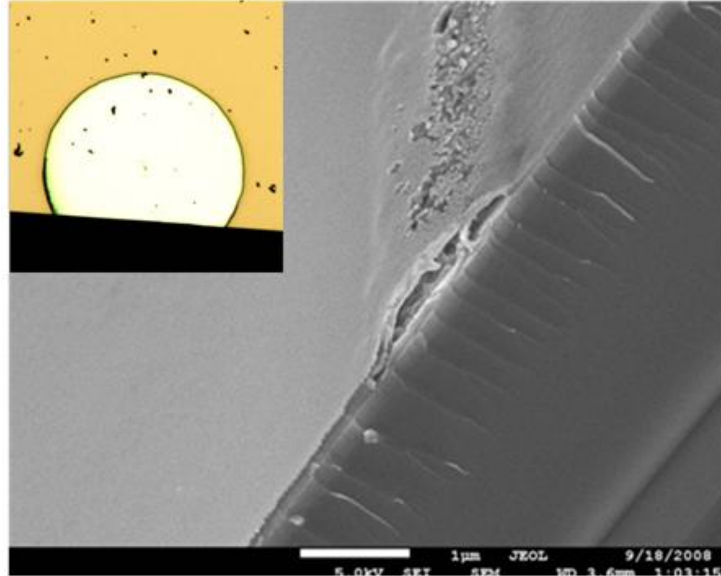

Fig. 18 SEM image of a breakdown cell having dark ring and bubbles on the TE edges of Pt/SiO_2-Pt/Mo, inset: optical microscope showing darkening at the edges.

I. Interface engineering

The initial, as-fabricated state of a Pt/SiO_2-Pt/SRO device is usually in the LR state. For a Pt/SiO_2-Pt/Mo film, the cells sometimes have a high initial resistance (IR) but it can be easily brought to the LR state through a very small voltage (< - 1 V), see Fig. 19(a). The low breakdown voltage suggests that the high resistance is probably due to a very thin layer on the Mo electrode, which may be attributed to an oxidized Mo/mixture interface. This interpretation is also consistent with our observation that in the Pt/Si_3N_4-Pt/SRO and Pt/SiO_2-Pt/Pt systems, the IR state is always the same as the LR state. Moreover, UV irradiation has no influence on the IR: the IR shows no change in resistance before and after UV irradiation (Fig. 19(b)). Therefore, the IR

state is not due to charge storage, as in the case of the HR state.

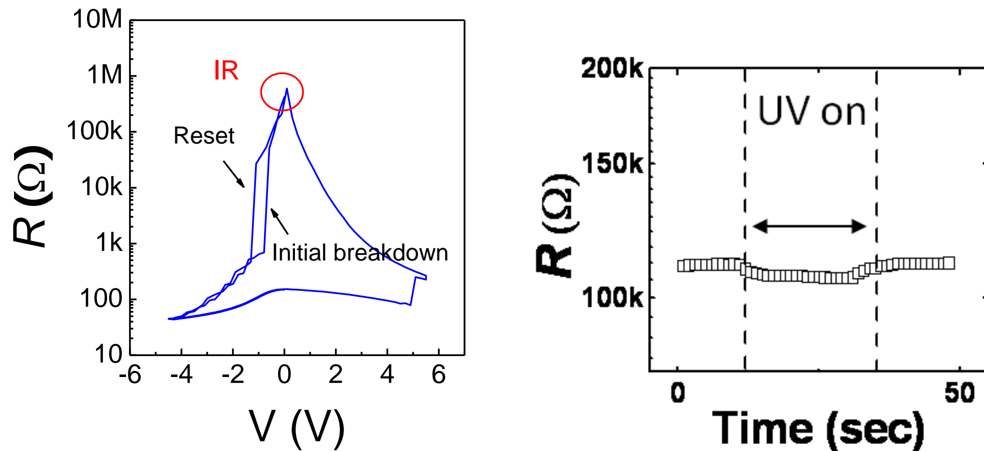

Fig. 19 (a) Initial breakthrough of IR of the as-fabricated device, and (b) UV irradiation of IR.

In Fig. 20(a), we investigate this IR state as a function of Pt concentration: the IR decreases as the Pt concentration increases. Furthermore, this IR state can be suppressed by lowering the chamber pressure down to low 10^{-7} torr, or by inserting (pre-depositing Pt before the mixture layer deposition) a thin Pt layer approximately 1 nm thick at the Mo/mixture interface. As shown in Fig. 20(b), this procedure can lower the initial resistance of the Pt/SiO_2-Pt/Mo from over 100 kΩ to about 200 Ω. The procedure has little influence on resistance switching. (However, a Pt coating of more than 3 nm thick will render the device not switchable, since it results in a configuration of symmetric electrodes.) In Fig. 19(a) and 20(c), a comparison is made between a device with 1 nm Pt overcoat on the Mo BE, and a device without the overcoat but after (low voltage) breakage of the barrier resistance. These observations

are all consistent with our interpretation of oxidized interface.

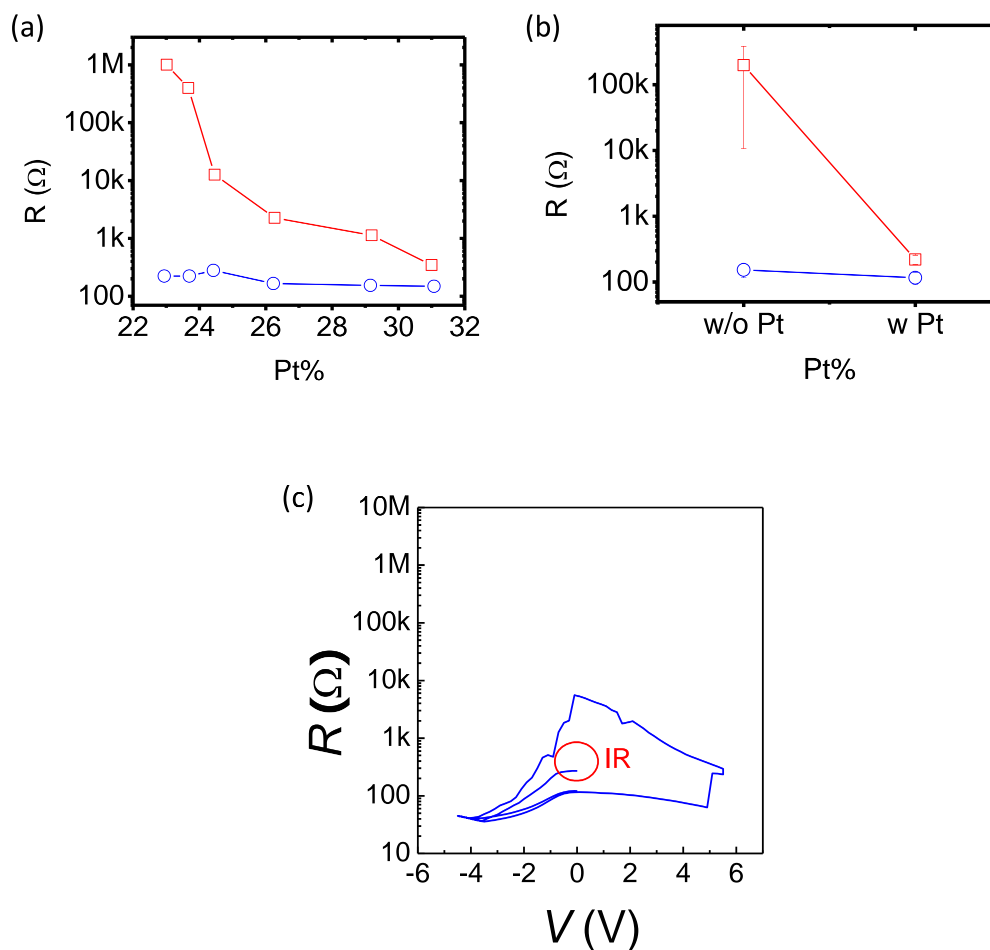

Fig. 20 (a) Pt concentration effect on IR (red) and LR (blue) of a Pt/SiO_2-Pt/Mo device, and (b) A comparison of IR (red) and LR (blue) with and without a 1nm thin Pt layer in between mixture/Mo interface. (c) IR of a device with Pt overcoat on Mo BE.

IV. Discussion

A. Ionic or electronic?

In ion-movement dictating RRAM, rupture of conducting filaments that involves either metal or oxygen (vacancies) migration has often been proposed[14,15]. This mechanism is found power-intensive: a high local temperature is thought to be needed, which implies a voltage-dependent incubation time for switching[15, 33]. This is evidenced in the switching voltage, which typically increases when the switching time is shorter than 1 μs.[15] In contrast, our switching time is independent of the pulse time down to the RC time limit of the circuit. This is consistent with our picture that our device switches via an electronic mechanism.

Temperature dependence provides another means to differentiate switching mechanisms. Switching temperature should play an important role in ion-based switching mechanism since ion movement is strongly thermally activated. However, localized Joule heating, which plays an important role in filamentary switching[34,35], may obscure the temperature effect since the local temperature due to Joule heating may well exceed the ambient temperature by a large amount[36]. In contrast, switching in our material is relatively insensitive to temperature, as already evident from the comparison of the retention data with and without thermal activation. Later in Chapter 6, we will show that switching can still be observed at 10K, at essentially the same

switching voltage.

The fact that the HR state can be triggered to switch to the LR state by UV irradiation implies that (a) switching is possible without a field, hence without ion movement, and (b) switching is possible with electron/hole supersaturation, without any thermal activation of ions. There has been recent reports that UV can also trigger resistance switching in TiO_2/molecular junction[34] or in Cu_xO broken filaments[35], when the electrode is in intimate contact with these junctions or filaments. This implies that UV can enable short-range redox reactions if facile electronic transfer (supply and removal) can be provided locally. In our device, nanometallicity naturally provides the pathways for such electron transfer: electrons released from the trapped sites during UV irradiation are immediately drained through the nanometallic paths nearby. This allows the material to permanently return to the LR state without the risk of electron retrapping which may occur if nanometallicity is not available.

B. Interface or bulk?

There are typically two types of interface switching mechanisms: Schottky barrier[37] and interface oxygen vacancy creation/diffusion[38,39]. We already excluded the oxygen vacancy mechanism, which is an ionic mechanism discussed in the previous section. The Schottky barrier model states that charge trapping/release at the interface

regulates the height of the Schottky barrier, which is typically ~ one unit cell thick[40]. The behavior of our device is inconsistent with the predictions of this mechanism in several respects. First, the I-V curves of both the HR state and the LR state are antisymmetric in voltage, whereas the Schottky barrier mechanism predicts a rectifying I-V behavior. Second, the as-fabricated state and the LR state both have a linear I-V behavior, which is also inconsistent with the Schottky barrier mechanism which predicts a highly non-linear I-V curve. Third, the HR has an extremely strong dependence on thickness, whereas the Schottky barrier mechanism should allow no thickness dependence. Therefore, our devices must operate by a bulk mechanism. This conclusion is also consistent with the strong area and thickness dependence of the HR of our devices.

C. Anisotropic resistance in vertical(thickness) and horizontal(cell area) directions

We have shown that HR exhibits an exponential thickness dependence in the previous chapter. This sensitive feature may allow the use of thickness as another means to tailor the device characteristic, such as device resistance and resistance ratio during switching. Meanwhile, the transverse resistance is very large, meaning cells are isolated from each other laterally if there is no communication via the common

bottom electrode. Such extreme resistance anisotropy may have interesting consequences on device design and operation.

V. Conclusion

1. In summary, we have demonstrated reproducible bipolar resistivity switching of the SiO_2-Pt device. The switching is purely electronic: the insulator to metal transition can be triggered by UV irradiation, which can be explained by detrapping electrons from the mixture film.
2. In addition, it is a bulk switching mechanism rather than an interface switching phenomenon, given the symmetric, linear I-V behavior.
3. The yield can reach 100% in device fabrication once the Pt concentration and the film thickness are optimized.
4. The fastest switching speed achieved so far is 25 ns, which is presently limited by circuit's RC time, below which the excitation voltage pulse is distorted and does not rise to the prescribed value promptly.
5. The device can retain their resistance state giving no indication of decay, it also possess constant switching parameters during repeated switching and under different switching modes.
6. Moreover, when a hermetic seal is introduced, there is no voltage-induced

breakdown at voltages that well exceed the values required for switching operation. These excellent intrinsic properties augur well for the consideration of our device as a strong candidate for future RRAM devices.

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Chapter 5 Multilevel Switching and the Switching Model

I. Introduction

In previous chapters, properties of the SiO_2-Pt resistive-switching random access memory (RRAM) device were studied focusing on bistable switching. The device shows promise in features such as high operation speed, low power consumption, and long retention time, which are desirable for extending the Moore's law and for following the International Technology Roadmap for Semiconductors to achieve high storage density[1,2]. For further improvement, it would be desirable to have a multilevel cell (MLC), which can increase the storage density, as already demonstrated in NAND flash memory[3]. While a cross-point memory cell requires a footprint of $4F^2$, where F is the smallest lithography dimension possible in current technology, a two-bit-per-cell MLC NAND flash memory occupies an effective footprint of $2F^2$, which doubles the storage density.

In recent RRAM literature, multilevel switching has been reported for several types of materials, including, for example, NiO[4], Ta_2O_5/TiO_2[5], TaO_x[6] and Cr_2O_3[7]. In the TaO_x case, intermediate resistance state (IRS) can be obtained by either applying a voltage slightly smaller than the V_{set} (switching high resistance to low resistance, or HR to LR), or a voltage slightly greater than V_{reset} (switching LR to HR). It is thought

that there are two tantalum oxides, Ta_2O_5 and TaO_2, with TaO_2 having a narrower band gap, which is more conducting[6]. In the NiO case, the intermediate resistance states have been associated with different defect concentrations/configurations in the active layer[4].

In this chapter, we explore the feasibility of MLC in our device. Multiple resistance states are indeed observed, most readily during the HR to LR transition. Controlling the current compliance or negative bias allows the use of lower switching voltages. Indeed, there appear to be a continuum of intermediate states that can be accessed by varying the current or voltage in the negative bias. We will also apply this technique to analyze film switching behavior with the aid of a simple circuit model.

Another aspect to be explored in this chapter is the so-called complementary resistance switching (CRS). As mentioned in Chapter 1, bipolar resistance switching devices suffer from a "parasitic-path-problem" in the crossbar configuration, which is schematically illustrated in Fig. 1. A current reading the resistance of cell 1, which is in a high resistance (HR) state, can actually pass through cells 2, 3, and 4 that are in a low resistance (LR) state, thus obtaining a low resistance readout. To overcome this problem, Linn, et al. proposed a CRS element [8], connects two bipolar resistive switching elements, both in the HR state, back-to-back, as shown in Fig. 2.

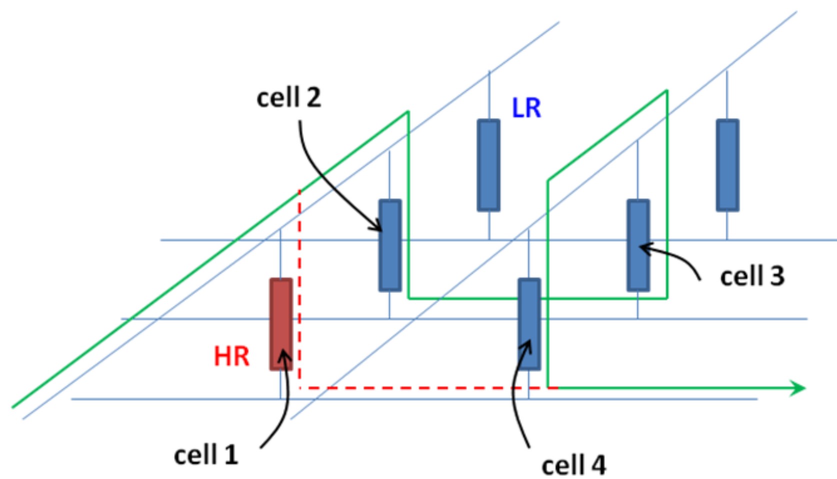
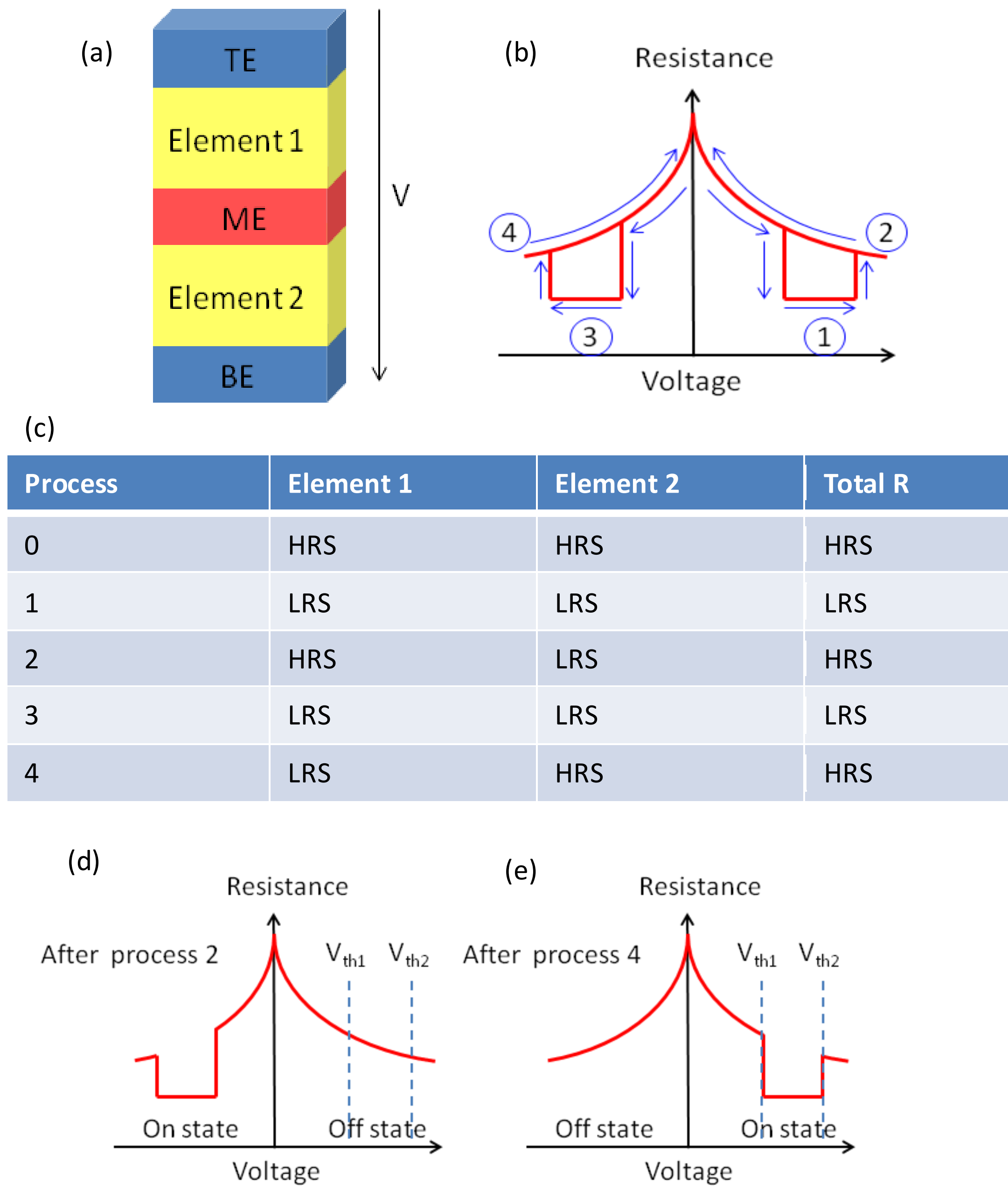


Fig. 1 The parasitic-path-problem caused by current passing through nearby cells of lower resistance.

Starting with the initial state (process 0, which is irreversible), when a sufficiently large negative bias is applied to the TE, element 1 switches to the LR state while element 2 remains in the HR state. Next, at a sufficiently large positive voltage, element 2 switches back to the LR state and now both elements are in the LR state (process 1 in Fig. 2). This corresponds to the “on” state. However, when a larger positive bias is applied to the cell, element 1 will switch to the HR state, causing the cell to return to the “off” state (process 2). Going again to the negative polarity (process 3) will switch element 1 back to the LR state, again reaching the “on” state. Finally, at a larger negative voltage, element 2 switches to the HR state (process 4) and the CRS element returns to the “off” state. The overall I-V curve thus has the shape of unipolar switching.

It turns out two resistance readouts can be further differentiated depending on the state of the device. For example, if the device after process 2, was read by a positive sweep bias (0→10V), the signal will sense a "0" state. If the device was read after process 4, then a positive sweep bias will cause it to switch to an "on" state and then back to the "off" state (assume 10V> V_{th2}). So the state will be determined as "1". This type of reading is called destructive readout process.



Process	Element 1	Element 2	Total R
0	HRS	HRS	HRS
1	LRS	LRS	LRS
2	HRS	LRS	HRS
3	LRS	LRS	LRS
4	LRS	HRS	HRS

Fig. 2 (a) Complementary resistive switch schematic, (b) typical CRS R-V curve, (c) table of current resistance states and the elements within, and (d) read operation R-V behavior.

In this chapter, we also investigate such CRS elements in the SiO_2-Pt RRAM device. We will show that, unlike other RRAM in which switching of the CRS

element requires twice the switching voltage of a simple bipolar element, our device has a relatively low switching voltage due to the existence of multiple resistance states.

II. Experimental Procedures

SiO_2-Pt mixture thin films with a Pt top electrode (Pt) and SRO or Mo bottom electrode (BE) were fabricated using the procedures described in previous chapters. The Pt composition f ranges from 0.2 to 0.3 and the thickness δ ranges from 10 to 25 nm. Electrical measurements follow the same procedure described in the previous chapters, with only slight modifications to introduce compliance when necessary. This aspect will be described in more detail later in the Chapter. For CRS elements, different cells are electrically connected using external wiring, then tested using a standard voltage sweep.

III. Results

A. Multi-level switching

Experiments to tune multilevel switching follow the following procedures: (a) in the negative bias, a programmed current compliance is used; for example, a sweep of

0 V → −5 V → 0 V under a current compliance of 5 mA; and (b) in the positive bias, the current compliance is removed and a similar sweep is used; for example, 0V → 5 V → 0 V. The role of the compliance is to limit the current: when the current value reaches the compliance, the applied voltage will adjust so that no higher current is applied; typically, this means a saturation voltage that remains constant until the current decreases to below the set compliance.

In one experiment, the cell was switched to the high resistance (HR) state, then switched back to a low resistance (LR) state under different current compliance. After that, the resistance value was read at 0.2V to “define” the resistance state of the cell. (The current compliance is inactive during read, which involves only a small current.) Figure 1 shows the various resistance states acquired at different current compliance: the “LR state” clearly contains multiple states and all of the states are apparently stable (non-volatile) at zero bias. With a lower current compliance, the corresponding state has a higher resistance. In other words, when less current is passed during the HR to LR transition, the LR state attained is more resistive.

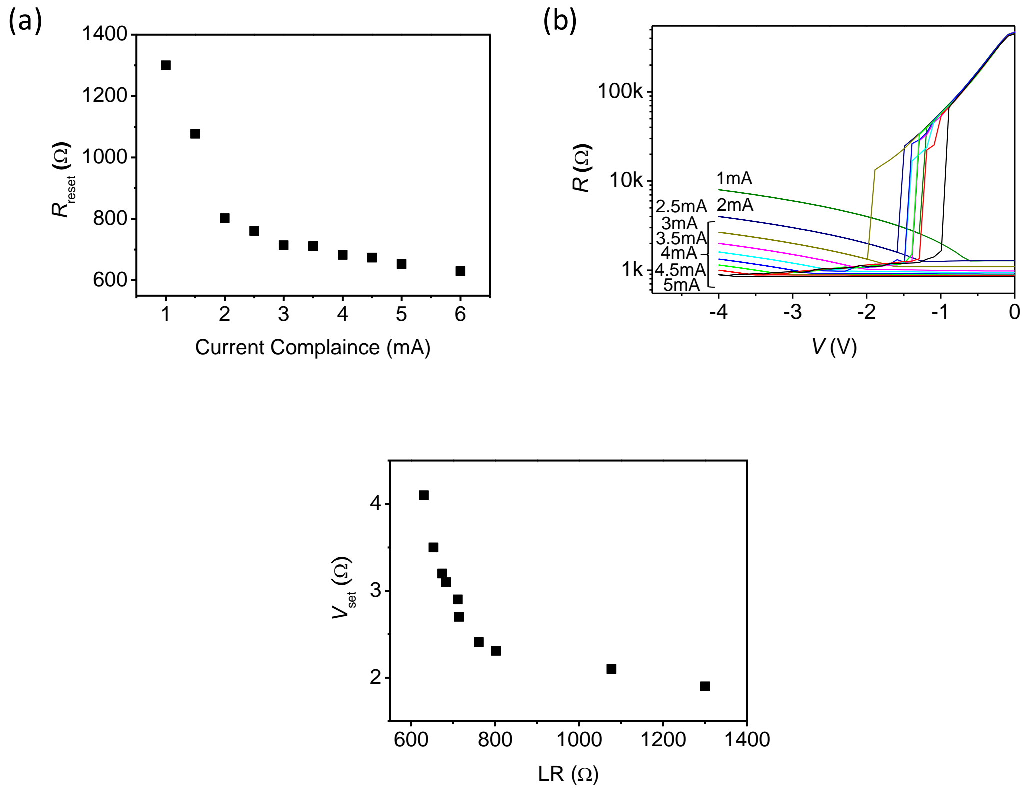


Fig. 3 (a) LR value under different levels of current compliance, (b) R-V curve of reset transition under different levels of current compliance, numbers indicate compliance level, and (c) LR states and their associated V_{set} value.

We next switched these states to a HR state by sweeping the cell through the positive bias. We found the switching voltage required increases with the current compliance previously used under the negative bias, as shown in Fig. 3(c), and each "LR" state is associated with a specific set voltage. A set voltage as low as 1.5 V was obtained in this way. Remarkably, all of the switching traces follow the same I-V curve once switching is complete: they all return to the same HR state. In other words, although the more resistive "LR" state has a smaller set voltage, all the "LR" states return to the same HR state. These data shown in Fig. 3(a) and 3(c) are for devices

with a SRO BE. The same phenomenon was also observed in devices with a Mo BE, except a smaller reset voltage was applied to avoid the oxidation of Mo BE.

Having established that there are multiple "LR states" using current compliance during reset, we seek to reconfirm these states and to determine their reset voltages without the current compliance. The cell is first reset past the first resistance drop without compliance, reaching a predetermined maximum voltage (referred to V_{reset} below) along with the corresponding current (I_{reset}), then returned to the positive bias to determine the set voltage (V_{set}) and the corresponding current (I_{set}). A plot of V_{reset} and I_{reset} versus V_{set} and I_{set} is shown in Fig. 4. A very similar trend of a nearly linear correlation is seen for both SRO BE and Mo BE samples. Without exception, the values for reset transitions are somewhat higher than those for set transitions. This is apparent by referring to the straight lines with a slope of unity in the above figures: all the datum points fall below such lines.

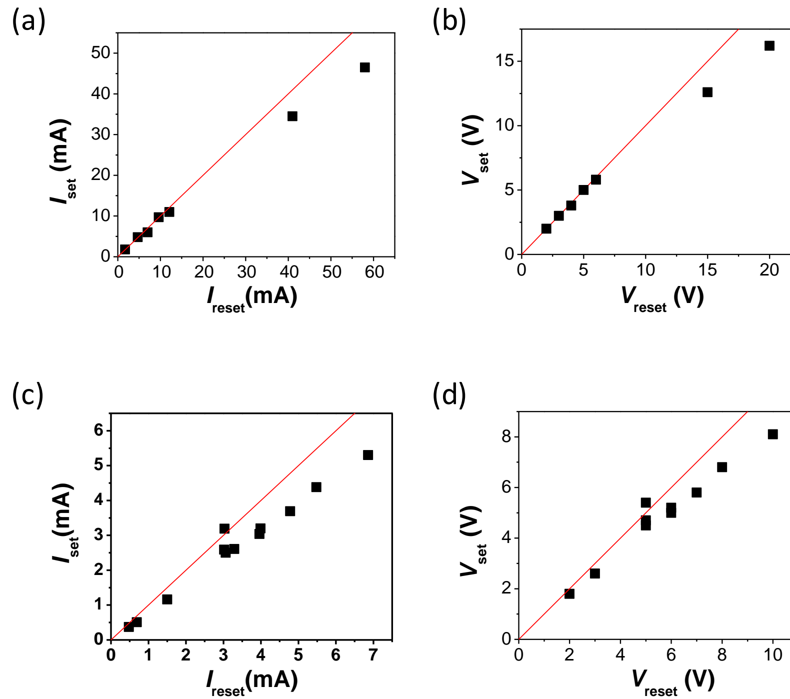


Fig. 4 Relationship of I_{reset} vs I_{set} and V_{reset} vs V_{set} in (a)(b) Pt/SiO$_2$-0.25Pt/SRO, and (c)(d) Pt/SiO$_2$-0.3Pt/Mo. Red lines indicate $I_{reset}=I_{set}$ or $V_{reset}=V_{set}$.

As already mentioned, different "LR states" all return to the same HR state after set transitions. Figure 5(a) shows R-V curves under various levels of current compliance; different LR states (also called intermediate LR (ILR) states) have different set voltages but they always go back to the same HR state. (The ratio of the HR to the LR is decreased because of the increase of the intermediate LR, but is still above 20 in these tests.) These hysteresis curves suggest that it is possible to have resistance switching with significantly lower switching voltages. This is illustrated in Fig. 5(b) by alternating positive and negative voltage pulses, and taking resistance readings at

0.2V between pulses. The device is first switched by + 5 V/ - 4 V 500ns pulses for 50 cycles, then switched by a set of progressively smaller negative voltage pulses; clearly, the cell can still function at these reduced voltages.

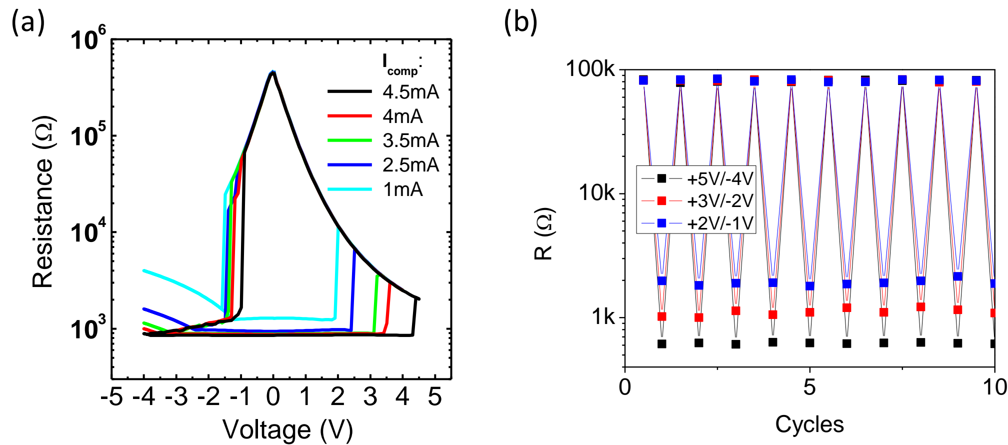


Fig.5 (a) Example of using different compliance obtaining different levels of LR state and V_{set}, (b) progressive switching utilizing different V_{reset}.

Until now, all the switching curves show a very sharp set transition. The full resistance jump almost always occurs in one voltage increment, which is 0.1 V in our standard test. This is not the case when the set voltage is low, made possible by using a small current compliance: the set transition then occurs gradually raising the resistance in several steps. This is illustrated in Fig. 6. Here, a very small current compliance (0.1 mA) is chosen to arrest the reset transition at a relatively high resistance. Next, the bias is reversed and the positive voltage is increased slowly. The first resistance increase is found relatively small, and it is followed by other small

resistance increases as the voltage increases. Therefore, the set transition is gradual in this case (Fig. 6(a)). Moreover, if the voltage is decreased after the first resistance increase, we can trace a switching hysteresis R-V loop that is much smaller than the regular R-V loop, featuring not only a higher "LR" but also a smaller "HR" (Fig. 6(b)). This indicates that in addition to intermediate LR states, there are also stable intermediate HR (IHR) states, with a set voltage at around 1 V. Note that in these experiments shown in Fig. 6, the "LR" is high and much exceeds the resistance of the bottom electrode. So the applied voltage is essentially all spent on the mixture film, and the set voltage above (~1 V) is the actual voltage that triggers the set transition in the film.

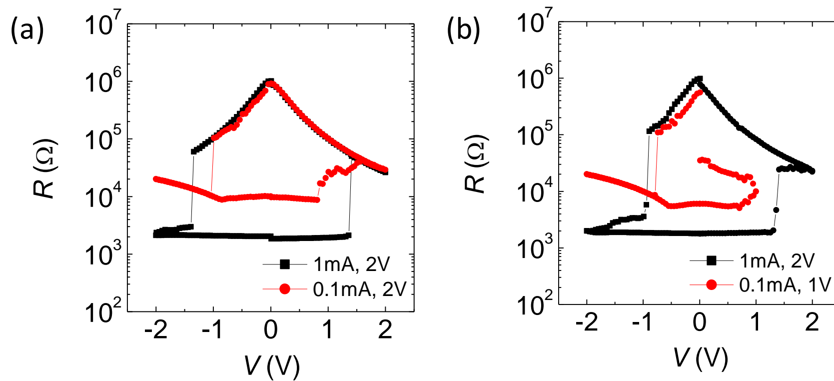


Fig. 6 (a) A gradual set transition (red) occurring when a smaller compliance (0.1 mA) is used. (b) Limiting the positive voltage to a smaller value captures the intermediate HR state which has a smaller resistance. In both cases, $R_{LRS} >> R_{BE}$.

To evaluate the stability of the intermediate states, retention tests under continuous voltage (0.1V) of four different states were investigated. The cell was sequentially switched to the HR, LR, IHR, and ILR states, and each state was subject to a retention test of 2000 sec. The HR and LR states were obtained by using 2 mA compliance during reset and no compliance during set; the ILR and IHR states were obtained by using 0.2 mA compliance during reset and 1.5 V without compliance during set. (The resistance of the two intermediate states differs by more than 10 times.) The result shown in Fig. 7 reveals that the resistance of all four states can sustain the test, with continuous small voltage stressing (reading at 0.2 V).

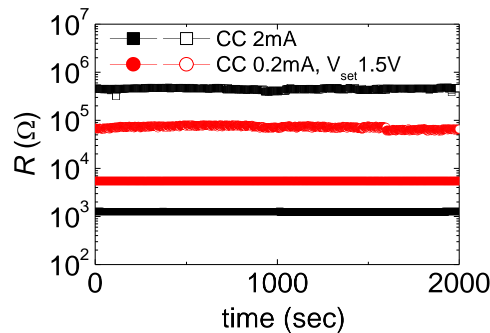


Fig.7 Retention of 4 different resistance states.

As already mentioned, in reaching the IHR state, a relatively high ILR that well exceeds the resistance of the bottom electrode was used. As a result, a reading of the

“ture” set voltage of ~1 V was possible. This is not the case for other tests in which the LR is comparable or even smaller than the resistance of the bottom electrode. To more accurately determine the “true” set voltage and to compare its value for the HR state and the IHR state, we need to establish the resistance of the bottom electrode accurately. The following experiments are attempted for this purpose.

We first investigate the switching behavior of a Pt/SiO_2-Pt/Mo sample under various external resistor loads, connected to the cell or bottom electrode in series. The standard I-V curve, without the external load, is shown in Fig. 8(a), which ranges from −5 V to +5 V, has a 4.8 V set voltage and an LR state of 200 Ω at −5 V. Next, when the cell is at the HR state, a load of 100 Ω is added before returning to the negative bias. A sweep to −5 V bias under the load switches the cell to an (intermediate) LR state of around 500 Ω at −5 V. When a positive bias is next applied, the cell switches to the HR state at approximate +2 V, which is lower than the set voltage without the load(Fig. 8(b)). This can be understood because the external load effectively provides a current compliance that raises the “LR”, hence lowers the V_{set}. However, if the same external load is added at the end of the negative sweep (i.e., when the cell is in the same LR state as in the unloaded device), then the subsequent positive bias sweep under the 100 Ω load finds a much higher set voltage of +8V(Fig. 8(c)). The apparent LR is now 300 Ω, which is the sum of the previous LR and the

100 Ω due to the load, indicating that they are indeed the same LR state. So the increase of the V_{set} may be attributed to the less favorable voltage partitioning between the film and the bottom electrode plus the external load. These two experiments clearly indicate that the apparent V_{set} need not be a constant, and will change in a sensitive way with the variation of BE resistance and external load while holding the LR state constant. However, the effect is masked if the LR state is not held constant, which is usually the case since the resistance sum of the bottom electrode and the external load serves as an effective compliance that regulates the "LR". It is this regulation that "buffers" the effect of bottom electrode resistance and the external load, rendering the apparent V_{set} constant.

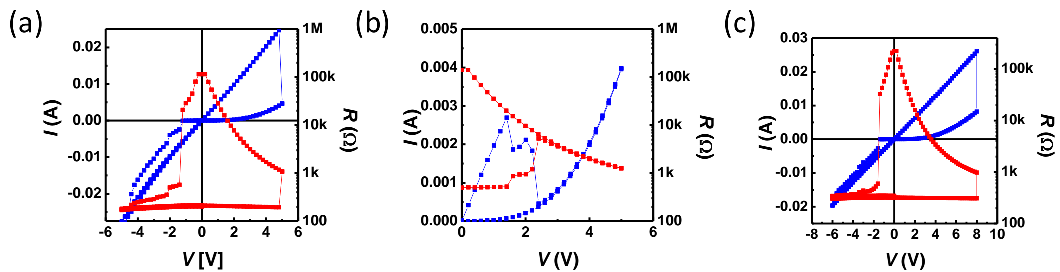


Fig. 8 (a) Standard I-V(blue) and R-V(red) switching curve of a Pt/SiO_2-0.25Pt/Mo device, (b)set switching(no load) after resetting with a 100Ω external load, (c)set switching with 100Ω external load connected.

Our interest is to find the true switching voltage across the mixture film, which we call V_m. Referring to the circuit in Fig. 8, we express the total resistance R_{total} in terms of the mixture film resistance R_m, which is variable depending on V_{reset} (here defined

as the highest voltage reached under the negative bias), the bottom electrode resistance (R_{BE}) and the load resistance (R_{Load}). Expressing R_m as V_m*/I_S, where V_m* is the true set voltage and I_s is the current at the set transition, this gives

$$R_{total} = R_m + R_{BE} + R_{Load} = V_m*/I_S + R_{BE} + R_{Load}, \quad \text{Eq. 5-1}$$

This suggests a plot of R_{total} against 1/I, which may be expressed as $R_{total} = A/I + B$, in which B is a constant unaffected by the changes of states of the film. In the special case of constant V_m*, this plot should show R_{total} scaling linearly with 1/I. Alternatively, if I_s is plotted against R_{total}, then extrapolation to $I_s = \infty$ should yield B, and a change in load resistance R_{Load} should simply horizontally translate this plot.

Measurements of I, V, and R under different R_L are used to construct such plots. In the first plot, Fig. 9(a) for Pt/SiO_2-Pt/SRO and Fig. 9(b) for Pt/SiO_2-Pt/Mo the set current I_s is plotted against the (total) resistance, which is tuned by using different negative voltage at the maximum negative bias, a larger bias giving a smaller resistance. (In the plot, this total resistance is denoted as LR, which remains constant when the voltage sweeps from the maximum negative bias to the set voltage.) As expected, an addition of R_{Load} simply shifts the curve to the right by an amount R_{Load}. Extrapolation to infinite I_s, along the curve without R_L allows an estimate of R_{BE}, which is around 300~400Ω for the SRO BE.

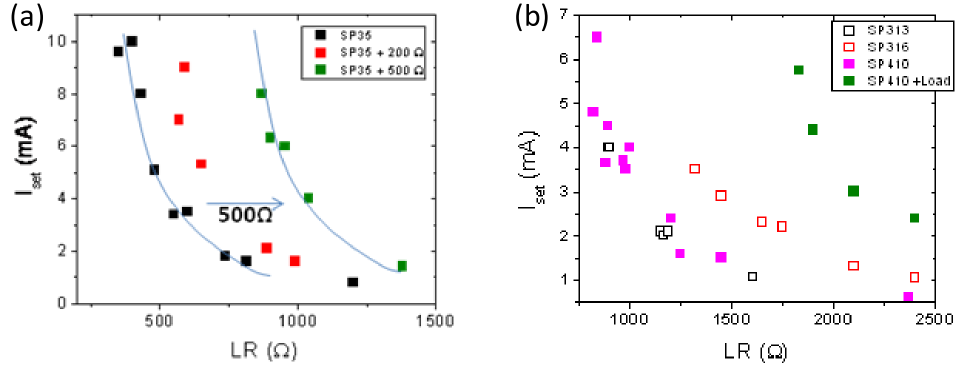


Fig.9 LR value versus I_{set} value under different external load of (a) Pt/SiO_2-Pt/SRO and (b) Pt/SiO_2-Pt/Mo device.

To construct the R-1/I plot, tests utilizing a very high reset voltage (current) are desirable. Measurements using a voltage ramp of ±20V in the SRO BE films (Fig. 10(a)) and ±10V in the Mo BE films (Fig. 10(b)), without any intentionally added external load, confirmed that the "LR" can be progressively lowered without affecting the ability to switch. The R-1/I plots (Fig. 10(c) for SRO BE and Fig. 10(d) for Mo BE) support a nearly linear relation overall, although there could be nonlinearity at smaller 1/I that may affect the extrapolated R_{BE} at 1/I=0. Ignoring the possible nonlinearity for the moment, the intercept obtained for R_{BE} is about 320 Ω for the case of SRO BE and 1320 Ω for the case of Mo BE. Using this value for R_{BE} value, we then back-calculate the V_m using the following equation:

$$V_m = I \times (R_{total} - R_{BE}) \quad \text{Eq. 5-2}$$

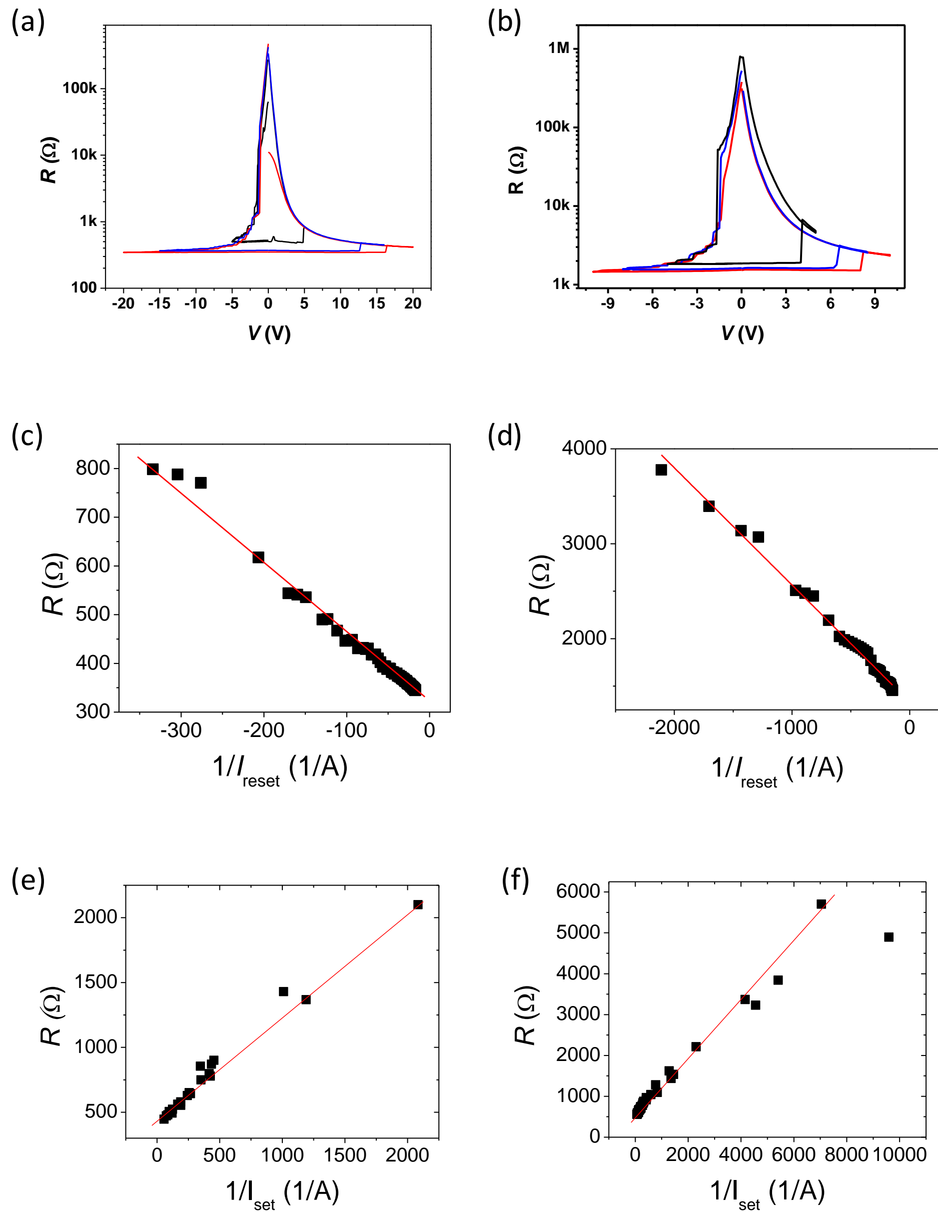


Fig.10 (a)DC-IV curves of Pt/SiO_2-0.25Pt/SRO and (b) DC-IV curves of Pt/SiO_2-0.25Pt/Mo device showing >±10V switching curves; R-1/I_{reset} of (c) Pt/SiO_2-0.25Pt/SRO and (d) Pt/SiO_2-0.25Pt/Mo; R-1/I_{set} of (c) Pt/SiO_2-0.25Pt/SRO and (d) Pt/SiO_2-0.25Pt/Mo.

The results shown in Fig. 11 have some scatter but the trend indicates a set voltage that slowly rises with I_{set}, i.e., the set voltage slightly increases when the LR decreases.

The range is 0.8 V to 1.3 V in the case of SRO BE and 0.6V to 1.2V in the case of Mo BE. In Fig. 11(a) and (b), these calculated set voltage are compared with the reset voltage, which can be directly read from the standard I-V curve since in reset R_m is huge compare to R_{BE}. Despite the scatter, it seems clear that the set voltage is slightly smaller than the reset voltage, although they are certainly comparable in magnitude. Here, the scatter of the reset voltage is intrinsic since the reset transition usually takes multiple steps, and there are some variations in the step position. The scatter of the set voltage is due to (a) the somewhat uncertain nature of the R_{BE} and (b) the fact that it is a calculated quantity and not a measured quantity.

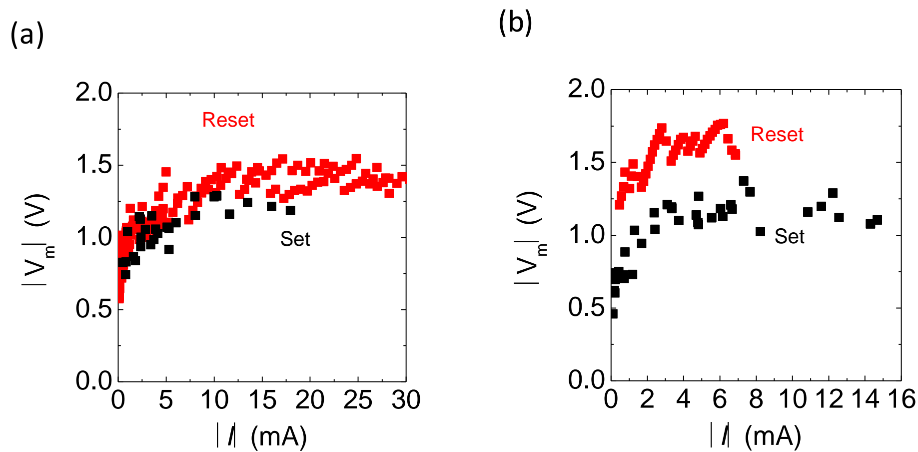


Fig. 11 V_m values obtained from set transition and reset of (a) Pt/SiO_2-Pt/SRO and (b) Pt/SiO_2-Pt/Mo device.

B. Complementary switching

Two cells connected back-to-back (the BE of one cell connected to the BE of the other cell; specifically, a Pt/SiO_2-Pt/SRO/SiO_2-Pt/Pt structure) as illustrated in Fig. 2(a) is used to investigate the CRS behavior. Both cells were in their fresh state (hence the LR state) before testing. First, a voltage from 0 → −5V causes cell 2 to switch to the HR state at around −4V; there is one HR cell and one LR cell, which defines the "off" state. Next, the voltage reverses and sweeps to positive polarity, and at about 1.5V, cell 2 switched to the LR state so there are two LR cells, which defines the "on" state. As voltage increases under the positive bias, cell 2 continues to lower its resistance until cell 1 switches to the HR state at about +4V; the circuit then returns to the "off" state.

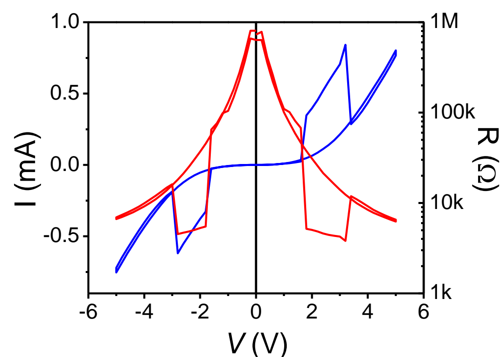


Fig.12 Complementary switching of a Pt/SiO_2-0.25Pt/SRO device.

IV. Modeling switching behavior including multiple switching states

We now introduce a circuit model to explain the switching behavior. We consider in Fig. 13 the mixture film to contain many (n) parallel conducting pathways (each having a resistance R_L), which are adjacent to a trap site that, when occupied by an electron, can switch the low resistance pathway to a highly resistive one (each having a resistance R_H).

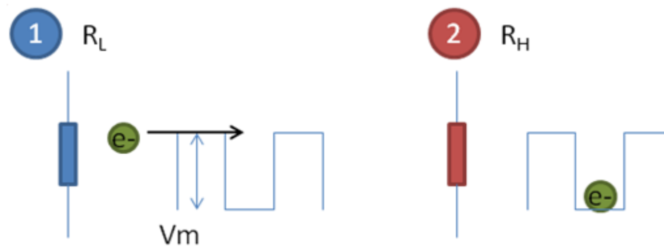


Fig.13 Indication of R_H and R_L.

In the extreme case when all pathways are blocked,

$$R_{total} = \frac{1}{n/R_H} + R_{BE} = \frac{R_H}{n} + R_{BE} \qquad \text{Eq.5-3}$$

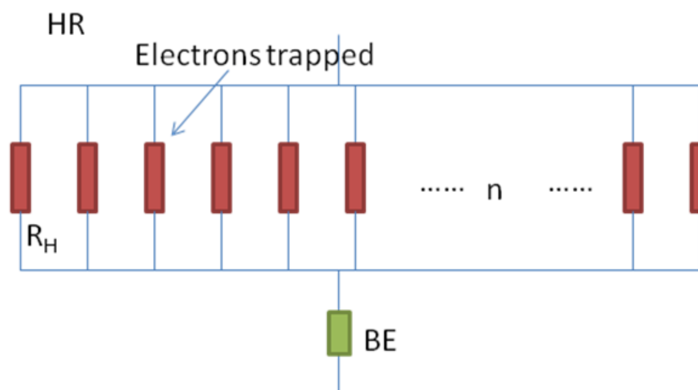


Fig.14 HR state parallel circuit model.

In the other extreme, when all traps are empty,

$$R_{total} = \frac{1}{n / R_L} + R_{BE} = \frac{R_L}{n} + R_{BE} \qquad \text{Eq. 5-4}$$

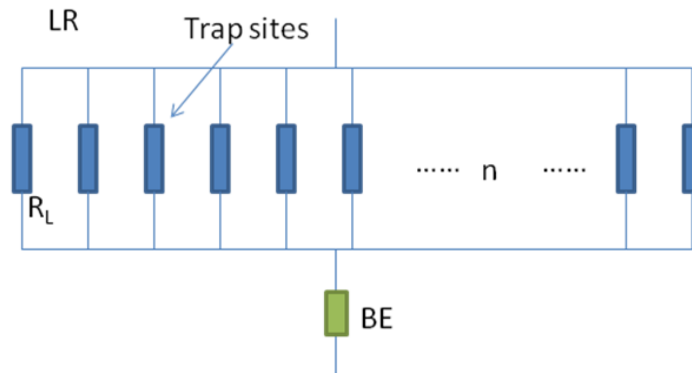


Fig.15 LR state parallel circuit model.

According to the V_m measurements, the trap sites are filled under a voltage trigger from 0.8V to 1.4V, which is slightly lower than the voltage required for detrapping. So, at approximately −1 V, reset switching (from HR to LR) begins to be triggered. The bottom electrode has little influence on this onset reset voltage if it is less resistive than R_H /n. If 1% of the trap sites are cleared by the first reset transition, then

$$R_{total} = \frac{1}{\frac{0.99n}{R_H} + \frac{0.01n}{R_L}} + R_{BE} \qquad \text{Eq.5-5}$$

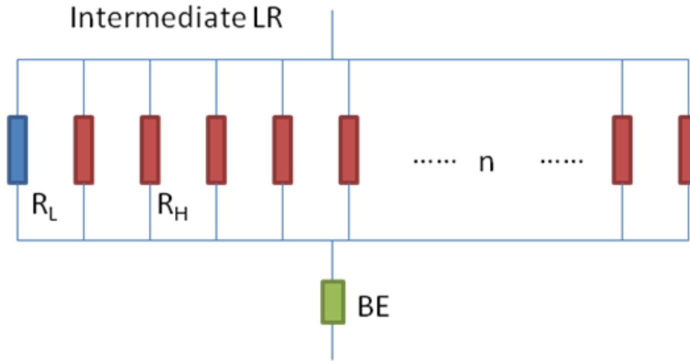


Fig. 16 Intermediate LR state parallel circuit model.

which despite of the small percentage is much lower than before. This corresponds to the first resistance drop in reset. The lower resistance may necessitate voltage sharing between the film and the bottom electrode,

$$R_{total} = \frac{1}{f/R_H + (1-f)/R_L} + R_{BE} \qquad \text{Eq. 5-6}$$

$$V_{real} = V_{total} \times \frac{R_m}{R_m + R_{BE}} \qquad \text{Eq. 5-7}$$

where f represents the fraction of circuits in R_H. This may lower V_{real} to a value less than V_m for reset, causing reset switching to halt until an increase of the external voltage, V_{total}, restores V_{real} to V_m, after that reset switching resumes again. This sequence of events is illustrated in Fig. 17 which shows the result of simulation for the V_{real} assuming a certain $\langle V_m \rangle$ for reset. As the resistance drop in the film becomes smaller as R_m becomes smaller, the LR resistance curve appears smoothly decreasing at higher (negative) voltage. The upper envelop of the simulated curve corresponds to the V_m, which slowly increases toward a somewhat saturated value as already shown

in Fig. 11. This “saturation” corresponds to the exhaustion of filled trap sites.

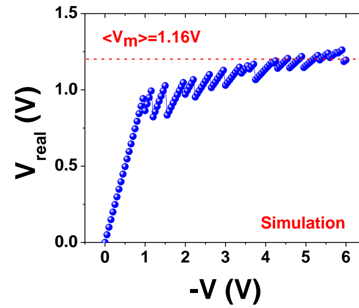


Fig.17 Simulation data of reset process. n=100, Vm = 0.8~1.2V, R_{BE}=500Ω.

We next turn to set transitions. Although the required V_m for set transition is only slightly less than that for reset transition, V_{real} before set transition is much lower than V_{total} because the cell is at a LR state. Therefore, a larger V_{total} is required to achieve V_{real} =V_m. This voltage is typically around 4~5 V in our standard test, for the mixture film to acquire approximately 1 V, which is consistent with a R_{BE} around 300Ω and a R_m around 100Ω . Once the first set switching is triggered, however, the resistance of the mixture film increases and so does V_{real}. Therefore, there is little problem for maintaining V_{real}> V_m, which propels the set transition to its rapid completion (all R_L elements switching to R_H elements.) This explains the abrupt set transition observed in most of our tests. The only exception is the case when the R_m is intentionally kept high (many R_H elements remaining). This allows most of the applied voltage to be

spent as V_{real}. The first set transition then occurs at about 1 V, which is accompanied by a small rise in R_m. So the rise in V_{real} is small and the intermediate HR state can be arrested.

The above model can be implemented to simulate the observed R-V curves. One such example is shown in Fig. 18. Here, the same Gaussian distribution of V_m is assumed for both set and reset transitions of 100 resistor elements, ranging from 0.8 V ~ 1.2 V, and a more realistic R_H having the desired R(V) dependence is used. Other parameters used are $R_L = 10^3$ and $R_{BE}=500\Omega$. The simulated curve is strikingly similar to the observed one including all details of set and reset transitions. However, we must note that the simulation is not a validation of the assumption: specifically, the same V_m for set and reset transitions. This is because the exact value of R_{BE} is difficult to obtain, and it has a direct influence on V_{real}, hence the condition of $V_{real}=V_m$.

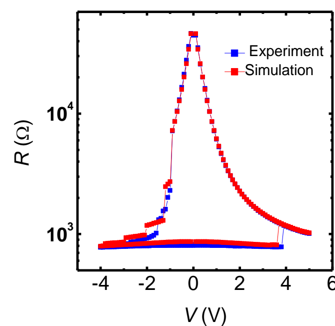


Fig.18 Simulation data using the above model.

V. Discussion

A. Multilevel switching and modeling

To assess the realism of the model, we here estimate the modeling parameters based on the general features of the observed switching curves. (1) Each R_L is at least $3\times10^4\Omega$. This comes from assuming the I-HRS, which is about $3\times10^4\Omega$, consists of only 1 R_L. (If there are more R_L, then each R_L should be more resistive.) This number is to be compared with the so-called maximum metallic resistance, which is about $8\times10^3\Omega$[9]. (2) If $R_L = 10^4\Omega$, then the number of conducting pathways is at least 10^3, since the lowest R_m is probably lower than 10 Ω. (3) $R_H = HR*n = 10^8\Omega$. (4)Based on the above parameters, we calculated that the standard switching range (+5V ~ -5V) using equation 6-6, involves transitions between f=0.9 to f=1. (From HR = R_H/n, and noting LR is around 100~1000 Ω, we obtain R_H=HR*n~10^8 Ω. Since R_L=10^4 Ω, therefore f should be 0.9~0.95.) (4) The V_m distribution is from 0.8 V ~ 1.4 V, which comes from Fig. 9 and is also supported by I-HRS measurements in which R_m>R_{BE}.

B. Resistance cell size dependence

The nature of SiO_2-Pt device switching originates from a uniformly trapping-detrapping process, which should incorporate cell size scaling in resistance. The HRS shows perfect cell size scaling, which is evidence of uniform top-down conduction.

The LR state, however, only shows weak cell size dependence. This is attributable to two reasons. First, the mixture film has an ultra-small resistance as measured in the 4-point measurement; simply convert the numbers with the cell size and film thickness will give a resistance around 1~10Ω. The measured LR state is actually dominated by the bottom electrode and spreading resistance, as the bottom electrode and the spreading resistance is typically 200~500Ω. Second, as discussed in the previous section, the LR state of the mixture film consists of many levels according to the reset bwhavior. However, the smaller cell size returns to a lower resistance state due to higher applied voltage on the mixture film, which originates from the higher value of the resistivity of the mixture film itself. Therefore, the thickness dependency is being suppressed.

C. Complementary switching

Complementary switching in the SiO_2-Pt cells shares similar features of other such switching reported in the literature. However, it also differs in some respects. In most RRAM devices, "reset" voltage (referring to LR to HR) generally doubles in a back-to-back configuration. This is because the two mixture layers having the same resistance must share the total voltage in equal fraction, so the voltage in each cell is only 50% of the applied voltage. This has the effect of narrowing the switching

window, which is evident from comparing Fig. 19(a) (for a single cell) and Fig. 19(b) (for a two cells back-to-back connected) taken from the literature. (As it would become obvious, this may be mitigated somewhat by adding a relatively large external load in series.) In contrast, our device does not suffer from this problem because there are multiple states of the LR type that can continue to decrease in resistance to compensate for voltage sharing. For example, when cell 1 is in the HR state and cell 2 in the LR state, a negative bias will switch cell 1 to the LR state at −1 V and, after that, continue to drive it toward lower resistance. (The above voltage is the same as in a single cell since cell 1 is much more resistive than cell 2, thus carrying nearly all of the applied voltage.) This helps to reduce the voltage on cell 1, so that cell 2 can have a larger fraction of the voltage, eventually becoming switchable to the HR state at −4V. (This voltage is the same as in a single cell. There is no resistance reduction in cell 2 because it is in the processes of being “set”, not “reset”, under the present bias.) Similar considerations for voltage sweep in the other direction will show that there is nearly no difference of the switching voltages of complementary switching and of ordinary, single cell switching.

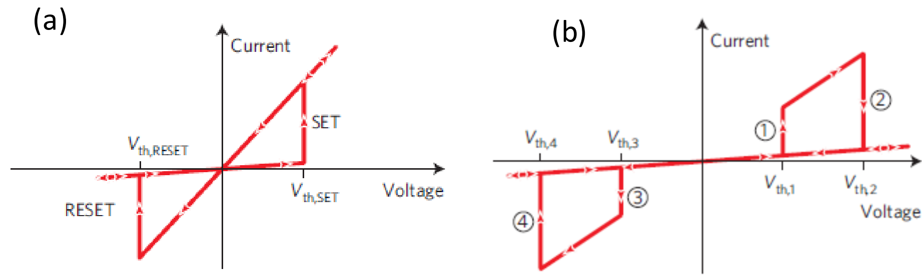


Fig. 19 (a) Single element RRAM, (b) complementary switching of two elements RRAM device showing doubling of reset voltage.

VI. Conclusions

1. There are many parallel nanometallic pathways in the SiO_2:Pt film that can be reversibly turned on and off at a voltage of ~ ±1 V.
2. By a carefully control of the real voltage across the film, using current compliance and related techniques, it is possible to access intermediate states that have some, but not all, nanometallic pathways available.
3. Intermediate states provide the SiO_2-Pt devices the ability of multiple level storage, increasing the storage density of the memory.
4. Continuous sampling of intermediate states allows the SiO_2:Pt devices to implement complementary switching without suffering from elevated switching voltages and narrowed switching windows.
5. The SiO_2:Pt device resistance may be tuned by using a negative voltage sweep, which turns on more nanometallic pathways.

VII. References

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Chapter 6 Temperature Dependence and the Conduction Mechanisms

I. Introduction

The switching mechanism of resistive random access memory (RRAM) has been studied for years but is still under debate. The analysis is usually based on current-voltage dependence or current-temperature dependence. Models such as trap-filled space charge limited conduction[1,2,3,4] (SCLC), Schottky emission[5] (SE), and Frenkel-Poole emission[5,6] (FE) have been applied. The mechanism is likely to vary from material to material. Also, only few studies have included current-voltage data over a sufficiently wide range of temperature[7,8,9]. Therefore, most analysis is incomplete and the actual mechanism may not be known yet.

In this chapter, both current-voltage (I-V) and current-temperature (I-T) characterization of different resistance states are presented. By investigating their characteristics, we have fitted the experimental data to identify the possible conduction mechanisms in the SiO_2-Pt RRAM device. For reference, a summary of conduction mechanisms in insulators is first provided.

II. Summary of Conduction Mechanisms in Insulators

A. Conduction of free electrons/holes

Conduction of free electrons in the Drude model follows Ohm's law, in which current is to the product of conductivity and field: J=σE. The conductivity σ is expressed by

$$\sigma = \frac{ne^2\tau}{m} \qquad \text{Eq. 6-1}$$

where e is the charge of the carrier and m is the mass of the carrier, n is the density of the carrier and τ is the mean free time between carrier collisions.

B. Ionic conduction

Ionic conduction was first established by Faraday in ionic solids such as PdF_2 and Ag_2S. This mechanism describes diffusion of ions (atoms that are positively or negatively charge) from one site to the other via lattice vacancies or interstitials.

C. Schottky emission (SE)

Schottky emission[10] describes high field emission of hot electrons from a metal into the conduction band of the insulator, which has a finite width. The system is supposed to be composed of an insulating layer sandwiched between two metals. Charge is activated by thermal energy to overcome a barrier $\emptyset_B$.

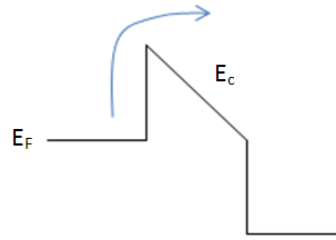

Fig. 1 Schematics of a SE conduction.

D. Frenkel-poole emission (FP)

Frenkel-Poole emission[11] describes a similar field emission, a type of thermal emission from a deep-level defect under an external electric field that lowers the barrier. Charged impurities inside traps see a largely lowered energy under a field. The FP emission basically has the same expression as SE emission, with a larger energy barrier lowering.

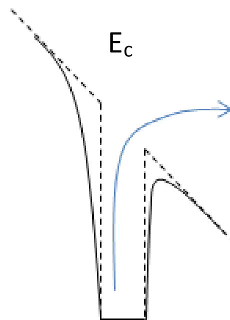

Fig. 2 Schematic of FP conduction mechanism.

E. Space Charge-limited Conduction (SCLC)

In space charge-limited conduction[12,13], the insulator with or without traps is considered as a part of a capacitor. At low field or high temperature, thermally activated Ohmic current dominates the conduction. At higher field or lower temperature, space-charge currents come into play. In a perfect insulator that has no trap sites, the voltage dependence of space charge current comes from the increasing charge on the capacitor's electrodes. The space-charge current thus has a stronger voltage dependence: the carrier density is proportional to V, and the velocity of charge in the insulator is also proportion to V. This gives a V^2 dependence for the current.

$$J = \frac{8\varepsilon_i \mu V^2}{9d^3} \qquad \text{Eq. 6-2}$$

where d is the plate separation. In the above, the mobility μ has a strong dependence on temperature. In an insulator that contains many trap sites, charge on the electrodes is shared by the traps, and as the traps are increasingly filled with injected electrons under a higher voltage, the Fermi level is elevated, and the activation to the conduction band is promoted[7,8]. The voltage-temperature dependence is approximately

$$I \propto V^{\left(\frac{T_c}{T}\right)+1} \qquad \text{Eq. 6-3}$$

Here T_c is related to the trap density and its distribution in energy. There is an additional temperature dependence in the prefactor that is not shown in Eq 6-3.

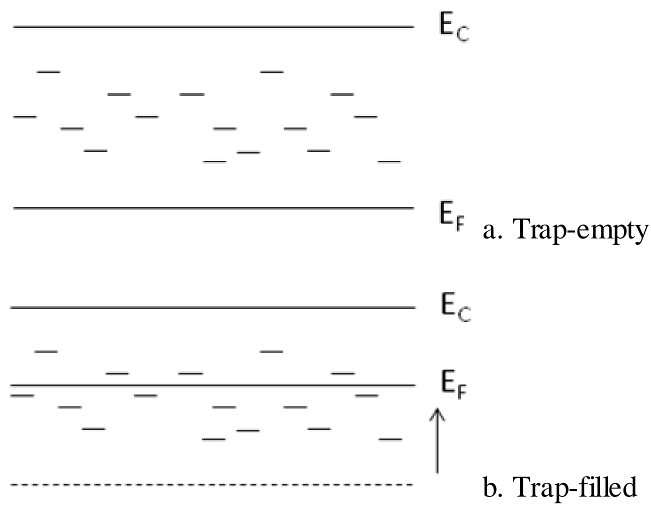

Fig. 3 Conduction of SCLC under (a) trap-empty and (b) trap-filled condition.

F. Direct tunneling

Directly tunneling[14] is elastic tunneling through a very thin insulator.

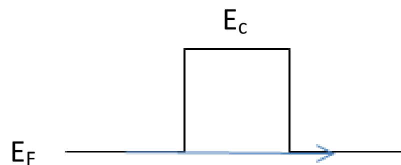

Fig. 4 Schematic of direct tunneling.

G. Fluctuation induced tunneling (FIT)

Fluctuation-induced tunneling describes elastic tunneling in disordered materials with large conducting regions separated by small insulating barriers[15]. Thermally activated voltage fluctuation across insulating gaps, treated as voltage fluctuation of a capacitor, $(kT/C)^{1/2}$, is the source of a weak temperature dependences of the conductivity. There is also a voltage dependence proposed for this process[16].

H. Fowler nordheim tunneling (FNT)

Fowler-Nordheim tunneling is a process where electrons tunnel through a sheared barrier under a high electric field[17,18]. The high electric field distorts the barrier so much that the effective barrier is triangular with a narrowing of the effective barrier width. (The undistorted barrier may have either an infinite width, or a width wider than the effective width.)

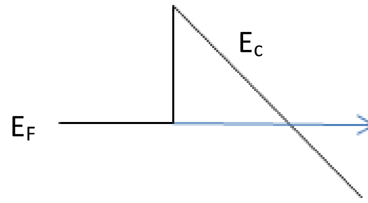

Fig. 5 FNT schematic.

I. Trap-assisted tunneling (TAT)

In trap-assisted tunneling[19], tunneling conduction proceeds between traps. The barrier is the difference in energy of the trap and the conduction band of the insulator. The presence of the traps largely reduces the tunneling distance, thus barrier width, facilitating tunneling though the insulator. Therefore, the current density is linearly dependent to the trap concentration[20]. Two tunneling probabilities, P1 and P2 are the involved, which can be expressed as

$$P_1 = \exp\left(-\frac{4\sqrt{2qm_e}}{3\hbar E}\left(\Phi_x^{3/2} - \Phi_t^{3/2}\right)\right) \quad \text{Eq. 6-4}$$

$$P_2 = \exp\left(-\frac{4\sqrt{2qm_e}}{3\hbar E}\left(\Phi_t^{3/2}\right)\right) \quad \text{Eq. 6-5}$$

Here Φ_x and Φ_t represent the barrier heights in Fig. 6 and m_e is the effective mass of electron.

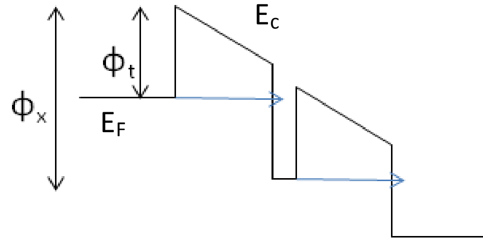

Fig. 6 Schematic of TAT conduction mechanism.

J. Variable Range Hopping (VRH)

Mott's variable-range hopping[21,22,23] describes inelastic tunneling (aided by phonons) between localized states with energies near the Fermi level, with an optimized set of jump distance and activation energy. The power in the exponent of the temperature term is related to the dimensionality (d) of the sample.

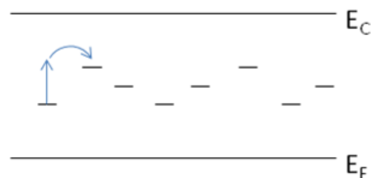

Fig. 7 VRH mechanism.

K. Activationless hopping

Activationless hopping[24] is the limiting case of VRH, under high electric field. The applied field is so huge that the barrier disappears. This allows the electrons to hop on at optimal distance along the field direction.

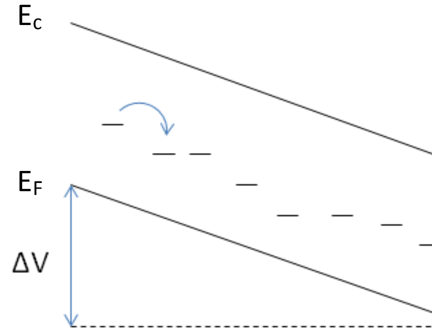

Fig. 8 Schematic of activationless hopping.

Table 1. Summary of conduction mechanisms and their equations.

Mechanism	Equation	V-T Dependence
Ionic Conduction	$J \sim \frac{E}{T} \exp\left(-\Delta E_{ai}/kT\right)$	$J \sim \frac{V}{T} \exp\left(-d/T\right)$
Schottky Emission	$J \sim AT^2 exp\left(\frac{-e(\emptyset_B - \sqrt{eE/4\pi\varepsilon_i})}{kT}\right)$	$J \sim T^2 \exp\left(\frac{a\sqrt{V}}{T} - e\emptyset_B/kT\right)$
Frenkel-Poole Emission	$J \sim Eexp\left(\frac{-e(\emptyset_B - \sqrt{eE/\pi\varepsilon_i})}{kT}\right)$	$J \sim Vexp\left(\frac{2a\sqrt{V}}{T} - e\emptyset_B/kT\right)$
Space-Charge-Limited Conduction	$J = \frac{8\varepsilon_i \mu V^2}{9d^3}$	$I \propto V^{\left(\frac{T_c}{T}\right)+1}$

Direct Tunneling	$J \sim V\exp(-\frac{8\pi\sqrt{2m^*}(e\emptyset_B)^{3/2}}{3heE}\frac{3V}{2\emptyset_B})$	
Fluctuation-Induced Tunneling	$G(T) = G_0\exp(-\frac{T_1}{T+T_0})$	$G(V) = G_{0,T}\frac{\exp(V/V_0)}{1+h_v[\exp(\frac{V}{V_0})-1]}$
Fowler-Nordheim Tunneling	$J \sim \mathrm{E}^2\exp(-\frac{4\sqrt{2\mathrm{m}^*}(\mathrm{e}\emptyset_\mathrm{B})^{3/2}}{3e\hbar E}$	$G = AVexp(-\frac{\beta}{V})$
Trap Assisted Tunneling	$J\frac{C_1eN_tP_2}{D}[DX_1 - \ln(\frac{1+P_2\exp(DX_1)}{1+P_2})]$	
Variable Range Hopping	$G = G_0\exp(-(\frac{T^*}{T})^{\frac{1}{d+1}})$	
Activationless Hopping	$G = G_0\exp(-(\frac{E_0}{E})^{\frac{1}{d+1}})$	

III. Experimental Procedures

Our study is focused on two types of devices: Pt/SiO_2-Pt/SRO and Pt/SiO_2-Pt/Mo, fabricated using the procedures described in previous chapters. Fuse silica substrates were used for low temperature measurements to obtain bottom electrode's I-T dependence (without getting signal from the substrate), which is needed for calibration. Several types of arrangements were used to access non-ambient temperatures. In one method, the sample was placed on a strip heater (Watlow, St. Louis) and the measurement was performed in a probe station. A preheat time of 30 minutes was used to

establish a stable, homogeneous temperature in the sample. In another method, a liquid nitrogen cryostat (Janis ST-100H), and a liquid helium cryostat (Sumitomo Heavy Industries) were used to cool the sample. The sample was placed in a chip holder and several cells were wire bonded with Al wires. Cooling began after the pressure of the chamber reached 10^{-6} torr, and measurements began after the system was stabilized at the lowest temperature. Calibration data were obtained by measuring the bottom electrode current from one silver-painted end to the other silver-painted end.

IV. Results

Firstly, device performance at high temperature is investigated. The R-V curve of a Pt/SiO_2-0.3Pt/SRO sample (Fig. 9(b)) at 150°C shows a decreased high resistance (HR) but the same low resistance (LR) compared to the room temperature curve, indicating that the HR state is an insulating state and that the LR state might be a metallic state. The R-V behavior of Pt/SiO_2-0.25Pt/Mo at 85°C and room temperature is similar as shown in Fig. 9(a). (A lower temperature is used here to prevent Mo oxidation.) The switching voltages in the Pt/SiO_2-0.3Pt/SRO sample basically remain constant, whereas the set voltage slightly increases in the Pt/SiO_2-0.25Pt/Mo sample. This could be due to several reasons. One is a possible reduction of Mo work function due to Mo oxidation[25]. It could also be caused by a smaller actual voltage in the mixture film because of (a) Mo oxidation and (b) lower LR due to a higher maximum negative bias used at 85°C, which is known to lower LR as described in previous chapter. These data are summarized in Fig. 10.

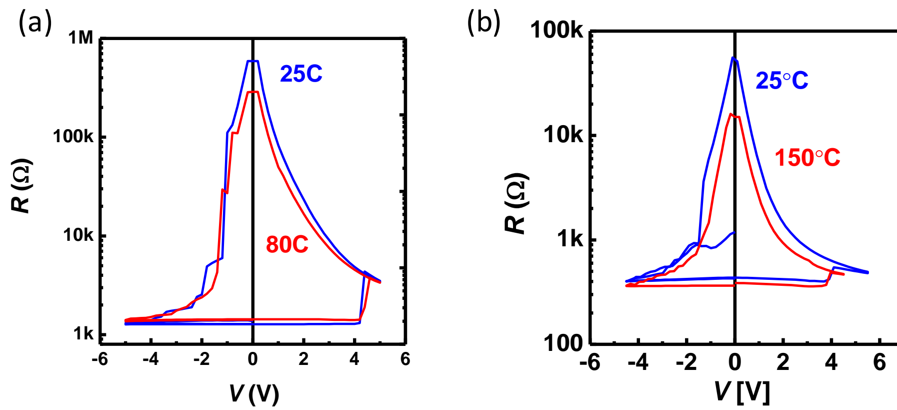

Fig. 9 R-V curves at different temperatures for (a) Pt/SiO_2-0.25Pt/Mo, and (b) Pt/SiO_2-0.3Pt/SRO.

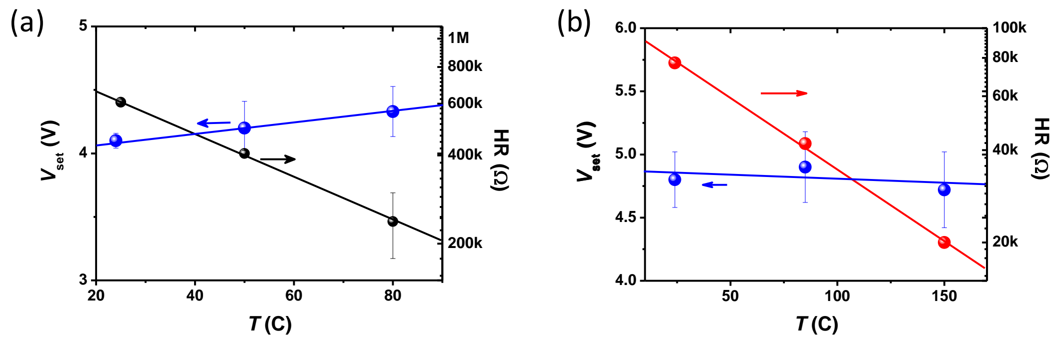

Fig. 10 V_{set} and HR for (a) Pt/SiO_2-0.25Pt/Mo, and (b) Pt/SiO_2-0.3Pt/SRO.

In Fig. 11, similar R-V characteristics for Pt/SiO_2-Pt/Mo are found at low temperatures: 78K, 200K, and 293K, showing a decrease of the HR with increasing temperature and a nearly constant LR. The switching voltages, especially for set transition, remain essentially unchanged. The I-V curve and the R-V curve at 10K confirm the same, as shown in Fig. 12 for a Pt/SiO_2-0.25Pt/Mo device, having almost the same switching voltages and LR (current) at 10K and room temperature despite hugely different HR. This

strongly argues against a thermally activated type of switching mechanism, such as ionic migration. Details will be discussed in the later section.

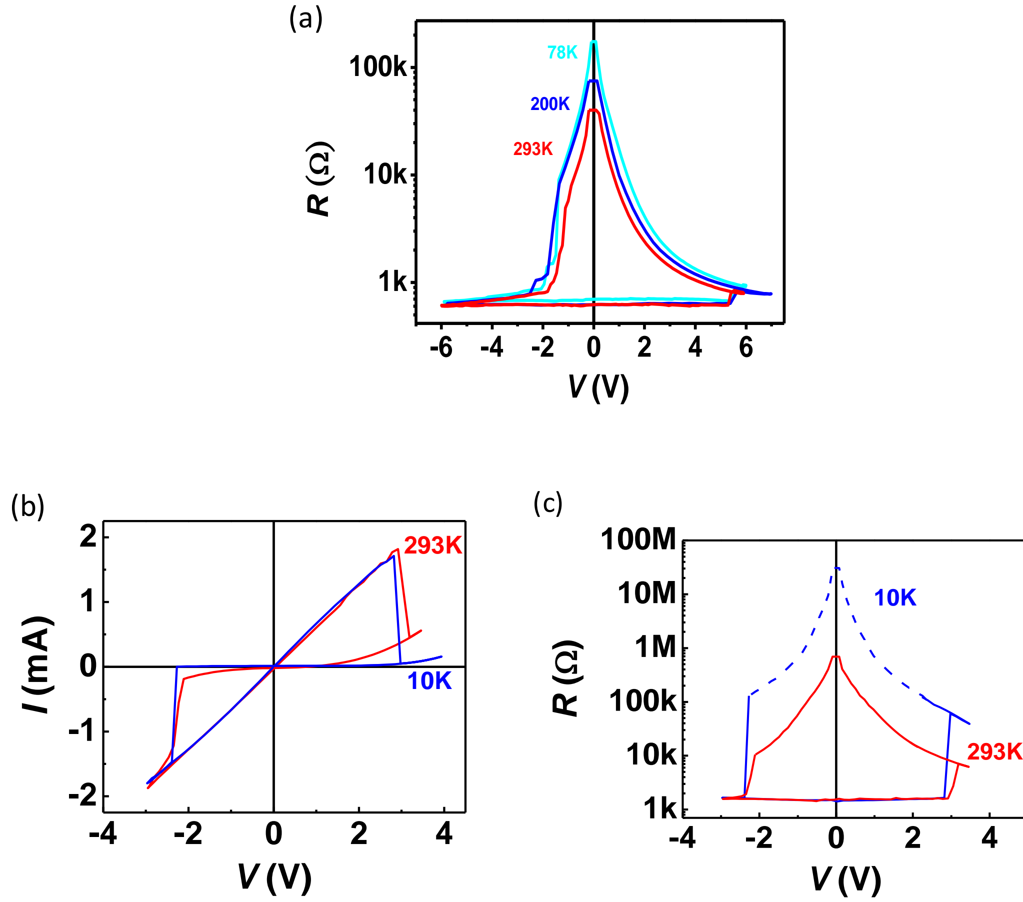

Fig. 11 (a) R-V curves of Pt/SiO$_2$-0.25Pt/Mo at three different temperatures (b)(c) I-V and R-V curves of Pt/SiO$_2$-0.2Pt/Mo switching at 293K and 10K. Broken line of 10K indicates the possible R-V curve because the current at 10K is too small to measure.

Small-voltage (0.1 V) I-T measurements were performed on a Pt/SiO$_2$-0.2Pt/Mo device. Referring to a standard R-V curve of the cell in the inset of Fig. 12, we arrested several intermediate LR states to measure their I-T dependence. The results are compared with the HR state in Fig. 12(a). Here, the BE resistance, shown in Fig. 12(b), has been

subtracted from all the data. Most intermediate states have remarkably flat I-T curves whose values decrease in a systematic manner as the (negative) "reset voltage" increases. Other large-voltage data, in the form of an I-V curves measured at various temperatures and for various film thickness, are presented in the next section along with curve fitting.

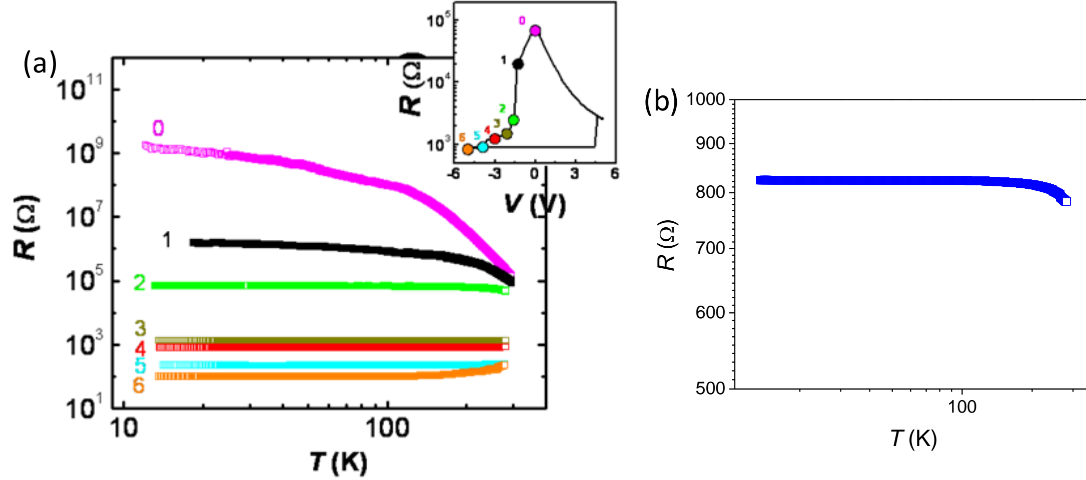

Fig. 12 (a) Temperature dependence (0.1V) of HR state and various I-LR states of a Pt/SiO_2-0.25Pt/Mo device. Inset: R-V curves of the same device, with points indicating the state of the device. (b) BE temperature dependence used for calibration of LR states.

V. Model Fitting

A. Temperature dependence

Firstly, the small voltage HR data are plotted against temperature in various ways in Fig. 13 to check the applicability of possible mechanisms. Ionic conduction, SE, FP and trap-empty SCLC models all predict an Arrhenius dependence on temperature, which appears to hold at the highest temperature (above 200K). (It is only in this dominance

regime that their voltage dependence will be analyzed as described later in this section.) The activation energy in this Arrhenius range is about 0.16 eV. This energy would be relatively low for ion motion, except in fast ion conductor. So it is likely to be associated with activated electron/hole hopping, possibly between traps.

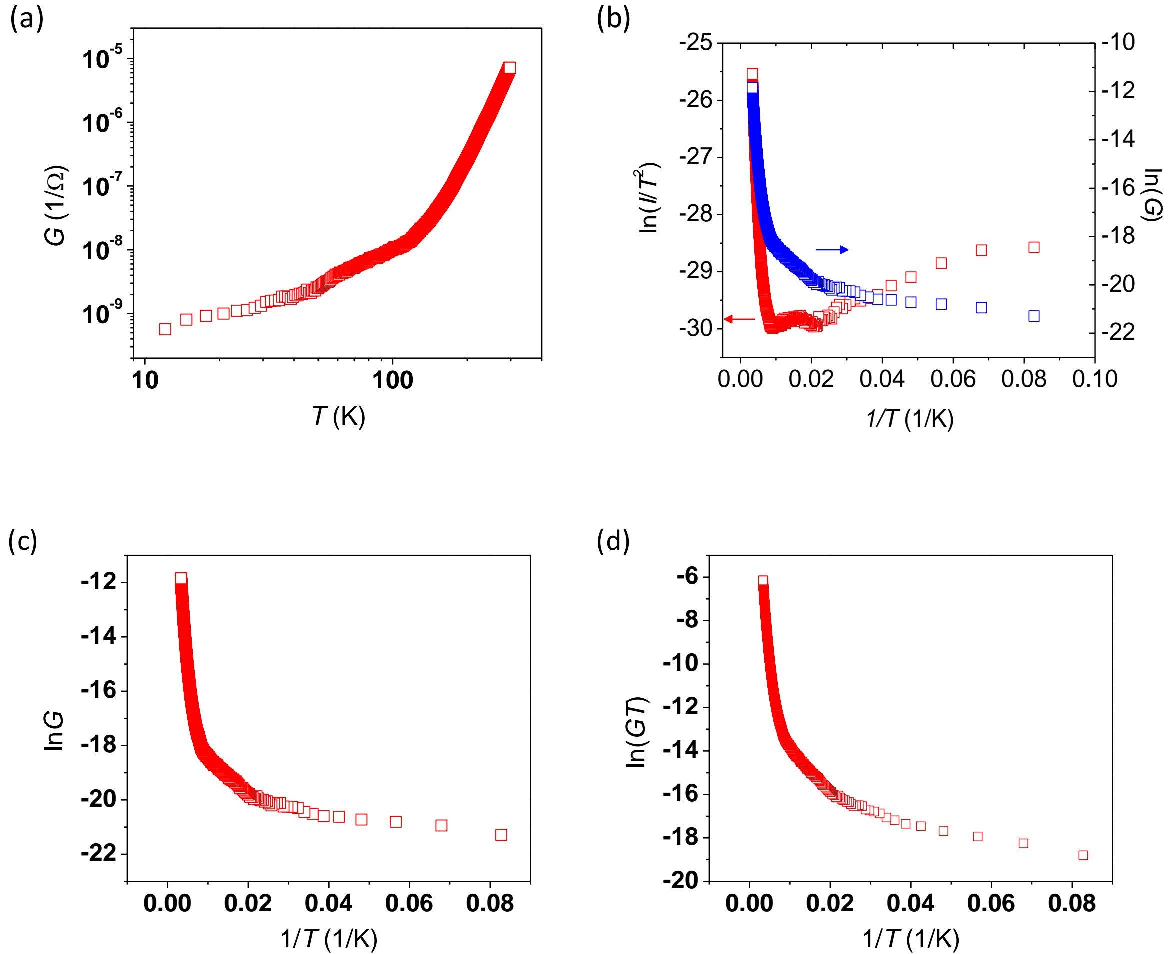

Fig. 13 Temperature dependence of the HR of a Pt/SiO_2-Pt/Mo device, curve 0 (HR state) in Fig. 21. (a) Experimental G-T curve, replotted in (b) SE and FP plot, (c) Ohmic and SCLC plot, (d) ionic plot.

The temperature dependence of VRH is much stronger than that of tunneling, but different from the Arrhenius dependence in that there is not a constant activation energy.

In Fig. 14(a), the best VRH fitting was obtained with d=3 and seems to hold above 180K. Applying the VRH model to this range, we find the fitted T^*

$$T^* = \frac{24\ \alpha^3}{\pi\ kN_u} \qquad \text{Eq. 6-6}$$

is about 141^4K for d=3. Here N_u is the density of states, and α is the localization radius, which may be related to localization length derived from the thickness dependence using the scaling theory. Using α =2 nm for a typical *f*=0.3 Pt concentration film, we estimate N_u to be about 10^{18} $cm^{-3}\cdot eV^{-1}$. The actual T* could be considerably higher if higher temperature data were taken to extend the range of VRH dominance. If so, the above N_u could be an overestimate.

In lower temperature part (10K~150K), the current gradually saturates, meaning that the conduction is rather temperature insensitive. This implies a tunneling type of mechanism rather than an activation type of mechanism. We apply the FIT model to fit the HR (curve 0 in Fig. 12), obtaining T_0=213K and T_1=2017K. The corresponding conduction gap geometry can be then calculated according to

$$T_1 = \frac{wA\varepsilon_0 E_0^2}{2k},\ T_0 = \frac{2T_1}{\pi\chi w} \qquad \text{Eq. 6-7}$$

$$\chi = \sqrt{8\pi^2 meV_0/h^2},\ E_0 = \frac{3V_B}{ew} \qquad \text{Eq. 6-8}$$

where kT_1 is the energy required for an electron to cross the gap between the conducting patches, A and w are the area and width of the gap, V_B is the effective barrier height (here we assume 1 eV), e and m are the electron charge and mass, h is Planck's constant, ε_0 is the dielectric permittivity of vacuum, χ is the tunneling constant and V_0 is the height of

the rectangular potential battier in the absence of image-force correction. The calculated width of the gap is approximately 1.2 nm and the area is 8 nm^2. The overall fitting for the entire temperature range for this HR is shown in Fig. 14(b), indicating the FIT region at low temperature and the VRH region at high temperature. We further fit curve 1 in Fig. 12, which is an IHR state, and obtain T_0 = 335K, T_1 = 1258. These parameters correspond to a smaller gap (approximately 0.5 nm in width and 2.3 nm^2 in area).

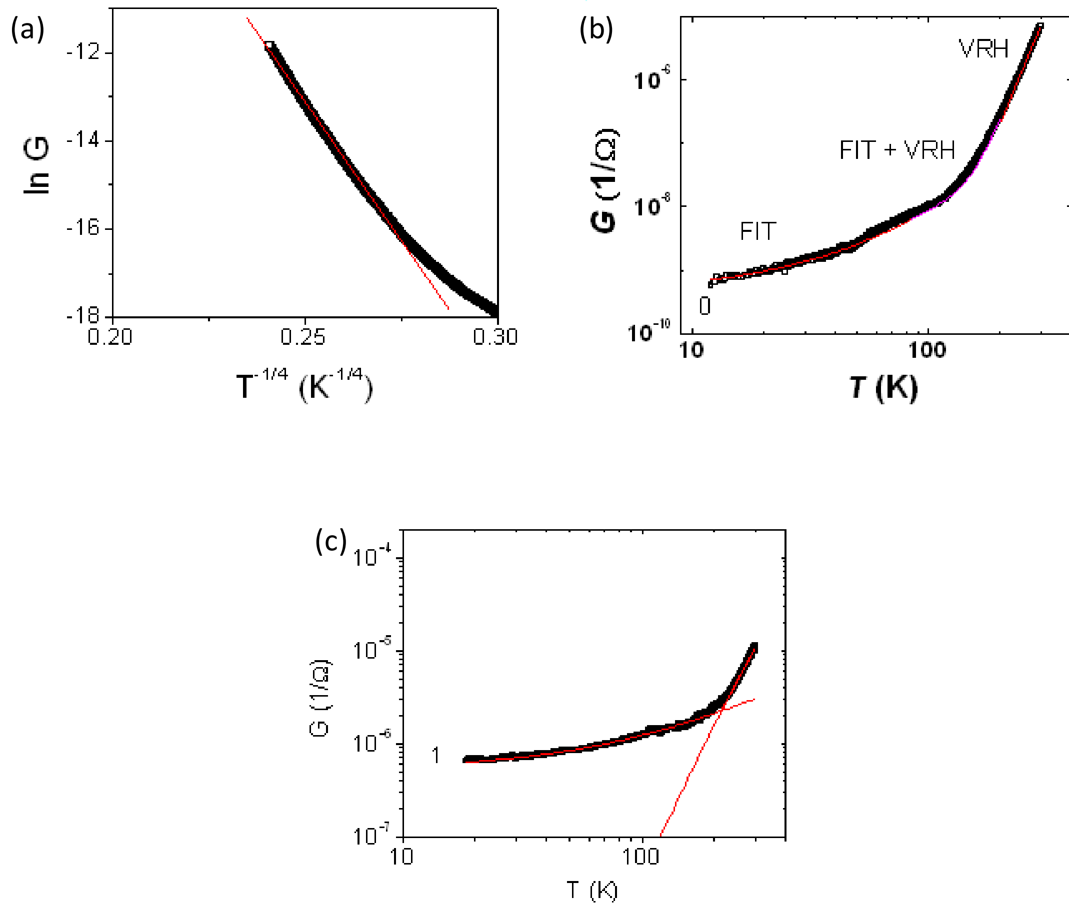

Fig. 14 Model fit of temperature dependence of conductance for Curve 0 (HR state), (a) FIT fitting, and (b) FIT + VRH fitting; and for (c) Curve 1 (an IHR state), FIT +VRH fitting.

B. Voltage dependence

We have verified the HR state of the device has FIT conduction at low temperature and certain Arrhenius dependence at high temperature (probably VRH). In this section, a series of R-V curves for the HR state measured at different temperature are shown in Fig. 15. To check whether the SE and FP models apply, we plot these data as I-V curves in the form of $\ln(J/T^2)$ versus $V^{1/2}$, which should yield a straight line according to the models. A linear region is indeed observed below 1 V as shown in Fig. 15(b). Next, we fit the low field linear region using

$$\text{SE}: J = AT^2 exp(\frac{-e(\emptyset_B - \sqrt{eE/4\pi\varepsilon_i})}{kT}) \quad \text{Eq. 6-9}$$

$$\text{FP}: J \sim E exp(\frac{-e(\emptyset_B - \sqrt{eE/\pi\varepsilon_i})}{kT}) \quad \text{Eq. 6-10}$$

Here, A is the effective Richardson Constant[26], k as the Boltzman Constant and ε_i as the relative permitivitty. To do so, we first plot the data of Fig. 15(a) in LnI-1/T, in which the intercept at 1/T=0 should converge to a single value (lnA) if the SE/FP model is applicable. However, in Fig. 16, the slopes of different V are apparently the same, suggesting no unique intercept is likely and that these models do not apply. This is despite the fact that, at any given temperature, the LnG-$V^{1/2}$ plot may show a straight line, as often reported in the literature for other RRAM; i.e., the latter plot based on one temperature study is not sufficient to validate the SE/FP mechanism.

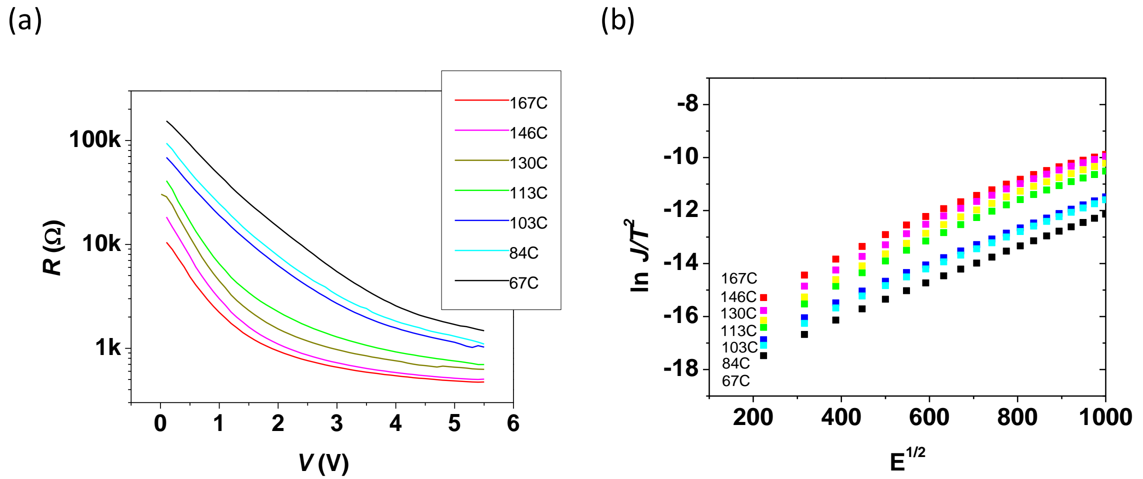

Fig. 15 (a)High temperature I-V measurements on Pt/SiO_2-0.25Pt/SRO film; and (b) same data under SE plot.

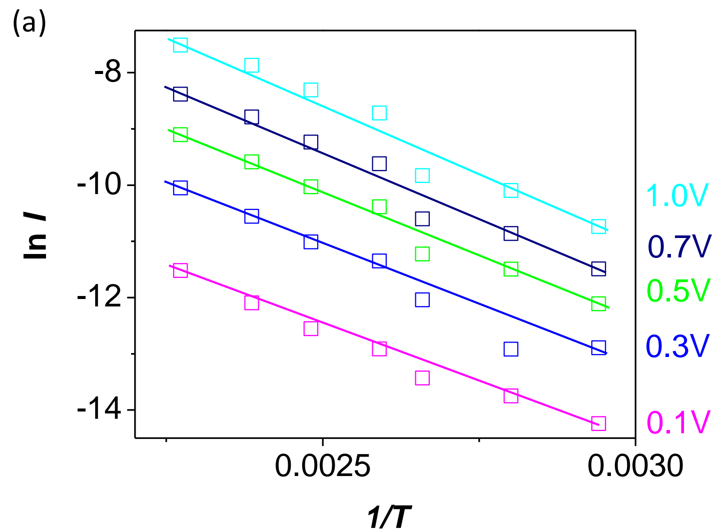

Fig. 16 (a) Ln(I)-1/T plot of the low voltage data in Fig. 15.

We next compare our HR data with the space charge-limited conduction (SCLC) model. Figure 17 shows same I-V curves above replotted to show a slope of about 1 at

low voltage, and a slope of about 2.4, which might be attributed to the space-charged-limited currents. According to the SCLC model, the slope at high voltage should decrease with temperature following

$$I \propto V^{(T_c/T)+1}, \qquad \text{Eq. 6-11}$$

(The trap distributions vary rapidly with energy, and hence, at higher temperature, space-charge-limited currents increase in a wider voltage range.) There is some evidence of a decreasing slope in our data. So SCLC may contribute to HR at higher temperatures. However, because of a lack of simple plotting strategy, we have not carried out a more detailed examination of whether these I-V curves at different temperatures are entirely consistent with a SCLC mechanism. As mentioned earlier, the activation energy is likely to be about 0.17 eV.

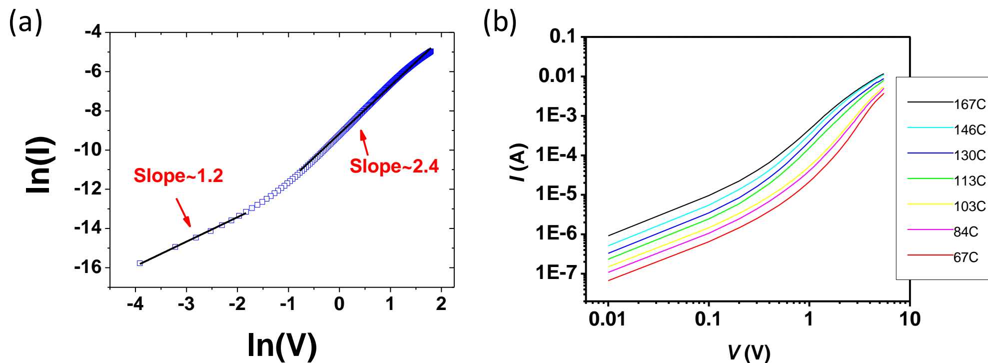

Fig. 17 (a) SCLC fitting and (b) I-V curve at elevated temperature of a of a Pt/SiO_2-Pt/Mo device.

Next we consider field-assisted tunneling models for HR. According to the FNT model, which applies at large voltages when the applied voltage exceeds the barrier height, the plot of log current (or its similar forms) against 1/V should yield a straight line. This plot

is shown in Fig. 18, which reveals a linear FNT-compatible region when the (applied) voltage is greater than 2 V. In this region, there is little temperature sensitivity, which is also consistent with the FNT model. Calculation using the fitted slope and equation 6-12 then gives the effective barrier height in the FNT model. The fitted FNT effective barrier height, using an effective thickness of 20 nm, is around 0.13 eV, and it only slightly decreases as the temperature increases. (A weak temperature dependence is predicted for FNT because of the slight broadening of the Fermi-Dirac distribution of charged carriers at higher temperatures'[27,28,29]. The effective thickness above is clearly too large for effective tunneling. Since FNT-like behavior is seen only above 2 V, we expect the barrier height to be of a similar magnitude. This suggests a barrier thickness of the order of 1 nm.

$$G = AVexp\left(-\frac{\beta}{V}\right),\ \beta = \frac{4(2m_{ox})^{1/2}t}{3q\hbar}\emptyset_b^{3/2} \qquad \text{Eq. 6-12}$$

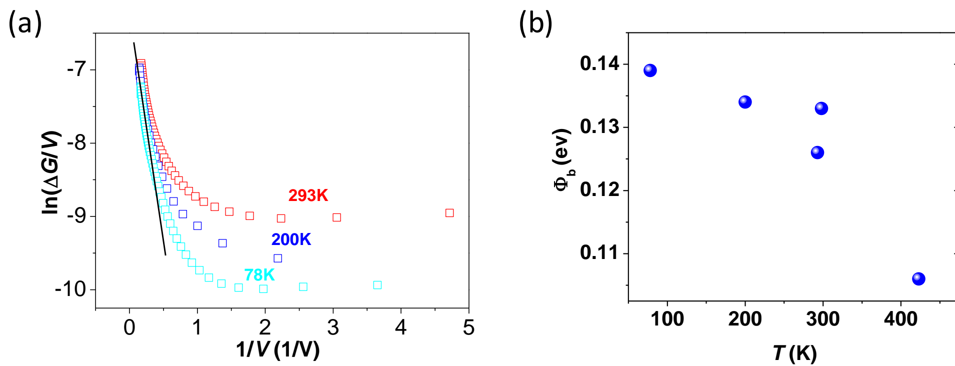

Fig. 18 (a) FNT plot of the I-V data of the HR state, (b) calculated barrier height using effective thickness 20nm.

The HR data for Pt/SiO_2-Pt/Mo devices of different thickness (20% Pt) and of different Pt content (20 nm thickness) span a wide range of resistance values. They follow systematic trends, showing an increase with increasing thickness and with decreasing Pt content. As described in a previous chapter, these changes can be attributed to the localization length: in thicker films, the thickness is long compared to the localization length; in Pt-richer film, the localization length decreases. We have not studied their temperature dependence, which would more clearly reveal the likely conduction mechanism. However, in lower HR films (thinner or higher Pt concentration), an empirical equation (Eq 6-13) attributing to the FIT model seems to fit the I-V data, as shown in Fig. 19. Note that the FIT prefactor $G_{0,T}$ is weakly temperature sensitive, which cannot be verified without the temperature study.

$$G(V) = G_{0,T} \frac{\exp(V/V_0)}{1+h_v[\exp\left(\frac{V}{V_0}\right)-1]} \qquad \text{Eq. 6-13}$$

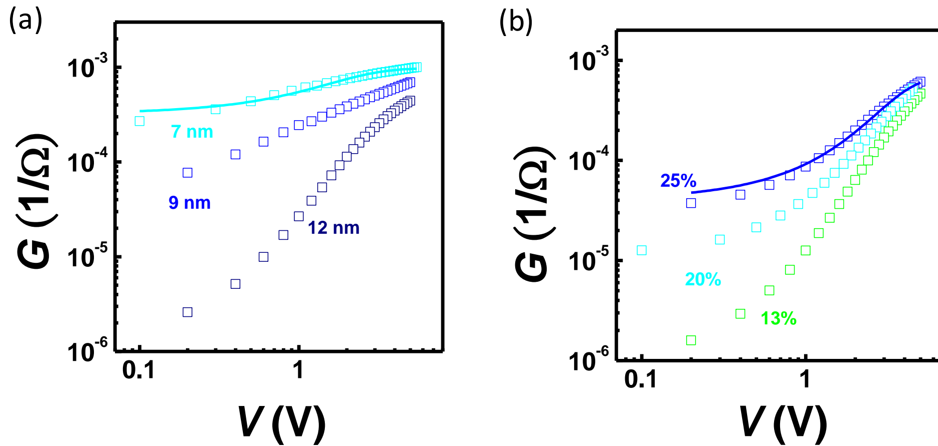

Fig. 19 G-V of (a) Pt/SiO_2-0.2Pt/Mo of three thickness, and (b) Pt/SiO_2-Pt/Mo with 20 nm of three Pt concentrations.

With the same reservation as stated above, we found that, at low voltages, the voltage dependence may be again described by equation (6-13) for the conductance of the intermediate HR state. The later experiments were performed on a 20 nm Pt/SiO_2-0.2Pt/Mo film. Here, a much more extended small voltage region was experimentally probed, showing Ohmic behavior in Fig. 20. In addition, measurements at different temperatures were also made. The low-voltage conductance has a relatively weak temperature dependence from 10 K to 293 K, which appears to suggest FIT. At high voltages, however, FIT's voltage dependence appears too weak to account for the data, and an FNT fit (see blue curve in Fig. 20) is used to supplement it.

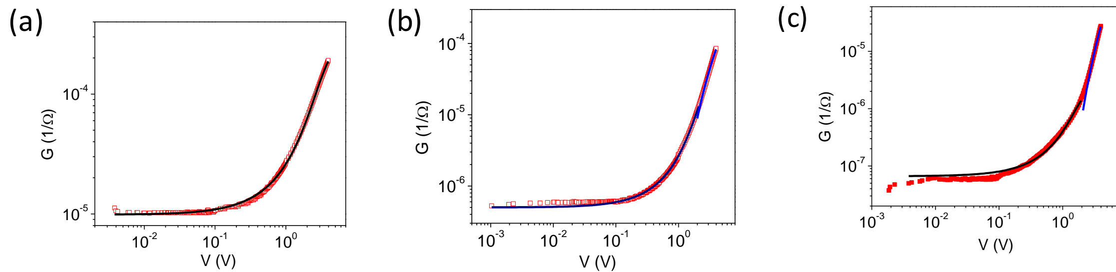

Fig. 20 Pt/SiO_2-0.2Pt/Mo G-V curves of an intermediate state (curve 1 in Fig. 12) - fitting with Eq. 6-13 (referred to as FIT fitting, in black) and with Eq. 6-12(referred to as FNT fitting, in blue),, at (a) 293K with FIT fitting, (b) 157 K with FIT + FNT fitting, and (c) 10 K with FIT + FNT fitting.

VI. Discussion

In both Pt/SiO_2-Pt/SRO and Pt/SiO_2-Pt/Mo devices, switching voltages have been measured over a wide range of temperature, 10K up to 428K, and they are temperature independent. This phenomenon strongly argues against a thermally activated switching

mechanism, such as filamentary formation and rupture or oxygen vacancy migration. (RRAM that involves ionic/atomic motion are usually strongly power dependence ($V \times I$), which should be dependent on local resistivity that is temperature sensitive in such material. Therefore, the switching voltage should also depend on temperature[8,9].) However, in certain filamentary type RRAM, resistance switching behavior is observed without increasing switching voltage at low temperature. This phenomenon is explained by the highly localized nature of filamentary forming/breaking[30]. So the voltage's temperature independence may not seem like a sufficient reason to rule out the filamentary mechanism by itself. On the other hand, in the SiO_2-Pt device, the HR state has a strong thickness dependence, which is consistent with a switching phenomenon that happens throughout the film, not at a certain "node". (The HR of filamentary RRAM is thickness independent.) Therefore, if the switching behavior is thermal activated, it should be reflected in the temperature dependence of the switching voltage, which is not in our case. This and other evidence presented elsewhere in this thesis clearly indicate that the SiO_2-Pt RRAM device is a purely electronic switching memory.

Concerning the conduction mechanism, our HR state conductance has a strong temperature dependence consistent with the Arrhenius type or the VRH type at high temperatures. Therefore, in this temperature range, it has the character of an insulator, with a strong thermal activation that motivates conduction. However, even this state often shows a saturating resistance at low temperatures, which is not the typical behavior of an insulator. Indeed, its low temperature conductance can be fit by a tunneling model, FIT, strongly suggesting a metallic behavior that provides the residual conductivity when the activation-driven conduction is exhausted. This behavior is similar to that of a bad

metal[25]. This metallic character becomes progressively stronger as the HR state transitions to the intermediate states, and eventually to the LR state. Although the resistance of the latter is difficult to ascertain, due to the strong contribution of the bottom electrode resistance to the apparent resistance, it is important to note that there is no evidence of resistance increase even at the lowest temperature, meaning that the LR remains very low throughout the temperature range studied here. We therefore believe this is consistent with a LR state being a metallic state.

The above picture is mainly obtained using a 20 nm film with a Pt content of 20%. In films of a lower resistance (thinner film or higher Pt concentration), there is evidence that FIT is becoming increasingly dominant, possibly responsible for conduction even at room temperature. This behavior is consistent with the nanometallic transition: the regime of nanometallicity becomes more dominant at thinner thickness and higher Pt content. However, more measurements of their temperature dependence are needed to substantiate this claim.

Lastly, at large voltages, there is evidence that conduction in the HR state is field driven, in a manner similar to that described in the FNT model. This is not surprising, since the barrier height in our material appears to be of the order of 1 eV, and the voltage in some experiments exceeded it. Interestingly, at 10K where the low voltage conduction of the HR state and intermediate HR states is clearly FIT without field assistance, the high voltage conduction still appears to follow the FNT picture.

VII. Conclusions

1. The switching voltages are temperature independent according to the I-V and R-V curves from 10K to 428K. This is strongly indicative of an electronic switching mechanism.
2. The nominal LR remains low and temperature independent down to 10K, showing no evidence of any uptick which could indicate insulating behavior. Therefore, most likely, the LR state is metallic.
3. An ohmic conduction region is found at low voltage for the HR state in the SiO_2-Pt device. In this region, the FIT mechanism at low temperature and FIT plus VRH mechanism at high temperature are responsible for conduction in the HR state.
4. The VRH mechanism is dominant at high temperatures, over which the HR state may be regarded as an insulator state. The Arrhenius activation energy is of the order of 0.17 eV.
5. At low temperatures, VRH and other thermally activated conduction mechanisms are exhausted, which lead to FIT dominance at temperature below 150K. Below this temperature the HR state may be regarded as a dirty metal.
6. The range of FIT dominance possibly expands as the range of nanometallicity expands: in thinner films, and in Pt-richer compositions.
7. FNT conduction is the dominant conduction mechanism at very high voltage in the HR state and intermediate states, even at 10K.

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Chapter 7 Capacitance

I. Introduction

Capacitance is an important characteristic for fast electronic devices. The operation speed is ultimately limited by the resistance-capacitance (RC) time constant of the circuit, in which the device capacitance sets the lower bound for the circuit capacitance. Signal fidelity is also influenced by the RC time constant, which may delay and distort the signal that hinders the function. This phase delay caused by the capacitors will become more important as the feature size of the device shrinks.

Impedance spectroscopy studies of resistive switching random access memory (RRAM)[1,2,3,4] have suggested different characters for the HR and LR states in filamentary type RRAM devices: an inductor dominates the conducting state of the device and a capacitive element dominates the insulating state[1,2]. In contrast, in Schottky barrier type RRAM, both states are dominated by capacitive elements[3]. The calculated dielectric constant from AC impedance data is quite close to that of the bulk dielectric material, indicating that this method is of great reliability.

In this chapter, we employ impedance spectroscopy to analyze SiO_2-Pt thin film devices. We will show that both the high resistance (HR) state and the low resistance (LR) state have a capacitive nature, making them behaving very differently from

filamentary type RRAM. We will also estimate the RC time constant as a function of cell size to ascertain its effect on device performance in fast operation. A comparison of R-C relations for different device configurations, Pt/SiO_2-Pt/SRO, Pt/SiO_2-Pt/Mo and Pt/SiO_2-Pt/Pt, will provide insight to their behavior.

II. Experimental Procedure

Three types of devices were investigated: Pt/SiO_2-Pt/SRO, Pt/SiO_2-Pt/Mo, and Pt/SiO_2-Pt/Pt. They were fabricated by the same method as described in previous chapters. After confirming the device switching performance by a Keithley 237 voltage/source measure unit, the cell was switched into the HR state, LR state or various intermediate LR (I-LR) state. For impedance spectroscopy analysis, an HP4192A Impedance Analyzer connected in series to the device was used. The typical frequency domain studied was between 100Hz and 1MHz over which reliable data could be obtained. Two types of tests were commonly performed: (a) a capacitance-voltage (C-V) scan, typically at the frequency of 10k Hz; and (b) a impedance-frequency scan with the results typically present in the Cole-Cole plot. In (a), the capacitance is calculated by the instrument (built-in: C_p mode in the instrument) software using a simple parallel R-C model.

Since our measurements used a probe station with long wires and probes,

considerable wire inductance was inevitable, which need to be removed by calibration or subtraction. Therefore, before any experiment was started/completed, a "blank" impedance-frequency scan was performed with the two probes shorted. (This scan showed an inductance behavior, as evident from Fig. 1.) The short-scan readings were subtracted from the device data to obtain the calibrated device data.

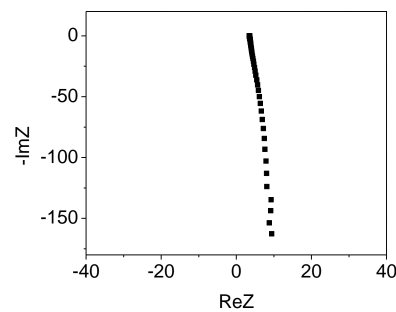

Fig. 1 Cole-Cole plot of short measurement.

III. Results

A. Pt/SiO_2-Pt/Mo system

The C-V scan of a Pt/SiO_2-Pt/Mo device shown in Fig. 2(a) verifies capacitance transitions that parallel the resistance transitions (Fig. 2(b)). In Fig. 2, the frequency is fixed at 10kHz, but essentially the same result is obtained at other fixed frequency of 10 kHz. The device, which starts at the LR state, initially has a low capacitance (~10 pF) that remains constant over a considerable range of voltage; this corresponds to the

ohmic LR state. At around + 5V, which is the same voltage for the resistance transition, the capacitance suddenly increases, indicating that the switching has been triggered and the device is now in the HR state. The HR state capacitance at 0 V is around 200 pF, which was considerably higher than that of the LR state. When a negative bias is applied to the cell, the capacitance decreases, but the slope increases visibly at about −1.5 V, which seems to parallel the reset transition in the R-V scan, suggesting that it is returning to the LR state.

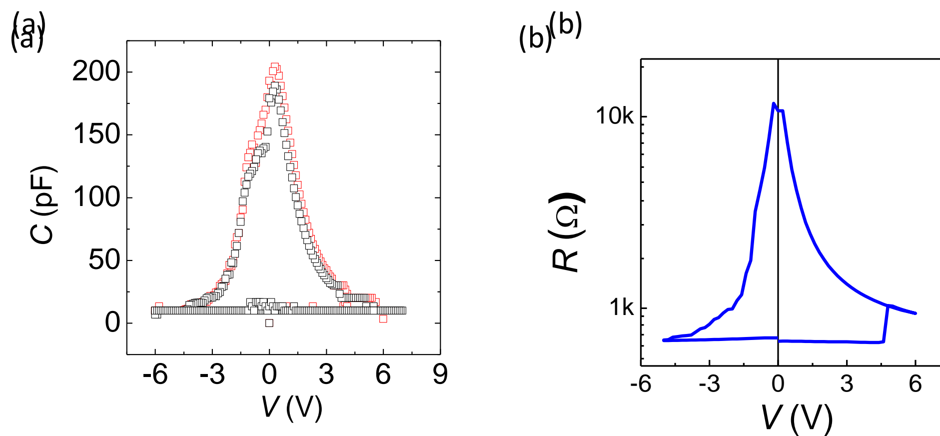

Fig. 2 (a) C-V scan on Pt/SiO_2-0.25Pt/Mo on fused Si substrate at 10 kHz, for two repeated scans. (b) R-V curve of the same sample.

As described in a previous chapter, there are usually many intermediate LR states, but the HR state is unique under normal testing conditions. Therefore, the varying capacitance seen in Fig. 2, especially the higher branch on the positive voltage side, is an indication that the HR state capacitor is non-linear, with a capacitance decreasing

with the voltage. In contrast, the LR state capacitor is linear, with a constant capacitance independent of the voltage. The gradual decrease of the upper branch on the negative voltage side, past the first reset transition, can now be attributed to gradual transition between ILR states, which apparently have various capacitances. Indeed, a lower-resistance ILR state must have a lower capacitance judging from the similar trend between the C-V hysteresis and the R-V hysteresis.

A typical Cole-Cole plot of the HR state in the Pt/SiO_2-0.3Pt/Mo device is shown in Fig. 3(a). The experiment is done by measuring the real part (ReZ) and the imaginary part (ImZ) of the impedance during a frequency scan under a constant voltage, with frequency ranging from 100Hz to 13MHz, from which the capacitance is computed. This is usually done through the Cole-Cole plot, shown in Fig. 3(b), with the aid of an equivalent circuit model, Fig. 3(c). (This equivalent circuit includes an external element R_o, which may be used to model the probe, the wire connection, and the bottom electrode contributions. The remaining parallel connection of a resistor and a capacitor is assigned to the film itself.) If the capacitor in the equivalent circuit has a fixed capacitance and no loss, then the Cole-Cole plot for the model should consist of two semicircles. The arcs in Fig. 3(b), however, are somewhat depressed, which necessitate the use of the constant phase element[5] (CPE) model for data analysis. This element has the following representation:

$$y = \sqrt{(\frac{0.5R}{sin(\theta)})^2 - (x - C_x - 0.5R)^2} - \frac{0.5R}{\tan(\theta)} \quad \text{Eq. 7-1}$$

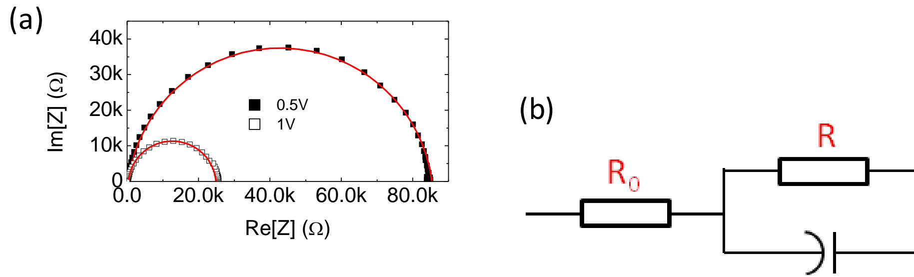

Fig. 3 (a) Cole-Cole plot of a Frequency scan on Pt/SiO_2-Pt/Mo film, and (b) CPE model schematic.

If R_o is ignored (only one circle), which is the case here because the probe contribution has been subtracted and the bottom electrode resistance is small compared to the HR, we can interpret the Cole-Cole plot in terms of CPE readily. The R value is the diameter of the half circle, C_x is the intercept of ReZ at the highest frequency, and θ is the offset of the circle by a rotation of the same angle, which causes depression. The n value, calculated from n= θ /90°, can then be used to judge the perfection of the circle: it approaches 1 for a perfect semicircle.

After obtaining the above parameters, we can calculate the capacitance of the device using:

$$C = 1 / (2 \cdot \pi \cdot R \cdot f) \quad \text{Eq. 7-2}$$

where R is the fitted result from the CPE model corresponds to the resistive element in the parallel part of the circuit and f is the highest point in the semi-circle. The calculated C value from Fig. 3(a) is about 65 pF for a cell of 80μm diameter.

The calculated capacitance values are compared with resistance values in Fig. 4. The C-V and the resistance-voltage (R-V) data have the same shape in this plot, although it should be noted that they use different scales. The results confirms that the capacitance of the HR state in this material (Pt/SiO_2:Pt/Mo) has a strong voltage dependence.

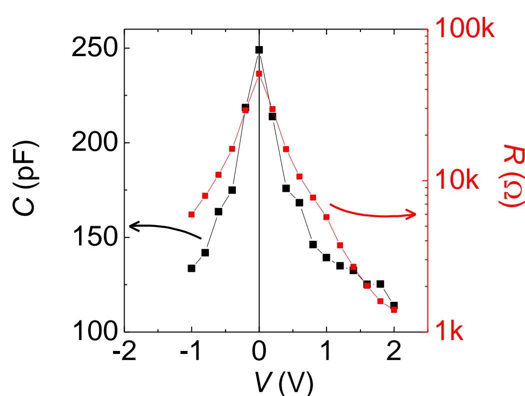

Fig. 4 C-V dependence of HR state with capacitance calculated from model fitting of Cole-Cole measurement.

The data of the LR state shows a strong inductance component when represented in the Cole-Cole plot. After subtracting the shorted-probe signal, the data better resemble a semicircle and the CPE model can now be used to fit the result, as shown in Fig. 5(a). The calculated capacitance value also appears to be 60 pF, but is relatively insensitive to the voltage. However, the n value is smaller, which probably indicates that there are other (dispersive) components in the half-circle.

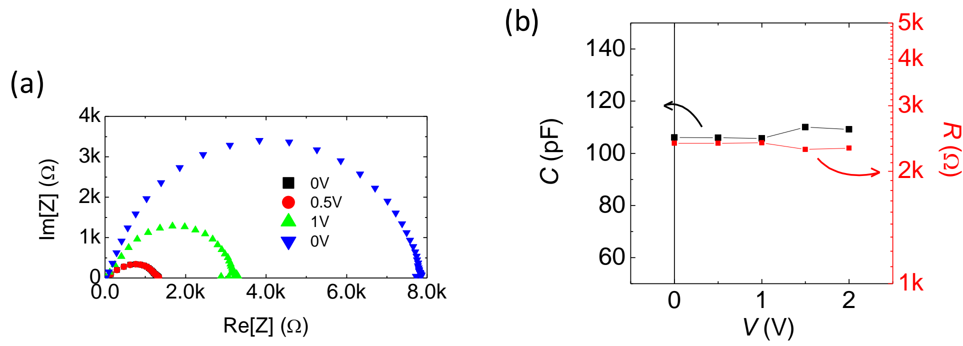

Fig. 5 (a) Cole-Cole plot of LR state after calibration, and(b)C-V dependence of Pt/SiO_2-0.25Pt/Mo LR state with capacitance from model fitting of Cole-Cole plot.

To probe the component of both HR and I-LR, Bode plot[6,7,8] is introduced to analyze the data. The Bode plot is obtained by plotting the imaginary part of impedance (ImZ) versus frequency. The peak frequency, corresponding to $f = 1 / (2\cdot\pi\cdot R\cdot C)$, is expected to move to higher frequency as the resistance changes due to switching or voltage. (The change in R(V) is much more than the change C(V), so it is R(V) that dominates.) However, in the Pt/SiO_2-Pt/Mo device, f saturates at large voltages when R falls below 1 kΩ. In addition, the shape of the plot at the low frequency is distorted. This indicates that another CPE (possibly due to the Mo BE) is in play in the low-R regime, which begins to dominate as the f (or R_{mix}) becomes smaller. The peak frequency determined in the Cole-Cole plot should be affected by such depression which result in a higher capacitance.

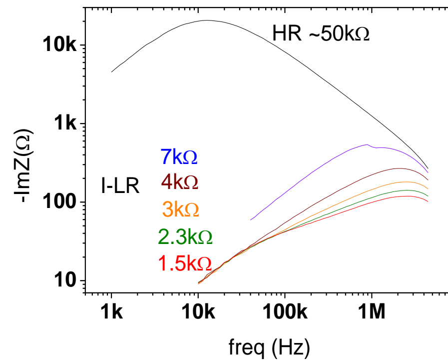

Fig. 6 Pt/SiO_2-0.25Pt/Mo bode plot, the black curve denotes HR state, and the others are I-LR state.

In Fig. 7, we summarize the R-C correlation from the HR state to I-LR state to LR state for Pt/SiO_2-Pt/Mo. The C decreases when R decreases, and seems to saturate at approximately 40 pF, which could be due to Mo BE element. In smaller cell size, the capacitance value calculated for LR states were more strongly affected by the line capacitance.

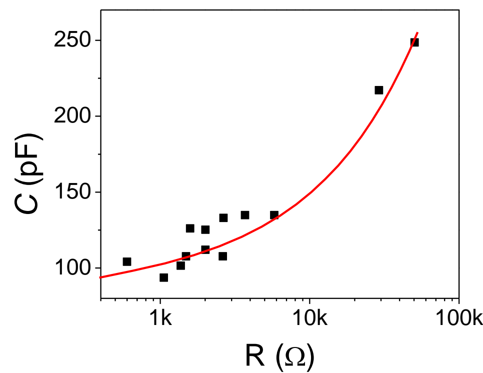

Fig. 7 C-R dependence data from HR state and LR state (cell size: 2.2 x 10^{-4} cm^2).

A comparison of the HR state capacitance in cells of different cell size is shown in Fig. 8(a). A linear dependence with a slope close to unity is found, indicating that the

capacitance is proportional to the cell area. For the LR state, the capacitance also decreases as the cell size decreases, but it reaches a saturation value of 60 pF at around 80μm diameter. This is probably due to stray capacitance, which comes from the nearby cells in the sample. (In the LR state, there is communication between neighboring cells if those cells are also in the LR state.) In fact, we found the RC becomes so large for smaller cell sizes that *f* can no longer be measured in the frequency range we used. This indicates that background signals either from the BE or the nearby cells, which does not follow area scaling, have come into play. In Fig. 8, the two branches crossover at a cell size about 70 to 80 μm. This crossover is real: we found the capacitance of the HR state indeed gradually decreased as the resistance decreased through the intermediate LR state, but the capacitance suddenly increased when at the resistance of the intermediate LR state falls further (Fig. 8(b)).

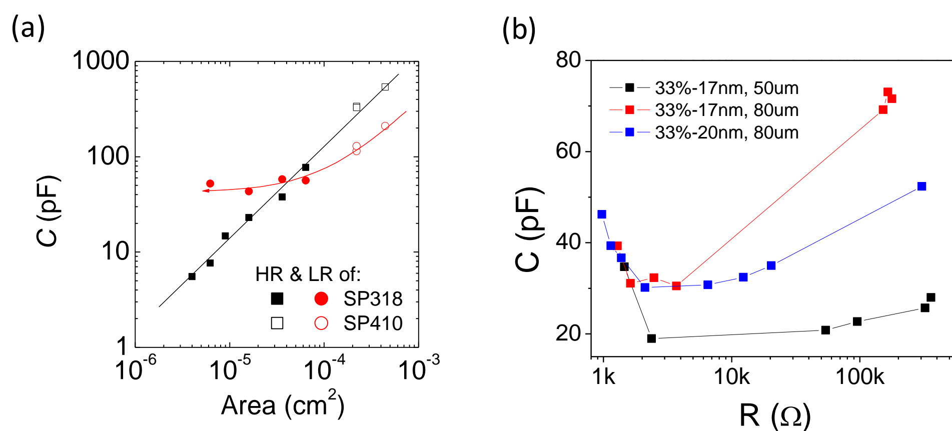

Fig. 8 (a) Cell size dependence for capacitance; black: HR state; red: LR state. (b) Sudden increase of capacitance when intermediate LR falls further in smaller cell size (red and blue: 5 x 10^{-5} cm^2, black: 2 x 10^{-5} cm^2).

Lastly, the thickness dependence of the HR state is presented in Fig. 9. The capacitance increases with decreasing thickness.

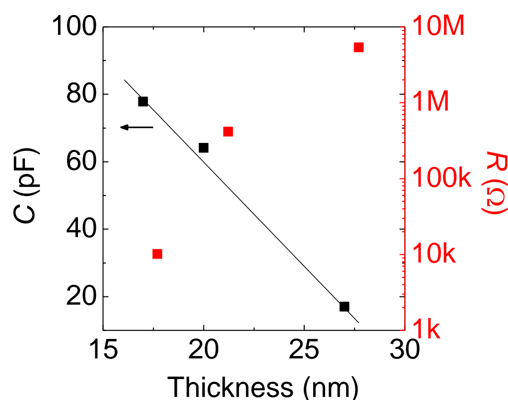

Fig. 9 Thickness dependence of black: capacitance, red: resistance.

B. Pt/SiO_2-Pt/SRO system

Frequency scan measurements made on an 80 μm diameter Pt/SiO_2-0.25Pt/SRO cell show a HR state capacitance of approximately 65 pF, which is not inconsistent with the capacitance of the Pt/SiO_2-Pt/Mo device. Unlike the Pt/SiO_2-Pt/Mo device, however, the capacitance of the Pt/SiO_2-0.25Pt/SRO device shows less voltage dependence. The C-V loop of the HR state for this cell shown in Fig. 10 is almost constant over the voltage range. C-V scans of LR value are untrustworthy, because LR is too low and the measured spectrum mainly comes from the BE and the line impedance, the conversion of the instrument using simplify RC model does not hold

for this situation.

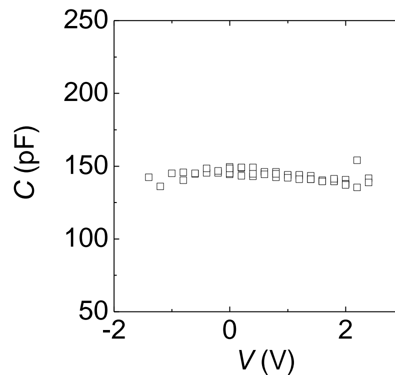

Fig. 10 C-V scan of the HR state of a Pt/SiO_2-0.25Pt/SRO device.

Further analysis of the capacitance was performed using the Cole-Cole plot. Both the HR state and the LR state have nearly constant capacitance, see Fig. 11. Also done here is the Bode plot analysis, shown in Fig. 12. Unlike the Pt/SiO_2-Pt/Mo case that shows saturation of frequency and distortion of the curve, the Pt/SiO_2-Pt/SRO system seems to be closer to an ideal capacitor and the curve at lower ILR state does not show depression. Again, we are not able to measure capacitance at below 1000 Ω for the LR state. The impedance is too low compared to the background that is included in the calibration (by subtracting the short measurement data), making the subtracted data inaccurate (mostly at high frequencies). In principle, this may be avoided by adding a load in series to shift the whole curve; but this has not been done. Therefore, there seem to be some problems with the quality of some of the data presented above.

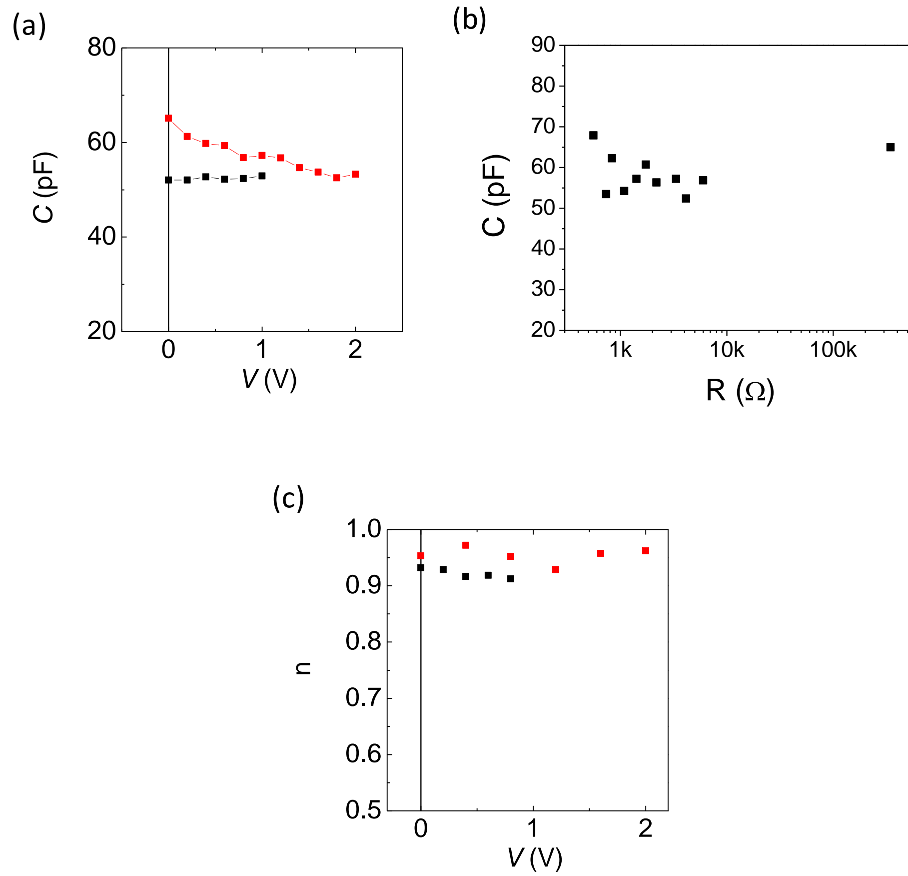

Fig. 11 (a) C-V dependence of a Pt/SiO_2-Pt/SRO device, (red: HR; black: LR) and (b) C-R dependence (c) n versus voltage plot of the same device.

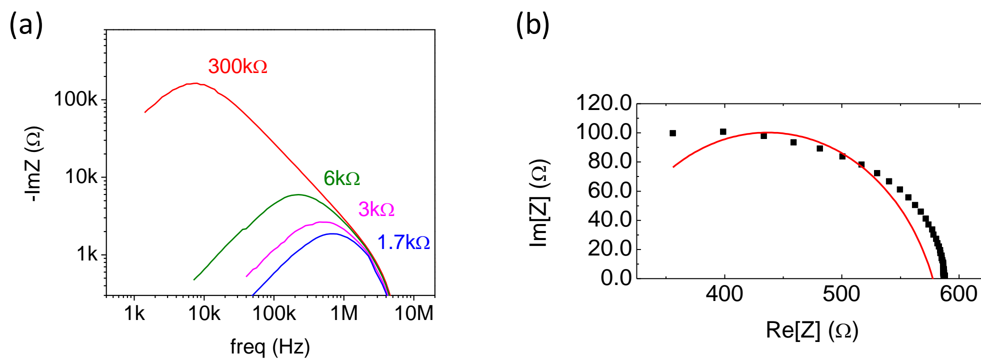

Fig. 12 (a) Bode plot of the Pt/SiO_2-Pt/SRO device of HR and various ILR states. (b) Low LR state after calibration showing poor data points at high frequencies (near the Im(Z) axis.).

C. Pt/SiO_2-Pt/Pt system

Since the Pt/SiO_2-0.25Pt/Pt device can be brought to the HR state, it is possible to take C-V measurements and the frequency scan giving the Cole-Cole plot for this state. In the Cole-Cole plot, the low frequency part is highly distorted, possible due to too high an impedance value. So only the high frequency part is fitted. It shows a capacitance around 300~400 pF for a 168 μm diameter cell. This value is not unlike the capacitance of other devices of a similar size. Just like the Pt/SiO_2-Pt/SRO device, it does not show any C-V dependence. The C-V scan under 10 kHz shows acapacitance value between 300~400 pF from −3 V to +3 V. A sudden drop always appear at > +2V for which we have no explanation.

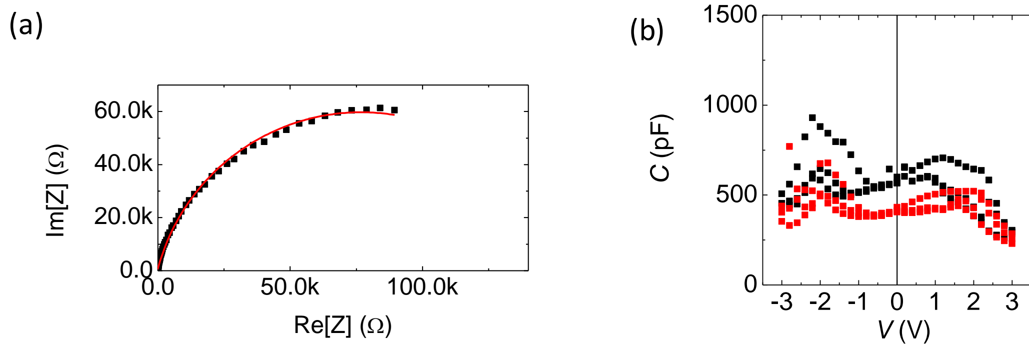

Fig. 13 (a) Cole-Cole plot of Pt/SiO_2-Pt/Pt device. (b) 2 C-V measurements of the same cell measuring from -3V to +3V and then back to -3V.

IV. Discussion

Unlike filamentary type RRAM devices, which show a strong inductive component in impedance spectroscopy when the cell is tested in the LR state, our devices all show capacitive behavior when the external (probe-wire) contribution is removed. This provides more evidence of non-filamentary type switching behavior.

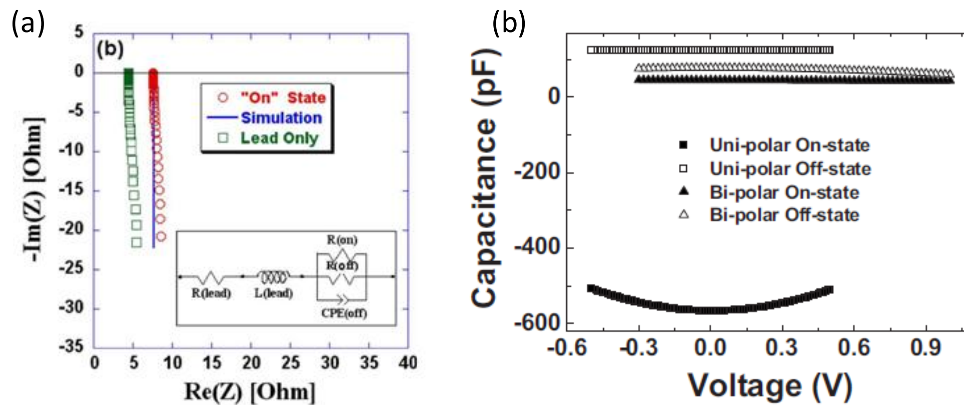

Fig. 14 (a) NiO RRAM LR state showing inductance behavior[1], (b) a unipolar NiO RRAM (Pt/NiO/Pt) showing inductive on state, and bipolar NiO RRAM (Pt/NiO/SRO) showing capacitive on state[2].

It is well known that a C(V) dependence may arise from a built-in field, which is due to the space charge of carriers[9,10]. As this space charge redistributes under a field, the capacitance changes. However, this model cannot be used in our systems because it also predicts an asymmetric C(V) upon change of polarity, which is not observed in our devices. Indeed, this lack of asymmetry immediately rules out any internal bias in our films.

One might suspect that the C(V) dependence may come from the field dependence of dielectric function, which is well documented in $(Ba,Sr)TiO_3$, for example. However, it is curious that only the device with a Mo bottom electrode shows a significant C(V) dependence. This usually implies that such dependence is related to the interface. Yet, an interface capacitor can be analyzed using an equivalent circuit, and it should not influence the R-C characteristics of the mixture film, which has no C(V) dependence in the absence of the Mo bottom electrode. This is puzzling. This could suggest that some defects are formed only in the Mo-containing device, and that they have diffused into the film. The other possibility is that the polar part of the electrode/film interface is not a simple interface. For example, it is not contiguous and must be regarded as both an element in parallel and in series. Further study of this aspect is needed.

The RC time constant is larger for the HR state. It has a value of about 10^{-5} s. For the LR state, it is 10^{-8} s. The cell size dependence of these constants is weak, as it should for conventional R-C configurations. (For parallel plates, R is inversely proportional to the cell area, and C is proportional to the cell area. The constancy of RC can be more generally proved for an arbitrary linear dielectric/conductive system.)

Lastly, we calculate the dielectric constant using

$$C = \varepsilon_0 \varepsilon_r \cdot A/d \qquad \text{Eq. 7-3}$$

where d is the effective thickness of the mixture film. The calculated ε_r, using a thickness of 20 nm, is about 34 for HR and 11 for LR, which are considerably higher than that of the SiO_2 dielectric constant. This overestimation could be due to an overestimation of the effective dielectric thickness. Our film contains a large population of nanometallic paths, and it is the junctions that separate these paths that contribute to the capacitance the most. The effective thickness must be very thin, since it can be overcome by electron tunneling during switching. Taking the dielectric constant of (dense) SiO_2 as 3.9, and that of a porous film as 3.4, we then find a thickness of 2 nm would be consistent with the capacitance of the HR state. The reason that the LR state has a lower capacitance may then be attributed to the shorts over many of the dielectric junctions.

According to the above C-R/C-A relation and the parallel circuit model discussed in the previous chapter, a simple prediction of the C-R relation can be made. Here, we assume each conduction path contains one resistor and one capacitor, and the BE (especially Mo) also contains a set of resistor and capacitor. The total capacitor in the mixture film can be expressed as:

$$C_{total\text{-}mix} = C_1 + C_2 + C_3 + \ldots + C_n \qquad \text{Eq. 7-3}$$

with each C having either a C_{HRS} or a C_{LRS} depending on the resistance state. We also

assume $C_{HRS} > C_{LRS}$.When the device is in the HR state, meaning

$$C_{total} = n \cdot C_{HRS}, \qquad \text{Eq. 7-4}$$

both R and C are high, resulting in a high frequency. When x paths are switched to the LR state,

$$C_{Total} = (n-x) \cdot C_{HRS} + x \cdot C_{LRS} \qquad \text{Eq. 7-5}$$

Meanwhile, the resistance also decreases as described in the previous chapter, so the maximum frequency decreases. This picture predicts the correct trend of the C-R dependence but quantitatively it does not provide a satisfactory fit to the data. More work is thus needed to explain our observations.

V. Conclusions

1. The SiO_2-Pt device has capacitive HR and LR elements, which is different from the filamentary type RRAM (that has an inductive LR state).
2. The capacitance scales proportionally with the cell size. This indicates that the RC value will remain constant when the cell size is scaled down.
3. The LR state has a smaller resistance and a smaller capacitance, thus it is more immune to the scaling issue. The above two points are summarized in Fig. 15.

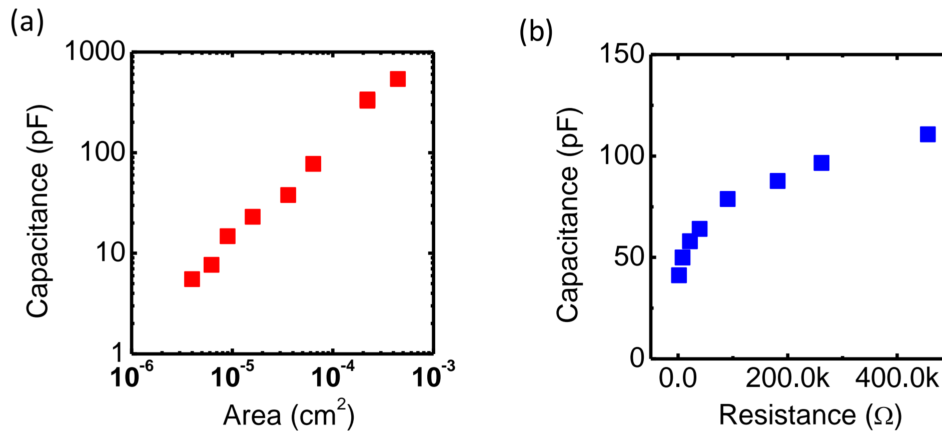

Fig. 15 (a)Capacitance vs area, (b) capacitance vs resistance of Pt/SiO_2-0.25Pt/Mo.

VI. References

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Chapter 8 Dynamic Switching

I. Introduction

Switching speed is important for resistive switching random access memory (RRAM). To compete with state-of-the-art flash technology, fast write/read operations are prerequisites. Phase-change memory (PRAM) [1,2] is promising in this respect because of its fast erase speed (~ns), but its write speed is relatively slow (~μs). RRAM devices are believed to have fast write/erase speed. Rupture of conducting channels involving local Joule heating or bias-driven oxygen vacancies over a very short distance can facilitate fast operation, which is the main switching mechanism proposed for the redox-based RRAM. The mechanism is considered to be very fast in both write and erase (~ns). In their study of dynamic switching of a TiO_2 and other ion-migration-based RRAM devices[3], Choi et al. found the transient time (recorded on an oscilloscope) of both set and reset switching to be power-dependent: shorter pulse width requires a larger voltage[4]. In the SiO_2-Pt device, switching is electronic in nature (electron speed ~ 0.01 to 0.1×speed of light), so it should switch faster than ion-migration-based RRAM devices, and it should not suffer from power dependency. On the other hand, a "voltage-time dilemma" has been recently claimed: that fast switching speed is incompatible with long retention time in electronic-switching

RRAM devices under normal operating voltages (a few V)[5]. Hence, documenting the switching speed relative to the retention time is needed in order to assess the practical prospect of the SiO_2:Pt device.

In this chapter, dynamic switching in SiO_2-Pt is studied by two methods. The first one is to determine the voltage required to effect switching within a certain pulse width. For an accurate determination of this relationship, detailed information of the excitation and response pulse shapes is recorded using an oscilloscope. The second one is to determine the change of resistance, as an indication of the change of state, under a certain voltage. This so-called constant voltage stressing (CVS)[6,7] test motivates the time-dependent switching in the "sub-critical" regime, because the voltage used is well below the standard set and reset voltages used for write/erase. This method has been widely used to evaluate dielectric breakdown of SiO_2 in metal-oxide-semiconductor field effect transistors (MOSFET)[8,9,10], and it provides information that may be used to estimate the tunneling or field-emission parameters, such as barrier height in the Fowler-Nordeihm tunneling (FNT) model[11,12]. Additional information on time-dependent structural changes may also be possible from such analysis.

II. Experimental Procedures

Fast switching dynamics was studied by measuring the waveforms of the excitation and the response as a function of time using the configuration in Fig. 1(a). An Agilent 81104A Pulse/Pattern generator connected in series with an Agilent function/arbitrary waveform generator provides the voltage excitation. Oscilloscope (HP Infinium) channel 1 records this excitation parallel to the device (Pt/SiO_2-Pt/Mo), and oscilloscope channel 2 records the voltage on a load, hence the current that passes through the device. The internal resistance of the oscilloscope is 50 Ω in both channels 1 and 2. The actual pulse shape measured by oscilloscope channel 1 shown in Fig. 1(c) for a square wave excitation suffers from distortion: the wave form of the first 50 ns is highly distorted, probably due to the RC time constant of the circuit itself. In contrast, a trapezoidal wave with a certain rise and fall time defined in Fig. 1(b) is much better preserved as shown in Fig. 1(d) (with 50 ns lead time and trail time, defined at the time to reach 50% of the desire pulse amplitude.)

Constant voltage stress test was performed by subjecting the cell to a constant voltage and observing the resistance value until it changes rapidly signaling resistance switching is being triggered. Both the HR state and the LR state (including intermediate LR states) of the Pt/SiO_2-Pt/SRO and Pt/SiO_2-Pt/Mo devices were tested for comparison. These tests were also repeated at high temperatures (85°C and 150°C

for samples with SRO BE, and 85°C only for Mo BE—to avoid Mo oxidation.) In addition, retention tests were performed at 85°C following the same procedure described in a previous chapter.

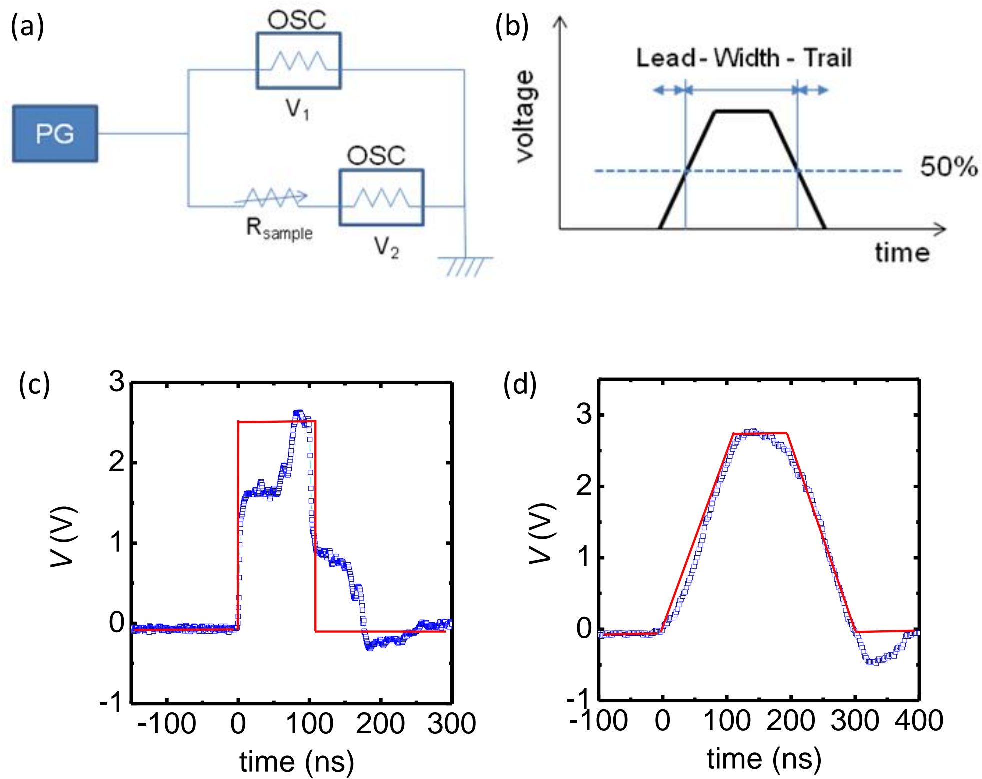

Fig.1 (a) Connection schematic, (b) definition of a pulse waveform, (c) a typical square pulse distorted by RC time delay, and (d) trapezoidal shape showing better signal.

III. Results

A. Fast switching

Comparisons are made for a cell undergoing (i) set switching from the LR state to

the HR state under a positive bias; (ii) non-switching with the device in the LR state under a positive bias; (iii) reset switching from the HR state to the LR state under a negative bias, to obtain information on switching. In Fig. 2, we show the current-time (I-t) traces (Oscilloscope channel 2) using an excitation with a pulse width of 200 ns and a 50 ns lead time and trail time. The two blue curves are essentially identical, both for the non-switching case (ii) under a positive bias but with the excitation voltage just short of being able to trigger a set transition. Their waveforms are similar to that of Fig. 1(d) and they may be taken to be the same as the excitation voltage, with some smoothing as it passes through the circuit.

During set switching (off switching), case (i), a slightly larger excitation voltage is used so the current shown in green in Fig. 2(a) has a slightly higher amplitude than the blue curve. It initially tracks the blue curve—the non-switching case, indicating a slightly higher current, hence the voltage in the cell is also slightly higher tracking the excitation voltage. Then it suddenly decreases relative to the blue curve, indicating a loss of current, thus an increase of the total and cell resistance, signaling the set transition. The post-switching green signal suffers from rapid oscillation, which is due to reflections in the cable used in the measurement circuit. This measurement was repeated after bringing the cell back to the original LR state, and essentially identical results shown as the red curve were obtained. Note that the sudden drop appears to be

faster than 50 ns, which may be taken as the switching time recorded in this experiment.

The reset switching (on- switching) of case (c) is shown in Fig. 2(b), with the two repeated tests represented in red and green, which are again essentially identical. The blue curve corresponds to the current on the load, with the cell reset to the LR state. After that, the cell is set to the HR state and a negative excitation is applied. The current on the red and green curves is initially smaller than the blue one because the cell now has a much higher resistance. Then it increases gradually after 50 ns and reaches the same value as the blue curve over another 50 ns, indicating that the cell resistance has returned to the LR state during the latter period so that the load current can rise. The important feature of reset transition is its gradual nature: no oscillations due to cable reflection is apparent. This difference is consistent with the multiple-step nature of the reset process in a standard R-V curve in which the resistance gradually returns to the LR state, in contrast to the one-step nature of the set process in which the resistance suddenly rises by a factor 3 to 4.

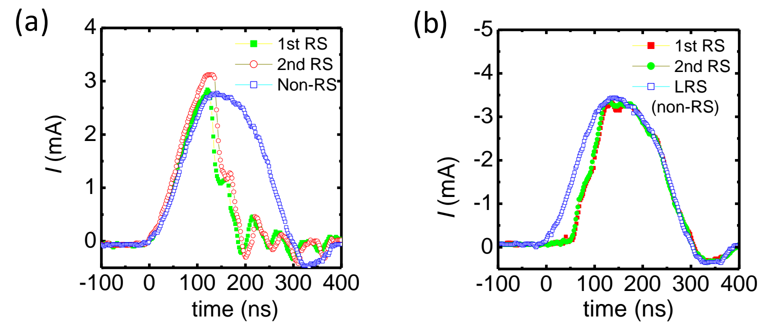

Fig.2 Fast switching of (a) set transition, and (b) reset transition, blue curve indicating non-switching case.

Next, we investigated the relation between the switching time and the switching voltage. A series of voltage pulses of increasing amplitude with either a positive or a negative bias were applied to the cell, and a small reading voltage was applied after each pulse. Measurement pulse time was varied from 10 ms to 50 ns. The results indicate there is no change in the value of the resistance obtained by switching; there is no systematic variation in the switching voltage, they all cluster at 3.5 V for set transition and −1.9 V for reset transition regardless of the pulse width.

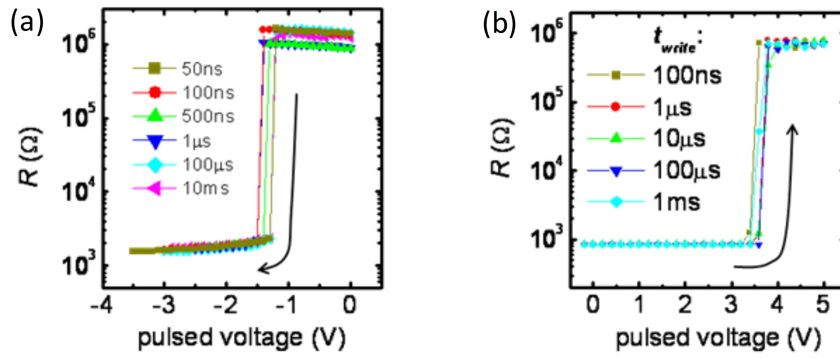

Fig. 3 (a)On-switching, and (b)Off switching under different applied pulse width.

B. Retention-write time relation

We investigated the retention behavior of cells that have been switched by pulses of different widths. Here we focus on two pulse widths (10 ms and 100 ns) that are sufficiently different. After write/erase, the cell was placed in an environment of 85℃, and the resistance is monitored over time by removing the sample from the environment to allow reading at room temperature. Both the HR and LR states written/erased using 10 ms and 100 ns pulses are able to retain their resistance states for 10^5 seconds, according to Fig. 4(a). These data are replotted in Fig. 4(b) in terms of the ratio, retention time/write time ($t_{retention}/t_{write}$), which may be regarded as a normalized memory retention relative to the write intensity. The normalized retention for memory written at 10 ms and 100 ns follows the same trend. If the trend, already held for $t_{retention}/t_{write}$ from 1 to 10^{12}, is extrapolated to the target $t_{retention}/t_{write}$ of 10^{16},

then our device should exhibit good memory retention for applications. (The slow increase of HR is probably due to Mo oxidation, as described in chapter 4 and also later in chapter 9.)

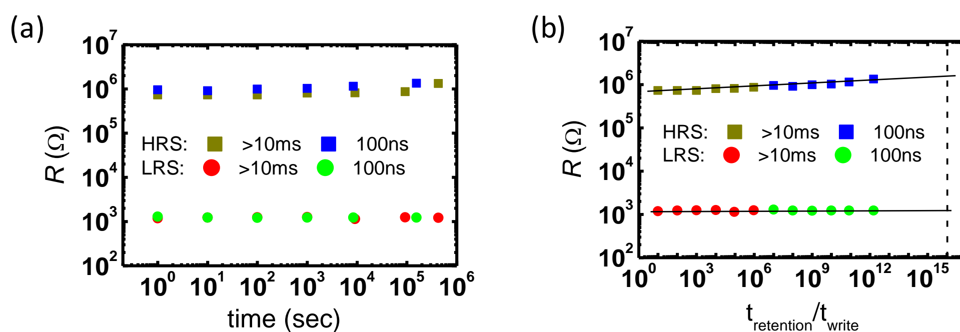

Fig. 4 (a)Retention at 85˚C under 10ms pulse and 100ns pulse, and (b) replotted against $t_{retention}/t_{write}$.

C. Constant voltage stressing experiment (CVS)

To study set transition under CVS, we first reset a Pt/SiO_2-Pt/SRO device to a LR state of about 1 kΩ . This LR state is one of the “intermediate” LR states, having a set voltage (V_{set}) of about 1.6 V in a standard I-V or R-V plot. Next, a set of constant voltage of 1 V, 1.2 V, 1.3 V, and 1.4 V is applied to the cell, and this voltage is held constant until resistance switching occurs, which appears as a relatively sudden rise in resistance over a relatively short period of time in Fig. 5(a). Under 1 V stressing, the cell switches to the HR state at about 20,000 seconds; under 1.4 V stressing it takes about 0.2 sec. Similar results are also shown for a Pt/SiO_2-Pt/Mo sample.

As described in a previous chapter, various LR states differ in the amount of trapped charge they contain, and they have different resistances and set voltages, which are positively correlated. This difference in set voltage is more a result of voltage sharing with the bottom electrode, and less an indication of changes in the intrinsic switching requirement, because the true switching voltage, V_m, remains rather constant. Therefore, we can regard the CVS of different LR states, with different V_{set}, as in Fig. 6, for six different states from V_{set} = 1.1 V to 5.3 V, as reflecting basically the same phenomenon, and with basically the same true voltage. Parallel data sets will be consistent with the idea of voltage partitioning, which appears to be the case here. The larger scatter in the data with a higher V_{set} is reasonable because the share of the voltage in the film is much smaller in such case, which makes the cell more susceptible to noise. Despite the scatter, however, it is clear that states with a higher V_{set} can retain their LR for a longer time if the same stressing voltage is used. Clearly, this would be advantageous for device stability.

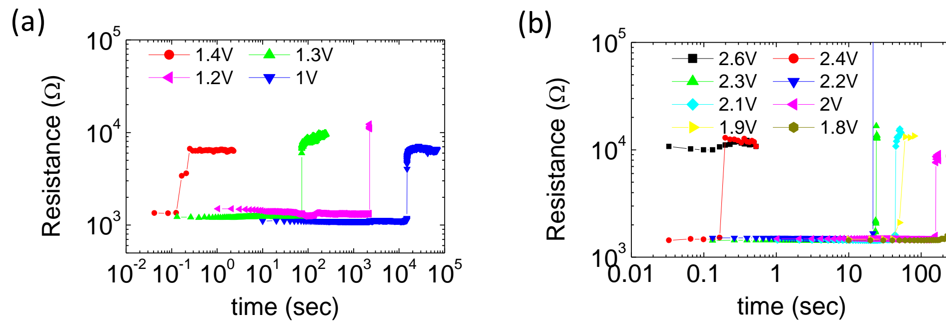

Fig. 5 CVS test under same resistance state on (a) Pt/SiO_2-0.3Pt/SRO device, and (b) Pt/SiO_2-0.3Pt/Mo Device.

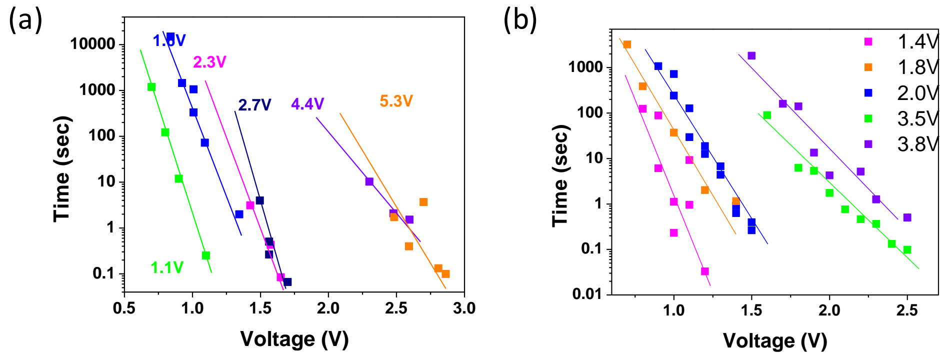

Fig. 6 CVS plot with different resistance states of (a) Pt/SiO_2-0.3Pt/SRO, and (b) Pt/SiO_2-0.25Pt/Mo device.

To study CVS for reset transition, the cell is first set to the HR state and a negative bias is applied to the cell to allow resistance decrease over times (typically monitored for at least 300 seconds). (As described in a previous chapter, the HR state usually is "unique", in that intermediate HR states are more difficult to attain in most experiments.) Figure 7(a) shows the data of a test under −1 V, which contain multiple steps, indicating that each rapid reset transition is followed by an incubation time before the next transition can be triggered. This is an entirely different behavior from

that shown in Fig. 5, in which the CVS triggers a sudden set transition to a common HR state.

We believe the step-like nature is due to the multiple-state nature of the LR states, and each step in Fig. 7(a) corresponds to an intermediate LR state. From the standard R-V curve of reset transitions, shown in Fig. 7(b), we can identify these states using their characteristic resistance values. This correspondence also provide the characteristic voltage for the state, which is now written next to the step in Fig. 7(a). With this information, the data in Fig. 7(a) can now be re-interpreted as (1) CVS of the HR state to the first intermediate LR state, that has the lowest characteristic voltage and the highest resistance, and (b) successive CVS (under −1 V) of various LR states of increasing characteristic voltage and decreasing resistance. In the following, we will refer to these characteristic voltages as "V_{reset}."

To repeat the above test under a different stressing voltage, we reset the cell to the HR state after a certain CVS time, then apply another negative CVS voltage, which ranges from −0.5 V, −0.7 V, −0.8 V, −0.9 V, to −1 V. The data of different CVS tests are compared by grouping together the steps from different tests but with the same V_{reset}, reading their "residence time" on the step, and plotting the residence time against the stressing voltage for each V_{set}. This is shown in Fig. 7(c). It is clear that longer CVS time is required to reset states that have higher V_{reset} values. The above

results are for Pt/SiO_2-Pt/SRO devices, but the same results are found in the Pt/SiO_2-Pt/Mo sample, as shown in Fig. 8.

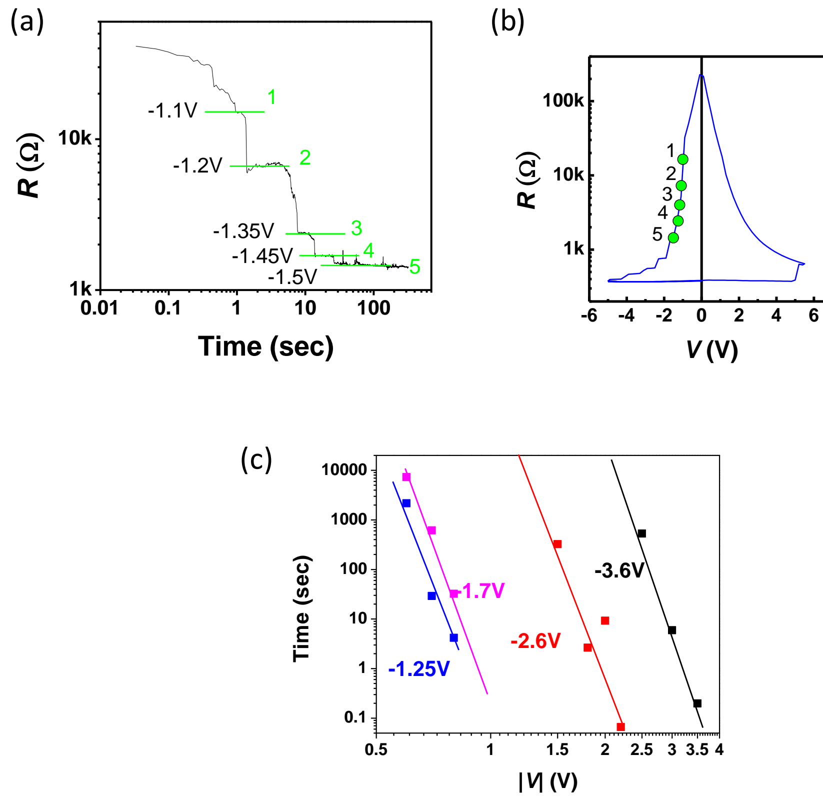

Fig. 7 (a) reset CVS test on a Pt/SiO_2-Pt/SRO device with their corresponding reset voltage, (b) standard R-V curve of the CVS test cell and the associate states in CVS stressing, and (c) CVS plot of reset process.

The high temperature CVS test results are shown in Fig. 8 for Pt/SiO_2-Pt/SRO devices. Similar tests were conducted using Mo BE, but at 85℃ to avoid Mo oxidation. The set transition shows a more gradual increase in resistance when compared with the room temperature result. Meanwhile, the switching time is more scattered (Fig. 8), and shorter. This is clear by comparing the temperature dependence

of the time-voltage plots in Fig. 8 for the same LR state in the Pt/SiO_2-Pt/SRO device. Very similar but more limited (only room temperature and 85°C) results are found in the Pt/SiO_2-Pt/Mo device.

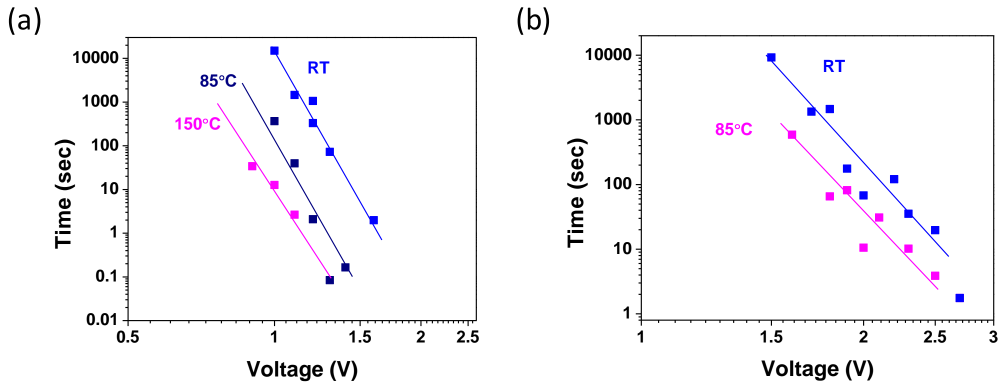

Fig. 8 Elevated temperature CVS in (a) Pt/SiO_2-0.3Pt/SRO and (b) Pt/SiO_2-0.25Pt/Mo device.

IV. Discussion

Firstly, from the V_m experiment mentioned in Chapter 6 (there, V_m is nealy a constant), we notice that there is a shared voltage from the bottom electrode depending on the mixture resistance. Hence, the stressing voltage cannot really represent the true voltage across the mixture film. We can convert the real applied voltage (V_{real}) on the mixture film from the resistance ratio of mixture and BE by the following equation:

$$V_{real} = V_{total} \times (R_{mix}/R_{total}) \quad \text{Eq. 8-1}$$

where V_{total} is the nominal applied voltage, R_{mix} is the resistance of the mixture film,

and R_{total} is the total resistance measured. This can be done by knowing the BE resistance, or simply by assuming that the effective voltage is the same since the BE resistance is not known with great accuracy. This means that each branch of the higher voltage data can be shifted horizonatally to coincide with the branch of the lowest voltage data, the latter nearly satisfy $V_{real} = V_{total}$ because its film resistance is the highest.

A. FNT model

The resistance switching phenomenon in the SiO_2-Pt device is governed by charge trapping/detrapping. Here, we apply a Fowler-Nordheim (FNT) tunneling model to the CVS experiment to estimate the barrier height and the retention time. The equation for FNT is shown below:

$$\frac{Q}{\tau V} = \frac{I}{V} = G = AV\exp(-\beta / V) \qquad \text{Eq. 8-2}$$

$$\ln(\tau V^2) = \ln\frac{Q}{A} + \frac{\beta}{V} \qquad \text{Eq. 8-3}$$

Here A is a pre-exponential coefficient, τ is taken as the time to trigger transition under CVS, and β is a constant of the dimension of voltage. The second form of the FNT equation suggests a linear FNT plot using τ and V.

Figure 9 and 10 is a FNT plot for both set and reset transitions of the SRO BE (Fig. 9(a) and 10(a)) and Mo BE (Fig. 9(b) and 10(b)) devices. Different colors in the same

figure refer to different LR states, having different initial resistance, which inversely correlates with the set voltage. But they have all been horizontally shifted to coincide with the lowest voltage branch. This procedure is justified since the actual film voltage in different branches should be quite similar in order to trigger set transition, which has a fairly narrowly distributed "critical voltage", so the actual voltage in the film must be nearly the same to trigger the same CVS phenomenon. Also shown in these figures are the requirement for 10 year retention (for τ). It can be seen that the data easily satisfy this requirement if the (read) voltage is set below a critical value. the LRS easily satisfied 10 years of retention even under 0.47 V voltage stressing, and the HRS satisfied 10 years retention under 0.43 V voltage stressing. These are true voltages in the film; the applied voltage can be much higher if there is much voltage sharing between the film and the BE.

We next calculated the reduced barrier height by the exponential coefficient β:

$$\beta = \frac{4(2m_{ox})^{1/2}t}{3q\hbar}\phi_b^{3/2} \qquad \text{Eq. 8-4}$$

Here, m_{ox} is the effective electron mass of SiO_2, and t is the effective thickness, which is unknown, but we will assume a reasonable tunneling thickness of 1~2 nm (obtained in Chapter 5). The calculated effective barrier height for set transition is 1.4 eV for the Pt/SiO_2-Pt/SRO device, and 1.18 eV for Pt/SiO_2-Pt/Mo. Similar results are

observed on reset transition. The barrier height is slightly smaller than that for the set transition, 1.35 eV for Pt/SiO_2-Pt/SRO device and 1.48 eV for Pt/SiO_2-Pt/Mo.

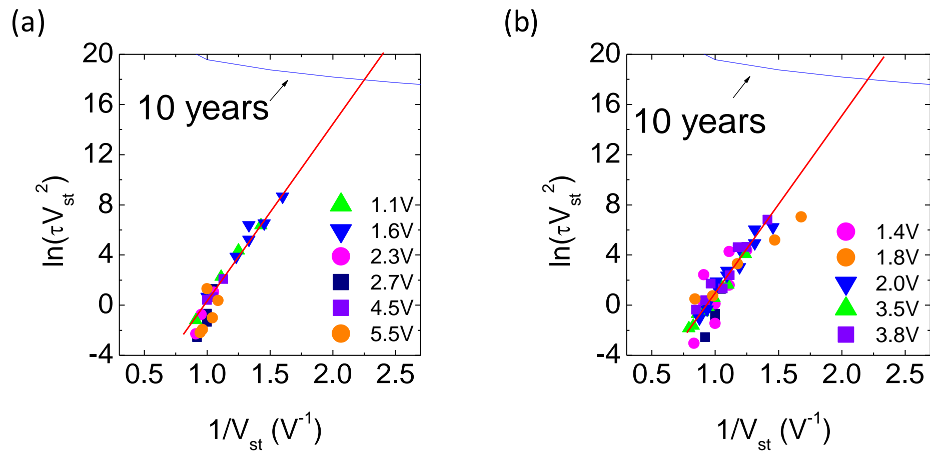

Fig. 9 FNT plot of set transition CVS test on (a) Pt/SiO_2-Pt/SRO device, and (b) Pt/SiO_2-Pt/Mo device.

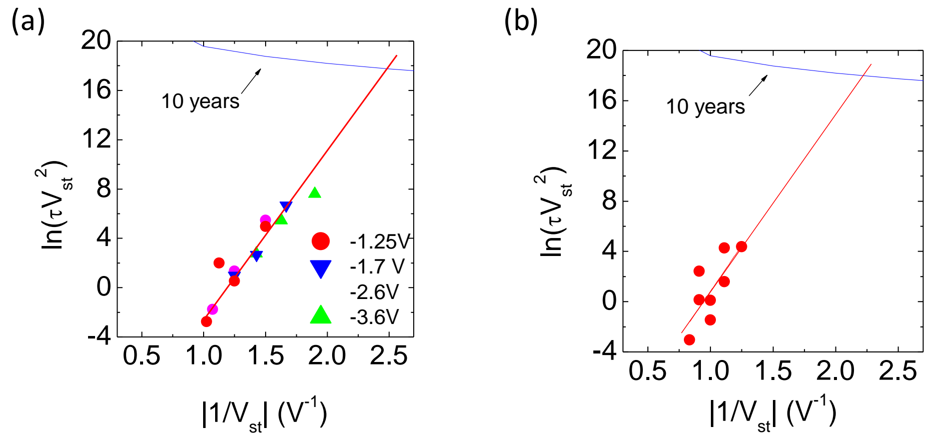

Fig. 10 FNT plot of reset transition CVS test on (a) Pt/SiO_2-Pt/SRO device, and (b) Pt/SiO_2-Pt/Mo device.

The high temperature CVS test is of interest. In a standard FNT model, which is a tunneling mechanism, the current and the time should be very insensitive to

temperature. This is because the thermal energy is only of the order of kT, which is around 0.025eV, much smaller than the tunneling barrier or the critical voltage for switching. Therefore, there is no temperature coefficient included in the model. However, both the SRO BE and Mo BE device show the retention time decreases as the temperature is elevated over 85℃, as shown in Fig. 11. The calculated effective barrier height at 85℃ shows a similar value under FNT fittings (give value: 1.4 eV for SRO BE sample and 1.1 for Mo BE sample). Only at 150℃ in the SRO BE films is there a significant decrease in the barrier height (give value: 0.87 eV). Although certain temperature dependence of FNT has been reported in several Electrically Erasable Programmable Read-Only Memories (EEPROM) and other similar Si MOS structure devices[13,14,15,16,17], the dependence should be very weak in theory. So even the rate increase at 85°C without an apparent change in the barrier height needs to be justified. (In the SiO_2-Pt case, the retention at 85°C decreases by a factor of 10). We suspect this could be due to certain structural relaxation caused by the annealing effect mentioned in Chapter 4.

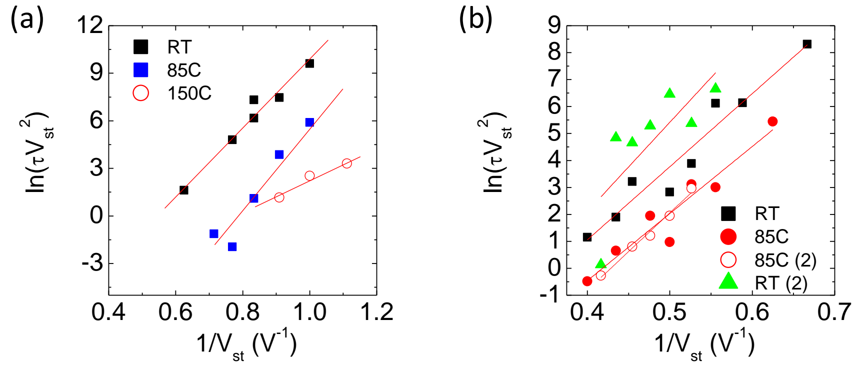

Fig. 11 FNT plot on set transition CVS test under elevated temperature of (a) Pt/SiO_2-Pt/SRO and (b) Pt/SiO_2-Pt/Mo device.

B. Negative U concept

We have shown that observations of fast switching (both set and reset) and long retention time are compatible, which is contrary to the voltage-time dilemma issue proposed by Schroeder *et al.*[5]. The rationale behind the "voltage-time dilemma" is that the same barriers need to be overcome—by direct tunneling in retention, or F-N tunneling in write/erase. On the other hand, if only retention involve a barrier, while write/erase (detrapping/trapping) does not, then the switch-on/switch-off can be facile, yet the off-state (HRS) is still highly stable. This, for example, can be realized if there are (Anderson's) negative-U centers in the material, which, when singly occupied, correspond to delocalized carrier states but, when doubly occupied, become localized states[12]. In the literature, U usually refers to the on-site Coulomb repulsion, thus it is

positive under normal circumstances. In a negative-*U* center, however, local bond distortions lower the energy so much that the net energy is now negative despite a positive Coulomb contribution. Thus, a prerequisite for such negative-*U* states is a strong electron-phonon interaction, which occurs (over a time of 10^{-13} to 10^{-12} s) shortly after electron filling (happening in ~10^{-15} s), and well within the residence time of the electron on the defect (over a time of 10^{-9} to 10^{-4} s) to lead to a sufficiently large local structural distortion[18]. The need for easy structural distortions therefore dictates that these centers tend to be situated near internal defects (e.g., vacancies) and surfaces (e.g., internal voids), as has been extensively reported in SiO_2, GaAs, amorphous chalcogenides, and other materials, including perovskites[19,20,21,22]. In this respect, mixing Pt and SiO_2 at the atomic level is expected to create many Pt/SiO_2 interfaces with dangling Si-O bonds, thus facilitating the formation of copious negative-*U* centers, to which extra electrons can be supplied by the Pt pathways. If so, *off-switching* (trapping/localization) that only requires carrier filling can be achieved by providing an electrode bias to tilt the Fermi level (to counter the bias due to the work function differences), without involving any barrier. The *on-switching* (detrapping/delocalization) will also required electric field in order to create local distortion of the bond and thus facilitates FNT to detrap the electrons. However, leakage (referring to retention) will involve thermal emission or field-assisted

tunneling past a barrier (typically of the order of 1 eV) created by the local distortions around the negative-U center. But because the voltage in retention (leakage) is low, there is probably not much distortion of the bond, thus lowering the barrier. In this way, the purely electronic RS operating in these random materials can become immune to the voltage-time dilemma, which troubles conventional charge-trapping devices.

The above discussion suggests that the CVS data represented in the FNT plot reflect field assisted tunneling without bond distortion, at least at low voltages. At high voltages approaching the set/reset voltage in fast switching, bond distortions will lower the barrier thus deviating from the FNT prediction. Some evidence for this may be seen in Fig. 9, in the the data appear to bend at the highest voltage causing a reduction of the retention time. This reduction is irrelevant to retention in practice because the read voltage is much smaller, but it is consistent with the fast write/erase speed of our device. In other words, a resolution of the voltage-time dilemma lies in the non-linear FNT plot which rapidly plunges at the switching voltage.

V. Conclusions

1. In the SiO_2-Pt device, there is no change in the switching voltage and the

resistance value attained at different switching speed, the latter varying over five orders of magnitude. This is consistent with an electronic switching mechanism.

2. Fast switching (<50 ns) and long retention (>10 years) can be obtained in the same SiO_2-Pt device despite the fact that it apparently switches by an electronic mechanism. Therefore, the device is apparently immune to the so-called "voltage-time dilemma" annunciated by Waser et al. CVS experiments provide another method to estimate the retention time, which confirm the same.
3. CVS data of set and reset transitions have been analyzed after taking into account the existence of multiple intermediate LR states and the need to discount voltage sharing between the film and the bottom electrode. They point to a barrier height of the order of 1.4 eV. It specifies a maximum "safe" read voltage of 0.4 V.
4. Temperature sensitivity at above $85^{o}C$ found in the CVS experiments is puzzling, although it could be due to structural relaxation similar to the annealing effect observed in a previous chapter.

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Chapter 9 Reliability, Statistics and the Weibull plot

I. Introduction

Signal uniformity has long been an issue for resistive switching memory (RRAM) devices. Most RRAM devices rely upon ion migration and redox-based switching mechanisms. It is commonly believed that switching in these devices involves either Joule heating (unipolar switching) or bias-driven concentration changes of oxygen vacancies (bipolar switching)[1]. These processes may induce physical damage, causing degradation and variation in properties. In TiO_2 or NiO type RRAM, it has been reported that electrodes were sometimes blown off during switching; the blown off region can span as large as a couple micro-meters[2,3]. Such regions are thought to coincide with sites of the most developed filaments, or the most active pathways for oxygen vacancy migration. The somewhat stochastic nature of filament/path/site development, both spatially and operational electric parameters, is the likely cause of the great uncertainty in switching resistance/voltage. Such uncertainty complicates the problem of noise control in these devices.

Naturally, much research has devoted to improving the switching uniformity in these devices. In filamentary-type RRAM, some improvement can be made by incorporating dopants[4,5,6,7,8,9,10] in the dielectric layer that serve as bridges to facilitate

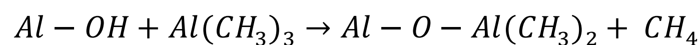
resistive switching. Examples include Mo[5] and Cr[6] doped $SrZrO_3$, Al doped HfO_2, Ti doped NiO, Pt doped TiO_2, and Mn doped ZnO. Others attempts, such as using a sub-oxide layer[11,12], a selection switch[13], or a stacking bilayer[14] have also been reported to improve the uniformity of the switching properties. However, even after intensive research on such systems, their switching reliability has not been improved to a satisfactory level.

Our SiO_2-Pt devices rely upon an entirely different switching mechanism, which is electronic in nature and has nothing to do with localized Joule heating or fast ion/oxygen diffusion paths. In this chapter, we first report the use of a thin Al_2O_3 topping layer that improves the durability and uniformity of our device. We next compare the Weibull statistics of the switching parameters of our device and filamentary-type RRAM devices. This comparison demonstrates that our device indeed has superior switching statistics than conventional RRAM devices.

II. Experimental Procedures

Devices fabricated in the same way as described in the previous chapters were used in this study with the following modification. After top electrode deposition of the SiO_2-Pt device, another "capping layer" was introduced by atomic later deposition (ALD). In this procedure, the sample was placed in an ALD chamber (Savannah 200,

Cambridge Nanotech, Cambridge, MA), in which a thin amorphous Al_2O_3 layer was deposited directly onto the device, as shown in Fig. 1, using the procedure recommended by the manufacturer. The deposition temperature was held at 150 ◦ C, and the time (during which repeated monolayer deposition steps were accomplished) was used to control the thickness. This process as illustrated in Fig. 2 uses H_2O and Tri-Methyl Aluminum (TMA) as precursors. At first, a H_2O pulse was introduced to the chamber, terminating the surface with OH^- bonds. Then, after the remaining H_2O was purged off, a TMA pulse was introduced. The TMA undergoes reaction with the surface OH^- according to the following reaction:



$$Al - OH + Al(CH_3)_3 \rightarrow Al - O - Al(CH_3)_2 + CH_4$$

the surface is then terminated with CH_3- bonds, forming an AlO layer beneath. Addition H^+ will react with CH_3-, forming CH_4 and then being pumped out. Uniform Al_2O_3 layers can thus be deposited by repeating the above procedure. A major advantage of the process is its low process temperature, avoiding chemical reaction of the mixture film with the precursors. Another advantage is the precise termination of the surface with the desired chemical group. The capping layer thickness ranges from 2~6 nm in our study.

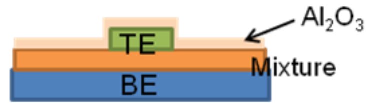


Fig.1 Schematic of capping layer on top of Pt/SiO_2-Pt device.

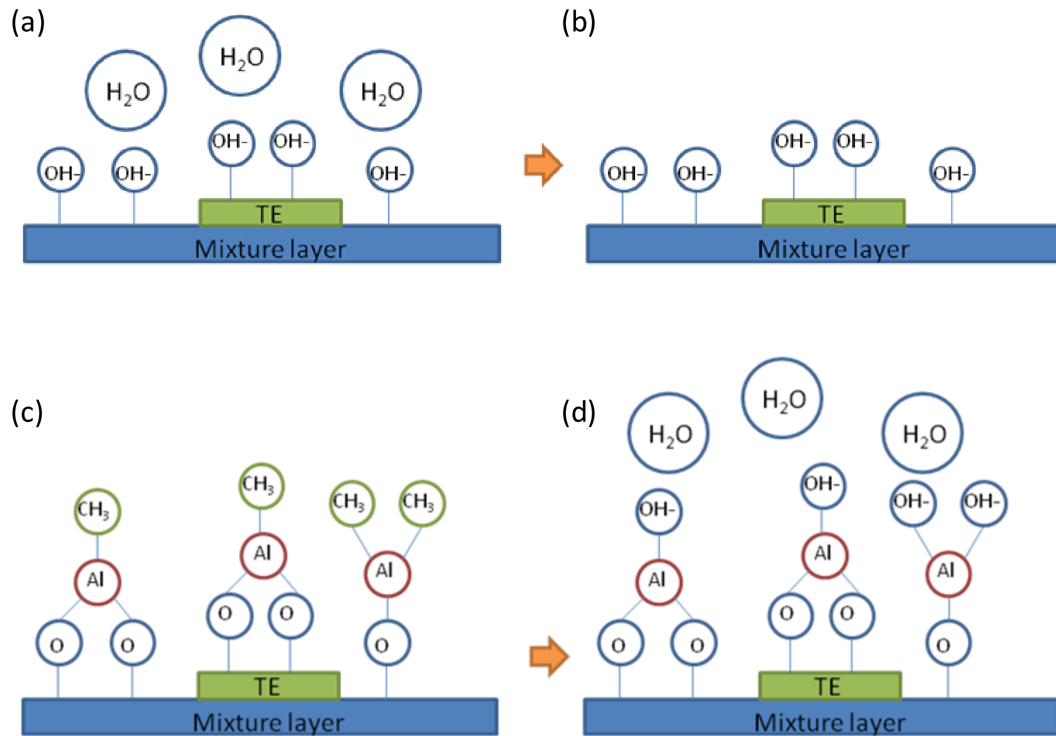


Fig. 2 ALD deposition process. (a) H_2O pulse terminating surface with OH^-, (b) purging remaining H_2O away, (c) TMA pulse terminating the surface with Al-CH_3 bondings, (d) repetition of H_2O pulse.

The capped samples were tested in the standard way for resistance switching in a probe station. The probe is used to apply an initial voltage, which serves to break the capping layer and to establish electric contact between the probe tip and the Pt top electrode. The resistance of the capped cell is initially higher than the HR state, but it can be broken by applying a voltage through the probe tip, at about ±3 V, as shown in Fig. 3. the thicker, 6 nm, capping layer is more difficult to brake, requiring 2~3

voltage stressing attempts to succeed. In addition to the “DC” switching experiments in which a voltage sweep was provided, pulse switching (“AC”) experiments were performed following the same procedure described in the preceding chapter.

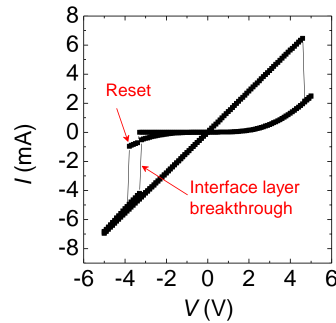


Fig. 3 Initial breakdown in capped film.

III. Results

A. The effect of capping layer

Figure 4(a) shows a series of resistance readings (0.2 V) of an uncapped Pt/SiO_2-Pt/Mo device after repeated switching using a standard “DC” voltage sweeping mode (−4 V to +5 V). The high resistance increases soon after the first cycle. This increase is evident in the I-V curve in Fig. 4(b), which also shows that the V_{set} and V_{reset} values are not constant from cycle to cycle. A longer cycling test (Fig. 5(a)) and a 300 hour retention test (Fig. 5(b)) again reveal the same trend of increasing high resistance,

even without a voltage as in the retention test.

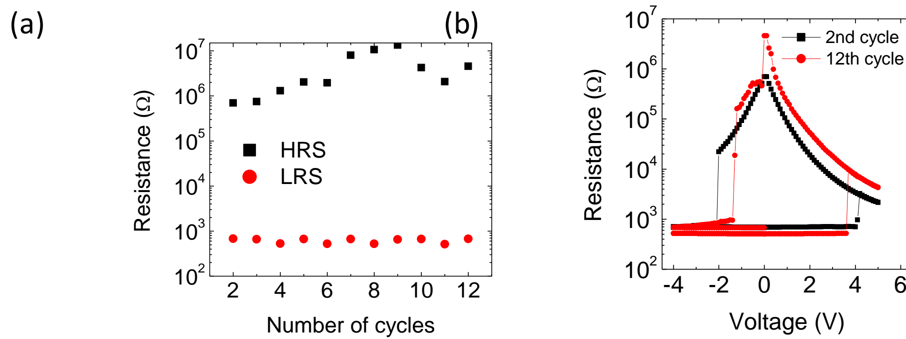


Fig. 4 (a) Increasing of HR states during DC measurements on a Pt/SiO_2-Pt/Mo device, (b) R-V curves of the 2nd cycle and 12th cycle DC sweep showing increasing HR value.

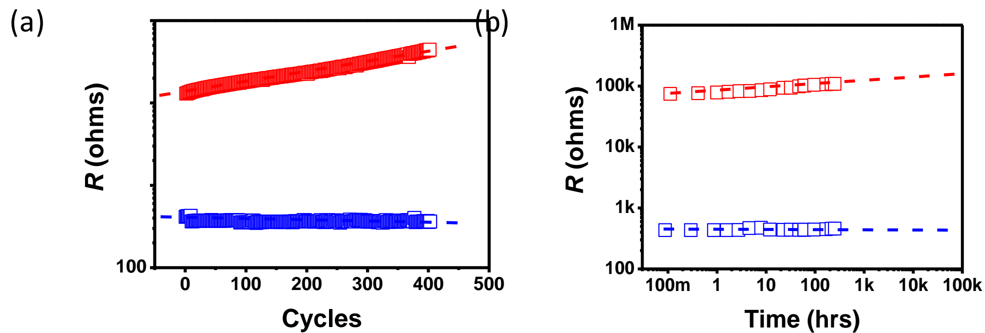


Fig. 5 (a) Cycling test, (b) retention test under room temperature.

Same experiments on a capped device yielded entirely different outcomes. Figure 6 shows the resistance of the HR and the LR state after 50 cycles of DC switching. The resistance of the HR state is almost constant (Fig. 6(a)), and the I-V curves (Fig. 6(b)) are almost identical. DC measurements after a couple days also show the same

resistance as on the first day.

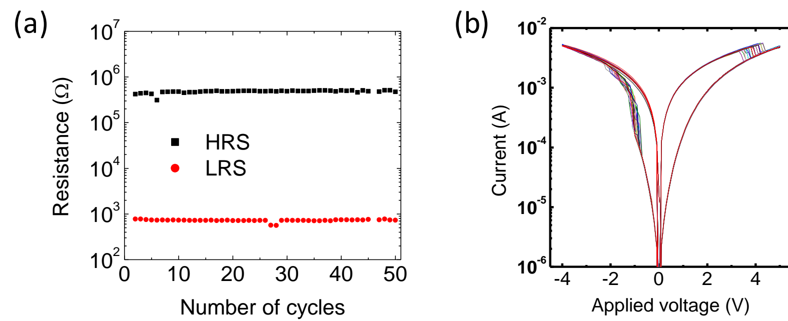


Fig. 6 (a) 50 cycles of DC measurements on a capped Pt/SiO_2-Pt/Mo device.

Moreover, in Fig. 7, the uncapped cell darkens after just 12 cycles of switching, whereas the capped cell shows no evidence of physical change after 50 cycles.

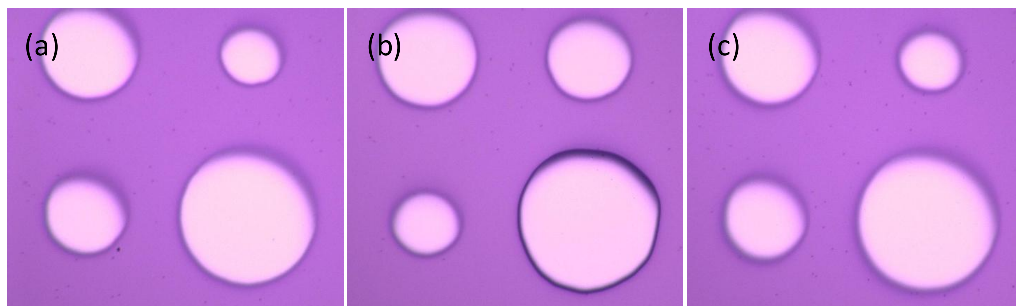


Fig. 7 (a) Fresh cells, (b) uncapped cells after 12 cycles of DC switching, (c) capped cells after 50 cycles of DC switching.

We also compared devices with different thickness of the capping layer: 2 nm, 4 nm, 6 nm. As shown in Fig. 8(a), the LR is similar in these samples, but the HR decreases as the capping layer thickness increases. This could be due to the annealing effect

(described in Chapter 4) during the capping process, given that the thicker layer was exposed to 150℃ for a longer time. Meanwhile, the set and reset voltages are almost the same for all three samples. In the endurance tests, the 2 nm samples failed after 10 cycles of DC switching (Fig. 8(a)) whereas the 4 nm (Fig. 8(b)) and 6 nm samples (Fig. 8(c)) remained stable after 25 cycles of measurements. So the 2 nm sample must be abandoned. The 6 nm capping layer, however, requires a very high breakdown voltage to penetrate, which may damage the device and is not practical. Therefore, a 4 nm capping layer appears to be the optimal choice. Further endurance tests (Fig. 9) on this sample showed that both the LR and the HR were constant after 1000 pulse cycles.

Longer cycling tests were not performed due to a technical difficulty. Because the probe is in contact with the Pt top electrode through a pin hole, electrical and mechanical vibrations make it difficult to maintain contact over a long time, thus limiting the duration of the cycling test.

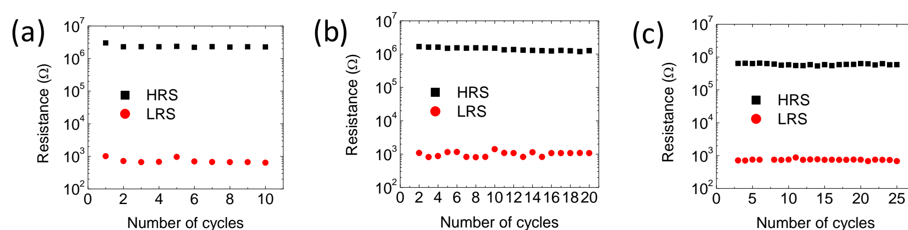


Fig. 8 Cycling tests of Pt/SiO_2-Pt/Mo device with a (a) 2 nm, (b) 4 nm, and (c) 6 nm capping layer.

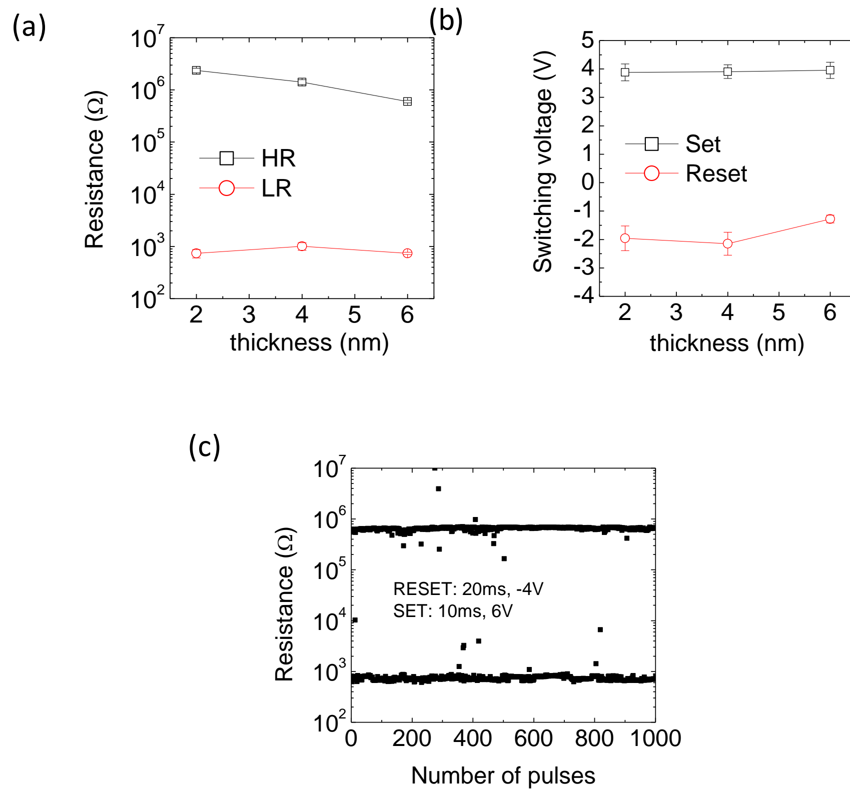


Fig. 9 Initial (a) HR/LR values, and (b) V_{set}/V_{reset} values with different capping layer thickness; (c) HR/LR values after 1000 switching cycles (100 ns pulse) on a 4 nm Al_2O_3 capped Pt/SiO_2-Pt/Mo device.

In addition, the retention property of the Pt/SiO_2-Pt/Mo device was highly improved. In Fig. 10, the HRS shows almost no change after 10^5 seconds.

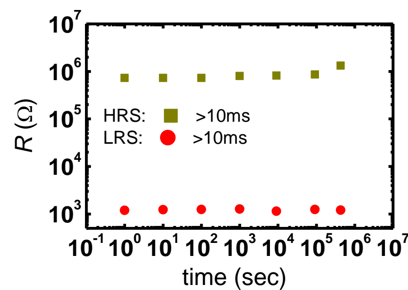


Fig. 10 Retention test of a capped Pt/SiO_2-Pt/Mo device.

B. Uniformity and statistics

We have demonstrated that the electronic resistance switching device has an excellent uniformity after Al_2O_3 capping. In the following section, we compare it to that of filamentary-type RRAM, which are prominently featured among RRAM. Both V_{set} and V_{reset} transitions in filamentary-type resistance switching are highly variable from run to run, even for the same cell. In our device, this is not the case.

In Fig. 6, we show 50 consecutive DC I-V curves. The I-V curves of these consecutive runs are almost identical. Both R_{HR} (43.8 ± 1.02 kΩ) and R_{LR} (810.8 ± 6.93 Ω) have low ratios of standard deviation (Δ) over mean (μ), at 0.0233 and 0.00855, respectively. This reproducibility is also manifest in the pulse switching mode (pulse width = 100 ns), as depicted in Fig. 9(c), showing very little fluctuation over 1000 switching cycles. The statistical distributions of the HRS and LRS shown in Fig. 11(a) and 11(b) are almost vertical, especially in the DC mode, indicating very little spread in uniformity.

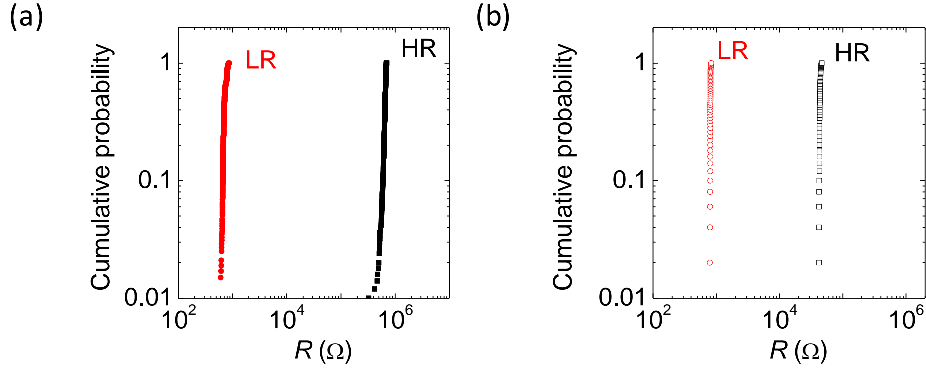


Fig. 11 Cumulative probability of Pt/SiO_2-0.25Pt/Mo device in (a) pulse switching mode (100ns pulse width), and (b) DC switching mode.

We investigate the variability of the switching voltages in two ways: studying (1) repeated switching from cycle to cycle in a single cell; and (2) variability from cell to cell. The results are quantified in two metrics. One is the Δ/μ value, which is mentioned in the previous paragraph. The other is the Weibull modulus. Here we introduce the Weibull distribution that is expressed as:

$$F(x) = 1 - exp(-(x/x_0)^k) \qquad \text{Eq. 9-1}$$

where F is the cumulative probability of finding the random variable (a switching parameter such as R_{HRS} or V_{off}) below x, x_0 being a scaling constant, and k is the Weibull exponent (modulus) for which a higher value corresponds to a narrower distribution. We then plot each statistical distribution into a Weibull plot, using

$$\mathrm{Ln}(-\mathrm{Ln}(1-F(x))) = k(\mathrm{Ln}x - \mathrm{Ln}x_0) \qquad \text{Eq. 9-2}$$

The fitted slope in this plot is the Weibull modulus k. This procedure of plotting

cumulative probability and its Weibul representation is demonstrated in Fig. 12 for the cumulative HR and LR from 10 cells. A more detailed comparison is given in Fig. 12 (a) - (f) which shows the single cell HRS/LRS, cell-to-cell HRS/LRS, same cell V_{set}, and different cell V_{set}, respectively. Meanwhile, the values of k and Δ/μ are summarized in Table 1. The k value for switching in a single cell is as high as 145 for LR and 50 for HR, and it is still above 10 when the statistics are pooled over 10 different cells in the same sample. The k value for the set voltage is also very high, typically greater than 17.

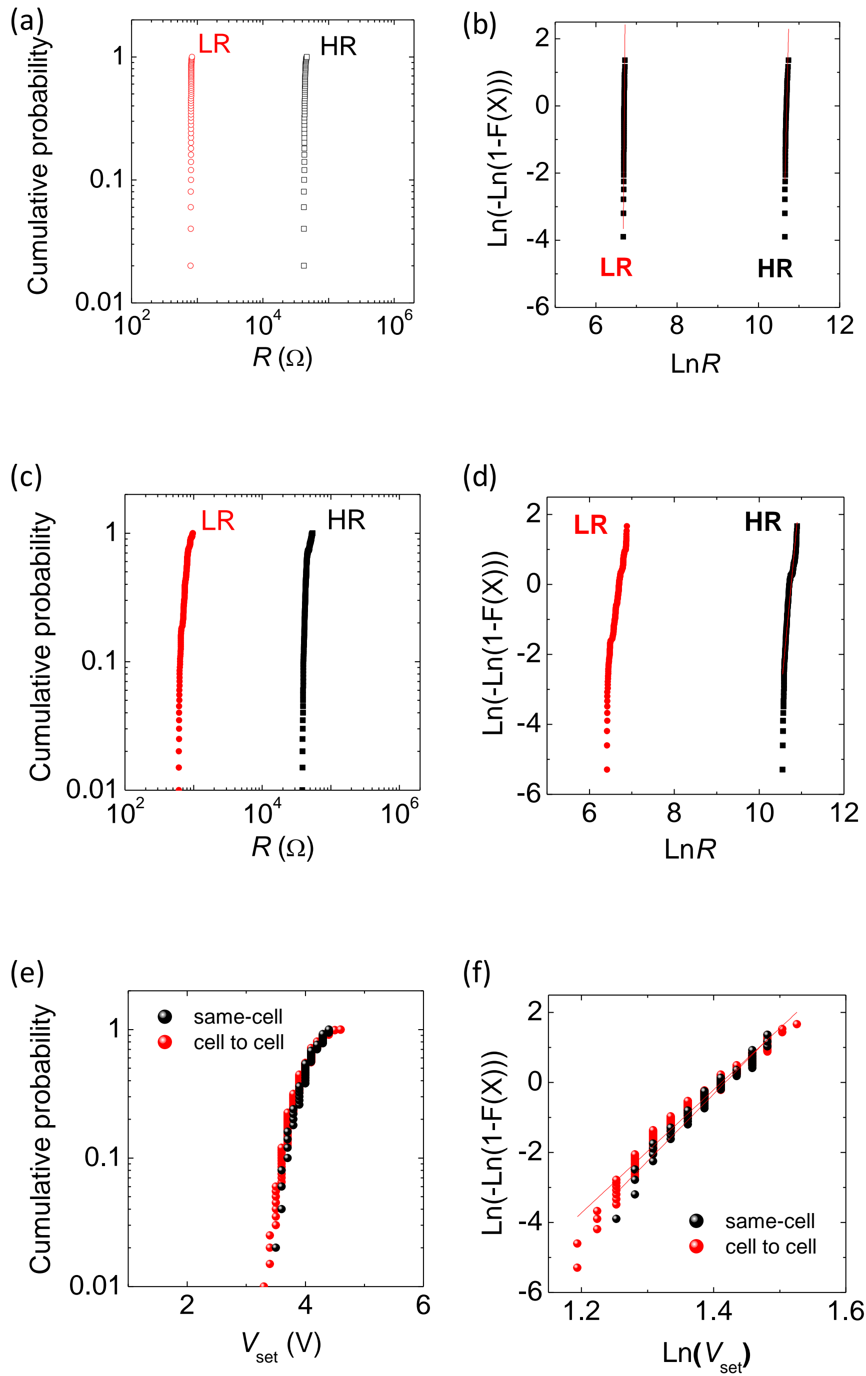


Fig. 12 Cumulative probability and Welbull plot of (a) (b) single cell HR and LR, (c) (d) HR and LR over 10 cells (each cells was measured 20 cycles); (e) (f)V_{set} statistics of same cell and 10 cells.

C. Comparison with other RRAM devices

We next compare our statistics with those of other RRAM reported in the literature using the above two metrics, k and Δ/μ. The switching statistics are classified according to the material and the proposed switching mechanism, which are listed in Table 2. The (binary oxide, filamentary switching mechanism) category represents the most common RRAM system. However, the statistics of both pure TiO_2[10,15] and NiO[13,16] in this category are poor, having a Weibull modulus k below 5. Some researchers have found the way to improve the uniformity of filamentary type RRAM is by incorporating minor dopants in the dielectric layer[7,9,10,11,13]. Their statistics are slightly improved but still not good.

Compared to filamentary-type RRAM devices, the interface redox and Schottky barrier type RRAM have shown better uniformity in the switching behavior. In ZrO_2[17], the k value was significantly raised when TiN was used as the top electrode; this is explained by TiN acting as an oxygen reservoir, which aids the interface between TiN/ZrO_2. In the Schottky barrier type RRAM, the switching uniformity was improved by adding Cr, Mo, or V dopants that serve as trap sites at the interface. The Weibull modulus k is above 10 and reaches 20 in some cases. In PCMO[18,19] devices, the switching uniformity can be enhanced by electrode engineering; however, only HRS or LRS was improved, not both. (They are improved one at a time, with the

other left unimproved.) Recently, Seagate [20] reported a highly-uniform resistance switching PCMO with a very small cell size. Yet, its Δ/μ is only around 0.3 when measured from cell to cell, which is still higher than that of the SiO_2-Pt device. (This PCMO's Δ/μ can be further decreased to 0.2 when the cell dimension is shrunk to 100 nm×100 nm.) The comparison indicates that our electronic switching RRAM is correlated with a better uniformity than filamentary-type switching RRAM, and that bipolar switching RRAM is much better than unipolar switching RRAM.

In summary, it is clear that the Δ/μ in Table 2 are much larger, and all the *k* much smaller, than those in Table 1. Therefore, compared to those devices reported in the literature, our device has a much smaller variability. This indicates that the SiO_2-Pt films are relatively uniform from cell to cell. Nevertheless, there is probably still room for improvement, which hopefully can raise the *k* value for cell-to-cell variation from 10 to 50, which is the same-cell cycle variability that is likely to be the limit.

D. The k vs Δ/μ graph

We have found one excellent way to represent the device statistics by plotting k and Δ/μ together. This is based on the observation that in Weibull statistics, the two parameters are analytically related by

$$\sigma = \lambda[\Gamma(1+2/k) - \Gamma^2(1+1/k)]^{1/2} \qquad \text{Eq. 9.3}$$

$$\mu = \lambda\Gamma(1+1/k) \qquad \text{Eq. 9-4}$$

$$\Delta/\mu = \frac{[\Gamma(1+2/k) - \Gamma^2(1+1/k)]^{1/2}}{\Gamma(1+1/k)} \qquad \text{Eq. 9-5}$$

In the above, Γ is the Gamma function. The k versus Δ/μ plot is a smooth curve shown in Fig. 13. This curve is validated by the data, including our R_{HRS} (both AC and DC), DC V_{set} and V_{reset} and the literature data of R_{HRS} and switching voltage (V_{set}) of a variety of RRAM. The SiO_2-Pt device properties are concentrated at the top left quadrant of the graph, which has the highest k and the lowest Δ/μ values, indicating excellent uniformity of the resistive switching properties.

The utility of this plot becomes obvious in cases when the reported data show either k, or Δ/μ, but not both. (If the cumulative statistics are shown, then they can be reanalyzed to obtain both parameters, but this is often not the case as the authors choose to report either k or Δ/μ only). Since the two metrics are related to each other, it is then possible to use the above plot to compare the data across k and Δ/μ.

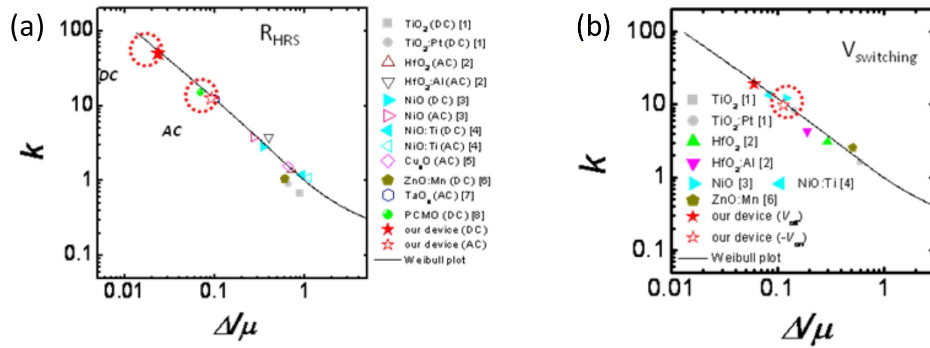


Fig. 13 k versus Δ/μ plot of (a) HR value and (b) switching V comparing our device to others reported in the literature.

Table 1. Pt/SiO_2-Pt/Mo Device Statistics.

	Property	k	Δ/μ	Figure
Same-cell	HR	50	0.0233	Fig.12(a)(b)
	LR	145	0.0086	
	V_{set}	19.2	0.0602	Fig.12(e)(f)
Cell-to-cell	HR	12.8	0.0918	Fig.12(c)(d)
	LR	9.5	0.125	
	V_{set}	17.6	0.0689	Fig.12(e)(f)
Cell-to-cell (Various area)	V_{set}	33	0.0304	

Table 2. Other devices – Part 1 HR and LR.

(Colors in red represents high statistics device with k value > 10)

The first type of materials ($SrTiO_3$ to TiO_2) are filamentary type RRAM, which are the most common seen RRAM materials. The second type is (TiO_2, Pt:TiO_2 to Mn:ZnO) improvements done to enhance switching stability (such as incorporating dopants) in filamentary type RRAM. The third type (Mo:SZO to ZrO_2) are the materials that proposed electronic switching mechanisms. Lastly, PCMO, which the mechanism is still under debate, were listed at the end of the table.

Material	Property	k	Δ/μ
($SrTiO_3$) [21] Same cell	HR	14.51	0.074
	LR	9.744	0.097
(NiO) [16] Same-cell	HR	5.518	0.276
	LR	2.4	0.42
(CuO)[22] Same cell	HR	2.24	0.643
	LR	3.53	0.319
(TiO_2)[15] Same cell	HR	5.494	0.21
	LR	15.31	0.082
(TiO2, Pt:TiO_2)[10] same-cell	HR	0.68, 0.91	0.882, 0.656
	LR	5.5, 11	0.225, 0.107

(HfO_2, Al:HfO_2)[7] cell-to-cell	HR	1.4, 3.8	0.707, 0.397
	LR	1.5, 15.5	0.762, 0.104
(NiO w/ diode)[13] same-cell	HR	2.85	0.347
	LR	1.65	0.488
(Cu_xO)[11] cell-to-cell	HR	1.56	0.647
(Mn:ZnO)[9] Same-cell	HR	1.06	0.597
	LR	1.81	0.554
(Mo:SZO)[5] Same cell	HR	2.641	0.353
	LR	4.871	0.215
($SrZrO_3$)[6]	HR	0.75	1.52
	LR	8.247	0.358
(Cr:SZO)[6] same-cell	HR	3.734	0.309
	LR	13.394	0.072
(ZrO_2)[17] same cell	HR	22.29	0.049
	LR	19.81	0.089
(PCMO)[18] Same cell	HR	3.307	0.299
	LR	14.454	0.106
(PCMO) same-cell[19]	HR	11.6	0.132
	LR	1.861	0.625

(PCMO)[20] cell to cell	HR	-	0.219

Table 3. Other devices – Part 2 Switching voltage.

Material	Property	k	Δ/μ
(TiO_2, Pt:TiO_2)[10] same-cell	V_{set}	1.6, 8.11	0.609, 0.146
(HfO_2, Al:HfO_2)[7] cell-to-cell	V_{set}	-	0.294, 0.192
(NiO w/ diode)[13] same-cell	V_{set}	12.2	0.121
(Mn:ZnO)[9] Same-cell	V_{set}	2.57	0.512
(SZO)[6]	V_{on}	4.38	0.265
	V_{off}	7.2	0.265
(Cr:SZO)[6]	V_{set}	38.07	0.024
	V_{off}	9.96	0.152

IV. Discussion

The beneficial effect of the capping layer strongly suggests an environmental effect that is responsible for device degradation. In our experience, the R_{HRS} increase over time was only observed in samples with a Mo bottom electrode, not in samples with a $SrRuO_3$ bottom electrode. This suggests that the increase is due to the slow oxidation of Mo over time, which does not occur to $SrRuO_3$. The resistance increase is more severe for R_{HRS} than for R_{LRS}, which can be explained by electron trapping in the HR state, which renders the film negatively charged, hence the bottom electrode positively charged. Such a bias will promote (a) O^{2-} and/or OH^- migration from the film toward the Mo electrode and (b) Mo-cation outdiffusion toward the electrode/film interface, thus more oxidation.

It is interesting to note that the "environmental effect" referred to above seems to operate mostly when the device is electrically tested or stressed. Although a long exposure to atmosphere can cause a slight increase in the resistance in the case of Mo bottom electrode, the effect is much more severe if an electric field is applied or if charge is trapped. We have attempted wet processing (involving exposure to several solutions and many steps of cleaning and drying) to deposit colloidal particles onto our samples. After that the cells are still switchable. Likewise, lithography involves many wet processing steps and reactive etching, which do not render the device

unswitchable either.

On the other hand, the procedure of forming a capping layer involves exposure to high temperatures, which seems to incur an annealing effect that lowers the HR. From our annealing study described in a previous chapter, the overall effect of annealing is not beneficial, and it will probably reduce the uniformity of the switching parameters of our device. Therefore, optimizing the ALD process could prove to be a way to further improve the uniformity of our devices.

Lastly, although it is tempting to suggest that electronic switching mechanism is responsible for the uniformity of the corresponding switching parameters, we should mention another possibility that may also be influential. As described in a previous chapter on multiple state switching, our device has a self-regulating property allowing the LR to be tuned by loading under a negative bias. This has the effect of normalizing the set voltage to one that is closely correlated to the maximum voltage used in the negative bias. This feature could have a decisive effect on the property uniformity, at least for the switching voltage. Meanwhile, in the same chapter mentioned above, we found the set transition in our device always ends at the same HR state, which is caused by an "unloading" effect for voltage redistributing from the bottom electrode to the film. This could have a beneficial effect on the uniformity of the HR. Lastly, since the LR in our device is often dominated by the resistance of the

bottom electrode, this characteristic again leads to the uniformity of LR. Therefore, it seems likely that the excellent uniformity of our switching properties may have as much to do with our device's "equivalent circuit" as with its electronic switching nature.

V. Conclusions

1. An Al_2O_3 capping layer has a decidedly beneficial effect on the uniformity and the durability of our device.
2. Compared with other RRAM devices in the literature, our capped device has superior uniformity, featuring much higher Weibull k values and much smaller Δ/μ values, which are analytically correlated to each other.
3. A review of the literature using the above two metrics strongly suggests that (a) electronic switching RRAM is correlated with a better uniformity than filamentary-type switching RRAM, and (b) bipolar switching RRAM is much better than unipolar switching RRAM.
4. Cell to cell statistics of our devices may be further improved by optimizing the ALD process, which hopefully can raise the *k* value for cell-to-cell variation from 10 to 50, same as the same-cell cycle variability.

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