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We present a simple silicon circuit for modeling voltage-dependent ion channels found within neural cells, capturing both the gating particle's sigmoidal activation (or inactivation) and the bell-shaped time constant. In its simplest form, our ion-channel analog consists of two MOS transistors and a unity-gain inverter. We present equations describing its nonlinear dynamics and measurements from a chip fabricated in a 0.25 μm CMOS process. The channel analog's simplicity allows tens of thousands to be built on a single chip, facilitating the implementation of biologically realistic models of neural computation.

Comments

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Neuronal Ion-Channel Dynamics in Silicon

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Abstract—We present a simple silicon circuit for modelling voltage-dependent ion channels found within neural cells, capturing both the gating particle’s sigmoidal activation (or inactivation) and the bell-shaped time constant. In its simplest form, our ion-channel analog consists of two MOS transistors and a unity-gain inverter. We present equations describing its nonlinear dynamics and measurements from a chip fabricated in a $0.25\mu\text{m}$ CMOS process. The channel analog’s simplicity allows tens of thousands to be built on a single chip, facilitating the implementation of biologically realistic models of neural computation.

I. ION CHANNELS

The brain is one of the most powerful computing machines today, capable of outperforming modern machines in many computational tasks. As such, the field of neuromorphic engineering seeks to emulate the brain by using the transistor’s physical properties to create silicon analogs of neural circuits. Silicon is an attractive medium because a single chip has thousands of (heterogeneous) silicon neurons that operate in real-time.

One of the key computational components within the brain is the voltage-gated ion channel. Ion channels are pores within the membrane of neurons, gating the flow of ions between the intracellular and extracellular media. The gating dynamics are membrane-voltage-dependent, and once open, the ionic currents can greatly influence the output of the cell, either facilitating or hindering the generation of an action potential.

To date, neuromorphic models have not captured the voltage dependence of the ion channel’s temporal dynamics. Since neuromorphic circuits are constrained by surface area on the silicon die, larger, more complicated, circuits translate to fewer silicon neurons on a single chip. Thus, previous models of voltage-dependent ion channels [1], [2] have sacrificed the voltage dependence of the time constant, opting to fix it to reduce the circuit size.

In certain areas of the brain, however, this voltage dependence is critical. One example is the low-threshold calcium channel in the relay neurons of the thalamus: The time constant for inactivation can vary over an order of magnitude depending on the membrane voltage. This variation defines the relative lengths of the interburst interval (long) and the burst duration (short) when the cell bursts rhythmically.

In this paper, we present a compact circuit that models the nonlinear dynamics of the ion channel’s gating particles. Our circuit is based on linear thermodynamic models of ion channels [3], which apply thermodynamic considerations to the gating particle’s movement. Similar considerations of the transistor makes clear that both the ion channel and the transistor operate under similar principles. This insight allows us to implement the voltage-dependence of the ion channel’s temporal dynamics, while at the same time using fewer transistors than previous neuromorphic models that do not possess these nonlinear dynamics. With a more compact design, we can incorporate a larger number of silicon neurons on a chip without sacrificing biological realism.

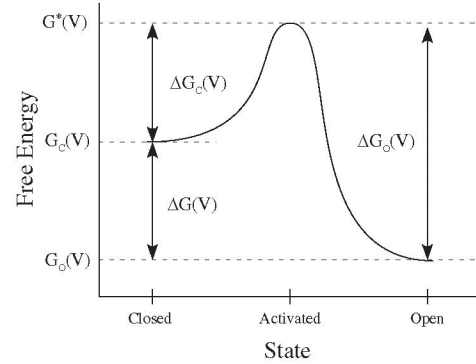


Fig. 1. Transition rates between two states depend on the height of the free energy barriers (ΔG_C and ΔG_O), which involve the difference in free energy between the activated state (G^*) and the initial state (G_C or G_O).

II. TRANSISTORS AND ION CHANNELS

Thermodynamic models of ion channels are an extension of Hodgkin and Huxley’s model of the ion channel, introducing structure by employing thermodynamic principles rather than being empirical. Both channel models consist of a series of independent gating particles, whose binary state—open or closed—determines the channel permeability. A *Hodgkin-Huxley (HH) variable* represents the probability of a particle being in the open state, or, with respect to the channel population, the fraction of open gating particles. The kinetics of the variable are simply described by

$$(1 - u) \xrightleftharpoons[\beta(V)]{\alpha(V)} u, \quad (1)$$

where $\alpha(V)$ and $\beta(V)$ define the voltage-dependent transition rates between the states (indicated by the arrow), u is the HH variable, and $(1 - u)$ represents the closed fraction. As such, the dynamics of u are described by the differential equation

$$\frac{du}{dt} = \alpha(V) (1 - u) - \beta(V) u, \quad (2)$$

or, in its more common form:

$$\frac{du}{dt} = -\frac{1}{\tau_u(V)} (u - u_\infty(V)), \quad (3)$$

where $u_\infty(V)$ and $\tau_u(V)$ represent the steady-state and time constant for u , respectively. Neuroscientists use this latter form more often as u_∞ and τ_u are easier to determine empirically. In addition, the dynamics of the variable are more intuitive in this form.

A HH variable is classified as either activation or inactivation. Activation variables increase when the cell’s membrane voltage is

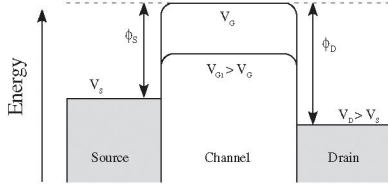


Fig. 2. The vertical dimension represents the energy of electrons within an NMOS transistor, while the horizontal dimension represents location within the transistor. ϕ_S and ϕ_D are the energy barriers faced by electrons attempting to enter the channel from the source and drain, respectively. V_D , V_S , and V_G are the terminal voltages, designated by their subscripts. During transistor operation, $V_D > V_S$, and thus $\phi_S < \phi_D$. V_{G1} represents another scenario with a higher gate voltage. Adapted from [8].

depolarized (excited), and decrease when the cell is hyperpolarized (inhibited). With respect to transition rates, as the cell depolarizes, $\alpha(V) > \beta(V)$, while when the cell hyperpolarizes, $\beta(V) > \alpha(V)$. The converse is true for inactivation variables: when the cell depolarizes, the variable decreases, and so $\beta(V) > \alpha(V)$; when the cell hyperpolarizes, $\alpha(V) > \beta(V)$ and the variable increases. In either situation, $\alpha(V)$ and $\beta(V)$ are both monotonic functions of voltage, but opposite in slope.

In thermodynamic models, state changes of a gating particle are related to changes in the conformation of the ion channel protein [4], [3], [5]. Each state possesses a free energy dependent on the interactions of the protein molecule within the electric field of the membrane. State transitions occur when the molecule overcomes an energy barrier (ΔG_C and ΔG_O in Fig. 1), the size of which defines the transition rate [6]:

$$\alpha(V) \propto e^{-\Delta G_C(V)/RT} \quad (4)$$

$$\beta(V) \propto e^{-\Delta G_O(V)/RT}, \quad (5)$$

where $\Delta G_C(V)$ and $\Delta G_O(V)$ are the voltage-dependent free energy barriers, R is the gas constant and T is the temperature in Kelvin. Linear thermodynamic models assume that linear interactions of the protein molecule—such as is produced by the movement of a monopole or dipole through an electric field [4], [7]—dominate, and so the energy barrier depends linearly on the membrane voltage. This reduces the above equations to simple exponentials of the membrane voltage.

MOS transistors operate under similar thermodynamic principles as linear thermodynamic models. In the subthreshold regime, charge flows across the channel by diffusion from the higher density at the source end to the lower density at the drain end. The density of charge carriers at the either end depends exponentially on the size of the energy barrier there (Fig. 2). These energy barriers exist due to a potential difference between the channel and the source or the drain. For the NMOS transistor's negatively charged electrons, increasing the source voltage decreases their energy level, increasing the barrier height. As a result, fewer electrons have the energy required to overcome the barrier, reducing the density in the channel. The gate voltage, which influences the potential at the surface of the channel, has the opposite effect: increasing it (e.g., from V_C to V_{G1} in Fig. 2) *decreases* the barrier height, but at both ends of the channel.

As such, the NMOS transistor's channel current has an exponential

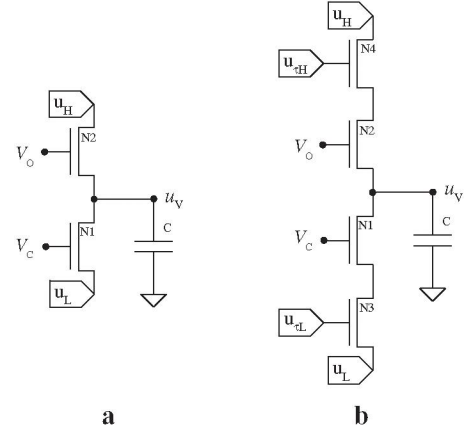


Fig. 3. **a**, The voltage u_V represents the logarithm of the HH variable u . V_O and V_C are linearly related to the membrane voltage, with slopes of opposite sign. u_H and u_L are adjustable bias voltages. **b**, Two transistors (N3 and N4) are added to saturate the variable's opening and closing rates; the bias voltages $u_{\tau H}$ and $u_{\tau L}$ set the saturation level.

relationship with its terminal voltages [8]:

$$I_{ds} = I_{ds0} \left(e^{\frac{\kappa V_{GB} - V_{SB}}{U_T}} - e^{\frac{\kappa V_{GB} - V_{DB}}{U_T}} \right), \quad (6)$$

where κ describes the relationship between the gate voltage and the potential at the channel surface. U_T is called the thermal voltage¹ (25.4mV at room temperature) and I_{ds0} is the baseline diffusion current, defined by the barrier introduced when the oppositely doped regions (p-type and n-type) were fabricated. When V_{DB} exceeds V_{SB} by $4U_T$ or more, the drain term becomes negligible and is ignored; the transistor is then said to be in *saturation*.

The similarities in the underlying physics of ion channels and transistors allow us to use transistors as thermodynamic isomorphs of ion channels. Thus, the current within the transistor becomes analogous to the transition rate within the gating particle population. Despite these similarities, however, the analogy is not complete, as we cannot model the channel population with a single transistor. The problem arises in trying to independently adjust the opening and closing transitions, while at the same time integrating the current to update the open fraction. While the source and drain provide independent means to adjust the energy barriers, this is not possible as one or the other voltage must change to accommodate integration (on a capacitor). And the gate, unfortunately, influences the size of both barriers equally. Thus, we require additional transistors, as discussed in the next section.

III. CIRCUIT DESCRIPTION

We use a voltage, u_V , to represent the logarithm of the HH variable u (Fig. 3a). Assuming transistor N1 remains in saturation, the dynamics of the circuit are described by the differential equation

$$\frac{du}{dt} = \frac{I_O}{Q_u} (1 - u) - \frac{I_C}{Q_u} u, \quad (7)$$

where $u = e^{u_V - u_H}$, $Q_u = C U_T$, representing the amount of charge required to e -fold u , $I_O = I_{ds0} e^{\kappa V_O - u_H}$ and $I_C = I_{ds0} e^{\kappa V_C - u_L}$. u_H and u_L are adjustable voltage biases, set outside the chip. In

¹For clarity, U_T will not appear in the remaining transistor current equations as all transistor voltages from hereon are given in units of U_T .

the figures, all such external biases (e.g., u_H and u_L in Fig. 3a) are enclosed within pointed boxes.

Comparing Equation 7 to Equation 2, we see I_O and I_C represent the channel transition rates: $\alpha(V) = I_O/Q_u$ and $\beta(V) = I_C/Q_u$. For these rates to change exponentially with V (the membrane voltage), V_O and V_C must both be linear functions of V . Note that, to remove the influence of the drain of transistor N1, we must ensure $u_V > u_L + 4U_T$.

The signs of V_O 's and V_C 's linear dependence on V determines whether the circuit represents an activation or inactivation variable. As discussed above, activation variables open with cell depolarization; this requires V_O to increase, and V_C to decrease, with V . Inactivation variables, which open with cell hyperpolarization, require V_C to increase and V_O to decrease with V . Thus, modelling activation or inactivation reduces to defining the sign of the slope of V_O and V_C with respect to V .

One flaw with linear thermodynamic models, and consequently with our circuit, is that the time constant decreases to extremely small values when either $\alpha(V)$ and $\beta(V)$ become large. One solution involves saturating the transition rates [9]. We realize this in our circuit by placing two additional transistors in series with the original two (Fig. 3b). Thus, when $V_O > u_{\tau H} + 4U_T$, $\alpha(V) \propto e^{\kappa u_{\tau H}}$, fixing the transition rate since $u_{\tau H}$ is a fixed bias. $u_{\tau L}$ functions similarly with V_C to saturate the closing transition rate.

We analyze the channel analog by deriving expressions for $u_\infty(V)$ and $\tau_u(V)$ for the circuit in Fig. 3b. We assume the opening and closing voltages' have the following form:

$$V_O = \phi_o + \gamma_o V \quad (8)$$

$$V_C = \phi_c - \gamma_c V \quad (9)$$

where the offsets ϕ_o and ϕ_c and the slopes γ_o and γ_c —all positive constants—are defined through additional circuitry. Since V_O has a positive slope with respect to V , the following derivation applies to an activation variable; a similar approach also applies for inactivation variables, with the signs of the slopes in Equations 8 and 9 reversed.

Under certain restrictions [10], u 's steady-state and time-constant equations possess the following form:

$$u_\infty(V) = \frac{1}{1 + \exp\left[-\frac{V-V_s}{V_s^*}\right]}, \quad (10)$$

$$\tau_u(V) = \tau_{\min} \left(1 + \frac{1}{\exp\left(\frac{V-V_1}{V_1^*}\right) + \exp\left(-\frac{V-V_2}{V_2^*}\right)} \right) \quad (11)$$

where

$$\begin{aligned} V_s &= (\phi_c - \phi_o + (u_H - u_L)/\kappa) / (\gamma_o + \gamma_c) \\ V_s^* &= (U_T/\kappa) / (\gamma_o + \gamma_c) \\ V_1 &= (u_{\tau H} - \phi_o) / \gamma_o \\ V_1^* &= U_T / (\kappa \gamma_o) \\ V_2 &= (\phi_c - u_{\tau H} + (u_H - u_L)/\kappa) / \gamma_c \\ V_2^* &= U_T / (\kappa \gamma_c) \\ \tau_{\min} &= (Q_u/I_{ds0}) e^{-(\kappa u_{\tau H} - u_H)} \end{aligned}$$

As is common for HH variables [6], the steady-state curve is sigmoidal and the time constant curve is bell-shaped. We assume the opening and closing rates saturate at the same level (i.e., $\kappa u_{\tau H} -$

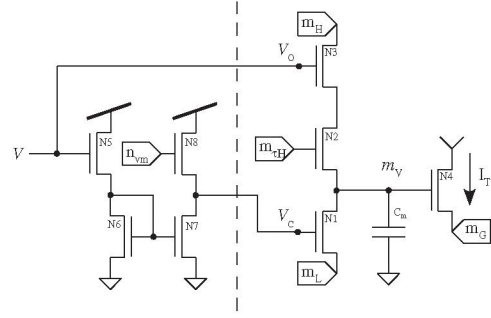


Fig. 4. A voltage inverter (N5-8) produces the closing voltage (V_C); The opening voltage (V_O) is identical to the membrane voltage (V). A channel variable circuit (N1-3) implements the variable's dynamics in the log-domain (m_V); the voltage biases m_H , m_L , and $m_{\tau H}$ are analogous to u_H , u_L , and $u_{\tau H}$. An antilog transistor (N4) produces a current (I_T) proportional to the variable.

$u_H = \kappa u_{\tau L} - u_L$). This equates the minimum time constant at hyperpolarized and depolarized levels, simplifying the expression to Equation 11. In addition, the bell-shape also requires τ_{\min} to be smaller than the peak time constant in the absence of saturation. The free parameters in these equations provide the flexibility not only to shift the curves, but also to adjust their slopes.

IV. CIRCUIT RESULTS

We fabricated a simple activation channel (Fig. 4) in a $0.25\mu\text{m}$ CMOS process. Transistors N1-3 implement the dynamics described in the previous section, except without a saturation transistor for the closing transition rate. The additional transistor (N4), which takes the anti-log of m_V , represents the collective action of open channels within the membrane; the current this transistor produces (I_T) can represent either the channel current [11] or channel conductance [2]. For this paper, the choice is irrelevant.

For the opening voltage (V_O), we connected it directly to the membrane voltage (V), yielding slope $\gamma_o = 1$ and intercept $\phi_o = 0$. Transistors N5-8 invert the membrane voltage for the closing voltage (V_C). In this case, the closing voltage's intercept $\phi_c = \kappa n_{vm}$ (set by a bias voltage n_{vm}) and its slope $\gamma_c = \kappa^2/(\kappa + 1)$.

For the opening voltage (V_O), we connected it directly to the membrane voltage (V), yielding slope $\gamma_o = 1$ and intercept $\phi_o = 0$. For the closing voltage, we used a four-transistor inverter (N5-8) instead of the standard unity-gain inverter (two transistors), as we wanted to capture the asymmetry displayed by the T-type calcium channel in relay cells, which this circuit was designed to model [12]. In this case, the intercept $\phi_c = \kappa n_{vm}$ (set by a bias voltage n_{vm}) and the slope $\gamma_c = \kappa^2/(\kappa + 1)$.

This eight-transistor design captures the ion channel's nonlinear dynamics, which we demonstrated through voltage clamp experiments (Fig. 5a). As the step size increases (starting from the same initial level), I_T 's time course and final amplitude both change, as expected. The relationship between I_T and the activation variable, defined as $m = e^{m_V - m_H}$, has the form

$$I_T = m^\kappa \bar{I}_T \quad (12)$$

Its maximum value $\bar{I}_T = e^{\kappa m_H - m_C}$, and its exponent $\kappa \approx 0.7$. Higher exponents are possible, but require a lot more transistors.

Through the relationship above, we extract the dynamics of m from I_T (Figure 5b,c). The solid lines are the fits of Equations 10 and 11, which reasonably capture the open fraction's steady-state level and time-constant. The time-constant data's range is limited because

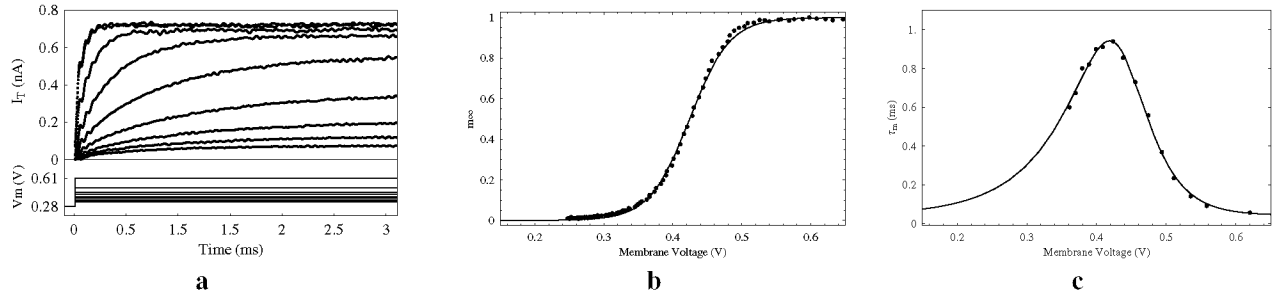


Fig. 5. **a**, Channel response during voltage clamp experiments. As the membrane-voltage step increases, the steady-state amplitude likewise increases, while the time-constant initially rises but then falls. **b**, Dependence of activation on membrane voltage in steady state, captured by sweeping the membrane voltage slowly and recording the normalized current output. **c**, Dependence of time constant on membrane voltage, extracted from the curves in Fig. 5a by fitting exponentials. Fits in **a** and **b** (solid lines) are of Equations 10 and 11: $V_s = 437.3\text{mV}$, $V_s^* = 25.2\text{mV}$, $\tau_{\min} = 0.0579\text{ms}$, $V_1 = 566.6\text{mV}$, $V_1^* = 37.2\text{mV}$, $V_2 = 218.0\text{mV}$, $V_2^* = 56.6\text{mV}$.

we need a steady-state significantly greater than zero to measure the temporal dynamics for opening. This limited range obviated the need to modify Equation 11 to allow the time-constant to go to zero at hyperpolarized levels (this circuit omits the second saturation transistor in Fig. 3b).

The extracted parameters from the fit, based on Equations 10 and 11 and our applied voltage biases, are reasonably close to our expectations, except for V_2^* , the voltage-scale at hyperpolarized levels. For $\kappa \approx 0.75$ and $U_T = 25.4\text{mV}$, we expected $V_2^* \approx 105\text{mV}$, but our fit yielded $V_2^* \approx 56.6\text{mV}$. There are two possible explanations, not mutually exclusive. First, both the limited data at lower voltages and the fact that Equation 11 assumes the presence of a saturation transistor may have contributed to the underfitting of that value. Second, κ is not constant within the chip, but possesses voltage-dependence. Overall, however, the analysis predicts reasonably well the performance of the circuit.

V. CONCLUSION

In this paper, we showed that the transistor is a thermodynamic isomorph of a channel gating particle, through considerations of the operation of both within the framework of energy models. Using this analogy, we synthesized a compact channel variable circuit. This circuit captures both the steady-state's sigmoid shape as well as the time-constant's bell shape, the latter relationship ignored in previous channel models [2], [1]. The circuit is not limited to activation variables; it can be readily altered to implement an inactivation variable. Channels that activate *and* inactivate are easily modelled by multiplying the variable circuits' output currents [2], [13].

Equally important in our design, we were able to use fewer transistors. For an equivalent single variable circuit as ours, Simoni et al. [2] would require 17 transistors, not including transistors implementing their variable conductance. At eight transistors, Mahowald and Douglas [1] match the version of our channel circuit presented here, but not its simplest form, which requires only four transistors. Furthermore, their implementation includes a few drawbacks, namely they reverse the order of the low-pass filter and sigmoid circuit, in addition to using subtraction rather than multiplication for multi-variable channels [2].

This efficiency in our design allows us to fit more silicon cells per unit area on a silicon die than these models. A simple silicon neuron [14], possessing the activation channel in Fig. 4, together with a single input synapse, requires about $330\mu\text{m}^2$ of area in a $0.25\mu\text{m}$ process. Not including pads, this corresponds to almost

30000 neurons on a 10mm^2 array. Thus, large-scale neural system designs are possible using this circuit.

ACKNOWLEDGMENT

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