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Interface Engineering to Control Charge Transport in Colloidal Semiconductor Nanowires and Nanocrystals

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Abstract

Colloidal semiconductor nanocrystals (NCs) are a class of materials that has rapidly gained prominence and has shown the potential for large area electronics. These materials can be synthesized cheaply and easily made in high quality, with tunable electronic properties. However, evaluating if colloidal nanostructures can be used as a viable semiconducting material for large area electronics and more complex integrated circuits has been a long standing question in the field. When these materials are integrated into solid-state electronics, multiple interfaces need to be carefully considered to control charge transport, these interfaces are the: metal contact/ semiconductor, dielectric/semiconductor and the nanocrystal surface.

Here, we use colloidal nanowire (NW) field-effect transistors (FETs) as a model system to understand doping and hysteresis. Through controllable doping, we fabricated PbSe NW inverters that exhibit amplification and demonstrate that these nanostructured materials could be used in more complex integrated circuits. By manipulating the dielectric interface, we are able to reduce the hysteresis and make low-voltage, low-hysteresis PbSe NW FETs on flexible plastic, showing the promise of colloidal nanostructures in large area flexible electronics. In collaboration, we are able to fabricate high-performance CdSe NC FETs through the use of a novel ligand, ammonium thiocyanate to enhance electronic coupling, and extrinsic atom in indium to dope and passivate surface traps, to yield mobilities exceeding 15 $cm^2V^{-1}s^{-1}$. Combining high-mobility CdSe NC FETs with our low-voltage plastic platform, we were able to translate the exceptional devices performances on flexible substrates. This enables us to construct, for the first time, nanocrystal integrated circuits (NCICs) constructed from multiple well-behaved, high-performance NC-FETs. These transistors operate with small variations in device parameters over large area in concert, enabling us to fabricate NCIC inverters, amplifiers and ring oscillators. Device performance is comparable to other emerging solution-processable materials, demonstrating that this class of colloidal NCs as a viable semiconducting material for large area electronic applications.

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SEMICONDUCTOR NANOWIRES AND NANOCRYSTALS

David K. Kim

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To My Family

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ABSTRACT

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SEMICONDUCTOR NANOWIRES AND NANOCRYSTALS

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Colloidal semiconductor nanocrystals (NCs) are a class of materials that has

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1-1:   Semiconductors

Since the invention of the germanium transistor in 1947 by Shockley, Bardeen

and Brattain, research and development of electronic devices has grown tremendously

and into one of the largest industries in the world. The class of materials that has been

largely responsible for this rapid advancement is semiconductors, materials that have a

tunable electrical resistivity (generally ranging from 10^{-2} to 10^{9} ohm-cm) through precise

control over the carrier concentration. In addition, the current conduction through

semiconductors can be modulated over a large range by injected charge carriers,

whether in the form of light, impurities or electrical gating.   From the single germanium

transistor that amplified small currents for telephone use to the highly complex

integrated silicon circuits used in our computer for processing, semiconductor

technology is now present in nearly every aspect of our daily lives.

Since semiconductors are integral in the advancement of modern electronics, it

is only natural that a significant amount of research be devoted to the exploration,

fundamental study and development of new and existing semiconductor materials. By

judiciously cataloguing the library of semiconductors, these materials have been

appropriately selected and optimized for their device technology, such as lead selenide

for infrared sensing, germanium arsenide for light emitting diodes, amorphous silicon

for liquid crystal displays and silicon for integrated circuits. With new applications and

creative device functionalities emerging every day, it is unlikely that a single

semiconductor material, or even a class of materials, will be able to universally address every current and future need.

In particular, over the past two decades, there has been intense industrial demand and academic research interest in the field of large-area electronics: devices that can be cheaply and easily made in high quality, with tunable material's properties (such as electrical, optical, thermal and/or magnetic).[1–4] The materials that are treated in this thesis focuses on colloidal semiconductor nanocrystals (NCs) and its derivative, colloidal nanowires, a class of materials that has rapidly gained prominence over the last two decades, and has shown the potential to address the needs of large area electronics. Chapter 1 will begin with a brief introduction to colloidal semiconductor NCs, explaining basic synthesis and unique size-dependent properties that arises from quantum confinement. Next, the impact surface bound ligands have on charge transport between NCs and methods that have been employed to enhance electronic coupling will be discussed. Finally, an outline of the thesis will be presented at the end of this chapter.

1-2: *Colloidal Semiconductor Nanocrystals*

Semiconductor NCs, zero-dimensional semiconductor structures with nanometer-scale dimensions, are tiny crystals of semiconductors that are on the scale of a nanometer. Depending on the chemical composition, shape and size of the NC, at small enough sizes, the wavefunctions in these NCs start to feel quantum-size effects

owing to the confinement in three directions, and can also be called quantum dots.[5–7]

In this regime, the electronic structure of the quantum dots can be tuned, giving rise to

very unique properties. This size-dependent phenomenon can be understood by

adapting the model of the Linear-Combination-of-Atomic-Orbitals[8,9] to NCs.[10]
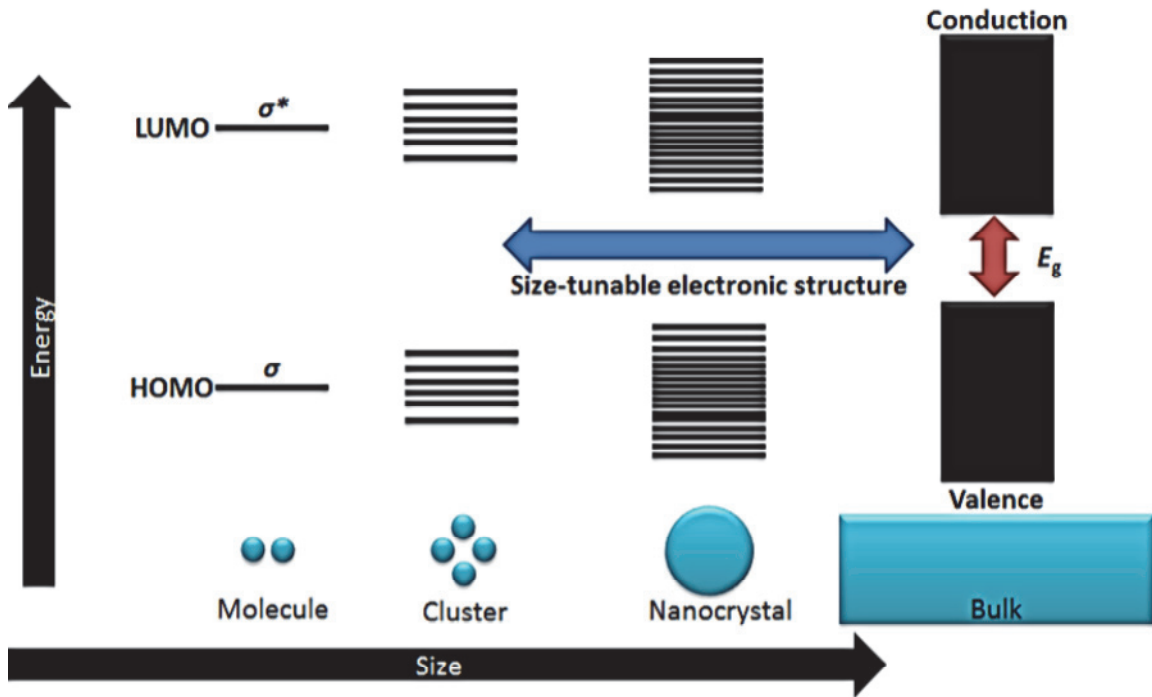
Figure 1-1: Evolution from a single set of sigma (σ) and sigma* (σ*) bonding orbitals, to
discrete molecular orbitals into a continuous energy band.

When two atoms are brought together, the atomic orbitals combine to form two sets of

bonding orbitals: the sigma (σ) bonding and sigma star (σ*) antibonding orbitals, with

electrons residing in the σ bond. As the number of atoms and size of the NC grows

(Figure 1-1), the single atomic orbital continues splitting to form discrete molecular

orbitals, with σ making up the highest-occupied-molecular orbital (HOMO) and σ*

making up the lowest-unoccupied-molecular orbital (LUMO). This can be taken to the

limit of a bulk solid, where the molecular orbitals become a continuous energy band, with the LUMO forming the conduction band and HOMO forming the valence band. In the case of a semiconductor, there exists a forbidden energy gap, which is a material dependent band-gap that is typically on the order of 1 – 3 electron volts. Quantum dots fall in the intermediate category between molecules and bulk, still displaying discrete quantized energy states, but exhibiting a *size-tunable* energy gap and electronic structure. The size at which quantum confinement occurs depends on the Bohr radius of the material's bulk exciton (an excited electron-hole pair). When semiconductors NCs become smaller than this value (for example: radii smaller than 6 nm for CdSe, 46 nm for PbSe, which are two very commonly studied NCs in the literature), the resulting exciton becomes delocalized and confined in all three dimensions. At this point, the NC can be treated as a particle-in-a-box in three-dimensions, with the electron and hole (particles) bound within the NC (box) by the surface of the particle (infinite potential). In these quantum-confined systems, the electron and holes can be treated independently and can be described by separate hydrogenic wavefunctions that occupy discrete energy levels. As such, the size-tunable bandgap arises from controlling the size of the "box", with smaller NCs having larger bandgaps and larger NCs having smaller bandgaps. These quantum dots have also been referred to as "artificial atoms,"[11,12] because of the atomic-like nature of their electronic wavefunctions and energy levels when quantum-confined.

While the particle-in-a-box is a convenient way to convey concepts of a NC's size-dependent bandgap and discrete energy states, it fails to explain the NC's dispersion relation (E vs k), which has been done in great detail by Efros' simple effective mass theory.[13] Initially, using the bulk electron and hole effective masses, the conduction and valence bands can be assumed to be continuous parabolas, representing a blueprint of available k values. However, unlike bulk solids where all k values are continuously allowed on the parabola, NCs display discrete electronic states that quantize the allowed k values, which is controlled by the NC's size. *Decreasing* the NC diameter will shift the first allowed electron and hole states to higher k values, *increasing* the separation between states to yield a quantum-confined bandgap larger than the bulk bandgap by tuning the electronic structure [Figure 1-2(A)]. This was verified by optical blue shifts in the absorption and emission energies [Figure 1-2(B, C)].[14] Manipulation of electronic states through the size and shape of the quantum dot allows us to further tune the material's density of states[15,16] and carrier concentration[17], which was cited earlier as one of the key strengths of semiconductors for electronics.
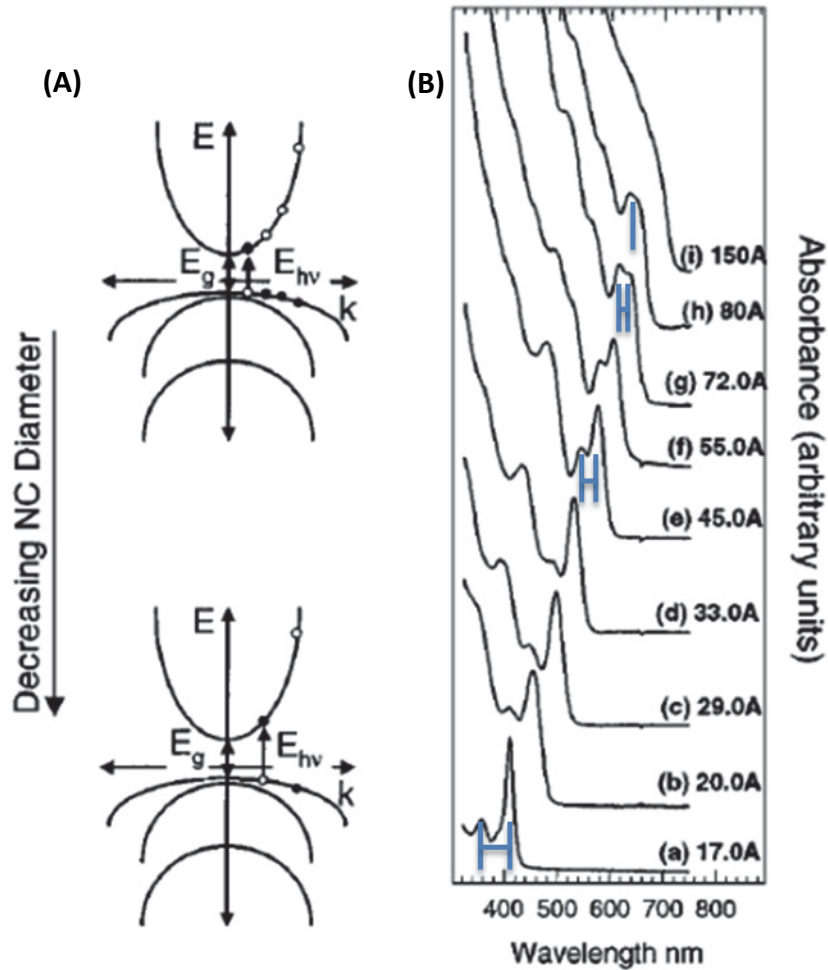
Figure 1-2: (A) Simple effective mass approximation method used to construct an energy diagram (*E* vs *k*) of the conduction and valence bands of a bulk semiconductor. At sizes smaller than the Bohr radius, confinement of the NC quantizes the allowed *k* values. Decreasing the NC diameter shifts the first state to larger *k* values, increasing the separation between discrete energy states. (B) This was experimentally observed spectroscopically as blue shifts in the absorption edge and larger separations between discrete energy states (separation between the 1st and 2nd states emphasized by blue lines to guide the eye). Reproduced from *Annu. Rev. Mater. Sci.* **30**, 545-610 (2000).

These NCs can be synthesized by a variety of methods, such as high-resolution electron beam lithography,[18,19] spontaneous island formation during strained epitaxy[20–22] and colloidal synthesis.[23] Of these methods, colloidal synthesis has emerged as the

most promising technique for large-area electronics, owing to its low-cost, low-temperature, high quality solution processing. While lithographic and island formation techniques have greatly aided in the understanding of structural and electronic properties of quantum-confined systems,[24,25] lithographic techniques are time-consuming and require expensive equipment and island formation has only been shown for select semiconducting materials. Wet chemical synthesis has been demonstrated for a wide range of semiconducting materials with exceptional control over its size, shape and dispersity.[26]
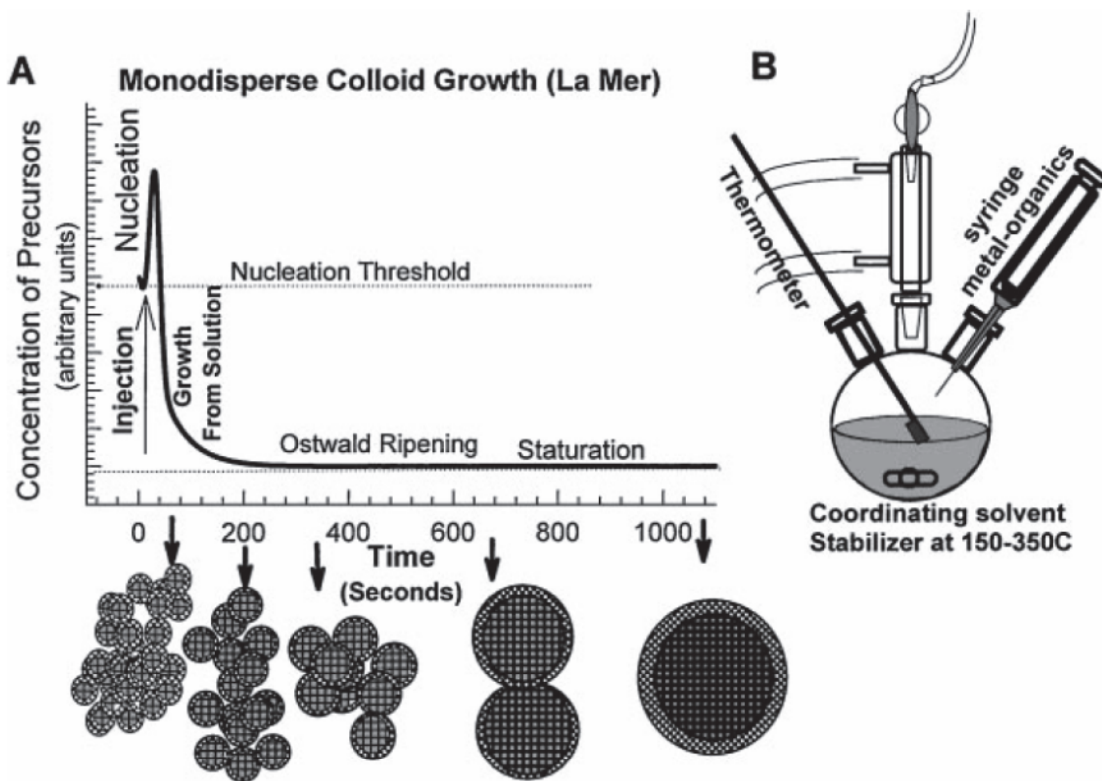
Figure 1-3: A general scheme for the growth of monodisperse NC after the initial "hot-injection" of precursors (in framework of the La Mer model). (B) Schematic of the setup used to prepare monodisperse NCs. Reproduced from *Annu. Rev. Mater. Sci.* **30**, 545-610 (2000).

Colloidal synthesis is not only a powerful technique that is applicable to a broad

range of materials, but is also extremely simple, enabling researchers all around the

world access to a library of nanomaterials. This simple wet chemical method was

pioneered by Murray, Norris and Bawendi in 1993, which describes the facile synthesis

of monodisperse CdSe NCs.[23] An example of a typical synthesis requires a combination

of organometallic [$(CH_3)_2Cd$] and elemental precursors (S, Se or Te), rapidly injected into

a "hot" (~300^oC) flask containing a vigorously stirring coordinating solvent. The rapid

addition of precursors supersaturates the solution above the nucleation threshold,

causing a burst of small crystallites to spontaneously nucleate in solution in order to

rapidly decrease the precursor concentration. After nucleation, the NCs undergo

controlled Oswald ripening, where the difference in free energy favors the growth of

large particles at the expense of small particles. The stabilizing molecules used in CdSe

synthesis (trioctylphosphine and trioctylphophine oxide) provide a significant steric

barrier to slow the growth kinetics to enable exquisite control over the size and shape of

the nucleated crystallites. These stabilizing agents are also necessary to prevent

aggregation and precipitation of the crystallites, effectively acting as "capping groups"

to create a colloidal suspension of NCs in solution.[27] After a NC growth, the reaction is

rapidly quenched at the desired NC size. Since then, the library of available

organometallic precursors and ligands used has broadened significantly and is now

applied to the synthesis of a wide range of chemical compositions. This "hot-injection"

method has been successfully applied by researchers worldwide to a wide range of

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semiconducting materials (II-VI,[28,29] III-V[30,31] and IV-VI[32,33]), shapes (cubes,[34,35] tetrapods,[36,37] rods,[38,39] wires[40–42]) and sizes , demonstrating the accessibility and applicability of this method.

1-3: *Charge Transport through Nanocrystal Solids*

Stabilizing molecules, generally long-chain, insulating, organic ligands that are used for exquisite synthetic control over the shape and size of NCs and passivation of surface electronic states, also sterically stabilize NCs in solution as a colloidal suspension. These high-quality, inorganic crystalline semiconductor NCs dispersions can also be thought of as "inks", and can be processed by a variety solution-based material deposition techniques (spincasting, dip-coating, inkjet printing, dropcasting, spraycoating)[43–48] to form uniform, but disordered NC thin films over large areas. As such, a great deal of work has been done in the field to controllably assemble NCs into ordered periodic structures. These surface ligands also play an important role in the self-assembly of ordered single or even multi-component (binary, ternary, etc) NC solids, known as "superlattices."[49–52] These superlattices are characterized by three-dimensional periodicity, exhibiting long-range order over hundreds of microns and can give rise to unique properties, such as enhanced thermal stability to prevent NC sintering when compared to disordered mixtures.[53]

However, the long ligands used for synthesis, stabilization, surface passivation and self-assembly also provide barriers that limit interparticle coupling and carrier

transport in between individual NCs, electronically isolating the NCs and making these thin-films insulating. For any solid-state device applications, strong interdot coupling is necessary for efficient charge transport through the solid. Annealing can be used to decompose the as-synthesized ligands with nanoparticles with higher melting points (such as FePt and MnO), but it often leads to sintering of semiconducting NCs (CdSe, HgTe, PbSe).[54–56] Sintering the NCs to remove the original capping ligands has also been found to contaminate semiconducting NC solids and leave behind carbonaceous species due to partial ligand pyrolysis.[57] In addition, sintered films have been found to exhibit carrier transport far inferior to similarly prepared thin films grown *via* chemical vapor deposition. Sintering CdSe NCs 2 nm in diameter at 350°C yielded a polycrystalline thin-film with domain sizes as large as 15 nm. Reported mobilities were 1 $cm^2V^{-1}s^{-1}$, more than two orders of magnitude lower than vapor-deposited CdSe thin films with comparable grain sizes.[54] In addition, sintered films exhibited large hysteresis, did not saturate properly and are no longer quantum confined, losing the electronic tunability that made them so unique. Another approach would be to replace the original bulk ligands with a smaller compact ligand to decrease interparticle spacing to enhance electronic coupling between NCs.

Over the past decade, a number of compact molecules have been investigated as ligands to enhance electronic coupling.[26] There are two methods commonly used to replace the long, bulky ligands with shorter, ligands: solid- and solution-exchange. Solid-exchange involves first depositing the NCs with the as-synthesized ligands into a thin-

film, which takes advantage of the solution-processibility of the NC dispersions. These films are then submerged in a solution containing an excess of the new shorter ligand for ligand exchange. Typical ligands used for solid-exchange for CdSe nanostructures have been 1-7-heptanediamine and 1,4-phenylenediamine,[58] butylamine[59–61]and sodium hydroxide[59,62,63] and for PbSe nanostructures have been methylamine and pyridine,[56] ethanedithiol,[64–66] Meerwein's salts[67] and hydrazine.[32,56,68,69] After exchange, these shorter ligands significantly decrease the interparticle spacing to enhance electronic coupling, but the NC films exhibit significant cracking due to the void spaces leftover from the original ligands. Subsequent depositions and exchanges are necessary to fill these empty spaces and remove remaining bulky ligands to get a continuous conductive film. Field-effect carrier mobilities in solid-exchanged NC thin-films have been typified by values of 10^{-2}-1 $cm^2V^{-1}s^{-1}$, indicative of thermally activated hopping transport.[63] Of these ligands, champion mobilities were reported for CdSe NCs using sodium hydroxide (0.6 $cm^2V^{-1}s^{-1}$)[63] and for PbSe NCs using either hydrazine (0.95 $cm^2V^{-1}s^{-1}$)[32,56] or a combination of ethanedithiol with atomic-layer deposition infilling (1.05 $cm^2V^{-1}s^{-1}$),[66] with I_{ON}/I_{OFF} ratios as high as 10^4.

Solution-exchange involves replacing the original bulky ligands with shorter compact ligands that maintains solution-dispersibility and processability of the NCs. This method has been explored significantly less compared to solid-exchange, since one of the main limitations is that many small-molecule ligands have poor colloidal solubility. After solution-phase exchange, the nanoparticles will aggregate and "crash

out" of solution. Only a handful of ligands had been identified as potential candidates, such as the weak coordinating solvent pyridine[23,70,71] for CdSe nanostructures and octylamine[72] for PbSe nanostructures. However, recent advances in ligand chemistry have brought this method a great deal of attention. Rather than using long alkyl chains to prevent aggregation in nonpolar solvents, small compact ligands (inorganic ions) can be used instead to provide electrostatic stabilization of NC colloids in polar solvents. Typical small electrostatically stabilizing ligands used for solution-phase exchange are nitrosonium tetrafluoroborate,[73] molecular metal chalcogenides (MMCs)[74] and chalcogenide anions,[75] ammonium thiocyanate[76] and Meerwein's salts,[67] which have been generally applied to a wide range of NCs. These novel ligands enable uniform NC thin-films to be deposited in a single, simple step with short interparticle distances and no noticeable film cracking. Of these ligands, MMCs and ammonium thiocyanate ligands have exhibited the highest electronic coupling with impressive reported mobilities exceeding 15 $cm^2V^{-1}s^{-1}$,[77,78] suitable for a wide range of large area electronics applications.

Intrinsic semiconductors are also inherently insulating, so while decreasing the interparticle distance can lead to improved electronic coupling, semiconductor NC thin-films often suffer from a low concentration of mobile carriers, especially in wide-gap semiconductors.[79,80] In semiconductor NCs, quantum-confinement widens the bandgap to further decrease the intrinsic carrier concentration [which exhibits an

$exp\left(-E_g\big/k_\mathrm{B}T\right)$ dependence]. An active area of research has been to develop a

rationale doping scheme for semiconductor NCs (akin to silicon technology) to increase

and/or modify the carrier concentration and carrier type (hole or electron). Approaches

to dope semiconductor NCs have included thermal evaporation of potassium metal,[58,81]

electrochemical doping[58], "remote doping," using hydrazine[32] or oxygen,[82] tuning the

stoichiometry[83–85] and substitutional doping with impurity atoms during synthesis.[86–90]

Despite doping challenges, recent successes utilizing thermal diffusion of indium[91] may

help us create a generalized scheme for controllable and stable doping for this class of

materials.

Finally, semiconductor NCs exhibit high concentrations of trap states, a problem

that also limits charge transport. The large surface-to-volume ratio further exacerbates

the issue, since the NC surface has multiple dangling bonds and mid-gap charge-trapping

states.[92] These surface states are highly sensitive to the NC's surrounding environment,

most notably the capping ligands, and have been extensively studied to minimize traps

related to photoluminescence (PL). To illustrate this, the original as-synthesized ligands

for CdSe NCs (TOP/TOPO), also passivates surface trap states on the NC surface to give

strong photoluminescence and minimal trap emission.[23] Other capping groups, such as

pyridine, reduces the PL,[93] while certain amines (hexadecylamine, dodecylamine and

allylamine)[94,95] have been found to drastically improve it. Coating the NC with an

appropriate inorganic "shell" during synthesis to make "core/shell" NCs has also been

found to an effective route to reduce surface trap states related to PL[94,96,97] and have made excellent materials for light-emitting-diodes.[75,98]

Similar to the research done to passivate traps related to photoluminescence, traps related to electronic transport (charge trapping, hysteresis, surface passivation)[26,85,99–101] in transistor applications have gained a great deal of attention. Some ligands found to passivate surface traps are Cl⁻, I⁻ and Br⁻, have yielded modest mobilities but impressive photovoltaic performances.[102] Besides ligands, post-synthetically treating a NC film with atomic layer deposition (ALD)[66,103] and successive ionic layer adsorption and reaction (SILAR)[104] and thermal annealing of indium[91] have been proposed as routes to passivate electronic trapping states for transistor applications. As such, appropriately addressing surface states will continue to be an area of active interest in the field.

1-4:   *Outline of Thesis*

Ultimately, the goal of this thesis is to determine if colloidal nanostructures can be used as a viable semiconducting material for large area electronics and more complex integrated circuits. In order to appropriately evaluate this class of materials, we must incorporate them into device architectures (single FETs, inverters, ring oscillators) to properly assess their performance and future outlook (device scalability, low voltage operation). However, when these materials are integrated into solid-state devices, additional device interfaces, most notably the metal/semiconductor[3,105,106] and

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dielectric/semiconductor[1,85,107–109] interfaces, further complicate the challenging issue of controlling charge transport. As such, a simplified approach utilizing colloidal nanowires as the semiconducting material was initially undertaken.

Similar to colloidal NCs, colloidal nanowires share many of the same issues, such as doping, trap density and ligand issues we discussed earlier for NCs. However, nanowires have excellent electronic coupling because they have no interparticle spacing! This simplifies the problem greatly and helps us focus on other interfaces without having to worry about other variables (interparticle spacing, coupling). In Chapter 2, we describe the synthesis of high-quality, single-crystalline PbSe NWs and the fabrication of PbSe NW FETs. Taking this FET platform, we investigate the role of hydrazine/oxygen doping on PbSe nanostructures and its effects on the energy band alignment at the metal/semiconductor interface. With this knowledge, we can control the carrier type to make the first colloidal PbSe NW inverters in Chapter 3. In Chapter 4, we further investigate the role of oxygen doping and show that small variations in stoichiometric balance can lead to large changes in carrier type. We also investigate interface trapping and find a robust gate dielectric to minimize hysteresis, and fabricate the first low-voltage colloidal PbSe NW FETs on flexible substrates.

Taking the knowledge we have gained from the NW charge transport measurements, we can similarly apply the same techniques to dope and decrease carrier trapping in NC systems. In Chapter 5, in collaboration with members of the Kagan and Murray groups, as well as National Institute of Standards and Technology

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(NIST), we are able to fabricate high-performance CdSe NC FETs. Through the use of a novel ligand, ammonium thiocyanate to enhance electronic coupling, and extrinsic atom in indium to dope and passivate surface traps to increase the carrier concentration, these FETs exhibit mobilities exceeding 15 $cm^2V^{-1}s^{-1}$. Additionally, the use of non-corrosive ligand ammonium thiocyanate and mild annealing to promote indium diffusion is compatible with flexible electronics.

In Chapter 6, we take the flexible platform developed in Chapter 4 to fabricate low-voltage, high-performance CdSe NC-FETs on plastic substrates. In order to demonstrate the viability of semiconducting NCs for more complex integrated circuits, we fabricated the first NC integrated circuit (NCICs) inverters, amplifiers and ring oscillator. In Chapter 7, future work to realize higher switching speeds and higher bandwidths needed for digital and analog electronic circuits, respectively, is described, followed by concluding remarks in Chapter 8.

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CHAPTER 2:   Colloidal Nanowire Synthesis and Nanowire Alignment[1]

Probing the electronic properties of nanostructured materials and exploiting

their characteristics in applications requires their integration in device architectures,

such as field-effect transistors (FETs). However, when these materials are integrated

into solid-state electronics, additional interfaces (metal/semiconductor[1–3] and

dielectric/semiconductor[4–8]) need to be considered because they play a large role in

controlling charge injection into and charge transport through the nanomaterial [Figure

1-4]. In order to understand the role of interfaces on charge transport, we fabricated

nanowire FETs atop varying dielectric stacks, which we utilize as a powerful platform to

unmask the intrinsic electronic properties of colloidal lead selenide (PbSe) nanowires.[3,8]

PbSe is a high mobility, infrared absorbing semiconductor that exhibits strong

quantum confinement in nanostructured materials due to its large Bohr exciton radius

(a_{ex} ~ 46 nm) and its uniquely large and similar electron and hole Bohr radii (a_e ~ a_h ~

23nm).[9] While colloidal nanocrystal FETs are more commonly used in the literature,[10,11]

charge transport in NC-FETs is further complicated by variations in inter-particle spacing

and film cracking, as the film shrinks into islands upon solid-state exchange of the long,

insulating ligands used in NC synthesis with the shorter ligands used to chemically dope

and to decrease the interparticle spacing, converting the initially insulating film to

become conductive [Figure 2-1].
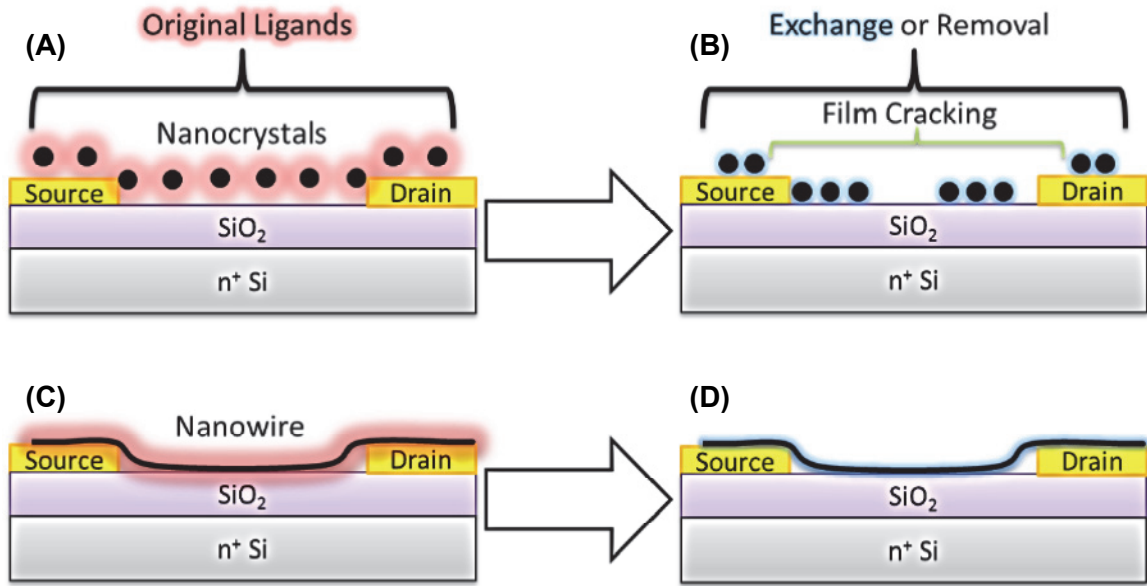
Figure 2-1: Typical bottom-gate/bottom contact field-effect transistor used to characterize electronic transport for nanostructured materials. Schematic of ligand-exchange for nanocrystals from (A) original long insulating organic chains to (B) shorter ligands. Similar schematic for nanowires with (C) original long-chain insulating ligands to (D) shorter chains. Original ligands appear as a large red glow, while shorter exchanged ligands appear as a smaller blue glow, to emphasize the significant void-space ligands leave behind in nanocrystal solids when removed/replaced, compared to in nanowires that have direct connection to the source/drain electrodes.

In order to simplify the problem and gain an understanding of the role interface modification has on electronic transport in nanostructured materials, we utilized single-crystalline colloidal NWs. The NWs bridge the entirety of the FET channel, avoiding the changes in inter-particle spacing and cracking in NC films upon ligand exchange, providing a model system to investigate the role of interface modification on the electrical properties of nanocrystalline devices [Figure 2-1].
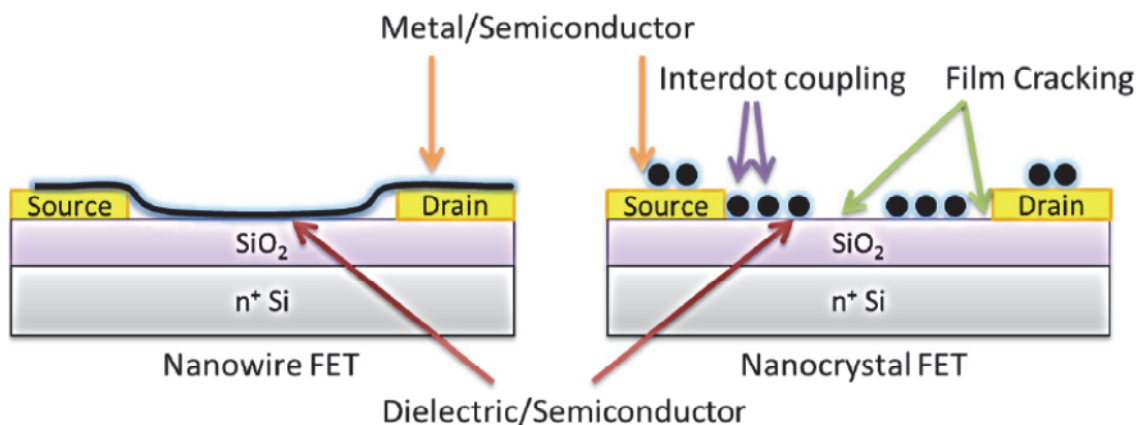
Figure 2-2: Schematic illustrating the different interfaces to consider in both a nanowire and nanocrystal field-effect transistor (FET). The blue halo around the different nanostructures represents the removal of as-synthesized ligands with shorter ones.

In Chapter 2, explicit detail on the air-free synthesis and purification of PbSe nanowires, varying dielectric stack preparation, FET fabrication methods and electric-field nanowire alignment techniques are described.

2-1:   PbSe Nanowire Synthesis

Single-crystalline PbSe nanowires were synthesized by wet-chemical methods *via* oriented attachment of nanocrystals, as reported previously.[12] Rigorous air-free conditions were used from synthesis to purification, fabrication, and characterization to prevent oxidation of the NWs, which has been observed in PbSe nanostructures.[13–17] All manipulations were carried out using standard Schlenk-line techniques under dry nitrogen. Tri-*n*-octylphosphine (further referred to as TOP, Aldrich, 90%), oleic acid (OA,

Aldrich, 90%), diphenyl ether (Aldrich, 99%), amorphous selenium pellets (Aldrich, 99.999%), lead acetate trihydrate (Fisher Scientific Co.), and n-tetradecylphosphonic acid (TDPA, Strem, 97%) were used as purchased without further purification. Anhydrous chloroform and hexane were bought from Aldrich. To prepare a 0.167M stock solution of trioctylphosphine selenide (TOPSe), 1.32 g of selenium was dissolved in 100 mL of TOP overnight by stirring at room temperature.

Lead acetate trihydrate (0.76 g) was dissolved in 2 mL of OA and 10 mL of diphenyl ether in a 125 mL three-neck conical flask. The solution was degassed at room temperature under vacuum below 1 Torr and refilled with nitrogen at least three times. For successful synthesis of straight nanowires, lead acetate trihydrate had to be purchased from Fisher. Other manufacturers, such as Sigma-Aldrich, did not yield straight nanowires due to impurities in the source material. After refilling the reaction vessel with nitrogen, a needle was placed in the septum to allow venting as the solution was heated to 150°C with vigorous stirring. The solution was heated at 150°C for 30 minutes under nitrogen flow in order to form a lead-oleate complex with a jaundice yellow color. Degassing and venting was found to be critical to controlling the color of the complex solution for successful nanowire synthesis. If the solution was not degassed, the complex would turn a deep orange-brown and yield zig-zag nanowires. If the venting began at 150°C, the solution would remain a clear color and a significant amount of undissolved lead-acetate would remain in the flask, mostly leading to a variety of nanocrystal shapes and what appeared to be unreacted reagents. Over thirty

30

minute period of time, some amount of material escaped the flask through the needle

vent. While the vented material was never characterized, it would be of interest to

study to understand how venting affected the complex formation and subsequent

nanowire synthesis.

The lead-oleate solution was then cooled to 60°C, the venting needle removed

and 4 mL of 0.167M TOPSe solution was added slowly to prevent premature nucleation

of PbSe. The combined lead-oleate/TOPSe solution was allowed to come back up to

60°C, taken up in a syringe and immediately injected under vigorous stirring into a hot

(250°C) growth solution containing 0.2 g TDPA dissolved in 15 mL of diphenyl ether in a

125 mL three-neck conical flask. This TDPA solution was also degassed and refilled with

nitrogen at least three times at room temperature before heating. The injection time

and temperature profile was found to be important in determining the reproducible

formation of straight nanowires. The injection of precursors must be fast, and the

temperature of the reaction vessel should not fall below 190°C after injection,

maintained above 210°C for nanowire growth, but should not go above 220°C. Upon

injection, the solution will slowly turn a purple/black color over about 20 to 30 seconds.

After ~50 seconds of heating, the reaction mixture was cooled to room temperature

using a water bath. Once cooled, the reaction vessel (still under N_2) was transferred to a

glovebox, where the crude solution was mixed with equal amounts of hexane, and the

nanowires were isolated by centrifugation at 4300 rpm for 5 minutes. The resulting

nanowire precipitate was redispersed in chloroform for characterization or device

fabrication. Transmission electron microscopy (TEM) [Figure 2-3(A)] shows the

synthesis produced crystalline PbSe NW samples approximately 10 nm in diameter and

over 10 μm in length. Optical absorption spectra of PbSe nanowires deposited on

double-side polished silicon substrates were collected with a Nicolet 8700 FTIR using

transmission IR. Figure 2-3(B) shows the absorption spectra of PbSe nanowires with a

bandgap energy of 0.45 eV.
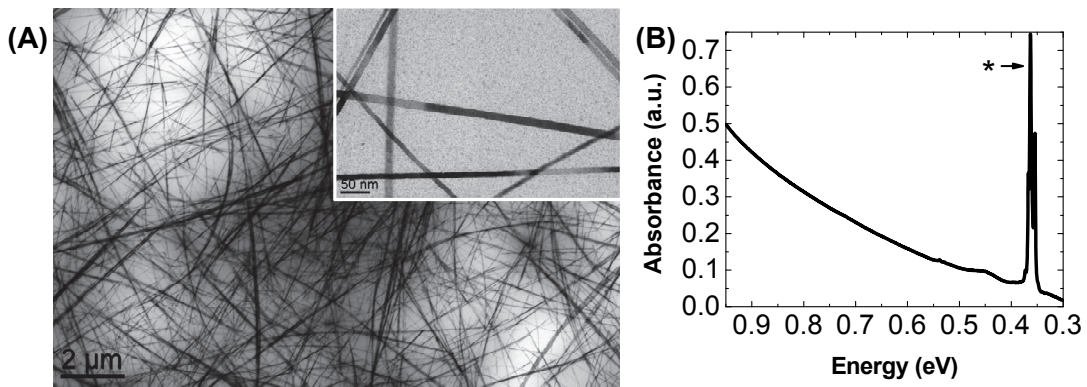
Figure 2-3: (A) Transmission Electron Microscope image of as-synthesized PbSe nanowires and (B) absorption spectrum of dropcast (* is from –CH stretches of Oleic Acid).

2-2: Device Fabrication on varying Dielectric Stacks

All devices with varying dielectric surfaces, except the flexible device, were

fabricated on an *n*-doped Si wafer with 250 nm thermally grown SiO_2 from Silicon Inc.

The Si wafers were treated with UV-Ozone for thirty minutes before deposition of

varying dielectrics. All film thicknesses were confirmed using either a capacitance

measurement (metal/dielectric/metal) using a HP 4276 A LCZ meter and/or surface

profilometry (Tencor, Alpha Step 200). The dielectric constant was calculated to be 3.05

for polyimide, 3.15 for parylene-C, 7.5 for SiN and 9.0 for Al_2O_3.

The following is a list of techniques to prepare a range of dielectric surfaces on

both rigid and flexible substrates. Later in Chapter 4, the effect of dielectric interface on

hysteresis and charge trapping is explored in further detail.

SiO_2/Polyimide Dielectric Stack: Polyimide precursors (PI-2611 series) were

purchased from HD MicroSystems, and diluted in N-methyl-2-pyrrolidone to a ratio of

1:2. The diluted polyimide precursor was then spin coated (3000 rpm for 30 sec) and

cured (350°C for 30 mins) to form an approximately 180 nm polyimide layer.

SiO_2/Parylene Dielectric Stack: Parylene-C was purchased from Specialty Coating

Systems and deposited in a PDS 2010 system to a thickness of about 250 nm.

SiO_2/Silicon Nitride Dielectric Stack: An Oxford Instruments PlasmaLab 100

system was used to deposit 35 nm of plasma-enhanced chemical vapor deposited

(PECVD) SiN.

SiO_2/Aluminum Oxide Dielectric Stack: A Cambridge Nanotech Savannah 200

system was used to deposit 30 nm of atomic layer deposited (ALD) Al_2O_3 at 250°C using

trimethylaluminum and water precursors.

Flexible Device Fabrication: Kapton$^®$ 200 Type E films were obtained from

DuPont^{TM} and served as the substrate. Kapton films were cleaned for 5 minutes each in

an ultrasonic bath of ethanol and distilled-H_2O, followed by a thirty minute UV-ozone.

Using a shadow mask, 20 nm of aluminum was deposited through a shadow mask and

then placed in an Oxford Instruments 80Plus parallel-plate reactive ion etcher (RIE). The

back-gate sample was briefly exposed to an oxygen plasma (150W, 15 s) to increase the

thickness of the native Al_2O_3 and create hydroxyl groups necessary for ALD Al_2O_3. After

forming a thin oxide on the aluminum back-gate, the flexible sample was placed in the

Cambridge Nanotech Savannah 200 ALD tool to deposit 30 nm of Al_2O_3.

Octadecyl-phosphonic acid Treatment of Al_2O_3: The Al_2O_3 device was prepared

with a self-assembled monolayer following a previously reported procedure.[18] Al_2O_3

devices were submerged in 0.005M octadecylphosphonic acid (ODPA) (PCI Synthesis) in

IPA solution over 16 hours to treat the Al_2O_3 surface. Flexible devices were similarly

treated with ODPA to passivate the Al_2O_3 back-gate.

Once the dielectric surface was prepared, electrodes were deposited through a

photopatterned resist or shadow mask. For SiO_2, SiN and Al_2O_3 dielectric substrates,

electrodes were patterned using photolithography with a bilayer of Lift-off Resist

(LOR3A from MicroChem) and S1813 (Microposit). Samples were photolithographically

patterned to define channel lengths of 20 μm and widths of 200 μm using a Karl Suss

Mask aligner and developed in MF-319 (Microposit). The exposed samples were

cleaned by a Technics plasma etcher with an oxygen plasma (100W, 3 minutes) and

metal was deposited by e-beam evaporation of 2 nm of Ti and 18 nm Au. Metal was

subsequently lifted off using Remover PG (MicroChem) at 75°C. Titanium (or similarly

chrome) is a necessary adhesion layer for gold metallization, since gold has poor

adhesion to SiO_2 surfaces and the patterned gold electrodes will lift-off. The SiO_2

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fabricated devices were then put in a YES (Yield Engineering Systems) Oven, where the

fabricated devices were first cleaned with an O_2 plasma and then vapor primed with

hexamethyldisilazane (HMDS, Aldrich, 99.9%) for five minutes at 150^oC. The SiN devices

were left untreated.

Polyimide, parylene and flexible devices were fabricated by evaporating Au

through a shadow mask made of silicon nitride membranes with very fine channel

lengths of 20 μm and widths of 1260 μm. Shadow masks were chosen for the polymer

dielectric surfaces since the substrate appears to swell when submerged in Remover PG,

even at room temperature. The swelling of the polyimide and parylene often causes

severe cracking and delamination of the patterned electrodes, making them unusable

for devices.

2-3:   Nanowire Alignment

Nanowires were aligned across device structures having channel lengths of 20

μm and channel widths of 200 μm (SiO_2, SiN/SiO_2 and Al_2O_3/SiO_2 dielectric stacks) or

channel lengths of 20 μm and channel widths of 1260 μm (polyimide/SiO_2,

parylene/SiO_2 dielectric stacks, flexible substrates). Nanowire solutions were dropcast

under dc electric fields of 10^4 to 10^5 V/cm [Figure 2-4(A)], aligning nanowire arrays

across the pre-fabricated bottom electrodes [Figure 2-4(B, C)]. The number of

nanowires spanning the electrode channel is controlled by varying the concentration

and volume of the nanowire solution that is dropcast. Nanowires were dispersed in

octane:nonane at a 1:1 (vol:vol) ratio with several drops of 10 wt% solution hexadecane-graft-polyvinylpyrrolidinone (HD-PVP) copolymer (M_n = ~7300) to improve the nanowires' dispersability. The presence of HD-PVP is absolutely critical to preventing the nanowires from aggregating and precipitating out of solution. Without the use of HD-PVP, nanowires "crash out" of solution and will align as mats of densely clumped nanowires.
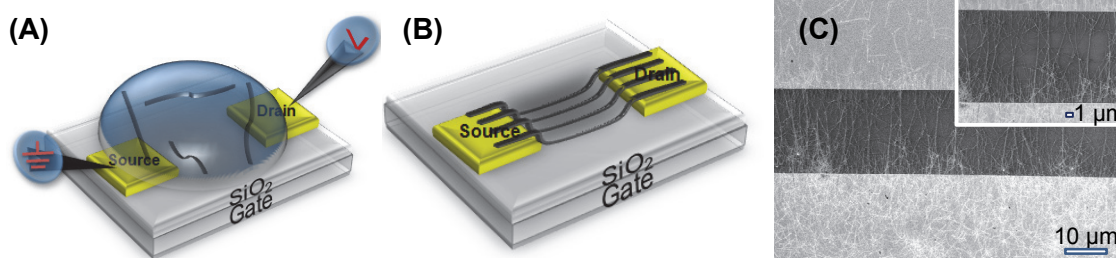
Figure 2-4: (A) Schematic of drop-casting NW dispersions for electric field directed-assembly. (B) Schematic of PbSe NW FET after alignment. (C) SEM of PbSe NW FET.

Devices were then well-washed in both ethanol and chloroform to remove excess ligands, namely the oleic acid used in nanowire synthesis and the HD-PVP used to aid nanowire dispersion. Transmission FTIR and FET electrical characteristics are correlated with device washing (Figure 2-5). Removing surface-bound ligands improved FET transport characteristics, whereas insufficient washing led to very poor FET current modulation.
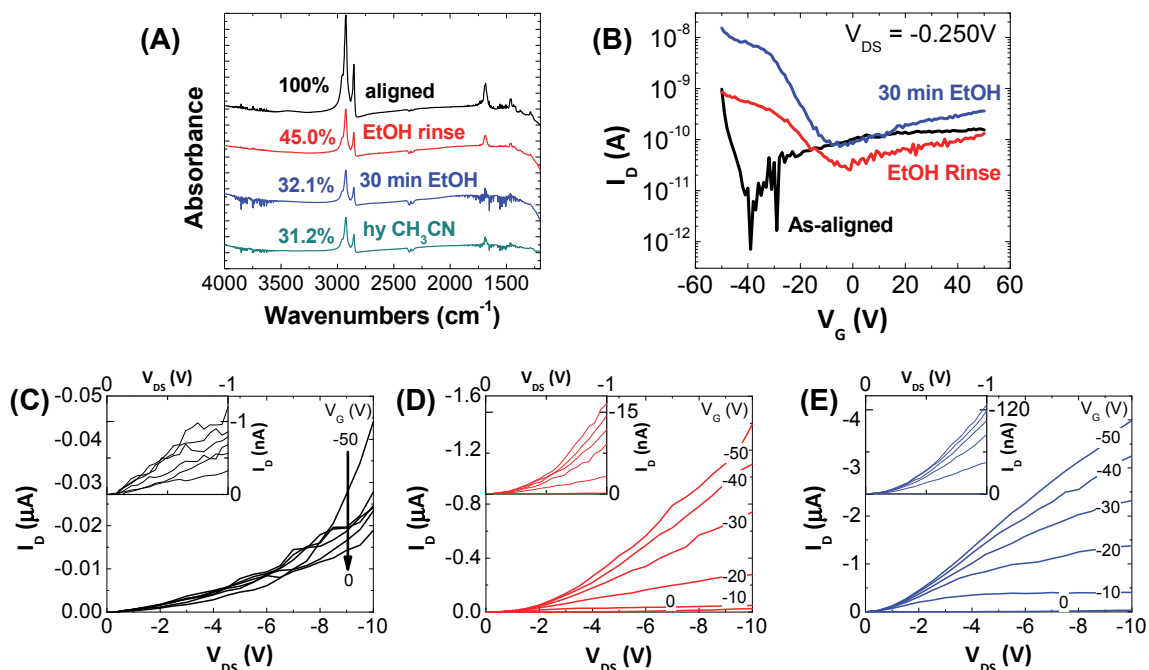
Figure 2-5: (A) Transmission FTIR spectra of PbSe NW ensembles on double polished silicon substrates measured for (——) as-deposited NWs representing as-aligned NWs with no wash, (——) rinsing with 1.0mL ethanol, (——) 30 min immersion in ethanol and (——) 4M hydrazine in CH_3CN for 30 minutes followed by pulling low vacuum for 60 minutes. [EtOH = ethanol, hy =hydrazine, CH_3CH = acetonitrile, the percentages indicate the remaining integrated CH stretch intensity]. (B) I_D-V_G characteristics of the NW FETs following (——) as-aligned (——) EtOH rinse, (——) submerging in EtOH for half an hour. I_D-V_{DS} characteristics of PbSe NW FETs (C) as-aligned, after (D) rinsing with 1.0 mL EtOH, and (E) 30 minutes in EtOH.

Electric-field directed assembly was carried out in an MBraun nitrogen glovebox and all solvents used were distilled and anhydrous. For *n*-type conversion of the *p*-type NW FETs, varying concentrations of hydrazine (Aldrich, 98%) in acetonitrile (Aldrich, anhydrous, 99.8%) was used and is explored in further detail in Chapter 3, which discusses the charge-transfer doping of PbSe nanowires and its role on the metal-semiconductor interface.

An Agilent 4156C parameter analyzer in combination with a Karl Suss PM5 probe station mounted in the nitrogen glovebox was used to measure device characteristics. The source was grounded and a highly *n*-doped silicon wafer was used as a back gate electrode.

2-4:   *References*

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CHAPTER 3:   Metal-Semiconductor Interface and Doping to Control Ambipolar and Unipolar Transport[2]

Similar to dopants in bulk semiconductors, exposing the surface of nanocrystals (NCs) to organic compounds has been reported to provide a route to modify the electronic properties of nanostructured materials.[1,2] Most effectively hydrazine has been reported to *n*-dope lead-selenide (PbSe) NC and nanowire (NW) field-effect transistors (FETs)[1,3–5] and improve device characteristics[6] at typical hydrazine concentrations of 1M.[1,3–5,7,8] Removal of hydrazine returns the NC FET behavior to *p*-type.[1]   Other simple amines[3] and ethanedithiol[7] have also been used to modify nanostructures, but the origin of the observed changes in carrier transport measured in FETs upon ligand exchange is not well understood and remains difficult to control.[4]

In Chapter 3, we unmask the intrinsic electronic properties of wet-chemically synthesized, PbSe NWs through air-free preparation and integration to form the active, semiconducting channels of FETs. Compared to colloidal NC FETs, which have additional interfaces and variables to consider, such as the interparticle spacing and film cracking upon removal of insulating ligands, single crystalline colloidal NW FETs are an ideal system to explore the role of interfaces on charge transport. We use spatially selective and concentration dependent surface modification to engineer the electrical characteristics of PbSe NW FETs. Ambipolar FETs were prepared at low concentrations

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of dopants, whereas at high concentrations, unipolar *n-* and *p-*type FETs were formed

using hydrazine and oxygen, respectively. At low concentrations of surface modifiers

commonly used to dope NC and NW FETs, charge transfer at the _metal-semiconductor_

interface of the FET modifies carrier injection and dominates the measured changes in

device behavior. While NCs have higher surface area and may be more readily doped

than NWs, carrier concentration modulation of the NWs in the channel is only observed

at much higher concentrations of chemical dopants.

3-1:   *Ambipolar PbSe Nanowire Field-Effect Transistors*

Single-crystalline PbSe NWs were synthesized by wet-chemical methods *via*

oriented attachment of NCs, as reported previously[9] and detailed in Chapter 2. A

solution of PbSe nanowires were dropcast under dc electric fields of 10^4 to 10^5 V/cm,

aligning NW arrays across the pre-fabricated bottom electrodes. Devices were then

well-washed in both ethanol and chloroform to remove excess ligands, namely the oleic

acid used in NW synthesis and the hexadecane-graft-polyvinylprrolidone (HD-PVP) used

to aid NW dispersion. Removing surface-bound ligands improved FET transport

characteristics, whereas insufficient washing led to very poor FET current modulation.

As-aligned PbSe NW FETs show evidence of both hole and electron transport,

known as ambipolar transport, but stronger hole transport gives predominantly *p*-type

behavior [Figure 3-1(A)]. This is observed as the I_D-V_{DS} characteristics show holes

accumulate in the NW channel near the source electrode at negative V_{DS} and V_G. The

closely spaced, sigmoidal I_D-V_{DS} characteristics at low-voltages, known as "current

crowding,"[10] [highlighted in the inset Figure 3-1(A)], limits the device on-current. After multiple washings with ethanol, chloroform and acetonitrile, the observed "current crowding" remains. We hypothesize that there is either intervening material or physical space that remains between the surface of the electrodes and the NWs, which is not removed upon washings with common solvents.
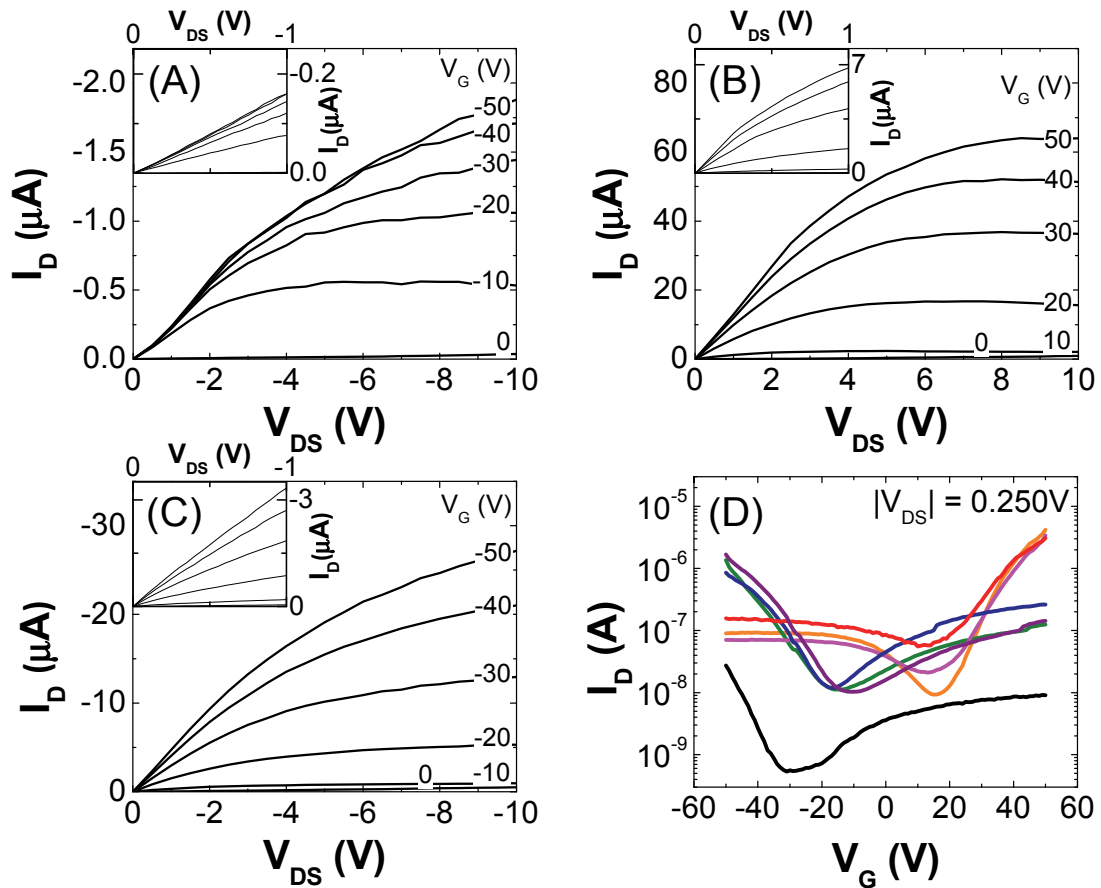
Figure 3-1: I_D-V_{DS} characteristics of PbSe NW FETs (A) as-aligned, after (B) first immersion in 4M hydrazine in acetonitrile, and (C) pulling low vacuum. (D) I_D-V_G characteristics of the NW FETs following the reversible conversion of FET behavior from predominantly hole to electron transport corresponding to: (—) Fig. 1(A), (—) Fig. 1(B), (—) Fig. 1(C), (—) 2nd 4M hydrazine immersion, (—) 2nd pulling vacuum, (—) 3rd 4M hydrazine immersion and (—) 3rd pulling vacuum.

Immersing these devices in 4M hydrazine in acetonitrile for 24 hours converts the device behavior to predominantly *n*-type. The device remains ambipolar, as both hole and electron transport is observed, but now the electron transport is more significant [Figure 3-1(B)]. After hydrazine treatment, the I_D-V_{DS} characteristics are linear at low voltages [inset Figure 3-1(B)] and the device on-current I_D is increased by a factor of 40. The electrons accumulate in the NW channel near the source electrode at positive V_{DS} and V_G. Pulling low vacuum (30 mTorr) for an hour on the devices is consistent with removing the hydrazine and recovers the NW FETs predominantly *p*-type characteristics [Figure 3-1(C)]. In order to verify that all the hydrazine was removed, devices were also placed under high vacuum (10^{-8} Torr) overnight and showed no difference in their characteristics from those pumped on under low vacuum. The predominantly *p*-type devices show improved I_D-V_{DS} characteristics [inset Figure 3-1(C)] and increased on-current by a factor of 15 compared to as-aligned PbSe NW FETs. Hydrazine, even though it is subsequently removed, is an aggressive and reducing solvent which may make a more intimate metal-NW interface than that of the as-aligned device. We show that this process is repeatedly reversible as NW FETs can be converted from ambipolar, predominantly *p*- to *n*-type, retaining their high current levels, and back over multiple exposures to 4M hydrazine and removal under vacuum [Figure 3-1(D)]. As shown in FTIR spectra from Chapter 2 [Figure 2-5], hydrazine does not continue to remove significant quantities of surface-bound oleic acid and HD-PVP, but may, as has been proposed, act as Lewis base[1] or hydrazinium cation at the PbSe NW surface, described

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further below. Besides the as-aligned device, all subsequent device characteristics show consistent and reproducible I_D-V_G characteristics, forming ambipolar, predominantly n-type FETs upon exposure to hydrazine and predominantly p-type FETs with vacuum removal of hydrazine, as exemplified by electron and hole on-currents. The devices retain the same threshold voltage (V_T) for electrons and holes when predominantly n- and p-type, respectively. Mobility values for the FETs range from 1-10 cm^{2}V^{-1}s^{-1} using standard FET equations,[10] but are based on the lithographically defined channel widths. Based on SEM images, the NWs sparsely span the junction along its 200 μm width (covering approximately 5% of the channel width); the mobility values should be considered a conservative estimate. The reversibility in the NW FET characteristics has been measured over tens of device structures fabricated at different times on different wafers.

While previous work on as-aligned PbSe NW FETs showed only hole transport,[5] rigorous air-free conditions enable these predominantly p-type devices to also show evidence of electron transport, as seen in the I_D-V_G curves, [Figure 3-1(D)] and the I_D-V_{DS} characteristics in the electron accumulation regime, indicating ambipolar behavior. The I_D-V_{DS} characteristics of ambipolar FETs show at high negative V_G hole accumulation, at high positive V_G electron accumulation, and at moderate V_G and high negative and high positive V_{DS} both electron and hole accumulation in the FET channel. Even after hydrazine treatment, the devices display ambipolar behavior when either predominantly p- or n-type. The asymmetry in the on-currents (I_{ON}) for both electrons

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and holes is only about one order of magnitude when operating both predominantly *p*- and *n*-type devices, even after multiple cycles of hydrazine exposure and removal. Measurement of the NW absorption in the FTIR reveals these 10 nm diameter NWs have a small effective bandgap of 0.45 eV [Figure 3-2(A)]. Given the small effective bandgap of the NWs, small barriers are presented for both hole and electron injection, as the sum of the energy barriers for electron and hole injection is equal to that of the energy gap.[10] Given the similar electron and hole mobilities for PbSe, the observed ambipolar behavior at low doping is anticipated. The small bandgap of PbSe also manifests in a large population of thermally generated carriers at room temperature, giving rise to off currents in the range of 1 to 10 nA for thousands of NWs spanning FET channels. By decreasing the operating temperature of the PbSe NW FET, strong ambipolar behavior is observed with a dramatic increase in the on/off ratio to 10^6 and an increase in both electron and hole mobilities by an order of magnitude [Figure 3-2(B)].
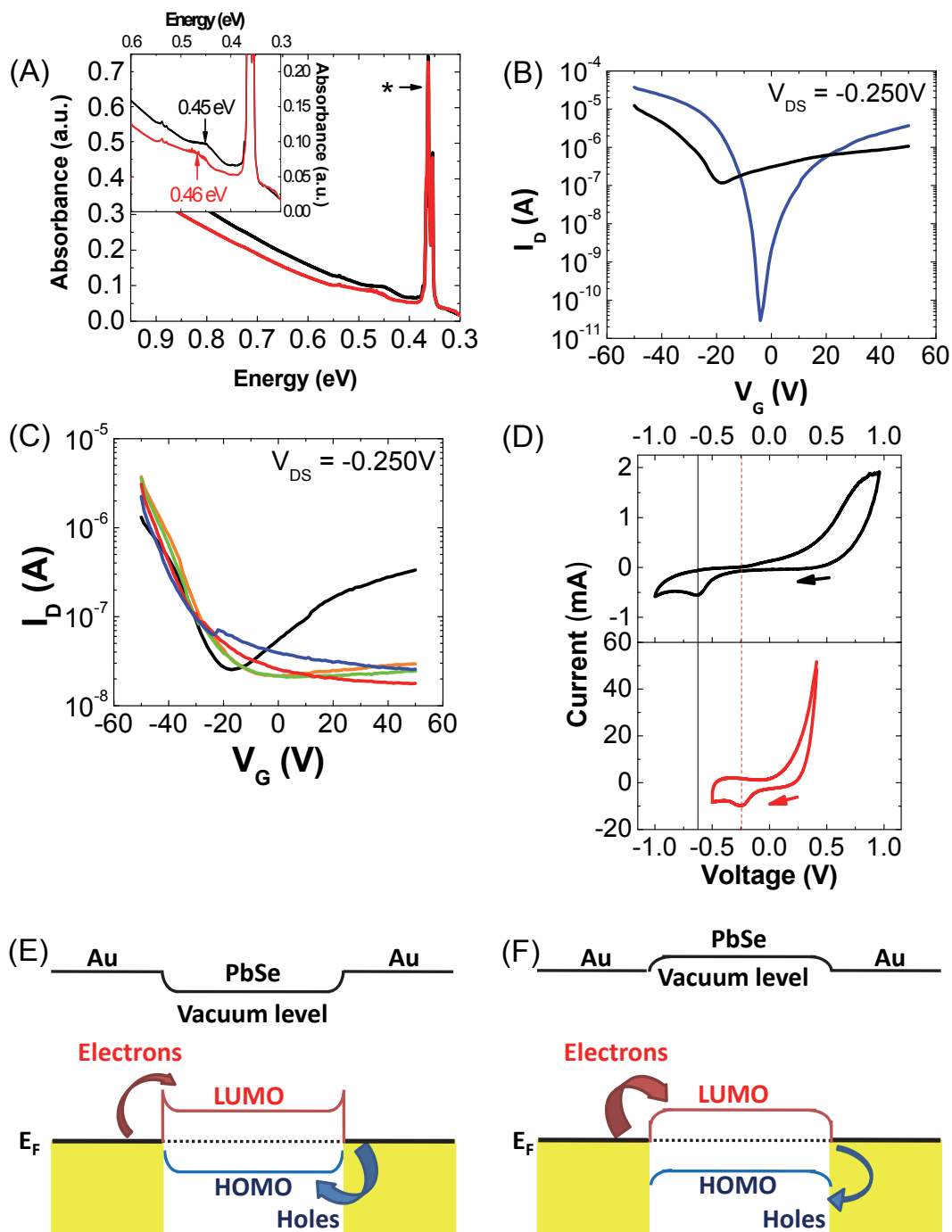
Figure 3-2: (A) Absorption spectrum of dropcast NWs (—) before oxidation and (—) after 10 minute exposure to UV-ozone. (* is from –CH stretches). (B) I_D-V_G characteristics of PbSe NW FETs (—) at room temperature and (—) 77K. (C) Room temperature I_D-V_G characteristics of PbSe NW FETs (—) treated with UV-ozone for (—) 5 seconds (—) 10 seconds, (—) 30 seconds and (—) 60 seconds. (D) Cyclic voltammetry

of PbSe NWs washed in (——) ethanol and (——) subsequently treated in hydrazine. Schematic band diagrams depicting the HOMO, LUMO and vacuum levels and the Fermi energy (E_F) for (E) as-aligned and (F) 4M hydrazine treated PbSe NW FETs.

The intrinsic ambipolar behavior can easily be missed if rigorous air-free conditions are not used to avoid oxidation of the PbSe nanostructures. Oxygen creates acceptor states in PbSe NCs,[11,12] which cause the material to become strongly *p*-type, increasing its hole concentration at the expense of its electron concentration and giving rise to a loss of gate modulation[3,7] in FET devices. PbSe NWs also suffer from the same sensitivity to oxygen as bulk PbSe, which was verified by a blue shift in the NW absorption peak after a ten minute UV-ozone exposure [Figure 3-2(A)]. However, controlled oxygen doping of PbSe NW FETs may serve to be advantageous for enhanced *p*-type characteristics. In order to better understand the role of oxygen, devices were treated under UV-ozone for varying times. Starting with an ambipolar *p*-type PbSe NW FET, we see a significant loss in electron current and a shift in the threshold voltage to more positive voltages even after a short 5 second UV-ozone exposure [Fig. 2(C)], highlighting the importance of air-free conditions in observing the intrinsic PbSe NW character. We see further improvement in the *p*-type characteristics for UV-ozone treatments up to 10 seconds, but subsequent UV-ozone treatments longer than 10 seconds cause the predominantly *p*-type PbSe NW FET to degrade in performance and to suffer poor gate modulation, similar to degradation reported for PbS NCs in solar cells.[13] Gold also forms a thin oxide upon exposure to UV-ozone, which acts to increase the metal work function by up to 0.16 eV at room temperature[14] and favors hole

injection. However, we observed the electron transport can be recovered after re-immersing the devices in a 4M hydrazine solution overnight. Gold oxide is unstable in solvent and will be removed[15] and the NW surface is expected to be reduced by hydrazine.[1] By controlling the UV-ozone exposure time of the NW FET, it is possible to control the degree of *p*-type behavior seen in PbSe FETs, ranging from predominantly *p*-type ambipolar to unipolar *p*-type.

Both optical [Figure 3-2(A)] and cyclic voltammetry (CV) measurements [Figure 3-2(D)] were used to characterize the absolute energy levels of the PbSe NWs before and after hydrazine treatment. The potential was recorded against the oxidation peak of ferrocene/ferrocenium (Fc/Fc$^+$) redox couple, which has a reported highest occupied molecular orbital (HOMO) energy level of –4.80 eV and served as an external standard in our system.[16] The first reduction peak was used to calculate the lowest unoccupied molecular orbital (LUMO) level, while the HOMO was evaluated using the optical energy gap from FTIR absorption spectroscopy (0.45 eV). Differences in the absolute potential levels of the PbSe NWs are in reference to the Pt electrode, which mimics the change that is observed against Au contacts. Based on the reduction peak for untreated NWs at -0.63 V and hydrazine treated NWs at -0.24 V, we can estimate LUMO/HOMO levels for untreated and hydrazine treated NWs to be 4.17/4.62 eV and 4.56/5.01 eV, respectively. While gold has been reported to have a work function of around 5.1 eV, this energy level can only be attributed to high purity clean gold under ultra-high vacuum (UHV). Outside of vacuum, the surface of gold is readily contaminated, which

can significantly modify its work function to 4.7 eV.[17,18] Since the NWs were dropcast in a nitrogen glovebox rather than in UHV, we expect the gold electrodes to be dirty. Based on the more favorable band alignment of the untreated PbSe HOMO level (4.62 eV) with the work function of the dirty gold contact, the predominantly *p*-type behavior of the as-aligned NW FETs may be attributed to band bending promoting hole injection [Figure 3-2(E)]. The predominantly *n*-type behavior of PbSe NW FETs upon exposure to hydrazine can be attributed to electron transfer from hydrazine to the NW to form $N_2H_4^+$,[19–21] which induces a negative charge and forms an inward-pointing surface dipole. This surface dipole reduces the local metal work function and effectively increases the electron affinity and ionization potential of the HOMO and LUMO levels of PbSe nanostructures,[8,22] shifting the material's LUMO level (4.77 eV) to be more favorable toward electron injection [Figure 3-2(F)]. This process is reversible in PbSe nanostructures and once the sample is under vacuum for a period of time, the hydrazine is removed and the work function returns to favor hole injection and suppress electron injection.

3-2: Isolating the Metal-PbSe Nanowire Contacts

To further understand and isolate the role of the metal/semiconductor junction on the measured electrical properties of NW FETs, a SiO_2 "blocking layer" was fabricated on top of 19 μm of the 20 μm NW channel to selectively dope 0.5 μm of the NW at the NW-source and drain interfaces [Figure 3-3(A, B)]. All methods to fabricate the blocking

layer were carried out in air-free conditions, as rigorously as possible. All e-beam resists and developers were degassed and used inside an MBraun nitrogen glovebox. An e-beam resist bilayer of 495 poly(methyl methacrylate) (PMMA) A4 (MicroChem) and 950 PMMA A4 (Microposit) was spincast and baked under nitrogen at 180 $^{\circ}$C for 2 minutes for each layer. The PMMA coated device was secured in a jar under nitrogen in the glovebox and taken to the e-beam lithography tool (Elionix ELS-7500EX), where the blocking layer was exposed. After exposure, the sample was developed in the glovebox with methyl isobutyl ketone in isopropyl alcohol (MIBK: IPA 1:3, Honeywell Burdick and Jackson). E-beam evaporation of the 50 nm SiO_2 blocking layer was carried out in a nitrogen glovebox with an integrated evaporator, followed by lift-off with anhydrous acetone. In fabricating the SiO_2 blocking layer, experiments were performed at each processing step, through lithography and SiO_2 evaporation, to ensure the integrity of the NW FETs remained unaffected. There were no signs of NW sintering or growth, as verified by scanning electron microscopy, which is consistent with reported heat treatments of PbSe NC films that show electrical characteristics and conductivity that remain essentially unchanged from the as-made films when heated to 200°C for an hour.[3] The e-beam resist developer MIBK:IPA suppressed the device's electron current, but pulling high vacuum (10^{-8} Torr) on the sample recovered the ambipolar behavior, as shown by the I_D-V_G curve after SiO_2 evaporation [Figure 3-3(C)].

(A)

(B)

(C) V_{DS} = 0.250 V

I_D (A)

V_G (V)
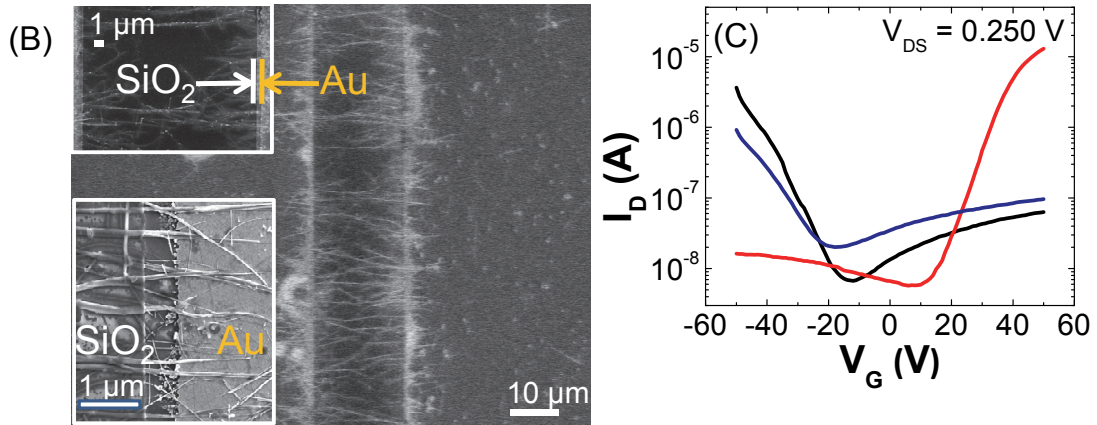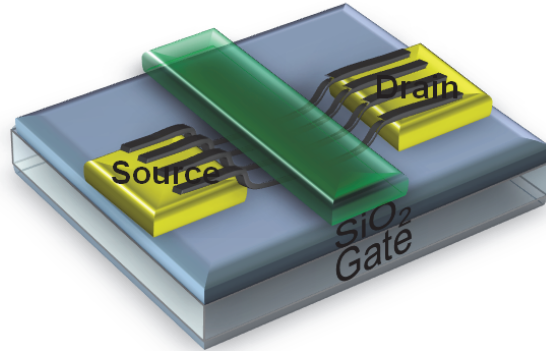
Figure 3-3: (A) Schematic of PbSe NW FET with top insulating SiO_2 blocking layer. (B) SEM of blocking layer atop the PbSe NW FET and inset, higher resolution images. (C) I_D-V_G characteristics following the conversion of the NW transport behavior when only modifying the NW-metal junction corresponding to the FET upon: (—) fabricating the blocking layer, (—) immersing in 4M hydrazine and (—) pulling vacuum.

The predominantly p-type, ambipolar FET behavior remained intact after fabrication of the blocking layer [Figure 3-3(C)]. Immersing the device in 4M hydrazine in acetonitrile for 24 hours still converted the device to predominantly n-type characteristics. Upon removing the hydrazine under vacuum, the device regained its predominantly p-type behavior. For predominantly n- and p-type FETs, the current

levels are similar to those for NW FETs without the blocking layer, upon exposure and removal of hydrazine and show reversible transport behavior by modifying only the contact region. Different blocking layer lengths of 18 and 16 μm were also fabricated on top of the 20 μm channel, creating 1 μm and 2 μm gaps at the source and drain contact regions. The device current levels for the FETs when exposed to hydrazine and when hydrazine is removed, is invariant with the size of the gap at the electrodes, despite the exposure and removal of more of the NWs length to hydrazine. Polarity switching of the majority carrier in FETs from hole to electron transport (from p-type to n-type) by selectively exposing the NW-metal junction and the changes in HOMO and LUMO energies extracted from cyclic voltammetry measurements show that the energy level alignment at the metal-nanostructure contact governs the measured device behavior.

Using 4M hydrazine, we were unable to achieve completely n-type unipolar devices. Therefore PbSe NW FETs were immersed in higher concentrations of hydrazine in acetonitrile [Figure 3-4(A)] to see if the devices could be more strongly n-doped. Without a blocking layer present, immersing the device in 8M hydrazine completely turned off the ambipolar behavior and converted the FET to fully n-type, shifting V_T more negative. By controlling the hydrazine concentration used to charge transfer dope the NW FETs, it is possible to control the degree of electron transport seen in the device, ranging from ambipolar, predominantly n-type to unipolar n-type behavior. On the other hand, using an SiO_2 blocking layer to protect the NW channel and exposing only the contacts to 8M hydrazine [Figure 3-4(B)], the device characteristics were still

ambipolar, predominantly *n*-type. These results show that only modifying the band

level alignment at the PbSe-metal junction is not sufficient to make a unipolar device.

Since PbSe is a small bandgap material, simply shifting the interface dipole without

changing the material's intrinsic carrier concentration is not enough to suppress its

inherent ambipolar characteristics because PbSe NW FETs will always have small

barriers to both electron and hole injection. The only way to fabricate a unipolar device

is to change the bulk carrier concentration by increasing the electron concentration at

the expense of the hole concentration, similar to our fabrication of unipolar *p*-type

devices using oxygen exposure [Figure 3-2(C)]. The PbSe FET without a blocking layer

upon exposure to 4M hydrazine still exhibits ambipolar behavior. At low to moderate

doping densities, contact modification dominates the measured transport

characteristics and the bulk carrier concentration has not been significantly affected.

Given that PbSe has a high population of thermally generated carriers, it is necessary to

dope at high concentrations (above the level achieved with 4M hydrazine) to

significantly impact the intrinsic carrier density and achieve unipolar transport. Figure 3-

4(C) shows a schematic band diagram for PbSe NW FETs modified with 8M hydrazine.

Both devices with and without blocking layers treated in 8M hydrazine can be returned

back to their predominantly *p*-type state under low vacuum for an hour. Immersing the

device in 12M hydrazine ruined the devices, since hydrazine is a caustic base and has

been shown to dissolve lead chalcogenides at high concentrations.[23,24]
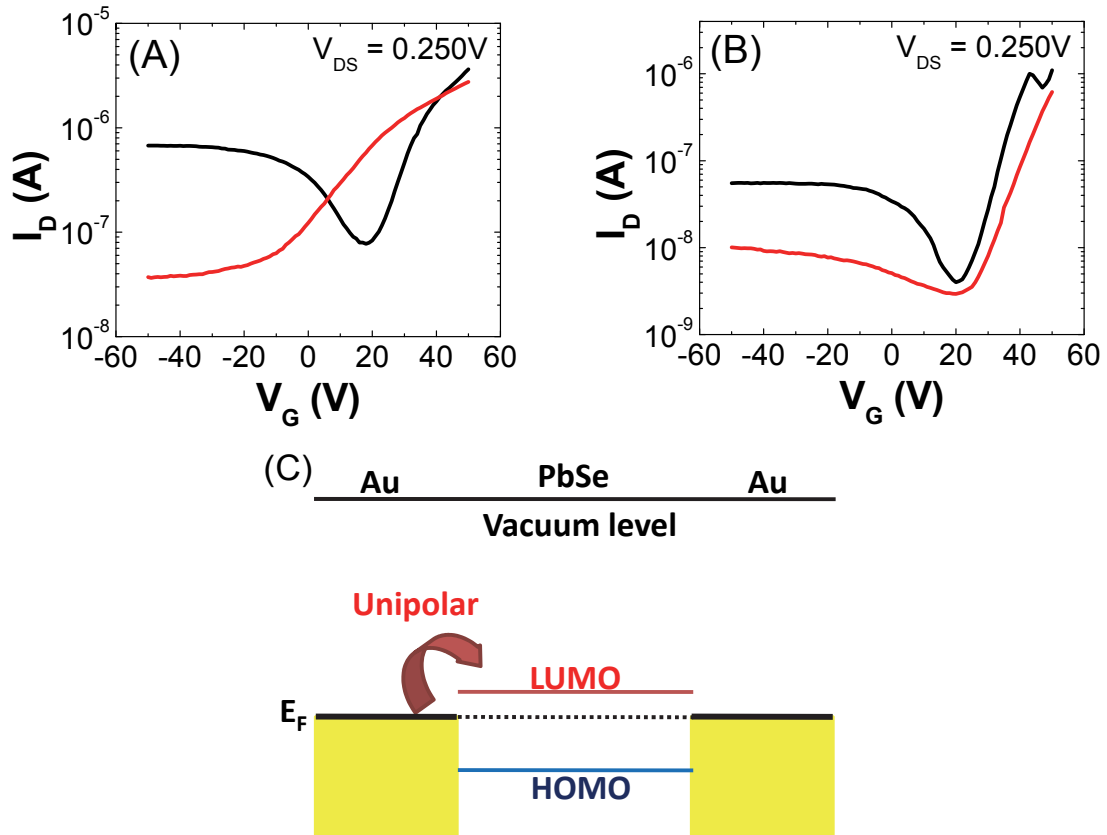
Figure 3-4: I_D-V_G characteristics of PbSe NW FETs treated with (━) 4M and (━) 8M hydrazine (A) without and (B) with a blocking layer. (C) Schematic band diagram depicting the HOMO, LUMO and vacuum levels and the Fermi energy (E_F) for 8M hydrazine doped PbSe NW FETs. Note the influence of 8M hydrazine on the magnitudes of the doping levels and interface dipole are not known quantitatively.

By taking advantage of the control we have over the PbSe device behavior, we fabricated bottom-contact inverters using a unipolar *p*-type FET (treated with 10 seconds UV-ozone) and a unipolar *n*-type FET (treated with 8M hydrazine) [Figure 3-5(A, B)]. The gates of the FETs were connected and used as the input of the inverter. These

are the first reported PbSe NW inverters which exhibit promising gains of ~8 for both

positive and negative V_{DD}.
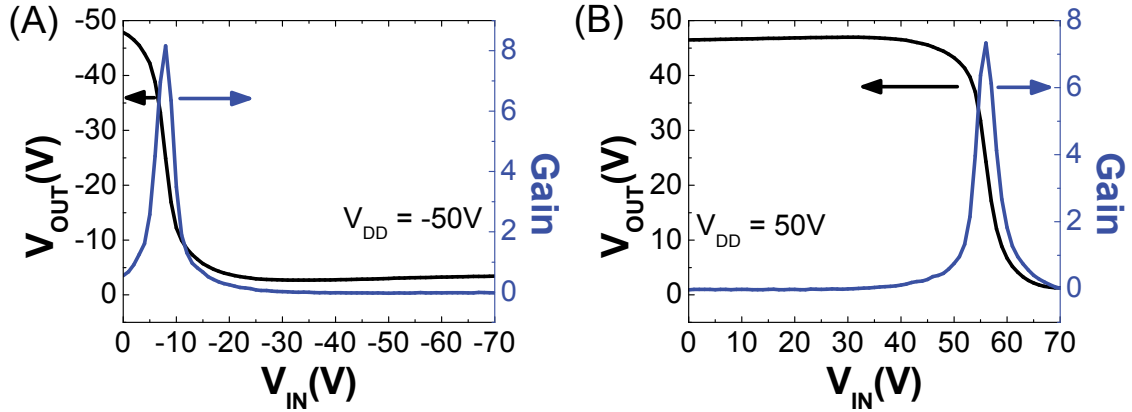
Figure 3-5: Transfer and gain characteristics of inverters constructed from unipolar *p*
and *n*-type PbSe NW FETs at (A) negative and (B) positive V_{DD}.

3-4:   Conclusions

In summary, we were able to show surface treated, bottom-contact PbSe NW

FETs with controllable and reversible device characteristics (V_T, I_{ON}), ranging from

oxygen treated unipolar *p*-type, ambipolar, to high hydrazine concentration treated

unipolar *n*-type. The fabrication processes we developed for the blocking layer

successfully preserved the intrinsic properties of these very oxygen and water sensitive

nanomaterials and we believe it can be used for a variety of other air sensitive materials

and more complicated devices, such as top gate and other dual gate configurations.

Selectively treating the contacts reversibly changes the predominant measured carrier

to holes or electrons, exhibiting the dominating role the metal-semiconductor NW

contacts have on charge injection in these devices at low to moderate doping

concentrations. The changes in band alignment are also consistent with cyclic

voltammetry measurements and reflect the importance of interfacial doping on charge

injection in FETs for nanostructured materials. Since PbSe is a small bandgap

semiconductor with a small barrier for both electrons and holes, the device's ambipolar

characteristics can only be suppressed by modifying the high number of thermally

generated carriers at high doping concentrations. As a development of this work,

measurements of PbSe single nanowire FETs to liquid helium temperatures have been

explored to quantitatively characterize charge injection and transport for different

surface modifications and concentrations.[25] By taking advantage of the control we have

over the electronic properties in PbSe NW FETs, we fabricated the first PbSe NW

inverters that show amplification and the promise of these nanostructured materials in

more complex integrated circuits.

3-5:   *References*

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CHAPTER 4: Dielectric Interface to Control Hysteresis and Flexible Integration[3]

Large hysteresis has been observed in both colloidal PbSe nanowire (NW) and nanocrystal (NC) field-effect transistors (FETs),[1–6] and more broadly in other colloidal semiconductor NW and NC FETs,[7–10] and is limits fundamental studies of charge transport, device performance and application in more complex, integrated circuits. While it is widely believed that the presence of surface-bound water that hydrogen-bonds to the silanol groups on the silicon dioxide (SiO_2) gate dielectric surface is principally responsible for hysteresis in carbon nanotube (CNT),[11,12] organic,[13,14] ZnO NW,[15] and Si NW FETs,[16,17] hydroxyl passivated and dehydrated PbSe NC[2,3] and NW devices show no significant improvement in the large hysteresis. It has been reported that coating single CNT devices with cured poly(methyl methacrylate) (PMMA) down to the gate dielectric surface nearly eliminates hysteresis.[11,18] This has been attributed to several key factors: 1) curing the PMMA releases surface bound water on both the dielectric and nanotube surfaces that causes hysteresis, 2) the carbonyl groups in PMMA can bond with the silanol groups on SiO_2 and 3) PMMA is hydrophobic and both (2) and (3) keep water from being re-adsorbed, preventing hysteresis from readily returning.

We show a similar reduction in hysteresis for PbSe NW FETs fabricated atop SiO_2 gate dielectric layers thermally grown on a Si back-gate when encapsulated in PMMA, providing a model system to understand more generally how to reduce hysteresis in

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[3] Much of this chapter appears in print: Adapted with permission from D. K. Kim, Y. Lai, T. R. Vemulkar, C. R. Kagan, *ACS Nano*, **5** (12) 10074 - 10083, 2011. Copyright 2011 American Chemical Society.

FETs from colloidal nanostructures. Unlike NC FETs, which are additionally complicated by interparticle spacing and film cracking, which may give rise to trap sites within the semiconductor active layer,[1–3,10] single crystalline colloidal NW FETs are an ideal system to investigate the role of charge transport[19] and the influence of device interfaces on hysteresis. Similar to CNT FETs, we show that the reduced hysteresis in PbSe NW FETs encapsulated in PMMA is consistent with unique hydrogen bonding that occurs between the hydroxyl terminated surface of the SiO_2 gate dielectric layer and the carbonyl group in PMMA.[11,20,21] PbSe NWs aligned *via* electric field assembly only span approximately 5-10% of the device channel, so PMMA can both encapsulate individual NWs and penetrate to the gate dielectric surface to interact with the hydroxyl groups in reducing hysteresis. However since most colloidal NC films deposited by various techniques form uniform and continuous thin films (spincasting[3,6], dip-coating[2] and dropcasting[5]), deposition of a top PMMA coating would be ineffective as PMMA would not penetrate to the SiO_2 interface needed to reduce trapping at the semiconductor-dielectric interface. Further, since PMMA cannot withstand the solvents and chemical treatments used in the deposition of many NC materials and in their doping, it is necessary to develop a robust bottom gate dielectric stack that does not require PMMA as a passivating layer.

In Chapter 4, we report bottom gold contact PbSe FETs atop a range of gate dielectric materials and show hysteresis is consistent with carrier trapping at the *semiconductor-gate dielectric interface*. Despite heat treatments and the use of

hydroxyl-free dielectric layers, large hysteresis is observed on hydrophillic silicon nitride (SiN) and hydrophobic polymer surfaces, indicating that surface water and charge-trapping hydroxyl groups in PbSe NW FETs are not solely responsible for the observed hysteresis. By modifying the gate dielectric surface chemistry we fabricate ambipolar predominantly *p* and predominantly *n*-type FETs with dramatically reduced hysteresis. We have identified a surface modified gate dielectric stack, assembling octadecylphosphonic acid (ODPA) on aluminum oxide (Al_2O_3) that allows low hysteresis FET operation. Further, by implementing this device geometry on flexible substrates, we show low hysteresis and low voltage operation on plastics and the promise of integrating these materials in complex integrated circuits.

4-1:   Encapsulation with Poly(methyl methacrylate) (PMMA)

Wet-chemically synthesized, straight single crystalline PbSe NWs approximately 10 nm in diameter[19] were aligned under an electric field of 10^4 to 10^5 V/cm between gold source and drain contacts to form FETs. FETs with channel lengths of 20 μm were fabricated atop 250 nm of silicon dioxide thermally grown on highly *n*-doped silicon wafers, serving as the gate dielectric layer and back-gate of the FETs, respectively. NW FETs were well washed in ethanol and chloroform to remove surface bound ligands, since insufficient cleaning leads to poor current modulation. Devices were then treated with 4.0M of hydrazine overnight to increase the current levels and reduce contact resistance to become predominantly *n*-type, and reverted back to predominantly *p*-type

by pulling low vacuum (30 mTorr) for an hour.[19] Post-hydrazine treated PbSe NW FETs

exhibit both hole and electron transport, but stronger hole transport gives rise to

predominantly *p*-type ambipolar behavior. Rigorous air-free conditions were used from

synthesis, purification, characterization and device fabrication to prevent unintentional

oxidation of the NWs, which has been shown to suppress the electron current[1,22,23] and

inherent ambipolar[19] behavior in PbSe nanostructures as oxygen creates acceptor states

in PbSe, effectively acting as a *p*-dopant.

PMMA 495 A4 (4wt% PMMA in anisole from MicroChem) was degassed, brought

into the glovebox and 180 nm film was spincast atop predominantly *p*-type ambipolar

PbSe FETs and baked in inert atmosphere at 180°C for 2 minutes to cure completely

[Figure 4-1(A)]. The drain current (I_D) *versus* gate voltage (V_G) characteristics show that

the originally predominantly *p*-type device with hysteresis of 30V became a

predominantly *n*-type device with reduced hysteresis of 15 V [Figure 4-1(B)]. Device

hysteresis is evaluated from the difference in threshold voltage (V_T), calculated as the

intercept in a linear fit of the I_D-V_G curve, for each sweep direction in V_G. Devices coated

with PMMA retained the reduced hysteresis of 15 V over several weeks, but the charge

transport characteristics shifted from predominantly *n*-type back to predominantly *p*-

type over time, which is discussed further in the next section. Removal of the PMMA

with acetone returned the device to its original *p*-type behavior with large hysteresis of

30V, as evidenced by the similar I_D-V_G curves before and after PMMA encapsulation,

showing that the effects of PMMA are completely reversible. Subsequent spin-casting,

heating and removal with acetone cycles have been repeatedly performed with independently fabricated devices from multiple synthetic batches of NW solutions and are shown to be consistently reversible and repeatable.
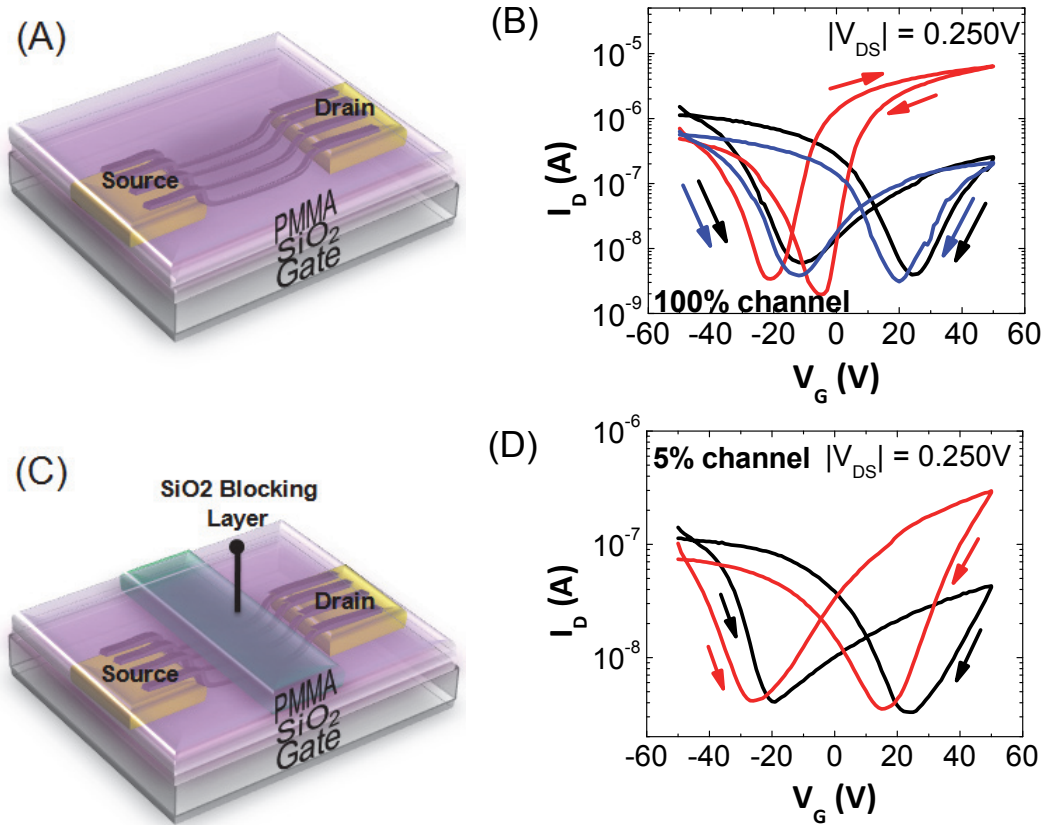
Figure 4-1: (A) Schematic of a PbSe NW FET with PMMA spincast on top and subsequently cured at 180˚C for two minutes. (B) I_D-V_G characteristics for a PbSe NW FET uncoated (**black**), with PMMA spincast and cured at 180 ˚C for two minutes (**red**) and with PMMA subsequently removed with acetone (**blue**). (C) Schematic of a PbSe NW FET with a SiO_2 blocking layer covering 95% of the NW channel and PMMA spincast on top and subsequently baked at 180 ˚C for two minutes.   (D) I_D-V_G characteristics of a PbSe NW FET with a SiO_2 blocking layer covering 95% of the NW channel uncoated (**black**) and with PMMA spincast on top covering the remaining exposed 5% of the channel at the source and drain contact regions and cured at 180 ˚C for two minutes (**red**).

For PbSe NW FETs, the reduction in hysteresis even occurs if the sample were not pre-treated in 4M of hydrazine, which has been shown to improve the current levels and dope the contact regions at these concentrations,[19] (Chapter 3) indicating that charge transfer doping of the semiconductor/metal interface is not responsible for hysteresis reduction.   To test whether the contacts or bulk were responsible for hysteresis reduction, a 50 nm thick SiO_2 blocking layer was fabricated, with rigorous air-free techniques,[19] on top of 19 μm of the 20 μm channel to selectively encapsulate 0.5 μm of the NW with PMMA at the NW-source and drain interfaces [Figure 4-1(C)]. The I_D-V_G characteristics show that the hysteresis remains unchanged when selectively encapsulating only the contacts [Figure 4-1(D)]. Using a different blocking layer length of 18 μm to selectively encapsulate 1.0 μm of the NW at each of the source and drain contacts with PMMA shows a more noticeable reduction in hysteresis. The reduction is not as significant as when 100% of the channel was passivated with PMMA, indicating that the semiconductor NW-gate dielectric interface dominates hysteresis in these devices. Measuring devices at lower temperatures also reduced hysteresis in PbSe NW FETs similar to PbSe NC FETs,[6] suggesting that the observed hysteresis is temperature dependent.

Unlike CNT FETs, which were encapsulated in PMMA in atmosphere, all encapsulations of PbSe FETs had to be done under the inert conditions of the nitrogen-filled glovebox due to the sensitivity of PbSe NWs to oxygen. Even with devices already

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passivated with PMMA, exposing the NW FETs to atmospheric conditions immediately increased the hysteresis to large values and made the FETs unipolar *p*-type, losing their electron current and therefore ambipolar behavior. Interestingly, upon removal of the PMMA with anhydrous acetone in the glovebox, the devices were returned to their original ambipolar predominantly *p*-type behavior despite being exposed to atmosphere for six hours; in contrast exposure of unpassivated NW FETs leads to irreversible oxidation and changes in the FET characteristics. This indicates that PMMA may be a sufficient blocking layer to prevent irreversible oxidation of the NWs, suggesting that short exposure to atmosphere of PMMA coated structures may allow e-beam lithography to provide a good route to fabricate advanced device structures while preserving the intrinsic properties of very oxygen and water sensitive nanomaterials.

4-2:   The Effect of Oxygen on PbSe NWs

We investigated the polarity switching (from ambipolar predominantly *p*- to *n*-type) observed upon encapsulating the PbSe NW FETs in PMMA. We confirmed that PMMA from different sources had no unintentional impurities that could lead to the observed *n*-type conversion and PMMA of varying molecular weight displayed nearly identical I_D-V_G behavior. Since the NW FETs are heated during the curing of PMMA, we studied the role of heating and cooling alone on the electrical behavior of the FETs. Without any PMMA encapsulant, heating the original, ambipolar predominantly *p*-type PbSe FET for two minutes at 180°C converted the device to ambipolar predominantly *n*-

type behavior. Devices that were heated for two minutes between 50°C to 180°C show a clear transition, with the electron current increasing and the hole current decreasing with increasing annealing temperatures, becoming equally ambipolar around 150°C and then predominantly *n*-type at higher temperatures [Figure 4-2(A)], for the same 2 minutes of annealing. Samples that were heated for an hour between 100°C and 180°C show a similar trend in both the electron and hole currents, indicating that the polarity switching happens within the first two minutes of heating [Figure 4-2(A)]. Twenty-four hours after removing the device from heat, the predominantly *n*-type character converted back to its original predominantly *p*-type behavior [Figure 4-2(B)], similar to devices coated in PMMA. Both the log of the electron and hole current levels change linearly over the log of the time. Conversion of the device characteristics upon heating and cooling was carried out consecutive times on the same device, and found to yield similar current levels. Similarly, re-heating/cooling PMMA coated samples would switch the polarity of the FET behavior.
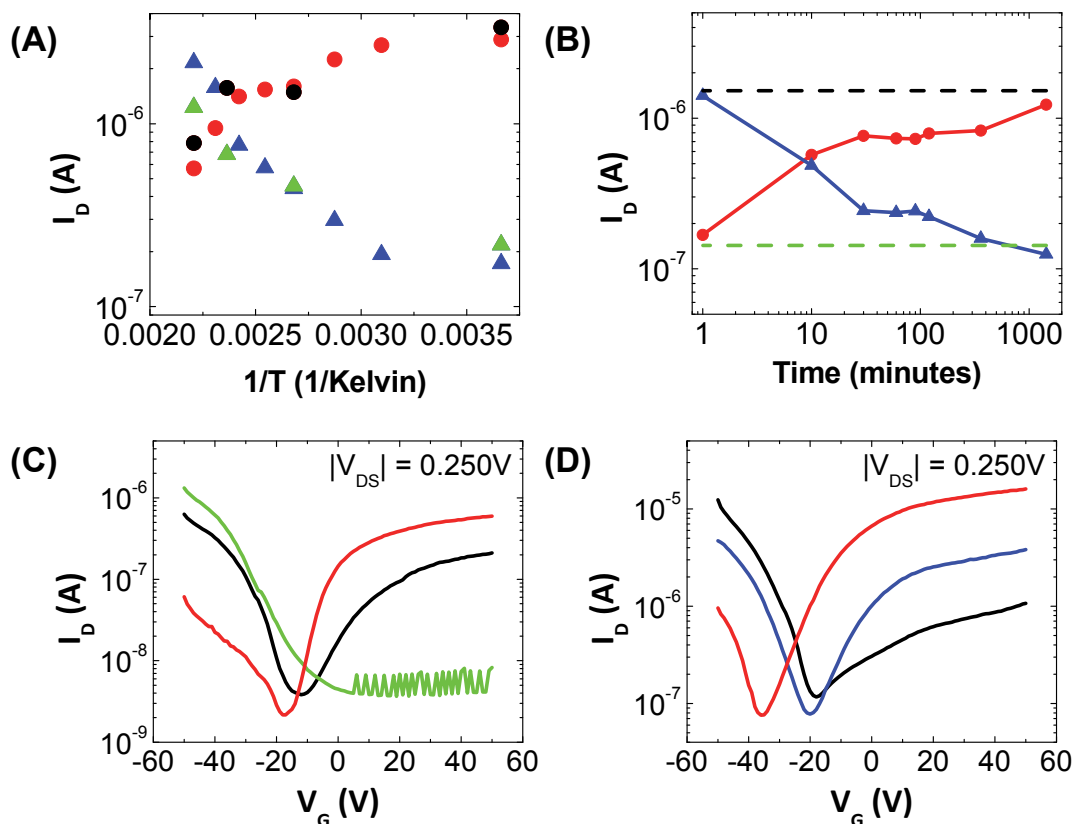
Figure 4-2: (A) On currents at $|V_G|$ = 50V for electrons as a function of annealing temperature for 2 minutes (**blue**) and 60 minutes (**green**), and for holes for 2 minutes (**red**) and 60 minutes (**black**). (B) Time evolution of electron (**blue**) and hole (**red**) on currents over 24 hours after cooling, as well as original currents levels before heating for electrons (**green dash line**) and holes (**black dash line**). (C) I_D-V_G characteristics of PbSe NW FETs before treatment (**black**), 10 second UV-ozone exposure (**green**) and heating at 180°C for 2 minutes (**red**). (D) I_D-V_G characteristics of PbSe NW FETs before vacuum (**black**), 1 day under vacuum (**blue**), and 2 days under vacuum (**red**).

PbSe is extremely sensitive to oxygen exposure. Even at low exposure levels of

5.3 x 10^{-3} Torr (<10 ppm), oxygen has been shown to adsorb on the surface of PbSe

nanostructures reversibly to dope it *p*-type.[1] Therefore, it can be expected that even

when storing air-free synthesized PbSe nanostructures inside a nitrogen glovebox, small

traces of oxygen are enough to *p*-dope it over time until the surface is saturated with

adsorbed oxygen to favor ambipolar predominantly *p*-type behavior. This is different

from the irreversible exposure at higher oxygen concentrations around 0.87 Torr[1]

(>1000 ppm), where oxygen will form covalent bonds with the NW surface and possibly

the bulk and lead to formation of permanent lead-selenide-oxides that suppress

electron currents.[24,25] Annealing PbSe NWs in a nitrogen glovebox may provide enough

energy to desorb the surface-bound oxygen that is acting as an unintentional *p*-type

dopant. PbSe thin films and crystalline powders have been reported to desorb surface

oxygen upon heating in vacuum, giving rise to changes in semiconductor conductivity

and type.[26,27] To test whether heat desorbs the oxygen on the surface of PbSe NWs,

samples were exposed to UV-ozone for 10 seconds, which has been demonstrated to

intentionally and controllably oxygen dope PbSe NWs to form unipolar *p*-type FETs[19] and

PbS NC solar cells.[28] Heating the oxidized PbSe NW FET in the glovebox returned the

device's electron current [Figure 4-2(C)], showing the oxygen-effect to be reversible

with heat.

The increase in electron current at the expense of the hole current with

increasing temperature [Figure 4-2(A)], suggests the Fermi level shifts as the *p*-doping

level is reduced and oxygen is desorbed. Using the changes in electron and hole

currents with temperature, assuming an Arrhenius activated energy process,[29] we find

an activation energy of ~0.2-0.3 eV for the desorption of oxygen. Differences in electron

and hole trapping and injection may give rise to variations in threshold voltages and

therefore the calculated activation energies. These results indicate that after oxygen

desorption PbSe NW FETs are ambipolar predominantly *n*-type FETs, which can be attributed to two factors. First, it was reported that exposing PbSe NCs to nitrogen reversibly converts it *n*-type,[1] which may contribute to the switch in carrier transport after annealing since the PbSe NW surface is now accessible to nitrogen-doping. Second, PbSe is known to be extremely sensitive to deviations in stoichiometry. Studies of single crystal powders and thin films have shown PbSe with excess lead forms an *n*-type semiconductor, whereas with excess selenium forms a *p*-type semiconductor.[27,30–33] It has been reported in the literature that colloidal PbSe NCs are characterized by an excess of lead on their surface.[34,35] Since NWs are formed through oriented attachment of many colloidal PbSe NCs,[36] it is likely that colloidal PbSe NWs may exhibit an excess of lead, favoring predominantly *n*-type behavior.

Upon removing the NW FETs from heat, over the next 24 hours, trace amounts of oxygen reversibly adsorb to the NW surface to return it to predominantly *p*-type behavior. Since devices were kept in a glovebox with low oxygen content, it may take considerable time to adsorb enough oxygen to become reversibly *p*-doped. We estimated in a glovebox with O_2 levels of 0.1 ppm, it would take approximately 20 hours to adsorb a monolayer of oxygen, using rates of oxygen uptake at room temperature from early studies of PbSe single crystal powders[37] and accounting for the differences in PbSe surface area and oxygen pressure. This agrees well with both our experiments [Figure 4-2(B)] and literature report on oxygen re-adsorption times of 20-24 hours upon cooling for PbSe thin films in vacuum.[26] PbSe NW FETs placed and measured under high

vacuum (10^{-7}-10^{-6} Torr) showed a slow conversion to predominantly *n*-type behavior [Figure 4-2(D)], indicating that adsorbed oxygen is slowly desorbed from the PbSe NW surface, similar to ethanedithiol (EDT)-treated PbSe NCs that exhibit ambipolar predominantly *n*-type transport when measured in vacuum.[1]   However, due to the extreme sensitivity of PbSe to oxygen, even inside a nitrogen glovebox, in most cases PbSe nanostructures would preferentially exhibit hole transport.

4-3:   Modifying the Dielectric Surface to Reduce Hysteresis

It is widely believed that the presence of surface-bound water that hydrogen-bonds to the silanol groups on the SiO_2 gate dielectric surface is principally responsible for hysteresis in CNT,[11,12] organic,[13,14] ZnO NW,[15] and Si NW FETs.[16,17] By encapsulating PbSe NW FETs in PMMA, the baking process to cure the PMMA should desorb the surface bound water and the hydrophobic nature of the PMMA coating would ideally prevent water re-adsorption. The surface-bound water on SiO_2 is also known to trap electrons,[38,39] which is evident in lower electron currents in FETs of a wide-range of materials. Therefore, eliminating surfaces that are easily hydrated (such as hydroxyl groups) or annealing the PbSe NW FETs should remove the surface bound water and cause a reduction in hysteresis and increase of electron current, even without the use of PMMA. We modified the SiO_2 gate dielectric with two commonly used methods to eliminate the surface adsorbed water.

First, prior to electric field alignment of the NWs, all SiO_2 substrates were treated with hexamethyldisilazane (HMDS) prior to electric field alignment. By passivating the polar silanol groups with trimethylsilyl-terminated groups, the surface exhibits a lower affinity for adsorbed water,[2,3,40] which should reduce the density of charge traps and the hysteresis. However, as reported with PbSe NCs,[2–4] surface modification of SiO_2 with HMDS did not cause a significant reduction in the hysteresis, especially when compared to devices passivated with PMMA [Table 4-1].   It has also been reported that octadecyltrimethoxysilane (OTMS) treated PbSe NC FETs exhibit large transients at room temperature.[6]

Treatment	SiO_2 +HMDS (250 nm) ΔV_T [Volts]	SiN Untreated (35 nm) ΔV_T [Volts]	Polyimide (180 nm) ΔV_T [Volts]	Parylene (250 nm) ΔV_T [Volts]	Al_2O_3 Untreated (20 nm) ΔV_T [Volts]	Al_2O_3+ODPA (20 nm) ΔV_T [Volts]
Aligned and EtOH	41.7 ± 12.7	60.7 ± 7.4	60.9 ± 10.2	32.5 ± 6.7	58.2 ± 5.10	32.1 ± 10.4
24 hours after Heating	39.4 ± 7.0	41.8 ± 6.2	58.8 ± 10.8	27.6 ± 3.4	38.4 ± 8.14	10.0 ± 7.0
PMMA	15.3 ± 7.5	27.5 ± 2.4	39.4 ± 5.5	33.7 ± 2.4	19.1 ± 1.0	6.6 ± 2.3

Table 4-1: Hysteresis for PbSe NW FETs fabricated with different gate dielectric stacks on top of 250 nm thermally grown SiO_2 and with surface modified gate dielectric surfaces.

Second, it has been reported that water-bound to silanols on SiO_2 can be removed by heating in dry environments at temperatures of 150^oC or above.[41]   More recent studies have suggested that temperatures of 200^oC[11,40] are needed to fully

dehydrate the SiO_2 surface, hence devices were also heated under vacuum (<0.1 Torr) for six hours at $200^{\circ}C$ as a comparison. The extended vacuum $200\ ^{\circ}C$ heat treatment yielded hysteresis values similar to that for devices only heated for 2 minutes in a glovebox at $180^{\circ}C$, indicating that the majority of water desorption occurred in the first few minutes of annealing PbSe NW FETs in inert atmosphere. Devices that were measured 24 hours after heating exhibited slightly reduced hysteresis and enhanced electron currents, suggesting that dehydration or HMDS passivation are not enough to significantly reduce the large hysteresis [Figure 4-3(A) and Table 4-1]. Since SiO_2 surfaces inherently have hydroxyl groups that can be easily saturated with surface bound water, we replaced the SiO_2 surface with reported hydroxyl-free dielectric surfaces, as described in Chapter 2-2.
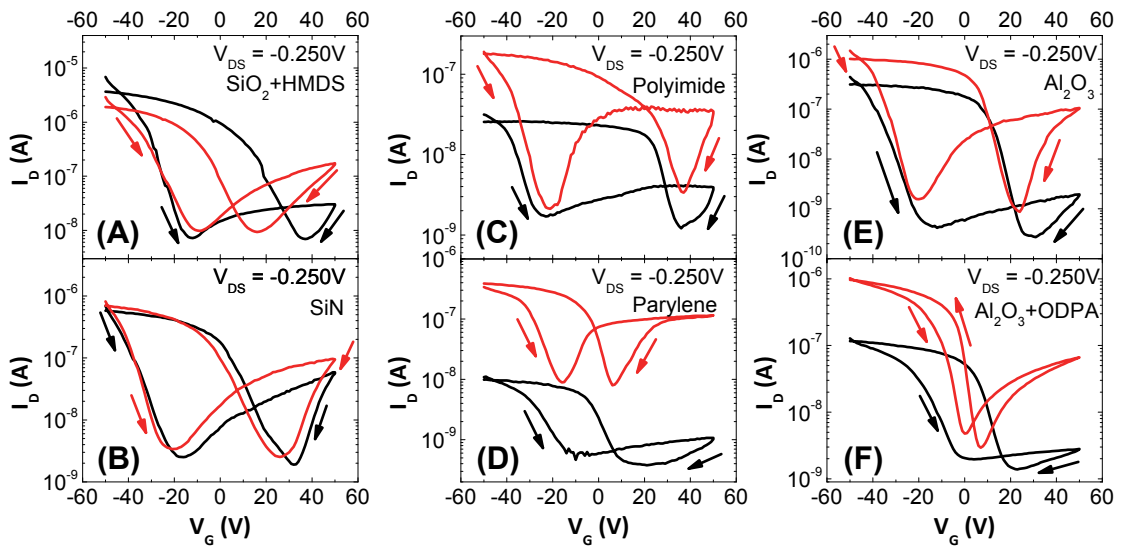
Figure 4-3: I_D-V_{DS} of PbSe NW FETs fabricated with (A) SiO_2, (B) SiN, (C) polyimide, (D) parylene, (E) Al_2O_3 and (F) octadecylphosphonic acid (ODPA) functionalized Al_2O_3 gate dielectric stacks on top of 250 nm thermally grown SiO_2 before (**black**) and 24 hours after heat treatment at $180^{\circ}C$ for 2 min. (**red**). Note: the current levels in each device

differ as the gate dielectric capacitance and number of nanowires spanning the channel are not the same.

Hydroxyl-free hydrophilic SiN,[42,43] and hydrophobic polyimide[44,45] and parylene[39,46] were employed because these surfaces are not hydrated by water molecules that are hydrogen-bonded to silanols as in SiO_2.[40,41] All samples were heated at $180^{\circ}C$ for two minutes to completely remove any residual water after electric field alignment of the NWs and the FETs were washed with ethanol and chloroform to take away ligands on the surface of the NWs. Measurements were done at least twenty four hours after heating to allow devices to return to predominantly p-type character. SiN substrates were left unpassivated because silane reagents have poor adhesion to the surface due to the lack of hydroxyl groups and work effectively when untreated.[47] PbSe NW FETs atop SiN [Figure 4-3(B)] show higher electron currents and therefore more balanced ambipolar behavior, indicative of the lack of hydroxyl groups, especially when compared to HMDS treated SiO_2 [Figure 4-3(A)]. Despite increased electron currents, the devices still exhibited large hysteresis after annealing. SiN devices were further vacuum heated at $180^{\circ}C$ for several hours to remove any remaining surface bound water, but did not yield improved hysteresis. Polyimide and parylene are both hydroxyl-free and hydrophobic substrates, which should present ideal surfaces for reduced hysteresis PbSe NW FETs. Heated polyimide and parlylene FETs yielded electron currents more comparable to hole currents [Figure 4-3(C, D)] than SiO_2/HMDS FETs, once again indicative of the lack of water-binding hydroxyl groups present on the surface that may act as electron trapping sites. However, while extended vacuum heat

treatments at 180°C and the use of hydroxyl-free, hydrophobic polymer surfaces show enhanced electron currents, the hysteresis remained largely unchanged in these PbSe NW FETs. Further, encapsulating the PbSe NW FETs with PMMA atop the various hydroxyl-free SiN, polyimide, and parylene dielectric surfaces did not yield devices with as low hysteresis as devices fabricated atop SiO_2 gate dielectric surfaces.

While dehydration of the FET and hydroxyl-free dielectric surfaces did not significantly reduce hysteresis, it was suggested that the carbonyl group on PMMA could hydrogen bond to the hydroxyl groups on the SiO_2 surface[20,21,48,49] and aid in hysteresis reduction.[11] FETs with SiO_2 gate dielectrics exhibited the most dramatic reduction in hysteresis when passivated with PMMA, indicating that there is a unique PMMA/SiO_2 surface chemistry that could promote hysteresis reduction in back-gated PbSe NW FETs. Encapsulating PbSe NW FETs with other hydrophobic polymers, such as carbonyl containing polycarbonate and flourinated CYTOP[TM], was not effective in reducing hysteresis, further signifying that PMMA uniquely lowers hysteresis. PMMA is an amphoteric molecule,[50] meaning it can react both as an acid or a base, but has been shown to adsorb more readily to acidic surfaces,[50] so the acidic nature of SiO_2[51–53] will promote PMMA/SiO_2 adsorption. Unfortunately, PMMA devices are sensitive to solvent and heat treatments, and a robust hydroxyl passivation chemistry is necessary for NW and NC device fabrication and doping. Other hydroxyl passivation chemistries were investigated, but PMMA proved to be the most effective encapsulant. In particular, while HMDS is expected to bond with surface SiO_2 hydroxyl groups as well and should

exhibit reduced hysteresis, HMDS is sterically hindered and its surface coverage is quite poor, resulting in incomplete passivation of hydroxyl groups,[52,54,55] which is evident in the low electron currents [Figure 4-3(A)]. Therefore, we turned our focus to an Al_2O_3 gate dielectric surface because it can be modified with phosphonic acid self-assembled monolayers (SAMs),[56,57] which have been shown to passivate the surface of dielectrics more effectively than silane based SAMs on SiO_2.[57]

Both untreated Al_2O_3 and octadecylphosphonic acid (ODPA) SAM treated Al_2O_3 dielectric layers were used to fabricate electric field aligned PbSe NW FETs, cleaned with solvents to remove ligands and heated at $180^{\circ}C$ for 2 minutes to remove any remaining solvent. We chose ODPA SAM modification of Al_2O_3 in particular as long alkyl-chain lengths form dense assemblies unlike shorter chain analogs.[58] PbSe NW FETs with bare untreated Al_2O_3 and SiO_2/HMDS gate dielectric layers behaved similarly, displaying low electron currents, yielding higher electron currents only upon heating [Figure 4-3(A, E)]. Similar to SiO_2 (even with HMDS passivation), the gate dielectric surface of Al_2O_3 is populated with hydroxyl groups that can act as electron trapping sites to suppress the inherent ambipolar behavior of PbSe NW FETs. PbSe NW FETs atop Al_2O_3 that were encapsulated in PMMA yielded hysteresis values comparable to SiO_2/PMMA devices, since both Al_2O_3 and SiO_2 possess the favorable hydroxyl/PMMA surface chemistry to reduce hysteresis. Treating the basic hydroxyl-terminated surface of Al_2O_3 with acidic ODPA SAMs through acid/base chemistry will form alkyl(aluminophosphate).[59] PbSe NW FETs fabricated atop Al_2O_3/ODPA yielded devices with hysteresis values even lower

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than SiO$_2$/PMMA encapsulated devices [Table 4-1 and Figure 4-3(F)]. Unlike the hydrogen bonding that has been reported to occur between SiO$_2$ hydroxyl groups and the PMMA carbonyl groups, the Al$_2$O$_3$/ODPA is a significantly stronger bond that reduces the hysteresis even further. The surface coverage and density of ODPA SAMs on the Al$_2$O$_3$ surface is also greater than the silane based materials on SiO$_2$.[57] The transistors also retained their low hysteresis when stored in a glovebox for several months, indicating that the Al$_2$O$_3$/ODPA is a stable dielectric stack. Devices were also immersed in 4.0 M hydrazine overnight to see if the gate dielectric stack would withstand a commonly used chemical treatment to dope nanostructured materials, become *n*-type and retain its low hysteresis. While devices became *n*-type, hydrazine increased the hysteresis significantly by at least 10 V, not only for Al$_2$O$_3$/ODPA PbSe NW FETs, but for SiO$_2$, SiN and the polymer devices as well. However, when heating post-hydrazine treated transistors at 180°C for two minutes, devices switched back to ambipolar predominantly *p*-type behavior and with low hysteresis, indicating that the ODPA treatment could withstand even a caustic base like hydrazine, making it a robust dielectric stack for NW and NC FETs.

4-4: *Flexible Low Voltage and Low Hysteresis FETs*

One of the technological benefits of using polyimide, parylene and Al$_2$O$_3$ gate dielectric layers is that these materials can be deposited at low temperatures and integrated in flexible electronics. PbSe NWs were aligned under an electric field on

varying dielectric stacks and exhibit ambipolar characteristics similar to devices with SiO$_2$ on a Si back gate, displaying the versatility of electric-field alignment for a variety of surfaces. Unfortunately, neither polyimide nor parylene are the optimal dielectric materials for low hysteresis devices. Aluminum oxide has been used as a back gate dielectric material, where Klauk *et al* showed that flexible ultralow-power organic FETs (OFETs) could be operated using approximately 3-4 nm thicknesses of Al$_2$O$_3$.[57] Since electric field alignment requires an electric field of 10^4 to 10^5 V/cm between gold source and drain contacts, 3-4 nm thickness of Al$_2$O$_3$ is an insufficient insulator and easily breaks down at such high field strengths, even when passivated with ODPA. An additional 30 nm of ALD (atomic layer deposition) Al$_2$O$_3$ was deposited and passivated with ODPA so electric field alignment could be employed to yield flexible PbSe NW FETs [Figure 4-4(A, B)]. Devices were heated to remove the solvent as done above to yield low hysteresis devices. The measured capacitance for the Al$_2$O$_3$/ODPA dielectric stack is 0.256 $\pm$ 0.014 µF/cm^2, allowing for low voltage operation. Leakage tests were performed on the FETs to verify device behavior was coming from the PbSe NWs. Devices still exhibit ambipolar behavior, as evidenced by both the electron and hole transport in I_D-V_G curves [Figure 4(D)]. These are the first flexible, low voltage (<5V) and low hysteresis (<1V) PbSe NW FETs and show the promise of these nanostructured materials in flexible electronics.
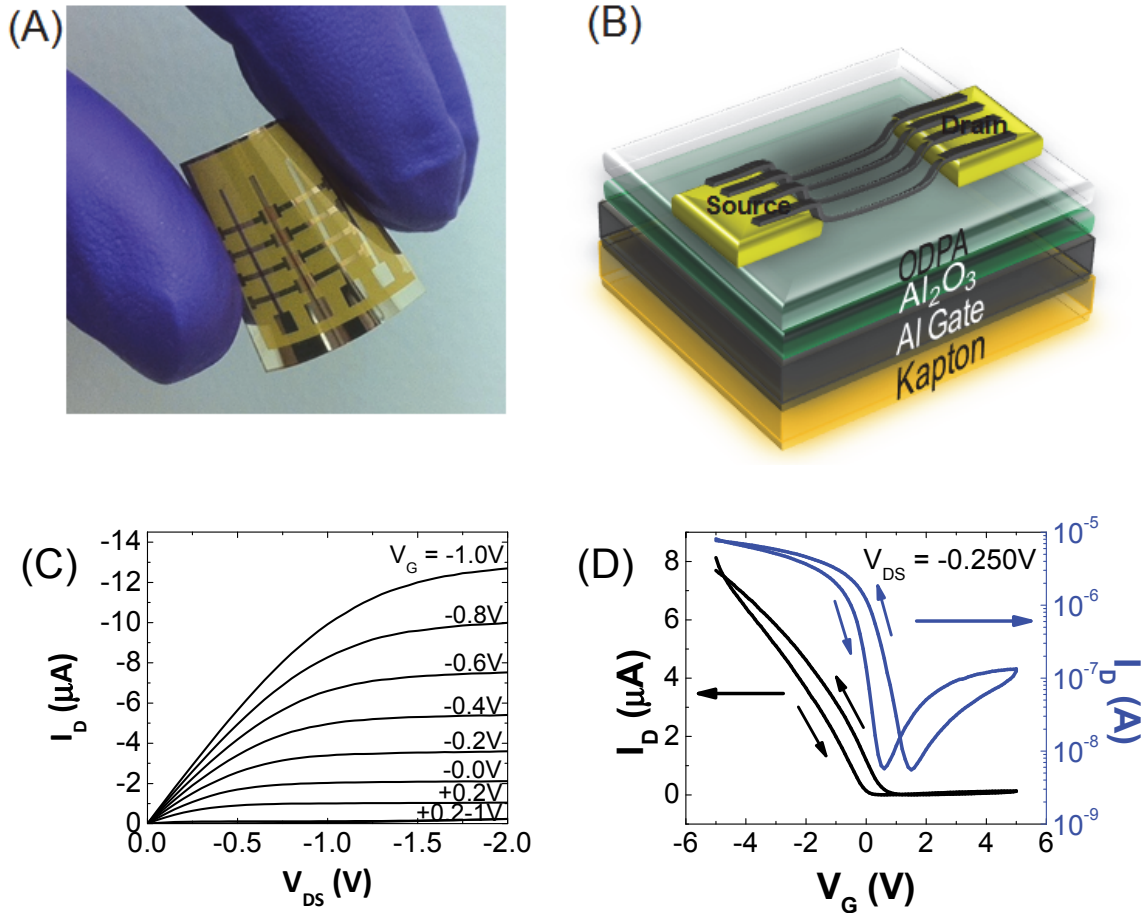
Figure 4-4: (A) Photograph and (B) schematic of flexible PbSe NW FET on Kapton® substrate. (C) I_D-V_{DS} and (D) I_D-V_G characteristics showing reduced hysteresis and low voltage flexible, PbSe NW FET operation.

4-5:   Conclusions

In summary, we show that surface bound water is not solely responsible for the observed hysteresis in bottom contact PbSe NW FETs. By encapsulating PbSe NW FETs in PMMA, we fabricated ambipolar predominantly *p* and predominantly *n*-type FETs with dramatically reduced hysteresis. Predominantly ambipolar *n*-type devices could be

achieved by annealing or placing devices under high vacuum to desorb the surface bound oxygen, which has been shown to suppress the electron current in PbSe nanostructures. Despite careful air-free handling of the NWs, PbSe exhibits extremely high sensitivity to trace amounts of oxygen, even in an inert glovebox environment. In addition, the excess lead on the surface of PbSe NWs was found to make these materials predominantly n-type, demonstrated by the interesting stoichiometric doping studies in our group led by Soong-Ju Oh.

We demonstrated the versatility of electric field alignment by fabricating bottom gold contact PbSe NW FETs atop a range of hydroxyl-free and hydrophobic gate dielectric materials that show enhanced electron currents, but still exhibit large hysteresis. We have identified a surface modified gate dielectric stack, ODPA SAMs on Al_2O_3, that exhibits low hysteresis FET operation. Exploration of alternative combinations of gate dielectric layers and SAM chemistries and/or surface modification of the NWs themselves may allow the small, residual hysteresis to be eliminated. This robust, low hysteresis dielectric stack will not only allow us to study the fundamentals of charge transport in PbSe NWs, but in other colloidal nanostructured systems as well. Additionally, by implementing this device geometry on flexible substrates, we show low hysteresis and low voltage operation on plastics and show that this class of colloidal materials is promising for large area flexible electronics.

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CHAPTER 5:   Thiocyanate Chemistry and Indium Doping for High Performance CdSe Transistors[4]

Similar to colloidal semiconductor nanowires (NWs), colloidal semiconductor nanocrystals (NCs) are similarly prized for their size- and shape-tunable electronic properties.[1–4] Wet-chemical methods have enabled the preparation of highly uniform, monodisperse, crystalline NCs for a wide variety of chemical compositions by commonly employing long-chain, organic ligands to control NC synthesis and to stabilize NC dispersions,[5] as described in Chapter 2. These NC solutions capped with long ligands can be easily processed by a variety of solution-based material deposition methods (spincasting, dip-coating, inkjet printing, dropcasting, spraycoating) to form uniform thin-films[6–11] for large area electronics.

While high quality NC synthesis and dispersibility relies on long ligands, these ligands are insulating and prevent strong coupling and charge transport between NCs once assembled in the solid state. The presence of these capping groups has posed a significant challenge to using these colloidal inks as technologically viable electronic materials for devices[12] and integrated circuitry.[13] Recent advances in ligand chemistry have shown that the original, long ligands used in synthesis can be replaced by shorter inorganic ligands[14–17] either in solution, and still maintain solution-dispersibility and thin-film processability, or in thin-film solids. These novel ligands preserve the discrete,

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[4] Much of this chapter appears in print: Adapted with permission from A. T. Fafarman, W.-k. Koh, B. T. Diroll, D. K. Kim, D.-K. Ko, S. J. Oh, X. Ye, V. Doan-Nguyen, M. R. Crump, D. C. Reifsnyder, C. B. Murray, C. R. Kagan, *Journal of the American Chemical Society*, **133** (39) 15753–15761, 2011 and J.-H. Choi, A. T. Fafarman, S. J. Oh, D.-K. Ko, D. K. Kim, B. T. Diroll, S. Muramoto, J. G. Gillen, C. B. Murray, C. R. Kagan, *Nano Letters*, **12** (5) 2631 – 2638, 2012. Copyright 2011 and 2012 American Chemical Society.

size-dependent features of quantum confinement and enhance electronic coupling between the NCs in thin-films.

Chapter 5 represents a large collaborative work with Dr. Ji-hyuk Choi, Benjamin T. Diroll, Dr. Aaron T. Fafarman, J. Greg Gillen, Dr. Dong-kyun Ko, Shin Muramoto and Soong-Ju Oh. Here, work by Fafarman, A.T. *et al.*[18] demonstrates dispersions of CdSe NCs exchanged with the compact ligand ammonium thiocyanate can be spincast to form dense, crack-free, thin-films with enhanced nanocrystal electronic coupling. Thiocyanate has been shown to be an effective ligand for both solid and solution-exchange NCs, but has been primarily optimized with solution-exchange to produce high-quality films for electronic measurements. Initial measurements of CdSe NC field-effect transistors (FETs) exhibited average mobilities of 1.5 $cm^2V^{-1}s^{-1}$ with indium electrodes. High-quality solid-exchanged NC-films are also being pursued in the group through means of dip-coating by E.D. Goodwin and Eric Wong. Similar to the work done in Chapter 3, work led by Choi *et al.*[19] correctly identified the mechanism by which indium, a low-work function metal, serves as a metal contact and simultaneous dopant for CdSe NCs.   In order to reduce charge trapping and hysteresis, like in Chapter 4, in collaboration we vary the dielectric/semiconductor interface. Combining all these concepts, in collaboration we are able to fabricate high-performance, low-hysteresis CdSe NC-FETs. These FETs show band-like transport with high electron mobilities exceeding 15 $cm^2V^{-1}s^{-1}$.[16,20–22] The solution-processability and high-performance of NC-

FETs make colloidal NC semiconductors extremely attractive as colloidal inks for low-cost, large-scale coating and printing of thin-film electronics.

5-1: *Thiocyanate to Enhance Electronic Coupling*

CdSe NCs are first synthesized using a modified literature procedure by Benjamin T. Diroll. Rigorous air-free conditions were used from synthesis to purification, fabrication, and characterization to prevent oxidation of the NCs. Anhydrous solvents (highest grade available) were purchased from Acros or purged and dried by standard methods. Ammonium thiocyanate (Acros, 99.8%+) was recrystallized from dry alcohol. Trioctylphosphine oxide (90%), tributylphosphine (97%), octadecylamine (99%), and selenium shot (99.99%) were purchased from Sigma-Aldrich. Cadmium stearate was purchased from MP Biomedicals. All manipulations were carried out using standard Schlenk-line techniques under dry nitrogen.

20.0 g trioctylphosphine oxide, 20.0 g octadecylamine, and 2.10 g cadmium stearate were held under vacuum 1 hour at 120 °C, then heated to 320 °C under nitrogen, then 10.0 mL 1.25 M selenium in tributylphosphine solution was injected. Particle growth continued at 290 °C for 15 minutes. The peak of the first absorption maximum ranged from 580 to 583 nm across several independently synthesized batches.

The SCN exchange was pioneered and performed by Dr. Aaron T. Fafarman in nitrogen atmosphere and optimized for each individual batch of NCs. Incomplete exchange will result in transistors exhibiting mobilities below 1 $cm^2V^{-1}s^{-1}$. Typically, 1.0

mL of NH_4SCN ranging in concentration from 100 to 250 mM in acetone was combined with 2.0 mL of CdSe NCs dispersed in hexane at an optical density of 5 to 10 per cm^3 at the first excitonic absorption feature. The mixture was stirred with a vortexing mixer at 3000 rpm for 2 min, with complete flocculation observed within seconds. The slurry was centrifuged at 3000g for 1 min and the *clear, colorless supernatant* (this must be true or ligand-exchange is incomplete) discarded. 2.0 mL of tetrahydrofuran was added and the slurry mixed at 3000 rpm for 2 min, centrifuged at 3000g for 1 min and the *clear, colorless supernatant* (this must still be true or ligand-exchange is *still* incomplete) discarded once more. 2.0 mL of toluene was added and the slurry mixed at 3000 rpm for 1 min, centrifuged at 3000g for 1 min and the clear, colorless supernatant discarded. Dimethylformamide was added to the pellet to the desired concentration and the mixture was gently agitated until the NCs were fully dispersed. This mixture will only be soluble for a very short period of time (less than four hours for a well-exchanged solution or up to a day if poorly exchanged) before the NCs begin to precipitate out of solution due to aggregation, so deposition must be done quickly after thiocyanate-exchange.

Thiocyanate-exchanged CdSe NCs were then spincast uniformly atop the *n*-doped Si wafers with either 130 nm or 250 nm of thermally grown SiO_2, which served as the gate and gate dielectric of the FET, respectively. The substrate was treated for at least 30 minutes in a UV-ozone immediately prior to NC deposition. For FETs, a dispersion with an optical density of 40 was filtered through a 0.2 μm

polytetrafluoroethylene filter and spincast at 500 rpm for 30 seconds, followed by 800

rpm for 30 seconds to yield dense, crack-free uniform NC thin-films. Ideal thicknesses

for transistors were approximately 20 – 40 nm, giving a film color between purple and

blue [Figure 5-1].
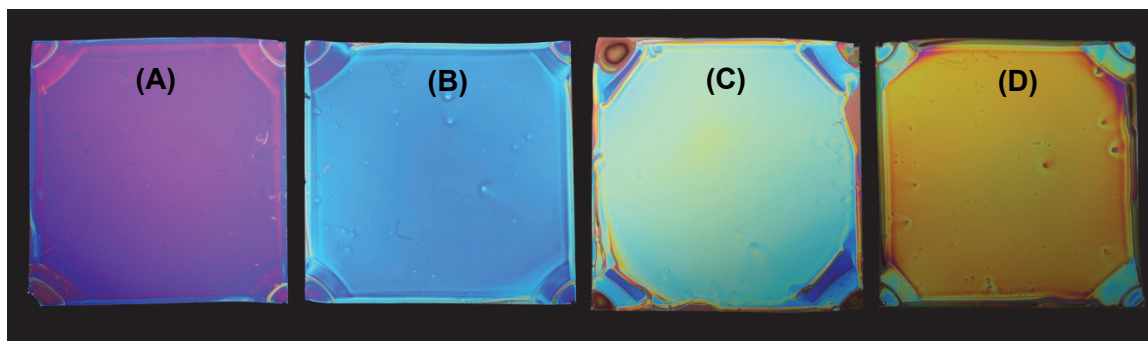
Figure 5-1: (a) Photograph of thiocyanate-exchanged CdSe nanocrystal films spin-cast onto 250 nm SiO_2/n+ Si substrates. The film thickness was increased from (A) 25 nm, (B) 40 nm, (C) 70 nm, to (D) 110 nm. Photo courtesy of Dr. Aaron T. Fafarman.

Indium source and drain electrodes (40 nm) were deposited by thermal

evaporation through a shadow mask to form top contact, bottom gate thin film FETs.

Indium was initially chosen as a suitable electrode for FETs because it was the known as

the best contact material for thin film CdSe[23] and had an appropriate work function

(ϕ_{Indium} = 4.12 eV) alignment with the lowest-unoccupied-molecular-level (LUMO) ($X_{CdSe\text{-}Electron\text{-}affinity}$ = 3.5 – 4.6 eV[24,25]) of CdSe NCs. In the next section of Chapter 5-2, we find

that the indium electrodes have the additional advantageous effect of doping the CdSe

NC thin films. Channel lengths (L) and widths (W) ranged from 30 – 200 μm with a

constant W/L of 15 for all devices. Devices were subsequently annealed at 250 °C for

ten minutes to remove remaining volatile ligands, high enough to decompose the

thiocyanate group and decrease interdot spacing to further enhance interparticle coupling, but low enough to prevent any observable NC sintering and retain quantum confinement. Annealing at temperatures above 250°C did not yield superior devices, causing a drop in the current, lower electron mobilities (μ_e), positive shift in the threshold voltage (V_T) and increase in the subthreshold swing (S) [Figure 5-2]. Devices also had to be annealed at temperatures of 200°C or higher or otherwise they yielded very low currents.
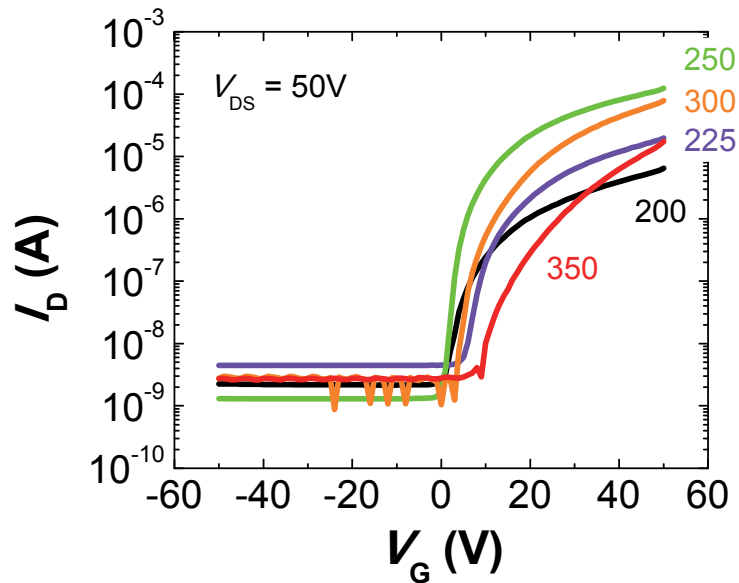
Figure 5-2: I_D-V_G curves of CdSe FETs with 40 nm of indium as electrodes with W/L = 15 on a 250-nm-thick SiO$_2$ gate dielectric on n$^+$ Si gate and heated at a range of temperatures (200°C to 350°C) for ten minutes.

To verify that these CdSe NC thin-films used for FETs retain quantum confinement after 250°C annealing, the optimal device annealing temperature, optical absorption spectra were taken by Benjamin T. Diroll and Dr. Aaron T. Fafarman for a range of temperatures [Figure 5-3(A)]. Both solutions and spincast thin-films of CdSe

NCs show quantized excitations between discrete hole and electron states, as well as the characteristic $1S_{hole}$-$1S_{electron}$ transition with a bandgap (584 nm) larger the bulk bandgap of CdSe (1.74 eV), consistent with quantum-confinement. Upon heating of the CdSe NC film to 250°C, the $1S_{hole}$-$1S_{electron}$ peak position redshifts (120 meV) and broadens [Full width at half maximum (FWHM) 180 meV], but still displays a residual structure with a bandgap larger than the bulk bandgap (<712 nm), consistent with quantum confinement. Continued heating of the sample to higher temperatures (300°C) also shows an evolving excitonic feature that continues to redshift, further suggesting quantum confinement exists at 250°C.
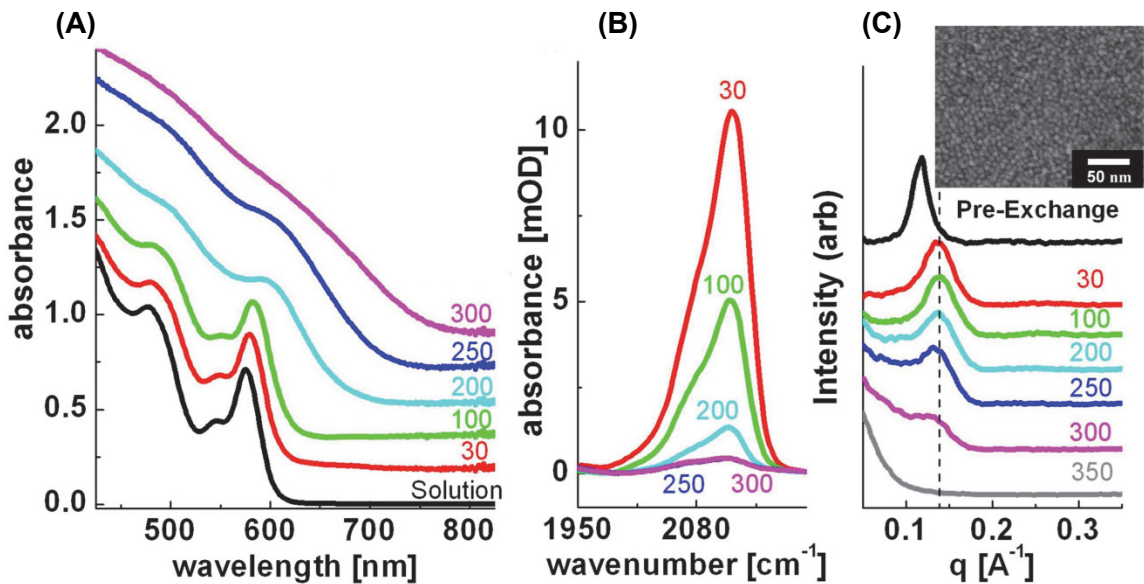
Figure 5-3: (A) Absorption spectrum of thiocyanate-capped CdSe NCs dipsersed in DMF and diffuse reflectance spectra of spin-cast NC thin-films as-cast and annealed at temperatures between 100˚C to 300˚C. (B) Grazing-angle total internal reflectance infrared spectra of CdSe NC films as a function of annealing temperature between 100 ˚C to 300 ˚C. (C) Transmission small-angle x-ray scattering (tSAXS) of CdSe NC thin-films pre-exchange with TOPO ligands, after exchange with thiocyanate, and subsequently annealed at temperatures from 100 ˚C to 350 ˚C. Inset SEM image of a CdSe NC film

annealed at 250°C. Figure courtesy of Benjamin T. Diroll (tSAXS), Dr. Aaron T. Fafarman (Absorption and FTIR) and Dr. Xingchen Ye (SEM).

In order to confirm the $1S_{hole}$-$1S_{electron}$ redshift and broadening was due to enhanced electronic coupling and not due to particle sintering, infrared absorption spectra and transmission small-angle X-ray scattering (tSAXS) spectra and SEM images were taken [Figure 5-3(B,C)] by Benjamin T. Diroll, Dr. Aaron T. Fafarman and Dr. Xingchen Ye to better understand the chemical and structural changes caused by annealing. Figure 5-3(B) shows the distinctive absorption band of the nitrile stretch from the thiocyanate ligand ionically bound to the positive cadmium dangling bond on the CdSe NC surface at 2120 cm^{-1}. After annealing, there is a reduction in the peak intensity, consistent with the known decomposition of metal-SCN bonds around 200°C, leaving behind a metal sulfide.[26] Figure 5-2(C) shows the tSAXS of thin films of CdSe NCs spincast from solutions with its original bulky ligands and after exchange with the thiocyanate ligand. The tSAXS patterns exhibit strong reflection due to nearest-neighbor interactions in the randomly close-packed films at 0.117 Å^{-1} in the pre-exchanged sample and 0.134 Å^{-1} after SCN-exchange, corresponding to a reduction in interparticle spacing from 1.5 nm to 0.5 nm.

The tSAXS patterns were also taken by Benjamin T. Diroll and analyzed at a range of annealing temperatures. While the intensity of the 0.134 Å^{-1} peak slowly decreased with higher temperatures, it retained a strong peak after 250°C annealing, strongly indicating that individual particles remained. Combined with the decomposition of the SCN with annealing as shown by the loss on intensity of the peak at 2120 cm^{-1}, inderdot

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spacing most likely becomes even smaller than 0.5nm, to particles touching or near

touching one another. Wide-angle X-ray scattering (WAXS) spectra of the CdSe NC-films

after annealing at 250°C were also taken to see if the optical broadening observed in

Figure 5-3(A) was caused by growth. The WAXS data showed almost no difference in

the spectra for CdSe films before and after-annealing at 250°C, indicating that no grain

growth occurred after heating. Finally, SEM images of the CdSe NC thin-films annealed

at 250°C display individual particles with no evidence of sintering. While it is not

possible to rule out interparticle necking due to the resolution of each of the techniques

used, the combination of UV-vis absorption, tSAXS, WAXS and SEM data support that

the CdSe NC thin films used for FETs remain as individual, quantum-confined particles

with enhanced electronic coupling after 250°C annealing.
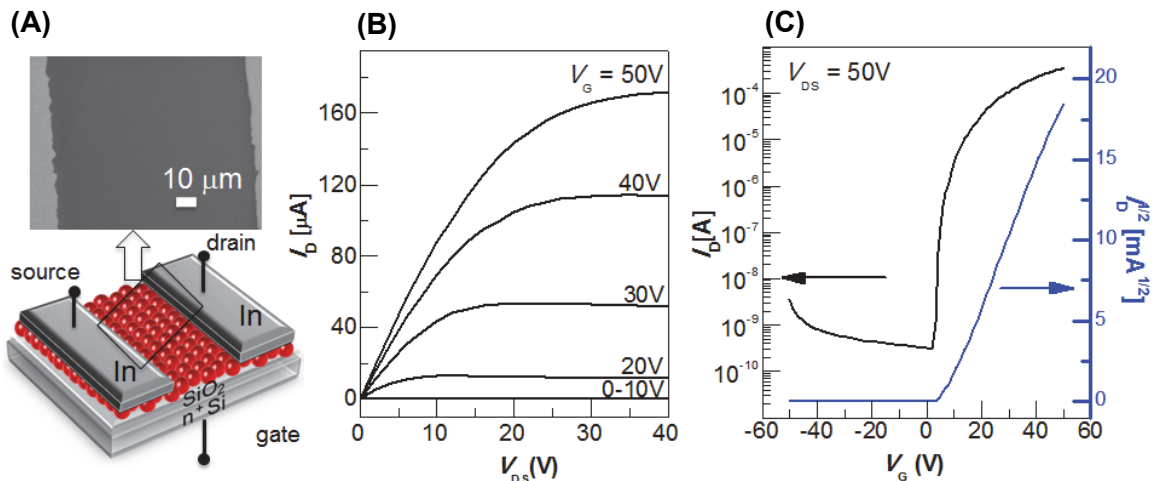
Figure 5-4: CdSe-SCN Field effect transistor characterization for a device annealed at
250 °C. (A) Cartoon of transistor geometry, showing from bottom to top: Doped Si
substrate, SiO_2 thermal oxide, spin-cast CdSe-SCN layer and indium top source and drain
electrodes. SEM image of the channel region, showing edges of Indium electrodes on
either side of the channel. (B) Output $I_D - V_{DS}$ and (C) transfer $I_D - V_G$ characteristics.
Left Y-axis is log-scale and right Y-axis is square-root-scale.

In Figure 5-4(A), the top-contact, bottom-gate configuration of the device is shown schematically, along with a SEM image of the channel, showing that spin-coating forms uniform thin films across micron-scale channel dimensions. Device characterization was performed on a Model 4156C semiconductor parameter analyzer (Agilent) in combination with a Karl Suss PM5 probe station mounted in the nitrogen glovebox. Figure 5-4(B) depicts representative drain current (I_D) versus source-drain voltage (V_DS) characteristics as function of applied gate voltage, indicating CdSe-SCN NC thin films form n-channel FETs. The devices operate in accumulation mode upon application of a positive gate bias as the concentration of majority carrier electrons contributing to I_D increases. The devices show well-behaved FET characteristics, rising linearly at low V_DS and saturating at high V_DS as the channel is pinched off near the drain electrode. Device operation is adequately modeled by standard FET equations.[27]

For low drain-source voltage (V_DS) operation, where the overdrive voltage (gate voltage minus threshold voltage) $V_\mathrm{G} - V_\mathrm{T} > V_\mathrm{DS} > 0$ (linear regime), the drain current (I_D) rises linearly with gate voltage (V_G), and a linear FET mobility can be determined by:

$$\mu_\mathrm{LIN} = \frac{L}{C_\mathrm{DIEL} W V_\mathrm{DS}} \left(\frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}} \bigg|_{V_\mathrm{DS}} \right)$$

where L is the channel length, W is the channel width, C_DIEL is the capacitance per unit area of the dielectric layer, and $\frac{\partial I_\mathrm{D}}{\partial V_\mathrm{G}}$ is extracted from a I_D vs V_G transfer curve at constant $V_\mathrm{DS.}$

For high V_{DS} operation, where $V_{DS} > V_G - V_T > 0$ (saturation regime), the saturation FET mobility can be determined by:

$$\mu_{SAT} = \frac{2L}{C_{DIEL}W}\left(\frac{\partial I_D}{\partial V_G}\right)^2$$

where the square-root of the current I_D rises linearly with V_G and can be used to extract the transconductance in the saturation regime.

I_D and $I_D^{1/2}$ vs V_G data in Figure 5-4(C) was used to calculate the field effect mobility for electrons (μ_e), current modulation (I_{ON}/I_{OFF}), threshold voltage (V_T), and subthreshold swing (S) in the linear and saturation regimes. The devices show an average μ_e of 1.5 ± 0.7 $cm^2V^{-1}s^{-1}$, with a best mobility of 3 $cm^2V^{-1}s^{-1}$ measured across 31 independent devices (with *only* indium electrodes, more details in Chapter 5-2 on how to increase it another order of magnitude). For a typical device, such as that shown in Figure 5-4, the mobility calculated in the linear and saturation regimes μ_{lin} and μ_{sat} are within 10% of each other. I_{on}/I_{off}, is ~10^6, with a threshold voltage of 7 V. The sub-threshold swing, a critical metric for how well the device turns on and off, is 0.73 V/decade, comparable to the industry standard for amorphous Si-based thin film FETs.[23]

5-2:   *Indium Electrode Doping*

Despite the use of thiocyanate to reduce interparticle distance and enhance electronic coupling, only thermally annealed devices with indium electrodes exhibited high mobility and well-behaved FET characteristics when compared to other similar work function electrodes. It appeared that similar to thin-films[28,29] and nanowires of

CdSe,[30] indium was being incorporated into the NC solid as an *n*-type dopant through thermal annealing to increase the carrier concentration, which is normally low due to the CdSe NC's large band-gap (>2eV). In addition, it has been shown that dangling Cd and Se bonds on the NC surface can give rise to both shallow and mid-gap trap states[31], which is expected to limit the mobility, decrease the measured current and increase the device hysteresis. In addition, it has been shown in polycrystalline CdSe thin-films indium diffuses along grain boundaries to passivate trap states arising from dangling bonds.[28,32,33] This is presumed to similarly occur for CdSe NCs where indium will not only passivate the dangling bonds to reduce the trap density, but will also simultaneously increase the carrier concentration through doping.

To prove that indium doping through thermal diffusion occurs in CdSe NCs, other similarly low work function metals were investigated in collaboration with Dr. Ji-hyuk Choi and Soong-Ju Oh, such as aluminum ($\phi_{Aluminum}$ = 4.28 eV) and magnesium/silver ($\phi_{Magnesium}$ = 3.7 eV). To fabricate contacts with different work functions, either 100 nm of thermally evaporated aluminum or 20 nm of magnesium with 80 nm of silver were deposited by thermal evaporation through a shadow mask. Electrodes were deposited atop a spincast film of SCN-exchanged CdSe NCs on degenerately doped silicon with 250 nm of thermal oxide to form top contact, bottom gate CdSe NC-FETs. Conductivity measurements were performed by Dr. Ji-hyuk Choi and Soong-Ju Oh and were done with films of both TOPO-capped and SCN-exchanged CdSe NCs atop a quartz substrate and with aluminum or indium electrodes with varying thicknesses.
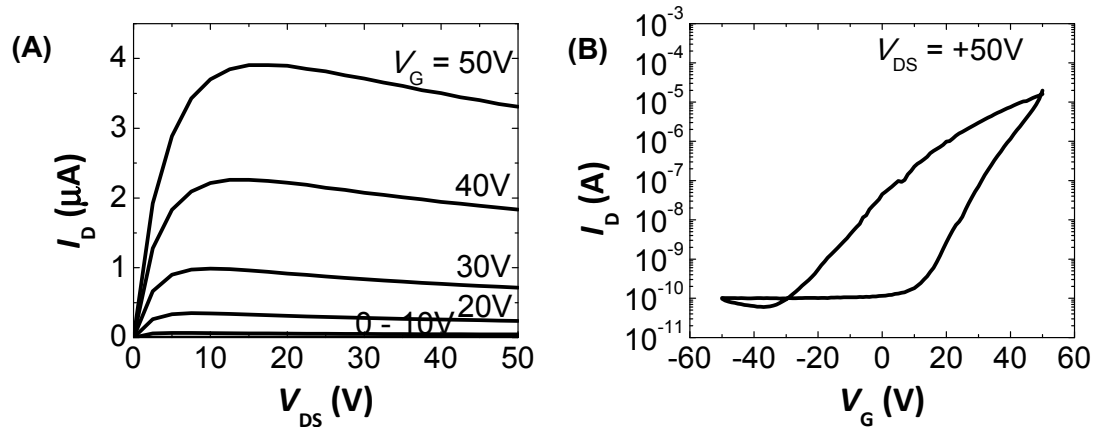
Figure 5-5: (A) I_D-V_{DS} and (B) I_D-V_G characteristics of a CdSe NC transistor with Al source and drain electrodes with $W/L = 15$ on a 250-nm-thick SiO_2 gate dielectric on n$^+$ Si gate.

Compared to CdSe NC-FETs fabricated with thermally annealed indium electrodes, low work function aluminum electrodes exhibit much lower mobilities in the range of 10^{-2} to 10^{-1} cm^{2}V^{-1}s^{-1}, lower currents, higher threshold voltages and do not saturate or show well behaved device characteristics [Figure 5-5]. CdSe NC-FETs were even sintered by heating at a temperature of 350°C and above in excess of 30 minutes to ideally make a continuous polycrystalline film of CdSe, but still yielded little to low currents. We found that before deposition of electrodes, thin films of CdSe NCs needed to be heated for ten minutes at 250°C *first*, since aluminum electrodes are prone to degradation, especially at elevated annealing temperatures. If the CdSe-FETs were annealed at 250°C after aluminum deposition, the transistors yielded little to no current. This was verified for multiple batches of CdSe NCs heated to a range of temperatures. As for magnesium/silver electrodes, only one sample exhibited appreciable current and gating, but was not reproducible.

All units of Siemens/cm	TOPO-CdSe No anneal	TOPO-CdSe 250°C	SCN-CdSe No anneal	SCN-CdSe 250°C
In Thickness: 0 nm	---	---	---	10^{-8}
In Thickness: 20-40 nm	10^{-10}	10^{-10}	10^{-9}	10^{-3}
In Thickness: 80-110 nm	---	---	---	10^{-2}
Al	---	---	10^{-9}	10^{-7}

Table 5-1: Conductivity of spincoated 40 nm CdSe NC films atop quartz substrates with various electrodes, indium thicknesses, ligand coverage and annealing treatments. Data courtesy of Dr. Ji-hyuk Choi and Soong-Ju Oh.

Conductivity tests performed by Dr. Ji-hyuk Choi and Soong-Ju Oh on quartz substrates were also done to verify the effect of indium doping versus the use of a non-doping electrode aluminum. Similar to the FET measurements to optimize annealing temperatures in Figure 5-2, conductivity of SCN-exchanged CdSe NC films remained low (10^{-9} S/cm) until a sharp increase at 200°C (10^{-6} S/cm) to 10^{-3} at 250°C. Aluminum electrodes show very small conductivities with negligible increase on annealing. TOPO-capped CdSe NCs, even with the use of indium electrodes show low conductivity. Finally, we are able to control the conductivity of the CdSe NC thin-film over a large range by varying the thickness of the indium electrodes, indicating that indium is playing an active role in controlling the number of charge carriers in these films.
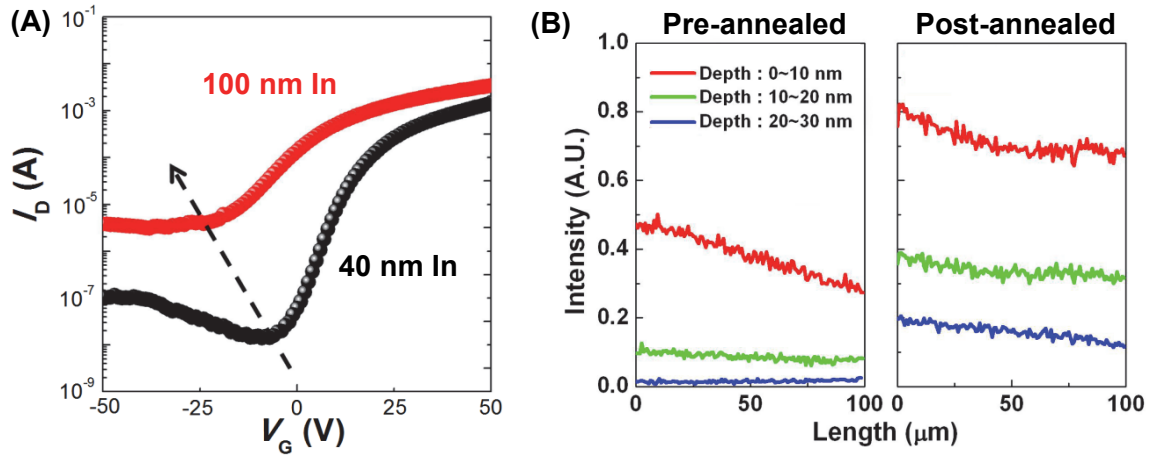
Figure 5-6: (A) I_D-V_G characteristics of CdSe NC-FETs heated for 30 minutes at 250°C with different indium electrode thicknesses using a channel length L = 180 μm, channel width W = 1800 μm and 250-nm-thick SiO_2 dielectric on an n$^+$ Si gate. (B) Lateral distribution of $^{113}In^+$ as a function of depth (left) pre-annealed and (right) post-annealed sample. FET figure courtesy of Dr. Ji-hyuk Choi and ToF-SIMs Shin Muramoto and J. Greg Gillen.

Different thickness of indium electrodes in FETs were also compared by Dr. Ji-hyuk Choi to further verify the role indium doping has on the carrier concentration [Figure 5-6(A)]. Both using thicker indium electrodes and longer annealing times were found to increase the OFF current and cause a negative shift in the threshold voltage, which are both consistent with an increased carrier concentration in the CdSe NC thin-film. Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) was also done courtesy of Shin Muramoto and J. Greg Gillen at the National Institute of Standards and Technology (NIST) to spatially probe for the presence of indium in the channel of the FET. Lateral profiling of the $^{113}In^+$ distribution showed an increasing amount towards the electrode edge within the top 10 nm of the CdSe before annealing, but negligible amounts at deeper depths [Figure 5-6(B)]. After annealing at 250°C for 10 minutes,

there is a substantial increase of the ^{113}In$^+$ distribution for all depth profiles, indicating a significant amount of indium diffusion (>100µm) from the source electrode. Similarly, depth profiling of the ^{113}In$^+$ showed a negligible amounts of indium deeper than 30 nm, but after annealing, there was a large and uniform distribution of indium throughout the depth of the CdSe NC thin-films (at least up to a thickness of 120 nm over a lateral distance of 100 µm).
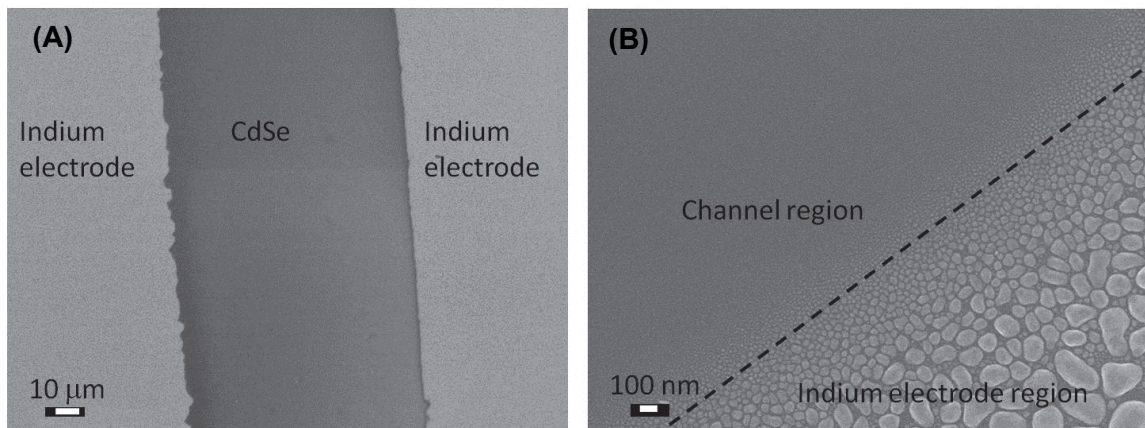
Figure 5-7: (A) SEM image of FET with 100 nm thick indium electrodes after 250°C annealing for 10 minutes. (B) The high magnified image of the boundary between electrode and channel region. Thermally evaporated indium metal electrodes patterned through a shadow mask on to thiocyanate-exchanged CdSe films show island formation. After annealing neither the macroscopic edges of the electrodes or the island size is changed.

While significant indium diffusion does occur throughout the CdSe NC thin-film, even when annealing the devices beyond indium's melting point (157°C), the electrodes do not deform or show evidence of bulk liquid flow into the channel [Figure 5-7]. However, the indium electrodes show significant island formation atop the CdSe NC thin-film and do not appear to form continuous metal contacts. Thermally evaporated

indium similarly forms islands atop a polished silicon surface, which yields no lateral

conductivity on the electrode. This is in contrast to indium foil, which is commonly used

as a conductive solder. Only indium contacts directly above the CdSe NC thin-films

exhibit a reasonable conductivity for device measurements, indicating that the CdSe

directly underneath the electrodes are degenerately n^{++} doped. However, any extended

indium electrodes that were not atop CdSe NCs were similarly not conductive.

In order to make a fully continuous conductive metal contact, an additional 40

nm of gold was deposited above the indium electrode islands. This improved the lateral

conductivity of the electrodes above the CdSe NC thin-film and above the bare

substrate. The addition of gold also helped increase the current levels by an order of

magnitude. Field-effect mobilities were 18.2 ± 2.8 cm^{2}V^{-1}s^{-1} and showed negligible

mobility-dependence on the source-drain voltage V_{DS} [Figure 5-8(A, B)]. Field-

dependent mobility is normally attributed to hopping transfer between localized sites of

different energies in disordered semiconductors.[34–36] By achieving mobility values

above the Mott-Ioffe-Regal limit[37] and more recently, Marcus Theory limit (for 3.9 nm

CdSe NCs with the -SCN ligand length of 0.5 nm or less, the upper limit is 5.9 cm^{2}V^{-1}s^{-1})[38],

it becomes necessary to consider the formation of extended electronic states in these

NC thin-films.[39,40]
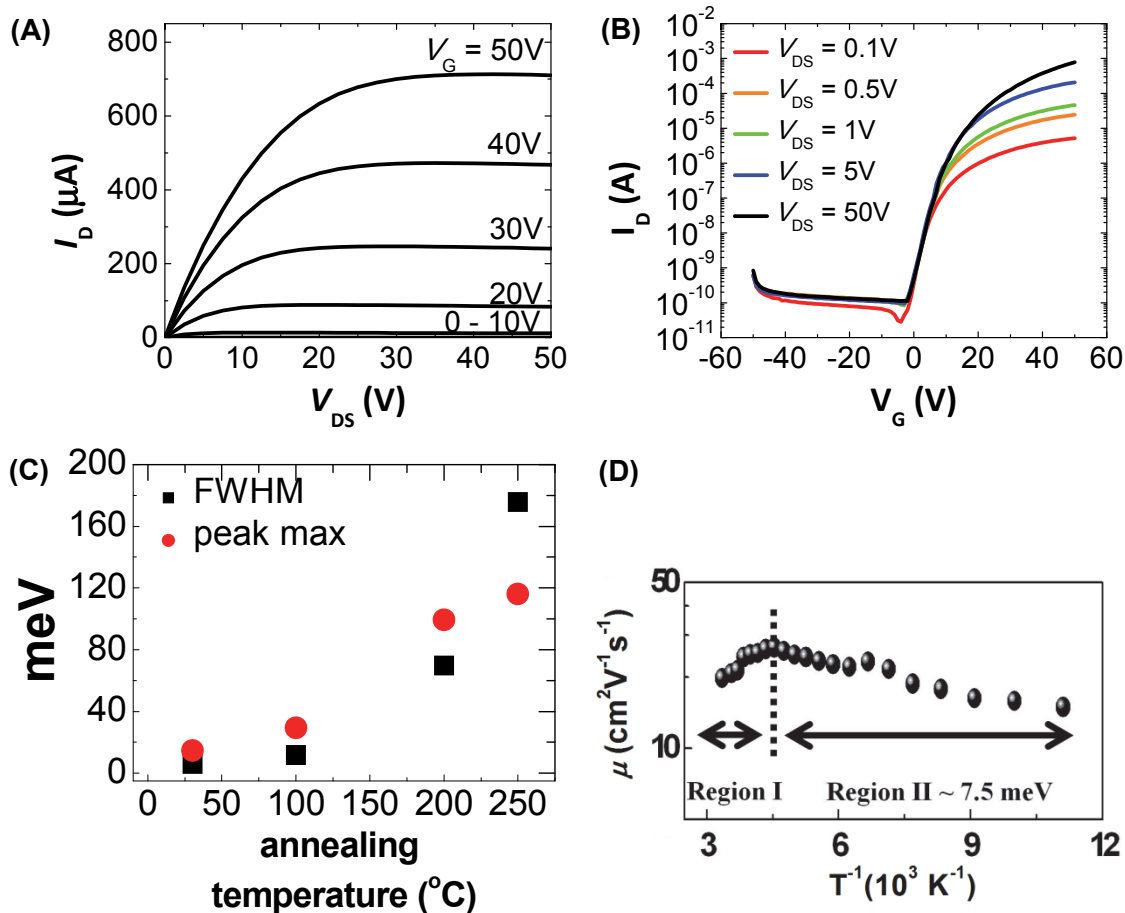
Figure 5-8: (A) I_D-V_{DS} and (B) I_D-V_G of CdSe NC transistor with indium/gold source and drain electrodes with W/L = 15 on a 250-nm-thick SiO_2 gate dielectric on n$^+$ Si gate. (C) Broadening (**black**) and red-shift (**red**) in the $1S_{hole}$-$1S_{electron}$ transition as a function of annealing temperature, relative to the NC dispersion in DMF, calculated from Figure 5-2(A) and (D) Temperature dependent mobility characteristics of a CdSe transistor. FWHM calculation courtesy of Dr. Aaron T. Fafarman and temperature dependent measurement courtesy of Dr. Ji-hyuk Choi and Soong-Ju Oh.

With measured carrier mobilities displaying mean free paths larger than the interparticle distance, there is strong evidence to support that charge transport through the CdSe NCs have transitioned from localized hopping to band-like transport. As such, the tight binding model, which is similar to the Linear-Combination-of-Atomic-Orbitals discussed in Chapter 1, can be used to explain the formation of electronic bands in the

NC thin-films. Similar to semiconductors solids, where isolated atomic wavefunctions overlap to give rise to bands, the wavefunctions of isolated nanocrystals (or more accurately: "artificial atoms") can also overlap and become delocalized over several NCs and give rise to band formation. The width of the band would be proportional to the strength of the overlap interaction (electronic coupling) between neighboring atoms.[41]

The evolution to the formation of extended was performed by Dr. Aaron T. Fafarman. We quantitatively measure the optical broadening of the $1S_{hole}$-$1S_{electron}$ peak [Figure 5-8(C)], which we attribute to the broadening of bandwidths (overlap interaction) of W_{hole} and $W_{electron}$ from initially isolated $1S_{hole}$ and $1S_{electron}$ states, respectively. Previously, through rigorous structural analysis of the annealed CdSe NC thin-films, it appeared that the majority of the observed optical broadening of the FWHM is due to the enhanced interparticle coupling and not due to particle sintering. The initial optical FWHM of isolated NCs, (W_o = 80 meV), was also taken as a standard to account for homogenous and inhomogenous broadening of the NC thin-film caused by site-energy dispersion and not from electronic coupling. CdSe NC thin-films annealed at 250^oC yielded a FWHM of 260 meV. Assuming that both hole and electron states contribute equally to the observed optical broadening, the bandwidths should be identical [W_{hole} = $W_{electron}$ = (FWHM − W_o)/2 = 90 meV].[42] Under the tight binding model, the bandwidths can be related to the interparticle coupling energy [$\beta = \langle \psi_1 | H | \psi_2 \rangle$], where ψ_n represents the isolated nanocrystal wavefunctions of the holes or electrons. Depending on the packing density of the CdSe NCs, the number of nearest neighbors

(NN) that will contribute to the total measured bandwidth ranges from 6 (simple cubic) to 12 (face-centered cubic). This will yield a coupling energy $\beta_{6\,NN} = \frac{W_o}{12}$ to $\beta_{12\,NN} = \frac{W_o}{16}$, to give $\beta = 6 - 8$ meV.[41] Note that $\beta \geq k_B T = 0.0256$ eV, another requirement for delocalized states.[43] The β term is also related to the minimum rate of carrier transfer (Γ) from one nanocrystal to another with equal energy $\left(\beta = h\frac{\Gamma}{4}\right)$, with h as Planck's constant. Combined with the Einstein-Smoluchowski relationship, we can calculate the expected mobility based on the measured bandwidth $\left(\mu = \Gamma \frac{ea^2}{k_b T}\right)$, with e as the elementary charge, a as the center-to-center nanocrystal distance, k_B as the Boltzmann constant and T as the temperature. The calculation yields a mobility as high as 55 cm^{-2}V^{-1}s^{-1}, consistent with the experimentally observed FET values.

Even with the combination of the dramatic redshifts and broadening spectroscopically, mobility values higher than the Mott-Ioffe-Regal/Marcus Theory limits and negligible V_{DS} dependence on mobility, Dr. Ji-hyuk Choi and Soong-Ju Oh used low temperature measurements to verify a negative temperature coefficient (dμ/dT < 0), a commonly known fingerprint for band-like transport.[20,44] Figure 5-8 shows the mobility increases linearly with decreasing temperature for 220K < T < 300K, experimentally validating band-like is realized in these NC thin-films.   At temperatures below 220K and down to 77K, charge transport is determined the presence of shallow traps with a small activation energy of 7.4 meV.

5-3:   Al$_2$O$_3$ Dielectric

While impressive average mobilities of 18.2 $\pm$ 2.8 cm^{2}V^{-1}s^{-1} were observed in

indium doped, SCN-treated CdSe NC FETs atop a SiO$_2$ dielectric atop degenerately doped

silicon, conventional thin-films of CdSe FETs utilized an Al$_2$O$_3$ gate dielectric layer to

improve device stability and reproducibility.[32] In Figure 5-9 (A – C), we show that by

switching to an Al$_2$O$_3$ (30 nm)/SiO$_2$ (250 nm) dielectric stack, we observe higher

currents, an increased average mobility of 27.8 $\pm$ 3.3 cm^{2}V^{-1}s^{-1}, and a slight reduction in

the hysteresis. All other device parameters, such as a high I_{on}/I_{off} and low subthreshold

swing as still preserved with the switch to a new dielectric stack. As described in

Chapter 4, shallow traps at the dielectric/semiconductor interface are known to limit

carrier mobility and give rise to larger hysteresis. To quantitatively compare the density

of interfacial trap states (N_T), Dr. Ji-hyuk Choi and Soong-Ju Oh evaluated the

subthreshold swing for CdSe NC-FETs atop SiO$_2$ and Al$_2$O$_3$/SiO$_2$ dielectric stacks with the

following expression: $N_T = \left(\frac{C_{DIEL}}{q}\right)\left[\frac{S \cdot q}{ln\,(10)k_B T} - 1\right]$, where C_{DIEL} is the total charge of

the dielectric, q is the charge of an electron, S is the measured subthreshold swing, k_B

as the Boltzmann constant and T as the temperature.[27] For devices with only SiO$_2$, the

interfacial trap density is 1.36×10^{13}cm^{-2}, while the Al$_2$O$_3$/SiO$_2$ sample has a reduced

value of 8.97×10^{12}cm^{-2}, consistent with the higher mobility, reduced hysteresis and

lower subthreshold swing.
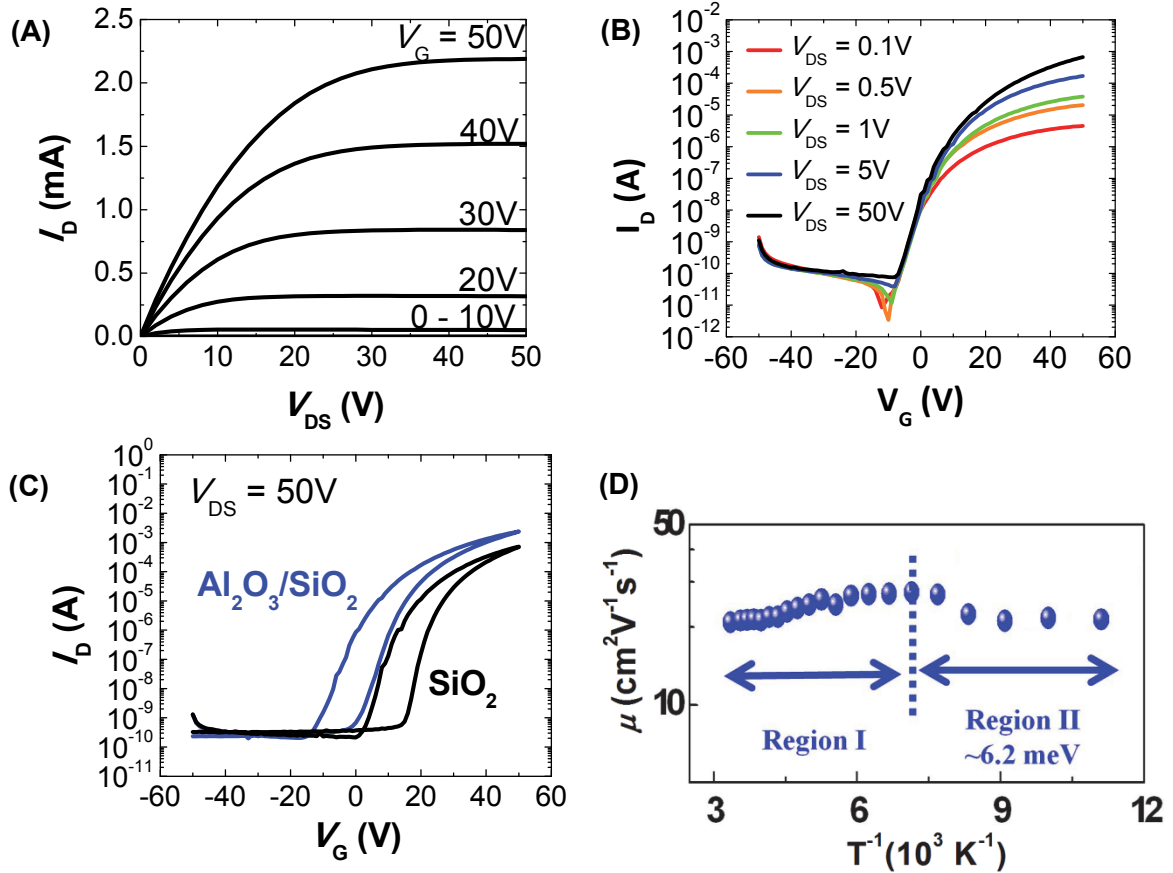
Figure 5-9: (A) I_D-V_{DS} (B, C) I_D-V_G and (D) temperature dependent mobility characteristics of a CdSe NC transistor with indium/gold source and drain electrodes with W/L = 15 on a 250-nm-thick SiO_2/20 nm Al_2O_3 gate dielectric stack on n$^+$ Si gate. Temperature dependent measurement courtesy of Dr. Ji-hyuk Choi.

Since the dielectric/semiconductor interface played such a crucial role in the

improvement of the CdSe NC-FETs, low temperature mobility measurements were

repeated by Dr. Ji-hyuk Choi and Soong-Ju Oh with Al_2O_3/SiO_2 devices. Figure 5-9(D)

shows that these devices retain its negative slope ($d\mu/dT$ < 0) over a larger temperature

range, with the turnover occurring at 140K (compared to SiO2 devices, which turned

over at 220K). In addition, the positive slope region from 140K to 77K exhibits a lower

activation energy, further suggesting that the SiO_2 interface has a larger density of

interfacial traps.
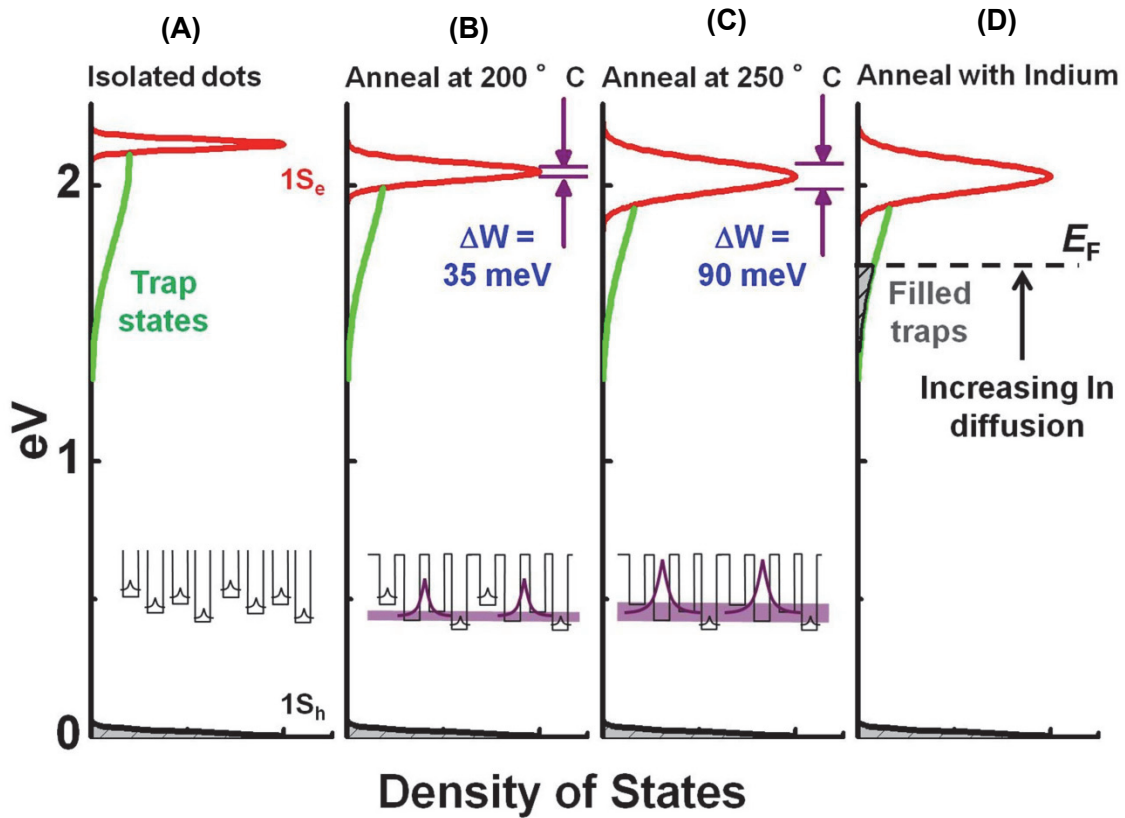
Figure 5-10: Electronic structure depicting (A) isolated, (B, C) annealed, and (D) indium doped CdSe NC films. The width of the $1S_{electron}$ state (**red**) and the bandwidth (**purple**) are evaluated as a function of annealing temperature from optical absorption measurements. Trap states (**green**) are drawn schematically to approximate unpassivated NC surface states and dielectric/NC interface states that tail into the energy gap. Increasing In doping by thermal diffusion raises the Fermi energy (E_F) and fills traps within the band gap. Inset: schematically shows evolution of bandwidth with increasing electronic coupling and wavefunction function overlap. Figure courtesy of Dr. Aaron T. Fafarman.

Figure 5-10 presents a model to explain how band-like transport arises in the

CdSe NC thin-films. Since the energy band alignment of indium electrodes with CdSe

NCs favors electron transport, only the $1S_{electron}$ states are represented. Initial synthesis

of highly mondisperse NCs with very small size distribution (standard deviation $\sigma < 5\%$) gives a very small distribution of site energies. However, the nanocrystals are electronically isolated from one another due to the large interparticle spacings (1.5 nm) from the bulky, insulating TOPO ligands [Figure 5-10(A)]. This is further represented by the inset, which shows that the nanocrystal wavefunctions are completely localized. With thiocyanate exchange and mild annealing, we see an optical broadening of the FWHM and redshifting of the $1S_{hole}$-$1S_{electron}$ peak, which is attributed to the enhanced electronic coupling due to the removal of the TOPO ligand and decreased interparticle spacings (<0.5nm).

Starting at 200°C, we begin to see the sharp increase in currents for both FET and conductivity measurements. The nanocrystal wavefunctions are no longer electronically isolated and begin to overlap with one another with increased coupling energies ($\beta = 2 - 3$ meV) [Figure 5-8(C)]. These overlap interactions give expected mobility values ($\mu = 16 - 21$ cm^{2}V^{-1}s^{-1} calculated from optical data using the tight-binding model presented above) still above the Mott-Ioffe-Regel/Marcus Theory limit, indicating we have already begun to see band formation [Figure 5-10(B)]. However, due to the dispersion in site energies, not all NCs participate in the delocalized states (shown in inset). With increased heating to 250°C [Figure 5-10(C)], the enhanced electronic coupling ($\beta = 6 - 8$ meV) is represented by the wider bandwidth, which encompasses a larger fraction of the NCs with different site energies.

However, as we have seen in samples using aluminum electrodes, just because band formation occurs does not mean the carriers will have access to the bands at room temperature. The large density of unpassivated NC surface states (Cd and Se dangling bonds) and dielectric/NC interface states introduces a high density of broadly distributed trap states, shown in Figure 5-10. In undoped and unpassivated aluminum electrode FETs, the Fermi level (E_F) lies below the trap levels, limiting carrier mobility. Doping with indium shifts the E_F closer to the extended states, increasing the carrier concentration. The trap density also fills deep traps by passivating the NC surface states, leaving behind shallow interface states. These shallow interface states can be further reduced by choosing the proper dielectric stack, as we have done so with Al_2O_3/SiO_2 instead of SiO_2. For $k_BT \gg$ trap depth, electrons occupy the extended states and exhibit band-like transport.

5-4:   Conclusions

We have shown that the use of the small, compact ligand thiocyanate and mild annealing forms extended states in NC-solids. Combined with indium doping to reduce surface trap states and increase the carrier concentration, high performance CdSe NC-FETs with band-like transport were constructed. We are able to further reduce carrier trapping by appropriately choosing an Al_2O_3/SiO_2 dielectric stack interface. In addition to the remarkable device metrics (high mobility, large I_{onn}/I_{off}, small subthreshold swing), the fabrication methods are non-caustic and can be applied to a large variety of

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substrates. Besides CdSe NCs, the general applicability of both thiocyanate exchange and the thermal diffusion method to other semiconductor NC materials and thin-films points the way forward to wide-spread implementation of solution-processed low-cost, large-area, high-performance NC-based electronics.

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CHAPTER 6:   Flexible, Low-voltage Nanocrystal Integrated Circuits[5]

While there has been significant progress in developing single high mobility NC-FETs that further operate with low-hysteresis[1,2] at low-voltage,[3] these high-performance NC-FETs have not been integrated into NC circuits in the literature. All circuit demonstrations have been limited to two single separate FETs connected externally to form an inverter.[3,4] In order to realize nanocrystal integrated circuits (NCICs) for large-area, thin-film electronics, it is necessary to go beyond discrete FET fabrication, to integrate multiple FETs into circuits and to evaluate device operation, such as the switching speed and signal amplification of the NC-FET. This requires that NC thin-films be processed and deposited over a large area to form uniform devices that operate in concert as circuits.

In Chapter 6, we demonstrate the first NCIC inverters, amplifiers, and ring oscillators fabricated from high mobility CdSe NC-FETs. In Chapter 5, we previously introduced high mobility CdSe NC-FETs that operated at high voltages on rigid substrates, achieved through both strong coupling, by introducing the compact ligand ammonium thiocyanate, and through doping, by thermal diffusion of indium at mild temperatures.[1] Thiocyanate is an environmentally benign and non-corrosive ligand, allowing solution-deposition of NC devices on a variety of substrates, including flexible plastic substrates, which we have previously demonstrated.[4] This greatly expands the

applicability of these materials compared to other recently developed novel ligands. For

example, while excellent mobilities have been observed with molecular metal

chalcogenide complexes,[2,3] these NCs are dissolved in hydrazine, an extremely caustic

solvent that is not compatible with flexible plastics. In addition, since a wide range of

flexible electronic applications are typically powered by small thin-film batteries or radio

frequency fields,[5,6] it is necessary to show the scalability of these colloidal inks to

minimize energy consumption. In Chapter 4, we demonstrated low-voltage operation of

flexible colloidal nanowire FETs using thin Al_2O_3 as our robust, high capacitance and low

leakage gate dielectric material compatible with plastics.[7] Here, we demonstrate high-

performance NC-FETs that operate at low-voltages on flexible plastics and serve as the

building blocks of complex integrated circuits, demonstrating this class of materials as a

viable flexible, electronic technology.

6-1:   Flexible, Low-Voltage CdSe FETs

To fabricate flexible devices, we used either a 25 or 50 μm thick polyimide

substrate and covered the substrate with 30 nm of atomic layer deposited (ALD) Al_2O_3 at

250 °C. Encapsulation with Al_2O_3 preshrinks the polyimide substrate prior to

subsequent thermal processing, which would otherwise cause severe delamination and

cracking of the deposited NC thin-films and metal electrodes. Similar to the fabrication

of flexible PbSe nanowire FETs described in Chapter 4, a 20 nm thick Al back gate was

deposited by thermal evaporation through a shadow mask. The device was exposed to

an oxygen plasma to increase the thickness of the native Al_2O_3 on the Al gate and to create additional hydroxyl groups necessary for subsequent growth of a 30 nm ALD Al_2O_3 gate dielectric layer. The measured capacitance of the dielectric layer was 0.253 +/- 0.019 $\mu F/cm^2$, allowing for low-voltage operation. We also characterized the FET gate leakage at pA levels to verify that current modulation arose from the CdSe NC thin-film channel and to show that the thin layer of ALD Al_2O_3 formed a robust gate oxide that is suitable for use in flexible electronics.

To prepare the NC dispersion for spincoating, monodisperse CdSe NCs with as-synthesized long insulating ligands were treated in solution with ammonium-thiocyanate in a nitrogen glovebox,[1,8] replacing the long ligands with the compact thiocyanate ligands, while maintaining solution dispersibility. The thiocyanate-exchanged NCs were redispersed in dimethylformamide and spincast atop the flexible substrates to form uniform, crack-free, randomly close-packed NC thin-film semiconducting channels. Unlike organic semiconductors, where the morphology and mobility of the material is reported to be highly dependent on the surface roughness,[9] we found that the NC thin-films are largely insensitive to a root mean squared value as large as a couple nanometers. Inside a nitrogen glovebox with an integrated evaporator, In/Au (50 nm/40 nm) electrodes were thermally deposited through a shadow mask atop the NC thin-film to complete back-gate/top-contact FETs [Figure 6-1(A, B)]. We have also fabricated back-gate/bottom-contact devices, but these devices typically suffer from larger contact resistance and therefore display poorer device

performance. For the back-gate/top-contact FETs, typical output [drain current versus

drain-source voltage (I_D-V_{DS})] [Figure 6-1(C)] characteristics show n-type device behavior

that is modulated by a small positive voltage as low as 2V. The extracted electron FET

mobilities from the transfer curves [drain current versus gate voltage (I_D-V_G)] [Figure 6-

1(D)] in the linear regime (V_{DS} = 0.1V) are 21.9 +/- 4.3 cm^{2}V^{-1}s^{-1} and in the saturation

regime (V_{DS} = 2V) are 18.4 +/- 3.6 cm^{2}V^{-1}s^{-1}. We translated our previous work on high-

performance CdSe NC-FETs on rigid wafers operating at high voltages[1] to plastic

substrates operating at low voltages. These FETs show high I_{ON}/I_{OFF} over 10^6, low

subthreshold swing (S = 0.28 +/- 0.09 V/dec), low threshold voltage (V_T = 0.38 +/- 0.15 V)

and low hysteresis (ΔV_T = 0.25 +/- 0.07 V) at V_{DS} = 2V. We attribute the low hysteresis to

passivation of the NC surface by indium and the selection of Al$_2$O$_3$ as the gate dielectric

material, which we have shown to reduce the density of trap states at the NC surface

and at the semiconductor-gate dielectric interface that give rise to hysteresis in NC-

FETs.[1] As such, the small variation in device parameters and large-area uniformity of

these NC-FETs enables their integration in flexible NCICs.
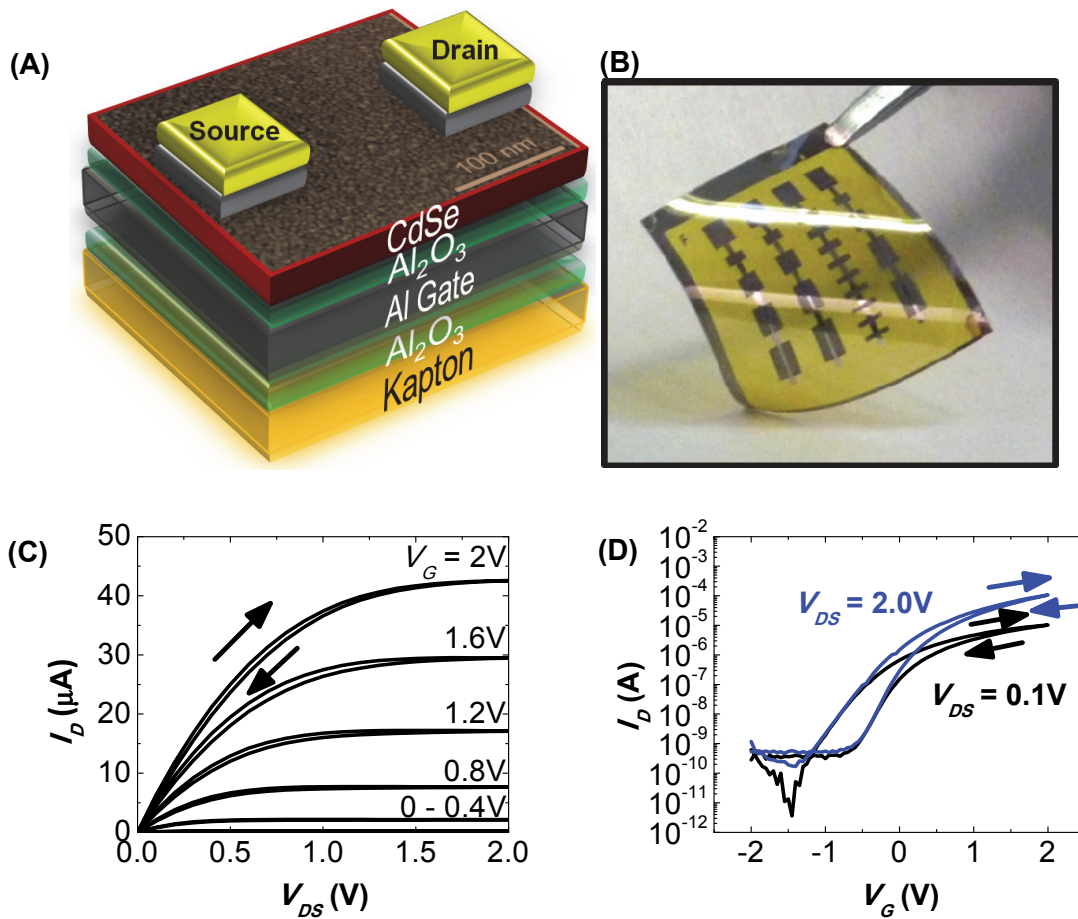
Figure 6-1: (A) Schematic and (B) photograph of a flexible CdSe NC-FET atop a Kapton® substrate. (C) Output $I_D - V_{DS}$ and (D) transfer $I_D - V_G$ characteristics of a flexible, CdSe NC-FET.

6-2: Nanocrystal Integrated Circuits on Plastic

To demonstrate the applicability of these high-performance, flexible CdSe NC FETs as building blocks in integrated circuits, we constructed *n*-type unipolar inverters, amplifiers and ring oscillators and studied their basic parameters for analog and digital circuit applications. Similar to our fabrication of flexible NC-FETs, circuits were

fabricated on either 25 or 50 μm thick preshrunk, Al_2O_3 encapsulated polyimide substrates with thermally deposited 20 nm Al gate patterns, but here we developed a simple, additive process for Au filled vertical interconnect access (VIA) holes to integrate device layers. This VIA process is unlike those previously developed through Al_2O_3 that required corrosive and subtractive etching.[10,11] A VIA shadow mask was microscopically aligned to the Al gate lines and 60 nm of Au was thermally deposited to pattern the VIAs. The sample (with both gate and VIAs) was then exposed to an oxygen plasma to selectively increase the thickness of the native Al_2O_3 atop the Al lines, which only grows an unstable oxide atop Au.[12,13] ALD Al_2O_3 then selectively deposits a high quality oxide atop the Al, but not atop the Au, which still retains conductivity after ALD, as experimentally verified. Thiocyanate-exchanged CdSe NCs were then spincast uniformly atop the samples, followed by thermal evaporation of In/Au electrodes through a shadow mask to form different integrated circuit topologies.
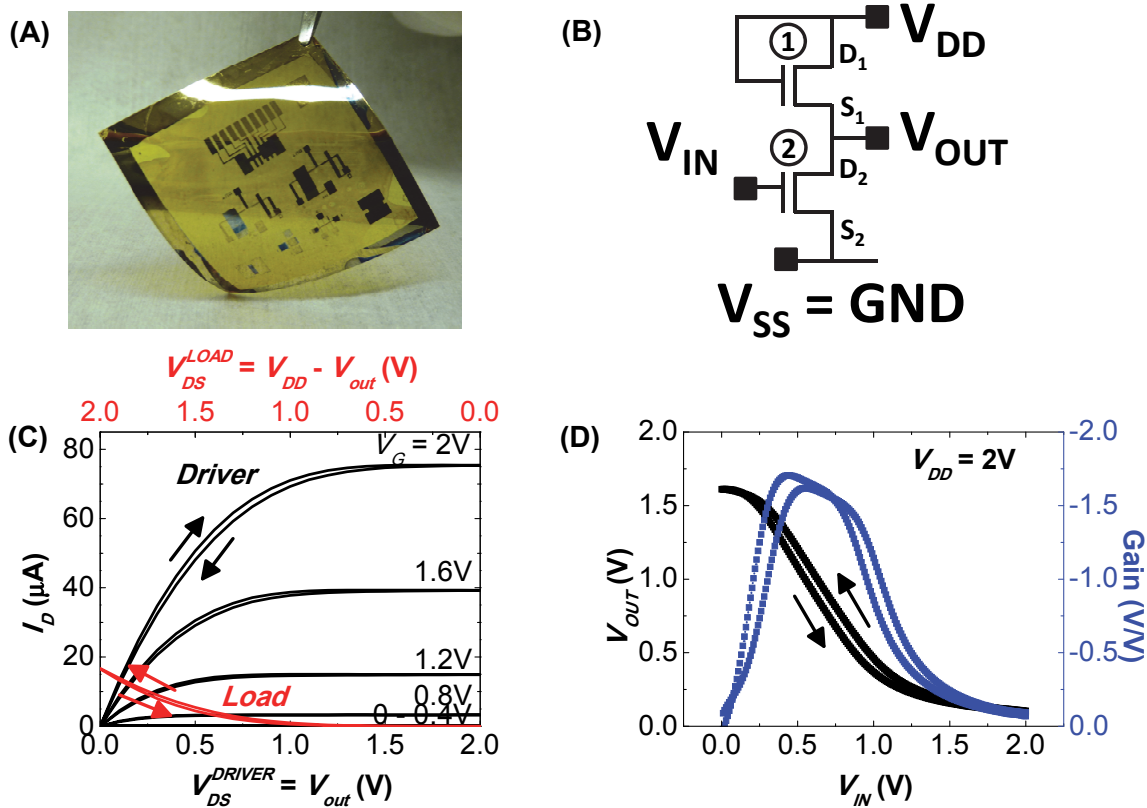
Figure 6-2: (A) Photograph and (B) circuit schematic of saturated-load inverters. (1) Load NC-FET and (2) Driver NC-FET. (C) Graphical analysis of constituent driver (**black**) and load (**red**) NC-FET output characteristics, sweeping in forward and reverse, comprising the NCIC inverter, and (D) the corresponding voltage transfer characteristics (**black**, left axis) and gain characteristics (**blue**, right axis) of the NCIC inverter sweeping forward and reverse at a supply voltage of 2V (V_{DD}).

Figure 6-2(A) shows an optical micrograph of solution-deposited CdSe NCIC inverters fabricated on flexible plastics substrates. The fabricated integrated inverters are based on a saturated-load design as depicted in the circuit layout [Figure 6-2(B)], where one *n*-type FET acts as an active load and the other *n*-type FET as a driver. Since the threshold voltage is positive and the drain and gate voltages are identical, the load FET always operates in saturation.   Our CdSe NCIC inverters were designed to have a

driver with channel length (L) and width (W) ratio of 40 (L = 40 µm, W = 1600 µm) and to

have a load with W/L of 10 (L = 40 µm, W = 400 µm). We measured the output

characteristics of the constituent driver and load FETs of the inverter element separately

to insure that they operated as designed [Figure 6-2(C)]. The on-current for the driver is

approximately four times larger than that for the load, as expected from the ratio of

channel W/L. Graphical analysis [Figure 6-2(C)] provides a construction of the voltage

transfer characteristic (VTC) of our integrated inverter from the constituent NC-FET

building blocks. A representative VTC measured from a fabricated flexible, integrated

inverter emulates the constructed VTC [Figure 6-2(D)]. The inverter gets its name from

inverting a "low" input signal to a "high" output signal, and a "high" input signal to "low"

output signal. For multiple flexible inverters, VTCs show a 1.5 +/- 0.1V output swing,

which makes use of 75% of the available supply voltage (V_{DD} = 2V). The output swing is

consistent with that expected for the saturated-load design, where the voltage output

high is limited by the FET threshold voltage to the difference between supply and

threshold voltages V_{DD}-V_T. Our inverters show voltage amplification with gains

averaging -1.58 +/- 0.26 V/V, reaching as high as the theoretical gain of -2 V/V. The

maximum gain of -2 V/V is consistent with that expected for a metal-oxide

semiconductor common-source amplifier with a saturated-load, defined by the channel

dimensions of the constituent FETs $\left[Gain = - \sqrt{\frac{(W/L)_{DRIVER}}{(W/L)_{LOAD}}} \right]$[14] and may be tailored by

choice of the load and driver geometries, depending on the design specification. The

low hysteresis in the inverter VTC is ascribed to hysteresis in the NC-FET characteristics.

The inverters' VTCs show wide, linear regions of gain, allowing for input signal

amplification, and inversion of logic output high and low at the extremes of the VTCs,

enabling signal switching. On the other hand, owing to the large input resistance (0.5

TΩ) and relatively low output resistance (few tens of kΩ), these amplifiers could also

serve as a buffer stage in circuitry. The inverter is the most basic element in circuits,

used to construct amplifiers for analog circuits and logic gates for digital circuits. The

NCIC inverters' VTCs follow circuit design expectations, with wide output swing and

proper gain and show adequate noise margin, large compared to the low hysteresis,

prerequisites for realizing larger and more complex integrated circuits.
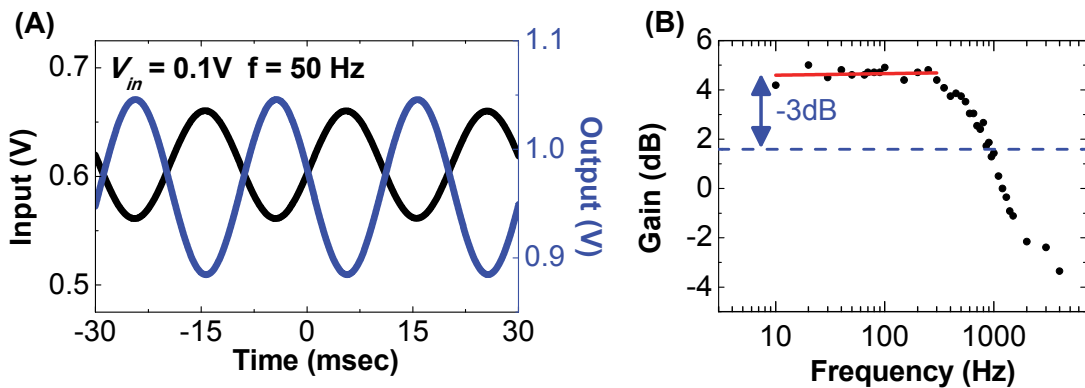
Figure 6-3: (A) Output waveform (**blue**, right axis) of NCIC voltage amplifier in response to a 50 Hz, 100 mV sinusoidal input on a 0.6V DC bias (**black**, left axis). (B) Frequency response of a voltage amplifier (**black** circles). A linear fit (**red** solid line) shows a 4.59 dB voltage gain at low frequency which is used to find the 3 dB bandwidth (**blue** dashed line).

In Figure 6-3(A) we demonstrate typical characteristics of the NCIC inverter

operating as a common-source with active load voltage amplifier. A 50 Hz, 100 mV

sinusoidal signal is superimposed on a 0.6V DC bias at the input (black). The output

waveform (blue) is a replica of the input signal that is linearly amplified with no

waveform distortion, is sinusoidally varying about a DC output voltage of 0.95V as

anticipated from the inverter's VTC, and exhibits a 180 degree phase shift as expected

from a common-source gain stage. The measured frequency response of the voltage

amplifier has a 3dB bandwidth (70.7% magnitude of the maximum gain of 4.59 dB) of

900 Hz [Figure 6-3(B)], which is limited by parasitic capacitance in our current circuit

design. We studied the single-time-constant network in the voltage amplifier, and

estimated a 3dB bandwidth of 1.4 kHz.
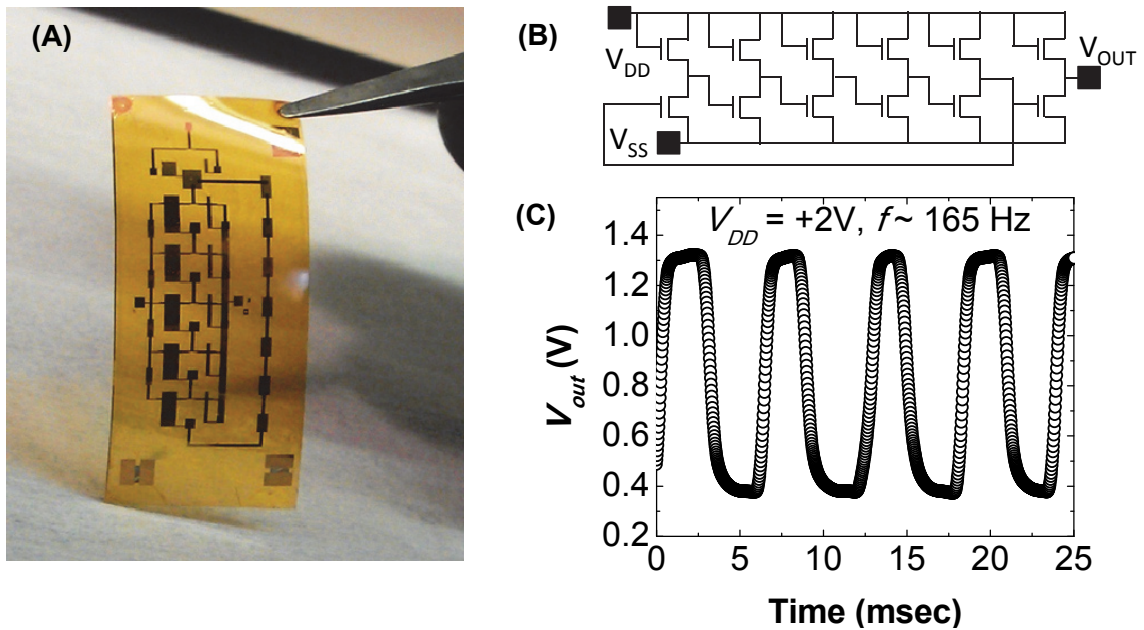
Figure 6-4: (A) Photograph, (B) circuit schematic and (C) output characteristics of a five-stage NCIC ring oscillator with a sixth stage buffer operating at a supply voltage of 2V (V_{DD}) with a frequency of 165 Hz.

Building on the CdSe NCIC inverter as a logic switch, we integrated multiple

inverter stages to construct the first NCIC ring oscillators. Using the same processes for

circuit fabrication and VIA integration described for the inverter and amplifier, 5-stage

ring oscillators (10 NC-FETs) were fabricated over areas of 2 cm by 6 cm on flexible

plastic [Figure 6-4(A)]. The circuit layout of the ring oscillator is depicted in Figure 6-

4(B), showing the output of the fifth inverter stage connected to the input of the first

inverter stage of the oscillator, and an additional sixth inverter used as a buffer stage to

minimize the load and interconnect capacitances. Figure 6-4(C) shows the output

characteristics of a 5-stage NCIC ring oscillator. The solution-deposited, NC-FETs

fabricated on plastic substrates form devices with uniform parameters over-large areas

to operate in concert as required to realize ring oscillators. The constituent NCIC

inverter stages have adequate noise margin to support signal propagation through logic

switching between "0" (low) and "1"(high). At the low 2V supply voltages, the ring

oscillator output characteristic has no distortion across the 1V rail-to-rail swing,

spanning 67% of the output swing or 50% of the supply voltage. The oscillation

frequency is ~165 Hz, *i.e.* the signal delay per inverter is 606 μs. Similar to the amplifier,

the measured frequency of the ring oscillator is limited by parasitic capacitances rather

than by the intrinsic properties of the NC thin-film. We estimated the signal delay per

stage of the constituent inverters in the 5-stage ring oscillator to be 170 μs, and is the

first reported NC-FET based ring oscillator.

The switching speed of the NCIC ring oscillator, which successfully operates at desired low supply voltages, is comparable to other emerging solution-processable materials with similar channel lengths (40 μm) and low-voltage operation,[15,16] suggesting that colloidal semiconductor NC inks form a promising class for low-cost thin-film analog and digital electronics. The switching speeds is sufficient for sensor and display applications.[17–19] Faster switching times may be realized by designing circuits with shorter channel lengths and minimizing the parasitic capacitance. Improved fabrication techniques to achieve better alignment or to even develop self-aligned[20–22] structures will minimize parasitic capacitances to the femto Farad scale, promising not only faster switching, but CdSe NCIC voltage amplifiers with MHz bandwidths.

In conclusion, we report the first NCICs, demonstrating low-voltage NCIC inverters, amplifiers and ring oscillators constructed from multiple high-performance NC-FET building blocks. By taking advantage of the non-corrosive thiocyanate ligand and doping of the CdSe NC thin-film by mild thermal annealing, we fabricated high-performance NC-FETs and NCICs from colloidal NC inks over large-areas on flexible plastics. The small variation in device parameters and large-scale uniformity of our solution-processed NC-FETs enabled functional NCIC circuits for both analog and digital applications. Recent demonstrations of more sophisticated pseudo-complementary metal-oxide semiconductor circuits based on unipolar devices may be applied to improve the performance of these flexible NCICs.[23] With continued advances in NC

ligand chemistry and doping, this class of solution-processable materials promises to grow beyond unipolar circuits to complementary metal-oxide semiconductor based NCICs constructed from high-performance *n*- and *p*-type NC-FETs from the wide-range of available colloidal NC ink chemistries.

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CHAPTER 7:   Future Work

7-1:   Remote Doping in CdSe Nanowires

Due to the large surface-to-volume ratio of colloidal nanostructures, these

materials are extremely sensitive to their surrounding environment, even small

deviations in the surface stoichiometry. Subtle changes in the surface composition or

additional of metal salts have been reported to drastically change the electronic

properties of these materials and can be seen as an effective route to "remote dope"

these nanostructures at the *surface*.[1–4] At the same time, introducing impurities into

the lattice of the nanostructure, similar to impurity doping in silicon doping with arsenic

or boron, substitutional doping the *bulk* of the NC with impurity atoms during

synthesis[5–9] is also being actively pursued to control the carriers. Due to the small sizes

of these NCs and the limited resolution of many analytical techniques, it is extremely

difficult to distinguish if an impurity (dopant) is on the surface or incorporated the bulk.

Effectively understanding how impurities get incorporated and affect electronic

transport is absolutely necessary to develop a generalized scheme for controllable and

stable doping for the field of semiconductor NCs.

To date, electron paramagnetic resonance (EPR) of Mn atoms[8] has been one of

the few techniques to distinguish if impurity atoms have been incorporated into the

bulk or on the surface for ZnSe NCs and more recently, electron energy loss

spectroscopy with annular dark-field scanning transmission electron microscopy (ADF-

STEM)[10] was used to detect Mn inside ZnSe. However, EPR depends on the hyperfine

interaction with the [55]Mn nuclear spin (I = 5/2), and cannot be used to image other types of dopants. ADF-STEM requires expensive equipment and may not be readily accessible to a large audience. As such, an effective and simple method to account for the location of the impurity is necessary.

We propose doing low-temperature measurements of colloidal nanowire field-effect transistors as an effective route to identify the location of dopants. Most thin films and nanocrystals a decrease in mobility low temperatures due to the presence of grain boundaries, dislocations, defects and thermally activated hopping mechanisms. We have previously shown that single-crystalline PbSe nanowires do not exhibit grain boundaries or defects, reflected in the monotonic increase of mobility with decreasing temperature.[11] In addition, incorporation of excess Pb or oxygen on the surface acts as a remote dopant and does not contribute to scattering at low temperatures. By similarly utilizing single-crystalline colloidal CdSe NWs, we can determine if indium is incorporated into the nanostructure bulk or surface based on low temperature measurements.

Here, we report using colloidal nanowires of CdSe in a field-effect transistor (FET) as a simple platform to understand the effect of surface stoichiometry on charge transport in CdSe nanostructures. Similar to the fabrication of PbSe NW FETs in Chapter 2 and exploration of doping in Chapter 3, we use CdSe NW FETs to investigate the role of "doping" the surface with different stoichiometries.
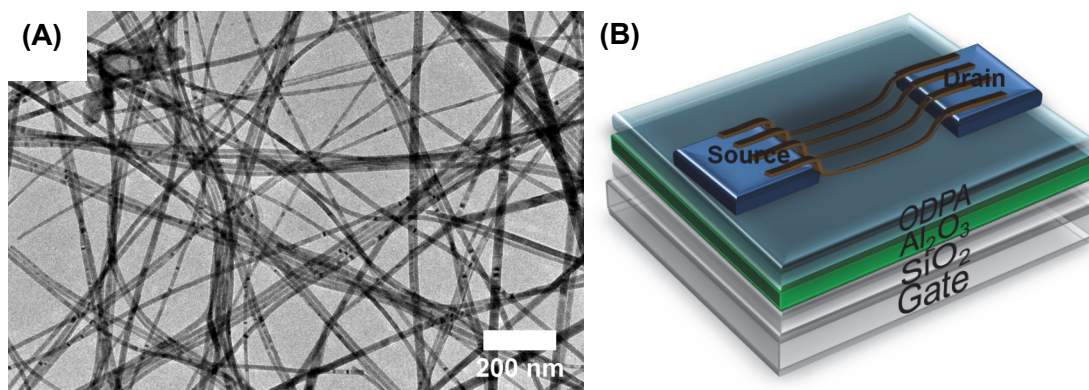
Figure 7-1: (A) TEM image of as-synthesized colloidal CdSe nanowires and (B) schematic of CdSe NW FETs atop an ODPA/Al_2O_3/SiO_2 dielectric stack.

Single-crystalline CdSe NWs over 20 μm in length and approximately 20 nm in diameter were synthesized via solution-liquid-solid synthesis[12] using bismuth nanoparticles as a seed catalyst[13] by Benjamin T. Diroll [Figure 7-1(A)]. Electrodes composed of Ti/Au/In (2 nm/10 nm/10 nm) were thermally deposited through silicon nitride membranes to form devices with a channel length of 20 μm and channel width of 1260 μm [Figure 7-1(B)]. These were fabricated atop a dielectric stack of octadecylphosphonic acid (ODPA) self-assembled monolayers on top of 20 nm of atomic layer deposited Al_2O_3 atop of 250 nm of thermal SiO_2 on degenerately doped silicon. Nanowire solutions were dropcast under dc electric fields (10^4 to 10^5 V/cm) to align nanowire arrays across pre-fabricated bottom electrodes. The number of nanowires spanning the electrode channel is controlled by varying the concentration and volume of the nanowire solution that is dropcast. Nanowires were dispersed in octane:nonane at a 1:1 (vol:vol) ratio with several drops of 10 wt% solution hexadecane-graft-polyvinylpyrrolidinone (HD-PVP) copolymer (M_n = ~7300) to improve the nanowires'

dispersability. The presence of HD-PVP is absolutely critical to preventing the nanowires

from aggregating and precipitating out of solution. Without the use of HD-PVP,

nanowires "crash out" of solution and will align as mats of densely clumped nanowires.

Devices were then well-washed in both ethanol and chloroform to remove excess

ligands, namely the ligands used in nanowire synthesis and the HD-PVP used to aid

nanowire dispersion. Removing surface-bound ligands improved FET transport

characteristics, whereas insufficient washing led to very poor FET current modulation.

Electric-field directed assembly was carried out in an MBraun nitrogen glovebox and all

solvents used were distilled and anhydrous.

Using metal salts of Cd-acetate and sodium selenide, we are able to change the

surface stoichiometry to be either more Cd-rich or Se-rich, respectively [Figure 7-2]. The

surface was thoroughly washed with ammonium chloride to remove excess Cd-acetate

or sodium selenide. This was done to ensure that only the surface is enriched and that

we were not forming a thick nanowire overcoating. We see that Cd-enrichment of the

surface leads to enhanced electron current and Se-enrichment of the surface leads to

electron suppression. Devices that were enriched with Cd also exhibited larger

hysteresis. This is consistent with results observed in Chapter 5, where unpassivated

dangling Cd and Se bonds can act as surface trap states to increase hysteresis. Samples

were also heated in order to improve the conductivity of samples, and similar trends as

the unheated samples still hold true. Changes in the surface stoichiometry were further

verified by infrared spectroscopy, using thiocyanate as a reporter molecule. Since the

SCN⁻ anion readily binds to dangling Cd bonds on the surface, thiocyanate was used to

quantitatively assess the concentration of Cd and Se on the NW surface in confirmation

with electrical measurements. Measurements also indicated that the surface of the

CdSe NWs initially start our Cd-rich.

Figure 7-2: Electric-field aligned colloidal CdSe nanowire field-effect transistors with
bottom contact gold electrodes atop an ODPA/Al$_2$O$_3$/SiO$_2$ dielectric stack. $I_D - V_G$
characteristics of different metal salt treatments for devices that are (A) unheated and
(B) heated at 250°C for 2 minutes.

Incorporating indium into CdSe NW FETs with different metal salt treatments

further sheds light on indium's doping mechanism [Figure 7-3]. Both CdSe NWs that

were left untreated and treated with an excess of Cd yielded similar current levels.

Devices treated with excess Cd also displayed significantly larger hysteresis, similar to

devices without indium incorporation. However, Se-enriched, indium doped CdSe NWs

showed a dramatic difference in conductivity from insulating to nearly semi-metallic

behavior upon annealing, unlike devices without indium incorporation. The Se-

enriched, indium doped CdSe NW behavior is similar to the high currents observed in

reports of CdSe NCs treated with $In_2Se_4^-$ molecular metal chalcogenides (MMCs).[14] We

attribute the improved currents to the presence of indium rather than heat, since

similar Se-enriched CdSe NW FETs did not show noticeable currents after heating [Figure

7-2(B)]. The presence of excess Se seems to have provided extra sites for the indium to

react with, leading us to believe that the formation of $In_2Se_4^-$ complexes occurred on the

surface of the NWs.

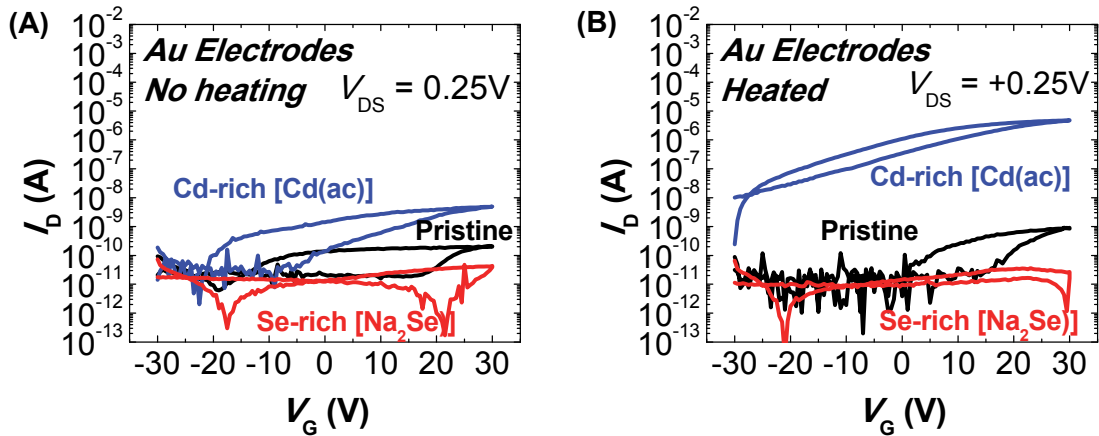

Figure 7-3: Electric-field aligned colloidal CdSe nanowire field-effect transistors with bottom contact indium/gold electrodes atop an $ODPA/Al_2O_3/SiO_2$ dielectric stack. I_D – V_G characteristics of different metal salt treatments for devices that are (A) unheated and (B) heated at 250°C for 2 minutes.

We further tested this theory by treating the surface of the CdSe NWs with the

metal salt sodium sulfide to enrich the NW surface with sulfur [Figure 7-3]. Nanowires

were washed with ammonium chloride once again to remove excess metal salts.

Without indium incorporation, similar to nanowires that were enriched with Se, the

devices showed insulating behavior. With indium incorporation, this yielded devices

with high current and high I_{ON}/I_{OFF} ratios, similar to previously reported thiocyanate-

exchanged CdSe NCs.[15,16] Metal-SCN bonds are known to decompose at 200°C, leaving

behind metal a sulfide bond.[17] Similar to the reaction with dangling Se bonds, dangling

S-bonds would have reacted with indium to form an $In_2S_4^-$ complex. We believe the

formation of indium complexes ($In_2Se_4^-$ and $In_2S_4^-$) are primarily responsible for the high
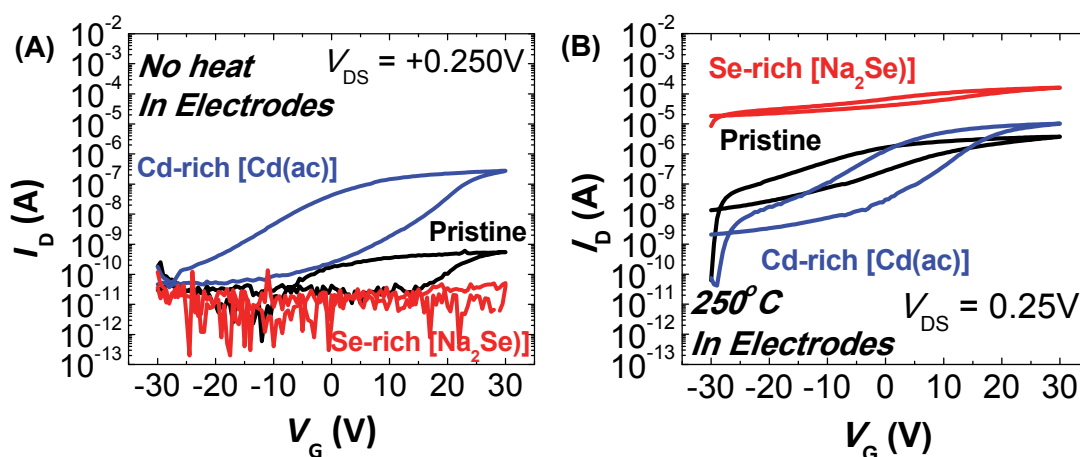
carrier densities observed in CdSe nanostructures.
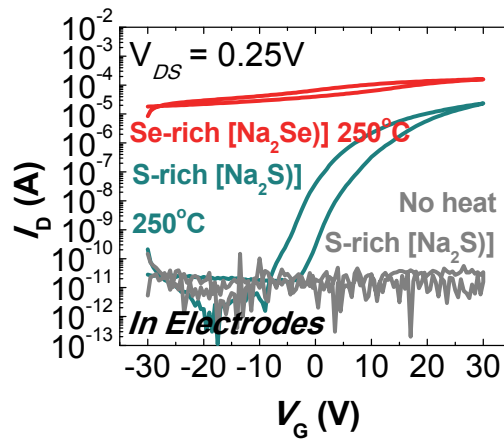
Figure 7-4: Electric-field aligned colloidal CdSe nanowire field-effect transistors with
bottom contact gold electrodes atop an ODPA/Al_2O_3/SiO_2 dielectric stack. $I_D − V_G$
characteristics of different metal salt treatments for devices that are (A) unheated and
(B) heated at 250°C for 2 minutes.

Future work will involve doing low temperature measurements to confirm the

position of indium complexes in the nanostructure. With the recent success of indium

doping in nanocrystals of CdSe to increase the carrier concentration,[16] it would be

beneficial to know if the dopant sits on the surface or in the bulk. Since indium has

been reported to diffuse along grain boundaries to passivate trap states arising from

dangling bonds in thin-films of polycrystalline CdSe,[18–20] we similarly expect indium to

diffuse to the NC surface and act as a "remote dopant" rather than being incorporated

in the bulk.
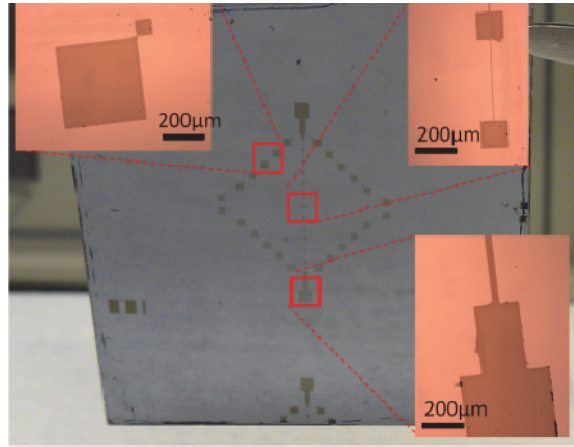
Figure 7-5: Photograph of photo-lithographically patterned CdSe NC solid on a 2 cm x 2 cm wafer. (inset) Higher resolution optical micrographs.

In collaboration with Yuming Lai, we have used photolithography to pattern the NC semiconductor layer. Patterning the CdSe NC solid is important to reduce cross-talk between constituent FETs and lower device OFF currents. After spin-coating a uniform CdSe NC thin film solid, photoresist will be spin-cast and photopatterned. We have found that tetramethylammonium hydroxide (TMAH) is an effective solvent, in this case a wet etchant, to delaminate thiocyanate-exchanged CdSe NC thin films. Desired active semiconductor NC solid areas will be protected by a film of photoresist, while photoexposed regions of photoresist and the underlying CdSe NC solid will be lifted-off, leaving behind well-patterned active areas, as shown in preliminary experiments in Fig. 7-8. We have demonstrated photopatterning to the 5 μm resolution (linewidth, Figure 7-8, upper right image) of the features on the parent photomask.

Future work will involve applying this process to the large-area fabrication of

NCICs. Complementary masks will be designed for device electrodes to implement

photolithography as an avenue to restrict the semiconductor NC layer to the channel

region of devices. The limits of the OFF currents achievable in discrete devices and their

subsequent impact in the design and performance metrics toward low-power, low OFF

current, integrated circuits will also have to be characterized in detail.

7-3:   Photolithography of CdSe Devices

In collaboration with Dr. Ji-hyuk Choi, Yuming Lai and Soong-Ju Oh, we developed processes to photolithographically pattern device contacts on top of the CdSe NC channel layer. Photolithographic patterning allowed us to reduce the device overlap capacitance and to scale down device size. To pattern NC solids, substrates of CdSe NC thin film solids were initially heated in the glovebox at 200°C for five minutes (as we used in Chapter 5 to increase interparticle coupling) and then placed in the atomic layer deposition (ALD) chamber to coat a 10 Å thin, permeable oxide uniformly over the film at 150°C. Heating at 200°C decomposes the thiocyanate ligand, making the CdSe NC layer significantly less soluble to the solvents used in the photolithography process, while the thin ALD layer acts as a porous net to further prevent the CdSe NC film from delaminating (especially from the TMAH, which is used as a developer). This porous film also allows the source-drain electrodes to still make effective contact with the CdSe NC thin film.
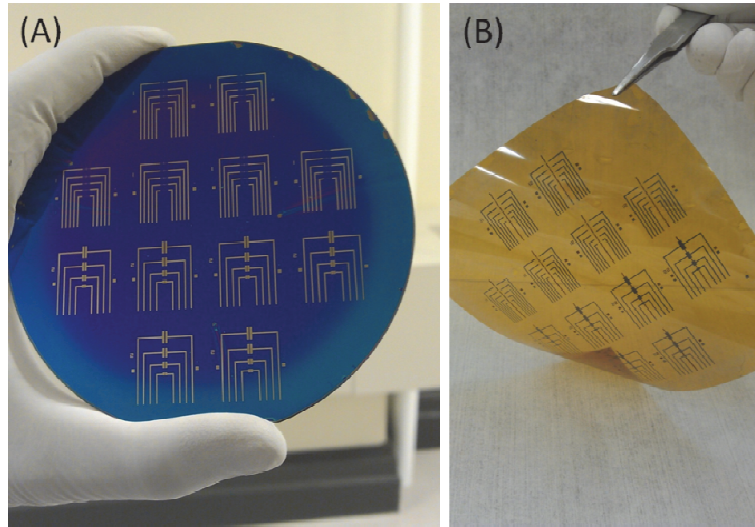
Figure 7-6: Photographs of photolithographically patterned source and drain electrodes on a uniform, spin-coated CdSe NC thin film solid on (A) an Al_2O_3 ALD coated, thermally oxidized, 4" n+ Si wafer, forming an array of common, back-gated FETs and (B) Al_2O_3 ALD coated, photolithography patterned Al electrodes forming an array of back-gated FETs on a 4 inch square Kapton® substrate.

Standard photolithography techniques were employed outside of the glovebox to pattern source and drain electrodes on the CdSe NC film, followed by thermal deposition of indium and gold for our contacts. Lift-off is done outside the glovebox, followed by a gentle annealing for 10 minutes at 250°C inside the glovebox to facilitate doping with indium (even with the thin film of ALD). Figure 7-9(A) shows an example of 54 CdSe NC FETs fabricated across a 4" n+ silicon wafer. The lithographically fabricated devices gave us 100% yield, exhibiting an average mobility of 27 $cm^2V^{-1}s^{-1}$, as we have realized previously for NC FETs on back-gated Si wafers with an Al_2O_3/SiO_2 gate dielectric layer. We have begun to extend this process to 4" square flexible substrates bearing photolithographically patterned Al gate lines with a thin ALD Al_2O_3 gate

dielectric layer for low-voltage operation [Figure 7-9(B)], as we have previously defined

by shadow masks in Chapter 6. The process has not been optimized yet, but has already

yielded promising results.

Future work will involve developing photolithography on plastic substrates for

discrete devices and apply the fabrication to the large-area NCICs. While current

parasitic capacitances arising from the use of shadow masks limited the theoretical

signal delay per stage of our ring oscillator to 170 μs, photolithography would allow us

to reduce the switching time to 9 μs, a significant leap forward that would demonstrate

the scalability of this class of materials.

7-4:   Nanoimprinting of CdSe Devices

Instead of using expensive and time-consuming e-beam lithography to fabricate small channel transistors, nanoimprinting has presented itself as a low-cost, high-volume, large-area and high-resolution patterning technique. In collaboration with Dr. Sung-Hoon Hong, we have used nanoimprint lithography (NIL) to print sub-micron CdSe NC-FETs. With the miniaturization of the transistor, we also have had to develop the appropriate device architectures to address the significant short-channel effects that arise with scaling: 1) increased contact resistance,[21] 2) electrostatic scaling[22] and 3) semiconductor isolation.[22] The increased contact resistance that arises with smaller channel lengths can be reduced with proper electrostatic scaling (typically a channel length to oxide thickness exceeding a 10:1 ratio) to more significantly pull down the barriers to charge injection. However, we will still need to understand the origin of contact resistance at these small scales. This scaling is also necessary to maintain current modulation and measure appreciable device currents.[22]
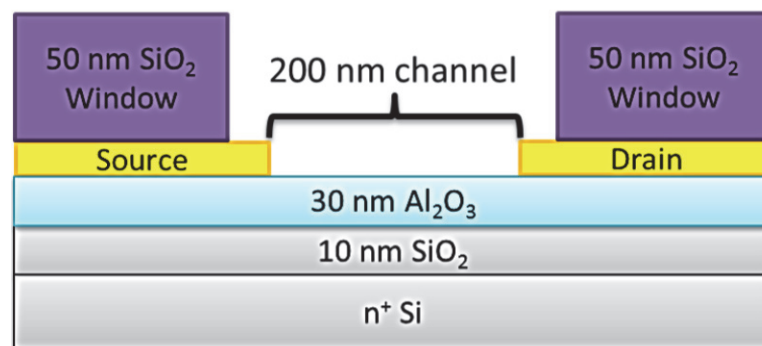

Figure 7-7: Schematic cross section of single CdSe FET. All structures were defined by nanolithography.

Figure 7-5 is a schematic of the device structure we utilized. All elements of the structure were defined by NIL, with the appropriate metal or insulator deposited for different layers. CdSe NCs were solution-exchanged then spincast everywhere, but the SiO_2 windows defined exact placement of NC thin films to form the sub-micron channel FETs. Without the SiO_2 windows, additional currents from the larger contact pads would swamp out the significantly smaller currents from the nanoelectrodes [Figure 7-6(A, B)].
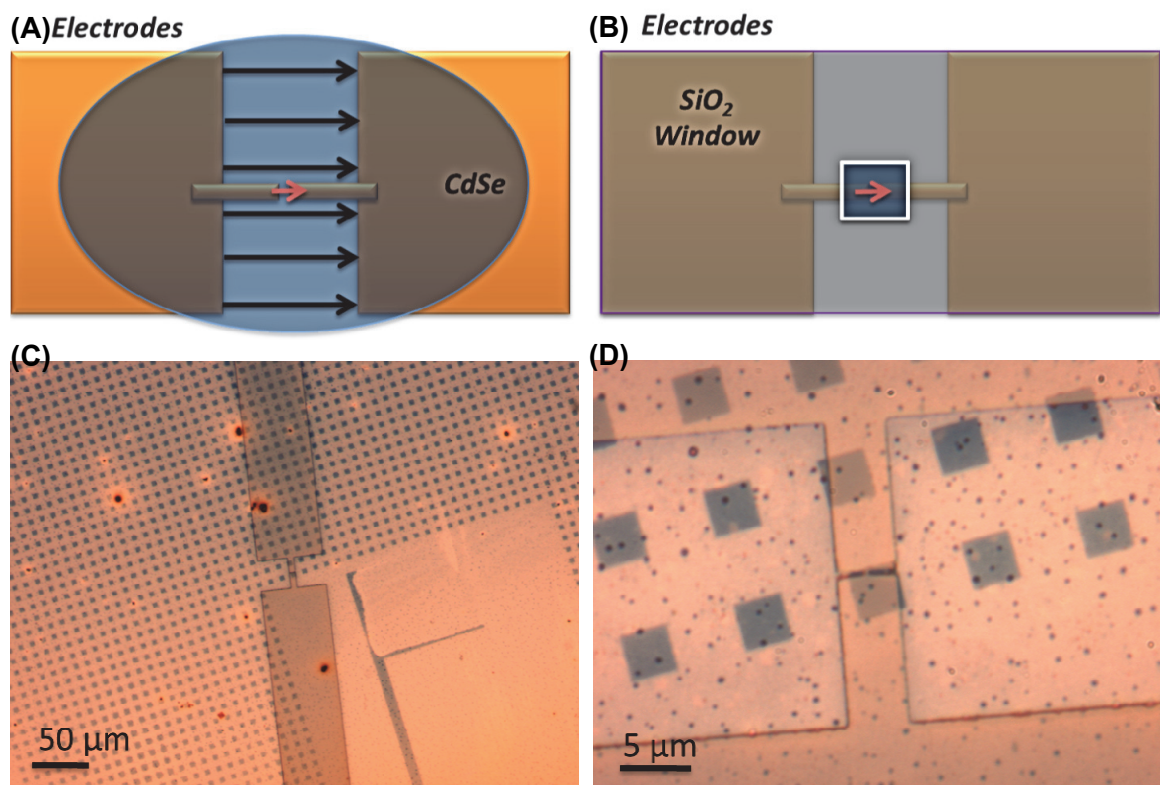
Figure 7-8: Schematic of small scale devices with (A) non-isolated and (B) isolated semiconducting CdSe NC channels. Optical images of spincast CdSe NC thin films on FET structures with SiO_2 windows at (C) low and (D) high resolution. The SiO_2 window is necessary to define and isolate the semiconducting channel from the rest of the electrode, and ensures that the measured electrical current is arising from the nanometer channels, rather than the large contact pads.

We have made bottom-contact, CdSe NC-FETs with sub-micron channel lengths [Figure 7-6 (C, D)]. These devices show a modest mobility with current modulation over three orders of magnitude [Figure 7-7(A, B)].

Figure 7-9: (A) I_D-V_{DS} and (B) I_D-V_G characteristics of CdSe NC FETs with channel lengths of ~200 nm and widths of ~200 nm to give a W/L ratio of 1. In the future, the channel width to length ratio must also be redesigned to exceed a 10:1 ratio to avoid fringing of the electric field at the edges of the channel. This will give rise to non-idealities and higher than expected mobility values. Electrodes were fabricated atop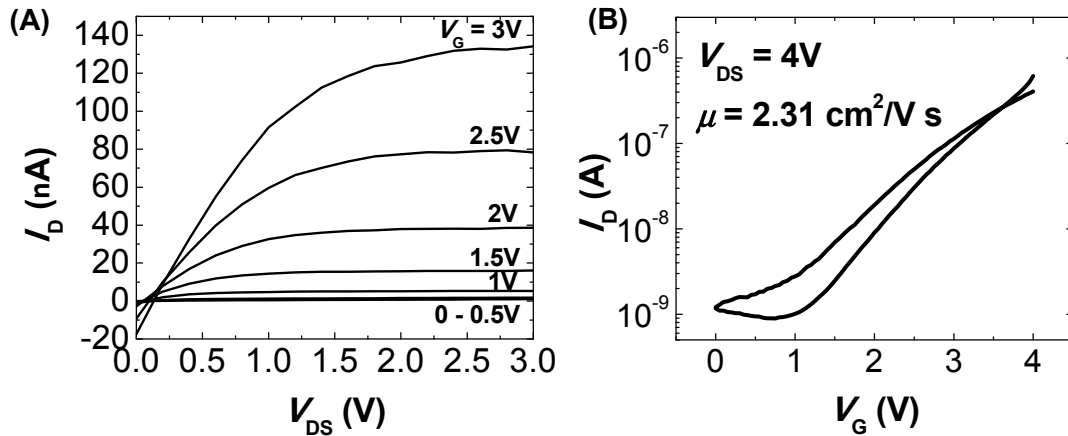 a dielectric stack of 30 nm of Al_2O_3 and 10 nm of thermal SiO_2 to give a total unit capacitance of about 150 nF/cm^2. A channel length of 200 nm would allow a maximum oxide thickness of 20 nm of SiO_2, yielding a total unit capacitance of 172 nF/cm^2. In the future, the gate oxide will need to be redesigned with a higher dielectric constant or be thinner to increase the unit capacitance beyond 172 nF/cm^2 for a 200 nm channel length device. Otherwise, given a gate oxide with unit capacitance of 150 nF/cm^2, the minimum allowable channel length would be 230 nm.

Future work will involve applying this technique over large area and increasing the mobility to values observed in micron-length channels. NIL also allows us to fabricate high resolution shapes and morphologies that can be investigated using this technique.

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7-5:   Mechanical Stability of Flexible Devices

While we have shown that CdSe NC films translate well onto plastics in Chapter 6, assessing the mechanical stability of these thin films is just as important. Simply showing device performance of flexible substrates on a flat surface does not adequately take advantage of the bendability of plastic. The ultimate goal is to have these devices be tightly rolled with a bending radii that is sub-millimeters, bent around sharp edges (e.g. to 100 μm) and repeatedly creased without significant device degradation. However, initial measurements on plastic substrates under both tension and compression suffer from a simultaneous increase in the threshold voltage, hysteresis and the sub-threshold swing. In addition, when the substrate is returned to its normal flat position, even though the device still operates like an FET at low-voltages, we see that we have irreversibly damaged it and does not return to its pre-bent characteristics. We also collected the gate capacitance under both tension and compression, and realize it affected the estimation of carrier mobilities and threshold voltage. The large mechanical strain also increased the leakage of the gate dielectric stack.

This is a limitation not just confined to NC thin films, but is a problem more general to all thin-film transistors on flexible platforms. It was recently reported by Someya[23] for bending applications, devices and circuits need to be encapsulated with a thick enough passivation layer so that the semiconducting layer lies in a neutral strain position, where the bending induced by compression and tension cancel each other.

Future work will involve similarly encapsulating CdSe NC devices to ensure the film would not be subject to any strain, be highly stable to sharp and repetitive bending, and maintain its high performance.   We found that encapsulating plastic devices in a thin layer of ALD (50 nm of Al_2O_3), which was originally developed by Dr. Ji-hyuk Choi to passivate the device and allow operation in air, can also increase mechanical stability of these devices. We will explore other commonly used passivation layers, such as parylene-C, CYTOP^{TM}, and polyimide that could be readily used to scale up to thicker encapsulation films to match the thickness of flexible substrates.

7-6: *References*

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CHAPTER 8:   Concluding Remarks

Evaluating if colloidal nanostructures can be used as a viable semiconducting material for large area electronics and more complex integrated circuits has been a long standing question in the field. Over the twenty years, we have seen tremendous growth and understanding of charge transport in these quantum-confined systems. With that knowledge, we have seen the successful demonstration of these nanostructured materials for a wide range of device technologies, ranging from field-effect transistors (FETs), thermoelectrics, photovoltaics and photodetectors. In this thesis, we initially began with colloidal nanowire (NWs) FETs as a simple, but effective platform to further elucidate the role of interfaces on charge transport for successful device integration and the application of large-area electronics.

In Chapter 2 and 3, we fabricated ambipolar, PbSe NW FETs to uncover their intrinsic electronic properties. Great care was taken to avoid unintentional doping, and we were able to successfully identify oxygen and hydrazine as effective p and n-type dopants. Combined with our understanding of the band-energy alignment at the metal-semiconductor interface, we were able to control the carrier types, ranging from unipolar p-type, ambipolar to unipolar n-type. Taking advantage of the control we have over the electronic properties in PbSe NW FETs, we fabricated the first PbSe NW inverters that show amplification and the initial demonstrations that these nanostructured materials could be used in more complex integrated circuits.

In Chapter 4, we used the same PbSe NW FET platform to further uncover its intrinsic properties and identify the causes of hysteresis in PbSe NW FETs. PbSe nanostructures were found to not only be extremely sensitive to surface ligands and bound oxygen, but to surface non-stoichiometry, since as-synthesized PbSe nanostructures are known to have an excess amount of Pb on the surface. Non-stoichiometry is being explored by our group as a means of doping in lead-chalcogenide nanostructures. At the semiconductor-gate dielectric interface, we found that the presence of surface bound water only suppressed electron currents, but did not give rise to hysteresis. We have identified that the semiconductor/dielectric interface is largely responsible for hysteresis and found that a surface modified gate dielectric stack [octadecylphosphonic acid (ODPA) self-assembled monolayers (SAMs) on Al_2O_3] exhibits low-hysteresis FET operation. Exploration of alternative combinations of gate dielectric layers and SAM chemistries and/or surface modification of the NWs will be a useful tool to reduce hysteresis in other nanostructured systems. Furthermore, we were able to scale down the dielectric stack on flexible substrates to show low-hysteresis and low-voltage PbSe NW FET operation on plastics and demonstrate that this class of colloidal materials could be used in large area flexible electronics.

In Chapter 5, in collaboration with the Kagan and Murray groups, as well as NIST, we were able to fabricate high-performance CdSe nanocrystal (NC) FETs. Through the use of a novel ligand, ammonium thiocyanate, we drastically enhanced interparticle electronic coupling to form extended electronic states in NC solids. Indium introduced

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by thermal evaporation and diffusion, dopes and passivates the surface of CdSe NC

solids, increasing the carrier concentration. Using our knowledge of engineering

dielectric interfaces, we reduced the trap density by using an Al_2O_3/SiO_2 dielectric stack.

These FETs exhibit mobilities exceeding 15 $cm^2V^{-1}s^{-1}$, low subthreshold swing and an

I_{ON}/I_{OFF} >10^6. Additionally, the use of non-corrosive ligand ammonium thiocyanate and

mild annealing to promote indium diffusion is compatible with flexible electronics.

Combining the high-mobility CdSe NC solids with our low-voltage plastic

platform, we were able to translate the exceptional device performances on flexible

substrates. This enabled us to construct, for the first time, nanocrystal integrated

circuits (NCICs) constructed from multiple well-behaved, high-performance NC-FETs.

These transistors operate with small variations in device parameters over large area in

concert. We demonstrated NCIC inverters, amplifiers and ring oscillators. Device

performance is comparable to other emerging solution-processable materials with

similar channel lengths (40 μm) and low-voltage operation, demonstrating that this class

of colloidal NCs as a viable semiconducting material for large area electronic

applications. With recent developments in our group to scale down these devices and

minimize parasitic capacitance to further improve device performance in Chapter 7,

plenty of work still needs to be done in order to realize the full potential of these

materials. With exciting new developments and discoveries in the field to inspire us

every day, it is my hope that the work in this thesis will encourage others to do the

same.