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Comments

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ISSCC Student Research Preview Debuts 22 Up-and-Coming Careers

90 Attend Event in 2010

The ISSCC Student Research Preview on Sunday afternoon, 7 February 2010, at the Society's flagship conference, included three consecutive sessions:

- Energy Efficient ADCs and Frequency Synthesis Circuits
- Innovations in RF and Wireline Circuits
- Emerging Technologies and Applications.

Founded as a pilot in 2008 by then Vice-Chair Anantha Chandrakasan and Laura Fujino, director of ISSCC

Publications, the principal aim of this event is to introduce promising young researchers to the requirements and rewards of ISSCC participation and to promote peer-group networking at an early stage in their careers. The 2010 Preview program featured 24 five-minute presentations and drew a total of nearly 90 attendees.

According to Jan Van der Spiegel, chair of the 2010 program, "The session brought together some of the best graduate students and pro-

vided the audience with a unique opportunity to interact with them and gain a concise overview of the rich palette of projects that are being conducted at university labs worldwide. The presentations were of exceptional quality, covering a spectrum of topics, ranging from low-power circuits, RF and MEMS to CNT circuits. I expect many of these short presentations to result in full-fledged presentations at future ISSCCs."

—Katherine Olstein

SINGLE-ENDED-TO-DIFFERENTIAL AND DIFFERENTIAL-TO-DIFFERENTIAL CHANNEL-SELECT FILTERS BASED ON PIEZOELECTRIC AIN CONTOUR-MODE MEMS RESONATORS FOR MULTI-FREQUENCY RECONFIGURABLE RF TRANSCEIVERS

Key issues for the realization of next-generation wireless communication systems are efficient spectral utilization, low-power consumption, and high-level integration. To adaptively use the electromagnetic spectrum, transceivers will need to selectively process radio frequency (RF) signals over a wide frequency range and rapidly switch from one band to another. It would be very inefficient to realize this multifrequency/multiband reconfigurable RF front end by simply putting multiple standard transceivers (for example, Global System for Mobile communications (GSM), Personal Communications Service (PCS), Code Division Multiple Access 2000 (CDMA2000), Wideband Code Division Multiple Access (WCDMA)) together on a single chip without any reutilization or optimization. Therefore we propose a non-traditional RF architecture (Figure 1) that can perform channel selection and frequency synthesis over a broad range of frequencies and can be easily reconfigured so that all standards can be unified into one single transceiver.

In this new RF architecture, both narrow-band channel-select filters and low-phase-noise local oscillators require high quality factor (Q) on-chip passive components, which are extremely hard if not impossible to make

using conventional integrated circuit (IC) technologies. A promising solution for the synthesis of high- Q , on-chip and CMOS compatible RF components is the use of RF microelectromechanical systems (MEMS). RF MEMS has been the topic of significant research for over a decade. Several groups have been developing high- Q MEMS resonator technologies based on electrostatic and piezoelectric transduc-

tion mechanisms that are capable of providing multiple frequencies of operation on the same silicon substrate, in contrast with conventional quartz crystal or film bulk acoustic resonator (FBAR) technologies for which only one frequency per substrate is possible. Among them, the piezoelectric aluminum nitride (AlN) contour-mode RF MEMS technology that has been developed by our group stands out as the only



Chengjie Zuo, with 2010 Student Research Preview Committee Member CK Wang, after being recognized at the SRP for receiving the Society's selective Predoctoral Fellowship for 2009-2010. Mr. Zuo presented an overview of his research at the session.

technology that can reliably span a wide frequency range from 10 MHz up to several gigahertz (operating in the fundamental mode of mechanical vibration) on the same silicon chip, and simultaneously offer high Q (1,000–4,000) and low motional resistance (25–500 Ω) in air, which allows the devices to be easily interfaced to conventional electronics without the need for special circuit design or complicated matching networks. Based on this technology, we have implemented narrow-band, low-insertion-loss, and high-rejection single-ended channel-select filters from 100 MHz to 2 GHz and multifrequency low-phase-noise CMOS oscillators from 100 MHz to 1 GHz. Especially, the 1 GHz MEMS oscillator has proven to satisfy the stringent phase noise requirement of GSM UHF local oscillators. We have also demonstrated that piezoelectric AlN RF MEMS switches can be monolithically fabricated and integrated with AlN contour-mode resonators and filters on the same chip and effectively used to turn on/off those devices for direct reconfiguration.

The work presented at the ISSCC 2010 Student Research Preview further advances piezoelectric AlN contour-mode RF MEMS technology by being the first demonstration of single-ended-to-differential and differential-to-differential (S2D and D2D) channel-select filters based on single-layer (SL) and dual-layer-stacked (DLS) piezoelectric AlN contour-mode MEMS resonators. The key filter performance in terms of insertion loss (as low as 1.4 dB), operating frequency (250–1280 MHz), and out-of-band rejection (up to 60 dB) represents a significant advancement over all other state-of-the-art RF MEMS differential filters. The fabrication process, namely stacking of two piezoelectric AlN layers (600 nm each) and three Pt electrode layers (100 nm each), is fully compatible with the previously demonstrated AlN RF MEMS switch process (also post-CMOS compatible), which makes it possible to implement multifrequency switchable filter banks on a single chip. The S2D configuration is able to combine three different functions of a balun, a filter, and an impedance transformer in a single MEMS structure and only takes on a very small form factor (60 × 200 μm), as shown in Figure 2. Compared with single-ended AlN contour-mode MEMS filters, the fully differential solution (D2D) achieves much lower insertion loss (from 4.2 to 1.8 dB) and comparable rejection and shape factor in a second order filter instead of third (which also means a smaller form factor for the device), while additionally

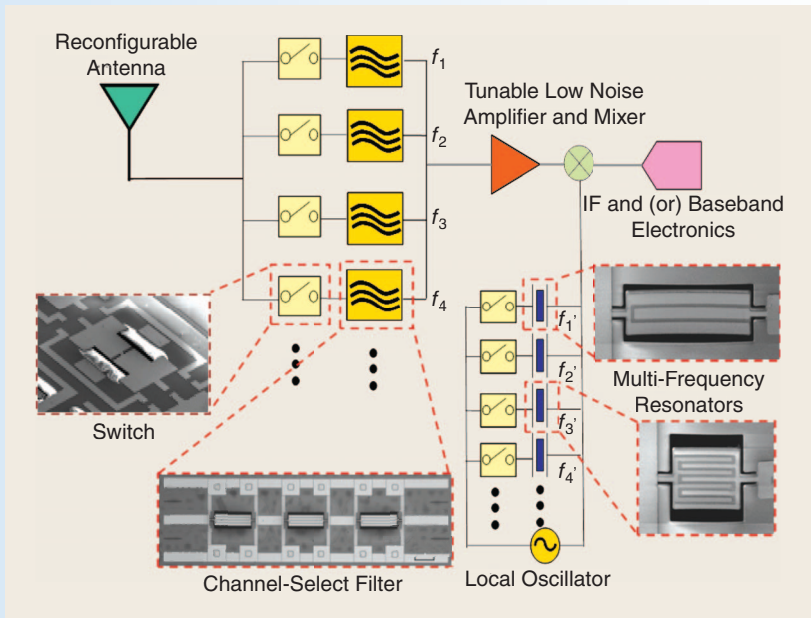


FIGURE 1. Proposed new multifrequency reconfigurable RF transceiver architecture that does channel selection and frequency synthesis over a broad range of frequencies.

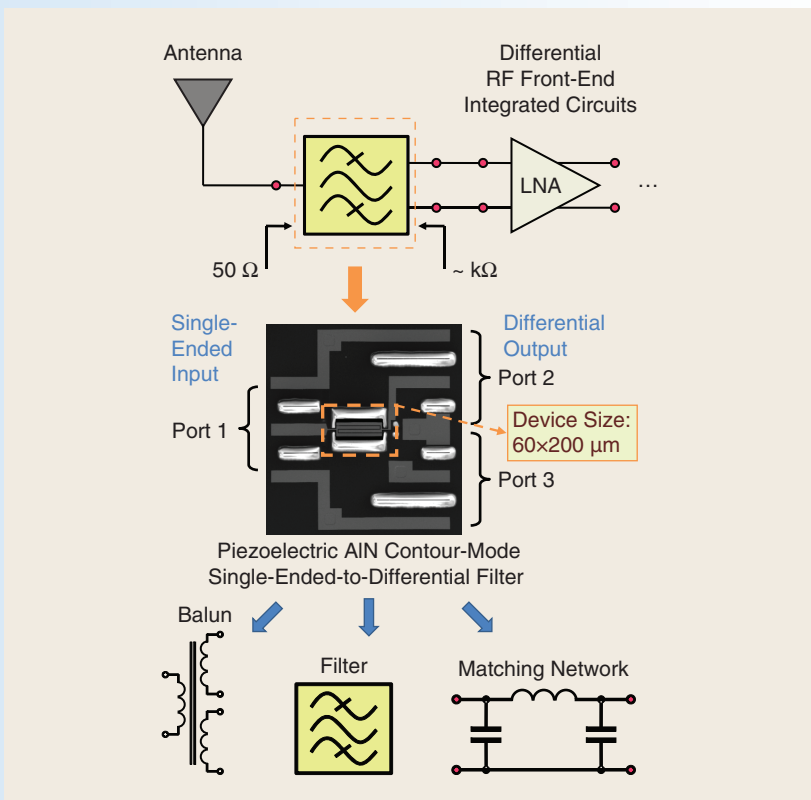


FIGURE 2. Schematic illustration showing how balun, narrow-band filter, and impedance transformer functions are combined in a single-ended-to-differential (S2D) AlN contour-mode MEMS filter.

providing common-mode suppression. These unique features have the potential to revolutionize the field of RF and microwave IC design by enabling MEMS-

IC codesign and the development of unconventional and low-power RF architectures.

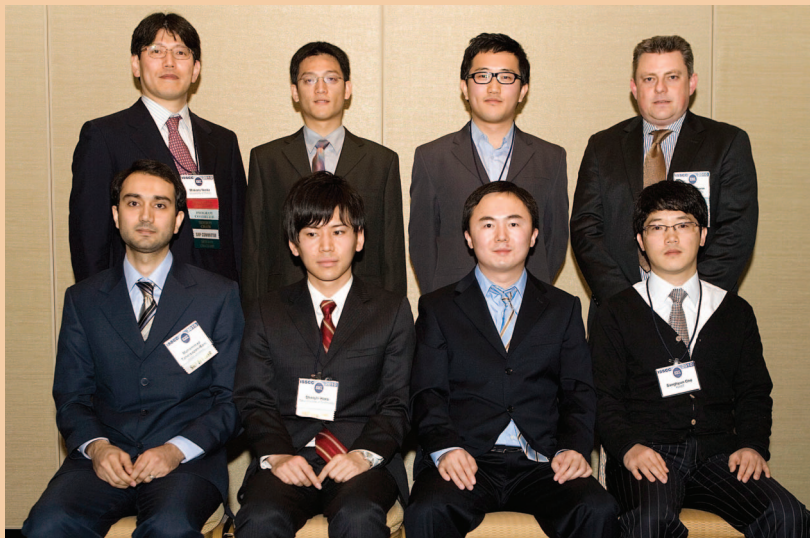
—Chengjie Zuo

Session 1: Energy Efficient ADCs and Frequency Synthesis Circuits

Session Chair: Makoto Ikeda, University of Tokyo, Japan.

Session Cochair: Boris Murmann, Stanford University, California.

- Le Wang, University of California Santa Barbara, Oversampled modulator tailored for biomedical applications.
- Mohammad Taherzadeh-Sani, McGill University, Montreal, Canada, Reconfigurable pipeline ADC.
- Sang-Hyun Cho, KAIST, Daejeon, Korea, Novel correction technique for large dynamic setting errors.
- Hsien-Ku Chen, National Taiwan University, Taipei, CMOS-multiband PLL for mm-wave radios.
- Pyoungwon Park, KAIST, Daejeon, Korea, Wide-band fractional-N frequency synthesizer.
- Shoichi Hara, Tokyo Institute of Technology, Japan, Quadrature frequency synthesis.



Members of the first Student Research Preview session were (from left back row) SRP Cochair and Session 1 Chair Makoto Ikeda, Kuan-Ting Lin, Pyoungwon Park, and Session 1 Associate Chair Boris Murmann. In front from left: Mohammad Taherzadeh-Sani, Shoichi Hara, Le Wang, and Sanghyun Cho.

Session 2: Innovations in RF and Wireline Circuits

Session Chair: Shahriar Mirabbasi, University of British Columbia, Vancouver, Canada.

Session Cochair: SeongHwan Cho, KAIST, Daejeon, Korea.

- Niklas Zimmermann, RWTH Aachen University, Germany, System concept and circuit implementation of an RF-DAC based multistandard, multimode transmitter.
- Karim Allidina, McGill University, Montreal, Canada, A compact and low power UWB transceiver with fast synchronization scheme.
- Jonathan Muller, ISEN, Lille, France, A high-speed FIR filter for direct digital-to-RF 60 GHz transmitter.
- Ruida Yun, Tufts University, Medford, Massachusetts, An inductor-less 10 Gb/s TIA for optical interconnects.
- Liang Wu, Hong Kong University of Science and Technology, China, A 24 GHz and 60 GHz dual band VCO using standing wave architecture.



Participants in the second Student Research Preview Session were (from left back row) Session Chair Shahriar Mirabbasi, Jonathan Muller, Chengjie Zuo, Karim Allidina, and Session 2 Associate Chair SeongHwan Cho. In front from left: Liang Wu, Niklas Zimmermann, Ruida Yun, and Chintan Thakkar.

- Chintan Thakkar, University of California Berkeley, Multi-Gb/s decision feedback equalizers for 60 GHz transceivers.
- Chengjie Zuo, University of Pennsylvania, Philadelphia, A first demonstration of channel select filters based on a CMOS compatible RF MEMs technology.

Session 3: Emerging Technologies and Applications

Session Chair: Eugenio Cantatore, Eindhoven University of Technology, Eindhoven, The Netherlands. Session Cochair: Vincent Gaudet, University of Alberta, Edmonton, Canada.

- Jinwook Oh, KAIST, Daejeon, Korea, A neuro-fuzzy inference engine.
- Tushar Krishna, Massachusetts Institute of Technology, Cambridge, A low-power network-on-chip design.
- Matthew Turnquist, Helsinki University of Technology, Espoo, Finland, Digital subthreshold techniques.
- Fopefolu Folowosele, John Hopkins University, Baltimore, Maryland, A 3-D-integrated neuron system.
- Thejas, Indian Institute of Science, Bangalore, India, High-resolution inertial sensors.
- Berkehan Ciftcioglu, University of Rochester, New York, Intra-chip optical interconnect technologies.



Session Three participants were (back row from left) Session Chair Eugenio Cantatore, Tushar Krishna, Thejas, Yu-Huei Lee, Berkehan Ciftcioglu, and Session Three Associate Chair Vincent Gaudet. Front row: Jinwook Oh, Noah Sturcken, Albert Lin, and Matthew Turnquist.

- Albert Lin, Stanford University, California, The evolution and application of carbon nanotubes.
- Noah Sturcken, Columbia University, New York, Power-management techniques based on magnetic materials.
- Yu-Huei Lee, National Chiao Tung University, Taiwan, A DVS Embedded power management for high efficiency integrated SoC in UWB system.

Industry Leaders and Academic Visionaries Assess the Economics of the Semiconductor Industry in 2025

The semiconductor industry has relied on Moore's law as a guiding economic principle for more than four decades. However, the economics of the solid-state circuit revolution

appear to be reaching their limits, with fabrication facility costs rising exponentially and semiconductor sales increasingly becoming a larger portion of electronics industry sales.

limits of this economic trajectory, industry leaders and academic visionaries met in an evening panel session that attracted as many as 300 attendees at the International Solid-State Circuits Conference (ISSCC) in San Francisco on 9 February 2010.

Digital Object Identifier 10.1109/MSSC.2010.936616

To brainstorm how semiconductor businesses may address the long-term



Presenters at the ISSCC evening panel "The Semiconductor Industry in 2025" were (from left) Tadahiro Kuroda (professor, Keio University), Pierre-Yves Lesaicherre (Senior VP and GM, NXP), Sreedhar Natarajan (director, TSMC), Gary Patton (VP, IBM R&D), Charlie Sodini (professor, MIT), Wally Rhines (chair and CEO, Mentor

Graphics), Mark Bohr (senior fellow, Intel), and Moderator Siva Narendra of Tyfone (Portland, Oregon) at the far right. The event was organized by Azeez Bhavnagarwala (IBM, Yorktown Heights, New York), Shekhar Borkar (Intel, Hillsboro, Oregon), and Takayasu Sakurai (University of Tokyo).