Penn Libraries
UNIVERSITY of PENNSYLVANIA

University of Pennsylvania
ScholarlyCommons

Departmental Papers (ESE)

Department of Electrical & Systems Engineering

7-1-2003

A Fully Integrated CMOS Phase-Locked Loop With 30MHz to 2GHz Locking Range and ±35 ps Jitter

Chao Xu
University of Pennsylvania

Winslow Sargeant
University of Pennsylvania

Kenneth R. Laker
University of Pennsylvania, laker@seas.upenn.edu

Jan Van der Spiegel
University of Pennsylvania, jan@seas.upenn.edu

Follow this and additional works at: http://repository.upenn.edu/ese_papers

Part of the Electrical and Computer Engineering Commons

A Fully Integrated CMOS Phase-Locked Loop With 30MHz to 2GHz Locking Range and ±35 ps Jitter

Abstract

A fully integrated phase-locked loop (PLL) fabricated in a 0.24μm, 2.5v digital CMOS technology is described. The PLL is intended for use in multi-gigabit-per-second clock recovery circuits in fiber-optic communication chips. This PLL first time achieved a very large locking range measured to be from 30MHz up to 2GHz in 0.24μm CMOS technologies. Also it has very low peak-to-peak jitter less than ±35ps at 1.25GHz output frequency.

Disciplines

Electrical and Computer Engineering

Comments

A FULLY INTEGRATED CMOS PHASE-LOCKED LOOP WITH 30MHZ TO 2GHZ LOCKING RANGE AND ±35PS JITTER

Chao Xu, Winslow Sargeant, Kenneth R. Laker, Jan Van der Spiegel

Department of Electrical Engineering, University of Pennsylvania
200 S 33rd Street, Philadelphia, PA 19104, USA
Email: chaoxu@seas.upenn.edu

[Abstract] A fully integrated phase-locked loop (PLL) fabricated in a 0.24μm, 2.5v digital CMOS technology is described. The PLL is intended for use in multi-gigabit-per-second clock recovery circuits in fiber-optic communication chips. This PLL first time achieved a very large locking range measured to be from 30MHz up to 2GHz in 0.24μm CMOS technologies. Also it has very low peak-to-peak jitter less than ±35ps at 1.25GHz output frequency.

1. INTRODUCTION

In recent years, there has been a significant research effort in the area of high-speed electronics for communication. High speeds are required in order to take full advantage of the extremely broadband capabilities of optical fibers. At the same time, the old communication protocols that use different low speeds are still being widely used. In order to be flexible for the different protocols, a large locking range PLL clock generator is highly needed. In particular, fully integrated CMOS solutions are sought for practical systems to reduce cost and improve reliability. Although a lot of different speed PLLs have been reported recently [1][2][3][4][8], a large locking range from 30 MHz to 2GHz CMOS PLL has not been seen in 0.24μm CMOS technologies. In addition to a large locking range, the generated clock signals are used to drive sampling circuits in which the random variation of the sampling instant, or jitter is a critical performance parameter. The low jitter PLL is becoming more and more

critical to the performance of the communication system.

In this paper, a fully integrated PLL, with a large locking range from 30 MHz to 2 GHz, peak–to-peak jitter noise ±35ps at 1.25GHz output frequency is descried. In section 2, a new dual-looped architecture is described. In section 3, the design of the voltage control oscillator (VCO) with large tuning range and low jitter noise is presented. The other PLL building blocks such as phase frequency detector (PFD), charge pump and dividers are described in section 4. Finally, measurement results of the chip and conclusions are given in section 5 and 6.

2. DUAL–LOOPED PLL ARCHITECTURE

A block diagram of a classical single-looped PLL is shown in Figure 1(a). There are some limitations in this single-looped architecture. Since the control voltage of a VCO is constraint by the supply voltage, the gain of the VCO need to be large in order to achieve a large locking range. A large gain of a VCO amplifies the noise and increases the PLL output jitter. So there is a trade-off between the large locking range and the low jitter requirement in the classical architecture.

In order to achieve a large locking range and low output clock jitter, a new dual-looped architecture was used in the design. The block diagram of this architecture is depicted in Figure 1(b). The new dual-looped PLL architecture consists of two classical single-looped PLLs, a master loop and a slave loop. The master loop achieved a large locking range by using a large gain VCO. Then the locked master loop set the slave loop's
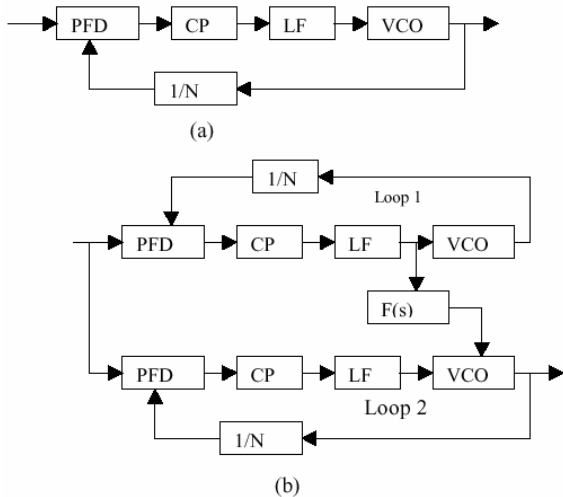
Figure1 (a) Classical single-looped PLL
(b) New dual-looped PLL architecture

frequency close to the locking frequency. The slave loop achieved the final lock by using a low gain VCO. The output clock jitter is reduced by the low gain slave loop. This new architecture dramatically increased the PLL locking range and reduced the output clock jitter at the same time.

2.1 Improving the locking range

In a single-looped PLL, the locking range is limited by the tuning range of the VCO. The dual-looped PLL architecture increased the locking range of the slave loop through the master loop providing the DC control voltage to the slave VCO to bring its running frequency close to the locking frequency. The slave loop itself only need to finely tune the VCO to get the final locking. Shown in Figure 1(b), one of the control voltages of the VCO in the slave loop is from the output of the loop filter of the master loop filtered by a narrow-banding filter F(s). This DC control voltage minimizes the frequency error in the slave loop and let the slave loop be able to lock to the designed frequency with a small gain VCO. In this way, the new architecture increased the overall PLL locking range.

2.2 Reducing the jitter noise
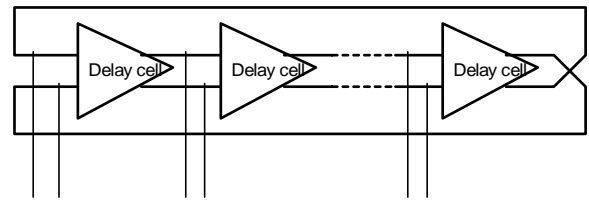
Output Multiphase Clocks

Figure 2. 8-stage Differential Ring Oscillator

In a single-looped PLL, there is always a tradeoff between a large locking range and low jitter. A large locking range requires a large VCO gain resulting more jitter and phase noise. The dual-looped architecture uses two loops to solve this design conflict. The VCO in the master loop is designed to have a large gain Kvco in order to have a large locking range. But the noise in the master loop is filtered out by a narrow-banding filter F(s). So a clean DC bias control voltage is provided to the slave loop. Meanwhile, the VCO in the slave loop is designed to have a small gain Kvco and the slave loop only need to finely tune the VCO frequency around the locking frequency. Therefore, the dual-looped architecture reduces the jitter of the output clock by reducing the VCO gain in the slave loop.

Also by having two loops architecture, we can select the different loop bandwidths for the master loop and the slave loop. Two loops give us the design flexibility to select the loop bandwidth of each loop so that we can achieve the optimum jitter performance.

3. LARGE RANGE VCO DESIGN

The VCO is the most important functional block in a PLL. This PLL was used as a clock synthesis unit in a gigabit-per-second optical-fiber transceiver. Multiple clock phases were required for signal processing. Ring oscillator topology is a suitable topology for this application [10]. Ring oscillators also have the advantages of wider oscillation frequency range and a small die size. Although ring oscillators have these advantages, they usually have poor phase
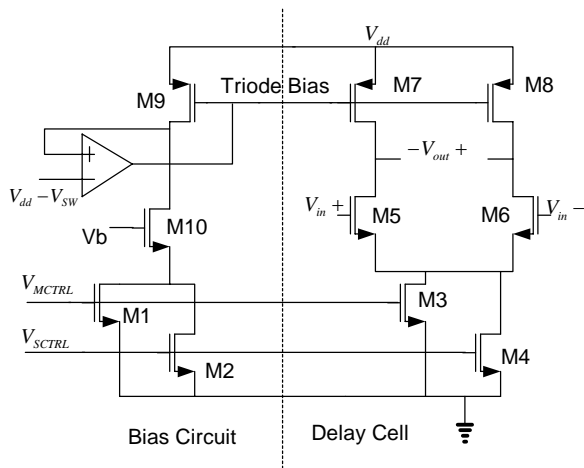
Figure 3. Differential delay cell and bias circuit

Figure 4: PFD block diagram

noise/timing jitter characteristics compared to high-Q LC oscillators. Careful design techniques need to be used to reduce the jitter or phase noise.

An 8-stage ring oscillator was designed as shown in Figure 2. A fully differential mode was used to reduce the power supply and substrate noise. The VCO circuit based on this CMOS ring oscillator consists of a bias circuit, the differential delay cells and differential current mode logic (CML) buffers to bring the high-speed clock out of the VCO.

The delay cell is based on a N-MOSFET source-coupled pair with voltage-controlled resistor (VCR) load elements that are implemented by the P-MOSFET devices biased in the deep-triode range. The oscillator control current is mirrored into the current sources in such a way that the output-voltage swing across the load remains constant over a wide range of control currents and output frequencies. A combined single delay stage of the VCO core circuit and the bias circuit are shown in Figure 3. Fully differential delay cells are used to reduce the sensitivity to power supply fluctuation and substrate noise and to reduce the distortion of the duty cycle.

In Figure 3, each delay cell has two control current sources M3 and M4. One of the control voltages, V_{MCTRL}, is controlled by the
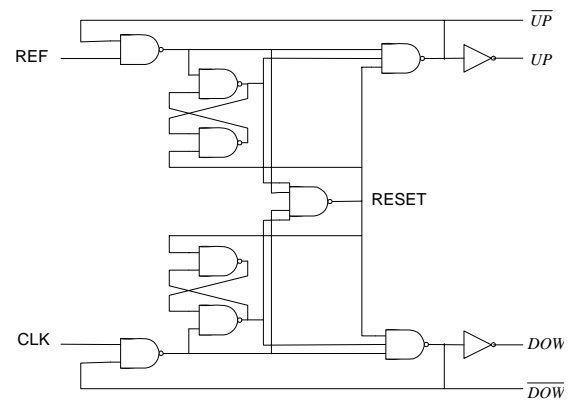
DC voltage from the master loop. This DC control voltage set the output frequency of the slave loop VCO close to the locking frequency. And the other control voltage, V_{SCTRL}, is used to finely tune the output frequency to the locking frequency by the slave loop itself.

In the design of the bias circuit, a large tuning range requires the load impedance to be adjusted inversely proportional to the g_m of the differential pair. The load impedance R, which was implemented by PMOS transistors M7 and M8, was adjusted inversely proportional to the transconductance of the differential pair by the biased circuit. For example, when the control voltage increased, the tail currents of the delay cell increased also. The bias circuit adjusted the bias voltage of the PMOS transistors M7, M8 to reduce the linear resistors. The bias circuit made the gain of the delay cell, A_v, almost constant in the whole tuning range so that it increased the tuning range of the VCO. Also the regulate opamp was used in the bias circuit to get the constant swing from the output of the delay cell. The constant swing of the output clocks made the signals easy to be brought out by the regular CML buffers.

4. OTHER PLL CIRCUITS

The Phase-Frequency Detector (PFD) was based on a conventional three-state phase detector shown in Figure 4. The inputs are
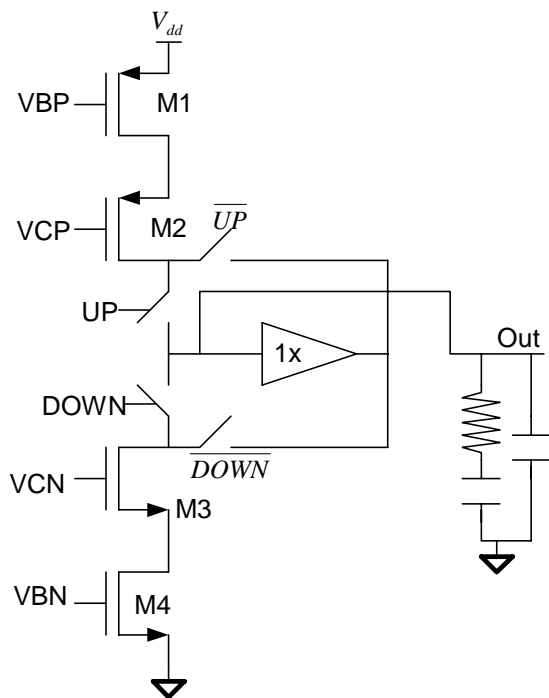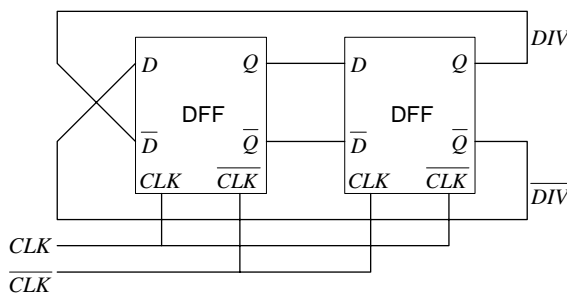
Figure 5. Charge pump circuit

Figure 6. Divideby2 Circuit

Figure 7. D flip-flop Circuit

Figure 8. Eye diagram with histogram of jitter

the reference clock (REF) and the feedback clock (CLK). The "dead zone" problem was avoided by adding delays in the loop. The PFD generates two minimum length UP and DOWN pulses, even when the compared waveforms (REF and CLK) are perfectly synchronized. Those pulses are identical in length, so the up and down currents cancel each other. When the input reference (REF) and the feedback clock (CLK) are not perfectly synchronized, PFD will generate unequal UP and DOWN pulse and let the charge pump to charge the loop filter to adjust the feedback clock phase or frequency.

The charge pump circuit used is shown in Figure 5 [9]. Since the PFD eliminates the
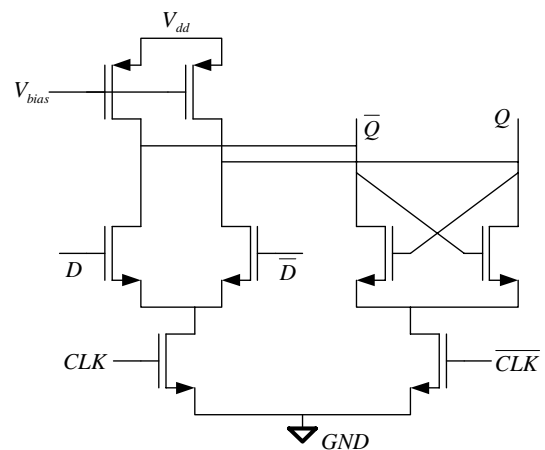
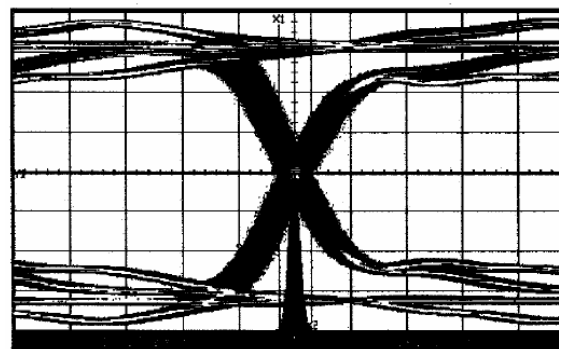"dead zone" by turning both sources on at the same time, a current mismatch between the sources can inject extra noise to the output control node. To avoid variations of the output current due to the output voltage, high-impedance cascode current sources M1, M2, M3 and M4 are used.

When the pulse controlling a source is low, normally the source would be turned off. This may cause charge injection at the switching time and slow response. To avoid this problem, the currents are redirected to the output of a unity gain buffer kept at the same voltage as the output of the loop filter. This prevents the current fluctuations that are due to the finite output impedance of the current sources.

The feedback divider number is 10. It consisted a high-speed $\div 2$ block and a $\div 5$ block. The $\div 2$ block is shown in Figure 6. The VCO output CML signal directly drives
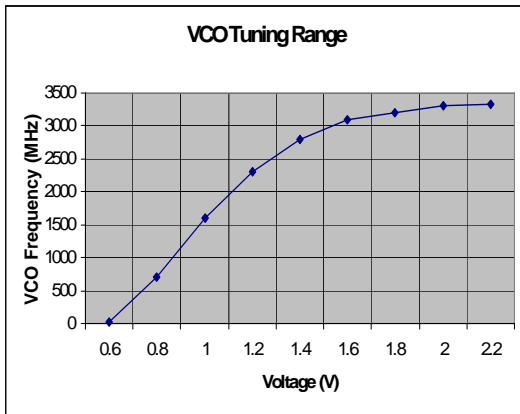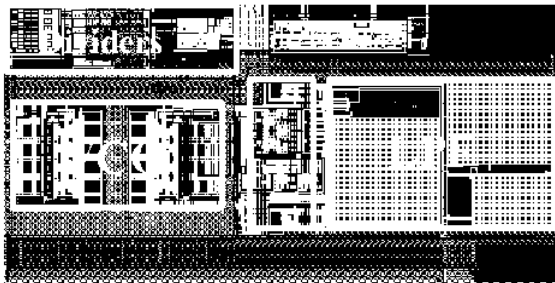
Figure 9. VCO Tuning Range

Figure 10.The micrograph of PLL (345x803 μm^2)

the $\div 2$ block. The dynamic D flip flop used in this block is shown in Figure 7. The positive feedback increases the speed of this block.

5. MEASURED RESULTS

The following table shows the measured performance of the PLL when functioning with the output frequency running at 1.25GHz.

Peak-to peak jitter	±35ps
Acquisition time	<15µs
Phase margin:	>70°
Power dissipation:	<300mw
Die area:	350x800 μm^2

Figure 8 shows the digital oscilloscope display of the eye diagram of the output clock at 1.25GHz superimposed with a histogram of its jitter. The measured VCO range of the PLL is shown in Figure 9. The range, which is as low as 30 MHz and as

high as 2 GHz, has been demonstrated across all the design corners. The Figure 10 shows the die micrograph of the PLL.

6. CONCLUSIONS

A large locking ranges from 30 MHz to 2 GHz PLL has been developed in a digital 0.24µm, 2.5V CMOS technology. It is the first time that such a large locking range PLL has been obtained in this technology. The PLL can operate as a part of a noisy logic CMOS chip and is designed to address a wide range of applications. It is fully integrated and has demonstrate lower peak-to-peak of ±35ps jitter at 1.25GHz output frequency.

REFERENCES

[1] J. Lee, B. Kim, "A 250MHz Low-jitter Adaptive Bandwidth PLL", ISSCC Dig. Tech. Papers, February 1999
[2] H. Wang, R. Nottenburg, "A 1Gb/s CMOS Clock and Data Recovery circuit", ISSCC Dig. Tech. Papers, February 1999
[3] J. Scott etc, "A 16Mb/s data detector and timing recovery circuit for token ring LAN", ISSCC Dig. Tech. Papers, 1989, pp150-151
[4] H.J. Sung, K.S. Yoon, "A 3.3V CMOS Dual-looped PLL with a Current-Pumping Algorithm", IEICE Trans, Fundamentals, VOL. E83-A, NO2, February, 2000
[5] F.M. Gardner, "Charge-Pump Phase-Lock Loop", IEEE Trans. Comm., vol. COM-28, pp. 1849-1858, November, 1980
[6] B. Kim, T.C. Weigandt, P. R. Gary, "PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design", Proc. of ISCAS, June 1994.
[7] H.S. Li, Y.C. Cheng, D. Puar, "Dual-loop Spread-Spectrum Clock Generator", ISSCC Dig. Tech. Papers, 1999
[8] A. Dec, Ken Suyama, "A 1.9GHz Micromachined-based Low-Phase-Noise CMOS VCO", ISSCC Dig. Tech. Papers, 1999

[9] I.A. Young, J.K. Greason, etc, "A PLL Clock Generator with 5 to 110MHZ of Lock Range for Microprocessor", JSSC, Vol 27, N11, pp 1599-1607, November, 1992

[10] S.K. Enam, A. Abidi, "NMOS ICs for clock and data regeneration in gigabit-per-second optical-fiber receivers," IEEE J. Solid-State Circuits, vol. 27, pp. 1763-1774, Dec. 1992