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Smart-Cut Layer Transfer of Single-Crystal SiC Using Spin-on-Glass

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Lee, Jae-Hyung; Bargatin, Igor; Park, Joonsuk; Milaninia, Kaveh M.; Theogarajan, Luke S.; Sinclair, Robert; and Howe, Roger T., "Smart-Cut Layer Transfer of Single-Crystal SiC Using Spin-on-Glass" (2012). *Departmental Papers (MEAM)*. 293.
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Lee, J., Bargatin, I., Park, J., Milaninia, K., Theogarajan, L., Sinclair, R., & Howe, R. (2012). Smart-Cut Layer Transfer of Single-Crystal SiC Using Spin-on-Glass. *Journal of Vacuum Science & Technology B, 30*(4), 042001. doi: 10.1116/1.4734006

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Smart-Cut Layer Transfer of Single-Crystal SiC Using Spin-on-Glass

Abstract

The authors demonstrate "smart-cut"-type layer transfer of single-crystal silicon carbide (SiC) by using spin-on-glass (SoG) as an adhesion layer. Using SoG as an adhesion layer is desirable because it can planarize the surface, facilitate an initial low temperature bond, and withstand the thermal stresses at high temperature where layer splitting occurs (800–900 °C). With SoG, the bonding of wafers with a relatively large surface roughness of 7.5–12.5 Å rms can be achieved. This compares favorably to direct (fusion) wafer bonding, which usually requires extremely low roughness (<2 >Å rms), typically achieved using chemical mechanical polishing (CMP) after implantation. The higher roughness tolerance of the SoG layer transfer removes the need for the CMP step, making the process more reliable and affordable for expensive materials like SiC. To demonstrate the reliability of the smart-cut layer transfer using SoG, we successfully fabricated a number of suspended MEMS structures using this technology.

Disciplines

Mechanical Engineering

Comments

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Smart-cut layer transfer of single-crystal SiC using spin-on-glass

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(Received 18 May 2012; accepted 21 June 2012; published 3 July 2012)

The authors demonstrate "smart-cut"-type layer transfer of single-crystal silicon carbide (SiC) by using spin-on-glass (SoG) as an adhesion layer. Using SoG as an adhesion layer is desirable because it can planarize the surface, facilitate an initial low temperature bond, and withstand the thermal stresses at high temperature where layer splitting occurs (800–900 °C). With SoG, the bonding of wafers with a relatively large surface roughness of 7.5–12.5 Å rms can be achieved. This compares favorably to direct (fusion) wafer bonding, which usually requires extremely low roughness (<2 Å rms), typically achieved using chemical mechanical polishing (CMP) after implantation. The higher roughness tolerance of the SoG layer transfer removes the need for the CMP step, making the process more reliable and affordable for expensive materials like SiC. To demonstrate the reliability of the smart-cut layer transfer using SoG, we successfully fabricated a number of suspended MEMS structures using this technology. © *2012 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4734006]

I. INTRODUCTION

Silicon carbide (SiC) is an attractive material for MEMS devices operating in harsh environments. There is a growing demand for devices made from a thin layer of SiC on a substrate[1–3] to enable lower-cost research in harsh environment MEMS applications. For example, we have recently been exploring the use of SiC structures for applications in thermionic energy converters (TECs), which can convert heat or solar energy directly to electricity.[3–5] Microfabricated TECs include high-temperature components that need to be suspended to keep them electrically and thermally isolated from the substrate, which is typically close to room temperature. This suspension and isolation can be easily achieved by using a silicon oxide sacrificial layer beneath the SiC structural layer.[3,4]

For some applications, it is important that the SiC be single crystal. For example, photon-enhanced thermionic energy converters[3,5] need a low-defect single-crystal cathode to reduce recombination and increase the conversion efficiency. A potential approach to obtaining a single-crystal film of SiC on buried oxide is epitaxial growth; however, to the best of our knowledge, there have been no reports of hetero-epitaxially grown SiC on top of oxidized silicon substrates. Alternatively, single-crystal SiC can be bonded to a substrate wafer. Recently, we created single-crystal SiC layers on oxide by directly (fusion) bonding a bulk (360 μm thick) SiC die onto an oxidized silicon wafer and then polishing it down to 50 μm SiC thickness.[3] Unfortunately, most of the SiC (>90%) was polished away through this process and therefore wasted. Finally, one can fabricate single-crystal SiC MEMS by using SiC wafer as a starting material and applying selective electrochemical etching.[6,7] However, multiple ion implantations of *n*-type and subsequent ion implantation of *p*-type are necessary to form a sacrificial layer and a device layer, respectively. Also, the method requires high temperature (1700 °C) annealing to activate the implanted dopants and no oxide isolation layer can be formed through this process.

Another approach is to use the smart-cut technique,[8] which uses wafer bonding of a hydrogen-implanted wafer. The implanted hydrogen forms a buried plane of microcavities parallel to the bonding interface at the ion penetration depth. At high temperatures (>600 °C), the wafer splits along this plane and the top portion of the SiC can be easily removed, leaving behind a thin single-crystal SiC film layer bonded to the substrate. Previously, SiC smart-cut was demonstrated only with the direct (fusion) bonding[9] technique, which typically requires extremely smooth surfaces

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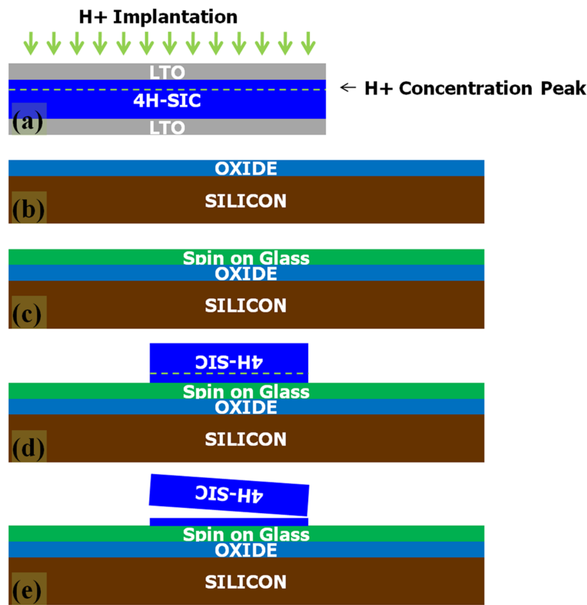

FIG. 1. (Color online) Outline of the fabrication process for smart-cut technique with spin on glass.

(roughness <2 Å rms[10]) on both wafers to obtain a high fabrication yield. As polishing SiC is extremely difficult, the SiC wafer can be thermally oxidized prior to the hydrogen implantation, and the oxide layer can then be polished after implantation to get a smooth surface.[9]

To increase the bonding strength, the wafer stack is typically annealed before the wafer splitting. Premature SiC splitting during anneal can be avoided if the temperature is lower than 600 °C. However, at such low temperatures, annealing times need to be as long as 24 h (Ref. 9) to ensure that the bond strength is sufficient and the SiC is transferred onto the oxidized silicon substrate as a continuous layer rather than multiple SiC flakes. Plasma activation can be used to achieve high bonding strength with shorter annealing times and lower temperatures,[11] but may not be readily available.

The approach presented here, using spin-on-glass (SoG) as an adhesion layer, makes it possible to relax both the roughness and annealing requirements. Previous studies successfully used SoG as an adhesion layer in a wafer bonding technique to bond compound III–V semiconductors to silicon wafers without using chemical-mechanical polishing (CMP).[12] Further, GaAs smart-cut using SoG has also been demonstrated.[13] Here we report the first demonstration of an SiC smart-cut using SoG as an adhesion layer. With this technique, SiC smart-cut can achieve high fabrication yield even for materials with surface roughness as high as 7.5–12.5 Å rms.

II. EXPERIMENT

A. Fabrication process

The fabrication process flow of the single-crystal SiC smart-cut technique with SoG is shown in Fig. 1. The process began with a commercial 3 in. *p*-type 4 H-SiC wafer from Cree, Inc. (360 μm thickness, $\sim$1 Ω cm resistivity, 8° off-axis orientation). A 50-nm-thick low temperature oxide (LTO) was deposited at 400 °C to act as a surface protection layer for wafer handling during the subsequent implantation [Fig. 1(a)]. As the commercial 3 in. *p*-type 4 H-SiC wafer comes miscut with an 8° off-axis orientation, protons were implanted vertically to create an 8° angle between the ion beam and the *c*-axis of the single-crystal wafer to avoid channeling effects. A proton dosage of $1 \times 10^{17}\,\mathrm{cm}^{-2}$ has

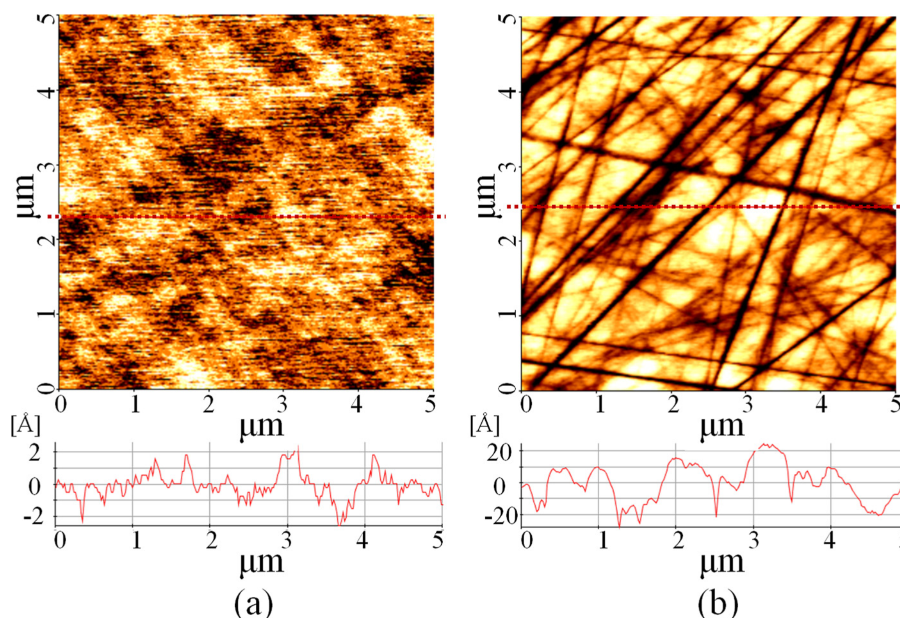

FIG. 2. (Color online) AFM measurement of an SiC sample die surface before (a) and after (b) the ion implantation. Its surface roughness was 0.8 Å rms before ion implantation (a); its surface roughness increased to 11.2 Å rms after the ion implantation (b). This increase is primarily due to the appearance of straight deep trenches on the surface after the ion implantation, probably caused by local damage due to high-intensity "hot spots" in ion beam. The straight deep trenches look close to a Lissajous pattern of two different frequencies of $\sim$5100 Hz in one axis and 500 Hz in the other, which was used for the fast axial scan of ion implanted beam (Ref. 16).

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been shown to be adequate for silicon carbide layer splitting[9] and was therefore selected for this experiment. As the location of the peak proton concentration is controlled by the implant energy, we chose the implant energies of 200 and 400 keV to achieve peak hydrogen concentrations ∼1.3 μm and ∼3.0 μm below the wafer surface, respectively.[9]

The implanted 3 in. 4 H-SiC wafer was then diced into ∼1 cm square pieces. After the wet etch of LTO, we cleaned a 1 cm^2 die of SiC, as well as an Si (100) substrate with a 1.6-μm-thick thermal oxide in de-ionized (DI) water, followed by a reverse RCA cleaning[14] to remove any contamination and to obtain hydrophilic surfaces. However, as the ion implantation increases the roughness of the SiC surface by about an order of magnitude (Fig. 2), an SiC die cannot easily be directly bonded to a carrier wafer. Further, polishing SiC to get a smooth surface is not trivial, and thermal oxidation is not an option for ion-implanted SiC wafers as the oxidation temperature is higher than the wafer splitting temperature. Therefore, rather than doing direct bonding, we used a flowable hydrogen-silsesquioxane-based inorganic SoG (Dow XR-1541) as an adhesion layer. This type of SoG was chosen for its ability to planarize the surface, facilitate an initial low temperature bond,[15] and withstand the thermal stresses at high temperatures where layer splitting occurs (800–900 °C).

In this study, a carrier wafer was coated with a 100–150-nm-thick layer of SoG, as shown in Fig. 1(c). The front SiC surface, through which ions had been implanted, was brought into contact with the SoG-coated carrier wafer. The two substrates were initially bonded together at room temperature with ∼1 MPa pressure applied for 1 min. We then heated the substrates to 80 °C for 1 min, 150 °C for another 1 min, and finally 250 °C while maintaining the same pressure on a hot plate. To help keep the pressure distribution uniform, we bonded three dies of SiC simultaneously; however, as SiC dies are not exactly identical, the thickest die tended to bond better than the other two. This bonding problem can be improved by using specialized bonding tools that can apply uniform pressure through each die. The bonded sample was then transferred to a tube furnace for the SiC splitting. The temperature was slowly ramped to 900 °C at a rate of less than 10 °C/min to avoid thermal shock, and then kept at this high temperature for 2 h to initiate the splitting along the plane of peak hydrogen

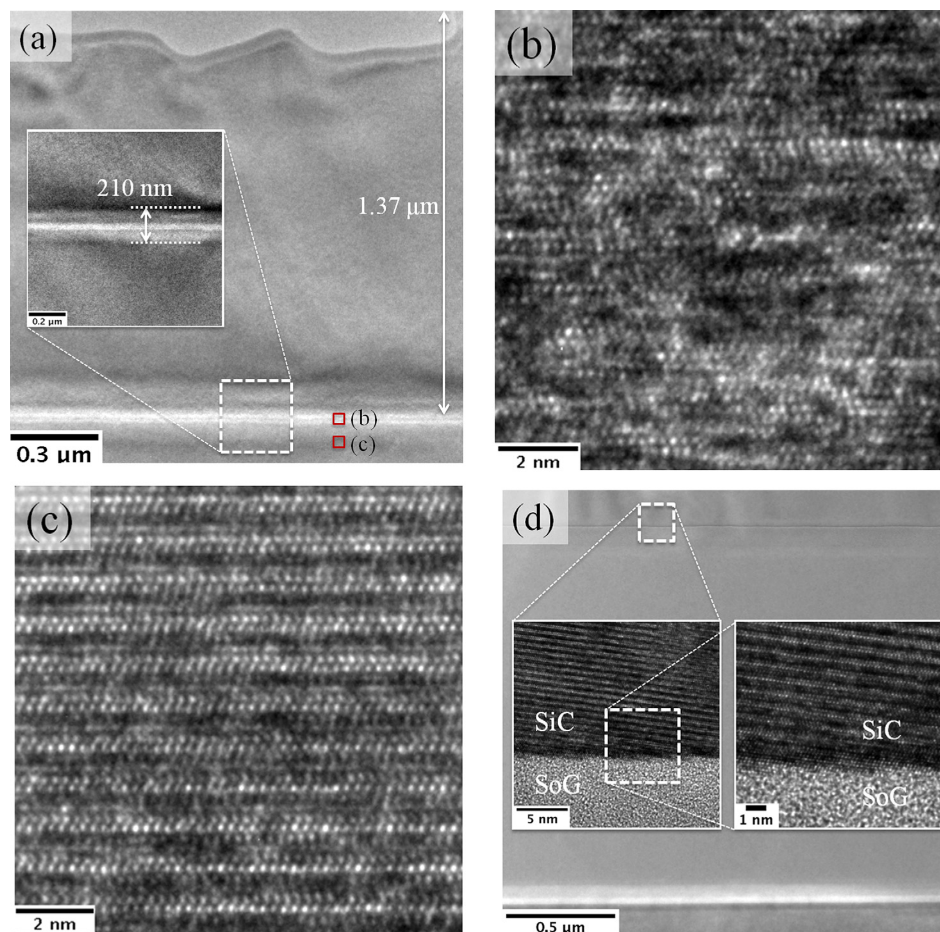

Fig. 3. (Color online) (a) TEM images of an SiC substrate after the ion implantation. The implant energy of 200 keV was chosen to achieve a peak hydrogen concentration ∼1.37 μm below the wafer surface. Inset of (a) shows the localized region highly damaged by ion implantation. (b) High magnitude TEM image of the damaged region [indicated by a rectangle with label (b) in panel (a)]. (c) High magnitude TEM image of the undamaged region [indicated by a rectangle with label (c) in panel (a)]. (d) SiC layer on top of the oxidized silicon substrate after the smart-cut using SoG. The eight-degree miscut of the original SiC wafer can be clearly seen.

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concentration.[8] As a result, a single-crystal 4 H-SiC layer with a thickness of $\sim$1.3 μm was successfully transferred onto the oxidized silicon substrate, as illustrated in Fig. 1(e). After the split, the remaining SiC substrate showed an average surface roughness of 25 Å rms; however, a few micron-scale SiC flakes were found on the remaining SiC dies, where the layer transfer was not complete. Note that with minor polishing, these SiC flakes can be removed and the remaining SiC substrate can be reused to conduct another "smart-cut" layer transfer process using this process.

Through the suggested fabrication process, over 80%–90% of layer was successfully transferred onto the silicon oxide substrate. With further optimization, 100% yield should be achievable.

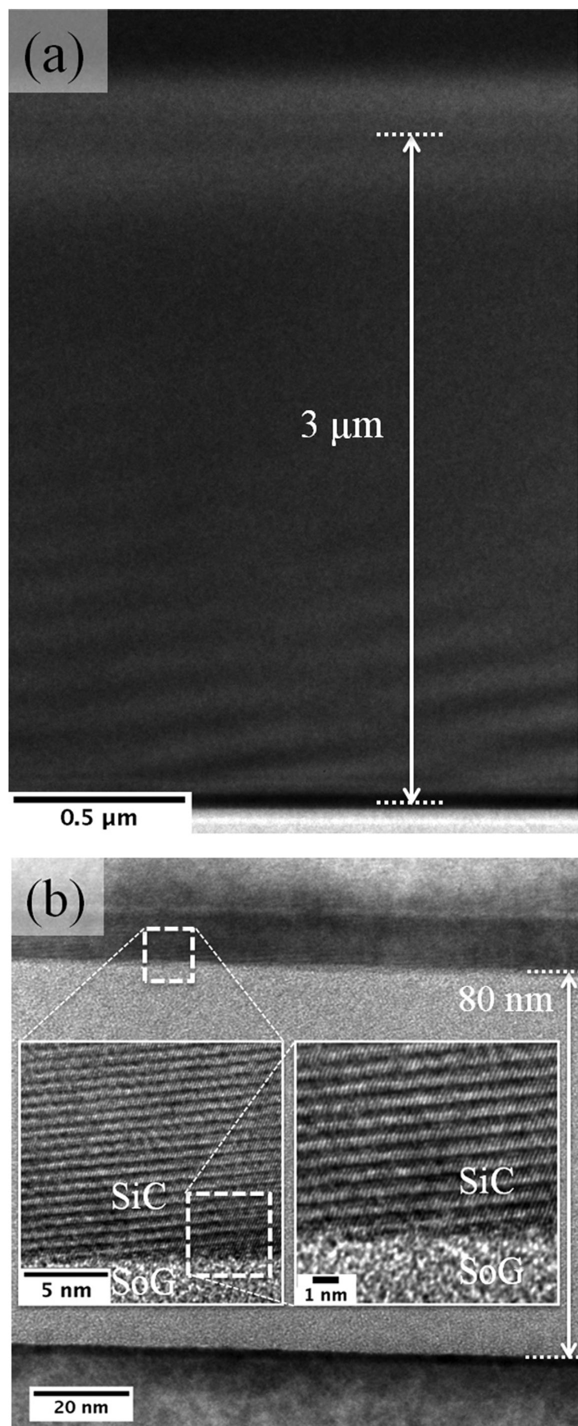

FIG. 4. (a) TEM images of an SiC substrate after the ion implantation. The implant energy of 400 keV was chosen to achieve a peak hydrogen concentration $\sim$3 μm below the wafer surface. Protons were implanted with a 7° tilt angle. (b) SiC layer on top of silicon substrate after the smart-cut using SoG. Note that the thickness of SoG decreased from 150 to 80 nm after all of the annealing steps due to densification.

B. TEM images

Preparing transmission electron microscopy (TEM) specimens with a conventional method (polishing, dimple grinding, and ion milling) was nearly impossible due to the deep ion implantation (>1 μm). All specimens except the 400 keV SiC transferred onto silicon substrate were prepared using a focused ion beam [(FIB) FEI Strata 235DB dual-beam FIB/SEM] lift-out Omni-probe technique that employed a Ga ion beam at 30 keV. Cross-sectional high-resolution transmission electron microscopy (HRTEM) images were taken using an FEI Tecnai G2F20 X-TWIN microscope operated at 200 kV.

Figure 3(a) shows the localized implant-induced highly damaged region with a thickness of 210 nm located

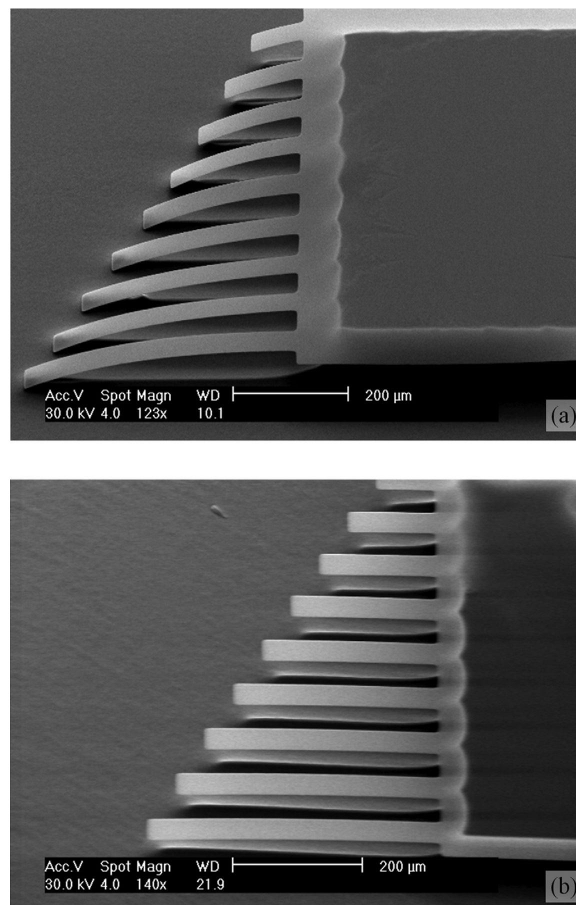

FIG. 5. Scanning electron micrographs (45°) of microfabricated cantilevers before (a) and after (b) high temperature annealing.

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~1.37 μm below the SiC surface. The HRTEM images of the SiC substrate of damaged and undamaged regions were shown in Figs. 3(b) and 3(c), respectively. Figure 3(d) shows the TEM image of a layer transferred SiC film. The detailed TEM images of a layer transferred SiC film show that the transferred SiC layer remains a high-quality single crystal after the smart-cut using SoG [the insets of Fig. 3(d)].

We repeated the same experiment with higher energy ion implantation to determine if this method can be applied to produce thicker film. The implant energy of 400 keV was chosen to achieve a peak hydrogen concentration ~3 μm below the wafer surface, and no CMP was done after the ion implantation. We successfully transferred the SiC layer again while maintaining the single-crystal structure, as illustrated by TEM images in Fig. 4. To the best of our knowledge, this thickness of the SiC layer transfer has never been demonstrated.

C. Stress gradient measurement

Using the transferred 1.3-μm-thick SiC film, we successfully fabricated a number of suspended microstructures in which the SoG layer and the substrate oxide layer together form a single sacrificial layer for the release etch. To characterize the bending caused by the stress gradient in the transferred SiC film, we fabricated cantilever structures with a width of 50 μm and lengths varying between 100 and 500 μm (Fig. 5).

After release, the average stress is zero, and the linear stress gradient can be inferred from the bending of the cantilever. The stress gradient can be estimated using elasticity theory for small beam bending[17]:

$$\Gamma = \left(\frac{E}{1-v}\right)\frac{1}{\rho}, \tag{1}$$

where ρ is the radius of curvature, and $E/(1-v)$ is the biaxial modulus of the beam material with E being Young's modulus and v Poisson's ratio. We used 700 GPa for Young's modulus and 0.19 for Poisson's ratio for layer transferred SiC cantilever.

The layer-transferred SiC was typically annealed for 4 h at 1140 °C immediately after being split to reduce the stress and stress gradient; however, to clarify the difference in material properties before and after annealing, a few prototypes of cantilevers and thermionic emitters were annealed after patterning and releasing. Figure 5 shows the SEM of single-crystal 4H-SiC cantilevers before and after high temperature annealing. Before annealing, the stress gradient was large enough to make all but the shortest cantilevers bend down and touch the substrate. Before annealing, the radius of curvature was ~0.3 mm and the estimated stress gradient of cantilevers was ~2.9 GPa/μm. After annealing, the suspended cantilevers for 4 h at 1140 °C, the measured radius of curvature increased to ~4.5 mm, and the estimated stress gradient dropped to ~190 MPa/μm. However, from a practical point of view, the most important fact is that cantilevers no longer touched the substrate and became virtually straight after annealing.

D. Residual average strain measurement

To estimate the residual average strain of the annealed SiC film, we fabricated microstrain gauges of various sizes (Fig. 6).[18] The residual strain, ε, can be calculated as follows:

$$\varepsilon \cong \left(\frac{2L_{sb}\delta_V}{3L_{ib}L_{tb}}\right) \approx 1.144 \times 10^{-4}, \tag{2}$$

where L_{sb} is the length of the slope beam, L_{ib} is the length of the indicator beam, L_{tb} is the length of the test beam, and δ_V is the measured deflection at the Vernier gauge site. The

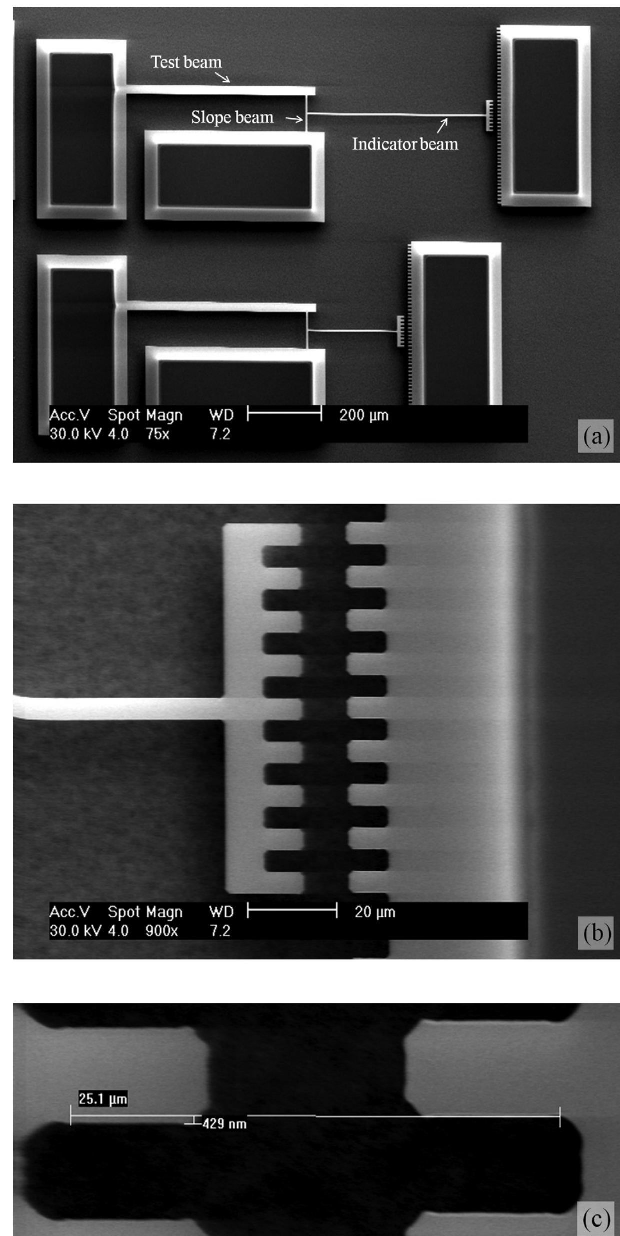

FIG. 6. (a) Scanning electron micrographs of microfabricated microstrain gauges with mechanical amplifier after high temperature annealing (b) Enlarged micrograph of indicator beam with $L_{sb} = 100\ \mu$m, $L_{ib} = 500\ \mu$m, and $L_{tb} = 500\ \mu$m. (c) Enlarged micrograph of (b) shows the deflection of a Vernier gauge site, $\delta V = 429$ nm.

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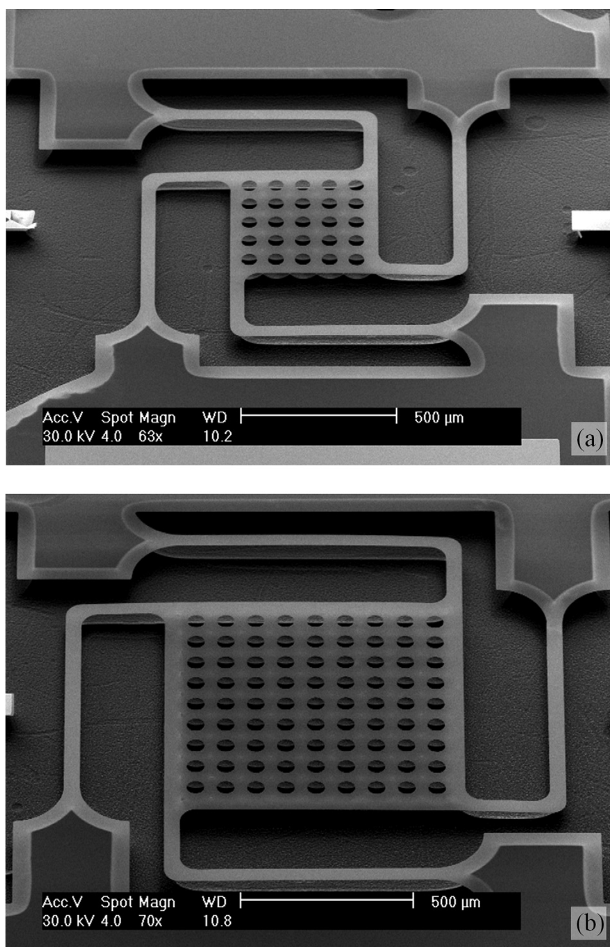

FIG. 7. Scanning electron micrographs of microfabricated emitters. The width of the legs was 50 μm and the size of center pad was 500 μm (a) and 700 μm (b).

residual stress, calculated by multiplying the residual strain and the Young's modulus, was ~80 MPa.

E. Applications

Last, we fabricated a single-crystal 4H-SiC thermionic emitter (Fig. 7) using the same SoG smart-cut technique, which is both quicker and more reproducible than the bonding and polishing approach used earlier.[3] The width of the legs was varied from 50 to 100 μm, and the size of center pad from 500 to 900 μm. Etch holes were used in the central pad to facilitate the release of the structure. Because the top surface of the transferred layer was most heavily damaged during implantation, we could not initially form a low-resistance electric contact between wire-bonding pads and the SiC layer. However, after the same high temperature annealing mentioned earlier, the transferred SiC layer became electrically conductive. This was probably due to the healing of implant-induced crystalline defects and the reactivation of aluminum dopant atoms.

III. CONCLUSION

We have demonstrated layer transfer of single-crystal SiC using a SoG-assisted smart-cut process. Unlike the previously used direct-bonding layer transfer, the SoG-assisted bonding is reliable even for a surface roughness as large as 7.5–12.5 Å rms. The use of SoG as an adhesion layer significantly relaxes requirements on surface roughness, which improves the reliability of the smart-cut layer transfer, opens up new design possibilities, and reduces the expense of working with a costly material like single-crystal SiC.

ACKNOWLEDGMENTS

This work is supported in part by the Defense Advanced Research Projects Agency (DARPA) N/MEMS S&T Fundamentals program under Grant No. N66001-10-1-4004 issued by the Space and Naval Warfare Systems Center Pacific (SPAWAR), Robert Bosch North America, and OCI Co. through the Center on Interfacial Engineering for MEMS (CIEMS), as well as BASF through the Stanford Energy and Environment Affiliates Program. J.-H.L. was supported by Samsung Scholarship. The authors thank Ron Eddy from Core Systems, inc., for helpful discussions.

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