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Demonstration and Modeling of Multi-Bit Resistance Random Access Memory

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Abstract
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Demonstration and modeling of multi-bit resistance random access memory

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Although intermediates resistance states are common in resistance random access memory (RRAM), two-way switching among them has not been demonstrated. Using a nanometallic bipolar RRAM, we have illustrated a general scheme for writing/rewriting multi-bit memory using voltage pulses. Stability conditions for accessing intermediate states have also been determined in terms of a state distribution function and the weight of serial load resistance. A multi-bit memory is shown to realize considerable space saving at a modest decrease of switching speed. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4790158]

Resistive random access memory (RRAM), which stores information through different resistance states, has potentially superior properties such as nano-second speed, >10 year retention, and $>10^7$ cycle endurance, along with good scalability (<100 nm).[1] RRAM can also exhibit >2 resistance states that may promise multi-bit storage.[2–8] In principle, if each single cell can display 2^N distinguished states, then for the same storage capacity the required die area will scale with $1/N$. Stated alternatively, for the same die area, each 2^N-state layer of a 2D memory has the same storage capacity of N 2-state layers of a 3D memory. Obviously, this will greatly increase the storage density and/or reduce the integration complexity.

In the literature, multilevel states of RRAM are usually revealed by imposing a current compliance[3,4] or through voltage programming.[2,7] The fact that these approaches seem to be applicable to all types of RRAM, irrespective of their underlying switching/conduction mechanisms, suggests a common understanding of their existence and control may be possible. However, no such understanding has been provided to-date. Moreover, despite the relatively common observation of multilevel states, there has been no report of two-way switching between all the 2^N states, which will be required in order for them to function properly as reprogrammable memory. Here we will demonstrate two-way switching for the $N=2$ case (4 multiple states: 00, 01, 10, 11); we will also employ a circuit model to explain multilevel switching.

We demonstrate these ideas using a recently developed nanometallic RRAM, which is a purely electronic, metal-insulator switching memory built on a hybrid amorphous structure with a distributed electronic energy profiles, thus naturally allowing multiple states.[7–10] Such RRAM exhibits several outstanding properties including excellent uniformity with small variations in switching voltages and resistance values, thus possibly providing highly reproducible multilevel states.[10] Although nanometallic RRAM can be implemented using a large variety of insulator:metal pairing, here we focus on Si_3N_4:Cr films (10 nm thick) with a Mo bottom electrode and a Pt top electrode (left inset in Figure 1(a)). The mixture film was co-sputtered on unheated Si substrates using separate Si_3N_4 and Cr targets in a magnetron sputtering system. To provide the bottom electrode, a Mo film (10 nm thick) was first deposited to cover the entire Si/SiO_2 substrate using DC sputtering. A top Pt electrode (40 nm thick) was later RF-sputter deposited through a shadow mask, forming cells of parallel capacitor type (Pt/Si_3N_4:Cr/Mo) with a diameter of 100 μm. The composition of the nanometallic films was determined to be 95% $SiN_{4/3}$:5% Cr according to energy dispersive X-ray spectroscopy (EDX) with additional calibration by electron energy loss spectroscopy (EELS).

As-fabricated RRAM devices exhibit bipolar switching behavior as shown in the I-V curve in Figure 1(a) obtained using the following voltage sweep sequence: 0 V, to 3 V, to −2 V, and to 0 V. Here a positive bias means current flowing from top to bottom. Initially conducting, the device shows a linear I-V curve corresponding to a flat resistance in the R-V curve (right inset in Figure 1(a)). With an increasingly positive voltage, the device is sharply "turned off" at ~2 V. Next, it stays at an insulating, high-resistance state (HRS) which exhibits a nonlinear I-V and R-V behavior. Under a negative voltage, the HRS passes through several intermediate states before eventually returning to the initial low-resistance state (LRS). From the shape of the I-V and R-V curves, it is obvious that there is easy access to the intermediate states from the HRS but not from the LRS. Similar

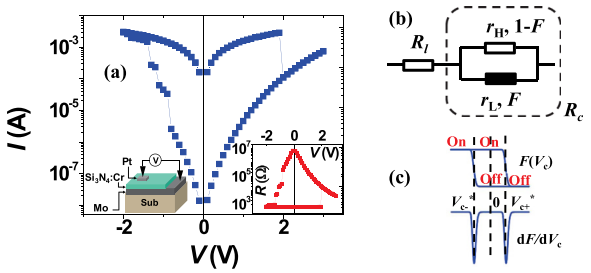

FIG. 1. (a) Characteristic I-V curve of nanometallic bipolar RRAM: On switching progresses in multiple steps, off switching displays one step. Left inset: schematic of device. Right inset: R-V curve. (b) Equivalent circuit of RRAM device. Cell resistor consists of high-resistance cross section (r_H per area, area fraction 1-F) and low-resistance cross section (r_L per area, area fraction F). (c) Schematic $F(V_c)$ and dF/dV_c depicting on-switching and off-switching.

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problems (with similar *I-V* and *R-V* curves) often exist for other types of RRAM according to the literature.[11–13]

As described in our previous work, *I-V*/*R-V* curves of the above kind can be very satisfactorily and quantitatively modeled by treating the device as a series connection of a load resistance R_l and a cell resistance R_c (Figure 1(b)). The reader is referred to Ref. 7 for the experimental procedure for determining R_l. Here, R_l is the sum of all the non-film resistances in the device (electrodes, interface, line, and compliance resistance), whereas R_c is the resistance of the film, which has a low-resistance cross section (area fraction $= F$, with a constant resistance $= r_L$ per area) and a high-resistance cross section (area fraction $= 1\text{-}F$, with a non-linear resistance $= r_H$ per area). As shown in Figure 1(c), on-switching corresponds to the transition from the initial $F = 0$ state to various larger F (intermediate) states at increasing $|V_c|$, around a characteristic $|V_{c-}^*|$. During such transition, the cell resistance R_c decreases, which causes $|V_c|$ on the cell to decrease and the voltage on R_l to increase. Therefore, to compensate for the drop in $|V_c|$, the partially switched device will need more external (negative) voltage before continuation of on-switching. This negative feedback during on-switching ensures a gradual *I-V*/*R-V* curve with many (indeed, infinite) intermediate states. Conversely, off-switching corresponds to the transition from the initial $F = 1$ state to a lower-F state when V_c rises past a characteristic V_{c+}^*. But since any decrease in F leads to an increase in R_c, hence a higher V_c, there is a positive feedback: it results in a self-propelling transition to HRS, a transition that is completed as soon as it is started.

Because asymmetric feedback, which is rooted in R_l, is the reason why intermediate states are not accessible during off-switching, tuning the R_c/R_l ratio should provide a means to adjust feedback to allow access. This idea was verified in our simulation (expressions and procedures for simulation are provided in Ref. 8, Methods). Figure 2(a) shows simulated *R-V* curves for a cell with a log-normally distributed dF/dV_c ($V_{c+}^* \sim 1.05$ V at $F = 0.5$, $\Delta V_{c+}^* = \pm 0.23$ V at $F = 0.1$ and 0.9, respectively). When simulation is run with an applied voltage increasing at 0.1 V increment, for a device starting at 0 V with a very low resistance (small R_c/R_l) corresponding to a large initial F, the off-switching is sharp and completed in one voltage increment (see $F = 0.9$ and 0.5 in Figure 2(a)). This is the case of large positive feedback: during the one-step transition, the voltage spent on the film rises from $\sim V_{c+}^*$ to $\sim V$, the latter well exceeding $V_{c+}^* + \Delta V_{c+}^*$, even though the applied voltage V merely increases by 0.1 V. After the transition, the final state already has $F = 0$ (HRS). On the other hand, if the device starts from a higher resistance (a smaller initial F, a larger R_c/R_l), then the required off-switching voltage is lower (see $F = 0.2$ and 0.05 in Figure 2(a)) because the cell now shares a higher fraction of the applied voltage. Meanwhile, intermediate states begin to appear on the switching curve. This corresponds to the case of limited feedback: even though V_c also rises from $\sim V_{c+}^*$ to approach V in one voltage increment, it has not exceeded $V_{c+}^* + \Delta V_{c+}^*$, thus not triggered avalanche switching.

The simulation also predicted the "unloading" *R-V*/*I-V* curves of the intermediate states (Figure 2(b)). For a device with an initial $F = 0.05$, three intermediate states of $F = 1\%$, 0.07%, and 0.005% are obtained after three successive V increments. Decreasing the applied voltage afterwards causes "unloading" of V_c, so these F values for the intermediate states remain unchanged. However, because r_H is non-linear, the "unloading" *R-V* curve is also non-linear, the more so the smaller F (Figure 2(b)). At $V = 0$, these intermediate states have distinctly different resistance values well separated from each other and from HRS ($F = 0$) and the nominal LRS ($F = 0.05$). If these memory states can be realized in practice, they should be rather easy to distinguish and to read.

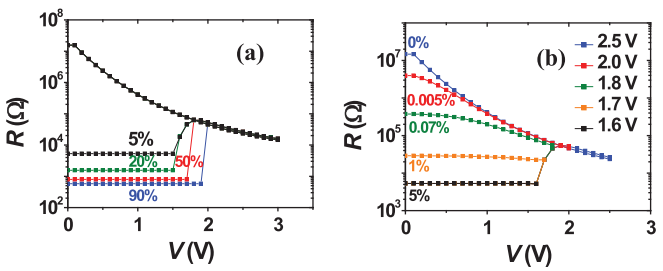

FIG. 2. Simulated *R-V* curves for off-switching using parallel circuit model in Figure 1(b). (a) *R-V* curves starting from different LRS, showing one step switching ($F = 0.9$ and 0.5) and multi-step switching ($F = 0.2$ and 0.05). (b) *R-V* curves for off-switching from one resistance state ($F = 0.05$) to four other resistance states ($F = 1\%$, 0.07%, 0.005%, 0%) by using different off-switching voltage. Simulation parameters: $V_{c+}^*(V) = 1.05$ (at $F = 0.5$), $\Delta V_{c+}^*(V) = \pm 0.23$ (+ at $F = 0.1$, − at $F = 0.9$), $R_l(\Omega) = 300$, $r_L(\Omega) = 250$, $r_H(\Omega) = \exp(17.05 - 5.45 \times |V| + 1.56 \times |V|^2 - 0.25 \times |V|^3 + 0.0193 \times |V|^4 - 0.0005913 \times |V|^5)$, where V is voltage in volt.

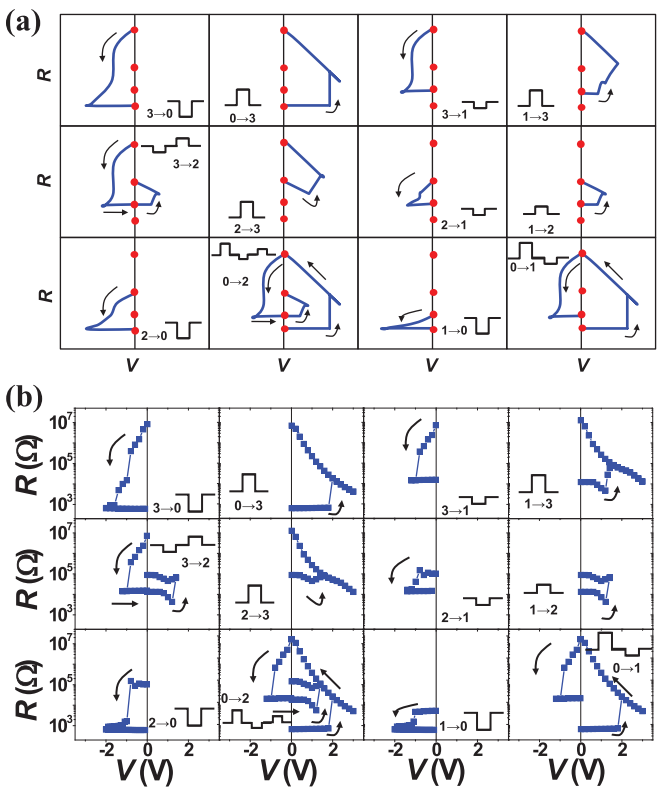

FIG. 3. (a) Schematic *R-V* curves of two-way switching in 2-bit memory between any two resistance states from 0 to 3 (resistance at 0 V in red). Inset: pulse trains of switching voltage. (b) Experimental *R-V* curves verifying (a). Memory cells constructed using nanometallic Mo/Si_3N_4:Cr/Pt film.

For these states we next illustrate a scheme for two-way switching. Here we use a 2-bit ($N=2$) memory, having four states that are ranked as 0–3 by their increasing resistance (note that this is different from the standard notation of calling the LRS the "1" state). The schematic switching R-V curves and triggering voltage-pulse trains are shown in Figure 3. Most (9 out of 12) switches are straightforward requiring only a one-step pulse. However, to access intermediate states (state 1 and 2) from the LRS (state 0), a multi-step pulse with a small negative voltage step is required to raise the cell resistance to limit off-switching avalanche. This is the case of $0 \rightarrow 2$ and $0 \rightarrow 1$, in which a detour *via* state 3 is made before applying the negative voltage step. For $3 \rightarrow 2$ switching, a two-step pulse is illustrated in Figure 3(a), but a one-step pulse for direct transition is also feasible if the device is under a compliance control that prevents $3 \rightarrow 1$ transition. The above scheme has been experimentally verified in nanometallic RRAM (its data provided in Figure 3(b)).

Next, we employ voltage pulses (single pulse width: 100 ns) to implement the above scheme at a realistic write/rewrite speed. The blue curve in Figure 4(a) shows that the initial state 0 holds its resistance until $V_{\text{pulse}} > 1.8$ V and then transitions to state 3. On the other hand, if the device starts from state 1, a 1 V pulse will transition it to state 2 (shown as the green curve), while a 2 V pulse will switch it to state 3. On a negative pulse, the state 3 can be reset back to either state 1 (with a -1 V pulse) or state 0 (with a -2 V pulse). These transitions are the essential ones that ensure the success implementation of the scheme in Figure 3, but other switches had all been verified using one-step or multi-step pulses. These states were stable: they maintained their resistance values without roll off during retention tests lasting over 10^5 s. As shown in Figure 4(b), states 0, 1, and 3 can all hold constant resistance. State 2 does show some resistance scatter, which may indicate exchanges between similar intermediate resistance states when subject to small perturbations. However, the scatter is small and will not affect distinguishing state 2 from neighboring state 1 and 3.

The two-bit memory above should not suffer from long RC time or slow switching speed. Concerning the RC time, we refer to Figure 1(b) and envision a cell capacitance C_c in parallel to R_c. It is then trivial to show that the RC time of the device is $R_l C_c(\frac{R_c}{R_c+R_l})$, which is bounded by $R_l C_c$ and essentially independent of the bit resistance. Typical values measured for our RRAM are $R_l \sim 1\,\text{k}\Omega$ and $C_c \sim 100$ pF for a $100 \times 100\,\mu\text{m}^2$ cell, which gives $R_l C_c \sim 10^{-7}$ s. Since R_l in our device is mainly due to spreading resistance and is relatively area-independent but the capacitance scales linearly with the area, the projected $R_l C_c$ is $\sim 10^{-13}$ s for a 100×100 nm^2 cell, which is more than satisfactory. Using the state-of-the-art CMOS technology, for which the typical sheet resistance for metal conductor layers is 0.05 Ω/sq, we also estimate for a 10 Gbit storage unit ($10^5 \times 10^5$) a line resistance of the order of 0.05 Ω/sq $\times$ 10^5 sq or 5 kΩ, which is 5 × the value for R_l above. Thus, the delay time (5× longer) is still extremely short for a 100×100 nm^2 cell. In addition, since nanometallic films can easily exhibit intermediate states with $R_{\text{intermediate}} \gg R_l$, R_l of the above type would not affect the readability/detectability of intermediate states.

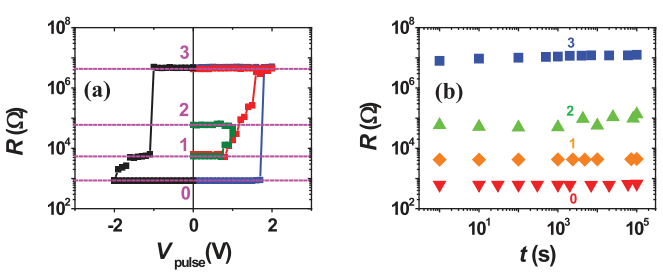

FIG. 4. (a) Resistance-pulse-voltage traces (pulse width = 100 ns) used to define four resistance states 0-3. After each voltage pulse, resistance is read at 0.2 V. (b) Resistance retention test (read at 0.2 V) for four states, each maintaining starting resistance over tested 10^5 s without roll-off.

Concerning the switching time, we refer to Figure 3(a) to compute an average for a 2-bit memory array, assuming all 4 states are equally populated and all 12 transitions are equally executed. Since 9 transitions need 1-step pulses, 2 transitions need 2-step pulses and 1 transition ($0 \rightarrow 2$) needs a 3-step pulse; the average switching time of this 2-bit-4-state memory is 1.33 times that of a 1-bit-2-state memory. Therefore, the tradeoff between a higher storage density (2×) and a slower writing speed seems favorable.

We now return to the constitutive basis of multistate memory. Referring to Figure 1(c), we see that multiple state transition is the result of the gradual inter-conversion curve ($F(V_c)$) between r_H and r_L elements. In nanometallic memory, the r_L state is the metallic state of a random conductor, and the r_H state is the insulating state in which charge-filled negative-U centers have blocked electron passage in their vicinity. Trapping and detrapping are thus responsible for the $r_L \leftrightarrow r_H$ conversion, which is voltage-driven governed by the energy landscape in the random material. Since the landscape in such material is inherently diverse, by nature this conversion must be energetically dispersive and can be triggered by a range of voltages as schematically illustrated in Figure 1(c). However, although a multitude of intermediate states naturally exist, they may be masked by voltage overload because of the positive feedback induced by the load resistance R_l. This can lead to a cell-voltage overshoot above the critical voltage ΔV_{c+}* and even beyond the energy dispersion (ΔV_{c+}*), which then creates a switching avalanche bypassing all intermediate states. The condition for this to occur can be obtained from the following simple analysis. (1) Because of voltage sharing, off-switching cannot be initiated until $V = \frac{R_l+R_c}{R_c} V^*_{c+}$. (2) Once initiated, with a positive feedback, the entire applied voltage is soon spent essentially on the cell, giving $V_c \sim V$. (3) If $V_c > V_{c+}* + \Delta V_{c+}*$, then overshoot will occur: transition will complete as soon as it is initiated. Combining (1)–(3), we obtain $R_l/R_c > \Delta V_{c+}*/V_{c+}*$ as the criterion for switching avalanche. In Figure 2, which uses $R_l = 300\ \Omega$ and $\Delta V_{c+}*/V_{c+}* = 0.22$, the condition separating sharp and continuous switching should be $R_c = 1363\ \Omega$. Indeed, continuous switching in Figure 2(a) begins with $F = 0.2$, corresponding to $R_c = 1250\ \Omega$.

As shown elsewhere for both bipolar and unipolar materials,[7,8] our circuit model can explain the switching I-V/R-V behavior of other RRAM irrespective of the underlying switching mechanisms. Multilevel states in other RRAM have been reported and are typically accessed by voltage programming or current compliance. Although it may seem

reasonable to attempt more storage bits by expanding the resistance range (e.g., lowering the LRS by using a larger on-switching voltage) or increasing the current compliance through a larger R_l, the above analysis points to the shortcomings of these approaches: a large R_l/R_c is inherently unstable for off-switching, and a large R_l will increase the RC time. On the other hand, RRAM with a negligible R_l has some advantage: for example, in Figure 3 state 0 can directly switch to state 2 if no positive feedback is provided. Systems with a highly dispersive dF/dV_c, i.e., a large $\Delta V_{c+}^*/V_{c+}^*$, are obviously desirable from this perspective.

Finally, we address two practical issues in implementing the current scheme. The first issue/concern for multilevel RRAMs is about their large R contrast, which could cover several orders of magnitude making it difficult to differentiate different states without using a complicated sensing circuit. Such concern is particularly valid for conventional (filamentary or/and ionic) multilevel RRAM, in which it is very difficult to tune the resistance values by fine-tuning the device composition and/or configuration. However, this is not the case in nanometallic RRAM. Indeed, a competitive advantage of nanometallic RRAM over conventional RRAM is its ability to tune the resistance values through either thickness (HR resistance increasing with thickness following an exponential dependence) or metal concentration (HR resistance decreasing with concentration spanning several orders of magnitude).[8–10] Therefore, it is entirely feasible to adjust the HR resistance to "squeeze" all the resistance states into a certain range so that they are all readable by the standard sensing circuit. The other concern is the complexity demanded on the drive circuit to generate the multi-impulse pulse trains in Figure 3. However, the complexity level of our pulse trains is fundamentally the same as that used in writing multilevel NAND memory. Moreover, since only one drive circuit is needed for each memory array, the complexity will not increase with storage size and therefore not significantly affect the space/cost saving consideration for using multi-bit cells.

In conclusion, we have demonstrated and analyzed a stable 2-bit-4-state nanometallic memory which can be read, written, and rewritten using voltage pulses. Even with only 2 bits, such storage memory already enjoys an advantage (2×) in space/area saving at a modest increase (1.33×) of average programming time. These results are applicable to other RRAM systems, and further advances in developing multiple bits may accelerate the adoption of highly integrated RRAM in future generations of digital memory.

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