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Abstract
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Size-dependent phase transition memory switching behavior and low writing currents in GeTe nanowires

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Synthesis and device characteristics of highly scalable GeTe nanowire-based phase transition memory are reported. The authors have demonstrated reversible phase transition memory switching behavior in GeTe nanowires, and obtained critical device parameters, such as write and erase currents, threshold voltage, and programming curves. The diameter dependence of memory switching behavior in GeTe nanowires was studied and a systematic reduction of writing currents with decreasing diameter was observed, with currents as low as 0.42 mA for a 28 nm nanowire. Results show that nanowires are very promising for scalable memory applications and for studying size-dependent phase transition mechanisms at the nanoscale. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2397558]

Chalcogenide materials such as GeTe, SbTe, and GeSbTe alloys have been widely used in the field of optical and electrical storage applications owing to their reversible crystalline to amorphous phase transitions, which is detected by the change of optical reflectivity and electrical resistivity.[1–5] Phase transition random access memory (PRAM) has attracted great attention due to their nonvolatile memory properties and fast write/read speeds,[6] and has the potential to solve many intrinsic limitations of conventional memory devices such as dynamic random access memory, static random access memory, and flash.[5,7–10] The realization of PRAM devices is, however, still limited due to the requirements of small cell size, high scalability, and low power consumption. The major bottleneck for achieving high density PRAM devices is the large writing currents needed to prepare the system in the amorphous physical state associated with high resistance (reset state).[8–10] The reduction of the writing currents is desirable because it can realize faster amorphization of material with less power consumed, enabling fast memory switching speed and with high reliability. The writing current depends on various factors including alloy composition, cell structure, and cell size. These challenges motivate the design of device schemes with sublithographic features based on bottom-up approach using nanowires (NWs) with small diameters.[11] The ability to synthesize NWs with small diameters will also facilitate systematic studies of size dependence of memory switching and phase-transition behavior down to sublithographic dimensions. Recently, GeTe and SbTe NW materials have been synthesized using the nanocluster-based catalyst approach;[12,13] however, not much is known about the memory switching properties of chalcogenide NWs. In this letter, we study in detail the memory switching properties of phase-change GeTe NWs, and the scaling of memory switching parameters such as the reset current with NW diameter.

GeTe NWs were synthesized via the metal catalyst-mediated vapor-liquid-solid (VLS) method.[14] Bulk GeTe powder (99.99%, Sigma-Aldrich) was vaporized at the center of a horizontal tube furnace at 650 °C and at a base pressure of 75 Torr. A Si (100) substrate covered with Au nanocolloids (diameter of ~40 nm) was placed in the furnace at the downstream side. GeTe vapor carried by Ar gas at a flow rate of 150 SCCM (SCCM denotes cubic centimeter per minute at STP) condensed on the substrate (400–480 °C) to produce NWs. The growth was done for ~1 h, and subsequently, the furnace was slowly cooled back to room temperature.

The morphology of the synthesized NWs was characterized using scanning electron microscopy. The density of the NWs was found to be dependent on the substrate temperature; dense NW growth occurred at higher substrate temperature [~480 °C, Fig. 1(a)] and less dense but very straight NWs obtained at lower temperature region [~400 °C, Fig. 1(b)]. Au catalysts were routinely observed at the NW ends [Fig. 1(b)], strongly suggesting that the growth occurs via the VLS mechanism. The diameters of the NWs ranged from 20 to 200 nm and with lengths up to ~50 μm.

The chemical composition of the as-synthesized NWs was determined by energy dispersive x-ray spectroscopy (EDS) in scanning transmission electron microscopy mode. The elemental mapping images for Ge and Te [Fig. 1(c)] show that Ge and Te are uniformly distributed along the whole NW without any local chemical variations. Quantitative analysis done on a large number of NWs by EDS point scanning confirmed that Ge and Te were present in a ratio of 51:49. The crystal structure of the GeTe NWs analyzed by high resolution transmission electron microscopy (HRTEM) showed that they were single crystalline [Fig. 1(d)]. Two-dimensional Fourier transform [Fig. 1(d), inset] of the HRTEM image also showed single spot diffraction patterns, further confirming that the NWs were single crystalline. The diffraction pattern was indexed to rhombohedral GeTe structure and the growth direction of the NW was determined to be along [220] direction, consistent with recent studies of GeTe NWs.[12] The spacing between the adjacent planes in the HRTEM image was measured to be 0.215 nm which corresponds to (024) lattice planes of the rhombohedral GeTe crystal structure.[13]

Electrical characterization of GeTe NWs is critical to understand their phase transition behavior. The GeTe NW memory devices were fabricated by transferring the as-grown NWs to an oxidized Si substrate (oxide thickness of

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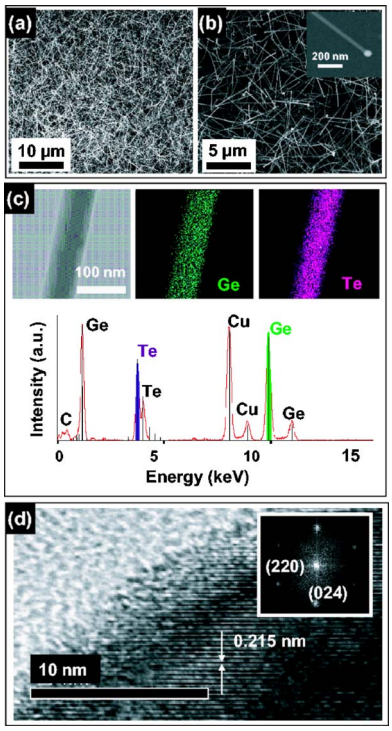

FIG. 1. (Color online) SEM image of GeTe NWs grown on the Si substrate (a) at a high temperature region (substrate temperature of ~480 °C) and (b) at a low temperature region (substrate temperature of ~400 °C). Au catalysts were clearly seen at the ends of most NWs (inset). (c) EDX elemental mapping of Ge (green) and Te (violet), and EDX spectrum obtained from the same part of the GeTe NW. (d) HRTEM image and diffraction pattern (inset) of GeTe NW, showing that the NW is single crystalline.

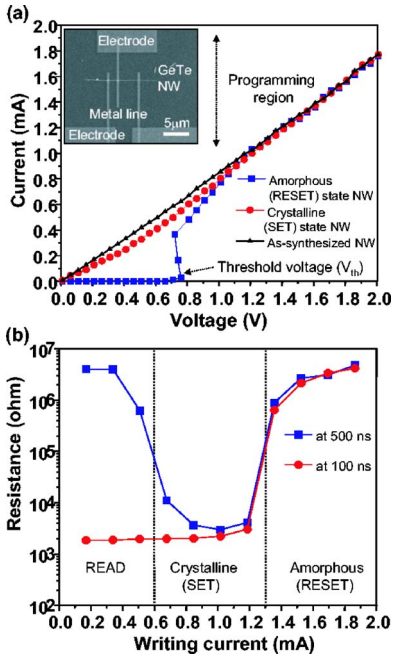

FIG. 2. (Color online) GeTe NW (diameter of 100 nm) memory switching characteristics. (a) Current-voltage (*I-V*) characteristics of the NW at different physical states: as-synthesized single crystalline (triangles), amorphous (reset, squares), and crystalline (set). Key device parameters such as threshold voltage, reset, set, and programing regions are marked. (b) Resistance change of the GeTe NW memory device as a function of writing pulses of varying current amplitude (programing curves). The read, set, and reset regions are clearly separated.

400 nm). Focused ion beam technique was employed to directly write 200 nm thick Pt electrodes on the NWs for which Ga^+ ion beam (30 kV, 10 pA) was used to decompose organometallic Pt precursor $[(CH_3)_3CH_3C_5H_4Pt]$. All electrical measurements reported in this work correspond to NW devices with electrode separation of 2 μm, and were performed with Keithley 237 *I-V* analyzer and Agilent 33250A pulse generator.

The as-synthesized GeTe NW memory device (diameter of 100 nm) initially displayed ohmic behavior (triangle) with a low resistance of ~1.2 kΩ [Fig. 2(a)], attributed to their original single-crystalline "set" state. The phase transition (memory switching) behavior and critical device characteristics of the GeTe NW were probed by applying short 100 ns electrical pulses with varying currents and subsequent measurements of resistance values [Fig. 2(b), circles]. Short current pulses are known to produce an amorphous state due to the rapid heating and quenching of the material.[10] For current pulses up to ~1.2 mA, not much change was observed in the resistance of the NW; however, higher current pulses (>1.4 mA) induced crystalline to amorphous phase transition leading to increased resistance (reset state), until saturation value of ~4.0 MΩ is reached. The *I-V* behavior of the reset state with high resistance of ~4.0 MΩ is shown in Fig. 2(a) (squares). Very low current flows through the device until a threshold voltage (V_{th}) of ~0.75 V due to highly resistive amorphous (reset) state. Above the V_{th}, the large heat generated in the NW causes amorphous to crystalline phase transition, leading to high currents. At higher applied voltages [>1.0 V, Fig. 2(a), squares], highly crystalline phase of NW (set state) is achieved due to which the *I-V* curve coincides with that obtained from the as-synthesized GeTe NW. The region where the two *I-V* curves coincide is the dynamic conduction state and used for the "programing" of the set and reset states upon the application of current pulses.

In order to characterize the current pulse amplitude dependence of the transition from amorphous to crystalline state, the GeTe NW device was switched back to amorphous state by applying a 100 ns pulse with a current amplitude of 1.8 mA. Then, longer pulses (500 ns) with varying current amplitudes were applied and the resistance of the NW was measured at each step [Fig. 2(b), squares]. Long current pulses are known to initiate amorphous to crystalline phase transformation by inducing nucleation and growth of crystallites in the material.[10] The resistance of the NW dropped dramatically for current amplitudes greater than 0.5 mA, which is due to amorphous to crystalline transition. A stable lower resistance state (set) was achieved for current pulses up to ~1.1 mA, whereas higher current pulses prepared the system back to the amorphous (reset) state. The *I-V* characteristics of the NW in the SET state with a resistance of 3.0 kΩ is shown in Fig. 2(a) circles), which shows that the initial resistance is higher than the as-synthesized NWs probably due to some amorphous regions. However, above 1.0 V, the *I-V* curve overlaps completely with the as-synthesized curve suggesting the formation of a highly crystalline NW. The programming curves given in Fig. 2(b) clearly separate the different regions associated with set, reset, and read (regions which are not affected by the current) states. Therefore, our results clearly demonstrate the fully reversible phase transition behavior in GeTe NWs, which is very promising for memory applications and studies of phase transition mechanisms in nanostructures.

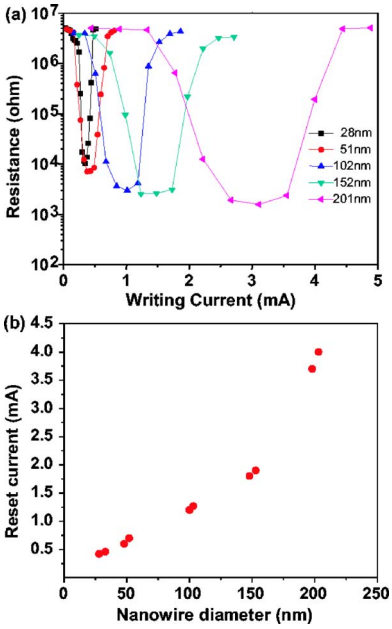

FIG. 3. (Color online) GeTe NW size-dependent memory switching properties. (a) Diameter-dependent reset and set programing curves as a function of writing current of the NW memory devices. (b) Diameter-dependent reduction of reset current. reset currents as low as 0.42 mA and 100 ns are sufficient to induce crystalline to amorphous phase transition in a 28 nm thick GeTe NW.

Significantly, for a set pulse as short as 500 ns, a large resistance change (reset: $4.0\times10^6\ \Omega$, set: $3.0\times10^3\ \Omega$ at 0.2 V) of over three orders of magnitude was achieved between the two programed states in the NW. These distinct states indicate that the GeTe nanowire possesses sufficient "sensing" range for memory switching applications. For long pulses (microseconds to milliseconds), a complete crystalline set state can be achieved with a larger resistance change from the reset state. However, such long programing times lead to slow memory switching, and a compromise needs to be done between the resistance change and writing speeds. Another technological bottleneck in thin film phase transition memory devices[10] is that the set resistance increases sharply with decrease of memory cell size. The increase of the set resistance is due to chemical etching-induced damage of the memory cells, and for sub-200-nm features[10] results in narrow sensing range and longer writing time. However, our data on GeTe NW [Fig. 2(b)] clearly show that the NW memory cells based on bottom-up approach are free of such increase in resistance and are promising for the development of small-sized phase transition memory devices.

The reduction of the reset current with memory cell size is an important criteria for achieving high density device integration with low power consumption. In order to study the size-dependent memory switching behavior in GeTe NWs, we performed a systematic study of the programming curves and reset writing current change as a function of NW diameter. Figure 3(a) shows the resistance and writing current characteristics for the set and reset programing curves as a function of NW diameter. Significantly, the programing curve shifts systematically from high to low writing currents with decreasing NW diameter. All NWs devices showed reversible phase transition memory switching, with NW with diameter as small as 28 nm showing attractive programing behavior with wide sensing range. These results show that the reset current is reduced drastically by scaling down the NW diameter. Figure 3(b) shows the systematic and significant reduction of reset current by reducing the NW diameter. The reset current pulse as low as 0.42 mA (100 ns) was achieved for 28 nm thick NW, a drastic decrease from a value of 4.0 mA (100 ns) for a 200 nm NW. The reset current of 0.42 mA obtained for 28 nm NW is much lower than that of state-of-the-art product level memory device in industry ($\sim$1.0 mA),[5,10] and is very encouraging for the development of low-power, highly dense memory devices.

The reset current is known to be dependent on the complex interplay of thermodynamic parameters such as melting temperatures, nucleation, heat of fusion, growth kinetics, current density, heat generation, dissipation, and transfer.[5,7,9] In particular, the phase transition observed in chalcogenide materials is primarily based on the Joule heating effect. Thus, for constant electrode spacing of our GeTe NW devices, the heat generation predominantly depends on the NW cross-sectional area. Heat generation due to high current density increases sharply with decreasing NW diameter, therefore leading to reduction of the reset current. However, the analysis of our data is currently based on the well-established literature on GeTe thin film studies[1,3] and therefore warrants more detailed experiments and analysis of GeTe NWs where novel nanoscale phenomena and surface effects will be important. Further experiments to obtain detailed microscopic information of the dynamics of phase switching behavior in NWs are currently being performed with *in situ* TEM techniques.

To summarize, our studies demonstrate that small size GeTe NWs are important structures for the study of memory switching behavior in nanostructures and opens interesting opportunities for applications in highly scalable memory devices, which are compatible to complementary-metal-oxide semiconductor (CMOS) or bi-CMOS architectures.

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