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Optimized Photolithographic Fabrication Process for Carbon Nanotube Devices

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Abstract
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Optimized photolithographic fabrication process for carbon nanotube devices

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We have developed a photolithographic process for the fabrication of large arrays of single walled carbon nanotube transistors with high quality electronic properties that rival those of transistors fabricated by electron beam lithography. A buffer layer is used to prevent direct contact between the nanotube and the novolac-based photoresist, and a cleaning bake at 300C effectively removes residues that bind to the nanotube sidewall during processing. In situ electrical measurement of a nanotube transistor during a temperature ramp reveals sharp decreases in the ON-state resistance that we associate with the vaporization of components of the photoresist. Data from nearly 2000 measured nanotube transistors show an average ON-state resistance of 250 $\pm$ 100 kΩ. This new process represents significant progress towards the goal of high-yield production of large arrays of nanotube transistors for applications including chemical sensors and transducers, as well as integrated circuit components. [doi:10.1063/1.3582820]

Since the discovery of single walled carbon nanotubes (SWNTs) twenty years ago,[1] there has been great interest in their use as electronic circuit elements, such as field effect transistors (FETs),[2,3] chemical sensors,[4,5] and transducers.[6] Electron beam lithography (EBL) has been the most commonly used fabrication method for SWNT circuits to date,[2,3] but EBL is a serial process, so the production of large arrays of devices or complex circuits is time-consuming and costly. A major goal for the field is thus the development of a fabrication method based on photolithography, a well established technique that enables parallel, wafer-scale patterning of circuits in a matter of seconds.[7]

Past investigations of photolithographically defined SWNT circuits all reported an undesirable scum layer that remains after processing.[8,9] One method to avoid the ill effects of this scum is to define and metalize the electrical leads before nanotube growth.[10] However, this geometry, with the nanotube on top of the leads, has been shown to result in less desirable device characteristics than when the leads are deposited on top of the nanotube.[11]

We report here on a photolithographic process for fabricating large arrays of SWNT field effect transistors (FETs) based on a resist bilayer of Shipley 1813 positive-tone photoresist on top of Microchem SF2S, a polymethyl glutarimide (PMGI) based resist. PMGI is designed for use in photolithographic processing as a sacrificial layer and as the under-layer in bi-layer lift-off metallization processing, and its effectiveness in EUV lithography has been demonstrated.[12] In the field of SWNT devices, PMGI has been shown to have excellent properties as a carrier material for iron catalyst particles for SWNT growth.[13] To our knowledge, however, there have been no reports of its use in an improved photolithographic process for fabricating contacts to high quality SWNT devices. After contact patterning by photolithography based on a PMGI-Shipley 1813 bilayer, we see no evidence of an undesirable scum layer. Device properties are further improved by a cleaning

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bake at 300C after contact metallization. We have measured the electronic characteristics of more than 1000 FETs fabricated using this process and find an "ON" state resistance of 250kΩ ± 100kΩ, indicating that the device quality is equal to that of FETs produced in our lab using electron beam lithography.

SWNTs were grown via catalytic chemical vapor deposition at 900C with a methane feedstock, on degenerately doped silicon wafers coated with 400nm of SiO_2.[14] SWNT-bearing wafers were spin coated with PMGI resist at 4000 rpm for 45 seconds, and then baked at 150C for five minutes. The samples were then spin coated with Shipley S1813 positive resist for 45 seconds at 5000 rpm, and baked at 130C for 3 minutes. Contacts to nanotube devices were patterned on a Karl Suss MA4 mask aligner, and the resist developed in a 2.2% tetramethylamonium hydroxide (TMAH) solution[15] that also isotropically etches the PMGI underlayer at a rate of ∼1nm/sec. Cr/Au contacts were deposited by thermal evaporation, followed by a two-step liftoff process. Samples were soaked in acetone at 65C for 10 minutes to dissolve the S1813 layer, and then transferred to a 2.4% TMAH solution for 15 minutes to dissolve the PMGI layer. The nanotube devices were then treated with a cleaning bake step in air at 300C for 1 hour. For comparison, additional devices were fabricated using a single layer of Shipley S1813 (i.e., no PMGI buffer layer), followed by the same cleaning bake step.

SWNT devices were characterized electrically using the degenerately doped silicon wafer as a gate electrode. Circuits consisting of a single semiconducting SWNT were selected based on their $I(V_G)$ characteristic. Figure 1 shows a histogram of the "ON" state resistance of 1000 semiconducting SWNT devices fabricated using the PMGI/S1813 bilayer resist, and 700 fabricated with S1813 alone. We find that devices fabricated using the PMGI/S1813 bilayer show an ON-state resistance of 250 kΩ ± 100 kΩ, a range that is essentially identical to the best results that we and other groups have obtained using EBL.[16–18] In contrast, samples made using S1813 alone had a much larger ON-state resistance with considerably larger fluctuations (5.0 MΩ ± 3.0 MΩ). This striking difference in contact resistance is attributed to the presence of scum from the S1813 photoresist on the SWNT sidewall and on the substrate surface when the PMGI buffer layer is omitted. Others have reported,[9] and we have verified, that standard photolithographic processing with S1813 alone results in residual nodules of photoresist (∼ 2-10 nm diameter) that decorate the sample surface and preferentially accumulate on the SWNT sidewall. This molecular contamination layer is expected to act as an additional tunneling barrier, in series with the Schottky barrier known to form at the nanotube metal junction[19,20] and in this way lead to sharply increased device resistance. No such contamination is observed on samples fabricated with the bilayer process.

We attribute the formation of this undesirable photoresist scum to the presence of π-conjugated aromatic components in the photoresist, e.g., the novolac resin that forms the base of the resist, the diazonapthoquinone (DNQ) photosensitizer, and trace amounts of cresol that arise during the production of the resin. Aromatic molecules bind strongly to the nanotube sidewall due to the attractive π-π interaction.[21–24] While this effect can be exploited to non-covalently attach aromatic molecules to carbon nanotubes, excessive photoresist contamination is very harmful to devices. The PMGI layer in our optimized process is free of π-conjugated species, similar to the electron beam resist PMMA, which can be used to fabricate high quality SWNT transistors. It thus interacts only weakly with the SWNT, and serves as a buffer layer that prevents deposition of photoresist scum after development. We find, however, that some surface contamination remains on the SWNT devices after lift-off, and that this contamination is effectively removed by a cleaning process described below. We attribute this surface contamination to dissolved species that redeposit onto the SWNT sidewall during liftoff.

In order to determine the ideal temperature for post process cleaning of the samples, as-fabricated devices were baked for 1 hour each at 100C, 200C, and 300C sequentially, and the current-gate voltage (I-V_G) characteristic was measured after each bake (Fig. 2). Typically this process resulted in a decrease in ON-state resistance of 2-3 orders of magnitude. We attribute this increase in conductance to both desorption of molecular species adsorbed along the FET channel,[25] and annealing of the contacts.[26] We also observed a progressive shift of the threshold voltage towards positive voltage, which is characteristic of decreased positive charge near the nanotube. This shift is also attributed to a reduction in molecules adsorbed onto the SWNT sidewall and the nearby SiO_2 surface due to the cleaning bake.

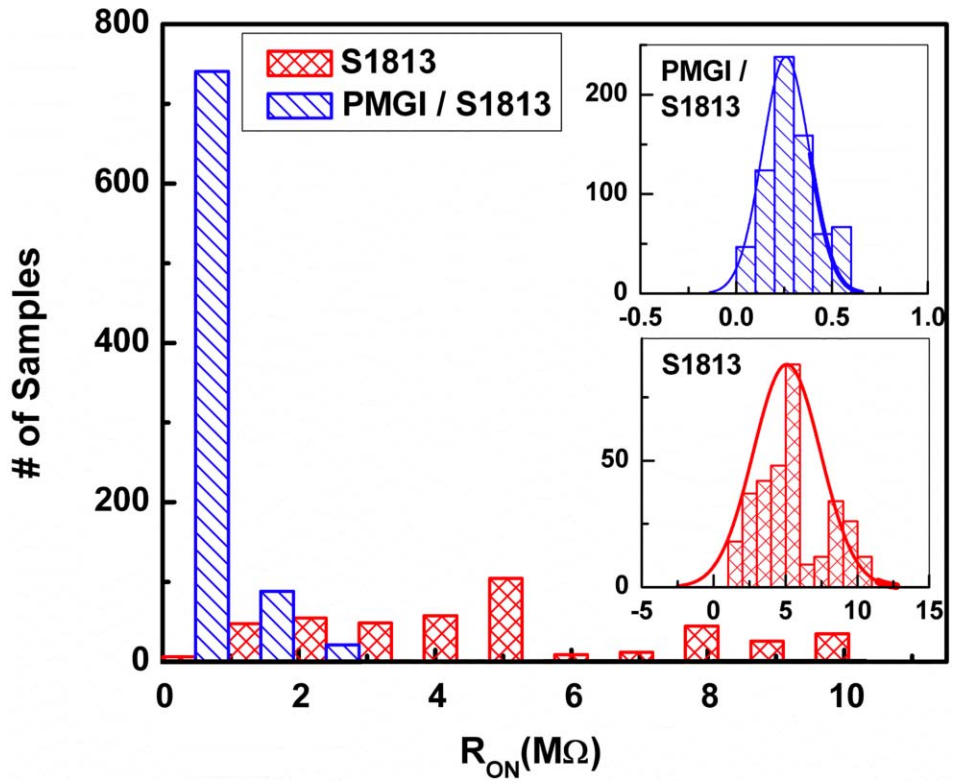

FIG. 1. Histogram of ON-state resistance of FETs fabricated with the PMGI/S1813 bilayer process and a process using a single layer of S1813. FETs fabricated with the bilayer procedure have an R_{ON} value strongly peaked at 250kΩ ± 100kΩ, while R_{ON} values for devices fabricated with S1813 alone are peaked at 5MΩ ± 3MΩ. Insets: Histogram of 80% of the devices fabricated by each method and a Gaussian fit used to extract the average R_{ON} values.

The observed decrease in ON-state resistance likely reflects desorption of multiple species of contaminants. To probe the dynamics of this process, the ON-state current of a device was monitored in situ as the temperature of the device was increased from room temperature to 300C, at a ramp rate of 0.5C/min (see Fig. 3). The bias voltage was 100mV, and the gate voltage was set at –8.5V, to assure that the device was in the ON-state at all times during the measurement. The ON-state resistance of the as-fabricated device was approximately 100MΩ, and it decreased to roughly 500kΩ after the procedure. Strikingly, we observe that the ON-state resistance decreases sharply at particular temperatures: 185C, 193C, 205C, 220C, 230C and 245C. We associate the first three temperature values with vaporization temperatures of component compounds of the Shipley 1813 photoresist and PMGI buffer layer. Specifically, tetrahydrofurfuryl alcohol (THFA), a solvent used in the production of PMGI resist, boils at 185C. The PMGI undergoes a glass transition at 190C, which may also contribute to this resistance decrease. The next two resistance drops (193C, 205C) correspond to the boiling points of different species of cresol (C_7H_8O), a π-conjugated aromatic compound used in the production of novolac resin resists, including S1813. The observation of such sharp decreases in ON-state resistance at the vaporization temperatures of known components of Shipley 1813 and PMGI demonstrates that residual contamination from the lithographic processing can be removed through baking at modest temperatures that have no ill effects on SWNT devices. The higher temperature jumps are attributed to either unidentified components of Shipley 1813 or PMGI, or annealing of the Cr/Au contacts.

In conclusion, we have developed a method for the reproducible production of large arrays of SWNT FET's. By enabling the use of photolithographic processing of SWNT circuits, parallel processing at the wafer scale is a reality. A buffer layer is used to prevent direct contact between the SWNT and the novolac-based photoresist, and a cleaning bake step at 300C is effective at removing

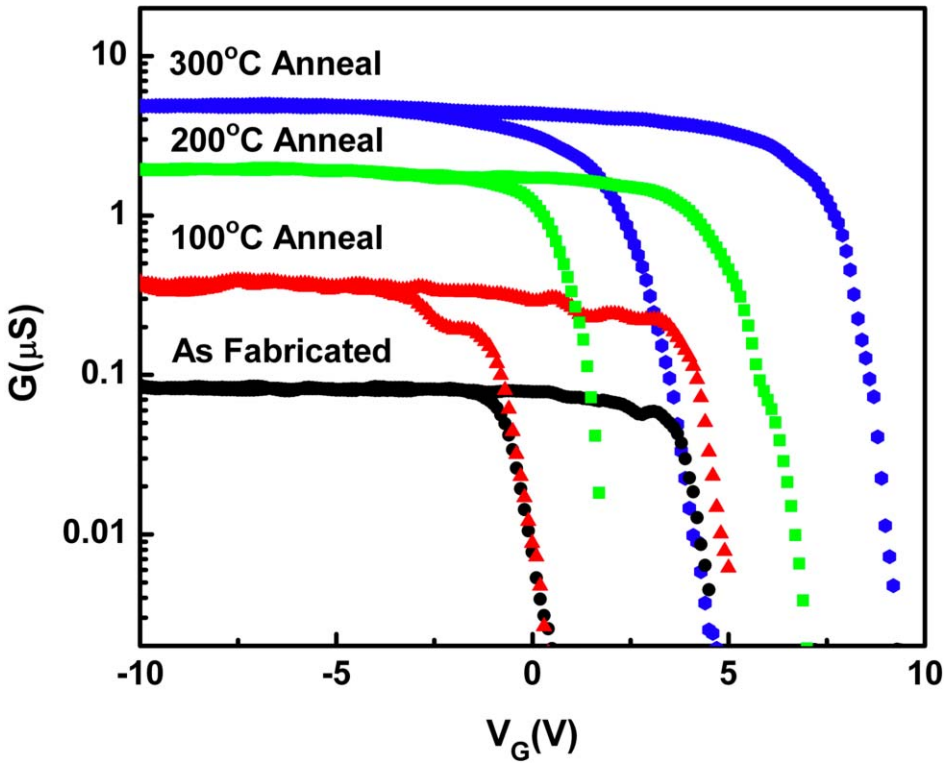

FIG. 2. FET conductance as function of gate voltage after successive bakes at 100, 200, and 300C. The ON-state conductance grows with each bake, with a total increase of a factor of 50. The bias voltage is 100mV.

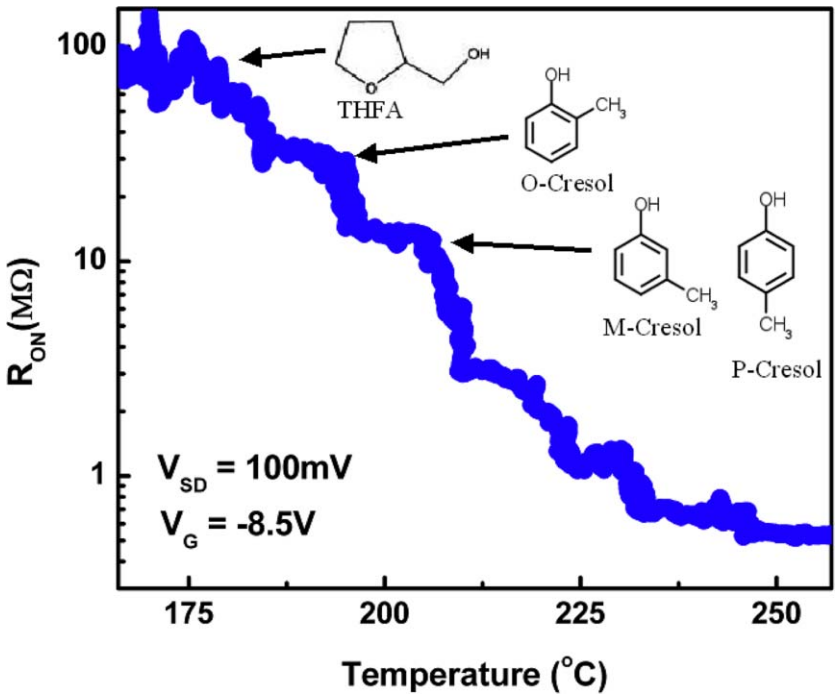

FIG. 3. ON-state Resistance of a SWNT FET decreases as the bake temperature is ramped at a rate of 0.5C/min. Sharp decreases in resistance are observed at temperatures assigned to desorption of specific contaminants that are components of the S1813 and PMGI resists.

residual compounds that bind to the SWNT sidewall during processing. This enables the production of SWNT transistors with an average ON-state resistance identical to the best quality devices fabricated by electron beam lithography. We selected an optimum temperature for the cleaning bake by treating a single sample multiple times at successively higher temperatures, and measuring the device electrical properties after each cleaning step. In situ electrical measurements revealed sharp decreases in the ON-state resistance of a device during a temperature ramp, which we associate with the vaporization of known components of PMGI and Shipley S1813 photoresist. This type of process should allow the integration of carbon nanotube devices into standard CMOS architectures given recent advances in low temperature growth of SWNTs[27] and the fact that our post process annealing temperature is compatible with CMOS devices.

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