September 2002

An Extended Frequency Range CMOS Voltage-Controlled Oscillator

Chao Xu
PMC-Sierra, Inc.

Winslow Sargeant
National Science Foundation

Kenneth R. Laker
University of Pennsylvania, laker@seas.upenn.edu

Jan Van der Spiegel
University of Pennsylvania, jan@seas.upenn.edu

Copyright 2002 IEEE. Reprinted from *Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2002)*, Volume 2, pages 425-428.
Publisher URL:http://ieeexplore.ieee.org/xpl/tocresult.jsp?isNumber=22423

An Extended Frequency Range CMOS Voltage-Controlled Oscillator

Abstract
This paper presents an extended frequency range CMOS monolithic voltage-controlled oscillator (VCO) design. A negative feedback control algorithm is used to automatically adjust the VCO range according to the control voltage. Based on this analog feedback control algorithm, the VCO achieves a wide range without any pre-register settings. Low phase noise is achieved by using both coarse control and fine control in VCO. A 600 MHz to 3.3 GHz monolithic CMOS PLL based on this wide range and low phase noise VCO has been fabricated in TSMC 0.18 μm, 1.8V CMOS technology and is used in many different applications such as FC, GE, and SONET etc.

Keywords
VCO, PLL, voltage-controlled oscillator, phase-locked loop, phase-noise

An Extended Frequency Range CMOS Voltage-Controlled Oscillator

Chao Xu[1], Winslow Sargeant[2], Kenneth Laker[3], Jan Van der Spiegel[3]
[1] PMC-Sierra, Inc. Allentown, PA, 18102
[2] National Science Foundation, Arlinton, VA, 22230
[3] Department of Electrical Engineering, University of Pennsylvania
chao_xu@pmc-sierra.com

[ABSTRACT] This paper presents an extended frequency range CMOS monolithic voltage-controlled oscillator (VCO) design. A negative feedback control algorithm is used to automatically adjust the VCO range according to the control voltage. Based on this analog feedback control algorithm, the VCO achieves a wide range without any pre-register settings. Low phase noise is achieved by using both coarse control and fine control in VCO. A 600MHz to 3.3GHz monolithic CMOS PLL based on this wide range and low phase noise VCO has been fabricated in TSMC 0.18um, 1.8V CMOS technology and is used in many different applications such as FC, GE, and SONET etc.

I. INTRODUCTION

With the exponential growth of the number of Internet nodes, the volume of the data transported by its backbone continues to rise rapidly. Among the available transmission media, optical fibers have the highest bandwidth with the lowest cost, serving as an attractive solution for the Internet backbone. However, the electronic interface proves to be the bottleneck in designing high-speed optical system. This fact, combined with the ever-shrinking time to market, indicates that designs based on flexible modules and macro-cells have great advantages. In the optical communication in a backbone infrastructure, flexibility means, for example, programmable bit rates requiring a phase-locked loop (PLL) with robust operation over a wide frequency range. A wide range PLL could be used by different protocols and applications so that we maximize the reusability and reduce the time to market [1].

A wide range PLL requires a wider tuning range of voltage-controlled oscillator (VCO). In this paper, a fully integrated CMOS VCO with an extended frequency range from 600MHz to 3.3 GHz is described. In section II, following a brief overview of conventional architecture for ring type based VCO design, the proposed architecture is described to solve the problems of conventional methods. A negative feedback control algorithm automatically adjusting VCO frequency range is used to extend the frequency range. A coarse control and fine control scheme is used to reduce the phase noise of VCO. In section III, circuits of this novel wide tuning range VCO are described. Measurement results are included in section IV. And finally concluding remarks are included in section V.

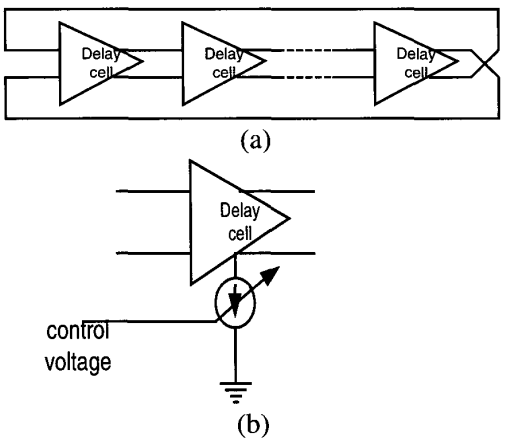

Figure 1 (a) Ring Typed Oscillator
(b) Voltage-controlled Delay Cell

II. ARCHITECTURE

A. Limited Range Problem of Conventional VCOs

The most common used architecture for the voltage-controlled oscillator in CMOS technology is voltage controlled ring typed oscillator [2]. It consists of several delay cells forming a close loop as shown in Figure 1(a). The output clock frequency is determined by the delay of each delay cell which is in turn controlled by the control voltage. A wide frequency range of oscillator means a wide tuning range for each delay cell.

The delay cell is usually a differential pair with a tail current and some active loadings. The delay of the delay cell is controlled by the value of the tail current shown in Figure 1(b). There are some difficulties associated with this architecture to achieve the wide tuning range. By using a single tail current, the tuning range is limited by the control voltage range. The control voltage range is usually constraint by the power supply voltage, i.e. $0 \le V_{control} \le V_{dd}$. If we choose the small tail current, the tail current is still not large enough even that the control voltage reach the up limit so that the high end frequency range of VCO is small. On the other hand, if we choose the large tail current, the tail current is still

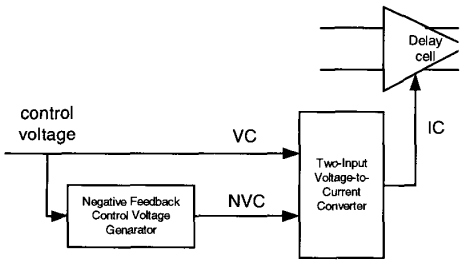

Figure 2. Block Diagram of the Proposed Architecture

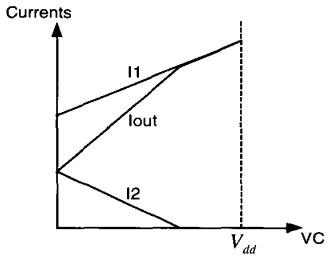

Figure 3. The relation between the currents and the control voltage

large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large.

B. Proposed Negative Feedback Control Architecture

In order to solve the limited range of conventional VCO architecture, the negative feedback controlled architecture is proposed. Figure 2 shows a block diagram of the proposed architecture. This architecture includes three blocks: a negative feedback control voltage generator, a two-input voltage to current converter and delay cells. The negative feedback control voltage generator converts the control voltage supplied by the PLL into the feedback control voltage which will be inputted to the voltage-to-current converter block. The two-input voltage-to-current converter converts the two control voltage inputs VC and NVC to the current IC which is supplied to the delay cell block. And, finally, the delay cell block delays the input signal to the output signal whose delay is controlled by the control current IC.

C. Negative Feedback Control Voltage Generator Design

The negative feedback control voltage generator takes the control voltage VC (supplied by PLL) as an input and

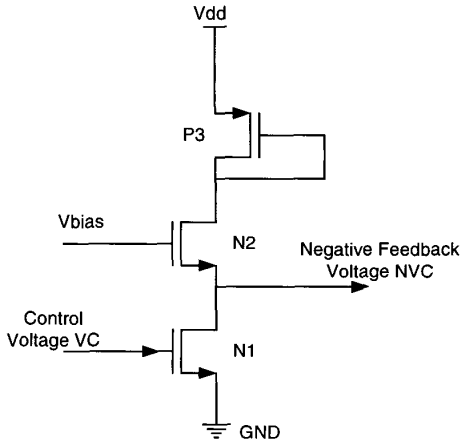

Figure 4. Negative Feedback Control Voltage Generator

generates the negative feedback control voltage NVC. This block doesn't need any additional pre-settings such as register bits or reference voltages for comparators. The purpose of this block is that when the input control voltage VC is low, the output negative feedback control voltage should be high. On the other hand, when the input control voltage VC is high, the output negative feedback control voltage should be low.

D. Two-input Voltage-to-Current Converter Design

The two-input voltage-to-current converter accepts the two control voltages VC and NVC as inputs and generates the control currents to each delay cell in the VCO. The purpose of this block is to generate the wide range currents with the limited range control voltage. The output current is designed as the subtraction of two current sources controlled by the two input voltages: control voltage supplied by PLL loop and the negative feedback control voltage. The relations between Iout, I1, I2 and the control voltage VC are shown in Figure 3. I1 increases with the control voltage VC (See curve I1 in Figure 3). I2 is controlled by the negative feedback control voltage which decreases with the increase of VC. So I2 decreases with the control voltage VC(See curve I2 in Figure 3). Iout=I1-I2 and is shown as the curve Iout in Figure 3. So when the control voltage VC is small, the effective output current Iout is small although the current source I1 controlled by VC is large. But when the control voltage VC is high, the effective output current Iout is equal to I1 which is high because the current source I2 is 0 and doesn't reduce the effective output current Iout. So the current range is effectively expanded.

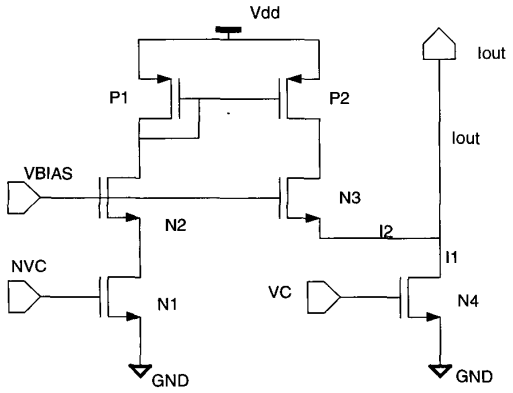

Figure 5. Two-input V2I Converter

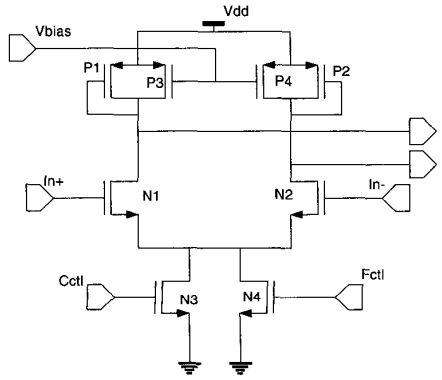

Figure 6. Delay Cell Circuit

E. Coarse Control and Fine Control Design

An addition to the basic architecture described above is noteworthy. The above arrangements for extended frequency range VCO results a large gain of VCO. Coarse control and fine control architecture is also used in PLL to reduce the gain of the VCO and reduce the jitter and phase noise [3]. The fine control of VCO will only take 10% of the total control voltage of the VCO and tremendously reduced the jitter and phase noise. The above negative feedback scheme combined with coarse control and fine control architecture generates a wide frequency range and low phase noise VCO.

III. CIRCUIT DESIGN

A. Negative Feedback Control Voltage Generator Circuit

The negative feedback control voltage generator is based on a common-source amplifier. The transistor diagram is shown in Figure 4. There are two NMOS transistors N1

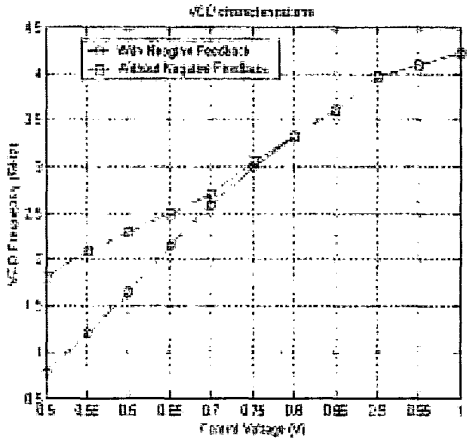
Figure 7. VCO Tuning Curve

and N2 and one PMOS transistor P1. The input signal is connected to the gate of N1 and the gate of N2 is connected to a bias voltage. P1 is diode-connected as a load and N1 is a single stage common source amplifier. The output signal is taken from the drain of N1. So when the input VC is low, NMOS transistor N1 is in cut-off region, the drain of the N1 will be pulled to a high voltage. On the other hand, when the input VC is high, N1 is on and pull the drain voltage almost to ground, i.e. the output voltage NVC will be very small.

B. Two-input Voltage-to-Current Converter Circuit

The two-input voltage-to-current converter circuit is shown in Figure 5. Control voltage VC controls the current source N4 and negative control voltage NVC controls the current source N1 which is mirrored by transistors N2, P1, P2. The output current Iout is equal to I2 subtracted from I1.

C. Delay Cell Circuit

The delay cell circuit is shown in Figure 6. The delay cell is differential pair with loading and bias controls. The self-biased techniques are used to reduce the jitter and process variations [4]. The coarse and fine control scheme is carried out by using two different tail current sources. The transistors N1, N2, N3, N4, P1, P2 are working in saturation modes while the P transistors P3 and P4 are biased in linear range as voltage controlled resistor loads.

IV. MEASUREMENT RESULTS

The VCO has been fabricated using 0.18um seven-metal CMOS process. The VCO is running in PLL and self-test circuit is built into the chip in order to measure the VCO performance. The negative feedback feature can be turned

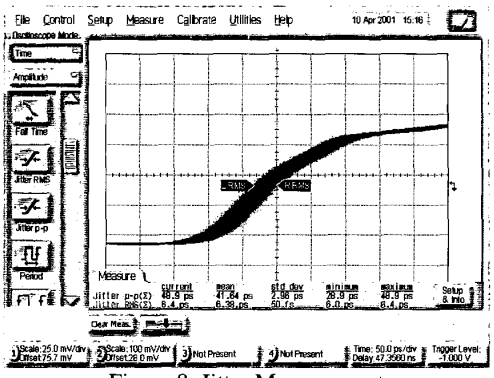

Figure 8. Jitter Measurement

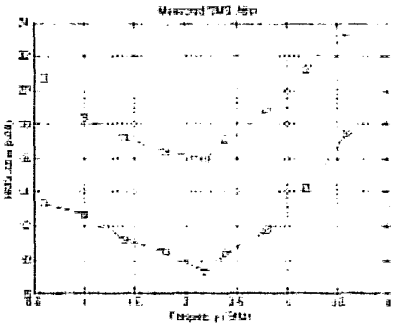
Figure 9. Measured PLL Output Jitter

on or off. The measured tuning range of VCO is shown in Figure 7. From the tuning curve, we can see the proposed architecture tremendously expanded the VCO frequency range in the lower end down to 600MHz. So it can be used for Gigabit Ethernet and Gigabit Fiber Channel

Process	0.18um 7-metal CMOS process
Power Supply	1.8V
Active Area	160umx270um
Current Consumption	20mA@3.125GHz
Operating Range	600MHz-3.3GHz with margins

Table I. Performance Summary of the Fabricated VCO

which run in 1GHz to 2GHz frequency range. The RMS jitter of the output clock of the PLL based on the VCO is also measured. WaveCrest is used to measure the jitter. The Figure 8 shows the jitter measurement at 2.5GHz output clock. In the chip, we have two PLL loops. The VCO in one loop doesn't have coarse and fine control scheme and the VCO in the other loop has enabled the coarse and fine control scheme. The jitters of both PLL clocks are measured and shown in Figure 9. From Figure 9, we can see the coarse and fine control scheme improve the jitter performance of the VCO. The following Table I show the performance summary of the fabricated VCO. The VCO has the frequency range from 600MHz to 3.3GHz with enough margins for different process corners. The VCO draws about 20mA current when it is running at 3.125GHz.

V. CONCLUSIONS

This paper presents an extended frequency range CMOS monolithic voltage-controlled oscillator (VCO) design. A negative feedback control algorithm is used to automatically adjust the VCO range according to the control voltage. Based on this analog feedback control algorithm, the VCO achieves a wide range without any pre-register settings. Low phase noise is achieved by using both coarse control and fine control in VCO. A 600MHz to 3.3GHz monolithic CMOS PLL based on this wide range and low phase noise VCO has been fabricated in TSMC 0.18um, 1.8V CMOS technology and is used in many different applications such as FC, GE, and SONET etc.

REFERENCES

[1] P. Larsson, "A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability", IEEE Journal Solid-State Circuits, vol. 34, no. 12, pp. 1951-1960, December 1999

[2] B. Razavi, Edited, "Monolithic Phase-Locked Loops and Clock Recovery Circuits Theory and Design", New York: IEEE Press, 1996

[3] C. Xu, W. Sargeant, K.R. Laker, J. Van der Spiegel, "Fully Integrated CMOS Phase Locked Loop with 30MHz to 2GHz locking range and ±35ps jitter", Proc. of the 8th IEEE International Conference on Electronics, Circuits and Systems, September, 2001, Malta

[4] J.G. Maneatis, "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE. Journal Solid-State Circuits, vol 31, no. 11, pp. 1723-1732, November 1996