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## Abstract

A 1.2 V, 38  $\mu$ W second-order  $\Delta\Sigma$  modulator ( $\Delta\Sigma M$ ) with a Signal Adaptive Control (SAC) architecture is fabricated in a 0.35  $\mu$ m standard CMOS technology ( $V_{t,n} = 0.6V$ ,  $V_{t,p} = -0.8V$ ). This modulator achieves 75 dB dynamic range and 63 dB of peak SNDR at 6.8kHz Nyquist rate and an oversample ratio of 64. The proposed architecture effectively reduces the power dissipation while keeping the modulator performance almost unchanged.

## Keywords

delta-sigma converter, modulator, oversampling, adaptive architecture

## Comments

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# A 1.2 V, 38 $\mu$ W SECOND-ORDER $\Delta\Sigma$ MODULATOR WITH SIGNAL ADAPTIVE CONTROL ARCHITECTURE

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## ABSTRACT

A 1.2 V, 38  $\mu$ W second-order  $\Delta\Sigma$  modulator ( $\Delta\Sigma M$ ) with a Signal Adaptive Control (SAC) architecture is fabricated in a 0.35  $\mu$ m standard CMOS technology ( $V_{i,n} = 0.6V, V_{i,p} = -0.8V$ ). This modulator achieves 75 dB dynamic range and 63 dB of peak SNDR at 6.8kHz Nyquist rate and an oversample ratio of 64. The proposed architecture effectively reduces the power dissipation while keeping the modulator performance almost unchanged.

## 1. INTRODUCTION

Recently, work [1] has been directed towards low-voltage/low-power  $\Delta\Sigma M$  designs with switched op-amp techniques. For an optimum power-resolution-speed trade-off in the  $\Delta\Sigma M$  design, the in-band quantization noise should be less than the in-band thermal noise. Even when this is satisfied, the first stage SC integrator usually consumes 60%-75% of the total power of the modulator. The reason for this is as follows. In the  $\Delta\Sigma M$  SC circuit, the dynamic range is limited by the voltage supply at the upper end and by noise at the lower end. For a low-voltage design, lowering the supply voltage inevitably reduces the linear signal swing, i.e. reduces the achievable dynamic range at the upper end. On the other side, it is the noise at the input node of the modulator that dominates the total noise of the modulator. This noise is proportional to  $kT/C_S$ , in which  $C_S$  is the sampling capacitance at the input node,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature. Thus, for a specific dynamic range and a reduced signal swing, the capacitors in the first integrator stage need to be large enough to suppress the noise, requiring a large current consumption and a large die area. The capacitors used in the following stages can be much smaller, because these capacitor sizes are determined by matching requirements rather than the noise. Further-

more, for a certain signal level, the integrator linearity degrades when the supply voltage is lowered. To save power and improve performance further, it is key to decrease the power and reduce the distortion at the first stage. For this purpose, this paper presents an architecture level solution, using Signal Adaptive Control (SAC) architecture.

## 2. LOW-VOLTAGE SC CIRCUIT

For advanced deep sub-micron CMOS technologies, the challenge is to implement low-voltage SC circuits without using a voltage multiplier or low-threshold devices. Using a voltage multiplier could necessitate the use of thicker gate oxides to maintain the specified MOS transistor reliability. The use of low transistor thresholds would increase the sub-threshold currents and degrade the performance of the switched capacitor circuit. In this implementation we used a switched op-amp [2] and a bootstrapped switch [3]. The bootstrapped switch in [3] was modified to be driven by a two-phase non-overlapping clock and the conventional voltage doubler was removed (see Fig.1). We also used a low-voltage class-AB differential OTA that is similar to the one being used in [1].

## 3. THE PROBLEMS IN A CONVENTIONAL ARCHITECTURE

In the conventional second-order  $\Delta\Sigma M$  (Fig.2), the first stage integrates the signal  $x[n] - v_f[n]$ . The input signal  $x$  is oversampled, therefore it can be considered constant for several successive iterations. The DAC feedback signal  $v_f$  takes the value of  $+V_{ref}$  or  $-V_{ref}$ , where  $V_{ref}$  is the reference voltage, in any iteration depending on the comparator output. As a result, the input to the first integrator stage can be as large as  $2V_{ref}$  and the output changes between two successive

iterations  $\Delta u_n = u[n] - u[n-1]$  are large. This results in a large amount of power consumption in the first stage, where large capacitances are usually used to suppress  $kT/C$  noise. If a class-AB OTA is used, its dynamic power dissipation is proportional to  $C_L(\Delta u)^2$ , where  $C_L$  is the effective load of the first stage OTA. If a class-A OTA is used, the required slew rate is proportional to  $\max(\Delta u_n)$ , the stand-by current must be large enough to accommodate the slew rate to satisfy the integration settling requirement.

In the low-voltage  $\Delta\Sigma M$  design, the first-stage configuration shown in Fig.3 is usually used. In this configuration, the OTA input common-mode signal can be set at ground to minimize the voltage supply of the OTA and to maximize the over-drive voltage ( $v_{gs} - V_t$ ) of the switches used at the input node. The disadvantage of this configuration is that the DAC feedback paths involving  $C_F$  and associated switches are introduced. This feedback path increases the effective load capacitance of the OTA, which is shown in Eq. (1).

$$C_{L,eff} = C_S + C_F + \frac{(C_I + C_S + C_F)C_L}{C_I} \quad (1)$$

where  $C_S, C_F, C_I$  are the sampling capacitance, the feedback capacitance, and the integrating capacitance respectively,  $C_L$  includes the sampling capacitance of the common-mode feedback circuits and the sampling capacitance of the next stage. The introduction of the DAC feedback paths also boosts the  $kT/C$  noise at the input node. To further improve the performance and reduce the power dissipation of the  $\Delta\Sigma M$ , in next section we propose a Signal Adaptive Control (SAC) architecture. In this architecture, we show that the feedback signal  $v_f$  to the first stage is not necessary in all integration iterations.

#### 4. SAC ARCHITECTURE

In the conventional  $\Delta\Sigma$  modulator (Fig.2), the DAC feedback signal  $v_f[n]$  to the first stage exhibits redundancy. When the analog input signal is small, i.e.  $|x| \ll V_{ref}$ , the DAC feedback signal  $v_f[n]$  takes  $+V_{ref}$  or  $-V_{ref}$  with almost equal probability. In the integration process of the first stage, the integrated contributions of  $v_f = \pm V_{ref}$  cancel each other out. This situation is equivalent to that where the first stage integrates on the input signal  $x[n]$  only. When the input signal is large, there still exist some iterations where  $v_f = +V_{ref}$  and  $v_f = -V_{ref}$  can cancel each other out, though less often than when the input signal is small. The basic operation of SAC architecture is to achieve this cancellation at successive iterations, while keeping the modulator output transparent to these actions.

This is accomplished in the SAC architecture shown in Fig.4, by adaptively controlling the switches S1, S2, S3 and S4. More detail about the SAC operation can be found in [4]. The essence of the SAC architecture is to switch off the DAC feedback to the first stage for some iterations in an adaptive manner and to compensate for the signal at the second stage. The signal load in the first stage is considerably reduced at the cost of a very small load increase in the second stage. But the overall power dissipation of the modulator is reduced because the first stage is much larger than the second stage. The signal load reduction at the first stage also improves the linearity of the first stage. The noise, distortion, and mismatching error introduced at the second stage are all suppressed with the first-order noise shaping.

*Reduced Power Dissipation.* If a class-AB OTA is used, its dynamic power dissipation is proportional to  $C_L(\Delta u)^2$ . However, the SAC operation reduces the output changes  $\Delta u$  of the first stage between two successive iterations (not for all successive iterations, but for some of them). When the DAC feedback path is switched off,  $C_F$  does not contribute to the OTA output effective load. Simulation shows that the dynamic power of the first stage can be reduced by 2/3 when the input is a sinusoid signal with an amplitude of  $0.7V_{ref}$  and a frequency of  $0.001f_s$ , where  $f_s$  is the sampling frequency of the modulator. If a class-A OTA is used, the SAC operation reduces the required slew rate (SR) of the OTA to half the SR required in a conventional modulator, which in turn reduces the power dissipation by half. In a  $\Delta\Sigma M$ , the integration settling process is more likely limited by the OTA's slew rate than by its gain-bandwidth product. The required slew rate of the first stage OTA is proportional to the maximum input level, which can be as large as  $2V_{ref}$  in the conventional architecture but is reduced to be  $V_{ref}$  in the SAC architecture.

*Improved First-Stage Linearity.* In an integration process, the nonlinear settling exists because of non-ideal factors which causes distortion. If referring to the input node, the time-domain error due to distortion can be expressed as follows [5].

$$e_n = \sum_{i=0} c_i (x[n-1] - v_f[n-1])^i \quad (2)$$

where coefficients  $c_i$  can be determined by simulation or measurements for a specific design. The SAC operation reduces the integrator input ( $x - v_f$ ) by switching off DAC feedback for some iterations, therefore, it reduces the first stage distortion.

	conventional modulator	SAC modulator
supply voltage	1.2 V	
sampling frequency	500 kHz	
signal bandwidth	300 Hz - 3.4 kHz	
max. input level	0.9 V	
peak SNR	75 dB	
peak SNDR	65 dB	63 dB
second-order distortion	-81 dB	-64 dB
third-order distortion	-62 dB	-70 dB
power consumption	60 $\mu W$	38 $\mu W$
chip core area	0.7 $mm^2$	
technology	0.35 $\mu m$ standard CMOS	

Table 1: The performance summary of the experimental prototype. The second-order and the third-order distortions were measured when the input is -3 dB of the full scale.

## 5. TEST RESULTS AND DISCUSSION

An experimental prototype, including both the conventional modulator and the proposed SAC modulator, was fabricated with a 0.35  $\mu m$  standard n-well CMOS technology ( $V_{t,n} = 0.6$  V and  $V_{t,p} = -0.8$  V). The measured performance of the prototype is summarized in Table 1. The test results show that the SAC modulator can reduce power dissipation with little to no degradation in performance. Fig.5(a) and (b) show the modulator output power spectrum plots for the conventional modulator and the SAC modulator, respectively. Fig.6(a) and (b) show the SNR/SNDR versus input plots for the conventional modulator and the SAC modulator, respectively. Comparing SAC modulator to the conventional one, the third-order distortion is reduced by 8dB, but the second-order distortion is increased by 17 dB. Ideally, the even-order harmonic distortion should be well suppressed because the fully differential configuration is employed. In reality, however, the differential circuit may not be ideally matched. Test results show that the SAC architecture is more sensitive to this kind of mismatch. This is mainly due to the three DAC feedback paths at the second stage operating in an adaptive manner. This is different from the conventional modulator where only one two-level DAC operates in all iterations, which maintains the linearity. As shown in Fig.7, simulations indicate that if the capacitor matching level of the second stage DACs is 0.1%, the second-order distortion performance of the SAC modulator is almost same as that of the conventional one. The tested distortion performance corresponds to 1% capacitor matching level of the second-stage DACs.

## 6. CONCLUSION

A 1.2 V, 38 $\mu W$  second-order  $\Delta\Sigma M$  with SAC architecture is presented. The SAC architecture effectively reduces the power dissipation while keeping the modulator performance almost unchanged. Higher than expected second-order distortions were measured for both the conventional and the SAC modulators, with that of the SAC modulator being larger. We believe that the larger SAC second-order distortion is due to its increased sensitivity to the capacitor mismatches at the second-stage DACs. Simulations indicate that improving the capacitor matching to 0.1% reduces the second-order distortion of both modulators and brings the second-order distortion of the SAC modulator to very close to that of the conventional modulator.

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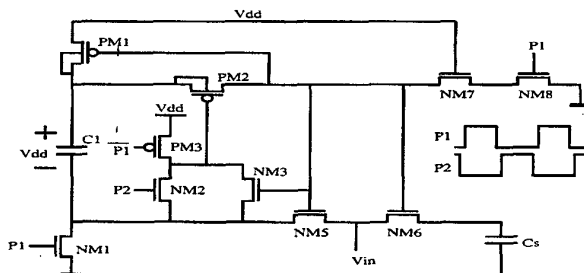


Figure 1: The bootstrapped switch used in the input node.

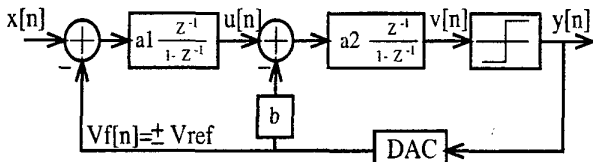


Figure 2: The block diagram of the conventional second-order  $\Delta\Sigma M$ .

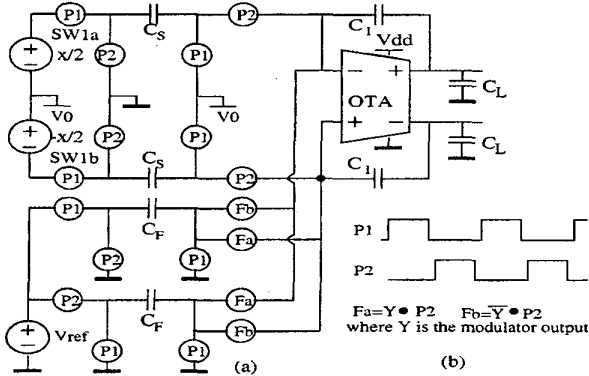


Figure 3: (a) A single-polarity reference SC integrator; (b) a non-overlapping two-phase clock and control signals. Switches SW1a and SW1b employ the bootstrapped switch shown in Fig.1.

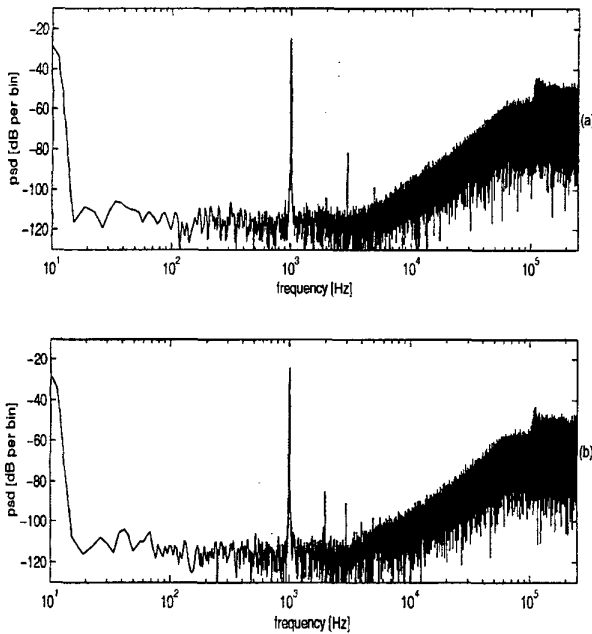


Figure 5: The measured power spectrum of the modulator output when the input is -3dB of full scale: (a) Conventional architecture; (b) SAC architecture.

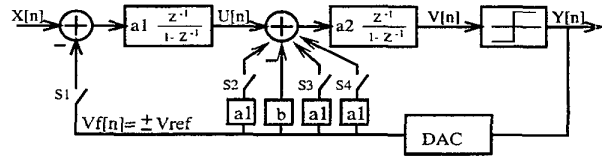


Figure 4: The block diagram of the SAC  $\Delta\Sigma M$ .

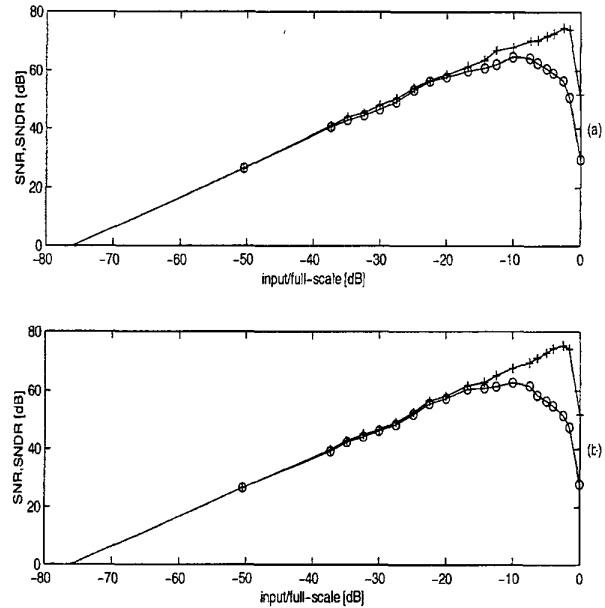


Figure 6: (a) SNR versus input curve (with sign +) and SNDR versus input curve (with sign o) for the conventional  $\Delta\Sigma$  modulator; (b) SNR versus input curve (with sign +) and SNDR versus input curve (with sign o) for the SAC  $\Delta\Sigma$  modulator.

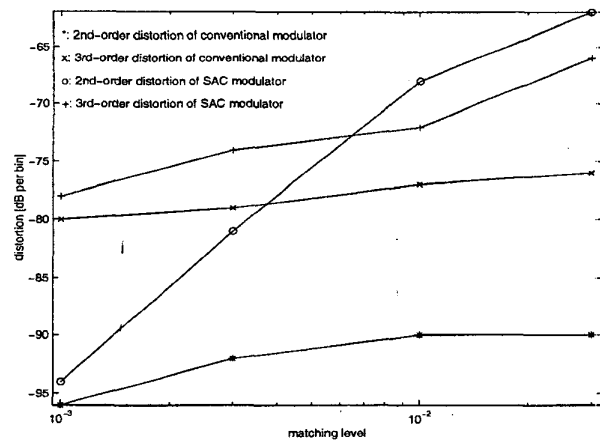


Figure 7: The distortion performance of both the conventional modulator and the SAC modulator versus the matching level of DACs at the second stage.