University of Pennsylvania
ScholarlyCommons

Departmental Papers (MEAM)

Department of Mechanical Engineering & Applied Mechanics

2009

Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches

Nipun Sinha
University of Pennsylvania, nipun@seas.upenn.edu

Timothy S. Jones
University of Pennsylvania, jonests@seas.upenn.edu

Zhijun Guo
University of Pennsylvania, zguo@seas.upenn.edu

Gianluca Piazza
University of Pennsylvania, piazza@seas.upenn.edu

Follow this and additional works at: http://repository.upenn.edu/meam_papers

Part of the Mechanical Engineering Commons

Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches

Abstract

This paper reports on the first implementation of low voltage complementary logic (< 1.5 V) by using body-biased aluminum nitride (AlN) piezoelectric MEMS switches. For the first time, by using opposite body biases the same mechanical switch has been made to operate as both an ntype and p-type (complementary) device. Body-biasing also gives the ability to precisely tune the threshold voltage of a switch. The AlN MEMS switches have shown extremely small subthreshold slopes and threshold voltages as low as 0.8 mV/dec and 30 mV, respectively. Furthermore, this work presents a fully mechanical body-biased inverter formed by two AlN MEMS switches operating at 100 Hz with a ± 1.5 V voltage swing.

Disciplines
Engineering | Mechanical Engineering

Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches

Nipun Sinha[1], Timothy S. Jones[2], Zhijun Guo[2] and Gianluca Piazza[1, 2]

[1]Department of Mechanical Engineering and Applied Mechanics, University of Pennsylvania
[2]Department of Electrical and Systems Engineering, University of Pennsylvania
Philadelphia, Pennsylvania 19104, USA. E-mail: {nipun, piazza}@seas.upenn.edu

Abstract

This paper reports on the first implementation of low voltage complementary logic (< 1.5 V) by using body-biased aluminum nitride (AlN) piezoelectric MEMS switches. For the first time, by using opposite body biases the same mechanical switch has been made to operate as both an n-type and p-type (complementary) device. Body-biasing also gives the ability to precisely tune the threshold voltage of a switch. The AlN MEMS switches have shown extremely small subthreshold slopes and threshold voltages as low as 0.8 mV/dec and 30 mV, respectively. Furthermore, this work presents a fully mechanical body-biased inverter formed by two AlN MEMS switches operating at 100 Hz with a ± 1.5 V voltage swing.

Introduction

Transistors are the fundamental building blocks that were responsible for ushering in the computational age. The ever-present push for miniaturization in the semiconductor industry has lead to continuous scaling of transistors and gate dielectrics. With the continuous scaling of planar bulk MOSFET technology to the nano-dimensions the International Technology Roadmap for Semiconductors (ITRS) has recognized the emergence of some important issues associated with the high channel doping, variability in threshold voltages and the increased effect of parasitics due to the ultra-thin body of the device. At the same time, due to these challenges it has become imperative to develop and implement new schemes of transistor operation, like Double Gate (DG) MOSFET, that require less power and can help in reducing the threshold voltages to the next level. There is also a need to investigate alternate nano devices, for a post-CMOS era, which can provide more linear and more energy efficient behavior and can replace the transistors in some applications where low power consumption is of paramount importance. The MOSFET has passive power dissipation because of the presence of a physical semiconductor channel always connecting the source to the drain. It is the sub-threshold conduction that occurs in this physical channel that leads to off-state power consumption. This loss of energy or flow of carriers in the off-state can be reduced by substituting this physical semiconductor channel with an air gap. The air-gap also helps in reducing the subthreshold slope below the 60 mV/dec level, which is governed by thermal noise in the material itself, and therefore enables the use of few mV for switching transistors on and off.

The prospect of using an air-gap opens up a whole new way of looking at a transistor. In the case of an air gap, it is no longer the modulation of a semiconductor channel that makes the transistor switch on, but it is the physical mating of contacts that turns the mechanical-transistor (switch) on. These individual mechanical transistors can be used to implement logic just like MOSFETs, but, at the same time, will provide significant power savings in both the standby state and during switching operations. Many actuation mechanisms can be used to close the aforementioned air-gap, like electrostatic, piezoelectric, magnetic, and thermal. Out of these mechanisms, piezoelectric actuation gives us the advantage of being extremely linear in nature, requiring low power for actuation, and scaling well to the nano range.

Previous experimental demonstration of a piezoelectric MEMS inverter was obtained using Lead Zirconate Titanate (PZT) (1). Several drawbacks are associated with the use of PZT. PZT is lead based and is therefore incompatible with CMOS foundries, has higher leakage than AlN, is harder to scale to the nano range because of degradation in the piezoelectric coefficients and requires complex stress calibration in order to synthesize n and p-type devices. At the same time, AlN provides high dielectric strength, easy scalability (2) and a post-CMOS compatible process. SG-MOSFET (3) has also shown low subthreshold slope operation, but relies on electrostatic actuation, which is highly non-linear and requires large voltage swings. In addition, no complementary operation was shown with the SG-MOSFET.

In this work, AlN-based piezoelectric MEMS switches have been used for implementing low-voltage (< 1.5V) complimentary MEMS logic. AlN MEMS switches have shown low subthreshold slopes and threshold voltages as low as 0.8 mV/dec and 30 mV, respectively. Two AlN MEMS switches have been used to demonstrate the first low voltage (± 1.5 V) digital inverter using body-biased AlN switches capable of fast switching (~ 220 ns). This device is presented as a micro-scale prototype of a piezoelectric NEMS alternative to CMOS logic.

Principle of Operation and Fabrication

The principle of operation of a body-biased MEMS switch is presented in Fig. 1. Two stacked layers of AlN (1 μm thick) are sandwiched between three layers of platinum (200 nm thick) that are used for the application of an electric field across the AlN films. The inverse piezoelectric effect strains the AlN films and consequently generates an equivalent bending moment about the neutral axis of the beam. Two opposing beams moving in opposite directions are employed to close a ~ 200 nm air gap and form an ohmic contact. The novel concept of body-biasing to demonstrate complementary logic is readily attainable by applying a fixed bias to one of the Pt electrodes. By doing so, the same effective electric field required to open and close the switch is applied across the AlN layer, but a much lower threshold voltage (*i.e.* a lower switching voltage) of even 30 mV (see Fig. 4), is used. A low swing voltage effectively corresponds to low switching power consumption, since exclusively this additional voltage is required to charge and discharge the gate capacitance. If the device capacitance is properly scaled, few hundred aJ switching energy (lower than state of the art CMOS) will be needed.

Complementary operation (n and p-type devices) is demonstrated by inverting the polarity of the body bias and by applying the potential to a different electrode. Positive and negative (*i.e.* n and p-type switches) threshold voltages can be attained in the same identical device, without any modification in the fabrication process. Complementary mechanical logic by using symmetric devices (not generally possible with CMOS) is therefore achieved.

The AlN switches have been fabricated on silicon substrates using an 8-mask potentially post-CMOS compatible process, as shown in Fig. 2 and previously reported in (4). A small 200 nm air gap was fabricated to achieve low voltage operation and fast switching times. The air gap (Fig. 3) is formed by patterning a thin sacrificial amorphous silicon and is released by using a XeF_2 vapor phase etching process. The dry release eliminates stiction problems that are generally encountered with wet release processes. The tip is planarized over the trench by using a photoresist refill process. The MEMS switch process (4) is easily scalable to the nano domain as shown by the demonstration of AlN nanoelectromechanical actuators by the same group (2).

Complementary Switch Technology Characterization

Fig. 4 shows the experimental validation that the same switch can be body-biased and used as a p-type or n-type mechanical transistor. Less than 1 V actuation (effectively 30-60 mV threshold voltages) for both p and n-type transistors with a body bias of 14 V has been demonstrated. The threshold voltage can also be tailored to different values by varying the applied body bias (Fig. 5). The extremely low threshold voltage is made possible by the fact that the device

has a subthreshold slope < 1 mV/dec. Thanks to the nanodimensions of the air gap and the large body bias, the device switching time has also been measured to be consistently < 1 μsec (~ 220 ns in Fig. 6). Despite the application of a large body bias, very small leakage between the body and source/drain (< 3 fA) is made possible by designing the switch in such a manner that there is no physical overlap between each other. A larger body to gate leakage of 100s of pA has been measured and is primarily due to the large capacitance currently associated with the input gate (for a 200x200 μm switch it is approximately 4.9 pF). Also, a low leakage (< 8 fA) was recorded from source to drain through the 200 nm air-gap. S-parameter measurements (Fig. 7) confirm the low leakage by showing good isolation of -54 dB at 1 GHz. Long term reliability tests have shown that these switches (with a Au-Pt contact) can operate for > 10^7 cycles with a resistance < 500 Ω, which is potentially sufficient for logic applications. This initial measurement suggests that the main issue that has hindered the commercialization of RF MEMS switches might not constitute a problem for computing applications.

Mechanical Inverter Characterization

As a proof of concept of complementary logic operations, a mechanical inverter formed by two normally open AlN MEMS switches (layout in Fig. 8) was tested at 100 Hz with a ± 1.5 V (square input wave) voltage swing (Fig. 9). The body biases for this inverter were set at + 19.9 V and - 17.2 V to synthesize p-type and n-type switches, respectively. A voltage transfer curve for a similar inverter (Fig. 10) shows the presence of two distinct voltage/logic states. Having two, clearly and sharply distinct logic states is not possible in standard CMOS technology and gives MEMS complementary logic a near ideal behavior in this testing regime.

Conclusions

Low voltage complimentary MEMS logic inverters using low subthreshold slope and fast AlN piezoelectric MEMS switches have been demonstrated for the first time by implementing a body-biasing technique. This MEMS prototype validates the low power functionalities (both standby and switching power) that can be achieved via mechanical transistors. Body-biasing in piezoelectric mechanical transistors has demonstrated the capability to make the same device function as a p-type or n-type transistor and has also enabled the tuning of the threshold voltage of a single switch.

References:
(1) D. Judy, *et al.*, *Workshop on Solid State Sensor, Actuator and Microsystems,* pp. 328 – 331, 2008.
(2) N. Sinha, *et al.*, *Applied Physics Letter,* 95, 053106, 2009.
(3) N. Abelé, *et al.*, IEDM, Late News, pp. 479-481, 2005.
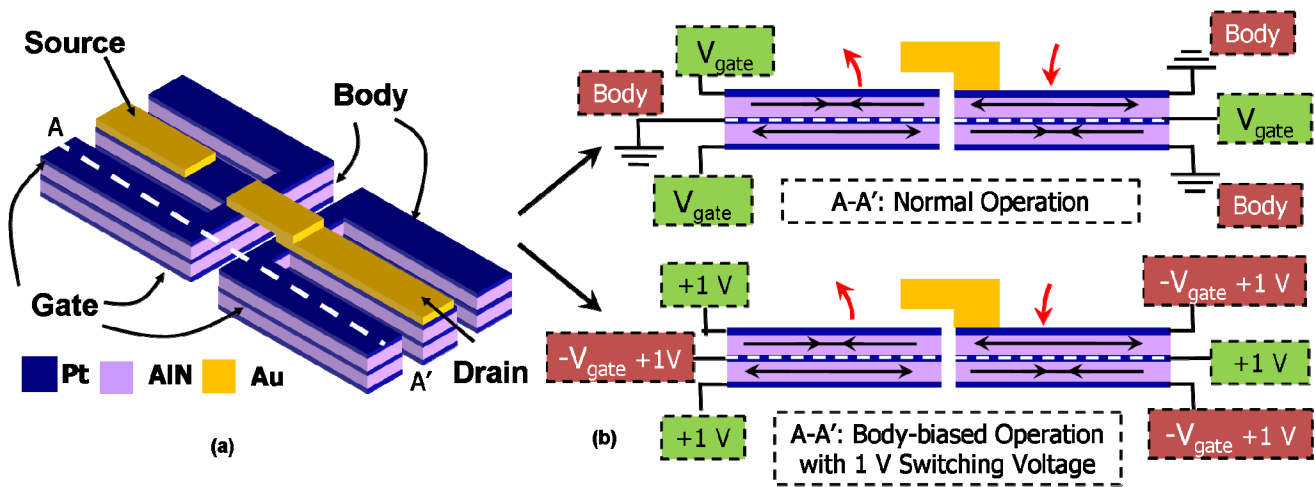(4) R. Mahameed, *et al.*, *J. Micromech. Microeng.* 18**,** 105011, 2008.

Fig. 1: (a) 3D schematic of the dual-beam AlN switch highlighting the source, drain, gate and body terminals. (b) Schematic representation of the principle of operation of an AlN MEMS switch in normal and body-biased mode of operation. By applying a bias to the body terminal ($-V_{gate} + 1$ V), the same effective voltage required to open and close the switch is applied across the AlN layer. The gate voltage can be lowered to < 1 V (1 V is used in the figure) and effectively reduces the energy required for the switching operation. The gold tip is drawn to show the direction of motion.
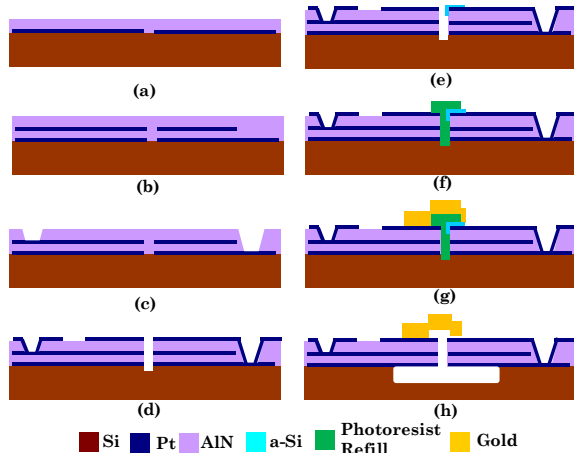
Fig. 2: An 8-mask post-CMOS compatible process is used for the fabrication of the AlN switches. The process is described in details in (4). a-Si and XeF_2 release are used to form the 200 nm air gap. Gold was used for quick prototyping of the contact, but can be replaced by any other CMOS compatible metal.
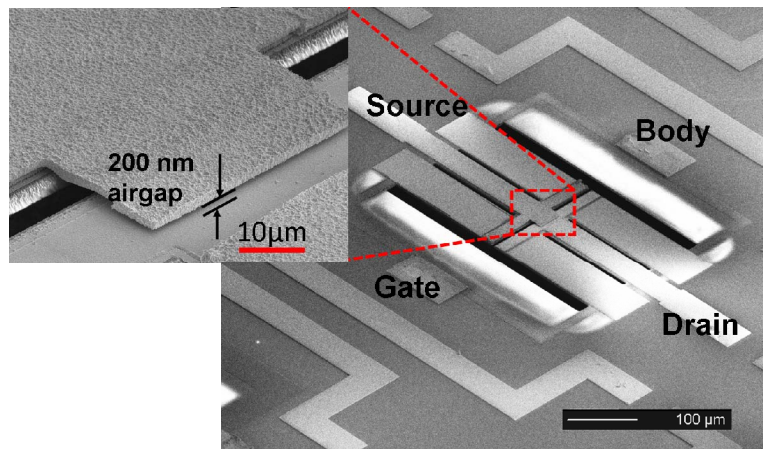

Fig. 3: A SEM of a fabricated AlN MEMS switch with a zoomed in view of the planarized nano-air gap (~ 200 nm) that is created by amorphous silicon and is released in the same step as the rest of the structure by XeF_2. Single gate and body terminals are created by appropriate electrode routing.
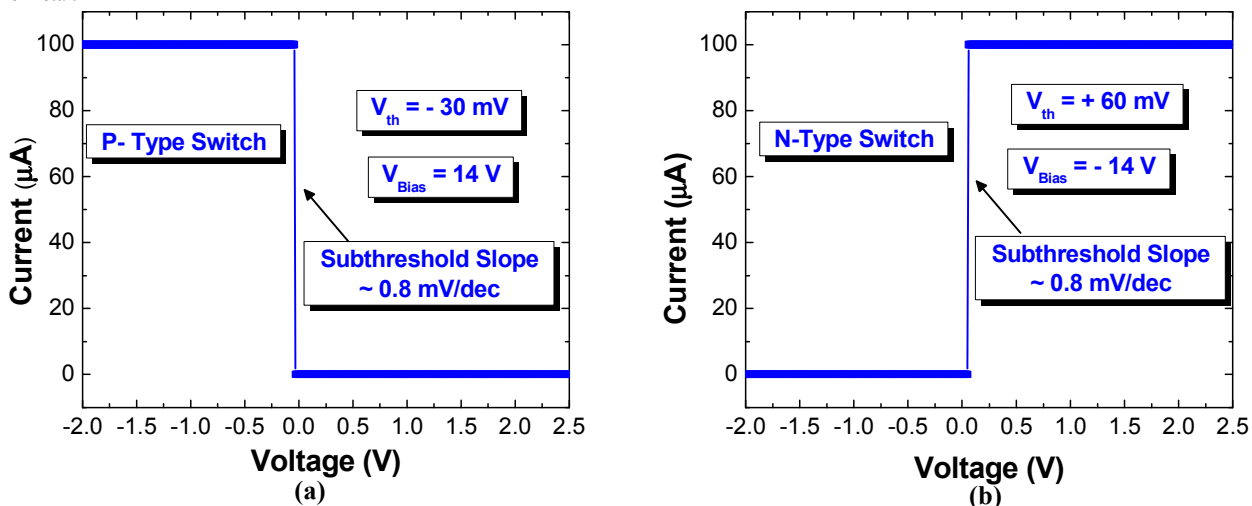

Fig. 4: Results of testing of the same switch as p-type and n-type mechanical transistor. (a) In a p-type implementation with a positive body bias of 14 V (V_{bias}) the switch was switched on with a small threshold voltage (V_{th}) of - 30 mV. (b) In an n-type implementation with a negative body-bias of - 14 V the same switch was switched on at + 60 mV. A subthreshold slope of ~ 0.8 mV/dec was recorded for both switches. The current measurement was limited to a maximum value of 100 µA.
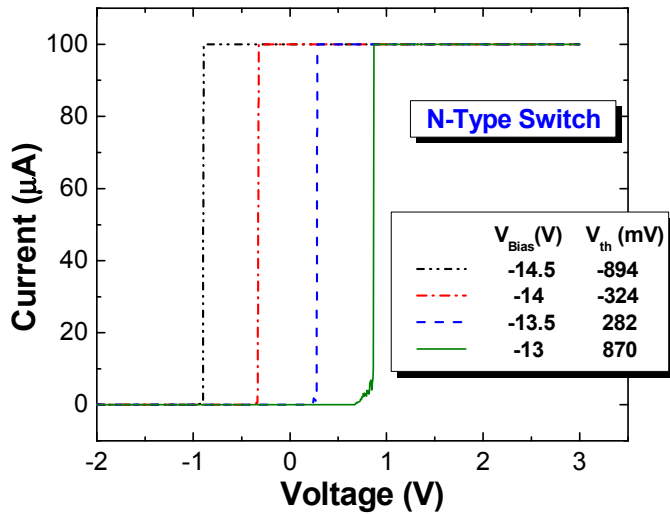
Fig. 5: Experimental data verifying that the switch threshold voltage (V_{th}) can be tuned by varying the value of the body bias. This data show that the body-bias technique enables the implementation of variable threshold voltages on the same die and in the same process. The current measurement was limited to a maximum value of 100 μA.
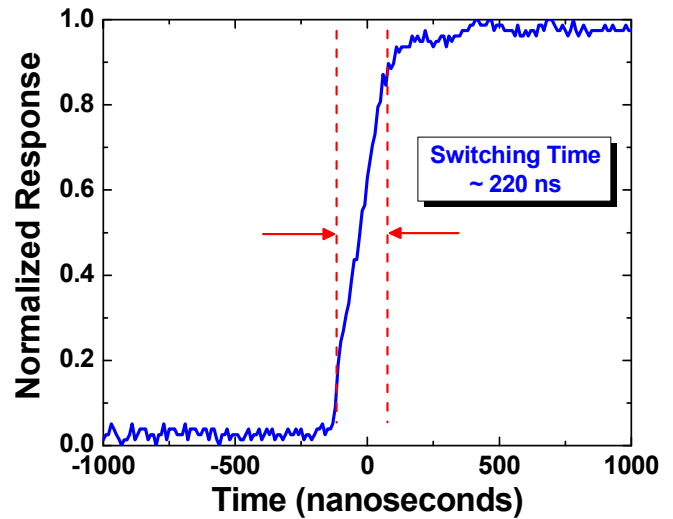

Fig. 6: Switching time measurements were performed for many AlN MEMS switches. The switches have consistently exhibited very fast switching. In the figure we show the plot of a switch turning on in ~ 220 ns.
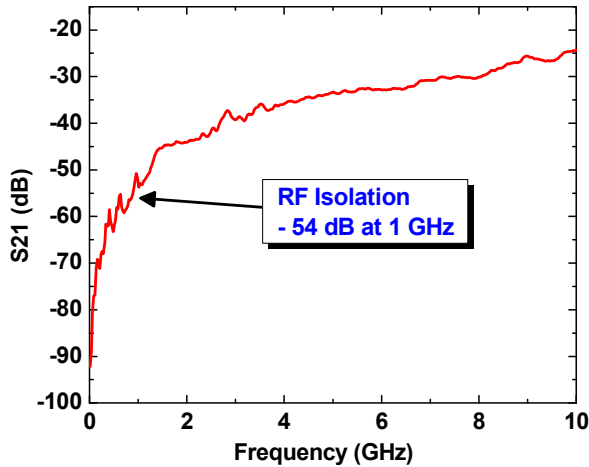

Fig. 7: S - parameter measurements were performed using an Agilent N5230 PNA-L network analyzer. The switch shows very good isolation up to GHz frequencies. It exhibits -54 dB isolation at 1 GHz and - 44 dB isolation at 2 GHz.
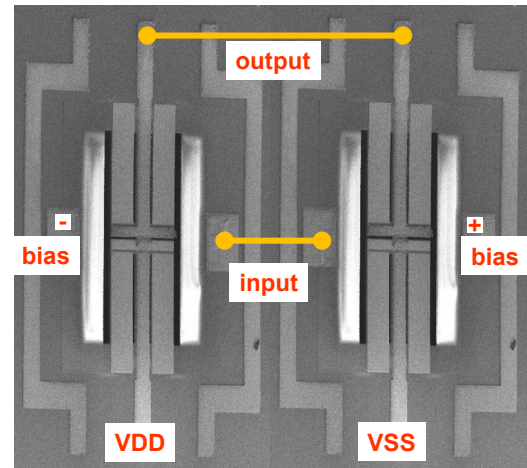

Fig. 8: The figure shows the two MEMS switches used for the testing of the complementary MEMS inverter. V_{DD}= + 1.5 V, V_{SS}=-1.5 V, V^+_{bias}=+19.9 V, V^-_{bias} = -17.2 V. A square wave input of ± 1.5 V was used.
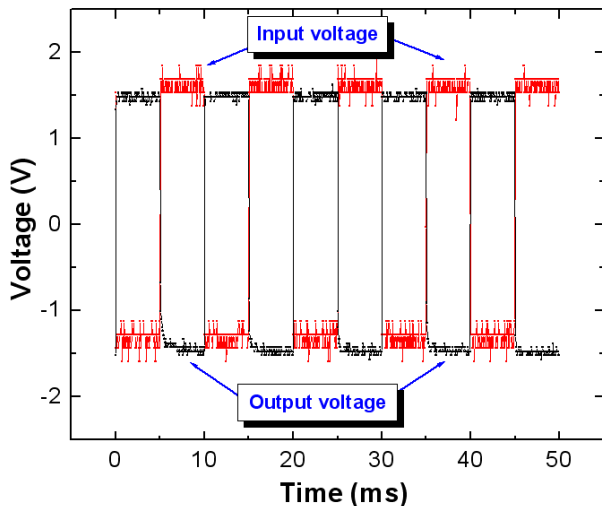

Fig. 9: By using two normally open AlN MEMS switches an inverter operating at 100 Hz with an input waveform of ± 1.5 V was demonstrated. This verifies that body-biasing technique can also be used in dynamic operations. 1 kHz inverter with ± 7.5 V was also demonstrated with another set of switches.
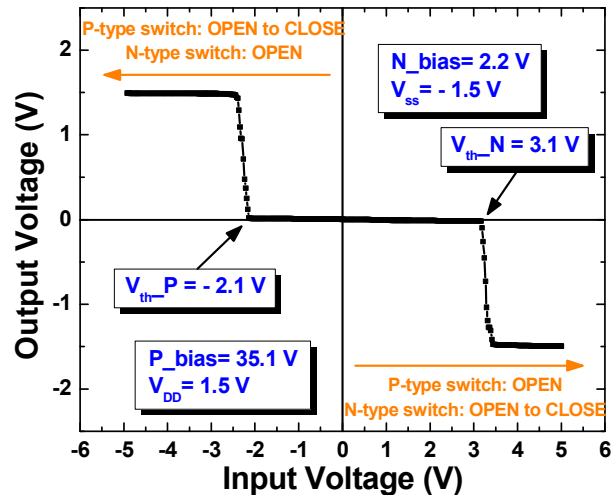

Fig. 10: Voltage transfer curve for another AlN MEMS inverter. This response approaches the ideal inverter transfer function with sharp transition between different logic states. This is not possible with standard CMOS technology. The V_{DD} and V_{SS} were limited to ± 1.5 V and the V_{th} was - 2.1 V and 3.1 V for the p-type and n-type switch, respectively.