September 1994

A CMOS Time to Digital Converter IC with 2 Level Analog CAM

Eric J. Gerds
University of Pennsylvania

Jan Van der Spiegel
University of Pennsylvania, jan@seas.upenn.edu

Rick Van Berg
University of Pennsylvania

Hugh H. Williams
University of Pennsylvania

L. Callewaert
Kath. University of Leuven

See next page for additional authors

Copyright 1994 IEEE. Reprinted from *IEEE Journal of Solid State Circuits*, Volume 29, Issue 9, September 1994, pages 1068-1076.
Publisher URL: http://dx.doi.org/10.1109/4.309902

A CMOS Time to Digital Converter IC with 2 Level Analog CAM

Abstract
A time to charge converter IC with an analog memory unit (TCCAMU) has been designed and fabricated in HP's CMOS 1.2-μm n-well process. The TCCAMU is an event driven system designed for front end data acquisition in high energy physics experiments. The chip includes a time to charge converter, analog Level 1 and Level 2 associative memories for input pipelining and data filtering, and an A/D converter. The intervals measured and digitized range from 8-24 ns. Testing of the fabricated chip resulted in an LSB width of 107 ps, a typical differential nonlinearity of < 35 ps, and a typical integral nonlinearity of < 200 ps. The average power dissipation is 8.28 mW per channel. By counting the reference clock, a time resolution of 107 ps over ~ 1 s range could be realized.

Keywords
time to charge converter, CAM, pipelining, associative memory

Author(s)
Eric J. Gerds, Jan Van der Spiegel, Rick Van Berg, Hugh H. Williams, L. Callewaert, W. Eyckmans, and Willy Sansen

A CMOS Time to Digital Converter IC with 2 Level Analog CAM

Eric J. Gerds, *Student Member, IEEE*, J. Van der Spiegel, *Senior Member, IEEE*, R. Van Berg, *Member, IEEE*, H. H. Williams, *Member, IEEE*, L. Callewaert, *Student Member, IEEE*, W. Eyckmans, and W. Sansen, *Senior Member, IEEE*

Abstract— **A time to charge converter IC with an analog memory unit (TCCAMU) has been designed and fabricated in HP's CMOS 1.2-μm n-well process. The TCCAMU is an event driven system designed for front end data acquisition in high energy physics experiments. The chip includes a time to charge converter, analog Level 1 and Level 2 associative memories for input pipelining and data filtering, and an A/D converter. The intervals measured and digitized range from 8–24 ns. Testing of the fabricated chip resulted in an LSB width of 107 ps, a typical differential nonlinearity of < 35 ps, and a typical integral nonlinearity of < 200 ps. The average power dissipation is 8.28 mW per channel. By counting the reference clock, a time resolution of 107 ps over $\sim$ 1 s range could be realized.**

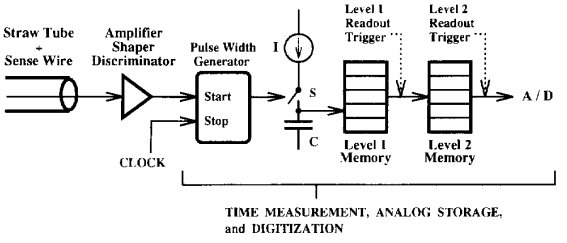


Fig. 1. Front-end readout system in a collider detector, including the time to digital converter (TDC).

I. Introduction

TIME to digital converters (TDC's) have a variety of industrial and research applications. They are used in time of flight (TOF) measurement systems as well as test equipment for electronic circuit characterization. TOF systems include such examples as laser range finders, positron emission tomographs, and various high energy physics particle detectors. To satisfy the increasingly stringent requirements of data acquisition in colliding beam physics experiments, a VLSI chip called the TCCAMU (time to charge converter with an analog memory unit) has been designed.

In large scale particle detectors, the particle tracks resulting from the beam collisions must be reconstructed as precisely as possible. Straw tube drift chambers, for example, accomplish track reconstruction by measuring electron drift times. The electrons are created when the charged particles being detected ionize the gas in the straw tubes [1]. It is therefore necessary to measure the electron arrival times at each of the drift chamber's many thousands of sense wires. A typical front end readout channel associated with a sense wire is shown in Fig. 1.

The charge signal on a sense wire first must undergo amplification and shaping. If the amount of charge arriving at the wire exceeds a predetermined threshold, a Discriminator (Discr) pulse will be generated. A high resolution TDC must then measure the arrival time of this Discr pulse with respect to an edge of the system clock. The random arrival times of the sense wire signals dictate a TDC double pulse resolution as small as 20–30 ns.

Asynchronous multichannel systems such as this often produce large amounts of data. Since only certain events found by the detectors are of interest, much of the data needs to be discarded at various levels by the front end readout electronics. Data filtering can be accomplished by readout triggers generated external to the front end electronics (Fig. 1). The filtering may occur before and/or after digitization of the signals.

Current generation detectors have $\sim 10^5$ channels, while future detectors could have even more. Such massive parallelism imposes very strict requirements on the data acquisition circuitry. Typically, the front end readout electronics must have (per channel) a high circuit density, a low power dissipation not more than several tens of mW, TDC resolution < 0.5 ns, TDC double pulse resolution of 20–30 ns, buffers for data filtering, a minimum of calibration constants for each channel, and good gain matching between channels [2].

There are various TDC architectures one might consider using to satisfy these requirements. One type of digital TDC architecture, for instance, uses a feedback stabilized delay line. This type of converter digitizes time intervals very quickly and with a low power dissipation. The LSB width for the Time Memory Cell (TMC) by Arai *et al.* [3] and similar circuits is typically $\sim$ 1 ns. Feedback stabilized delay lines are more power efficient than high speed counters or shift registers for time measurements.

A second TDC approach involves a digital vernier technique [4]. Short time intervals are expanded by beat signals and then interpolated. Essentially this gives a very high resolution measurement of the delay between 2 periodic signals. While

Manuscript received January 7, 1994; revised May 18, 1994.

E. J. Gerds and J. Van der Spiegel are with the Electrical Engineering Department, University of Pennsylvania, Philadelphia, PA 19104 USA.

R. Van Berg and H. H. Williams are with the Physics Department, University of Pennsylvania, Philadelphia, PA 19104 USA.

L. Callewaert, W. Eyckmans, and W. Sansen are with the Katholieke Universiteit Leuven, Belgium.

IEEE Log Number 9404022.

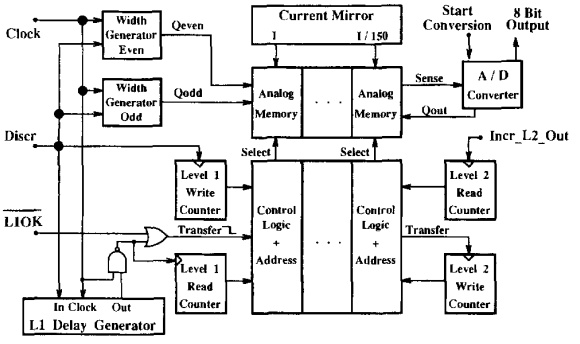


Fig. 2. Block diagram of the TCCAMU circuit.

the digital vernier TDC can achieve $\sim$ 1 ps resolution using bipolar technology, it would not be practical in systems with an asynchronous single pulse input.

A third approach is based on an analog technique, such as that discussed by Stevens [5]. By integrating a current "I" on a capacitor during the time interval being measured, we have a time to voltage converter. The resulting voltage can then be digitized. Although this technique can be more complicated to implement than the stabilized delay line architecture, it does achieve sub-nanosecond resolution in addition to low power dissipation. This analog approach can be subdivided into two groups: those analog TDC's using a time-to-voltage converter (TVC) and those using a time-to-charge converter (TCC).

The TCC, which is part of a dual slope converter, is well suited for massively parallel data acquisition systems. It has the advantages over the TVC of insensitivity to capacitor and integration current variations, and a calibrationless gain. The TCCAMU chip discussed in Section II utilizes a CMOS TCC, giving it a very low power dissipation and a subnanosecond resolution.

II. TCCAMU Architecture

A. Overview of TCCAMU

The TCCAMU measures time intervals, stores and filters the measured data in analog memory, and finally performs a digitization. The interval to be measured occurs between the leading edge of an asynchronous Discr pulse and an edge of the system clock. The system clock frequency for the TCCAMU is 62.5 MHz (16-ns period). By counting the clock cycles, it should be possible to accurately determine the arrival time of a Discr pulse over a wide dynamic range.

A time to charge conversion starts with a Discr pulse activating one of two width generators (Fig. 2). The even and odd generators take turns accepting Discr inputs, resulting in time measurements with improved double pulse resolution. The selected width generator generates an output pulse whose width equals the interval being measured. For the duration of this output pulse, the TCCAMU steers a current "I" onto an integration capacitor in its analog memory. The resulting charge is proportional to the measured time interval.

The analog associative memory which stores and filters the charge data consists of Level 1 and Level 2 buffers. The read/write locations in both buffers are chosen by the Level 1 Read/Write counters and the Level 2 Read/Write counters. The outputs of the counters are decoded by control logic to select the proper capacitors in the associative memory.

The signal from a time to charge conversion is stored initially in Level 1 for 1 μs. Because only a fraction of the events found by a particle detector will be useful, the system external to the chip will usually decide to discard the signal during that 1 μs. Signals that are kept are transferred to Level 2 for a longer term storage. Additional filtering in Level 2 decided by the external system occurs before the actual digitization.

The Level 1 delay generator shown in Fig. 2 determines the storage time in the Level 1 analog buffer. A Discr pulse applied to the $L1$ delay generator input produces an output pulse 1 μs later. If the external system decides to keep the signal during that time, a Level 1 readout trigger called $L1OK$ (Level 1 datum OK) is given to the chip at the end of that 1 μs delay. This in turn causes the Level 1 datum to be transferred to the Level 2 analog memory. If the $L1OK$ pulse were not present at the end of that 1 μs, the Level 1 signal would be discarded. Future chip versions could contain a programmable $L1$ delay generator, yielding an adjustable $L1$ trigger latency for the TCCAMU.

Note the absence of a Level 2 delay generator. The latency in the Level 2 buffer is not predetermined.

Any signal that passes through both levels of the analog memory will then be digitized by the on chip Wilkinson A/D converter. A current "I/150" discharges the appropriate storage capacitor while the number of clock cycles are counted, resulting in an output digital word.

An important issue here is that the analog variable being stored and digitized is a charge, not a voltage. The TCCAMU gain therefore depends on the ratio of the charge and discharge currents, "I" and "I/150" respectively. This ratio can be made relatively process insensitive. Mismatches between channels in the integrating current "I" have little effect on the TDC gain matching. Mismatches in the integrating capacitors within and between channels also have little effect. Gain calibrations for the TCCAMU in a multichannel system would therefore be unnecessary.

For TDC's using a time-to-voltage converter (TVC), on the other hand, it is the capacitor voltage that is digitized. The gain would depend on the absolute value of the integrating current and the integrating capacitors. For multichannel systems, it can be cumbersome dealing with gain mismatches and gain drifts.

B. Width Generator

The time interval Δt to be measured and digitized by the TCCAMU occurs between a Discr pulse's leading edge and a rising edge of the system clock. The width generator (Fig. 3) produces an output pulse of width Δt, leading to a charge IΔt being placed on the appropriate storage capacitor.

The capacitors in the analog memory are reset to a reference level prior to the time to charge conversion (reset switches are not shown). During the standing state, transistor M is on and transistors $M0 - MN$ are off. When the width generator

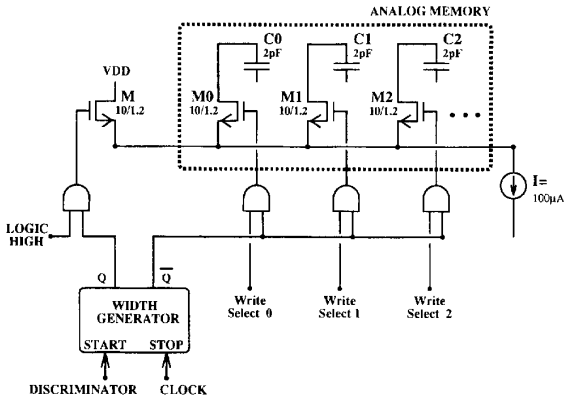
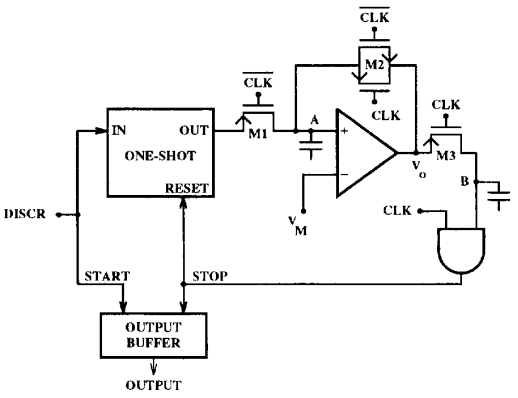
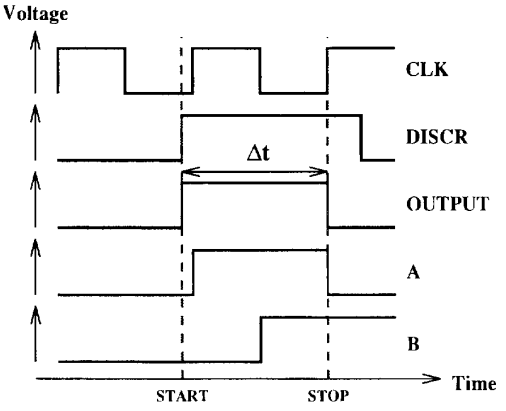


Fig. 3. Simplified schematic of the width generator and analog memory.



(a)



(b)

Fig. 4. (a) Block diagram of the width generator with internal positive feedback. (b) Time measurement of delay between leading Discr edge and a Clock edge. Measurement range is 1/2–3/2 clock cycles.

detects a Discr input pulse, it STARTS the integration as the current "I" is steered to the selected capacitor. The width generator waits for a falling clock edge, and then uses the rising clock edge after that to STOP the integration (see Fig. 4(b)). This waiting feature gives us a pulse width range of 8 ns $< \Delta t <$ 24 ns, thereby avoiding any nonlinearities due to zero integration times.

A simplified schematic for a width generator and the relevant waveforms are shown in Fig. 4. Much of the circuitry in the generator is devoted to determining which rising clock edge will stop the integration. The Discr enters the one shot, which guarantees a minimum pulse width at the source of $M1$. When the clock goes high, node A also goes high, causing the comparator output V_o to switch high. When the clock then goes low, node B goes high. The next rising clock edge then generates the STOP signal, which resets the one-shot.

The important issue of metastability arises here when the falling clock edge occurs at the same time as the rising Discr edge. Transistor $M1$ will start turning off just as the output of the one-shot begins to raise $M1$'s drain voltage. This case would produce an analog voltage at node A instead of a well defined logic level. The width generator could then become metastable, resulting in an arbitrarily wide pulse output. When the CLK goes low, however, $M2$ closes the positive feedback loop. This forces the comparator to resolve the analog voltage to a valid logic level usually within 1/2 clock cycle. A positive feedback loop therefore greatly reduces the range of Discr arrival times that cause metastable behavior.

In order to reduce the comparator's area and eliminate its dc power dissipation, the "comparator" was made to consist merely of 2 inverters in series. The feedback switch $M2$ connects the output V_o of the second inverter to the input A of the first. The voltage V_M shown in Fig. 4(a) is actually the metastable voltage for these 2 inverters when $A = V_o$. When $M2$ closes, the comparator produces a logic "1" if $V_o > V_M$ and a logic "0" if $V_o < V_M$.

C. Analog Input Pipeline with Data Filtering

In asynchronous systems such as particle detectors, the Discr input to a TDC arrives at random points in time. The question naturally arises as to how we can handle the worst case Discr input rates. For this discussion, let:

DT_{MIN}	minimum time between successive Discr arrivals,
DT_{AVE}	average time between successive Discr arrivals,
CT	conversion time for a digitization, and
S	Discr rejection factor.

DT_{MIN} is the double pulse resolution requirement of the TDC, which equals 20–30 ns. The average time DT_{AVE} between successive Discr arrivals in a drift tube chamber is assumed to be $\sim$ 100–200 ns. Only 1 in S Discr inputs are left over after data filtering in the detector front end electronics, where typically $S \sim 10^4 - 10^6$. The filtering can be accomplished before and/or after the time interval digitization.

Given the average and the maximum input rates to a TDC, we can make one of several choices. Assuming we wanted to digitize all the incoming data, we could use a flash TDC where $CT < DT_{MIN}$. This condition would guarantee that data never arrives faster than the converter can handle. The disadvantages of the flash converter, however, are its

complexity, a large power dissipation, and a large chip area. In massively parallel data acquisition systems, a very high speed TDC would not necessarily be the most efficient approach.

An alternative would be to use an analog memory which stores the incoming data before digitization. This is analogous to a pipelined sample and hold in a voltage sampling A/D converter. We would thus have the more relaxed requirement of $CT < DT_{AVE}$. On those occasions when $CT > DT$, the data would simply pile up in the analog buffer until serviced by the A/D converter. The TCCAMU uses this approach.

The speed requirements for an input pipelined TDC are easier to satisfy. This approach requires a much simpler A/D with less power dissipation and less chip area. The reduced complexity of the circuitry would allow a number of TDC channels to be placed on a single die substrate for use in a high density front end readout system.

Additional advantages in using analog input buffers have to do with the data filtering. Obviously, it would be much more power efficient to decimate the information in an analog pipeline before digitization. Using the rejection factor, we also see that the converter now would need to satisfy the condition $CT < (S) \times (DT_{AVE})$ where $S >> 1$.

Note that there will be occasions when the pipeline overflows due its finite size and the finite CT. One can determine the minimum number of storage locations needed in the pipeline using queuing theory or Monte Carlo simulations [6]. The minimum size of the analog buffer will be determined by a number of factors: DT_{MIN}, DT_{AVE}, CT, S, the storage time in the analog pipeline (or queue), the maximum acceptable probability that the pipeline will be full when a Discr input arrives, and of course the probability distribution for the Discr arrival times.

D. Two Level Analog Content Addressable Memory

The analog memory in the TCCAMU consists of 12 shielded storage capacitors. The capacitors use the gates of PMOS transistors placed in an isolated n-well. These 12 storage devices are part of a 2-level analog content addressable memory (CAM). The CAM is used to implement the analog input pipeline.

In general, an analog CAM has write, read, and match functions. A write operation stores analog information in unused word locations. A match operation involves a parallel search through all the stored words for a match with the input word. The read operation returns the analog information associated with the matched word [7].

In the TCCAMU chip, the analog CAM is divided into 2 levels: Level 1 and Level 2. The Level 1 buffer accesses 8 storage capacitors and the Level 2 buffer accesses 4. A data register assigned to each of the analog storage capacitors holds a unique address and ID tag. A capacitor, therefore, is chosen for read/write operations according to the contents of its data register. The ID tag contained by register i identifies the level (1 or 2) that capacitor i is associated with, and the address contained by register i is the address within that level.

Because the contents of data register i can be changed, it is possible to "move" the data on capacitor i from one CAM level to another without actually disturbing the analog information on that capacitor. This is the reason for choosing an analog CAM over an analog RAM.

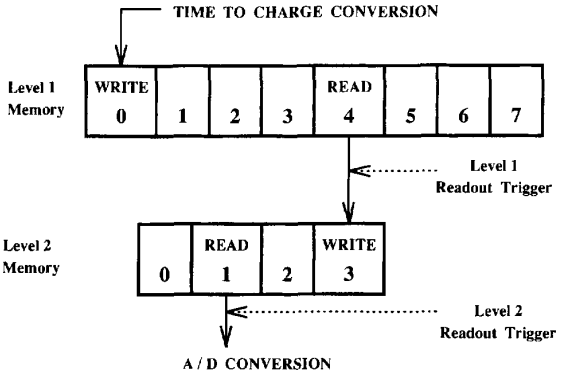


Fig. 5. Data flow through the 2 Level analog CAM (content addressable memory).

The two-level analog CAM outlined in Fig. 5 has simultaneous Read/Write capabilities for both levels. During the CAM's Level 1 write operation, the charge generated by a time measurement is placed on the capacitor whose Level 1 address matches the address chosen by the Level 1 Write counter (Fig. 2). Let this be referred to as address j. After a 1 μs latency, a Level 1 Read operation occurs whereby address j for that capacitor now matches the address given by the Level 1 Read counter. An $L1$ readout trigger will then determine whether to discard the $L1$ datum being read ($L1$ reject) or to accept the datum for further processing ($L1$ accept). An $L1$ accept results in the data register contents being changed from a Level 1 address j to a Level 2 address k. The Level 2 Write counter determines the address k that is loaded into the register. This operation of transferring analog data from address j in Level 1 to address k in Level 2 can simply be called a virtual Level 1 to Level 2 transfer. After an undetermined latency, the Level 2 Read counter will choose address k for a Level 2 read operation. A Level 2 readout trigger can then accept or reject that datum. If it is accepted, the analog data at address k will be digitized. The TCCAMU thus has 2 levels of filtering prior to digitizing a measured time interval.

Note that there are several requirements for a Level 1 to Level 2 transfer. First of all, the transfer must be accomplished quickly so that the Level 1 address j can be made available for writing again. Secondly, we do not want the analog information being transferred to be corrupted by the transfer process itself. Thirdly, we should dissipate as little power as possible to minimize the total power of the multichannel system.

A virtual Level 1 to Level 2 transfer satisfies the previous requirements. Instead of transferring the charge itself from one capacitor to another (as in an analog RAM), we have the data registers for the $L1$ Read capacitor and the $L2$ Write capacitor swap their contents. As a result, the analog information on a capacitor is never disturbed during a $L1$ Read or $L2$ Write operation. Hence there is no need for any high

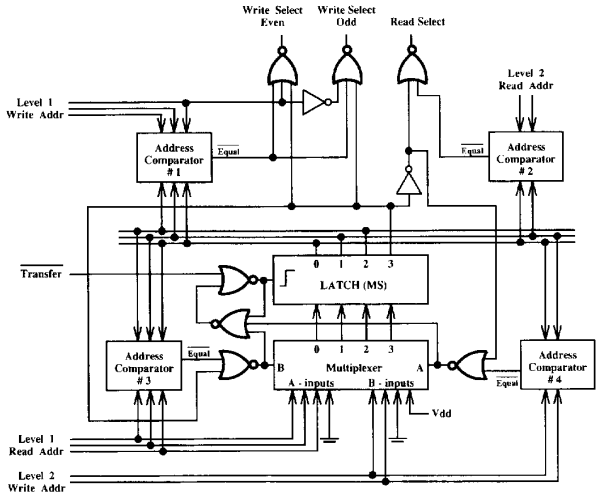


Fig. 6. Block diagram of the control logic for each storage capacitor in the analog CAM.

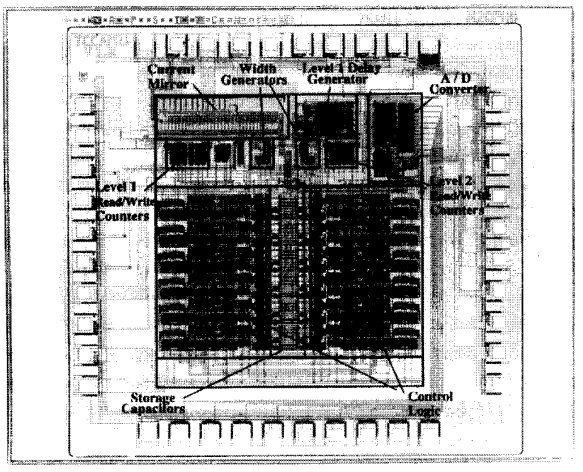


Fig. 7. Microphotograph of the TCCAMU chip.

power unity gain amplifiers to do a fast charge transfer, since these amplifiers would introduce unwanted gain and offset errors.

E. Control Logic for the Analog Memory

Each capacitor in the analog memory has a control logic circuit (Fig. 6). Each control block can select its capacitor for reading and writing. The logic basically consists of a latch, which contains the storage capacitor's virtual address, and 4 address comparators. The comparators check for a match between the latch contents and the Level 1/Level 2 Read/Write addresses.

The capacitors in the analog memory are accessed for read/write operations according to the contents of their address latches. Hence we have a content addressable memory. Each latch contains a unique address so that no two capacitors undergo the same operation at the same time.

Bits 0–2 of the master–slave latch hold the virtual address, and Bit 3 contains the ID tag. When the capacitor belongs to the Level 1 CAM, the ID tag = 0. The Level 2 CAM has an ID tag = 1.

Comparators #1 and #2 select the capacitor for Level 1 Write and Level 2 Read operations, respectively. In a Level 1 Write operation, the "Write Select" output (even or odd) of the control logic permits the width generator (even or odd) to place charge on that capacitor. In a Level 2 Read operation, the "Read Select" output permits the Wilkinson A/D to remove charge from the capacitor during a digitization.

Comparators #3 and #4 select the capacitor for Level 2 Write and Level 1 Read operations, respectively. They choose the 2 capacitors that will swap virtual addresses during a Level 1 to Level 2 data transfer. For the capacitor whose comparator #3 sees a match between its latch contents and the Level 1 Read address, the multiplexer passes the Level 2 Write address to the latch input. For the other capacitor whose comparator # 4 sees a match between its latch contents and the Level 2 Write address, the multiplexer passes the Level 1 Read address to the latch input. When the signal Transfer then goes low, these two latches accept their inputs to complete the Level 1 to Level 2 transfer.

III. Experimental Results

The TCCAMU shown in Fig. 7 has been fabricated in HP's CMOS 1.2-μm n-well process, and has been tested with an HP82000 chip tester. This 2.0 mm $\times$ 2.2 mm circuit has 9700 transistors, with 8 storage locations in its analog Level 1 CAM, and 4 storage locations in its analog Level 2 CAM. The digital logic in this IC operates between -3 V and 0 V power supplies, while the analog circuitry operates between -3 V and +3 V.

The average power dissipation during A/D conversions was measured to be 8.28 mW / channel. The $L1$ delay generator, consisting of numerous clocked shift registers, dissipates $\sim$ 3 mW according to simulations. The current mirror uses $\sim$ 0.75 mW, and the on chip A/D dissipates the rest of the power.

Measurements to test the analog memory revealed a charge leakage of 1 LSB roughly every 25 s at room temperature. Signals placed on any given capacitor did not influence the data on any adjacent storage capacitors. Due to the analog input pipeline, the TCCAMU achieved a double pulse resolution between 16–32 ns, despite a 4-μs conversion time.

The differential nonlinearity (DNL) of an A/D converter can be defined as the difference between the actual width of an output code and the ideal width of that code. The DNL of the TCCAMU was measured using a code density test (see Appendix). In this particular test, the probability distribution of the randomized Discr input was a Gaussian. A histogram of the outputs was produced, and the widths and DNL's of the output codes were calculated from this information. Typically the DNL at any given analog storage site was measured to be $<$ 35 ps (see Fig. 8), and the rms DNL over all output codes was 10 ps rms. Using 1000 input samples to measure the width of each LSB, we obtained an uncertainty in the DNL measurements of $<$ 8.5 ps rms.

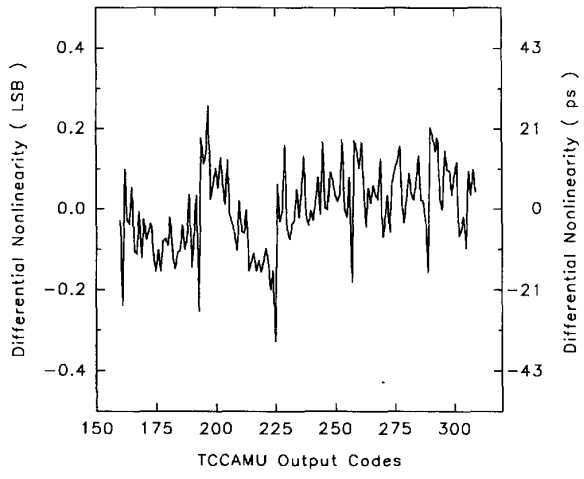


Fig. 8. Typical differential nonlinearity data at a given analog memory location.

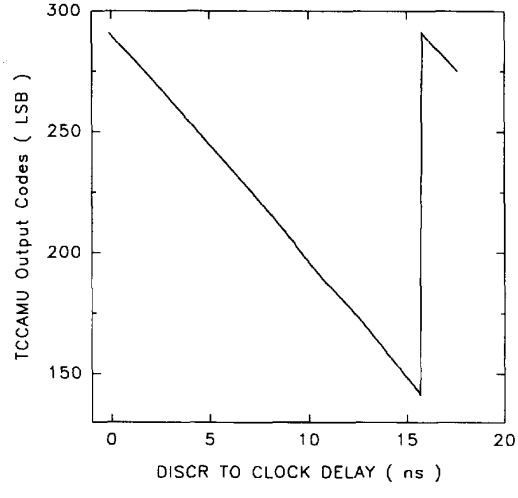


Fig. 9. Analog input versus digital output of the TCCAMU.

In order to find the analog input versus digital output curve for the TCCAMU, a known input time interval was supplied to the chip, and the outputs were recorded. A Gaussian jitter was intentionally added to the input Discr delay. For each particular input delay, 250 corresponding output samples were taken and averaged over this jitter to get a precision within a fraction of an LSB. With interpolation, the input delay corresponding to the center of an output LSB was found, resulting in the analog input versus digital output plot in Fig. 9. Note that the timing nonlinearities of the calibrated test system supplying the Discr signals had to be much smaller than the timing nonlinearities of the TDC being measured.

The output shown in Fig. 9 is a sawtooth waveform with a periodicity equal to that of the 16 ns system clock. The input range to the TCCAMU therefore is also 16 ns. By counting the clock cycles, however, it will be possible to greatly extend the dynamic range.

Note that at the sudden low to high output transition the width generators must decide whether to generate a maximum or a minimum width pulse. A metastable state at this transition exists where the width generators cannot decide which pulse width to create. This state of indecision will occur when a Discr input lands in a very narrow time window centered at that transition. Measurements of the TCCAMU output did not reveal any metastability near this region, however, meaning that the width of the metastable time window must be $<<$ 1 LSB. The narrow width of this window results from the use of a positive feedback loop in the width generators. According to SPICE simulations, the width of the metastable window should be $<$ 10 ps.

The slope of the output curve in Fig. 9 is $\sim$ 1 LSB/107 ps. Because of the independence from capacitor and integrating current mismatches, the channel to channel (i.e., chip-to-chip) variations in the slope are $<$0.2%.

The integral nonlinearity (INL) can be defined as the difference between the measured output data and the best fit straight line through that data. The INL was calculated from the curve in Fig. 9. The typical INL for any given analog storage location is $<$ 200 ps, with a typical rms INL of 90 ps rms (see Fig. 10). The overall pattern of the INL curve is very similar from capacitor to capacitor, and even chip-to-chip. It is believed that this pattern noise stems from on-chip coupling effects between sensitive signal paths.

The random noise referred back to the input Discr consists of quantization noise and jitter. The quantization noise of the TCCAMU is calculated to be $\sim$ 31 ps rms. The jitter of our time to digital converter, due to thermal noise sources, was measured to be $\sim$ 25 ps rms. Combining both factors gives a total TCCAMU input referred random noise of 40 ps rms.

The maximum pedestal offset between any 2 analog storage locations in a given chip is $<$ 8 LSB's. The offsets, however, are not due to any mismatches in the capacitors themselves. Rather, the offsets result from a combination of mismatches in the input and output switches of the storage capacitors, and the large parasitic capacitance of the common bus connecting those switches. Efforts are currently underway to reduce these offsets to an expected value of $\sim$ 1 LSB.

IV. Conclusion

A time to charge converter with an analog memory unit (TCCAMU) and an on-chip A/D converter has been successfully designed, fabricated, and characterized. This IC measures the delay between the leading edge of an asynchronous Discr signal and a following edge of a 62.5 MHz system clock. The analog information from the time to charge conversion is pipelined in a two level analog CAM (content addressable memory). The data in Levels 1 and 2 of the CAM are filtered by externally generated Level 1 and Level 2 readout triggers. After a Level 2 accept, the analog information is digitized.

The TCCAMU was fabricated in HP's 1.2-μm n-well, double metal process. This 2.0 mm $\times$ 2.2 mm circuit was verified to be capable of measuring and digitizing its entire 16 ns input range with a $\sim$ 107 ps / LSB resolution. Despite its 4-μs conversion time, this chip achieves a double pulse resolution of 16–32 ns by using an analog input pipeline.

TABLE I
TCCAMU PERFORMANCE SUMMARY

INL (typical)	< 200 ps
rms INL	90 ps rms
DNL (typical)	< 35 ps
rms DNL	10 ps rms
LSB Width	107 ps
Input Range	16 ns
Output Range	150 LSB
Average Power Dissipation (including A/D conversion)	8.28 mW
Area of TCCAMU	2.0 mm x 2.2 mm
Technology	CMOS 1.2 μm nwell
Chip to chip gain mismatch	< 0.2 %
Max pedestal offsets between analog capacitors	< 8 LSBs
Input Referred Random Noise (quantization + jitter)	40 ps rms

The average power dissipation during A/D conversions is 8.28 mW/channel. A small chip to chip gain mismatch of < 0.2 % was accomplished with the use of a time to charge converter (TCC). Pedestal offsets between any two capacitors within a channel are < 8 LSB's; efforts are underway to reduce these offsets to ~ 1 LSB.

In summary, the TCCAMU's high performance and low power dissipation make it suitable for massively parallel data acquisition systems. By counting the reference clock, the dynamic range can be greatly extended for use in high energy physics experiments.

V. APPENDIX

A. Measurement of the DNL

Finding the DNL (differential nonlinearity) involves measuring the width of each output LSB. The DNL of code "Y" can be expressed as:

$$DNL_Y = \text{Code Width}_Y - 1\,\text{LSB}. \tag{1}$$

The width of an output LSB can be found with a code density test. By randomizing the TDC analog input a histogram of the output LSBs can be produced, and from this one can statistically determine the width of each code. The probability distribution for the random inputs is often chosen to be a constant over the entire input range. In our case, however, a Gaussian distribution was used for the code density test. This was easily accomplished by adding a finite amount of jitter to the Discr arrival time in the test setup.

The total jitter σ_J occurring at the TCCAMU output can be written as the sum of the jitters in the Discr, system clock, and the TCCAMU itself:

$$\sigma_J^2 = \sigma_{\text{Clock}}^2 + \sigma_{\text{Discr}}^2 + \sigma_{\text{TCCAMU}}^2 \tag{2}$$

The jitter that was added to the Discr was made to dominate the contributions from the Clock and the TCCAMU. In

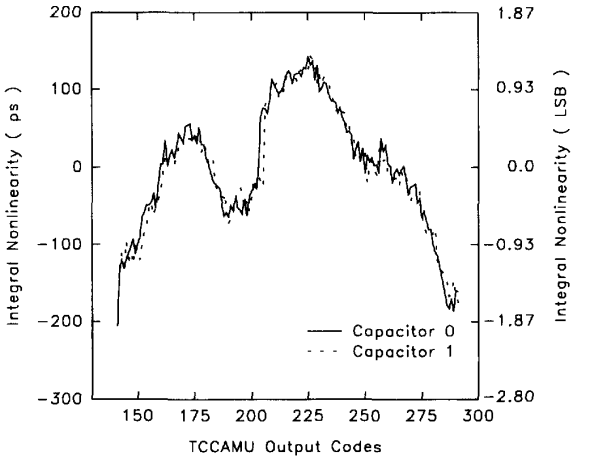


Fig. 10. Typical integral nonlinearity data for two different analog memory locations.

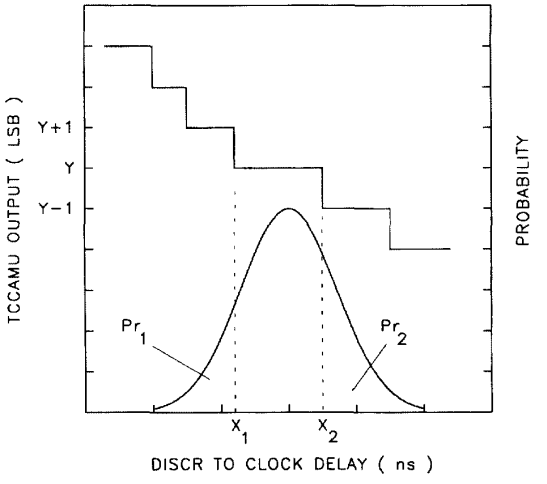


Fig. 11. The staircase curve is a close-up view of the analog Discr input delay versus digital output of the TCCAMU. The Gaussian curve represents the total output jitter referred back to the input Discr arrival time.

Fig. 11, the total output jitter from σ_J is shown when referred back to the input Discr. Note that the Gaussian covers a sufficient input range to produce the output LSB Y as well as several of its nearest neighbors ($Y-1, Y-2, \ldots$ and $Y+1, Y+2, \ldots$). For each particular output LSB whose width was being measured, 1000 input samples were generated. From this, we were able to calculate Pr_1 and Pr_2. Note that Pr_1 in (3a) is the measured probability in the tail of the Gaussian occupied by the LSB's $Y-1, Y-2, \ldots$ and so forth. Pr_2 is the measured probability in the tail corresponding to the LSB's $Y+1, Y+2, \ldots$ and so forth. We can express these probabilities as:

$$Pr_1 = \int_{-\infty}^{X_1} \frac{1}{\sqrt{2\pi\sigma_J^2}} \exp(-(z-\mu)^2/2\sigma_J^2)dz$$
$$= \frac{1}{2} erfc(\gamma_1/\sqrt{2}) \tag{3a}$$

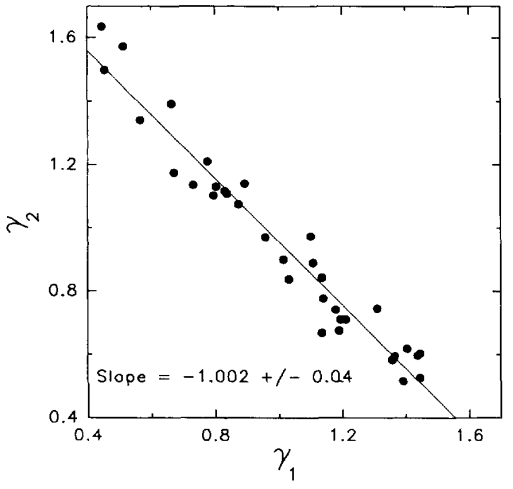


Fig. 12. Plot of γ_1 versus γ_2 to verify the shape of the total Gaussian jitter that is measured at the output of the TCCAMU.

$$Pr_2 = \int_{X_2}^{+\infty} \frac{1}{\sqrt{2\pi\sigma_J^2}} \exp(-(z-\mu)^2/2\sigma_J^2)dz = \frac{1}{2} erfc(\gamma_2/\sqrt{2}) \quad (3b)$$

where μ is the center of the Gaussian shown in Fig. 11, and X_2 - X_1 corresponds to the range of input Discr arrival times that produces the output code Y. The γ_1 and γ_2 are given by:

$$\gamma_1 = (\mu - X_1)/\sigma_J \quad (4a)$$

$$\gamma_2 = (X_2 - \mu)/\sigma_J. \quad (4b)$$

Using a lookup table for the erfc function, we get the numbers γ_1 and γ_2 which correspond to the measured Pr_1 and Pr_2. Combining (4a) and (4b) we get the measured width of code Y:

$$\text{Code Width}_Y = (X_2 - X_1)_Y = \sigma_J(\gamma_1 + \gamma_2)_Y. \quad (5)$$

Thus, by measuring Pr_1 and Pr_2 we can find γ_1 and γ_2, which in turn give us the width of a particular code. Note that these equations assume that the code Y being evaluated has the Gaussian center μ located between X_1 and X_2. By extending this theory it should be possible to measure several codes at a time.

Finally, the measured differential nonlinearity of code Y is given by:

$$\text{DNL}_Y = \sigma_J(\gamma_1 + \gamma_2)_Y - 1\,\text{LSB} \quad (6)$$

where σ_J is in units of LSB's.

B. Width and Shape of Output Gaussian

In order to make use of (6), we must know the value of σ_J. The value of σ_J can be written as :

$$\sigma_J = \#\,\text{TCCAMU Output Codes}/\sum_Y (\gamma_1 + \gamma_2)_Y \quad (7)$$

where the summation is over all possible output codes. Note here that the % error in determining σ_J is much smaller than the % error in the measurement of a single code width.

The other aspect when making DNL and INL measurements with a Gaussian input signal is to verify that the jitter due to σ_J has a true Gaussian shape (or nearly so). If we refer to (5) and take the derivative d/dγ_2 of both sides, we find that:

$$d\gamma_1/d\gamma_2 = -1. \quad (8)$$

(8) tells us that if the total output jitter σ_J is Gaussian, and if we vary the input Discr delay over a small range to get a number of (γ_1, γ_2) pairs for a given output code, then these points should all lie on a straight line with a slope of -1. Fig. 12 verifies that we have a Gaussian-shaped jitter to within the measurement error. There were 1000 output samples taken for each data point shown.

C. Measurement Uncertainty in DNL

In order to find the measurement uncertainty in the DNL, we must find the uncertainties in γ and Pr. Let:

N =	number of input samples generating the Gaussian,
Pr =	measured probability in tail of Gaussian,
σ_P =	Std dev of Pr from the actual probability,
σ_1 (or σ_2) =	Std dev of measured γ_1 (or γ_2),
σ_{12} =	Std dev of measured γ_1 + γ_2
σ_J =	total rms jitter at the TCCAMU output
σ_{DNL} =	measurement uncertainty in the DNL, and
σ_{Width} =	measurement uncertainty in a code width.

Using the binomial distribution to determine how many of the N inputs actually land in the tail of the Gaussian, we find that:

$$\sigma_P = \sqrt{\frac{Pr(1-Pr)}{N}}. \quad (9)$$

If we now take the derivative $d/d\gamma$ of both sides of (3) using the Leibnitz Rule, assuming that σ_P is sufficiently small (i.e., N large), then we can write:

$$\sigma_1 \approx \sqrt{2\pi}\sigma_P \exp(\frac{\gamma^2}{2}). \quad (10)$$

Finally, from (5) and (6) we see that :

$$\sigma_{\text{Width}} = \sigma_{DNL} = \sigma_J\sigma_{12} < 2\sigma_J\sigma_1. \quad (11)$$

For $N = 1000$ and $0.5 > Pr > 0.05$, we use (3), (9), and (10) to find that $\sigma_1 < 0.066$. In our measurements, we added a jitter to the Discr such that $\sigma_J \approx 0.6$ LSB. Using (11) we finally have :

$$\sigma_{\text{DNL}} < 0.079\,\text{LSB} = 8.5\,\text{ps} \quad (12)$$

Increasing the value of N will decrease the measurement uncertainties in both the DNL and the code widths.

REFERENCES

[1] H. H. Williams, "Design principles of detectors at colliding beams," *Annu. Rev. Nucl. Particle Sci.*, pp. 361–417, 1986.

[2] L. Callewaert *et al.*, "Front end and signal processing electronics for detectors at high luminosity colliders," *IEEE Trans. Nucl. Sci.*, vol. 36, pp. 446 - 457, Feb. 1989.

[3] Y. Arai, T. Matsumura, and K. Endo, "A CMOS four-channel x 1 K time memory LSI with 1-ns/b resolution," *IEEE J. Solid-State Circuits*, vol. 27, pp. 359–364, March 1992.

[4] T.-I. Otsuji, "A picosecond-accuracy, 700-MHz range, Si-bipolar time interval counter LSI," *IEEE J. Solid-State Circuits*, vol. 28, pp. 941–947, Sept. 1993.

[5] A. Stevens, R. Van Berg, J. Van der Spiegel, and H. H. Williams, "A time-to-voltage converter with analog memory for colliding beam detectors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1748–1752, Dec. 1989.

[6] A. Holscher, G. Stairs, and P. K. Sinervo, "Front end and dcc simulations for the SDC straw tube system," Workshop on Data Acquisition and Trigger System Simulations for High Energy Physics, SSCL-SR-1211, pp. 33–60, April 1992.

[7] A. J. McAuley and C. J. Cotton, "A self-testing reconfigurable CAM," *IEEE J. Solid-State Circuits*, vol. 26, pp. 257 - 261, March 1991.

Eric J. Gerds (S'88) was born in Mount Vernon, NY, on November 9, 1965. He received the B.S. and M.S. degrees from the Moore School of Electrical Engineering at the University of Pennsylvania, Philadelphia, in 1987 and 1991. He is currently working towards the Ph.D. degree at the Moore School.

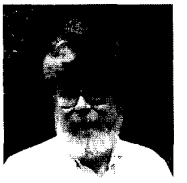
During the summer of 1990, he designed detector instrumentation for the Sudbury Neutrino Observatory (SNO) in Canada. Since that time, he has been working in conjunction with Penn's High Energy Physics group designing high resolution CMOS Time to Digital Converters (TDC's) for particle collider detectors. His research interests include mixed analog/digital IC design, low power detector instrumentation, and high performance CMOS TDC's.

Mr. Gerds is a member of Eta Kappa Nu.

Jan Van der Spiegel (S'73-M'79-SM'90) was born in Aalst, Belgium. He received the engineering degree in Electromechanical Engineering, and the Ph.D. degree in Electrical Engineering from the Katholieke University of Leuven, Belgium in 1974 and 1979, respectively. From 1980 to 1981, he was a postdoctoral fellow at the University of Pennsylvania, Philadelphia.

He became an assistant professor of Electrical Engineering at the University of Pennsylvania in 1981, and is currently an associate professor in Electrical Engineering. His research interests are in artificial neural networks, CCD sensors, microsensor technology and low-noise, low-power, and high-speed analog integrated circuits.

Dr. Van der Spiegel holds the Bicentennial Chair of the Class of 1940, is Director of the Center for Sensor Technologies and House Faculty Master of Ware College at the University of Pennsylvania. He is the editor for North and South America of Sensors and Actuators, and is on the editorial board of the International Journal of High Speed Electronics. He received the Presidential Young Investigator's Award, the R. Warren and the C. & M. Lindback Awards for distinguished teaching. He is a member of the International Neural Network Society, Phi Beta Delta and Tau Beta Pi.



Richard Van Berg (M'72) received the B.A. in physics from Haverford College in 1964 and the M.S. in physics from the University of Pennsylvania, Philadelphia, in 1966.

He has worked at the University of Pennsylvania on instrumentation for High Energy Physics research since 1964. While he has worked on particle detector design and fabrication, his primary interest has been in the detector-electronics interface. He was primary architect of and electronics group leader for the 20,000 element Brookhaven Experiment 734 (1978), the 1,000 photomultiplier tube Kamiokande II detector (1984), and the 140,000 channel SDC Straw Tracker (1989-93). He is presently leading the electronics group for the Sudbury Neutrino Observatory and has begun to work with groups at CERN interested in the 500,000 channel ATLAS Transistion Radiation Tracker at LHC.

Mr. Van Berg is a member of the American Physical Society.

Hugh H. Williams (M'89) received the Ph.D. in Physics from Stanford University, Stanford, CA, in 1972. He was a postdoctoral fellow at Brookhaven National Laboratory from 1972-1974.

He joined the University of Pennsylvania, Philadelphia, as Assistant Professor of Physics in 1974. He has been a Full Professor since 1982. His primary research interests are in the study of very high energy particle collisions with an emphasis on the search for new particles and new types of interactions. He recently participated in an experiment providing the first direct evidence for top quarks. Since 1987, he has also specialized in developing custom integrated circuits from high-speed, low-noise, low-power signal processing of signals for various sensors.

Ludwig Callewaert (S'84) was born in Kortrijk, Belgium, on March 16, 1960. He received the engineering degree in electronics from the Katholieke Universiteit Leuven, Heverlee, Belgium, in 1983.

Since September 1983, he has been employed at the Laboratory Elektronika, Systemen, Automatisatie, en Technologie (ESAT), Katholieke Universiteit Leuven, where he has been working as an assistant, only interrupted by his military service from November 1985 to September 1986. His interests are in the design of analog and digital integrated circuits and medical electronics.

W. Eyckmans photograph and biography not available at time of publication.

Willy Sansen (S'66-M'72-SM'86) received the M.S. degree in electrical engineering from the Katholieke Universiteit Leuven, in 1967 and the Ph.D. degree in electronics from the University of California, Berkeley, in 1972.

Since 1981, he has been a full Professor at ESAT Laboratory, Katholieke Universiteit Leuven. During the period 1984–1990 he was the Head of the Electrical Engineering Department. He was a Visiting Professor at Stanford University, Stanford, CA, in 1978, at the Federal Technical University Lausanne, Switzerland, in 1983, and at the University of Pennsylvania, Philadelphia, in 1985. He has been involved in design automation and in numerous analog integrated cicuit designs for telecom, consumer electronics, medical applications, and sensors. He has been supervisor of 25 Ph.D. dissertations in that field and has authored and coauthored four books and 300 papers in international journals and conference proceedings.