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A CMOS Monolithic Implementation of a Nonliniear Interconnection Module for a Corticonic Network

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Keywords
corticonic network, cortical patch, nonlinear interconnection

A CMOS Monolithic Implementation of a Nonlinear Interconnection Module for a Corticonic Network

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***Abstract*— A nonlinear interconnection module for a corticonic network is designed and fabricated in a 0.6 μm CMOS process. The module uses NMOS transistors in weak-inversion region for nonlinearity. A calibration scheme is developed to compensate for the process and temperature variation of the circuit. The designed module has an area of 0.35mm^2. It consumes 200mW of power, with 5V power supply. Simulation results show that the circuit is able to implement the target parametric coupling function accurately.**

I. Introduction

Macroscopic modelling can pave a way leading to the design of high-performance complex and intelligent systems. Extensive research suggests that cortical column (CC) is the basic functional unit in the cortex. A macroscopic modelling approach for a cortical patch has been proposed in [1]. Inside the network, a group of nonlinear dynamic elements are coupled through nonlinear connections, as shown in Fig. 1. The element is designed in such a way that its individual dynamics conforms to or are similiar to that of a CC.

As a further effort, a cortical patch similiar to Fig. 1 is implemented in silicon [2]. In an accompanying paper [3], the circuit design of integrated-circuit relaxation oscillator neuron (IRON) is presented. The IRONs are able to generate arbitrary one-dimensional map in high resolution.

In order to control and correlate the dyanmics of different IRONs, nonlinear parameterical coupling is used in the network [1]. In this paper, the CMOS design of the nonlinear interconnection module is presented. Hspice simulation results are included to show the characteristics of the designed module.

II. Parametrical Coupling

The processing element presented in [3] uses a bifurcation parameter μ to control the dynamic behavior. The parametrical coupling is a type of nonlinear interconnection that is used to control μ whose value depends on its own output and those of other IRONs. The bifurcation parameter for the i-th IRON is controlled by both external and internal influences according to

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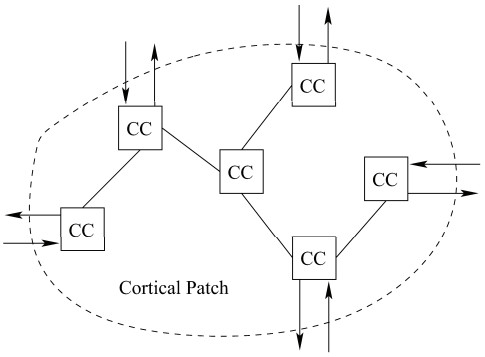

Fig. 1. Functional diagram of a cortical patch

$$\mu_i(t) = e^{-\alpha t} g(X_i^s, C_i^s) + \frac{1 - e^{-\alpha t}}{N_i} \sum_{j \subset \{N_i\}} g(X_j, C_{ij}) \quad (1)$$

Where $X_i^s \in [0,1]$ is the i-th IRON's external input, $X_j \in [0,1]$ is the output from the j-th IRON, C_i^s is the coupling parameter for i-th external input, and C_{ij} is the coupling parameter from j-th IRON to the i-th IRON.

The first term in Eqn. 1 represents the influence of the external input, while the second term is the average effect from IRONs inside the network. $e^{-\alpha t}$ is named the forgetting factor (FF), while $1 - e^{-\alpha t}$ is denoted as $\overline{\text{FF}}$. As the network adapts, FF exponentially decreases. As a result, the external influence gradually gives way to internal influence. The $g()$ function in Eqn. 1 is a nonlinear function, as defined in Eqn. 2, and is plotted in Fig. 2

$$g(X, C) = X^C, \qquad X \in [0,1] \quad (2)$$

$\{N_i\}$ in Eqn. 1 is the group of IRONs connected to the i-th IRON. In our corticonic network, local coupling (LC), consisting of self and nearest neighbors, is used, which sets $N_i = 3$. The local interconnection scheme of the i-th IRON in the network is shown in Fig. 3. Hence, the designed corticonic network consists of dozens of processing elements (PE), each of which includes an IRON and an LC module.

III. Circuit Description

The parametrical LC in Eqn. 1 is designed in a 0.6μm CMOS process. The supply voltage is 5V. The block diagram

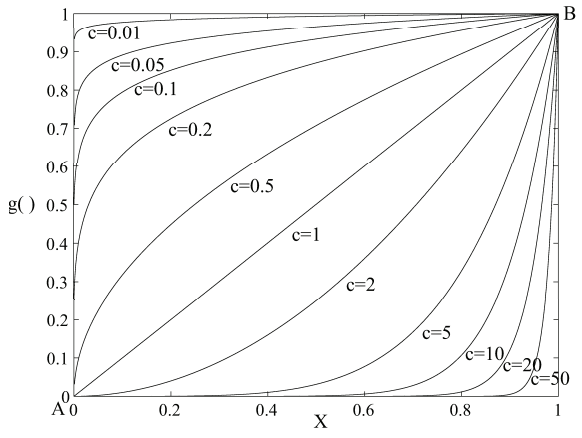

Fig. 2. The function of $g(X, C) = X^C$

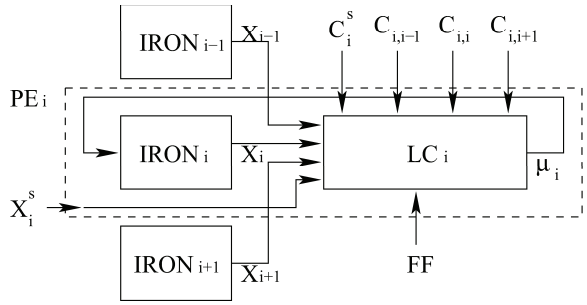

Fig. 3. Local interconnection for i-th IRON

of the implemented LC is shown in Fig. 4. All the operations are carried out in the voltage domain. X's are the firing phases from the IRONs, which lie in the voltage range of [2.8V, 3.2V]. In normal operation, X's changes their value with a frequency of 1MHz, as stated in [3]. C's are coupling parameters with voltage values in the range of [3.0V, 3.4V]. FF are the same for all the PE's in the network. In our simulations, the decay time constant α is set to be 10μs. Therefore, FF and $\overline{\text{FF}}$ can be controlled from off-chip through two normal analog pads.

The design of a reliable nonlinear function $g()$ is central in the LC circuit. The nonlinear $g()$ function in Eqn. 2 can be

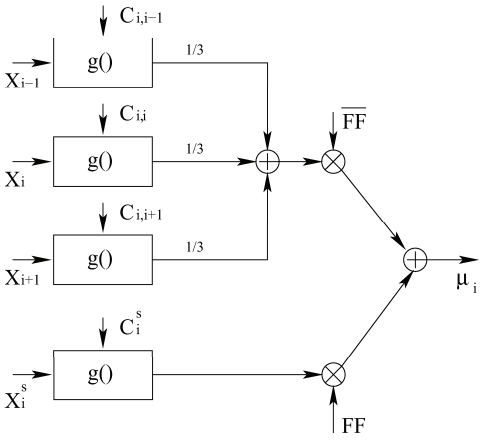

Fig. 4. The block diagram of local coupling module

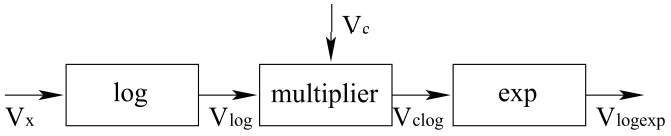

Fig. 5. The cascode of $g()$ function

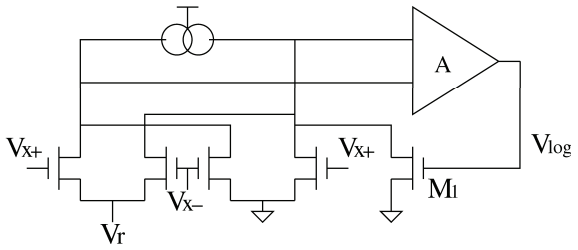

Fig. 6. The logarithmic module

discomposed into a series of functions, as shown in Eqn. 3. Hence, it can be implemented as a cascade of stages, consisting of a logarithmic module, a multiplier and an exponential module, as shown in Fig. 5.

$$g(X, C) = X^C = exp(C \times log(X)) \tag{3}$$

A. Logarithmic Module

The circuit of the logarithmic module is shown in Fig. 6. It includes a Gilbert cell, and an NMOS M1, which is designed with a large W/L to be biased in the weak inversion region. Without considering the OPAMP offset, using the MOS BSIM3 model in [4], the equation for the Gilbert cell and the NMOS transistor is in Eqn. 4. One can write that

$$k_{log} V_x V_r = I_{s01} exp(\frac{V_{log} - V_t - V_{off}}{n\nu_t}) \tag{4}$$

Where k_{log} is a coefficient related to transistors in the Gilbert cell, I_{s01} and V_{off} are coefficients related to M1, V_t is the threshold voltage of M1, ν_t is the thermal voltage, n is the subthreshold slope parameter.

Hence, the output signal of the logarithmic module in Fig. 6 can be derived as shown in Eqn. 5.

$$V_{log} = V_t + V_{off} + n\nu_t log(\frac{k_{log} V_x V_r}{I_{s01}}) \tag{5}$$

B. Multiplier

The voltage multiplier in the $g()$ module is shown in Fig. 7. It includes two cross-connected Gilbert cells. Again, igoring the OPAMP offset, the circuit equation for the voltage multiplier in Fig. 7 is shown in Eqn. 6.

$$k_{gc1}(V_{log} - V_T)V_c = k_{gc2}(V_{clog} - V_T)V_{cr} \tag{6}$$

Where k_{gc1} and k_{gc2} are the transistor related coefficients for the two Gilbert cells. If transistors in the two cells match, the output of the voltage multiplier would be in Eqn. 7.

$$V_{clog} = V_T + \frac{V_c}{V_{cr}}(V_{log} - V_T) \tag{7}$$

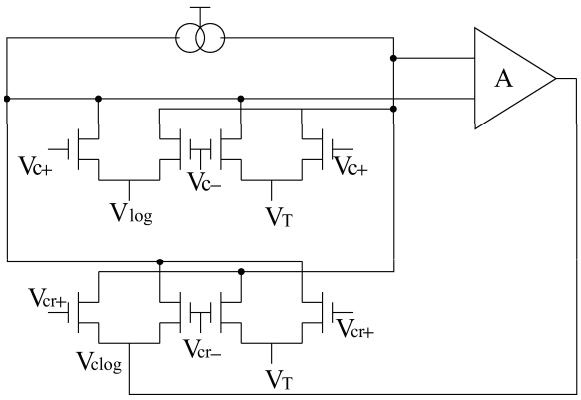

Fig. 7. The voltage multiplier

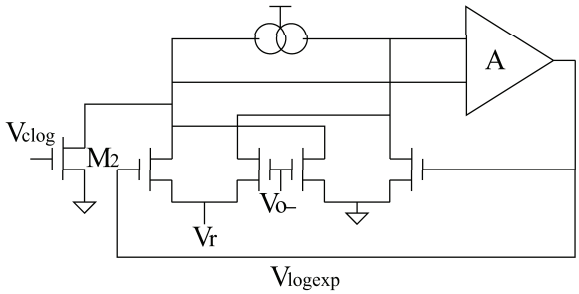

Fig. 8. The exponential module

C. Exponential Module

The exponential module is shown in Fig. 8. It includes an NMOS M2 in weak inversion, and a Gilbert cell in the feedback loop. Like M1 in Fig. 6, W/L of M2 is designed to be large enough to bias M2 in the weak inversion region. Without considering the OPAMP offset, the circuit equation is given by Eqn. 8.

$$I_{s02}exp(\frac{V_{clog}-V_t-V_{off}}{n\nu_t}) = k_{exp}(V_{logexp}-V_{o-})V_r \quad (8)$$

Where I_{s02} , V_{off}, V_t, ν_t and n are of the same annotation as in Eqn. 4, k_{exp} is the transistor related coefficient of the Gilbert cell. Hence, the module output can be written as in Eqn. 9.

$$V_{logexp} = V_{o-} + \frac{I_{s02}}{k_{exp}V_r}exp(\frac{V_{clog}-V_t-V_{off}}{n\nu_t}) \quad (9)$$

As a result, the output signal of Fig. 5 can be obtained from Eqn. 5, Eqn. 7 and Eqn. 9. If extra layout matching techniques and biasing considerations are used to match the two weak inverted NMOS M1 and M2, the transistor related coefficients in Eqn. 5 and Eqn. 9 can be the same. The two Gilbert cells in Fig. 6 and Fig. 8 can also be designed to match, so that

$$k_{log} = k_{exp} = k \quad (10)$$

If the bias V_T in the multiplier is set to achieve Eqn. 11, the ideal output is given by Eqn. 12.

$$V_T = V_t + V_{off} \quad (11)$$

$$\frac{V_{logexp}-V_{o-}}{\frac{I_{s0}}{kV_r}} = (\frac{V_x}{\frac{I_{s0}}{kV_r}})^{\frac{V_c}{V_{cr}}} \quad (12)$$

If the biasing voltage V_r can be set as in Eqn. 13, the output voltage can be expressed by Eqn. 14.

$$V_r = \frac{I_{s0}}{k} \quad (13)$$

$$V_{logexp} - V_{o-} = (V_x)^{\frac{V_c}{V_{cr}}} \quad (14)$$

Therefore, the value of C in Eqn. 3 is set by $\frac{V_c}{V_{cr}}$.

D. Generalized Threshold Calibration

The ideal $g()$ function in Fig. 2 has two converging points, A and B. Point A represents 0 input. For the circuits in Fig. 6-8, the convergence at point A can be fulfilled relatively easy. However, the convergence at point B is not easy to obtain, because, in reality, it is difficult to set biases to fulfill Eqn. 11 and Eqn. 13. The process parameters on the right side of the equations are not known accurately. Instead, we use a calibration process to resolve this biasing problem.

Let us assume that the differential input signal V_x varies between 0 and V_{inmax}. The maximum input can be used to calibrate for point B. The input of the circuit is set to V_{inmax} first. Then, the generalized threshold voltage V_T is adjusted to align the output signal V_{logexp} to the converging point B, which means V_{logexp} would not change with different C values, i.e. $\frac{V_c}{V_{cr}}$. Thus, using Eqn. 7, we can write V_T as follows,

$$V_T = V_t + V_{off} + n\nu_t log(\frac{kV_rV_{inmax}}{I_{s0}}) \quad (15)$$

With Eqn. 5, Eqn. 7, Eqn. 9 and Eqn. 15, the output signal from the $g()$ module can be shown to be in Eqn. 16.

$$\frac{V_{logexp}-V_{o-}}{V_{inmax}} = (\frac{V_x}{V_{inmax}})^{\frac{V_c}{V_{cr}}} \quad (16)$$

E. Offset Effect

The derivation so far are based on ideal OPAMPs. The OPAMP offset generates current offset between the two branches of PMOS current mirrors, in Fig. 6-8. The current offsets are the most significant systematic error for the module.

If we assume the existence of current offsets ΔI_1, ΔI_2 and ΔI_3 for the three operation modules, using equations similiar to Eqn. 4, Eqn. 6 and Eqn. 8, the output voltage can be written as Eqn. 17, under the condition of Eqn. 11.

$$\frac{V_{logexp}-V_{o-}+\frac{\Delta I_3}{kV_r}}{\frac{I_{so}}{kV_r}} = e^{-\frac{\Delta I_2}{k_{gc}V_{cr}n\nu_t}}(\frac{V_x+\frac{\Delta I_1}{kV_r}}{\frac{I_{so}}{kV_r}})^{\frac{V_c}{V_{cr}}} \quad (17)$$

Compared to Eqn. 12, the offset effect is plotted in Fig. 9. The shaded area is the region for ideal $g()$ function. ΔI_1 moves the box along the X axis, ΔI_3 moves the box along the g axis, while ΔI_2 streches the box in $g()$ direction. Because the weak-inverted NMOSs M1-2 have large W/L size, k in Eqn. 17 is large. The error $\frac{\Delta I_1}{kV_r}$ and $\frac{\Delta I_3}{kV_r}$ can be designed to be less than 1mV. In our application, their effects can be neglected. The effect of ΔI_2 can be compensated by the following FF weighing circuit.

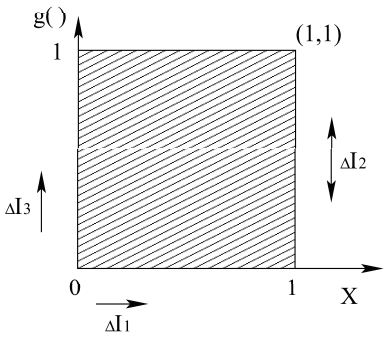

Fig. 9. The current offset effect

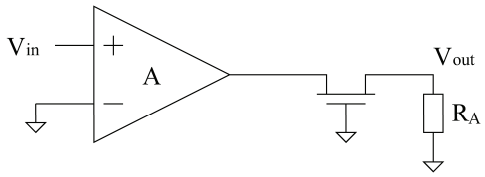

Fig. 10. Loop stability analysis

F. Stability

Enhancing the OPAMP gain can effectively reduce the offset level. However, the loops in Fig. 6-8 are susceptible to instability. The feedback loop of the multiplier in Fig. 7 is opened in Fig. 10. Without extra care, the phase margin in the loop can fall short. The feedback loops of Fig. 6 and Fig. 8 are similiar, but with a common source stage. In order to improve the loop phase margin, the OPAMP can be designed to have low gain, or the resistance at the common drain nodes can be lowered. Unfortunately, both methods tend to increase the current offset level in the loop. In our design, we used both methods to guarantee the loop stability under different Spice corner models and temperature variations.

G. FF Weighing Circuit

The FF factors are added by the circuit in Fig. 11. It includes five Gilbert cells for current operation. If all the Gilbert cells match, the output voltage can be expressed as in Eqn. 18.

$$V_u = \frac{V_{fb}}{V_{fr}} V_{lx4} + \frac{V_{f/3}}{V_{fr}} \sum_{i=1}^{3} V_{lxi} \tag{18}$$

Therefore, $\overline{\text{FF}}$ is set by $\frac{V_{fb}}{V_{fr}}$ and FF is set by $\frac{V_f}{V_{fr}}$. Similiar offset analysis shows that the offset in Fig. 11 can be compensated by adjusting V_{u-}.

IV. Simulation Results

The interconnection module is designed and fabricated in a 0.6μm CMOS process. The active die area is $970\mu m \times 360\mu m$. The power consumption is 200 mW for a 5V supply. The chip is being tested, and results will be available at the time of conference.

The design is fully simulated by Hspice, for different corner models including temperature variations. Loop stability is guaranteed over the full range. The Hspice simulation results

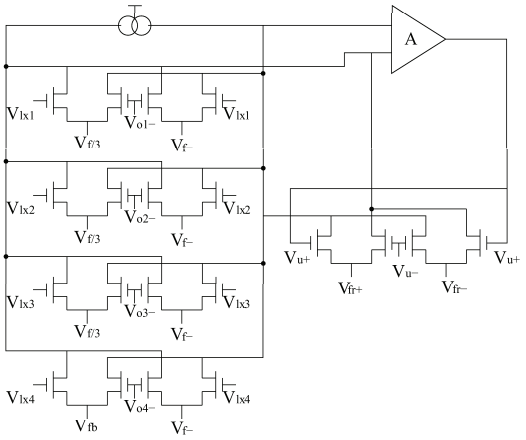

Fig. 11. FF weighing circuit

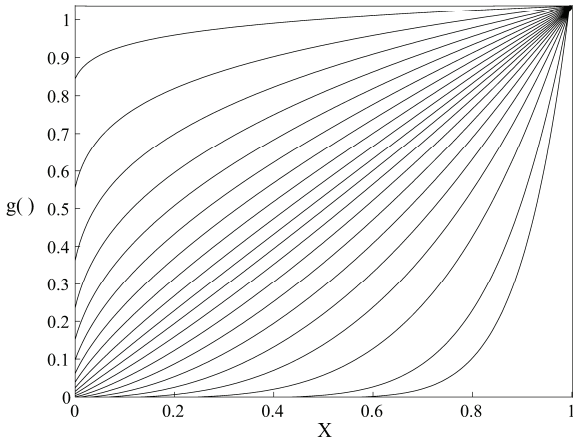

Fig. 12. Simulation results of $g()$ module, with typical models at 25 C°

of the $g()$ module after generalized threshold calibration, with typical Spice models and room temperature, is shown in Fig. 12. The over-streching due to the current offset ΔI_2 is less than 5%. It can be compensated by the value of $\frac{V_{fb}}{V_{fr}}$ and $\frac{V_f}{V_{fr}}$ in the FF weighing circuit.

V. Conclusion

The nonlinear parametrical coupling of a corticonic network is presented. The interconnection module is used to control and coordinate the dynamics of bifurcating neurons in the network.

The circuit is implemented and fabricated in a 0.6μm CMOS process. The circuit uses NMOS in weak-inversion for nonlinear operation. The designed circuit employs a calibration scheme to compensate process variation and temperature variation for the circuit, especially for the weak-inverted NMOSs.

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