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Cort-X II: Low Power Element Design of a Large-Scale Spatio-Temporaral Pattern Clustering System

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Abstract
Complex spatio-temporal patterns can be clustered using a network of parametrically coupled logistic maps. This paper describes the processing element design of such a Cort-X system. Each Cort-X element consists of a non-linear coupling (LC) and a non-linear dynamic element (IRON). The circuits are designed for low-power operation and to be robust against process variations. This has been accomplished by using openloop circuits, and a self-calibration technique that compensate for process variations. The circuits were implemented in a 0.25 um, 2.5V CMOS process and consumes a total of 12mW of power at 1MHz which is about a factor of 20 less power than previous realizations. This opens the possibility for building a large-scale Cort-X system on a chip for the recognition of complex spatio-temporal patterns.

Keywords
neural network, spatio-temporal pattern, logistic map, recognition, non-linear elements

Cort-X II: low power element design of a large-scale spatio-temporal pattern clustering system

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***Abstract*— Complex spatio-temporal patterns can be clustered using a network of parametrically coupled logistic maps. This paper describes the processing element design of such a Cort-X system. Each Cort-X element consists of a non-linear coupling (LC) and a non-linear dynamic element (IRON). The circuits are designed for low-power operation and to be robust against process variations. This has been accomplished by using open-loop circuits, and a self-calibration technique that compensate for process variations. The circuits were implemented in a 0.25 um, 2.5V CMOS process and consumes a total of 12mW of power at 1MHz which is about a factor of 20 less power than previous realizations. This opens the possibility for building a large-scale Cort-X system on a chip for the recognition of complex spatio-temporal patterns.**

I. INTRODUCTION

Neurophysiologic study suggests that the biological cortex is organized hierarchically at the macroscopic level and modularly at the microscopic level [1]. At the microscopic level, a cortical patch is composed of a modular network of cortical columns. It has been shown that a network of parametrically coupled logistic maps (PCLMN) can model the biological structure of the cortical patch [2]. Through system-level simulations, the PCLMN shows superior capability for clustering spatio-temporal patterns (STP). The PCLMN also has advantages of network capacity and hardware implementation, which paves the way to a large-scale intelligent system for STP recognition. The system can be useful for applications such as epileptic seizure anticipation, and automated target recognition (ATR).

A small PCLMN with five processing elements (PEs) is given in Fig. 1. The PEs are coupled through nonlinear interconnections. Each PE in the network includes an interconnection module and a 1-D parametrically coupled/driven logistic map. The 1-D logistic map can be generated by an integrated-circuit relaxation oscillator neuron (IRON) [3].

The PCLMN has been previously designed in CMOS circuits in a 0.6um 5V CMOS process [5] and [6], which is named Cort-X I [4]. Although Cort-X I was able to achieve good system-level results, the power consumption is high. This was in part due to the use of feedback to implement the nonlinear functions.

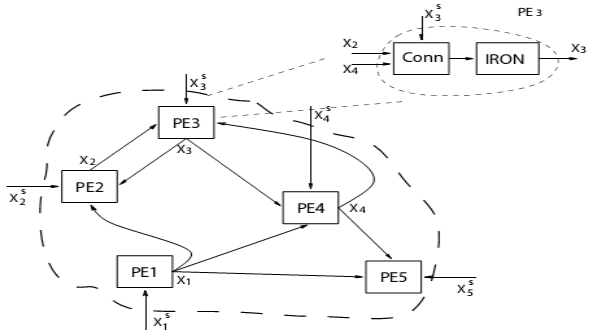

Figure 1. A 5-element parametrically coupled logistic map network

For large-scale integration of a Cort-X system, a low-power design is needed. Open-loop circuits and new structures are used to reduce power consumption. To compensate for the process variations for which the open-loop circuits are more sensitive, a self-calibration technique is developed. Cort-X II was fabricated in a 0.25um 2.5V CMOS process. In this paper, the CMOS design and measurements of the new Cort-X II element is presented.

II. THE CORT-X ELEMENT

Inside a PE, as shown in Fig. 2, the Local Coupling (LC) module implements the nonlinear interconnection and controls the dynamics of the nonlinear element IRON, by generating the bifurcation parameter u.

A. IRON

As presented in [5], the IRON model is similar to an integrate-and-fire neuron. As illustrated in Fig. 3, the dynamics of an IRON is limited by a threshold voltage (V_t) and a rest potential (V_r). The membrane potential (V_m) builds up at a constant rate. When V_m reaches V_t, the IRON fires,

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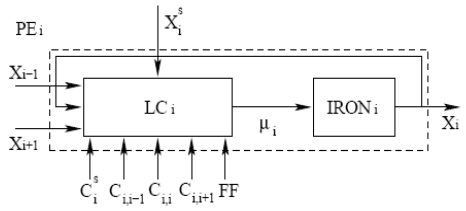

Figure 2. The structure of element PE_i, with local interconnection for i-th IRON.

and V_m descends to V_r within a refractory period (T_r). With a periodic rest potential, the phase of the pulse sequence $\{t_i\}$ fired by the IRON conforms to a 1-D map. It can be verified [5] that the IRON can generate the 1-D logistic map with the driving waveform in Eqn. 1.

$$V_r(t) = V_a \frac{t}{T} - 4\mu \frac{t}{T}\left(1 - \frac{t}{T}\right)V_a + V_b, \mu \in [0,1] \qquad (1)$$

B. Parametrical Coupling

As presented in [6], the parametrical coupling of the i-th PE is nonlinearly modulated by both external and internal influences according to the expression,

$$\mu_i(t) = e^{-\alpha t} g(X_i^s, C_i^s) + \frac{1 - e^{-\alpha t}}{N_i} \sum_{j \in \{N_i\}} g(X_j, C_{ij}), \qquad (2)$$

where X_i^s is the external stimulus for the i-th IRON, X_j is the output from the j-th IRON, C_i^s is the coupling parameter for the external stimulus of the i-th IRON, and C_{ij} is the coupling parameter from the j-th IRON to the i-th IRON.

The first term in Eqn. 2 represents the influence of the external input, while the second term is the average effect from IRONs inside the network. $e^{-\alpha t}$ represents a forgetting factor (FF), while $1-e^{-\alpha t}$ is the complement. As the network adapts, FF exponentially decreases. As a result, the external influence gradually gives way to the internal influence. During this transition, the network accepts the external STP and, ultimately, adapts itself to an internal attractor. The nonlinear g() function is in Eqn. 3.

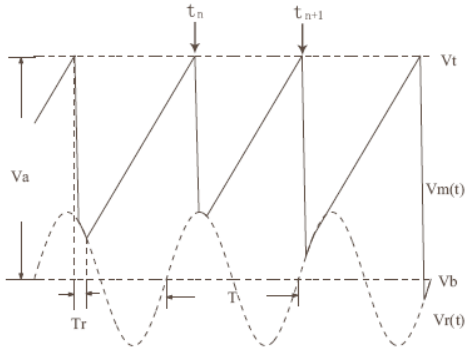

Figure 3. The dynamics of a sine-circle IRON with sinusoidal driving waveform

$$g(X, C) = X^C, \quad X \in [0,1] \qquad (3)$$

III. CORT-X II CIRCUIT DESCRIPTION

Cort-X II is primarily designed to reduce the power consumption of Cort-X I, which is described in [5] and [6].

A. IRON Circuit

The IRON circuit of Cort-X I is a spike-based design [5], shown in Fig. 4. When V_m charges beyond V_t, the circuit generates a narrow pulse, which switches the membrane capacitor C_r to the rest potential generation circuit, so that V_m is discharged to V_r. After the pulse, C_r is switched back to the reference current to start a new charging cycle. Hence, the discharging process of C_r is limited to the width of the narrow pulse, which is designed to be 20ns. This narrow pulse requires a high speed OPAMP in order to discharge the capacitor fast enough. As a result about half of the power consumption of the IRON is due to the amplifier [5].

A new designed two-phase IRON, shown in Fig. 5, avoids narrow pulses. In this IRON, two branches operate alternatively. The phase detector generates charging phases S1 and S2 based on the decisions from the two comparators. During S1 phase, branch 1 is charging, and branch 2 is discharging. During S2 phase, the branches switch their roles. The advantage of the two-phase scheme is that the discharging phase for both branches is considerably longer than the 20ns pulse in Cort-X I. Fig. 6 is an illustration of this. The transitions of S1 and S2 are the moments that the IRON is supposed to fire a pulse. For the current two-phase scheme, the length of S1 and S2 phases are indeed the distance between two pulses, which is about 1us in normal operation. Therefore, the driving requirement on the rest potential generation circuit is considerably relaxed, which allowed us to eliminate the power-hungry amplifier of the previous version.

Another major factor underlying power consumption in the IRON in Cort-X I is the closed-loop S/H deck [5], which accounts for about 25% of the power consumed by the IRON. Since the resolution requirement of the IRON is 10bits, in the current design, open-loop sampling is used.

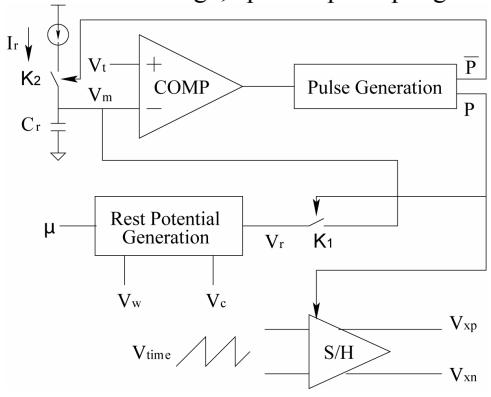

Figure 4. The block diagram of the IRON circuit in Cort-X I

As a result, the power of the newly designed IRON is reduced to 2mW from the original 40mW level.

B. LC Circuit

The local coupling (LC) circuit in Cort-X I [6] consists mainly of feedback circuits, which requires OPAMPs. To reduce the power consumption, the nonlinear g() function in Eqn. 3 is designed with only feedforward circuits, while the overall function in Eqn. 2 is implemented by current mode circuits.

The newly designed g() function is shown in Fig. 7. It is composed of a logarithmic circuit, a voltage multiplier and an exponential circuit similar to the one in Cort-X I. Using the BSIM3 model as in [6], the transfer function of the circuit, Eqn. 4, can be obtained, assuming good matching between M3 and M11, which are weakly inverted.

$$\frac{I_{\log\exp}}{I_{s0}} = e^{\frac{\Delta V}{n v_t}} \left(\frac{2}{I_{s0}\left(R_1 + \sqrt{\frac{1}{k_1 I_1}}\right)} V_x \right)^{\sqrt{2k_5 k_9} R_2 V_c}, \tag{4}$$

Here I_{s0} is the leakage current of M3 and M11; ν_t is the thermal voltage; n is the swing factor; ΔV is the voltage difference between the biasing voltage V_{tdr} and the threshold voltage V_T of M3 and M11.

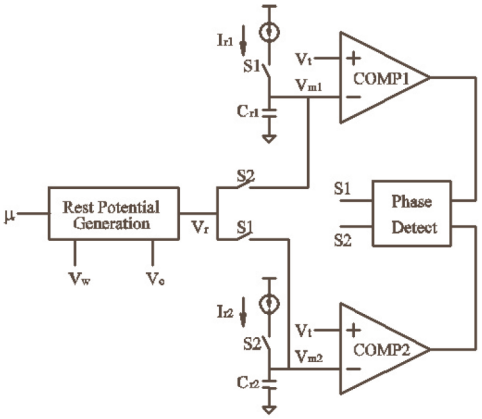

Figure 5. The two-phase IRON in Cort-X II

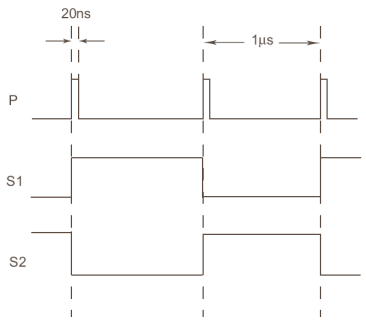

Figure 6. The length of S1 and S2 phases are considerably longer than the 20ns pulse width

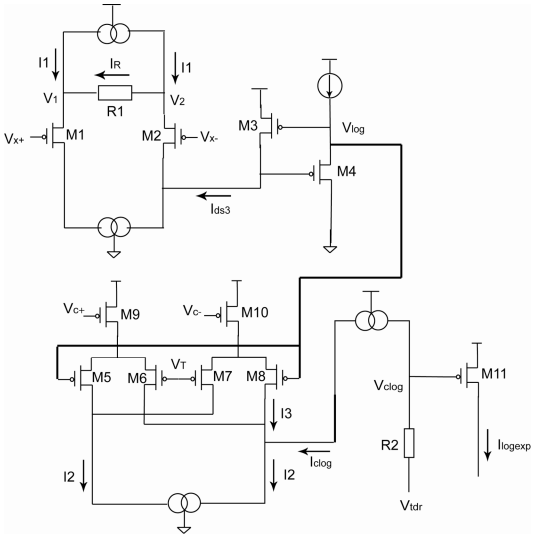

Figure 7. The circuit for g() function in Cort-X II

The parametrical power function in Eqn. 4 is process dependent. In order to remove this dependency, a self-calibration technique is implemented in the g() function circuit in Fig. 7. The calibration procedure operates in two phases. During the calibration phase, the maximum input V_{xmax} is applied to the circuit. The output V_{log} from the logarithmic module is stored. During the normal operation phase, the stored value of V_{log} serves as the V_T for the conversion. One can derive the transfer function shown in Eqn. 5 from this calibration scheme. Because the process dependent I_{s0} can be tuned out by adjusting $V_{tdr,}$ the process variation can be effectively removed by this self-calibration procedure.

$$I_{\log\exp} = \left(I_{s0} e^{\frac{\Delta V}{n v_t}} \right) \left(\frac{V_x}{V_{x\max}} \right)^{\sqrt{2k_5 k_9} R_2 V_c} \tag{5}$$

Since the output of the g() function circuit is a current, current mode processing becomes a more power-efficient method for the overall LC module, shown in Fig. 8.

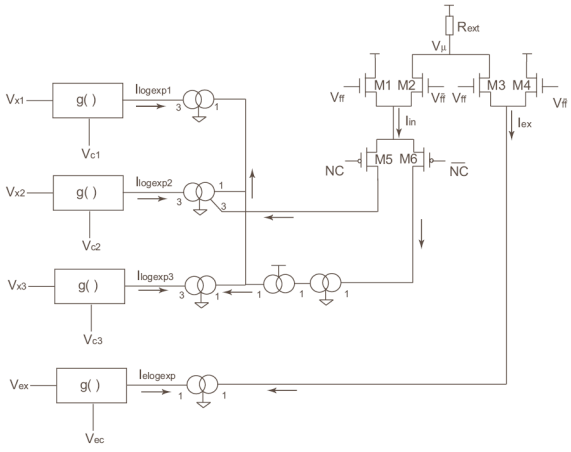

Figure 8. The current mode LC module

IV. EXPERIMENTAL RESULTS

The die photo of the Cort-X II chip is shown in Fig. 9. The active die area of the chip is 3mm×2.3mm, which includes 16 LCs and 16 IRONs. Each LC circuit occupies 0.4mm×0.46mm and consumes 10mW. Each IRON has a dimension of 0.17mm×0.22mm and consumes 2mW.

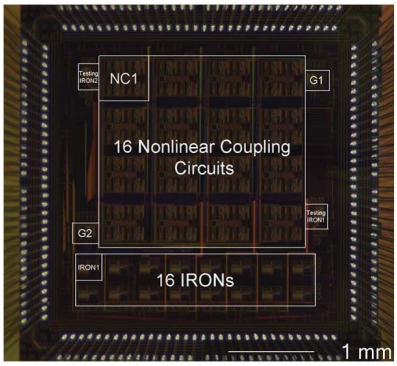

Figure 9. The die photo of the Cort-X II chip

A 6-layer testing board has been designed to characterize the chip. The transfer function of the nonlinear g() function is measured, and plotted in Fig. 10. The measurements show that the nonlinear coupling circuit is able to accurately implement the function g().

The IRON has been tested for its dynamic performance at 1MHz. Fig. 11 shows the bifurcation diagram measured for the logistic map. Although phase noise is present in the diagram, bifurcations between the different characteristic types of dynamics are evident. We expect that a significant amount of noise is due to the test board. We are now developing a low-noise testing board. This improved setup will reduce the phase noise of the IRON significantly.

V. CONCLUSIONS

Spatio-temporal patterns can be classified using parametrically coupled logistic maps. This paper describes a new Cort-X element needed to realize such a system on a chip. It consists of two components: the non-linear local coupling element (LC) and the dynamic element (IRON). By using open-loop circuits together with a self-calibration technique, we were able to compensate for process variations and reduce the power consumption by as much as 20 times as compared to the previous version of Cort-X.

A Cort-X II chip is fabricated in a 0.25um 2.5V CMOS process. Each element consumes 12mW power. Test results show that the nonlinear coupling circuits implement good nonlinear transfer function with fast settling. These elements

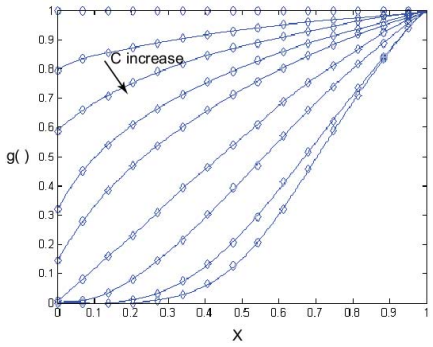

Figure 10. The measured static nonlinear function g(). The diamonds are the mearsured points. The curves are the polynomially fits from the mearsured points.

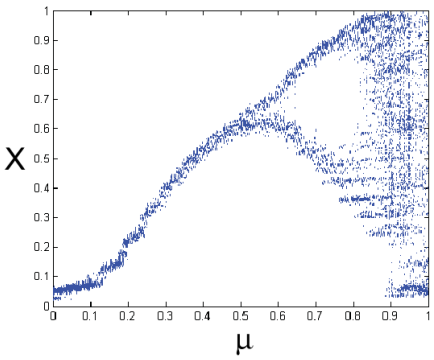

Figure 11. The measured bifurcation diagram from a logistic IRON

form the basis for the realization of a large-scale system-on-chip for classification of complex spatio-temporal patterns.

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