May 2006

A CMOS Monolithic Implementation of a Nonlinear Element for Arbitrary 1-D Map Generation

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Abstract
In a macroscopic approach, a single-chip cortical patch is designed based on a the model of a bifurcating neuron. In this paper, the monolithic design of the bifurcating neuron is presented. The dynamic element is able to generate an arbitrary one-dimensional map with 12-bit resolution. The CMOS design employs a calibration scheme to maintain robustness against process variations. The element is fabrication in a 0.6um CMOS process, and it driven under signals with 1MHz frequency. It covers a die of 0.2 square mm, and consumes 40mW power, with a 5V supply.

Keywords
cortical patch, bifurcating neuron, nonlinear element, one-dimensional logistic map

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***Abstract*— In a macroscopic approach, a single-chip cortical patch is designed based on the model of a bifurcating neuron. In this paper, the monolithic design of the bifurcating neuron is presented. The dynamic element is able to generate an arbitrary one-dimensional map with 12-bit resolution. The CMOS design employs a calibration scheme to maintain robustness against process variations. The element is fabricated in a 0.6μm CMOS process, and is driven under signals with 1MHz frequency. It covers a die has an area of 0.2mm^2, and consumes 40mW power, with a 5V supply.**

I. Introduction

Artificial neural models have traditionally been developed to model the behavior of biological neural nets consisting of individual interacting neurons. These microscopic approaches have made noteworthy contributions in fields, such as vision, auditory systems, associative memory and pattern recognition. However, there is evidence that the main processing unit for higher-level processing in the brain is not the individual neuron but a population of interacting neurons forming a cortical column (CC), and that a CC has emergent properties that can be modeled by a one-dimensional nonlinear map. Based on this hypothesis, a mathematical theory of a network for a cortical patch has been proposed in [1]. Inside the network, a group of nonlinear dynamic elements, or bifurcating neurons (BN), interact through nonlinear connections, as depicted in Fig. 1. The element is designed in such a way that its individual dynamics conforms to or is similiar to that of a CC.

In [1], elements with logistic map are suggested for the network. While in [2], elements with sine circle map are used to find different properties from the network. A more general model is proposed in [4], where the integrated-circuit relaxation oscillator neuron (IRON) is derived to generate arbitrary one-dimensional maps.

As further effort to implement the cortical patch in silicon[3], the IRON is designed and fabricated with the corticonic network in a 0.6μm CMOS process. In this paper, the CMOS monolithic implementation of IRON is presented. The design is suitable for a monolithic corticonic network with reasonable large size. Through multi-chip scaling, a large corticonic network with complex dynamic properties can be easily obtained.

This work was supported by the Office of Naval Research under Grant N00014-94-1-0932, by the Army Research Office under MURI Grant Prime DAAD 19-01-1-0603 via Georgia Institute of Technology Subcontract E-18-677-64 and by the Army Research Office under DURIP Grant W911NF-04-1-0177.

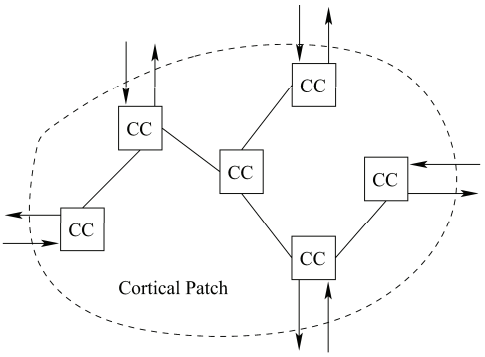

Fig. 1. Functional diagram of a cortical patch

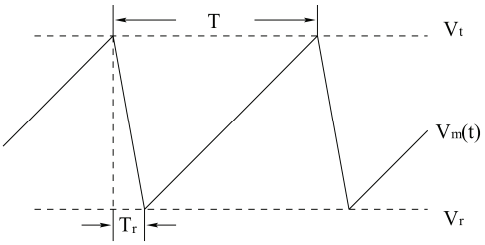

Fig. 2. The dynamics of integrate and fire neuron model

II. IRON Fundamental

The IRON model originates from the integrate-and-fire neuron model. In an integrate-and-fire neuron, there exists a threshold voltage (V_t) and a rest potential (V_r), as shown in Fig. 2. Without leakage, the membrane potential (V_m), which is named after its biological analogy, builds up at a constant rate. Until V_m reaches over V_t, the neuron fires, and V_m descends to V_r within a refractory period (T_r).

When the rest potential is modulated by some periodic waveform, the phase of the fired pulse conforms to a bifurcation diagram. A sine circle map can be generated by the modulation of a sinusoidal waveform, as in Eqn. 1. The dynamics of the IRON for sine circle map is shown in Fig. 3.

$$V_r(t) = \mu V_a sin(2\pi\frac{t}{T}) + V_b, \qquad \mu \in [0,1] \tag{1}$$

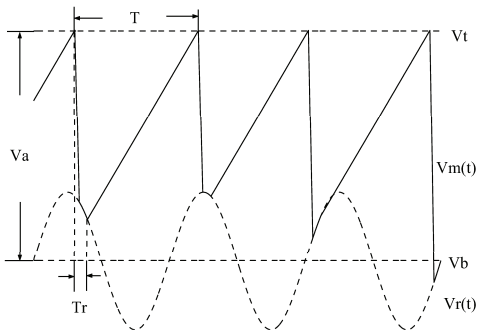

Fig. 3. The dynamics of IRON driven by sinusiodal waveform

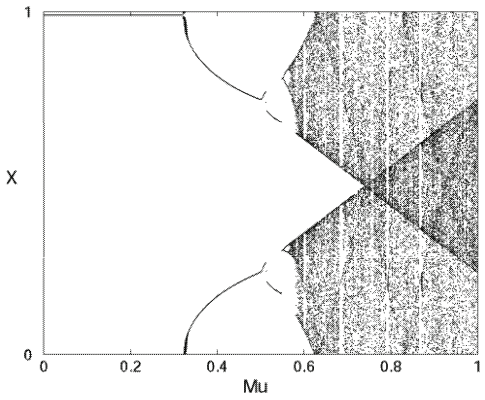

Fig. 4. Bifurcation of the ideal sine-circle map

Where V_a is the voltage difference between threshold V_t and the DC bias V_b of the sinusiodal waveform.

By changing the modulating waveform of the rest potential, different maps can be generated. Another important map for corticonic networks is the logistic map. The logistic map can be generated under modulation by a quadratic waveform, as shown in Eqn. 2.

$$V_r(t) = V_a\frac{t}{T} - 4\mu\frac{t}{T}(1-\frac{t}{T})V_a + V_b,\ \mu \in [0,1], t \in [0,T] \quad (2)$$

By numerical simulation, the bifurcation diagram of the IRON can be obtained. The sine circle map is plotted in Fig. 4, where X is the state variable and μ is the bifurcation parameter.

III. Circuit Description

The IRON is designed in a 0.6μm CMOS process. The block diagram of the IRON circuit is shown in Fig. 5. The membrane potential is obtained by charging a capacitor with a constant current source. Once the membrane potential reaches above the threshold voltage, the output of the comparator switches the polarity, which causes the pulse generation module to output a pulse with constant width. This pulse causes the capacitor C_r to discharge to the rest potential. At the same time, the sample/hold module samples a regular timing signal to obtain the phase of the firing moment. When the pulse ends, the capacitor switches back to the reference current source, and IRON starts a new active period.

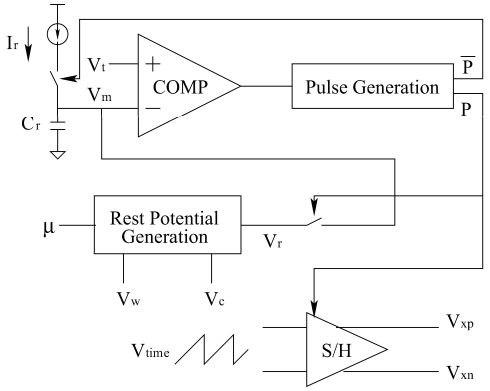

Fig. 5. The block diagram of IRON circuit

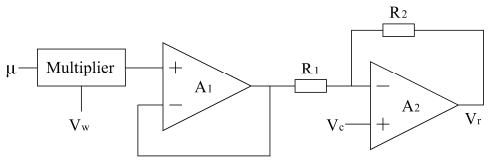

Fig. 6. Rest potential generation block diagram

A. Rest Potential Generation

In order to generate the waveforms in Eqn. 1 and Eqn. 2, a general formula can be used as in Eqn.3.

$$V_r(t) = \mu \times V_w(t) + V_c(t) \quad (3)$$

For the sine circle map, the waveforms $V_w(t)$ and $V_c(t)$ are given by Eqn. 4-5.

$$V_w(t) = V_a sin(2\pi\frac{t}{T}) \quad (4)$$

$$V_c(t) = V_b \quad (5)$$

While for the logistic map, the waveforms are given by Eqn. 6-7.

$$V_w(t) = -4V_a\frac{t}{T}(1-\frac{t}{T}) \quad (6)$$

$$V_c(t) = V_a\frac{t}{T} + V_b \quad (7)$$

Hence, the rest potential generation (RPG) circuit includes a multiplier and an adder. The block diagram of the module is shown in Fig. 6. The expression of the rest potential is shown in Eqn. 8.

$$V_r(t) = (1+\frac{R_2}{R_1})V_c(t) - \frac{R_2}{R_1}\mu \times V_w(t) \quad (8)$$

The bifurcation diagram of the IRON is sensitive to the waveform of the rest potential. The harmonic distortion of the analog multiplier deteriorates for large signal swings. Therefore, cascading stages are used to reduce the distortion level. Relatively small signals are used in the multiplier. Amplifier A_1 in Fig. 6 is a buffer stage to drive the next amplification stage, and A_2 amplifies the signal five times, with the addition of signal $V_c(t)$.

For our application, signals used in this module have a frequency of 1MHz. Therefore, ordinary two-stage OPAMP can be used, with unity-gain bandwidth at the order to tens

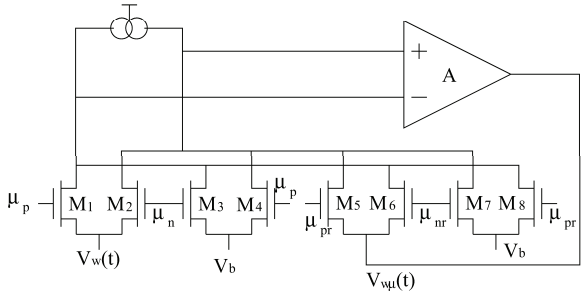

Fig. 7. The analog voltage multiplier

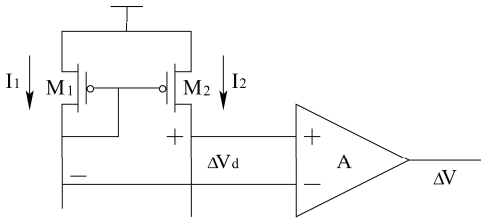

Fig. 8. The PMOS current mirror with offset

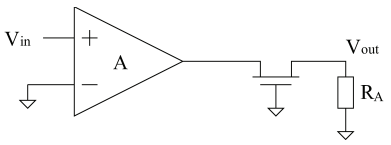

Fig. 9. The feedback loop in voltage multiplier

of MHz. The addition of two OPAMPs can introduce offsets into the rest potential. However, with the reference current calibration technique, the OPAMP offsets can be compensated.

B. Multiplier

The analog multiplier in the RPG circuit is shown in Fig. 7. It includes two cross-connected Gilbert cells, M1-M4 and M5-M8. Without considering the OPAMP offset, the OPAMP forces the currents in the two braches of the PMOS current mirror identical, which gives the current equation of Eqn. 9.

$$k_1(\mu_p - \mu_n)(V_w(t) - V_b) = k_5(\mu_{pr} - \mu_{nr})(V_{w\mu}(t) - V_b) \quad (9)$$

Where k_1 and k_5 are transistor related constants. If the two Gilbert cells match, the two constants would be the same, in both saturation region and in triode region. The output signal $V_{w\mu}(t)$ is then given in Eqn. 10.

$$V_{w\mu}(t) - V_b = \frac{\mu_p - \mu_n}{\mu_{pr} - \mu_{nr}}(V_w(t) - V_b) \quad (10)$$

Hence,

$$\mu = \frac{\mu_p - \mu_n}{\mu_{pr} - \mu_{nr}} \quad (11)$$

When μ_n is set to be μ_{nr}, μ_p can vary within μ_{pr} to achieve the required range $[0, 1]$ for μ.

The OPAMP will introduce offset into the multiplier, which generates current difference between the two current mirror branches. We assume a fixed output resistence for the PMOS transistors. Following the same method for the ideal multiplier, the output signal for OPAMP's fixed offset can be derived as shown in Eqn. 12. Only an offset is added at the bias voltage, which will be compensated during the reference current calibration. For the variable offset, as shown in Fig. 8, the voltage offset on the PMOS's is given in Eqn. 13. The output signal can be derived to be Eqn. 14. As a result, the value of μ would be changed from its ideal value. But, the signal is kept free of distortion.

$$V_{w\mu}(t) - V_b' = \frac{\mu_p - \mu_n}{\mu_{pr} - \mu_{nr}}(V_w(t) - V_b) \quad (12)$$

$$\Delta V_d = \frac{\Delta V}{A} \quad (13)$$

$$\Delta V_{w\mu}(t) = \mu' \Delta V_w(t) \quad (14)$$

However, when the output resistance of the PMOS varies with signal, Eqn. 12 and Eqn. 14 will not be valid. Instead, nonlinear distortion arises. Unfortunately, due to current variations in both PMOSs, the output resistance can change significantly in a nonlinear fashion. One could suggest to increase the OPAMP gain or to keep the PMOSs deep into the saturation region to alleviate the distortion. However, both methods would damage the stability of the multiplier. Under normal OPAMP gain and normal output resistance of the PMOSs, the nonlinear distortion increases dramatically with the signal swing range.

The voltage multiplier in Fig. 7 is susceptible to instability. The equivalent feedback loop is shown in Fig. 9. R_A is the impedance at the drains of the PMOS current mirror. This loop includes three amplification stages. Without extra care, the phase margin of the loop can fall short. To increase the phase margin, a small gain can be designed for the OPAMP, or the impedance at the common drains can be lowered. In our design, both methods are used to guarantee the loop stability.

C. Pulse Generation

The pulse generation module is shown in Fig. 10. Normally, the comp input (from the comparator) is low what causes the NOR gate to be high and the capacitor C_p to be discharged. When V_m reaches V_t (Fig. 5), the comparator goes high, making the NOR gate to go low. The capacitor C_p will then pull the iput of the inverter low causing the output to go high. The capacitor charges up causing the inverter output to go low again. This completes the generation of one pulse.

Because the pulse from the inverter controls also the charging process of the IRON, using this pulse can end the charging process of C_p prematurely. This would generate pulses of different widths, which introduces noise into the bifurcation diagram. Hence, in our circuit, several gates are cascaded

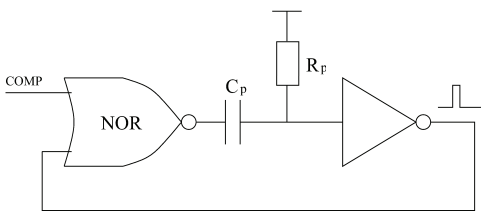

Fig. 10. The pulse generation module

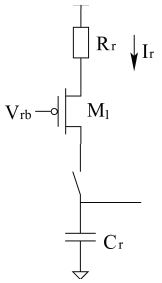

Fig. 11. The reference current calibration scheme

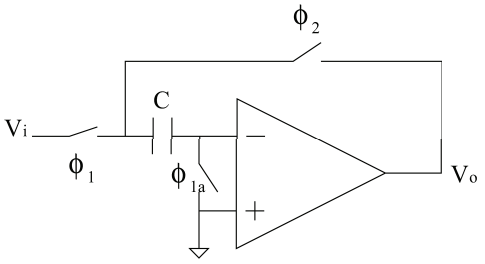

Fig. 12. Single-ended S/H deck

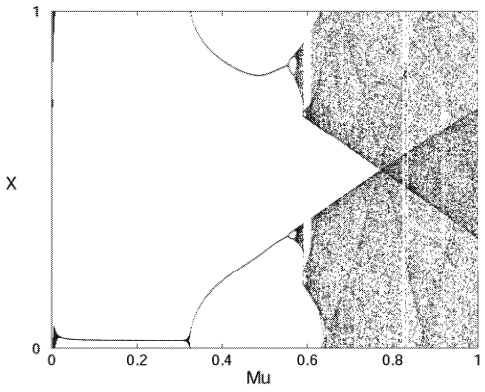

Fig. 13. Sine circle map with Hspice simulation, with typical model at 25C°

after the output of the inverter to introduce extra delay for the pulse. As a result, the width of the pulse is determined by the on-chip R_p and C_p , and is around 20ns. A relatively large resistance, at the order to $k\Omega$, is required for a small capacitor at hundreds fF. The resistor is laid out using the high-resistance layer provided by the process.

D. Reference Current Calibration

A major issue to achieve good performance of the IRON is to keep the synchronization between the membrane build-up process and the externally driven signals. Otherwise, the resulting bifurcation diagram would be different.

Without calibration, this synchronization is difficult to maintain. In order to keep a build-up natural frequency of 1MHz, the reference current I_r needs to be kept very close to its nominal value, so as to the capacitor C_r. On the other hand, both the offset of the comparator, and the offsets from the RPG module can variate the effective voltage difference between the threshold voltage and bias voltage, which can change the natural frequency.

The reference current calibration scheme is shown in Fig. 11. Before calibration, the IRON is put under natural firing mode by setting μ_p to be equal to μ_n. V_{rb} should be adjusted to keep the natural firing frequency of the IRON accurately to be 1MHz. In order to achieve good control of the small reference current I_r, R_r should be kept in the order of tens of $k\Omega$. High-resistance layer can be used for R_r.

E. Sample and Hold Module

A fully-differential bottom-plate sampling S/H deck is used. The single-ended version of it is shown in Fig. 12. Its input is a build-up timing signal. Once IRON initiates a pulse, it completes the sampling during the pulse. Hence, the settling requirement for the OPAMP can be much larger than the pulse width. In our circuit, we designed the deck to achieve settling within 50ns, with 12-bit resolution. Using a CAD tool GBOPCAD [5], the S/H deck has been designed, and consumes a biasing current of 2.4mA.

IV. Simulation Results

The IRON was fabricated in a 0.6μm CMOS process. The supply voltage is 5V. The threshold voltage V_t is set to be 1.5 V, and the bias voltage V_b is set to be 1V. The frequency of the driving signals are 1MHz. The chip is currently being tested. The results will be available at the time of conference.

Full chip level simulation has been carried out, with corner models under temperature variations. The bifurcation diagram of the sine circle map obtained from Hspice simulation with typical model and room temperature is shown in Fig. 13. The simulation shows the dynamics of the designed IRON circuit is similiar to that of a sine circle map in high-resolution.

V. Conclusion

In an effort to design a scalable single-chip cortical patch, a monolithic CMOS implementation of the IRON is designed and fabricated. The designed IRON is able to generate any arbitrary one-dimentional map. The IRON circuit is designed to be robust against different variations using a reference current calibration scheme.

The fabricated chip is under testing. The full-chip simulation results show that the designed IRON is able to generate the map of interest, sine-circle map, in high-resolution.

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