Penn Libraries
UNIVERSITY OF PENNSYLVANIA

University of Pennsylvania
ScholarlyCommons

Departmental Papers (ESE)   Department of Electrical & Systems Engineering

May 2002

A Low Distortion MOS Sampling Circuit

Sameer R. Sonkusale
University of Pennsylvania

Jan Van der Spiegel
University of Pennsylvania, jan@seas.upenn.edu

Follow this and additional works at: http://repository.upenn.edu/ese_papers

A Low Distortion MOS Sampling Circuit

Abstract

This paper presents a sampling technique with reduced distortion for use in a sample-and-hold circuit for high resolution analog-to-digital converters and switched capacitor filters. The technique involves bootstrapping both the gate and the bulk terminal of the sampling switch to improve linearity. Circuit implementation and SPICE level simulation results are presented.

A LOW DISTORTION MOS SAMPLING CIRCUIT

Sameer R Sonkusale, Jan Van der Spiegel

University of Pennsylvania
200, S.33rd Street, Philadelphia, PA 19104 USA

ABSTRACT

This paper presents a sampling technique with reduced distortion for use in a sample-and-hold circuit for high resolution analog-to-digital converters and switched capacitor filters. The technique involves bootstrapping both the gate and the bulk terminal of the sampling switch to improve linearity. Circuit implementation and SPICE level simulation results are presented.

1. INTRODUCTION

With increasing demands for high resolution analog-to-digital (A/D) converters, there is a greater need for a high performance sample-and-hold(S/H) circuits. In most cases, the dynamic performance of the front-end S/H circuit limits the overall dynamic performance of the systems such as A/D converters and switched-capacitor filters. Most S/H circuits use passive sampling technique for high speed applications. The performance of S/H circuits in CMOS technology is limited by the variation in the on-resistance of the MOS sampling switch with the input signal. The variation exists on account of dependence of the gate-source voltage and the threshold voltage on the input signal. Various techniques have been proposed to improve the linearity of the switch ([1], [2],[3],[4]). However, these techniques prove ineffective in completely eliminating the nonlinearity due to threshold voltage variation with the input (body effect) or they suffer from reliability issues. This paper proposes a reliable technique which does not have these problems.

2. BACKGROUND

The sampling front-end in CMOS technology for majority of switched capacitor implementations of the A/D converters and filters is shown in the Fig.1. The voltage across the capacitor tracks the input signal when the clock phase ϕ is high. The instantaneous value of the input signal is stored as a charge across the floating terminals of the capacitor when the switch M2 turns off. This charge is then processed by the following circuit to perform a desired function. Input dependence of the charge injection is minimized by turning off transistor M2 slightly before M1 (popularly known as
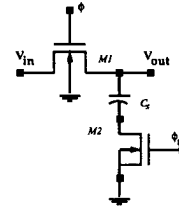

Fig. 1. Simple MOS sample and hold circuit

bottom plate sampling). For such a S/H circuit, the expression for the on-resistance of the MOS switch can be given by:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_t)} \tag{1}$$

Eq.(1) illustrates that the on-resistance R_{on} depends on the input signal through $V_{gs} = V_{dd} - V_{in}$ and through threshold voltage V_t as given in Eq.(2)

$$V_t = V_{t0} + \gamma[\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}] \tag{2}$$

Various methods have been devised to reduce the dependence of the on-resistance of a single MOS switch on the input signal. One such technique is to connect the gate to a voltage higher than V_{dd} during the on-phase ($V_{GS} > V_{dd}$)[5]. However such a technique suffers from a long term reliability problem due to high voltage switching across the gate oxide. This problem was solved in [1], where the gate voltage of the sampling switch is held at V_{dd} above the input signal during the on-phase. A conceptual representation of this technique is shown in Fig.2. The battery in the Fig.2 can be implemented using a switch capacitor configuration shown in Fig.3. The capacitor C_{boost} is charged to a value of the battery voltage $V_{battery} = V_{b2} - V_{b1} \le V_{dd}$ during the hold phase and connected between the gate and the source terminals of the sampling switch during the sampling phase, making the V_{gs} of the transistor a constant and independent of the input signal. The value of C_{boost} is chosen sufficiently large to minimize the effect due to charge sharing between C_{boost} and the parasitic gate capacitance of the sampling switch. Such an implementation still suffers from input dependent threshold voltage variation due to
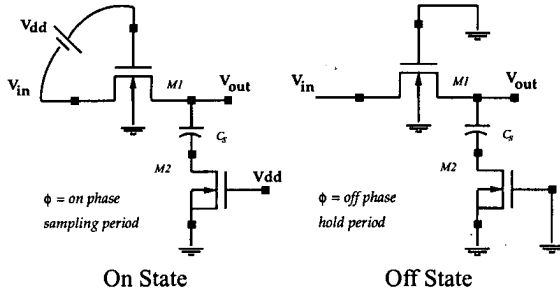
Fig. 2. Bootstrapped switch method by Abo[1]

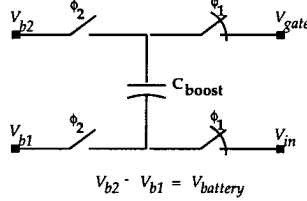
$$V_{b2} - V_{b1} = V_{battery}$$

Fig. 3. Switched capacitor battery voltage generator

body effect. This results in the variation of the on-resistance of the sampling switch resulting in distortion. Recently, a few techniques to eliminate the non-linearity due to body effect were proposed [2],[3]. The conceptual representation of these techniques during the on-phase is shown in Fig.4. The battery V_{bat} in this figure can be implemented using the switched capacitor technique shown in Fig.3. The basic idea in these techniques is to bootstrap the gate of the sampling switch such that the applied gate-source bias accounts for the threshold voltage variation with the input. The applied gate source bias is generated using a replica M2 of the sampling switch M1. The transistor M2 carries a fixed current I_b while the opamp is used in negative feedback to force the source of M2 to equal V_{in}. The battery at the output of the opamp is used to adjust the output common mode of the opamp, since the gate voltage of M2 can exceed the supply voltage. The gate of the transistor M2 and consequently that of M1 will have a value:

$$(V_{gate})_{M1} = V_{in} + V_{TM2}(V_{in}) + \sqrt{\frac{2I_b}{\mu_n C_{ox}(W/L)_{M2}}} \quad (3)$$

Therefore, from eq.(1), the value of the on-resistance for the sampling switch M1 will be as follows:

$$R_{on} = \frac{1}{\mu_n C_{ox}(W/L)[V_{TM2} - V_{TM1} + \sqrt{\frac{2I_b}{\mu_n C_{ox}(W/L)_{M2}}}]} \quad (4)$$

In many cases, the overdrive provided by M2 is not sufficient to guarantee a low on-resistance for M1 in which case,

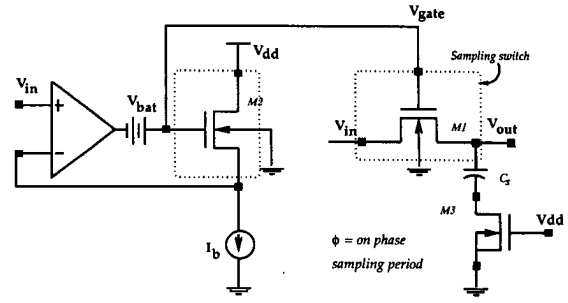the gate voltage of M2 is further boosted [3]. R_{on} will be in-

Fig. 4. Sampling network proposed by Pan et.al[2] during on phase

put independent if $V_{TM2} = V_{TM1}$ which is assumed to be the case since M1 and M2 are replica transistors and both have the same gate-source and bulk-source voltages. However that is not the case since the transistor M2 operates in saturation while the actual sampling switch M1 is operating in the non-saturation region resulting in mismatch between M1 and M2's threshold voltages. Also, in short channel technologies, due to drain induced barrier lowering, $V_{TM2} \neq V_{TM1}$, since $V_{dsM2} \neq V_{dsM1}$. Another main limitation of this technique is the use of an opamp which consumes a lot of power to ensure high accuracy and fast settling. Distortion can result due to variation in opamp gain and incomplete settling. This paper demonstrates a passive technique which does not suffer from the above drawbacks.

3. OVERVIEW OF THE PROPOSED TECHNIQUE

The method proposed in Fig.2 [1] provides an excellent technique for cancelling the nonlinearity due to gate-source voltage variation with the input. However the bulk-source voltage variation with the input signal (body effect) still limits the linearity of the switch. To remove the nonlinearity introduced by the body effect, one may think of a solution to tie the bulk to the source [4]. However, the switch is bidirectional and symmetric, since the source and drain terminals interchange their roles depending on *the value of input signal and the value of the voltage sampled on the capacitor during the previous sampling instant.* Since the source terminal is not precisely defined, it is inappropriate to make a fixed bulk-source connection as it may cause latchup during sampling. The conceptual representation of the proposed technique is shown in Fig.5 for a PMOS sampling switch. The main idea behind the technique is to bootstrap both the gate and the bulk terminal such that the gate-source voltage and the bulk-source voltage is constant during the sampling phase within the reliability constraints. In the proposed technique, the threshold voltage of the sampling

switch remains constant, eliminating the nonlinearity introduced due to the bulk-source voltage variation with the input signal. However this technique will not be feasible in an nwell CMOS process with an NMOS sampling switch, since it's bulk terminal would be required to be connected to the most negative potential on the chip. For the proposed
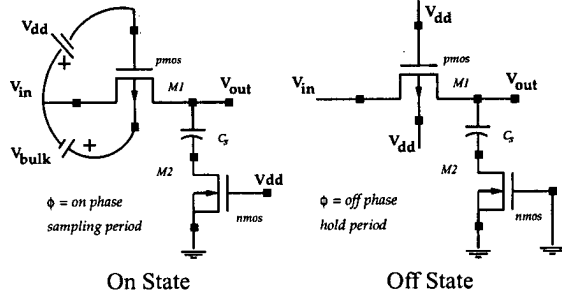

On State   Off State

Fig. 5. Conceptual Proposed Sampling Technique for PMOS Sampling Switch

technique, V_{gs} is equal to V_{dd} and V_T is given by Eq.(5), which is constant and independent of the input voltage.

$$V_T = V_{T0} + \gamma[\sqrt{2|\phi_F| + V_{bulk}} - \sqrt{2|\phi_F|}] \qquad (5)$$

Therefore, from Eq.(1), the on resistance of the sampling switch is constant over the input range. This guarantees distortion-free performance of the sampling network. In Fig.5, the value of the voltage for the battery V_{bulk} is chosen such that the bulk potential is always greater than the source and the drain potential to avoid latch-up. In other words, $V_{bulk} > V_{max} = max(V_{in})$. For the technique proposed in [4], the bulk is tied to the source ($V_{bulk} = 0$) during the on phase, making it susceptible to latchup.

4. CIRCUIT IMPLEMENTATION

The circuit implementation of the proposed scheme is shown in Fig.6. Since an nwell process is used, a PMOS transistor acts as the input sampling switch to implement the proposed sampling scheme. The sampling occurs when the clock phase ϕ_1 is high. Clock signals are shown in Fig.7. When the clock phase ϕ_1 is low(off phase) , transistor M3 is *on*, connecting the gate of the sampling switch to V_{dd} and consequently turning off the sampling switch M1. The capacitor now holds the sampled value of the input signal. As explained in section 2, transistor M2 is turned off prior to the sampling switch M1 to avoid input dependent charge injection at turn off. During the off phase, source of M4 and the gate of M8 are bootstrapped to $2V_{dd}$, turning on M4 and M8. The capacitor C_{gate} charges to $-V_{dd}$. The bulk is connected to V_{dd} and the capacitor C_{bulk} charges to $V_{dd} - V_{bias}$. When
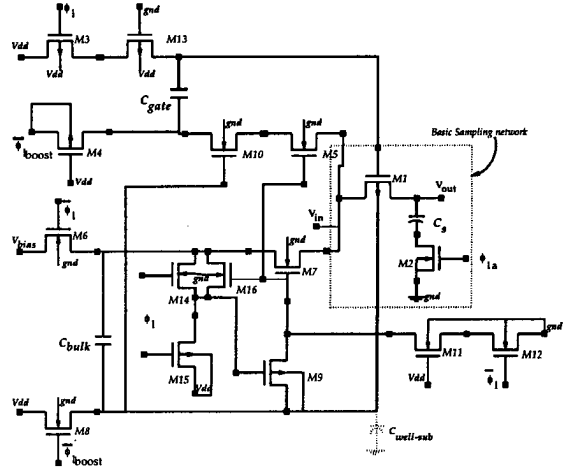

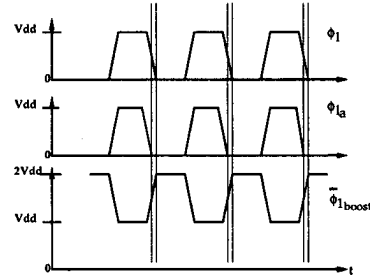**Fig. 6.** Circuit Implementation of the proposed scheme

Fig. 7. Waveform signals used in the proposed scheme

the clock phase ϕ_1 goes high again, the gate of the transistor M9 is pulled low by M14 turning it on [1]. Consequently, the voltage seen at the gate of M5 and M7 changes from 0 to $V_{in} + V_{dd} - V_{bias}$ during the sampling phase, which turns on M5 and M7. At the same time the gate of M10 changes from V_{dd} to $V_{in} + V_{dd} - V_{bias}$. During this phase, the capacitor C_{gate} is connected between the input and the gate terminal of the sampling switch M1. The gate voltage for M1 is now at $V_{in} - V_{dd}$. Similarly the capacitor C_{bulk} is connected between the input and the bulk terminal. The bulk voltage for M1 is now equal to $V_{in} + V_{dd} - V_{bias}$. Thus a constant V_{gs} overdrive and a constant V_{bs} overdrive is provided to the sampling switch M1 ensuring little or no variation in the on-resistance with the input signal. This value of on-resistance is given by the Eq.(6).

$$R_{on} = \frac{1}{\mu_p C_{ox}(W/L)(V_{dd} - V_{tcons})} \qquad (6)$$

where, V_{tcons} is a constant and given by:

$$V_{tcons} = V_{t0} + \gamma[\sqrt{2|\phi_F| + V_{dd} - V_{bias}} - \sqrt{2\phi_F}] \qquad (7)$$

Transistors M11 and M12 are used to turn off the gate voltage for M5 and M7 during the off phase. Also note that the transistor M10 and M13 are always conducting to ensure reliability of the circuit, as discussed in the next section. The implementation is passive in nature and does not consume any static power.

5. IMPLEMENTATION AND RELIABILITY ISSUES

The reliability constraints requires that the absolute value of relative terminal voltages be less than V_{dd}. This puts restrictions on the nature of the switches used and the values of their terminal voltages. Some of them are discussed below. Since a PMOS sampling switch M1 is used, the gate voltage for M1 will be negative during the on phase. That refrains us from using any switch between C_{gate} and the gate of the sampling switch M1 because that switch would be required to conduct a negative potential to the gate of the PMOS sampling transistor which is not a possibility. Transistor M3 has been used to perform the job of turning off the sampling switch M1 when ϕ_1 goes low by connecting the gate to V_{dd}. To charge the capacitor C_{gate} to V_{dd}, any transistor at M4 would be required to conduct the voltage of value $2V_{dd}$. This is achieved by the use of a PMOS transistor at M4 with $\overline{\phi}_{1boost}$ as the source voltage and V_{dd} as its gate voltage. The $\overline{\phi}_{1boost}$ can be generated using the clock booster as in [1]. In the absence of M10, the gate-source voltage of M5 would be $2V_{dd}$. M10 reduces the gate-source voltage experienced by M5. A long channel device at M10 prevents M5 (and itself) from punch-through at the start of the on phase. Similarly, M11 helps to reduce the drain-source voltage for M12 during turn-off to avoid punch through and to maintain the gate-source voltage of M12 less than V_{dd} during the on phase. M13 provides similar purpose for M3. The role of M16 is to ensure that the V_{gs} for M7 does not exceed V_{dd} [1].

To avoid the effect of charge sharing between C_{bulk} and the well capacitance, V_{bias} is reduced while C_{bulk} is kept at a resonable minimum value (7-8 times the well capacitance). This does introduce a small input-dependent variation in the bulk voltage, however it does not contribute significant levels of distortion.

6. CIRCUIT LEVEL SIMULATION RESULTS USING SPICE

To test the efficacy of the proposed technique, the circuit of Fig.6 was designed in a TSMC 0.35μ process. A differential configuration was implemented (the circuit shows the single ended implementation for simplicity). An input sinusoid signal of 7.5MHz is applied to be sampled at a frequency of 100MHz. Fig.8(a) shows the FFT of the sampled voltage across the capacitor when the bulk is tied to
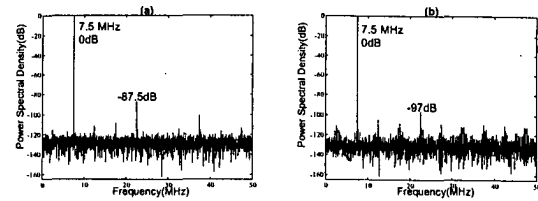

Fig. 8. Power Spectral Density output with (a) constant bulk potential[1] and (b) proposed technique,$F_s = 100MHz, F_{in} = 7.5MHz$

a constant potential V_{dd}[1]. Fig.8(b) shows the FFT of the sampled voltage across the capacitor for the proposed technique. The plots indicate a 97dB SFDR, a 9.5dB increase over the commonly used technique as shown in Fig.8(a)[1] with just the gate bootstrap.

7. CONCLUSION

A novel passive sampling circuit is presented for high linearity sample and hold by bootstrapping the bulk terminal in addition to the gate of the sampling switch. The circuit is designed for reliablity and does not exhibit latch-up. Simulation results in TSMC 0.35μm show better suppression of higher order harmonics compared to prior art.

8. REFERENCES

[1] Andrew M. Abo and Paul R. Gray, "A 1.5v, 10-bit, 14.3-ms/s cmos pipeline analog-to-digital converter," IEEE JSSC, vol. 34, no. 5, pp. 599–605, May 1999.

[2] Hui Pan et.al, "A 3.3-v 12-b 50-ms/s a/d converter in 0.6-μm cmos with over 80-db sfdr," IEEE JSSC, vol. 35, no. 12, pp. 1769–1780, December 2000.

[3] A.K. Ong et.al, "A method for reducing the variation in "on" resistance of a mos sampling switch," Proc. IEEE ISCAS, vol. 5, pp. 437–440, 2000.

[4] Jesper Steensgard, "Bootstrapped low-voltage analog switches," Proc. IEEE ISCAS, vol. 2, pp. 29–32, 1999.

[5] T. Cho and P.R Gray, "A 10b 20ms/s, 35mw pipeline a/d converter," IEEE JSSC, vol. 30, no. 3, pp. 166–172, March 1995.