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Low Fixed Pattern Noise Current-mode Imager Using Velocity Saturated Readout Transistors

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Abstract
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Keywords
Current-mode CMOS Imager, Velocity saturation, fixed-pattern noise, active pixel sensor

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***Abstract*— This paper described a novel current-mode active pixel sensor (APS) imager. Conversion of photodiode voltage to output current is done using transistors operating in velocity saturation region. The high output impedance of this region makes it more suitable for current-sourcing operation than the linear region. The transistors also exhibit high linearity, allowing us to suppress fixed pattern noise (FPN) by correcting for both offset and gain variations among pixels. Experimental results on the fabricated 110×200 pixel array are presented. With conventional correlated double sampling (CDS), FPN is reduced from 3.8% to 0.85%. Further reduction requires compensation of gain variations, and results in a final FPN of 0.19%. A triple sampling approach is introduced to implement the described correction in hardware.**

I. Introduction

CMOS image sensors have received much attention over the last decade. Since the introduction of active pixel sensors (APS), there has been continuous research effort to improve its performance, targeting low noise, low power consumption, high speed readout and high dynamic range. CMOS imagers have already become a strong contender to CCD's as the imaging front-end. In addition, a big advantage with CMOS imagers is their ability of system integration. Many functionalities that come after the front-end of an imaging system, which require external circuit support for CCD's, can be integrated together within a CMOS sensor. For example, digital control electronics, analog-to-digital converters, and noise suppression circuitry can be added to form a complete camera on a chip [1]. Image processing functions are also implemented on CMOS image sensors for applications such as image enhancement or motion detection [2]. Compared with the computational cost to implement these functions in a digital processor, the analog approach is more power-efficient, and is quicker to obtain results.

It is noticeable that many of the computational processing are done in the current domain. Indeed, arithmetic operations such as addition or scaling on current values can be effortlessly implemented. Their voltage domain counterparts exist (through switched capacitor circuits), but tend to be more complex. Nevertheless, the biggest problem with a current-mode imaging system lies in the front-end. Historically, current-mode imagers suffer from high level of fixed pattern noise (FPN) compared to source-follower based voltage-mode APS [1]. For this reason, designers sometimes resorted to use voltage-to-current converters to connect voltage-mode pixels to current-mode processing units [3]. Recently reported linear current-mode pixel lowered FPN through correlated double sampling (CDS) [4]; however its effectiveness is limited due to inherent linearity problems, namely mobility degradation and relatively low output impedance [5].

In this paper we describe the performance of our recently proposed current-mode pixel [5]. The readout transistor exhibits high linearity and large output impedance by operating in the velocity saturation region. We show the experimental results that low FPN is achieved after applying CDS and gain correction techniques.

II. Operation under Velocity Saturation

Velocity saturation is a short-channel effect. It occurs when the electric field along the channel (lateral E-field) increases beyond a critical value E_C, so that the carrier velocity v approached a saturated value v_{sat}. The critical value E_C is about 1.5×10^4 V/cm for p-type silicon [6]. Further increase in the lateral E-field will only decrease the mobility, but won't increase the velocity. As the saturation current is limited, it is generally undesirable to enter velocity saturation.

Assuming source is grounded, the drain current I_D at the onset of velocity saturation can be modeled as [7]:

$$I_D = \frac{v_{sat}C_{ox}W[2(V_G - V_T) - V_{DSAT}]V_{DSAT}}{E_C L + V_{DSAT}} \quad (1)$$

where V_{DSAT} is the drain-to-source voltage at which the carriers at the drain become velocity saturated, or when the lateral E-field at the drain end of the channel becomes equal to E_C. It is expressed as

$$V_{DSAT} = \frac{E_C L(V_G - V_T)}{E_C L + (V_G - V_T)} \quad (2)$$

We can observe two results. First, when the gate overdrive $V_G - V_T$ is small, i.e. $E_C L \gg V_G - V_T$, (2) becomes $V_G - V_T$. Then the drain current is

$$I_D = \frac{v_{sat}C_{ox}W(V_G - V_T)^2}{E_C L} = \frac{\mu_{eff}C_{ox}}{2}\frac{W}{L}(V_G - V_T)^2 \quad (3)$$

which still follows the square-law.

On the other hand, as we increase the gate voltage such that $V_G - V_T \gg E_C L$, (2) becomes $E_C L$. (1) is reduced to

$$I_D = v_{sat}C_{ox}W(V_G - V_T - E_C L/2) \quad (4)$$

which has linear dependency on V_G. Also in the case of a very short channel,

$$\lim_{E_C L \to 0} I_D = v_{sat}C_{ox}W(V_G - V_T) \quad (5)$$

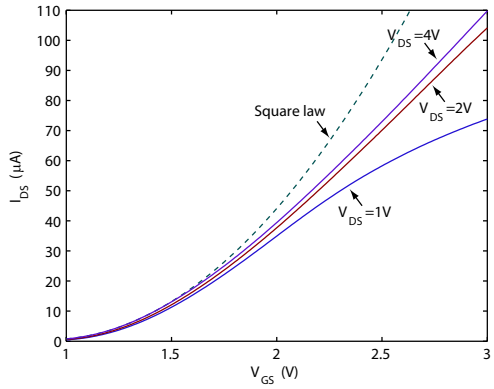


Fig. 1. Drain current measurement of a velocity saturated readout transistor with W=0.9μm, L=0.6μm, and V_{DS} fixed at 1V, 2V and 4V.

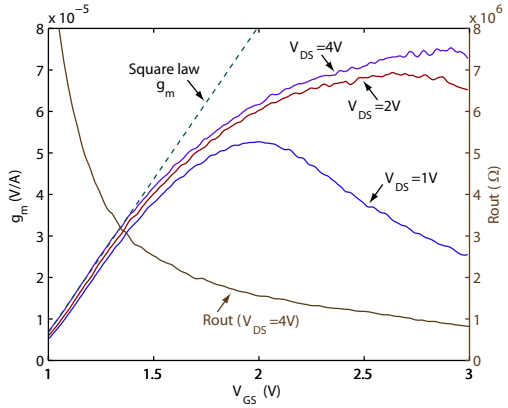


Fig. 2. Measured transconductance (g_m, left axis) and output impedance (R_{out}, right axis) of the transistor in Fig. 1 as a transconductance amplifier.

It is worth noting that the above results are independent of the drain voltage; i.e. if the device operates as a transconductance amplifier, it would have infinite output impedance. In reality the drain voltage affects the length of the velocity saturated region, analogous to channel length modulation. However the effect is small for a minimal-length transistor as most of the channel is velocity saturated [8]. Therefore a large but finite output impedance is expected.

The velocity saturated operation is verified in experiments. Fig. 1 shows the drain current of a $0.9/0.6$ μm transistor with fixed V_{DS}. As the gate voltage increases beyond threshold, square-law behavior is first observed, in agreement with (3). This can also be seen from the g_m plot in Fig. 2, where the curves all start with a constant slope. At larger V_{GS} the linear I-V relationship of velocity saturation (4) emerges. The g_m curves descend and reach a flat top where the highest linearity is achieved. When V_{GS} increases further the transistor enters linear region, and g_m drops down due to mobility degradation.

Compared with a long-channel transistor (Fig. 3), it is evident that the g_m curves in Fig. 2 deviates sooner from the square-law dictated straight line. This is the indication of velocity saturation as V_{DSAT} is reduced from $V_G - V_T$. It creates a plateau where the gain is relatively constant.

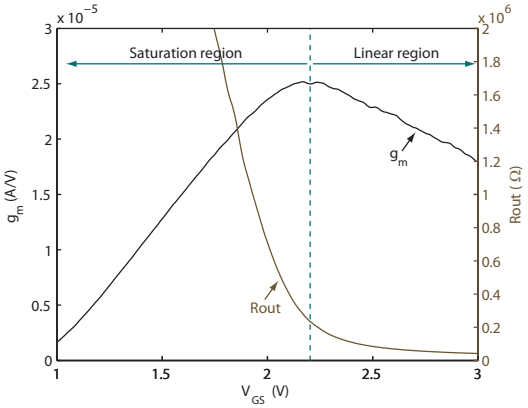


Fig. 3. g_m and R_{out} of a long-channel readout transistor. W=0.9μm, L=1.8μm, V_{DS}=1V.

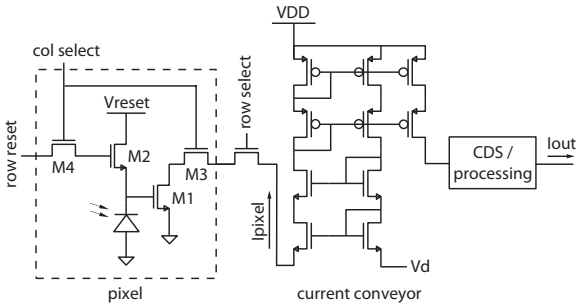


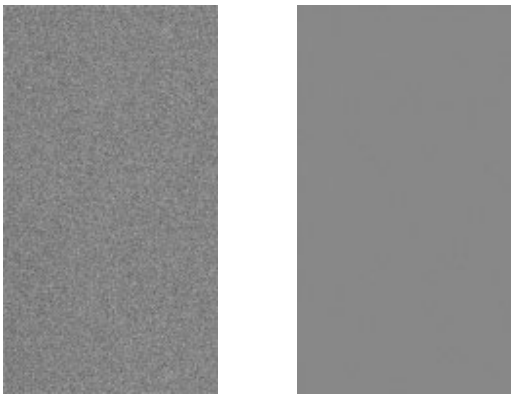
Fig. 4. Schematic of the imager, showing one pixel and the chip-level readout circuit.

Also, the output impedance is around $1\times10^6\Omega$ which is much higher than the long-channel transistor in linear region (about $5\times10^4\Omega$). The high output impedance makes the transistor a suitable current source that is insensitive to bias voltage variation, which is a source of nonlinearity in [4].

III. Pixel and Readout Architecture

Fig. 4 shows the schematic of the current-mode pixel and its readout circuit. The pixel is similar to the classical 3-transistor APS design [1], with an additional reset switch $M4$ to allow individual pixel reset. $M1$ is the readout transistor working under velocity saturation. A current conveyor is used to pin the voltage on the output line, and provide the drain voltage bias for $M1$. It also mirrors a copy of the pixel current for the FPN correction circuit; which could be a CDS unit, or other analog processing functions. On the fabricated chip, only a difference double sampling function was implemented [5]. The FPN reductions in the next section were obtained by processing in the digital domain.

The velocity saturated operation can also benefit column-parallel architecture to achieve fast readout. Offset mismatch created by column-level current conveyors can be better tolerated owing to the pixels' high output impedance. The current conveyors may also have mismatched gains; however these can be corrected together with the gain variation in pixels. We show in the next section that the correction can



(a) (b)

Fig. 5. FPN reduction by image subtraction. (a) Raw image, taken when a constant voltage is applied at the gate of every readout transistor. FPN=3.71%.(b) Corrected image, after subtracting an image taken at the reset level. FPN=0.29%.

be quite effective if readout is linear, as is the case in velocity saturation.

IV. Experimental Results

Our imager was fabricated in a standard 0.5μm CMOS process. It contains a 110×200 array of pixels designated for velocity saturated operation. The pixels have a pitch of 12μm and a fill factor of 31.25%. The readout transistors are minimum-sized, with W=0.9μm and L=0.6μm.

Due to the limited voltage range of the current conveyor, the readout transistors are biased at V_D=1.2V (i.e. a less degree of velocity saturation). V_{reset} in Fig. 4 is 2.2V. Saturation level is assumed to be 0.5V below the reset level. This is less than the full capacity of the photodiode; it was chosen to ensure that g_m stays relatively constant. The total temporal noise amplitude in the imager is 0.47% normalized to the signal range. This translates to a dynamic range of 46.6dB. In subsequent FPN measurements, temporal noise was removed by averaging multiple frames.

Without any FPN reduction, the imager has a high FPN of 3.8%. To locate the source of the FPN, we close the reset switches and apply a constant voltage directly to the gate of the readout transistors. This yields a FPN of 3.71% (Fig. 5(a)). Therefore we conclude that the high FPN is mainly caused by variation among readout transistors, but not photodiodes.

In (4), if we assume that the gain term ($v_{sat}C_{ox}W$) is the same for all pixels, then any mismatch in the offset term ($V_T + E_C L/2$) can be canceled out using CDS, or by subtracting an image taken at the reset level (which contains the same noise). Applying this to the image in Fig. 5(a), we get a much cleaner image with 0.29% FPN. However, we noticed that even after CDS, FPN tends to increase for higher light intensity. With uniform illumination at a range of intensities, we obtain the plot in Fig. 7. The worst case FPN with CDS is 0.85%. It suggests that there must be a gain mismatch among pixels.

The gain and offset values of each readout transistor can be obtained by fitting a straight line through its measured

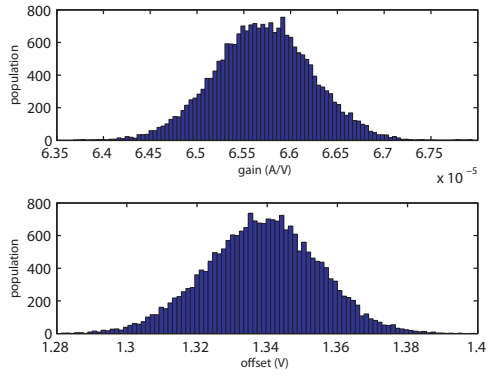


Fig. 6. Gain and offset distribution of readout transistors in the fabricated imager.

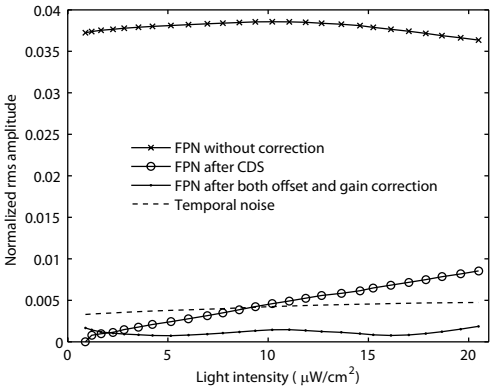


Fig. 7. FPN measurements of the imager under uniform illumination.

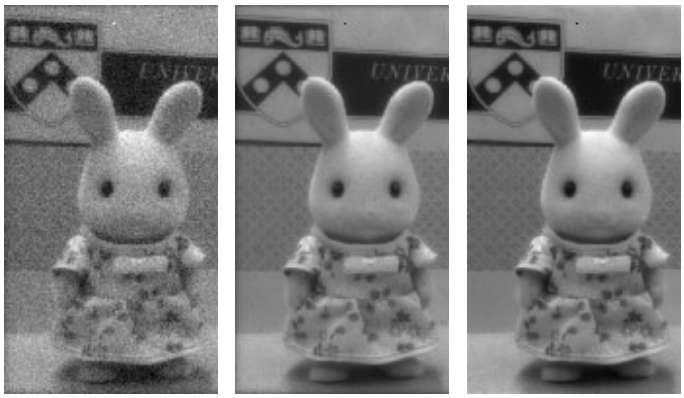
transfer function. The result is shown in Fig. 6 for all pixels. We noticed a spread in both terms. The standard deviation of gain is 5.19×10^{-7}A/V, over the input range of 0.35V this is a variation of 0.18μA, which is 0.6% of the full output range. This agrees with the FPN result after CDS is applied.

With each transfer function characterized, we can map the output current back to input voltage. The FPN of the reconstructed image from Fig. 5(a) is lowered to 0.10% (not shown). Similar steps can also be applied to include gain mismatch of photodiodes, by measuring and inversing the transfer function from light intensity to output current. This yields a worst case FPN of 0.19% (Fig. 7).

Fig. 8 shows a sample picture taken with the imager before and after FPN corrections. With digital CDS, most of the FPN is suppressed. However, pixels near the borders appear darker, where the photodiodes have a lower quantum efficiency. With gain correction, the edge effect is eliminated.

One might notice that Fig. 8(c) has slightly better contrast than Fig. 8(a). This is a side effect of processing in the digital domain. Because the raw data contain high FPN, the range of analog-to-digital conversion has to be extended to accommodate the large variation. Therefore the picture appears underexposed. With gain correction, the original dynamic range at the input is restored.

The imager is summarized in Table I.



(a) (b) (c)

Fig. 8. Sample pictures taken with the imager. (a) Raw image. (b) After CDS. (c) After both offset and gain correction.

TABLE I

IMAGER CHARACTERISTICS

Technology	0.5μm 3M2P CMOS
Array size	110×200
Pixel size	12μm×12μm
Frame rate	30fps
Dynamic range	46.6dB
Dark current	1.18fA
Worst-case FPN (uncorrected)	3.8%
Worst-case FPN (CDS)	0.85%
Worst-case FPN (offset & gain correction)	0.19%

V. IMPLEMENTATION OF GAIN CORRECTION

In the previous section, gain values were calculated using a linear fit. Ignoring higher order effects in the transfer function, we can also obtain the gain by taking the output difference ΔI at two known input levels with ΔV apart. The gain is simply $\Delta I/\Delta V$, where ΔV is a constant. After sampling the signal level and offset correction, we can then remove the gain by dividing the CDS output with ΔI. We call this a *triple sampling* approach.

Specifically, 3 samples are taken for each pixel at the reset level V_{Grst}, the saturation level V_{Gsat} and the integrated signal level V_{Gph}. The sampled currents are:

$$I_{Drst} = v_{sat}C_{ox}W(V_{Grst} - V_T - E_CL/2) \quad (6)$$

$$I_{Dsat} = v_{sat}C_{ox}W(V_{Gsat} - V_T - E_CL/2) \quad (7)$$

$$I_{Dph} = v_{sat}C_{ox}W(V_{Gph} - V_T - E_CL/2) \quad (8)$$

First, CDS is applied to cancel the offset:

$$I_{CDS} = I_{Dph} - I_{Drst} = v_{sat}C_{ox}W(V_{Gph} - V_{Grst}) \quad (9)$$

Then, gain is compensated for by dividing the CDS output with $(I_{Dsat} - I_{Drst})$:

$$\frac{I_{CDS}}{I_{Dsat} - I_{Drst}} = \frac{V_{Gph} - V_{Grst}}{V_{Gsat} - V_{Grst}} \quad (10)$$

In the last expression, we have obtained a ratio that is proportional to V_{Gph} with constant gain and offset.

The circuits needed to implement gain correction include a current memory (or CDS) and a divider. Different designs for current-mode division are available, that present result in either current [9] or voltage [10].

VI. CONCLUSIONS

We demonstrated the performance of an imager with velocity saturated current readout. The high linearity in the transfer function allowed us to achieve very low FPN, using offset and gain correction techniques. The reduced FPN is close to or better than some voltage mode APS [11], [12]. We showed an approach to implement the correction in hardware.

With the scaling of CMOS technology, velocity saturation becomes a more prevailing effect. Pixels designed to operate in this region can take advantage of the reduced device size, thus having lower bias voltage and power consumption. Such pixels make a good front-end in imaging systems, that seamlessly connect to current-mode processing elements without sacrificing image quality.

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